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PATENT
Docket No. PM07027D1CIP1C6 (3430.2.388US6CIP1)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Igor Polishchuk et al.	
Serial No.:	Not assigned	
Filed:	Concurrently herewith	Group Art Unit: Not assigned
Title:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	
Examiner:	Not assigned	

PRELIMINARY AMENDMENT

TO THE COMMISSIONER FOR PATENTS:

Before examination, please amend the above-identified patent application as follows.

Amendments to the Specification begin on page 2.

Remarks begin on page 3 of this paper.

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AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0001] of the specification with the following:

[0001] This application is a continuation of U.S. Patent Application Number 16/429,464, filed June 3, 2019, which is a continuation of U.S. Patent Application Number 15/864,832, filed January 8, 2018, now U.S. Patent Number 10,312,336, issued June 4, 2019, which is a continuation of U.S. Patent Application Number 15/335,180, filed on October 26, 2016, now U.S. Patent Number 9,929,240, issued March 27, 2018, which is a continuation of U.S. Patent Application Number 14/811,346, filed July 28, 2015, now Patent Number 9,502,543, issued on November 22, 2016, which is a continuation of U.S. Patent Application Number 14/159,315, filed on January 20, 2014, now Patent Number 9,093,318, issued on July 28, 2015, which is a continuation of U.S. Patent Application number 13/539,466, filed on July 1, 2012, now Patent Number 8,633,537, issued on January 21, 2014, which is a continuation-in-part of Patent Application Number 13/288,919, filed November 3, 2011, now Patent Number 8,859,374, issued on October 14, 2014, which is a divisional of U.S. Patent Number 12/152,518, filed May 13, 2008, now U.S. Patent Number 8,063,434, issued November 22, 2011, which claims the benefit of priority to U.S. Provisional Patent Application Number 60/940,160, filed May 25, 2007, all of which ~~application~~ are hereby incorporated by reference in their entirety.

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REMARKS

The Applicant respectfully submits that the Application is in condition for allowance. If the Examiner notes any further matters that may be resolved by a telephone interview or Examiner's amendment, the Examiner is encouraged to contact the Applicant using the contact information listed below.

Respectfully submitted,

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Electronic Acknowledgement Receipt

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Application Number:	17157350
International Application Number:	
Confirmation Number:	6135
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
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Filer:	Michael Lee Bartholomew
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Specification	3430-2-388US6CIP1_Specification.pdf	1612879 560909d9619c5043c6cbbd23b457ca12449f4b8b	no	39

Warnings:

Information:					
2	Claims	3430-2-388US6CIP1_Claims.pdf	37797 9bdcadd0432d1f1b1099b309e92070c68bac3ca7	no	1
Warnings:					
Information:					
3	Abstract	3430-2-388US6CIP1_Abstract.pdf	17073 997ae7db9b9868aa0f79f177e92c3fbb1791e5e4	no	1
Warnings:					
Information:					
4	Drawings-only black and white line drawings	Drawings.pdf	570446 1bbb712de9d01c6552917709290784 8f8dfeaa9c	no	13
Warnings:					
Information:					
5	Oath or Declaration filed	PM07027D1CIP1C6_Declaration.pdf	586217 6f1a4ab9c4a4c226cd84771add845b73face7dc1	no	3
Warnings:					
Information:					
6	Power of Attorney	POA.pdf	2279316 e95ea7113efa260c8c8bcb851acd1c1aa54a7828	no	2
Warnings:					
Information:					
7	Application Data Sheet	PM07027D1CIP1C6_ADS.pdf	1360781 c742dfaa56de33ba07d8324848fa1fc5db7ce184	no	9
Warnings:					
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8		PreliminaryAmendment.pdf	71953 b7bee030e56975d7d5ae1dc62955f823433 91143	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	

	Preliminary Amendment	1	1
	Specification	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application Number 15/335,180, filed on October 26, 2016, which is a continuation of U.S. Patent Application Number 14/811,346, filed July 28, 2015, now Patent Number 9,502,543, issued on November 22, 2016, which is a continuation of U.S. Patent Application Number 14/159,315, filed on January 20, 2014, now Patent Number 9,093,318, issued on July 28, 2015, which is a continuation of U.S. Patent Application number 13/539,466, filed on July 1, 2012, now Patent Number 8,633,537, issued on January 21, 2014, which is a continuation-in-part of Patent Application Number 13/288,919, filed November 3, 2011, now Patent Number 8,859,374, issued on October 14, 2014, which is a divisional of U.S. Patent Number 12/152,518, filed May 13,2008, now U.S. Patent Number 8,063,434, issued November 22, 2011, which claims the benefit of priority to U.S. Provisional Patent Application Number 60/940,160, filed May 25, 2007, all of which application are hereby incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] The present invention relates generally to semiconductor devices, and more particularly to integrated circuits including non-volatile semiconductor memories and methods of fabricating the same.

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BACKGROUND

[0003] Non-volatile semiconductor memories are devices that can be electrically erased and reprogrammed. One type of non-volatile memory that is widely used for general storage and transfer of data in and between computers and other electronic devices is flash memory, such as a split gate flash memory. A split gate flash memory transistor has an architecture similar to that of a conventional logic transistor, such as Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), in that it also includes a control gate formed over a channel connecting a source and drain in a substrate. However, the memory transistor further includes a memory or charge trapping layer between the control gate and the channel and insulated from both by insulating or dielectric layers. A programming voltage applied to the control gate traps a charge on the charge trapping layer, partially canceling or screening an electric field from the control gate, thereby changing a threshold voltage (V_T) of the transistor and programming the memory cell. During read-out, this shift in V_T is sensed by the presence or absence of current flow through the channel with application of a predetermined read-out voltage. To erase the memory transistor, an erase voltage is applied to the control gate to restore, or reverse the shift in V_T.

[0004] An important measure of merit for flash memories is data retention time, which is the time for which the memory transistor can hold charge or remain programmed without the application of power. The charge stored or trapped in the charge trapping layer decreases over time due to leakage current through the insulating layers, thereby reducing the difference between a programmed threshold voltage (VTP) and an erased threshold voltage (VTE) limiting data retention of the memory transistor.

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[0005] One problem with conventional memory transistors and methods of forming the same is that the charge trapping layer typically has poor or decreasing data retention over time, limiting the useful transistor lifetime. Referring to FIG. 1A, if the charge trapping layer is silicon (Si) rich there is a large, initial window or difference between VTP, represented by graph or line 102, and the VTE, represented by line 104, but the window collapse very rapidly in retention mode to an end of life (EOL 106) of less than about 1.E+07 seconds.

[0006] Referring to FIG. 1B, if on the other hand the charge trapping layer is if a high quality nitride layer, that is one having a low stoichiometric concentration of Si, the rate of collapse of the window or Vt slope in retention mode is reduced, but the initial program-erase window is also reduced. Moreover, the slope of Vt in retention mode is still appreciably steep and the leakage path is not sufficiently minimized to significantly improve data retention, thus EOL 106 is only moderately improved.

[0007] Another problem is that increasingly semiconductor memories combine logic transistors, such as MOSFET's, with memory transistors in integrated circuits (ICs) fabricated on a common substrate for embedded memory or System-On-Chip (SOC) applications. Many of the current processes for forming performance of memory transistors are incompatible with those used for fabricating logic transistors.

[0008] Accordingly, there is a need for memory transistors and methods of forming the same that provides improved data retention and increased transistor lifetime. It is further desirable that the methods of forming the memory device are compatible with those for forming logic elements in the same IC formed on a common substrate.

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SUMMARY OF THE INVENTION

[0009] The present invention provides a solution to these and other problems, and offers further advantages over conventional memory cells or devices and methods of fabricating the same.

[0010] Generally, the device includes a memory transistor comprising a polysilicon channel region electrically connecting a source region and a drain region formed in a substrate, an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, and a high work function gate electrode formed over a surface of the ONNO stack. In one embodiment, the ONNO stack includes a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer. In another embodiment, the multi-layer charge-trapping region further includes an oxide anti-tunneling layer separating the first nitride layer from the second nitride layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] These and various other features and advantages of the present invention will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

[0012] FIG. 1A is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a large initial difference between programming and erase voltages but which loses charge quickly;

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[0013] FIG. 1B is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a smaller initial difference between programming and erase voltages;

[0014] FIGs. 2A through 2D are partial cross-sectional side views of a semiconductor device illustrating a process flow for forming a semiconductor device including a logic transistor and non-volatile memory transistor according to an embodiment of the present invention;

[0015] FIG. 3 is a partial cross-sectional side view of a semiconductor device including a logic transistor and non-volatile memory transistor comprising high work function gate electrodes according to an embodiment of the present invention;

[0016] FIGs. 4A and 4B illustrates a cross-sectional view of a non-volatile memory device including an ONONO stack;

[0017] FIG. 5 depicts a flowchart representing a series of operations in a method for fabricating a non-volatile charge trap memory device including an ONONO stack, in accordance with an embodiment of the present invention;

[0018] FIG. 6A illustrates a non-planar multigate device including a multi-layer charge-trapping region;

[0019] FIG. 6B illustrates a cross-sectional view of the non-planar multigate device of FIG. 6A;

[0020] FIGs. 7A and 7B illustrate a non-planar multigate device including a multi-layer charge-trapping region and a horizontal nanowire channel;

[0021] FIG. 7C illustrates a cross-sectional view of a vertical string of non-planar multigate devices of FIG. 7A;

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[0022] FIGs. 8A and 8B illustrate a non-planar multigate device including a multi-layer charge-trapping region and a vertical nanowire channel;

[0023] FIGs. 9A through 9F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 8A; and

[0024] FIGs. 10A through 10F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 8A.

DETAILED DESCRIPTION

[0025] The present invention is directed generally to non-volatile memory transistor including a multi-layer charge storage layer and high work function gate electrode to increase data retention and/or to improve programming time and efficiency. The structure and method are particularly useful for embedded memory or System-On-Chip (SOC) applications in which a semiconductor device includes both a logic transistor and non-volatile memory transistor comprising high work function gate electrodes formed on a common substrate.

[0026] In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures, and techniques are not shown in detail or are shown in block diagram form in order to avoid unnecessarily obscuring an understanding of this description.

[0027] Reference in the description to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the

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embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification do not necessarily all refer to the same embodiment. The term "to couple" as used herein may include both to directly connect and to indirectly connect through one or more intervening components.

[0028] Briefly, a non-volatile memory transistor according to the present invention includes a high work function gate electrode formed over an oxide-nitride-oxide (ONO) dielectric stack. By high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased.

[0029] In certain preferred embodiments, the high work function gate electrode comprises a doped polycrystalline silicon or polysilicon (poly) layer, the fabrication of which can be can be readily integrated into standard complementary metal-oxide-semiconductor (CMOS) process flows, such as those used fabricate metal-oxide-semiconductor (MOS) logic transistors, to enable fabrication of semiconductor memories or devices including both memory and logic transistors. More preferably, the same doped polysilicon layer can also be patterned to form a high work function gate electrode for the MOS logic transistor, thereby improving the performance of the logic transistor and increasing the efficiency of the fabrication process. Optionally, the ONO dielectric stack includes a multi-layer charge storage or charge trapping layer to further improve performance, and in particular data retention, of the memory transistor.

[0030] A semiconductor device including a non-volatile memory transistor comprising a high work function gate electrode and methods of forming the same will now be described in detail with reference to FIGs. 2A through 2D, which are partial cross-sectional side views of intermediate structures illustrating a process flow for forming a

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semiconductor device including both memory and logic transistors. For purposes of clarity, many of the details of semiconductor fabrication that are widely known and are not relevant to the present invention have been omitted from the following description.

[0031] Referring to FIG. 2, fabrication of the semiconductor device begins with formation of an ONO dielectric stack 202 over a surface 204 of a wafer or substrate 206. Generally, the ONO dielectric stack 202 includes a thin, lower oxide layer or tunneling oxide layer 208 that separates or electrically isolates a charge trapping or storage layer 210 from a channel region (not shown) of the memory transistor in the substrate 206, and a top or blocking oxide layer 212. Preferably, as noted above and as shown in FIGs. 2A-2D, the charge storage layer 210 is a multi-layer charge storage layer including at least a top, charge trapping oxynitride layer 210A and a lower, substantially trap free oxynitride layer 210B.

[0032] Generally, the substrate 206 may include any known silicon-based semiconductor material including silicon, silicon-germanium, silicon-on-insulator, or silicon-on-sapphire substrate. Alternatively, the substrate 206 may include a silicon layer formed on a non-silicon-based semiconductor material, such as gallium-arsenide, germanium, gallium-nitride, or aluminum-phosphide. Preferably, the substrate 206 is a doped or undoped silicon substrate.

[0033] The lower oxide layer or tunneling oxide layer 208 of the ONO dielectric stack 202 generally includes a relatively thin layer of silicon dioxide (SiO_2) of from about 15 angstrom (Å) to about 22 Å, and more preferably about 18 Å. The tunneling oxide layer 208 can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using chemical vapor deposition (CVD). In a preferred embodiment, the tunnel dielectric layer is formed or grown using a steam anneal.

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Generally, the process includes a wet-oxidizing method in which the substrate 206 is placed in a deposition or processing chamber, heated to a temperature from about 700°C to about 850°C, and exposed to a wet vapor for a predetermined period of time selected based on a desired thickness of the finished tunneling oxide layer 208. Exemplary process times are from about 5 to about 20 minutes. The oxidation can be performed at atmospheric or at low pressure.

[0034] In a preferred embodiment, the oxynitride layers 210A, 210B, of the multi-layer charge storage layer 210 are formed or deposited in separate steps utilizing different processes and process gases or source materials, and have an overall or combined thickness of from about 70 Å to about 150 Å, and more preferably about 100 Å. The lower, trap free oxynitride layer 210B can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a process gas including a silicon source, such as silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane (SiH_2Cl_2), tetrachlorosilane ($SiCl_4$), a nitrogen source, such as nitrogen (N_2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas, such as oxygen (O_2) or N_2O. In one embodiment the trap free oxynitride layer 210B is deposited in a low pressure CVD process using a process gas including dichlorosilane, NH_3 and N_2O, while maintaining the chamber at a pressure of from about 5 millitorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3

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mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm).

[0035] The top, charge trapping oxynitride layer 210A can be deposited over the bottom oxynitride layer 210B in a CVD process using a process gas including Bis-TertiaryButylAminoSilane (BTBAS). It has been found that the use of BTBAS increases the number of deep traps formed in the oxynitride by increasing the carbon level in the charge trapping oxynitride layer 210A. Moreover, these deep traps reduce charge losses due to thermal emission, thereby further improving data retention. More preferably, the process gas includes BTBAS and ammonia (NH_3) mixed at a predetermined ratio to provide a narrow band gap energy level in the oxynitride charge trapping layer. In particular, the process gas can include BTBAS and NH_3 mixed in a ratio of from about 7:1 to about 1:7. For example, in one embodiment the charge trapping oxynitride layer 210A is deposited in a low pressure CVD process using BTBAS and ammonia NH_3 at a chamber pressure of from about 5 mT to about 500 mT, and at a substrate temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes.

[0036] It has been found that an oxynitride layer produced or deposited under the above conditions yields a trap-rich oxynitride layer 210A, which improves the program and erase speed and increases of the initial difference (window) between program and erase voltages without compromising a charge loss rate of the memory transistor, thereby extending the operating life (EOL) of the device. Preferably, the charge trapping oxynitride layer 210A has a charge trap density of at least about $1E10/cm^2$, and more preferably from about $1E12/cm^2$ to about $1E14/cm^2$.

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[0037] Alternatively, the charge trapping oxynitride layer 210A can be deposited over the bottom oxynitride layer 210B in a CVD process using a process gas including BTBAS and substantially not including ammonia (NH_3). In this alternative embodiment of the method, the step of depositing the top, charge trapping oxynitride layer 210A is followed by a thermal annealing step in a nitrogen atmosphere including nitrous oxide (N_2O), NH_3, and/or nitrogen oxide (NO).

[0038] Preferably, the top, charge trapping oxynitride layer 210A is deposited sequentially in the same CVD tool used to form the bottom, trap free oxynitride layer 210B, substantially without breaking vacuum on the deposition chamber. More preferably, the charge trapping oxynitride layer 210A is deposited substantially without altering the temperature to which the substrate 206 was heated during deposition of the trap free oxynitride layer 210B.

[0039] A suitable thickness for the lower, trap free oxynitride layer 210B has been found to be from about 10 Å to about 80 Å, and a ratio of thicknesses between the bottom layer and the top, charge trapping oxynitride layer has been found to be from about 1:6 to about 6:1 , and more preferably at least about 1:4.

[0040] The top oxide layer 212 of the ONO dielectric stack 202 includes a relatively thick layer of SiO_2 of from about 20 Å to about 70 Å, and more preferably about 45 Å. The top oxide layer 212 can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using CVD. In a preferred embodiment, the top oxide layer 212 is a high-temperature-oxide (HTO) deposited using CVD process. Generally, the deposition process includes exposing the substrate 306 to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-containing gas, such as O_2

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or N_2O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

[0041] Preferably, the top oxide layer 212 is deposited sequentially in the same tool used to form the oxynitride layers 210A, 210B. More preferably, the oxynitride layers 210A, 210B, and the top oxide layer 212 are formed or deposited in the same tool used to grow the tunneling oxide layer 208. Suitable tools include, for example, an ONO AVP, commercially available from AVIZA technology of Scotts Valley, California.

[0042] Referring to FIG. 2B, in those embodiments in which the semiconductor device is to further include a logic transistor, such as a MOS logic transistor, formed on the surface of the same substrate the ONO dielectric stack 202 is removed from a region or area of the surface 204 in which the logic transistor is to be formed, and an oxide layer 214 the formed thereon.

[0043] Generally, the ONO dielectric stack 202 is removed from the desired region or area of the surface 204 using standard photolithographic and oxide etch techniques. For example, in one embodiment a patterned mask layer (not shown) is formed from a photo-resist deposited on the ONO dielectric stack 202, and the exposed region etched or removed using a low pressure radiofrequency (RF) coupled or generated plasma comprising fluorinated hydrocarbon and/or fluorinated carbon compounds, such as $C_2H_2F_4$ commonly referred to as Freon®. Generally, the processing gas further includes argon (Ar) and nitrogen (N_2) at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

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[0044] The oxide layer 214 of the logic transistor can include a layer of SiO_2 having a thickness of from about 30 to about 70 Å, and can be thermally grown or deposited using CVD. In one embodiment, the oxide layer 214 is thermally grown using a steam oxidation process, for example, by maintaining the substrate 206 in a steam atmosphere at a temperature of from about 650°C to about 850°C for a period of from about 10 minutes to about 120 minutes.

[0045] Next, a doped polysilicon layer is formed on a surface of the ONO dielectric stack 202 and, preferably, the oxide layer 214 of the logic transistor. More preferably, the substrate 206 is a silicon substrate or has a silicon surface on which the ONO dielectric stack is formed to form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a SONOS memory transistor.

[0046] Referring to FIG. 2C, forming of the doped polysilicon layer begins with the deposition of a conformal polysilicon layer 216 having a thickness of from about 200 Å to about 2000 Å over the ONO dielectric stack 202 and the oxide layer 214. The polysilicon layer 216 can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a silicon source or precursor. In one embodiment the polysilicon layer 216 is deposited in a low pressure CVD process using a silicon containing process gas, such as silane or dichlorosilane, and N_2, while maintaining the substrate 206 in a chamber at a pressure of from about 5 to 500 mT, and at a temperature of from about 600°C to about 1000°C for a period of from about 20 minutes to about 100 minutes to a substantially undoped polysilicon layer. The polysilicon layer 216 can be formed or grown directly as a doped polysilicon layer through the addition of

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gases such as phosphine, arsine, diborane or difluoroborane (BF_2) to the CVD chamber during the low pressure CVD process.

[0047] In one embodiment, the polysilicon layer 216 is doped following the growth or formation in the LPCVD process using ion implantation process. For example, the polysilicon layer 216 can be doped by implanting boron (B^+) or BF_2 ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) SONOS memory transistor and, preferably, a P-type (PMOS) logic transistor having high work function gate electrodes. More preferably, the polysilicon layer 216 is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV.

[0048] Alternatively, the polysilicon layer 216 can be doped by ion implantation after patterning or etching the polysilicon layer and the underlying dielectric layers. It will be appreciated that this embodiment includes additional masking steps to protect exposed areas of the substrate 206 surface 204 and/or the dielectric layers from receiving undesired doping. However, generally such a masking step is included in existing process flows regardless of whether the implantation occurs before or after patterning.

[0049] Referring to FIG. 2D, the polysilicon layer 216 and the underlying dielectric stack 202 and oxide layer 214 are patterned or etched to form high work function gate electrodes 218 of the memory transistor 220 and logic transistor 222. In one embodiment polysilicon layer 216 can be etched or patterned using a plasma comprising hydrobromic acid (HBr), chlorine (CL_2) and/or oxygen (O_2) at a pressure of about 25 mTorr, and a power of about 450 W. The oxide layers 208, 212, 214, and oxynitride layers 210A, 210B, can be

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etched using standard photolithographic and oxide etch techniques as described. For example, in one embodiment the patterned polysilicon layer 216 is used as a mask, and the exposed oxide layers 208, 212, 214, and oxynitride layers 210A, 210B, etched or removed using low pressure RF plasma. Generally, the plasma is formed from a processing gas comprising a fluorinated hydrocarbon and/or fluorinated carbon compounds, and further including Ar and N_2 at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

[0050] Finally, the substrate is thermal annealed with a single or multiple annealing steps at a temperature of from about 800 °C to about 1050 °C for a time of from about 1second to about 5 minutes to drive in ions implanted in the polysilicon layer 216, and to repair damage to the crystal structure of the polysilicon layer caused by ion implantation. Alternatively, advanced annealing techniques, such as flash and laser, can be employed with temperatures as high as 1350 °C and anneal times as low as 1 millisecond.

[0051] A partial cross-sectional side view of a semiconductor device 300 including a logic transistor 302 and non-volatile memory transistor 304 comprising high work function gate electrodes according to an embodiment of the present invention is shown in FIG. 3. Referring to FIG. 3, the memory transistor 304 is formed on a silicon substrate 306 and comprises a high work function gate electrode 308 formed from a doped polysilicon layer overlying a dielectric stack 310. The dielectric stack 310 overlies and controls current through a channel region 312 separating heavily doped source and drain (S/D) regions 314. Preferably, the dielectric stack 310 includes a tunnel dielectric layer 316, a multi-layer charge storage layer 318A, 318B, and a top or blocking oxide layer 320. More preferably, the multi-layer charge storage layer 318A, 318B, includes at least a top, charge trapping

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oxynitride layer 318A and a lower, substantially trap free oxynitride layer 318B. Optionally, as shown in FIG. 3, the memory transistor 304 further includes one or more sidewall spacers 322 surrounding the gate stack to electrically insulate it from contacts (not shown) to the S/D regions 320 and from other transistors in the semiconductor device formed on the substrate 306.

[0052] The logic transistor 302 comprises a gate electrode 324 overlying an oxide layer 326 formed over a channel region 328 separating heavily doped source and drain regions 330, and, optionally, can include one or more sidewall spacers 332 surrounding the gate electrically insulate it from contacts (not shown) to the S/D regions. Preferably, as shown in FIG. 3, the gate electrode 324 of the logic transistor 302 also comprises a high work function gate electrode formed from a doped polysilicon layer.

[0053] Generally, the semiconductor device 300 further includes a number of isolation structures 334, such as a local oxidation of silicon (LOCOS) region or structure, a field oxidation region or structure (FOX), or a shallow trench isolation (STI) structure to electrically isolate individual transistors formed on the substrate 306 from one another.

Implementations and Alternatives

[0054] In one aspect the present disclosure is directed to semiconductor devices including memory transistors with a high work function gate electrode and a multi-layer charge-trapping region. FIG. 4A is a block diagram illustrating a cross-sectional side view of an embodiment of one such memory transistor 400. The memory transistor 400 includes a ONNO stack 402 including an ONNO structure 404 formed over a surface 406 of a substrate 408. Substrate 408 includes one or more diffusion regions 410, such as source

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and drain regions, aligned to the gate stack 402 and separated by a channel region 412. Generally, the ONNO stack 402 includes a high work function gate electrode 414 formed upon and in contact with the ONNO structure 404. The high work function gate electrode 414 is separated or electrically isolated from the substrate 408 by the ONNO structure 404. The ONNO structure 404 includes a thin, lower oxide layer or tunnel dielectric layer 416 that separates or electrically isolates the ONNO stack 402 from the channel region 412, a top or blocking dielectric layer 420, and a multi-layer charge-trapping region 422.

[0055] The nanowire channel region 412 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 412 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[0056] The high work function gate electrode 414 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. As noted above, the polysilicon layer of the high work function gate electrode 414 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or difluoroborane (BF_2) to the CVD chamber during the low pressure CVD process, or can be doped following the growth or formation in the CVD process using an ion implantation process. In either embodiment, the polysilicon layer of the high work function gate electrode 414 is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 414 is doped by implanting boron (B^+) or BF_2 ions at an energy of from about 5 to about 100

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kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) memory transistor.

[0057] The tunnel dielectric layer 416 may be any material and have any thickness suitable to allow charge carriers to tunnel into the multi-layer charge-trapping region 422 under an applied gate bias while maintaining a suitable barrier to leakage when the memory transistor 400 is unbiased. In one embodiment, the tunnel dielectric layer 416 is formed by a thermal oxidation process and is composed of silicon dioxide or silicon oxy-nitride, or a combination thereof. In another embodiment, the tunnel dielectric layer 416 is formed by chemical vapor deposition (CVD) or atomic layer deposition (ALD) and is composed of a dielectric layer which may include, but is not limited to, silicon nitride, hafnium oxide, zirconium oxide, hafnium silicate, hafnium oxy-nitride, hafnium zirconium oxide and lanthanum oxide. In a specific embodiment, the tunnel dielectric layer 416 has a thickness in the range of 1-10 nanometers. In a particular embodiment, the tunnel dielectric layer 416 has a thickness of approximately 2 nanometers.

[0058] In one embodiment, the blocking dielectric layer 420 comprises a high temperature oxide (HTO). The higher quality HTO oxide enables the blocking dielectric layer 420 to be scaled in thickness. In an exemplary embodiment, the thickness of the blocking dielectric layer 420 comprising a HTO oxide is between 2.5 nm and 10.0 nm.

[0059] In another embodiment, the blocking dielectric layer 420 is further modified to incorporate nitrogen. In one such embodiment, the nitrogen is incorporated in the form of an ONO stack across the thickness of the blocking dielectric layer 420. Such a sandwich structure in place of the conventional pure oxygen blocking dielectric layer advantageously reduces the EOT of the entire stack 402 between the channel region 412 and high work

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function gate electrode 414 as well as enable tuning of band offsets to reduce back injection of carriers. The ONO stack blocking dielectric layer 420 can then be incorporated with the tunnel dielectric layer 416 and the multi-layer charge trapping layer 422 comprising an oxygen-rich first nitride layer 422a, an oxygen-lean second nitride layer 422b and an anti-tunneling layer 422c.

[0060] The multi-layer charge-trapping region 422 generally includes at least two nitride layers having differing compositions of silicon, oxygen and nitrogen, including an oxygen-rich, first nitride layer 422a, and a silicon-rich, nitrogen-rich, and oxygen-lean second nitride layer 422b, a silicon-rich. In some embodiments, such as that shown in FIG. 4B, the multi-layer charge-trapping region further includes an anti-tunneling layer 422c comprising an oxide, such as silicon dioxide, separating the oxygen-lean second nitride layer 422b from the oxygen-rich, first nitride layer 422a, to provide a ONONO stack 402 including an ONONO structure 404.

[0061] It has been found that an oxygen-rich, first nitride layer 422a decreases the charge loss rate after programming and after erase, which is manifested in a small voltage shift in the retention mode, while a silicon-rich, nitrogen-rich, and oxygen-lean second nitride layer 422b improves the speed and increases of the initial difference between program and erase voltage without compromising a charge loss rate of memory transistors made using an embodiment of the silicon-oxide-oxynitride-oxide-silicon structure, thereby extending the operating life of the device.

[0062] It has further been found the anti-tunneling layer 422c substantially reduces the probability of electron charge that accumulates at the boundaries of the oxygen-lean second nitride layer 422b during programming from tunneling into the first nitride layer

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422a, resulting in lower leakage current than for a conventional non-volatile memory transistor.

[0063] The multi-layer charge-trapping region can have an overall thickness of from about 50 Å to about 150 Å, and in certain embodiments less than about 100 Å, with the with the thickness of the anti-tunneling layer 422c being from about 5 Å to about 20 Å, and the thicknesses of the nitride layers 404b, 404a, being substantially equal.

[0064] A method or forming or fabricating a semiconductor device including a memory transistor with a high work function gate electrode and a multi-layer charge-trapping region according to one embodiment will now be described with reference to the flowchart of FIG. 5.

[0065] Referring to FIG. 5, the method begins with forming a tunnel dielectric layer, such as a first oxide layer, over a silicon containing layer on a surface of a substrate (500). The tunnel dielectric layer can be formed or deposited by any suitable means, including a plasma oxidation process, In-Situ Steam Generation (ISSG) or a radical oxidation process. In one embodiment, the radical oxidation process involves flowing hydrogen (H_2) and oxygen (O_2) gas into a processing chamber or furnace to effect growth of a the tunnel dielectric layer by oxidation consumption of a portion of the substrate.

[0066] Next, an oxygen-rich first nitride layer of the multi-layer charge-trapping region is formed on a surface of the tunnel dielectric layer (502). In one embodiment, the oxygen-rich first nitride layer is formed or deposited in a low pressure CVD process using a silicon source, such as silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane or DCS (SiH_2Cl_2), tetrachlorosilane ($SiCl_4$) or Bis-TertiaryButylAmino Silane (BTBAS), a nitrogen source, such as nitrogen (N_2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous

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oxide (N_2O), and an oxygen-containing gas, such as oxygen (O_2) or N_2O. Alternatively, gases in which hydrogen has been replaced by deuterium can be used, including, for example, the substitution of deuterated-ammonia (ND_3) for NH_3. The substitution of deuterium for hydrogen advantageously passivates Si dangling bonds at the silicon-oxide interface, thereby increasing an NBTI (Negative Bias Temperature Instability) lifetime of the devices.

[0067] For example, the lower or oxygen-rich first nitride layer can be deposited over the tunnel dielectric layer by placing the substrate in a deposition chamber and introducing a process gas including N_2O, NH_3 and DCS, while maintaining the chamber at a pressure of from about 5 milliTorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700 degrees Celsius to about 850 degrees Celsius and in certain embodiments at least about 760 degrees Celsius, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm). It has been found that an oxynitride layer produced or deposited under these condition yields a silicon-rich, oxygen-rich first nitride layer.

[0068] Next, an anti-tunneling layer is formed or deposited on a surface of the first nitride layer (504). As with the tunnel dielectric layer, the anti-tunneling layer can be formed or deposited by any suitable means, including a plasma oxidation process, In-Situ Steam Generation (ISSG) or a radical oxidation process. In one embodiment, the radical oxidation process involves flowing hydrogen (H_2) and oxygen (O_2) gas into a batch-

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processing chamber or furnace to effect growth of the anti-tunneling layer by oxidation consumption of a portion of the first nitride layer.

[0069] The top or oxygen-lean second nitride layer of the multi-layer charge-trapping region is then formed on a surface of the anti-tunneling layer (506). The oxygen-lean second nitride layer can be deposited over the anti-tunneling layer in a CVD process using a process gas including N_2O, NH_3 and DCS, at a chamber pressure of from about 5 mT to about 500 mT, and at a substrate temperature of from about 700 degrees Celsius to about 850 degrees Celsius and in certain embodiments at least about 760 degrees Celsius, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 20 sccm. It has been found that a nitride layer produced or deposited under these condition yields a silicon-rich, nitrogen-rich, and oxygen-lean second nitride layer, which improves the speed and increases of the initial difference between program and erase voltage without compromising a charge loss rate of memory transistors made using an embodiment of the silicon-oxide-oxynitride-oxide-silicon structure, thereby extending the operating life of the device.

[0070] In some embodiments, the oxygen-lean second nitride layer can be deposited over the anti-tunneling layer in a CVD process using a process gas including BTBAS and ammonia (NH_3) mixed at a ratio of from about 7:1 to about 1:7 to further include a concentration of carbon selected to increase the number of traps therein. The

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selected concentration of carbon in the second oxynitride layer can include a carbon concentration of from about 5% to about 15%.

[0071] Next, a top, blocking oxide layer or blocking dielectric layer is formed on a surface of the oxygen-lean second nitride layer of the multi-layer charge-trapping region (508). As with the tunnel dielectric layer and the anti-tunneling layer the blocking dielectric layer can be formed or deposited by any suitable means, including a plasma oxidation process, In-Situ Steam Generation (ISSG) or a radical oxidation process. In one embodiment, the blocking dielectric layer comprises a high-temperature-oxide (HTO) deposited using CVD process. Generally, the deposition process includes exposing the substrate 306 to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-containing gas, such as O_2 or N_2O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

[0072] Alternatively, the blocking dielectric layer is formed using an ISSG oxidation process. In one embodiment, the ISSG is performed in an RTP chamber, such as the ISSG chamber from Applied Materials described above, at pressures of from about 8 to 12 Torr and a temperature of about 1050 °C with an oxygen rich gas mixture hydrogen to which from about 0.5% to 33% hydrogen has been added.

[0073] It will be appreciated that in either embodiment the thickness of the second nitride layer may be adjusted or increased as some of the oxygen-lean second nitride layer will be effectively consumed or oxidized during the process of forming the blocking dielectric layer.

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[0074] Finally, a high work function gate electrode is formed upon and in contact with the blocking dielectric layer (510). The high work function gate electrode includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. As noted above, the polysilicon layer of the high work function gate electrode can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or difluoroborane (BF_2) to the CVD chamber during the low pressure CVD process, or can be doped following the growth or formation in the CVD process using an ion implantation process. In either embodiment, the polysilicon layer of the high work function gate electrode is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode is doped by implanting boron (B^+) or BF_2 ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) memory transistor.

[0075] With the completion of the gate stack fabrication, further processing may occur as known in the art to conclude fabrication of a SONOS-type memory device.

[0076] In another aspect the present disclosure is also directed to multigate or multigate-surface memory transistors including charge-trapping regions overlying two or more sides of a channel region formed on or above a surface of a substrate, and methods of fabricating the same. Multigate devices include both planar and non-planar devices. A planar multigate device (not shown) generally includes a double-gate planar device in which a number of first layers are deposited to form a first gate below a subsequently

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formed channel region, and a number of second layers are deposited thereover to form a second gate. A non-planar multigate device generally includes a horizontal or vertical channel region formed on or above a surface of a substrate and surrounded on three or more sides by a gate.

[0077] FIG. 6A illustrates one embodiment of a non-planar multigate memory transistor including with a high work function gate electrode. Referring to FIG. 6A, the memory transistor 600, commonly referred to as a finFET, includes a channel region 602 formed from a thin film or layer of semiconducting material overlying a surface 604 on a substrate 606 connecting a source region 608 and a drain region 610 of the memory transistor. The channel region 602 is enclosed on three sides by a fin which forms a gate 612 of the device. The thickness of the gate 612 (measured in the direction from source region to drain region) determines the effective channel region length of the device. As with the embodiments described above, the channel region 602 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 602 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[0078] In accordance with the present disclosure, the non-planar multigate memory transistor 600 of FIG. 6A can include a high work function gate electrode and a multi-layer charge-trapping region. FIG. 6B is a cross-sectional view of a portion of the non-planar memory transistor of FIG. 6A including a portion of the substrate 606, channel region 602 and the gate 612 illustrating a high work function gate electrode 614 and a multi-layer charge-trapping region 616. The gate 612 further includes a tunnel dielectric layer 618 overlying a raised channel region 602, and a blocking dielectric layer 620 overlying the

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blocking dielectric layer to form a control gate of the memory transistor 600. The channel region 602 and gate 612 can be formed directly on substrate 606 or on an insulating or dielectric layer 622, such as a buried oxide layer, formed on or over the substrate.

[0079] As with the embodiments described above, the high work function gate electrode 614 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. The polysilicon layer of the high work function gate electrode 614 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, and is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 614 is doped to a concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2}.

[0080] Referring to FIG. 6B, the multi-layer charge-trapping region 616 includes at least one lower or bottom oxygen-rich first nitride layer 616a including nitride closer to the tunnel dielectric layer 618, and an upper or top oxygen-lean second nitride layer 616b overlying the oxygen-rich first nitride layer. Generally, the oxygen-lean second nitride layer 616b includes a silicon-rich, oxygen-lean nitride layer and includes a majority of a charge traps distributed in the multi-layer charge-trapping region, while the oxygen-rich first nitride layer 616a includes an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the oxygen-lean second nitride layer to reduce the number of charge traps therein. By oxygen-rich it is meant wherein a concentration of oxygen in the oxygen-rich first nitride layer 616a is from about 15 to about 40%, whereas a concentration of oxygen in oxygen-lean second nitride layer 616b is less than about 5%.

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[0081] In one embodiment, the blocking dielectric 620 also includes an oxide, such as an HTO, to provide an ONNO structure. The channel region 602 and the overlying ONNO structure can be formed directly on a silicon substrate 606 and overlaid with a high work function gate electrode 614 to provide a SONNOS structure.

[0082] In some embodiments, such as that shown in FIG. 6B, the multi-layer charge-trapping region 616 further includes at least one thin, intermediate or anti-tunneling layer 616c including a dielectric, such as an oxide, separating the oxygen-lean second nitride layer 616b from the oxygen-rich first nitride layer 616a. As noted above, the anti-tunneling layer 616c substantially reduces the probability of electron charge that accumulates at the boundaries of the oxygen-lean second nitride layer 616b during programming from tunneling into the first nitride layer 616a.

[0083] As with the embodiments described above, either or both of the oxygen-rich first nitride layer 616a and the oxygen-lean second nitride layer 616b can include silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The oxygen-lean second nitride layer 616b has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the oxygen-rich first nitride layer 616a, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

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[0084] In those embodiments including an intermediate or anti-tunneling layer 616c including oxide, the anti-tunneling layer can be formed by oxidation of the bottom oxynitride layer, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100 degrees Celsius using a single wafer tool, or 800-900 degrees Celsius using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0085] Finally, in those embodiments including a blocking dielectric 620 including oxide the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of the blocking dielectric 620 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric 620 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the top nitride thickness may be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer. A third option is to oxidize the second nitride layer to a chosen depth using radical oxidation.

[0086] A suitable thickness for the oxygen-rich first nitride layer 616a may be from about 30Å to about 160Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 616c. A suitable thickness for the oxygen-lean second nitride layer 616b may be at least 30Å. In certain embodiments, the oxygen-lean second nitride layer 616b may be formed up to 130Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric 620. A ratio of thicknesses between the oxygen-rich first nitride layer 616a and

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oxygen-lean second nitride layer 616b is approximately 1:1 in some embodiments, although other ratios are also possible.

[0087] In other embodiments, either or both of the oxygen-lean second nitride layer 616b and the blocking dielectric 620 may include a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0088] In another embodiment, shown in FIGs. 7A and 7B, the memory transistor can include a nanowire channel region formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source region and a drain region of the memory transistor. By nanowire channel region it is meant a conducting channel region formed in a thin strip of crystalline silicon material, having a maximum cross-sectional dimension of about 10 nanometers (nm) or less, and more preferably less than about 6 nm.

[0089] Referring to FIG. 7A, the memory transistor 700 includes a horizontal nanowire channel region 702 formed from a thin film or layer of semiconducting material on or overlying a surface on a substrate 706, and connecting a source region 708 and a drain region 710 of the memory transistor. In the embodiment shown, the device has a gate-all-around (GAA) structure in which the nanowire channel region 702 is enclosed on all sides by a gate 712 of the device. The thickness of the gate 712 (measured in the direction from source region to drain region) determines the effective channel region length of the device. As with the embodiments described above, the nanowire channel region 702 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 702 includes a crystalline silicon, the channel

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region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[0090] In accordance with the present disclosure, the non-planar multigate memory transistor 700 of FIG. 7A can include a high work function gate electrode and a multi-layer charge-trapping region. FIG. 7B is a cross-sectional view of a portion of the non-planar memory transistor of FIG. 7A including a portion of the substrate 706, nanowire channel region 702 and the gate 712 illustrating a high work function gate electrode 714 and a multi-layer charge-trapping region 716a-716c. Referring to FIG. 7B, the gate 712 further includes a tunnel dielectric layer 718 overlying the nanowire channel region 702, and a blocking dielectric layer 720.

[0091] As with the embodiments described above, the high work function gate electrode 714 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. The polysilicon layer of the high work function gate electrode 714 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, and is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 714 is doped to a concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2}.

[0092] The multi-layer charge-trapping region 716a-716c includes at least one inner oxygen-rich first nitride layer 716a comprising nitride closer to the tunnel dielectric layer 718, and an outer oxygen-lean second nitride layer 716b overlying the oxygen-rich first nitride layer. Generally, the outer oxygen-lean second nitride layer 716b comprises a

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silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in the multi-layer charge-trapping region, while the oxygen-rich first nitride layer 716a comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the outer oxygen-lean second nitride layer to reduce the number of charge traps therein.

[0093] In some embodiments, such as that shown, the multi-layer charge-trapping region 716 further includes at least one thin, intermediate or anti-tunneling layer 716c comprising a dielectric, such as an oxide, separating outer oxygen-lean second nitride layer 716b from the oxygen-rich first nitride layer 716a. The anti-tunneling layer 716c substantially reduces the probability of electron charge that accumulates at the boundaries of outer oxygen-lean second nitride layer 716b during programming from tunneling into the oxygen-rich first nitride layer 716a, resulting in lower leakage current.

[0094] As with the embodiment described above, either or both of the oxygen-rich first nitride layer 716a and the outer oxygen-lean second nitride layer 716b can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The outer oxygen-lean second nitride layer 716b has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the oxygen-rich first nitride layer 716a, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

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[0095] In those embodiments including an intermediate or anti-tunneling layer 716c comprising oxide, the anti-tunneling layer can be formed by oxidation of the oxygen-rich first nitride layer 716a, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100 degrees Celsius using a single wafer tool, or 800-900 degrees Celsius using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0096] Finally, in those embodiments in which the blocking dielectric 720 comprises oxide, the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of blocking dielectric layer 720 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric layer 720 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the thickness of the outer oxygen-lean second nitride layer 716b may need to be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer.

[0097] A suitable thickness for the oxygen-rich first nitride layer 716a may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 716c. A suitable thickness for the outer oxygen-lean second nitride layer 716b may be at least 30Å. In certain embodiments, the outer oxygen-lean second nitride layer 716b may be formed up to 70Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric layer 720. A ratio of thicknesses between the oxygen-rich first

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nitride layer 716a and the outer oxygen-lean second nitride layer 716b is approximately 1:1 in some embodiments, although other ratios are also possible.

[0098] In other embodiments, either or both of the outer oxygen-lean second nitride layer 716b and the blocking dielectric layer 720 may comprise a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0099] Figure 7C illustrates a cross-sectional view of a vertical string of non-planar multigate devices 700 of FIG. 7A arranged in a Bit-Cost Scalable or BiCS architecture 726. The architecture 726 consists of a vertical string or stack of non-planar multigate devices 700, where each device or cell includes a channel region 702 overlying the substrate 706, and connecting a source region and a drain region (not shown in this figure) of the memory transistor, and having a gate-all-around (GAA) structure in which the nanowire channel region 702 is enclosed on all sides by a gate 712. The BiCS architecture reduces number of critical lithography steps compared to a simple stacking of layers, leading to a reduced cost per memory bit.

[00100] In another embodiment, the memory transistor is or includes a non-planar device comprising a vertical nanowire channel region formed in or from a semiconducting material projecting above or from a number of conducting, semiconducting layers on a substrate. In one version of this embodiment, shown in cut-away in FIG. 8A, the memory transistor 800 comprises a vertical nanowire channel region 802 formed in a cylinder of semiconducting material connecting a source region 804 and drain region 806 of the device. The channel region 802 is surrounded by a tunnel dielectric layer 808, a multi-layer

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charge-trapping region 810, a blocking dielectric layer 812 and a high work function gate electrode 814 overlying the blocking dielectric layer to form a control gate of the memory transistor 800. The channel region 802 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or can include an annular layer formed over a cylinder of dielectric filler material. As with the horizontal nanowires described above, the channel region 802 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 802 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[00101] As with the embodiments described above, the high work function gate electrode 814 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. The polysilicon layer of the high work function gate electrode 814 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, and is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 814 is doped to a concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2}.

[00102] In some embodiments, such as that shown in FIG. 8B, the multi-layer charge-trapping region 810 includes at least an inner or oxygen-rich first nitride layer 810a closest to the tunnel dielectric layer 808, and an outer or oxygen-lean second nitride layer 810b. Optionally, as in the embodiment shown, the oxygen-rich first nitride layer 810a and

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the oxygen-lean second nitride layer 810b are separated by an intermediate oxide or anti-tunneling layer 810c comprising oxide.

[00103] Either or both of the oxygen-rich first nitride layer 810a and the oxygen-lean second nitride layer 810b can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer.

[00104] Finally, either or both of the oxygen-lean second nitride layer 810b and the blocking dielectric layer 812 may comprise a high K dielectric, such as HfSiON, HfSiO, HfO, ZrSiON, ZrSiO, ZrO, or Y_2O_3.

[00105] A suitable thickness for the oxygen-rich first nitride layer 810a may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 820. A suitable thickness for the oxygen-lean second nitride layer 810b may be at least 30Å, and a suitable thickness for the blocking dielectric layer 812 may be from about 30-70Å.

[00106] The memory transistor 800 of FIG. 8A can be made using either a gate first or a gate last scheme. FIGs. 9A-F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 8A. FIGs. 10A-F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 8A.

[00107] Referring to FIG. 9A, in a gate first scheme a first or lower dielectric layer 902, such as an oxide, is formed over a first, doped diffusion region 904, such as a source region or a drain region, in a substrate 906. A high work function gate electrode 908 is formed over the first dielectric layer 902 to form a control gate of the device, and a second

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or upper dielectric layer 910 formed thereover. As with embodiments described above, the high work function gate electrode 908 can be formed by depositing and/or doping polysilicon layer having a thickness of from about 200 Å to about 2000 Å and a dopant concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2} so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. The polysilicon layer can be deposited in a low pressure CVD process as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, or can be doped using an ion implantation process following deposition.

[00108] The first and second dielectric layers 902, 910, can be deposited by CVD, radical oxidation or be formed by oxidation of a portion of the underlying layer or substrate. Generally the thickness of the high work function gate electrode 908 is from about 40-50Å, and the first and second dielectric layers 902, 910, from about 20- 80Å.

[00109] Referring to FIG. 9B, a first opening 912 is etched through the overlying high work function gate electrode 908, and the first and second dielectric layers 902, 910, to the diffusion region 904 in the substrate 906. Next, layers of a tunneling oxide 914, charge-trapping region 916, and blocking dielectric 918 are sequentially deposited in the opening and the surface of the upper dielectric layer 910 planarized to yield the intermediate structure shown in FIG. 9C.

[00110] Although not shown, it will be understood that as in the embodiments described above the charge-trapping region 916 can include a multi-layer charge-trapping region comprising at least one lower or oxygen-rich first nitride layer closer to the tunnel dielectric layer 914, and an upper or oxygen-lean second nitride layer overlying the oxygen-rich first nitride layer. Generally, the oxygen-lean second nitride layer comprises

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a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in the multi-layer charge-trapping region, while the oxygen-rich first nitride layer comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the oxygen-lean second nitride layer to reduce the number of charge traps therein. In some embodiments, the multi-layer charge-trapping region 916 further includes at least one thin, intermediate or anti-tunneling layer comprising a dielectric, such as an oxide, separating the oxygen-lean second nitride layer from the oxygen-rich first nitride layer.

[00111] Next, a second or channel region opening 920 is anisotropically etched through tunneling oxide 914, charge-trapping region 916, and blocking dielectric 918, FIG. 9D. Referring to FIG. 9E, a semiconducting material 922 is deposited in the channel region opening to form a vertical channel region 924 therein. The vertical channel region 924 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or, as shown in FIG. 9E, can include a separate, layer semiconducting material 922 surrounding a cylinder of dielectric filler material 926.

[00112] Referring to FIG. 9F, the surface of the upper dielectric layer 910 is planarized and a layer of semiconducting material 928 including a second, doped diffusion region 930, such as a source region or a drain region, formed therein deposited over the upper dielectric layer to form the device shown.

[00113] Referring to FIG. 10A, in a gate last scheme a dielectric layer 1002, such as an oxide, is formed over a sacrificial layer 1004 on a surface on a substrate 1006, an opening etched through the dielectric and sacrificial layers and a vertical channel region 1008 formed therein. As with embodiments described above, the vertical channel region 1008 can include an annular region in an outer layer of a substantially solid cylinder of

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semiconducting material 1010, such as polycrystalline or monocrystalline silicon, or can include a separate, layer semiconducting material surrounding a cylinder of dielectric filler material (not shown). The dielectric layer 1002 can comprise any suitable dielectric material, such as a silicon oxide, capable of electrically isolating the subsequently formed high work function gate electrode of the memory transistor 800 from an overlying electrically active layer or another memory transistor.

[00114] Referring to Figure 10B, a second opening 1012 is etched through the etched through the dielectric and sacrificial layers 1002, 1004, to the substrate 1006, and the sacrificial layer 1004 at least partially etched or removed. The sacrificial layer 1004 can comprise any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 1002, substrate 1006 and vertical channel region 1008. In one embodiment the sacrificial layer 1004 comprises an oxide that can be removed by Buffered Oxide Etch (BOE etch).

[00115] Referring to Figure 10C and 10D, a tunnel dielectric layer 1014, a multi-layer charge-trapping region 1016A-C, and a blocking dielectric layer 1018 are sequentially deposited in the opening, and the surface of the dielectric layer 1002 planarized to yield the intermediate structure shown in Figure 10C. As in the embodiments described above, the multi-layer charge trapping layer 1016A-C is a split multi-layer charge trapping layer including at least an inner oxygen-rich first nitride layer 1016A closest to the tunnel dielectric layer 1014, and an outer, oxygen-lean second nitride layer 1016B. Optionally, the first and second charge trapping layers can be separated by an intermediate oxide or anti-tunneling layer 1016C.

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[00116] Next, a high work function gate electrode 1022 is deposited into the second opening 1012 and the surface of the upper dielectric layer 1002 planarized to yield the intermediate structure illustrated in Figure 10E. As with the embodiments described above, the high work function gate electrode 1022 includes a doped polysilicon layer having a dopant concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2} so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. The polysilicon layer of the high work function gate electrode 1022 is grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, to the CVD process. Finally, an opening 1024 is etched through the gate layer 1022 to form control gates of separate memory devices 1026A and 1026B.

[00117] The foregoing description of specific embodiments and examples of the invention have been presented for the purpose of illustration and description, and although the invention has been described and illustrated by certain of the preceding examples, it is not to be construed as being limited thereby. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications, improvements and variations within the scope of the invention are possible in light of the above teaching. It is intended that the scope of the invention encompass the generic area as herein disclosed, and by the claims appended hereto and their equivalents. The scope of the present invention is defined by the claims, which includes known equivalents and unforeseeable equivalents at the time of filing of this application.

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WHAT IS CLAIMED IS:

1. A memory device, comprising:

a gate structure including a gate electrode comprising a polysilicon layer;

a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and

a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel,

wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers.

ABSTRACT

An example memory device includes a channel positioned between and electrically connecting a first diffusion region and a second diffusion region, and a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel. The multi-layer charge trapping layer includes a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers. The anti-tunneling layer includes an oxide layer. The first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.

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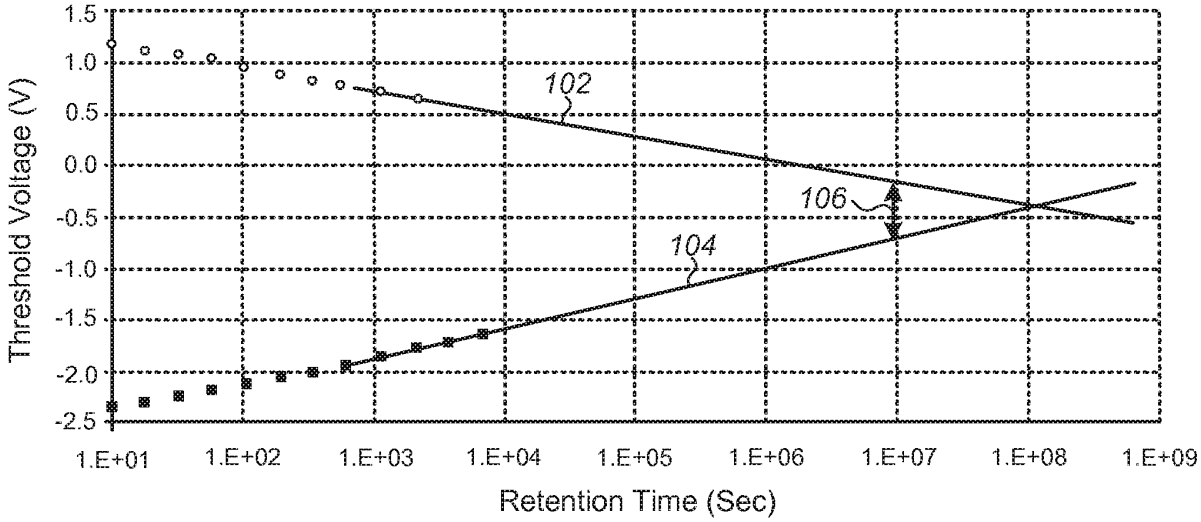

Threshold Voltage (V)
1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
102
104
106
1.E+01
1.E+02
1.E+03
1.E+04
1.E+05
1.E+06
1.E+07
1.E+08
1.E+09
Retention Time (Sec)

FIG. 1A

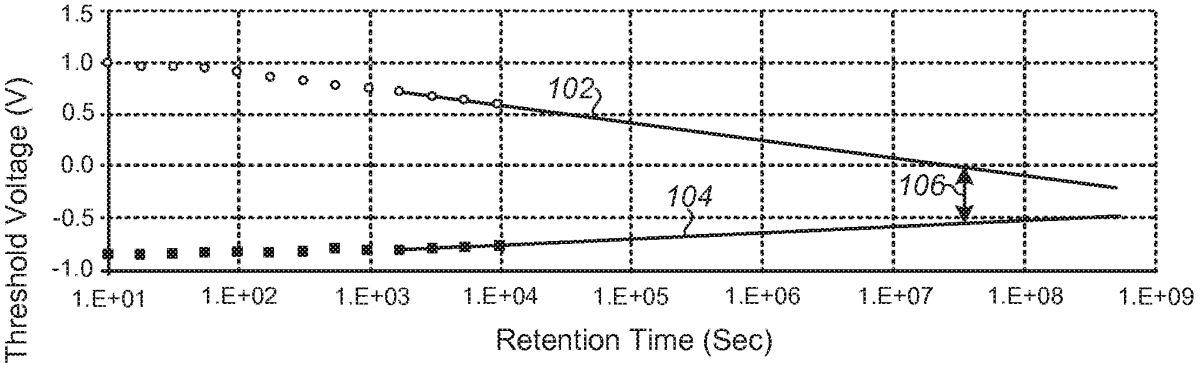

Threshold Voltage (V)
1.5
1.0
0.5
0.0
-0.5
-1.0
102
104
106
1.E+01
1.E+02
1.E+03
1.E+04
1.E+05
1.E+06
1.E+07
1.E+08
1.E+09
Retention Time (Sec)

FIG. 1B

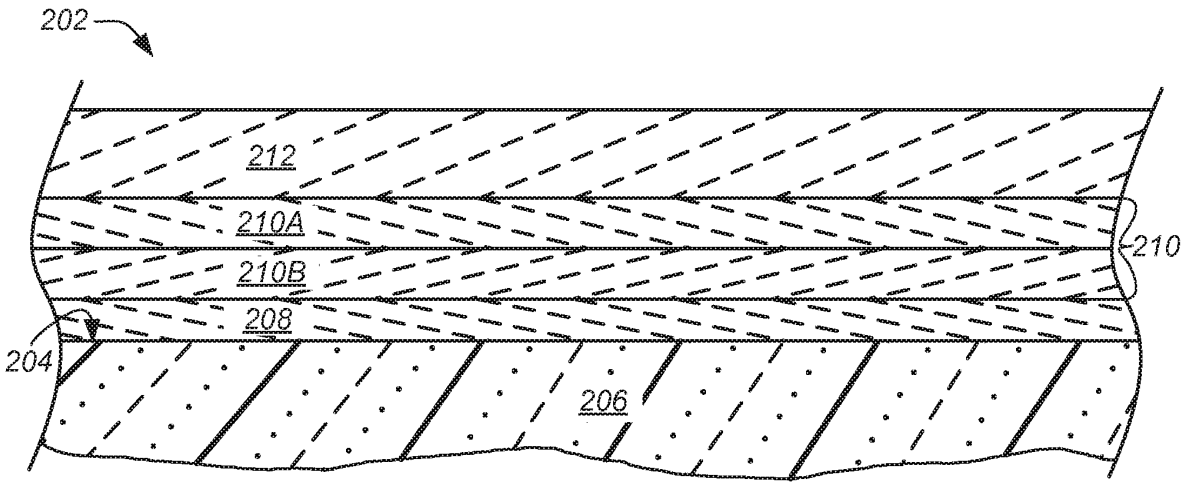

202
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210A
210B
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210
204
206

FIG. 2A

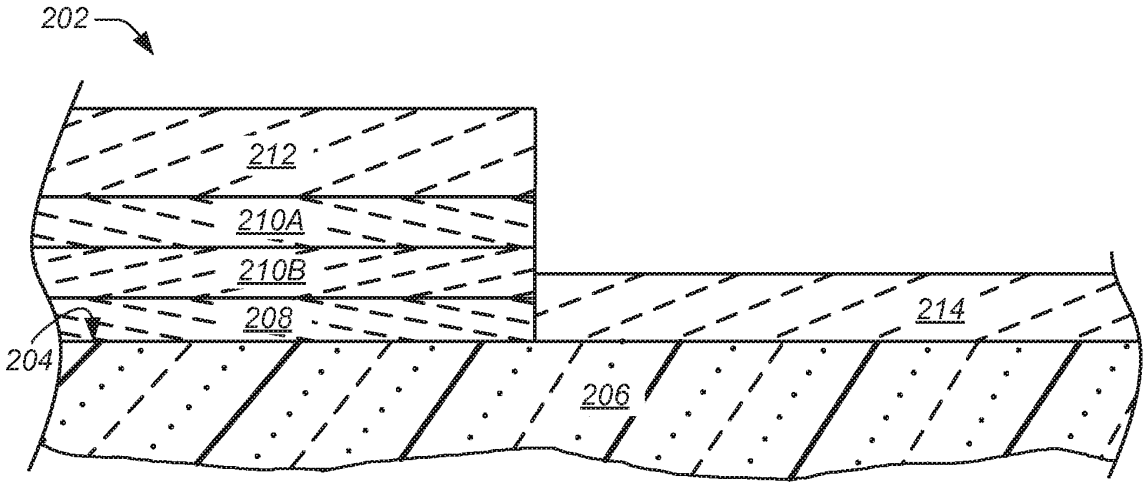

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210A
210B
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206

FIG. 2B

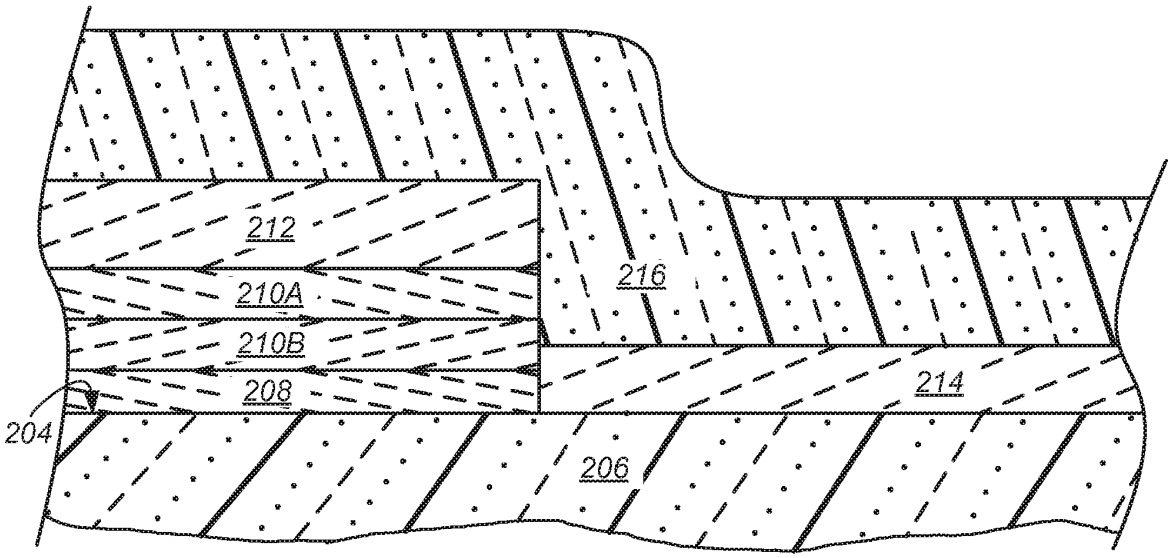

212
210A
210B
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204
216
214
206

FIG. 2C

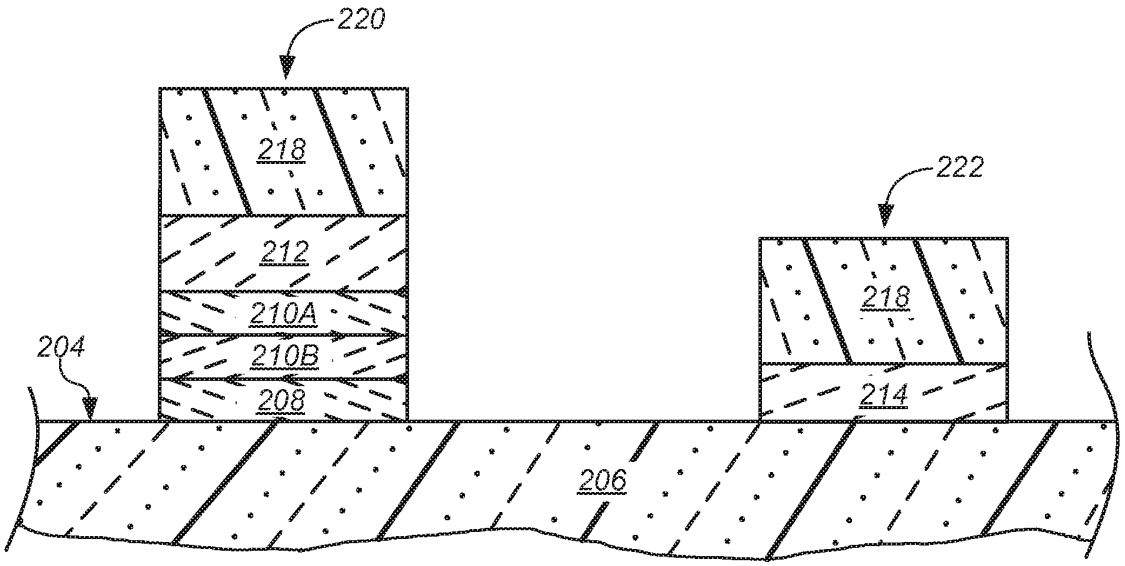

220
218
212
210A
210B
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222
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214
206

FIG. 2D

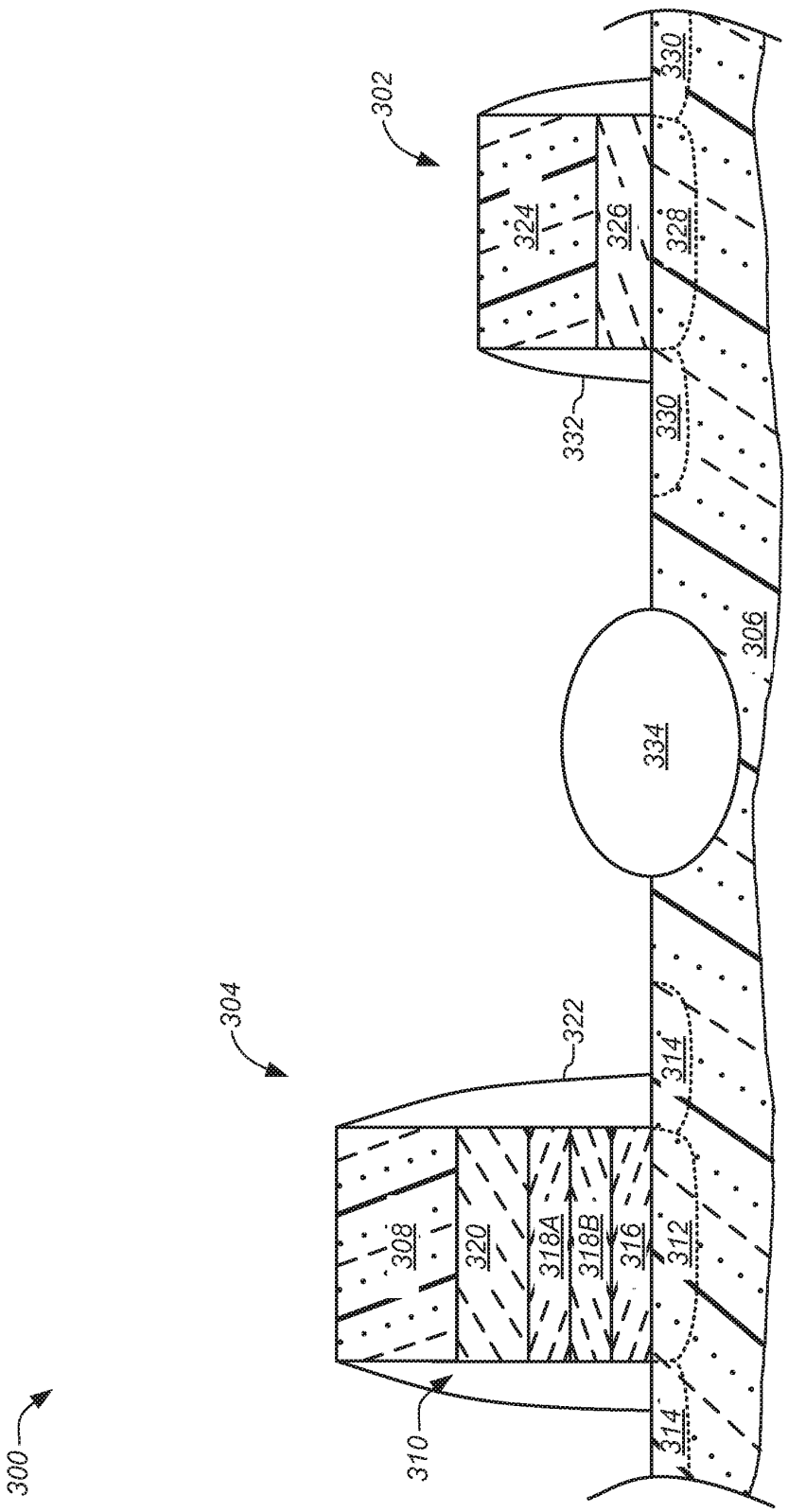

300
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318A
318B
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332
334

FIG. 3

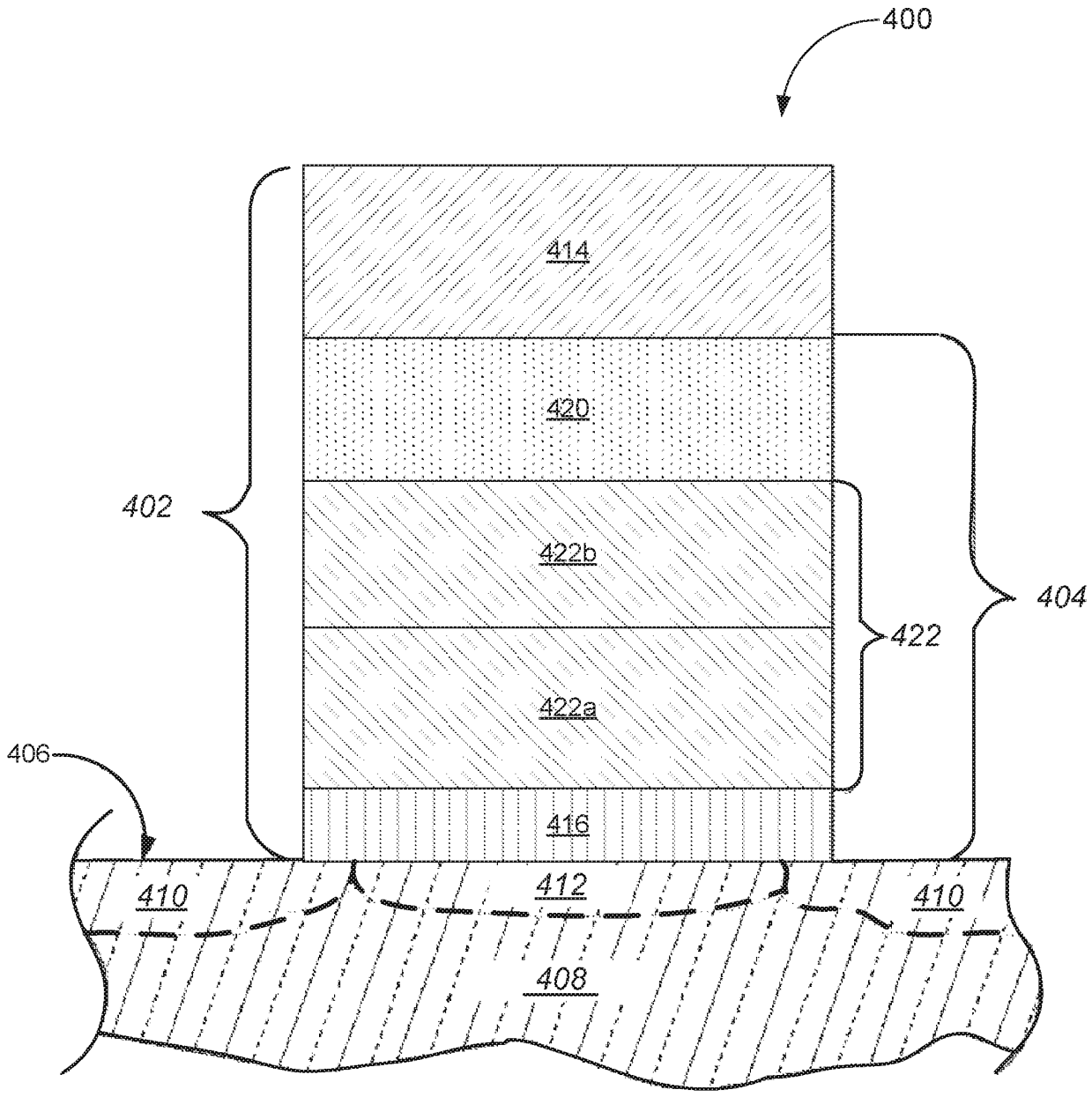


FIG. 4A

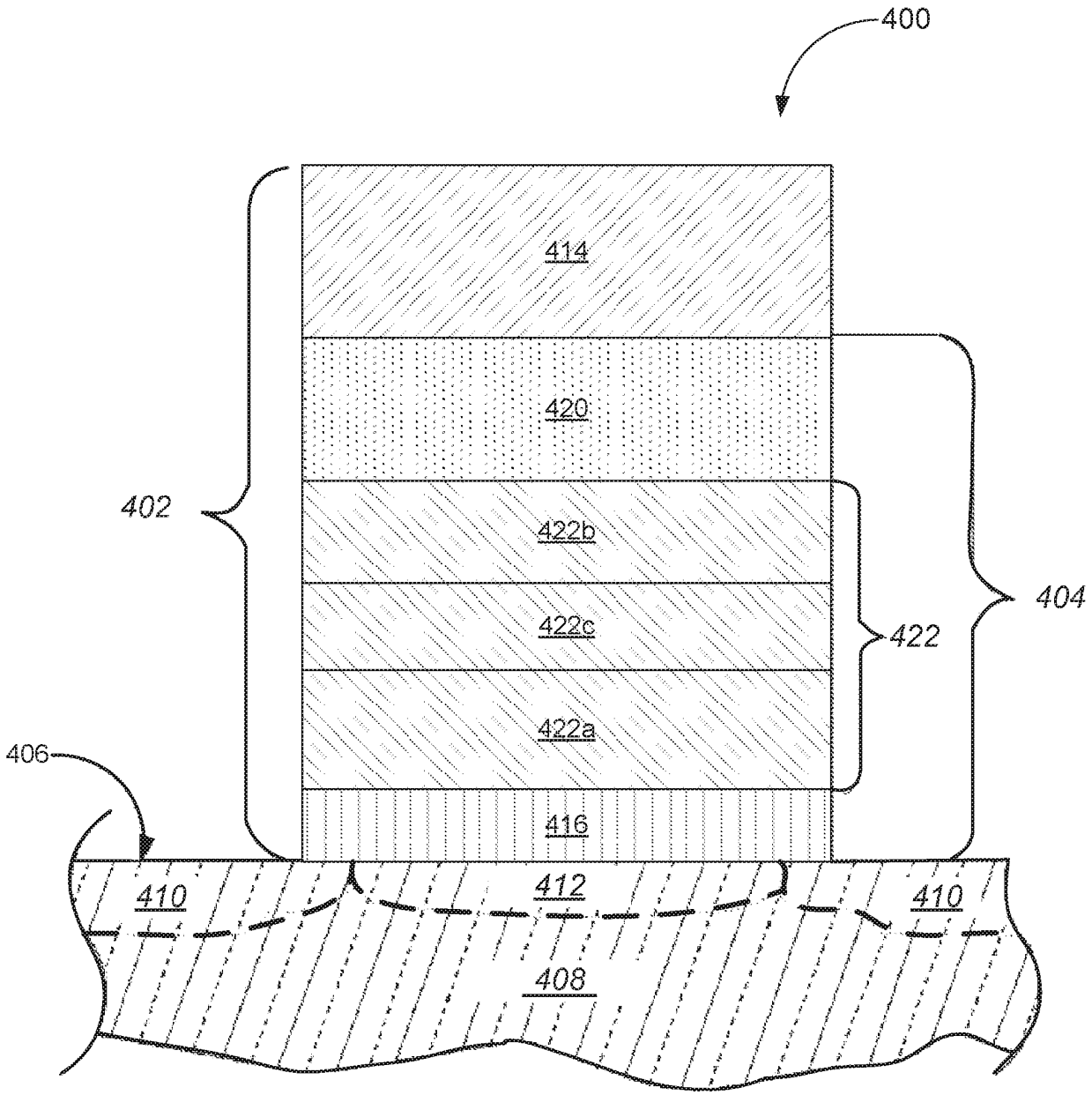


FIG. 4B

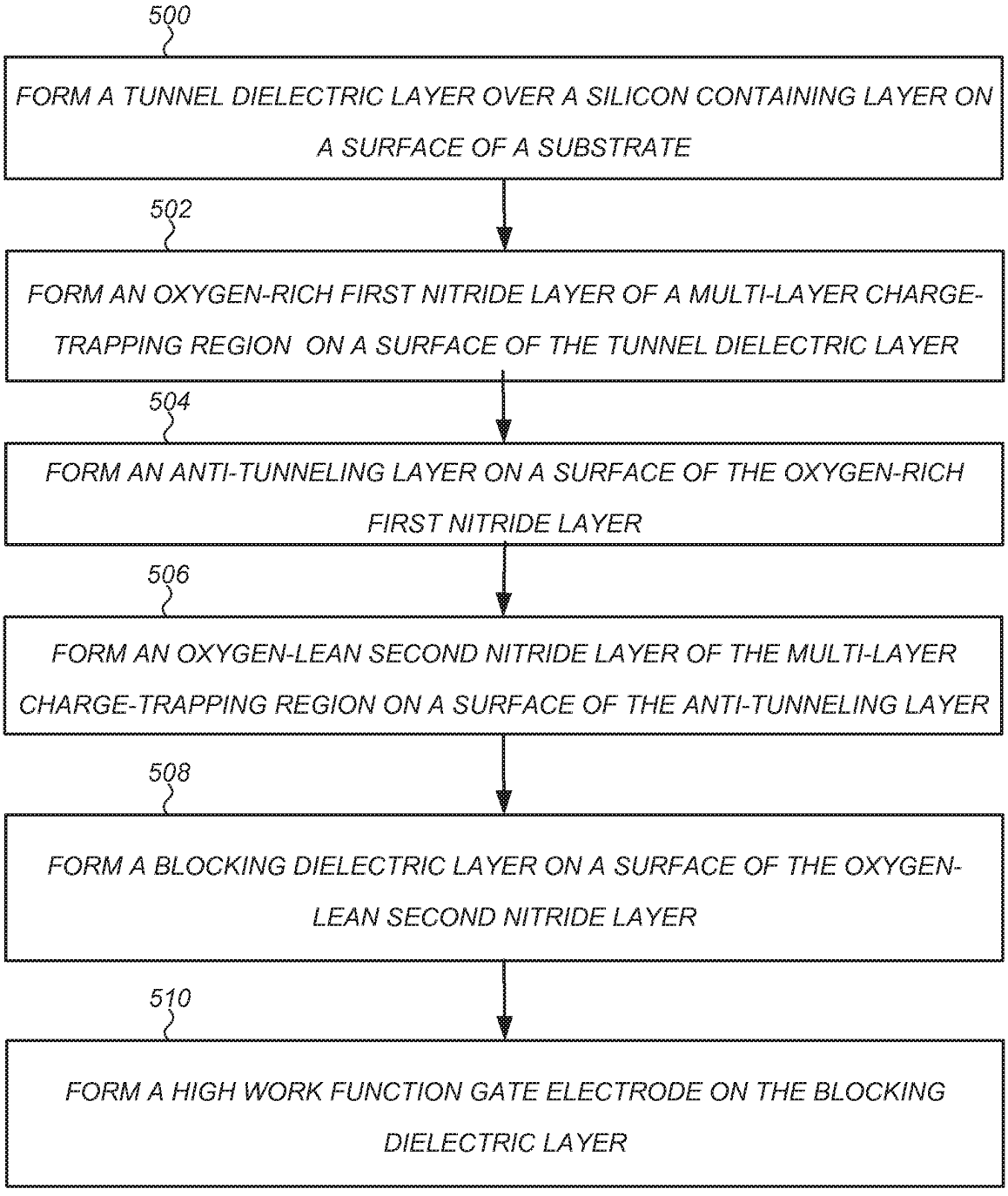

500
FORM A TUNNEL DIELECTRIC LAYER OVER A SILICON CONTAINING LAYER ON A SURFACE OF A SUBSTRATE
502
FORM AN OXYGEN-RICH FIRST NITRIDE LAYER OF A MULTI-LAYER CHARGE-TRAPPING REGION ON A SURFACE OF THE TUNNEL DIELECTRIC LAYER
504
FORM AN ANTI-TUNNELING LAYER ON A SURFACE OF THE OXYGEN-RICH FIRST NITRIDE LAYER
506
FORM AN OXYGEN-LEAN SECOND NITRIDE LAYER OF THE MULTI-LAYER CHARGE-TRAPPING REGION ON A SURFACE OF THE ANTI-TUNNELING LAYER
508
FORM A BLOCKING DIELECTRIC LAYER ON A SURFACE OF THE OXYGEN-LEAN SECOND NITRIDE LAYER
510
FORM A HIGH WORK FUNCTION GATE ELECTRODE ON THE BLOCKING DIELECTRIC LAYER

FIG. 5

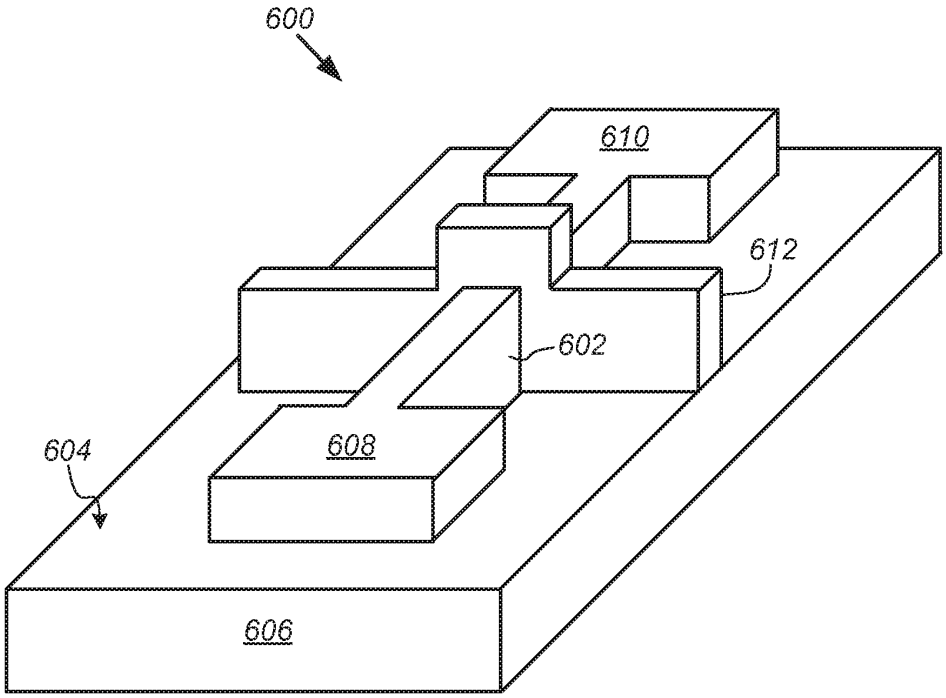


FIG. 6A

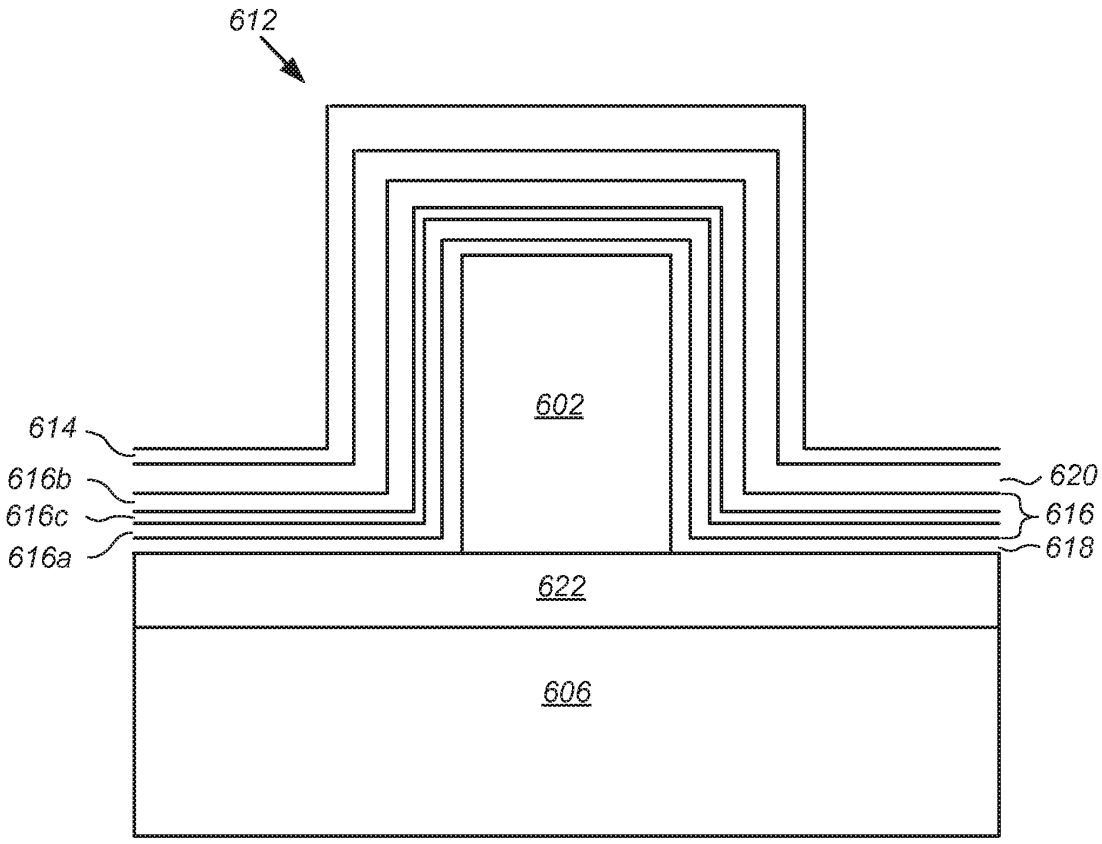


FIG. 6B

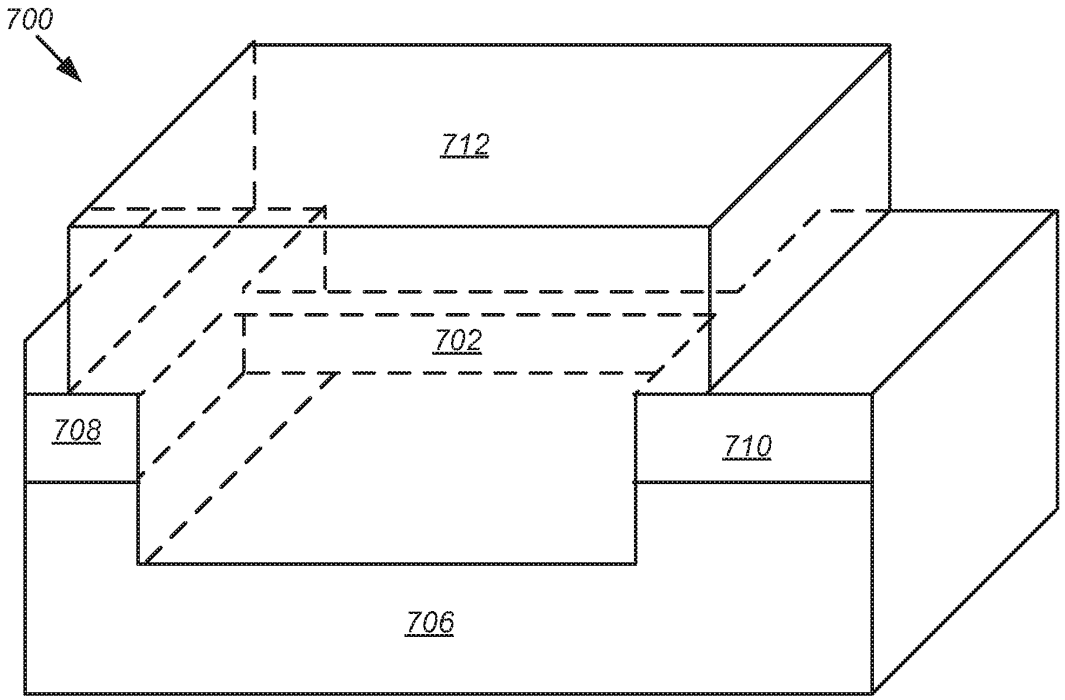


FIG. 7A

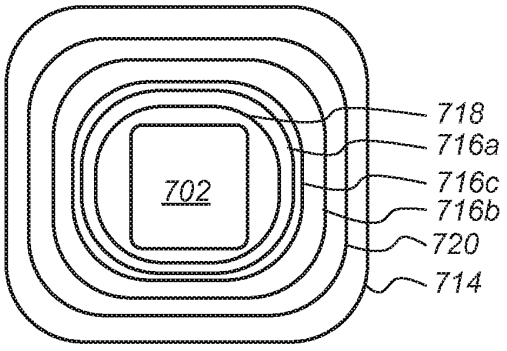


FIG. 7B

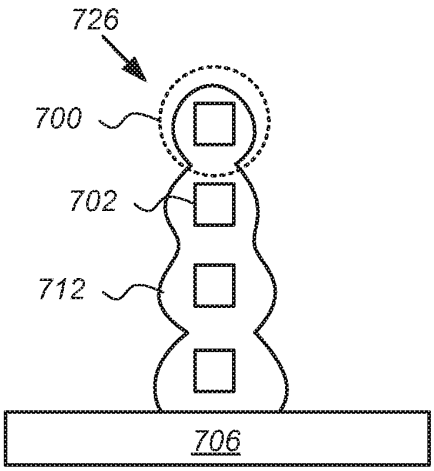


FIG. 7C

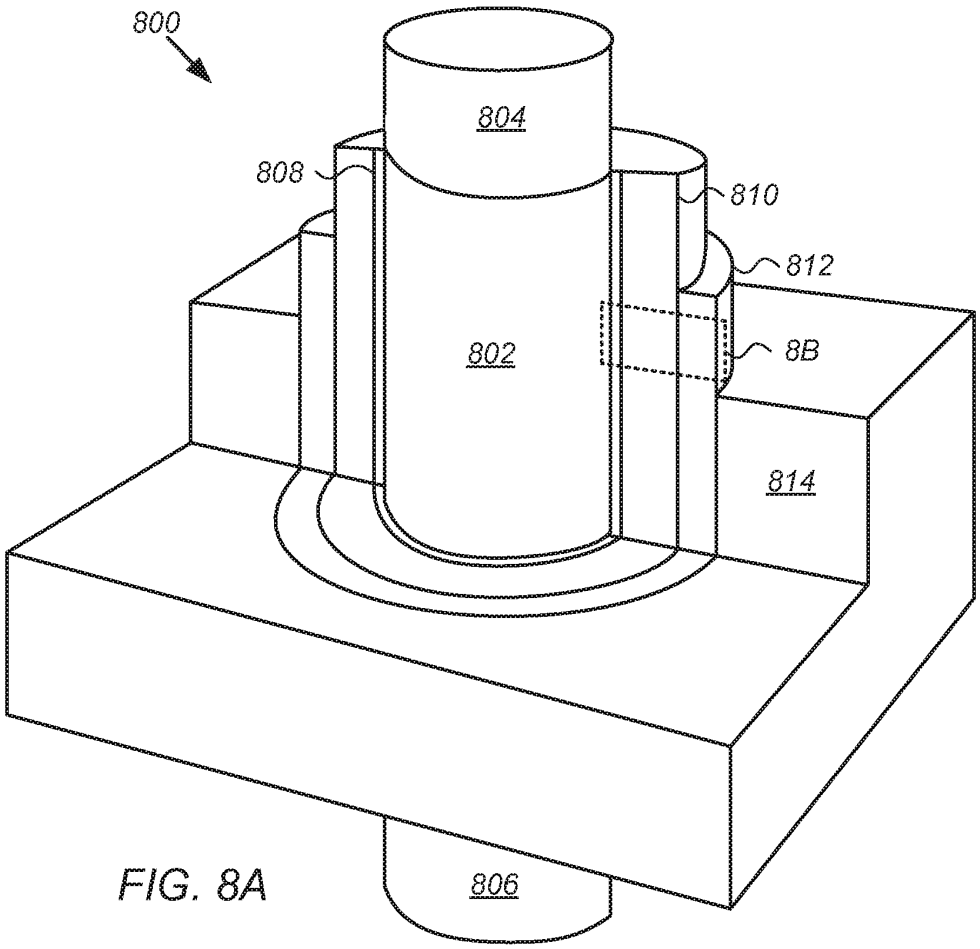


FIG. 8A

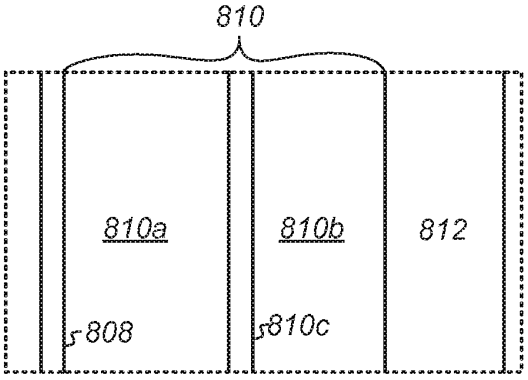


FIG. 8B

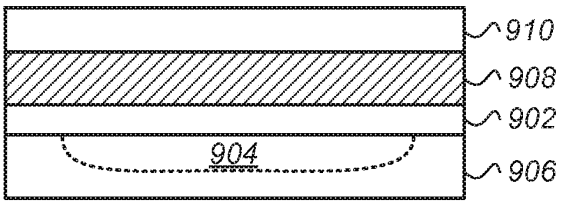


FIG. 9A

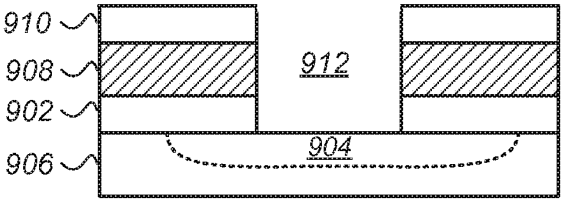


FIG. 9B

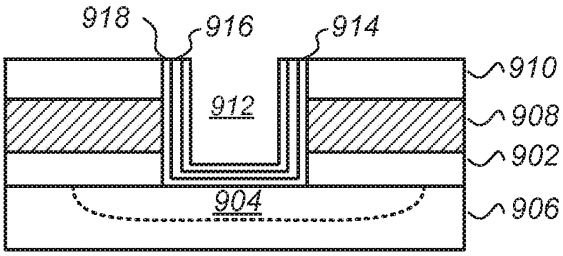


FIG. 9C

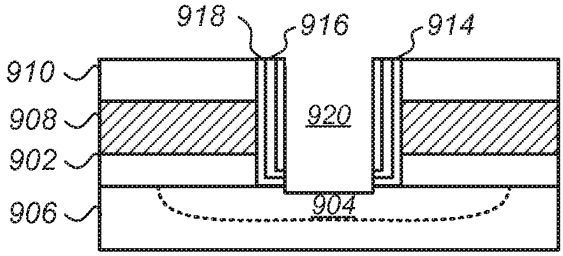


FIG. 9D

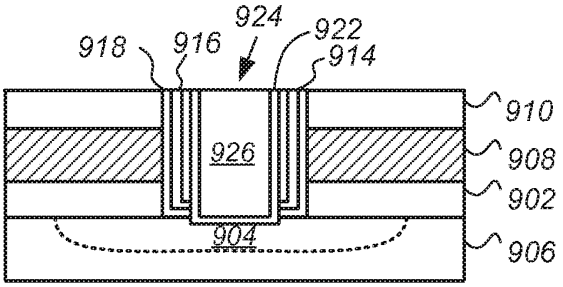


FIG. 9E

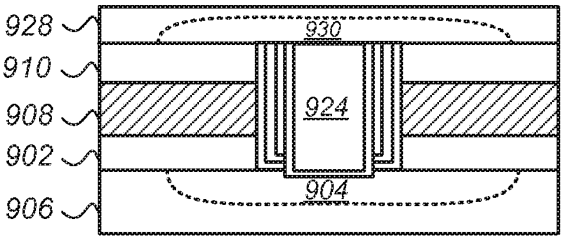


FIG. 9F

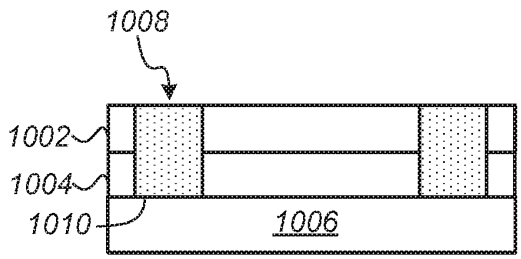


FIG. 10A

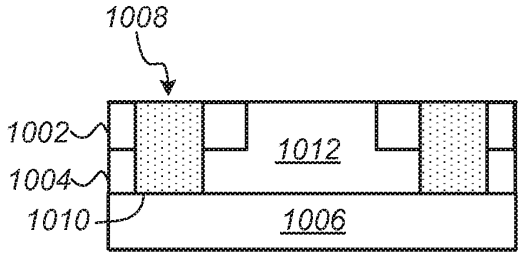


FIG. 10B

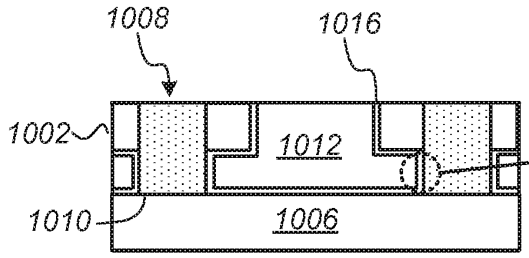


FIG. 10C

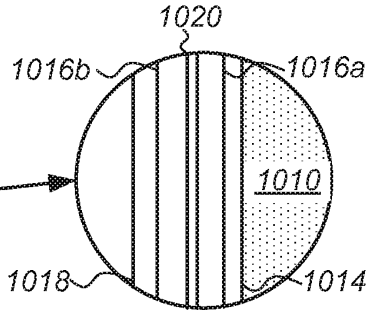


FIG. 10D

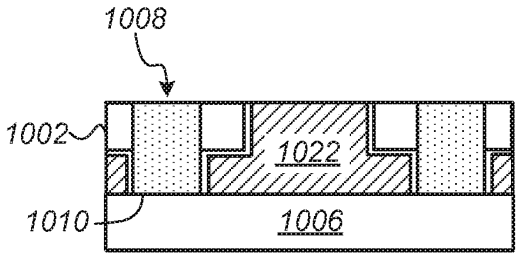


FIG. 10E

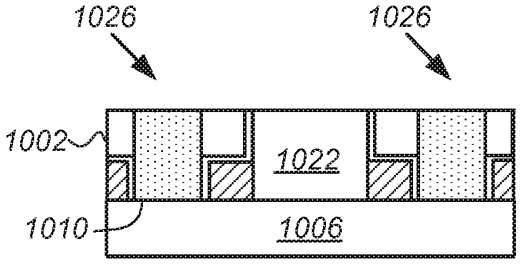


FIG. 10F

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Attorney Docket Number	PM07027D1C1

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 14/307,858 filed on June 18, 2014

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above identified application.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Krishnaswamy Ramkumar Date: 4/13/2015

Signature: Krrrrrrrr

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Attorney Docket Number	PM07027D1C1

As the below named inventor, I hereby declare that:

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LEGAL NAME OF INVENTOR

Inventor: Igor Polishchuk Date: Dec 19 2014

Signature:

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Attorney Docket Number	PM07027D1C1

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 14/307,858

filed on June 18, 2014

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above identified application.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Sagy Charel Levy Date: 4/23/2015

Signature: Sagy Levy

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	
Filing Date	
First Named Inventor	Igor Polishchuk
Title	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Art Unit	
Examiner Name	
Attorney Docket Number	PM07027D1CIP1C6

SIGNATURE of Applicant or Patent Practitioner

Signature	/Michael L. Bartholomew/	Date (Optional)	
Name	Michael L. Bartholomew	Registration Number	60225
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	LONGITUDE FLASH MEMORY SOLUTIONS LTD.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

36491

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Longitude Flash Memory Solutions Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	/Garrett Dempsey/	Date (Optional)	14 MAY 2019
Name	Garrett Dempsey		
Title	DIRECTOR		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Igor		Polishchuk	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Fremont	CA	US

Mailing Address of Inventor:

Address 1	43355 Paseo Padre Pkwy
Address 2	

City	State/Province	Postal Code	Country
Fremont	CA	94539	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sagy	Charel	Levy	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Zichron Yaakov		IL

Mailing Address of Inventor:

Address 1	44 Yigal Alon Street
Address 2	

City	State/Province	Postal Code	Country
Zichron Yaakov		03900	IL

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Krishnaswamy		Ramkumar	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

City	San Jose	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	1193 Lynbrook Way		
Address 2			
City	San Jose	State/Province	CA
Postal Code	95129	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	36491		
Email Address	docket@kba.law	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
Attorney Docket Number	PM07027D1CIP1C6	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	36491		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16429464	Continuation of	15864832	2018-01-08	10312336	2019-06-04
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15864832	Continuation of	15335180	2016-10-26	9929240	2018-03-27
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15335180	Continuation of	14811346	2015-07-28	9502543	2016-11-22
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14811346	Continuation of	14159315	2014-01-20	9093318	2015-07-28
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14159315	Continuation of	13539466	2012-07-01	8633537	2014-01-21
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13539466	Continuation in part of	13288919	2011-11-03	8859374	2014-10-14

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13288919	Division of	12152518	2008-05-13	8063434	2011-11-22
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
12152518	Claims benefit of provisional	60940160	2007-05-25		
Prior Application Status	Pending				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
	Continuation of	16429464	2019-06-03		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.					Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	LONGITUDE FLASH MEMORY SOLUTIONS LTD.		
Mailing Address Information For Applicant:			
Address 1	BRACKEN ROAD, SANDYFORD		
Address 2	FIRST FLOOR, BLACKTHORN EXCHANGE		
City	DUBLIN	**State/Province**	
Country	IE	Postal Code	D18 P3Y9
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Remove

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Michael L. Bartholomew/			Date (YYYY-MM-DD)	2021-01-25
First Name	Michael	Last Name	Bartholomew	Registration Number	60225

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/157,350	01/25/2021	1737	0.00	PM07027D1CIP1C6	1	1

CONFIRMATION NO. 6135

36491
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

FILING RECEIPT

OC000000123168380

Date Mailed: 02/05/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Igor Polishchuk, Fremont, CA;
Sagy Charel Levy, Zichron Yaakov, ISRAEL;
Krishnaswamy Ramkumar, San Jose, CA;

Applicant(s)

LONGITUDE FLASH MEMORY SOLUTIONS LTD., Dublin, IRELAND

Power of Attorney: The patent practitioners associated with Customer Number 36491

Domestic Priority data as claimed by applicant

This application is a CON of 16/429,464 06/03/2019 PAT 10903325

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/04/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/157,350**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Preliminary Class

430

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

Sandisk Technologies, Inc. - Ex. 1002, Page 000077

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/157,350	01/25/2021	Igor Polishchuk	PM07027D1CIP1C6

CONFIRMATION NO. 6135

36491
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

FORMALITIES LETTER

OC000000123168381

Date Mailed: 02/05/2021

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **320** basic filing fee.
- $ **160** surcharge.
- $ **700** search fee.
- $ **800** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1980** TOTAL FEE BALANCE DUE.

Sandisk Technologies, Inc. - Ex. 1002, Page 000079

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/jmilani/

Sandisk Technologies, Inc. - Ex. 1002, Page 000080

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/157,350	01/25/2021	Igor Polishchuk	PM07027D1CIP1C6

CONFIRMATION NO. 6135

36491
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

IMPROPER CFR REQUEST

OC000000123168360

Date Mailed: 02/05/2021

RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

Continuity, Priority Claims, Petitions, and Non-Publication Requests

In response to your request for a corrected Filing Receipt, the Office is unable to comply with your request because:

- One or more of the benefit claims under 35 U.S.C. § 120 cannot be included on the Filing Receipt since applicant did not specify whether the application is a continuation, divisional or continuation-in-part of the prior application. Applicant must submit a new application data sheet (ADS) that sets forth the relationship, and the ADS must be accompanied by a petition under 37 CFR 1.78 if filed after the time period set forth in 37 CFR 1.78.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/spkannathip/

Sandisk Technologies, Inc. - Ex. 1002, Page 000081

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/157,350

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

To: docket@kba.law,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 36491

Feb 05, 2021 04:20:43 AM

Dear PAIR Customer:

Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 36491 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
17157350	APP.FILE.REC	02/05/2021	PM07027D1CIP1C6
	NTC.MISS.PRT	02/05/2021	PM07027D1CIP1C6
	M327	02/05/2021	PM07027D1CIP1C6

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

CERTIFICATE OF TRANSMISSION
I hereby certify that this correspondence is being transmitted by either submission using the EFS WEB submission system, fax to the U.S. Patent and Trademark office to fax number 571-273-8300, or is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 to on February 22, 2021. __/Michael L. Bartholomew/__ Attorney for Applicant

PATENT
Docket No. PM07027D1CIP1C6 (3430.2.388US6CIP1)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	LONGITUDE FLASH MEMORY SOLUTIONS LTD.	
Serial No.:	17/157, 350	
Filed:	January 25, 2021	Group Art Unit: 1737
For:	**MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE**	

CORRECTION OF APPLICATION DATA SHEET

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner:

Applicant respectfully submits a corrected application data sheet. The domestic priority has been adjusted to be in the correct format and has the most recent related application at the top with the application number box left blank.

Respectfully submitted,

Date: February 22, 2021

/ Michael L. Bartholomew /

Michael L. Bartholomew
Reg. No. 60225
Attorney for Applicants

50 W. Broadway, 10th Floor
Salt Lake City, Utah 84101
Telephone: 801/994-4646

Sandisk Technologies, Inc. - Ex. 1002, Page 000085

Electronic Acknowledgement Receipt

EFS ID:	41984440
Application Number:	17157350
International Application Number:	
Confirmation Number:	6135
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	36491
Filer:	Michael Lee Bartholomew
Filer Authorized By:	
Attorney Docket Number:	PM07027D1CIP1C6
Receipt Date:	22-FEB-2021
Filing Date:	25-JAN-2021
Time Stamp:	16:30:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	PM07027D1CIP1C6_ADS-2ndCopy.pdf	131976 e83fd21a48d0eed2207e748bb9a7f7e0c1ca2d32	no	10

Warnings:

Information:					
This is not an USPTO supplied ADS fillable form					
2	Transmittal Letter	Corrected_ADS_Letter.pdf	64522 d54ec2ce48e633e169bfb186ea31583426b1a435	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	196498	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fail under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Igor		Polishchuk	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Fremont	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	43355 Paseo Padre Pkwy		
Address 2			
City	Fremont	State/Province	CA
Postal Code	94539	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sagy	Charel	Levy	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Zichron Yaakov	State/Province		Country of Residence	IL

Mailing Address of Inventor:

Address 1	44 Yigal Alon Street		
Address 2			
City	Zichron Yaakov	State/Province	
Postal Code	03900	Country i	IL

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Krishnaswamy		Ramkumar	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

City	San Jose	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	1193 Lynbrook Way		
Address 2			
City	San Jose	State/Province	CA
Postal Code	95129	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	36491		
Email Address	docket@kba.law	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
Attorney Docket Number	PM07027D1CIP1C6	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	(●) Customer Number	( ) US Patent Practitioner	( ) Limited Recognition (37 CFR 11.9)
Customer Number	36491		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16429464	2019-06-03

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16429464	Continuation of	15864832	2018-01-08	10312336	2019-06-04

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15864832	Continuation of	15335180	2016-10-26	9929240	2018-03-27

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15335180	Continuation of	14811346	2015-07-28	9502543	2016-11-22

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14811346	Continuation of	14159315	2014-01-20	9093318	2015-07-28

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14159315	Continuation of	13539466	2012-07-01	8633537	2014-01-21
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13539466	Continuation in part of	13288919	2011-11-03	8859374	2014-10-14
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13288919	Division of	12152518	2008-05-13	8063434	2011-11-22
Prior Application Status	Expired			Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
12152518	Claims benefit of provisional	60940160	2007-05-25		

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◯ Assignee	◯ Legal Representative under 35 U.S.C. 117	◯ Joint Inventor
◯ Person to whom the inventor is obligated to assign.	◯ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	

If the Applicant is an Organization check here. ☒

Organization Name	LONGITUDE FLASH MEMORY SOLUTIONS LTD.

Mailing Address Information For Applicant:

Address 1	BRACKEN ROAD, SANDYFORD		
Address 2	FIRST FLOOR, BLACKTHORN EXCHANGE		
City	DUBLIN	**State/Province**	
Country	IE	Postal Code	D18 P3Y9
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Michael L. Bartholomew/			Date (YYYY-MM-DD)	2021-02-22
First Name	Michael	Last Name	Bartholomew	Registration Number	60225

Additional Signature may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C6
	Application Number	
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This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/157,350	01/25/2021	Igor Polishchuk	PM07027D1CIP1C6

CONFIRMATION NO. 6135

36491
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

FORMALITIES LETTER

OC000000123168381

Date Mailed: 02/05/2021

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **320** basic filing fee.
- $ **160** surcharge.
- $ **700** search fee.
- $ **800** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1980** TOTAL FEE BALANCE DUE.

Sandisk Technologies, Inc. - Ex. 1002, Page 000098

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/jmilani/

Sandisk Technologies, Inc. - Ex. 1002, Page 000099

Electronic Patent Application Fee Transmittal

Application Number:	17157350
Filing Date:	25-Jan-2021
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Filer:	Michael Lee Bartholomew
Attorney Docket Number:	PM07027D1CIP1C6

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
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UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1980**

Electronic Acknowledgement Receipt	
EFS ID:	42362250
Application Number:	17157350
International Application Number:	
Confirmation Number:	6135
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	36491
Filer:	Michael Lee Bartholomew
Filer Authorized By:	
Attorney Docket Number:	PM07027D1CIP1C6
Receipt Date:	05-APR-2021
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Warnings:					
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/157,350

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
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Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/157,350	01/25/2021	1737	1980	PM07027D1CIP1C6	1	1

CONFIRMATION NO. 6135

UPDATED FILING RECEIPT

36491
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

OC000000124673182

Date Mailed: 04/07/2021

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Inventor(s)

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Applicant(s)

LONGITUDE FLASH MEMORY SOLUTIONS LTD., Dublin, IRELAND

Power of Attorney: The patent practitioners associated with Customer Number 36491

Domestic Priority data as claimed by applicant

This application is a CON of 16/429,464 06/03/2019 PAT 10903325
which is a CON of 15/864,832 01/08/2018 PAT 10312336
which is a CON of 15/335,180 10/26/2016 PAT 9929240
which is a CON of 14/811,346 07/28/2015 PAT 9502543
which is a CON of 14/159,315 01/20/2014 PAT 9093318
which is a CON of 13/539,466 07/01/2012 PAT 8633537
which is a CIP of 13/288,919 11/03/2011 PAT 8859374
which is a DIV of 12/152,518 05/13/2008 PAT 8063434
which claims benefit of 60/940,160 05/25/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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Permission to Access Search Results: Yes

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/157,350**
Projected Publication Date: 07/15/2021
Non-Publication Request: No
Early Publication Request: No
Title

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Preliminary Class

430

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Application	Document	Mailroom Date	Attorney Docket No.
17157350	APP.FILE.REC	04/07/2021	PM07027D1CIP1C6

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

Achieving Uniform nMOS Device Power Distribution for Sub-micron ESD Reliability

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Abstract

The ESD reliability of the advanced sub-micron technologies is a major concern because of the shallow LDD junctions. This paper will show that by achieving uniform power distribution during the entire ESD event in a large multi-finger nMOS device of 0.6 μm technology, protection levels in excess of 10 kV can be realized. The evidence of this uniform power distribution resulting from the multi-finger parasitic *npn* turn-on is shown through an emission microscopy analysis.

Introduction

During the past few years, advances in integrated circuit technologies towards the sub-micron feature lengths have shown considerable impact on the electrostatic discharge (ESD) protection capability. In particular, the LDD structures introduced shallow junctions leading to higher current densities during the ESD event and hence lower failure thresholds [1][2][3]. Compounding this, the use of silicided diffusions reduced the desired ballast resistance at the drain junction. This can lead to current localization and much degraded ESD levels [4][5]. Solutions such as silicide-block through mask option [6] or LDD implant dose variations can be somewhat effective but they result in either increased cost in manufacturing or a trade-off with other reliability concerns such as hot carrier effects [7][8]. However, in this paper we will show that even for an advanced 0.6 μm CMOS technology, very effective protection levels can be achieved if uniform power dissipation is implemented into the NMOS protection design.

The design of output buffer ESD protection has been the most challenging issue with the LDD/silicide technologies. Conventionally, the nMOS output transistor itself can be used as the protection device where it operates as a parasitic bipolar *npn* transistor with the drain as the collector, the substrate as the base, and the source as the emitter. Even if a large nMOS multi-finger transistor is used as the protection device, uniform conduction of all parallel parasitic bipolar devices is difficult to achieve and hence the full protection level is never efficiently realized [9]. For improved uniform conduction, a dynamic gate-coupled device, as first reported in [10], can be used. This work will illustrate the use of this technique to achieve uniform power dissipation in a 0.6 μm technology as well as report the critical design issues for the gate coupling effect.

ESD Experiments and Results

The structures studied in this work were 0.6 μm poly gate transistors of 110 Å gate oxide. The process, similar to the one described in [11], involved a boron punch-through implant followed by a phosphorous LDD implant and arsenic source-drain implants. An nMOS device cross-section and simulated doping profiles are shown in Figures 1a and 1b. As seen, the effective junction depth is nearly 0.37 μm for this technology.

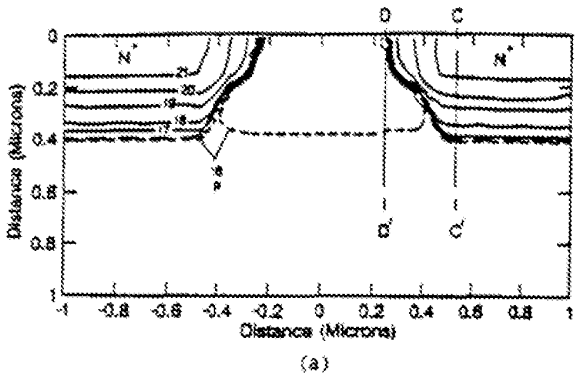
The ESD protection investigations were done on a novel gate-coupled multi-finger nMOS (GCnMOS) structure [10] schematically shown in Figure 2. The purpose of the field oxide device (FOD) is to turn off the MOSFET gate under high ESD current conditions after the nMOS gate is coupled above V_t due to the drain-gate overlap capacitance. The gate transient above V_t lowers the individual *npn* breakdown and facilitates the uniform turn-on of all fingers in a multi-finger device. This will result in a much improved ESD performance as shown below.

To demonstrate the gate-coupling effect, a monitor device, as shown in Figure 3, was built into the silicon test structure. A constant current source and a 510 Ω resistor were connected to the terminals of the monitor device. When a large pulse is applied at V_{PAD}, the gate coupling should change the conduction state of the monitor device. This is illustrated in Figure 4 where the oscilloscope traces for V_{PAD} and the drain-source voltage of the monitor device are shown for a single 1.0 μs pulse applied to the V_{PAD}. As the pad voltage increases, the coupled gate causes the effective resistance seen by the constant current source to drop, thus decreasing the measured V_{dsm}. It should be noted here that the protection nMOS is expected to go through MOS and parasitic bipolar current conduction, while the monitor device will only carry MOS current.

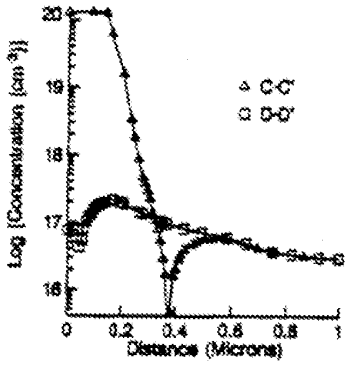
The gate coupling under ESD Human Body Model (HBM) was estimated by circuit simulation [12] of the structure depicted in Figure 3. The simulation results corresponding to a 5 kV ESD-HBM event are shown in Figure 5. The pad voltage reaches a maximum of about 25 V at 10 ns and then, with the decay of the stress

0-7803-0817-4/92 $3.00 © 1992 IEEE

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(a)



(b)

Fig. 1. (a) Cross section of an nMOS device with concentration contours given in $\log_{10}$ (atoms/cm^3); (b) doping profiles along the views indicated in (a).

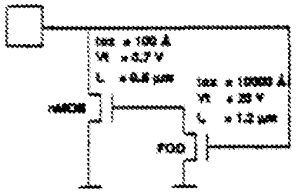


Fig. 2. Circuit Schematic of a typical GCnMOS structure.

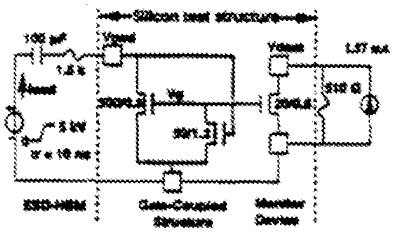


Fig. 3. Equivalent circuit used for circuit simulation of a GCnMOS structure with a built-in monitor device.

current (I_{ESD}), it approaches approximately 10 V corresponding to the bipolar snapback voltage. At the same time, the drain potential of the monitor device goes through a minimum corresponding to peak gate coupling, and slowly increases as the gate discharges. It should be noted here that with the pad voltage going beyond 20 V, the FOD in Figure 2 turns on to control

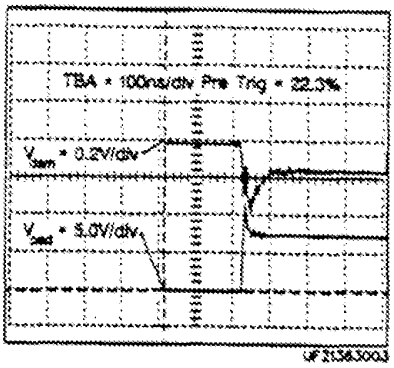


Fig. 4. Measured voltage responses to a square pulse applied to V_{PAD} for a GCnMOS structure with monitor device connected as in Fig. 3.

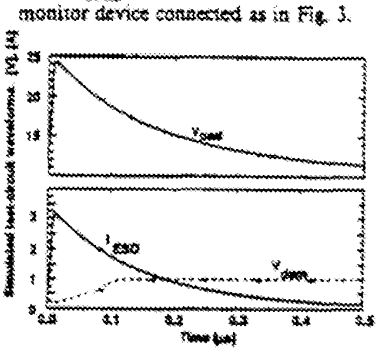


Fig. 5. Simulated waveforms for the equivalent circuit shown above in Figure 3 under a 5 kV ESD-HBM event.

the nMOS gate time constant. By matching the sim lated waveforms with the measurements, we confirm that the nMOS gate indeed goes above V_t for ES events. This should result in optimum ESD performan as mentioned above.

Several GCnMOS structures with varying layout para eters were subjected to ESD-HBM and Machine Mo (MM) stress. It was found that the drain-contact to g space (DGS) is an important parameter that increas the ballast resistance for each finger which, in turn, lows the quick trigger of all *npn* fingers in only a f nanoseconds. The measured minimum and maximu ESD-HBM failure thresholds as a function of DGS a shown in Figure 6 for 500 μm wide devices. The da corresponds to a subset of 40 GCnMOS structures. C cuit simulation results of the gate transient for the va ous values of DGS considered are shown in Figure Note that although the gate on-time in Figure 7 is abo 4 ns for all four cases, Figure 6 indicates that a tig ESD-HBM failure level distribution is attained as DG increases. It is likely that not all the fingers participate the ESD event for low DGS values. To understand th the measured breakdown I-V characteristics with squa wave current pulses are shown in Figure 8. It can be se that the gate-coupling lowers the drain avalanc

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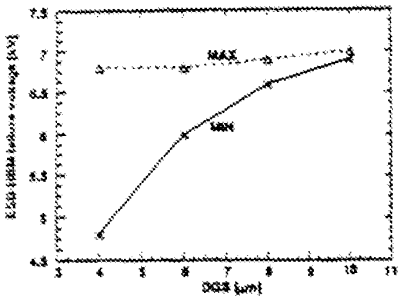


Fig. 6. Measured minimum and maximum ESD-HBM failure thresholds for 500 μm wide GCnMOS devices.

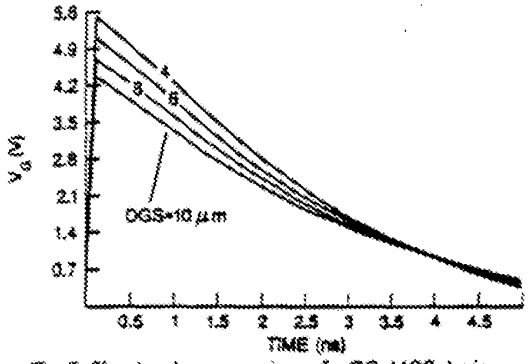


Fig. 7. Simulated gate transient of a GCnMOS device with 500 μm/0.6 μm nMOS and 50 μm/1.2 μm FOD.

close to the snapback voltage. After the first *npn* snapback, a larger DGS with higher resistance allows more of the fingers to rapidly turn on within the rise time of a typical ESD event (5–10 ns). On the other hand, this analysis also indicates that for smaller DGS values, a longer on-time is required which in turn can be controlled by the field oxide device size. Thus DGS is an important layout parameter that involves the proper gate transient design. In contrast to the GCnMOS, a grounded gate nMOS (GGnMOS), also shown in Figure 8, has to go through large voltage excursions to turn each subsequent finger. In most cases the GGnMOS reaches a failure point before even two or three fingers turn on.

The uniform power distribution in these devices was studied using emission microscopy (EMMI) [13]. First, the EMMI photograph for a 1.8 μm LDD technology GGnMOS is shown in Figure 9a. The device was being stressed with 250 ns current pulses of 500 mA. In the 0.6 μm technology, Figure 9b shows the emission photograph obtained from a GGnMOS device being stressed with 450 mA current pulses. In both cases, only one finger "locks-on" which can lead to failure corresponding to a single finger device. In some cases of the 0.6 μm technology, however, 2 or 3 fingers were seen to turn on but this was always a random event. The GCnMOS device emission results are shown in Figure 10. As the current level was increased from Figure 10a (100 mA) to

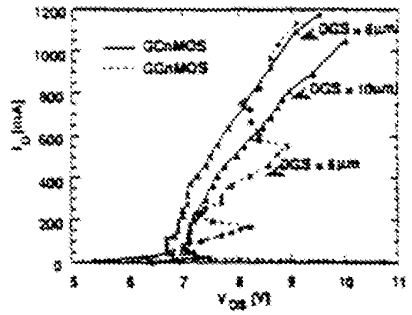


Fig. 8. Measured I-V breakdown characteristics.

Figure 10c (500 mA), more and more fingers turn on until all eight fingers participate in the event. It is important to note that, unlike the GGnMOS case, lock-on with a single finger dominating does not occur. Even in a sixteen finger device all of the fingers can participate as shown in Figure 10d. This sixteen finger device has shown an ESD failure level of 13 kV or 13 V/μm for this 0.6 μm technology. Thus, the emission results clearly illustrate that uniform power distribution can be achieved with optimum gate coupling. A floating gate device without the field oxide device was also studied under EMMI at the same current levels. No emission was observed indicating that the nMOS device conduction dominates in this case.

Conclusions

This paper demonstrated the effect of dynamic gate coupling for sub-micron ESD protection structures and the impact it has in obtaining more than 10kV of ESD-HBM performance. It was shown that the optimum gate transient is a critical function of the nMOS protection device layout parameters. Using emission microscopy, this work also has demonstrated that for sub-micron technologies excellent ESD levels can be obtained when uniform power distribution is achieved through gate-coupling in a multi-finger nMOS device. For future technologies thus harnessing the maximum available *npn* protection can become a key ESD reliability advantage.

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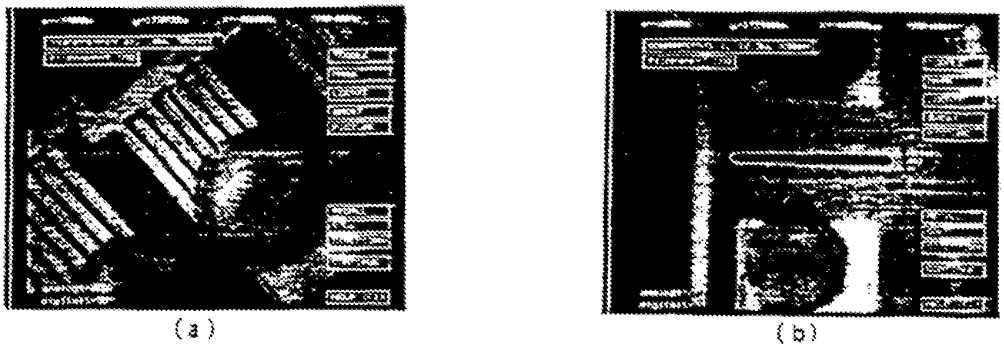


Fig. 9. EMMI photographs of GGnMOS devices in the (a) 1.2 μm technology at 500 mA stress current level and (b) 0.6 μm technology at 450 mA stress current level.

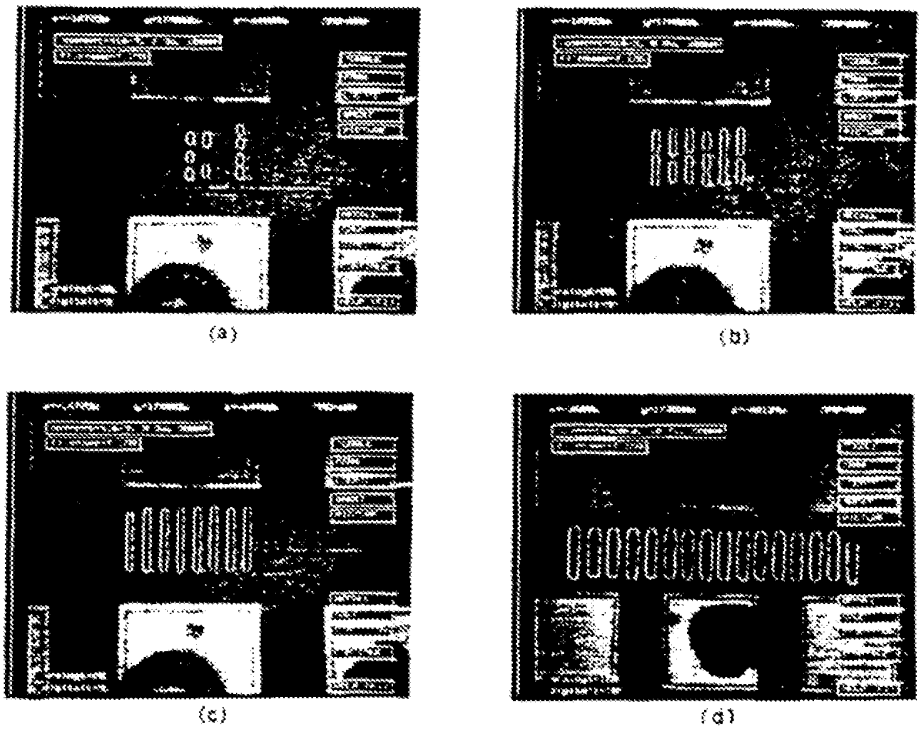


Fig. 10. EMMI photographs of GCnMOS devices in the 0.6 μm technology: (a), (b), and (c) are for a 500 μm device being stressed with 100 mA, 300 mA, and 500 mA current pulses, respectively; (d) shows a 1000 μm device subjected to 500 mA current pulse.

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AIP Applied Physics Letters

High-performance gate-all-around polycrystalline silicon nanowire with silicon nanocrystals nonvolatile memory

Min-Feng Hung, Yung-Chun Wu, and Zih-Yun Tang

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High-performance gate-all-around polycrystalline silicon nanowire with silicon nanocrystals nonvolatile memory

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Nonvolatile memory (NVM) that is based on gate-all-around (GAA) and polycrystalline silicon (poly-Si) nanowires structure with silicon nanocrystals (NCs) as the storage nodes is demonstrated. The GAA poly-Si–SiO_2–Si_3N_4–SiO_2–poly-Si (SONOS) NVMs are also fabricated and compared. The GAA NCs NVMs have a 4.2 V of threshold voltage shift at 18 V for 1 ms, and are faster than the GAA SONOS NVMs do. In reliability studies, this NVM shows superior endurance after 10^4 program/erase (P/E) cycles, and loses only 14% of its charges lose after ten years at 85 °C. © *2011 American Institute of Physics*. [doi:10.1063/1.3582925]

Flash memory, an nonvolatile memory (NVM), is extensively adopted in portable products owing to its high density and low cost.[1] Recent efforts have witnessed the aggressive scaling down of flash memory, which follows Moore's law, making device fabrication increasingly difficult. Three-dimensional (3D) multilayer-stack memory based on poly-Si thin-film transistor (TFT) has subsequently been introduced for ultrahigh-density memory.[2,3] As has been well established, the multigate nanowires (NWs) structure significantly improves the performance of flash memory, and has been exploited in FinFET,[4] Trigate,[5] Pi-gate,[6] and even gate-all-around (GAA), for example.[7,8] The GAA structure has the highest electric field in the tunneling oxide, and therefore the highest program and erase speed. Nanocrystals (NCs) that were embedded in flash memory provide several advantages, including low-voltage operation, elimination of the drain-induced turn-on effect, elimination of the floating gate coupling effect, and reduction in stress induced leakage current effect. Accordingly, various NCs materials, including Si,[9,10] Ge,[11] metal,[12] and dielectrics[13] have been embedded in flash memory devices. Silicon NCs promote high P/E efficiency owing to their narrow bandgap, deep conduction band. Moreover, they are highly compatible with the current flash memory process and absence of metal contamination.

This investigation studies a poly-Si NWs NVM with GAA structure and Si-NCs electron storage nodes. The performance and reliability of this Si-NCs GAA NVM is compared with that without Si-NCs [poly-Si–SiO_2–Si_3N_4–SiO_2–poly-Si (SONOS) GAA NVM].

Figure 1 schematically depicts the GAA poly-Si NWs Si-NCs (GAA NCs) NVM device. An NW is magnified to show the hybrid Si-NCs. The thickness of each layer is marked in NW. Figure 2(a) is the high-resolution transmission electron microscopy (TEM) image of one NW. The poly-Si channels are in a rectangular shape surrounded by n^+ poly-Si gate to form the GAA structure. The width and height of the NWs are 60 and 25 nm [the effective width of the NW (W_{eff}) is 170 nm]. Figure 2(b) shows the top view of the Si-NCs surround by Si_3N_4. The diameter of the NCs is around 3 to 7 nm.

The GAA NCs NVMs devices were fabricated on a 6 in. silicon wafer with a 400-nm-thick thermal dioxide layer. A layer of 40-nm amorphous silicon (α-Si) deposited by low-pressure chemical-vapor deposition (LPCVD) at a temperature at 550 °C, followed by treating solid-phase crystallized process at 600 °C for 24 h in nitrogen ambient. The active layer with NWs was defined by electron beam (e-beam) and transferred by reactive ion etching. The samples were dipped in buffered oxide etch solution for forming suspending NWs. The tunneling oxide, nitride, amorphous Si (α-Si), and nitride are grown and deposited sequentially by LPCVD. Then the sample is annealed in high temperature to form the NCs. The 200-nm-thick *in situ* doped N^+ poly-silicon was deposited as a gate electrode, and patterned by e-beam and reactive ion etching (RIE). Finally, the standard passivation and metallization were performed. A control sample, SONOS NVM

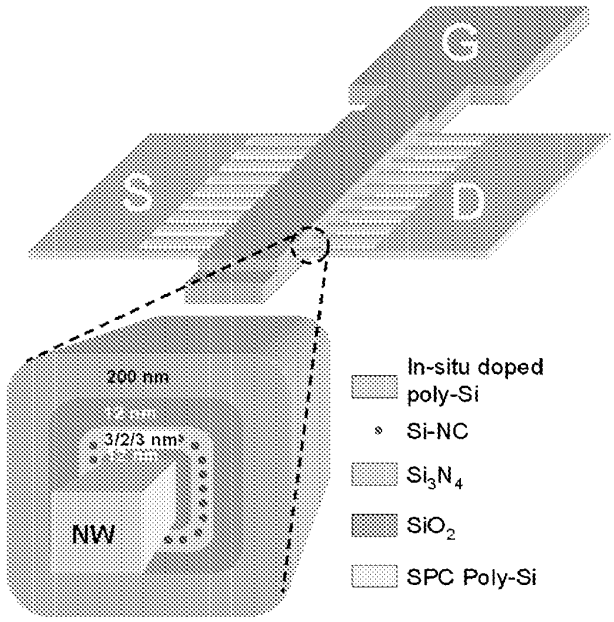


FIG. 1. (Color online) GAA poly-Si NWs NVM device, showing magnified NW, thickness of each layer, and Si NCs.

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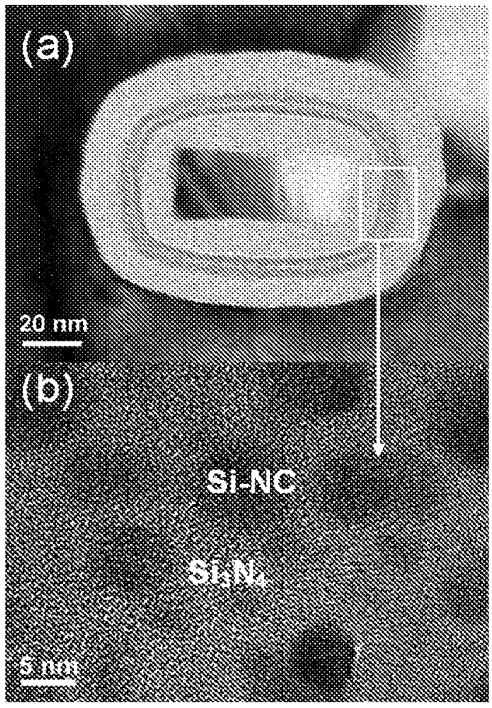


FIG. 2. (a) TEM image of one NW of the GAA poly-Si NWs NVM device with NCs. (b) TEM top view image of the Si-NCs surrounded by Si_3N_4. The diameter of the NCs is around 3 to 7 nm.

with the same GAA structure, was also formed as the above processes except the processes to form the hybrid Si-NCs. The thickness of the Si_3N_4 is 8 nm.

Figure 3 shows programming and erasing characteristics of the GAA poly-Si NWs NVM devices with and without NCs. Our tunneling oxide in this work is relatively thick, which is 12 nm at the edges and 9 nm at the corners. Thanks to the GAA structure enhancing the electric field in tunneling oxide,[14] the programming voltage is acceptable and similar with other papers, such as the Ref. 15 and 16. Additionally, four corners of the rectangular NWs enhance the electric field. Notably, the NCs NVM were programmed and erased faster than the SONOS NVM. The interface between NCs and nitride contains numerous trapping sites, which can store the tunneling charges.[17,18] Moreover, the Si NCs have deep conduction and valence bands. The tunneling distance for

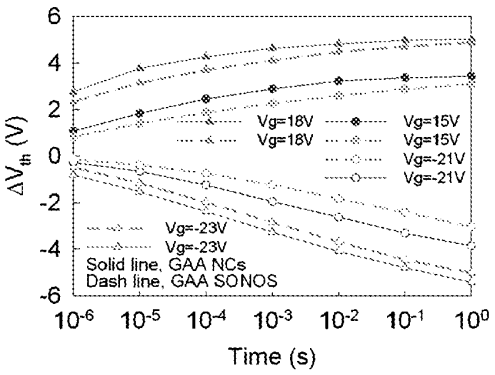


FIG. 3. (Color online) Program/erase characteristics of the GAA NCs and GAA SONOS NVM.

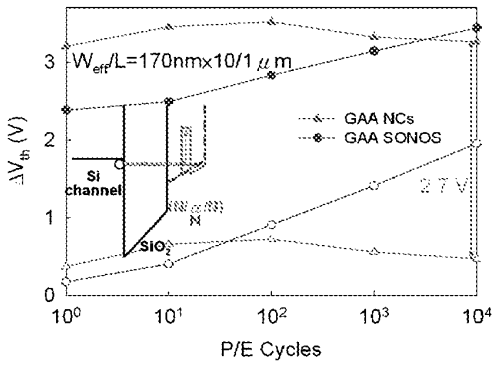


FIG. 4. (Color online) Endurance characteristics of the GAA NCs and GAA SONOS NVMs. The band diagram in erasing condition is embedded in figure.

both the electron and hole in NCs device is shorter than that in the SONOS device, so the former device has a higher electron/hole tunneling probability than the latter device.

The GAA structure enhances the electric field in the tunnel oxide, and therefore raises an issue of reliability. Figure 4 plots the endurance characteristics of the GAA NCs and GAA SONOS NVM devices. The programming and erasing conditions are V_g=15 V for 1 ms and V_g=−23 V for 0.1 s, respectively. The memory window of the GAA NCs NVM device barely decreases and shifts during 10k P/E cycles. The GAA SONOS device, however, exhibits significant upward shifting of the threshold voltage during 10k P/E cycles. These results can be explained as follows. First, the NCs device has a higher hole tunneling current because the tunneling depth therein is lower than in the SONOS device. The inset in Fig. 4 presents an energy band diagram of the NCs and SONOS NVM devices during erasing. Second, high density deep-traps in the interface and NCs capture the tunneling charge.[17,18] Most of the electrons and holes are trapped in the NCs or the interface; therefore, the tunneling holes can efficiently recombine with stored electrons.

Figure 5 shows the retention characteristics of GAA poly-Si NWs NVM device with Si-NCs and an Si_3N_4 trapping layer at 85 °C. By extrapolation at ten years, the memory window of the GAA Si-NCs NVM device remains 86% of its initial value, while that of GAA SONOS NVM remains 79% of its initial value. The GAA NCs NVM has better retention because of the deep conduction and valence bands of the Si NCs. Most of the injected charge can be

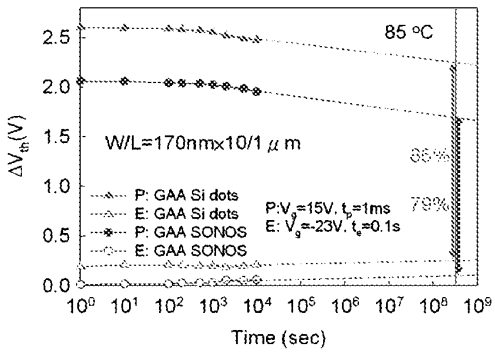


FIG. 5. (Color online) Retention characteristics of the GAA NCs and GAA SONOS NVMs.

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stored in NCs or in the interface between NCs and Si_3N_4.[17,18] The trapped charges in Si_3N_4 can also be redistributed to NCs by trap-assisted tunneling at high temperature. Therefore, most of the stored charge can be concentrated in a deep level of NCs.

In conclusion, with the same GAA structure, the NVM with NCs program and erase faster than the SONOS NVM does because of the high deep-trap density in NCs and short tunneling distance of charges to NCs. Furthermore, the use of Si NCs improves the endurance and retention of the device. The program and erase voltages can be further reduced by thinning the thickness of the tunneling oxide and the blocking oxide. The fabrication of a GAA NVM device is simple and highly compatible with the current flash process. This investigation would examine the NWs poly-Si TFT memories on future 3D stacked high-density applications.

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DISCLOSURE TITLE: Algorithm for Managing Multiple First-in, First-Out Queues From a Single Shared Random-Access Memory

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DISCLOSURE TEXT:

- In the following, a technique is described for efficiently managing a plurality of first-in, first-out (FIFO) queues in a single shared random-access memory (RAM). This technique obviates the necessity for garbage collection procedures, i.e., operations to reorganize memory containing scattered records and to gather unused memory cells.
- FIFO queues can be implemented in a RAM, with associated control to maintain the head and tail pointers of each queue. When the requirement arises to implement multiple FIFO queues, the classical approach is to accomplish some physical or logical separation of the RAM and have each queue implemented in such a partition. The total required memory is then the sum of these partitions. The size of a partition is determined by the estimated maximum (or average) queue size for a particular queue. A disadvantage of this method is that the collection of queues can not effectively share the whole RAM. It is, for example, not possible that a queue which temporarily exceeds its allocated space 'steals' some RAM space from a queue which is not using its allocation. In general, this leads to a waste of RAM space, because every partition is sized for its maximum expected length.
This implementation is
denoted as the fixed partitioned case.
- From some operating systems, examples of queues implemented in shared RAM are known. However, the algorithms usually require a 'garbage-collection' operation to reorganize fragmented memory after some period of operation. These garbage collection operations are not suited for implementation in hardware.
- An algorithm is proposed which allows a full sharing of the total available RAM space among a set of queues. An extension to this algorithm is given which guarantees for every queue a certain amount of 'private' space. The proposed algorithm does not require garbage collection, and, therefore, lends itself easily for hardware implementation. Key to the algorithm is that the collection of not

occupied cells in the shared RAM is treated as an extra queue: for every element which leaves one of the data queues, this 'empty-queue' grows by one element, and for every element which enters one of the data queues, the empty-queue shrinks by one element.

- In the figure, a hardware implementation of the algorithm is shown. The shared data RAM 19 contains the queue elements. The n_part RAM 20 together with the data RAM 19 forms a linked list for every queue. In the n_part RAM 20 the address of the next element in a queue is found on the same address where the current element in that queue is stored. Thus, whenever an element is taken from a queue, the corresponding n_part entry points to the next element in that queue. A reading of zero indicates that the queue is empty. This holds also for the 'empty-queue', and therefore the n_part RAM 20 is initialized such that the contents of every address i point to the next address in the n_part RAM: i+1. Only the last position in the n_part RAM contains the value zero, and when this is read, there is no free data RAM 19 location left.
- Whenever data is put into the data RAM 19, the corresponding value of the n_part RAM 20 points to the next free location in the data RAM 19. This reading is saved in the *n_nf* register 17.
- For an initial description of the operation, disregard the Config. Mem. 9 and the nf RAM 25. Input data to queue:

Assume that input counter (inp.cnt.) 1 selects to add an element to queue 'q'. Selector 7 will select the value of the counter to select the proper queue index in the qi RAM 3 and qo RAM 6. The qi RAM 3 contains a pointer to where the last element was added to this queue. If the value is zero, this queue has currently no elements. If the value is non-zero, then comparator 14 will be used to select the value of u_nf by selector 21, and address qi(q) by selector 16, to write the pointer to this added element to the chained list for this queue. The *nf_c* register 27 holds the address where the data element is to be stored. This value is latched through selector 24 in u_nf register 23.

If the value of nf_c
register 27 is zero, then the data RAM is full, and a FULL is signalled by comparator 28.

- At the selected address 'q' in the qi RAM 3 the value of u_nf will be written, selected by selector 2. Because there is no next element in this queue, at the corresponding address (u_nf) in the n_part RAM 20 the value zero is written. The address is selected by selector 16, the data by selector 21. Before this write occurs, the value of the addressed location in the n_part RAM 20 is saved in n_nf register 17. This value points to the next free location in the data RAM 19, and is used as the next value nf_c. At the end of the input cycle, this value is selected by selector 26 and written to nf_c register 27.
- At the same time, the output-chain for this queue is to be started, and qo RAM 6 points to the next element to be output for this queue. Only if qo(q) is zero, this qo(q) is set to u_nf. Address to qo RAM 6 is 'q', and data is selected by selector 5.
- This completes the input cycle. The following has taken place: qi(q) has been set to the address in the data RAM where this element was written. The old value of qi(q), when not zero, was used to write the pointer in the n_part RAM to the added element, thereby forming

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the chained pointer list. The value of n_part where the new element was written is used as the address for writing the next element (for any queue) in the data RAM. This entry in n_part is set to zero, to indicate the end of this queue. When qo(q) was zero, it is set to the address where this data element was stored. qo(q) is a pointer to the next element output from this queue.

- Output data from queue: Assume the output counter (out cnt.) 8 determines a queue number 'q' from which an element is to be read. Selector 7 selects the proper counter to provide the address 'q' for the qi RAM 3 and qo RAM 6. When the addressed value qo(q) is equal to zero, comparator 11 will flag EMPTY and the cycle is done.
- When this is not the case, selector 18 will select qo(q) as the address to be read, and the data is fetched from the data RAM 19. The next element in this queue is obtained from the corresponding value n_part(qo(q)) in n_part RAM 20. Selector 5 selects this value to be set into qo RAM 6. This value can be zero when there are no more elements in this queue. If this value is zero, then comparator 4 instructs to set qi(q) to zero. The original value of qo(q) is temporarily stored in qo_temp register 10. This value is now used to set the corresponding address in the n_part RAM 20 to the current value of u_nf. (For this case equal to nf_c). The cycle is finished by setting nf_c to the value stored in qo_temp register 10.
- This completes the output cycle. The following has taken place: The data item pointed to by qo(q) has been fetched from data RAM 19. If there was no next item in this queue, qi(q) has been set to zero to indicate that there are no elements in this queue for a subsequent input operation. The value of qo(q) has been set to point to the next item in the list (or zero). This pointer was obtained from the corresponding qo(q) address in the n_part RAM 20. The corresponding n_part RAM entry was set to point to the next empty location in the data RAM 19 which was obtained from u_nf. The value of nf_c has been set to the address of the just read location. Note that the 'next-free' queue is thus a sort of last-in, first-out (LIFO) queue. This ensures that if the value of u_nf is zero, there are really no empty locations in the data RAM 19.

Additional Features:

In the proposed algorithm it is possible that one of the queues in the system monopolizes the whole data RAM 19 space at the cost of the other queues. There is no effective mechanism to guarantee a minimum queue length for each queue. The additional elements in the figure, namely: nf RAM 25, Config.Mem. 9, comparators 12 and 13, and selectors 22 and 24 are used to guarantee each queue a minimum queue length at all times.

- The basic mechanism is to put some zero entries in the n_part RAM 20 and to implement a next-free pointer for every queue plus one, the last one being the next-free pointer in the 'common queue area'.
- The following example is used to clarify this operation:

Assume there are two queues, with a minimum queue length of 5 and 3 elements, respectively. The rest of the data area is common queue memory from which each queue can claim space, as required.

- The following shows the initialization of n_part RAM 20, Config. Mem. 9, nf RAM 25, and nf_c register 27:

n_part(0) = 1 Config.Mem.(0) = 6

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n_part(1) = 2 Config.Mem.(1) = 10
n_part(2) = 3
n_part(3) = 4 nf(0) = 0
n_part(4) = 5 nf(1) = 7
n_part(5) = 6
n_part(6) = 0 nf_c = 11
n_part(7) = 8
n_part(8) = 9
n_part(9) = 10
n_part(10) = 0
n_part(11) = 12
n_part(12) = 13
etc.

- Instead of selecting the nf_c pointer for every input to a queue, the 'private nf pointer' for a queue is selected from nf RAM 25 first. If this renders a value of zero, comparator 12 will detect so, and on input to a queue then the common queue memory nf_c pointer 27 is selected to set u_nf (23). If both 25 and 27 are zero, then there is no possibility to add an entry to this queue. This means that the private queue space and the common queue space are full. The difference is, however, that for another queue there can be space left in its private queue space, and it is possible to add an entry there.
- When, on an output cycle, the value returned by qo RAM 6 is greater then the fixed value in the Config.Mem. 9 for this queue, then comparator 13 will detect so, and the nf_c pointer 27 is selected to partition in the output cycle. Overhead

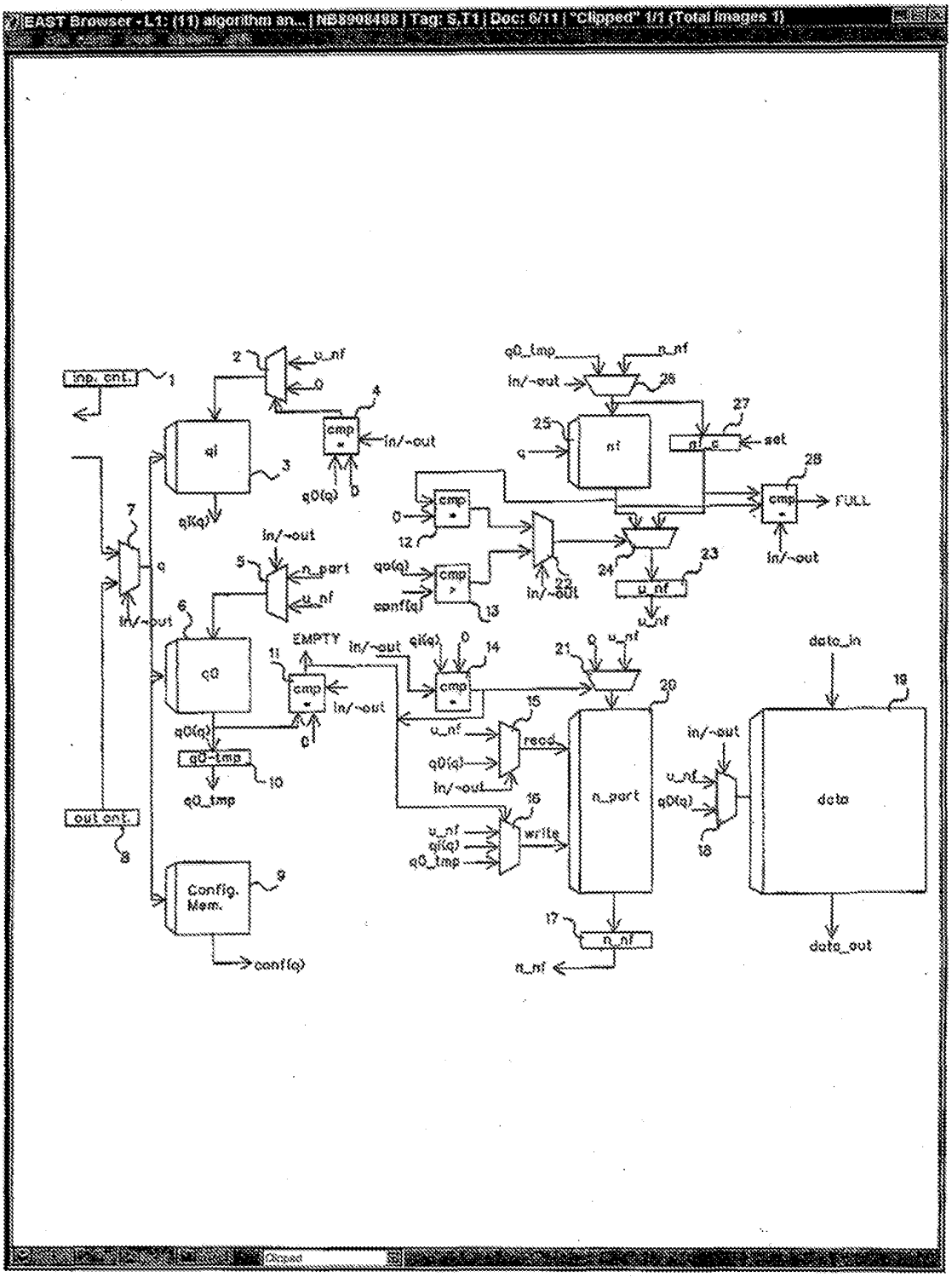
Compared to the simple case of fixed partitioning of the data RAM 19, the n_part RAM 20 is the only additional resource required. The qi RAM 3, qo RAM 6, and Config.Mem. 9 are also required to handle the pointer management in the fixed (or semi-fixed) partitioned case. The size of n_part RAM 20 is determined by the following parameters: 1) it needs the same amount of addresses as there are entries in the data RAM 19. 2) its width must be enough to accommodate the addressing of all the entries of the data memory.

- Example: If the data RAM 19 has 1024 entries (of any given size), then the n_part RAM 20 is 10 bits wide and has 1024 entries.
- It is estimated that the additional selectors and comparators shown in the figure are comparable to those of the fixed partitioned case.

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inp. cnt.
out cnt.
qi
q0
nf
n_part
data
Config. Mem.
cmp
in/~out
q0(q)
qi(q)
conf(q)
q0_tmp
n_nf
u_nf
set
reset
write
EMPTY
FULL
data_in
data_out

A SINGLE POLY EPROM FOR CUSTOM CMOS LOGIC APPLICATIONS

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Fremont, California 94538

Abstract

A non volatile memory element which employs a single floating polysilicon gate is described. The cell comprises of a floating gate n-channel transistor and a control gate. The control gate is an n-well which is capacitively coupled to the floating gate. No additional process steps are required to implement this cell in an n-well CMOS technology. The single poly EPROM is programmed by channel hot carrier injection into the floating poly similar to a conventional EPROM. The cell is erased by exposure to UV light. A P^+ region is formed on a portion of the well to prevent the well-floating gate capacitor from going into deep depletion and, therefore, to enhance the gate coupling and AC response. The single poly cell is implemented in a 2Kx8 array employing standard EPROM array architecture.

Introduction

Application Specific Integrated Circuits (ASIC) have become a rapidly growing section of the semiconductor market in the past few years. The availability of EPROMs enhances the power of application specific chips to a large degree. The key point in implementing EPROM cells on custom chips is to maintain the process simplicity and, therefore, to keep the manufacturing costs low. Fabrication of conventional EPROMs usually requires two layers of polysilicon. As a result, implementation of double floating gate EPROM on custom chips complicates the process, degrades the yield, and increases the manufacturing costs.

The present paper describes a single poly EPROM as an alternative for custom CMOS logic applications. Fabrication of the single poly EPROM requires no additional processing steps in n-well CMOS process. As a simple extension of CMOS process this memory cell can be applied in a memory array, programmable logic array, or incorporated in a standard cell CMOS library.

The single poly EPROM can also be used as a redundancy element in DRAM, SRAM, and ROMs. Other applications of this cell are chip trace and trimming analog circuitry.

Cell Structure and Fabrication Technology

Cross section of the cell is shown in Figures 1(a) and 1(b). The floating polysilicon gate extends over an n-well and forms the gate coupling area. The n-well is used as the control gate during programming and read. The coupling between the control gate (n-well) and the floating gate is designed by selecting the ratio between the area of the floating gate over the n-well to the area of the floating gate over the channel.

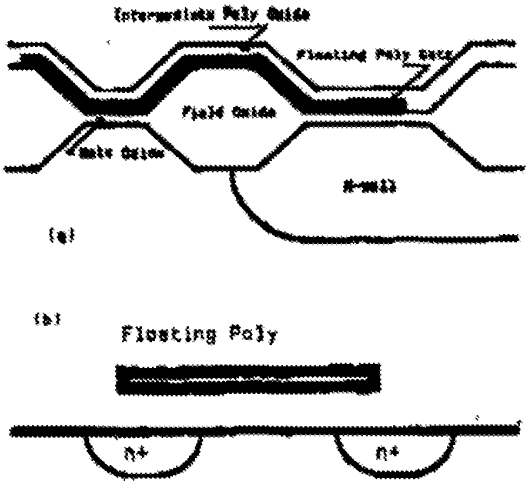


Fig. 1. The cross sections of the single poly EPROM.

A cross section of the gate coupling area is shown in Figure 2(a). In this structure, when the control gate (n-well) is pulsed high the floating poly to n-well capacitance goes into deep depletion and the gate coupling is strongly reduced. To overcome the "deep depletion" problem, a P^+ region is formed on part of the gate coupling area, as shown in Figure 2(b). The P^+ region in this structure provides a source of minority carriers (holes) which prevents the floating poly to n-well capacitance from going into deep depletion when the n-well is raised high. The layout of the cell with the additive

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of the P+ layer is shown in Figure 3. The word line is formed by the n-well which is the control gate of the single poly EPROM. The cell area in the array is 150μ.²

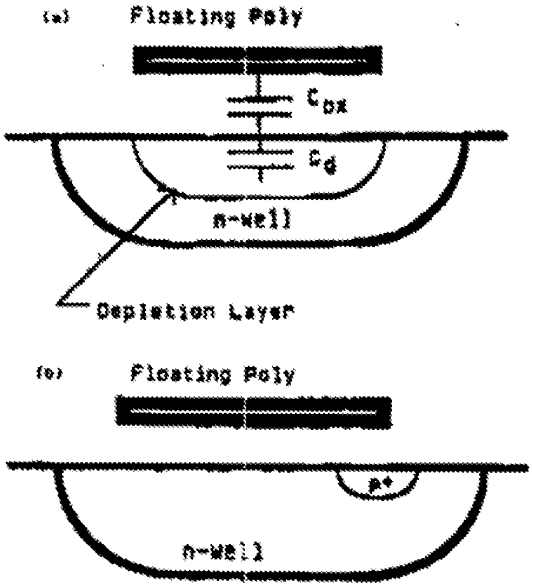


Fig. 2. Cross section of the gate area. (a) deep depletion capacitor, (b) added P+ layer.

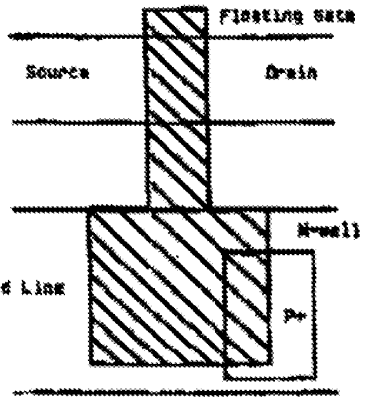


Fig. 3. Cell layout

Single poly EPROM cells are fabricated in a n-well CMOS process on P⁻-epi wafers. The key process features are presented in Table I. Conventional locos isolation and self aligned source/drain process are used. The single poly EPROM has the same gate oxide and source/drain junctions as NMOS devices. The gate coupling oxide is grown at the same time as the gate oxide. No additional process steps are implemented to fabricate the memory cells. The typical cell has a minimum effective channel length at 1.2μm.

TABLE I

L_{eff} (min)	NMOS	1.2μm
L_{eff} (min)	PMOS	1.2μm
L_{eff} (min)	EPROM	1.2μm
Gate Oxide	275Å	
Field Oxide	7000Å	
Intermediate Oxide	~300Å	
Junction depth	N+	0.35μm
Junction depth	P+	0.50μm
Junction depth	n-well	4.0μm
Typical cell size		150μm²

Performance

The I_D-V_D characteristics of the fabricated EPROM cells is shown in Figure 4. The initial threshold voltage of the cell is mainly controlled by the gate coupling. The cell read current becomes larger with increasing the effective gate coupling. The typical cell with a 1.2μm effective channel length and 36μm² gate coupling area has an initial threshold of 1.9 volts and a read current of 220μA.

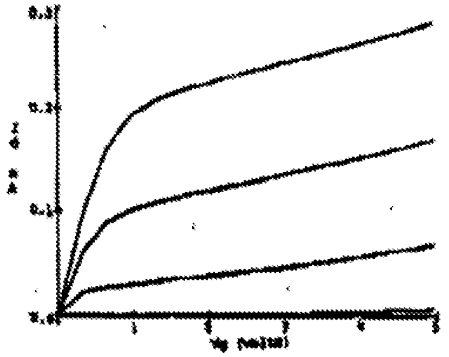


Fig. 4. Cell I_DV_D characteristics

The effect of coupling area on both I_R and V_{T1} is shown in Figure 5(a), 5(b). Initially, the I_R increases with gate coupling area as the V_{T1} decreases. Both I_R and V_{T1} become less sensitive to gate coupling as the gate area becomes large and gate coupling approaches unity. The cell read current, however, can be increased to desired level by adjusting the device width.

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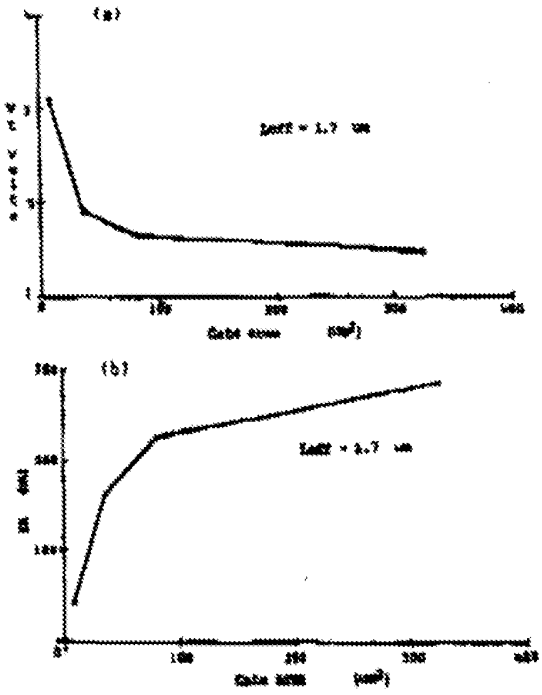


Fig. 5. Effect of gate coupling area on, (a) initial threshold voltage, (b) read current.

The single poly EPROM is programmed by channel hot carrier injection as the control gate and drain are simultaneously raised high. The programming rate is primarily controlled by the effective channel length and gate coupling. Programming characteristics of the cell is shown in Figure 6, for different channel lengths. The single poly EPROM exhibits programming speed which is comparable to conventional double poly EPROMs. For a cell programmed threshold voltage of greater than 5.5 volts, a programming pulse time of less than .10 msec is needed. The effect of gate coupling on cell programming is shown in Figure 7. The programmed threshold as a function of time is shown for different gate coupling areas. The programming rate initially increases with the gate coupling. Beyond a point, the programming rate is degraded with increasing gate coupling.

The single poly EPROM is implemented in a standard EPROM array architecture as shown in Figure 8. Array sizes of up to 2KX8 are readily implemented on less than 2800 mil^2 area. To reduce word line, RC delay which is caused by large n-well resistance, a (256X32) array organization is selected.

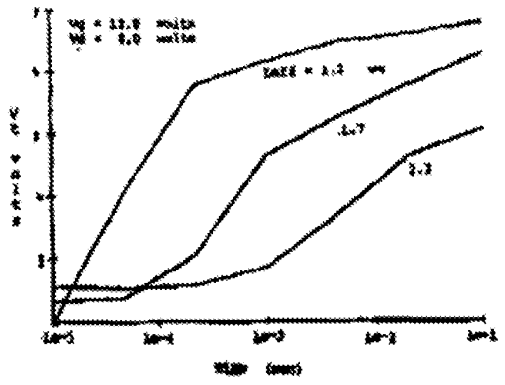


Fig. 6. The cell programming characteristics

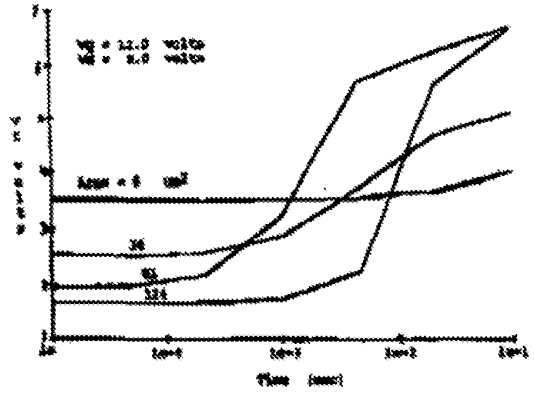
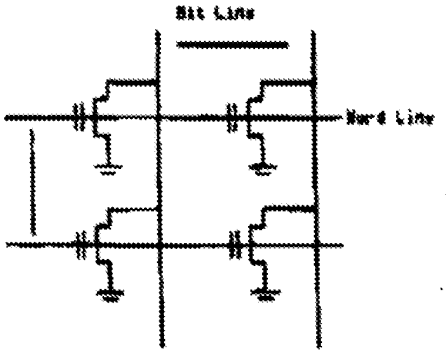


Fig. 7. The effect of gate coupling on cell programming



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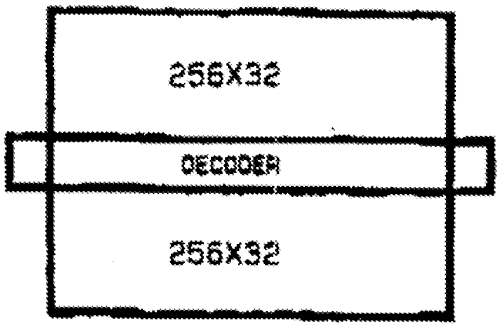


Fig. 8. Array implementation for single poly EPROM.

Reliability

Data retention characteristics of single poly EPROM cells is evaluated on single cells at three temperatures of 200, 250, and 300°C. A threshold voltage shift of less than 500 mV over a 10 year operation at 125°C (150°C for storage) is assured.

The single poly EPROM is erased by exposure to UV light. The erase characteristics of the cell is shown in Figure 9. The single poly EPROM is erased in less than 10 minutes which compares to conventional double poly EPROM. The UV erase rate is lower for the larger gate area. Photon injection of electrons from the edges of the polysilicon is suggested to be the dominant erase mechanism, which explains the decrease in UV erase rate as the gate area increases. (The increase in gate area results in a decrease in the ratio of gate perimeter to gate area.)

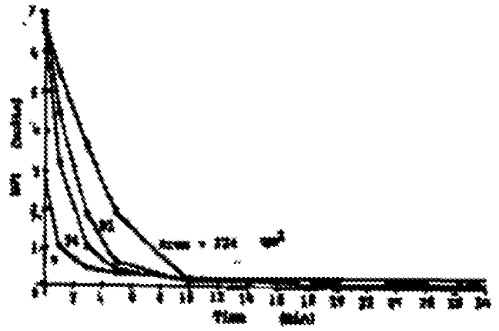


Fig. 9. UV erase characteristics of the single poly EPROM

Summary

The single poly EPROM is very attractive for custom CMOS logic applications where the cell size is traded off for process simplicity.

The memory element is successfully implemented in a small CMOS technology without any additional processing steps. The cell has a high read current and a fast programming speed which is comparable to conventional double poly EPROMs. The single poly EPROM is easily implemented in standard EPROM array architecture. The charge retention and UV erase characteristics of the cell are similar to double poly EPROM. No experimental problem or reliability hazards are found to prevent use of the single poly EPROM in production.

Acknowledgement

The authors wish to thank Dr. E. Harari and Dr. Steve Su for their continuous encouragement and Dr. T. Wu and Mr. Ching Hu for assistance and processing support. We wish to also thank N. Ghilzai and J. Montes for helping to prepare the manuscript.

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INITIAL RELEASE
Final Electrical Specifications

LTC1799

1kHz to 30MHz Resistor Set SOT-23 Oscillator

January 2001

FEATURES

- **One External Resistor Sets the Frequency**
- **1kHz to 30MHz Frequency Range**
- **SOT-23 Miniature Package**
- Frequency Error ≤1.5% 5kHz to 20MHz (T_A = 25°C)
- Frequency Error ≤2% 5kHz to 20MHz (T_A = 0°C to 70°C)
- ±40ppm/°C Temperature Stability
- 0.05%/V Supply Stability
- 50% ±1% Duty Cycle 1kHz to 2MHz
- 50% ±5% Duty Cycle 2MHz to 20MHz
- 1mA Typical Supply Current
- 100Ω CMOS Output Driver
- Operates from a Single 2.7V to 5.5V Supply

APPLICATIONS

- Low Cost Precision Oscillator
- Charge Pump Driver
- Switching Power Supply Clock Reference
- Clocking Switched Capacitor Filters
- Fixed Crystal Oscillator Replacement
- Ceramic Oscillator Replacement
- Small Footprint Replacement for Econ Oscillators

DESCRIPTION

The LTC®1799 is a precision oscillator that is easy to use and occupies very little PC board space. The oscillator frequency is programmed by a single external resistor (R_{SET}). The LTC1799 has been designed for high accuracy operation (≤1.5% frequency error) without the need for external trim components.

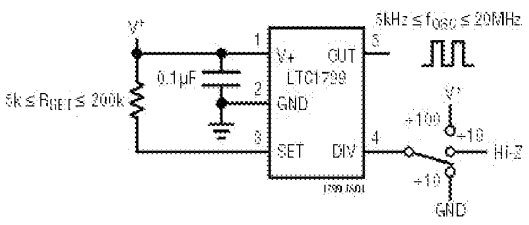
The LTC1799 operates with a single 2.7V to 5.5V power supply and provides a rail-to-rail, 50% duty cycle square wave output. The CMOS output driver ensures fast rise/fall times and rail-to-rail switching. The frequency-setting resistor can vary from 3.32k to 1M to select a master oscillator frequency between 100kHz and 30MHz (5V supply). The three-state DIV input determines whether the master clock is divided by 1, 10 or 100 before driving the output, providing three frequency ranges spanning 1kHz to 30MHz (5V supply). The LTC1799 features a proprietary feedback loop that linearizes the relationship between R_{SET} and frequency, eliminating the need for tables to calculate frequency. The oscillator can be easily programmed using the simple formula outlined below:

$$f_{OSC} = 10MHz \cdot \frac{10k}{N \cdot R_{SET}}, \quad N = \begin{cases} 100, & DIV\ PIN = V^+ \\ 10, & DIV\ PIN = Hi\text{-}Z \\ 1, & DIV\ PIN = GND \end{cases}$$

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

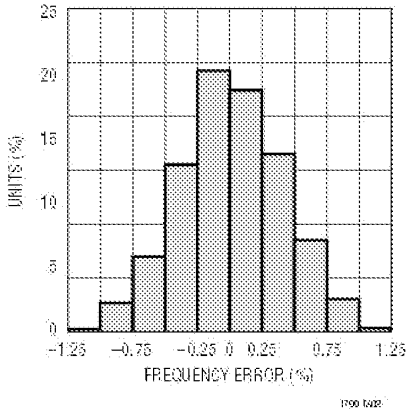
TYPICAL APPLICATION

Basic Connection



SOT-23 Actual Size

Typical Distribution of Frequency Error, T_A = 25°C



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

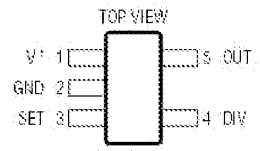
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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) to GND ..... –0.3V to 6V
DIV to GND ..... –0.3V to (V^+ + 0.3V)
SET to GND ..... –0.3V to (V^+ + 0.3V)
OUT to GND ..... –0.3V to (V^+ + 0.3V)
Operating Temperature Range
LTC1799C ..... 0°C to 70°C
LTC1799I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S5 PACKAGE
5-LEAD PLASTIC SOT-23

T_{JMAX} = 125°C, θ_{JA} = 256°C/W

ORDER PART NUMBER
LTC1799CS5 LTC1799IS5
S5 PART MARKING
LTND LTNE

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The λ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 2.7V to 5.5V, R_L=5k, C_L = 5pF, Pin 4 = V^+ unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Δf	Frequency Accuracy	V^+ = 5V	5kHz < f < 20MHz			±0.5	±1.5	%
			5kHz < f < 20MHz, LTC1799C	λ			±2	%
			5kHz < f < 20MHz, LTC1799I	λ			±2.5	%
	(Notes 2, 3)		1kHz < f < 5kHz			±2.5		%
			20MHz < f < 30MHz			±2.5		%
		V^+ = 3V	5kHz < f < 10MHz			±0.5	±1.5	%
			5kHz < f < 10MHz, LTC1799C	λ			±2	%
			5kHz < f < 10MHz, LTC1799I	λ			±2.5	%
			1kHz < f < 5kHz			±2.5		%
			10MHz < f < 20MHz			±2.5		%
R_{SET}	Frequency-Setting Resistor Range	Δf < 1.5%		V^+ = 5V	8		200	kΩ
				V^+ = 3V	10		200	kΩ
f_{MAX}	Maximum Frequency	Δf < 2.5%, Pin 4 = 0V		V^+ = 5V		30		MHz
				V^+ = 3V		20		MHz
f_{MIN}	Minimum Frequency	Δf < 2.5%, Pin 4 = V^+				1		kHz
Δf/ΔT	Freq Drift Over Temp (Note 3)	R_{SET} = 31.6k		λ		±0.004		%/°C
Δf/ΔV	Freq Drift Over Supply (Note 3)	V^+ = 2.7V to 5.5V, R_{SET} = 31.6k		λ		0.05	0.1	%/V
	Timing Jitter (Note 4)	Pin 4 = V^+				0.06		%
		Pin 4 = Floating				0.13		%
		Pin 4 = 0V				0.4		%
	Long-Term Stability of Output Frequency					300		ppm/$\sqrt{kHr}$
	Duty Cycle	Pin 4 = V^+ or Floating (DIV Either by 100 or 10)		λ	49	50	51	%
		Pin 4 = 0V (DIV by 1)		λ	45	50	55	%
V^+	Operating Supply Range			λ	2.7		5.5	V
I_S	Power Supply Current	R_{SET} = 200k, Pin 4 = V^+, R_L = 0	V^+ = 5V	λ		0.7	1.1	mA
		R_{SET} = 10k, Pin 4 = 0V, No Load	V^+ = 5V	λ			2.4	mA
			V^+ = 3V	λ			2	mA
V_{IH}	High Level DIV Input Voltage			λ	V^+ – 0.4			V
V_{IL}	Low Level DIV Input Voltage			λ			0.5	V
I_{DIV}	DIV Input Current	Pin 4 = V^+		λ		5	8	μA
		Pin 4 = 0V		λ		–5	8	μA

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ELECTRICAL CHARACTERISTICS

The λ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V⁺ = 2.7V to 5.5V, R_L=5k, C_L = 5pF, Pin 4 = V⁺ unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{OH}	High Level Output Voltage	V⁺ = 5V	I_{OH} = –1mA	λ	4.8	4.95		V
			I_{OH} = –4mA	λ	4.5	4.8		V
		V⁺ = 3V	I_{OH} = –1mA	λ	2.7	2.9		V
			I_{OH} = –4mA	λ	2.2	2.6		V
V_{OL}	Low Level Output Voltage	V⁺ = 5V	I_{OL} = 1mA	λ		0.05	0.15	V
			I_{OL} = 4mA	λ		0.2	0.4	V
		V⁺ = 3V	I_{OL} = 1mA	λ		0.1	0.3	V
			I_{OL} = 4mA	λ		0.4	0.7	V
t_r	OUT Rise Time (Note 5)	V⁺ = 5V	Pin 4 = V⁺ or Floating, R_L = 0			14		ns
			Pin 4 = 0V, R_L = 0			7		ns
		V⁺ = 3V	Pin 4 = V⁺ or Floating, R_L = 0			19		ns
			Pin 4 = 0V, R_L = 0			11		ns
t_f	OUT Fall Time (Note 5)	V⁺ = 5V	Pin 4 = V⁺ or Floating, R_L = 0			13		ns
			Pin 4 = 0V, R_L = 0			6		ns
		V⁺ = 3V	Pin 4 = V⁺ or Floating, R_L = 0			19		ns
			Pin 4 = 0V, R_L = 0			10		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Frequencies near 100kHz and 1MHz may be generated using two different values of R_{SET} (see the Table 1 in the Applications Information section). For these frequencies, the error is specified under the following assumption: 10k < R_{SET} ≤ 100k.

Note 3: Frequency error (defined as the deviation from the f_{OSC} equation) includes drift over temperature and over supply.

Note 4: Jitter is the ratio of the peak-to-peak distribution of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

Note 5: Output rise and fall times are measured between the 10% and 90% power supply levels. These specifications are based on characterization.

PIN FUNCTIONS

V⁺ (Pin 1): Voltage Supply (2.7V ≤ V⁺ ≤ 5.5V). This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane.

GND (Pin 2): Ground. Should be tied to a ground plane for best performance.

SET (Pin 3): Frequency-Setting Resistor Input. The value of the resistor connected between this pin and V⁺ determines the oscillator frequency. The voltage on this pin is held by the LTC1799 to approximately 1.1V below the V⁺ voltage. For best performance, use a precision metal film resistor with a value between 10k and 200k and limit the capacitance on this pin to less than 2pF.

DIV (Pin 4): Divider-Setting Input. This three-state input selects among three divider settings, determining the value of N in the frequency equation. Pin 4 should be tied to GND for the ÷1 setting, the highest frequency range. Floating Pin 4 divides the master oscillator by 10. Pin 4 should be tied to V⁺ for the ÷100 setting, the lowest frequency range. To detect a floating DIV pin, the LTC1799 attempts to pull the pin toward midsupply. Therefore, driving the DIV pin high requires sourcing approximately 5µA. Likewise, driving DIV low requires sinking 5µA. When floated, the DIV pin will be held near midsupply by these current sources. When it is floated, it is recommended that the DIV pin be bypassed by a 1nF capacitor or surrounded by a ground shield to prevent excessive coupling from other PCB traces.

OUT (Pin 5): Oscillator Output. This pin can easily drive 5kΩ or 10pF loads. Larger loads may cause inaccuracies due to supply bounce at high frequencies.

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APPLICATIONS INFORMATION

Selecting the Divider Setting and Resistor

The LTC1799's master oscillator has a frequency range spanning 0.1MHz to 30MHz. However, accuracy may suffer if the master oscillator is operated at greater than 10MHz with a supply voltage lower than 4V. A programmable divider extends the frequency range to greater than three decades. Table 1 describes the recommended frequencies for each divider setting. Note that the ranges overlap; at some frequencies there are two divider/resistor combinations that result in the desired frequency.

In general, any given oscillator frequency (f_{OSC}) should be obtained using the lowest master oscillator frequency. Lower master oscillator frequencies use less power and are more accuate. For instance, f_{OSC} = 100kHz can be obtained by either R_{SET} = 10k, N = 100, master oscillator = 10MHz or R_{SET} = 100k, N = 10, master oscillator = 1MHz. The R_{SET} = 100k is preferred for lower power and better accuracy.

Table 1. Frequency Range vs Divider Setting

DIVIDER SETTING			FREQUENCY RANGE
÷1	⇒	DIV (Pin 4) = GND	>500kHz*
÷10	⇒	DIV (Pin 4) = Floating	50kHz to 1MHz
÷100	⇒	DIV (Pin 4) = V+	<100kHz

*At master oscillator frequencies greater than 10MHz (R_{SET} < 10kΩ), the LTC1799 may suffer reduced accuracy with a supply voltage less than 4V.

After choosing the proper divider setting, determine the correct frequency-setting resistor. Because of the linear correspondence between oscillation period and resistance, a simple equation relates resistance with frequency.

$R_{SET} = 10k \bullet [10MHz/(N \bullet f_{OSC})]$, N = 1, 10, 100
(R_{SETMIN} = 3.32k (5V Supply), 5k (3V Supply),
R_{SETMAX} = 1M)

Any resistor, R_{SET}, tolerance adds to the inaccuracy of the oscillator, f_{OSC}.

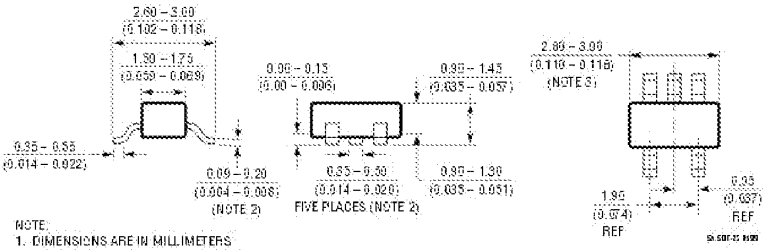
Settling Time

The settling time is proportional to R_{SET} and is approximately $t_{SETTLE} \approx R_{SET} \bullet (5\mu s/k\Omega)$. This parameter is guaranteed by design and not 100% tested.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S5 Package
5-Lead Plastic SOT-23
(LTC DWG # 05-08-1633)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
4. MOLD FLASH SHALL NOT EXCEED 0.254mm
5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)

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BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability

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Abstract

A bandgap engineered SONOS with greatly improved reliability properties is proposed. This concept is demonstrated by a multi-layer structure of O1/N1/O2/N2/O3, where the ultra-thin "O1/N1/O2" serves as a non-trapping tunneling dielectric, N2 the high-trapping-rate charge storage layer, and O3 the blocking oxide. The ultra-thin "O1/N1/O2" provides a "modulated tunneling barrier" -- it suppresses direct tunneling at low electric field during retention, while it allows efficient hole tunneling erase at high electric field due to the band offset. Therefore, this BE-SONOS offers fast hole tunneling erase, while it is immune to the retention problem of the conventional SONOS. With a N^+-poly gate, we achieve self-convergent erased Vt ~3 V, suitable for NOR Flash application. On the other hand, by using a P^+-poly gate, a depletion mode device (Vt < 0) is obtained, and a very large memory window (> 6 V) is achieved, ideal for MLC- NAND application. Excellent performance and reliability for both applications are demonstrated. Furthermore, with this simple structure and no new materials BE-SONOS is readily manufacturable.

I. Introduction

Floating gate devices are rapidly approaching serious scaling challenges due to inter-floating gate coupling, while nitride-trapping device is free from such limitations. Nitride-trapping device consists of two main types: SONOS [1] which uses channel program/erase, and NROM [2] which store charges locally. SONOS suffers from retention problems due to direct tunneling leakage through the thin tunnel oxide, and NROM is sensitive to hot-hole induced damages [3, 4]. There has been several proposals that promise the further scaling of NROM [5, 6], however, new solutions that do not invoke hot holes are still desirable.

A multi-layer SONOS with stacked thin nitride films (<4 nm) has been previously reported [7]. The purpose was to introduce a double trapping layer in order to increase the trapping efficiency. However, this device suffers from slow programming speed (>100 msec) and small memory window (< 2 V).

Contrary to the previous work [7], we found that ultra-thin nitride (<2 nm) has negligible charge trapping. Therefore, we propose a bandgap engineered ONO tunneling dielectric to replace the traditional tunnel oxide in SONOS.

An analogy is the concept of "crested barrier" [8], which was previously proposed to modulate the electron tunneling current for floating gate devices. However, such concept often requires high-k gate dielectric [9] and so far no practical application is successful. On the other hand, our proposed ONO tunneling dielectric serves as an efficient hole tunneling barrier for SONOS, and it is much more reliable and practical.

In this work, we have designed BE-SONOS devices using N^+ and P^+ poly gates that are suitable for NOR and NAND Flash applications (illustrated in Table 1), respectively.

II. Principle of the BE-SONOS – ONO tunneling dielectric

The structure and parameters of n-channel BE-SONOS are illustrated in Fig. 1 and Table 2, respectively. The "O1/N1/O2" tunneling dielectric consists of ultra-thin (<2 nm) oxide and nitride that modulates the hole tunneling current. The thicker (7 nm) N2 serves as the charge-trapping layer and O3 (9 nm) serves as the blocking oxide. O3 is grown by thermal conversion of N2 so that efficient interfacial traps between N2/O3 are provided [10].

The properties of ultra-thin O1/N1/O2 tunneling dielectric are characterized by both MOSFET and capacitors. The MOSFET with ultra-thin O1/N1/O2 gate dielectric shows negligible charge trapping regardless of the injection mode: CHE, +FN and –FN (Fig. 2). Constant current stressing (CCS) of the capacitor (Fig. 3) indicates excellent stress tolerance. The poor trapping efficiency may be due to that the capture mean free path is much longer than the ultra-thin nitride thickness. In addition, no interfacial traps between O1/N1 and N1/O2 are introduced during processing.

Since the ultra-thin ONO layer has negligible charge trapping, it is suitable for tunneling dielectric. The principal merit comes from the low hole-tunneling barrier (~1.9 eV) of SiN compared to that of oxide (~4.5 eV). The band diagrams of the ONO tunneling dielectric (O1/N1/O2=15/20/18 Å) are shown in Figs. 4 and 5. Under low electrical field during retention (Fig. 4), hole direct tunneling cannot happen because the total thickness of O1/N1/O2 is large. On the other hand, band offset happens under high electric field (Fig. 5) and the hole barriers of N1 and O2 are below the valence band. Thus a large hole tunneling current through O1 occurs under –FN bias. This is clearly shown by WKB simulation of the hole tunneling current in Fig. 6, where a high ON-OFF ratio of tunneling currents is achieved.

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The experimental hole tunneling current can be extracted by differentiation of the erase characteristic in Fig. 7 using the transient analysis method [10]. The experimental hole currents are well matched with the simulation.

III. NOR Application Using N^+-Poly Gate

For NOR applications, the device is programmed by CHE method. Since electrons are locally trapped near the junction, the reverse read method [2] can be employed for 2-bit/cell memory operation. Contrary to NROM for which hot-hole is used for erase, the erase operation is performed by uniform hole tunneling to compensate the electrons. During $-V_G$ erase, both electron injection from N^+-poly gate and hole injection from substrate happen simultaneously, leading to a dynamic balancing condition [5, 6], (Fig. 7). Figure 8 shows that the self-convergent V_T is controlled by the erase voltage. As expected, a higher gate voltage results in a higher saturation V_T because gate injection is stronger. This self-convergent erase is very desirable for NOR Flash because the over-erase problem is avoided.

Figure 9 illustrates the excellent P/E cycling endurance. Contrary to NROM, there is no hard-to-erase [5, 6] even after dumb-mode 10K cycles (without any P/E verify and stepping algorithm), since channel hole-tunneling erase is a uniform erase thus electrons cannot pile up at the channel center region. Figure 10 shows that the *I-V* curves have very slight degradation after 10K P/E cycles. Subthreshold swing stays mostly the same, indicating small interface trap generation. In addition, charge pumping measurement (Fig. 11) also shows no excess hole traps after P/E cycles because excess hole traps are compensated by the gate injected electrons. High-temperature (150 ^{0}C) baking (Fig. 12) shows excellent electron retention for this BE-SONOS device.

Apart from the FN annealing effect [5, 6], the superb reliability performance is also due to that hole tunneling erase causes much less damage than hot-hole erase used in NROM.

IV. NAND Application Using P^+-Poly Gate

For NAND application, depletion mode device ($V_T < 0$) for the erased state is desired. By using a P^+-poly gate, the gate injection is reduced [6] and the device can be erased into depletion mode ($V_T < 0$), as shown in Fig. 13.

Figure 13 shows that the erase speed is increased when applying a higher gate voltage. However, erase saturation may happen because gate injection is stronger at higher gate voltage. Figure 14 shows the +FN programming speed, where more than 7 V memory window can be achieved within 10 msec.

Excellent cycling endurance is shown in Fig. 15; only very small degradation is observed. V_G accelerated retention test (Fig. 16) shows that the direct tunneling at low electric field (<4 MV/cm) is completely suppressed. As a result, more than 6 V memory window is preserved even after 500 hours of 150 ^{0}C baking (Fig. 17). The large memory window (>6 V) and the excellent retention are the best reported results so far for NROM and SONOS-type devices.

The erase characteristics of BE-SONOS can be controlled by the thickness of ONO tunneling dielectric (Fig. 18) and gate material engineering (Fig. 19). Figure 18 shows that the erase speed is mainly dominant by O1 because the band offset as shown in Fig. 5 effectively screens out the barrier of N1 and O2. Figure 19 shows that the gate injection of a high work function Platinum (Pt) gate can almost be completely suppressed so that erase saturation does not happen. Figure 20 shows the retention of various P/E cycled conditions. The cycling induced charge loss is very small, indicating a small P/E induced damage. Furthermore, the retention of the short-loop capacitors (up to metal 1) are consistent with the full-run MOSFET (up to metal 3). The device dimension and back-end metal processes have little impact on the retention of BE-SONOS.

V. Summary

BE-SONOS with bandgap engineered tunneling dielectric is proposed. This new device is free from the direct tunneling leakage of conventional SONOS, and hot-hole induced damages of NROM devices. Excellent reliability and performance are demonstrated. BE-SONOS may be used for both NOR and NAND applications and is readily manufacturable. Without the floating gate coupling interference problem, BE-SONOS is a promising candidate for the next-generation Flash memories.

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	N^+-Poly Gate	P^+-Poly Gate
Applications	NOR-type Flash	NAND-type Flash
Self-convergent V_T	>0 V	<0 V
Programming Method	CHE	+FN
Reading Method	Reverse Read Method (2-bit/cell)	Normal Read (1-bit/cell or MLC)
Erasing Method	Hole Tunneling Erase V_G= -15 V	Hole Tunneling Erase V_G= -18 V

Table 1 Summary of the applications of BE-SONOS with N^+ and P^+-poly gate.

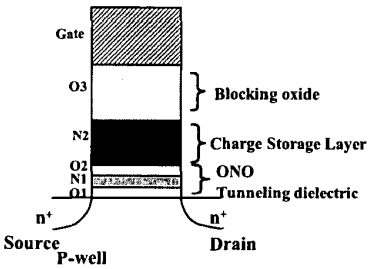


Fig. 1 Structure of the n-channel BE-SONOS using ultra-thin ONO tunneling dielectric.

Bottom Oxide (O1)	15 Å
Inter Nitride (N1)	20 Å
Inter Oxide (O2)	18 Å
Trapping Nitride (N2)	70 Å
Blocking Oxide (O3)	90 Å
Gate Material	N^+-Poly (NOR-type) P^+-Poly (NAND-type)
Channel Length	0.22 μm
Channel Width	0.16 μm

Table. 2 Typical parameters of the n-channel BE-SONOS.

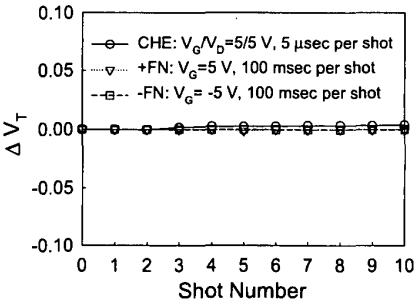


Fig. 2 The characteristics of nMOSFET with ONO tunneling dielectric O1/N1/O2=15/20/18 Å. Various injection methods including +FN, -FN and CHE all show negligible charge trapping.

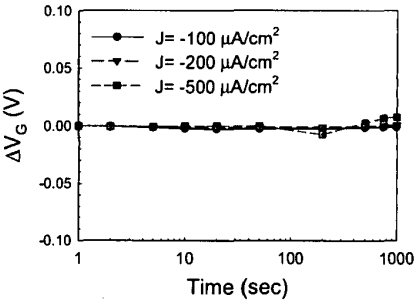


Fig. 3 Constant current stress (CCS) of the ONO tunneling dielectric (15/20/18) capacitor. Small charge trapping is observed under negative gate current stress.

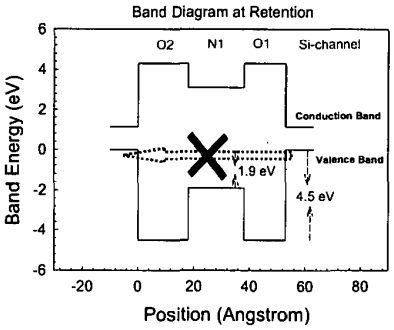


Fig. 4 Band diagram of the of O1/N1/O2 tunneling dielectric at zero electrical field. Hole direct tunneling can not happen due to the thick ONO layer. The charge loss during retention can be suppressed.

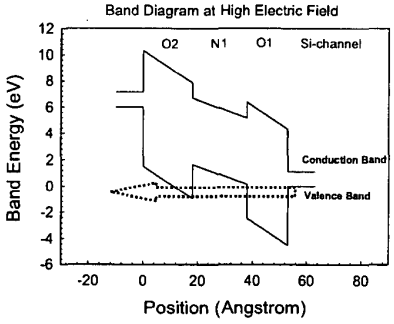


Fig. 5 Band diagram of the of O1/N1/O2 tunneling dielectric under negative gate bias. The tunnel barriers of N1 and O2 are almost screened due to the band offset such that hole direct tunneling through O1 can happen.

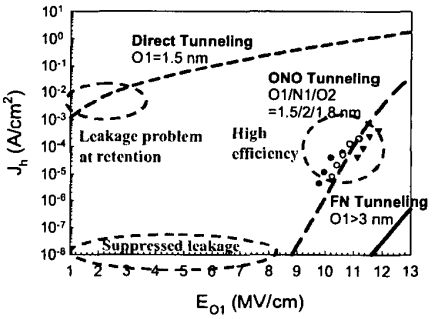


Fig. 6 The measured and simulated hole tunneling current for this device. The measured hole tunneling current (dotted symbols) are extracted by the transient analysis method [10] in Fig 7. WKB method is used to calculate the tunneling barrier in Fig. 5.

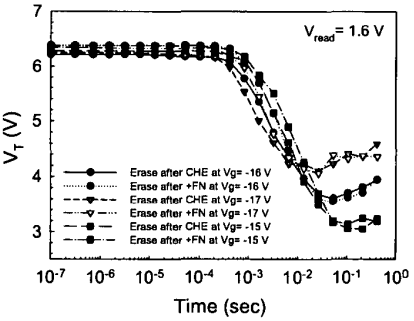


Fig. 7 Erase characteristics of the N^+-poly gate BE-SONOS at various gate voltages. The erase saturates at a positive V_T. The erase speeds for CHE and +FN programmed devices are similar.

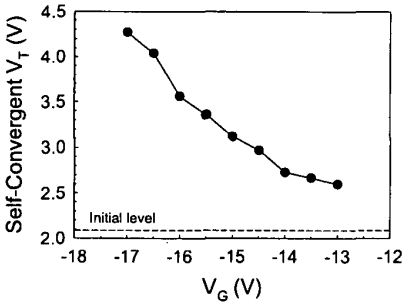


Fig. 8 Self-convergent V_T as a function of erase V_G of the N^+-poly gate BE-SONOS. A larger V_G corresponds to a larger convergent V_T because gate injection is higher.

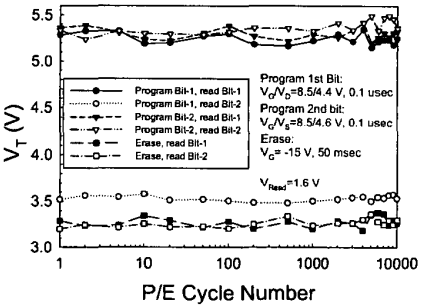


Fig. 9 P/E cycle endurance of N^+-poly gate BE-SONOS (NOR-type). Only one-shot program and one-shot erase were used without P/E verify, and the device possesses excellent endurance property.

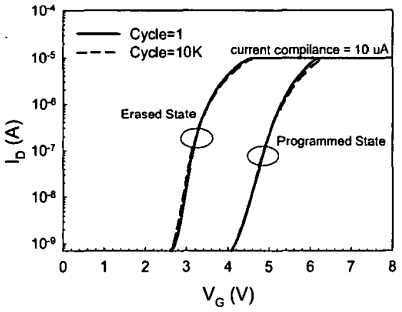


Fig. 10 *IV* curves during 10K P/E cycles in Fig. 9. It shows small degradation of sub-threshold slope and trans-conductance.

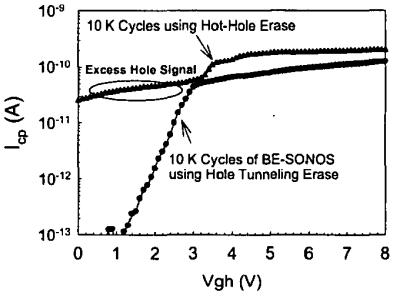


Fig. 11 Charge pumping measurement of the NOR-type operations after 10K P/E cycles. A comparison with the condition using hot-hole erase is also provided.

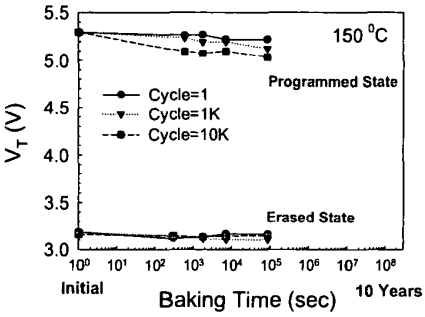


Fig. 12 High-temperature baking of the NOR-type operations at various P/E cycle condition.

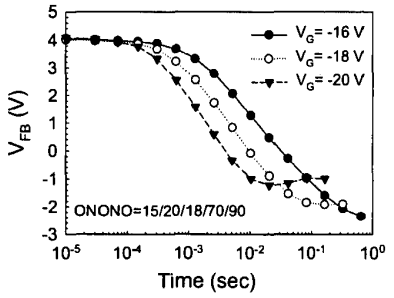


Fig. 13 Erase characteristics of the P+-poly BE-SONOS capacitors. Gate injection is suppressed and negative V_{FB} can be achieved. At larger V_G, gate injection becomes significant, resulting in erase saturation.

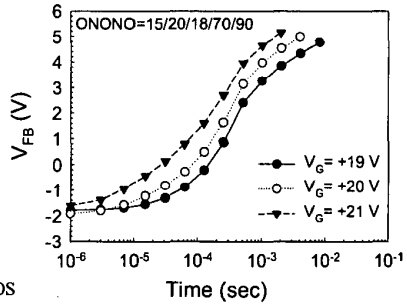


Fig. 14 +FN programming characteristics of the P+-poly gate capacitor. A large memory window (>7 V) can be obtained within 10 msec.

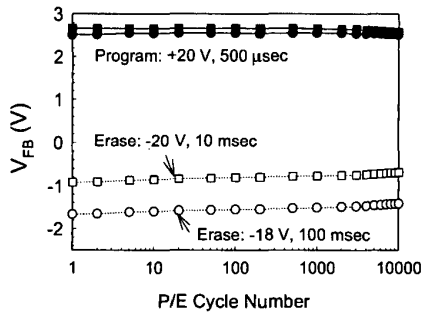


Fig. 15 P/E cycle endurance of the P+-poly gate capacitor. Only one-shot program and one-shot erase was used during P/E cycles.

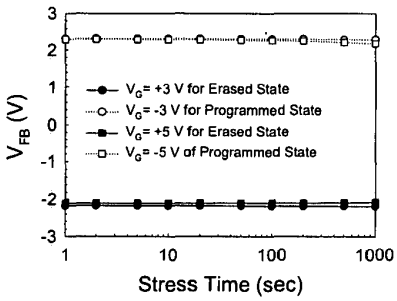


Fig. 16 V_G accelerated retention test. $-V_G$ is applied for programmed state and $+V_G$ for erased state. The small charge loss and charge gain indicate that direct tunneling are suppressed below medium field (< 4 MV/cm).

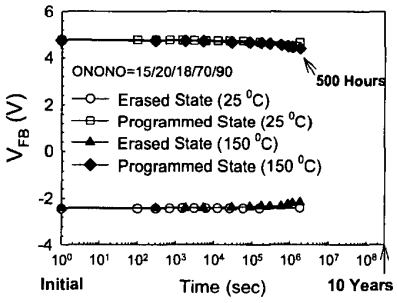


Fig. 17 Charge retention of the P+-poly gate capacitor (P/E cycle=1). The charge loss and charge gain are negligible at room temperature. More than 6.5 V memory window can be preserved even after 500 hour of 150 °C baking.

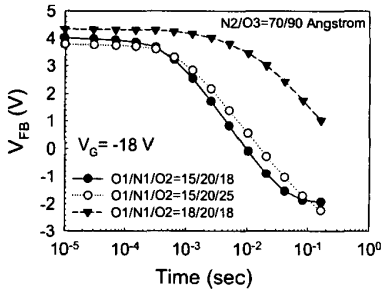


Fig. 18 Erase characteristics of various O1/N1/O2 tunneling dielectric with P+-poly gate. The erase speed is very sensitive to O1, while O2 has much smaller effect. This is because ONO tunneling is dominated by O1, while O2 is almost screened by the band offset (shown in Fig. 5).

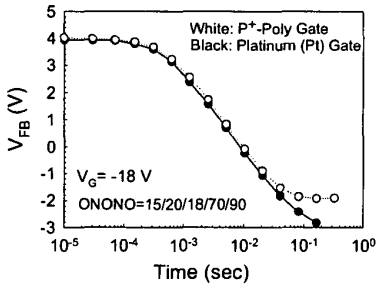


Fig. 19 Comparison of the erase characteristic of P+-poly gate and Platinum (Pt) gate capacitors. Pt has a high work function that can suppress gate injection, leading to a non-saturated erase. Pt gate was patterned by the lift-off process.

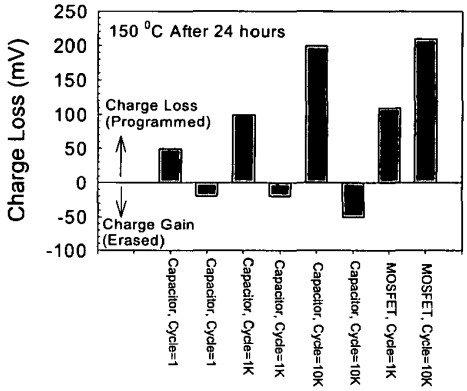


Fig. 20 Comparison of the charge loss/charge gain after 24-hour baking for various P/E cycle conditions. The programmed and erased delta V_T are +3 V and -2 V referenced to the initial state, respectively. The P/E cycle induced charge loss is small. Furthermore, the retention results of a full-run MOSFET device (Lg=0.16 μm) with up to metal 3 processes are close to that of the short-loop capacitors with only metal 1 processes. It indicates that the retention properties of BE-SONOS is insensitive to back-end processes. It is only related to the intrinsic properties of ONONO.

Reliability Model of Bandgap Engineered SONOS (BE-SONOS)

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Abstract -

Reliability properties of bandgap engineered SONOS (BE-SONOS) [1] are extensively studied. First, the erase mechanism of BE-SONOS is confirmed as substrate hole tunneling through the ultra-thin ONO tunneling dielectric. Next, very long-term (>3,000 hours) high-temperature baking data (from 150 to 250°C) for various programmed/erased states and cycling history are collected and analyzed for a thorough understanding of the retention property. By transforming retention data (V_{FB}-time) into de-trapping current (J) and modeling its dependence on electric field and temperature, the long-term retention of various programmed states are consistently and accurately predicted. This modeling technique avoids the ambiguity of the common Arrhenius plot, and is useful for developing other predictive models too. We have shown that BE-SONOS surpasses the 10-year 85°C storage criterion for Flash memory applications.

I. Introduction

Recently, floating gate flash memories are rapidly approaching scaling limits such as the coupling ratio issues, and charge-trapping memory devices are forecasted as the solution below 45 nm node [1,2]. Although there are many varieties proposed, the major challenge is whether these new devices can pass the 10-year 85^0C storage criterion. In fact, charge-trapping devices tend to suffer memory window closure after long-term high-temperature baking and so far there is no general consensus on a predictive model. Therefore, a reliable device as well as an accurate life-time prediction model is in urgent need.

Last year, we proposed BE-SONOS [1] device for both NOR and NAND Flash applications. The structure and typical process condition of the BE-SONOS device are shown in Fig. 1 and Table 1, respectively. This new device exploits a bandgap engineered tunnel dielectric to replace the traditional thin tunnel oxide in SONOS. As shown in Fig. 2, under high electric field during erase, the hole tunneling distance is effectively reduced to the thin O1 due to the band offset. Therefore, efficient hole tunneling current is achieved. On the other hand, at low electric field during retention, charge leakage is completely blocked by the thick ONO barrier. Hence, good data retention is granted by the entire ONO barrier that prevents direct tunneling. With its simple structure and using only known materials, BE-SONOS is a very promising solution for below 45nm node. In this work, the reliability of BE-SONOS is extensively studied and an accurate retention model is developed.

II. Erase Characteristics of BE-SONOS

The *IV* characteristics of the thin ONO barrier are shown in Fig. 3. The results show that the measured hole current at high electric field is consistent with the theoretical calculation from WKB approximation. Moreover, the *IV* characteristics of ONO tunneling dielectric show no degradation after continuous current stress. This excellent stress tolerance makes the ultra-thin ONO an ideal variable-thickness tunneling barrier.

Note that the ultra-thin ONO does not need to be perfect. Even if the SiN in the thin ONO is slightly trappy, the band diagram in Fig. 2 is still valid so that the program/erase operations are not affected. On the other hand, the retention of SONOS-type devices can be excellent for a non-perfect tunnel barrier because charges are deeply trapped in nitride. Therefore, the tunnel barrier engineering in SONOS-type devices is much more feasible than that in the floating-gate devices.

In order to further clarify the erase mechanism, a refill [3] technique is applied. The refill method is a repeating sequence of partial erasing followed by reprogramming in order to alter the trap energy spectrum. The detailed procedure is illustrated in Fig. 4. For comparison, a SONOS device with a thick tunnel oxide (4.5nm) is also measured. Since the thick tunnel oxide does not allow hole tunneling and the erase speed is much slower than BE-SONOS, this SONOS device is erased through a de-trap tunneling mechanism. Figure 4 shows that the erase speed of SONOS is significantly reduced after the refill method, while BE-SONOS shows a constant erase speed. This indicates that the two devices have different erase mechanisms.

For the de-trapping tunneling mechanism, the refill method reduces the shallowly-trapped electrons [3], thus reduces the erase speed. On the other hand, BE-SONOS device uses hole tunneling for the erase, which does not depend on the electron trap energy. Hence, its erase speed is not affected by the refill method.

Therefore, the refill behavior serves as a tool to distinguish hole tunneling from electron de-trapping. Since hole-tunneling erase is independent of the electron trap energy, the erase speed of BE-SONOS is insensitive to the programming method, as shown in Fig. 5.

Figure 6 shows that the erase speed is not degraded after 10K P/E cycling, indicating very excellent endurance, consistent with Fig. 3. Figure 7 illustrates the erase speed characteristics with respect to various ONO barrier. The results clearly indicate that the erase speed for BE-SONOS is

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dominated by the thin O1, while O2 and N1 thickness have very small effect. This is consistent with the bandgap engineering concept (Fig. 2), where the barriers of N1 and O2 are almost screened due to the band offset [1].

III. Long-Term High-Temperature Baking

Figure 8 shows the long-term retention of various PV and EV states at three temperatures (150, 200 and 250°C). The characteristics can be briefly summarized:

(1) The programmed states (excess electron) do not show any significant charge loss until a particular life time, and the life time decreases as temperature increases.
(2) The erased states (excess hole) do not show significant charge gain even after 250°C/1,000 hour baking. Moreover, the retention is insensitive to the temperature.
(3) The P/E cycled devices show only a slightly larger initial charge loss (for PV) or charge gain (for EV), but the long-term retention behavior is the same as un-cycled devices. The long-term charge loss rate is very similar.

IV. Retention Model

Arrhenius plots are often used [4] to extrapolate the device life time. In this method, life time is plotted versus 1/kT. By assuming that the slope is equal to the activation energy (E_A), life time can be extrapolated. However, this method has ambiguities in the definition of life time. Besides, Arrhenius fitting is always inconsistent for various programmed state, as shown in Fig. 9. The reason is that Arrhenius analysis does not include the effect of built-in electric field.

In this work, we model the de-trapping current (J) instead of Vt (or V_{FB}). J is obtained by differentiation of Vt with respect to time, and it is physical and has direct dependence on temperature and electric field. The detailed procedures and related equations are listed in Tables 2-4. Since excess-hole states show very small charge gain even under 250°C baking, only electron retention is considered here. For simplicity, the fresh state is considered first.

Following Table 2, the retention data (Vt-time) can be transformed into J-E at various temperatures, where E is the built-in electric field. This method is similar to the transient analysis method [5]. The extracted J-E for various programmed state and baking temperatures are shown in Fig. 10. Interestingly, the experimental curves show very similar behaviors with the Frenkel-Poole (F-P) equation. Therefore, we adopted a F-P equation to fit these data, as illustrated in Table 3. There are three parameters. E_A is the activation energy that accounts for the temperature acceleration factor. b is the factor that accounts for the electric field factor. $b=1$ for the ideal F-P equation. a is a global coefficient for F-P equation.

The major parameter of this fitting is E_A, which is extracted by fitting the distance between J-E curves of various temperatures. E_A is found to be close to 1.1 eV, as shown in Table 5. The extracted E_A indicates the major trapping energy level. Interestingly, it is consistent with the previous result using thermionic emission model [6].

In Fig. 10, J-E curves have a well-fitted $E^{1/2}$ dependence, which is consistent with the F-P equation. Finally, the extracted F-P parameters can be used to simulate the retention at various temperatures. Following Table 4, Vt can be obtained by integrating J with respect to time using iteration methods. The simulation results in Figs. 11-13 show very accurate fitting for various PV states and temperatures, using only three parameters (E_A, a and b). Based on this model, the charge loss after 10-year 85°C storage is less than 300 mV for PV= + 4 V (Fig. 14). The excellent long-term retention and the well-predicting model of BE-SONOS are the best-reported results so far for nitride storage devices.

Table 5 compares BE-SONOS devices with various ONO tunneling dielectrics; the extracted F-P parameters are very similar. This indicates that the F-P mechanism is governed by the nitride-trapping layer. We also compare the P/E stressed devices (Fig. 15), and find that the long-term charge loss rate is similar with the fresh device. This may indicate that the effect of P/E stressing can be regarded as an effective increase in shallow traps. The shallow trap generation is calculated as ~5 % (200 mV for PV=+4V), which contributes to the faster initial charge loss (Fig. 15). However, the long-term charge loss is dominated by the deeper traps, which is an intrinsic (fresh) behavior.

The retention behaviors of various electron injection techniques are shown in Fig. 16. Hot-electron (CHE for n-channel device [1] and BBHE for p-channel device [7]) programming shows larger initial charge losses, but the long-term retention behavior converges with FN programming.

V. Summary

The reliability model for BE-SONOS is developed. We have shown that BE-SONOS surpasses the 10-year 85°C storage criterion for Flash memory applications. Moreover, the present work also provides useful characterization methods for other charge-trapping non-volatile memory devices.

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Bottom Oxide (O1)	ISSG, 15 Å
Inter Nitride (N1)	LPCVD, 20 Å
Inter Oxide (O2)	HTO, 25 Å
Trapping Nitride (N2)	LPCVD, 70 Å
Blocking Oxide (O3)	Furnace, 90 Å
Gate Material	P+-Poly

Table 1 Typical process condition of BE-SONOS.

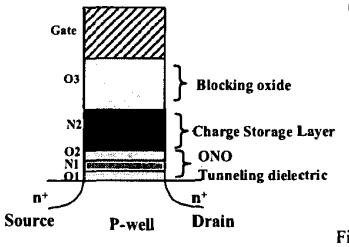


Fig. 1 Structure of the n-channel BE-SONOS using ultra-thin ONO tunneling dielectric.

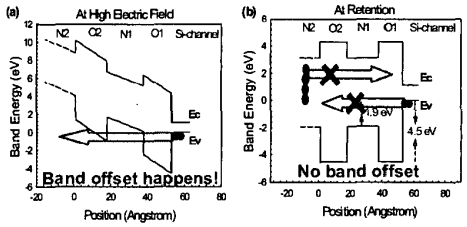


Fig. 2 Bandgap engineering concept for the BE-SONOS device. (a) At high field during erase, band offset reduces the hole tunneling barrier to merely O1. (b) At low field during retention, both electron de-trapping and hole back tunneling are prohibited by the full O1/N1/O2 barrier stack.

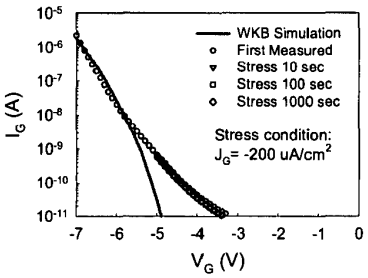


Fig. 3 I_G-V_G of ONO tunneling dielectric (O1/N1/O2=15/20/25) with P+-poly gate after constant current stressing. The solid line is the hole current simulated by WKB method.

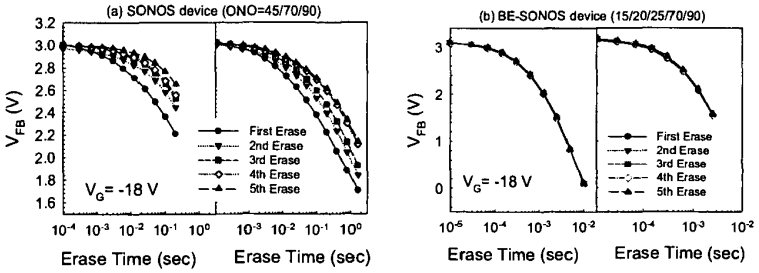


Fig. 4 Refill [3] comparison of (a) SONOS (45/70/90) (b) BE-SONOS (15/20/25/70/90) capacitors. A heavily-doped P+-poly gate is used to suppress gate injection. The device is first programmed to V_{FB}=+3V, and then erased (to a non-saturated state) with various erase times, and then re-programmed (refill) to the programmed state. This process is repeated several times to eliminate the shallowly trapped electrons. BE-SONOS device shows constant erase speed after the refill process, while the SONOS device with a thick tunnel oxide (45 Å) shows lower erase speed after the refill process.

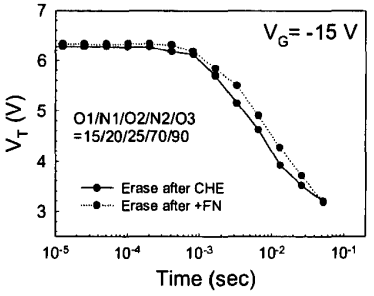


Fig. 5 The erase behavior for BE-SONOS using +FN injection and CHE injection. The device is an n-channel MOSFET with L/W=0.18/0.16 um. The erase speed is independent of the programming method.

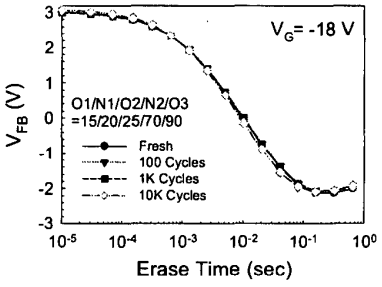


Fig. 6 The erase speed comparison after P/E cycling stress. BE-SONOS device shows very small erase speed degradation after 10K P/E cycles.

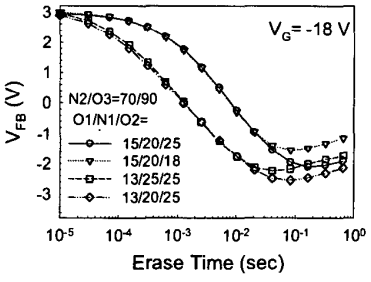


Fig. 7 Erase speed comparison for BE-SONOS with various ONO tunneling dielectrics. The erase speed is dominated by O1.

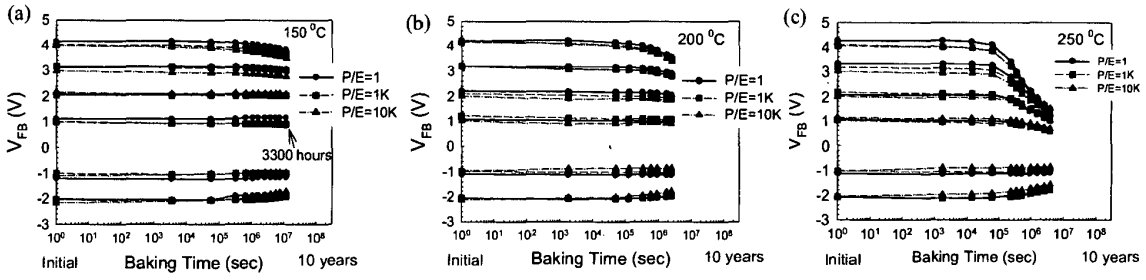


Fig. 8 Long-term retention data for BE-SONOS at (a) 150 (b) 200 (c) 250 °C. Various programmed states (up to PV= +4V) and erased states (up to EV= -2 V) with P/E cycle = 1 (fresh), 1K and 10K are tested. The testing devices are identical BE-SONOS capacitors with O1/N1/O2/N2/O3=15/20/25/70/90A.

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Step 1: Plot J-E

$$J = \frac{\varepsilon_0 \cdot \varepsilon_{ox}}{T_{Tox}} \frac{dV_{FB}}{dt}$$

$$E = \frac{(V_{FB} - V_{FB\_i}) \cdot \varepsilon_n}{T_{Box} \cdot \varepsilon_n + T_{Tox} \cdot \varepsilon_n + T_{SiN} \cdot \varepsilon_{ox}}$$

Table 2 The equations for obtaining the de-trapping current (J) and built-in electric field (E) from the baking retention data (V_{FB}-t). J is obtained by differentiating V_{FB} with respect to time (t). T_{BOX}, T_{TOX}, T_{SiN} are the equivalent oxide thickness of O1/N1/O2, O3, and N2, respectively. V_{FB_i} is the initial uncharged V_{FB} of BE-SONOS, which is close to 0 V for P+-poly gate.

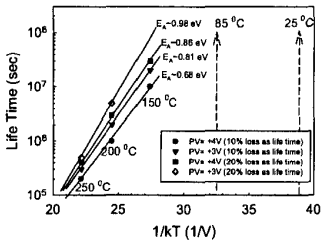


Fig. 9 Arrhenius plots for life time extrapolation. Life time is defined at 10 % or 20 % charge loss. Various definitions and PV states produce inconsistent results.

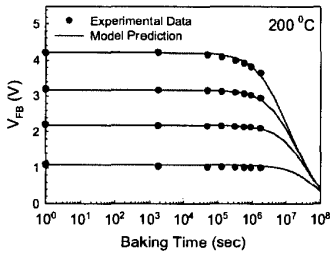


Fig. 12 Comparison of experimental and simulated retention data at 200 °C using the procedure in Table 4. The F-P parameters are identical to those in Fig. 10.

O1/N1/O2 (Å)	E_A (eV)	a (A/cm^2)	b
15/20/25	1.17	5E-4	0.90
13/20/25	1.18	6E-4	0.90
15/20/18	1.15	4E-4	0.88
13/25/25	1.17	8E-4	0.87

Table 5 The extracted F-P parameter for various ONO tunneling dielectrics. The parameters are very similar, indicating that BE-SONOS retention is insensitive to ONO tunneling dielectric. The long-term retention is determined by the intrinsic nitride trap property.

Step 2: Fit J-E

$$J = a \cdot Exp\left(-\frac{E_A - b\sqrt{qE_N / \pi\varepsilon_N\varepsilon_0}}{kT/q}\right)$$

Table 3 The Fenkel-Poole equation used to fit the extracted J-E plots at various temperatures. E_A is the activation energy that accounts for the temperature (T) dependency. b is the parameter that accounts for dependency on nitride electric field (E_N), where $E_N = E \cdot \varepsilon_{ox} / \varepsilon_n$
a is the parameter of proportional constant.

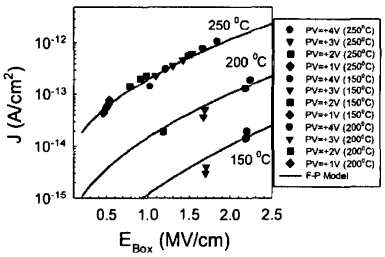


Fig. 10 The extracted de-trapping current (J) as a function of built-in electric field (E) in the bottom oxide at various temperatures and PV states. The line is the fitting results (Table 3) using Frenkel-Poole equation with E_A=1.17 eV, a= 5.1E-4 (A/cm^2), b=0.9.

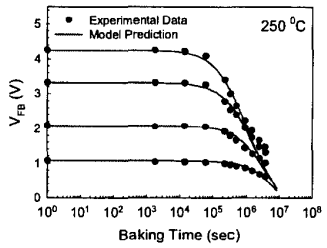


Fig. 13 Comparison of experimental and simulated retention data at 250 °C using the procedure in Table 4. The F-P parameters are identical to those in Fig. 10.

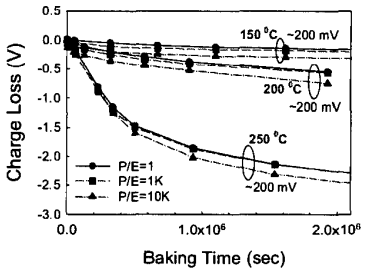


Fig. 15 Comparisons of charge loss for PV=+4V state at various temperatures. The P/E cycled devices show larger initial charge losses, but the charge loss rate converges with the fresh state, leading to a constant difference (~200 mV).

Step 3: Simulate V_{FB}-t

$$E = \frac{(V_{FB}(t) - V_{FB\_i}) \cdot \varepsilon_n}{T_{Box} \cdot \varepsilon_n + T_{Tox} \cdot \varepsilon_n + T_{SiN} \cdot \varepsilon_{ox}} \quad , E_N = E \cdot \varepsilon_{ox} / \varepsilon_n$$

$$J = a \cdot Exp\left(-\frac{E_A - b\sqrt{qE_N / \pi\varepsilon_N\varepsilon_0}}{kT/q}\right)$$

$$V_{FB}(t + \Delta t) = V_{FB}(t) - J \cdot \Delta t \cdot \frac{T_{OX}}{\varepsilon_0 \cdot \varepsilon_{ox}}$$

Table 4 The retention (V_{FB}-t) simulation methods. For any given V_{FB} (t), the built-in electric field and de-trapping current (J) are calculated. V_{FB}-t at any temperature and time can be obtained by iteration.

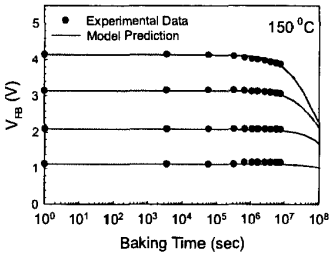


Fig. 11 Comparison of experimental and simulated retention data at 150 °C using the procedure in Table 4. The F-P parameters are identical to those in Fig. 10.

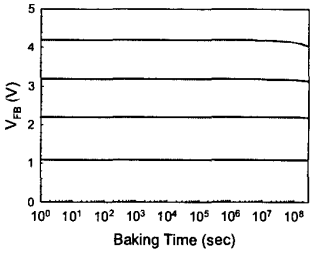


Fig. 14 Simulated retention data at 85 °C after 10 years. It shows only 300 mV charge loss for PV=+4V, and negligible charge loss for PV<=+3V.

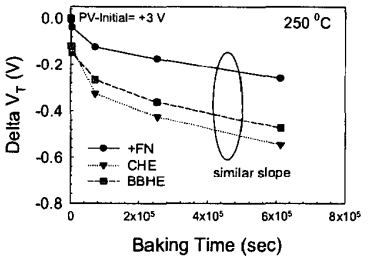


Fig. 16 The retention comparisons of +FN, CHE and BBHE (p-channel device in Ref. [7]). PV is +2V referenced to the initial state. Hot-carrier injection shows a faster initial charge loss, but the long-term charge loss slope (J) is similar to +FN programming..

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An Experimental 5-V-Only 256-kbit CMOS EEPROM with a High-Performance Single-Polysilicon Cell

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Abstract — A 256-kbit (32K-words × 8-bit) 5-V-only electrically erasable and programmable read-only memory (EEPROM) with a high-performance cell has been developed. A unique single-polysilicon EEPROM cell, called DIFLOX (DIFfused Layer controlled floating-gate-type cell with thin Oxide), was applied to this memory. The floating-gate voltage is controlled by two thin oxide capacitors coupled with two N^+ diffused layers: the drain and the control gate. Its size is reduced to 86.25 μm^2 by exploiting 1.2-μm photolithograph and scaled transistors with 1.4-μm gate length. For programming time reduction, a PAGE-MODE programming scheme was applied. Successive data of up to 16 bytes are loaded into internal storage and are programmed simultaneously. All high voltages needed to perform the ERASE/PROGRAM (E/P) function are generated internally, and two kinds of timers were designed using an improved switched-capacitor technique. Owing to the open-bit-line scheme, cell data were detected with high sensitivity in spite of the large bit- and word-line parasitic capacitance. The EEPROM offers typically 150-ns address access time, 80-mW active and 1-μW standby power dissipation. It was successfully fabricated in a single-polysilicon and single-metal CMOS process. The chip is 7.33 × 6.23 mm^2 and is packed into the DIP 28 pin, which is pin-to-pin compatible to 256-kbit SRAM.

I. INTRODUCTION

RECENTLY, electrically erasable and programmable read-only memory (EEPROM) has been developed by the electronic industry due to its in-system reprogramming capability. So far, several kinds of devices up to 64 kbits [1]–[8] have been intensively demonstrated. They have one standardization of 5-V-only operation, which is achieved by the internal generated high voltage taking advantage of extremely low current consumption for their ERASE/PROGRAM function. On the other hand, they revealed many diversities, too. One was demonstrated to have high-reliability characteristics, such as over 10^6 endurance with on-chip ECC, or extended temperature operations. Another aimed at high-speed access time competitive with the bipolar PROM. And there is a synchronous EEPROM like microprocessors operated by some commands. However, in order to apply the nonvolatile mass storage for microcomputer peripherals, it is necessary to achieve high-density EEPROM with lower cost, in addition to ease of use and high reliability. For this purpose, a small-sized cell with a simple structure is required. Utilizing the electron tunneling through thin oxide from the bulk to the floating gate, several types of cells aiming to be used for a large bit capacity EEPROM were reported [9], [10]. One of the most popular structures is composed of two transistors, that is the select transistor and the floating-gate transistor, fabricated in a double-polysilicon process. In order to gain larger capacitance coupling between the control gate and the floating gate within the limited stacked area, it is necessary to decrease the interpolysilicon oxide thickness. However, this is accompanied by several fabrication difficulties such as the asperity growth, affected by the impurity concentration of polysilicon and the annealing condition [11]. Of course, there are some attempts for obtaining thin dielectric films by use of an oxide–nitride–oxide structure. However, one of the simplest approaches for size reduction is to use the single-polysilicon structure, since the larger capacitance coupling with the control gate can be obtained through a reliable thin oxide on bulk without sacrificing large cell area. In addition, no special technique is required. Previously, a single-polysilicon cell for 2-kbit EEPROM was reported [12]. However, it occupied 440 μm^2, rather larger than the double-polysilicon ones, because it was designed for compatibility with the logic circuits.

In the high-density EEPROM, there are several hedges to achieve the design goal besides the cell area reduction. One is the data detection technique, as a large parasitic capacitance affects the small signal generated by the scaled cell, which has a comparatively low drive capability. The second is the ERASE/PROGRAM time reduction, because it increases proportional to the bit density. Utilizing a differential amplifier constructed by a CMOS current mirror circuit or a bipolar one is a way to detect small bit-line signals [13]–[15]. However, as is used for high-speed or high-density SRAMs [16], the internally synchronous approach is one of the promising methods for single-ended bit-line cells such as EPROM's and EEPROM's. In particular, the scheme has a good compatibility with the

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PAGE-MODE programming function, which is effective in reducing the ERASE/PROGRAM time.

This paper describes a 256-kbit 5-V-only EEPROM fabricated by a single-polysilicon and single-metal CMOS process. The cell structure will be revealed in Section II. The READ and ERASE/PROGRAM scheme of this memory will be explained in Sections III and IV, respectively. The measurement results of the device will be given in Section V.

II. Cell Structure

In this paper, the ERASE state is defined as the positive threshold shift of the floating-gate transistor, and the PROGRAM state is the negative. The electric field between the floating gate and the drain, which dominates the Fower–Nordheim current flow, is approximately given by

$$E = \frac{C_2 V_{CG} - (C_2 + C_3) V_D - Q_F}{d_1 C_T} \qquad (C_T = C_1 + C_2 + C_3)$$

where

- Q_F stored negative charge on the FG,
- C_1 thin oxide capacitance,
- C_2 control-gate capacitance,
- C_3 gate oxide capacitance,
- V_{CG} control-gate voltage,
- V_D drain voltage, and
- d_1 thin oxide thickness.

Now, we define an appropriate high voltage as V_{PP}. The ERASE conditions are $V_D = 0$, $V_{CG} = V_{PP}$, and the PROGRAM's are $V_D = V_{PP}$, $V_{CG} = 0$. A larger threshold shift ΔV_{th} is caused by a larger tunneling current, or a larger electric field. Although the most efficient way for increasing E is to increase V_{PP}, this approach is opposed to the reduction of the maximum applied voltage, which is required to achieve VLSI with higher packing density. So, it is natural to increase the ratio C_2/C_T or $(C_2 + C_3)/C_T$ to get sufficient ΔV_{th} with the limited applicable voltage and the thin oxide thickness.

Fig. 1 shows an optimized single-polysilicon cell layout for a high-density EEPROM, which is named DIFLOX (DIFfused Layer controlled floating-gate-type cell with thin OXide). It is composed of a select- and a floating-gate transistor. The floating-gate voltage is controlled by the capacitance coupling of the N^+ diffused layer and the drain through thin oxide. A large capacitance coupling value between the N^+ control gate and the floating gate can be obtained with this structure. The capacitance ratio C_2/C_T is mainly determined by the thin oxide area ratio, as the thin films are formed simultaneously. The ratio of DIFLOX is designed as 0.83. The equivalent circuit of the DIFLOX cell array configurations is shown in Fig. 2. The program line PL is connected to the diffused control gate via a transfer gate, which is controlled by the word line. It is to be noted that the N^+ region of the control gate is common to only one byte (eight cells). The N^+ implantation dose for this region must be chosen carefully. A lower concentration suppresses the effective applied voltage to the thin oxide in the negative gate bias condition, while a higher concentration lowers the barrier height of the thin oxide [17]. Under the optimized concentration applied to DIFLOX, the resistance and junction capacitance of the N^+ control-gate region were measured to be 20 kΩ and 14 fF, respectively. So the RC time constant is calculated to be lower than 1 ns, and the delay caused by this diffused layer is not a dominant factor on the access time.

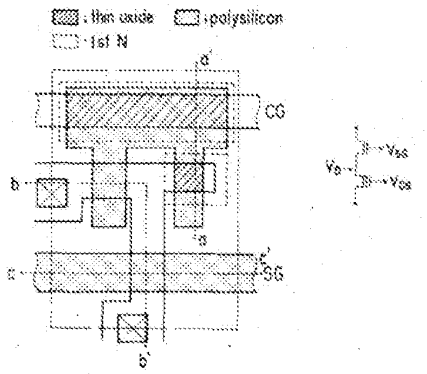


Fig. 1. Layout pattern of a new single-polysilicon EEPROM cell, named DIFLOX. The cell is composed of a select-gate and a floating-gate transistor.

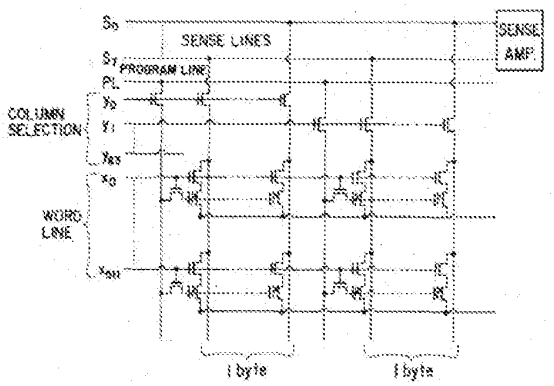


Fig. 2. Cell arrays of DIFLOX. The select gate is equivalent to the word line, and the control gate is connected to the program line (PL) via a transfer gate transistor.

To reduce the cell area of DIFLOX, the isolation between active regions is one of the most important technologies. A new isolation technology, SEPOX [18], was applied to the cell, which can realize a field distance between the active regions as narrow as the minimum dimension determined by the photoetching. In addition to this technology, a high-voltage structure was contrived to perform the ERASE/PROGRAM function. Fig. 3 shows the cross-sectional views of DIFLOX, along the lines a–a', b–b', and c–c' in Fig. 1. As shown in Fig. 3(a), the high concentration N^+ below the thin oxide was covered with a lower doped zone of 0.2 μm thick. This structure improves the breakdown voltage of the p-n junction. In order to optimize the distance between the N^+ control gate and the drain, the field inversion effect under the floating gate

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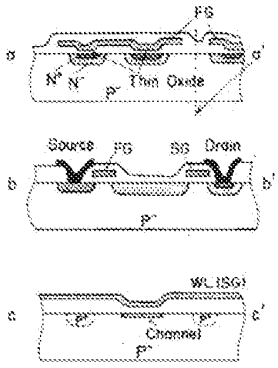


Fig. 3. Cross-sectional views of DIFLOX, along the lines $a-a'$, $b-b'$, and $c-c'$ in Fig. 1.

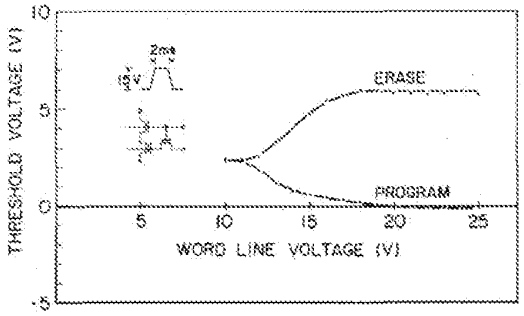


Fig. 5. Threshold shifts of DIFLOX in the ERASE/PROGRAM state as a function of a word-line voltage. $V_{PP} = 15$ V, $d_1 = 85$ A.

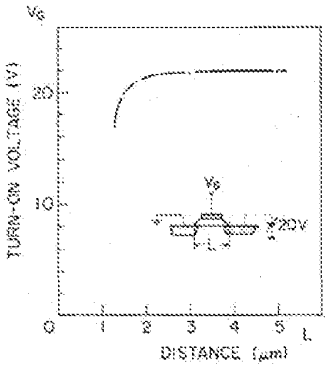


Fig. 4. Turn-on voltage of the field transistors as a function of the distance. It is defined as the leakage current exceeding 10^{-10} A/μm. The drain is biased to 20 V.

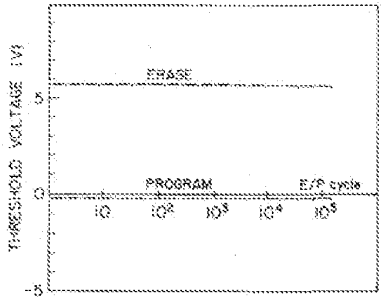


Fig. 6. Endurance characteristics of DIFLOX. $V_{PP} = 15$ V, $d_1 = 85$ A, $V_{WL} = 20$ V.

must be counted. By defining the turn-on voltage as the gate voltage at which the leakage current exceeds 10^{-10} A/μm under a drain bias of 20 V, the field turn-on voltages as a function of the length are measured as shown in Fig. 4. It is indicated that a 2-μm field length can guarantee the 15-V ERASE/PROGRAM operation. To eliminate the leakage current from the drain regions of the select- and floating-gate transistors to the substrate due to the avalanche breakdown, the source and drain of the select-gate transistors were doped with a low impurity concentration of 10^{17}/cm^3, as shown in Fig. 3(b). The value is about one order of magnitude lower than the usual lightly doped drain (LDD), used for 1.2-μm NMOS FET for 5-V circuits [21]. In order to reduce the contact resistance between the aluminum and the N^+ region, a high dose implantation of arsenic was carried out through the contact holes. This self-aligned formation of the diffusion area contributes to the cell area reduction. Only the source of the floating-gate transistor was formed by N^+, as is used for 5-V circuits.

In order to be able to design the peripheral circuits, the characteristics of the cell in the array of Fig. 2 must be analyzed. The V_{th} shift of DIFLOX cell in the erased and programmed state as a function of the select-gate voltage is shown in Fig. 5. The thin oxide thickness d_1 is 85 A, and a pulse of 15 V height, 2 ms width is provided to the program line or bit line. To obtain the wider threshold window, or eliminate the degradation by the select gate, the word-line voltage should be elevated above 20 V. This voltage might be achieved as it was. However, in order to take some margin, as is taken in the case of the drain control-gate voltage design, heavy channel-stop ion implantation was carried out between the select gates as shown in Fig. 3(c).

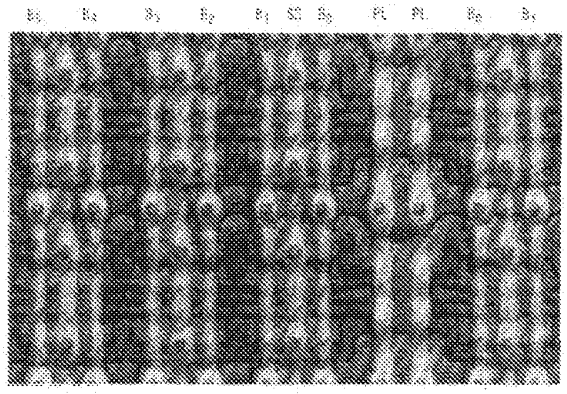
The read current measured with $V_{PL} = V_{BIT} = 2.5$ V and the word-line voltage $V_{WL} = 5$ V exceed 100 μA in the conductive state by employing 1.4-μm gate length, in spite of the series connection of two high-voltage transistors. The endurance characteristics of DIFLOX are shown in Fig. 6. Although it uses larger thin oxide area than the conventional double-polysilicon cells, no characteristics' degradation could be observed up to 10^5 ERASE/PROGRAM cycles.

The charge retention characteristics would be drastically degraded, if a thin oxide thickness of below 60 A were used, because of the direct tunneling effect of oxide. However, up to the thickness, the retention characteristics are mainly dominated by the barrier height of polysilicon oxide, surrounding the floating gate, rather than that of thin oxide [17]. So, the cell can guarantee the same retentivity as the conventional UV EPROM cell.

The microphotograph of the DIFLOX cell array is shown in Fig. 7.

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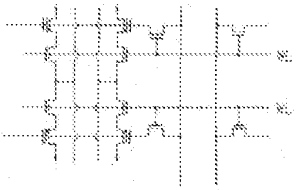


Fig. 7. Microphotograph of DIFLOX cell array. The cell size is 7.5× 11.5 μm.

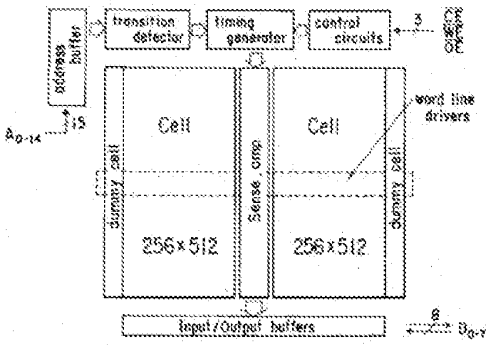


Fig. 8. Block diagram of 256-kbit EEPROM in the READ operation.

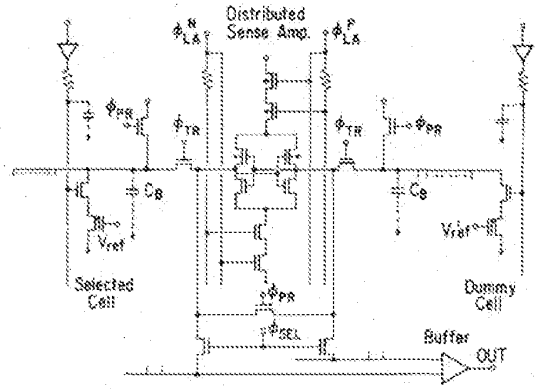


Fig. 9. Cell peripheral circuitry. Improved open-bit-line scheme and distributed sense amplifiers are shown.

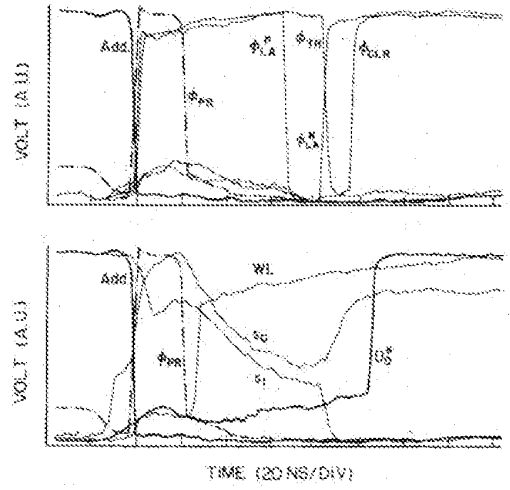


Fig. 10. Monitored waveforms of internal nodes, observed by the electron beam tester. s_0 and s_1 are two nodes of a sense amplifier, and D_0^* corresponds to the output signal before one buffer. The voltage levels are incorrect, not only absolutely, but also relatively, because they are disturbed by the electron scattering of neighbor patterns.

III. Open Bit-Line Structure

In order to compensate the large bit-line parasitic capacitance, an open bit-line scheme was improved and applied to the EEPROM. The block diagram of the memory in READ operation is shown in Fig. 8. The cell arrays are divided into left and right hemispheres, and the sense amplifiers are located between them. Every bit line has 256 cells and one dummy cell. When the memory cell on a hemisphere is selected, the dummy cell on the other side is selected as a reference. The cell peripheral circuitry in the READ operation is shown in Fig. 9. At the transition edge of the address input signals, the precharge pulse Φ_{PR} is generated internally. It precharges bit-line pairs and their corresponding sense-amplifier nodes, and equalizes them, simultaneously. The successive clocks triggered by Φ_{PR} control all of the reading procedure as follows. In the period of the precharge, the bit lines are raised to $V_{DD} - V_{th}$. The level is estimated to be 2.5 V by the body effect of NMOS FET. All word lines including the dummy cell's are biased to zero. When Φ_{PR} goes low, the selected- and the dummy-cell word lines are raised simultaneously. So, both bit-line levels begin to fall gradually, according to the conductance of the selected and dummy cells. As no pull-up devices are activated, the level variation in this free-running state is expected to be fast. In addition, the effect of the equivalent parasitic capacitances connected to the bit-line pairs compensate each other. After an appropriate period, Φ_{LA}^{p} goes low and then Φ_{LA}^{n} goes high. In other words, the sense amplifiers are activated, and the bit-line data are boosted by them. Finally, Φ_{TR} goes low and the bit lines are isolated from the sense amplifiers. In the quiescent state, as Φ_{CLR} goes high, the bit lines are biased to zero in order to eliminate the idle current and to avoid cell data destruction by noise. The program line *PL* is kept about 2.5 V during the READ operation. These internal timings of READ mode were verified by the tester with electron beams, as shown in Fig. 10. It is important for these open-bit-line schemes to synchronize the bit-line

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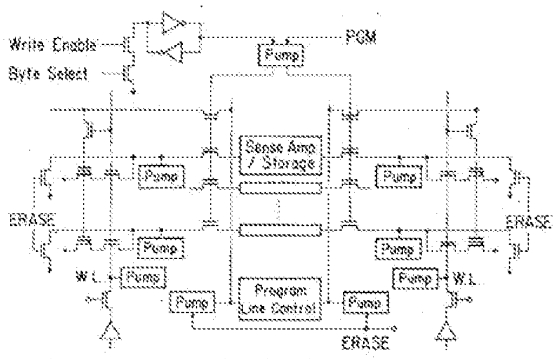


Fig. 11. Cell peripheral circuitry in ERASE/PROGRAM operation.

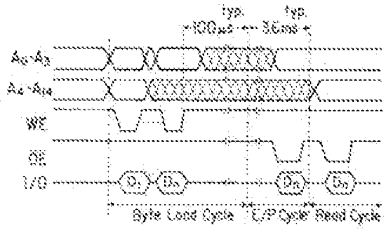


Fig. 12. Timing chart of the PAGE-MODE programming and the data polling.

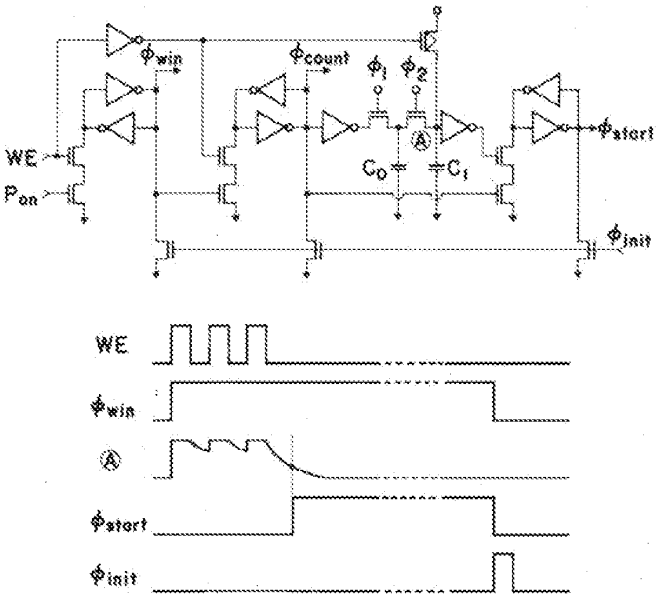


Fig. 13. Successive data loading control circuits (Φ_{start} generator). A period of 100 μs is counted by the switched capacitor.

signal variation associated with the word-line delay to the activation of sense amplifiers. So, a scheme of distributed sense amplifiers was applied. The activation of sense amplifiers is designed to depend on the distance from the word-line drivers, by adjusting the gate capacitance and the line resistance. This enables the bit-line data to be latched just at the time when the voltage difference reaches an appropriate level, wherever it may be located. It also reduces the large current peak caused by the sense-amplifier activation.

It is necessary for the nonvolatile memories that the logical data coincide with the physical data, which is different from the case of the RAM. Therefore the final output data are inverted on the buffer if they come from the left hemisphere. So the data in the chip clear state, which is defined as all cells in positive threshold, correspond to all one.

IV. ERASE/PROGRAM CONTROL CIRCUITS

The PAGE-MODE programming gives one solution to reduce the ERASE/PROGRAM (E/P) time. This feature applied to the 256-kbit EEPROM allows programming up to 16 byte (128 bits) simultaneously. The scheme fits into the open-bit-line structure, since the flip-flop which acts as a bit-line sense amplifier in the READ mode plays the role of a temporary storage for programming data, shown in Fig. 11. Therefore the data can be written in almost the same timing as a SRAM. The timing chart of E/P procedure is shown in Fig. 12. Once the WRITE ENABLE *WE* is detected by the chip, all the sense amplifiers are activated and isolated from the bit lines. The programming data are loaded to the latches successively. If the time, 100 μs, lapses without any *WE* input, the chip goes into the ERASE state automatically. In this state, the bit lines are biased to zero and the program lines of the selected columns are elevated to V_{PP}. Therefore the data of the selected cells are erased. Next, the chip turns in the PROGRAM state. Φ_{PR} goes high and the stored data are transferred to the bit lines. The charge pumps only elevate bit-lines of logical high to V_{PP}. As the *PL* is biased to zero, the programming is performed on the corresponding cells. As each byte storage has one additional flag latch, the E/P procedure is performed only on bytes that are actually being programmed.

The data polling function, shown in Fig. 12, is accomplished by reading the stored data on the sense amplifiers during the E/P state, which are inverted from the data to be read.

The timing circuits constructed by the switched-capacitor technique take care of the complicated E/P procedure. This technique is widely applied to recent MOS analog circuits such as digital filters [19], [20]. The lapse of the 100-μs waiting time for successive *WE* pulses is controlled by the Φ_{start} generator circuit as shown in Fig. 13. The rising and falling edges of the first *WE* pulse under an appropriate applied voltage V_{DD} above 4 V (P_{on} is high) cause two control signals, Φ_{win} and Φ_{count}, respectively. Φ_{win} initiates the flip-flops including flag latches, and Φ_{count} activates internal oscillator of 10 MHz and raises V_{PP}. This basic clock goes to some high-voltage pumps, and generates nonoverlap pulses Φ_1 and Φ_2. The voltage of node *A* falls gradually with the discharge of the capacitor. The *RC* time constant is calculated from the switched-capacitor theory as C_1/fC_0, where f is the frequency of Φ_1 and Φ_2. Every time the *WE* pulse becomes

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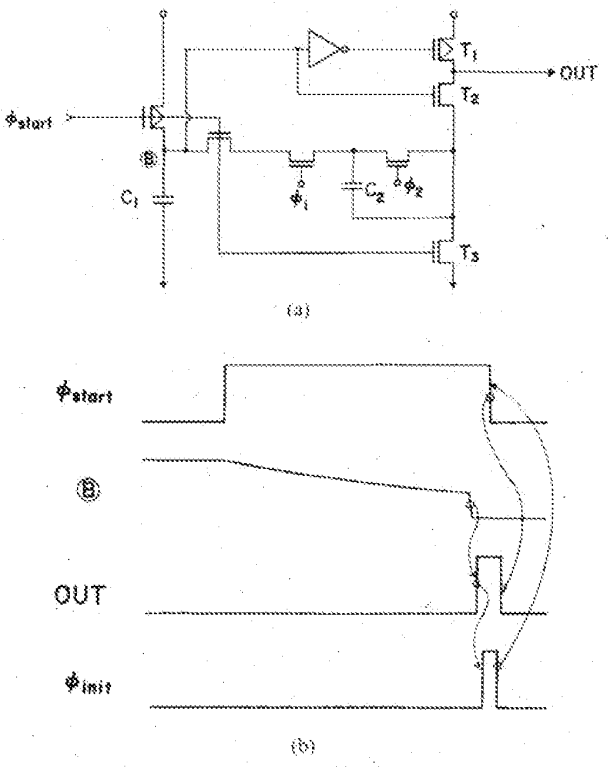


Fig. 14. (a) Timer circuit for ERASE/PROGRAM. Improved switched-capacitor technique is applied. It counts 1.8-ms lapse time. (b) Continued.

high, the capacitor C_1 is charged, or the state is initialized. At the crosspoint of the falling edge of node A and the threshold voltage of the next inverter, the clock Φ_{start} is generated. This Φ_{start} makes all E/P circuits active and initiates the second timer which controls longer time for E/P, as is shown in Fig. 14(a) and (b). This second timer designed by using a modified switched-capacitor technique counts the millisecond-order ERASE and PROGRAM time within the reasonable capacitance occupied area. In contrast with the conventional one, the voltage drop through the discharge capacitor C_2 is determined by the conductance ratio of two transistors, T_2 and T_3. In other words, the combination of higher conductance of T_2 and lower conductance of T_3 keeps the drain of T_3 high and makes the amount charge pumped out of C_1 small. Consequently, by adjusting the conductance ratio of T_2 and T_3, the capacitance area was reduced to about one-tenth in comparison with the conventional technique.

Figs. 15 and 16 show the drivability characteristics of the internal high-voltage generator and the pumping circuits. To supply sufficient current, this high-voltage generator (Fig. 15) has a comparatively low output impedance. The output terminal is clamped by the series connection of diodes for regulation. The rise time of this high voltage does not affect the thin oxide stress. On the other hand, the pumps (Fig. 16), which are attached to every bit and word line, have relatively small drive capability, which results in the decrease of the rising speed of the voltage for

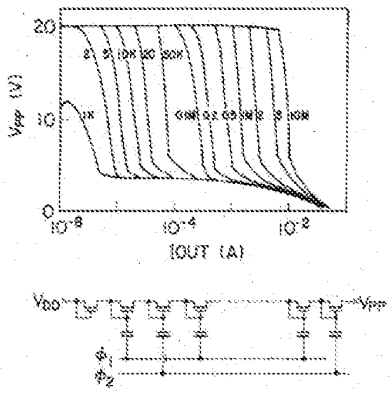


Fig. 15. Output characteristics of high-voltage generator. In the memory, the basic frequency of the internal oscillator is set to 10 MHz.

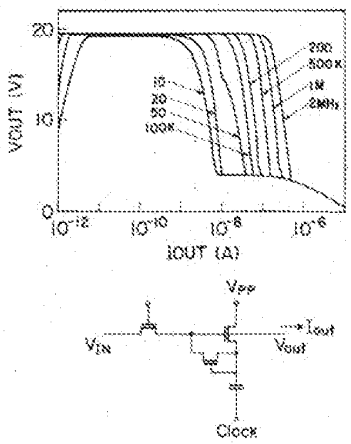


Fig. 16. Output characteristics of high-voltage pump. It is attached every bit and word line.

the lines connected to the tunnel oxides. The rise time was measured as 50 μs, and it reduces thin oxide stress.

V. Performance and Results

The microphotograph of the 5-V-only 256-kbit CMOS EEPROM is shown in Fig. 17. The die size is 6.23×7.33 mm and is packed into the DIP 28-pin standard package. It is pin-to-pin compatible with 256-kbit SRAM [21].

The chip contains several circuits which enable the chip clear and the READ margin check functions. They are activated by providing 12 V to appropriate pins.

The monitored waveforms of the internally generated V_{pp} and the E/P time control signal ϕ_{EP} and the WRITE ENABLE input clock $\overline{WE}$ are given in Fig. 18. It is indicated that V_{pp} is elevated to 20 V and that all the timings are well controlled corresponding to the PAGE-MODE programming. The total amount of the ERASE and PROGRAM time is 3.6 ms/16 byte at 5-V power supply.

The microphotograph of the address and data out waveforms with external 100-pF load is shown in Fig. 19. The address access time of 150 ns was successfully ob-

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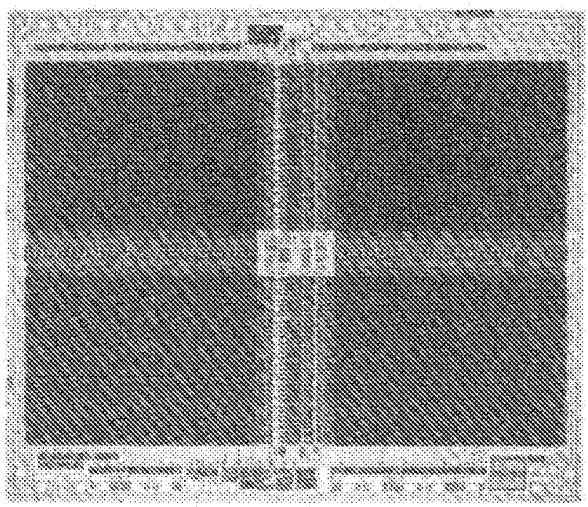


Fig. 17. Microphotograph of the whole chip of 256-kbit EEPROM. The size is 7.33 × 6.23 mm².

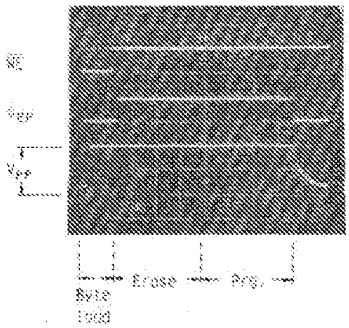


Fig. 18. The monitored waveforms of Φ_{EP} and V_{PP}. V_{PP} is elevated to 20 V.

tained with a nominal 5-V voltage supply. The active power dissipation is 80 mW. Similar to the other CMOS devices, the active power dissipation depends on the READ cycle time. It reduces to 35 mW at a 1-MHz READ cycle, and drops below 1 μW at the STANDBY mode.

The characteristics of this EEPROM are summarized in Table I.

VI. Conclusion

A 5-V-only 256-kbit CMOS EEPROM employing a new single-polysilicon cell, DIFLOX, has been successfully designed and fabricated. Exploiting 1.2-μm design rules and 1.4-μm gate length, the cell size was reduced to 86.25 μm². The cell was designed to eliminate any leakage current caused by the junction breakdown and the field inversion. The cell, which offers a 5-V threshold window between the ERASE and PROGRAM state, allows 100-μA reading current in the conductive state. It guarantees over 10^5 ERASE/PROGRAM cycles. By employing the PAGE-MODE programming, the EEPROM allows successive data load up to 16 bytes with the same timings as an SRAM. The ERASE/PROGRAM is carried out at once within 3.6 ms. All timings are controlled by several kinds of clocks, all of which are generated internally by timers constructed by the switched-capacitor technique. The improved open bit-line scheme was applied for the READ operation. This internally synchronous architecture fits with the PAGE-MODE programming, because the sense amplifiers are also used to share the internal storage of the programming data. Due to the CMOS circuit configuration, the chip offers extremely small standby power dissipation.

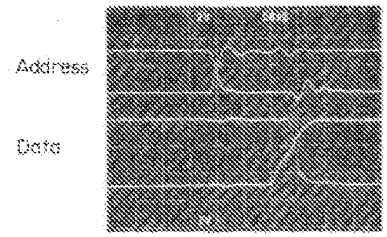


Fig. 19. The oscillograph of the address and data out waveforms with external loads.

TABLE I
Characteristics of 5-V-only 256-kbit EEPROM

Organization	32K words × 8 bit
Operation	Fully asynchronous (with internal clocks)
Technology	N-well CMOS (single poly & single Al)
Minimum gate length	1.4 μm
Gate oxide thickness	250 A
Thin oxide thickness	85 A
Cell size	86.25 μm²
Die size	7.33 × 6.23 mm²
I/O interface	TTL
Address access time	150 ns (typical)
Chip select-access time	150 ns (typical)
ERASE/PROGRAM time	3.6 ms (typical) (16-byte page)
Active power	80 mW 35 mW (1 MHz)
Standby power	1 μW
Package	28-pin DIP (256-kbit CMOS SRAM compatible)

Acknowledgment

The authors would like to thank T. Sako for his design support, and S. Tanaka and Dr. Y. Nishi for their encouragement throughout the work and useful suggestions.

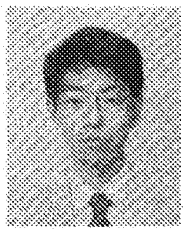
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Materials Science of Thin Films

Deposition and Structure

Second Edition

Milton Ohring
Department of Materials Science and Engineering
Stevens Institute of Technology
Hoboken, New Jersey



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6.8.3 Deposition and Structure of Amorphous Silicon Films

Amorphous silicon (a-Si) and hydrogenated versions of it, e.g., a-Si:H, are the basic materials discussed in this section. They have been deposited by both PVD and CVD techniques. Of the elements, silicon and others in column IV of the periodic table are among the easiest to prepare in amorphous form. Further, they do not require particularly low substrate temperatures (T_S) for their preparation. When normalized to the melting point (T_M), the ratio of T_S/T_M for amorphous CVD materials is higher by at least a factor of ~ 5 relative to what is required to amorphize typical PVD metal alloys. What accounts for the particular ease in amorphizing Si by CVD is the steric hindrance provided by molecular groups. Such structural obstruction leads to the high viscosity conducive to glass formation in bulk hydrocarbon polymers and oxide melts. In the case of a-Si:H films derived from SiH_4–H_2 mixtures, for example, the assorted radical and molecular fragments, e.g., SiH_3, SiH_2, Si_2H_6, are the source of the steric hindrance. A continuum of Si–H structures links the gas phase of $SiH_4 + H_2$ to the deposit surface. Contained within this transition region are assorted fragmented molecular species, which in turn connect to the film growth zone and eventually to the stable a-Si:H network beneath the film surface. Atom incorporation reactions are complex and not known with certainty (Refs. 53, 54); they resemble network polymerization of assorted Si_nH_{2n} molecular fragments and include dissociation and hydrogen desorption as well. The net result is the incorporation of as much as 35 at.% hydrogen (Ref. 55) into a silicon deposit disordered by bond stretching and distortion.

6.8.4 Amorphous Silicon Nitride

Silicon nitride is normally prepared by reacting silane with ammonia in an argon plasma, but a N_2/SiH_4 discharge can also be used. During plasma deposition, as much as 30 at.% hydrogen can be incorporated which apparently forms bonds to both Si and N. It is in this sense that silicon nitride is often described as a ternary solid-solution alloy, SiNH. Amorphous silicon nitride should be distinguished from the stoichiometric compound, Si_3N_4, formed by reacting silane and ammonia at 900°C in an atmospheric CVD reactor. It is instructive to further compare the physical and chemical property differences in three types of silicon nitride (Ref. 57), and this is done in Table 6-5. While Si_3N_4 is denser and more resistant to chemical attack and has higher resistivity and dielectric breakdown strength, SiNH tends to provide better step coverage. An upper temper-

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Table 6-5
Physical and Chemical Properties of Silicon Nitride Films from $SiH_4 + NH_3$

Property	Si_3N_4 1 atm CVD (900°C)	Si_3N_4(H) LPCVD (750°C)	SiNH PECVD (300°C)
Density (g/cm^3)	2.8–3.1	2.9–3.1	2.5–2.8
Refractive index	2.0–2.1	2.01	2.0–2.1
Dielectric constant	6–7	6–7	6–9
Dielectric breakdown field (V/cm)	10^7	10^7	6×10^6
Bulk resistivity (Ω-cm)	10^{15}–10^{17}	10^{16}	10^{15}
Stress at 23°C (GPa)	0.7–1.2(T)	0.6(T)	0.3–1.1(C)
Color transmitted	None		Yellow
H_2O permeability	Zero		Low–none
Thermal stability	Excellent		Variable >400°C
Si/N ratio	0.75	0.75	0.8–1.0
Etch rate, 49% HF (23°C)	80 Å/min		1500–3000 Å/min
Na^+ penetration	<100 Å		<100 Å
Step coverage	Fair		Conformal

Note: T = tensile; C = compressive.
Adapted from Refs. 56 and 57.
Stress data from S. M. Hu, *J. Appl. Phys.* **70**, R60 (1991).

limit that can be tolerated in some completed integrated circuits is ~300°C because interconnection metallizations begin to react with the surrounding insulation beyond this point. Since SiHN can be deposited at such temperatures and is an effective barrier against moisture penetration, it has been used to encapsulate IC chips.

Further aspects of the structure of amorphous elemental and alloy films, including silicon nitride, will be deferred to Section 9.6.

6.8.5 Ultrahard Thin Films

In this section we discuss films based on the three hardest substances known, diamond, boron nitride, and carbon nitride, and consider their deposition, properties, and uses. In common, they are all primarily produced by CVD methods. Diamond is by far the most important of these materials and is therefore given the greatest attention.

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A PLANAR TYPE EEPROM CELL STRUCTURE BY STANDARD CMOS PROCESS FOR INTEGRATION WITH GATE ARRAY, STANDARD CELL, MICROPROCESSOR AND FOR NEURAL CHIPS

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ABSTRACT

A Planar type EEPROM cell structure which consists of adjacently placed a NMOS and a PMOS transistors with an electrically isolated common polysilicon gate by standard CMOS process (no ultra thin oxide,no stacking of floating and control gates) is developed. 5 to 10 volts shifts of threshold and more than thousands cycles of endurance is obtained.This EEPROM cell can be easily integrated with Gate Array, Standard Cell,Microprocessor LSIs. This can store Analog data and be applied to Neural chips.

1. INTRODUCTION

BIOS and micro-codes for system controls are stored in EPROM or EEPROM chips and used with system control logic LSIs. Integration of EEPROM with logic LSIs, Gate Array, Standard Cell and Microprocessor bring many merits.But such integration requires EEPROM unique processings, ultra thin oxide, stacking of floating and control gates and others.

We developed a Planar type EEPROM cell structure by Standard CMOS process without any conventional EEPROM process. By this EEPROM cell structure, we can easily make EEPROM integratedGate Array,Standard Cell and Microprocessor LSIs with many merits of lower cost, more space saving and easier micro-code storing/updating, etc.

2. PRINCIPLE OF EEPROM OPERATION

Our developed Planar type EEPROM consists of adjacently placed NMOS and PMOS transistors with a common poly Si gate.The common gate is electrically isolated from another component. It works as "Floating Gate". The P+ diffusions and N well are wired together, and work as "Control Node". See Fig-1-A,1-B,1-C. Fig-1-A is the concept of this EEPROM cell, and Fig-1-B the physical structure. This EEPROM cell is symbolically expressed as shown in Fig-1-C.

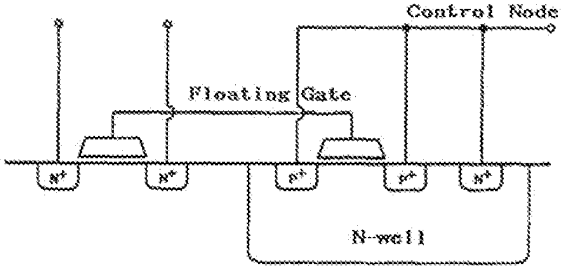


Fig-1-A : Concept

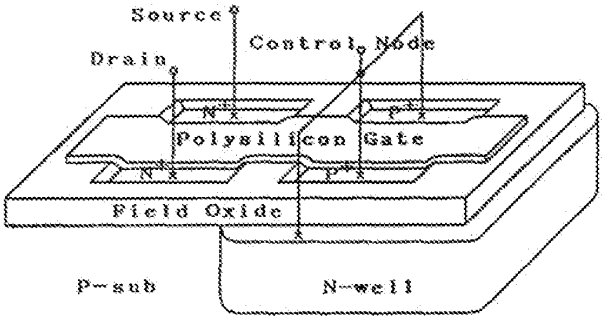


Fig-1-B : Physical Structure

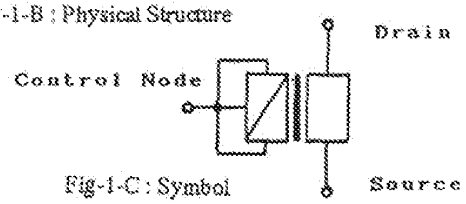


Fig-1-C : Symbol

2.1. WRITE OPERATION

There are two modes of Write operation as shown in Fig-2-A-1 and 2-A-2. One is by NMOS channel hot electron injection (NCHE Write) and the other by NMOS FN tunneling injection (NFN Write).

(A) NMOS Channel Hot Electron Injection (NCHE Write)

As shown in Fig-2-A-1, the source of NMOS is grounded, a medium voltage is applied to the drain and a high voltage Vp to the Control Node.Vp is divided by the series capacitances of PMOS and NMOS gates.A proper combination of the drain and Vp voltages is selected for channel hot electron injection into the FloatingGate, and the FloatingGate is negatively charged.

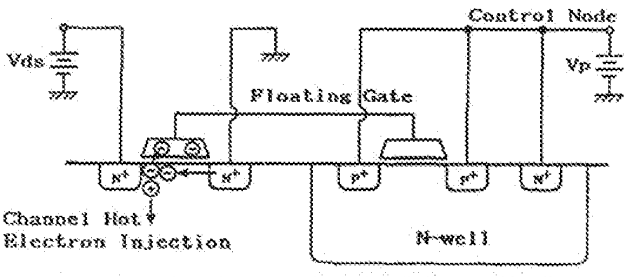


Fig-2-A-1 : Write Operation by NMOS Channel Hot Electron Injection (NCHE Write)

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(B) NMOS Gate FN Tunneling Injection(NFN Write)

The N+ diffusions of NMOS transistors are grounded, and a high voltage Vp is applied to the Control Node as shown in Fig-2-A-2. This mode is used when the gate capacitance ratio of CGP/CGN is larger than 2 or 3. Under this condition FN tunneling occurs in NMOS gate oxide. Many electrons are injected into the gate from N+ diffusions. The amount of injected electrons is determined by Vp and CGP/CGN.It is a linear function of Vp. This means that this mode can be used for Analog data storing. This EEPROM cell is applicable to Neural chips.

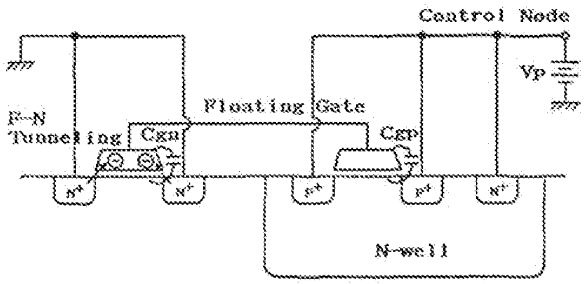


Fig-2-A-2 : Write Operation by NMOS F/N Tunneling (NFN Write)

2.1. READ OPERATION.

Read operation is done as shown in Fig-2-B.A medium voltage Vr is applied to the Control Node. When there is no charge on the Floating Gate, the NMOS transistor is in ON state. On the other hand, if the floating gate is negatively charged by the Write operation, the NMOS transistor is in OFF state. Sensing the ON/OFF state, the Read operation is done.

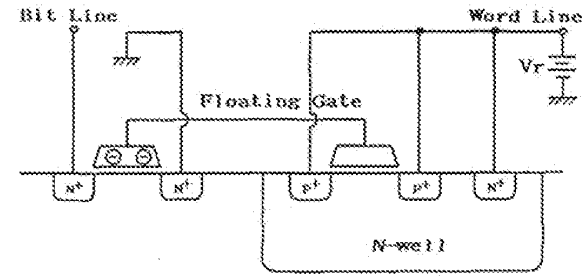


Fig-2-B : Read Operation

2.2. ERASE OPERATION

There are two modes of Erase Operation as shown in Fig-2-C-1 and 2-C-2. One is by FN tunneling in the oxide of PMOS, and the other by FN tunneling in the oxide of NMOS.

(A) PMOS Gate FN Tunneling (PFN Erase)

N+ diffusions of NMOS transistor are grounded, and a high voltage Ve is applied to the Control Node. When the gate capacitance ratio CGP/CGN is less than 1, the electric field across the PMOS oxide is larger and FN tunneling between the Floating Gate and P+ diffusions/channel occurs. And the charges on the Floating Gate are removed and the gate is recovered.

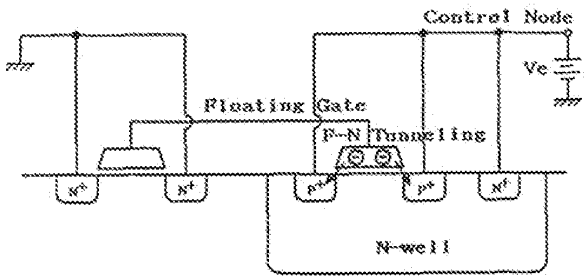


Fig-2-C-1 : Erase Operation by PMOS F/N Tunneling (PFN Erase)

(B) NMOS Gate FN Tunneling (NFN Erase)

As shown in Fig-2-C-2, the Control Node is grounded, and N+ diffusion of NMOS transistor are kept at a high potential Ve.The high electric field across the N+ diffusion and the Floating Gate causes FN tunneling. And the charges on the Floating Gate are removed.

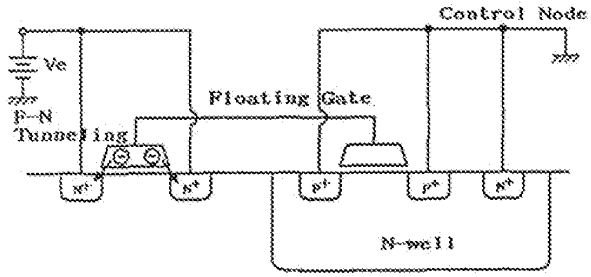


Fig-2-C-2 : Erase Operation by NMOS F/N Tunneling (NFN Erase)

3. EXPERIMENTS

Fig-3 shows the test chip.This is by standard 0.8um CMOS process, tox=150A, Ln=Lp=0.8um, EEPROM cells with various combination of NMOS and PMOS channel widths.

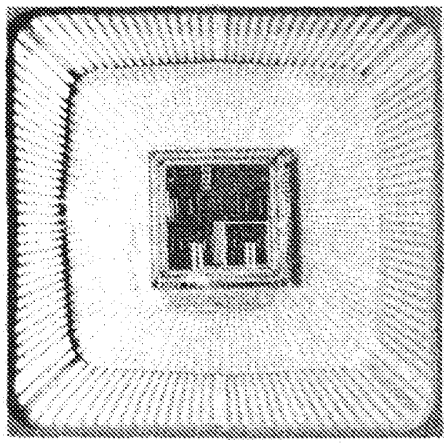


Fig-3 : Test Chip

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3.1. THRESHOLD VOLTAGE SHIFTS

The threshold voltage shifts of Write operation by NMOS Channel Hot Electron Injection (NCHE Write) is shown in the Fig-4-A. The gate capacitance ratio CGP/CGN=1.0. More than 9 volts shifts are observed at Vp=15V and Vds=9V. 5V shift is achieved at Vp=12V and Vds=8V. The write pulse duration is 100mS. When 10 mS, the shifts are 0.3 volts smaller.

Write operation by NMOS FN Tunneling Injection (NFN Write) gives the results in Fig-4-B. We see linear relations between the programming voltage Vp and threshold shifts. Larger ratio of CGP/CGN brings more shifts.

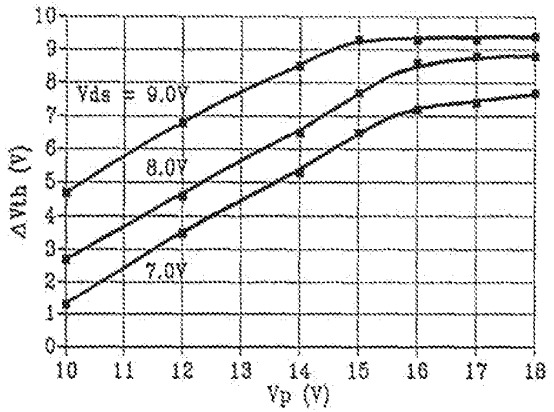


Fig-4-A : Vth Shift Characteristic (NCHE Write)

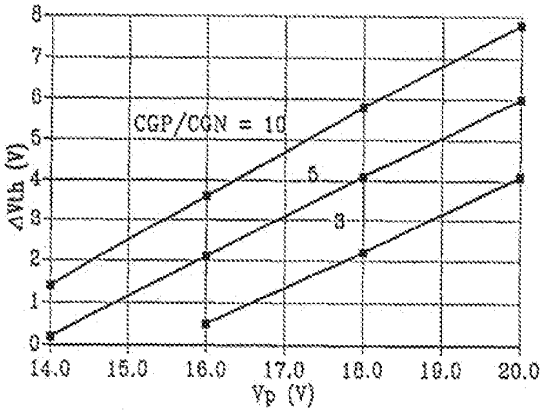


Fig-4-B : Vth Shift Characteristic (NFN Write)

3.2. ENDURANCE CHARACTERISTICS

In Fig-5-A, endurance characteristics of (NCHE Write + PFN Erase) is shown. The capacitance ratio CGP/CGN=2/3. The write is done at Vp=15V, Vds=9V with 10mS duration. Erase operation is done at Ve=18V with 100mS duration.

In Fig-5-B ,the endurance data of (NFN Write+ NFN Erase) is shown. The capacitance ratio CGP/CGN=5.0. Write is done at Vp=19V,Erase at Ve=14V with the same duration of 100mS.

After thousands cycles enough threshold voltage differences are obtained. This is the result of standard CMOS process. It is very enough for BIOS or micro-code storage.

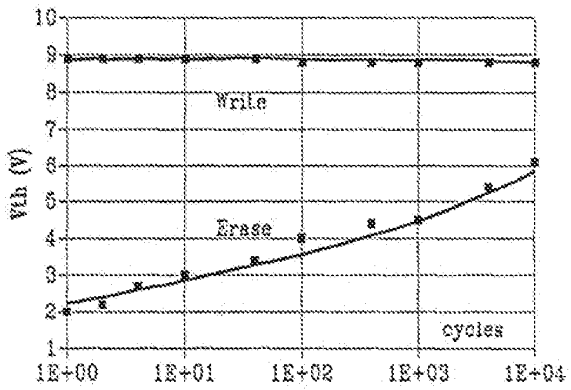


Fig-5-A : Endurance Characteristic (NCHE Write+PFN Erase)

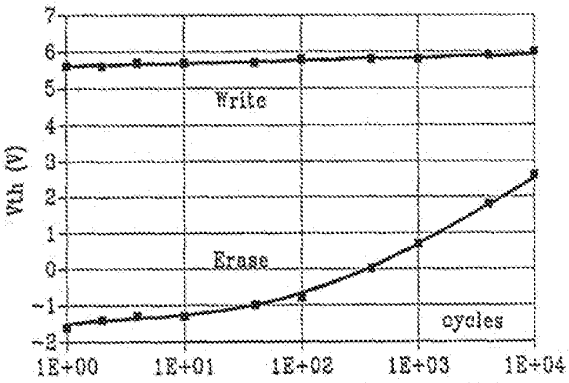


Fig-5-B : Endurance Characteristic (NFN Write+NFN Erase)

3.3. ENHANCEMENT OF ENDURANCE

The change of ERASE characteristic after thousands cycles is due to electron trapping in the oxide layer which reduces the electric field strength. This can be enhanced to some extent by optimizing erase potential Ve. Fig-6-A shows an endurance data by Ve optimization. Write was done at Vp=19V and 100mS by NFN write, erase at 100mS by NFN erase. The optimized Ve potential is shown in the Fig-6-B. A few more volts bring good erase characteristics (like in early erase cycles) after 10 thousands cycles. This kind of Ve control is easily done by on-chip circuits.

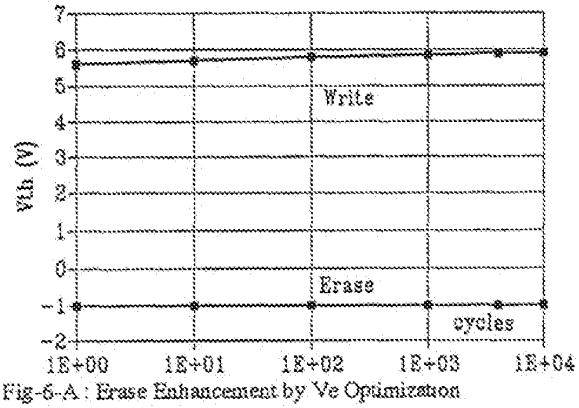


Fig-6-A : Erase Enhancement by Ve Optimization

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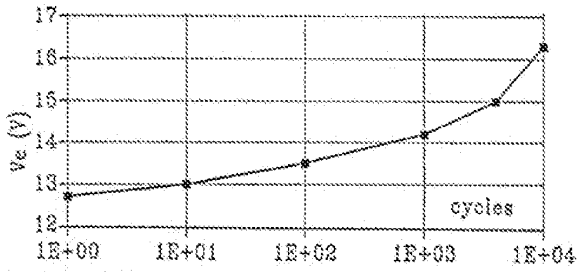


Fig-6-B : Ve Optimization

3.4. HIGH TEMPERATURE DATA RETENTION

In Fig-7 the high temperature data retention characteristic is shown. Assuming failure at 30% charge loss and the activation energy of 1.4eV, the life under 85 degree C is more than thousands years.

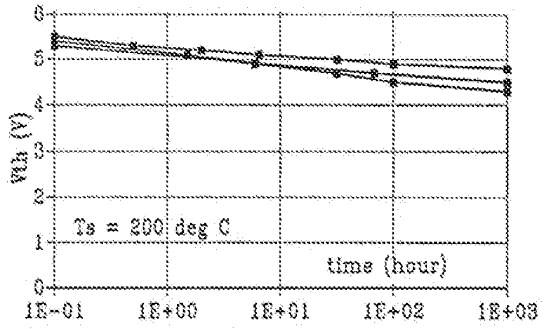


Fig-7 : High Temperature Data retention

4. APPLICATIONS

Almost all systems and sub-systems are software controlled and the software codes are stored in separate chips of EPROM or EEPROM. The size of such codes are small, a few KBytes. And a number of Write/Erase cycles is very small, less than 10. By integrating this EEPROM cells into Gate Array, Standard Cell and Microprocessor,we can enjoy many merits. Utilization of standard CMOS process line brings no cost increase in chip manufacturing. And lower cost in system/sub-system manufacturing, space saving (compact), easy micro-code storing and updating through LSI data bus, etc. are achieved.

The endurance can be greatly enhanced by oxide process optimization. And applications to NVRAM are possible too.

4.1. EEPROM ARRAY CIRCUIT

An example of EEPROM array circuit is shown in Fig-8-A. A control node is wired to a specific "Word Line", a drain to a "Bit Line", a source to a "Virtual Gnd Line" respectively. The Bit Line BL(i) is shared by Cell(i,j)-upper and Cell(i,j)-lower, the Virtual GND Line VGND(i,i+1) by Cell(i,j)-lower and Cell (i+1,j)-upper.

The principles of the circuit operation are described in Fig-8 -B. Selection of Cell(i,j)-upper or Cell(i,j)-lower is done by controls of VGND(i-1,i) and VGND(i,i+1). In Write / Read phases, VGND(i-1,i) and BL(i) are shorted and drived by same signals when Cell(i,j)-lower is selected, BL(i) and VGND(i,i +1) when Cell(i,j)-upper.The controls (Cell(i,j)-lower selected) in Fig-8-B is by NCHE write mode and PFN erase mode. Other combinations of Write and Erase modes are possible. Erase is done from WL to WL.

An example of this array is shown in Fig-9.

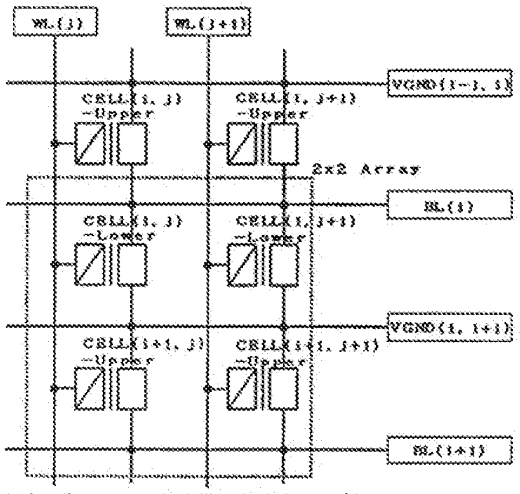


Fig-8-A : Example of EEPROM Array Circuit

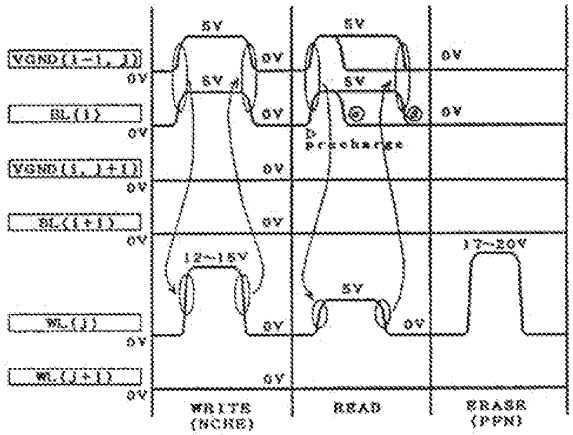
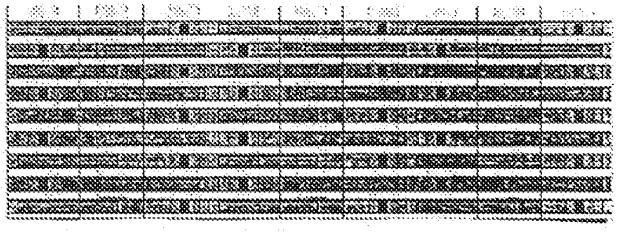


Fig-8-B : Control Signals


Fig-9 : Example of EEPROM Array

4.2. ANALOG DATA MEMORY

As shown in Fig-5-A, this EEPROM cell can store analog data by NFNwrite mode.The threshold shift is a linear function of the programming potential Vp. Precise Neural circuits are realized by this EEPROM cell structure.

ACKNOWLEDGEMENT

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Cypress SONOS Technology

Cypress Semiconductor White Paper

By Krishnaswamy Ramkumar

Executive Summary

This white paper discusses the key features of Cypress SONOS technology, its performance, and reliability. It also presents a comparison between the SONOS technology and other Flash technologies.

Introduction

The demand for embedded Flash memory in System-on-Chip (SOC) designs has grown steeply in recent years as newer applications evolve in communications and consumer electronics. The memory content of complex SOC has increased due to increased demand on system performance. Flash memory is highly desirable in most applications to store critical data and code. Flash memory in a SOC enables field programming that provides great flexibility for the end user to make system level changes through software. Cypress's Programmable System-on-Chip (PSOC) is a great example of a versatile SOC whose functionality can be modified by code stored in the embedded flash memory. SOC designers, however, require the Flash memory to easily integrate with the rest of the circuitry without impacting the existing IP blocks so that existing design IP can be re-used. This requirement is challenging and was a barrier for the growth of SOCs with Flash memory.

SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) technology has been known as a Flash technology since the 1980s. However, in the past it was not very successful in competing against the floating gate technology for standalone nonvolatile memories. In recent years, with the increasing demand for embedded nonvolatile memory, SONOS, being easier to integrate with the logic technology, is becoming very attractive.

This document provides an overview of the Cypress SONOS technology, its features, and its integration into a logic process flow.

Flash Memories

Nonvolatile memories (NVM) retain stored information even if the power supply to the memory is switched off. There are different types of nonvolatile memories including Flash, read-only memory (ROM), one-time programmable (OTP), and multiple-time programmable (MTP) memories. Flash memory is the most versatile because it can be programmed and erased thousands of times with no degradation in the sense margin and data retention performance.

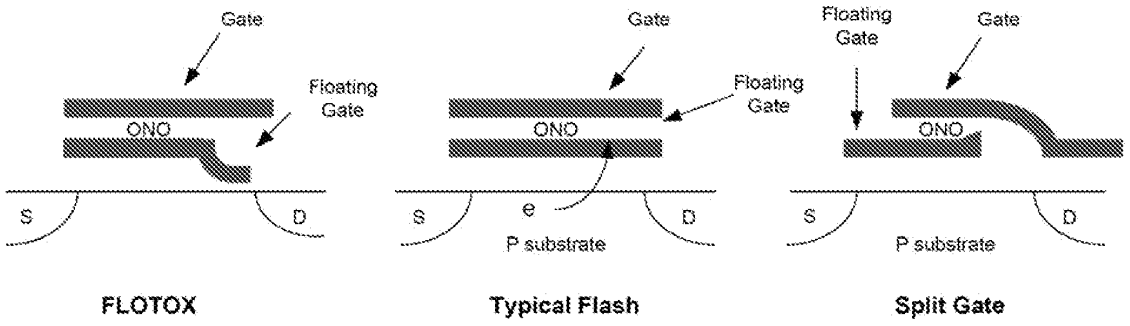
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Floating Gate Flash Memory Technology

Flash memory technology has evolved over the last 30 years to meet the demand for higher density and improved performance. Starting from UV erased PROMs, they have now evolved into page erased EEPROMs. Figure 1 shows the cross section structures of key Flash memory cells developed in the last 30 years. The charge storage layer is the same in all the generations. A floating gate in a metal-oxide-semiconductor field-effect transistor (MOS FET) is used to store the charge. The floating gate is sandwiched in between the channel and the control gate. It is separated from the channel by a thin tunnel oxide and from the control gate by an ONO dielectric. The method of injecting (programming of memory) and removing (erasing of memory) charge from the floating gate can be different and has led to different families of Flash memory.

The charge is injected from the channel to the floating poly through the "tunnel oxide." The injection is either by direct Fowler–Nordheim (FN) tunneling or channel hot electron injection (CHEI). The erasing is typically done by FN tunneling of the required type of charge from the channel to the floating gate. The FLOTOX cell uses a thin tunnel oxide at one end of the channel to enable FN tunneling of carriers. The more typical Flash cell has a device with thicker tunnel oxide but uses CHEI for programming. The split gate cell uses the same mechanism to program or erase but has a different structure.

Figure 1. Cross Section Structures of Flash Memory Cells



There are two types of Flash memory depending on the memory cell: NAND and NOR. The comparison of the two types is given in the following table. Floating gate Flash memory of both types is available from many manufacturers.

Table 1. Comparison between NAND and NOR Memory Cells

	NAND	NOR
Read access	Serial	Random
P/E methods	CHEI/FN	CHEI/FN
Cell size (F^2)	5–6	10–12
Application	Data storage	Code storage

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SONOS or Charge Trap Memory Technology

Interest in SONOS has increased in recent years because the scalability of floating gate NVM technology is reaching its limits beyond the 45 nm node. One of the challenges stems from the need to isolate the floating gate from surrounding layers. When device dimensions shrink, the insulating layers surrounding the gate must also shrink. This leads to increased capacitive coupling between memory bits and greater likelihood of small "pinhole" manufacturing defects in the insulating layers, creating a discharge path. The second challenge that arises from shrinking dimensions is the increasing mismatch between the voltage needed to cause tunneling and the normal circuit operating voltage. As the technology shrinks, circuits must operate at lower voltages to avoid device damage, but the voltage needed to induce tunneling does not drop proportionately. This makes it increasingly difficult to integrate erase and write circuitry into the rest of the memory device. The voltage mismatch also increases the likelihood of long term damage to the floating gate transistor with each write/erase cycle, an effect known as "wear out."

In contrast to the floating gate type, a SONOS memory uses an insulating layer such as silicon nitride with traps as the charge storage layer. The traps in the nitride capture the carriers injected from the channel and retain the charge. This type of memory is also known as "Charge Trap Memory." Since the charge storage layer is an insulator, this storage mechanism is inherently less sensitive to the "pinhole" defects and more robust for data retention. One of the key advantages of SONOS technology is the relatively low voltages required for program/erase as compared to Floating gate Flash. However, the retention performance of SONOS has been questioned in the past. SONOS also did not have multi-level or multi-bit capability previously. A very significant research effort has been underway the last 10 years to further improve the reliability of SONOS and develop multi-level and multi-bit capability. Much of the research effort is focused on the SONOS stack, where band gap engineering of ONO layers, high K dielectrics and metal gates have been evaluated. However, most of the SONOS technology in volume production still uses conventional materials such as silicon dioxide and silicon nitride. This technology is currently used in high volume manufacturing mainly for stand alone Flash memories. These memories typically use hot electron injection (HEI) mechanism for programming and Hot Hole injection or Band to Band Tunneling for erasing. They meet all the performance and reliability requirements and also have multi-bit capability.

Overview of Cypress SONOS Technology

Cypress's SONOS technology is an embedded nonvolatile technology that integrates the highly reliable SONOS transistor into a CMOS process flow with minimum additional mask layers and minimal impact on the electrical parameters of the existing CMOS FETs. Cypress uses a unique process for the SONOS transistor to achieve superior reliability. With integration simpler than that of floating gate Flash, the Cypress SONOS technology can enable a faster ramp to a high yield process flow. This technology is qualified in Cypress manufacturing plants and in multiple foundries. The Cypress SONOS cell is highly suitable for designing and manufacturing EEPROM and embedding Flash memory into logic integrated circuits. The Cypress SONOS technology uses fewer mask layers than floating gate technology. It is very compatible with CMOS logic technology, which makes it ideal for embedded Flash. Cypress SONOS technology has been in production since 2001 and over a billion chips that have true e-flash have been shipped to customers so far. The 0.35 um and 130 nm SONOS technologies are currently in high volume manufacturing and 65 nm SONOS technology is in development. This technology is also scalable to more advanced technology nodes such as 45 nm and 28 nm.

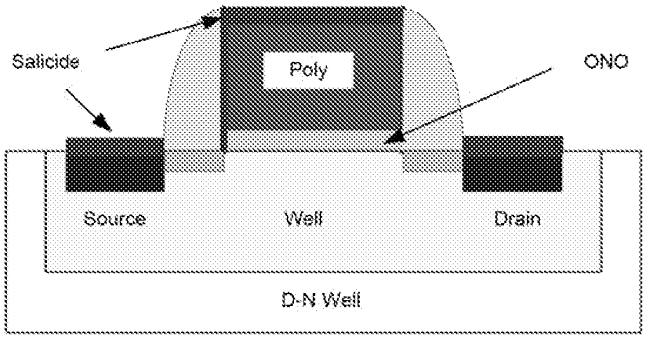
Cypress SONOS Transistor and Cell

The heart of the Cypress SONOS technology is the SONOS FET shown in Figure 2.

This is a MOS transistor with ONO stack as the gate dielectric. The ONO stack is designed to provide the required program or erase speeds and excellent reliability. The stack is engineered to yield a memory cell with outstanding endurance and retention characteristics. Further, the stack is suitable for high volume manufacturing with high Cpk. The SONOS transistor shares many of the key process steps with the CMOS transistors. Hence, many regions of the SONOS transistor, such as source, drain, and gate, are identical to those of the CMOS transistors. This makes the process architecture of the embedded SONOS technology significantly simpler.

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Figure 2. SONOS Transistor Schematic



The schematic shown in Figure 2 is a SONOS transistor that is fabricated using a typical logic CMOS process flow. The device has salicided gate, source, and drain regions and the gate stack is made up of salicided polysilicon. The device structure is slightly different in an SRAM flow with the gate stack having an insulator on top of the polysilicon to enable formation of self-aligned contacts. The source and drain regions are typically not salicided in an SRAM process.

The Cypress SONOS technology currently offers multiple cell options to fit into different application focuses, without compromising reliability.

SONOS Cell Operation

The SONOS cell is programmed by raising the gate voltage of the SONOS transistor to the required positive value. Electrons are injected from the substrate into the charge storage layer of the ONO stack by FN tunneling. The device is erased by applying the required negative voltage to the gate, which causes FN tunneling of holes from the substrate to the charge storage layer. The required program and erase voltage between the gate and substrate is obtained by applying appropriate voltages to the gate and the p-well. Typical voltages for a 10 V program and erase are shown in Table 2.

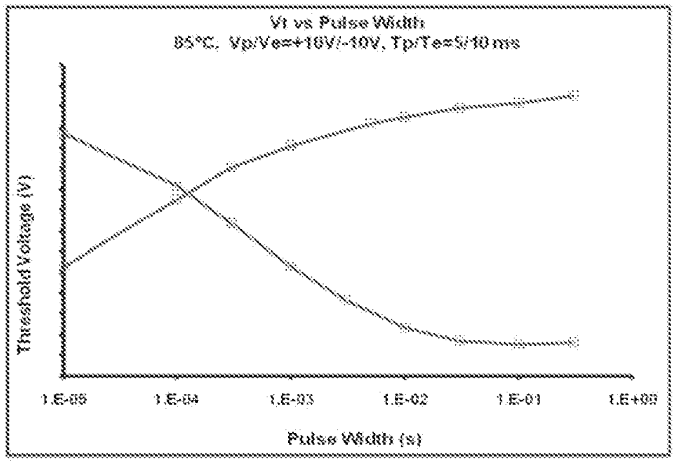
Table 2. Voltages for 130 nm SONOS Operation

	Program	Erase	Read
Vg	7 V	-7 V	0
Vpw	-3 V	3 V	0
Vs	-3 V	3 V	0
Vd	-3 V	3 V	1.2 V

A typical program and erase characteristic of the Cypress SONOS device at 85 °C is shown in Figure 3. High voltages required for program and erase are generated by on-chip charge pump circuits.

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Figure 3. Program and Erase Characteristics of Cypress SONOS FET



The current program speed is 1 to 3 ms and erase speed is 5 to 10 ms depending on cell option and macro architecture.

Cypress 130 nm SONOS Performance Specifications

The optimized Cypress SONOS technology guarantees the following specifications, which are all proved on silicon:

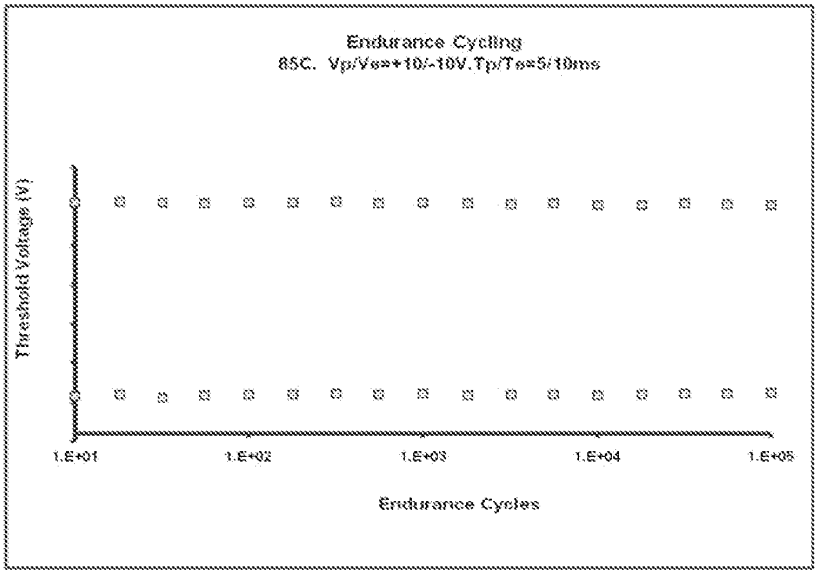
- Program time: 1 to 5 ms; Erase time: 3 to 10 ms
- Program Vt (BOL): ~1 V; Erase Vt (BOL): ~–1 V
- Minimum selected erased cell read current: 8 µA/cell
- Maximum selected programmed cell read current: 100 nA/cell
- Maximum unselected cell leakage at 100 °C: 4 nA/cell

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SONOS Cell Reliability

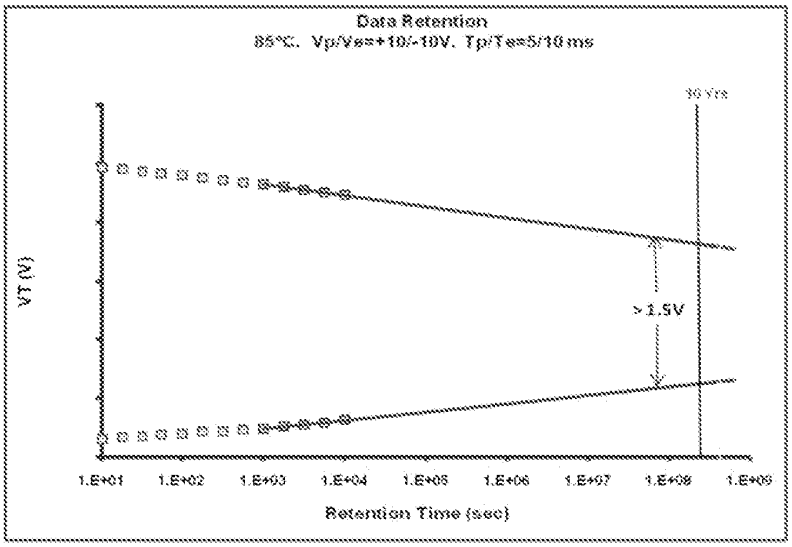
A key requirement for an NVM cell is reliability. The End-of-life (EOL) Vt window is determined by the degradation caused by program/erase cycles (Endurance) and Vt decay during storage (Data retention). Endurance is typically characterized by cycling a SONOS cell through the required number of program/erase cycles and measuring the shift of program and erase Vts. Retention is characterized by taking the SONOS cell through a fixed number of program/erase cycles and then measuring the change of Vt (program or erase) with time at an elevated temperature. Cypress SONOS technology guarantees retention of 20 years after 100 K cycles. Figure 4 and Figure 5 illustrate the typical endurance and retention characteristics.

Figure 4. Endurance Characteristics of Cypress SONOS FET



The endurance characteristics show that Vt shifts less than 100 mV after 100 K program/erase cycles at 85 °C

Figure 5. Retention Characteristics of Cypress SONOS FET



The retention characteristics show that the Cypress SONOS device has an EOL window greater than 1.5 V after 10 years at 85 °C.

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The memory macro is also characterized for reliability. Both at the device level and the macro level, the Cypress SONOS cell show the EOL window greater than 1 V. The reliability specifications fro Cypress SONOS technology, are given in Table 3.

Table 3. Reliability Specifications for SONOS Technology

Specification	Type of NVM	Endurance (Cycles)	Data Retention (Yrs)	Ave ambient Temperature (C)
Industrial	Flash	100 K	20	< 55
		10 K	10	< 85
	EEPROM	1 M	20	< 25
		100 K	20	< 55
		10 K	10	< 85

SONOS Integration

The SONOS module can easily be embedded into a logic process flow or an SRAM process flow with the addition of three to five masking layers. The integration scheme includes a dual gate oxide process, which enables the chip to be compatible with multiple supply voltages. The SONOS has been integrated into a state-of-the-art logic process flow, which includes salicided junctions, stress layers, and Cu-low K interconnects. The integration can be done at many of the technology nodes such as 130 nm, 90 nm, or 65 nm with very few changes except for cell shrink with more aggressive design rules. The optimized thermal budget of SONOS integration ensures a negligible impact on the electrical parameters of existing CMOS devices. This has been proven on very sensitive devices in the 65 nm technology. This means that with minimal changes, all the design IP of the original CMOS platform can be used in the embedded ICs. The integration of SONOS into a logic process flow uses significantly fewer masks than FG Flash, as shown in Table 4.

Table 4. Comparison of Additional Masks for FG Flash and SONOS Embedded into Logic Flow

Process Step	Embedded Floating Gate NVM	CY Embedded SONOS
Wells	+3 Masks	+1 Mask
Floating gate patterning	+1 Mask	
Other NVM related patterning	+2 Masks	+1 Mask
High voltage oxidation/patterning	+1 Mask	+1 Mask
NVM /source/drain implants	+2 Masks	+ 1 Mask
High voltage source/drain implant	+2 Masks	
Masking step adder	+11	+4

Compared to the split gate Flash technology, it is simpler and easier to integrate the Cypress SONOS into a logic CMOS process flow with fewer additional steps (see Table 5). Further, the yield on a SOC with SONOS is limited almost entirely by the CMOS portion of the die.

Table 5. Comparison of FG Flash, Split Gate Flash, and SONOS

Issue	Stack FG	Split Gate	CY SONOS
Poly layers	Double	Triple	Single
Floating gate patterning	Yes	Yes	No
Word line poly patterning	Yes	Yes	Yes
Steps for floating gate formation	4 to 5	10 to 12	0
Yield impacting additional process steps	2	3 to 5	1

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SONOS Integration into foundry 65 nm process

The integration of SONOS into the 65 nm process flow involves the foundry CMOS baseline, which is already in high volume production. The critical issues in this integration are (1) no impact to existing devices and design IP and (2) no degradation in yield. Device matching and no impact to design IP have been successfully demonstrated. It has been shown that there is no impact to the baseline yield due to the integration of SONOS.

The 65 nm SONOS technology has the additional challenge of even lower program/erase voltages. Since the baseline 65 nm technologies has an I/O voltage of 2.5 V, the program / erase voltages are limited to about 7 to 8 V. The SONOS stack has been re-optimized to meet the performance and reliability requirements at these lower program/erase voltages.

Cypress 65 nm SONOS Performance Goals:

The optimized Cypress 65 nm SONOS technology has the following performance goals:

- Program time: 1 to 5 ms; Erase time: 3 to 10 ms
- Program Vt (BOL): ~1 V; Erase Vt (BOL): ~–1 V
- Minimum selected erased cell read current: 3 uA
- Maximum selected programmed cell read current: 1 uA
- Maximum unselected cell leakage at 100 °C: 3.9 nA
- Data retention at 55 C after 10 K P/E cycles at 55 C: 20 yrs

SONOS Data Security

Because SONOS stores the charge in dielectric materials, ion scans and scanning electron microscopes cannot read the programming state of SONOS cells, as they can in floating gate cells. Therefore, SONOS has super capability to provide physical layer security.

Summary

The Cypress SONOS technology is a low cost, highly reliable approach to embed nonvolatile memory into logic platforms. The CMOS design IP is virtually unchanged by SONOS integration. This technology has unbeatable endurance and retention and is scalable to more advanced technology nodes with very little change in process integration.

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Ultra-Pocket® 5 Kit

Rapid Development Kit for 3.0-Megapixel Credit Card Cameras with Color TFT LCD Display

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Credit Card Cameras for Stylish Spontaneity

SMaL Camera Technologies created the credit card camera category. SMaL's Ultra-Pocket® 5 Kit enables uniquely thin 3.0-megapixel resolution cameras with color TFT display as eye-catching alternatives to the inconvenient and bulky digital cameras enabled by other digital camera platforms.

- Ultra-portable
- Uniquely fashionable
- Longest battery life

Fast Time to Market

Leverage SMaL's kit and get to market in record time. The kit includes:

- 3.0-megapixel color CMOS imager with Autobrite®
- ASIC controller
- Lithium-polymer rechargeable battery
- Taking lens
- Complete camera reference design

Longevity™ – Saves Users Power, Time and Expense

Longevity, SMaL's ultra-low-power system design, enables ultra-thin credit card designs with extraordinary battery life. Cameras with Longevity consume less than 10% of the power of traditional alternative designs.

- Stores enough charge for up to 180 shots (with 1.5" LCD and 100% strobe use) – 5 times more than alternative slim cameras

Kit Features

3.0MP Color CMOS Image Sensor

- Resolution: 2000 x 1500 pixels
- Autobrite captures details in both very bright and dim regions – perfect for mixed lighting conditions

ASIC

Imaging

- Controller for SMaL's DSC image sensor
- Complete integrated functions fc digital still application
- LCD support: 1.5" or 1.8" color TFT
- 2x digital zoom
- Lossless image compression
- Integrated flash strobe interface

Power

- Low power dissipation
- 3 integrated voltage regulators, allowing a separate low noise image sensor supply
- Lithium-polymer battery charger via USB
- Battery monitor and protection circuitry

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- Battery charges automatically via USB during picture download
- Eliminates the frequent hassle and expense of battery changes

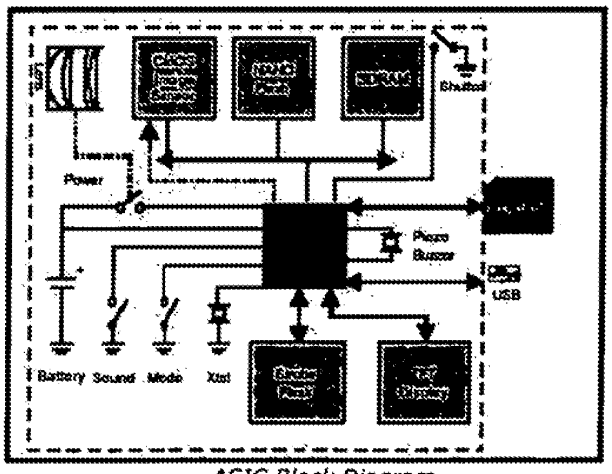
High Integration – Small Form Factors, High Quality

Cameras enabled by SMaL's Ultra-Pocket 5 Kit use 1/2 to 1/3 the number of components compared to other digital cameras. In addition, the kit includes an all glass lens that has been optimized to the sensor. The combined benefits are:

- Smaller form factors, higher manufacturing yields and higher product reliability
- 3.0-megapixel images with film-like sharpness and clarity - produce high quality 8 x 10-inch prints

Autobrite – Adapts to Brightness as Your Eyes Do

The Ultra-Pocket 5 Kit uses SMaL's proprietary Autobrite wide dynamic range technology which adapts to varying light conditions such as glare, backlighting and shadows.



ASIC Block Diagram

- Integrated flash strobe interface
- Low-power embedded microprocessor and SRAM
- Multiple power modes, including automatic power down

Programmable

- Programmable color LCD interfa
- Programmable user interface, including international fonts
- I/O interface to SDRAM, Flash, SD/MMC, EEPROM

USB

- USB 2.0 full-speed compliance with integrated transceiver
- USB to SD conversion
- Firmware upgrades via USB

Lithium-Polymer Battery

- Ultra-thin: 4.5 mm
- Capacity: 190 mA -hr.
- Shots per charge: Ten times longer battery life than standard digital cameras with LCD and strobe on (approx. 170 images)

Taking Lens: Glass/plastic, F/3.0

Supported Operating Systems

- Win 98SE, ME, 2000, XP; Mac OSX
- TWAIN (Windows 98SE, ME, 200 XP)
- WIA (Windows XP)
- ICA (Mac OSX)

Imager	
Model Number	IMG0042 3MP color CMOS image sensor with Autobrite
Active Array Format	2000 x 1500 pixels
Image Resolution Settings	High (2304 x 1768) (4MP)* Medium (2000 x 1500) (3MP) Low (800 x 600) (1MP)*
Pixel Size	3.35 µm x 3.35 µm
Pixel Type	Adaptive dynamic range photo diode
Sensor Area	6.75 mm x 5.08 mm
Intra-Scene Dynamic	

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Range	up to 120 dB with Autobrite
Optical Format	1/2-inch
Maximum Frame Rate	13 frames per second
Maximum Date Rate	70 megabytes per second at 8 bits
Supply Voltage	3.0 to 3.6V
Operating Temperature	0° to 40° C
Digital Gain	1x to 16x
Output	8 or 12-bit digital (selectable)
Shutter	Electronic rolling shutter
Correlated Double Sampling (CDS)	On-chip
Analog-to-Digital Converter (ADC)	On-chip 12-bit column parallel
Package	48-pin LCC plastic
Timing and Control	On-chip
Programmable Controls	Adaptive compression characteristics, power control, signal gain, exposure parameter

Optics

Lens	4-element glass/plastic, focal length = 8.2 mm, F/3.0 (equivalent to 44 mm lens on a 35 mm camera), FOV 54 degrees
Lens Focus	Fixed, 1.5 m (4.9 ft) to infinity

System

Exposure Control	Automatic with Autobrite and low-light-level strobe activation
Exposure Time	1/30 second to 1/10,000 second

** Higher resolution (interpolated) available based on customer request.*

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An Analog PLL-Based Clock and Data Recovery Circuit with High Input Jitter Tolerance

SAM YINSHANG SUN, MEMBER, IEEE

Abstract—**A clock and data recovery circuit for a T1 network is described. A fully integrated PLL extracts the carrier signal embedded in the data. Two trimming DAC's simultaneously bring the VCO center frequency and the PLL closed-loop bandwidth to their specified values. A triple sampler captures the jittering data and aligns them with the recovered clock. The input jitter tolerance of this circuit is three times more than previously reported PLL-based circuits.**

I. Introduction

RECENT advances in the Integrated Service Digital Network (ISDN) have made its realization for the general public a likely prospect in the near future. For its primary rate interface, 1.544 Mbit/s in the U.S. and 2.048 Mbit/s in Europe, a higher input jitter tolerance requirement has been newly imposed demanding better performance of its line interface unit (LIU). This requirement challenges the performance of the key circuit block in the LIU, namely the clock and data recovery circuit, to a greater level.

Clock and data recovery circuits can be categorized into three types: *LC* tuned tank, digital PLL-based, and analog PLL-based circuits. The *LC* tank requires tuning of the external components and is sensitive to the data pattern. The digital PLL suffers high-speed phase "hit" on its output which is inherent to the scheme. The analog PLL can be fully integrated and provides a smooth clock output. Nevertheless, the performance of the analog PLL-based circuit needs to be optimized. Designed to be highly tolerant of input jitter, this paper describes a fully integrated analog PLL-based clock and data recovery circuit in a monolithic LIU using novel techniques to meet the performance challenge.

II. Circuit Description

The circuit shown in Fig. 1 is constructed with a signal slicer to convert the alternate mark inversion (AMI) signal into a return-to-zero (RZ) signal, a charge-pump PLL to extract the carrier clock embedded in the input data stream, and a triple sampler to capture the jittering data and align them with the recovered clock (RCLK). A frequency comparator is also included to monitor the PLL lock-in status.

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IEEE Log Number 8826245.

A. Charge-Pump Phase-Locked Loop

As illustrated in Fig. 2 the PLL consists of a data-activating frequency/phase detector (FPD), a charge-pump loop filter (LF), and a current-controlled relaxation oscillator (ICO) [1]. Two current DAC's are used to trim the VCO center frequency and the PLL closed-loop bandwidth respectively. The FPD compares the phase difference between the RZ data and VCO output RCLK and steers the LF current sources to charge or discharge the large capacitor C. The voltage change on C will then drive the VCO output frequency to a direction to reduce the phase difference. The small capacitor C_2 is used to suppress the ripple in the charge-pump LF.

The capture range of this PLL is approximately the same as the VCO frequency range because the frequency/phase detector shown in Fig. 3 compares not only the phase difference, but also the frequency difference. When a pulse is present on RZ data this FPD will be activated as follows: if the phase of RZ data leads the RCLK phase, the UP output will be ON for a duration proportional to the phase difference; if RZ data lags RCLK, the DOWN output will be ON in the same fashion. The output logic prevents the UP/DOWN outputs from being ON simultaneously. This FPD has 1 bit of memory to keep the last comparison result that will eliminate an output phase jump at the beat frequency when the two input signals have different frequencies. When no pulse appears on RZ data, these two outputs will be deactivated and the VCO is free running until the next pulse comes.

The VCO consists of two parts. One is a relaxation ICO; its output frequency is controlled by its input current I_p as shown in Fig. 4. Two identical holding capacitors and auto-reset comparators provide near 50-percent duty cycle on clock output without a dividing counter. The VCO center frequency is switchable from 1.544 to 2.048 MHz by changing the trigger level of the comparators. The other part of the VCO is a 4-bit current DAC with VCO input

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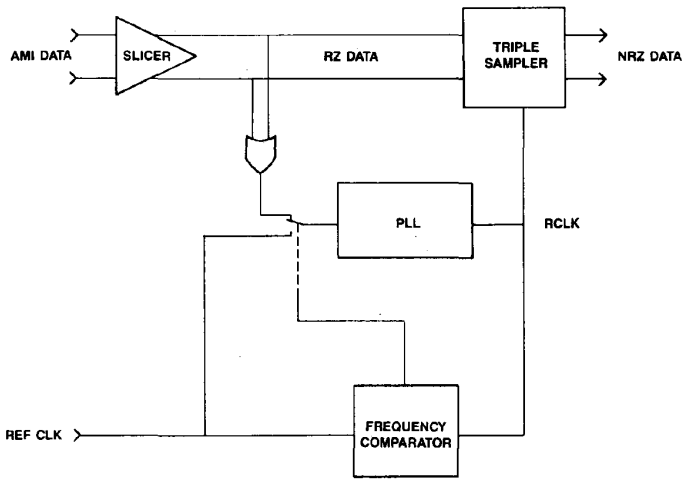


Fig. 1. Functional block diagram.

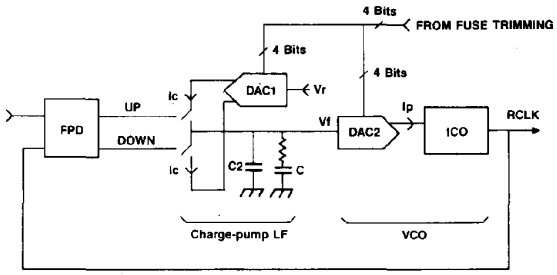


Fig. 2. Charge-pump PLL block diagram.

voltage V_f as its reference voltage. This DAC functions as a programmable voltage-to-current converter to adjust the transfer curve between the input voltage V_f and output current I_p to the ICO under different digital input codes. The VCO center frequency f_o and VCO gain K_o are delineated in the expressions below:

$$f_o = \frac{1}{2V_T} \cdot \frac{I_p}{C_h} \tag{1}$$

$$K_o = 0.8\pi \cdot f_o. \tag{2}$$

The other DAC is used in the charge-pump loop filter with a preset reference voltage V_r to provide a suitable injecting current I_c to determine the PLL closed-loop bandwidth which can be expressed by (3) [1]:

$$f_n^2 = \frac{K_o}{8\pi^3} \cdot \frac{I_c}{C} \tag{3}$$

$$\xi = \pi RCf_n. \tag{4}$$

The PLL is a second-order loop of which the damping factor ξ is determined in (3) by the resistor R, capacitor C, and PLL closed-loop bandwidth f_n. The two DAC's are made identically in the circuit and layout with the intention to adjust these key circuit parameters.

Two inherently conflicting aspects were considered when deciding the PLL closed-loop bandwidth. Stable locking to a random data stream needs a narrow bandwidth while a reliable data recovery demands a wide bandwidth to enable RCLK to quickly track the jittering data phase instance. The key performance characteristic of a clock/data recovery circuit is its input jitter tolerance. The input jitter tolerance is the maximum amount of phase jittering on an input data stream tolerable by the circuit that still recovers the clock and data from input. Fig. 5 shows the input jitter tolerance of a conventional PLL-based circuit with different closed-loop bandwidths. It is apparent that the wide loop bandwidth yields better performance in low jitter frequencies below 10 kHz while the narrow loop bandwidth produces a better result in higher frequencies.

B. Triple Sampling Data Recovery

To alleviate the dilemma of choosing the PLL closed-loop bandwidth, a triple sampler for data recovery was developed in an attempt to relax the phase tracking requirement. Instead of sampling the RZ signal only at 90° as the conventional approach, the triple sampler samples at 0°, 90°, and 180° as shown in Fig. 6. Whichever sampler detects a ONE, the output will be ONE due the characteristic of the RZ signal. This scheme makes the acceptable instantaneous phase error between the RZ signal and RCLK as high as 180° in contrast to the 90° from the conventional approach. The closed-loop bandwidth was then chosen to be 8 kHz for optimal jitter performance. Fig. 7 shows the measured PLL phase jitter frequency response (i.e., PLL phase-transfer function).

III. Circuit Adjustment

The circuit integration on silicon demands adjustments for the VCO center frequency and the PLL closed-loop bandwidth to compensate for the large component varia-

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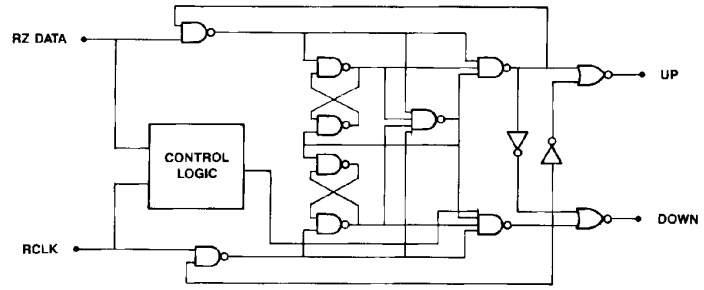


Fig. 3. Schematic of data activating frequency/phase detector.

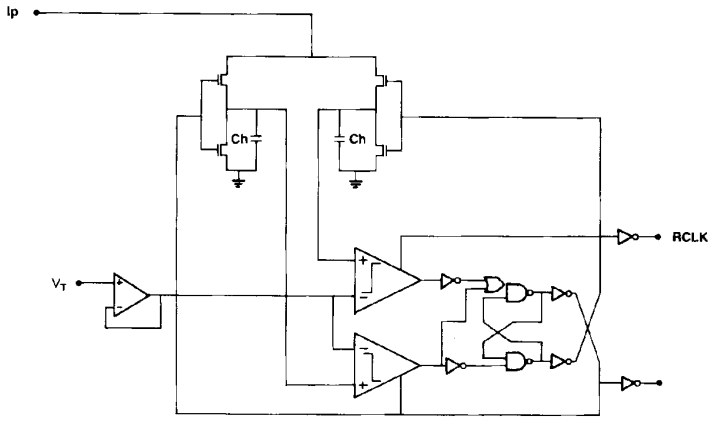


Fig. 4. Schematic of current-controlled oscillator (ICO).

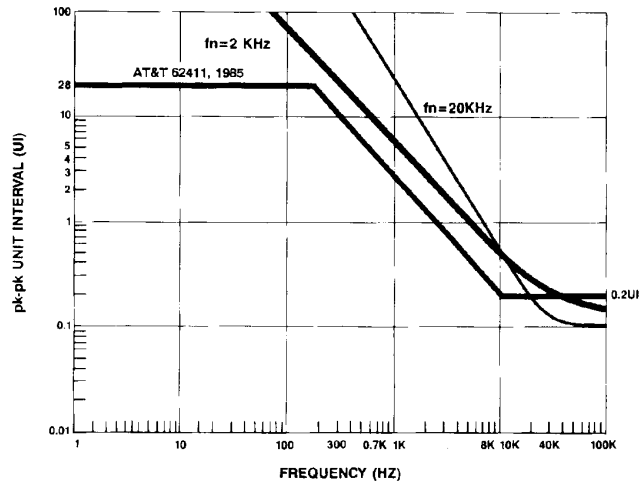


Fig. 5. Input jitter tolerance of the prototype with different PLL closed-loop bandwidth.

tions in MOS fabrication process. In mass production measuring the VCO center frequency is fast but measuring the PLL closed-loop bandwidth takes a relatively long time. Instead of calibrating them separately, a new technique was developed to complete the two tasks with one trimming. Two identical current DAC's were used to trim these two key parameters. At the wafer test stage, the on-chip polysilicon fuses were blown according to the VCO frequency measurement. The resulting digital code controlled the VCO current DAC to adjust the transfer

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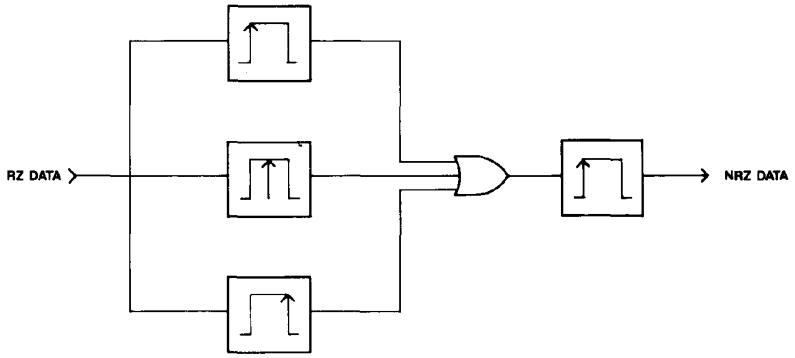


Fig. 6. Triple sampler data recovery.

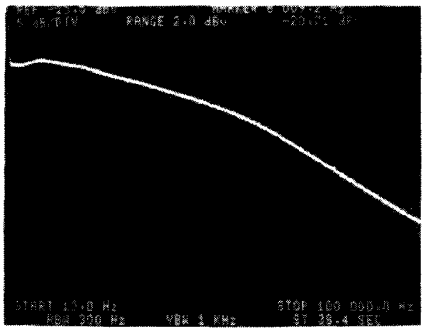


Fig. 7. Measured PLL phase jitter frequency response to a random data input.

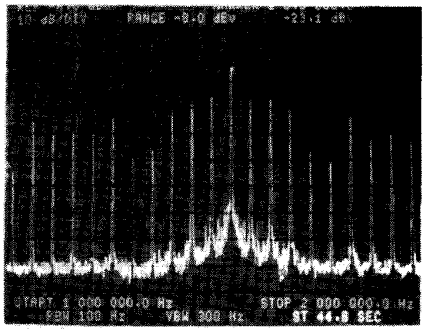


Fig. 8. Frequency spectrum of a repetitive data pattern.

curve between the VCO input voltage and the charging current I_p which allows the VCO to oscillate at the desired frequency. The same digital code was also used to change the current DAC of the charge-pump LF to adjust the charging current I_c which, in turn, centered the PLL closed-loop bandwidth to a predetermined frequency.

The correlation between these two adjustments is apparent when examining the mechanisms of the VCO frequency and the formation of the PLL closed-loop bandwidth. As expressed in (1) the VCO center frequency f_o is proportional to its charging current I_p divided by capacitance C_h. The PLL closed-loop bandwidth f_n^2 (see (2)) is also proportional to its charging current I_c divided by holding capacitance C. The input voltages of the two identical DAC's in the VCO and LF are equal by design and by definition. With the same digital input code the ratio of the DAC's output current I_p to I_c is approximately constant within the precision of component matching in the process. That is,

$$I_p/I_c = A \tag{5}$$

where A is a constant. Therefore, the PLL closed-loop bandwidth is derived as

$$f_n^2 = \frac{0.2V_T}{A\pi^2} \cdot \frac{C_h}{C} \cdot f_o^2. \tag{6}$$

Thus, trimming I_p by a certain percentage to let f_o reach a desired value will also change I_c by the same percentage, consequently making f_n come near the predetermined bandwidth. This is accomplished by the simultaneous control of the two identical DAC's used in the VCO and the charge-pump LF circuits.

IV. Anti-Harmonic Lock Technique

One inherent danger in the analog PLL-based clock and data recovery circuit is the PLL being locked onto the subharmonic of the data carrier frequency, especially when the data pattern is repetitive. The spectrum of a repetitive data pattern shown in Fig. 8 has local peaks at a subharmonic frequency near the peak of the carrier frequency. A commonly used scheme is to limit the VCO frequency range to within 6 or 7 percent of the center frequency to avoid locking onto the frequency outside the VCO range [2]. This scheme provides only limited protection to subharmonic locking and is useless to subharmonic locking within the VCO range. The nearest local peak on Fig. 8 is about 3 percent away from the carrier frequency, where the PLL was observed to be locked onto it in the prototype experiment. Further reduction of the VCO range creates problems under different operating conditions and temperatures.

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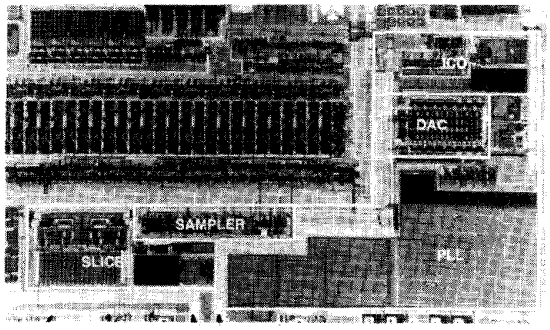


Fig. 9. Die photo of the clock and data recovery circuit.

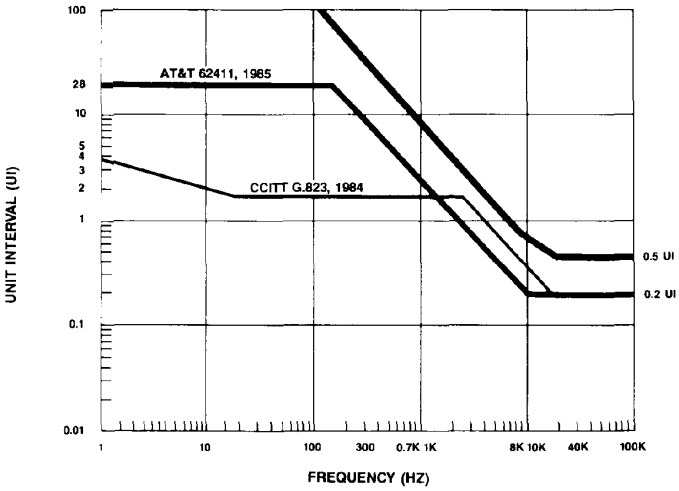


Fig. 10. Input jitter tolerance to a random data input.

A unique technique was developed to detect and correct potential subharmonic locking. As shown in Fig. 1 a frequency comparator was added to monitor the recovered clock RCLK against a precision reference clock also derived from the data stream. If the RCLK frequency deviates from the reference frequency, it will be declared abnormal and the PLL input will be switched to the reference clock for training and then switched back to the RZ data stream. Since the trained VCO clock is very close to the carrier frequency of the data it will easily lock onto it. Thus, instead of resisting the subharmonic locking, this circuit detects the subharmonic locking and corrects it.

V. Experimental Result

This circuit was realized with a 3-μm bulk CMOS process and occupied 5500 mil^2. A die photo of this circuit is shown in Fig. 9. The input jitter tolerance given in Fig. 10 exceeds the requirement of the newly revised AT&T pub. 62411 "High Capacity Digital Service Interface Specification" [3]. The high jitter frequency tolerance is at least three times better than previously reported PLL clock and data recovery circuits [2]. The performance is summarized in Table I.

TABLE I
Device Characteristics

Technology	CMOS 3 micro double poly
Power Supply	5 V ± 10%
Power Consumption	25 mW (typical)
Silicon Area	5500 mil^2
Allowable Instant Phase Error	± 0.47 UI
PLL loop Bandwidth	8 KHz ⊥ 1 KHz
Pull-in Time	< 200 us
Tolerance to "0" stream	300 "0"s (typical)
Intrinsic Jitter Output	0.01 UI (All "1" input) 0.015 UI (Random data)
Max. Static Phase Error	15°

VI. Conclusion

A high input jitter tolerance was achieved in this analog PLL-based clock and data recovery circuit. The task of making the circuit system stable and fast data phase cap-

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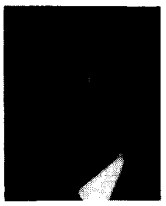
turing was accomplished by adjusting the key PLL parameters and using a novel data recovery circuit. Full integration in CMOS technology makes this circuit a useful functional block which can be incorporated easily into VLSI systems.

ACKNOWLEDGMENT

The author would like to express his gratitude to S. Hao and Dr. K.-L. Lee for their suggestions and encouragement. The author would also like to thank R. R. Co for the initial work on the PLL architecture.

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Since 1984 he has worked as a Design Engineer for Precision Monolithics Inc. on data acquisition IC and for Rockwell International on CMOS process development and on analog IC for ISDN systems. He is currently a member of the technical staff in the Semiconductor Product Division of Rockwell International, Newport Beach, CA. His interests include the design of analog and digital integrated circuits with particular interest in circuits for telecommunication systems.

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A Novel Integration Technology of EEPROM Embedded CMOS LOGIC VLSI Suitable for ASIC Applications

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Abstract

A novel process technology has been developed to fabricate an EEPROM embedded CMOS VLSI. The new technique utilizing a single poly-Si EEPROM cell reduces process steps by 25% as compared with the conventional double poly-Si EEPROM cell. The EEPROM-embedded CMOS LOGIC LSI can be shrunk over future technology generations by introducing three kinds of gate oxide thickness. A widely operating voltage ranging from 1.5 V to 6.0 V and a stand-by current below 100 nA have been achieved.

Introduction

Recently, in an era of SYSTEM ON CHIP, the demand for embedding EEPROM in a large scale CMOS LOGIC has been increasing for a data memories on one chip, especially for installing a security system on a chip, even when the bit size is small. It has been reported that EEPROM and CMOS LOGIC can be put on one chip[1].

Figure 1 shows the comparison of characteristics for important key factors in an ASIC between pure CMOS and conventional EEPROM. A conventional EEPROM has an advantage of high functionality(ZERO turn-around-time and 10^6 program cycles), compared with a pure CMOS. However, it has a disadvantage in its process sequence, operating voltage, and power consumption, compared with a CMOS. Target characteristics are required. The conventional EEPROM cell has a double poly-Si structure and requires a long process sequence. Therefore, a simple structure and a simple process sequence are required. Technologies for low voltage operation and low power consumption are indispensable for future ASIC applications. A low voltage operation is required for the trend of reducing the supply voltage. A low power is required for systems with battery back-up. A new cell technique with a single poly-Si EEPROM[2] embedded CMOS process and circuit technology has been developed. It is easy to apply it to future generation logic.

In this paper, the process, device technologies, and LSI characteristics are described.

Fabrication process

Figure 2 shows a cross-sectional view of the new single poly-Si EEPROM cell and CMOS. The cell has three types of MOSFETs with different gate oxide thicknesses. The tunnel oxide thickness, coupling capacitor thickness, and high voltage gate oxide thickness are 9 nm, 15 nm, and 40 nm, respectively. The CMOS has a twin-well and the logic gate oxide thickness is 15 nm. The new cell requires a large control gate area in order to gain a high coupling ratio. Therefore, this cell size is approximately 2.5 times larger than the double poly-Si cell size. In general, the chip cost of a memory LSI is proportional to the cell size. However, an EEPROM embedded CMOS LSI does not have a proportional relationship when considering both the process complexity and the area ratio of EEPROM to CMOS. From the view-points of chip cost and bit capacity, a single poly-Si EEPROM cell with a bit capacity of less than a certain value, has an advantage to a double poly-Si EEPROM cell. Both single poly-Si EEPROM and double poly-Si EEPROM line up on the 1.0 um rule.

Figure 3 shows the process flow up to gate formation. The EEPROM channel and N^+ implantations are carried out after field oxidation. First, gate oxide is grown, CMOS channel implantation is carried out, and then, the oxide at the logic region and the coupling capacitor region are removed using a masking step, and the second gate oxide is grown. Next, the tunnel window region is opened using a masking step, and the tunnel oxide is grown. Finally, poly-silicon is deposited. The logic gate oxide thickness can be easily shrunk through this process, taking the capability for coming generations into account, because this oxide can be controlled flexibly, using this 2-step oxidation technique (second gate oxidation and tunnel oxidation). These insulators consist of only oxides. They don't require complex insulating film formation like an ONO (oxide-nitride-oxide). Therefore, this process can be used in a CMOS logic fabrication line.

Figure 4 shows the reliability data for the 2-step gate oxide and conventional CMOS gate oxide. It has been verified by TDDB measurement that both have the same reliability.

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Device characteristics

A new cell layout and cross-sectional view are shown in Fig.5. The cell consists of 2 transistors. The cell is fundamentally the same as that for FLOTOX. The control gate is formed with an N+ diffused layer under the floating gate. The N+ diffused layer(control gate, source, and drain of the select-transistor) is formed with only one implantation by using a one masking step. Therefore, select-transistor is not a self-aligned structure. This is the most effective in a long process sequence to reduce the process step. Figure 6 shows the erase, write, and read mode bias set ups for the new cell, compared with those for the conventional cell. The erase and write operating biases are the same conditions. The read line in the new cell is precharged by the Vcc level. An inverter sense amplifier is used to achieve low voltage and low power consumption[3].

Figure 7 shows the cell characteristics of erase, write, and read operations, compared with Toshiba's double poly-Si EEPROM cell. After being erased, the threshold voltage, Vth, of a single poly-Si cell is lower than that of a double poly-Si cell, because the surface of the control gate is in an inverse state and the depletion layer voltage drops when the control gate of the single poly-Si cell is positively biased. The Icell has compatible characteristics between a single poly-Si cell and a double poly-Si cell even when different reading methods(source read mode and drain read mode) are used. It has been certified that a single poly-Si cell has the same coupling ratio as a double poly-Si cell.

The device characteristics on a 1.0 um EEPROM embedded CMOS and the pure CMOS process show in Table 1. Both processes have achieved the same performance. Therefore, EEPROM and CMOS logic VLSIs designed on Toshiba's CAD [4] can be on one chip.

LSI performances

Table 2 lists the chip features. A test chip can operate over a wide range of supply voltage, 1.5 V~ 6.0 V and consume only 300 uA at 4 MHz. This low operating voltage down to 1.5 V has not been achieved before (even for an external Vpp). Furthermore, its stand-by current is extremely low, below 100 nA.

A wide operating voltage for the test chip has been verified with a schmoo plot, as shown in Fig.8.

Figure 9 shows a test chip photograph. A 64 byte EEPROM core has been designed, using 1.0 um single poly-Si EEPROM embedded CMOS technology. The 64 byte EEPROM core size is 1.54 x 0.67 mm with a memory cell area of 175 um2.

Conclusions

A new cell technique utilizing a single poly-Si EEPROM cell reduces the process sequences by 25% as compared with a double poly-Si EEPROM. A wide operating voltage ranging from 1.5 V to 6.0 V and a stand-by current below 100 nA have been achieved for consumer oriented ASIC applications. It has been verified that EEPROM embedded CMOS LSIs are promising for future generations by utilizing novel process technology.

Acknowledgments

The authors would like to thank F.Tanaka for their continuous encouragement. T.Maruyama, H.Aoyagi, K.Noguchi, and H.Tanaeda for their fruitful discussions.

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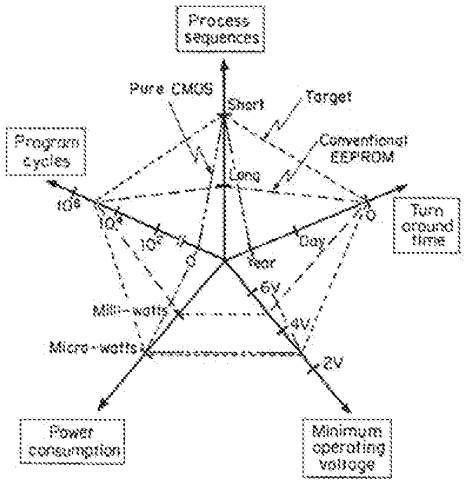


Fig.1 Comparison of characteristics between pure CMOS and conventional EEPROM

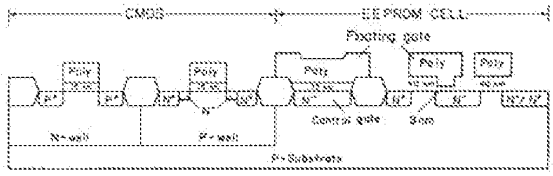


Fig.2 Cross-sectional view of single poly-Si EEPROM cell and CMOS

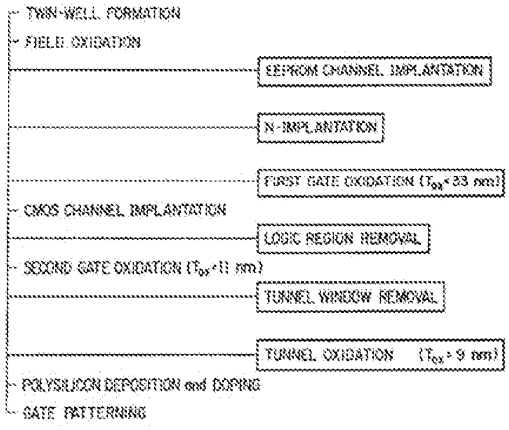


Fig.3 Single poly-Si EEPROM embedded CMOS process sequence

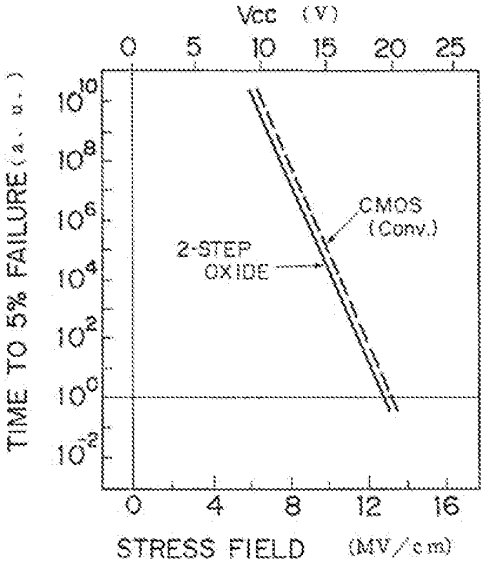


Fig.4 Dependence of times to 5% failure for 2-step oxide and conventional CMOS on stress field

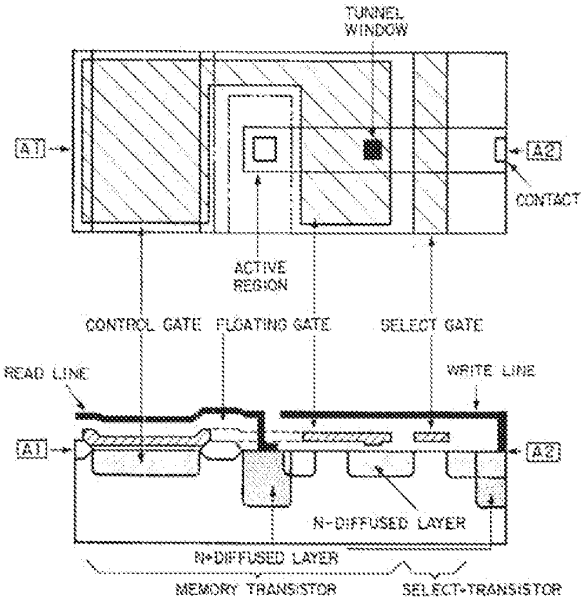


Fig.5 Layout and cross-sectional view of single poly-Si EEPROM cell

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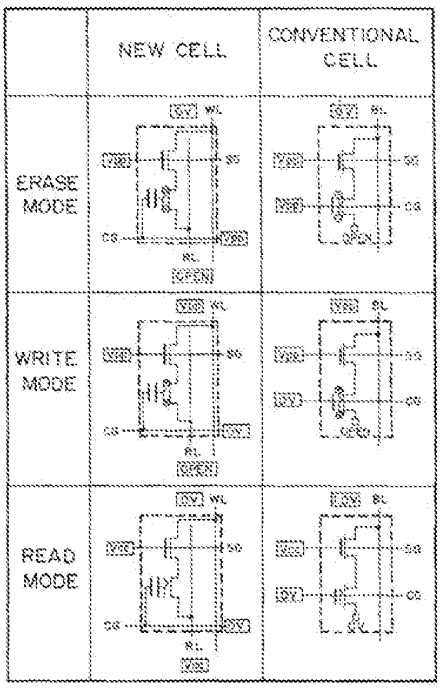


Fig.6 Schematics of new cell and conventional cell

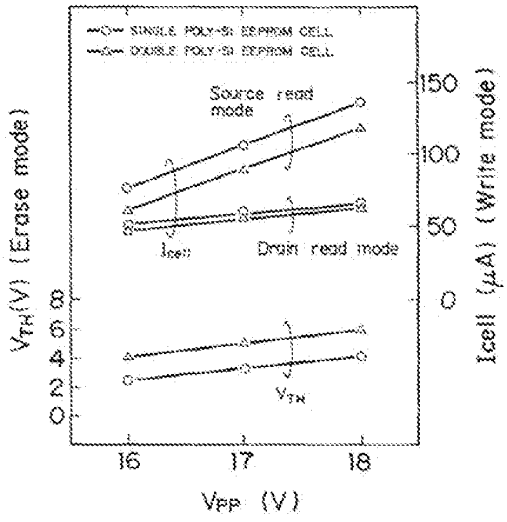


Fig.7 Erase/write characteristics:
Source read mode: WL or BL=0V, SG=5V, CG=0V, BL or source=5V
Drain read mode: WL or BL=1V, SG=5V, CG=0V, BL or source=0V

Table 1 Device characteristics of CMOS and EEPROM-CMOS processes

	PURE CMOS	EEPROM - CMOS
NMOS	1.0μm LDD	—
V_{th} (V)	0.85	—
I_{dn} (μA/μm)	240	220
PMOS	1.0μm Conv.	—
V_{tp} (V)	-0.85	—
I_{dp} (μA/μm)	-160	-160

Table 2 Test chip features

Device technology	1.0μm EEPROM EMBEDDED CMOS
Total Transistors of number	2000
Core size	1.54 x 0.67 mm
Standby current(clock stop mode)	100 nA(Vcc=5.5V)
Operation current (f=4MHz)	300 μA(Vcc=5.5V)
Operating voltage	4.5~6.0 V
Program voltage	16 V
Erase time	2ms TYP.
Write time	2ms TYP.
EEPROM	64 bytes

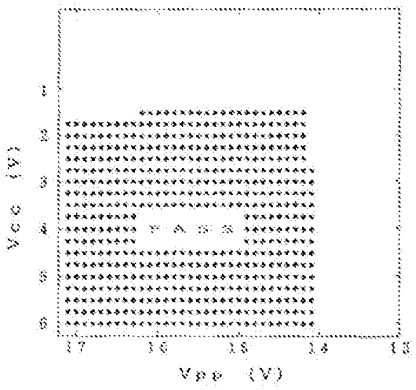


Fig.8 Schmoo-plot of operating voltage as a function of Vpp

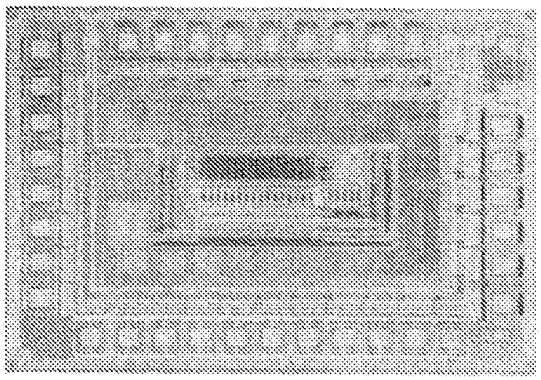


Fig.9 Test chip photograph (64 byte EEPROM core)

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RELIABILITY AND PROCESSING EFFECTS OF BANDGAP ENGINEERED SONOS (BE-SONOS) FLASH MEMORY

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ABSTRACT

The reliability properties of BE-SONOS [1] are extensively studied. BE-SONOS employs a multi-layer O1/N1/O2/N2/O3 stack, where O1/N1/O2 serves as a bandgap engineered tunneling barrier that provides an efficient hole tunneling erase but eliminates the direct tunneling leakage. BE-SONOS can overcome the fundamental limitation of the conventional SONOS, for which fast erase speed and good data retention cannot be simultaneously achieved. In this work, we provide a comprehensive understanding of the reliability of BE-SONOS. Various processes to form the critical O1/N1/O2 barrier, the trapping layer (N2), and the top blocking oxide (O3) are investigated. The results of this work provide design and processing guidelines for optimizing the performance and reliability of BE-SONOS Flash memory devices.

I. Introduction

Recently, SONOS-type devices are forecasted to be the solution for NAND Flash beyond 45 nm node [1,2]. Unlike floating-gate device, SONOS device has no floating gate coupling ratio issue hence it greatly saves the process complexities in the floating poly geometry. Since charges are independently trapped, it is naturally immune to the capacitance coupling interference due to the adjacent memory cells [2]. Moreover, SONOS-type device requires very few electrons (<500) and is without erratic behaviors. Therefore, SONOS device is ideal in terms of scaling and reliability.

However, the conventional SONOS has a fundamental limitation. Since electrons are deeply trapped in nitride, de-trapping speed is very slow if tunnel oxide is thick (>3nm). A higher electric field does not help since it introduces a large gate injection [3] negating the erase operation. Therefore, SONOS devices are often designed with a thin tunnel oxide (~2 nm), where hole direct tunneling from the substrate can compensate the trapped electrons during erase operation. However, such thin oxide leads to very poor data retention because hole direct tunneling occurs even at very low field.

Recently, we proposed BE-SONOS [1] to overcome this limitation. The structure of BE-SONOS is shown in Fig. 1. Unlike SONOS, a bandgap engineered ONO barrier is used to replace the tunnel oxide. The band diagram concept is illustrated in Fig. 2. Under high electric field, the band offset can reduce the hole tunneling distance to effectively the thin O1, thus a large hole current is allowed. On the other hand, at low electric field during retention, both electron-de-trapping and hole direct tunneling are completely prohibited by the total barrier thickness (O1+N1+O2).

The simulated hole tunneling current is shown in Fig. 3. For a thin oxide used in the conventional SONOS, the direct tunneling current cannot be turned-off even at 1 MV/cm, which is typically the built-in electric field for a device in the programmed state. Therefore, severe charge leakage is observed even at room temperature for SONOS. For a thick oxide (>3nm), the hole tunneling current is negligible ($<10^{-6}$A/cm^2) because of the large hole barrier height of oxide (4.5 eV). Therefore, conventional SONOS with a thick tunnel oxide has a very slow erase speed. On the other hand, the engineered ONO barrier behaves entirely differently. At high field (~10 MV/cm), the hole current is high, ~10^{-3}A/cm^2 and provides high erase speed, yet it is completely suppressed at low field (<2 MV/cm). Therefore, BE-SONOS provides both fast erase speed and good data retention.

The basic characteristics of BE-SONOS devices were described in previous works [4-7]. Recently we have carried out very long-term (>1000 hours) retention tests at various temperatures, and developed a model to predict the lifetime of BE-SONOS [4]. In this work, the reliability properties and their correlation with processing methods of BE-SONOS are examined in detail. The present work provides a comprehensive understanding of BE-SONOS reliability.

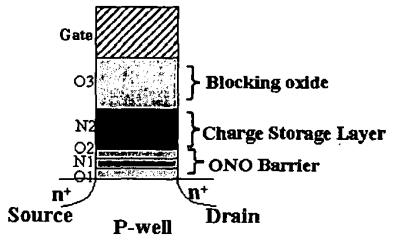


Fig. 1 Structure of the n-channel BE-SONOS using ultra-thin ONO tunneling barrier.

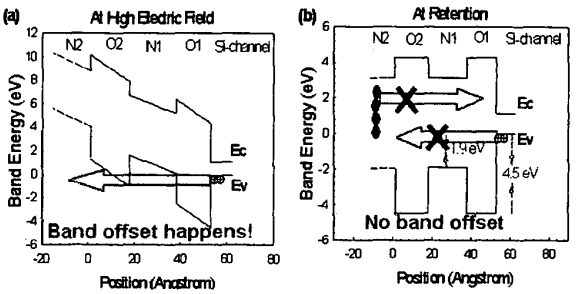


Fig. 2 Bandgap engineering concept for the BE-SONOS device. (a) At high field during erase, band offset reduces the hole tunneling barrier to merely O1. (b) At low field during retention, both electron de-trapping and hole back tunneling are prohibited by the full O1/N1/O2 barrier stack.

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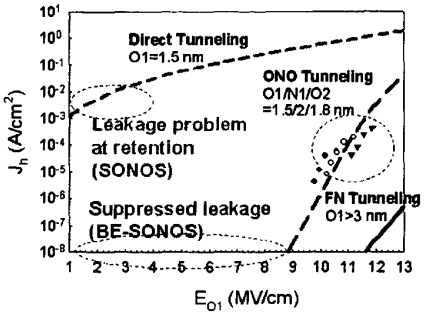


Fig. 3 J-E characteristics of various tunneling barrier. Thin oxide (1.5 nm), thick oxide (>3 nm) and ONO barrier are compared.

II. Processing Description

The ultra-thin oxide (<2 nm) is fabricated by in-situ steam generation (ISSG). ISSG is a rapid-thermal radical reaction method. Since ultra-thin oxide is critical for BE-SONOS, a test run on control wafer is carried out before O1 formation in order to guarantee the thickness control. The thickness is measured by optical ellipsometer. The thickness accuracy can be controlled within 1 Å.

LPCVD is used for nitride deposition (for both N1 and N2). The typical thickness for N1 and N2 are 2 and 7 nm, respectively. Deposition is carried out at 680^{0}C with DCS and NH_3 precursors. For the SiON thin films (N2), additional N_2O gas is applied in the gas flow.

For the inter oxide (O2), LPCVD oxide (HTO) with thickness thinner than 3 nm is deposited. For the top oxide (O3), the standard method is the thermal conversion of nitride in furnace at high temperature (950-1000^{0}C) with O_2 and H_2O gas (wet conversion process). In this process, a 13 nm nitride is converted into a 9 nm top oxide, with 7 nm nitride remaining. The wet conversion process produces a strong top oxide that can withstand a large P/E cycling stress. However, it requires a large thermal budget. In some samples, HTO and ISSG top oxides are fabricated for comparison. The typical thickness for O3 is 9 nm.

A heavily doped P^+-poly gate is used for all the samples in this work. P^+-poly gate can greatly reduce the gate injection during –FN erase, thus resulting in lower erase saturation V_{FB}.

III. Properties of Ultra-Thin ONO Barrier

BE-SONOS employs an ultra-thin ONO as the tunneling barrier. The first nitride N1 serves as a non-trapping dielectric that alters the hole tunneling current. The non-trapping behavior of the ONO barrier is shown in Fig. 4, where constant current stress (CCS) shows no significant trapping even after1000 sec continuous stress. Figure 5 shows that the measured I_G-V_G curve is consistent with the theoretical calculation at high field. Besides, the I_G-V_G curves show no degradation after current stress.

Figure 6 shows the I_G-V_G curves of the ONO barrier at various temperatures. The measured current is insensitive to temperature. This further supports that the measured current is indeed tunneling current rather than Frenkel-Poole (F-P) current, since F-P current strongly depends on the temperature.

Recently, many high-*k* dielectrics are found to have a fast transient injection effects [8]. In order to clarify this possible effect, we have carried out the pulsed *IV* measurement [6] for BE-SONOS device. The result is shown in Fig. 7, where the pulsed *IV* shows identical drain current as the DC results. This indicates that the ultra-thin ONO does not have any instant charge trapping/de-trapping within a short (~20 μsec) transient time.

We have found that the capture efficiency of nitride significantly decreases for thickness below 3 nm [9]. The physical reason is not completely understood even now. A possible reason is that the capture mean free path is larger than the nitride thickness such that very low trapping can occur. Moreover, both oxide and nitride are very thin thus the electrons gain very small energy during the tunneling process.

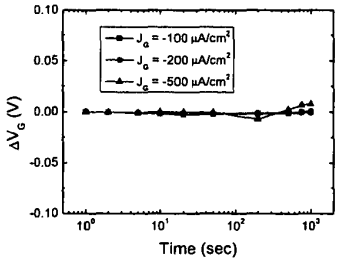


Fig. 4 Constant current stress (CCS) of the ONO capacitor (15/20/25 Å). The selected current density is chose to be close to that during typical –FN erase (<10^{-3}A/cm^2).

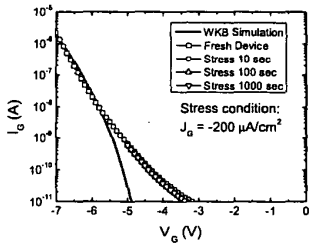


Fig. 5 Constant current stress (CCS) of the ONO (15/20/25 Å) capacitor. The selected current density is chose to be that used in the erase (<10^{-3}A/cm^2). P^+-poly gate is used to suppress the gate injection during –Vg stress.

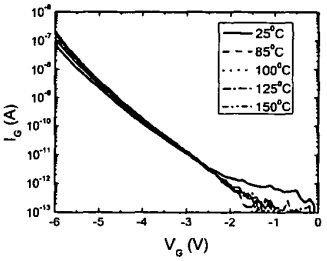


Fig. 6 I_G-V_G curve of ONO barrier at various temperatures.

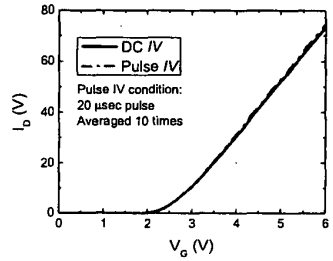


Fig. 7 Comparison of the pulse IV and DC IV results of a BE-SONOS transistor. The pulse IV measurement is carried out in a Keithley 4200 system.

It should be noted that SONOS-type devices tolerate a much less perfect tunneling barrier than the floating-gate device. In the floating-gate device, a single defect in the tunneling barrier can drain the entire charge in the floating-gate, leading to severe charge loss and erratic behaviors. Therefore, tunneling barrier engineering, such as the "crested barrier" [10] concept, for floating-gate devices is difficult to realize due to reliability concerns.

On the other hand, the charges are discretely trapped in SONOS-type devices, hence it is much less sensitive to defects in the tunneling barrier. Therefore, even as the bandgap engineered ONO barrier is not perfect (it contains a SiN layer), BE-SONOS has already shown excellent reliability performance.

IV. Comparisons of BE-SONOS and the Conventional SONOS

Figure 8 compares the –FN erase speed of various SONOS and BE-SONOS devices. The erase speed of BE-SONOS with a 15/20/25Å ONO barrier is comparable with SONOS using a 20Å tunnel oxide. However, SONOS with a 25Å tunnel oxide has a dramatically slower erase speed. For the device erased from fresh state (Fig. 8(a)), the gate injection current is even larger than hole tunneling. This is because oxide has a large hole barrier height (~4.5 eV) so that FN tunneling of hole is negligible for a thicker oxide. Hole direct tunneling occurs only for very thin oxide (<2.5 nm).

Figure 9 indicates that the retention of SONOS with tunnel oxide equal to 20Å is very poor. Although the retention of SONOS with a 25Å tunnel oxide is improved (but still much worse than BE-SONOS), the erase speed becomes too slow for practical applications. Therefore, there is no single tunnel oxide thickness that can satisfy both erase speed and retention requirements for the conventional SONOS.

BE-SONOS can overcome this limitation. BE-SONOS provides far superior data retention than conventional SONOS for the same erase speed. This is achieved by employing the bandgap engineered ONO barrier. In the following sections, the processing methods and reliability performance of BE-SONOS are investigated.

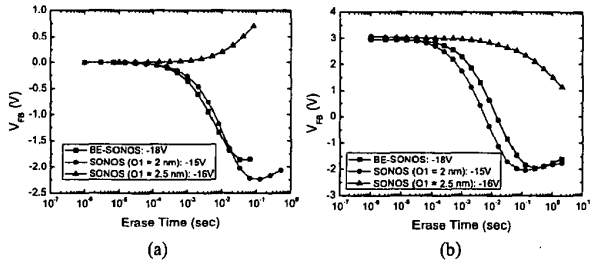


Fig. 8 Comparison of the –FN erase speed of BE-SONOS (15/20/25/70/90Å), SONOS (20/70/90 Å) and SONOS (25/70/90 Å). (a) Erased from fresh state. (b) erased from V_{FB}=+3V. The bias voltages are selected to make these samples to have approximately the same electric field.

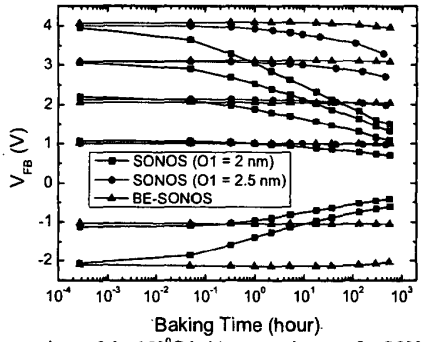


Fig. 9 Comparison of the 150°C baking retention test for SONOS and BE-SONOS (15/20/25/70/90Å). A wide range of PV state (up to +4 V) and EV states (down to EV= -2V) are tested.

V. BE-SONOS Characteristics with Various O1/N1/O2 Tunneling Dielectric

The erase characteristics of BE-SONOS with various ONO barrier thickness are shown in Fig. 10. The results indicate that the erase speed is mainly dominant by O1 only, while O2 and N1 have a small effect. This is consistent with the bandgap engineering concept, where the band offset effectively screens out N1 and O2 so that the thickness dependency is insignificant.

In Fig. 11, the erase speed of various nitridation of O1 is examined. The ONO barrier with thickness of 15/20/25 Å is adopted for all the samples. Two nitridation treatment processes in NO ambient are conducted. One is to apply NO annealing on O1, and the other is to grow O1 directly in NO ambient. Both processes have the same final optical thickness of 15Å.

Significantly enhanced erase speed is achieved with O1 nitridation treatment. This indicates that the speed of hole direct tunneling is raised. One possible reason is the lowering of oxide barrier height by nitridation. Interestingly, the retention shows insignificant dependence on various ONO barrier processes, as shown in Figs. 12 and 13. This implies that we can improve the erase speed by O1 processing tuning without scarifying the retention of BE-SONOS devices.

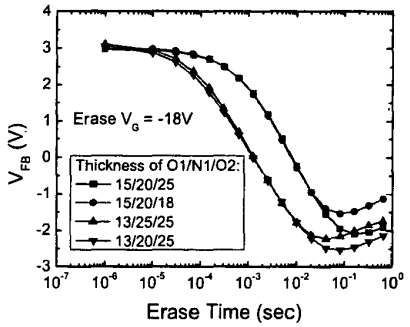


Fig. 10 Comparisons of the –FN erase speed of BE-SONOS devices with various thickness O1/N1/O2 (Å) tunneling barrier. The thickness scheme of N2/O3 is 70/90 (Å) for all samples.

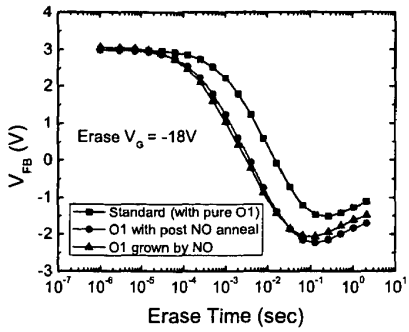


Fig. 11 Comparisons of the –FN erase speed of BE-SONOS devices with various nitridation treatments on O1. The same erase Vg of –18V is applied on all devices.

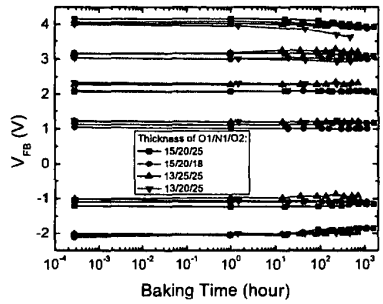


Fig. 12 Comparisons of the150^{0}C retention of BE-SONOS with various ONO barrier thickness (the same devices in Fig. 10).

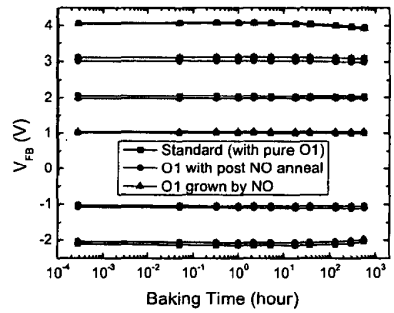


Fig. 13 Comparisons of the150^{0}C retention of BE-SONOS with various nitridation treatments on O1 (the same devices in Fig. 11). All devices perform comparable and this indicates that O1 engineering is not sensitive to data retention characteristic in BE-SONOS device.

VI. BE-SONOS Characteristics with Various O3 Top Dielectric

The top oxide process is also critical for both BE-SONOS and SONOS devices. The role of top oxide is often not seriously taken into account for floating gate devices because most research focuses on the tunnel oxide. However, SONOS-type devices do not have coupling ratio design as the floating gate device and the top oxide must endure similar electric field as that in the bottom oxide during program/erase. This large electric field stress causes a significant impact on the device reliability.

Figure 14 illustrates the -FN erase for various top oxide processes. For the standard wet conversion process, the erase saturated V_{FB} is the lowest one, while HTO top oxide shows a larger saturated V_{FB}. Previous study [11] shows that HTO top oxide has a lower electron barrier height (<3.0 eV) than wet converted top oxide (~3.2 eV). The smaller electron barrier height can results in a larger gate injection of electrons during –FN erase, leading to larger erase saturation V_{FB}.

Fig. 15 shows the endurance performance for both programmed and erased states. All the samples are subjected to the same voltage stress during cycling. For a clear comparison, the threshold voltage shift with respect to the first-cycle result is shown to illustrate the program/erase degradation. The programmed state all shows small degradation. On the other hand, significant erase degradation of HTO top oxide is observed after 1K cycles. Correspondingly, the retention for HTO top oxide is worse than the wet conversion process, especially for the P/E cycled device. These results imply that HTO top oxide is weaker than the furnace wet converted top oxide.

The HTO top oxide can be greatly improved by high temperature annealing. The annealing is carried out in a furnace using a similar thermal budget used in wet conversion. The improvement in the HTO quality in turn improves the endurance and retention performance, as shown in Figs. 15-16. In Fig. 15(b), the erase degradation due to weaker HTO top oxide is greatly improved by the post thermal annealing. The data retention is also improved as shown in Fig. 16, especially for 1K-cycled devices. Recently, we have shown [9] that HTO top oxide easily traps charges under high FN stress. The charge trapping in the HTO top oxide may be the cause of endurance and retention degradation.

We have also applied ISSG to convert nitride into top oxide. ISSG is a low-thermal budget process. In Fig. 14, the erase saturation is in between the HTO and wet conversion. The reliability performance shown in Figs. 15-16 is only slightly worse than that from the wet conversion. These results are encouraging since ISSG has significantly lower thermal budget thus can be applied to TFT memory devices [6,7].

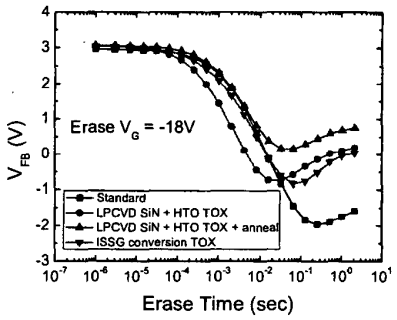


Fig. 14 Comparisons of the –FN erase speed of BE-SONOS devices with various top oxide (O3). The same erase Vg of –18V is applied on all devices.

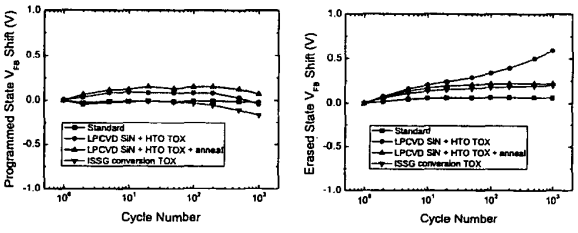
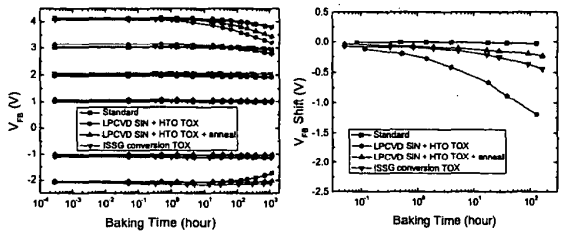


Fig. 15 Comparisons of the endurance for (a) programmed state and (b) erased state. All the device are programmed by +20 V, 200 μsec to V_{FB}~+3V, and erased by –18V 50msec to V_{FB}~ -1 V. The threshold voltage shifts

compared with the first-cycle result are shown to illustrate the program/erase degradation.



(a) (b)

Fig. 16 Comparisons of the 150°C retention for BE-SONOS with various top oxide (O3). (a) fresh device without P/E cycles, (b) charge loss of V_{FB}=+3 V sate for the 1K cycled device. The cycling condition is as the same as that in Fig. 15. The processes with converted top oxide perform consistent even after 1K-cycling stress. The severe degradation in data retention that caused by weak HTO top oxide is revealed in (b). While applied with post thermal anneal, the degradation is significantly reduced.

VII. BE-SONOS Characteristics with Various N2 Trapping Dielectric

The trapping material plays an important role in data storage characteristics. An understand of the trapping layer behavior may lead us to understand why BE-SONOS has such superior reliability performance.

The trapping SiN of BE-SONOS is fabricated by a LPCVD SiN film that is then partially converted to top oxide by high temperature furnace wet oxidation. During this wet oxidation, a transition SiON layer between top oxide and SiN is formed [11].

Our previous works have revealed that there exists some correlation of trapping characteristics between the transition SiON layer and the LPCVD SiON thin film [12]. However, the correlation to reliability characteristics such as data retention has not been evaluated yet. Since the thermal conversion of SiON into top oxide is much more complicated, a HTO top oxide is adopted. From section VI, the HTO top oxide can be strengthened by a furnace thermal anneal in order to minimize the reliability degradation. Here three different trapping materials of standard process, LPCVD SiN, and LPCVD SiON are conducted on BE-SONOS devices to examine the role of the transition SiON layer in the standard process.

The SiN (without wet conversion) trapping material is deposited in a vertical LPCVD furnace using dichlorosilane (DCS) and NH_3, while the SiON is deposited in the same tool using DCS, NH_3 and N_2O. Fig. 17 shows the data retention performance of fresh devices under different baking temperatures. In Fig. 17(a), the standard process continues to show superior data retention even when the initial V_{FB} is programmed to 4V (<200 mV charge loss at 150°C 1000 hours baking). The LPCVD SiON trapping material shows comparable retention performance to that of the standard process but the LPCVD SiN trapping material is significantly worse. When the samples are baked to 250°C (Fig. 17(b)), the programmed state vertical charge loss increases but the SiON group (the standard process and the LPCVD SiON trapping layer) still performs much better than that with only the SiN trapping material. Therefore, it is clearly shown that SiON indeed provides better trapping stability than SiN. Additionally, this suggests that the transition SiON layer very possibly plays a key role in the superior data retention of the standard BE-SONOS process.

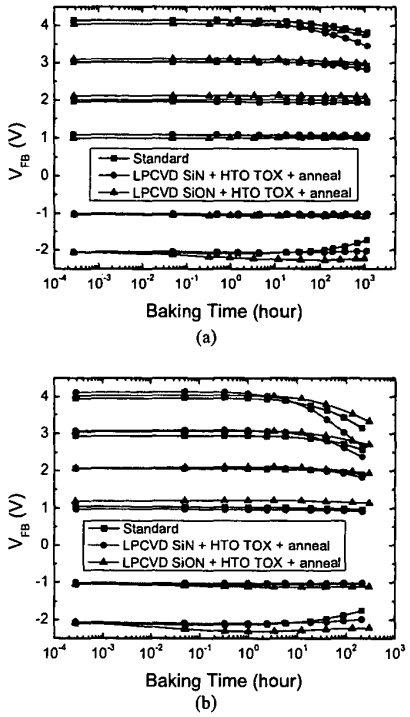


Fig. 17 (a) 150°C and (b) 250°C retention comparisons of BE-SONOS device with standard wet conversion, SiN with HTO and SiON with HTO processes. The tests are executed on fresh devices that directly programmed or erased to the respective six different V_{FB} levels from –2V to 4V.

IIX. Discussions and Summary

The present work provides a comprehensive understanding of BE-SONOS reliability and processing methods. The processing guideline is briefly summarized below:

(1) The erase speed is mainly determined by the thin O1. Therefore, the process control in O1 ($\leq$ 15Å) is critical. On the other hand, N1 and O2 have little impact on the erase speed. Therefore, they are not critical and just have to maintain enough thickness to prevent leakage.

(2) The top oxide must be strengthened so that lower erase saturation Vt and better endurance and retention performances can be obtained. However, this layer often uses the largest thermal budget. Therefore, new low thermal-budget processes such as ISSG or plasma oxidation are the best.

(3) The trapping layer can be replaced by other trapping materials. SiON is found to have better retention than standard SiN. However, it requires more process integration with the top oxide.

(4) For the gate material, a heavily doped P^+-poly gate is used to reduce gate injection during –FN erase.

BE-SONOS uses only well known materials including nitride, oxide, and poly gate. Therefore, it is readily manufactured by CMOS process.

Finally, it should be noted that BE-SONOS is also readily integrated with high-*k*/metal gate materials to further enhance the performances.

SONOS Device With Tapered Bandgap Nitride Layer

Kuo-Hong Wu, Hua-Ching Chien, Chih-Chiang Chan, Tung-Sheng Chen, and Chin-Hsing Kao

Abstract—**A unique, band-engineered, configuration of the charge-trapping layer in silicon–oxide–nitride–oxide–silicon (SONOS) devices is proposed for high-density Flash memory applications. In this paper, a varying Si–N ratio in modified silicon nitride is obtained by controlling reaction gas flow-rate during deposition. This generates a graded composition profile from Si-rich at the bottom to N-rich at the top in a nitride film. The nonuniform composition profile of the silicon nitride layer corresponds to a tapered bandgap and results in significant improvement in device performance and reliability characteristics including operation window, cycling endurance and data retention. The dramatic improvement can be attributed to increased charge-trapping efficiency of the nitride layer since a significant number of highly accessible trapping levels are created in the tapered bandgap. In addition, the increased barrier height between the nitride and tunnel oxide layers also reduces back-tunneling probability and assists charge trapping. The SONOS device designed in this paper is suitable for next-generation Flash memory applications.**

Index Terms—**Endurance and retention, SONOS, tapered bandgap, trapping efficiency.**

I. Introduction

THE RAPIDLY increasing market for portable electronic products such as digital cameras, MP3 players, personal digital assistants (PDA), mobile phones, and external data storage devices for personal computers, has stimulated the development of nonvolatile memory profoundly. Among various nonvolatile memory architectures, Flash memory has out run other competitors due to its full process compatibility with CMOS technology and superior performance. However, conventional floating-gate structure will soon face a limit due to the aggressive scaling trend in the vertical dimension. As a result, the SONOS structure has become an appealing alternative for next-generation Flash memory applications due to its numerous advantages such as film scalability, process simplicity, power economy, operation versatility and radiation hardness [1]–[6]. Nevertheless, some performance and reliability issues such as insufficient charge-trapping efficiency, poor endurance, and short retention must be overcome before SONOS can be utilized in commercial production [7], [8]. In this paper, a promising bandgap-engineering technique using gradual variation of the Si–N ratio during nitride deposition is proposed and a tapered bandgap nitride in a SONOS device is formed [9]. The purpose of the graded composition profile is to adjust the nitride bandgap into a tapered shape so that the substrate-injected charges fall into shallow trapping levels and are transferred to adjacent deeper levels by lateral hopping. This increases the charge-trapping efficiency of the nitride layer. Furthermore, the increased barrier height between the nitride and the bottom tunnel oxide may help constrain the tunneled charges in the nitride and increase its charge-trapping probability. Significantly improved performance and reliability of SONOS devices is achieved.

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II. Experimental

The preparation of test devices basically follows a standard nMOSFET process except that the gate oxide is replaced by an ONO structure and the key process steps for the dielectric layers are as follows. First, a bottom dielectric tunnel oxide (3 nm) was grown by diluted N_2O dry oxidation at 1 standard liter per minute (slm) gas flow rate at 800 °C. Then, the charge-trapping silicon nitride layer (5 nm) was formed in a low-pressure chemical vapor deposition (LPCVD) reactor under various process conditions at 780 °C. In order to manipulate the composition of the nitride layer, the SiH_2Cl_2–NH_3 gas flow-rate ratio was set differently for various film deposition conditions [10], [11]. The SiH_2Cl_2–NH_3 gas flow-rate ratio for standard nitride and uniform Si-rich nitride was maintained constant at 0.23 and 2.07 respectively. In the case of modified nitride, the deposition process was divided into five steps and the gas flow-rate ratio of SiH_2Cl_2–NH_3 was varied from 2.07 at the first step to 0.1 at the last step. The final composition profile of the tapered bandgap nitride film was thus silicon-rich at the bottom and nitrogen-rich at the top. Subsequent to nitride film deposition, a 4.5-nm-thick LPCVD tetraethylorthosilicate (TEOS) blocking oxide was deposited as a capping dielectric. Once the ONO structure was formed, $POCl_3$-doped polysilicon deposition, gate patterning, TEOS coverage, contact hole etching, S/D implant, and the rest of the process simply followed standard CMOS procedure. The final equivalent oxide thickness (EOT) of the ONO stack was 10.3-nm as determined by capacitance–voltage (C–V) characterization and confirmed by scanning electron microscopy (SEM) and high-resolution transmission electron microscopy (HRTEM).

For the sake of evaluating performance and reliability characteristics of all fabricated SONOS devices, an HP4156 high-precision semiconductor parameter analyzer was utilized as the main characterization tool. Essential Flash memory device parameters, such as program/erase (P/E) speed, operation window, cycling endurance and data retention, were examined and compared for different nitrides.

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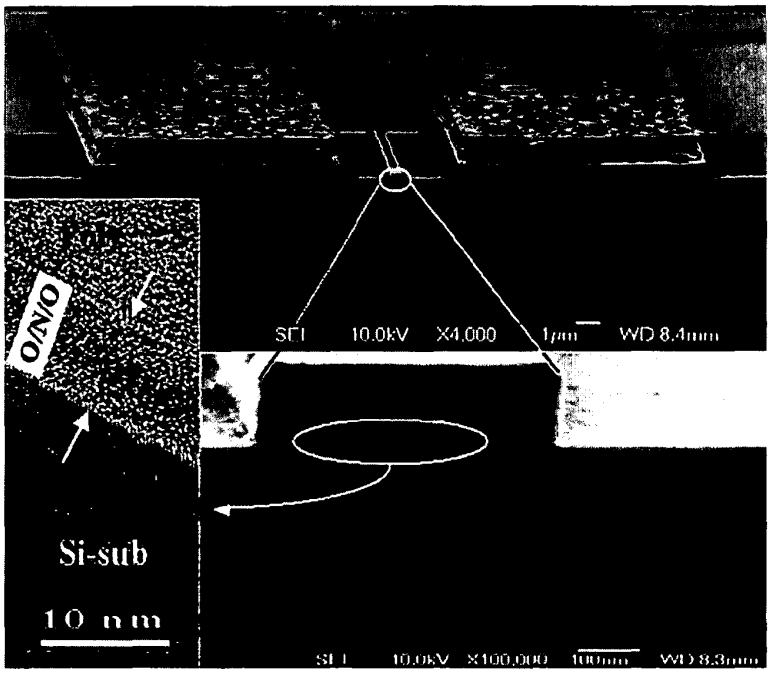


Fig. 1. Cross-sectional SEM and TEM micrographs of a SONOS device confirm the physical thickness of the ONO film.

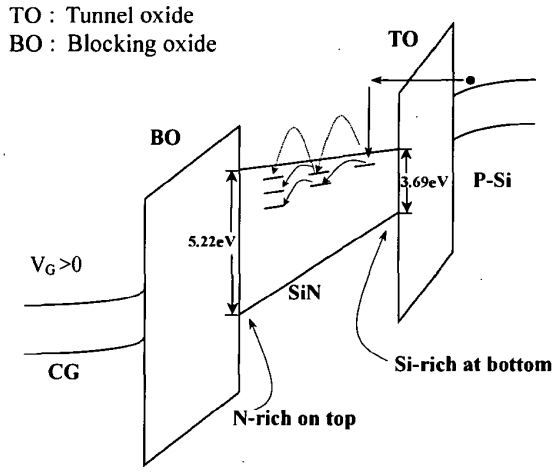


Fig. 2. Tapered bandgap of modified nitride in an ONO structure and the corresponding charge trapping mechanism.

III. Results and Discussion

Fig. 1 shows a cross-sectional SEM micrograph of a test device with tapered bandgap nitride and the physical thickness of each layer of the ONO film is confirmed with TEM analysis. The result of micrographic analysis is consistent with electrical *C–V* characterization. Fig. 2 illustrates the band diagram of a test device incorporating the proposed tapered bandgap nitride. As reported previously [12], [13], the Si–N content ratio determines the bandgap of nitride. A SONOS structure with a varying Si–N composition ratio corresponds to a tapered nitride bandgap and its function may be explained as follows. A gradually increasing bandgap from the bottom to the top of the nitride increases the accessibility of deep trapping levels and an increased nitride/oxide barrier height reduces back tunneling of injected charges. In standard nitride, shallow trapping levels catch incoming charges easily while deep trapping levels are buried underneath and may not be able to capture electrons easily. For uniform Si-rich nitride, the trapping levels are too shallow to trap electrons tightly and they are insufficient in number as well. Consequently, the modified nitride serves as a better solution that provides sufficient and accessible charge-trapping levels for efficient memory storage. As shown in Fig. 2, the substrate-injected charges are first caught by shallow trapping levels and then migrate to deeper trapping levels through lateral hopping. Thus, more trapping levels are available for charge storage. In addition, the increased barrier height between the nitride and the bottom tunnel oxide reduces the probability that injected charges leave trap states in the nitride and therefore increases the charge-trapping probability. Overall, the charge-trapping efficiency of tapered bandgap nitride is improved by its tapered bandgap.

The tapered bandgap is predicted in its design, but it would be highly desirable if the actual bandgap of the nitride could be measured. However, the very thin film thickness (5 nm) and nonuniform bandgap makes any direct measurement almost impossible. As an alternative, two uniform nitride films were grown separately. One is Si-rich ($SiH_2Cl_2/NH_3 = 2.07$) and the other is N-rich (SiH_2Cl_2–$NH_3 = 0.1$) using exactly the same gas flow-rate conditions as the first and the last steps in the tapered bandgap nitride. The optical bandgaps (E_g) of the two different nitride films were characterized by an N&K 1200 thin-film analyzer [14], [15]. The results indicate an Eg of 3.7

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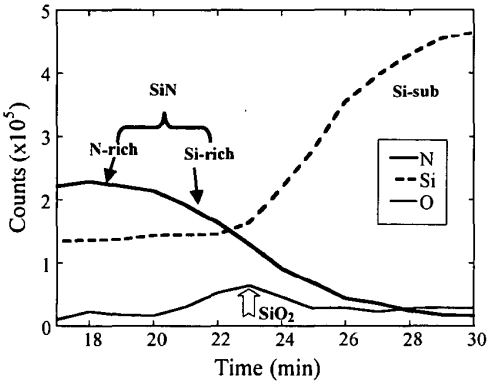


Fig. 3. Auger analysis of a thickened modified nitride in an ONO structure.

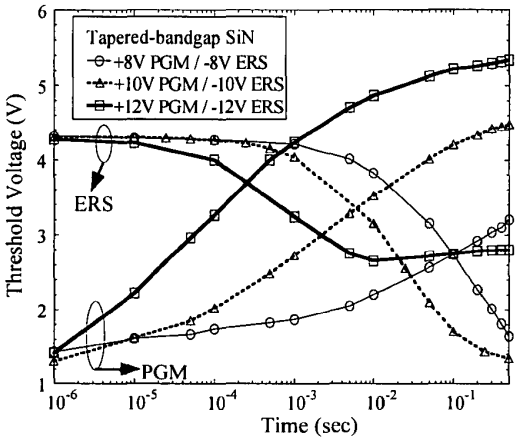


Fig. 4. P/E characteristics of test devices with tapered bandgap nitride under various bias conditions.

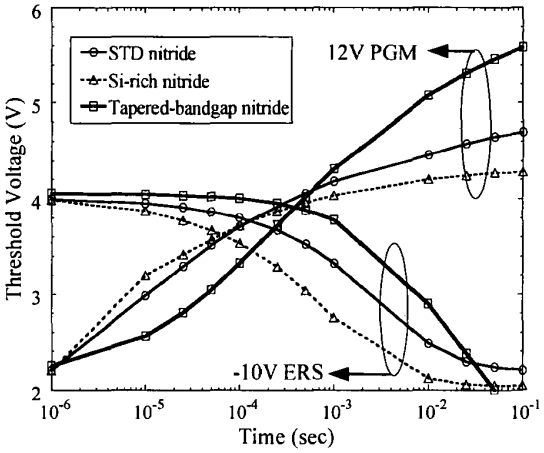


Fig. 5. Comparison of P/E speeds and operation windows for devices with three different nitride films.

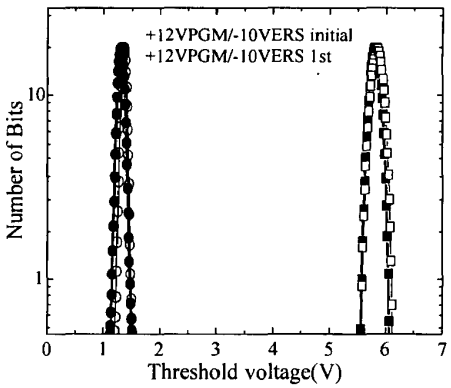


Fig. 6. V_T distribution of test devices initially and after the first P/E operation.

eV for Si-rich nitride and 5.2 eV for N-rich nitride respectively. Another way to probe the actual composition profile of tapered bandgap nitride is to perform an Auger analysis on a thicker sample of tapered bandgap nitride (50 nm thick) prepared by the same five-step gas flow-rate conditions as in the 5-nm-thick modified nitride but with extended deposition times. Since the extended modified nitride film is resolvable by Auger analysis, it can be thought of as a magnification of the original 5-nm-thick modified nitride. A graded composition profile from Si-rich near bottom portion to N-rich near top segment of film is confirmed as shown in Fig. 3.

After detailed material analysis of the ONO dielectrics, a series of electrical characterizations were then carried out. Fig. 4 surveys the P/E response of test devices with modified nitride under different biasing conditions. Although higher voltages result in faster program speed and larger V_T shift, an undesirable early saturation phenomenon occurs after 300 ms during -12 V erasing operations. Therefore, an optimal asymmetric P/E operating voltage of $+12/-10$ V was determined. Once P/E bias conditions were established, the operation speed and window of SONOS devices with three different nitride films were compared in Fig. 5. As shown clearly, test devices with tapered bandgap nitride films exhibit the largest threshold voltage shifts and hence wider P/E operation windows. For test devices with standard and uniform Si-rich nitride, faster initial P/E speed (<0.5 ms) is observed compared to those with modified nitride. The early-stage behavior may be attributed to the fast filling of widespread shallow trapping levels. However, quick saturation also occurs because most accessible trapping levels are filled up instantaneously. For test devices with tapered bandgap nitride, the threshold voltage surpasses that of standard or uniform Si-rich nitride at 0.5 ms due to the greater number of accessible trapping levels and less back-tunneling probability. Although the erase speed of test devices with tapered bandgap nitride seems to be slower, an erase time of 50 ms is sufficient for most operation specifications since block erase is a common operation in Flash circuits. In addition, the self-convergence property of test devices is quite beneficial for multibit operation design. To test reproducibility, a survey of threshold voltage dispersion after P/E operation was conducted and a very tight distribution is observed in Fig. 6. The concentrated threshold voltage distribution suggests that the tested SONOS devices will not suffer tail-bits-sensitivity problems [6] and a shorter block erase time can be expected.

In order to evaluate operational reliability, endurance characteristics of all test devices were compared in Fig. 7. The results imply that residual charges are gradually accumulated

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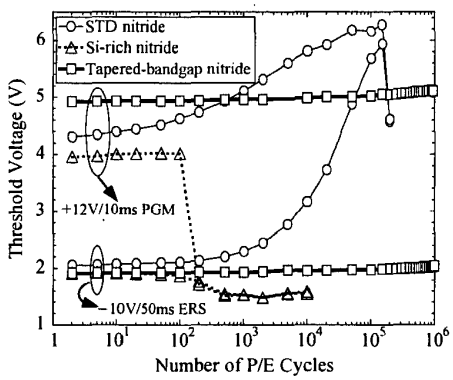


Fig. 7. Endurance characteristics of test devices with three different nitride films.

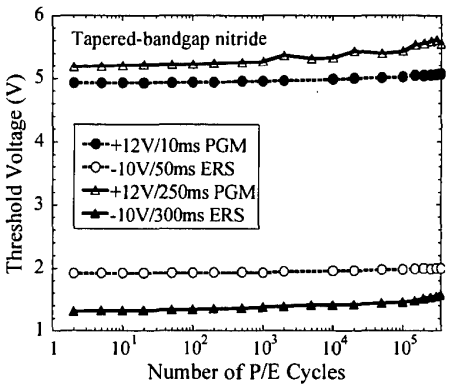


Fig. 9. Highly stressed cycling test of devices with tapered bandgap nitride.

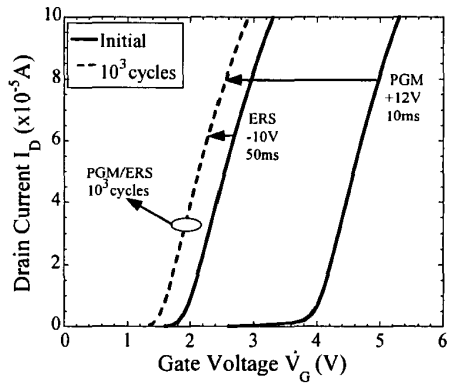


Fig. 8. *I–V* characteristics of test devices with Si-rich nitride before and after 10^3 P/E cycles.

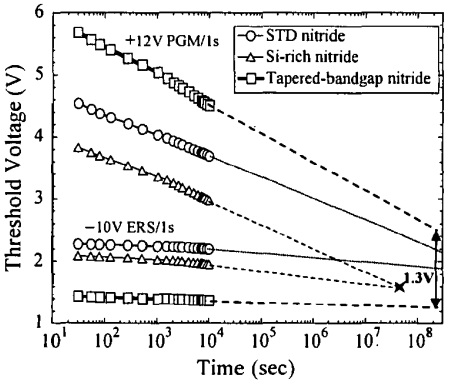


Fig. 10. Data retention characteristics of test devices with different nitride films.

in standard nitride during P/E operation as previously reported by Min She *et al.* [16]. This leads to increasing V_T and eventual loss of charge-trapping ability after 2×10^5 cycles. The charge accumulation takes place by gradual charge transition from shallow trapping levels down to deep trapping levels during repeated program operations. Since the deep trapping levels are buried underneath, the transition is very difficult to reverse by erase operations. Si-rich nitride cannot withstand P/E operations for more than 200 cycles. This result indicates that the extremely shallow trapping levels lose their trapping ability quickly. For the device with tapered bandgap nitride, no observable endurance degradation is observed even after 10^6 cycles. The long endurance of tapered bandgap nitride can be attributed to the highly accessible trapping levels that allow charges to be trapped and de-trapped during P/E operation without much trouble. Although the samples with standard nitride and uniform Si-rich nitride fail after a certain number of cycles, none of the devices actually broke down. Fig. 8 shows the *I–V* characteristics of test devices with uniform Si-rich nitride before and after 10_3 P/E cycles. These electrical stressing results suggest that the tunnel oxide does not breakdown and it is only nitride that loses its ability to trap charges since the off-leakage of the failed device is actually not degraded. The test device with modified nitride survives well even under severe stress condition (+12 V/250 ms and −10 V/300 ms) as shown in Fig. 9.

Another reliability requirement for Flash memory devices is to retain data longer than 10 years. In the retention characterization at room temperature shown in Fig. 10, tapered bandgap nitride exhibits a window of 1.3 V after ten years while the other two do not preserve sufficient charges under same test conditions. Based on extrapolation of these retention characteristics, it is believed that the large operation window of modified nitride is inherited from its superior performance at the beginning. The fact that all samples reveal similar slopes indicates that the nitride layer does not dominate the retention characteristics in our experiment. Therefore, retention characteristics seem to be dictated by the insulating quality of the tunnel oxide in SONOS devices [17]. Similar trends in read disturbance are shown in Fig. 11. However, the self-recovery or soft-programming mechanism during read operation actually improves retention characteristics of device with modified nitride. For devices with standard and uniform Si-rich nitride, serious read-disturb problems lead to shortened data retention as reported previously [18]. One possible theory of the peculiar V_T upsurge of erased bits within the first minute is that the holes pulled in during erase operations tend to accumulate near the bottom oxide due to their poor propagation ability and hence they lower E_c momentarily until incoming electrons recombine with them during a read operation. For devices with tapered bandgap nitride, the substrate-injected holes can migrate easily toward the increased bandgap near the top oxide by lateral hopping and hence do not contribute

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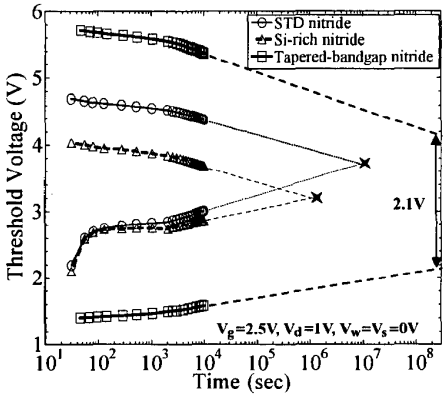


Fig. 11. Read-disturb characteristic of test devices with three different nitride films.

much to electron tunneling during read operations. Overall, the tapered bandgap nitride stands out among the three different nitride structures as demonstrating superior device performance and reliability.

IV. Conclusion

A highly efficient and reliable SONOS device has been developed by optimization of the nitride layer. Based on bandgap engineering, a new SONOS device structure with nonuniform composition nitride has been created. It is found that nitride modified by careful manipulation of the Si–N gas flow-rate ratio during nitride film deposition resultes in a tapered bandgap and significant improvement of device performance as well as reliability. The SONOS device with modified nitride exhibits improved charge-trapping efficiency, cycling endurance, data retention and read disturbance characteristics. The unique modified nitride structure provides a very promising solution for future high-density Flash memory design.

Acknowledgment

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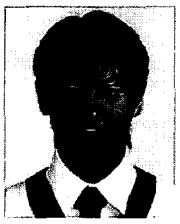
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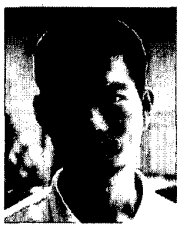
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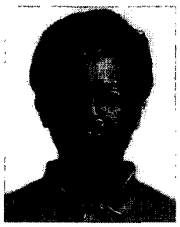
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Reliability considerations in scaled SONOS nonvolatile memory devices

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Abstract

The memory characteristics and reliability of a SONOS nonvolatile memory device are determined, to a large extent, by the charge transport and trapping properties of its storage nitride film. In this paper we investigate carrier trapping phenomenon in a scaled SONOS transistor with an effective gate oxide thickness of 94 and a nitride storage layer deposited with LPCVD at 680°C. Atomic Force Microscopy (AFM) has been employed to examine the surface quality of deposited nitride films. We have found that nitride film deposited at 680°C shows the lowest surface roughness, as compared to the films formed at 725C and 650°C. With a charge separation technique, we have demonstrated that the charge centroid is deep into the nitride layer at low injection levels and moves towards the center of the film as the injection level is increased. From our measurement, a trap density of 1.7×10^{19} cm^{-3} in the nitride has been determined. Devices with nitride (2.1 Å RMS roughness) deposited at 680°C show less degradation in data retention with respect to erase/write cycling when compared to devices with nitride (2.9 Å RMS roughness) deposited at 725°C. © 1999 Elsevier Science Ltd. All rights reserved.

Keywords: Nonvolatile semiconductor memory; SONOS; EEPROM

1. Introduction

Since the 1960's, there have been two major technologies in the field of nonvolatile semiconductor memories (NVSM): the floating-gate structure [1] and the SONOS (polysilicon-blocking oxide-silicon nitride-tunnel oxide-silicon) structure [2]. The principal structural differences between these two types of devices are the nature of the storage medium and the thickness of the tunnel oxide. The relatively thick (70–120 Å) tunnel oxide in floating-gate type memories provides good long-term data retention. A thick tunnel oxide also eases the process control in oxide growth, thus making floating-gate technology a popular choice in the semiconductor industry. However, floating-gate type memories are subject to single pin-hole defects in the tunnel oxide which permit stored charge to escape from the conducting polysilicon layer. On the other hand, the SONOS memory device stores charges in a high density of traps located within an insulating nitride layer. These traps are isolated with each other and, thereby, provide immunity to the deleterious effects of single pinhole defects. The tunnel oxide thickness is in the range of 10–30 Å for SONOS structures. The control of this ultra-thin tunnel oxide was considered to be difficult in the 70's and manufacturers had relatively little experience with the use of thin layers of silicon oxide

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and nitride. As a result, SONOS devices found applications primarily in space and strategic applications due to their radiation hardness. However, as the industry gained familiarity with nitride films in localized oxidation of silicon (LOCOS), SiN cap passivation, multiple dielectrics in DRAM's and interpoly-dielectrics in polysilicon FLASH EEPROM's and ultra-thin CMOS gate oxides of 30–40 Å for 1000–2000 Å channel lengths, the reproducibility of ONO triple dielectrics has been improved greatly and the SONOS structure has become a viable candidate for scaled NVSM technology.

Recently, interest in SONOS technology has been stimulated by the advance of portable computers and personal telecommunication devices. For floating-gate type memories, the on-chip programming voltage is generally higher than 12 V and the scaling of these structures has become difficult. On the contrary, the scalability of SONOS device allows operation at low programming voltage of 5–8 V [3,4]. In addition, channel current is necessary to program floating-gate devices while the programming of SONOS memories does not require channel current, which makes SONOS attractive for battery operated applications.

SONOS nonvolatile memory devices employ Modified-Fowler-Nordheim (MFN) tunneling in both erase and write operations. A high density of traps in the silicon nitride is responsible for charge storage and memory action. To date, the microscopic structure of these traps is not well understood. From their low-temperature electron spin resonance measurement data, Kamigaki et al. [5] proposed a two-trap model in which electrons and holes are captured at different trap centers. They have suggested electron/hole traps are at the interface between silicon cluster and silicon nitride bulk, while hole traps are at nitrogen vacancies in silicon nitride bulk. According to theoretical calculations, Robertson and Powell [6] have suggested that the trivalent silicon center with a dangling bond is the origin of both electron and hole trapping in silicon nitride. The electron spin resonance and injection experiments by Fujita and Sasake [7] and Krick et al. [8] have supported this amphoteric model.

This paper concentrates on reliability considerations of scaled SONOS memory devices with particular emphasis on data retention degradation due to excess erase/write cycling. We investigate the correlation between retention degradation and surface roughness of the nitride film in the ONO dielectric stack. In SONOS devices, a rough silicon nitride surface causes local thinning in the ONO dielectric stack. This local thinning results in a local electric field enhancement which, combined with an increase in nitride conductivity during erase/write cycling, leads to acceleration in charge decay. In the next section, an AFM is used to measure the surface roughness of nitride films deposited at various temperatures. An optimum deposition temperature is found for a given gas flow ratio to achieve minimum surface roughness. Then, the charge trapping properties of this nitride film, including the trap density and the charge centroid movement, is studied. Finally, data retention behavior of devices with a minimum nitride surface roughness and devices with a higher nitride surface roughness are compared.

2. Effect of deposition temperature on nitride surface roughness

Silicon nitride films serve as the storage medium in SONOS devices and optimization of its trapping properties is an important issue. In early studies, the nitride film deposition was performed by atmospheric pressure chemical vapor deposition (APCVD) with a dilute mixture of silane and ammonia at temperatures in the range of 800–900°C [9]. These films suffered nonuniformity due to the high deposition rate. In today's state-of-the-art technology, low pressure chemical vapor deposition (LPCVD) is used to deposit the silicon nitride. The LPCVD nitride is obtained in a reactor at a temperature of 650–750°C when dichlorosilane and ammonia react at the wafer surface. The chemical composition and deposition temperature greatly influence the trapping properties of the silicon nitride. According to Fujita et al. [10], silicon dangling bonds create deep trapping states in the nitride while oxygen and hydrogen atoms act as terminators to decrease the amount of traps. Therefore, silicon nitride films deposited with high $SiCl_2H_2/NH_3$ gas flow ratios show high trap densities, which leads to an improvement in the programming speed of the SONOS memories. A $SiCl_2H_2/NH_3$ gas flow ratio of 75:25 (sccm) has been employed in SONOS transistors designed for fast programming [11]. On the other hand, films deposited with low $SiCl_2H_2/NH_3$ ratios exhibit low trap density. These films have weaker Coulombic repulsion between the trapped charges and reduced charge interaction, which translates into improved data retention. To further improve the data retention of SONOS devices, oxynitride deposited with a mixture of $SiCl_2H_2$, NH_3 and N_2O has been used in place of silicon nitride as the storage medium [12]. The incorporation of oxygen in these films further reduces the trap density and results in longer data retention [13]. As a result, chemical composition in silicon nitride deposition process can be used as a means to control the trap density in SONOS devices. In our work, we have selected a $SiCl_2H_2/NH_3$ gas flow ratio of 10:100 (sccm) to obtain SONOS devices with simultaneous good overall performance in programming speed and data retention.

Deposition temperature is another important parameter to achieve high-quality silicon nitride films.

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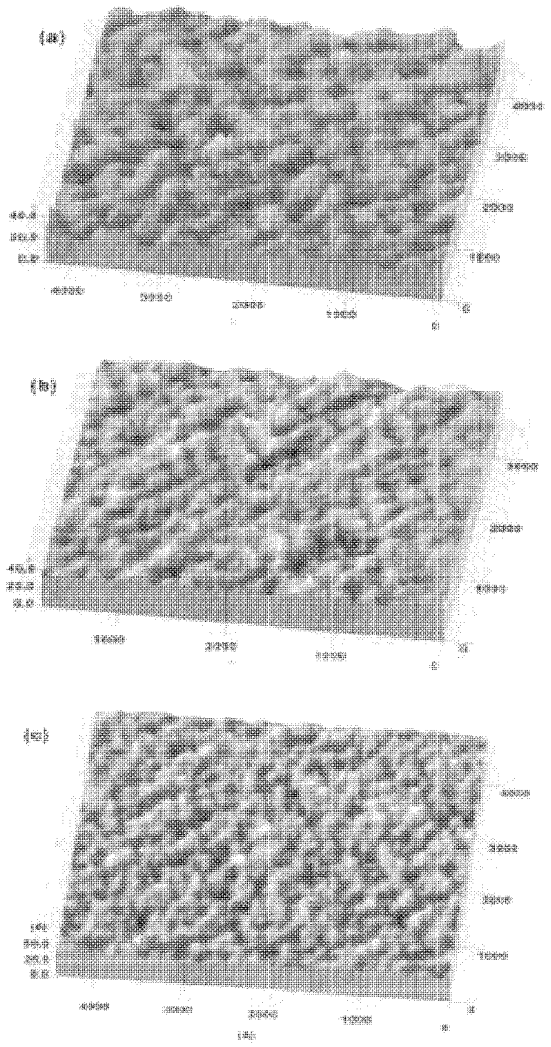


Fig. 1. AFM images of the nitride films in a square region about 4000 Å × 4000 Å. LPCVD nitride deposition temperature are (a) 650°C, (b) 680°C, and (c) 725°C, respectively.

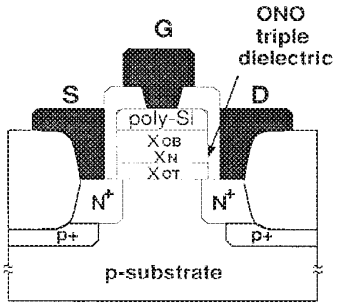


Fig. 2. The device structure of a n-channel SONOS transistor. X_{OT} is the tunnel oxide thickness, X_N is the nitride film thickness and X_{OB} is the blocking oxide thickness.

Tanaka et al. [14] have found nitride films deposited at lower temperatures provide improved breakdown characteristics for the ONO composite films in DRAM storage capacitors. In SONOS devices, surface roughness can cause reliability problems. At a place where local thinning occurs, the local electrical field is enhanced. This film thinning combined with local field enhancement accelerates the charge decay and causes a faster deterioration of the device to erase/write cycling. We have conducted AFM studies on silicon nitride films deposited at different temperatures and discovered an optimum temperature for LPCVD nitride deposition, which achieves minimum surface roughness and improves memory retention.

To investigate the impact of deposition temperatures on silicon nitride surface roughness, three groups of samples, each with 50 Å silicon nitride film deposited at a different temperature on a p-type (100) silicon wafer, have been used in our study. An in situ tunnel oxide of 10–12 Å has been formed in the LPCVD reactor prior to the nitride deposition The silicon nitride deposition has been performed with $SiCl_2H_2$:NH_3 = 10:100 sccm at 650, 680 and 725°C, respectively. The surface roughness of silicon nitride films has been evaluated with an AFM. Fig. 1 shows the AFM images of the nitride films in a square region about 4000 Å × 4000 Å. The surface roughness data from the image analysis is shown in Table 1. The surface roughness is reduced as the deposition tempera-

Table 1
Surface roughness data from the image analysis

Deposition temperature (°C)	Peak to valley (Å)	Mean height (Å)	RMS roughness (Å)
650	37	19	3.4
680	18	8.8	2.1
725	28	14	2.9

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ture is lowered from 725 to 680°C. As the deposition temperature is further lowered to 650°C, an increase in surface roughness is observed.

3. SONOS transistor fabrication

SONOS transistors have been fabricated with N-well CMOS technology and LOCOS isolation processes. The starting material is 2–3 Ω cm (100) p-type substrates. The structure of an n-channel SONOS transistor is shown in Fig. 2. The processing sequence is identical to conventional CMOS technology except for the formation of the ONO dielectric stack. The quality of the tunnel oxide, silicon nitride and blocking oxide determines the electrical properties of these films, which in turn, determines the device characteristics.

Prior to the tunnel oxide growth, the wafers are cleaned with a standard RCA clean procedure, followed by a 100:1 dilute HF etch to remove the thermally and chemically grown oxide. A tunnel oxide of 15 Å is grown at 700°C for 30 minutes by using an argon-diluted oxygen ambient (1.5% O_2 in Ar) in a custom-designed triple wall oxidation furnace [15]. Next, a thin layer of silicon nitride is immediately deposited in a LPCVD reactor for 20 min at 680°C with gas flow rate of $SiCl_2H_2$:NH_3 = 10:100 (sccm). To obtain high quality films, the wafer transfer time from the oxidation furnace to the LPCVD reactor is minimized (i.e. less than 1 min). A thin layer of LPCVD oxide is then deposited with $SiCl_2H_2$:N_2O = 10:100 (sccm) at 725°C, followed by a steam densification at 900°C for 30 minutes. During this steam densification, about 5 to 10 Å of silicon nitride is converted to oxide [16]. The final nitride thickness is 62 Å and the blocking oxide thickness is 42 Å. After the ONO triple dielectric film is formed, a layer of polysilicon is deposited and doped with a $POCL_3$ process. Next, the gate is patterned and the contact windows are opened. A forming gas anneal at 500°C is performed to improve the quality of the Si-SiO_2 interface [17]. The electrodes are then formed with Al(1% Si) sputtering and a 30 min post metal anneal (PMA) is performed at 400°C in a forming gas ambient.

4. Charge injection analysis

In order to understand and model the behavior of SONOS devices, we have examined the charge transport and trapping properties of the nitride films. In this section, we use a charge separation technique to investigate the charge injection, back-tunneling and charge centroid in scaled SONOS transistors. The charge separation, a split C-V technique, is a generalization of the linear voltage ramp (LVR) technique. This

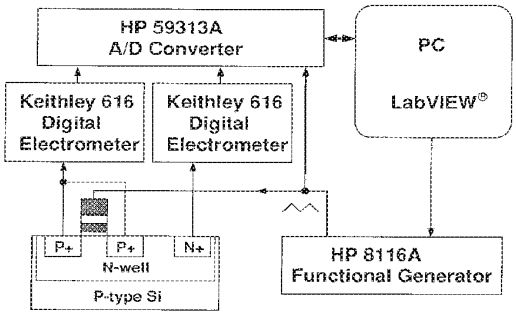


Fig. 3. Block diagram of a computer-aided split C-V data acquisition system. The experimental setup is controlled by a PC using Lab-VIEW® software.

technique was first introduced by Koomen [18] and later pursued by Sodini et al. [19] to investigate the mobility of channel carriers. The difference between this technique and the LVR method is the separate measurement of the bulk and channel charge current as a function of the gate voltage. Agarwal et al. [20] applied this technique to study the charge injection and back tunneling across the tunnel oxide in SONOS transistor. Electron injection and hole back tunneling may be studied with a n-channel SONOS transistor, while hole injection and electron back tunneling can be investigated with a p-channel device. The back tunneling minority carriers cannot be collected by the source/drain junctions due to their recombination with majority carriers at the accumulated semiconductor surface. In a dual-channel SONOS structure, Roy et al.

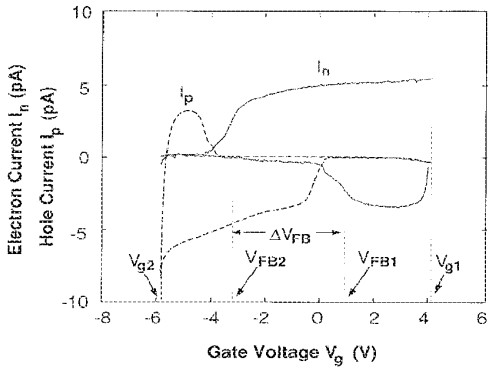


Fig. 4. Experimental curve of a split C-V measurement on a p-channel SONOS transistor with 15 Å tunnel oxide, 62 Å storage nitride and 42 Å blocking oxide. Parasitics have been subtracted from the data. The gate voltage is linearly ramped between a positive voltage V_{g1} and a negative voltage V_{g2} with a ramp rate α of 100 mV/s.

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[21] demonstrated electron and hole charge separation for both gate polarities within one device structure. In our work, we study hole injection and the movement of the hole charge centroid within the nitride film for different injection levels with a p-channel SONOS transistor. The memory or data retention behavior of the excess hole state is presented in the next section.

Figure 3 illustrates the block diagram of a computer-aided split C-V data acquisition system. The experimental setup is controlled by a PC using Lab-VIEW® software. The linear voltage is supplied by a programmable function generator with a triangular waveform. The source and drain electrodes are shorted together. The source and bulk currents are measured with Keithley 616 digital electrometers. In the measurement, the parasitic components are determined and subtracted from the data [20]. Fig. 4 shows an experimental curve of a split C-V measurement on a p-channel SONOS transistor with the parasitics subtracted from the data.

The gate voltage is linearly ramped between a positive voltage V_{g1} and a negative voltage V_{g2} with a ramp rate α of 100 mV/s. The ramp starts at V_{g1} with the p-channel SONOS device in accumulation. Electrons tunnel from the silicon into the nitride conduction band and are captured by the traps in the nitride film. The negatively charged nitride layer corresponds to a positive flatband voltage V_{FB1}. As the gate voltage ramps towards V_{g2}, the semiconductor surface moves successively from accumulation to flatband, depletion, and finally to inversion. During this process, two charge transfer processes may occur: (1) holes may tunnel from the inversion layer to the nitride and trap in the nitride film, and (2) a portion of the previously trapped electrons may back-tunnel from the nitride film to the semiconductor substrate. The net result is a positively charged nitride film and the flatband voltage of the device shifts negatively from V_{FB1} to V_{FB2}.

The injected positive charges, ΔQ_p^{inj}, and the back-tunnel negative charges, ΔQ_n^{bt}, can be written as [21,22]:

$$\Delta Q_p^{inj} = \frac{1}{\alpha A_g}\left(\int_{V_{FB1}}^{V_{g2}} I_p dV_g - \int_{V_{g2}}^{V_{FB2}} I_p dV_g\right) \quad (1)$$

$$\Delta Q_n^{bt} = \frac{1}{\alpha A_g}\left(\int_{V_{FB1}}^{V_{g2}} I_n dV_g - \int_{V_{g2}}^{V_{FB2}} I_n dV_g\right), \quad (2)$$

where α is the gate voltage ramp rate, and A_g is the device gate area. V_{FB1} and V_{FB2} are the device flatband voltages corresponding to electron trapped and hole trapped states, respectively. In the development of these equations we assume a quasi-equilibrium condition during the voltage ramp with all injected charge

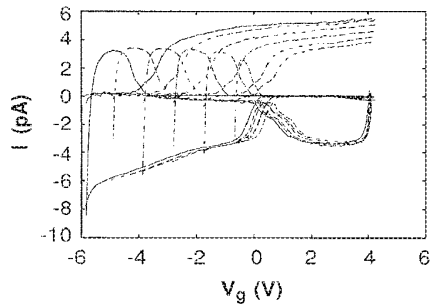


Fig. 5. Experimental results of the split-CV measurement. Parasitics have been subtracted from the data.

remaining in the nitride film. The shift in flatband voltage, ΔV_{FB}, is related to the charge transfer by the following expression [21]:

$$\Delta V_{FB} = \Delta Q_p^{inj}\left(\frac{x_N - \bar{x}_p^{inj}}{\epsilon_n} + \frac{x_{OB}}{\epsilon_{ox}}\right) + \Delta Q_n^{bt}\left(\frac{x_N - \bar{x}_n^{bt}}{\epsilon_n} + \frac{x_{OB}}{\epsilon_{ox}}\right), \quad (3)$$

where $\bar{x}_p^{inj}$ is the injected hole charge centroid, $\bar{x}_n^{bt}$ is the back-tunnel electron charge centroid, x_N is the nitride layer thickness, with ϵ_{ox} and ϵ_n the permittivity of the silicon oxide and nitride, respectively. The charge centroids are measured from the tunnel oxide-nitride interface.

In order to obtain a good signal to noise ratio, we have employed transistors with a length of 100 μm and a width of 100 μm. In our experiments, the gate voltage ramps from a fixed $V_{g1} = 14$ V to a varying V_{g2} ranging from −1 to −6 V. Fig. 5 shows the experimental results of the measurement. As the amplitude of V_{g2} increases, the amount of positive charge in the nitride film and the magnitude of flatband voltage,

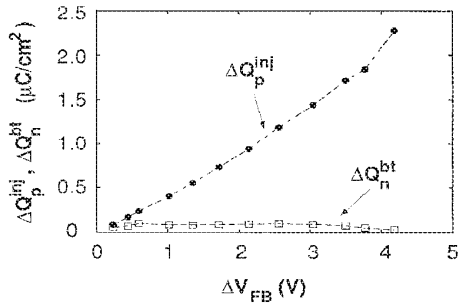


Fig. 6. Relationship between flatband voltage shifts, ΔV_{FB}, and injected holes, ΔQ_p^{inj}, and back-tunneled electrons, ΔQ_n^{bt}.

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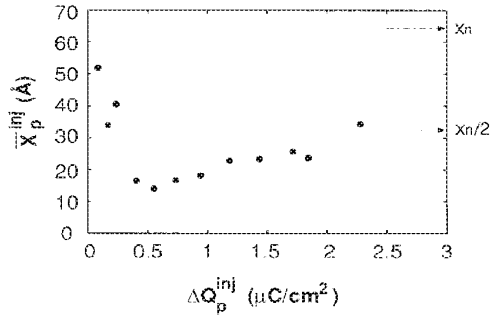


Fig. 7. Extracted values of charge centroid as a function of ΔQ_p^{inj} for $\bar{x}_n^{bt} = 20$Å.

V_{FB2}, increases. The injected hole charge and back-tunneled electron charge are evaluated numerically using Eqs. (1) and (2). Fig. 6 shows the relationship between flatband voltage shift, ΔV_{FB}, and injected hole charge, ΔQ_p^{inj}, and back-tunneled electron charge, ΔQ_n^{bt}. At low injection levels, ΔV_{FB} increases linearly with injected charge ΔQ_p^{inj} while the back-tunnel charge ΔQ_n^{bt} appears constant. Libsch [23] pointed out that even though ΔQ_n^{bt} is a small quantity compared to ΔQ_p^{inj}, it should not be neglected in the calculation of the charge centroid using Eq. (3), especially at low injection levels. In Eq. (3), the value of $\bar{x}_p^{inj}$ can not be exactly determined because $\bar{x}_n^{bt}$ is unknown, even though ΔV_{FB}, ΔQ_p^{inj} and ΔQ_n^{bt} can be obtained experimentally. From the observation of time duration for the back-tunnel process, Roy estimated $\bar{x}_n^{bt}$ to be about 20 Å [21]. Assuming a $\bar{x}_n^{bt}$ value of 20 Å, we can extract the charge centroid as a function of ΔQ_p^{inj}, as shown in Fig. 7. At low injection levels, the electric fields are low and the charge injection occurs at a position close to the nitride-blocking oxide interface (i.e. $\bar{x}_p^{inj} \approx x_N$) which results in a large charge centroid. As the charge injection level increases, the fields are higher, the band bending is more severe and the charge centroid moves closer to the tunnel oxide-nitride interface. Assuming a uniform trap distribution in the nitride, the charge centroid should approach half the nitride film thickness at high injection levels. Using Chao's approach [24], the trap density of the nitride film, N_{T0} can be obtained from the slope of Fig. 7 at increased injection levels:

$$N_{T0} = \frac{1}{4q} \times \left| \frac{\Delta(\Delta Q_p^{inj})}{\Delta \bar{x}_p^{inj}} \right| = 1.7 \times 10^{19} cm^{-3} \quad (4)$$

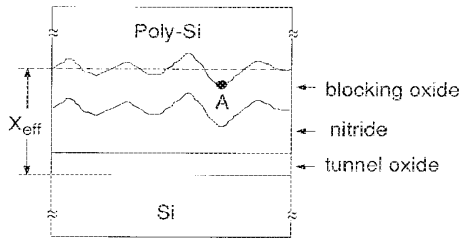


Fig. 8. Schematic cross section of a portion of the channel in a SONOS transistors. Due to surface roughness of the nitride film, electric field at point A is enhanced.

5. Data retention reliability

The nitride films deposited at 680°C have 'smoother' surfaces than films deposited at a higher temperature (725°C) or lower temperature (650°C). In this section, we address the correlation between surface roughness of the nitride film and the data retention characteristics, in particular the resistance of data retention to erase/write cycling for a SONOS transistor. Hu et al. [16] have pointed out charge loss mechanisms in scaled SONOS devices are (1) tunneling of trapped charges to silicon conduction band, (2) tunneling of trapped charges to Si-SiO_2 interface traps, and (3) tunneling of charges from silicon substrate to nitride traps and subsequent recombination of electrons and holes. These tunneling processes are strong functions of electric fields. In nitride films with rough surfaces, local thinning causes an increase in local electric fields for a given voltage. These increased local fields enhance the tunneling processes and accelerate the local charge decay. Fortunately, the nonconducting nature of the nitride prevents the complete discharging from these discrete, localized sites.

The consequences of nitride films with rough surface may not be noticeable. If, however, the device experiences a considerable amount of erase/write cycles, then the nitride film can deteriorate. During erase/write cycling, electrons and holes are injected into the nitride. These injected charges, along with the high field stress, can change the microscopic bond structure and increase the conduction between traps within the nitride [25]. In addition, local thinning can accelerate the nitride deterioration. Fig. 8 illustrates the cross section of a portion of the channel region in a SONOS transistor, assuming the oxide surface roughness is small. At point A in Fig. 8, local field is enhanced by the surface roughness [22]:

$$E = \left(1 + \frac{X_{eff}}{r_c}\right) E_0, \quad (5)$$

where r_c is the local radius parameter characterizing

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Table 2
Fabrication parameters of devices

	Tunnel oxide thickness (Å)	Nitride film thickness (Å) and deposition temperature °C	Blocking oxide thickness (Å)
lot A	15	62, 680	42
lot B	18	50, 725	40

the surface roughness, X_{eff} is the average value of the effective dielectric thickness, and E_0 is the average electric field, respectively. For a programming voltage of 7 V, the maximum value of E_0 is about 8 to 9 MV/cm depending on the amount of stored charges in the nitride. Because of the local thinning, the local fields can be much higher than E_0. These enhanced electric fields facilitate the injected charges with higher energies, thereby accelerating the degradation of nitride films. As a result of a local field enhancement and an increased nitride conductivity, an increase in charge decay rate becomes observable after extensive erase/write cycling.To examine the effect of nitride surface roughness on data retention reliability, SONOS nonvolatile memory transistors have been employed from two lots, A and B. Devices in lots A and B are fabricated with basically the same technology outlined in the device fabrication section, except for the formation of the ONO triple dielectrics. Except for a slight difference in dielectric film thickness, the storage nitride in lot A is deposited at 680°C while the nitride in lot B is deposited at 725°C under the same gas ratio and reactor pressure. The differences in ONO layer parameters between lot A and lot B are summarized in Table. 2. We have examined the data retention characteristics for the excess electron state in devices from both lots. The retention characteristics do not show degradation to erase/write cycling. On the other hand, erase/write cycling influences the data retention of the excess hole state. Similar observations have been made by White et al. [26]. Fig. 9 shows a typical data retention characteristic for the excess hole state of an n-channel SONOS devices from lot A, before and after 1 million erase/write cycles. Retention characteristics for the n-channel SONOS devices from lot B are shown in Fig. 10. These measurements are performed at 85°C, which is the highest temperature specified for commercial EEPROMs. First, we notice in both Figs. 9 and 10 the device threshold voltage is shifted positively after 1 million erase/write cycles which indicates a net increase in negative charge trapping within the dielectric [27]. Secondly, the threshold voltage decay rate is a measure of the discharging rate because the threshold voltage shift is proportional to the amount of charge trapped in the nitride. The threshold voltage decay rate is 0.16 V/dec for devices in lot A and remains unchanged after the device experiences 1 million erase/write cycles. For devices in lot B, the threshold voltage decay rate is 0.14 V/dec before the erase/write cycling, which is slightly smaller than that of lot A due to the slightly thicker tunnel oxide. However, the threshold voltage decay rate is increased to 0.17 V/dec after 1 million erase/write cycles. In order to make meaningful comparison, erase/write cycling conditions must be carefully arranged. In our experiments, the devices from both lots experience the same electric field strength (about 8.5 MV/cm) with approximately the same

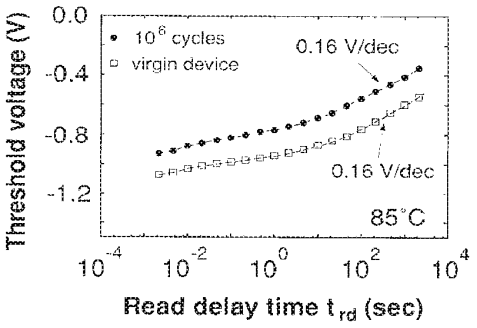


Fig. 9. Typical data retention of n-channel SONOS transistors of lot A. Open squares are data taken before erase/write cycling, while solid circles are data taken after 1 million erase/write cycles. All data is taken at 85°C.

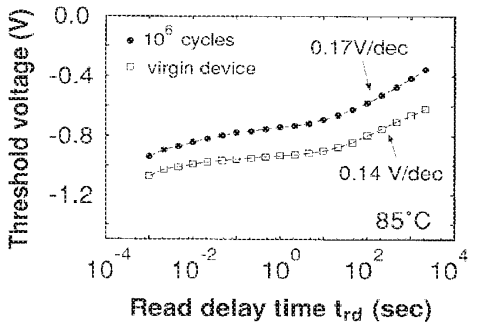


Fig. 10. Typical data retention of n-channel SONOS transistors of lot B. Open squares are data taken before erase/write cycling, while solid circles are data taken after 1 million erase/write cycles. All data is taken at 85°C.

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amount of charge passing through the tunnel oxide during erase/write cycling.

6. Conclusion

Silicon nitride film surface roughness can be reduced when LPCVD is performed at 680°C, as compared with 650 and 725°C, which indicates there exists an optimized temperature range for nitride deposition to achieve a silicon nitride film with a smoother surface. With a charge separation technique, we have investigated the trapping properties of nitride films deposited at 680°C. The effects of nitride surface roughness on SONOS device data retention reliability are discussed. We postulate local thinning due to silicon nitride films with rough surfaces can (1) accelerate the nitride degradation with erase/write cycling, and (2) enhance the discharge of trapped charges in the nitride. Furthermore, we demonstrate the data retention of scaled SONOS nonvolatile memory devices can be improved by employing a smoother nitride.

Acknowledgements

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An EPROM Cell Structure for EPLD's Compatible with Single Poly-Si Gate Process

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Abstract—**A single poly-Si gate EPROM cell structure, which can eliminate the process complexity involved in conventional double poly-Si EPROM technologies, is proposed to realize EPLD's with a faster turnaround time. Since the proposed cell uses an n^+ diffused layer on a bulk Si substrate as a control gate instead of a second poly-Si, markedly improved reliability is obtained, especially for bias stress data retention. This is due to the higher quality of bulk Si oxide, compared with an interpoly insulator of double poly EPROM's. Basic cell characteristics (write, erase, *I–V*, high temperature data retention, etc.) are almost the same as those for a double poly cell. It was found that the single poly cell is easily combined with logic's single poly and double metal process, therefore it should greatly contribute to developing CMOS EPLD's in spite of the cell area increase.**

I. Introduction

With the rapid development in application specific integrated circuits (ASIC's), CMOS erasable programmable logic devices (EPLD's) are now receiving much attention. CMOS EPLD's can realize user programmable and reconfigurable logic devices with a faster production turnaround time. Moreover, new devices with more sophisticated AND, OR, NAND or NOR array configurations can be easily developed by EPLD's. Therefore, it should be necessary to combine current double poly CMOS EPROM technologies [1]–[3] with advanced architecture and circuit techniques. Since most popular logic devices use a single poly-Si gate and double metal technologies, the introduction of conventional double poly-Si EPROM technology to a logic process naturally leads to fabrication process complexity and degrades production yields, resulting in die cost increase. Moreover, novel process technologies should be used to form a reliable interpoly-Si insulator, such as high temperature oxidation [4] and stacked CVD film technology [5], as well as double poly cell formation with plasma etching. Recently, several attempts have been made to introduce a single poly technology into EPROM memories [6]–[8].

This paper describes newly developed single poly-Si gate EPROM cell technology in detail. The structure uses an n^+ diffused layer on a Si substrate as a control gate (CG) to meet the previously mentioned requirements. As the n^+ layer is additionally formed for CG and used instead of an n-well layer [6], relatively smaller cell sizes are realized. Obtained cell performance and reliability have been found sufficient for fabricating EPLD's. Thus, the possibility of applications to logic and microprocessors are also increased.

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II. Cell Structure and Fabrication Process

A typical cross section of proposed single poly-Si gate cell structure is shown in Fig. 1(a), compared with a conventional double poly cell (Fig. 1(b)). In the single poly cell, the n^+ diffused layer in the bulk Si substrate is used for a control gate (CG), instead of a second poly layer, which is capacitively coupled to an extended poly-Si floating gate (FG). A top view photograph is shown in Fig. 2. Both the cell transistor channel region and the CG n^+ layer are fabricated on the Si substrate and are electrically isolated from each other by an isolation field oxide. Fig. 3 shows one example of the cell layout in the memory array. Control gate and source regions are shared by two adjacent cells. The unit cell area is about two and a half times larger than for conventional cells. For example, about 50-μm^2 cell size with 1.2-μm design rule has been realized, compared with the 19.8-μm^2 double poly cell. It should be noted that this cell size can be applicable not only for the logic and microprocessor field, but also for medium scale memory devices and logic devices with medium density memories. In the new cell, since the CG is embedded in the Si substance, the CG's total capacitance increases to around five times that of a conventional double poly cell. Considering that n^+ CG sheet resistance ($\sim$40 Ω) is comparable to that for a poly CG, RC delay will increase. Since n^+ word line resistance can be reduced by a second Al snapping technique, a word line delay increase can be prevented. If the second Al can not be available, an n^+ CG should be divided appropriately.

Table I shows device process parameters for fabricated cells. The process sequence is shown in Fig. 4, which is based on a 1.2-μm NMOS technology with 200-Å gate oxide. After the field isolation oxide formation, a photo mask step was carried out to define CG n^+ layers. Then, the first gate oxide and control gate oxide were simultaneously formed. The first gate oxide was 200-Å thick. Oxide thickness on the n^+ control gate layer usually becomes more than 200 Å, due to the oxidation rate enhancement for highly doped n^+ layers. After that, the

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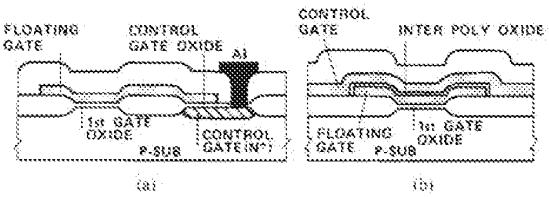


Fig. 1. Cross-sectional views of (a) single poly gate EPROM cells, and (b) conventional double poly gate cells.

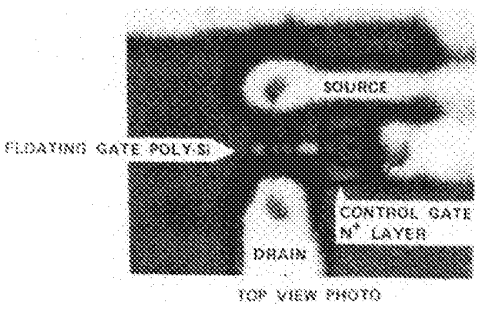


Fig. 2. Top view photograph of the single poly cell test structure.

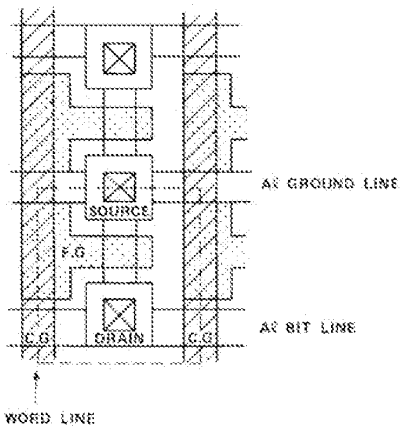


Fig. 3. Typical memory cell layout.

poly-Si layer was deposited, followed by phosphorus doping. Finally, the poly-Si gates were defined.

Essentially, for the new EPROM cell, only one extra photomask step to define the CG n^+ layer and the n^+ ion implant process, has to be added to conventional logic process. However, if logic parts require LDD or DDD NMOS, one more extra mask step with additional n^+ implants will be necessary [8].

One of the key fabrication technologies for the cell is the gate oxide formation. For an EPROM cell, capacitance coupling between FG and CG strongly affects the electrical characteristics. Gate oxide thickness, between FG and CG, namely CG oxide thickness, determines coupling ratio. The oxide thickness ratio between CG oxide and cell gate oxide greatly affects the coupling ratio. This

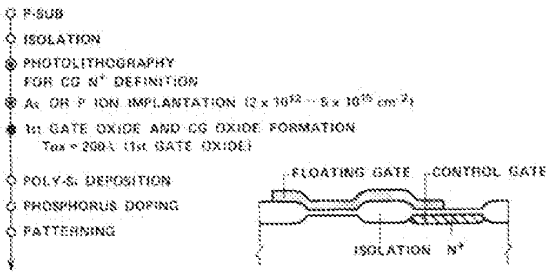


Fig. 4. Process sequence for the single poly cell.

TABLE I
DEVICE PROCESS PARAMETERS FOR SINGLE POLY CELLS

Leff	0.7 μm
W	1.2 μm
GATE OXIDE	200 Å
CG OXIDE	200 ~ 600 Å
CG N+	As 1/1 2×10^{12}cm^{-2}, 100 keV
STRUCTURE	As 1/1 5×10^{15}cm^{-2}, 35 keV
	P 1/1 5×10^{15}cm^{-2}, 35 keV

oxide thickness ratio depends upon oxidation temperature, because CG oxide is formed on an n^+ diffused layer. Fig. 5 shows the relationship between the first gate oxide thickness and CG oxide thickness as a function of oxidation temperature. The first gate oxide thickness was controlled to 200 Å. Higher oxidation temperature can realize a relatively thinner control gate oxide. Thus, using the diluted high-temperature oxidation method, a thin gate oxide can be formed on the channel and the CG n^+ region, simultaneously. An increase in capacitance coupling, due to thin oxide formation, leads to fast READ/WRITE speed or reduction in the unit cell size. Note that since the breakdown field strength for CG oxide on n^+ is generally lower than that for cell gate oxide, i.e., around 70 percent of oxide on lightly doped substrate even with diluted oxidation method, thicker CG oxide will be preferable for production.

To investigate the effect of deep depletion layer formation in CG on WRITE characteristics, various CG n^+ diffused structures were examined. The CG n^+ layers, formed by P ion implantation and As ion implantation with higher and lower dosages, were examined.

III. Experimental Results and Discussion

A. Electrical Cell Characteristics

Basic WRITE characteristics for the new cell with W/L_{eff} = 1.2 μm/0.7 μm are shown in Fig. 6. The new cell shows better WRITE speed than the conventional cell, but this comes from a smaller CG to FG capacitance coupling capacitance ratio and a shorter effective channel length. Since the cell WRITE properties fundamentally are governed by the coupling capacitance ratio and gate length, the new cell and conventional cell will show almost the

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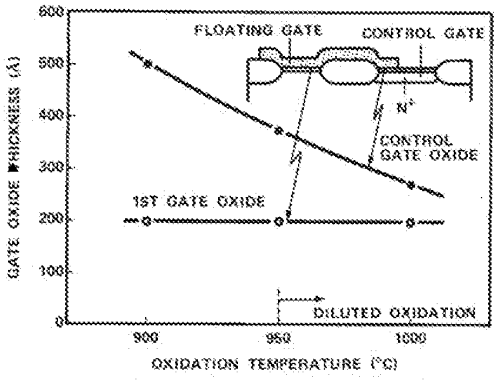


Fig. 5. Relationship between first gate oxide thickness and control gate oxide thickness as a function of oxidation temperature. N^+ CG region is formed by As ion implants, with 5×10^{15} cm^{-2} dose. Oxidation conditions are 900°C, dry O_2, 950°C, 20-percent N_2 diluted—and 1000°C, 20-percent N_2 diluted oxygen oxidation, respectively.

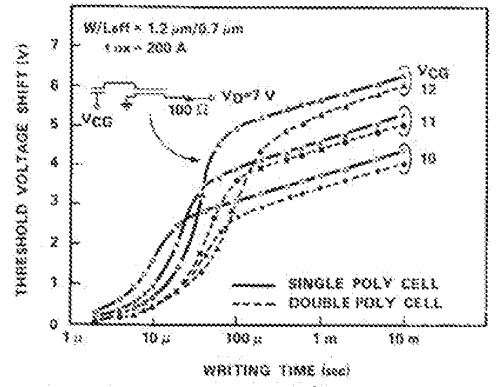


Fig. 6. Write characteristics for single poly cells as a function of control gate voltage, compared with those for double poly cells. Cell parameters are as follows: 1) for single poly cell, $t_{ox} = 200$ Å, $CG_{ox} = 500$ Å, CG–FG coupling area $= 5.52$ μm^2, $L_{eff} = 0.7$ μm, and 2) for double poly cell, $t_{ox} = 200$ Å, interpoly $= 280$ Å, CG–FG coupling area $= 4.32$ μm^2, $L_{eff} = 0.72$ μm.

same characteristics, if these parameters are the same. It is clear that around a 5-V threshold voltage shift can be obtained after writing within 100-μs of writing time. This value is substantial for practical application.

In the new cell, since the CG is formed by an n^+ diffused layer and isolated from the channel region by the field oxide, maximum write voltage exists. This is determined by the lowest voltage for the CG n^+ junction breakdown voltage, the turn-on voltage for the parasitic poly-gate field transistor, and the punchthrough voltage between the CG and the channel region for the cell. Fig. 7 shows the limiting CG voltage as a function of isolation oxide width. Above 1.2-μm isolation width, the punchthrough voltage and the threshold voltage for the field transistor are higher than 14 V, which is the junction breakdown voltage. Therefore, a standard 1.2-μm EPROM WRITE voltage, 12.5 V, can be used with sufficient margin.

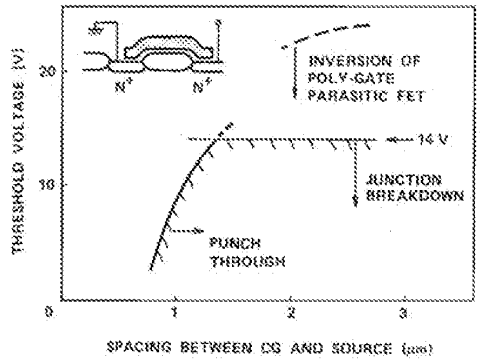


Fig. 7. Limiting control gate voltages as a function of field isolation width.

In order to evaluate the CG n^+ doping concentration effect on the WRITE characteristics, three junction structures were examined. Phosphorus ion implant (5×10^{15}cm^{-2}), arsenic ion implants at higher (5×10^{15} cm^{-2}) and lower (2×10^{12} cm^{-2}) dosages were compared. As the doping concentration in n^+ layer decreases, the depletion layer in the CG becomes easily formed, leading to effective writing voltage decrease. To estimate this effect, threshold voltage shifts after writing, as shown in Fig. 8, were examined. Around 1 V degradation for 2×10^{12} cm^{-2} As dosage is observed. As this value is not so large, it becomes possible to utilize this CG formation dose by optimizing WRITE CG voltage and writing time. Since EPROM's sometimes use depletion (D) type NMOS (As dose is around 2×10^{12} cm^{-2}) in the circuits, the D-type NMOS channel implants can replace CG n^+ doping ion implants, if D-type NMOS is implemented in EPLD's. In this case, the extra n^+ defined mask and n^+ ion implant process can be completely reduced.

Fig. 9 shows typical *I–V* characteristics for the cell. Cell READ current I_d of 140 μA at $V_d = 1.5$ V with a 5.5-μm^2 gate coupling area is obtained. This is about 1.5 times larger than that for the conventional cell. Essentially, since the channel width and the FG potential determines the cell READ current, it is possible to gain more READ current by increasing the channel width, along with increasing the CG area, to meet the requirement for higher speed operation.

Ultraviolet (UV) light ERASE characteristics are shown in Fig. 10. Erasing speed is almost 2.8 times faster than that for the double poly cell. This enchancement is well explained by the model [9], in which the UV irradiated FG perimeter length, facing the n^+ layer, dominates the erasing speed [6], [9]. To maintain this desirable fast erasing feature, precautions on actual cell layout are necessary to maximize the FG perimeter length as much as possible.

B. Reliability

One of the most important items regarding EPROM reliability is the bias stress data deprogramming immunity [1], [5] and high-temperature data retention.

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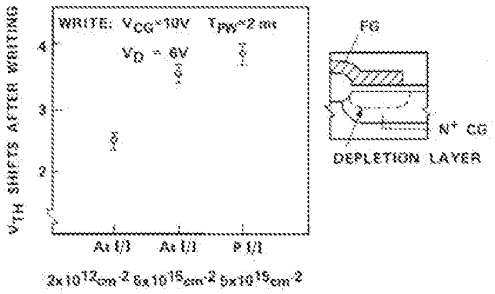


Fig. 8. Control gate doping concentration effect on the threshold shift after writing.

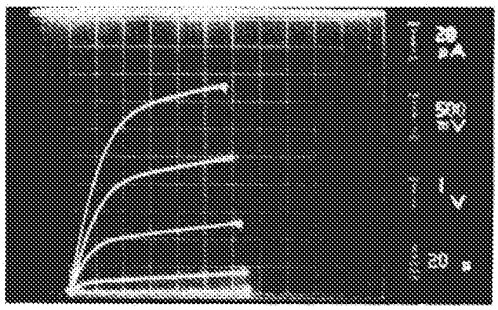


Fig. 9. Typical I-V curve for single poly EPROM cells with 5.5-μm^2 gate coupling area. L_{eff} = 0.7 μm, and W = 1.2 μm. $V_{D\,MAX}$ = 5 V.

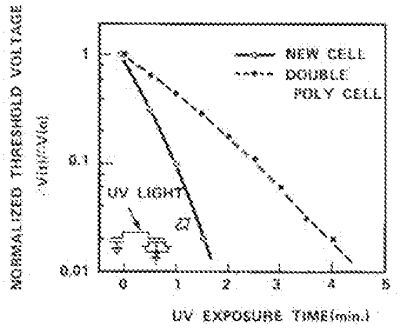


Fig. 10. Erase characteristics for single poly cells, compared with those for double poly cells.

Data deprogramming characteristics for the new cell, by applying a positive voltage on CG, are shown in Fig. 11. More than 5-MV/cm electric field strength for the single poly cell was obtained, which is about 2 MV/cm higher than that for a conventional double poly cell with poly oxides as an interpoly insulator. Below the CG n^+ layer junction breakdown voltage, current leakage from FG is completely suppressed. This feature results from the use of the bulk Si oxide instead of a poly oxide for a double poly cell. The poly-oxide leakage electric field strength is generally lower than that for bulk Si oxide, due to the grown poly-Si surface asperity [10] and the degradation in oxide quality related defect density increase [11].

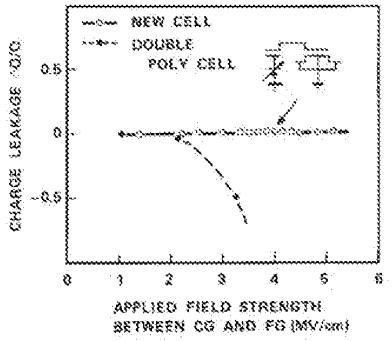


Fig. 11. Data deprogramming characteristics as a function of applied positive bias electric field on control gate.

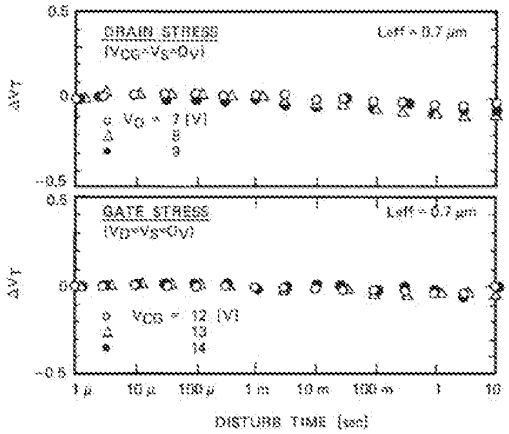


Fig. 12. Write-disturb characteristics for drain and gate stress conditions as a function of stress time.

Moreover, the single poly-Si gate structure itself improves the leakage resistance. Generally, the electric field enhancement at the FG poly-Si edge, which is conformally surrounded by the CG poly-Si, dramatically reduces the electric field strength for a double poly cell. On the other hand, since the single poly cell structure has no edge effect, no electric field enhancement problems occur. As a result, without a special interpoly insulator (high quality poly oxide [4], stacked CVD layer, such as ONO structure [5], etc.) technology, a reliable cell can be obtained. Fig. 12 shows WRITE-DISTURB characteristics as a function of stress time. Both for gate and drain stress conditions, no significant degradation is observed.

Fig. 13 shows the worst cell data retention characteristics for the single poly-gate structure as a function of temperature. High temperature retention is found to be essentially the same as for conventional double-poly gate EPROM cells, because the quality of the poly oxide covering the FG determines the thermionic electron emission from the floating gate [12]. Since about 0.8-eV activation energy was obtained for the worst case samples, more than 10 years' data retention at 150°C has been ensured.

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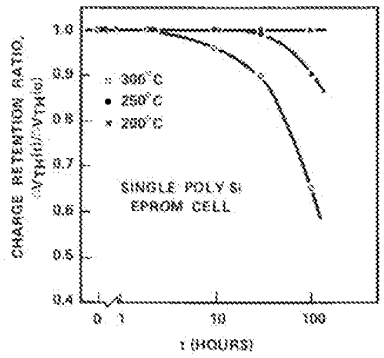


Fig. 13. High temperature bake retention characteristics.

IV. Summary and Conclusion

A single poly-Si gate EPROM cell technology has been described and discussed. In spite of a slight increase in unit cell area with a single poly-Si gate cell, the proposed cell shows marked reliability and realizes substantial cell electrical performance. Thus, by adding a few extra process steps, the introduction of this cell to the logic and microprocessor field will greatly contribute to the development of ASIC's.

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Application Number:	17157350
International Application Number:	
Confirmation Number:	6135
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
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First Named Inventor	Igor Polishchuk
Art Unit	1737
Examiner Name	Not Yet Assigned
Attorney Docket Number	PM07027D1CIP1C6

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The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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Signature	/Michael L. Bartholomew/	Date (YYYY-MM-DD)	2021-05-25
Name/Print	Michael L. Bartholomew	Registration Number	60225

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	3	20090011609	A1	2009-01-08	Ramkumar et al.	
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Application Number:	17157350
International Application Number:	
Confirmation Number:	6135
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
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1	Transmittal Letter	IDS-Letter_2021-05-24.pdf	80808 fa5e4f81ffb9b82fab73e488a19679fa2109cae4	no	1

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2	Foreign Reference	WO2013148343A1.pdf	3484314 bd90146dc2cb581f36d591983a1fd77c0029d175	no	54
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37	Non Patent Literature	10GEA_10_Gigabit_Ethernet_Technology_Overview_White_Paper_2001_pages_1-22.pdf	697558 56f2ac092e91d33c051ad579217efca4233aea87	no	22
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47	Non Patent Literature	CARLEY_Trimming_Analog_Circuits_Using_Floating-Gate_Analog_MOS_Memory_1989_pages_1-7.pdf	537853 57071e2c6c83e707088ed0fc6e15b29258d57ce9	no	7
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48	Non Patent Literature	CHEN_Performance_Improvement_of_SONOS_Memory_2004_pages_1-3.pdf	219359 dbc8157cd94508f1f43a629723e04cc57fc2ed44	no	3
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49	Non Patent Literature	CHIEN_Two-bit_SONOS_type_Flash_2005_pages_1-2.pdf	191171 11a64c9a9be27d92f261251d4ffdfe8cff7e192d	no	2
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50	Non Patent Literature	CHO_A_Novel_Robust_and_Low_Cost_Stack_Chips_Package_2000_pages_257-265.pdf	782100 19582e08a7438f735fe9443bfa07e9b02d112e17	no	10
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51	Non Patent Literature	CUPPENS_An_EEPROM_for_Microprocessors_and_Custom_Logic_1985_pages_603-608.pdf	941974 fb5591f0d8abe708a125c821b9cfd2550d5204df	no	6
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52	Non Patent Literature	CYPRESS_1-8V_500-MHz_10-Output_JEDEC-Compliant_Zero_Delay_Buffer_2004_pages_1-9.pdf	288137 4ee46add5f9eff439e20337d31f96f382793a6a4	no	9
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Igor Polishchuk et al.

Application No.: 17157350 Confirmation No.: 6135

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Title: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Examiner: Not Yet Assigned

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To Whom it May Concern:

In compliance with 37 C.F.R. § 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08.

Pursuant to MPEP 609.02, Applicant(s) expect the Examiner to also consider all the references submitted, cited, or otherwise considered during the prosecution of all the ancestor applications listed on the application data sheet of the present application. The Applicant(s) are resubmitting a listing of references submitted, cited, or otherwise considered during the prosecution of all the ancestor applications listed on the application data sheet so they may appear in the cited references section of the patent should this application proceed to issue.

No fee is required for the submission of this Information Disclosure Statement.

Dated: May 24, 2021

Respectfully submitted,

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Espacenet

WO2013148343A1 OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

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Inventors: GEHA SAM [US],JENNE FREDRICK [US],LEVY SAGY [IL],RAMKUMAR KRISHNASWAMY [US]

Classifications:
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OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

Abstract

An embodiment of a semiconductor memory device including a multi-layer charge storing layer and methods of forming the same are described. Generally, the device includes a channel formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide layer overlying the channel; and a multi-layer charge storing layer including an oxygen-rich, first oxynitride layer on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean, second oxynitride layer on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense. In one embodiment, the device comprises a non-planar transistor including a gate having multiple surfaces abutting the channel, and the gate comprises the tunnel oxide layer and the multi-layer charge storing layer.

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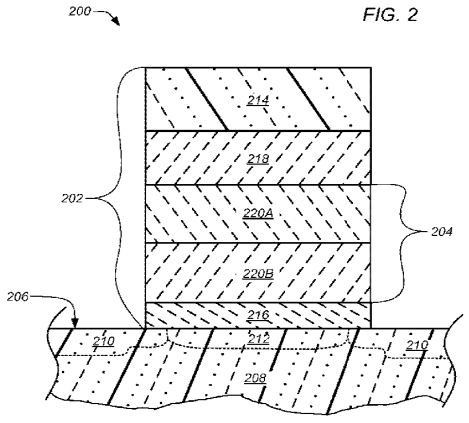
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(54) **Title**: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

FIG. 2



(57) **Abstract**: An embodiment of a semiconductor memory device including a multi-layer charge storing layer and methods of forming the same are described. Generally, the device includes a channel formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide layer overlying the channel; and a multi-layer charge storing layer including an oxygen-rich, first oxynitride layer on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean, second oxynitride layer on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense. In one embodiment, the device comprises a non-planar transistor including a gate having multiple surfaces abutting the channel, and the gate comprises the tunnel oxide layer and the multi-layer charge storing layer.

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Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of co-pending U.S. application Ser. No. 11/811,958, filed June 13, 2007, which claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 60/931,947, filed May 25, 2007, both of which are incorporated by reference herein.

TECHNICAL FIELD

[0002] This invention relates to semiconductor processing and, more particularly to an oxide-nitride-oxide stack having an improved oxide-nitride or oxynitride layer and methods of forming the same.

BACKGROUND

[0003] Non-volatile semiconductor memories, such as a split gate flash memory, typically use a stacked floating gate type field effect transistors, in which electrons are induced into a floating gate of a memory cell to be programmed by biasing a control gate and grounding a body region of a substrate on which the memory cell is formed.

[0004] An oxide-nitride-oxide (ONO) stack is used as either a charge storing layer, as in silicon-oxide-nitride-oxide-silicon (SONOS) transistor, or as an isolation layer between the floating gate and control gate, as in a split gate flash memory.

[0005] FIG. 1 is a partial cross-sectional view of an intermediate structure for a semiconductor device 100, such as a memory device, having a SONOS gate stack or structure 102 including a conventional ONO stack 104 formed over a surface 106 of a silicon substrate 108 according to a conventional method. In addition, the device 100

typically further includes one or more diffusion regions 110, such as source and drain regions, aligned to the gate stack and separated by a channel region 112. Briefly, the SONOS structure 102 includes a poly-silicon (poly) gate layer 114 formed upon and in contact with the ONO stack 104. The poly gate layer 114 is separated or electrically isolated from the substrate 108 by the ONO stack 104. The ONO stack 104 generally includes a lower oxide layer 116, a nitride or oxynitride layer 118 which serves as a charge storing or memory layer for the device 100, and a top, high-temperature oxide (HTO) layer 120 overlying the nitride or oxynitride layer.

[0006] One problem with conventional SONOS structures 102 and methods of forming the same is the poor data retention of the nitride or oxynitride layer 118 that limits the device 100 lifetime and/or its use in several applications due to leakage current through the layer.

[0007] Another problem with conventional SONOS structures 102 and methods of forming the same is the stoichiometry of the oxynitride layer 118 is neither uniform nor optimized across the thickness of the layer. In particular, the oxynitride layer 118 is conventionally formed or deposited in a single step using a single process gas mixture and fixed or constant processing conditions in an attempt to provide a homogeneous layer having a high nitrogen and high oxygen concentration across the thickness of the relatively thick layer. However, due to top and bottom effects this results in nitrogen, oxygen and silicon concentrations, which can vary throughout the conventional oxynitride layer 118. The top effect is caused by the order in which process gases are shut off following deposition. In particular, the silicon containing process gas, such as silane, is typically shut off first resulting in a top portion of the oxynitride layer 118 that is high

in oxygen and/or nitride and low in silicon. Similarly, the bottom effect is caused by the order in which process gases are introduced to initiate deposition. In particular, the deposition of the oxynitride layer 118 typically follows an annealing step, resulting in a peak or relatively high concentration of ammonia (NH_3) at the beginning of the deposition process and producing in a bottom portion of the oxynitride layer that is low in oxygen and silicon and high in nitrogen. The bottom effect is also due to surface nucleation phenomena in which that oxygen and silicon that is available in the initial process gas mixture preferentially reacts with silicon at the surface of the substrate and does not contribute to the formation of the oxynitride layer. Consequently, the charge storage characteristics, and in particular programming and erase speed and data retention of a memory device 100 made with the ONO stack 104, are adversely effected.

[0008] Accordingly, there is a need for a memory device having an ONO stack with an oxynitride layer as a memory layer that exhibits improved programming and erase speed and data retention. There is a further need for a method or process of forming an ONO stack having an oxynitride layer that exhibits improved oxynitride stoichiometry.

SUMMARY

[0009] A semiconductor memory device including a multi-layer charge storing layer and methods of forming the same are provided. Generally, the device includes a channel formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide layer overlying the channel; and a multi-layer charge storing layer including an oxygen-rich, first oxynitride

layer on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean, second oxynitride layer on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense. In one embodiment, the device comprises a non-planar transistor including a gate having multiple surfaces abutting the channel, and the gate comprises the tunnel oxide layer and the multi-layer charge storing layer. Other embodiments are also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] These and various other features and advantages of the present structure and method will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

[0011] FIG. 1 (prior art) is a block diagram illustrating a cross-sectional side view of an intermediate structure for a memory device for which a method having an oxide-nitride-oxide (ONO) stack formed according to conventional method;

[0012] FIG. 2 is a block diagram illustrating a cross-sectional side view of a portion of a semiconductor device having a silicon-oxide-oxynitride-oxide-silicon structure including a multi-layer charge storing layer according to an embodiment of the present disclosure;

[0013] FIG. 3 is flow chart of a method for forming an oxide-oxynitride-oxide structure including a multi-layer charge storing layer according to an embodiment of the present disclosure;

[0014] FIG. 4 is a graph showing an improvement in data retention for a memory device using a memory layer formed according to the present disclosure as compared to a memory device using a conventional memory layer;

[0015] FIG. 5 is flow chart of a method for forming an oxide-oxynitride-oxide structure including a multi-layer charge storing layer according to another embodiment of the present disclosure;

[0016] FIG. 6 is an energy band diagram of a programmed conventional memory device having an ONO structure;

[0017] FIGs. 7A and 7B are energy band diagrams of a memory device including a multi-layer charge storing layer according to an embodiment of the present disclosure prior to and following programming;

[0018] FIG. 8A illustrates a non-planar multigate device including a split charge-trapping region;

[0019] FIG. 8B illustrates a cross-sectional view of the non-planar multigate device of FIG. 8A;

[0020] FIGs. 9A and 9B illustrate a non-planar multigate device including a split charge-trapping region and a horizontal nanowire channel;

[0021] FIGs. 10A and 10B illustrate a non-planar multigate device including a split charge-trapping region and a vertical nanowire channel;

[0022] FIG. 11A and 11B illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 10A; and

[0023] FIG. 12A and 12B illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 10A.

DETAILED DESCRIPTION

[0024] The present invention is directed generally to a device comprising a silicon-oxide-oxynitride-oxide-silicon gate structure including a multi-layer charge storing layer and methods for making the same. The gate structure and method are particularly useful for forming a memory layer in a memory device, such as a memory transistor.

[0025] In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be evident, however, to one skilled in the art that the present structure and method may be practiced without these specific details. In other instances, well-known structures, and techniques are not shown in detail or are shown in block diagram form in order to avoid unnecessarily obscuring an understanding of this description.

[0026] Reference in the description to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. The appearances of the phrase "in one embodiment" in various places in the specification do not necessarily all refer to the same embodiment. The term "to couple" as used herein may include both to directly connect and to indirectly connect through one or more intervening components.

[0027] Briefly, the method involves forming a multi-layer charge storing layer including multiple oxynitride layers, such as silicon oxynitride (Si_2N_2O) layers, having differing concentrations of Oxygen, Nitrogen and/or Silicon. The oxynitride layers are formed at higher temperatures than nitride or oxynitride layers in conventional ONO

structures, and each of the layers are formed using differing process gases mixtures and/or at differing flow rates. Generally, the oxynitride layers include at least a top oxynitride layer and a bottom oxynitride layer. In certain embodiments, the stoichiometric compositions of the layers is tailored or selected such that the lower or bottom oxynitride has a high oxygen and silicon content, and the top oxynitride layer has high silicon and a high nitrogen concentration with a low oxygen concentration to produce an oxygen-lean, silicon-rich nitride or oxynitride. The silicon-rich and oxygen-rich bottom oxynitride layer reduces stored charge loss without compromising device speed or an initial (beginning of life) difference between program and erase voltages. The silicon-rich, oxygen-lean top oxynitride layer increases a difference between programming and erase voltages of memory devices, thereby improving device speed, increasing data retention, and extending the operating life of the device. In some embodiments, the silicon-rich, oxygen-lean top oxynitride layer can further include a concentration of carbon selected to increase the number of traps therein.

[0028] Optionally, the ratio of thicknesses between the top oxynitride layer and the bottom oxynitride layer can be selected to facilitate forming of the oxynitride layers over a tunneling or first oxide layer of a silicon-oxide-oxynitride-oxide-silicon gate structure following the forming of the first oxide layer using a dry or wet oxidation.

[0029] A silicon-oxide-oxynitride-oxide-silicon structure and methods for fabricating the same according to various embodiments of the present disclosure will now be described in greater detail with reference to FIGs. 2 through 4.

[0030] FIG. 2 is a block diagram illustrating a cross-sectional side view of a portion of a semiconductor memory device 200 having a silicon-oxide-oxynitride-oxide-

silicon gate structure including a multi-layer charge storing layer according to one embodiment. Referring to FIG. 2, the memory device 200 includes a silicon-oxide-oxynitride-oxide-silicon gate structure or gate stack 202 including a multi-layer charge storing layer 204 formed over a surface 206 of silicon layer on a substrate or a silicon substrate 208. In addition, the device 200 further includes one or more diffusion regions 210, such as source and drain regions or structures, aligned to the gate stack 202 and separated by a channel region 212. Generally, the silicon-oxide-oxynitride-oxide-silicon gate structure includes a silicon containing gate layer, such as a poly-silicon or poly gate layer 214 formed upon and in contact with the multi-layer charge storing layer 204, and a portion of the silicon layer or substrate 208. The poly gate layer 214 is separated or electrically isolated from the substrate 208 by the multi-layer charge storing layer 204. The silicon-oxide-oxynitride-oxide-silicon structure includes a thin, lower oxide layer or tunneling oxide layer 216 that separates or electrically isolates the gate stack 202 from the channel region 212, a top or blocking oxide layer 218, and the multi-layer charge storing layer 204. As noted above and as shown in FIG. 2, the multi-layer charge storing layer 204 includes at least two oxynitride layers, including a top oxynitride layer 220A and a bottom oxynitride layer 220B.

[0031] The substrate 208 may include any known silicon-based semiconductor material including silicon, silicon-germanium, silicon-on-insulator, or silicon-on-sapphire substrate. Alternatively, the substrate 208 may include a silicon layer formed on a non-silicon-based semiconductor material, such as gallium-arsenide, germanium, gallium-nitride, or aluminum-phosphide. In certain embodiments, the substrate 208 is a doped or undoped silicon substrate.

[0032] The lower oxide layer or tunneling oxide layer 216 of the silicon-oxide-oxynitride-oxide-silicon structure generally includes a relatively thin layer of silicon dioxide (SiO_2) of from about 15 angstrom (Å) to about 22 Å, and in some embodiments about 18 Å. The tunneling oxide layer 216 can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using chemical vapor deposition (CVD). Generally, the tunnel oxide layer is formed or grown using a thermal oxidation in oxygen ambient. In one embodiment, the process involves a dry oxidation method in which the substrate 208 is placed in a in a deposition or processing chamber, heated to a temperature from about 700°C to about 850°C, and exposed to oxygen for a predetermined period of time selected based on a desired thickness of the finished tunneling oxide layer 216. In another embodiment, the tunnel oxide layer is grown in an ISSG (In-Situ Steam Generation) chamber with a radical oxidation using a reaction between oxygen (O_2) and hydrogen (H_2) on the substrate at temperatures of at least 1000°C. Exemplary process times are from about 10 to about 100 minutes. The oxidation can be performed at atmospheric or at low pressure.

[0033] As noted above, the multi-layer charge storing layer generally includes at least two oxynitride layers having differing compositions of silicon, oxygen and nitrogen, and can have an overall thickness of from about 70 Å to about 150 Å, and in certain embodiments about 100 Å. In one embodiment, the oxynitride layers are formed or deposited in a low pressure CVD process using a silicon source, such as silane (SiH4), chlorosilane (SiH_3Cl), dichlorosilane or DCS (SiH_2Cl_2), tetrachlorosilane ($SiCl_4$) or Bis-TertiaryButylAmino Silane (BTBAS), a nitrogen source, such as nitrogen (N2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas,

such as oxygen (O_2) or N_2O. Alternatively, gases in which hydrogen has been replaced by deuterium can be used, including, for example, the substitution of deuterated-ammonia (ND_3) for NH_3. The substitution of deuterium for hydrogen advantageously passivates Si dangling bonds at the silicon-oxide interface, thereby increasing an NBTI (Negative Bias Temperature Instability) lifetime of the devices.

[0034] For example, the lower or bottom oxynitride layer 220B can be deposited over the tunneling oxide layer 216 by placing the substrate 208 in a deposition chamber and introducing a process gas including N_2O, NH_3 and DCS, while maintaining the chamber at a pressure of from about 5 millitorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700°C to about 850°C and in certain embodiments at least about 760°C, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm). It has been found that an oxynitride layer produced or deposited under these condition yields a silicon-rich, oxygen-rich, bottom oxynitride layer 220B, that decrease the charge loss rate after programming and after erase, which is manifested in a small voltage shift in the retention mode.

[0035] The top oxynitride layer 220A can be deposited over the bottom oxynitride layer 220B in a CVD process using a process gas including N_2O, NH_3 and DCS, at a chamber pressure of from about 5 mT to about 500 mT, and at a substrate temperature of from about 700°C to about 850°C and in certain embodiments at least

about 760°C, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N2O and NH3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 20 sccm. It has been found that an oxynitride layer produced or deposited under these condition yields a silicon-rich, nitrogen-rich, and oxygen-lean top oxynitride layer 220A, which improves the speed and increases of the initial difference between program and erase voltage without compromising a charge loss rate of memory devices made using an embodiment of the silicon-oxide-oxynitride-oxide-silicon structure, thereby extending the operating life of the device.

[0036] In some embodiments, the silicon-rich, nitrogen-rich, and oxygen-lean top oxynitride layer 220A can be deposited over the bottom oxynitride layer 220B in a CVD process using a process gas including BTBAS and ammonia (NH_3) mixed at a ratio of from about 7:1 to about 1:7 to further include a concentration of carbon selected to increase the number of traps therein. The selected concentration of carbon in the second oxynitride layer can include a carbon concentration of from about 5% to about 15%.

[0037] In certain embodiments, the top oxynitride layer 220A is deposited sequentially in the same tool used to form the bottom oxynitride layer 220B, substantially without breaking vacuum on the deposition chamber. In certain embodiments, the top oxynitride layer 220A is deposited substantially without altering the temperature to which the substrate 208 was heated during deposition of the bottom oxynitride layer 220B. In one embodiment, the top oxynitride layer 220A is deposited sequentially and immediately following the deposition of the bottom oxynitride layer 220B by decreasing

the flow rate of the N_2O/NH_3 gas mixture relative to the DCS/NH_3 gas mixture to provide the desired ratio of the gas mixtures to yield the silicon-rich, nitrogen-rich, and oxygen-lean top oxynitride layer 220A.

[0038] In certain embodiments, another oxide or oxide layer (not shown in these figures) is formed after the formation of the gate stack 202 in a different area on the substrate 208 or in the device using a steam oxidation. In this embodiment, the top oxynitride layer 220A and top or blocking oxide layer 218 of the silicon-oxide-oxynitride-oxide-silicon structure are beneficially steam annealed during the steam oxidation process. In particular, steam annealing improves the quality of the top or blocking oxide layer 218 reducing the number of traps formed near a top surface of the blocking oxide layer and near a top surface of the underlying top oxynitride layer 220A, thereby reducing or substantially eliminating an electric field that could otherwise form across the blocking oxide layer, which could result in back streaming of charge carriers therethrough and adversely affecting data or charge retention in the charge storing layer.

[0039] A suitable thickness for the bottom oxynitride layer 220B has been found to be from about 10 Å to about 80 Å, and a ratio of thicknesses between the bottom layer and the top oxynitride layer has been found to be from about 1:6 to about 6:1, and in certain embodiments at least about 1:4.

[0040] The top or blocking oxide layer 218 of the silicon-oxide-oxynitride-oxide-silicon structure includes a relatively thick layer of SiO_2 of from about 30 Å to about 70 Å, and in certain embodiments about 45 Å. The top or blocking oxide layer 218 can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using CVD. In one embodiment, the top or blocking oxide layer 218

is a high-temperature-oxide (HTO) deposited using CVD process. Generally, the deposition process involves exposing the substrate 208 to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-containing gas, such as O_2 or N_2O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

[0041] In certain embodiments, the top or blocking oxide layer 218 is deposited sequentially in the same tool used to form the oxynitride layers 220A, 220B. In certain embodiments, the oxynitride layers 220A, 220B, and the top or blocking oxide layer 218 are formed or deposited in the same tool used to grow the tunneling oxide layer 216. Suitable tools include, for example, an ONO AVP, commercially available from AVIZA technology of Scotts Valley, California.

[0042] A method or forming or fabricating a silicon-oxide-oxynitride-oxide-silicon stack according to one embodiment will now be described with reference to the flowchart of FIG. 3.

[0043] Referring to FIG. 3, the method begins with forming a first oxide layer, such as a tunneling oxide layer 216, of the silicon-oxide-oxynitride-oxide-silicon gate stack 202 over a silicon containing layer on a surface of a substrate 208 (300). Next, the first or bottom oxynitride layer 220B of a multi-layer charge storing layer 204 including oxynitride is formed on a surface of the first oxide layer (302). As noted above, this first or bottom oxynitride layer 220B can be formed or deposited by a CVD process using a process gas including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second or top

oxynitride layer 220A of the multi-layer charge storing layer 204 is then formed on a surface of the first or bottom oxynitride layer 220B (304). The second or top oxynitride layer 220A has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the first or bottom oxynitride layer 220B. In particular, and as noted above, the second or top oxynitride layer 220A can be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top oxynitride layer. Finally, a top or blocking oxide layer 218 of the silicon-oxide-oxynitride-oxide-silicon structure is formed on a surface of the second layer of the multi-layer charge storing layer (306). As noted above, this top or blocking oxide layer 218 can be formed or deposited by any suitable means, but in some embodiments is deposited in a CVD process. In one embodiment the top or blocking oxide layer 218 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the top or blocking oxide layer 218 can be thermally grown, however it will be appreciated that in this embodiment the thickness of the top oxynitride 220A may be adjusted or increased as some of the top oxynitride will be effectively consumed or oxidized during the process of thermally growing the top or blocking oxide layer 218.

[0044] Optionally, the method may further include forming or depositing a silicon containing layer on a surface of the top or blocking oxide layer 218 to form a silicon-oxide-oxynitride-oxide-silicon stack or structure (308). The silicon containing layer can be, for example, a polysilicon layer deposited by a CVD process to form a control or poly gate layer 214 of the transistor or device 200.

[0045] A comparison of data retention for a memory device using a memory layer formed according to an embodiment of the present disclosure as compared to a memory device using a conventional memory layer will now be made with reference to FIG 4. In particular, FIG. 4 illustrates the change in threshold voltage of devices in an electronically erasable programmable read-only memory (EEPROM) during programming (VTP) during erase (VTE) over device life for an EEPROM made using a conventional ONO structure and a silicon-oxide-oxynitride-oxide-silicon structure having a multi-layer oxynitride layer. In gathering data for this figure both devices were pre-cycled for 100K cycles at an ambient temperature of 85°C.

[0046] Referring to FIG. 4, the graph or line 402 illustrates the change over time of a VTP for an EEPROM made using a conventional ONO structure having a single oxynitride layer without refreshing the memory after the initial writing – program or erase. Actual data points on line 402 are shown by unfilled circles, the remainder of the line showing an extrapolation of VTP to a specified end-of-life (EOL) for the EEPROM. Graph or line 404 illustrates the change over time of a VTE for the EEPROM made using a conventional ONO structure. Actual data points on line 404 are shown by filled circles, and the remainder of the line shows an extrapolation of VTE to EOL for the EEPROM. Generally, the specified difference between the VTE and VTP for an EEPROM at EOL is at least 0.5 V to be able to identify or sense the difference between the program and erase state. As seen from this figure an EEPROM made using a conventional ONO structure has a difference between VTE and VTP of about 0.35V at a specified EOL of 20 years. Thus, an EEPROM made using a conventional ONO structure and operated under the

conditions described above will fail to meet the specified operating life by at least about 17 years.

[0047] In contrast, the change in VTP and VTE over time for an EEPROM made using a silicon-oxide-oxynitride-oxide-silicon structure having a multi-layer oxynitride layer, illustrated by lines 406 and 408 respectively, shows a difference between VTE and VTP of at least about 1.96V at the specified EOL. Thus, an EEPROM made using a silicon-oxide-oxynitride-oxide-silicon structure according to an embodiment of the present disclosure will meet and exceed the specified operating life of 20 years. In particular, graph or line 406 illustrates the change over time of VTP for an EEPROM using a silicon-oxide-oxynitride-oxide-silicon structure according to an embodiment of the present disclosure. Actual data points on line 406 are shown by unfilled squares, the remainder of the line showing an extrapolation of VTP to the specified EOL. Graph or line 408 illustrates the change over time of VTE for the EEPROM, and actual data points on line 408 are shown by filled squares, the remainder of the line showing an extrapolation of VTE to EOL.

[0048] A method or forming or fabricating a semiconductor device according to another embodiment is now described with reference to the flowchart of FIG. 5.

[0049] Referring to FIG. 5, the method begins with forming a tunneling oxide layer 216 on a substrate (500). Next, an oxygen-rich, first or bottom oxynitride layer 220B of a multi-layer charge storing layer 204 is formed on a surface of the tunneling oxide layer 216 (502). As noted above, this oxygen-rich, first or bottom oxynitride layer 220B can be formed or deposited by a CVD process using a process gas comprising a dichlorosilane (SiH_2Cl_2)/ammonia (NH_3) mixture at a ratio in the range of about 5:1 to

15:1; and a nitrous oxide (N_2O)/NH_3 mixture at a ratio in the range of about 2:1 to 4:1 and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer which is substantially trap free. That is the stoichiometric composition of the first or bottom oxynitride layer 220B comprises a high concentration of oxygen selected to increase retention performance of the multi-layer charge storing layer by acting as a barrier between charge trapped in the second or top oxynitride layer 220A and the substrate 208. The selected concentration of oxygen in the first or bottom oxynitride layer 220B can include an oxygen concentration of from about 15% to about 40%, and, in certain embodiments about 35%.

[0050] An oxygen-lean, second or top oxynitride layer 220A is then formed on a surface of the first or bottom oxynitride layer 220B (504). The second or top oxynitride layer 220A has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the first layer. In particular, and as noted above, the second or top oxynitride layer 220A can be formed or deposited by a CVD process using a process gas using a process gas comprising a N_2O/NH_3 mixture at a ratio in the range of about 1:6 to 1:8 and a SiH_2Cl_2/NH_3 mixture at a ratio in the range of about 1.5:1 to 3:1 to provide a trap dense oxynitride layer having an oxygen concentration of about 5% or less. Thus, the second or top oxynitride layer 220A comprises a charge trap density at least 1000 times greater than the first or bottom oxynitride layer 220B.

[0051] Finally, a top or blocking oxide layer 218 is formed over the second or top oxynitride layer 220A of the multi-layer charge storing layer 204 (506). As noted above, this top or blocking oxide layer 218 can be formed or deposited by any suitable means. In one embodiment the second or blocking oxide layer 218 is formed a manner that results

in thinning of the second or top oxynitride layer 220A to a predetermined thickness through oxidization of a portion of the second oxynitride layer. Finally, as noted above with respect to FIG. 4, the increased retention performance of the multi-layer charge storing layer 204 increases an end-of-life (EOL) for the semiconductor device at a specified difference between program voltage (VTP) and erase voltage (VTE) to at least about 20 years.

[0052] In another aspect, the multi-layer charge storing layer of the present disclosure has bandgap energy engineered to generate an electrical field opposing that built-up due to charge storage in the charge storing layer in a programmed state, thereby increasing data retention, without impacting programming voltages and/or device speed. An energy band diagram of a programmed conventional device including a channel in silicon substrate 602, a tunneling oxide layer 604, a homogeneous nitride or oxynitride charge storing layer 606, oxide blocking layer 608 and a polysilicon control gate 610 is illustrated in FIG. 6. Referring to FIG. 6, it is noted that large number of trapped charges located near the center of the charge storing layer 606 results in a build-up of a large electric field away from the tunneling oxide layer 604 towards the trapped charges, and which can cause or result in loss of stored charges

[0053] In contrast, in a memory device including the multi-layer charge storing layer of the present disclosure engineering the bandgap energy multi-layer charge storing layer results in a build-up of an electrical field pointing inward (from the charge storing layer toward the tunnel oxide), which opposes the build-up of the electric field due to the stored charge increasing charge retention. An unprogrammed memory device including a multi-layer charge storing layer 706 is shown in FIG. 7A. The device includes a channel

in silicon substrate 702, a tunneling oxide layer 704, an oxygen-lean oxynitride layer 706A, an oxygen-rich bottom oxynitride layer 706B, an oxide blocking layer 708 and a polysilicon control gate 710. Referring to FIG. 7A, the trap sites in the oxygen-lean top oxynitride layer 706A, produces an electric field that will oppose the electric field produced by the trapped charges in the programmed device. The resultant bandgap diagram of a device including a multi-layer charge storing layer 706 in a programmed state is shown in FIG. 7A.

Implementations and Alternatives

[0054] In another aspect the present disclosure is directed to multigate or multigate-surface memory devices including charge-trapping regions overlying two or more sides of a channel formed on or above a surface of a substrate, and methods of fabricating the same. Multigate devices include both planar and non-planar devices. A planar multigate device (not shown) generally includes a double-gate planar device in which a number of first layers are deposited to form a first gate below a subsequently formed channel, and a number of second layers are deposited thereover to form a second gate. A non-planar multigate device generally includes a horizontal or vertical channel formed on or above a surface of a substrate and surrounded on three or more sides by a gate.

[0055] FIG. 8A illustrates one embodiment of a non-planar multigate memory device including a charge-trapping region. Referring to FIG. 8A, the memory device 800, commonly referred to as a finFET, includes a channel 802 formed from a thin film or layer of semiconducting material overlying a surface 804 on a substrate 806 connecting a

source 808 and a drain 810 of the memory device. The channel 802 is enclosed on three sides by a fin which forms a gate 812 of the device. The thickness of the gate 812 (measured in the direction from source to drain) determines the effective channel length of the device.

[0056] In accordance with the present disclosure, the non-planar multigate memory device 800 of FIG. 8A can include a split charge-trapping region. FIG. 8B is a cross-sectional view of a portion of the non-planar memory device of FIG. 8A including a portion of the substrate 806, channel 802 and the gate 812 illustrating a multi-layer charge storing layer 814. The gate 812 further includes a tunnel oxide layer 816 overlying a raised channel 802, a blocking dielectric 818 and a metal gate layer 820 overlying the blocking layer to form a control gate of the memory device 800. In some embodiments a doped polysilicon may be deposited instead of metal to provide a polysilicon gate layer. The channel 802 and gate 812 can be formed directly on substrate 806 or on an insulating or dielectric layer 822, such as a buried oxide layer, formed on or over the substrate.

[0057] Referring to FIG. 8B, the multi-layer charge storing layer 814 includes at least one lower or bottom charge-trapping layer 824 including nitride closer to the tunnel oxide layer 816, and an upper or top charge-trapping layer 826 overlying the bottom charge-trapping layer. Generally, the top charge-trapping layer 826 includes a silicon-rich, oxygen-lean nitride layer and includes a majority of a charge traps distributed in multiple charge-trapping layers, while the bottom charge-trapping layer 824 includes an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the top charge-trapping layer to reduce the number of charge traps therein. By oxygen-rich it is meant wherein a concentration of oxygen in the bottom charge-trapping layer 824 is from about

15 to about 40%, whereas a concentration of oxygen in top charge-trapping layer 826 is less than about 5%.

[0058] In one embodiment, the blocking dielectric 818 also includes an oxide, such as an HTO, to provide an ONNO structure. The channel 802 and the overlying ONNO structure can be formed directly on a silicon substrate 806 and overlaid with a doped polysilicon gate layer 820 to provide a SONNOS structure.

[0059] In some embodiments, such as that shown in FIG. 8B, the multi-layer charge storing layer 814 further includes at least one thin, intermediate or anti-tunneling layer 828 including a dielectric, such as an oxide, separating the top charge-trapping layer 826 from the bottom charge-trapping layer 824. The anti-tunneling layer 828 substantially reduces the probability of electron charge that accumulates at the boundaries of the upper nitride layer 826 during programming from tunneling into the bottom nitride layer 824, resulting in lower leakage current than for the structures illustrated in FIG. 1 and FIG. 6.

[0060] As with the embodiments described above, either or both of the bottom charge-trapping layer 824 and the top charge-trapping layer 826 can include silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The top charge-trapping layer 826 has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the bottom charge-trapping layer 824, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and

N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

[0061] In those embodiments including an intermediate or anti-tunneling layer 828 including oxide, the anti-tunneling layer can be formed by oxidation of the bottom oxynitride layer, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100°C using a single wafer tool, or 800-900°C using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0062] Finally, in those embodiments including a blocking dielectric 818 including oxide the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of the blocking dielectric 818 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric 818 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the top nitride thickness may be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer. A third option is to oxidize the top nitride layer to a chosen depth using radical oxidation.

[0063] A suitable thickness for the bottom charge-trapping layer 824 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 828. A suitable thickness for the top charge-trapping layer 826 may be at least 30Å. In certain embodiments, the top charge-trapping layer 826 may be formed up to 130Å thick, of

which 30-70Å may be consumed by radical oxidation to form the blocking dielectric 818. A ratio of thicknesses between the bottom charge-trapping layer 824 and top charge-trapping layer 826 is approximately 1:1 in some embodiments, although other ratios are also possible.

[0064] In other embodiments, either or both of the top charge-trapping layer 826 and the blocking dielectric 818 may include a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0065] In another embodiment, shown in FIGs. 9A and 9B, the memory device can include a nanowire channel formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device. By nanowire channel it is meant a conducting channel formed in a thin strip of crystalline silicon material, having a maximum cross-sectional dimension of about 10 nanometers (nm) or less, and more preferably less than about 6 nm. Optionally, the channel can be formed to have <100> surface crystalline orientation relative to a long axis of the channel.

[0066] Referring to FIG. 9A, the memory device 900 includes a horizontal nanowire channel 902 formed from a thin film or layer of semiconducting material on or overlying a surface on a substrate 906, and connecting a source 908 and a drain 910 of the memory device. In the embodiment shown, the device has a gate-all-around (GAA) structure in which the nanowire channel 902 is enclosed on all sides by a gate 912 of the device. The thickness of the gate 912 (measured in the direction from source to drain) determines the effective channel length of the device.

[0067] In accordance with the present disclosure, the non-planar multigate memory device 900 of FIG. 9A can include a split charge-trapping region. FIG. 9B is a cross-sectional view of a portion of the non-planar memory device of FIG. 9A including a portion of the substrate 906, nanowire channel 902 and the gate 912 illustrating a split charge-trapping region. Referring to FIG. 9B, the gate 912 includes a tunnel oxide layer 914 overlying the nanowire channel 902, a split charge-trapping region, a blocking dielectric 916 and a gate layer 918 overlying the blocking layer to form a control gate of the memory device 900. The gate layer 918 can include a metal or a doped polysilicon. The multi-layer charge storing layer includes at least one inner charge-trapping layer 920 including nitride closer to the tunnel oxide layer 914, and an outer charge-trapping layer 922 overlying the inner charge-trapping layer. Generally, the outer charge-trapping layer 922 includes a silicon-rich, oxygen-lean nitride layer and includes a majority of a charge traps distributed in multiple charge-trapping layers, while the inner charge-trapping layer 920 includes an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the outer charge-trapping layer to reduce the number of charge traps therein.

[0068] In some embodiments, such as that shown, the multi-layer charge storing layer further includes at least one thin, intermediate or anti-tunneling layer 924 including a dielectric, such as an oxide, separating outer charge-trapping layer 922 from the inner charge-trapping layer 920. The anti-tunneling layer 924 substantially reduces the probability of electron charge that accumulates at the boundaries of outer charge-trapping layer 922 during programming from tunneling into the inner charge-trapping layer 920, resulting in lower leakage current.

[0069] As with the embodiment described above, either or both of the inner charge-trapping layer 920 and the outer charge-trapping layer 922 can include silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The outer charge-trapping layer 922 has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the inner charge-trapping layer 920, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

[0070] In those embodiments including an intermediate or anti-tunneling layer 924 including oxide, the anti-tunneling layer can be formed by oxidation of the inner charge-trapping layer 920, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100°C using a single wafer tool, or 800-900°C using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0071] Finally, in those embodiments in which the blocking dielectric 916 includes oxide, the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of blocking dielectric 916 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric 916 or blocking oxide layer

may be thermally grown, however it will be appreciated that in this embodiment the thickness of the outer charge-trapping layer 922 may need to be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer.

[0072] A suitable thickness for the inner charge-trapping layer 920 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 924. A suitable thickness for the outer charge-trapping layer 922 may be at least 30Å. In certain embodiments, the outer charge-trapping layer 922 may be formed up to 120Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric 916. A ratio of thicknesses between the inner charge-trapping layer 920 and the outer charge-trapping layer 922 is approximately 1:1 in some embodiments, although other ratios are also possible.

[0073] In other embodiments, either or both of the outer charge-trapping layer 922 and the blocking dielectric 916 may include a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0074] In another embodiment, the memory device is or includes a non-planar device including a vertical nanowire channel formed in or from a semiconducting material projecting above or from a number of conducting, semiconducting layers on a substrate. In one version of this embodiment, shown in cut-away in FIG. 10A, the memory device 1000 includes a vertical nanowire channel 1002 formed in a cylinder of semiconducting material connecting a source 1004 and drain 1006 of the device. The

channel 1002 is surrounded by a tunnel oxide layer 1008, a multi-layer charge storing layer1110, a blocking layer 1012 and a gate layer 1014 overlying the blocking layer to form a control gate of the memory device 1000. The channel 1002 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or can include an annular layer formed over a cylinder of dielectric filler material. As with the horizontal nanowires described above, the channel 1002 can include polysilicon or recrystallized polysilicon to form a monocrystalline channel. Optionally, where the channel 1002 includes a crystalline silicon, the channel can be formed to have <100> surface crystalline orientation relative to a long axis of the channel.

[0075] In some embodiments, such as that shown in FIG. 10B, the multi-layer charge storing layer 1010 can be a multi-layer charge storing layer including at least a first or inner charge trapping layer 1016 closest to the tunnel oxide layer 1008, and a second or outer charge trapping layer 1018. Optionally, the first and second charge trapping layers can be separated by an intermediate oxide or anti-tunneling layer 1020.

[0076] As with the embodiments described above, either or both of the first charge trapping layer 1016 and the second charge trapping layer 1018 can include silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer.

[0077] Finally, either or both of the second charge trapping layer 1018 and the blocking layer 1012 may include a high K dielectric, such as HfSiON, HfSiO, HfO, ZrSiON, ZrSiO, ZrO, or Y_2O_3.

[0078] A suitable thickness for the first charge trapping layer 1016 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 1020. A suitable thickness for the second charge trapping layer 1018 may be at least 30Å, and a suitable thickness for the blocking dielectric 1012 may be from about 30-70Å.

[0079] The memory device 1000 of FIG. 10A can be made using either a gate first or a gate last scheme. FIG. 11A-F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 10A. FIG. 12A-F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 10A.

[0080] Referring to FIG. 11A, in a gate first scheme a first or lower dielectric layer 1102, such as a blocking oxide, is formed over a first, doped diffusion region 1104, such as a source or a drain, in a substrate 1106. A gate layer 1108 is deposited over the first dielectric layer 1102 to form a control gate of the device, and a second or upper dielectric layer 1110 formed thereover. As with embodiments described above, the first and second dielectric layers 1102, 1110, can be deposited by CVD, radical oxidation or be formed by oxidation of a portion of the underlying layer or substrate. The gate layer 1108 can include a metal deposited or a doped polysilicon deposited by CVD. Generally the thickness of the gate layer 1108 is from about 40- 50Å, and the first and second dielectric layers 1102, 1110, from about 20 - 80Å.

[0081] Referring to FIG. 11B, a first opening 1112 is etched through the overlying gate layer 1108, and the first and second dielectric layers 1102, 1110, to the diffusion region 1104 in the substrate 1106. Next, layers including a tunnel oxide layer 1114, multi-layer charge storing layer 1116, and blocking dielectric 1118 are sequentially

deposited in the opening and the surface of the upper dielectric layer 1110 planarize to yield the intermediate structure shown in FIG. 11C.

[0082] Although not shown, it will be understood that as in the embodiments described above the multi-layer charge storing layer 1116 can include a multi-layer charge storing layer including at least one lower or bottom charge-trapping layer closer to the tunnel oxide layer 1114, and an upper or top charge-trapping layer overlying the bottom charge-trapping layer. Generally, the top charge-trapping layer includes a silicon-rich, oxygen-lean nitride layer and includes a majority of a charge traps distributed in multiple charge-trapping layers, while the bottom charge-trapping layer includes an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the top charge-trapping layer to reduce the number of charge traps therein. In some embodiments, the multi-layer charge storing layer 1116 further includes at least one thin, intermediate or anti-tunneling layer including a dielectric, such as an oxide, separating the top charge-trapping layer from the bottom charge-trapping layer.

[0083] Next, a second or channel opening 1120 is anisotropically etched through tunnel oxide layer 1114, multi-layer charge storing layer 1116, and blocking dielectric 1118, FIG. 11D. Referring to FIG. 11E, a semiconducting material 1122 is deposited in the channel opening to form a vertical channel 1124 therein. The vertical channel 1124 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or, as shown in FIG. 11E, can include a separate, layer semiconducting material 1122 surrounding a cylinder of dielectric filler material 1126.

[0084] Referring to FIG. 11F, the surface of the upper dielectric layer 1110 is planarized and a layer of semiconducting material 1128 including a second, doped

diffusion region 1130, such as a source or a drain, formed therein deposited over the upper dielectric layer to form the device shown.

[0085] Referring to FIG. 12, in a gate last scheme a dielectric layer 1202, such as an oxide, is formed over a sacrificial layer 1204 on a surface on a substrate 1206, an opening etched through the dielectric and sacrificial layers and a vertical channel 1208 formed therein. As with embodiments described above, the vertical channel 1208 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material 1210, such as polycrystalline or monocrystalline silicon, or can include a separate, layer semiconducting material surrounding a cylinder of dielectric filler material (not shown). The dielectric layer 1202 can include any suitable dielectric material, such as a silicon oxide, capable of electrically isolating the subsequently formed gate layer of the memory device 1000 from an overlying electrically active layer or another memory device. The sacrificial layer 1204 can include any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 1202, substrate 1206 and vertical channel 1208.

[0086] Referring to FIG. 12B, a second opening 1212 is etched through the etched through the dielectric and sacrificial layers 1202, 1204, to the substrate 1206, and the sacrificial layer 1204 etched or removed. The sacrificial layer 1204 can include any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 1202, substrate 1206 and vertical channel 1208. In one embodiment the sacrificial layer 1204 includes silicon dioxide that can be removed by buffered oxide etch (BOE etch).

[0087] Referring to FIGs. 12C and 12D, layers of a tunnel oxide layer 1214, multi-layer charge storing layer 1216, and blocking dielectric 1218 are sequentially deposited in the opening and the surface of the dielectric layer 1202 planarize to yield the intermediate structure shown in FIGs. 12C and 12D. In some embodiments, such as that shown in FIG. 12D, the multi-layer charge storing layer 1216 can be a multi-layer charge storing layer including at least a first or inner charge trapping layer 1216a closest to the tunnel oxide layer 1214, and a second or outer charge trapping layer 1216b. Optionally, the first and second charge trapping layers can be separated by an intermediate oxide or anti-tunneling layer 1220.

[0088] Next, a gate layer 1222 is deposited into the second opening 1212 and the surface of the upper dielectric layer 1202 planarized to yield the intermediate structure illustrated in FIG. 12E. As with embodiments described above, the gate layer 1222 can include a metal deposited or a doped polysilicon. Finally, an opening 1224 is etched through the gate layer 1222 to form control gate of separate memory devices 1226.

[0089] Embodiments of the charge retention devices described herein may be employed in logic circuits to function as machine-memory. Those having skill in the art will appreciate that there are various logic implementations that may embody the described structures, and that the preferred vehicle will vary with the context in which the processes are deployed. For example, if an implementer determines that speed and accuracy are paramount, the implementer may opt for a hardware and/or firmware vehicle; alternatively, if flexibility is paramount, the implementer may opt for a solely software implementation; or, yet again alternatively, the implementer may opt for some combination of hardware, software, and/or firmware. Hence, there are many vehicles that

may employ the devices described herein, none of which is inherently superior to the other in that any vehicle to be utilized is a choice dependent upon the context in which the vehicle will be deployed and the specific concerns (e.g., speed, flexibility, or predictability) of the implementer, any of which may vary. Those skilled in the art will recognize that optical aspects of implementations may involve optically-oriented hardware, software, and or firmware.

[0090] Although shown and described above as having only two oxynitride layer, i.e., a top and a bottom layer, the present disclosure is not so limited, and the multi-layer charge storing layer can include any number, n, of oxynitride layers, any or all of which may have differing stoichiometric compositions of oxygen, nitrogen and/or silicon. In particular, multi-layer charge storing layers having up to five oxynitride layers each with differing stoichiometric compositions have been produced and tested. However, as will be appreciated by those skilled in the art it is generally desirable to utilize as few layers as possible to accomplish a desired result, reducing the process steps necessary to produce the device, and thereby providing a much simpler and more robust manufacturing process. Moreover, utilizing as few layers as possible also results in higher yields as it is simpler to control the stoichiometric composition and dimensions of the fewer layers.

[0091] It will further be appreciated that although shown and described as part of a silicon-oxide-oxynitride-oxide-silicon stack in a memory device, the structure and method of the present disclosure is not so limited, and the silicon-oxide-oxynitride-oxide-silicon structure can be used in or with any semiconductor technology or in any device requiring a charge storing or dielectric layer or stack including, for example, in a split

gate flash memory, a TaNOS stack, in a 1T (transistor) SONOS-type cell, a 2T SONOS-type cell, a 3T SONOS-type cell, a localized 2-bit cell, a multilevel programming or cell, and/or a 9T or 12T non-volatile semiconductor memory (NVSM) cells without departing from the scope of the disclosure.

[0092] The foregoing detailed description has set forth various embodiments of the devices and/or processes via the use of block diagrams, flowcharts, and/or examples. Insofar as such block diagrams, flowcharts, and/or examples contain one or more functions and/or operations, it will be understood as notorious by those within the art that each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof

[0093] Embodiments of the structures described herein may be employed in Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), central processing units (CPUs), digital signal processors (DSPs), or other integrated formats. However, those skilled in the art will recognize that some aspects of the embodiments disclosed herein, in whole or in part, can be equivalently implemented in dedicated memory circuits, for the purpose of storing digital information for data and/or programs running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more processors (e.g., as one or more programs running on one or more microprocessors), as firmware, or as virtually any combination thereof

[0094] In a general sense, those skilled in the art will recognize that the various structures described herein may be embodied, individually and/or collectively, by a wide

range of electrical circuitry. As used herein "electrical circuitry" includes, but is not limited to, electrical circuitry having at least one discrete electrical circuit, electrical circuitry having at least one integrated circuit, electrical circuitry having at least one application specific integrated circuit, electrical circuitry forming a general purpose computing device configured by a computer program (e.g., a general purpose computer configured by a computer program which at least partially carries out processes and/or devices described herein, or a microprocessor configured by a computer program which at least partially carries out processes and/or devices described herein), electrical circuitry forming a memory device (e.g., forms of random access memory), and/or electrical circuitry forming a communications device (e.g., a modem, communications switch, or optical-electrical equipment).

[0095] Those skilled in the art will recognize that it is common within the art to describe devices and/or processes in the fashion set forth herein, and thereafter use standard engineering practices to integrate such described devices and/or processes into larger systems. That is, at least a portion of the devices and/or processes described herein can be integrated into a network processing system without an undue amount of experimentation.

IN THE CLAIMS

WHAT IS CLAIMED IS:

1. A memory device comprising:

a channel formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device;

a tunnel oxide layer overlying the channel; and

a multi-layer charge storing layer including an oxygen-rich, first oxynitride layer on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean, second oxynitride layer on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense.

2. The memory device of claim 1, wherein the channel comprises polysilicon.

3. The memory device of claim 1, wherein the channel comprises recrystallized polysilicon.

4. The memory device of claim 1, wherein the channel comprises a silicon nanowire.

5. The memory device of claim 1, wherein the memory device comprises a non-planar transistor including a gate having multiple surfaces abutting the channel, and

wherein the gate comprises the tunnel oxide layer and the multi-layer charge storing layer.

6. The memory device of claim 5, wherein the gate further comprises a blocking dielectric overlying the multi-layer charge storing layer, and a metal gate layer overlying the blocking dielectric layer

7. The memory device of claim 6, wherein the blocking dielectric comprises a high K dielectric.

8. The memory device of claim 1, wherein the second oxynitride layer further comprises a concentration of carbon selected to increase a number of traps therein.

9. A memory device comprising:

an electrically conducting channel formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; and

a gate having multiple surfaces abutting the channel, the gate comprising:

a tunnel oxide layer overlying the channel; and

a multi-layer charge storing layer including a first oxynitride layer closer to the tunnel oxide layer, and a second oxynitride layer, wherein the first

oxynitride layer is separated from the second oxynitride layer by an anti-tunneling layer comprising an oxide.

10. The memory device of claim 9, wherein the channel comprises a silicon nanowire.

11. The memory device of claim 9, wherein the device comprises a finFET, and wherein the gate further comprises a blocking dielectric overlying the multi-layer charge storing layer, and a metal gate layer overlying the blocking dielectric layer.

12. The memory device of claim 11, wherein the blocking dielectric comprises a high K dielectric.

13. The memory device of claim 9, wherein the anti-tunneling layer comprises a portion of the first oxynitride layer that has been oxidized by radical oxidation.

14. The memory device of claim 9, wherein the first oxynitride layer is a substantially trap free, oxygen-rich, oxynitride layer, and the second oxynitride layer is a trap dense, oxygen-lean, oxynitride layer further comprising a concentration of carbon selected to increase a number of traps therein.

15. A memory device comprising:

a vertical channel formed from a thin projection of semiconducting material extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region;

a tunnel oxide layer abutting the vertical channel; and

a multi-layer charge storing layer abutting the tunnel oxide layer, the multi-layer charge storing layer including a first oxynitride layer comprising an oxygen-rich nitride closer to the tunnel oxide layer, and a second oxynitride layer comprising a silicon-rich, oxygen-lean nitride overlying the first oxynitride layer,

wherein the second charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region.

16. The memory device of claim 15, wherein the channel comprises a vertical silicon nanowire.

17. The memory device of claim 16, wherein the multi-layer charge storing layer further comprises an oxide anti-tunneling layer separating the first oxynitride layer from the second oxynitride layer.

18. The memory device of claim 16, further comprising a high K blocking dielectric overlying the multi-layer charge storing layer.

19. The memory device of claim 18, wherein the multi-layer charge storing layer further comprises an oxide anti-tunneling layer separating the first oxynitride layer from the second oxynitride layer.

20. The structure of claim 15, wherein the second oxynitride layer further comprises a concentration of carbon selected to increase a number of traps therein.

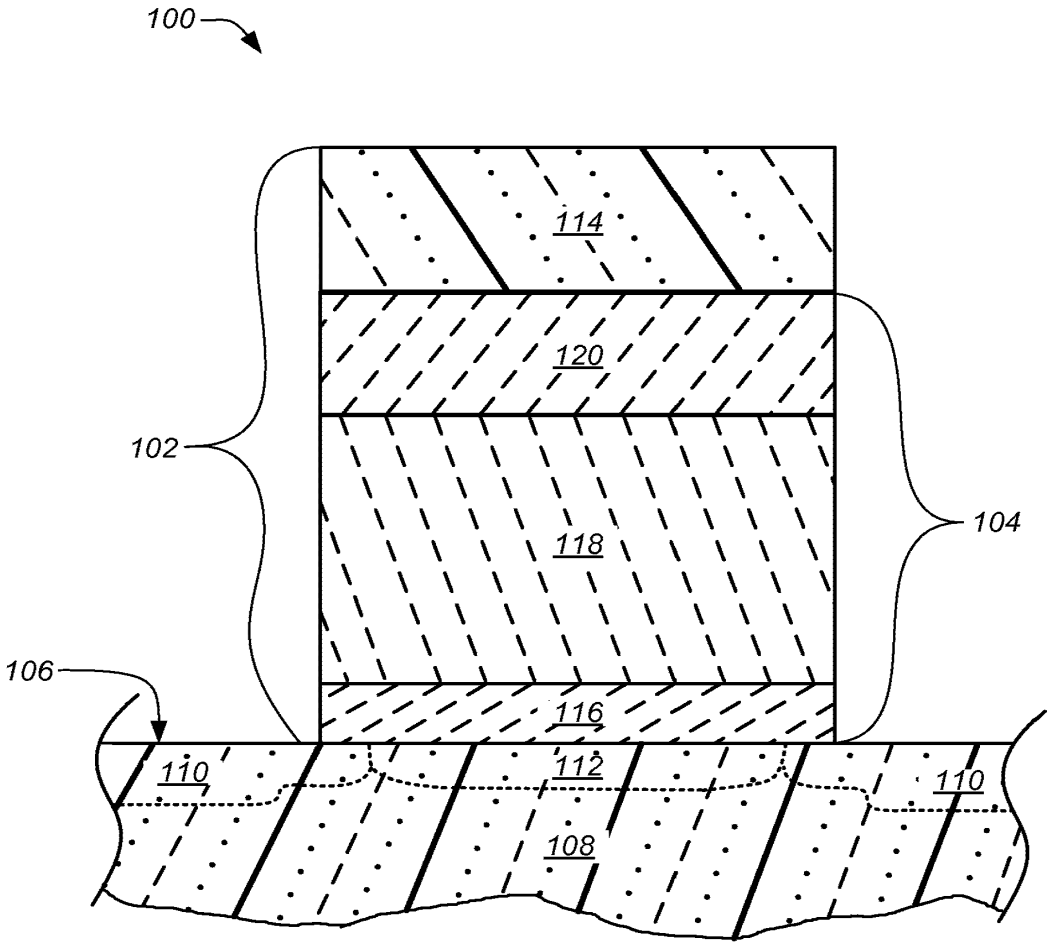


FIG. 1 (Prior Art)

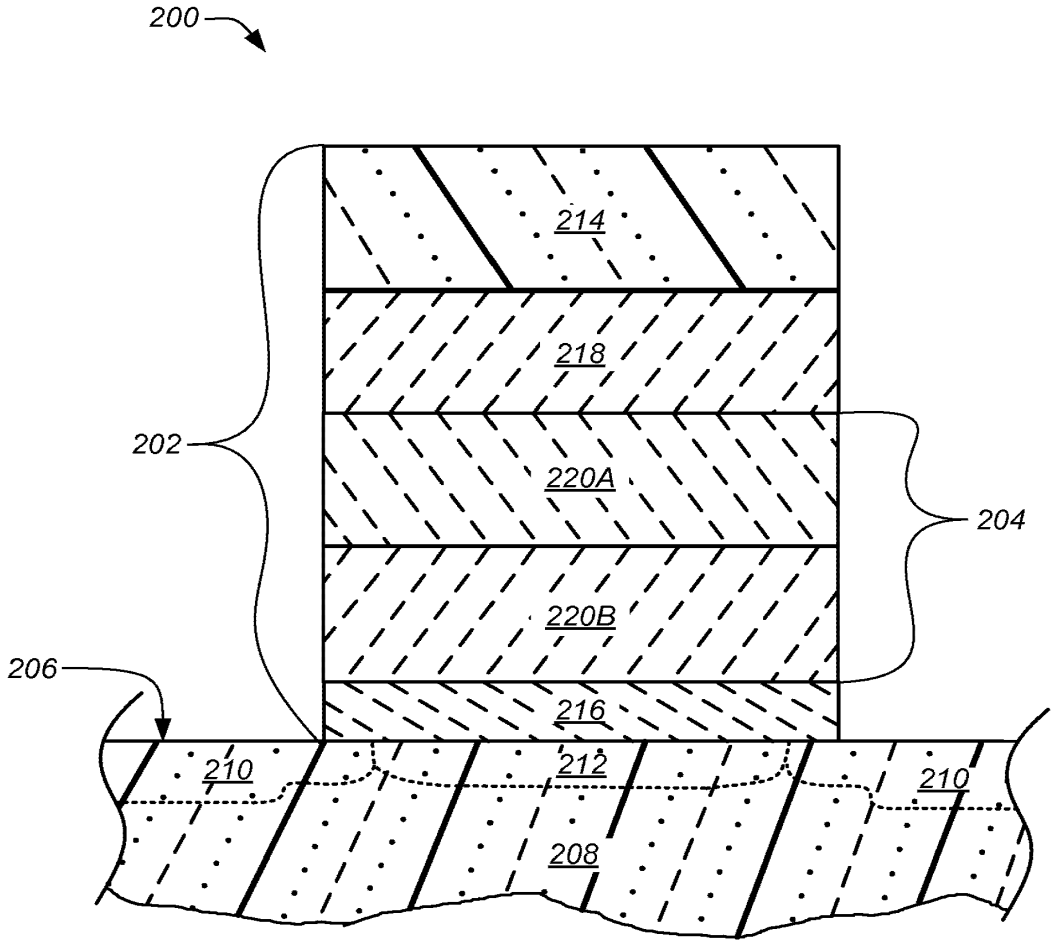


FIG. 2

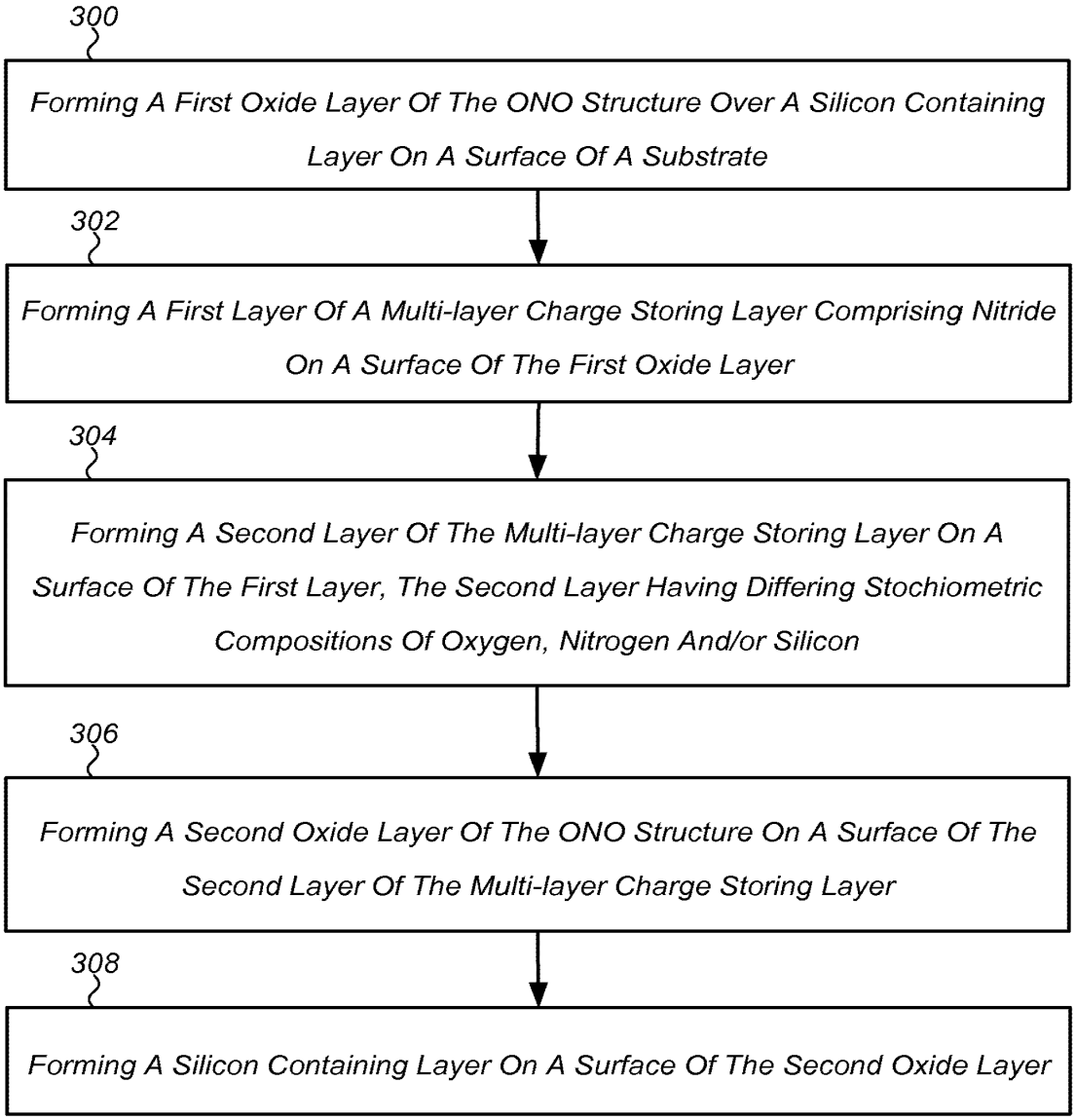

300
Forming A First Oxide Layer Of The ONO Structure Over A Silicon Containing Layer On A Surface Of A Substrate
302
Forming A First Layer Of A Multi-layer Charge Storing Layer Comprising Nitride On A Surface Of The First Oxide Layer
304
Forming A Second Layer Of The Multi-layer Charge Storing Layer On A Surface Of The First Layer, The Second Layer Having Differing Stochiometric Compositions Of Oxygen, Nitrogen And/or Silicon
306
Forming A Second Oxide Layer Of The ONO Structure On A Surface Of The Second Layer Of The Multi-layer Charge Storing Layer
308
Forming A Silicon Containing Layer On A Surface Of The Second Oxide Layer

FIG. 3

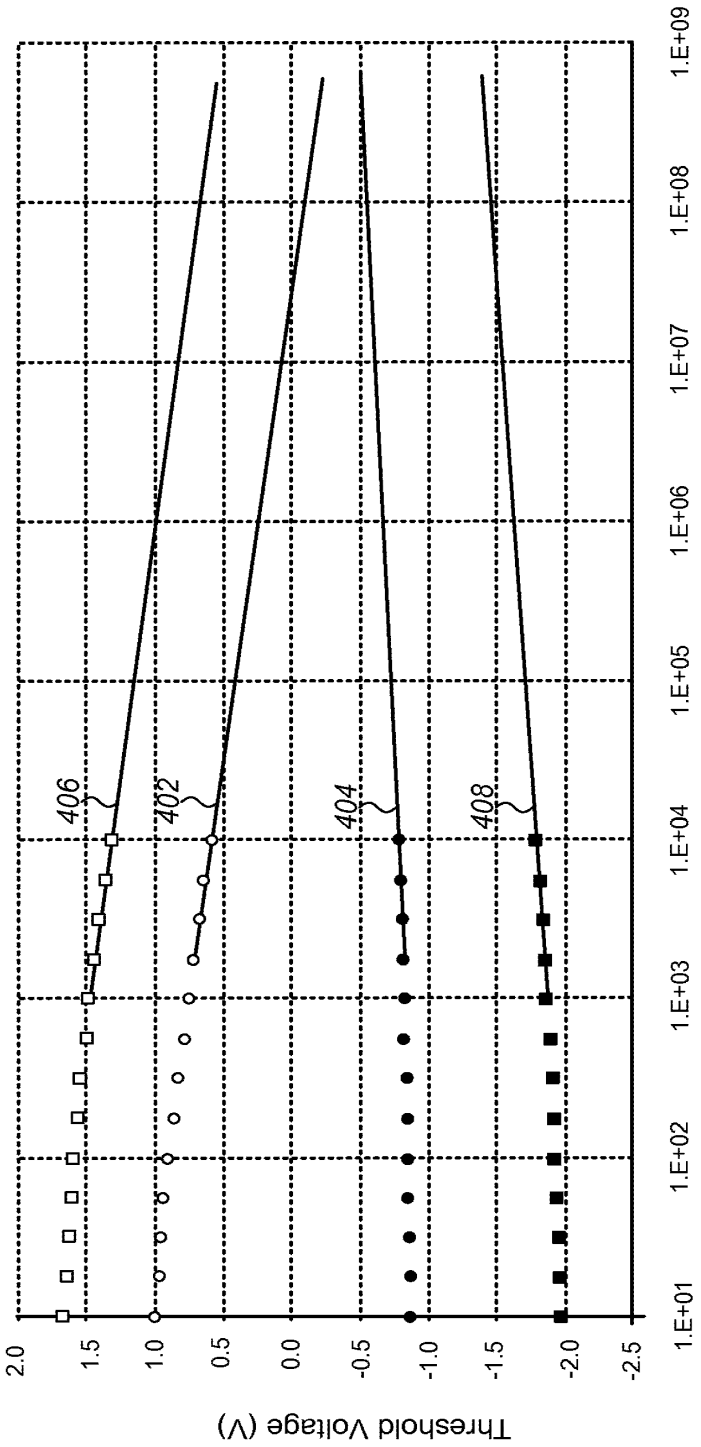

Threshold Voltage (V)
2.0
1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
1.E+01
1.E+02
1.E+03
1.E+04
1.E+05
1.E+06
1.E+07
1.E+08
1.E+09
Retention Time (Sec)
406
402
404
408

FIG. 4

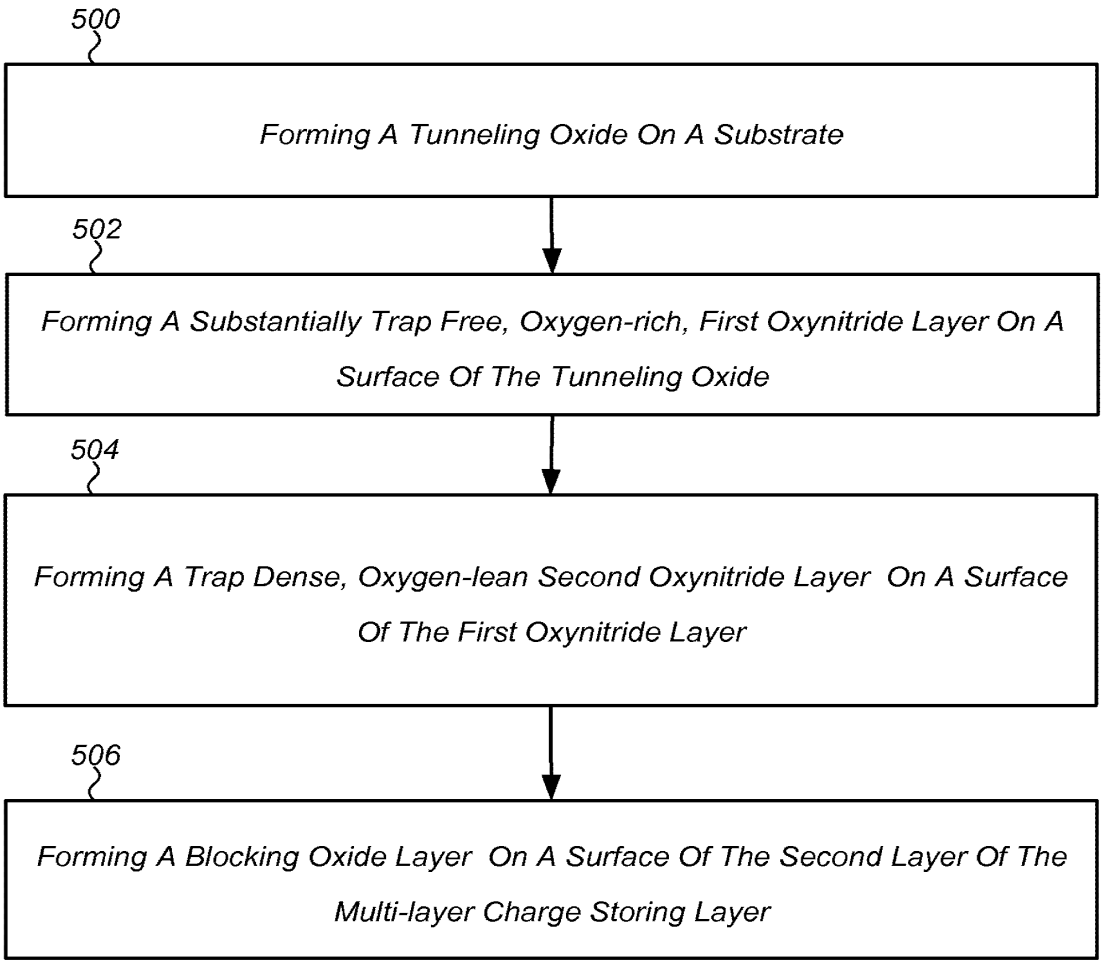

500
Forming A Tunneling Oxide On A Substrate
502
Forming A Substantially Trap Free, Oxygen-rich, First Oxynitride Layer On A Surface Of The Tunneling Oxide
504
Forming A Trap Dense, Oxygen-lean Second Oxynitride Layer On A Surface Of The First Oxynitride Layer
506
Forming A Blocking Oxide Layer On A Surface Of The Second Layer Of The Multi-layer Charge Storing Layer

FIG. 5

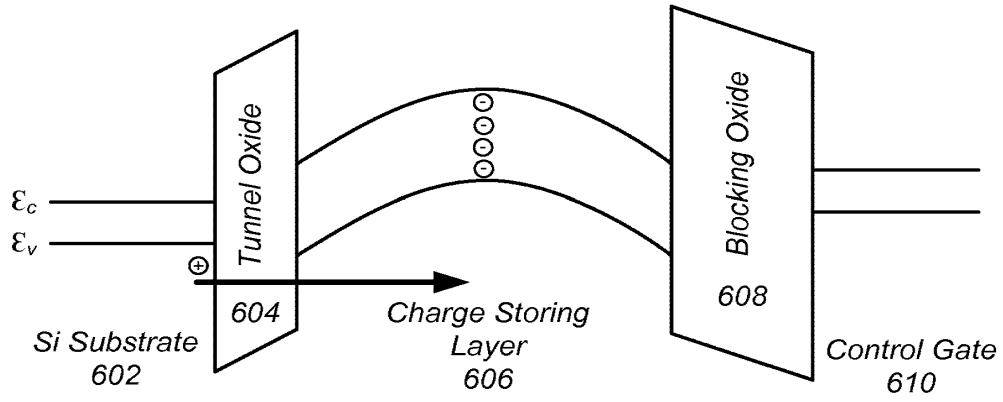


FIG. 6

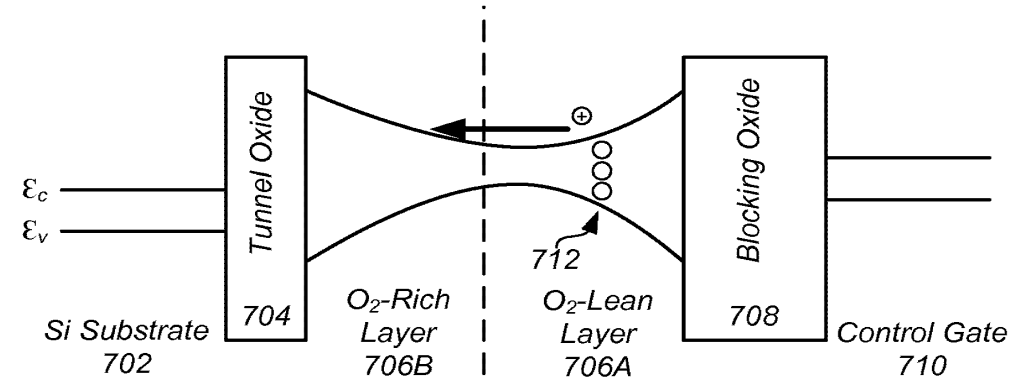


FIG. 7A

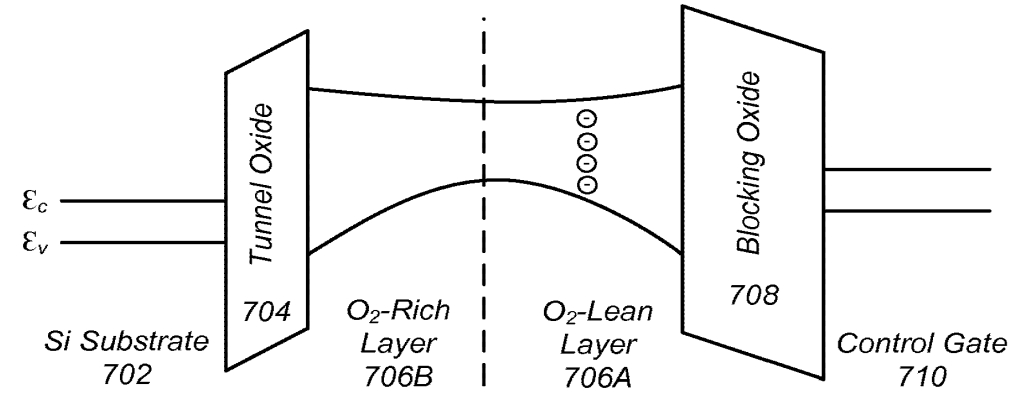


FIG. 7B

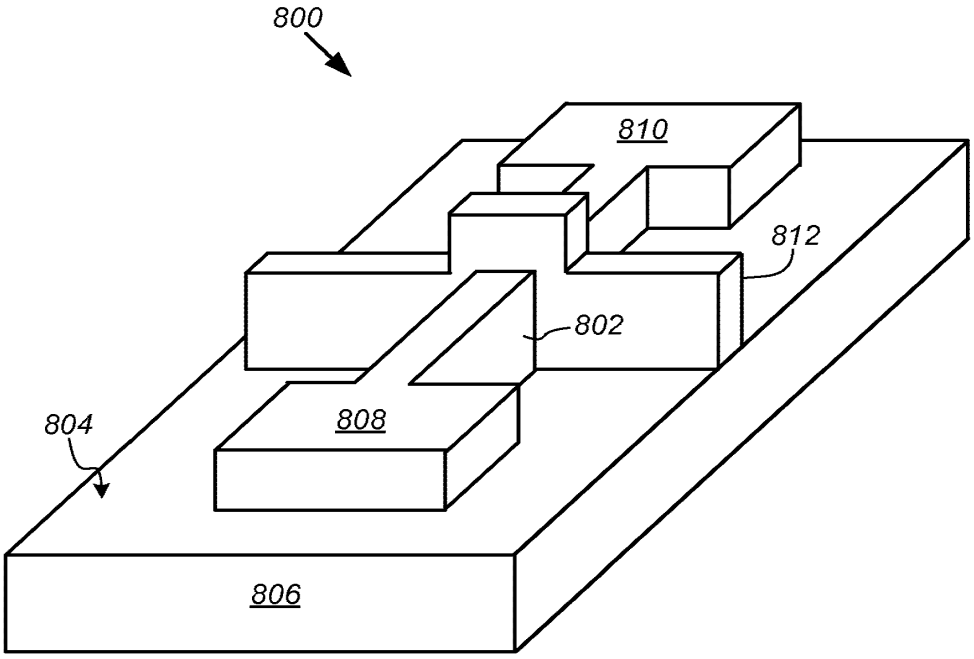


FIG. 8A

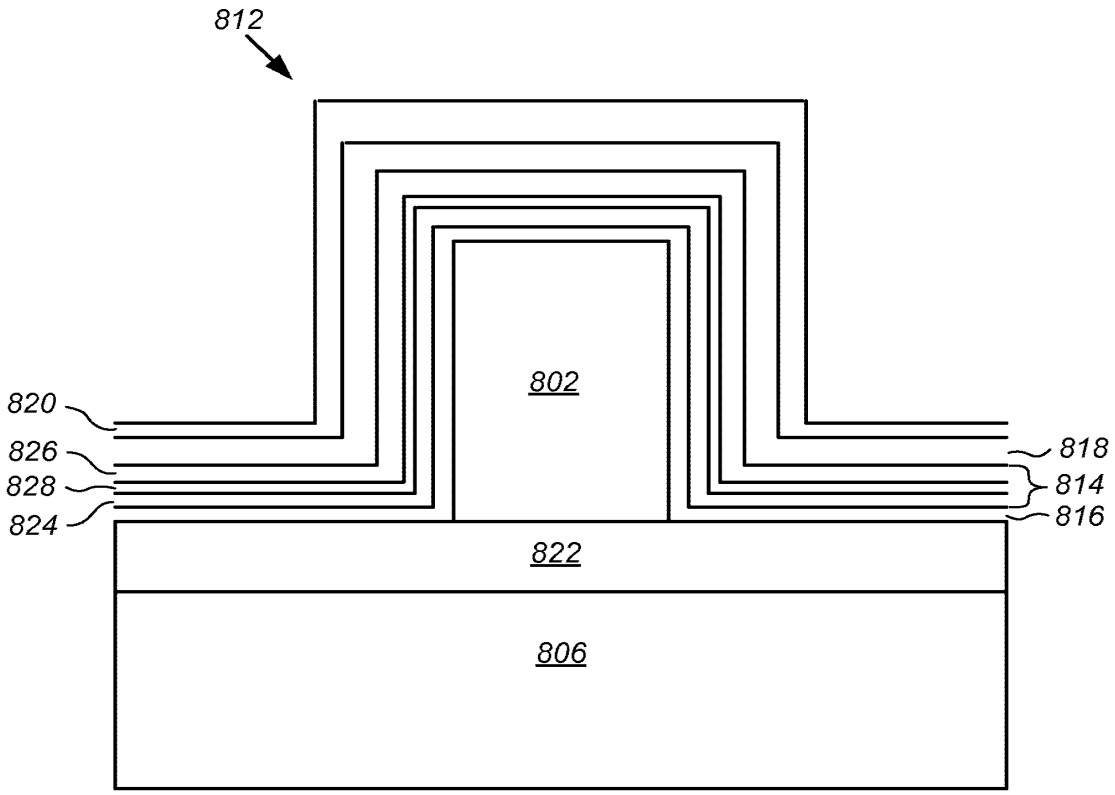


FIG. 8B

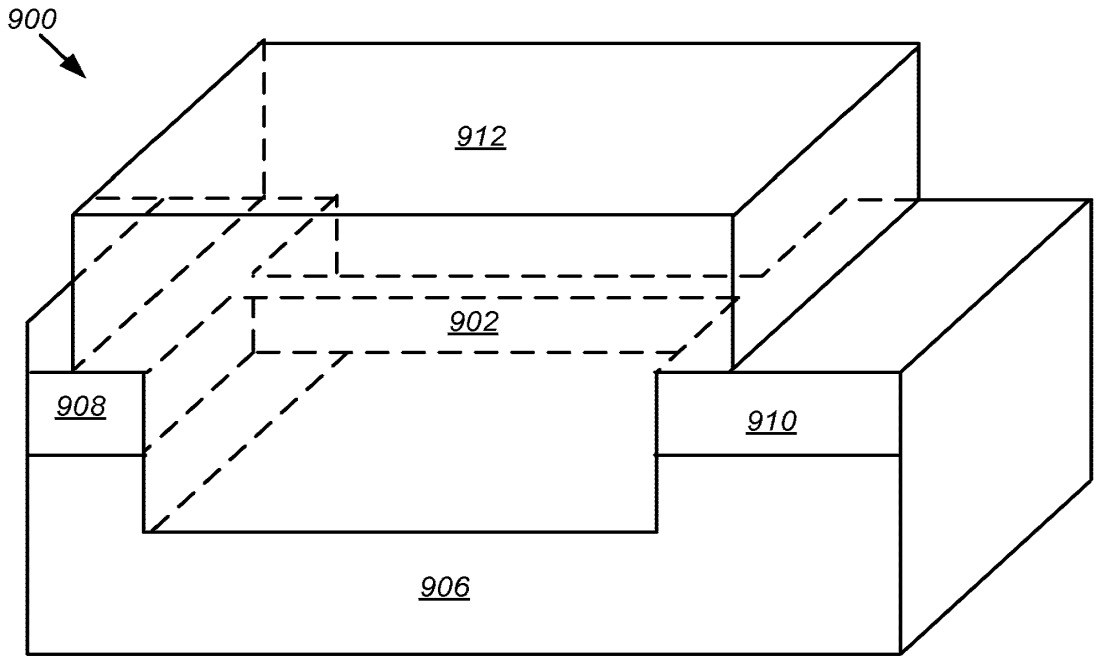


FIG. 9A

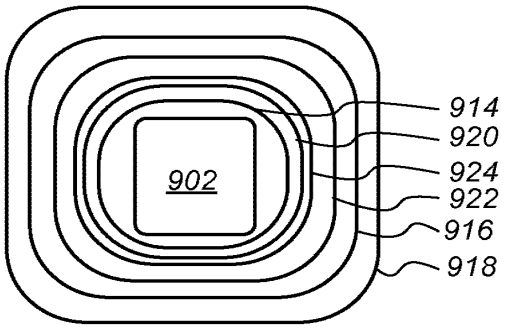


FIG. 9B

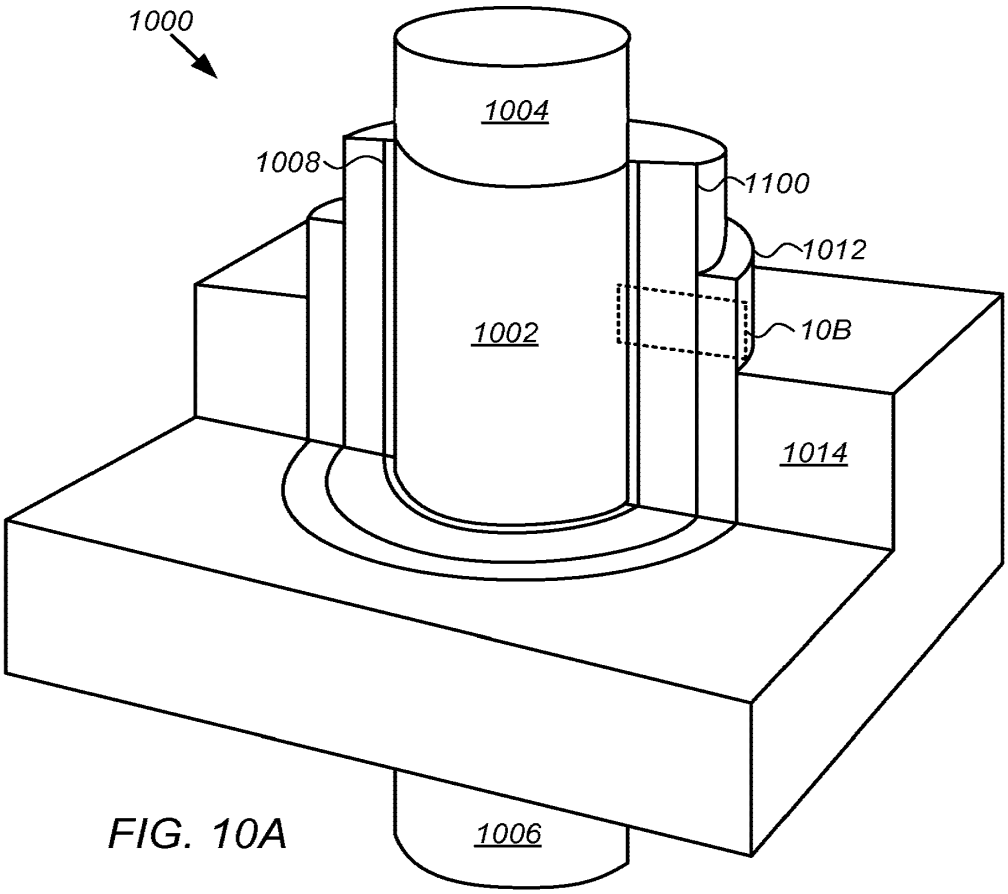


FIG. 10A

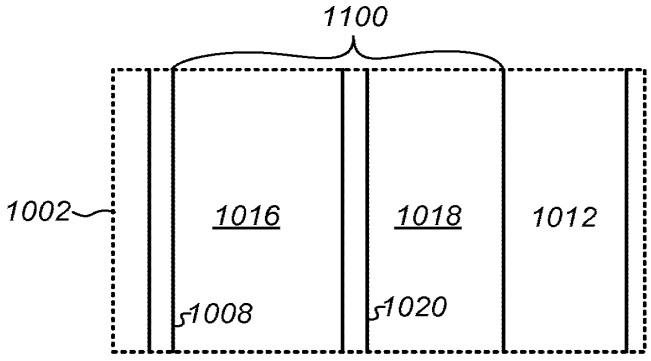


FIG. 10B

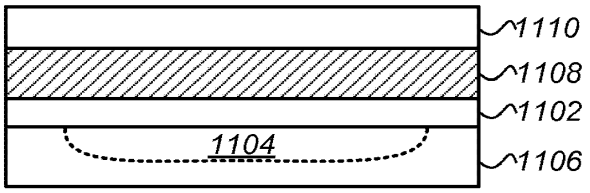


FIG. 11A

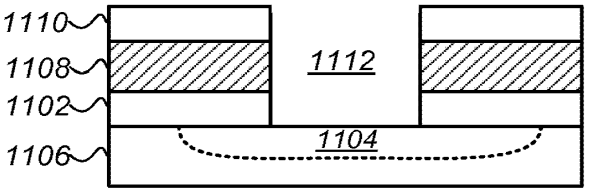


FIG. 11B

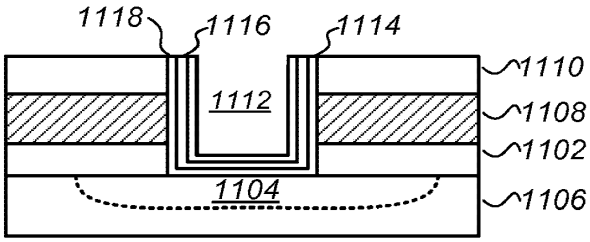


FIG. 11C

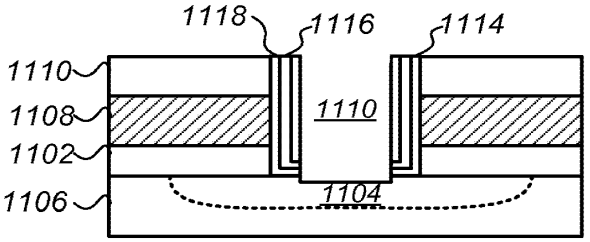


FIG. 11D

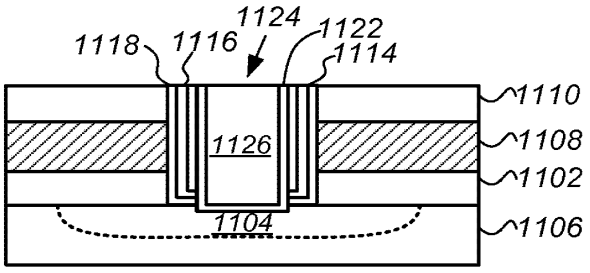


FIG. 11E

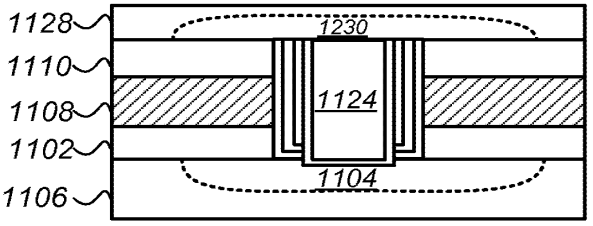


FIG. 11F

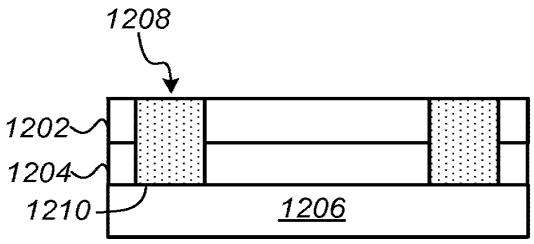


FIG. 12A

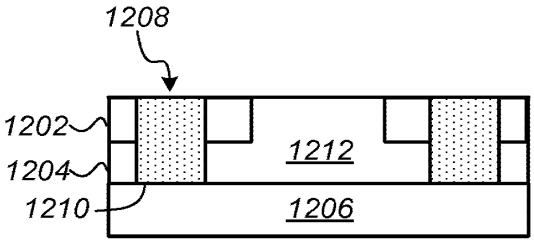


FIG. 12B

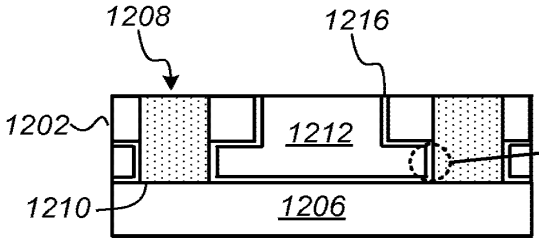


FIG. 12C

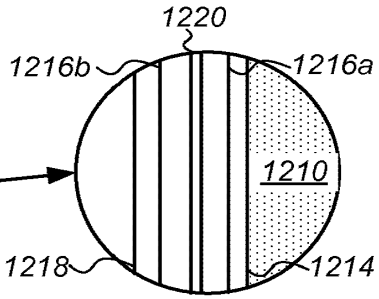


FIG. 12D

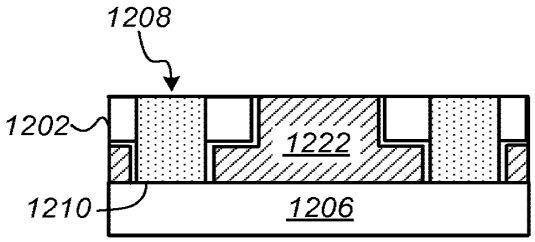


FIG. 12E

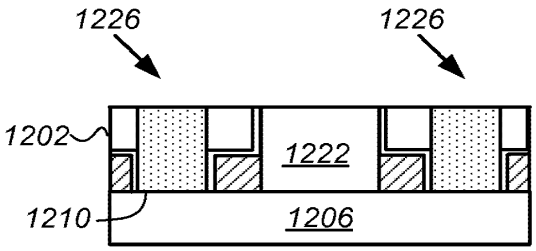


FIG. 12F

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/032339

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/792 (2013.01)
USPC - 257/411
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/336, 29/792 (2013.01)
USPC - 257/324, 406, 411, E21.423, E29.309; 438/287, 763

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
CPC - H01L 29/792; 29/7926 (2013.01)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Orbit, Google Patent, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X – Y	US 8,063,434 B1 (POLISHCHUK et al) 22 November 2011 (22.11.2011) entire document	1, 8 – 2-7, 9-20
Y	US 2008/0048237 A1 (IWATA) 28 February 2008 (28.02.2008) entire document	2, 3
Y	US 2005/0275010 A1 (CHEN et al) 15 December 2005 (15.12.2005) entire document	4-7, 9-14
Y	US 6,709,928 B1 (JENNE et al) 23 March 2004 (23.03.2004) entire document	9-14, 17, 19
Y	US 2008/0293255 A1 (RAMKUMAR) 27 November 2008 (27.11.2008) entire document	13
Y	WO 2011/162725 A1 (SINGH et al) 29 December 2011 (29.12.2011) entire document	15-20
A	US 8,067,284 B1 (LEVY) 29 November 2011 (29.11.2011) entire document	1-20
A	US 2009/0179253 A1 (LEVY et al) 16 July 2009 (16.07.2009) entire document	1-20
P,A	US 8,222,688 B1 (JENNE et al) 17 July 2012 (17.07.2012) entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 May 2013	30 MAY 2013
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

Espacenet

WO2013148112A1 SONOS STACK WITH SPLIT NITRIDE MEMORY LAYER

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Inventors: JENNE FREDRICK [US],RAMKUMAR KRISHNASWAMY [US]

Classifications:
IPC ***H01L29/792;***

CPC **B82Y10/00 (EP); H01L27/11582 (EP); H01L29/0673 (EP); H01L29/0676 (EP); H01L29/40117 (EP); H01L29/42348 (EP); H01L29/513 (EP,CN); H01L29/518 (EP,CN); H01L29/66439 (EP); H01L29/66833 (EP,CN); H01L29/775 (EP); H01L29/792 (EP,CN); H01L29/7926 (EP,CN);** H01L29/785 (EP);

Priorities: US201213431069A 2012-03-27

Application: WO2013148112A1·2013-03-08

Publication: WO2013148112A1·2013-10-03

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SONOS STACK WITH SPLIT NITRIDE MEMORY LAYER

Abstract

Embodiments of a non-planar memory device including a split charge-trapping region and methods of forming the same are described. Generally, the device comprises: a channel formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide overlying the channel; a split charge-trapping region overlying the tunnel oxide, the split charge-trapping region including a bottom charge-trapping layer comprising a nitride closer to the tunnel oxide, and a top charge-trapping layer, wherein the bottom charge-trapping layer is separated from the top charge-trapping layer by a thin anti-tunneling layer comprising an oxide. Other embodiments are also disclosed.

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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[Continued on next page]

(54) Title: SONOS STACK WITH SPLIT NITRIDE MEMORY LAYER

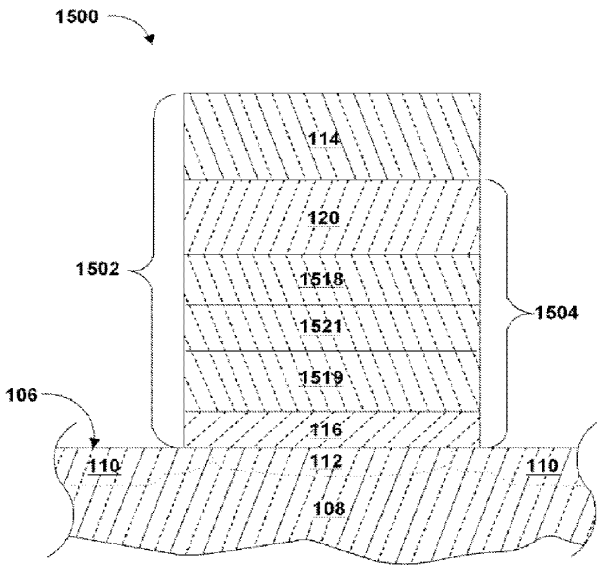


FIG. 11

(57) Abstract: Embodiments of a non-planar memory device including a split charge-trapping region and methods of forming the same are described. Generally, the device comprises: a channel formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide overlying the channel; a split charge-trapping region overlying the tunnel oxide, the split charge-trapping region including a bottom charge-trapping layer comprising a nitride closer to the tunnel oxide, and a top charge-trapping layer, wherein the bottom charge-trapping layer is separated from the top charge-trapping layer by a thin anti-tunneling layer comprising an oxide. Other embodiments are also disclosed.

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Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

Published:

— *with international search report (Art. 21(3))*

SONOS STACK WITH SPLIT NITRIDE MEMORY LAYER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of co-pending U.S. application Ser. No. 12/767,105, filed April 26, 2010, which claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 61/172,320, filed on April 24, 2009, both of which are incorporated by reference herein.

TECHNICAL FIELD

[0002] Embodiments of the present invention relate to the field of semiconductor devices.

BACKGROUND

[0003] Non-volatile semiconductor memories, such as a split gate flash memory, sometimes use a stacked floating gate structure, in which electrons are induced into a floating gate of a memory cell to be programmed by biasing a control gate and grounding a body region of a substrate on which the memory cell is formed.

[0004] An oxide-nitride-oxide (ONO) stack may be used as either a charge storing layer, as in silicon-oxide-nitride-oxide-silicon (SONOS) transistor, or as an isolation layer between the floating gate and control gate, as in a split gate flash memory.

[0005] FIG. 1 is a partial cross-sectional view of a structure for a semiconductor device 100 having a SONOS gate stack or structure 102. The structure 100 includes a conventional ONO stack 104 formed over a surface 106 of a silicon substrate 108. The device 100 typically further includes one or more diffusion regions 110, such as source and drain regions, aligned to the gate stack and separated by a channel region 112. The SONOS structure 102 includes a polysilicon gate layer 114 formed upon and in contact with the ONO stack 104. The poly gate 114 is separated or electrically isolated from the

substrate 108 by the ONO stack 104. The ONO stack 104 generally includes a lower (tunnel) oxide layer 116, a nitride or oxynitride layer 118 which serves as a charge storing or memory layer for the device 100, and a top oxide layer 120 overlying the nitride or oxynitride layer 118.

[0006] One problem with this conventional SONOS structure 102 is the poor data retention of the nitride or oxynitride layer 118 that limits the device 100 lifetime and/or its use in several applications due to leakage current through the layer. Another problem with conventional SONOS structures 102 is that the stoichiometry of the layer 118 is non-uniform across the thickness of the layer. In particular, the layer 118 is conventionally formed or deposited in a single step using a single process gas mixture and fixed or constant processing conditions in an attempt to provide a homogeneous layer having a high nitrogen and high oxygen concentration across the thickness of the relatively thick layer. However, this may result in nitrogen, oxygen and silicon concentrations that vary throughout the conventional layer 118. Consequently, the charge storage characteristics, and in particular programming and erase speed and data retention of a memory device 100 made with the ONO stack 104, are adversely effected.

[0007] FIG. 2-5 illustrate charge retention and migration in a conventional SONOS structure such as the one illustrated in FIG. 1. Charge traps are distributed through the nitride layer 118. The distribution of traps is uniform under ideal stoichiometric conditions (FIG. 2), but typically the distribution would not be so ideally uniform. When an ERASE (FIG. 3) is performed, holes migrate toward the blocking oxide 120. Electron charge accumulates at the layer boundaries after programming (FIG. 4). This stored charge distribution can lead to significant leakage due to tunneling at the

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nitride boundaries, for example by the process illustrated in the energy diagram FIG. 5, in which stored charge transitions among trapped states (e.g. E_{TA}, E_{TD}) to cause leakage.

[0008] Thus there is an ongoing need for a memory device that exhibits improved data retention and improved stoichiometry.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] These and various other features and advantages of the present structure and method will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

[0010] FIG. 1 is a cross-sectional view of a conventional SONOS structure.

[0011] FIGs. 2-4 illustrate charge retention and migration in a conventional SONOS structure such as the one illustrated in FIG. 1.

[0012] FIG. 5 illustrates an energy band diagram for a conventional SONOS structure, in which stored charge transitions among trapped states (e.g. E_{TA}, E_{TD}) to cause leakage.

[0013] FIG. 6 is a cross-sectional view of a SONNOS structure.

[0014] FIG. 7-9 illustrate charge retention and migration in a SONNOS structure such as the one illustrated in FIG. 6.

[0015] FIG. 10 illustrates an energy band diagram for a SONNOS structure in which stored charge transitions among trapped states (e.g. E_{TA}, E_{TD}) to cause leakage.

[0016] FIG. 11 is a cross-sectional view of a SONONOS structure.

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[0017] FIG. 12-14 illustrate charge retention and migration in a SONONOS structure such as the one illustrated in FIG. 14.

[0018] FIG. 15 illustrates an energy band diagram for a SONONOS structure in which stored charge transitions among trapped states (e.g. E_{TA}, E_{TD}) to cause leakage.

[0019] FIG. 16A illustrates a non-planar multigate device including a split charge-trapping region;

[0020] FIG. 16B illustrates a cross-sectional view of the non-planar multigate device of FIG. 16A.

[0021] FIGs. 17A and 17B illustrate a non-planar multigate device including a split charge-trapping region and a horizontal nanowire channel.

[0022] FIGs. 18A and 18B illustrate a non-planar multigate device including a split charge-trapping region and a vertical nanowire channel.

[0023] FIG. 19A and 19B illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 18A.

[0024] FIG. 20A and 20B illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 18A.

DETAILED DESCRIPTION

[0025] References to "one embodiment" or "an embodiment" do not necessarily refer to the same embodiment, although they may.

[0026] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in the sense

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of "including, but not limited to." Words using the singular or plural number also include the plural or singular number respectively. Additionally, the words "herein," "above," "below" and words of similar import, when used in this application, refer to this application as a whole and not to any particular portions of this application. When the claims use the word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list and any combination of the items in the list.

Overview

[0027] A charge-storage circuit may be formed with multiple charge storing layers including multiple nitride layers having differing concentrations of oxygen, nitrogen and/or silicon. The nitride layers may include at least a top nitride layer and a bottom nitride layer. At least the bottom nitride layer may comprise silicon oxynitride (e.g. $Si_xO_yN_x$). The stoichiometric compositions of the layers may be tailored or selected such that the lower or bottom nitride has a high oxygen and silicon content, and the top nitride layer has high silicon and a high nitrogen concentration with a low oxygen concentration to produce a silicon-rich nitride or oxynitride. The silicon-rich and oxygen-rich bottom nitride layer reduces stored charge loss without compromising device speed or an initial (beginning of life) difference between program and erase voltages. The silicon-rich, oxygen-lean top nitride layer increases a difference between programming and erase voltages when the structure is employed in memory devices, thereby improving device speed, increasing data retention, and extending the operating life of the device.

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[0028] However, this structure also has drawbacks in terms of charge retention. Therefore, a middle oxide layer may be formed between the two nitride layers, forming a split charge trapping region comprising two nitride layers separated by a relatively thin oxide layer. In one embodiment, the two nitride layers are approximately equal thicknesses. Each nitride layer may be at least 30Å. The middle oxide layer may be at least 5A. Some tolerance for process variations is also envisioned, for example ±2Å. In general, the middle oxide layer will be thin relative to the two nitride layers, where 'thin relative to' means at least a ratio of about .75:1. One nitride layer (the bottom layer) may be closer to a substrate, and oxygen-rich relative to the other (upper) nitride layer.

[0029] One process for manufacturing such a semiconductor device includes forming a first oxide layer on a silicon substrate; forming a first nitride layer on the first oxide layer; applying radical oxidation to the first nitride layer to form a second oxide layer; and forming a second nitride layer on the second oxide layer. The first nitride layer is made oxygen-rich relative to the second nitride layer by varying the process parameters. For example, each nitride layer may be formed using a low pressure CVD process using a silicon source, a nitrogen source, and an oxygen-containing gas. With appropriate process parameters, a bottom oxynitride layer may be formed that is a silicon-rich and oxygen-rich, and a top nitride layer is may be formed that is silicon-rich, nitrogen-rich, and oxygen-lean. In one embodiment the first (lower) nitride layer is formed to a thickness of between 35Å and 50Å, oxidized to a depth of between 5Å and 20Å to form the middle oxide layer, and then the second nitride layer is formed over the middle oxide layer to a thickness of between 30Å and 60Å. The first (tunnel) oxide layer

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on the silicon substrate may be formed to a thickness of about 15-20Å. Again, some tolerance for process variations are envisioned, for example ±2Å.

[0030] A third oxide layer may be formed over the second nitride layer, to a thickness of about 40- 50Å, and a polysilicon or metal gate layer may be formed over the third oxide layer.

Multi-Layer Charge Storing Structure

[0031] FIG. 6 is a block diagram illustrating a cross-sectional side view of a portion of a semiconductor memory device 800. The memory device 800 includes a SONNOS gate stack 802 including an ONNO structure 804 formed over a surface 106 of silicon layer on a substrate 108. The device 800 further includes one or more diffusion regions 110, such as source and drain regions, aligned to the gate stack 802 and separated by a channel region 112. Generally, the SONNOS structure 802 includes a gate layer 114 formed upon and in contact with the ONNO structure 804. The gate 114 is isolated from the substrate 108 by the ONNO structure 804. The ONNO structure 804 includes a thin, lower oxide layer or tunneling oxide layer 116 that isolates the gate stack 802 from the channel region 112, a top or blocking oxide layer 120, and a multi-layer charge storing layer 804 including multiple nitride containing layers. Preferably, the multi-layer charge storing layer 804 includes at least two nitride layers, including a top nitride layer 818 and a bottom nitride layer 819.

[0032] FIG. 7-9 illustrate charge retention and migration in a SONNOS structure such as the one illustrated in FIG. 6. Charge traps are distributed through the nitride

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layers 818, 819, with a distribution that is uniform under ideal stoichiometric conditions (FIG. 7). As a result of an ERASE (FIG. 8), holes migrate toward the blocking oxide 120. Electron charge accumulates at the boundaries of the upper nitride layer 818 after programming (FIG. 9), and there is less accumulation of charge at the lower boundary of the lower nitride layer 819. This may result in lower leakage current. Nonetheless, this charge distribution may lead to charge leakage due to tunneling at the nitride boundaries, as shown for example in FIG. 10, which illustrates how charge may transition among different trapped states (e.g. E_{TA}, E_{TD}) to cause leakage after programming.

Oxide Split Multi-Layer Charge Storing Structure

[0033] FIG. 11 is a block diagram illustrating a cross-sectional side view of a semiconductor memory device 1500. The memory device 1500 includes a SONONOS stack 1502 including an ONONO structure 1504 formed over a surface 106 of a substrate 108. Substrate 108 includes one or more diffusion regions 110, such as source and drain regions, aligned to the gate stack 1502 and separated by a channel region 112. Generally, the SONONOS structure 1502 includes a polysilicon or metal gate layer 114 formed upon and in contact with the ONONO structure 1504. The gate 114 is separated or electrically isolated from the substrate 108 by the ONONO structure 1504. The ONONO structure 1504 includes a thin, lower oxide layer or tunneling oxide layer 116 that separates or electrically isolates the stack 1502 from the channel region 112, a top or blocking oxide layer 120, and a multi-layer charge storing layer 1504 including multiple nitride containing layers 1518, 1519. Preferably, the multi-layer charge storing layer 1504

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includes at least two nitride layers, including a top nitride layer 1518, a bottom oxynitride layer 1519, and an intermediate oxide layer 1521.

[0034] The various layers of the device 1500 may be fabricated to certain thicknesses. Different possibilities for the thicknesses are described herein, representing possible different embodiments. In general, the middle oxide layer will be relatively thin in comparison to the two nitride layers. For example, the middle oxide may be between approximately 5Å and 20Å. The nitride layers may be the same or different thicknesses as one another, but will typically be at least approximately 30Å. With advances in process technology and material science, nitride thicknesses as low as 20Å may be possible in the near future.

[0035] FIG. 12-14 illustrate charge retention and migration in a SONONOS structure such as the one illustrated in FIG. 11. Charge traps are distributed in the two nitride layers 1518, 1519, with a discontinuity where the intermediate oxide layer 1521 resides (few or no traps form in the oxide layer 1521). The majority of traps form in the top nitride layer 1518. Within each nitride layer, trap distribution is more or less uniform under ideal stoichiometric conditions (FIG. 12). As a result of an ERASE (FIG. 13), holes migrate toward the blocking oxide 120, but the majority of trapped hole charges form in the top nitride layer 1518. Electron charge accumulates at the boundaries of the upper nitride layer 1518 after programming (FIG. 14), and there is less accumulation of charge at the lower boundary of the lower nitride layer 1519. Furthermore, due to the intermediate oxide 1521, the probability of tunneling by trapped electron charges in the upper nitride layer 1518 is substantially reduced. This may result in lower leakage current than for the structures illustrated in FIG. 1 and FIG. 6. This charge distribution

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significantly lowers the probability of tunneling from the upper nitride layer, as shown for example in the energy band diagrams FIG. 15, which illustrate the obstacles to tunneling that charges encounter as they transition among different trapped states (e.g. E_{TA}, E_{TD}) after programming.

Fabrication Techniques

[0036] A process of forming a SONOS structure with superior charge retention begins with forming a first oxide layer, such as a tunneling oxide layer, of the ONO structure over a substrate. The substrate may be, for example, polysilicon, or a silicon surfaced germanium substrate. Next, the first nitride layer of a multi-layer charge storing structure is formed on the first oxide layer. This first or bottom nitride layer may be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The first nitride layer is then oxidized to a chosen depth using radical oxidation. This forms the middle oxide layer. Radical oxidation may be performed, for example, at a temperature of 1000-1100°C using a single wafer tool, or 800-900°C using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0037] The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The second nitride layer has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the first (lower)

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nitride layer. The second nitride layer may be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer. Finally, a second oxide layer of the ONO structure is formed on a surface of the second nitrided layer. This top or blocking oxide layer may be formed or deposited by any suitable means. In one embodiment the top oxide is a high temperature oxide deposited in a HTO CVD process. Alternatively, the top or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the top nitride thickness may be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer. A third option is to oxidize the top nitride layer to a chosen depth using radical oxidation.

[0038] In some embodiments, it may be possible perform fabrication by forming the tunnel oxide layer in one chamber of a CVD tool, then form the bottom oxynitride layer in a second chamber of the CVD tool, then radical oxidize the lower oxynitride layer in the first chamber, then deposit more nitride in the second chamber, then radical oxidize the second nitride layer in the first chamber again, thus forming the semiconductor device using a two-chamber process.

[0039] Fabrication may further involve forming or depositing a silicon containing layer on a surface of the second oxide layer to complete a SONOS stack. The silicon containing layer may, for example, be a polysilicon layer deposited by a CVD process to form a control gate of a SONOS transistor or device. In some embodiments metal may be deposited instead of polysilicon.

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[0040] Generally, the substrate 108 may include any known silicon-based semiconductor material including silicon, silicon-germanium, silicon-on-insulator, or silicon-on-sapphire substrate. Alternatively, the substrate 108 may include a silicon layer formed on a non-silicon-based semiconductor material, such as gallium-arsenide, germanium, gallium-nitride, or aluminum phosphide. Preferably, the substrate 108 is a doped or undoped silicon substrate.

[0041] The lower oxide layer or tunneling oxide layer 116 generally includes a relatively thin layer of silicon dioxide (SiO_2) of from about 15Å to about 22Å, and more preferably about 18-20Å, with some process variation (e.g. ±1Å). The tunneling oxide layer 116 may be formed or deposited by any suitable means including, for example, being thermally grown or deposited using chemical vapor deposition (CVD). In one embodiment, the tunnel oxide layer is formed or grown using a steam anneal. This involves a wet-oxidizing process in which the substrate 108 is placed in a in a deposition or processing chamber, heated to a temperature from about 700°C to about 850°C, and exposed to a wet vapor for a predetermined period of time selected based on a desired thickness of the finished tunneling oxide layer 116. Exemplary process times are from about 5 to about 20 minutes. The oxidation may be performed at atmospheric or at low pressure, or using a dry process under ambient conditions using either batch or single wafer tools.

[0042] The multi-layer charge storing structure generally includes at least two nitride layers having differing compositions of silicon, oxygen and nitrogen, and a middle oxide layer between the two nitride layers. In a preferred embodiment the nitride layers are formed or deposited in a low pressure CVD process using a silicon source, such as

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silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane (SiH_2Cl_2), tetrachlorosilane ($SiC1_4$) or Bis-TertiaryButylAmino Silane (BTBAS), a nitrogen source, such as nitrogen (N2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas, such as oxygen (0_2) or N_2O. Alternatively, gases in which hydrogen has been replaced by deuterium can be used, including, for example, the substitution of deuterated-ammonia (ND_3) for NH_3. The substitution of deuterium for hydrogen advantageously passivates Si dangling bonds at the silicon-oxide interface, thereby increasing the endurance of the devices.

[0043] For example, the lower or bottom oxynitride layer 819, 1519 may be deposited over the tunneling oxide layer 116 by placing the substrate 108 in a deposition chamber and introducing a process gas including N_2O, NH3 and DCS, while maintaining the chamber at a pressure of from about 5 millitorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700°C to about 850°C, and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes. The process gas may include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and may be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm). A layer produced or deposited under these condition yields a silicon-rich, oxygen-rich, bottom oxynitride layer 819, that decrease the charge loss rate after programming and after erase, which may be manifested in a small voltage shift in the retention mode.

[0044] The top nitride layer 818, 1518 may be deposited in a CVD process using a process gas including N_2O, NH3 and DCS, at a chamber pressure of from about 5 mT

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to about 500 mT, and at a substrate temperature of from about 700°C to about 850°C, and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes. The process gas may include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and may be introduced at a flow rate of from about 5 to about 20 sccm. A layer produced or deposited under these condition yields a silicon-rich, nitrogen-rich, and oxygen-lean top nitride layer 818, 1518.

[0045] Preferably, the top nitride layer 818, 1518 is deposited sequentially, after formation of the middle oxide layer, in the same process chamber used to form the bottom oxynitride layer 819, 1519, without altering the temperature to which the substrate 108 was heated during deposition of the bottom oxynitride layer 819, 1519. In one embodiment, the top nitride layer 818, 1518 is deposited sequentially following the deposition of the bottom oxynitride layer 819, 1519 by (1) moving to a different process chamber to form the middle oxide layer by radical oxidation of the bottom oxynitride layer, (2) returning to the process chamber used to form the bottom oxynitride layer and decreasing the flow rate of the N_2O/NH_3 gas mixture relative to the DCS/NH_3 gas mixture to provide the desired ratio of the gas mixtures to yield the silicon-rich, nitrogen-rich, and oxygen-lean top nitride layer 818, 1518.

[0046] A suitable thickness for the bottom oxynitride layer 819, 1519 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the middle oxide layer. A suitable thickness for the top nitride layer 818, 1518 may be at least 30Å. In certain embodiments, the upper nitride layer may be formed up to 130Å thick, of which

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30-70Å may be consumed by radical oxidation to form the top oxide layer. A ratio of thicknesses between the bottom oxynitride layer and the top nitride layer is approximately 1:1 in some embodiments, although other ratios are also possible.

[0047] The top oxide layer 120 includes a relatively thick layer of SiO_2 of from about 30Å to about 70Å, and more preferably about 40-50Å. The top oxide layer 120 may be formed or deposited by any suitable means including, for example, being thermally grown or deposited using CVD. In one embodiment, the top oxide layer 120 is a high-temperature-oxide (HTO) deposited using CVD process. This deposition process involves exposing the substrate 108 to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-containing gas, such as O_2 or N_2O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

[0048] The top oxide layer 120 may be formed by oxidizing the top nitride layer 818, 1518. This may be accomplished in the same chamber used to form the nitride layers 116, 818, 819. The nitride layers 818, 819, 1518, 1519 may be formed in a first chamber, and the oxide layers 116, 1521, 120 may formed in a second chamber, of a two-chamber tool. Suitable tools include, for example, an ONO AVP, commercially available from AVIZA technology of Scotts Valley, Calif.

[0049] Although shown and described above as having two nitride layers, i.e., a top and a bottom layer, the present invention is not so limited, and the multi-layer charge storing structure may include a number, n, of nitride layers, any or all of which may have differing stoichiometric compositions of oxygen, nitrogen and/or silicon. In particular,

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multi-layer charge storing structures having up to five, and possibly more, nitride layers each with differing stoichiometric compositions are contemplated. At least some of these layers will be separated from the others by one or more relatively thin oxide layers. However, as will be appreciated by those skilled in the art it is generally desirable to utilize as few layers as possible to accomplish a desired result, reducing the process steps necessary to produce the device, and thereby providing a simpler and more robust manufacturing process. Moreover, utilizing as few layers as possible also results in higher yields as it is simpler to control the stoichiometric composition and dimensions of the fewer layers.

[0050] It will further be appreciated that although applicable as part of a SONOS stack in a SONOS memory device, the structure and method of the present invention is not so limited, and the ONO structure can be used in or with any semiconductor technology or in any device requiring a charge storing or dielectric layer or stack including, for example, in a split gate flash memory, a TaNOS stack, in a 1 T (transistor) SONOS cell, a 2T SONOS cell, a 3T SONOS cell, a localized 2-bit cell, and in a multilevel programming or cell, without departing from the scope of the invention.

[0051] Advantages of ONO structures and methods of forming the same according to an embodiment of the present invention over previous or conventional approaches include: (i) the ability to enhance data retention in memory devices using the structure by dividing the nitride layer into a plurality of films or layers and tailoring the oxygen, nitrogen and silicon profile across each layer, with an intermediate oxide layer to reduce the probability of charge tunneling; (ii) the ability to enhance speed of a memory device without compromising data retention; (iii) the ability to meet or exceed data

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retention and speed specifications for memory devices using an ONO structure of an embodiment of the present invention at a temperature of at least about 125°C; and (iv) provide heavy duty program erase cycles of 100,000 cycles or more.

Implementations and Alternatives

[0052] In another aspect the present disclosure is directed to multigate or multigate-surface memory devices including charge-trapping regions overlying two or more sides of a channel formed on or above a surface of a substrate, and methods of fabricating the same. Multigate devices include both planar and non-planar devices. A planar multigate device (not shown) generally includes a double-gate planar device in which a number of first layers are deposited to form a first gate below a subsequently formed channel, and a number of second layers are deposited thereover to form a second gate. A non-planar multigate device generally includes a horizontal or vertical channel formed on or above a surface of a substrate and surrounded on three or more sides by a gate.

[0053] FIG. 16A illustrates one embodiment of a non-planar multigate memory device including a charge-trapping region. Referring to FIG. 16A, the memory device 1600, commonly referred to as a finFET, includes a channel 1602 formed from a thin film or layer of semiconducting material overlying a surface 1604 on a substrate 1606 connecting a source 1608 and a drain 1610 of the memory device. The channel 1602 is enclosed on three sides by a fin which forms a gate 1612 of the device. The thickness of the gate 1612 (measured in the direction from source to drain) determines the effective channel length of the device.

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[0054] In accordance with the present disclosure, the non-planar multigate memory device 1600 of FIG. 16A can include a split charge-trapping region. FIG. 16B is a cross-sectional view of a portion of the non-planar memory device of FIG. 16A including a portion of the substrate 1606, channel 1602 and the gate 1612 illustrating a split charge-trapping region 1614. The gate 1612 further includes a tunnel oxide 1616 overlying a raised channel 1602, a blocking dielectric 1618 and a metal gate layer 1620 overlying the blocking layer to form a control gate of the memory device 1600. In some embodiments a doped polysilicon may be deposited instead of metal to provide a polysilicon gate layer. The channel 1602 and gate 1612 can be formed directly on substrate 1606 or on an insulating or dielectric layer 1622, such as a buried oxide layer, formed on or over the substrate.

[0055] Referring to FIG. 16B, the split charge-trapping region 1614 includes at least one lower or bottom charge-trapping layer 1624 comprising nitride closer to the tunnel oxide 1616, and an upper or top charge-trapping layer 1626 overlying the bottom charge-trapping layer. Generally, the top charge-trapping layer 1626 comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in multiple charge-trapping layers, while the bottom charge-trapping layer 1624 comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the top charge-trapping layer to reduce the number of charge traps therein. By oxygen-rich it is meant wherein a concentration of oxygen in the bottom charge-trapping layer 1624 is from about 15 to about 40%, whereas a concentration of oxygen in top charge-trapping layer 1626 is less than about 5%.

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[0056] In one embodiment, the blocking dielectric 1618 also comprises an oxide, such as an HTO, to provide an ONNO structure. The channel 1602 and the overlying ONNO structure can be formed directly on a silicon substrate 1606 and overlaid with a doped polysilicon gate layer 1620 to provide a SONNOS structure.

[0057] In some embodiments, such as that shown in FIG. 16B, the split charge-trapping region 1614 further includes at least one thin, intermediate or anti-tunneling layer 1628 comprising a dielectric, such as an oxide, separating the top charge-trapping layer 1626 from the bottom charge-trapping layer 1624. The anti-tunneling layer 1628 substantially reduces the probability of electron charge that accumulates at the boundaries of the upper nitride layer 1626 during programming from tunneling into the bottom nitride layer 1624, resulting in lower leakage current than for the structures illustrated in FIG. 1 and FIG. 6.

[0058] As with the embodiments described above, either or both of the bottom charge-trapping layer 1624 and the top charge-trapping layer 1626 can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The top charge-trapping layer 1626 has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the bottom charge-trapping layer 1624, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

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[0059] In those embodiments including an intermediate or anti-tunneling layer 1628 comprising oxide, the anti-tunneling layer can be formed by oxidation of the bottom oxynitride layer, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100°C using a single wafer tool, or 800-900°C using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0060] Finally, in those embodiments including a blocking dielectric 1618 comprising oxide the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of the blocking dielectric 1618 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric 1618 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the top nitride thickness may be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer. A third option is to oxidize the top nitride layer to a chosen depth using radical oxidation.

[0061] A suitable thickness for the bottom charge-trapping layer 1624 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 1628. A suitable thickness for the top charge-trapping layer 1626 may be at least 30Å. In certain embodiments, the top charge-trapping layer 1626 may be formed up to 130Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric 1618. A ratio of thicknesses between the bottom charge-trapping layer 1624

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and top charge-trapping layer 1626 is approximately 1:1 in some embodiments, although other ratios are also possible.

[0062] In other embodiments, either or both of the top charge-trapping layer 1626 and the blocking dielectric 1618 may comprise a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0063] In another embodiment, shown in FIGs. 17A and 17B, the memory device can include a nanowire channel formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device. By nanowire channel it is meant a conducting channel formed in a thin strip of crystalline silicon material, having a maximum cross-sectional dimension of about 10 nanometers (nm) or less, and more preferably less than about 6 nm. Optionally, the channel can be formed to have <100> surface crystalline orientation relative to a long axis of the channel.

[0064] Referring to FIG. 17A, the memory device 1700 includes a horizontal nanowire channel 1702 formed from a thin film or layer of semiconducting material on or overlying a surface on a substrate 1706, and connecting a source 1708 and a drain 1710 of the memory device. In the embodiment shown, the device has a gate-all-around (GAA) structure in which the nanowire channel 1702 is enclosed on all sides by a gate 1712 of the device. The thickness of the gate 1712 (measured in the direction from source to drain) determines the effective channel length of the device.

[0065] In accordance with the present disclosure, the non-planar multigate memory device 1700 of FIG. 17A can include a split charge-trapping region. FIG. 17B is

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a cross-sectional view of a portion of the non-planar memory device of FIG. 17A including a portion of the substrate 1706, nanowire channel 1702 and the gate 1712 illustrating a split charge-trapping region. Referring to FIG. 17B, the gate 1712 includes a tunnel oxide 1714 overlying the nanowire channel 1702, a split charge-trapping region, a blocking dielectric 1716 and a gate layer 1718 overlying the blocking layer to form a control gate of the memory device 1700. The gate layer 1718 can comprise a metal or a doped polysilicon. The split charge-trapping region includes at least one inner charge-trapping layer 1720 comprising nitride closer to the tunnel oxide 1714, and an outer charge-trapping layer 1722 overlying the inner charge-trapping layer. Generally, the outer charge-trapping layer 1722 comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in multiple charge-trapping layers, while the inner charge-trapping layer 1720 comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the outer charge-trapping layer to reduce the number of charge traps therein.

[0066] In some embodiments, such as that shown, the split charge-trapping region further includes at least one thin, intermediate or anti-tunneling layer 1724 comprising a dielectric, such as an oxide, separating outer charge-trapping layer 1722 from the inner charge-trapping layer 1720. The anti-tunneling layer 1724 substantially reduces the probability of electron charge that accumulates at the boundaries of outer charge-trapping layer 1722 during programming from tunneling into the inner charge-trapping layer 1720, resulting in lower leakage current.

[0067] As with the embodiment described above, either or both of the inner charge-trapping layer 1720 and the outer charge-trapping layer 1722 can comprise silicon

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nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The outer charge-trapping layer 1722 has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the inner charge-trapping layer 1720, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

[0068] In those embodiments including an intermediate or anti-tunneling layer 1724 comprising oxide, the anti-tunneling layer can be formed by oxidation of the inner charge-trapping layer 1720, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100°C using a single wafer tool, or 800-900°C using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0069] Finally, in those embodiments in which the blocking dielectric 1716 comprises oxide, the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of blocking dielectric 1716 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric 1716 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the thickness of the outer charge-trapping layer 1722 may need to be adjusted or increased as

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some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer.

[0070] A suitable thickness for the inner charge-trapping layer 1720 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 1724. A suitable thickness for the outer charge-trapping layer 1722 may be at least 30Å. In certain embodiments, the outer charge-trapping layer 1722 may be formed up to 130Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric 1716. A ratio of thicknesses between the inner charge-trapping layer 1720 and the outer charge-trapping layer 1722 is approximately 1:1 in some embodiments, although other ratios are also possible.

[0071] In other embodiments, either or both of the outer charge-trapping layer 1722 and the blocking dielectric 1716 may comprise a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0072] In another embodiment, the memory device is or includes a non-planar device comprising a vertical nanowire channel formed in or from a semiconducting material projecting above or from a number of conducting, semiconducting layers on a substrate. In one version of this embodiment, shown in cut-away in FIG. 18A, the memory device 1800 comprises a vertical nanowire channel 1802 formed in a cylinder of semiconducting material connecting a source 1804 and drain 1806 of the device. The channel 1802 is surrounded by a tunnel oxide 1808, a charge-trapping region 1810, a blocking layer 1812 and a gate layer 1814 overlying the blocking layer to form a control

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gate of the memory device 1800. The channel 1802 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or can include an annular layer formed over a cylinder of dielectric filler material. As with the horizontal nanowires described above, the channel 1802 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel. Optionally, where the channel 1802 includes a crystalline silicon, the channel can be formed to have <100> surface crystalline orientation relative to a long axis of the channel.

[0073] In some embodiments, such as that shown in FIG. 18B, the charge-trapping region 1810 can be a split charge-trapping region including at least a first or inner charge trapping layer 1816 closest to the tunnel oxide 1808, and a second or outer charge trapping layer 1818. Optionally, the first and second charge trapping layers can be separated by an intermediate oxide or anti-tunneling layer 1820.

[0074] As with the embodiments described above, either or both of the first charge trapping layer 1816 and the second charge trapping layer 1818 can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer.

[0075] Finally, either or both of the second charge trapping layer 1818 and the blocking layer 1812 may comprise a high K dielectric, such as HfSiON, HfSiO, HfO, ZrSiON, ZrSiO, ZrO, or Y_2O_3.

[0076] A suitable thickness for the first charge trapping layer 1816 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer

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1820. A suitable thickness for the second charge trapping layer 1818 may be at least 30Å, and a suitable thickness for the blocking dielectric 1812 may be from about 30-70Å.

[0077] The memory device 1800 of FIG. 18A can be made using either a gate first or a gate last scheme. FIG. 19A-F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 18A. FIG. 20A-F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 18A.

[0078] Referring to FIG. 19A, in a gate first scheme a first or lower dielectric layer 1902, such as a blocking oxide, is formed over a first, doped diffusion region 1904, such as a source or a drain, in a substrate 1906. A gate layer 1908 is deposited over the first dielectric layer 1902 to form a control gate of the device, and a second or upper dielectric layer 1910 formed thereover. As with embodiments described above, the first and second dielectric layers 1902, 1910, can be deposited by CVD, radical oxidation or be formed by oxidation of a portion of the underlying layer or substrate. The gate layer 1908 can comprise a metal deposited or a doped polysilicon deposited by CVD. Generally the thickness of the gate layer 1908 is from about 40- 50Å, and the first and second dielectric layers 1902, 1910, from about 20- 80Å.

[0079] Referring to FIG. 19B, a first opening 1912 is etched through the overlying gate layer 1908, and the first and second dielectric layers 1902, 1910, to the diffusion region 1904 in the substrate 1906. Next, layers of a tunneling oxide 1914, charge-trapping region 1916, and blocking dielectric 1918 are sequentially deposited in the opening and the surface of the upper dielectric layer 1910 planarize to yield the intermediate structure shown in FIG. 19C.

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[0080] Although not shown, it will be understood that as in the embodiments described above the charge-trapping region 1916 can include a split charge-trapping region comprising at least one lower or bottom charge-trapping layer closer to the tunnel oxide 1914, and an upper or top charge-trapping layer overlying the bottom charge-trapping layer. Generally, the top charge-trapping layer comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in multiple charge-trapping layers, while the bottom charge-trapping layer comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the top charge-trapping layer to reduce the number of charge traps therein. In some embodiments, the split charge-trapping region 1916 further includes at least one thin, intermediate or anti-tunneling layer comprising a dielectric, such as an oxide, separating the top charge-trapping layer from the bottom charge-trapping layer.

[0081] Next, a second or channel opening 1920 is anisotropically etched through tunneling oxide 1914, charge-trapping region 1916, and blocking dielectric 1918, FIG. 19D. Referring to FIG. 19E, a semiconducting material 1922 is deposited in the channel opening to form a vertical channel 1924 therein. The vertical channel 1924 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or, as shown in FIG. 19E, can include a separate, layer semiconducting material 1922 surrounding a cylinder of dielectric filler material 1926.

[0082] Referring to FIG. 19F, the surface of the upper dielectric layer 1910 is planarized and a layer of semiconducting material 1928 including a second, doped diffusion region 1930, such as a source or a drain, formed therein deposited over the upper dielectric layer to form the device shown.

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[0083] Referring to FIG. 20, in a gate last scheme a dielectric layer 2002, such as an oxide, is formed over a sacrificial layer 2004 on a surface on a substrate 2006, an opening etched through the dielectric and sacrificial layers and a vertical channel 2008 formed therein. As with embodiments described above, the vertical channel 2008 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material 2010, such as a polycrystalline or monocrystalline silicon, or can include a separate, layer semiconducting material surrounding a cylinder of dielectric filler material (not shown). The dielectric layer 2002 can comprise any suitable dielectric material, such as a silicon oxide, capable of electrically isolating the subsequently formed gate layer of the memory device 1800 from an overlying electrically active layer or another memory device. The sacrificial layer 2004 can comprise any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 2002, substrate 2006 and vertical channel 2008.

[0084] Referring to FIG. 20B, a second opening 2012 is etched through the etched through the dielectric and sacrificial layers 2002, 2004, to the substrate 1906, and the sacrificial layer 2004 etched or removed. The sacrificial layer 2004 can comprise any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 2002, substrate 2006 and vertical channel 2008. In one embodiment the sacrificial layer 2004 comprises silicon dioxide that can be removed by buffered oxide etch (BOE etch).

[0085] Referring to FIGs. 20C and 20D, layers of a tunneling oxide 2014, charge-trapping region 2016, and blocking dielectric 2018 are sequentially deposited in the opening and the surface of the dielectric layer 2002 planarize to yield the intermediate

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structure shown in FIGs. 20C and 20D. In some embodiments, such as that shown in FIG. 20D, the charge-trapping region 2016 can be a split charge-trapping region including at least a first or inner charge trapping layer 2016a closest to the tunnel oxide 2014, and a second or outer charge trapping layer 2016b. Optionally, the first and second charge trapping layers can be separated by an intermediate oxide or anti-tunneling layer 2020.

[0086] Next, a gate layer 2022 is deposited into the second opening 2012 and the surface of the upper dielectric layer 2002 planarized to yield the intermediate structure illustrated in FIG. 20E. As with embodiments described above, the gate layer 2022 can comprise a metal deposited or a doped polysilicon. Finally, an opening 2024 is etched through the gate layer 2022 to form control gate of separate memory devices 2026.

[0087] "Logic" refers to signals and/or information that may be applied to influence the operation of a device. Software, hardware, and firmware are examples of logic. Hardware logic may be embodied in circuits. In general, logic may comprise combinations of software, hardware, and/or firmware.

[0088] Embodiments of the charge retention devices described herein may be employed in logic circuits to function as machine-memory. Those having skill in the art will appreciate that there are various logic implementations that may embody the described structures, and that the preferred vehicle will vary with the context in which the processes are deployed. For example, if an implementer determines that speed and accuracy are paramount, the implementer may opt for a hardware and/or firmware vehicle; alternatively, if flexibility is paramount, the implementer may opt for a solely software implementation; or, yet again alternatively, the implementer may opt for some combination of hardware, software, and/or firmware. Hence, there are many vehicles that

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may employ the devices described herein, none of which is inherently superior to the other in that any vehicle to be utilized is a choice dependent upon the context in which the vehicle will be deployed and the specific concerns (e.g., speed, flexibility, or predictability) of the implementer, any of which may vary. Those skilled in the art will recognize that optical aspects of implementations may involve optically-oriented hardware, software, and or firmware.

[0089] The foregoing detailed description has set forth various embodiments of the devices and/or processes via the use of block diagrams, flowcharts, and/or examples. Insofar as such block diagrams, flowcharts, and/or examples contain one or more functions and/or operations, it will be understood as notorious by those within the art that each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof

[0090] Embodiments of the structures described herein may be employed in Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), central processing units (CPUs), digital signal processors (DSPs), or other integrated formats. However, those skilled in the art will recognize that some aspects of the embodiments disclosed herein, in whole or in part, can be equivalently implemented in dedicated memory circuits, for the purpose of storing digital information for data and/or programs running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more processors (e.g., as one or more programs running on one or more microprocessors), as firmware, or as virtually any combination thereof

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[0091] In a general sense, those skilled in the art will recognize that the various structures described herein may be embodied, individually and/or collectively, by a wide range of electrical circuitry. As used herein "electrical circuitry" includes, but is not limited to, electrical circuitry having at least one discrete electrical circuit, electrical circuitry having at least one integrated circuit, electrical circuitry having at least one application specific integrated circuit, electrical circuitry forming a general purpose computing device configured by a computer program (e.g., a general purpose computer configured by a computer program which at least partially carries out processes and/or devices described herein, or a microprocessor configured by a computer program which at least partially carries out processes and/or devices described herein), electrical circuitry forming a memory device (e.g., forms of random access memory), and/or electrical circuitry forming a communications device (e.g., a modem, communications switch, or optical-electrical equipment).

[0092] Those skilled in the art will recognize that it is common within the art to describe devices and/or processes in the fashion set forth herein, and thereafter use standard engineering practices to integrate such described devices and/or processes into larger systems. That is, at least a portion of the devices and/or processes described herein can be integrated into a network processing system without an undue amount of experimentation.

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IN THE CLAIMS

WHAT IS CLAIMED IS:

1. A memory device comprising:

a channel formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device;

a tunnel oxide overlying the channel;

a split charge-trapping region overlying the tunnel oxide, the split charge-trapping region including a bottom charge-trapping layer comprising a nitride closer to the tunnel oxide, and a top charge-trapping layer, wherein the bottom charge-trapping layer is separated from the top charge-trapping layer by a thin anti-tunneling layer comprising an oxide.

2. The memory device of claim 1, wherein the top charge-trapping layer comprises a silicon-rich, oxygen-lean nitride, the bottom charge-trapping layer comprises an oxygen-rich nitride, and further comprising a blocking dielectric layer overlying the split charge-trapping region.

3. The memory device of claim 2, wherein the top charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region.

4. The memory device of claim 2, wherein the blocking layer comprises a high K dielectric.

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5. The memory device of claim 2, wherein the channel is fabricated from silicon having <100> surface crystalline orientation relative to a long axis of the channel.

6. The memory device of claim 2, wherein the channel comprises polysilicon.

7. The memory device of claim 2, wherein the channel comprises recrystallized polysilicon.

8. The memory device of claim 2, wherein the channel comprises a silicon nanowire.

9. The memory device of claim 2, wherein the tunnel oxide comprises a nitrided oxide.

10. The memory device of claim 1, wherein the top charge-trapping layer comprises a high K dielectric.

11. The memory device of claim 1, wherein the channel projects above the surface on the substrate, and further comprising a fin intersecting and overlying at least a portion of the channel, the fin comprising the tunnel oxide and the split charge-trapping region overlying the tunnel oxide.

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12. The memory device of claim 11, wherein the top charge-trapping layer comprises a silicon-rich, oxygen-lean nitride, the bottom charge-trapping layer comprises an oxygen-rich nitride layer, and further comprising a blocking oxide layer overlying the split charge-trapping region.

13. The memory device of claim 12, further comprising a metal gate layer overlying the blocking oxide layer.

14. A memory device comprising:

a vertical channel formed from a thin projection of semiconducting material extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region;

a tunnel oxide abutting the vertical channel;

a split charge-trapping region abutting the tunnel oxide, the split charge-trapping region including a first charge-trapping layer comprising an oxygen-rich nitride closer to the tunnel oxide, and a second charge-trapping layer comprising a silicon-rich, oxygen-lean nitride overlying the first charge-trapping layer,

wherein the second charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region.

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15. The non-planar memory device of claim 14, wherein the first charge-trapping layer is separated from the second charge-trapping layer by a thin anti-tunneling layer comprising an oxide.

16. The non-planar memory device of claim 15, wherein the vertical channel comprises silicon.

17. The non-planar memory device of claim 15, further comprising a high K dielectric blocking layer abutting the split charge-trapping region

18. The non-planar memory device of claim 14, further comprising a high K dielectric blocking layer abutting the split charge-trapping region.

19. A process of manufacturing a semiconductor device, the process comprising:

forming a channel from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device;

forming a tunnel oxide overlying the channel;

forming a split charge-trapping region over the tunnel oxide including a bottom charge-trapping layer comprising an oxygen-rich nitride overlying the tunnel oxide, a thin anti-tunneling layer comprising an oxide overlying the tunnel oxide bottom charge-trapping layer, and a top charge-trapping layer comprising a silicon-rich, oxygen-lean nitride overlying the thin anti-tunneling layer,

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wherein the top charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region.

20. The process of claim 19, wherein forming the channel comprises forming from the thin film of semiconducting material overlying the surface on the substrate a channel connecting a source and a drain raised above the surface on the substrate.

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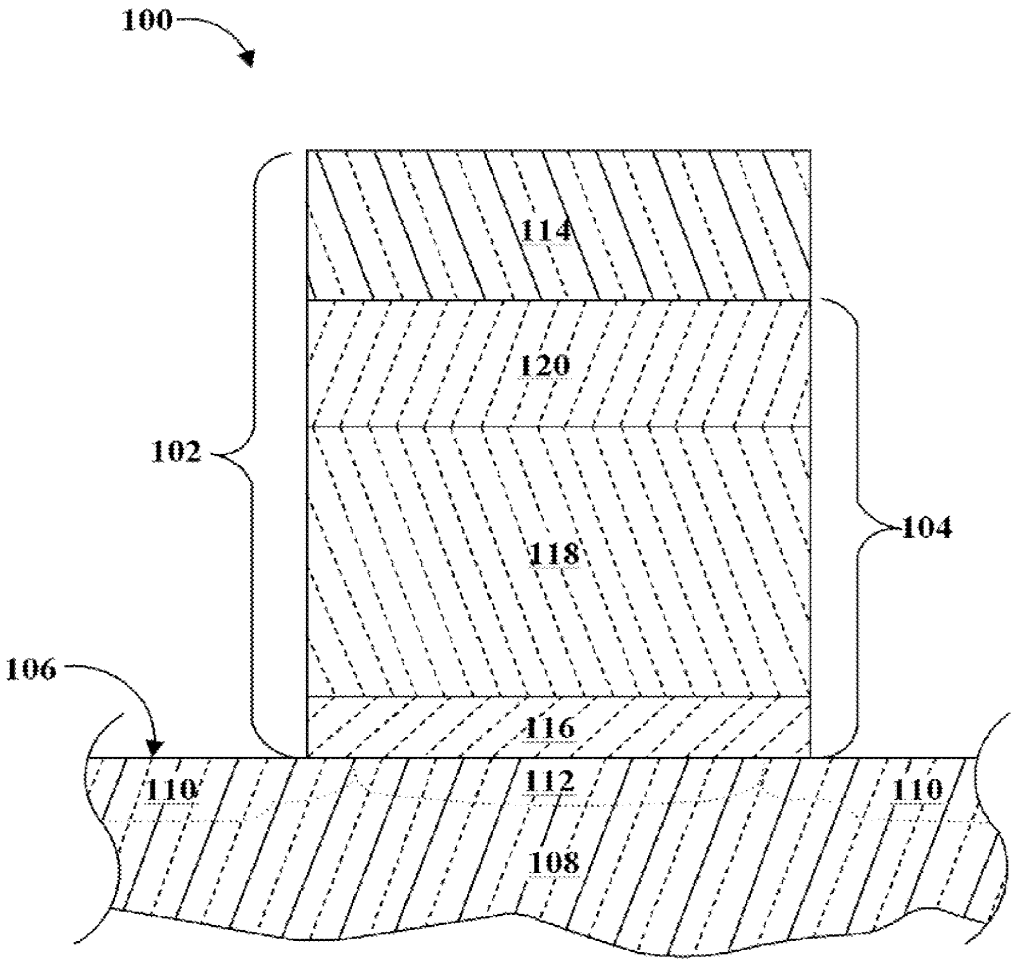


FIG. 1 (Prior Art)

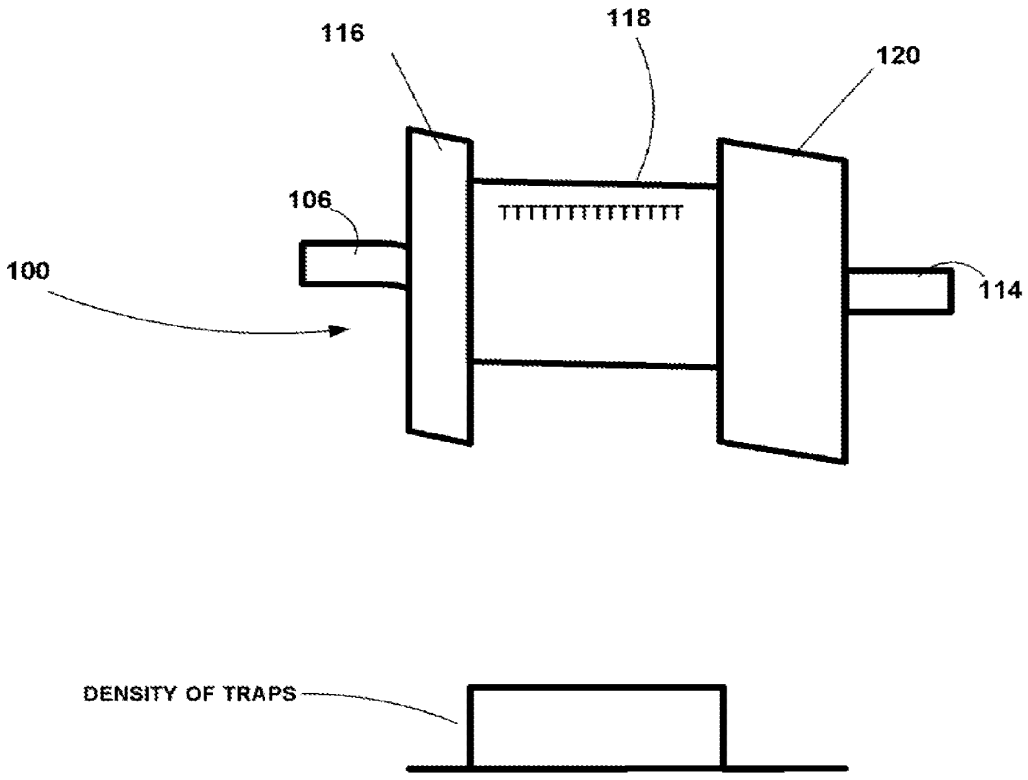


FIG. 2 (Prior Art)

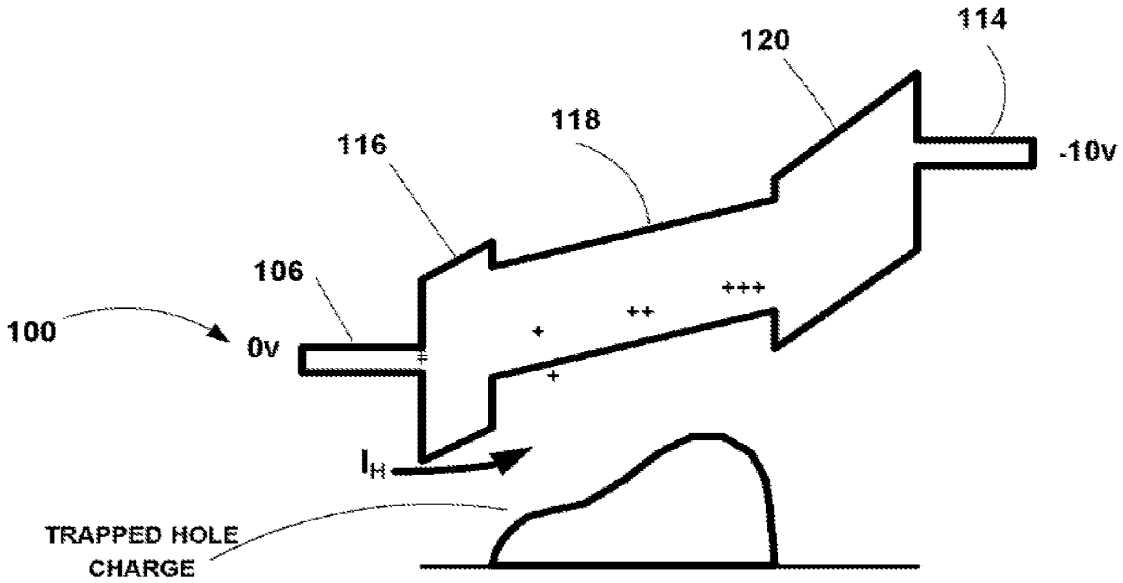


FIG. 3 (Prior Art)

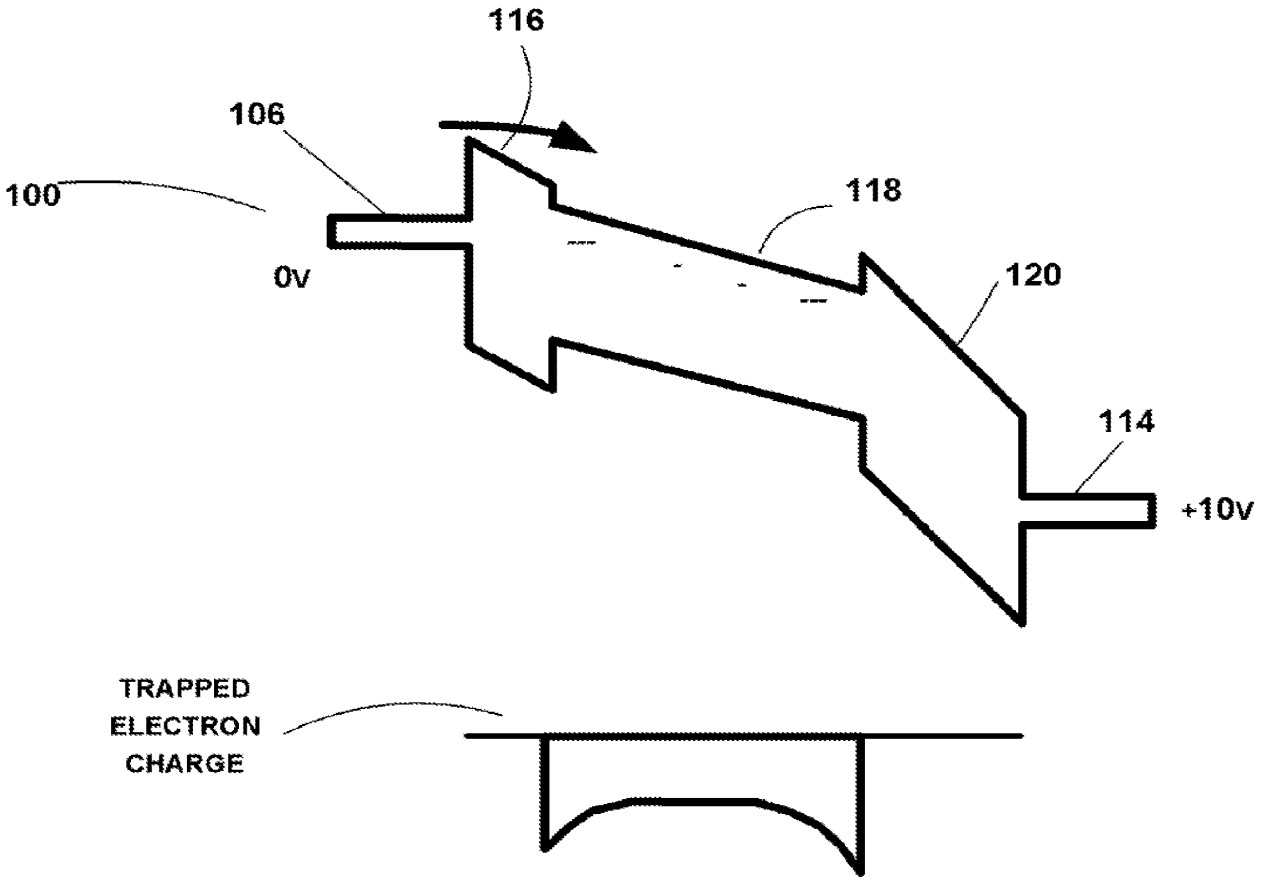


FIG. 4 (Prior Art)

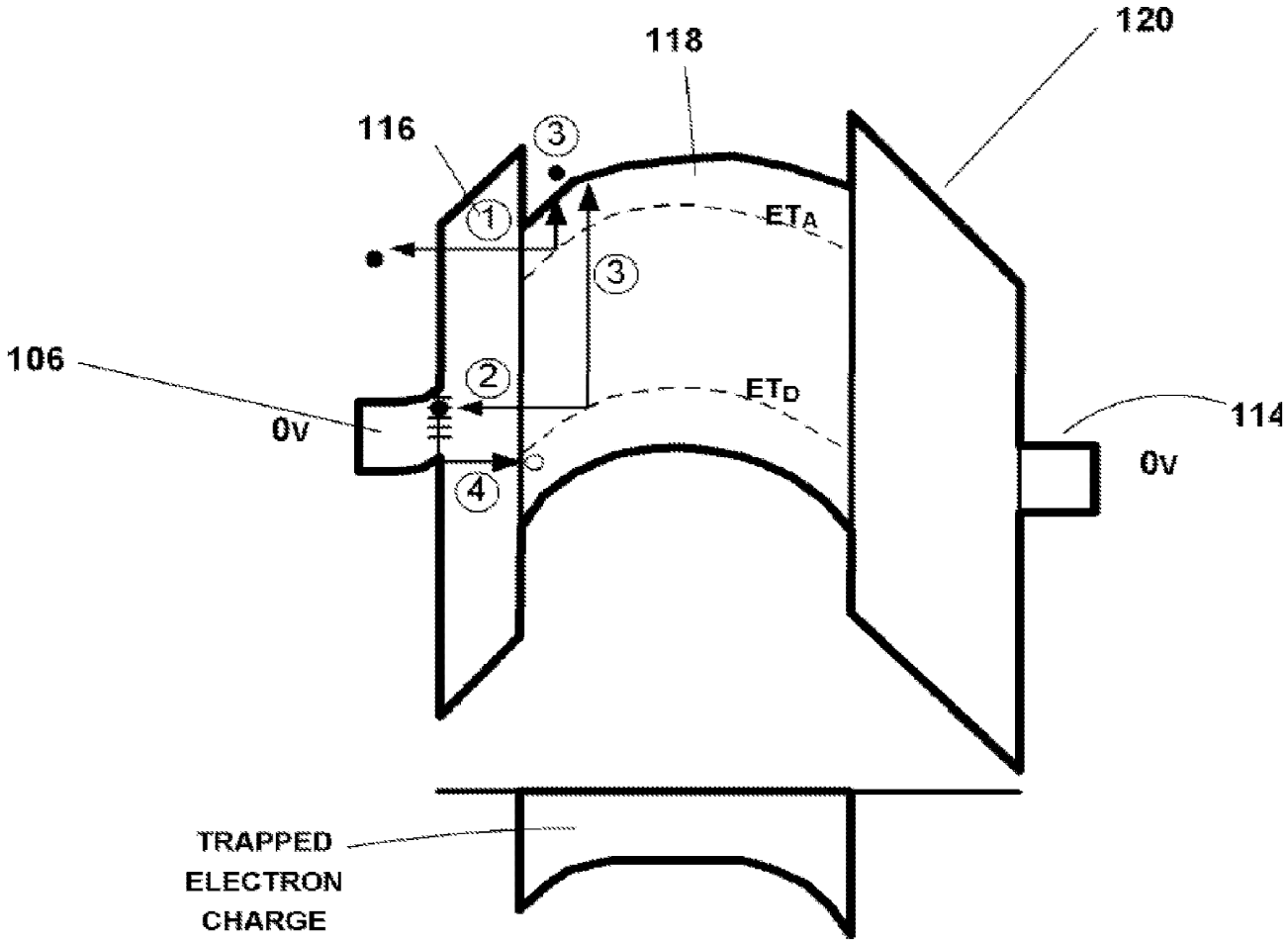


FIG. 5 (Prior Art)

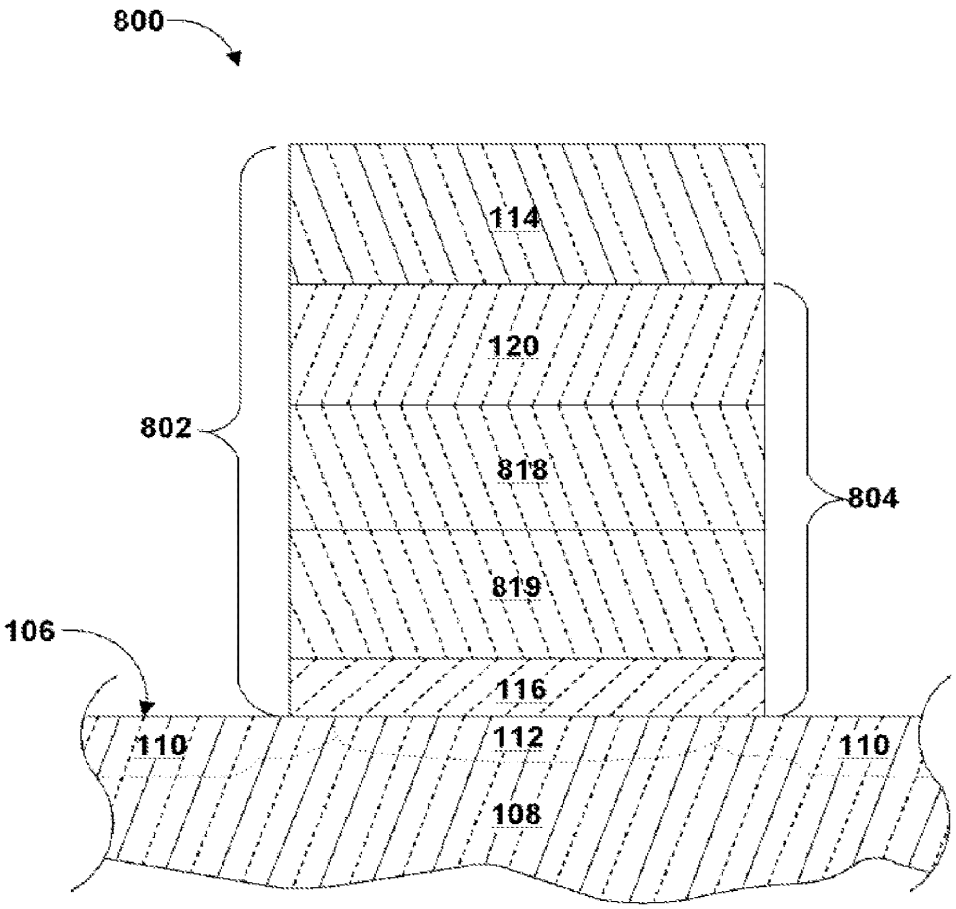


FIG. 6

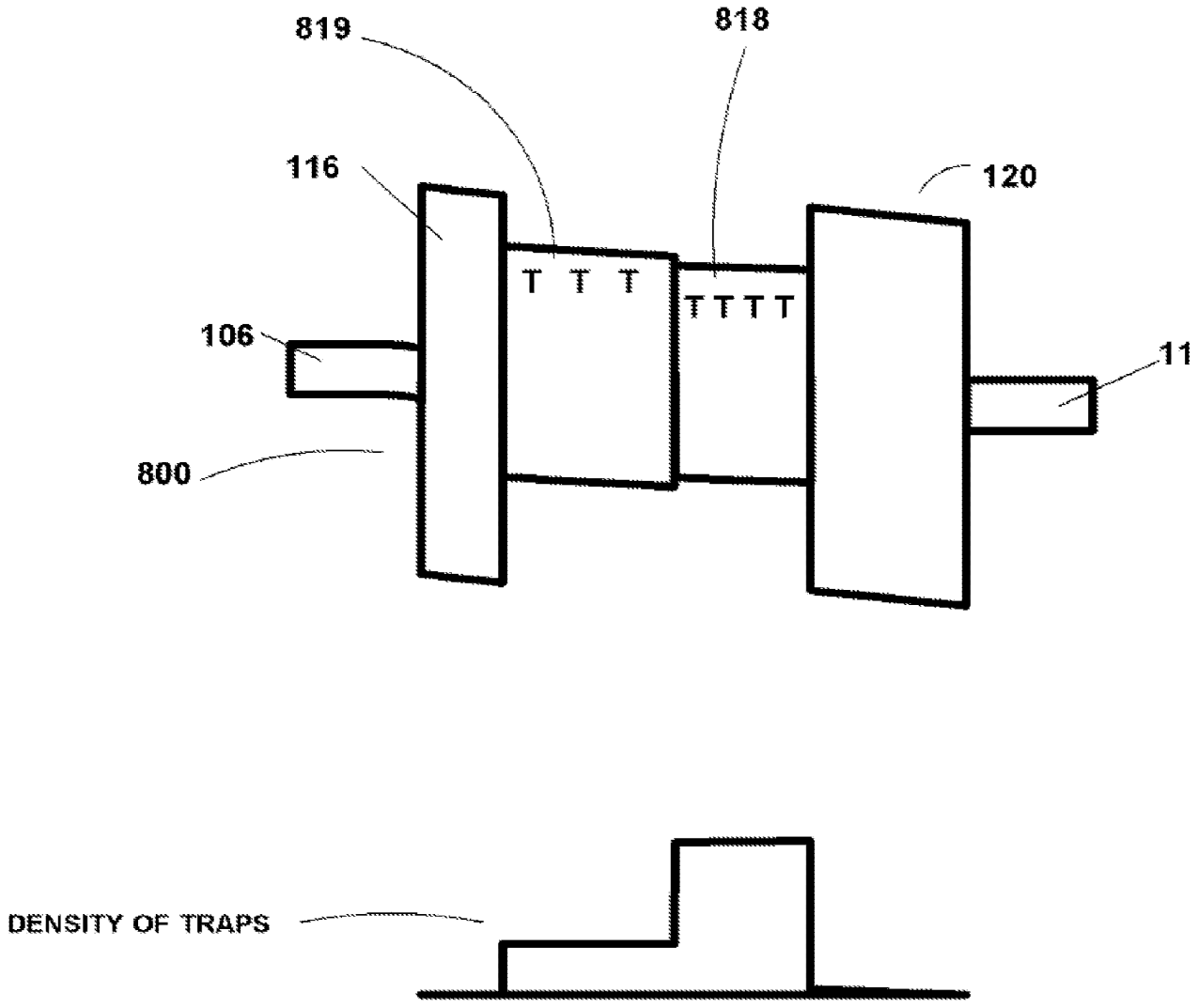


FIG. 7

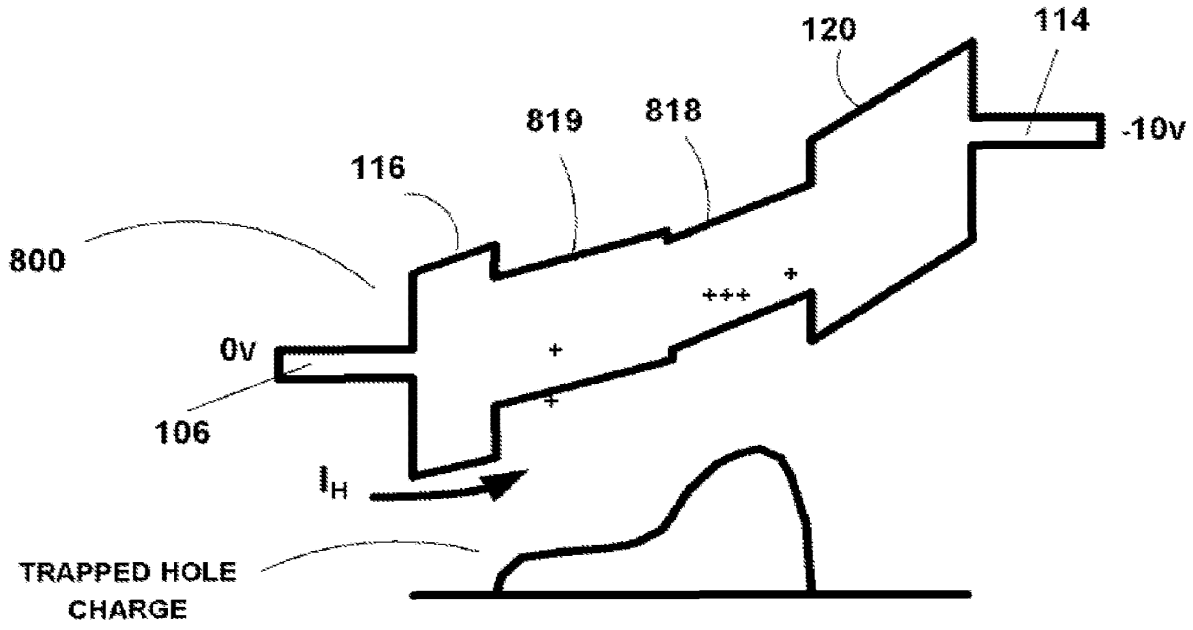


FIG. 8

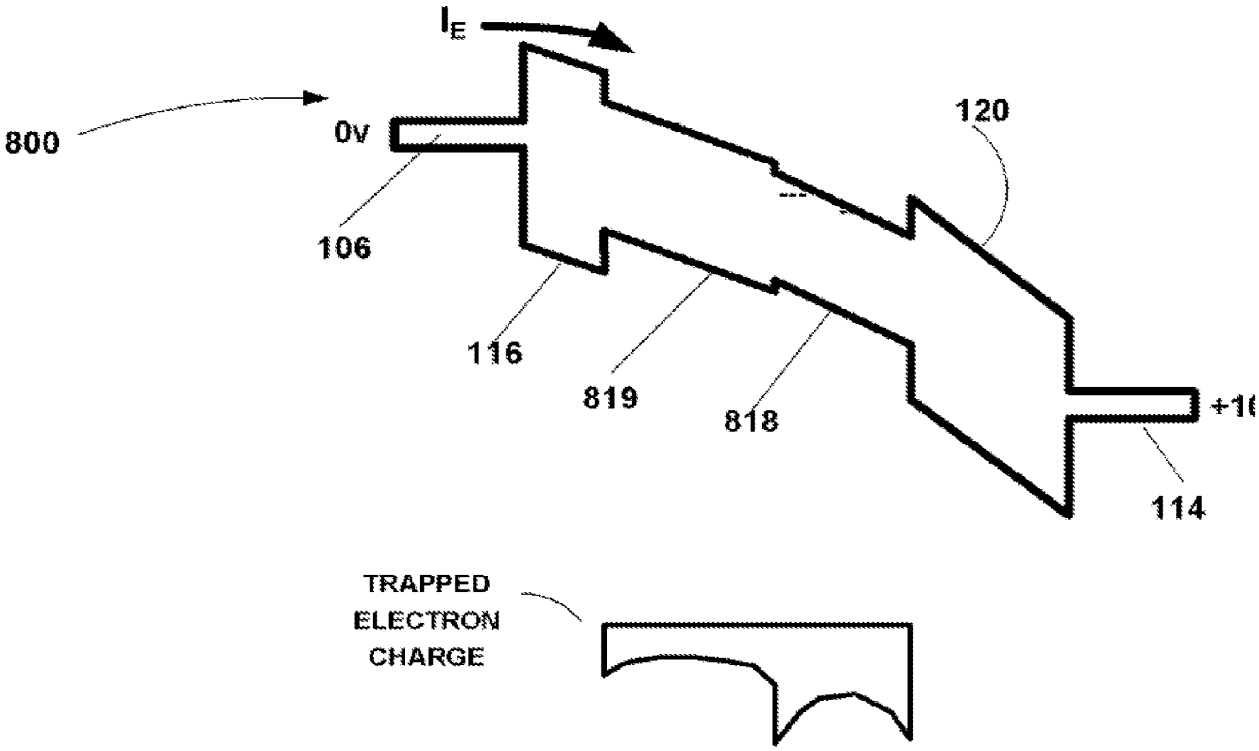


FIG. 9

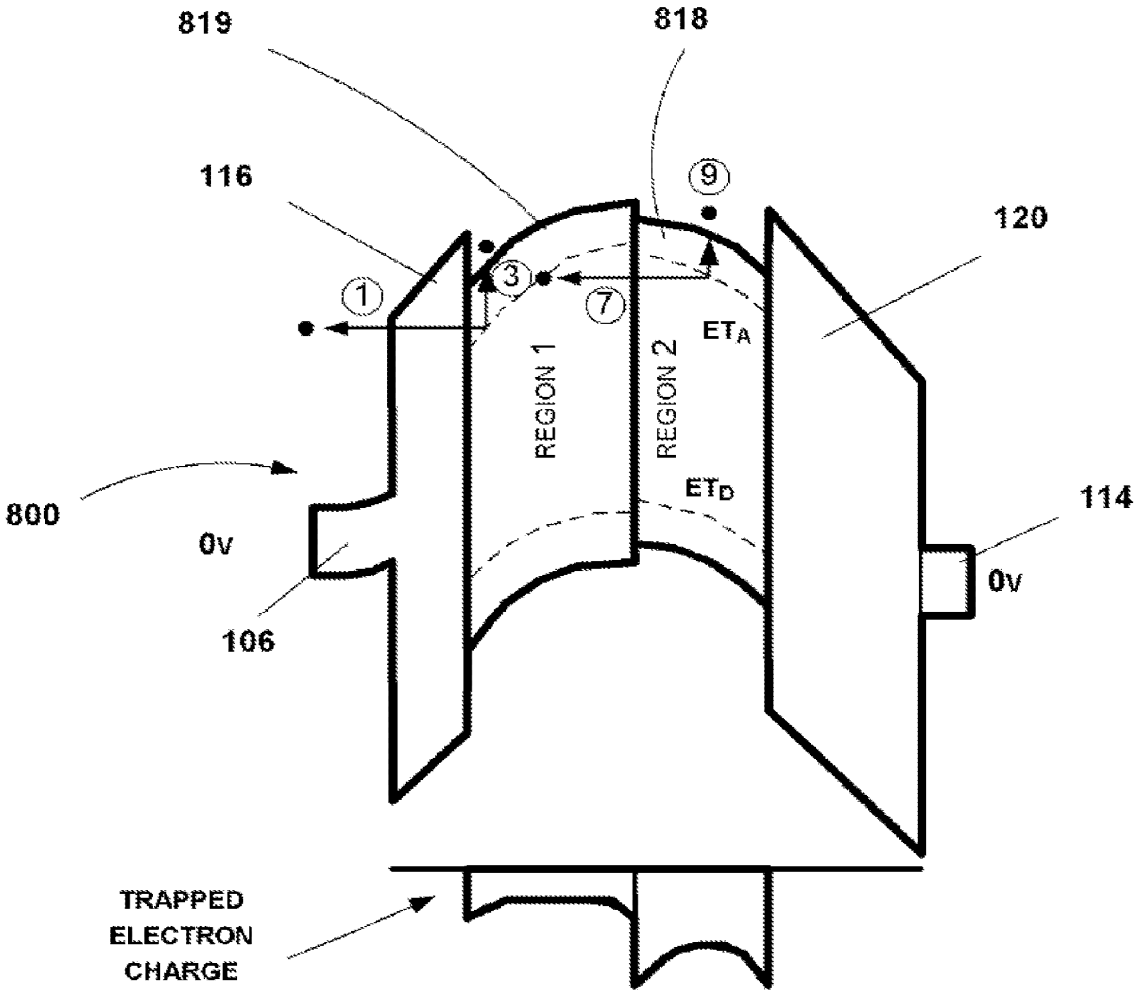

819
818
116
9
120
1
3
7
ETA
REGION 1
REGION 2
ETD
800
0V
114
0V
106
TRAPPED
ELECTRON
CHARGE

FIG. 10

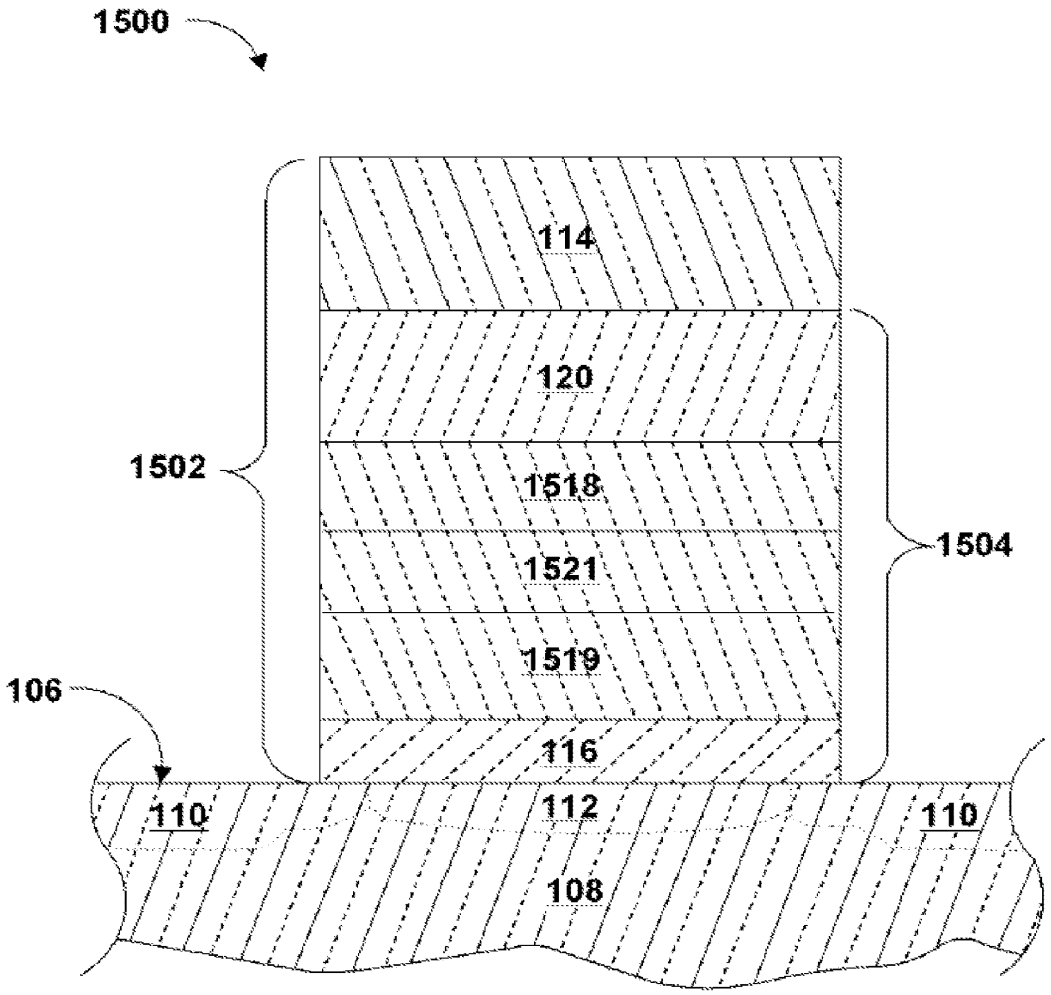


FIG. 11

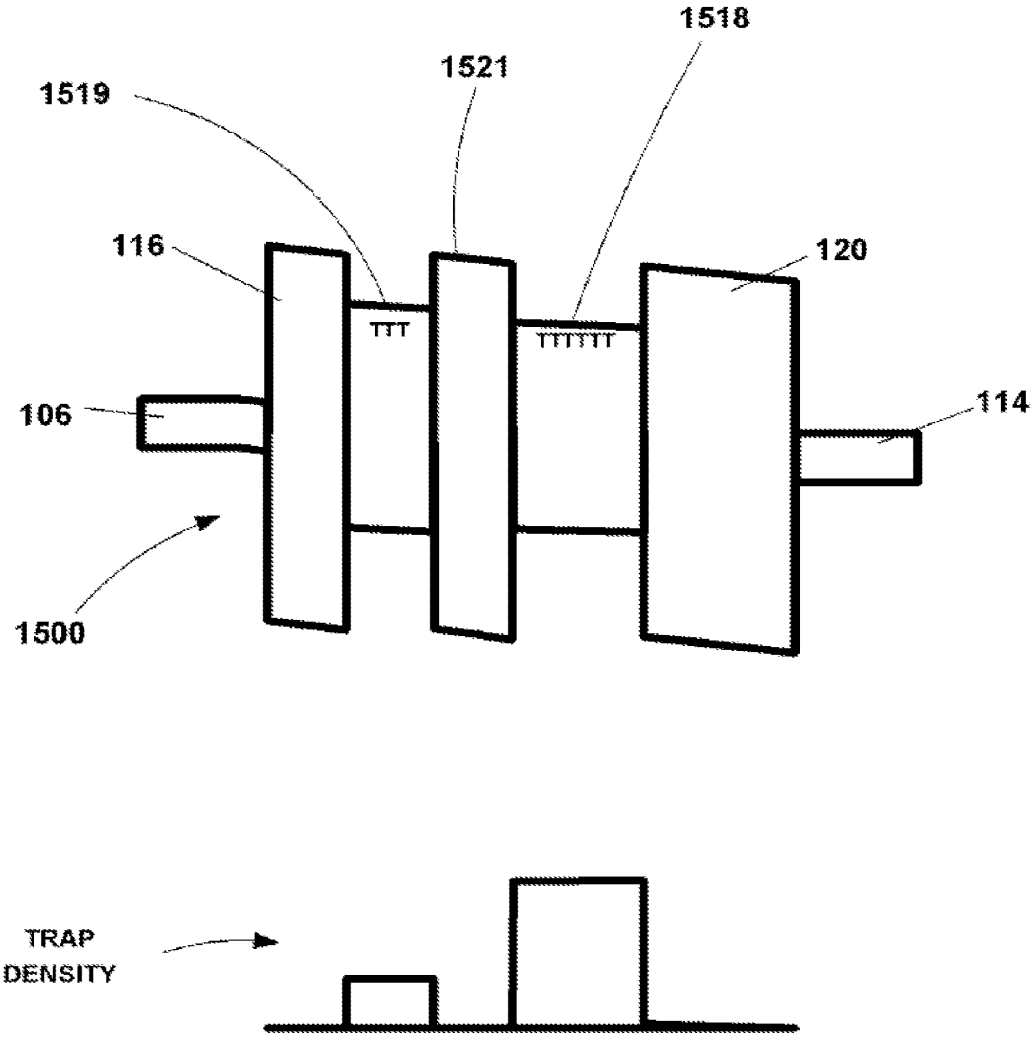


FIG. 12

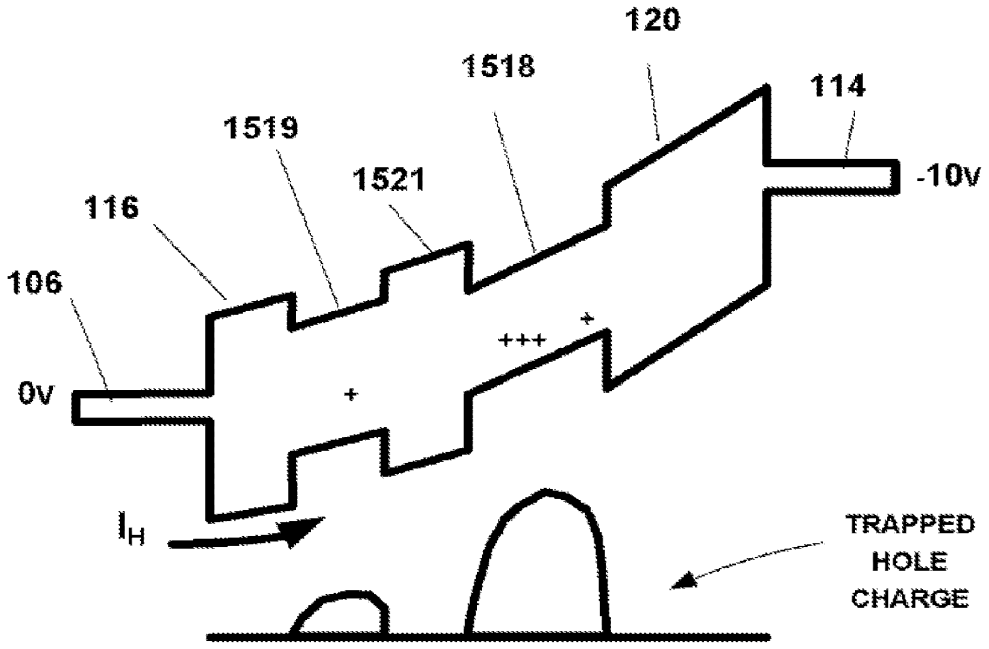


FIG. 13

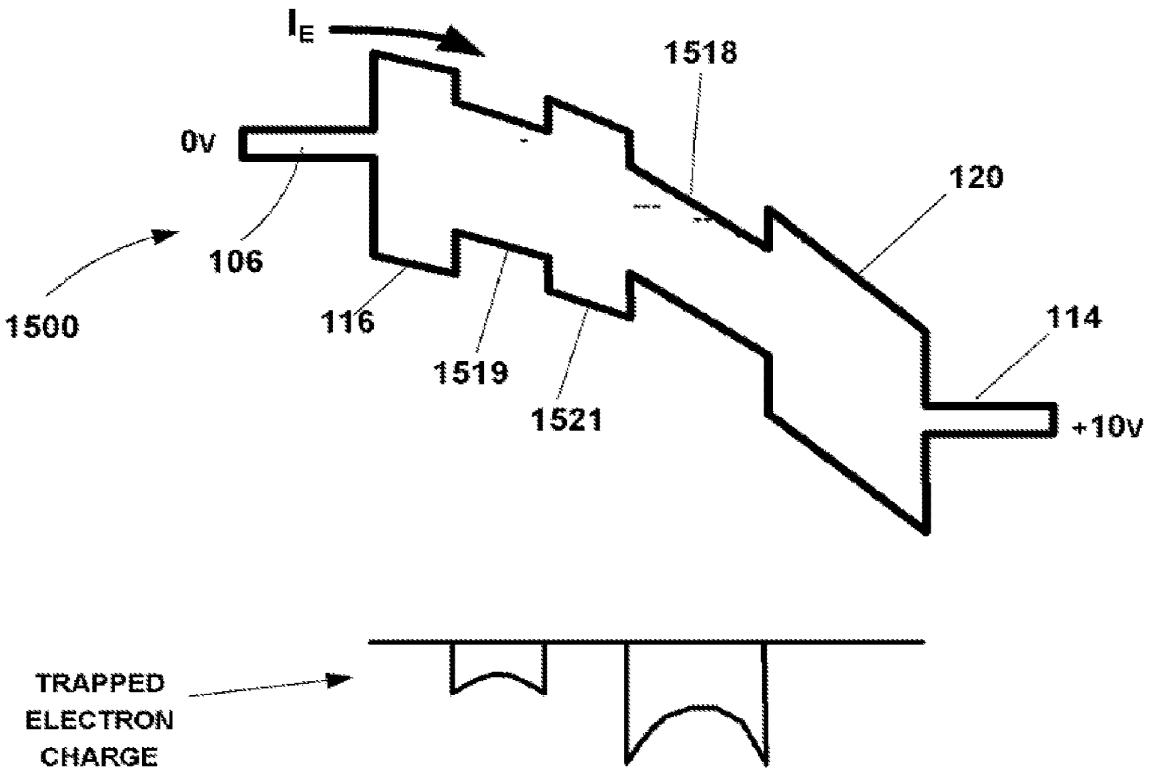

I_E
1518
0V
120
106
1500
116
114
1519
1521
+10V
TRAPPED
ELECTRON
CHARGE

FIG. 14

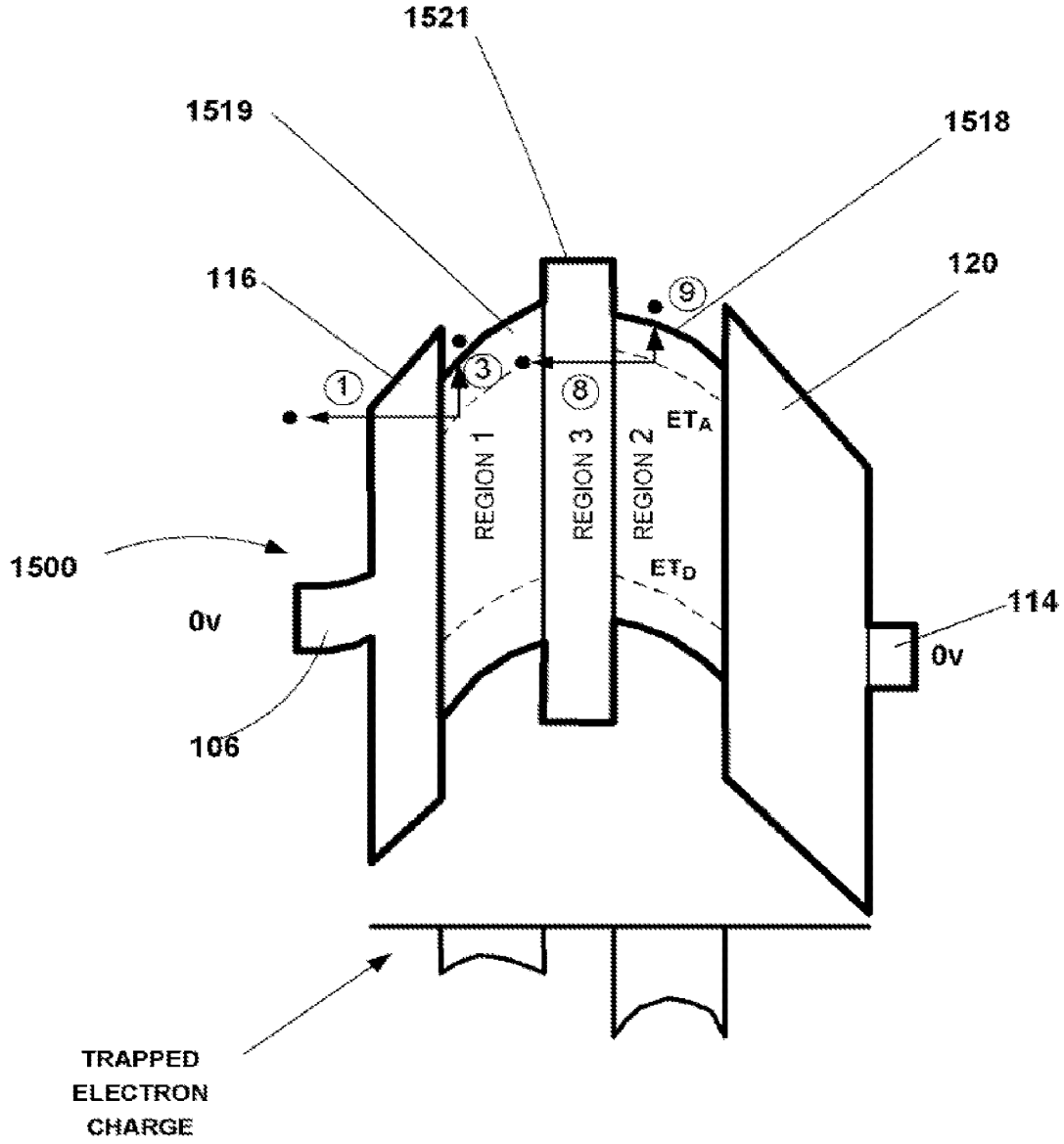

1521
1519
1518
116
120
9
3
1
8
REGION 1
REGION 3
REGION 2
ET_A
ET_D
1500
0v
114
0v
106
TRAPPED
ELECTRON
CHARGE

FIG. 15

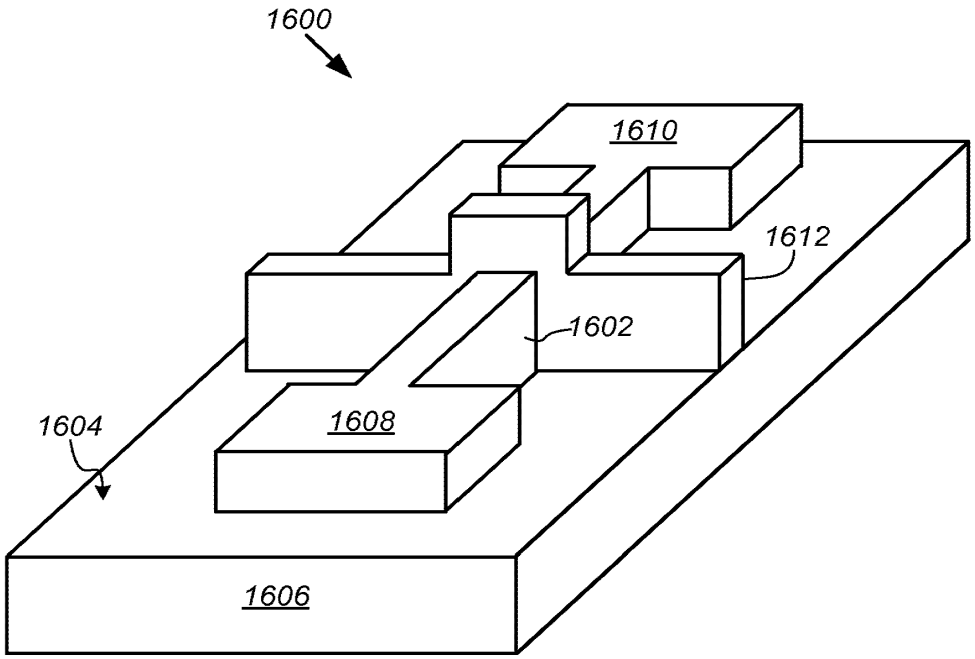


FIG. 16A

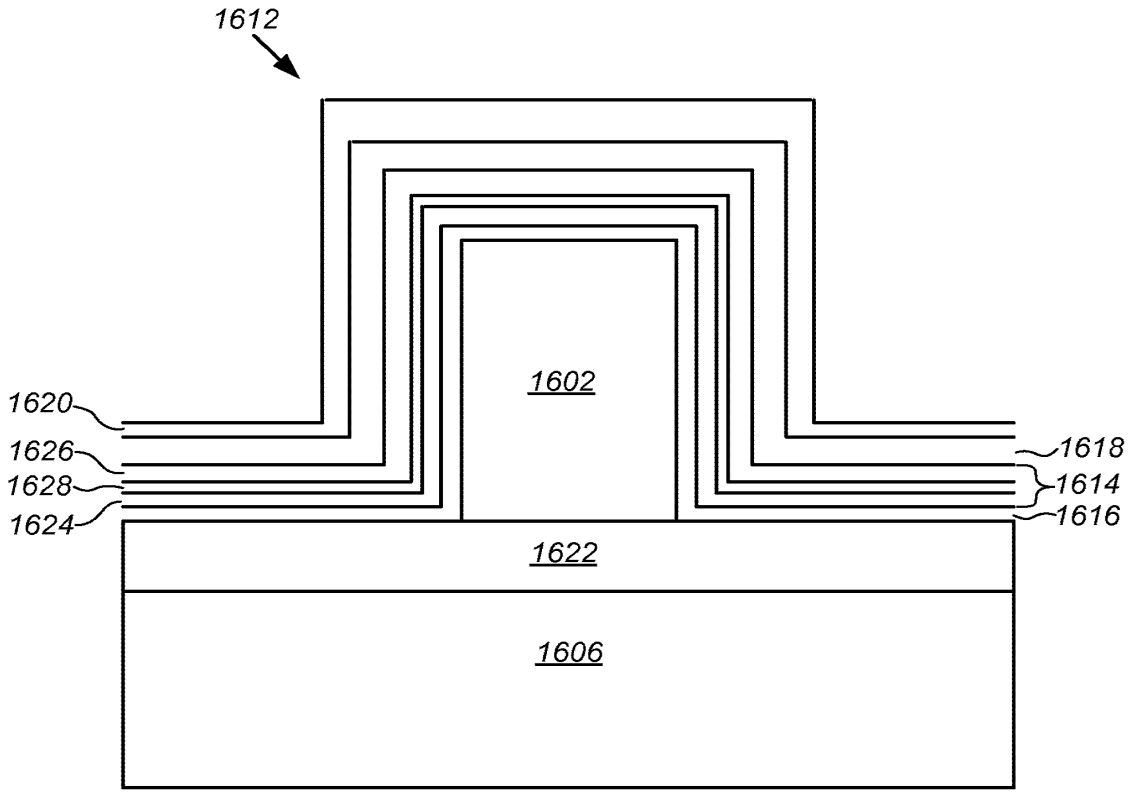


FIG. 16B

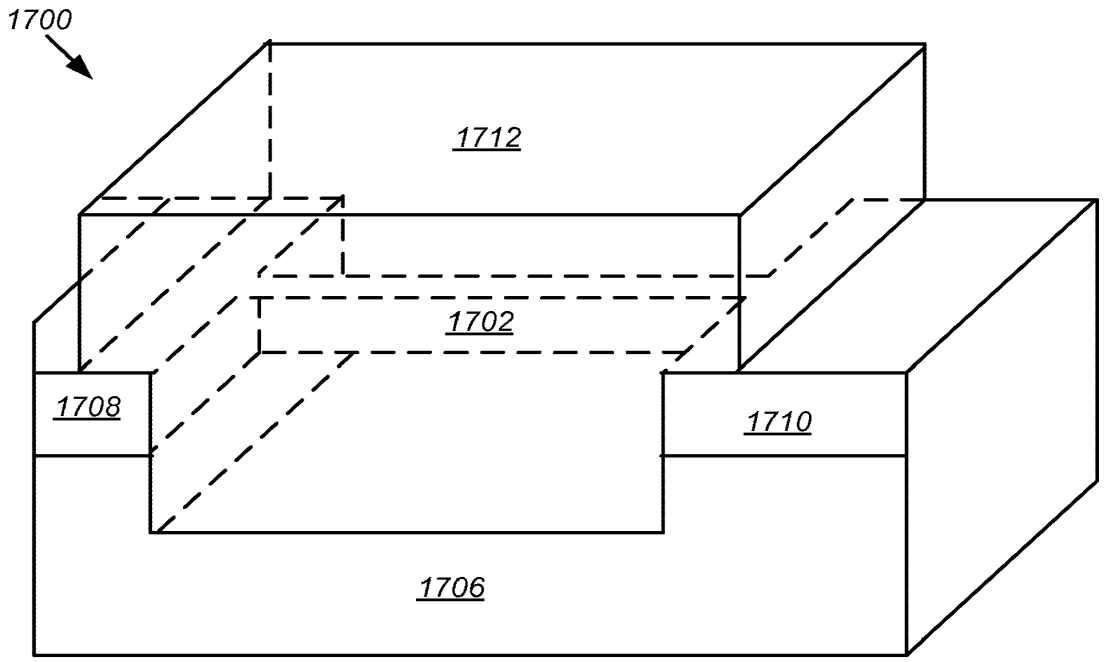


FIG. 17A

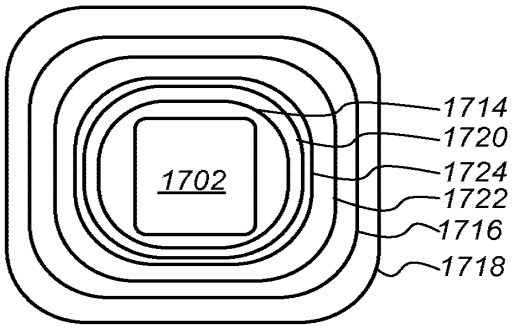


FIG. 17B

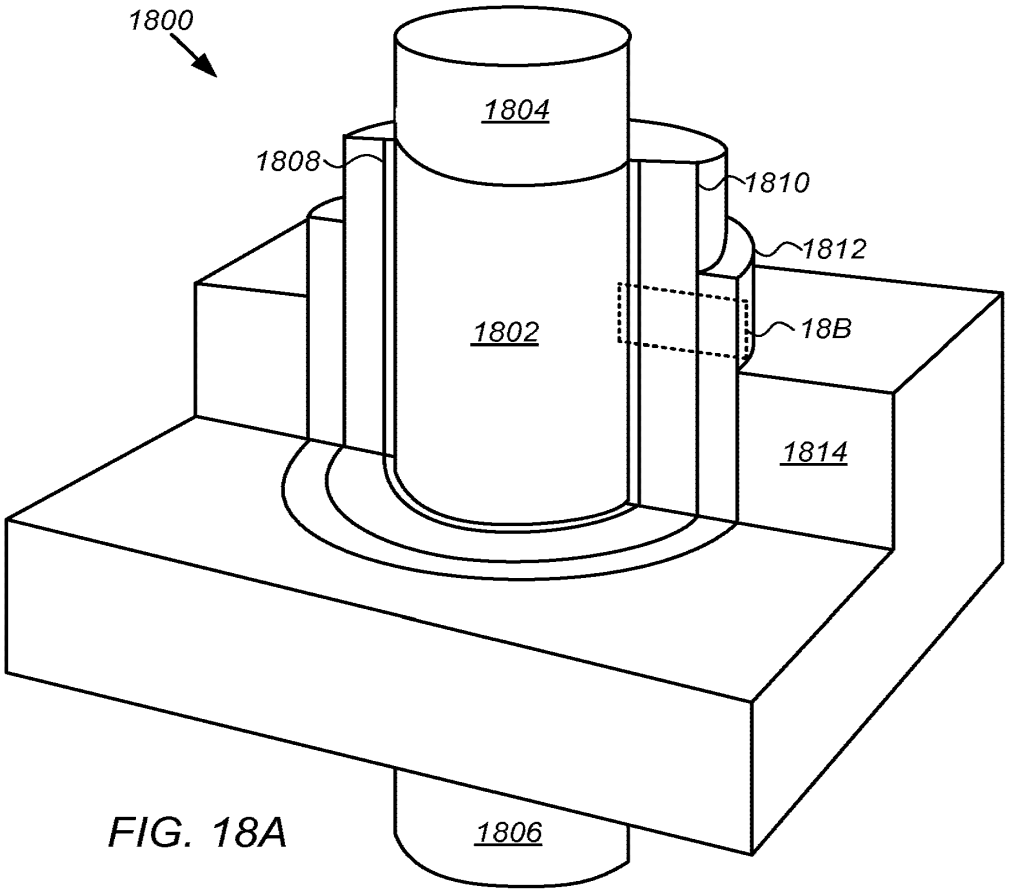


FIG. 18A

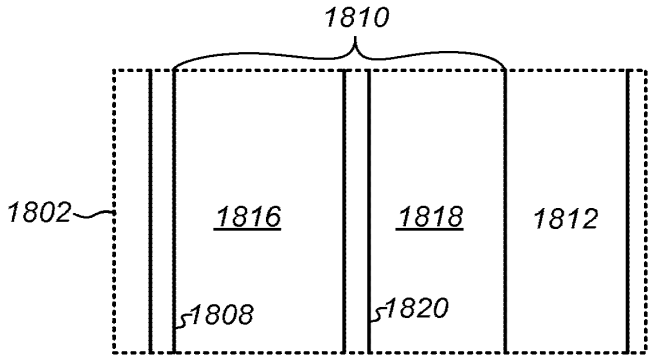


FIG. 18B

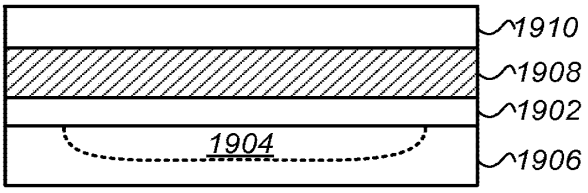


FIG. 19A

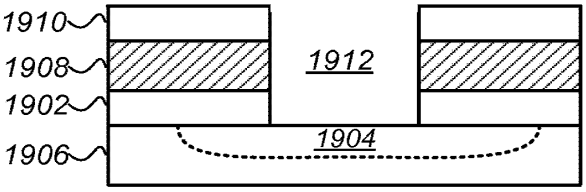


FIG. 19B

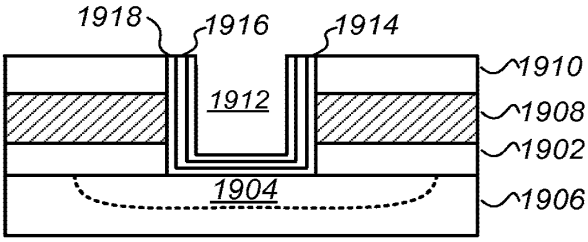


FIG. 19C

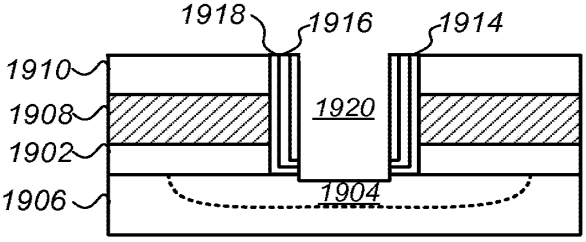


FIG. 19D

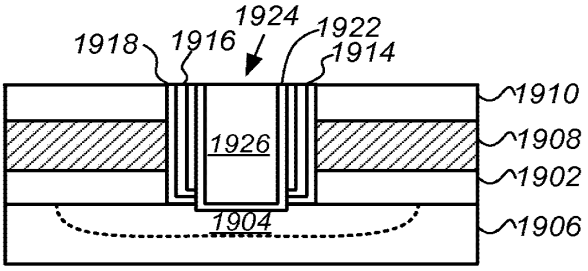


FIG. 19E

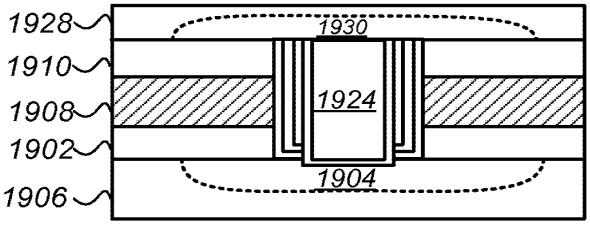


FIG. 19F

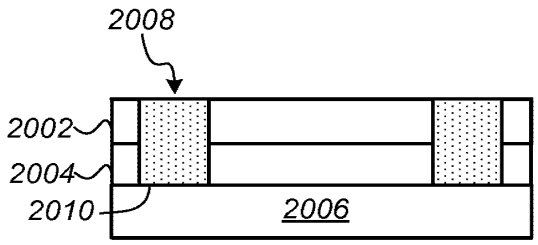


FIG. 20A

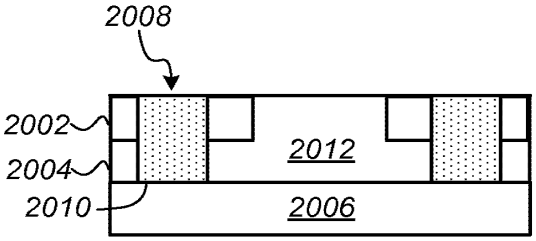


FIG. 20B

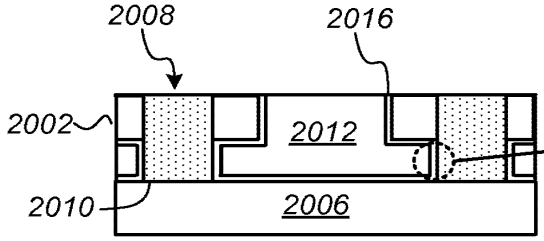


FIG. 20C

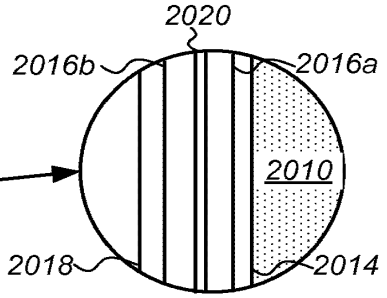


FIG. 20D

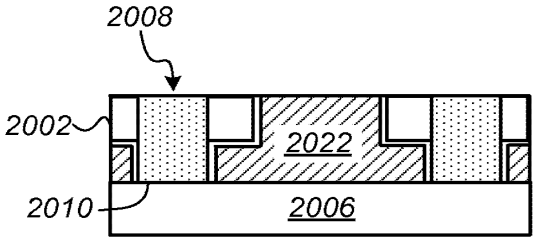


FIG. 20E

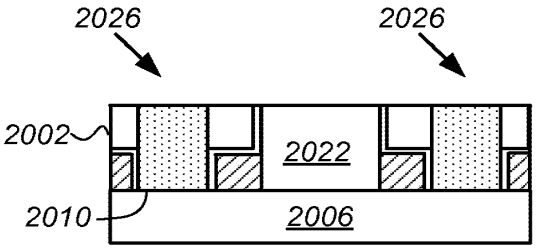


FIG. 20F

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US13/29784

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/792 (2013.01)
USPC - 438/591; 257/324, E29.308
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 29/792 (2013.01)
USPC - 438/920, 591; 257/321, 324, 325, E29.308, E29.309

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); Google Patents; Google Scholar; IP.COM, IEEE Xplore; Search Terms Used: Search Terms Used: non volatile memory, memory, NVM, charge trapping layers, SONOS, silicon oxynitride, tunneling layer, anti-tunneling layer, high K dielectric, thin film, nanowire*, FinFET, metal gate, nitrated oxide.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/0248332 A1 (LEVY S et al.) October 13, 2011, Figure 2, paragraphs [0022], [0025], [0045].	1-20
Y	US 7,999,295 B2 (LAI E et al.) August 16, 2011, column 3, lines 29 – 39, column 3, line 60 to column 4, line 4.	1-13, 15-17, 19, 20
Y	US 7,723,789 B2 (LIN H et al.) May 25, 2010, Figures 1A – 1H, column 2, line 63 to column 3, line 45.	7, 8, 11-18
Y	US 2009/0039414 A1 (LUE H et al.) February 12, 2009, Abstract.	4, 9, 13, 17, 18
Y	US 2009/0011609 A1 (RAMKUMAR K et al.) January 08, 2009, Figures 6E, 7A, paragraphs [0059] – [0065].	5

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
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WO2011162725A1 NANOWIRE TRANSISTOR AND METHOD FOR MANUFACTURING A NANOWIRE TRANSISTOR

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NANOWIRE TRANSISTOR AND METHOD FOR MANUFACTURING A NANOWIRE TRANSISTOR

Abstract

According to embodiments of the present invention, a nanowire transistor is provided. The nanowire transistor includes a carrier; a vertical nanowire structure extending from the carrier, the vertical nanowire structure comprising a channel region, and the vertical nanowire structure being made of the same material as the carrier; a gate insulator region covering at least a portion of the vertical nanowire structure; and at least one gate region covering at least a portion of the gate insulator region. In various embodiments, there is no doped junction between the channel region and the source/drain regions of the nanowire transistor.

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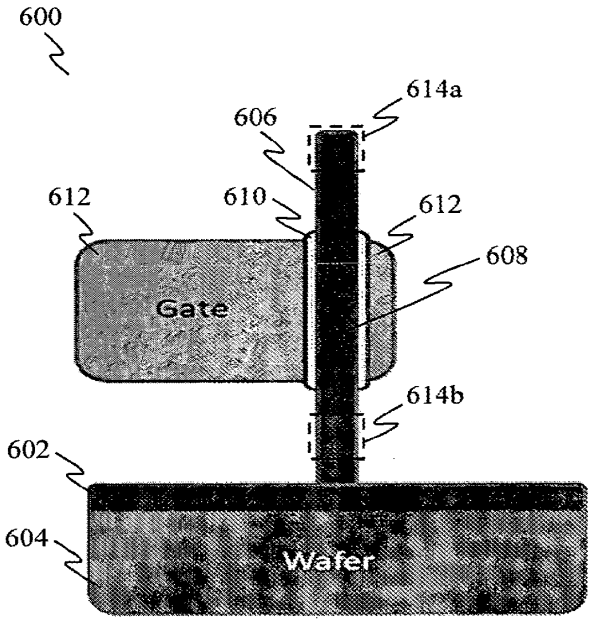


FIG. 6

(57) Abstract: According to embodiments of the present invention, a nanowire transistor is provided. The nanowire transistor includes a carrier; a vertical nanowire structure extending from the carrier, the vertical nanowire structure comprising a channel region, and the vertical nanowire structure being made of the same material as the carrier; a gate insulator region covering at least a portion of the vertical nanowire structure; and at least one gate region covering at least a portion of the gate insulator region. In various embodiments, there is no doped junction between the channel region and the source/drain regions of the nanowire transistor.

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NANOWIRE TRANSISTOR AND METHOD FOR MANUFACTURING A NANOWIRE TRANSISTOR

Cross-Reference To Related Application

[0001] This application claims the benefit of priority of Singapore patent application No. 201004576-3, filed 25 June 2010, the content of it being hereby incorporated by reference in its entirety for all purposes.

Technical Field

[0002] Various embodiments relate to a nanowire transistor and a method for manufacturing the nanowire transistor, a memory cell including the nanowire transistor and a method for manufacturing the memory cell, and a memory device including the memory cell.

Background

[0003] Feature size scaling in complementary metal oxide semiconductor (CMOS) technology has continued to follow Moore's law for more than the last forty years. Although the structure has remained planar, the CMOS device architecture has undergone many changes to sustain the scaling pace. Implementations of lightly doped drain (LDD), lateral non-uniformity in channel doping, reduction in junction depth, and vertical non uniformity in well doping including pocket and HALO implants are a few examples. In addition, the performance of scaled devices has been further improved by introducing stressors in the structure to improve the mobility (H.-S.P. Wong, "Beyond Conventional transistor", IBM J. Res. And Dev., vol. 46, no. 2/3, pp. 133-168, 2002; K.-W. Ang, J. Lin, C.-H. Tung,; N. Balasubramanian, G. S. Samudra, and Y.-C. Yeo, "Strained n-MOSFET with embedded source/drain stressors and strain-transfer structure (STS) for enhanced transistor performance", IEEE Transactions on Electron Devices, vol. 55, no. 3, pp. 850-857, March, 2008). Furthermore, the gate current leakage issue is tackled by (a) slowing

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down the scaling of the gate oxide thickness, and (b) by introduction of high-k materials in the gate dielectric (D. J. Frank, R.H. Dennard, E. Novak, P.M. Solomon, Y. Taur, H.-S.P.Wong, "Device Scaling Limits of Si MOSFETs and Their Application Dependencies", Proc. IEEE, Vol. 89, no. 3, p. 259, 2001.). Presently, 32 nm circuits with high-K and metal gates are in production.

[0004] The device scaling, however, appears to be reaching the end-of-the-technology roadmap. The major challenges being faced in further scaling are: (a) degraded gate electrostatic control of the channel potential leading to short-channel effects, such as threshold voltage roll-off, large drain induced barrier lowering (DIBL) and poor sub-threshold slope (SS), (b) increased gate and junction leakages, (c) reduced channel mobility, and (d) increased source drain (S/D) resistance. The increased doping in the channel which is needed to help the control of gate over the channel vis-à-vis that of source and drain terminals also leads to degraded performance. In addition, controlling junctions in MOS devices has become a challenging issue. As the junction depth decreases and doping increases with scaling, steeper junctions are required as scaling progresses.

[0005] The electrostatics of devices are improved in multiple-gate structures (L. Chang, Y-K. Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, C. Hu, T-J King, "Extremely Scaled Silicon Nano-CMOS", Proc. IEEE, Vol. 91, no. 11, p.1860, 2003) as the gate influences the channel potential from more than one-side and thus relaxes the demand on the doping. FIG. 1 shows a schematic cross-sectional view 100 of an evolution of multiple-gate transistors in order of increasing gate electrostatic control. The device structure progresses from single gated planar to fully gate-all-around nanowire MOSFETs.

[0006] The gate-all-around (GAA) structure appears to be the most resistant to short channel effects among all the emerging device structures for a given silicon body thickness. Simulations (E. Gnani, S. Reggiani, M. Rudan, and G. Baccarani, "Design considerations and comparative investigation of ultra-thin SOI, double-gate and cylindrical nanowire FETs", in IEEE ESSDERC Proceeding, 2006, pp. 371-374.) indicate that in cylindrical GAA architecture, the gate length can be scaled to 5 nm with the corresponding scaling of the intrinsic nanowire channel body. Further, the cylindrical geometry gives inverse logarithmic dependence of the gate capacitance on the channel

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diameter, and, thus, the gate length in these devices can be scaled with wire diameter without reducing the gate dielectric thickness.

[0007] However, GAA nanowire devices when fabricated on a lateral platform, suffer from practical challenges in defining shorter length wires due to the corner rounding effect in lithography. Gate uniformity and wire shape control are the other concerns. The device area scaling also follows the conventional scaling rule. In this regard, vertical wire devices are found more suitable than lateral. Nevertheless, controlling junctions in nanowire is even more challenging, and the impact of poor junction control on device performance and reliability can be significant.

[0008] SONOS memory cell uses standard MOS transistor as a base device. Fabricated on nanowires in a gate-all-around (GAA) configuration, SONOS cells have shown great performance with promises towards density improvement (Fu J, Singh N, Buddharaju KD, Teo SHG, Shen C, Jiang Y, Zhu CX, Yu MB, Lo GQ, Balasubramanian N, Kwong DL, Gnani E, Baccarani G, "Si-nanowire based gate-all-around nonvolatile SONOS memory cell", IEEE Electron Device Letters, Volume 29 Issue 5, pp 518-521, 2008). Besides better scalability, multi-bit storage and stacking of the cells have been reported using vertical nanowires/pillars (Sun Y, Yu HY, Singh N, Shen NS, Lo GQ, Kwong DL, "Multibit Programmable Flash Memory Realized on Vertical Si Nanowire Channel", IEEE Electron Device Letters, Volume 31 Issue 5, pp 390-392, 2010; Sun Y, Yu HY, Singh N, Leong KC, Gnani E, Baccarani G, Lo GQ, Kwong DL, "Vertical-Si-Nanowire-Based Nonvolatile Memory Devices With Improved Performance and Reduced Process Complexity", IEEE Transactions On Electron Devices, Volume 58 Issue 5, pp 1329-1335, 2011; Sun Y, Yu HY, Singh N, Leong KC, Lo GQ, Kwong DL, "Junctionless Vertical-Si-Nanowire-Channel-Based SONOS Memory With 2-Bit Storage per Cell", IEEE Electron Device Letters, Volume 32 Issue 6, pp 725-727, 2011). However, stacking of cells on vertical nanowire provide challenging issues, in particular the fabrication method when forming junctions on nanowires between the cells.

[0009] FIG. 2A shows a CMOS inverter logic 201 using a planar device, for example as represented by 200 for an n-gate device, while FIG. 2B shows a CMOS inverter logic 221 using a vertical wire device, for example a p-gate device 220a and an n-gate device 220b, for area comparison of the devices and the inverter logic to illustrate the scaling

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advantages of the devices based on vertical wire configuration. The parameter F is the minimum feature size or half pitch for the corresponding technology node.

[0010] The planar device CMOS inverter 201 includes a p-gate 202 coupled to a source 204 and a drain 206, and an n-gate 208 coupled to a source 210 and a drain 212. The vertical wire CMOS inverter 221 includes a p-gate device 220a with a p-gate 222 surrounding a part of the vertical wire, with the top part of the wire not covered by the gate 222 forming the source/drain 224, and an n-gate device 220b with an n-gate 226 surrounding a part of the vertical wire, with the top part of the wire not covered by the gate 224 forming the source/drain 228. While not shown in FIG. 2B, the bottom part of the respective wire of the p-gate device 220a and the n-gate device 220b are not covered by the p-gate 222 and the n-gate 226, thereby forming another respective source/drain.

[0011] For the CMOS inverter logic 201 using a planar device, the device area (e.g. of the n-gate device 200) is approximately $8F^2$ (i.e. $2F \times 4F$) while the inverter area is approximately $40F^2$ (i.e. $10F \times 4F$). For the CMOS inverter logic 221 using a vertical wire device, the device area (e.g. of the p-gate device 220a and the n-gate device 220b) is approximately $4F^2$ (i.e. $2F \times 2F$) while the inverter area is approximately $12F^2$ (i.e. $6F \times 2F$). The vertical wire device (e.g. the p-gate device 220a and the n-gate device 220b) of the CMOS inverter logic 221 occupies a device area that is approximately 50% of the device area occupied by the n-gate device 200 of the CMOS inverter logic 201. An even bigger advantage is in terms of the resulting circuits, e.g. a CMOS inverter can be fabricated in an area of approximately $12F^2$ using vertical wires against an area of approximately $40F^2$ in planar technology. It is assumed that device matching is accomplished through gate length, thus both n- and p-MOS occupy the same area.

[0012] As a result of smaller device/circuit area, the junction capacitances decrease with the area and ultimately the circuit speed is increased significantly. The inverter delay is expected to be reduced by ~6× compared to that of the planar device. Furthermore, the power consumption, $P = fCV^2$ (where f is frequency, C is capacitance and V is operating voltage) is also reduced by 60% of the planar devices.

[0013] Though excellent in term of electrostatic control, performance and scalability, forming junctions on nanowire devices, especially for vertical nanowire device is very challenging. One issue with vertical wire device is the non self aligned gate, as at least

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the bottom electrode implant cannot be aligned with the gate edge. This causes either higher parasitic overlap capacitance or higher extension resistance through under-lap.

[0014] FIGS. 3A to 3C explain possible issues due to non self aligned gate structure in vertical wire devices of the prior art. FIG. 3A shows a schematic of a vertical wire device 300 with the gate 302 aligned with the source and drain (e.g. 304a, 304b). FIG. 3B shows a schematic of a vertical wire device 320 with the gate 322 aligned with the top electrode (source/drain) 324a but under-lapped with the bottom electrode (source/drain) 324b, resulting in a higher parasitic resistance. FIG. 3C shows a schematic of a vertical wire device 340 with the gate 342 aligned with the top electrode (source/drain) 344a but overlapped with the bottom electrode 344b, resulting in a higher parasitic capacitance. The vertical wire devices 300, 320, 340, include an opposite polarity region 303, 323, 343, respectively. For example, the opposite polarity region 303 has a polarity that is opposite to that of the source and drain (e.g. 304a, 304b) and the gate 302. These opposite polarity regions 303, 323, 343, are called channels or channel regions, which are separated from their respective source and drain by junctions. The doping in the channel is of an opposite conductivity type to the source and drain. For example, an N-type device (NMOS) has an n-type source/drain (i.e. n-doped) but a p-type channel (i.e. p-doped). Generally, doping type of the gate follows that of the source/drain.

[0015] The vertical wire devices 300, 320, 340, further include a gate dielectric 306, 326, 346, respectively, which serves to electrically isolate the respective gate from the respective channel and source/drain regions. For example, in the vertical wire device 300, the gate dielectric 306 serves to electrically isolate the gate 302 from the channel 303 and the source/drain regions 304a, 304b.

Summary

[0016] According to an embodiment, a nanowire transistor is provided. The nanowire transistor may include a carrier; a vertical nanowire structure extending from the carrier, the vertical nanowire structure including a channel region, and the vertical nanowire structure being made of the same material as the carrier; a gate insulator region covering

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at least a portion of the vertical nanowire structure; and at least one gate region covering at least a portion of the gate insulator region.

[0017] According to an embodiment, a memory cell is provided. The memory cell may include a nanowire transistor as described above and wherein the gate insulator region includes a first dielectric layer configured to cover at least the portion of the vertical nanowire structure; a second dielectric layer; and a third dielectric layer, wherein the second dielectric layer is disposed between the first dielectric layer and the third dielectric layer, and wherein a bandgap of the second dielectric layer is smaller than a respective bandgap of the first dielectric layer and the third dielectric layer.

[0018] According to an embodiment, a memory device is provided. The memory device may include a memory cell as described above.

[0019] According to an embodiment, a method for manufacturing a nanowire transistor is provided. The method may include removing material from a carrier to form a vertical nanowire structure extending from the carrier; covering at least a portion of the vertical nanowire structure with a gate insulator material to form a gate insulator region; and covering at least a portion of the gate insulator region with a gate material to form at least one gate region.

[0020] According to an embodiment, a method for manufacturing a memory cell is provided. The method may include the method for manufacturing a nanowire transistor as described above, and wherein covering at least a portion of the vertical nanowire structure with the gate insulator material comprises forming a first dielectric layer to cover at least the portion of the vertical nanowire structure; forming a second dielectric layer; and forming a third dielectric layer, wherein the second dielectric layer is disposed between the first dielectric layer and the third dielectric layer, and wherein a bandgap of the second dielectric layer is smaller than a respective bandgap of the first dielectric layer and the third dielectric layer.

Brief Description of the Drawings

[0021] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis

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instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the invention are described with reference to the following drawings, in which:

[0022] FIG. 1 shows a schematic cross-sectional view of an evolution of multiple-gate transistors in order of increasing gate electrostatic control of the prior art.

[0023] FIGS. 2A and 2B show CMOS inverter logic using a planar device and a vertical wire device respectively of the prior art.

[0024] FIGS. 3A to 3C show possible issues due to non self aligned gate structure in vertical wire devices of the prior art.

[0025] FIG. 4A shows a schematic block diagram of a nanowire transistor, according to various embodiments.

[0026] FIG. 4B shows a schematic block diagram of a nanowire transistor, according to various embodiments.

[0027] FIG. 4C shows a schematic block diagram of a memory cell, according to various embodiments.

[0028] FIG. 5 shows a flow chart illustrating a method for manufacturing a nanowire transistor, according to various embodiments.

[0029] FIG. 6 shows a schematic cross sectional view of a nanowire transistor, according to various embodiments.

[0030] FIG. 7 shows a schematic cross-sectional view of a fabrication process for manufacturing a nanowire transistor, according to various embodiments.

[0031] FIG. 8 shows scanning electron microscope (SEM) images of structures formed during a fabrication process for manufacturing a nanowire transistor, according to various embodiments. The width of each image is about 1 μm.

[0032] FIG. 9 shows a transmission electron microscope (TEM) image of a nanowire transistor, according to various embodiments.

[0033] FIG. 10A shows a plot of drain current-gate voltage (I_d-V_g) characteristics of a nanowire transistor, for different drain voltages (V_d), according to various embodiments.

[0034] FIG. 10B shows a plot of drain current-drain voltage (I_d-V_d) characteristics of a nanowire transistor, for different gate voltages (V_g), according to various embodiments.

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[0035] FIGS. 11A and 11B show cross-sectional transmission electron microscope (TEM) images respectively of a vertical silicon nanowire gate-all-around junction-less SONOS and an oxide-nitride-oxide (ONO) gate stack, according to various embodiments.

[0036] FIG. 12 shows a plot of drain current-gate voltage (I_d-V_g) characteristics of a junction-less SONOS of various embodiments and a junction-based SONOS.

[0037] FIG. 13 shows a plot of drain current-gate voltage (I_d-V_g) characteristics of junction-less SONOS with different nanowire diameters, according to various embodiments.

[0038] FIG. 14 shows a plot of drain current-gate voltage (I_d-V_g) characteristics of junction-less SONOS with different channel doping concentrations, according to various embodiments.

[0039] FIG. 15 shows plots of simulated electric field distributions of junction-less SONOS for different nanowire diameters, according to various embodiments.

[0040] FIG. 16 shows plots of simulated electric field distributions of junction-less SONOS for different channel doping concentrations, according to various embodiments.

[0041] FIGS. 17A and 17B show plots of programming characteristics of junction-less SONOS memory cells for different gate voltages, according to various embodiments.

[0042] FIG. 17C shows a plot of programming characteristics of a junction-based SONOS memory cell for different gate voltages.

[0043] FIGS. 18A and 18B show plots of erasing characteristics of junction-less SONOS memory cells for different gate voltages, according to various embodiments.

[0044] FIG. 18C shows a plot of erasing characteristics of a junction-based SONOS memory cell for different gate voltages.

[0045] FIG. 19 shows a plot of programming/erasing (P/E) speed of junction-less SONOS memory cells for different nanowire diameters, according to various embodiments.

[0046] FIG. 20 shows a plot of multi-bit programming characteristics of a junction-less SONOS memory cell, according to various embodiments.

[0047] FIG. 21A shows a plot of retention characteristics at 85°C for junction-less SONOS memory cells of various embodiments and a junction-based SONOS memory cell.

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[0048] FIG. 21B shows a plot of endurance characteristics at 85°C for junction-less SONOS memory cells of various embodiments and a junction-based SONOS memory cell.

[0049] FIG. 22A shows a schematic cross-sectional view of a 3-D memory device based on vertical junction-less silicon nanowire SONOS memory cells, according to various embodiments.

[0050] FIG. 22B shows a schematic of an equivalent circuit for the embodiment of FIG. 22A.

Detailed Description

[0051] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[0052] Various embodiments provide a semiconductor nanowire device and a method for manufacturing the same. In particular, various embodiments may provide a vertical nanowire device and a method for manufacturing the same.

[0053] Various embodiments may provide a vertical nanowire device (e.g. a vertical nanowire transistor) free of any junction and a method of fabricating the same, which is simple and involves fewer processes. The vertical nanowire device may include a gate-all-around (GAA) wire architecture for improved control of short channel effects (SCE), a vertical architecture for improved size scaling per device/circuit and reduced power, and a junction-less architecture so that the device may be free from challenges associated with junction control and non-self aligned gate in the vertical architecture. Various embodiments may provide self-aligned vertical wire GAA transistors or devices. In the context of various embodiments, the term "self-aligned" as applied to a junction-less

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device, may mean that the junction-less device behaves like a self-aligned device, as there are no doped junctions.

[0054] Various embodiments may provide a junction-less vertical nanowire device (e.g. a junction-less vertical nanowire transistor) that is free of any physical or chemical junction (e.g. a p-n junction), as the junction-less vertical nanowire device is based on electrical doping.

[0055] The junction-less nanowire transistors of various embodiments may also provide a self-aligned gate with the source/drain regions when the transistors or devices are in operation, thereby providing self-aligned "junctions". In various embodiments, the gate is self-aligned as different regions, for example the channel, source and drain regions, are formed electrically rather than by doping. In various embodiments, the channel may be formed electrically by removing the depletion, thereby creating carriers in the nanowire region under the gate. In contrast, in a conventional transistor (e.g. a transistor with junctions), depletion is formed, followed by inversion, in order to create the channel.

[0056] During operation of the junction-less nanowire transistors of various embodiments, in the ON state, at least substantially the entire body of the nanowire functions as the channel or channel region in contrast to a surface channel for a junction-based nanowire device or transistor, while in the OFF state, the channel in the junction-less nanowire transistor is depleted using the gate work function.

[0057] Various embodiments may provide vertical nanowire devices (e.g. a vertical nanowire transistors), for example a gate-all-around (GAA) junction-less MOSFETs using CMOS compatible technology, based on vertical silicon nanowires having diameters of approximately 100 nm or less (i.e. $\leq$ 100 nm), for example between about 5 nm to about 80 nm, between about 20 nm to about 60 nm or about 40 nm to about 50 nm. The device of various embodiments may be more symmetric, with minimal or no overlap parasitic capacitance, with minimal or no under-lap parasitic resistance, more reliable and provide improved performances, compared to conventional (junction-based) vertical nanowire MOSFETs. In addition, various embodiments may provide a more efficient and cost-effective method for fabricating highly scalable and high-performance transistors.

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[0058] Various embodiments may provide highly scalable single crystalline silicon channels based on silicon nanowires (with nanowire diameters down to sub-20 nm) with thermally grown oxide on the silicon nanowires, for use in forming memory devices. This may alleviate or minimize any reliability issues, such as sub-threshold swing, leakage, threshold voltage Vt distribution and data retention.

[0059] Various embodiments may provide a channel region or channel length of approximately 200 nm or less (i.e. ≤ 200 nm), for example between about 50 nm to about 180 nm, between about 100 nm to about 150 nm or about 100 nm to about 200 nm.

[0060] Various embodiments may provide a high-k dielectric/metal gate stack, where the parameter k refers to dielectric constant.

[0061] The nanowire transistors of various embodiments may offer a wider effective channel volume, higher density, lower power consumption, higher speed, with a larger turn-on current I_{on}, and better electrostatic control, and may be fabricated on bulk wafers (e.g. bulk silicon wafer) and SOI wafers, thereby providing a low-cost approach. In addition, there is better process control as the transistors may be functionalized on nanowires with width greater than the thickness of the SOI substrate needed for lateral junction-less tri-gate devices. Furthermore, the nanowire transistors may offer a chemically simpler structure.

[0062] Various embodiments may provide a nanowire transistor that may be vertically stacked, for example for memory applications. The stacked memory may have a plurality of cells per wire, e.g. 4 physical cells per wire.

[0063] Various embodiments may also provide a high performance GAA junction-less, vertical silicon nanowire-based, silicon-oxide-nitride-oxide-silicon (SONOS) memory, for example for three dimensional (3-D) (e.g. 3-D multi-level integration) ultra-high density applications. The GAA nanowire architecture may be used for SONOS type non-volatile memory applications where the gate dielectric has to be necessarily thicker, as the gate length in the devices with the GAA nanowire architecture may be scaled with wire diameter without reducing the gate dielectric thickness.

[0064] The vertical nanowire-based junction-less SONOS memory or memory cells of various embodiments may be stacked vertically, and involve simple fabrication method, with less manufacturing cost. Various embodiments of the junction-less SONOS memory

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realized on vertical silicon nanowire GAA channel may have full memory functionality, for example for nanowire diameters down to about 20 nm, and having a high I_{on}/I_{off} ratio (e.g. up to approximately 1×10^8) and a more robust thermal budget tolerance.

[0065] Various embodiments may provide a scalable architecture, in the form of GAA nanowire devices, which may be provided to replace planar CMOS at the 22 nm technology node and below, for example for logic and memory circuits and applications.

[0066] In order that the invention may be readily understood and put into practical effect, particular embodiments will now be described by way of examples and not limitations, and with reference to the figures.

[0067] FIG. 4A shows a schematic block diagram of a nanowire transistor 400, according to various embodiments. The nanowire transistor 400 includes a carrier 402, a vertical nanowire structure 404 extending from the carrier 402, the vertical nanowire structure 404 comprising a channel region 406, and the vertical nanowire structure 404 being made of the same material as the carrier 402, a gate insulator region 408 covering at least a portion of the vertical nanowire structure 404, and at least one gate region 410 covering at least a portion of the gate insulator region 408. In various embodiments, the carrier 402, the vertical nanowire structure 404 and the channel region 406 may form a continuous structure.

[0068] In various embodiments, the gate insulator region 408 surrounds at least the portion of the vertical nanowire structure 404, and the at least one gate region 410 surrounds at least the portion of the gate insulator region 408.

[0069] FIG. 4B shows a schematic block diagram of a nanowire transistor 420, according to various embodiments. The nanowire transistor 420 may include elements of the embodiment of the nanowire transistor 400 of FIG. 4A.

[0070] The nanowire transistor 420 may further include an insulator material 424 covering at least a portion of a base of the vertical nanowire structure 404. The term "base" may mean a bottom part or a portion near the bottom part of the vertical nanowire structure 404, proximal to the carrier 402. In various embodiments, the same insulator may be used with the transistor 400.

[0071] In various embodiments, the insulator material 424 may be an oxide or a nitride. The oxide may be any oxide (e.g. silicon dioxide), for example deposited using plasma-

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enhanced chemical vapor deposition (PECVD), low-pressure chemical vapor deposition (LPCVD) or high-density plasma (HDP). In various embodiments, the insulator material 424 may be a PECVD low-k dielectic layer such as black diamond, or a spin coat layer of a low-k dielectric such as silk.

[0072] In various embodiments, the channel region 406 and the carrier 402 may be doped with doping atoms 426 of a conductivity type. In other words, the channel region 406 and the carrier 402 may be doped with doping atoms 426 of the same conductivity type.

[0073] The nanowire transistor 420 may further include a first source/drain region 428 coupled to the channel region 406, and a second source/drain region 430 coupled to the carrier 402, wherein the first source/drain region 428 and the second source/drain region 430 are doped with doping atoms 426 of the same conductivity type as the channel region 406. In other words, the carrier 402, the channel region 406, the first source/drain region 428 and the second source/drain region 430 may be doped with doping atoms 426 of the same conductivity type.

[0074] In various embodiments, the first source/drain region 428 may be formed from a portion of the vertical nanowire structure 404, e.g. a top portion or a tip of the vertical nanowire structure 404, or the first source/drain region 428 may be part of the vertical nanowire structure 404, for example at a position distal from the carrier 402.

[0075] In various embodiments, the second source/drain region 430 may be formed from a portion of the carrier 402, or the second source/drain region 430 may be part of the carrier 402. In various embodiments, the second source/drain region 430 may be formed from a portion of the vertical nanowire structure 404, or may be part of the vertical nanowire structure 404, for example at a position proximal to the carrier 402, for example at the base of the vertical nanowire structure 404.

[0076] In various embodiments, the vertical nanowire structure 404, the channel region 406 and the first source/drain region 428 may form a continuous structure. In various embodiments, the carrier 402 and the second source/drain region 430 may form a continuous structure.

[0077] In various embodiments, the carrier 402, the vertical nanowire structure 404, the channel region 406, the first source/drain region 428 and the second source/drain region 430 may form a continuous structure.

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[0078] The nanowire transistor 420 may further include an isolation oxide 432 disposed between the at least one gate region 410 and at least one of the first source/drain region 428 and the second source/drain region 430. The isolation oxide 432 may be a HDP, PECVD or LPCVD oxide.

[0079] In various embodiments, the channel region 406 is free of a junction (i.e. the channel region 406 is not isolated from the first source/drain region 428 and the second source/drain region 430 with a respective junction), such as a p-n junction.

[0080] In various embodiments, the gate insulator region 408 includes a gate oxide, such as silicon oxide.

[0081] Various embodiments may also provide a memory cell including a nanowire transistor of the embodiments of FIGS. 4A or 4B. In various embodiments, the memory cell may include a plurality of the nanowire transistors. In various embodiments, the data storage in the memory cell may be in the form of discrete change trapping inside the gate dielectric (e.g. the gate insulator material) or by incorporating a floating gate.

[0082] Various embodiments may further provide a memory device including a memory cell, the memory cell including one or more nanowire transistors of the embodiments of FIGS. 4A or 4B. In various embodiments, the memory device may include a plurality of memory cells. The plurality of memory cells may be formed on the same nanowire transistor.

[0083] FIG. 4C shows a schematic block diagram of a memory cell 440, according to various embodiments. The memory cell 440 may include elements of the embodiments of the nanowire transistor 400 of FIG. 4A and/or the nanowire transistor 420 of FIG. 4B. In the memory cell 440, the gate insulator region 408 includes a first dielectric layer 442a configured to cover at least the portion of the vertical nanowire structure 404, a second dielectric layer 442b, and a third dielectric layer 442c, wherein the second dielectric layer 442b is disposed between the first dielectric layer 442a and the third dielectric layer 442c, and wherein a bandgap of the second dielectric layer 442b is smaller than a respective bandgap of the first dielectric layer 442a and the third dielectric layer 442c.

[0084] In the context of various embodiments, all of the first dielectric layer 442a, the second dielectric layer 442b, and the third dielectric layer 442c may not be of the same material. In the context of various embodiments, the second dielectric layer 442b is of a

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material with a lower bandgap than the material of the first dielectric layer 442a and the third dielectric layer 442c in order to maintain the charges trapped inside the well of the gate insulator material created by the differences in the bandgaps among the three dielectric layers. In various embodiments, the first dielectric layer 442a and the third dielectric layer 442c may be of the same material.

[0085] In various embodiments, each of the first dielectric layer 442a and the third dielectric layer 442c includes an oxide, for example silicon oxide (SiO_2), aluminium oxide (Al_2O_3) or hafnium oxide (HfO_2), or any high-k dielectric material.

[0086] In various embodiments, the second dielectric layer 442b includes a material selected from the group consisting of a nitride (e.g. silicon nitride), an oxide (e.g. aluminium oxide or hafnium oxide), polycrystalline silicon (i.e. polysilicon), amorphous silicon and a metal. However, it should be appreciated that the second dielectric layer 442b may include any high-k dielectric material.

[0087] In various embodiments, each of the first dielectric layer 442a, the second dielectric layer 442b and the third dielectric layer 442c are of high-k dielectric materials or only the second dielectric layer 442b is of a high-k dielectric material.

[0088] In the context of various embodiments, where the second dielectric layer 442b includes a continuous layer of polysilicon, a continuous layer of amorphous silicon or a continuous layer of a metal, the memory cell 440 may be a floating gate memory.

[0089] In various embodiments, where the second dielectric layer 442b includes a nitride, the nitride dielectric layer may be configured to store charges and the memory cell 440 may be a non-volatile memory cell.

[0090] In various embodiments, the second dielectric layer 442b may include nanocrystals, for example polysilicon nanocrystals, germanium nanocrystals or metal nanocrystals. In various embodiments, the entire second dielectric layer 442b may be made up of the nanocrystals or the second dielectric layer 442b may include the nanocrystals on a surface of the second dielectric layer 442b.

[0091] In the context of various embodiments, where the second dielectric layer 442b includes nanocrystals, the second dielectric layer 442b may be used for discrete charge trapping and the memory cell 440 may be a nanocrystal memory.

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[0092] Various embodiments may provide a memory device including a memory cell. The memory cell may be of the embodiment of FIG. 4C. In various embodiments, the memory device may further include a nanowire transistor of the embodiments of FIG 4A or 4B, wherein the nanowire transistor may be configured to couple to the memory cell. In various embodiments, the memory cell and the nanowire transistor may be provided on the same level, for example side by side, on the same carrier, with their own respective vertical nanowire structure. In various embodiments, the memory cell and the nanowire transistor may be provided on one continuous vertical nanowire structure. In other words, the memory cell and the nanowire transistor may share one common continuous vertical nanowire structure.

[0093] In various embodiments of the memory device, the memory cell may be arranged over the nanowire transistor (e.g. in a vertical stack), and the respective vertical nanowire structure of the memory cell and the nanowire transistor is the same vertical nanowire structure (i.e. the memory cell and the nanowire transistor share one common continuous vertical nanowire structure), and the respective carrier of the memory cell and the nanowire transistor is the same carrier (i.e. the memory cell and the nanowire transistor are formed on a common carrier.

[0094] In various embodiments, the memory device may include a second memory cell, wherein the memory cell and the second memory cell may be arranged one over the other on the same vertical nanowire structure, for example in a vertical stack.

[0095] In various embodiments, the memory device may include a plurality of the memory cells, where at least two of the plurality of memory cells are arranged one over the other (e.g. in a vertical arrangement or a vertical stack). Therefore, various embodiments may provide a memory device including a vertical stack of memory cells of various embodiments. In various embodiments, the respective vertical nanowire structure of the at least two memory cells of the plurality of memory cells arranged one over the other may be a common continuous vertical nanowire structure. In other words, each vertical nanowire structure may form part of each of the memory cells in the stack arrangement, thereby providing a common continuous vertical nanowire structure through the stacked memory cells.

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[0096] In the context of various embodiments, where a memory cell is arranged over a nanowire transistor (e.g. in a stack arrangement) or where a further memory cell is arranged over a memory cell (e.g. two memory cells arranged in a vertical stack and arranged over the nanowire transistor (e.g. in a stack arrangement)), the memory cell or cells and the nanowire transistor share one common continuous vertical nanowire structure formed on a carrier. In such embodiments, the memory cell or cells are formed at an elevated position or positions from the surface of the carrier, and that the memory cell or cells may not have its respective separate carrier but share the same carrier as that of the nanowire transistor.

[0097] In the context of various embodiments, the memory cell may be a silicon-oxide-nitride-oxide-silicon (SONOS) memory cell and the memory device may be a SONOS memory device.

[0098] FIG. 5 shows a flow chart 500 illustrating a method for manufacturing a nanowire transistor, according to various embodiments.

[0099] At 502, material is removed from a carrier to form a vertical nanowire structure extending from the carrier. In various embodiments, the carrier may be etched to remove material from the carrier in order to form the vertical nanowire structure, such that the vertical nanowire structure is made of the same material as the carrier and that the carrier and the vertical nanowire structure may be a continuous structure.

[0100] At 504, at least a portion of the vertical nanowire structure is covered with a gate insulator material to form a gate insulator region. In various embodiments, at least the portion of the vertical nanowire structure is surrounded with the gate insulator material.

[0101] At 506, at least a portion of the gate insulator region is covered with a gate material to form at least one gate region. In various embodiments, at least the portion of the gate insulator region is surrounded with the gate material.

[0102] In various embodiments, the method may further include covering at least a portion of a base of the vertical nanowire structure with an insulator material. In various embodiments, the insulator material may be an oxide or a nitride. The oxide may be any oxide (e.g. silicon dioxide), for example deposited using plasma-enhanced chemical vapor deposition (PECVD), low-pressure chemical vapor deposition (LPCVD) or high-density plasma (HDP). In various embodiments, the insulator material may be a PECVD

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low-k dielectic layer such as black diamond, or a spin coat layer of a low-k dielectric such as silk.

[0103] In various embodiments, the carrier may be doped with doping atoms of a conductivity type prior to removal of material from the carrier, such that the vertical nanowire structure formed extending from the carrier comprises a channel region, and the vertical nanowire structure being made of the same material as the carrier. In various embodiments, the method may further include forming a first source/drain region coupled to the channel region, forming a second source/drain region coupled to the carrier, and doping the first source/drain region and the second source/drain region with doping atoms of the same conductivity type as the channel region.

[0104] In embodiments where the carrier is doped with doping atoms of a conductivity type prior to removal of material from the carrier, the carrier may be doped to a particular doping depth in the carrier such that a top portion or region of the carrier is doped. Subsequently, material is removed from the carrier to form a vertical nanowire structure such that the length of the vertical nanowire structure is less than the doping depth so that the vertical nanowire structure has the same material with the doping atoms as that of the doped portion of the carrier.

[0105] In various embodiments where material is removed from the carrier to form the vertical nanowire structure extending from the carrier, the vertical nanowire structure and the carrier may be doped with doping atoms for forming a channel region in the vertical nanowire structure, a first source/drain region coupled to the channel region and a second source/drain region coupled to the carrier, wherein the doping atoms are of a conductivity type (e.g. p-conductivity type or n-conductivity type). In such embodiments, the vertical nanowire structure and the carrier are doped after the formation of the nanowire or the vertical nanowire structure.

[0106] In various embodiments, an isolation oxide may be disposed between the at least one gate region and at least one of the first source/drain region and the second source/drain region. The isolation oxide may be a HDP, PECVD or LPCVD oxide.

[0107] In various embodiments, the method may be free of forming a junction in the channel region. The method may be free of forming a junction between the channel region and the first source/drain region and the second source/drain region.

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[0108] Various embodiments may provide a method for manufacturing a memory cell. The method may include the method for manufacturing a nanowire transistor as described above. The method for manufacturing a memory cell may further include forming the gate insulator material, including forming a first dielectric layer to cover at least the portion of the vertical nanowire structure, forming a second dielectric layer, and forming a third dielectric layer, wherein the second dielectric layer is disposed between the first dielectric layer and the third dielectric layer, and wherein a bandgap of the second dielectric layer is smaller than a respective bandgap of the first dielectric layer and the third dielectric layer.

[0109] Each of the first dielectric layer and the third dielectric layer may include an oxide, for example silicon oxide (SiO_2), aluminium oxide (Al_2O_3) or hafnium oxide (HfO_2) or any high-k dielectric material. The second dielectric layer may include a material selected from the group consisting of a nitride (e.g. silicon nitride), an oxide (e.g. aluminium oxide or hafnium oxide), polycrystalline silicon (i.e. polysilicon), amorphous silicon and a metal. In embodiments where the second dielectric layer includes a nitride, the nitride dielectric layer may be configured to store charges. However, it should be appreciated that the second dielectric layer may include any high-k dielectric material.

[0110] In various embodiments, the method for manufacturing a memory cell may further include providing nanocrystals, for example silicon nanocrystals, germanium nanocrystals or metal nanocrystals, in the second dielectric layer.

[0111] In the context of various embodiments, a reference to "a vertical nanowire structure" may include a reference to "a plurality of vertical nanowire structures". Each vertical nanowire structure of the plurality of vertical nanowire structure may be of the embodiments of FIGS. 4A or 4B. In embodiments where there are a plurality of vertical nanowire structures, different vertical nanowire structures may be doped with doping atoms of different conductivity types. In other words, some vertical nanowire structures may be p-doped while other vertical nanowire structures may be n-doped.

[0112] In the context of various embodiments, the terms "junction-less" and "free of a junction" with respect to a device (e.g. nanowire transistor of various embodiments), may mean that the device does not include a physical junction or a chemical junction, for example such as a p-n junction, between the source/drain and channel, as at least

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substantially the entire nanowire is doped with doping atoms of the same conductivity type.

[0113] In the context of various embodiments, the term "channel region" may mean a channel or a conduction path, for example for the flow of electrons. In the context of various embodiments, the vertical nanowire structure under the gate may be the channel region, thereby providing a volumetric channel region.

[0114] In the context of various embodiments, the vertical nanowire structure may have a diameter in a range of between about 10 nm to about 200 nm, for example between about 50 nm to about 150 nm, between about 80 nm to about 120 nm, or between about 10 nm to about 100 nm.

[0115] In the context of various embodiments, the three dielectric layers of the gate insulator material at the gate insulator region may be an oxide-nitride-oxide (ONO) stack or arrangement.

[0116] In the context of various embodiments, the term "source/drain region" may mean a region which may be interchangeably configured as a source or a drain. For example, the source/drain region may be configured as a source or a drain, depending on the need in a circuit or in an application.

[0117] In the context of various embodiments, the doping atoms may be of a p-conductivity type such that a material doped with such doping atoms may be p-doped or the doping atoms may be an n-conductivity type such that a material doped with such doping atoms may be n-doped.

[0118] The term "p-doped" may mean a host material that is doped with doping atoms that may accept weakly-bound outer electrons from the host material, thereby creating vacancies left behind by the electrons, known as holes. Such doping atoms are also generally referred to as acceptor atoms.

[0119] The term "n-doped" may mean a host material that is doped with doping atoms that may provide extra conduction electrons to the host material, thereby resulting in an electrically conductive n-doped host material with an excess number of mobile electrons (negatively charged carriers). Such doping atoms are also generally referred to as donor atoms.

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[0120] In various embodiments, where the host material is silicon, which is a Group IV element, the host material may be doped or implanted with Group III doping atoms or elements, for example boron (B), aluminium (Al) or gallium (Ga), to form a p-doped material, or doped or implanted with Group V doping atoms or elements, for example phosphorus (P), arsenic (As) or antimony (Sb), to form an n-doped material.

[0121] In the context of various embodiments, doping may be carried out with a dopant concentration of between about $1 \times 10^{17}/cm^{-3}$ to about $5 \times 10^{20}/cm^{-3}$.

[0122] In the context of various embodiments, the at least one gate region may include a plurality of gate regions. In other words, a plurality of gate regions may be provided along the length or longitudinal axis of the vertical nanowire structure, In various embodiments, the plurality of gate regions may provide a plurality of cells (e.g. memory cells), enabling storage of multiple data bits for the foot print of one transistor.

[0123] In the context of various embodiments, the carrier may include a semiconductor. In various embodiments, the carrier may be a planar semiconductor layer. The semiconductor may be silicon or germanium. In embodiments where the carrier includes silicon, the carrier may be a silicon substrate or a silicon-on-insulator (SOI) substrate.

[0124] In embodiments where the carrier includes germanium, the germanium carrier may be disposed over a substrate, wherein the substrate comprises silicon. In various embodiments, the germanium carrier may be a layer of germanium on the substrate.

[0125] In various embodiments, the vertical nanowire structure is made of the same material as the carrier. In various embodiments, the vertical nanowire structure may be made of the same material as the top surface or portion (e.g. a thickness of a few micron or less, e.g. ≤ 5 μm) of the carrier. For example, the top surface or portion of the carrier may be p-doped or n-doped, for fabricating CMOS devices, or the top surface or portion of the carrier may include a layer of material disposed on the carrier, for example a layer of high mobility material such as germanium, on silicon.

[0126] In the context of various embodiments, the nanowire transistor may be a field effect transistor, such as a metal semiconductor field effect transistor (MESFET), a metal oxide semiconductor field effect transistor (MOSFET) or a metal insulator semiconductor field effect transistor (MISFET).

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[0127] Using MOSFET as an example and not limitations, doping with doping atoms of the p-conductivity type may provide a p-channel MOSFET (PMOS FET) while doping with doping atoms of the n-conductivity type may provide a n-channel MOSFET (NMOS FET).

[0128] FIG. 6 shows a schematic cross sectional view of a nanowire transistor 600, according to various embodiments.

[0129] The nanowire transistor 600 includes a carrier 602, which may be part of a wafer (e.g. silicon wafer) 604. The carrier 602 may be doped with doping atoms of n-conductivity type or p-conductivity type. The nanowire transistor 600 includes a vertical nanowire structure 606 extending from the carrier 602, the vertical nanowire structure 606 being made of the same material as the carrier 602. The vertical nanowire structure 606 and the carrier 602 may be a continuous structure, for example the vertical nanowire structure 606 may be etched from the carrier 602. The vertical nanowire structure 606 includes a channel region 608, which may be doped with doping atoms of the same conductivity type as that of the carrier 602.

[0130] The nanowire transistor 600 includes a gate insulator region 610 covering at least a portion of the vertical nanowire structure 606, and a gate region 612 covering at least a portion of the gate insulator region 610.

[0131] The nanowire transistor 600 includes a source/drain region, for example as represented by the square box 614a, and another source/drain region, for example as represented by the square box 614b. The source/drain region 614a is coupled to the channel region 608, while the source/drain region 614b is coupled to the carrier 602 and the channel region 608. However, it should be appreciated that the source/drain regions 614a, 614b, may be provided at other locations on the nanowire transistor 600.

[0132] The nanowire transistor 600 is a junction-less (i.e. free of a juntion) device as there is no junction (e.g. p-n junction) formed between the source/drain regions 614a, 614b, and the channel region 608, in comparison to the prior art of FIGS. 3A to 3C. In addition, the nanowire transistor 600 is junction-less as the whole nanowire structure 606 has the same conductivity type doping.

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Fabrication and experimental data

[0133] The fabrication process for manufacturing a nanowire transistor of various embodiments is now described with reference to FIGS. 7 and 8. FIG. 7 shows a schematic cross-sectional view of a fabrication process 700 for manufacturing a nanowire transistor, according to various embodiments. FIG. 8 shows SEM images of structures formed during a fabrication process for manufacturing a nanowire transistor, according to various embodiments. The SEM images of FIG. 8 are obtained using a tilted top view SEM. For illustration and clarity purposes, only one vertical nanowire structure is shown in FIGS. 7 and 8.

[0134] The nanowire transistor (e.g. a junction-less GAA-vertical nanowire NMOS transistor) may be fabricated on a bulk silicon wafer (e.g. polycrystalline silicon). Wafers with a layer of approximately 50 Å screening oxide may be used.

[0135] The silicon wafer is implanted with phosphorous (P) to form n-doped silicon (e.g. n+ silicon) and annealed to achieve various uniform doping concentration of aprroximately 1×10^{18} cm^{-3} to approximately 5×10^{19} cm^{-3} over the silicon wafer. The doping process produces a deep and uniform doped region, including source/drain doping. As shown in FIG. 7, a structure 701 may be obtained, including an undoped silicon wafer 702 and an n-doped silicon region (n+ Si) 704. In various embodiments, the concentration of the dopants may be varied with the nanowire diameter or to adjust the threshold voltage. In various embodiments where a heavily or moderately doped wafer is used, the implantation process may be optional.

[0136] A layer of silicon nitride (Si_3N_4) or silicon oxide (SiO_2), acting as a hard mask, may be optionally deposited on the structure 701. Circular resist patterns having diameters substantially similar or bigger than the required wire diameter may be patterned on the hard mask layer. The resist circular patterns or dots may be subsequently trimmed to the required diameters, for example about 50 nm to about 100 nm. Plasma dry-etch may be carried out to etch the hard mask layer and the underlying doped silicon, thereby transferring the resist patterns to the underlying silicon, to form silicon pillars. In various embodiments, different etching processes may be used, for example a $C_4F_8 + SF_6$ based etch for silicon. As an example and not limitation, the critical dimensions used for

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the mask may be about 200 nm, for patterning a dot/pillar on the wafer which may then be transformed into nanowire through etching and oxidation.

[0137] FIG. 8 shows an SEM image 800 of a silicon pillar 801. Part of the hard mask layer 802 may be observed at the tip of the silicon pillar 801.

[0138] Sacrificial oxidation at high temperature (for example between about 800°C to about 1100°C), for example to form silicon oxide (SiO_2), may be carried out to reduce the roughness of the pillar sidewalls as well as to reduce the diameters of the silicon pillars in order to form nanowires. Subsequently, the sacrificial oxide is removed by a wet etch process, and vertical nanowires with diameters of approximately 20 to 40 nm may be obtained. In various embodiments, the final wire diameter depends on the thickness of the sacrificial oxide along with the wire diameter before oxidation.

[0139] As shown in FIG. 7, a structure 706 may be obtained, including a silicon nanowire 708, dry-etched and formed from the n-doped silicon region 704. In addition, FIG. 8 shows an SEM image 804 of a silicon nanowire 806 formed, after removal of the sacrificial oxide.

[0140] A high density plasma (HDP) oxide (e.g. silicon oxide) or a PECVD oxide having poor conformality may be deposited, followed by a wet etch-back to form an isolation layer. The oxide isolation layer provides a separation between the gate and source. In various embodiments, the isolation oxide may also be formed with any thick oxide deposition, that is thicker than the nanowire height, and then polishing using, for example, chemical mechanical polish process, and then etch back in a dry plasma or a wet solution such as diluted hydrofluoric acid (DHF) or buffered oxide etch (BOE).

[0141] Subsequently, a 45 Å thick gate oxide is grown on the sidewall of the silicon nanowires, followed by a deposition of approximately 50 nm of amorphous silicon (a-silicon or α-silicon) via low pressure chemical vapor deposition (LPCVD). In further embodiments, a dry oxidation process at about 850°C may be performed to grow the gate oxide. However, it should be appreciated that other processes may be used at different temperatures and to grow different thicknesses of the oxide. In further embodiments, deposited oxides such as SiO_2 or any high-k dielectrics may be used.

[0142] The deposited amorphous silicon may be implanted with boron (B) to form a gate electrode. The nanowires, the gate oxide and the amorphous silicon form a gate stack. In

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various embodiments of the method, it should be appreciated that polycrystalline silicon (poly-silicon) may be deposited in place of the amorphous silicon.

[0143] As shown in FIG. 7, a structure 710 may be obtained, including a layer of HDP oxide 712, a layer of gate oxide 714 and a layer of amorphous silicon 716 (gate electrode). In addition, FIG. 8 shows an SEM image 808 of a silicon nanowire 806 and a layer of HDP oxide 810, exposing the upper portion of the nanowire 806.

[0144] It should be appreciated that where a high-k metal gate device is fabricated, doping of the deposited amorphous silicon 716 may be optional.

[0145] A gate definition process is then carried out, which may include removal of parts of the gate oxide 714 and the amorphous silicon 716 of the gate stack to define a gate pad, and deposition of HDP oxide and wet etching of the deposited HDP oxide to expose the top portion or cap of the amorphous silicon 716 to define the gate length. In further embodiments, this process may be achieved by deposition of a thick gate dielectric, followed by polishing and an etch back process.

[0146] As shown in FIG. 7, a structure 718 may be obtained, including a gate pad 719 and a layer of HDP oxide 720, which has been etched back to expose the top portion of the amorphous silicon 716. In addition, FIG. 8 shows an SEM image 812 of a gate stack 813 covered with a gate oxide and amorphous silicon, and a gate pad 814, after a gate-etch. FIG. 8 also shows an SEM image 816 of a HDP oxide 818 and an exposed top portion of the gate stack 813 (e.g. the gate tip), after etch-back of the deposited HDP oxide.

[0147] The exposed top portion of the amorphous silicon 716 may be subsequently wet etched in a tetramethylammonium hydroxide (TMAH) solution or etched using a dry isotropic etch process, e.g. in a SF_6 based plasma, and the underlying gate oxide is also etched to expose the underlying tip of the silicon nanowire 708. The gate oxide may be etched in DHF solution or using a dry etch process. In embodiments where a dry etch process is used, the gate oxide may be etched during the gate-etch, due to limited selectivity of different materials and the gate oxide being thin. Where polysilicon is used instead of amorphous silicon 716, the polysilicon may be etched using a dry isotropic etch process, e.g. in a SF_6 based plasma.

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[0148] As shown in FIG. 7, a structure 722 may be obtained, showing the exposed tip of the silicon nanowire 708. In addition, FIG. 8 shows an SEM image 820 of the exposed tip of the nanowire 806, after etching of the exposed gate stack tip.

[0149] Optionally, a spacer such as a silicon nitride (Si_3N_4) spacer or a silicon oxide (SiO_2) spacer, may be deposited on the sidewall of the exposed tip of the nanowire 708 of the structure 722 to provide isolation.

[0150] Subsequently, a pre-metal dielectric layer (e.g. undoped silicon glass (USG), HDP oxide) is deposited and planarized followed by wet etching to expose the nanowire tip. The pre-metal dielectric layer provides a separation between the gate and drain. Contact holes are then etched for the gate and source (which is coupled to the base of the nanowire 708), followed by metallization, for example using tantalum nitride/aluminium/tantalum nitride (TaN/Al/TaN), tungsten (W) or copper (Cu), for filling the contact holes and forming contacts. Metal etch may be performed to define different contacts.

[0151] As shown in FIG. 7, a structure 724 may be obtained, including a gate contact 726, a drain contact 728 and a source contact 730. In addition, FIG. 8 shows an SEM image 822 of metal contacts after a metal etch. Three metal contacts are formed, including a gate contact 824, a drain contact 826 and a source contact 828. It should be appreciated that the drain contacts 728, 826 and the source contacts 730, 828 may be interchangeable (e.g. the contact labelled as 826 may be the source contact while the contact labelled as 828 may be the drain contact), depending on the need in the circuit or device.

[0152] FIG. 9 shows a TEM image 900 of an NMOS transistor, according to various embodiments. The inset shows a close-up image 902 of the nanowire channel 904. The diameter of the nanowire channel 904 is about 20 nm. However, it should be appreciated that other diameters may be formed.

[0153] FIG. 10A shows a plot 1000 of drain current-gate voltage (I_d-V_g) transfer characteristics of a nanowire transistor, for different drain voltages (V_d), according to various embodiments. FIG. 10A shows the results for a drain voltage at about 0.05 V (as represented by 1002a) for a nanowire transistor, and for drain voltages at about 0.05 V (as represented by 1002b) and at about 1.2 V (as represented by 1004) for a nanowire

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transistor. Schottky contact like behaviour is observed from the results 1002a, which may be resolved or alleviated by, for example, increasing the doping at the nanowire tip or siliciding the tip.

[0154] The results shown in FIG. 10A show that the fabricated vertical junction-less nanowire transistor of various embodiments exhibit an ON/OFF ratio of approximately 10^7, a sub-threshold slope (SS) of approximately 65 mV/dec and a drain induced barrier lowering (DIBL) of approximately 0 mV/V.

[0155] FIG. 10B shows a plot 1010 of drain current-drain voltage (I_d-V_d) output characteristics of a nanowire transistor, for different gate voltages (V_g), according to various embodiments. The results of FIG. 10B are obtained for a gate length (Lg) of approximately 150 nm.

[0156] FIG. 10B shows the results for gate voltages at 0 V(as represented by 1012), at about 0.5 V (as represented by 1014), at about 1.5 V (as represented by 1016) and at about 2.0 V (as represented by 1018).

[0157] The results shown in FIG. 10B show a relatively slow turn-on in the I_d-V_d characteristics due to Schottky barrier formation with the metal contacts. In various embodiments, the turn-on may be improved by increasing the doping level at the ends of the nanowires and/or silicide the ends of the nanowires with a low barrier height metal.

[0158] The fabrication process for manufacturing a vertical silicon nanowire (SiNW) based junction-less (JL) SONOS memory cell of various embodiments is now described. Reference is made to FIGS. 7 and 8 for illustration and understanding purposes. In various embodiments, the fabrication process of the SONOS memory cell are similar to the fabrication process of the nanowire transistor of various embodiments as described above, except for the gate dielectric. The SONOS gate dielectric may include an oxide-nitride-oxide (ONO) stack while the nanowire transistor includes an oxide or includes only an oxide.

[0159] In various embodiments, in integrated circuits (ICs), both the nanowire based junction-less SONOS memory cell and the nanowire transistor may be provided or formed side by side or on the same vertical nanowire structure. For example, the nanowire transistor may be provided on a 1st level and the memory cell may be provided

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on a 2nd level and other higher level or both the nanowire transistor and the memory may be provided on the same level, depending on the design and applications.

[0160] An implantation process is carried out at an energy of approximately 170 keV with various dopant concentrations of phosphorous (P) (e.g. P^+-doped or heavily doped with P) on a wafer (e.g. silicon wafer), followed by an annealing process in a furnace at about 1000°C for about 3 hours, in order to form a uniform dopant profile in a portion of the wafer to form n-doped silicon (e.g. n+ silicon). A structure similar to structure 701 of FIG. 7 may be obtained.

[0161] A top-down approach may then be used to form vertical silicon nanowires of various diameters, with downscaling of the diameters to approximately 20 nm. A similar process for forming vertical silicon nanowires in the context of the nanowire transistor as described with reference to FIGS. 7 and 8 may be used. A structure similar to structure 706 of FIG. 7 and also as shown in the SEM image 804 of FIG. 8 may be obtained.

[0162] A high density plasma (HDP) oxide (e.g. silicon oxide) or any non-conformal oxide or any low dielectric constant (i.e. low-k) materials, may then be deposited, followed by a wet etch-back to form an isolation layer. In further embodiments, planarization, followed by etch back may also be used as to create such isolation.

[0163] Subsequently, an oxide-nitride-oxide (ONO) stack may be formed directly on the silicon nanowires to at least substantially cover or surround the silicon nanowires. The ONO stack may include a tunneling thermal oxide (e.g. silicon oxide) with a thickness of approximately 5 nm, a trapping layer of LPCVD silicon nitride with a thickness of approximately 7nm (i.e. the silicon nitride is formed via low pressure chemical vapor deposition (LPCVD)), and a blocking LPCVD oxide (e.g. silicon oxide) with a thickness of approximately 7 nm. The layer of tunneling thermal oxide is formed on the sidewalls of the silicon nanowires, followed by the layer of silicon nitride and the layer of blocking oxide.

[0164] Subsequently, approximately 80 nm of LPCVD poly-silicon as control gate may be deposited, followed by phosphorus (P) (e.g. P^+-doped or heavily doped with P) implantation and activation. The gate stack including the nanowire, the ONO stack and the poly-silicon may be patterned and etched to define a gate pad. A HDP oxide may then

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be deposited and wet etched-back to define the gate length. A structure similar to structure 718 of FIG. 7 and also as shown in the SEM image 812 of FIG. 8 may be obtained. Based on the structure 718 of FIG. 7, the ONO stack may be represented as 714 and the poly-silicon may be represented as 716.

[0165] The exposed tip of the gate stack may then be processed to remove the poly-Si in a TMAH solution and the ONO stack in a HF/H_3PO_4 solution. A structure similar to structure 722 of FIG. 7 and also as shown in the SEM image 820 of FIG. 8 may be obtained.

[0166] Subsequently, deposition of a HDP oxide and etch-back may be performed to create gate to drain isolation and to expose the tip of the nanowire. Contact holes to the gate pad and source (which is coupled to the base of the nanowire) are created, for example via etching, and metallisation of TaN/Al/TaN is performed to form metal contacts. Alloy annealing at about 420°C in about 10% hydrogen (H_2) may be performed. A structure similar to structure 724 of FIG. 7 and also as shown in the SEM image 822 of FIG. 8 may be obtained.

[0167] In the fabrication method, no source/drain implantation is performed for the junction-less SONOS (JL-SONOS), thereby reducing process cost and complexity.

[0168] FIGS. 11A and 11B show cross-sectional transmission electron microscope (TEM) images 1100 and 1120 respectively of a vertical silicon nanowire gate-all-around junction-less SONOS 1101 and an oxide-nitride-oxide (ONO) gate stack 1122.

[0169] As shown in the TEM image 1100 of FIG. 11A, the SONOS 1101 includes a nanowire 1102 with a diameter of about 20 nm and a gate length of about 120 nm. The SONOS 1101 also includes a gate 1104, a source 1106 and a drain 1108. The inset shows a close-up image 1110 of the nanowire channel 1112.

[0170] As shown in the TEM image 1102 of FIG. 11B, the well-defined ONO stack 1122 has a stack of thermal oxide 1124 / nitride 1126 / blocking oxide 1128, with a dimension of about 5 nm/7 nm/7 nm. The thermal oxide 1124 is provided on the sidewall of the silicon nanowire 1130, with the silicon nanowire 1130 heavily-doped with a doping concentration of approximately $1x10^{19}/cm^{-3}$. The TEM image 1102 also shows a layer of polysilicon 1132.

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[0171] It should be appreciated that while FIGS 11A and 11B illustrate an embodiment that may be provided, other embodiments with different parameters or dimensions, for example the dimensions of the nanowire diameter, gate length and the ONO stack and the doping concentration of the nanowire, may be provided.

[0172] FIG. 12 shows a plot 1200 of drain current-gate voltage (I_d-V_g) characteristics of a junction-less SONOS (as represented by 1202) of various embodiments and a junction-based SONOS (as represented by 1204). The I_d-V_g characteristics of the junction-less SONOS 1202 and the junction-based SONOS 1204 are obtained for a nanowire diameter of about 20 nm. In addition, the channel doping for the junction-less SONOS is approximately $1 \times 10^{19}/cm^{-3}$. It should be appreciated that in various embodiments, the channel doping for a junction-less SONOS may be varied from about $1 \times 10^{17}/cm^{-3}$ to about $5 \times 10^{20}/cm^{-3}$.

[0173] As shown in FIG. 12, the JL-SONOS shows comparable I_d-V_g characteristics (switching function) to the junction-based SONOS, with a turn-off current (I_{off}) down to approximately 1×10^{-14} A. This may be attributed to the highly scaled wire channel and therefore better gate control owing to the GAA structure. Therefore, when a negative bias is applied on the channel, the channel electrons may be fully-depleted and the device may be at least substantially completely turned off.

[0174] FIG. 13 shows a plot 1300 of drain current-gate voltage (I_d-V_g) characteristics of junction-less SONOS with different nanowire diameters, according to various embodiments. The I_d-V_g characteristics are obtained for junction-less SONOS with a channel doping concentration of approximately $1 \times 10^{19}/cm^{-3}$, for nanowire diameters of about 20 nm, about 40 nm, about 50 nm and about 110 nm, with the arrow 1302 showing the results in the direction of increasing nanowire diameter. As the nanowire diameter increases, the channel electrons may be more difficult to be completely depleted and the body effect may increase the I_{off}. Therefore, a smaller nanowire diameter results in a smaller I_{off}. In addition, scaling down of the nanowire diameter also improves the sub-threshold swing. Nevertheless, the nanowire diameter which may be used is a function of the doping inside the nanowire. A larger nanowire diameter may be used with reduced doping and vice versa.

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[0175] FIG. 14 shows a plot 1400 of drain current-gate voltage (I_d-V_g) characteristics of junction-less SONOS with different channel doping concentrations, according to various embodiments. The I_d-V_g characteristics are obtained for junction-less SONOS with a nanowire diameter of about 20 nm, for channel doping concentrations of approximately $1 \times 10^{17}/cm^{-3}$ (as represented by 1402) and approximately $1 \times 10^{19}/cm^{-3}$ (as represented by 1404). While a more negative V_g may be needed for full depletion, the junction-less SONOS with heavily doped (i.e. $1 \times 10^{19}/cm^{-3}$) channel exhibits a higher I_{on}/I_{off} ratio due to its higher channel conductivity in the normally-on mode, and therefore a much higher I_{on}.

[0176] FIG. 15 shows plots 1500, 1502 of simulated electric field distributions of junction-less SONOS for different nanowire diameters, according to various embodiments. The simulated electric field distributions are obtained for the silicon nanowire channel and ONO stack at V_g of about 4.5 V and a channel doping concentration of approximately $1 \times 10^{19}/cm^{-3}$, for nanowire diameters of about 20 nm and about 40 nm.

[0177] FIG. 16 shows plots 1600, 1602 of simulated electric field distributions of junction-less SONOS for different channel doping concentrations, according to various embodiments. The simulated electric field distributions are obtained for the silicon nanowire channel and ONO stack at V_g of about 4.5 V and a nanowire diameter of about 20 nm, for channel doping concentrations of approximately $1 \times 10^{17}/cm^{-3}$ and approximately $1 \times 10^{19}/cm^{-3}$.

[0178] The results shown in FIGS. 15 and 16 show increased fields for junction-less SONOS with a smaller diameter and a heavily doped channel, which may lead to improved programming at low gate voltages.

[0179] FIGS. 17A to 17C and 18A to 18C show the programming/erasing (P/E) characteristics of junction-less SONOS (JL-SONOS) and junction-based SONOS with different channel doping concentrations. The JL-SONOS may be programmed and erased using Fowler-Nordheim (FN) tunneling with a pulse applied on the gate, with the source and drain grounded.

[0180] FIGS. 17A and 17B show plots 1700, 1704 of programming characteristics of junction-less SONOS memory cells for different gate voltages, according to various

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embodiments, while FIG. 17C shows a plot 1708 of programming characteristics of a junction-based SONOS memory cell for different gate voltages.

[0181] The programming characteristics shown in FIGS. 17A and 17B for the junction-less SONOS memory cells are obtained for channel doping concentrations of approximately $1 \times 10^{17}/cm^{-3}$ and approximately $1 \times 10^{19}/cm^{-3}$ respectively. The programming characteristics shown in FIG. 17C are obtained for a junction-based SONOS memory cell with an undoped channel. The programming characteristics shown in FIGS. 17A to 17C are obtained for a nanowire diameter of about 20 nm.

[0182] The programming characteristics shown in FIGS. 17A and 17B are obtained for gate voltages of about 12 V, about 13 V, about 14 V, about 15 V and about 18 V, with the arrows 1702 (FIG. 17A) and 1706 (FIG. 17B) showing the results in the direction of increasing voltage. The programming characteristics shown in FIG. 17C are obtained for gate voltages of about 12 V, about 14 V, about 15 V, about 16V and about 18 V, with the arrow 1710 showing the results in the direction of increasing voltage.

[0183] FIGS. 18A and 18B show plots 1800, 1804 of erasing characteristics of junction-less SONOS memory cells for different gate voltages, according to various embodiments, while FIG. 18C shows a plot 1808 of erasing characteristics of a junction-based SONOS memory cell for different gate voltages.

[0184] The erasing characteristics shown in FIGS. 18A and 18B for the junction-less SONOS memory cells are obtained for channel doping concentrations of approximately $1 \times 10^{17}/cm^{-3}$ and approximately $1 \times 10^{19}/cm^{-3}$ respectively. The erasing characteristics shown in FIG. 18C are obtained for a junction-based SONOS memory cell with an undoped channel. The erasing characteristics shown in FIGS. 18A to 18C are obtained for a nanowire diameter of about 20 nm.

[0185] The erasing characteristics shown in FIGS. 18A and 18B are obtained for gate voltages of about -12 V, about -13 V, about -14 V, about -15 V and about -18 V, with the arrows 1802 (FIG. 18A) and 1806 (FIG. 18B) showing the results in the direction of increasing negative voltage. The erasing characteristics shown in FIG. 18C are obtained for gate voltages of about -12 V, about -14 V, about -15 V, about -16V and about -18 V, with the arrow 1810 showing the results in the direction of increasing negative voltage.

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[0186] For the lightly doped JL-SONOS with a channel doping concentration of approximately $1 \times 10^{17}/cm^{-3}$, and a nanowire diameter of about 20 nm, there is a memory window of about 3.2 V at the P/E time of about 1 ms measured at voltages of about +15 V and about -18 V.

[0187] A comparison between the P/E speed characteristics for the junction-based SONOS and JL-SONOS show that memory cells or devices with lower channel doping concentrations exhibit faster erase speed, as shown in FIGS. 18A to 18C. As SONOS relies mainly on the hole injection from the channel for erasing, n-type doped channel may make hole tunnelling more difficult due to the increased barrier height for holes.

[0188] FIG. 19 shows a plot 1900 of programming/erasing (P/E) speed of junction-less SONOS memory cells for different nanowire diameters, according to various embodiments. The results obtained are shown in terms of a threshold voltage shift (ΔV_{th}) at a program (PGM) voltage of about 15 V and an erase (ERS) voltage of about - 15V for junction-less SONOS with a channel doping concentration of about $1 \times 10^{19}/cm^{-3}$, for nanowire diameters of about 20 nm and about 40 nm. The results shown in FIG. 19 show that junction-less SONOS memory cells with a smaller nanowire diameter exhibit faster programming and erasing speeds, as a result of enhanced electric field in the tunnel oxide layer and reduced electric field in the blocking oxide of the ONO stack, due to the reduced curvatures of the nanowire.

[0189] FIG. 20 shows a plot 2000 of multi-bit programming characteristics of a junction-less SONOS memory cell, according to various embodiments. The results are obtained for a junction-less SONOS memory cell with a nanowire diameter of about 20 nm and a channel doping concentration of approximately $1 \times 10^{19}/cm^{-3}$, for different gate bias voltages of about 13 V, about 14 V and about 18 V for about 1 ms. As shown in FIG. 20, the junction-less SONOS memory cell is able to store 2 bits per cell using four states "00" (erase), "01" (program gate bias voltage of about 13 V), "10" (program gate bias voltage of about 14 V) and "11" (program gate bias voltage of about 18 V) with each state defined at a different transistor threshold voltage, V_t, of greater than 1 V (i.e. > 1 V).

[0190] FIG. 21A shows a plot 2100 of retention characteristics at 85°C for junction-less SONOS memory cells of various embodiments and a junction-based SONOS memory cell. The high temperature retention characteristics shown in FIG. 21A show that the

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heavily-doped junction-less SONOS memory cells with a channel doping concentration of about $1 \times 10^{19}/cm^{-3}$ exhibit less voltage shift (ΔV_{th}) as compared to lightly doped junction-less SONOS memory cells with a channel doping concentration of about $1 \times 10^{17}/cm^{-3}$ or the junction-based SONOS with an undoped channel. With higher channel doping concentrations, the tunnel barrier for the trapped electrons may be increased and thus more reliable charge storage is achieved. FIG. 21A shows that the memory window may be maintained for up to 10^5 seconds.

[0191] FIG. 21B shows a plot 2120 of endurance characteristics at 85°C for junction-less SONOS memory cells of various embodiments and a junction-based SONOS memory cell. The endurance characteristics (cycling characteristics) shown in FIG. 21B show that the junction-less SONOS memory cells with different channel doping concentrations of about $1 \times 10^{17}/cm^{-3}$ and about $1 \times 10^{19}/cm^{-3}$ or the junction-based SONOS with an undoped channel are able to maintain the P/E window even after 10^4 cycles at about 85°C.

[0192] FIG. 22A shows a schematic cross-sectional view of a 3-D memory device 2200 based on vertical junction-less silicon nanowire SONOS memory cells, according to various embodiments. The 3-D memory device 2200 is a 3-D multi-level stacked NAND structure using the junction-less SONOS as the building blocks. As there is no junction for both the selection gate transistors and memory cells, the integration process may be simplified.

[0193] The 3-D memory device 2200 includes a plurality of memory cells, for example as represented by 2202a and 2202b for two memory cells, arranged in a vertical stack. The 3-D memory device 2100 further includes a plurality of vertical nanowire structures, for example as represented by 2204a and 2204b for two vertical nanowire structures. As shown in FIG. 22A, each of the vertical nanowire structures 2204a and 2204b is provided for the plurality of memory cells 2202a and 2202b, such that continuous vertical nanowire structures 2204a and 2204b are provided through the stacked memory cells 2202a and 2202b of the 3-D memory device 2200.

[0194] The 3-D memory device 2200 may further include a plurality of bit lines (BL) 2206, based on the plurality of vertical nanowire structures 2204a and 2204b, a

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plurality of control gates (CG) 2208, an upper select gate (USG) 2210, a lower select gate (LSG) 2212 and a select line (SL) 2214.

[0195] FIG. 22B shows a schematic of an equivalent circuit 2240 for the embodiment of FIG. 22A. Features in the equivalent circuit 2240 of FIG. 22B that are equivalent to that of the 3-D memory device 2200 of FIG. 22A are denoted with the same reference numbers.

[0196] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

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CLAIMS

1. A nanowire transistor, comprising:

a carrier;

a vertical nanowire structure extending from the carrier, the vertical nanowire structure comprising a channel region, and the vertical nanowire structure being made of the same material as the carrier;

a gate insulator region covering at least a portion of the vertical nanowire structure; and

at least one gate region covering at least a portion of the gate insulator region.

2. The nanowire transistor as claimed in claim 1,

wherein the gate insulator region surrounds at least the portion of the vertical nanowire structure, and

wherein the at least one gate region surrounds at least the portion of the gate insulator region.

3. The nanowire transistor as claimed in claim 1 or 2, further comprising an insulator material covering at least a portion of a base of the vertical nanowire structure.

4. The nanowire transistor as claimed in claim 3, wherein the insulator material comprises an oxide or a nitride.

5. The nanowire transistor as claimed in any one of claims 1 to 4, wherein the channel region and the carrier are doped with doping atoms of a conductivity type.

6. The nanowire transistor as claimed in claim 5, further comprising:

a first source/drain region coupled to the channel region; and

a second source/drain region coupled to the carrier,

wherein the first source/drain region and the second source/drain region are doped with doping atoms of the same conductivity type as the channel region.

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7. The nanowire transistor as claimed in claim 6, further comprising an isolation oxide disposed between the at least one gate region and at least one of the first source/drain region and the second source/drain region.

8. The nanowire transistor as claimed in any one of claims 5 to 7, wherein the doping atoms are selected from a group consisting of boron, aluminium and gallium or are selected from a group consisting of phosphorus, arsenic and antimony.

9. The nanowire transistor as claimed in any one of claims 1 to 8, wherein the at least one gate region comprises a plurality of gate regions.

10. The nanowire transistor as claimed in any one of claims 1 to 9, wherein the carrier comprises a semiconductor.

11. The nanowire transistor as claimed in claim 10, wherein the semiconductor comprises silicon or germanium.

12. The nanowire transistor as claimed in claim 11, wherein the germanium carrier is disposed over a substrate, and wherein the substrate comprises silicon.

13. The nanowire transistor as claimed in any one of claims 1 to 12, wherein the channel region is free of a junction.

14. The nanowire transistor as claimed in any one of claims 1 to 13, wherein the gate insulator region comprises a gate oxide.

15. The nanowire transistor as claimed in any one of claims 1 to 14, wherein the nanowire transistor is a field effect transistor.

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16. A memory cell comprising the nanowire transistor as claimed in any one of claims 1 to 13, wherein the gate insulator region comprises:

a first dielectric layer configured to cover at least the portion of the vertical nanowire structure;

a second dielectric layer; and

a third dielectric layer,

wherein the second dielectric layer is disposed between the first dielectric layer and the third dielectric layer, and

wherein a bandgap of the second dielectric layer is smaller than a respective bandgap of the first dielectric layer and the third dielectric layer.

17. The memory cell as claimed in claim 16, wherein each of the first dielectric layer and the third dielectric layer comprises an oxide.

18. The memory cell as claimed in claim 17, wherein the oxide is silicon oxide, aluminium oxide or hafnium oxide.

19. The memory cell as claimed in any one of claims 16 to 18, wherein the second dielectric layer comprises a material selected from the group consisting of a nitride, an oxide, polycrystalline silicon, amorphous silicon and a metal.

20. The memory cell as claimed in claim 19, wherein the oxide is aluminium oxide or hafnium oxide.

21. The memory cell as claimed in claim 19, wherein the nitride dielectric layer is configured to store charges.

22. The memory cell as claimed in any one of claims 16 to 21, wherein the second dielectric layer comprises nanocrystals.

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23. A memory device comprising the memory cell as claimed in any one of claims 16 to 22.

24. The memory device as claimed in claim 23, further comprising the nanowire transistor as claimed in any one of claims 1 to 15, wherein the nanowire transistor is configured to couple to the memory cell.

25. The memory device as claimed in claim 24,

wherein the memory cell is arranged over the nanowire transistor,

wherein the respective vertical nanowire structure of the memory cell and the nanowire transistor is the same vertical nanowire structure, and

wherein the respective carrier of the memory cell and the nanowire transistor is the same carrier.

26. The memory device as claimed in claim 25, further comprising a second memory cell, wherein the memory cell and the second memory cell are arranged one over the other on the same vertical nanowire structure.

27. A method for manufacturing a nanowire transistor; the method comprising:

removing material from a carrier to form a vertical nanowire structure extending from the carrier;

covering at least a portion of the vertical nanowire structure with a gate insulator material to form a gate insulator region; and

covering at least a portion of the gate insulator region with a gate material to form at least one gate region.

28. The method as claimed in claim 27,

wherein covering at least a portion of the vertical nanowire structure comprises surrounding at least the portion of the vertical nanowire structure with the gate insulator material, and

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wherein covering at least the portion of the gate insulator region comprises surrounding at least the portion of the gate insulator region with the gate material.

29. The method as claimed in claim 27 or 28, further comprising covering at least a portion of a base of the vertical nanowire structure with an insulator material.

30. The method as claimed in claim 29, wherein the insulator material comprises an oxide or a nitride.

31. The method as claimed in any one of claims 27 to 30, further comprising

doping the carrier with doping atoms of a conductivity type prior to removing material from the carrier, such that the vertical nanowire structure formed extending from the carrier comprises a channel region, and the vertical nanowire structure being made of the same material as the carrier.

32. The method as claimed in claim 31, further comprising:

forming a first source/drain region coupled to the channel region;

forming a second source/drain region coupled to the carrier; and

doping the first source/drain region and the second source/drain region with doping atoms of the same conductivity type as the channel region.

33. The method as claimed in any one of claims 27 to 30, further comprising:

doping the vertical nanowire structure and the carrier with doping atoms for forming a channel region in the vertical nanowire structure, a first source/drain region coupled to the channel region and a second source/drain region coupled to the carrier,

wherein the doping atoms are of a conductivity type.

34. The method as claimed in claim 32 or 33, further comprising disposing an isolation oxide between the at least one gate region and at least one of the first source/drain region and the second source/drain region.

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35. The method as claimed in any one of claims 31 to 34, wherein the doping atoms are selected from a group consisting of boron, aluminium and gallium or are selected from a group consisting of phosphorus, arsenic and antimony.

36. The method as claimed in any one of claims 27 to 35, wherein the at least one gate region comprises a plurality of gate regions.

37. The method as claimed in any one of claims 27 to 36, wherein the carrier comprises a semiconductor.

38. The method as claimed in claim 37, wherein the semiconductor comprises silicon or germanium.

39. The method as claimed in claim 38, further comprising disposing the germanium carrier over a substrate, wherein the substrate comprises silicon.

40. The method as claimed in any one of claims 27 to 39, wherein the method is free of forming a junction in the channel region.

41. The method as claimed in any one of claims 27 to 40, wherein the gate insulator region comprises a gate oxide.

42. The method as claimed in any one of claims 27 to 41, wherein the nanowire transistor is a field effect transistor.

43. A method for manufacturing a memory cell, comprising the method for manufacturing a nanowire transistor as claimed in any one of claims 27 to 40, and wherein covering at least a portion of the vertical nanowire structure with the gate insulator material comprises:

forming a first dielectric layer to cover at least the portion of the vertical nanowire structure;

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forming a second dielectric layer; and

forming a third dielectric layer,

wherein the second dielectric layer is disposed between the first dielectric layer and the third dielectric layer, and

wherein a bandgap of the second dielectric layer is smaller than a respective bandgap of the first dielectric layer and the third dielectric layer.

44. The method as claimed in claim 43, wherein each of the first dielectric layer and the third dielectric layer comprises an oxide.

45. The method as claimed in claim 44, wherein the oxide is silicon oxide, aluminium oxide or hafnium oxide.

46. The method as claimed in any one of claims 43 to 45, wherein the second dielectric layer comprises a material selected from the group consisting of a nitride, an oxide, polycrystalline silicon, amorphous silicon and a metal.

47. The method as claimed in claim 46, wherein the oxide is aluminium oxide or hafnium oxide.

48. The method as claimed in claim 47, wherein the nitride dielectric layer is configured to store charges.

49. The method as claimed in any one of claims 43 to 48, further comprising providing nanocrystals in the second dielectric layer.

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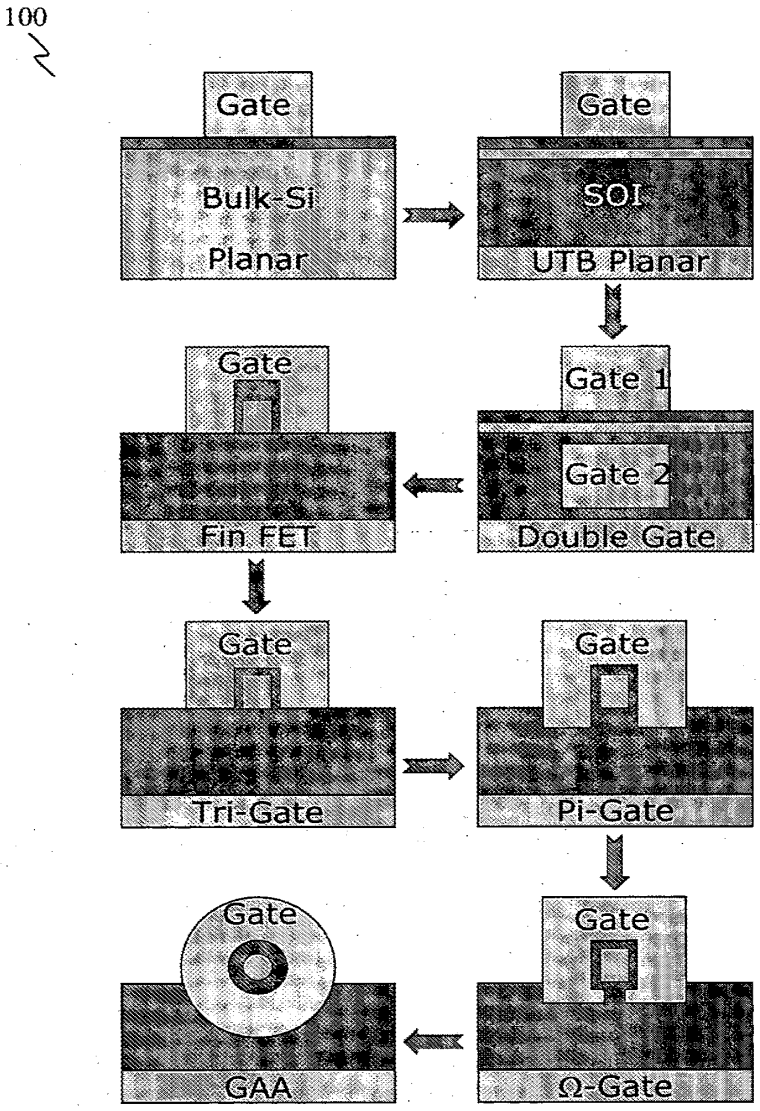


FIG. 1
(Prior Art)

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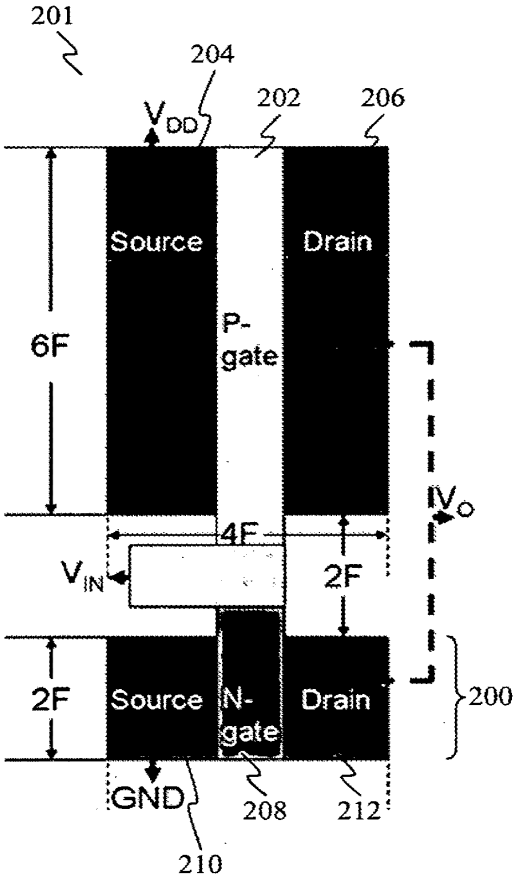


FIG. 2A
(Prior Art)

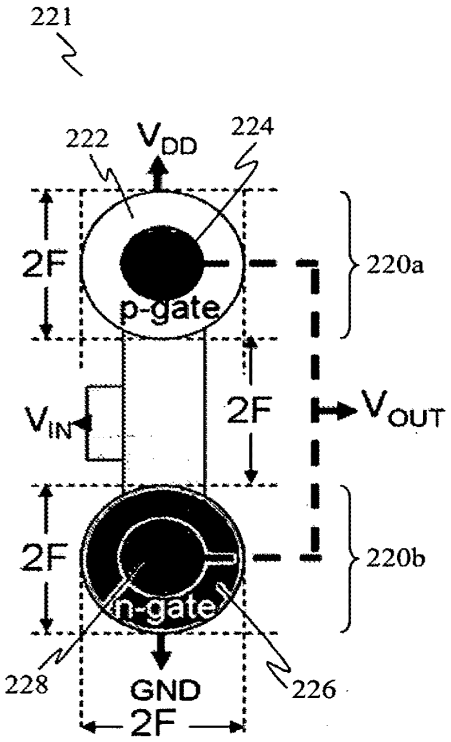


FIG. 2B
(Prior Art)

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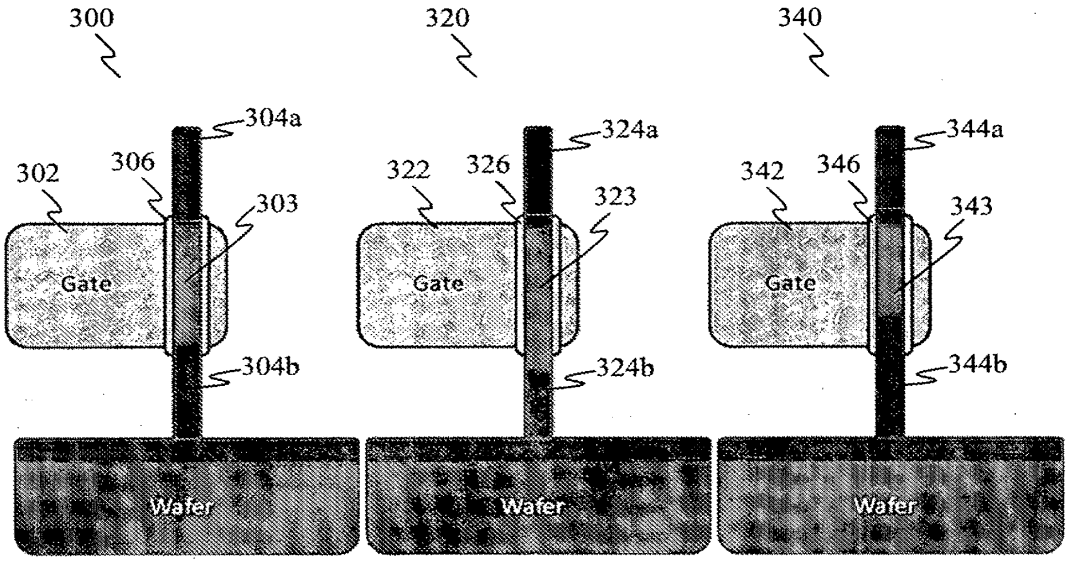


FIG. 3A
(Prior Art)

FIG. 3B
(Prior Art)

FIG. 3C
(Prior Art)

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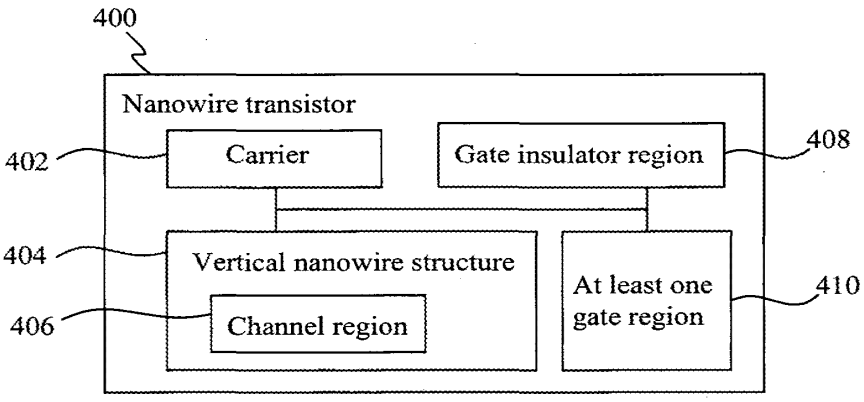


FIG. 4A

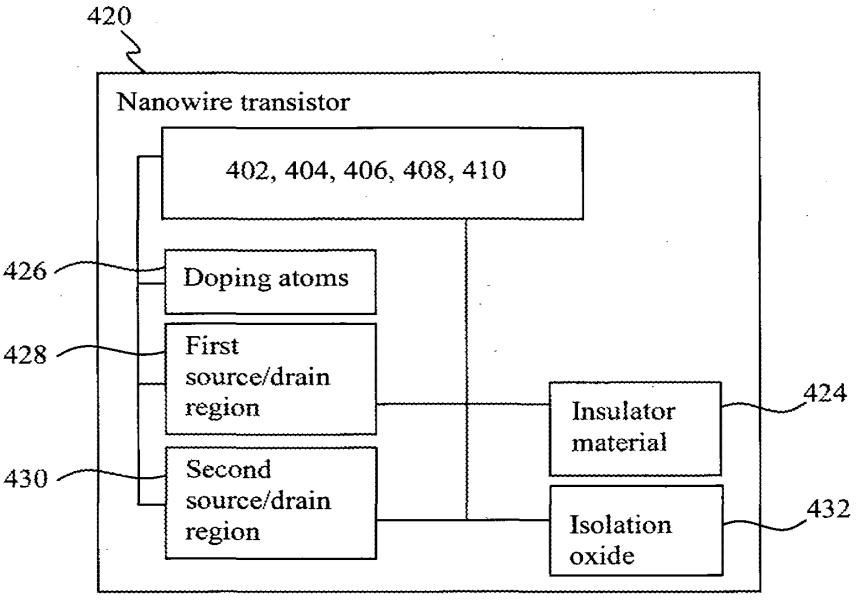


FIG. 4B

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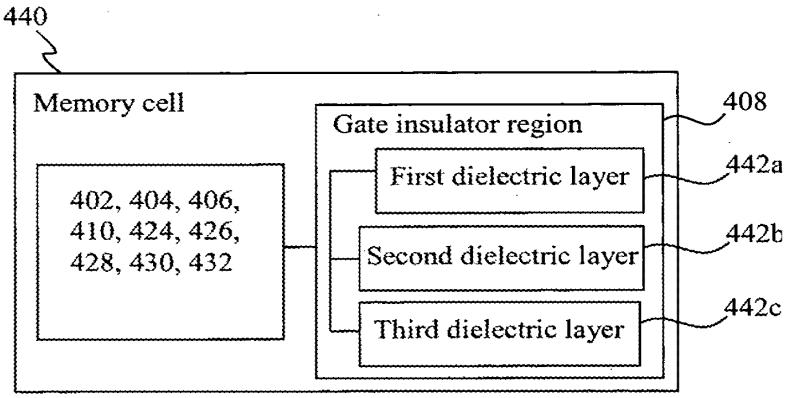


FIG. 4C

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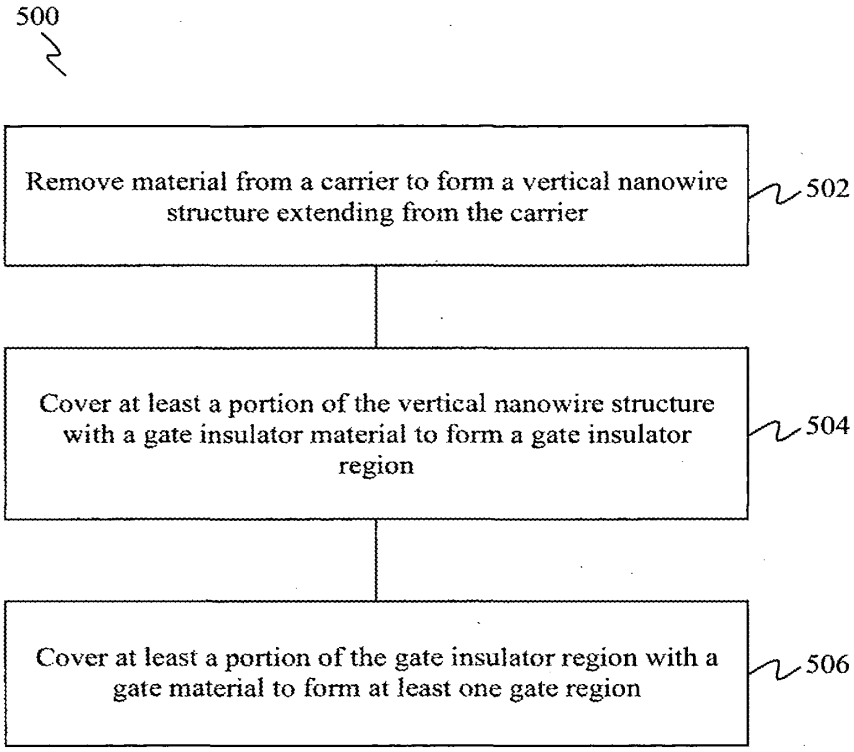


FIG. 5

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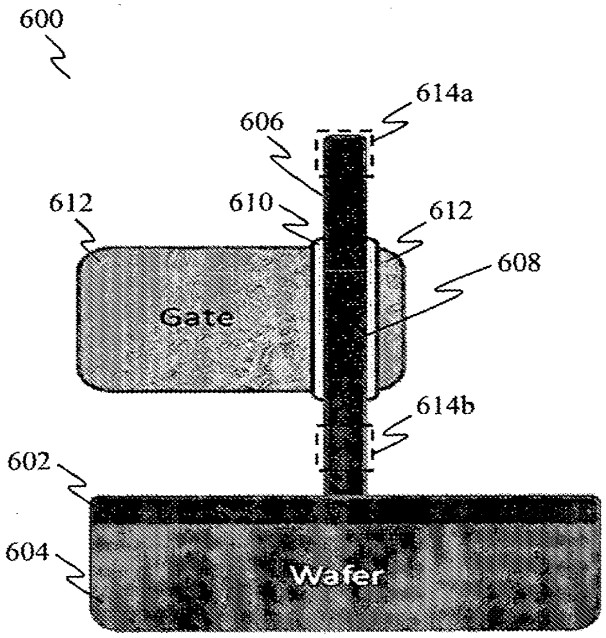


FIG. 6

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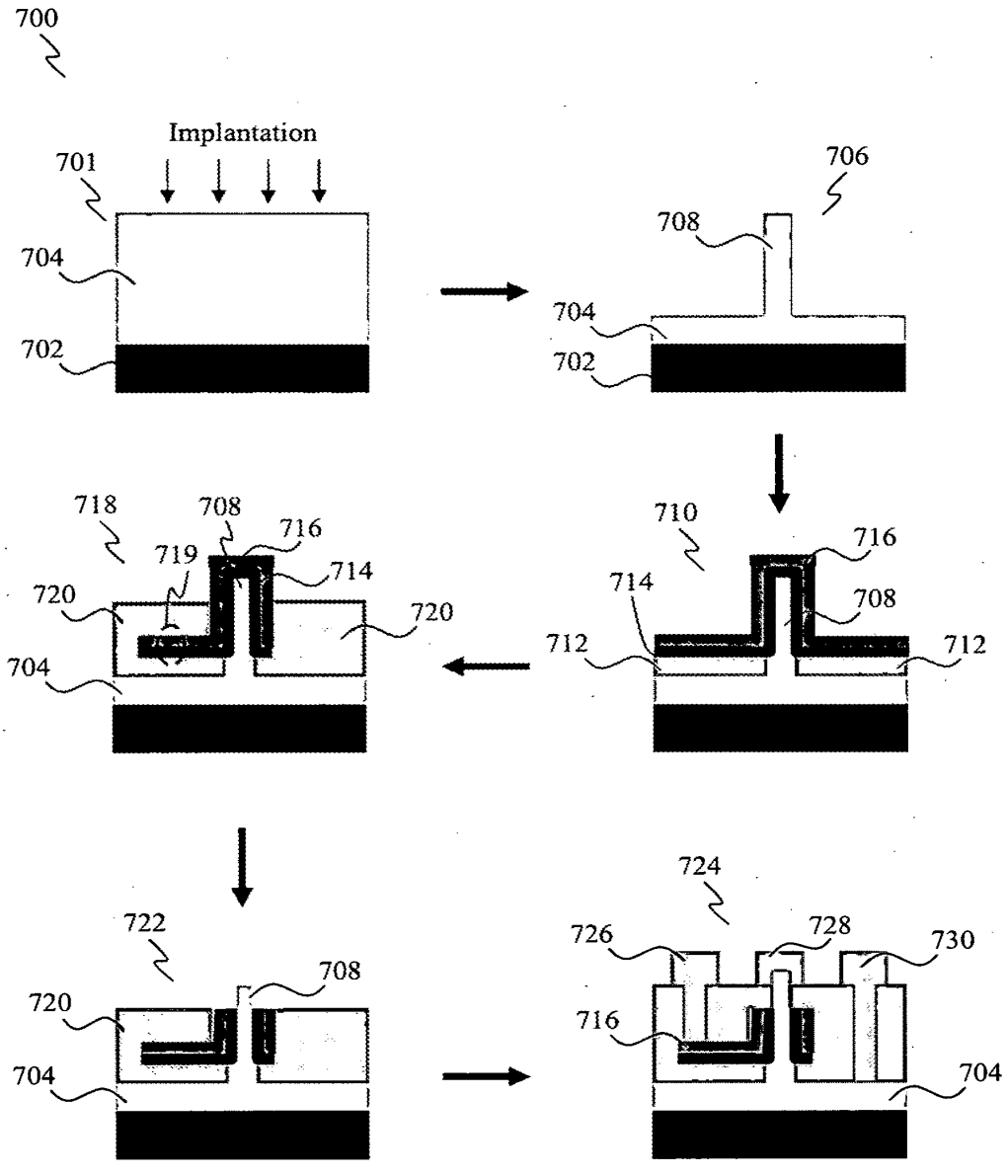


FIG. 7

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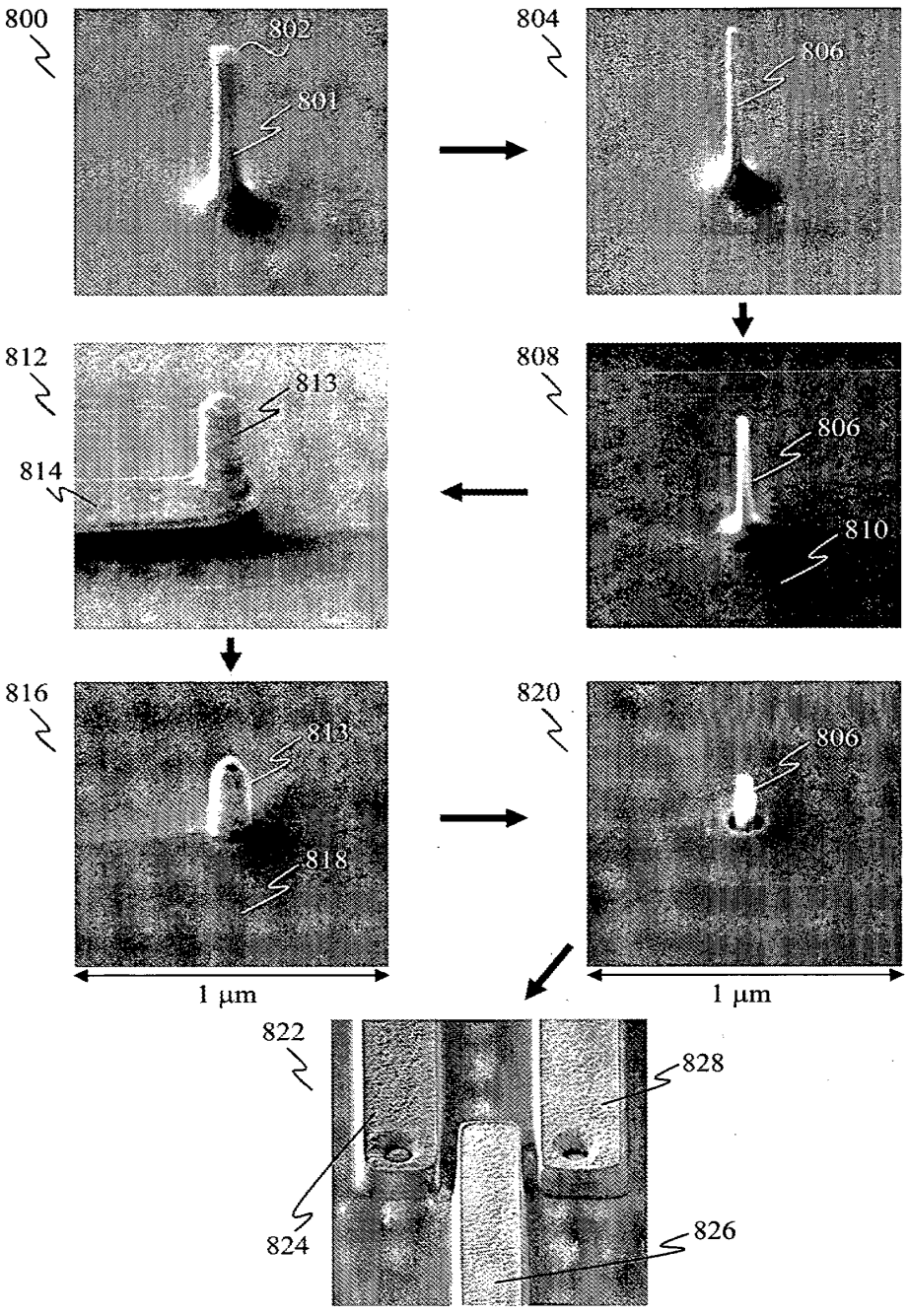


FIG. 8

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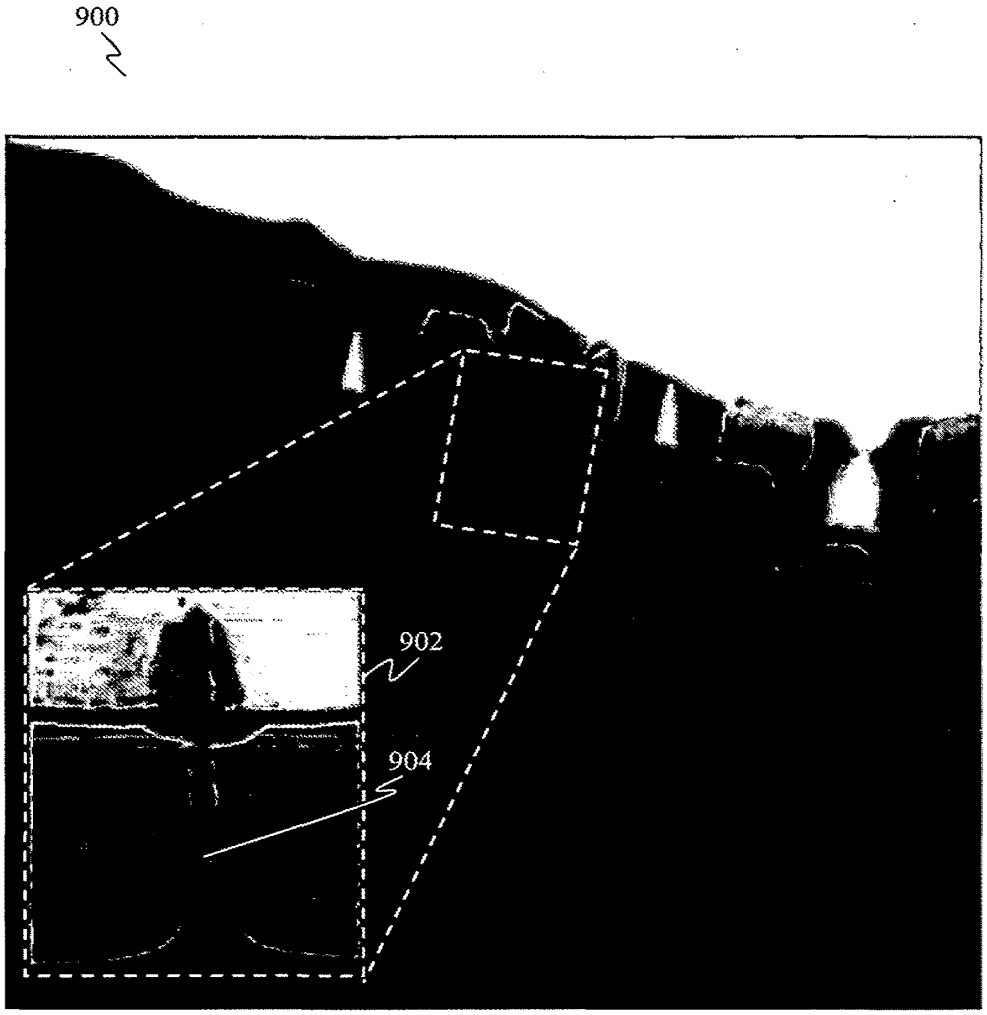


FIG. 9

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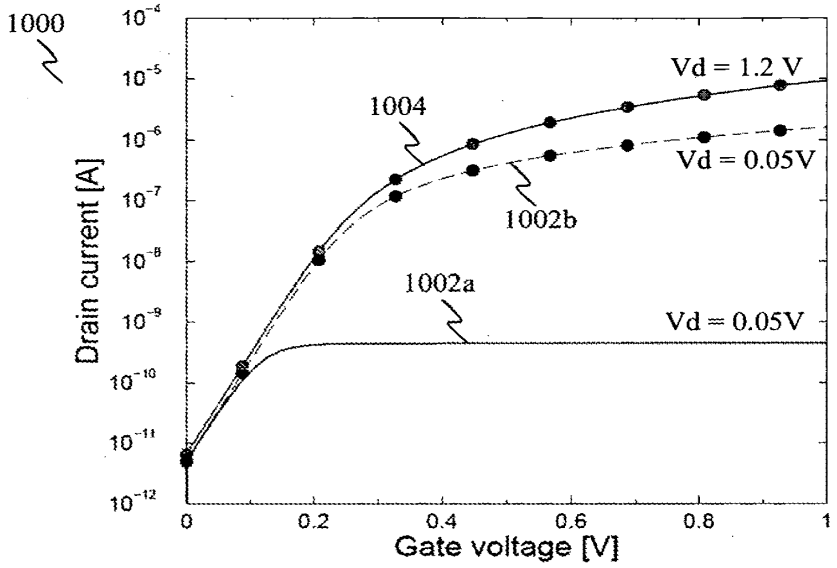


FIG. 10A

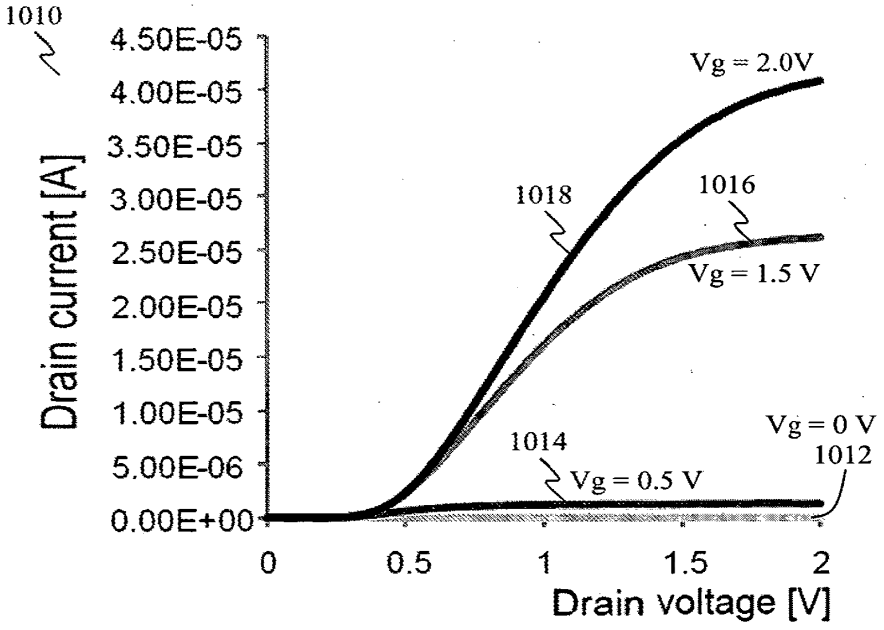


FIG. 10B

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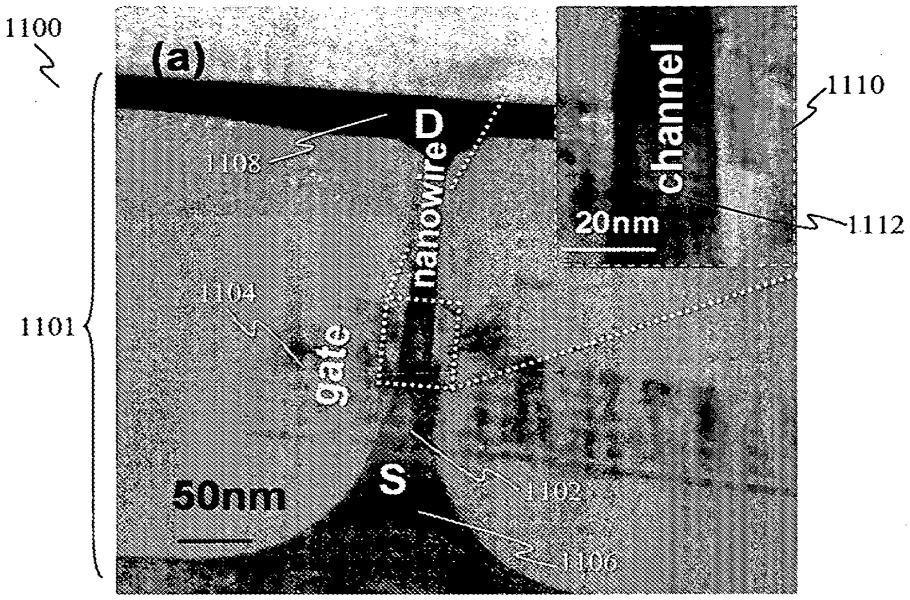


FIG. 11A

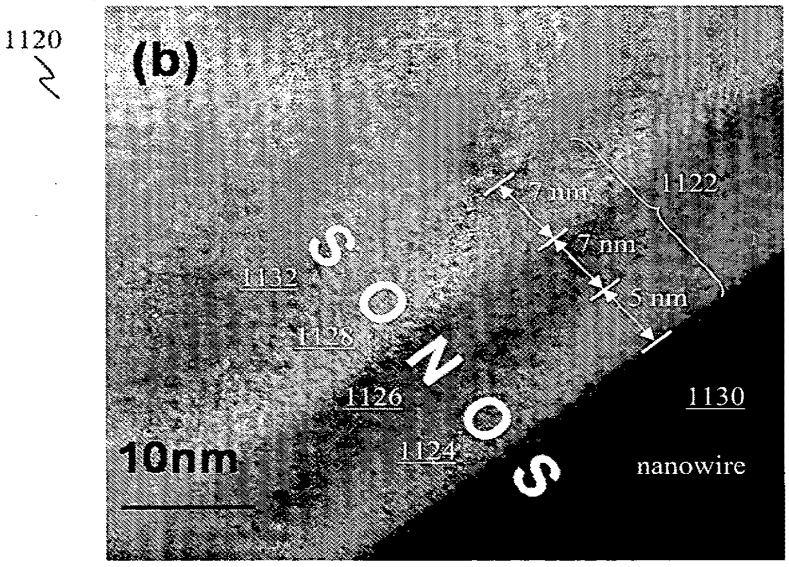


FIG. 11B

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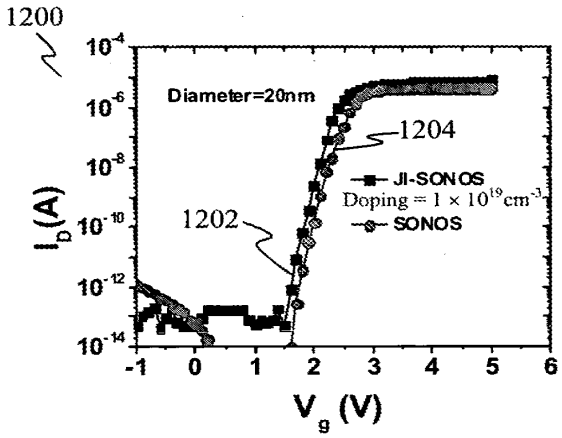


FIG. 12

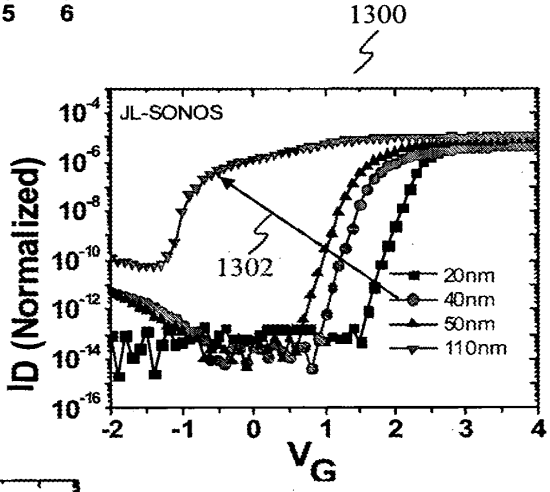


FIG. 13

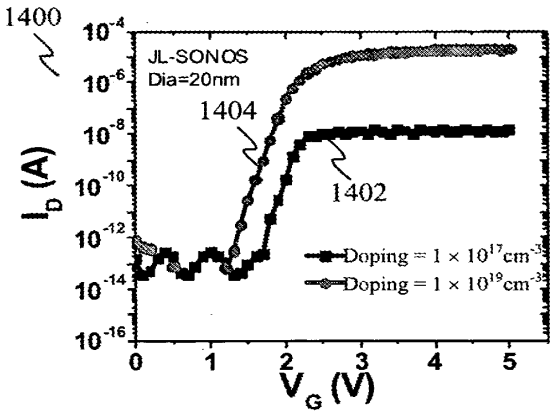


FIG. 14

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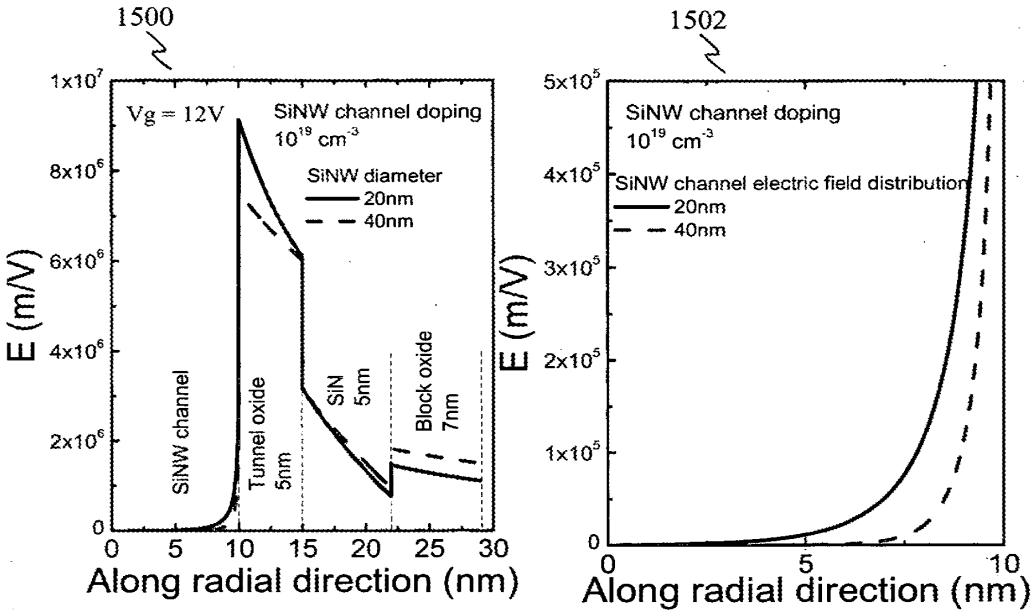


FIG. 15

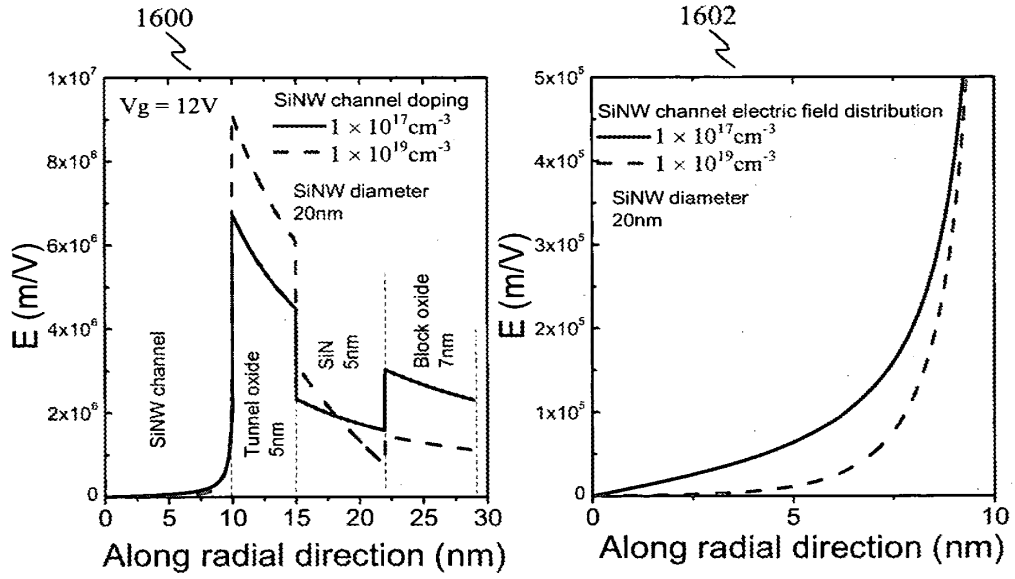


FIG. 16

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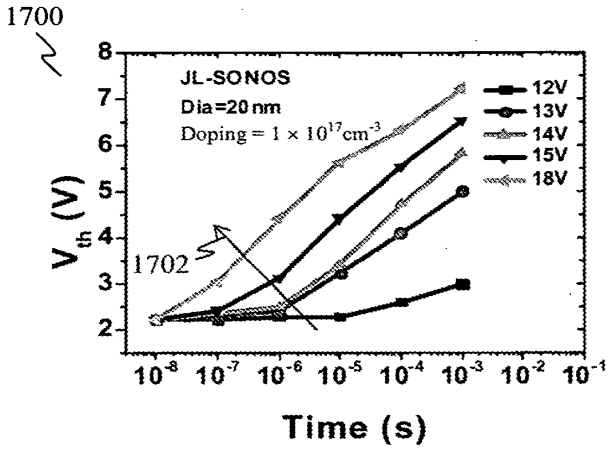


FIG. 17A

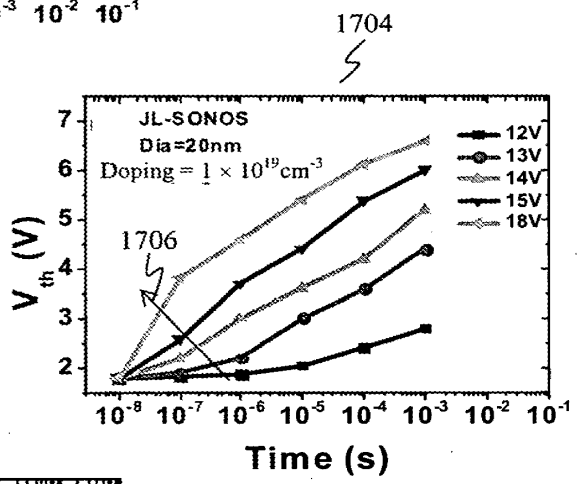


FIG. 17B

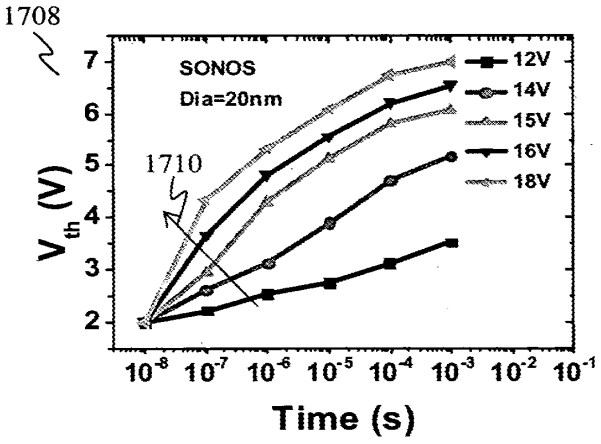


FIG. 17C

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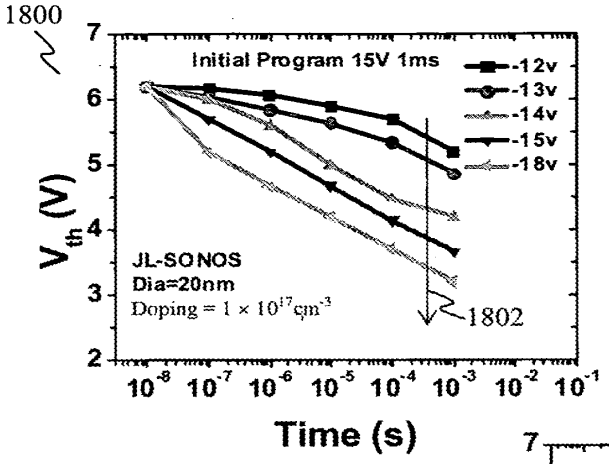


FIG. 18A

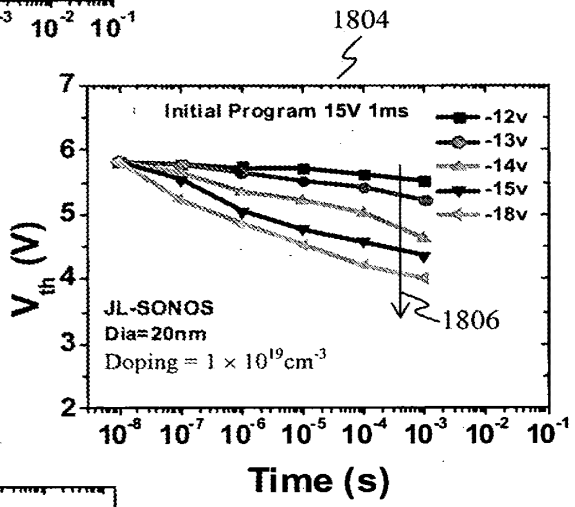


FIG. 18B

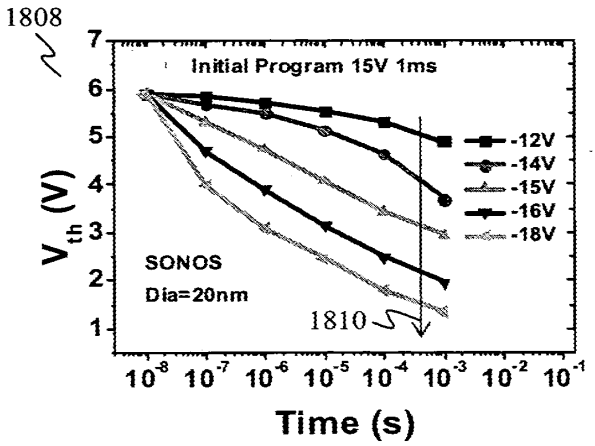


FIG. 18C

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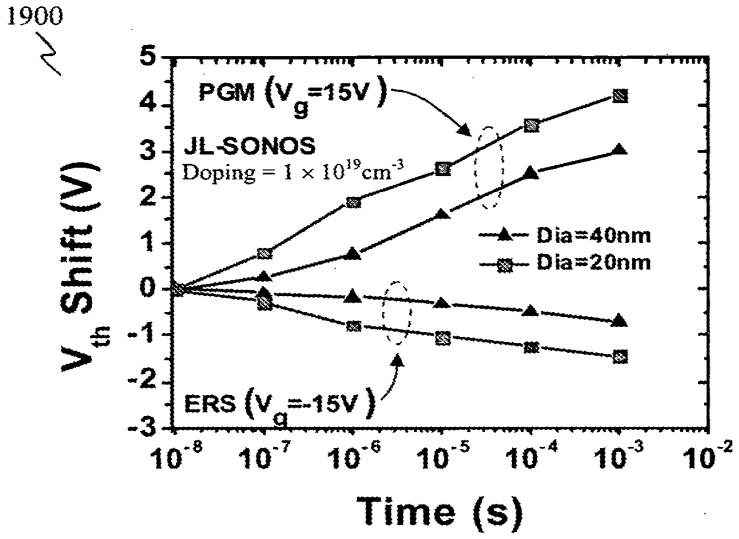


FIG. 19

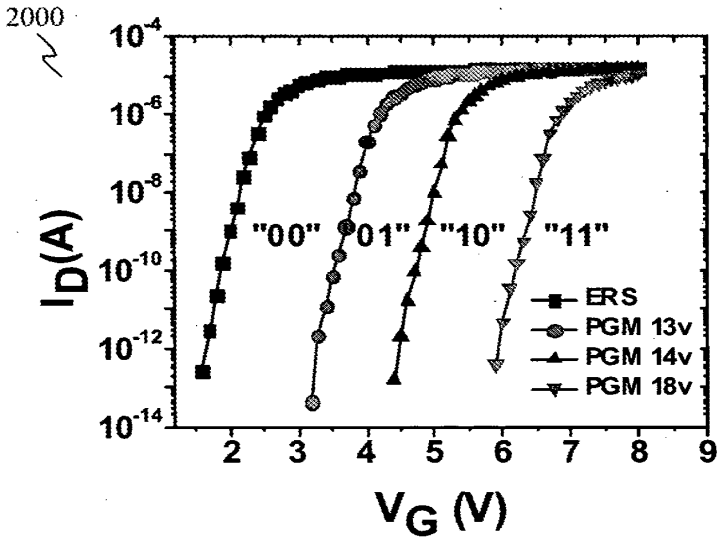


FIG. 20

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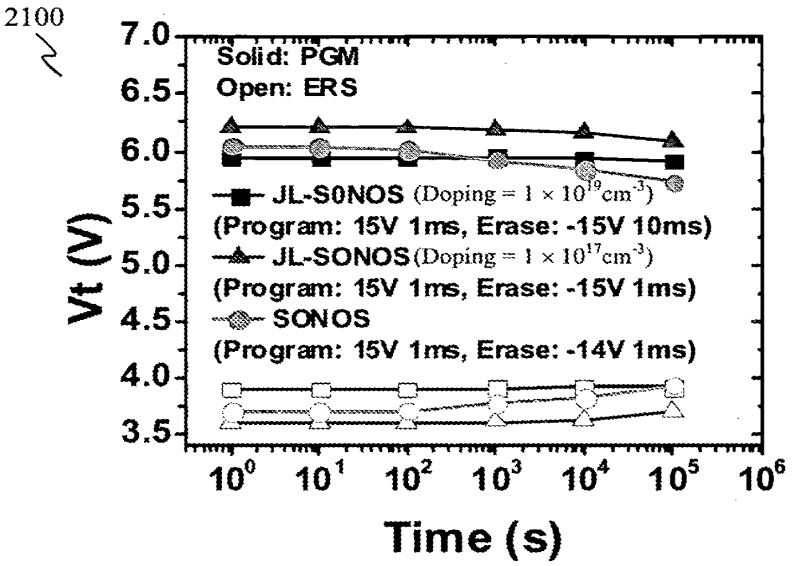


FIG. 21A

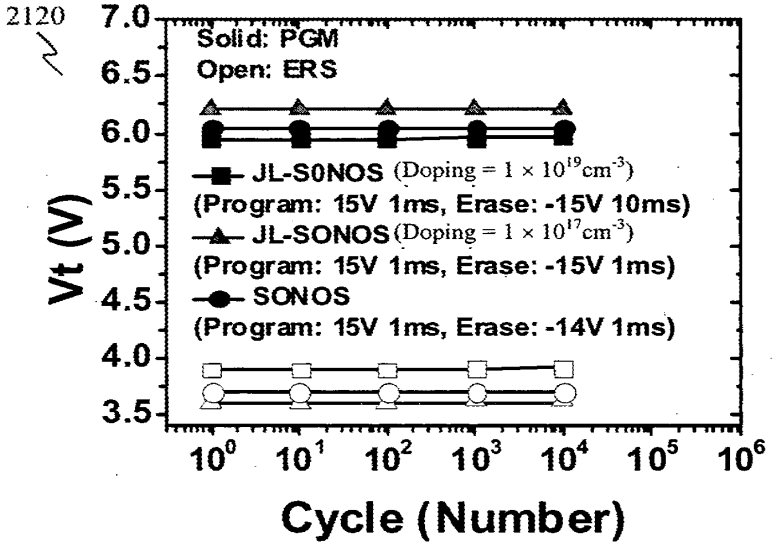


FIG. 21B

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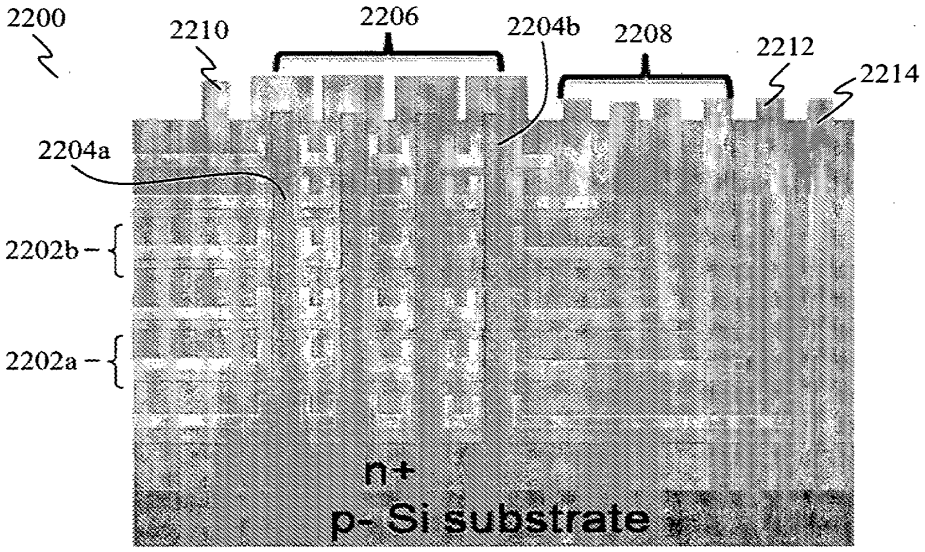


FIG. 22A

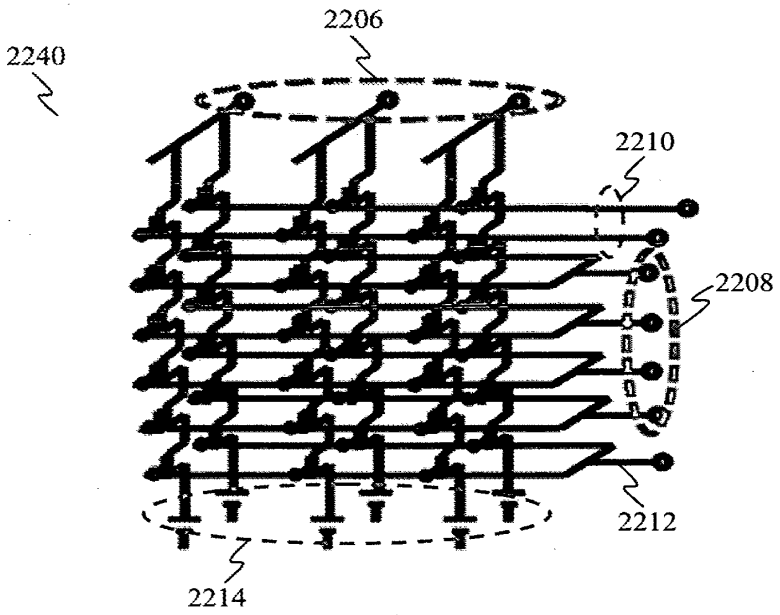


FIG. 22B

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2011/000222

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H01L 29/772 (2006.01) ***B82Y 10/00*** (2011.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPI and EPODOC: nanowire, nanorod, transistor, fet, mosfet, vertical, perpendicular, junction and similar terms
Googlepatents and espacenet: nanowire, vertical, transistor, junctionless and similar terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	US 2007/0222074 A1 (BAKKERS et al.) 27 September 2007	
X	Abstract; Paragraphs 1, 8, 9, 13, 17, 18, 47-61; Figures 1a-1k	1-15
Y		16-26, 29-42
	WO 2009/072983 A1 (AGENCY FOR SCIENCE, TECHNOLOGY AND RESEARCH) 11 June 2009	
X	Figures 4A-4F	27, 28
Y	Paragraph 52; Figure 2A; Page 14 line 25 – Page 15 line 11	16-26, 29-42

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 August 2011	08 August 2011
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **ANDREW WALKER** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6222 3676

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG2011/000222

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	2007222074	CN	1957477	EP	1754260	JP	2008500719
		WO	2005117131				
WO	2009072983	JP	2011507230	US	2011018053		

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX

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Espacenet

WO2008129478A1 NONVOLATILE MEMORY CELL COMPRISING A NANOWIRE AND MANUFACTURING METHOD THEREOF

Applicants: AKIL NADER [BE],BOUTCHICH MOHAMED [BE],GOLUBOVIC DUSAN [BE],HUERTA ALMUDENA [BE],NXP BV [NL],VAN DUUREN MICHIEL JOS [BE]

Inventors: AKIL NADER [BE],BOUTCHICH MOHAMED [BE],GOLUBOVIC DUSAN [BE],HUERTA ALMUDENA [BE],VAN DUUREN MICHIEL JOS [BE]

Classifications:

IPC ***G11C16/04; H01L21/28; H01L21/336; H01L21/8246; H01L21/8247; H01L27/115; H01L29/06; H01L29/423; H01L29/78; H01L29/788; H01L29/792;***

CPC **B82Y10/00 (EP,US); H01L27/115 (EP); H01L27/11521 (EP); H01L27/11556 (EP); H01L27/11568 (EP); H01L29/0665 (EP); H01L29/0673 (EP); H01L29/0676 (EP); H01L29/40114 (EP); H01L29/40117 (EP); H01L29/42324 (EP); H01L29/4234 (EP); H01L29/66825 (EP); H01L29/66833 (EP); H01L29/7881 (EP); H01L29/792 (EP); H01L29/7926 (EP);** G11C16/0433 (EP); H01L27/0203 (EP);

Priorities: EP07106502A 2007-04-19

Application: WO2008129478A1 2008-04-17

Publication: WO2008129478A1 2008-10-30

Published as: **CN101675502A; EP2147461A1; US2010117138A1; US8546863B2;** WO2008129478A1

NONVOLATILE MEMORY CELL COMPRISING A NANOWIRE AND MANUFACTURING METHOD THEREOF

Abstract

A memory cell (300, 500), the memory cell (300, 500) comprising a substrate (301), a nanowire (302) extending along a vertical trench formed in the substrate (301), a control gate (303) surrounding the nanowire (302), and a charge storage structure (320, 501) formed between the control gate (303) and the nanowire (302).

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
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(43) International Publication Date
30 October 2008 (30.10.2008)

PCT

(10) International Publication Number
WO 2008/129478 A1

(51) International Patent Classification:
H01L 21/28 (2006.01) *H01L 29/792* (2006.01)
H01L 21/336 (2006.01) *G11C 16/04* (2006.01)
H01L 21/8246 (2006.01) *H01L 29/423* (2006.01)
H01L 21/8247 (2006.01) *H01L 29/06* (2006.01)
H01L 27/115 (2006.01) *H01L 29/78* (2006.01)
H01L 29/788 (2006.01)

(21) International Application Number:
PCT/IB2008/051478

(22) International Filing Date: 17 April 2008 (17.04.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
07106502.3 19 April 2007 (19.04.2007) EP

(71) Applicant *(for all designated States except US)*: **NXP B.V.** [NL/NL]; High Tech Campus 60, NL-NL - 5656 AG Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **HUERTA, Almudena** [ES/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **VAN DUUREN, Michiel Jos** [NL/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **AKIL, Nader** [FR/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **GOLUBOVIC, Dusan** [RS/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **BOUTCHICH, Mohamed** [FR/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT).

(74) Agents: **RÖGGLA, Harald** et al.; NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

[Continued on next page]

(54) Title: NONVOLATILE MEMORY CELL COMPRISING A NANOWIRE AND MANUFACTURING METHOD THEREOF

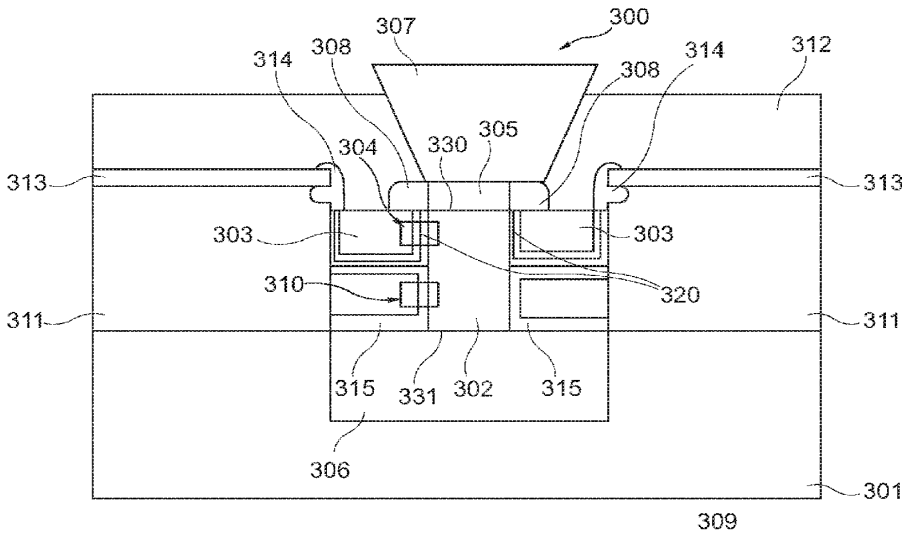


FIG. 3

(57) Abstract: A memory cell (300, 500), the memory cell (300, 500) comprising a substrate (301), a nanowire (302) extending along a vertical trench formed in the substrate (301), a control gate (303) surrounding the nanowire (302), and a charge storage structure (320, 501) formed between the control gate (303) and the nanowire (302).

WO 2008/129478 A1

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

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NONVOLATILE MEMORY CELL COMPRISING A NANOWIRE AND MANUFACTURING METHOD THEREOF

FIELD OF THE INVENTION

The invention relates to a memory cell.

Moreover, the invention relates to a memory array.

Beyond this, the invention relates to a method of manufacturing a memory cell or a memory array comprising a plurality of memory cells.

BACKGROUND OF THE INVENTION

The storage of huge amount of information on computer systems becomes more and more important. Particularly, flash memory arrays may be employed for this purpose.

Two-transistor configurations in a memory cell with an access transistor and a memory transistor allow fast random access and low power program and erase by tunnelling.

Fig. 1 shows a conventional two-transistor configuration with a conventional floating gate memory cell 100.

In a silicon substrate 101, a source region 102, a source and drain region 103 and a drain region 104 are provided as highly doped portions. An access transistor 110 comprises a gate oxide layer 111, an access gate 112, an interpolydielectric (IPD) layer 113, a contact structure 114 and a polysilicon structure 115. Furthermore, a memory transistor 120 is provided which comprises a tunnel oxide layer 111, a floating gate 121, an interpolydielectric layer 113 and a control gate 122.

Thus, Fig. 1 shows a transistor configuration in which the memory transistor 120 is implemented with a floating gate 121. Typically, the gate oxide 111 is approximately 8 nm thick. The memory transistor 120 stores the information (charge) in the floating gate 121. Both tunnel oxide 111 and interpolydielectric 113 layer are thicker than 8 mm due to retention issues.

According to another conventional two-transistor memory architecture which is shown as a memory cell 200 in Fig. 2, an access transistor 210 is provided as well as a memory transistor 220. As a charge carrier storage structure, the memory transistor 220 includes an ONO layer 221, that is a silicon oxide - silicon nitride - silicon oxide layer sequence.

Fig. 2 shows a so-called SONOS memory cell 200 (semiconductor - silicon oxide - silicon nitride - silicon oxide - semiconductor).

The access transistor 110, 210 (basically a MOSFET) which acts like a switch contributes to the selection/inhibition of a memory transistor 120, 220 in a memory array comprising a large number of memory cells 100, 200. The use of an access transistor 110, 210 allows the memory 100, 200 to be fully programmed and erased by Fowler-Nordheim tunnelling and allows to operate the individual memory cells 100, 200 without disturbing cross talk. The memory transistor 120, 220 stores the information that is encoded in stored electric charge. This charge can be injected in a polysilicon floating gate layer 121, a nitride layer of the ONO layer 221, nano-crystal dots, etc.

Fig. 2 therefore illustrates a transistor configuration in which the memory transistor 220 is implemented as a SONOS sequence. In this case, both the access transistor 210 and the memory transistor 220 have a single poly layer 112, 122. The gate oxide 111 of the access transistor 210 has a thickness of approximately 8 nm. The memory transistor 220 stores the information (charge) in a nitride layer 230 of approximately 6 nm thickness and is sandwiched between two insulator (SiO_2) layers, namely a bottom oxide 231 and a top oxide 232 of 2 nm and 8 nm thickness, respectively, whereas the three layers 230 to 232 form the ONO layer 221.

However, it is a problem that a standard planar flash memory cannot be scaled properly beyond 50 nm. Particularly, the scaling of tunnel and control dielectric thickness is limited by concerns for data-retention, yielding low coupling ratios and consequently high operating voltages. Moreover, one of the major limiting scaling parameters for two-transistor flash cells is the length of the access gate transistor 110, 210, which under worst case conditions (Fowler-Nordheim program inhibit) should have a leakage current not exceeding approximately 100 pA with as much as 5 V on its drain. These circumstances result in the fact that future scaled cells suffer of short channel effects and punch through phenomena, as well as of small on-current/off-current ratio, thus reducing the sensing margin.

A possible strategy is to increase the control of the gate over the channel with configurations such as double gate and FinFET transistors to increase the coupling efficiency between the control gate over the floating gate. Higher coupling is needed to scale down the programming voltages so as the memory cell dimensions. However, double gate and FinFET transistors are difficult in manufacture and operation.

US 2003/0015755 A1 discloses a vertical transistor, a memory arrangement

and a method for fabricating a vertical transistor. Particularly, US 2003/0015755 A1 discloses a vertical transistor which has a source region, a drain region, a gate region, and a channel region between the source region and the drain region, which are arranged in a vertical direction in a semiconductor substrate, the gate region having an electrical insulation from the source region, from the drain region and from the channel region and being arranged around the channel region in such a way that the gate region and the channel region form a coaxial structure.

However, with the procedure of forming a memory arrangement according to US 2003/0015755 A1, it may be difficult to obtain a sufficient integration density of memory cells. Furthermore, the manufacturing procedure according to US 2003/0015755 A1 is difficult and cost intensive.

OBJECT AND SUMMARY OF THE INVENTION

It is an object of the invention to provide a memory having a sufficient integration density.

In order to achieve the object defined above, a memory cell, a memory array, and a method of manufacturing a memory cell according to the independent claims are provided.

According to an exemplary embodiment of the invention, a memory cell is provided, the memory cell comprising a substrate, a nanowire (particularly an oblong nanowire) extending along a vertical trench formed in the substrate, a control gate surrounding the nanowire, and a charge storage structure formed between the control gate and the nanowire.

According to another exemplary embodiment of the invention, a memory array is provided, the memory array comprising a plurality of memory cells having the above-mentioned features and formed in the (common) substrate.

According to still another exemplary embodiment of the invention, a method of manufacturing a memory cell is provided, the method comprising forming a vertical trench in a substrate, forming a nanowire (particularly an oblong nanowire) extending along the vertical trench, forming a control gate surrounding the nanowire, and forming a charge storage structure between the control gate and the nanowire.

The term "memory cell" may particularly denote a physical structure (such as a layer sequence) which allows to store information in an electronic manner. An amount of

information stored in a memory cell may be 1 bit (which may be encoded, for instance, in the presence or absence of charge carriers in a dedicated structure) or may be more than 1 bit (which may be encoded, for instance, in the amount of stored charge and/or the type of the charge carriers, that is to say positively or negatively charged charge carriers).

The term "substrate" may denote any suitable material, such as a semiconductor, glass, plastic, etc. According to an exemplary embodiment, the term "substrate" may be used to define generally the elements for layers that underlie and/or overlie a layer or portions of interest. Also, the substrate may be any other base on which a layer is formed, for example a semiconductor wafer such as a silicon wafer or silicon chip.

The term "nanowire" may denote a wire-like structure of dimensions in the order of magnitude of several to several hundreds of nanometers (and may also cover larger or smaller dimensions). Many different types of nanowires may be used for embodiments of the invention, including semiconducting nanowires (for instance made of silicon, germanium, InP, GaN, etc.), metallic nanowires (for instance nickel, platinum, gold), and nanotubes, particularly carbon nanotubes (intrinsic or doped). According to an exemplary embodiment of the invention, such nanowires may form the channel of a transistor.

The term "oblong nanowire" may denote that the length of the nanowire is larger, particularly significantly larger, than a dimension perpendicular to the length extension. In other words, typical nanowires may exhibit aspect ratios (the ratio between length to width) of more than one, particularly of more than 2, more particularly of more than 5, or up to 1000 or more. For instance, a tubular nanowire may have a length of 50 nm to 70 nm and may have a diameter of 10 nm.

The term "charge storage structure" may particularly denote a structure that is specifically adapted to allow introducing electric charge in this structure by tunnelling or other programming procedures. The charge storage structure may be adapted in a manner that this charge is stored and remains stored within the structure for a sufficiently long time. Examples for appropriate charge storage structures are a floating gate, a nitride layer of an ONO layer sequence, etc.

The term "source/drain region" may particularly denote a source region or a drain region. Since the functionality of a source region and a drain region may depend on the operation mode of a transistor, for instance voltages applied thereto, the term source/drain region may denote a structure which can act as a source region or as a drain region.

The term "vertical trench" may denote an oblong blind hole formed in a surface

and extending inside of the substrate. In other words, a substrate usually has a main surface, and the trench is usually formed perpendicularly to this main surface. However, the term "vertical" may cover also embodiments in which a certain deviation from the 90° angle between trench and main surface of the substrate is present, but in which the trench still has a relatively steep orientation inside of the material of the substrate.

According to an exemplary embodiment of the invention, a method of producing memory cells is provided in which vertical nanowires are grown or are formed using an etching procedure as channels of transistors of the memory cells, wherein a gate stack may be partially or all-wrapped around the respective channel, for instance to form a coaxial structure. Furthermore, the nanowires may be grown within trenches surrounded by electrically insulating structures such as silicon oxide that provides electrical isolation between word lines in a memory array configuration. By taking this measure, it may be made possible to improve scaling issues. In other words, an area required for a memory array may be scaled down to a great extent with enhanced control over the channel. Beyond this, efficient process integration is possible to build memory arrays with vertical nanowire-based transistors.

A measure for advanced solid-state nanoelectronic devices is the surrounding gate geometry. Transistors having a surrounding gate structure have proper sub-threshold behaviour due to the high coupling efficiency and a significant reduction of short channel effects compared to double gate or FinFET devices. Silicon nanowire-based transistors exhibit advantageous properties. Moreover, vertically aligned nanowires are capable to reduce the processing complexity and result in ultra high transistor densities as the transistor geometry is pushed into the third dimension. 3D geometry also shows more relaxed conditions regarding transistor lengths that greatly helps as the access transistor should sustain 5V on its drain at low leakage current. By forming a nanowire within a trench, the growing or etching procedure may be very simple and may allow to mechanically protecting the relatively sensitive nanowire.

Such memory cells may be implemented in a SONOS (semiconductor - silicon oxide - silicon nitride - silicon oxide - semiconductor) or floating gate architecture with a single transistor or a two-transistor configuration in stand-alone flash memories. In other words, an array of 3D memory cells with one or two nanowire-based transistors may be provided for ultrahigh integration densities. Particularly, a vertical memory cell may be built around a nanowire with a gate stack of one or more transistors all wrapped around the nanowire.

More particularly, an easy process integration scheme is provided to build

arrays of three-dimensional memory cells comprising nanowire-based transistor configurations with one or two transistors. Such a cell design may enable the reduction of the whole memory array to a great extent. Moreover, as the gate stack may be all-wrapped around the nanowire, a high coupling coefficient may be obtained. By providing an all-wrapped around gate for a vertical nanowire, positioning the channel as a vertical nanowire may allow to obtain ultrahigh densities. As the gate may be all-wrapped around, there is full control of the gate over the channel that prevents short channel effects and increases the drive current density (improved access time). For an embodiment of a floating gate flash, the coupling characteristic between the control gate and the floating gate may be greatly improved, since the control gate may be all-wrapped around the floating gate. In an embodiment in which a nanowire is grown (for instance on a catalyst or precursor), there is no surface etching needed which results in a simple manufacturing architecture. In case of growing nanowire, the surface may be smooth so that it is possible to gain mobility (less traps).

By using a two-transistor configuration with an access transistor and a memory transistor, it may be possible to allow for a fast random access and a low power operation, since the program procedure and the erase procedure can be fully realized by tunnelling. The access transistor (basically a MOSFET transistor), which may act like a switch, may help in the selection/inhibition of the memory transistor within the array. The use of the access transistor may allow the memory to be fully programmed and erased by Fowler-Nordheim tunnelling.

It may be possible to select the dimensions of the nanowire width to be approximately ten (10) nm or several ten nanometers, which may be particularly advantageous in combination with the use of nitride spacers at the drain which reliably prevents any electrical contact between the drain and the gate, thus the nanowire can be much smaller than the contact. Therefore, an increased integration density may be obtained. It is also possible to manufacture the gate to be self-aligned to the trenches at the beginning of the process integration to isolate the word lines. When trenches are used, one mask may be saved which results in reduced costs. Thus, in order to define the source lines and the gates, this may be performed within one mask. The trench formation may require one additional mask, but then the source lines and the gate lines may be self-aligned to the trenches. Furthermore, the use of silicon nanowires may be cheap in manufacture.

According to an exemplary embodiment, a flash cell may be provided which is a non-volatile memory being able to store its information for a long period of time without

refreshment.

Thus, it is possible to provide a memory array with an area that is scaled down to a great extent with enhanced control over the channel (reduced drain-induced barrier lowering, short channel effects, etc.) and drive current density (improved access time). A nanowire based memory cell according to an exemplary embodiment of the invention does not suffer from corner effects, in contrast to FinFET approaches.

The coupling efficiency between the control gate over the floating gate may be greatly improved as the control gate is all wrapped around the floating gate. The process integration is relatively easy and makes it feasible to build memory arrays with a large number of cells comprising vertical nanowire-based transistors. The process integration covers several memory cell implementations with a memory transistor implemented as a floating gate or as a SONOS, with or without an access transistor, etc.

The 3D geometry of a cell has the advantage that the channel current may flow vertically so that there is no need to scale down the length of the transistors. As the length of the transistor can be relatively long due to the vertical integration, it is possible to store multiple bits in the charge storage layer or structure, for instance with a SONOS memory transistor programmed by hot carrier injection (similar to an NROM).

Therefore, vertical nanowires may be grown as a channel of transistor of the memory cell, where the gate stack may be all-wrapped around a channel. The nanowire may be grown within trenches surrounded by silicon dioxide which may provide isolation between the bit lines in an array configuration.

Next, further exemplary embodiments of the memory cell will be explained. However, these embodiments also apply to the memory array and to the method.

The memory cell may comprise a first source/drain region (particularly a drain) coupled to a substrate external end portion of the nanowire and may comprise a second source/drain region (particularly a source) coupled to a substrate internal end portion of the nanowire. In other words, the end portion of the nanowire which is deepest buried within the trench connected to the substrate may form the second source/drain region, whereas the end portion of the nanowire which is closer to the main surface of the layer sequence (close to the bit lines) may form the first source/drain region. The first and second source/drain regions may be doped, for instance n^+-doped or p^+-doped. In contrast to this, the nanowire may be intrinsically or weakly doped, for instance may be n-doped or p-doped. Thus, the nanowire may form the channel portion of a nanowire-based field effect transistor.

A contact structure may be coupled to the first source/drain region. Such a contact structure may be an electrically conductive portion which provides an electric coupling between the nanowire and an environment external to the memory cell which may be formed as a monolithically integrated circuit. Thus, such a contact structure may be a filled via and may be made of materials such as highly doped polysilicon, silicide, or may be made from a metallic material such as copper or nickel.

The memory cell may comprise an electrically insulating spacer structure surrounding the first source/drain region for securely electrically decoupling the first source/drain region from the control gate. Such an electrically insulating spacer structure may be formed on a laterally limited layer sequence, whereas the lateral walls of such a layer sequence may be covered with an electrically insulating material such as silicon dioxide (SiO_2) or silicon nitride (Si_3N_4). It may be highly advantageous to reliably decouple the source/drain region from the control gate to avoid undesired current paths or leakage currents.

The contact structure may be broader than the first source/drain region in a lateral direction. Such a lateral direction may be orthogonal to the vertical direction along which the nanowire extends. When the nanowire is smaller than the contact, an undesired electrically contact between the drain and the gate may be prevented.

The charge storage structure may comprise at least one of the group consisting of a floating gate, an ONO structure, a silicon nitride structure, and a nano-crystal dot structure. A floating gate may be an electrically conductive portion such as a polysilicon structure in which charge carriers may be stored by tunnelling or other programming procedures. An ONO structure is a silicon oxide - silicon nitride - silicon oxide layer sequence, wherein charge carriers may be permanently stored in the nitride layer by Fowler-Nordheim tunnelling or the like. A simple silicon nitride layer may also serve as a basis for a proper charge storage structure, for instance in an embodiment in which miniature dimension of the memory cell is desired. However, also nano-crystals may be used to store charge carriers such as electrons or holes.

The control gate may surround the nanowire along its entire circumference. In other words, the control gate may be provided with a blind hole through which the nanowire extends, thereby forming a coaxial nanowire gate structure. This may allow for an accurate control of the electrical conductivity of the nanowire by applying an electric voltage to the control gate.

A cross-section of the nanowire may have a diameter of less than 100 nm,

particularly of less than fifty (50) nm, more particularly of less than twenty (20) nm. According to a preferred embodiment, the nanowire has a diameter of 10 nm that allows to properly control conductivity by the surrounding gate.

Furthermore, an access gate may be provided surrounding the nanowire. The access can be part of an access transistor which may be considered as a switch which can be switched on or off by applying a voltage to the access gate. By such a two-transistor configuration, namely a configuration with an access gate and a control gate, a properly controllable memory system may be provided.

The access gate may be buried deeper within the trench than the control gate. In other words, a current flow may occur from the second source/drain region through the portion of the nanowire adjacent to the access gate, through the portion of the nanowire adjacent to the control gate, and to the first source/drain region, or vice versa.

The nanowire may be a semiconductor nanowire (such as made from silicon, germanium, etc.), a carbon nanotube (electrically conductive or semiconductive), a silicon nanowire or a group III-group V nanowire such as made of gallium arsenide.

Next, further exemplary embodiments of the memory array will be explained. However, these embodiments also apply to the memory cell and to the method.

The memory array may comprise a plurality of memory cells, particularly thousands or millions or billions or more of memory cells. These may be arranged in a matrix-like manner, wherein each of the individual memory cells can be addressed by bit lines and word lines, as known by the skilled person.

For programming, a memory cell may be selected by activating a specific access transistor, and by applying corresponding voltages to the control gate and to the source/drain connections so as to induce tunnelling or other programming effects which inject charge carriers in the charge carrier structure. After such a programming procedure, the charge carriers may remain permanently or for a long time in the charge carrier structure.

For reading out the stored information, a memory cell may again be selected by applying a readout voltage to the access gate. The current flow along the nanowire may then depend on the conductivity of the channel portion adjacent to the memory transistor, and therefore from the fact whether the charge carrier structure has been provided with charge carriers during a previous programming phase or not. Therefore, a current flowing between the source/drain regions depends on the stored information and is indicative of the stored information.

In order to avoid or suppress artefacts (when programming or reading out the memory cell or in a passive mode of the memory cell) due to leakage or tunnelling effects, electrically insulating regions may be formed between adjacent trenches formed in the same substrate. This may allow to reliably decouple different word lines.

A common control gate may be provided for a sub-group of at least two of the plurality of memory cells. For instance, a single assigned control gate may control a column or row of memory cells. This may allow for a secure readout and an efficient architecture.

The memory array may be a two-dimensional arrangement of the memory cells, but may also be a three-dimensional stack of memory cells. Particularly, the latter measure further increases the storage volume and the integration density.

Next, further exemplary embodiments of the method will be explained. However, these embodiments also apply to the memory cell and to the memory array.

The nanowire may be formed by a growing procedure. For this purpose, a precursor may be provided in the trench so as to define a location at which the growth of the nanowire starts. This is a very simple procedure that allows to accurately define a portion at which a nanowire grows.

Alternatively, the nanowire may be formed by an etching procedure using a wafer (n-type or p-type). In such a scenario, the trench may be filled with material forming the nanowire, and a subsequent etching procedure may then define the lateral extension of the nanowire.

The method may be carried out in CMOS technology. Since the described procedures are compatible with CMOS technology, it may be possible to form a memory purely in semiconductor technology.

In an embodiment of the invention in which a floating gate configuration is implemented, programming a memory cell may be performed by applying a voltage of 12 V to 15 V to the control gate, and by simultaneously grounding the two source/drain regions (i.e. source and drain). Then, charge carriers may be injected into the floating gate by Fowler-Nordheim tunnelling. Since embodiments of the invention significantly improve the coupling efficiency, the programming voltage may be reduced compared to conventional approaches. Reading out a memory cell may be performed by applying a voltage of 1 V to the control gate, by applying a voltage of 0.5 V to the drain and by grounding the source. A voltage of 1 V may be applied to the access gate. Erasing a memory cell may be performed by applying a voltage of -12 V to -15 V to the control gate, and by simultaneously grounding the two source/drain

regions (i.e. source and drain), so that charge carriers may be injected into or removed from the floating gate by Fowler-Nordheim tunnelling. The given voltage values are only examples and may vary over a broad interval. They may depend on dimensions, materials and electronic characteristics of the memory cell such as the threshold voltage of the transistor(s).

For any method step, any conventional procedure as known from semiconductor technology may be implemented. Forming layers or components may include deposition techniques like CVD (chemical vapour deposition), PECVD (plasma enhanced chemical vapour deposition), ALD (atomic layer deposition), or sputtering. Removing layers or components may include etching techniques like wet etching, vapour etching, etc., as well as patterning techniques like optical lithography, UV lithography, electron beam lithography, etc.

Embodiments of the invention are not bound to specific materials, so that many different materials may be used. For conductive structures, it may be possible to use metallization structures, silicide structures or polysilicon structures. For semiconductor regions or components, crystalline silicon may be used. For insulating portions, silicon oxide or silicon nitride may be used.

The structure may be formed on a purely crystalline silicon wafer or on an SOI wafer (Silicon On Insulator).

Any process technologies like CMOS, BIPOLAR, and BICMOS may be implemented.

The aspects defined above and further aspects of the invention are apparent from the examples of embodiment to be described hereinafter and are explained with reference to these examples of embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in more detail hereinafter with reference to examples of embodiment but to which the invention is not limited.

Fig. 1 shows a conventional two-transistor memory cell comprising an access transistor and a floating gate memory transistor.

Fig. 2 shows a conventional two-transistor memory cell comprising an access transistor and an ONO memory transistor.

Fig. 3 shows a cross-sectional view of a memory cell comprising an access

transistor and an ONO memory transistor according to an exemplary embodiment of the invention.

Fig. 4 shows a partial plan view of the memory cell of Fig. 3.

Fig. 5 shows a cross-sectional view of a memory cell comprising an access transistor and a floating gate memory transistor according to an exemplary embodiment of the invention.

Fig. 6 shows a partial plan view of the memory cell of Fig. 5.

Fig. 7 to Fig. 30 show layer sequences (cross-sectional views and partial plan views) obtained during carrying out a method of forming the memory cell of Fig. 3 according to an exemplary embodiment of the invention.

Fig. 7 to Fig. 17, Fig. 31 to Fig. 46 show layer sequences (cross-sectional views and partial plan views) obtained during carrying out a method of forming the memory cell of Fig. 5 according to an exemplary embodiment of the invention.

Fig. 47 to Fig. 58 show layer sequences (cross-sectional views and partial plan views) obtained during carrying out another method of forming a nanowire according to an exemplary embodiment of the invention.

DESCRIPTION OF EMBODIMENTS

The illustration in the drawing is schematical. In different drawings, similar or identical elements are provided with the same reference signs.

In the following, referring to Fig. 3, a memory cell 300 according to an exemplary embodiment of the invention will be explained.

The memory cell 300 comprises a substrate 301 that is an n-type silicon wafer. An oblong nanowire 302 extends along a vertical trench formed in the substrate 301. Furthermore, a control gate 303 is provided which surrounds the nanowire 302 in a coaxial manner along a portion of the vertical extension of the nanowire 302. A charge storage structure 304 is formed as an ONO layer sequence and is arranged between the control gate 303 and the nanowire 302. Actually, the charge will be stored in the nitride layer of the ONO layer sequence 304.

The memory cell 300 further comprises a first source/drain region 305 (which may particularly act as a drain) and is formed by an n^+-doped silicon material. The first source/drain region 305 is coupled to a substrate external end portion 330 of the nanowire

302. The first source/drain region 305 may be a doped portion of the nanowire 302 or may be configured as a separate component. A buried second source/drain region 306 (which may particularly act as a source) is provided in the substrate 301 and is another n^+-doped portion. The second source/drain region 306 is coupled to a substrate internal end portion 331 of the nanowire 302. The second source/drain region 306 may be a portion of the substrate 301 or may be configured as a separate component. A contact structure 307 of an electrically conductive material is provided and is electrically coupled to the first source/drain region 305. Beyond this, an electrically insulating spacer structure 308 surrounds the first source/drain region 305 and is adapted for electrically decoupling the first source/drain region 305 from the control gate 303.

As can be taken from Fig. 3, the contact structure 307 is broader (in a horizontal direction of Fig. 3) than the first source/drain region 305. The control gate 303 circumferentially surrounds the nanowire 302 entirely, i.e. along its entire diameter. A diameter of the nanowire along a horizontal direction of Fig. 3 is approximately 10 nm.

Furthermore, an access gate 309 is provided below the control gate and is therefore buried deeper within the trench than the control gate 303. The access gate 309 surrounds the nanowire along its entire circumference and along a part of its vertical extension. Depending on a voltage to be externally applied to the access gate 309, the value of the electrical conductivity of a controllable portion 310 of the nanowire 302 may be adjusted so that the access gate 309 serves as an access transistor with the nanowire 302 acting as a channel region.

The memory cell 300 further comprises a lateral silicon oxide (SiO_2) structure 311. On a surface of the structure 300, an electrically insulating layer 312 is provided, which may also be made from silicon oxide (SiO_2). A silicon nitride layer 313 separates the electrically insulating layers 311 and 312. Furthermore, an electrically insulating spacer structure 314 is provided. With regard to its environment, the access gate 309 is electrically insulated by an encapsulation structure 315.

In a similar manner, the control gate 303 is partially encapsulated by the ONO layer sequence 304, that is to say by a sequence comprising a first silicon oxide layer, a silicon nitride layer and a second silicon oxide layer.

Fig. 3 shows a cross-section of the memory cell 300 with a two-transistor configuration, namely the described access transistor and the memory transistor, wherein the memory transistor is implemented in a SONOS design. Possible misalignments of the contact

307 with respect to the source/drain region 305 are indicated schematically in Fig. 3.

The intrinsically doped silicon nanowire 302 with an approximate width/diameter of 10 nm or tens of nanometers forms the channel (n-channel) of the access transistor and of the memory transistor and connects drain region 305 and source region 306 which are n-type doped as well but to a higher extent compared to the nanowire 302. The control gate 303/ONO stack 304 (part of the memory transistor) and the access gate 309/gate oxide stack 310 (part of the access transistor) are all wrapped around the channel 302. Since the gate stack 304 and the access gate/gate oxide 310 are all around the channel 302, the controllability of the conductivity of the channel 302 is greatly enhanced. This may lead to a large density drive current and low-density leakage. In the memory cell design, it is taken into account that the contact 307 to the drain 305 may be much larger than the nanowire 302 and that it can also have some misalignment (non-self-aligned contact), this is why nitride spacers 308 may be formed at the drain side 305.

Fig. 4 shows a top view of the cross-section of Fig. 3 where the contact 307 and the silicon oxide passivation layer 312 are not present to make easier the visualization of all the different layers being part of the gate stack around the channel 302.

More particularly, the plan view of Fig. 4 shows a first word line 400 and a second word line 401. However, any desired number of word lines is possible.

An enlarged view 410 is indicated in the overview of Fig. 4 as well. Furthermore, the top oxide, nitride, bottom oxide layer sequence 304, the nanowire 302, the control gate 303 and a nitride spacer 308 are shown as well. Thus, Fig. 4 shows the top view of Fig. 3 without the contact 307 to the drain 305 and the silicon oxide passivation layer 312. The insert 410 shows the different layers within the gate stack all around the channel (nanowire) 302.

In the following, referring to Fig. 5, a memory cell 500 according to another exemplary embodiment of the invention will be explained.

The embodiment of Fig. 5 differs from the embodiment of Fig. 3 particularly in that the ONO layer 304 as a charge storage structure is substituted by a floating gate 501, that is to say by an electrically conductive structure which is surrounded by an electrically insulating encapsulation 502. Therefore, charge carriers (such as electrons or holes) stored in the electrically conductive floating gate 501 which may be made of a polysilicon material, may be kept for a long duration in the floating gate 501 to store information. The conductivity of the channel region 302 adjacent to the storage region 304 depends on the type and amount of

charge carriers located within the floating gate 501.

Therefore, Fig. 5 shows a two-transistor floating gate memory cell configuration 500. In this embodiment, the memory transistor is implemented using the floating gate 501. The principle is similar as for the SONOS memory cell 300. However, in the embodiment of Fig. 5, the control gate 303 - IPD - floating gate 501 - tunnel oxide 502 stack of the memory transistor and the access gate 309 - gate oxide 502 stack of the access transistor are all wrapped around the nanowire 302 serving as a cylindrical channel region with an essentially circular cross-section.

Fig. 6 shows a top view 600 of the memory cell 500 of Fig. 5 without the contact 307 and the silicon passivation layer 312. The insert 610 shows the different layers within the gate stack all around the channel 302 (nanowire). As indicated in the insert 610, the floating gate 501, the tunnel oxide 502 and the nanowire 302 are (partially) covered by the nitride spacer 308.

In the following, referring to Fig. 7 to Fig. 58, embodiments will be explained as to how to build memory cells according to the invention in detail with the whole process integration scheme and some possible variations (such as growing nanowires versus silicon etching of nanowires, one transistor versus two transistor configurations, and floating gate versus SONOS configurations). Silicon oxide has been considered as the dielectric material in these embodiments, although other materials different from silicon oxide (for instance high-k materials or silicon nitride) can also be used for dielectric components. In each of Fig. 7 to Fig. 58, a top view is shown on the left-hand side and a cross-sectional view is shown on the right-hand side.

Fig. 7 shows a layer sequence 700 that consists of an n-type silicon wafer 301. Such an n-type wafer 301 may be used to make a contact to the lower source of a nanowire transistor configuration to be manufactured. A p-well type as a substrate (planar) is not needed in this embodiment, but may be used in other embodiments of the invention.

Fig. 8 shows a layer sequence 800 obtained after having deposited a layer of silicon oxide (SiO_2) 311 which may later serve to isolate the word lines. Thus, an electrically insulating layer 311 is formed on the substrate 301.

Fig. 9 shows a layer sequence 900 obtained after deposition of a layer of silicon nitride 901 on the silicon oxide layer 311.

Fig. 10 shows a layer sequence 1000 that is obtained after depositing and etching an auxiliary layer 1001 (such as a photoresist) for patterning the word lines.

Fig. 11 shows a layer sequence 1100 that is obtained after removing an exposed portion of the layers 901, 311 using the patterned auxiliary layer 1001 as a mask. After having etched a trench 1101 in the layers 901, 311, an exposed portion of the substrate 301 is doped by an n^+-implantation to thereby generate an n^+-doped source region 306. Arrows 1102 indicate the implantation schematically.

Fig. 12 shows a layer sequence 1200 obtained after deposition of a precursor structure 1201 which will be later used to grow a nanowire. Gold may be used to form the precursor structure 1201. Less contaminate materials such as a titanium catalyst may be used as well. The precursor 1201 is deposited onto a specific position within the trench 1101.

Fig. 13 shows a layer sequence 1300 obtained after growing a nanowire 302 on the precursor 1201 which will later form the channel of the access and memory transistor of the memory cell to be manufactured. Optionally, the precursor 1201 is removed, and the auxiliary layer 1001 may be removed as well.

The layer sequence 1400 shown in Fig. 14 is obtained by forming (for instance by thermal oxidation) an electrically insulating layer 1401, for instance of silicon oxide, on the surface of the silicon nanowire 302 and of the source/drain region 306 within the trench 1101. As can be taken from Fig. 14, the grown silicon oxide material 1401 builds a gate oxide 1403 of the access transistor. In a surface region where a higher concentration of a dopant is present, namely on the surface of the source/drain region 306, the oxidation will result in a thicker silicon oxide layer 1402 as compared to a region at the surface of the nanowire 302 which is intrinsically doped. This effect is favourable for providing isolation between the polysilicon (deposited later on) and the source/drain region 306.

The layer sequence 1500 shown in Fig. 15 is obtained by depositing a polysilicon layer 1501 on the layer sequence 1400. The material of the polysilicon layer 1501 may later form the basis for an access gate.

In order to obtain the layer sequence 1600 shown in Fig. 16, the polysilicon structure 1501 is partially removed by CMP ("chemical mechanical polishing").

To obtain the layer sequence 1700 shown in Fig. 17, the polysilicon structure 1501 is then etched selectively to oxide and nitride. The remaining polysilicon will later form the basis for the gate region of the access transistor, denoted with reference numeral 309. The polysilicon material is in situ doped.

In order to obtain a layer sequence 1800 shown in Fig. 18, the exposed portion of the silicon oxide structure 1401 is etched, so that it is selectively removed from the

nanowire 302, and indentations or recesses 1801 may be formed as well as a consequence of the etching procedure.

In order to obtain a layer sequence 1900 shown in Fig. 19, a bottom oxide 1901 of an ONO layer (in a configuration of a SONOS memory transistor) is grown, for instance by thermal oxidation. Again, in the polysilicon region 309, the formed oxide layer 1901 is thicker (see portion 1902) than in the nanowire 302 region providing an insulation (see portion 1903). Particularly, the portion 1902 serves as an electrically insulating portion, and the portion 1903 serves as a bottom oxide of the ONO stack (memory transistor in SONOS design).

In order to obtain a layer sequence 2000 as shown in Fig. 20, a nitride layer 2001 of the ONO stack to be formed is deposited. The deposition procedure may be performed in a manner that the thickness of the layer 2001 will be essentially uniform. Reference numeral 2002 indicates a portion of the nitride layer 2001 of the ONO stack (control gate in SONOS configuration), i.e. a portion in which charge may be stored for encoding information.

In order to obtain a layer sequence 2100 as shown in Fig. 21, a top silicon oxide layer 2101 is deposited, again essentially uniformly. Therefore, as indicated with reference numeral 2102, an ONO (oxide/nitride/oxide) stack is formed.

In order to obtain a layer sequence 2200 shown in Fig. 22, a polysilicon layer 2201 is deposited, forming a basis for a control gate polysilicon structure.

In order to obtain the layer sequence 2300 shown in Fig. 23, the further polysilicon layer 2201 is planarized by CMP ("chemical mechanical polishing").

The layer sequence 2400 shown in Fig. 24 is obtained by selectively etching the polysilicon structure 2201 relative to silicon oxide, thereby constituting the polysilicon control gate 303 of the memory transistor. The polysilicon gate 303 is in situ doped.

In order to obtain the layer sequence 2500 shown in Fig. 25, the exposed portions of the ONO layer 1901, 2001, 2101 are removed. It is not detrimental if the remained ONO layer 1901, 2001, 2101 is not aligned to the control gate 303 polysilicon material, whenever the ONO layer 1901, 2001, 2101 fully covers the region below the control gate 309. It should be prevented that the ONO layer 1901, 2001, 2101 is overetched below the control gate polysilicon material 303. As can be taken from Fig. 25, the described processing manufactures the memory transistor (SONOS) and the access transistor. The memory portion of the ONO layer 1901, 2001, 2101 which actually stores the charge is shown as a portion

illustrated as a rectangular 304.

To obtain the layer sequence 2600 of Fig. 26, nitride spacers 308 are formed to make a contact to the drain (to be formed subsequently feasible). Nitride spacers 314 may be formed as well.

In order to obtain the layer sequence 2700 shown in Fig. 27, a shallow n^+-implantation procedure is performed in order to form the drain region (denoted with reference numeral 305, see Fig. 3 or Fig. 28). This is indicated by arrows 2701 in Fig. 27.

Consequently, an n^+-drain 305 is formed, as indicated in the layer sequence 2800 as shown in Fig. 28.

In order to obtain the layer sequence 2900 shown in Fig. 29, a silicon oxide layer 312 is deposited on the entire surface of the layer sequence 2800.

In order to obtain the layer sequence 3000 shown in Fig. 30, the electrically insulating layer 312 is patterned using a lithography procedure and an etching procedure, thereby forming a through hole in the layer 312 to thereby expose a surface of the drain region 305. Then, electrically conductive material is filled in the hole to form an electrically conductive contact 307.

In other words, manufacture of a contact to the drain 305 stopping at the nitride structure 308 is performed. The contact 307 may be wider than the nanowire 302, and possible misalignments (non-self-aligned contact) may be taken into account and are not harmful thanks to the nitride spacers 308.

The configuration shown in Fig. 30 essentially equals to the configuration shown in Fig. 3.

As an alternative to such an implementation of the memory transistor using a SONOS architecture, it is also possible to manufacture the memory transistor including a floating gate.

For this purpose, the manufacturing procedures described above referring to Fig. 7 to Fig. 17 can be performed and can be combined with the processing procedures that will be explained below referring to Fig. 31 to Fig. 46. As a result, a memory cell similar to that shown in Fig. 5 is obtainable.

Referring to Fig. 31, after forming the access gate 309 (common to SONOS), a tunnel oxide layer 3101 is grown, providing isolation at the polygate side 309.

The layer sequence 3200 shown in Fig. 32 is obtained by depositing polysilicon material for the floating gate, thereby forming a polysilicon layer 3201.

The layer sequence 3300 shown in Fig. 33 is obtained by planarizing the polysilicon structure 3201 by CMP ("chemical mechanical polishing").

To obtain a layer sequence 3400 as shown in Fig. 34, the polysilicon structure 3201 is further etched and therefore selectively removed relative to silicon oxide to build the floating gate.

In order to obtain the layer sequence 3500 shown in Fig. 35, a top portion of the electrically insulating structure 3101 is removed by wet etching.

In order to obtain the layer sequence 3600 shown in Fig. 36, lateral silicon nitride spacers 308, 314 are formed to cover lateral walls of the first source/drain region to be able to contact without harming the device.

In order to obtain the layer sequence 3700 of Fig. 37, a polysilicon overetch procedure is performed, removing the non-exposed portions of the polysilicon material 3201 which is not covered by the nitride spacers 308, 314.

A layer sequence 3800 shown in Fig. 38 is obtained by depositing silicon oxide (SiO_2) as interpolydielectric material, thereby forming a layer 3801 covering the layer sequence 3700.

In order to obtain the layer sequence 3900 shown in Fig. 39, polysilicon material 3901 is deposited on the surface of the layer sequence 3800, thereby providing material for forming the control gate.

In order to obtain a layer sequence 4000 shown in Fig. 40, the polysilicon structure 3901 is planarized by performing a CMP procedure ("chemical mechanical polishing").

In order to obtain the layer sequence 4100 shown in Fig. 41, a control gate 303 are formed by selectively etching polysilicon material of the structure 3901 relative to silicon oxide.

By etching the silicon oxide material on the surface of the layer sequence 4100, the layer sequence 4200 shown in Fig. 42 is obtained.

Subsequently, as shown in a layer sequence 4300 in Fig. 43, an n^+-shallow implantation procedure is performed to form the drain 305 in an upper portion of the nanowire 302 (see Fig. 44). Arrows 4301 indicate this doping procedure schematically.

Consequently, the layer sequence 4400 shown in Fig. 44 shows the second source/drain region 305.

The layer sequence 4500 shown in Fig. 45 is obtained by depositing silicon

oxide material on the surface of the layer sequence 4400, thereby forming an electrically insulating layer 312.

Then, as can be taken from the layer sequence 4600 in Fig. 46, a contact to the drain 305 is provided by item 307. Again, possible misalignments of the contact 307, or the fact that the contact 307 for contacting the drain 305 is larger than the nanowire 302, is not harmful thanks to the nitride spacers 308.

The layer sequence 4600 essentially corresponds to the memory cell 500 shown in Fig. 5.

The above-described Fig. 7 to Fig. 13 explain a procedure of growing a nanowire 302.

Alternatively, the nanowire can also be manufactured by etching a silicon structure, which will be explained in the following.

Therefore, after having manufactured the layer sequence in a manner as shown in Fig. 47 to Fig. 58, the procedures of Fig. 14 to Fig. 46 can be performed in a similar manner.

Fig. 47 shows a view 4700 of a wafer 301.

In order to obtain the layer sequence 4800 shown in Fig. 48, a nitride layer 901 is deposited on the wafer 301 to create a stopping layer for a later CMP ("chemical mechanical polishing") procedure.

As indicated in Fig. 49 showing a layer sequence 4900, an active mask 4901 is applied as a template for forming trenches (such as STI trenches, "shallow trench isolation").

In order to obtain the layer sequence 5000 shown in Fig. 50, the entire wafer 301 is etched, thereby forming STI trenches 5001. The active mask 4901 may be removed.

As shown in Fig. 51 illustrating a layer sequence 5100, the trenches 5001 are filled with silicon oxide material, and an additional amount of silicon oxide material is deposited over this layer structure. Consequently, a silicon oxide layer 5101 is formed.

As shown in Fig. 52 illustrating a layer sequence 5200, silicon oxide material of layer 5101 is removed by CMP ("Chemical Mechanical Polishing"), wherein the silicon nitride material 901 is used as a stopping layer.

In order to obtain the layer sequence 5300 shown in Fig. 53, silicon nitride material 5301 is deposited on top of the layer sequence 5200.

Fig. 54 shows a layer sequence 5400 in which a patterned mask 5401 is shown. The inverse 5401 to the active mask 4901 (instead of light field dark field) is used to remove

the silicon nitride material of top of the silicon wafer 301.

Etching the layers 5301 and 901 results in the layer sequence 5500 shown in Fig. 55.

The nanowire 302 is then defined by etching silicon material of the substrate 301.

The result of such an etching procedure is shown as the layer sequence 5600 in Fig. 56.

Fig. 57 shows a layer sequence 5700 and arrows 5701 indicating an n^+-implantation to define the source and the drain. With a 0° tilt angle of the implantation, it is possible to avoid the doping of the nanowire 302.

A layer sequence 5800 illustrated in Fig. 58 shows the result with the two source/drain regions 305 and 306.

Starting with the layer sequence 5800, it is possible to continue with Fig. 14.

Finally, it should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be capable of designing many alternative embodiments without departing from the scope of the invention as defined by the appended claims. In the claims, any reference signs placed in parentheses shall not be construed as limiting the claims. The word "comprising" and "comprises", and the like, does not exclude the presence of elements or steps other than those listed in any claim or the specification as a whole. The singular reference of an element does not exclude the plural reference of such elements and vice-versa. In a device claim enumerating several means, several of these means may be embodied by one and the same item of software or hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. A memory cell (300, 500), the memory cell (300, 500) comprising
a substrate (301);
a nanowire (302) extending along a vertical trench formed in the substrate (301);
a control gate (303) surrounding at least a part of the nanowire (302);
a charge storage structure (320, 501) arranged between the control gate (303) and the nanowire (302).

2. The memory cell (300, 500) according to claim 1, comprising a first source/drain region (305) coupled to a substrate external end portion (330) of the nanowire (302) and comprising a second source/drain region (306) coupled to a substrate internal end portion (331) of the nanowire (302).

3. The memory cell (300, 500) according to claim 2, comprising a contact structure (307) coupled to the first source/drain region (305).

4. The memory cell (300, 500) according to claim 2, comprising an electrically insulating spacer structure (308) surrounding the first source/drain region (305) for electrically decoupling the first source/drain region (305) from the control gate (303).

5. The memory cell (300, 500) according to claim 3, wherein the contact structure (307) has a larger dimension than the first source/drain region (305) in a direction being perpendicular to the vertical extension of the trench.

6. The memory cell (300, 500) according to claim 1, wherein the charge storage structure comprises one of the group consisting of a floating gate (501), a silicon oxide-silicon nitride-silicon oxide layer sequence (320), a silicon nitride structure, and a nano-crystal dot structure.

7. The memory cell (300, 500) according to claim 1, wherein the control gate (303) surrounds the nanowire (302) along the entire circumference of the nanowire (302).

8. The memory cell (300, 500) according to claim 1, wherein the nanowire (302) has a diameter of less than 100 nm, particularly of less than 50 nm, more particularly of less than 20 nm, in a direction perpendicular to the vertical extension of the trench.

9. The memory cell (300, 500) according to claim 1, comprising an access gate (309) surrounding at least a part of the nanowire (302), particularly surrounding the nanowire (302) along the entire circumference of the nanowire (302).

10. The memory cell (300, 500) according to claim 9, wherein the access gate (309) is arranged deeper within the trench than the control gate (303).

11. The memory cell (300, 500) according to claim 1, wherein the nanowire (302) comprises one of the group consisting of a semiconductor nanowire, a carbon nanotube, a silicon nanowire, and a group III-group V nanowire.

12. The memory cell (300, 500) according to claim 1, adapted as a flash memory cell (300, 500).

13. The memory cell (300, 500) according to claim 1, adapted as a multi-bit memory cell (300, 500).

14. A memory array (400, 600), the memory array (400, 600) comprising a plurality of memory cells (300, 500) according to claim 1 formed in the substrate (301).

15. The memory array (400, 600) according to claim 14, comprising electrically insulating regions (311) between adjacent trenches.

16. The memory array (400, 600) according to claim 14, wherein a common control gate (303) is provided in common for a sub-group of at least two of the plurality of memory cells (300, 500).

17. A method of manufacturing a memory cell (300, 500), the method comprising
forming a vertical trench in a substrate (301);
forming a nanowire (302) extending along the vertical trench;
forming a control gate (303) surrounding at least a part of the nanowire (302);
arranging a charge storage structure (320, 501) between the control gate (303) and the nanowire (302).

18. The method according to claim 17, wherein the nanowire (302) is formed by one of the group consisting of a growing procedure and an etching procedure.

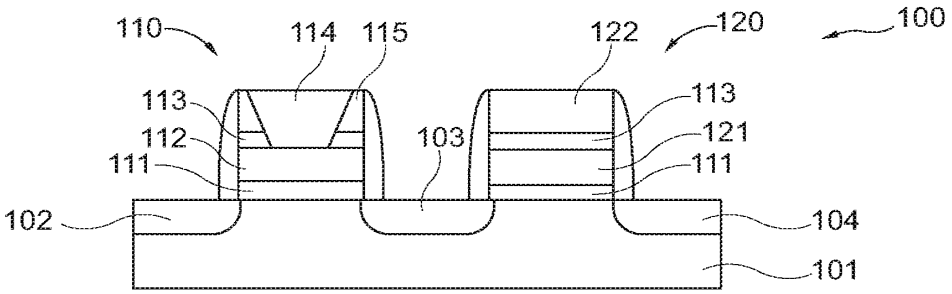


FIG. 1

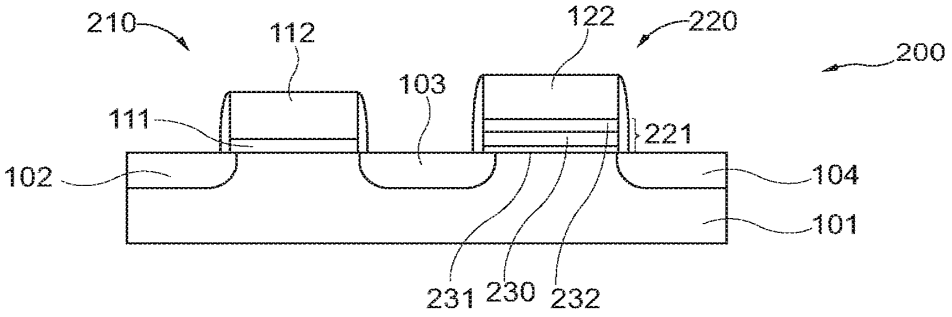


FIG. 2

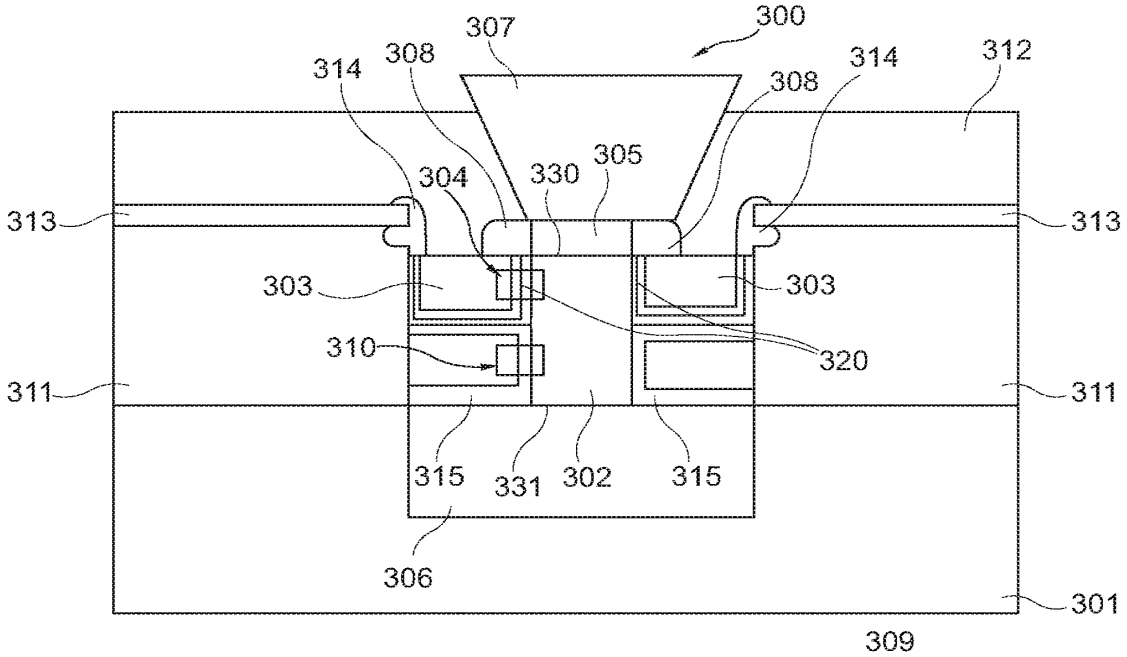


FIG. 3

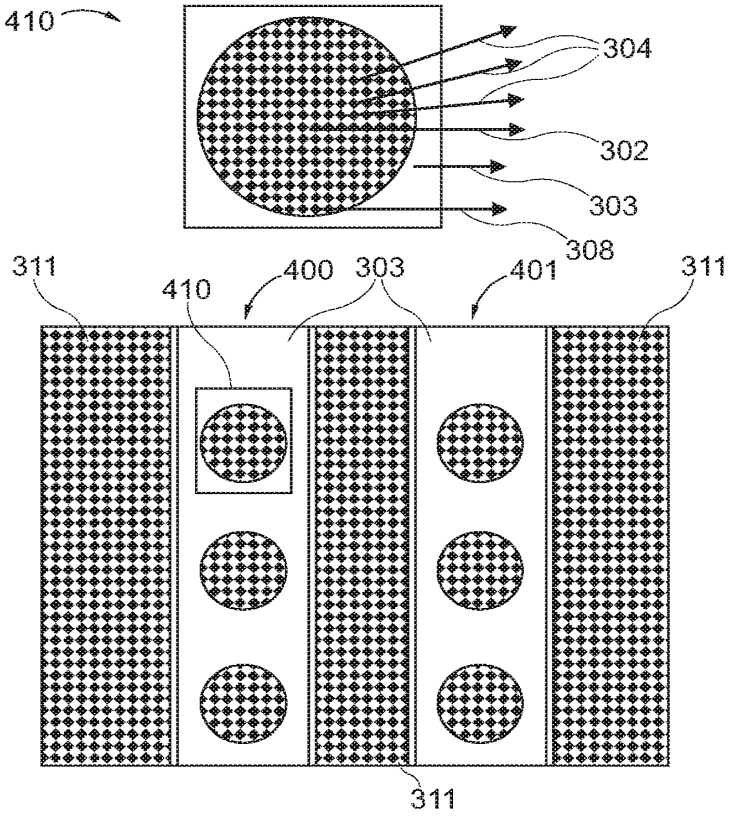

410
304
302
303
308
311
400
303
401
311
410
311

FIG. 4

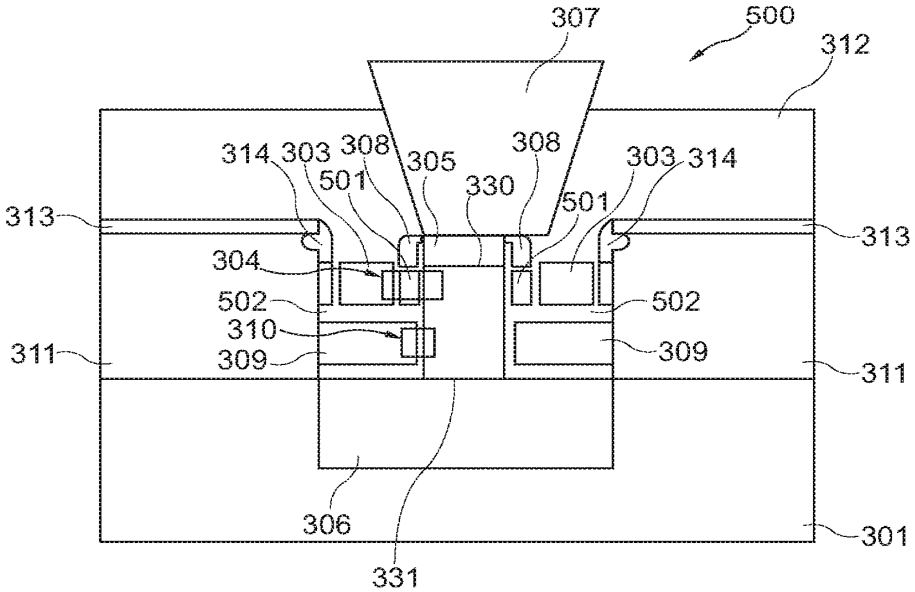

307
500
312
314
303
308
501
305
330
308
501
303
314
313
313
304
502
502
310
309
309
311
311
306
301
331

FIG. 5

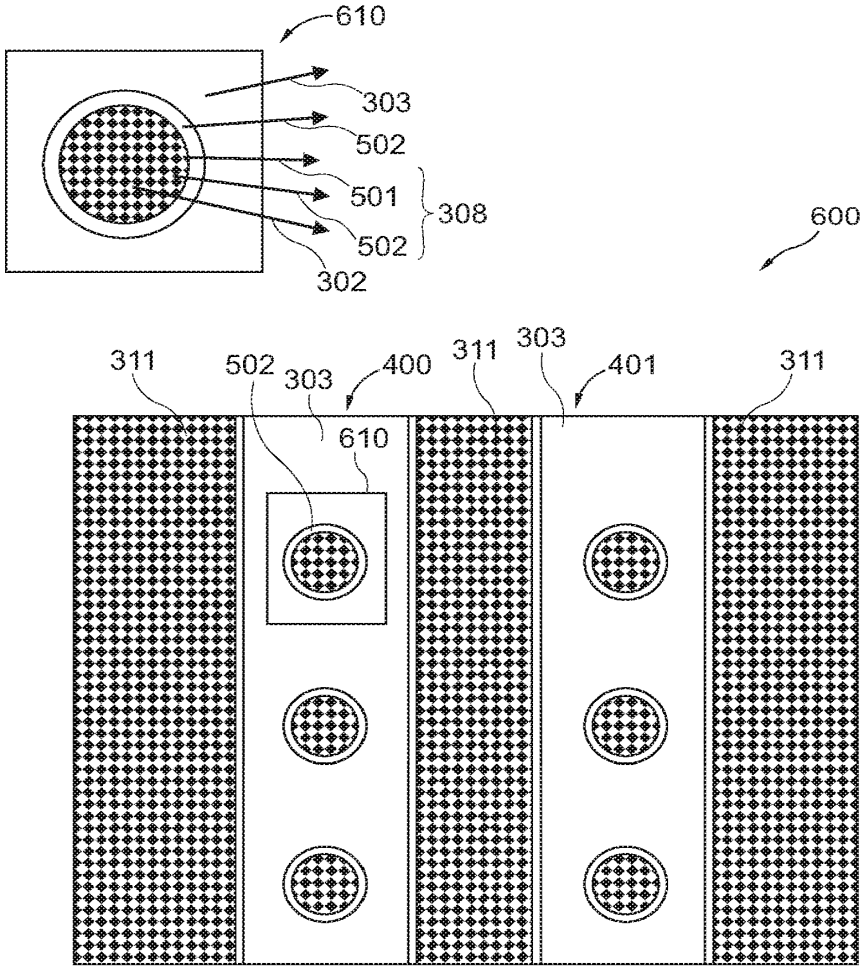

610
303
502
501
308
502
302
600
311
502
303
400
311
303
401
311
610

FIG. 6

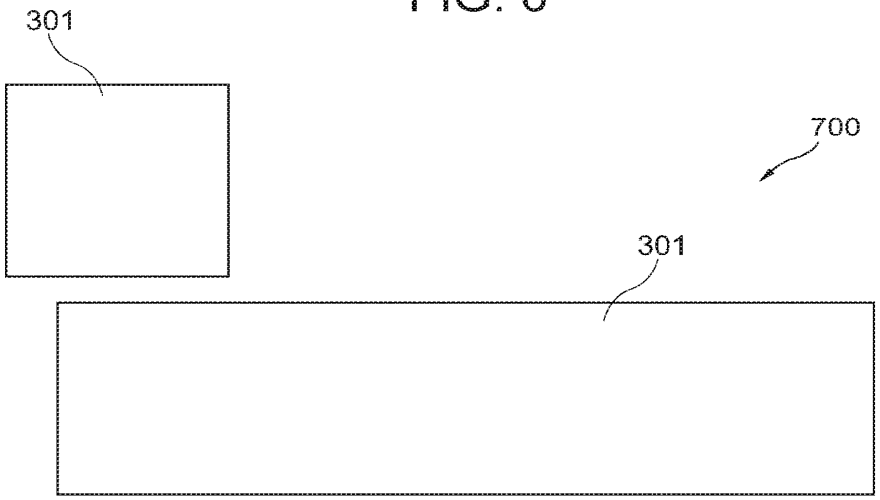

301
700
301

FIG. 7

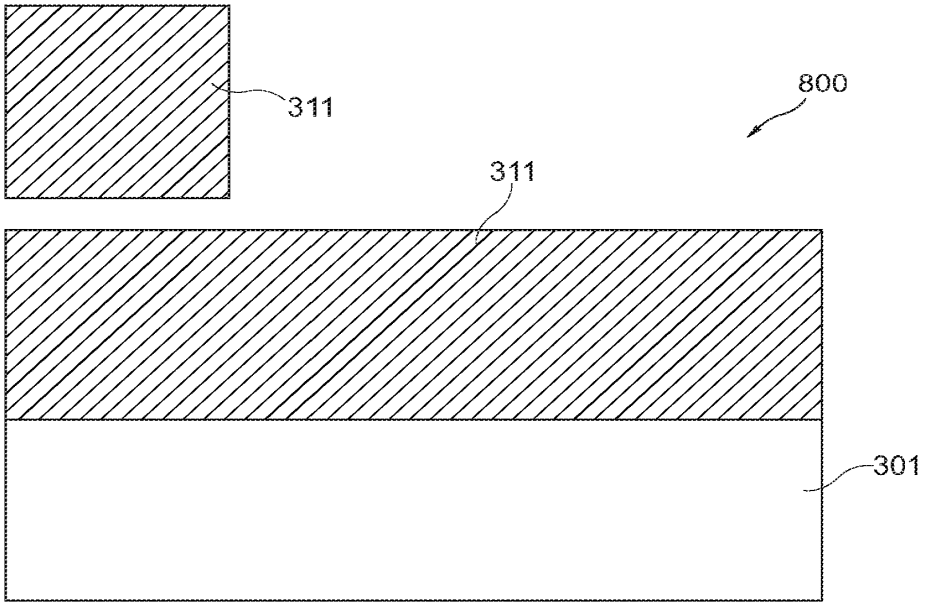


FIG. 8

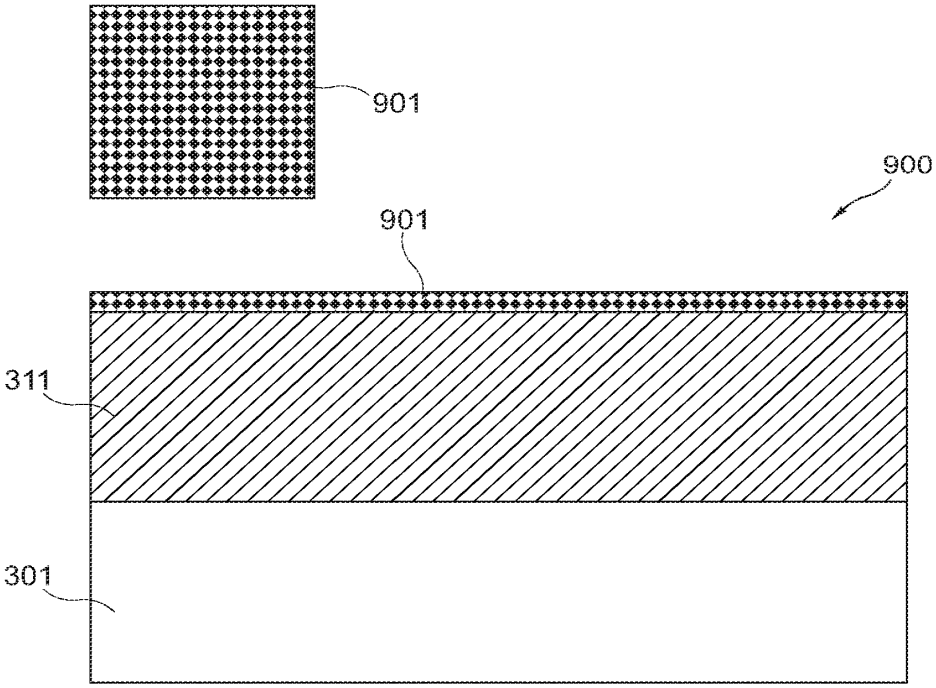


FIG. 9

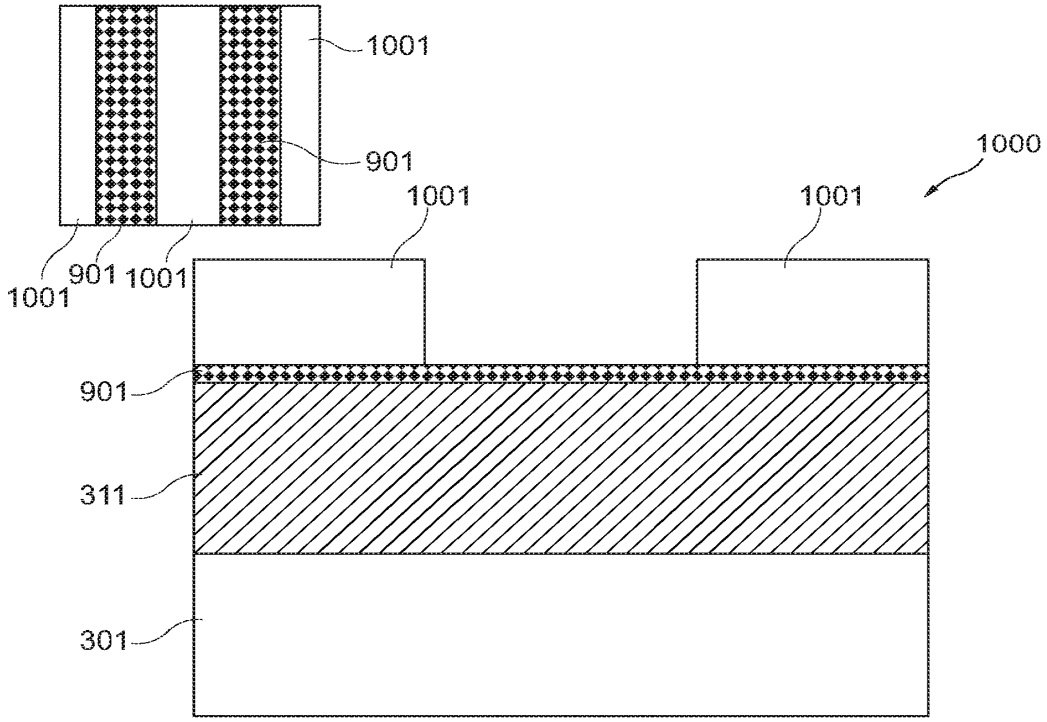

1001
901
1000
1001
1001
1001
901
1001
901
311
301

FIG. 10

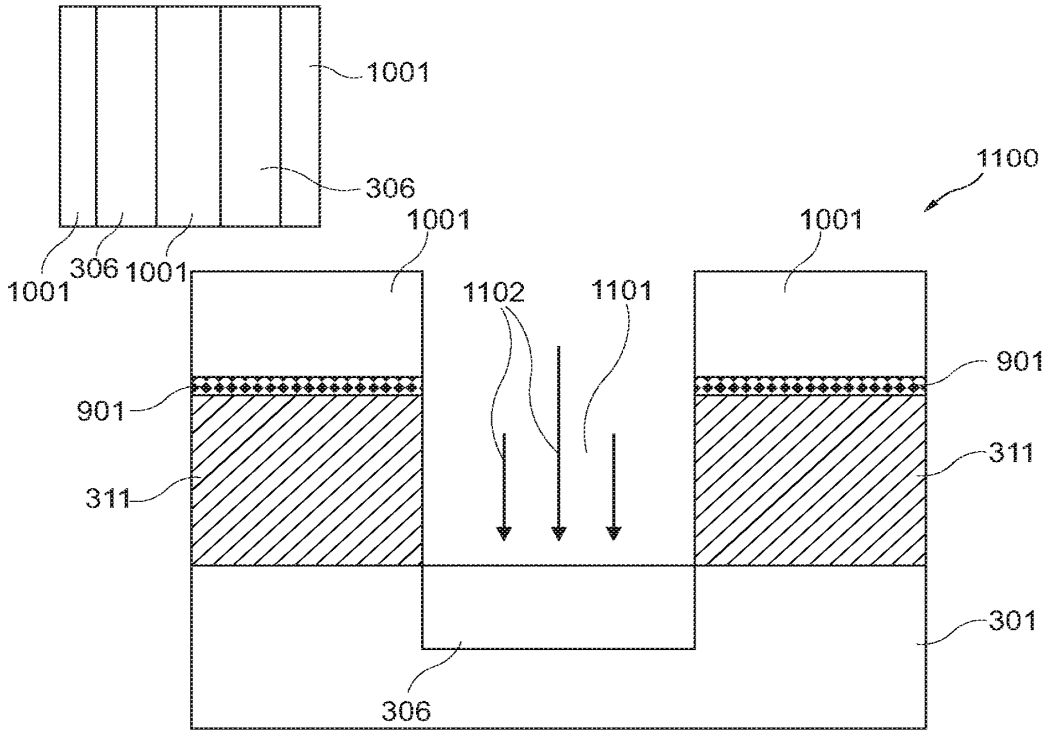

1001
306
1100
1001
1001
1001
306
1001
1102
1101
901
901
311
311
301
306

FIG. 11

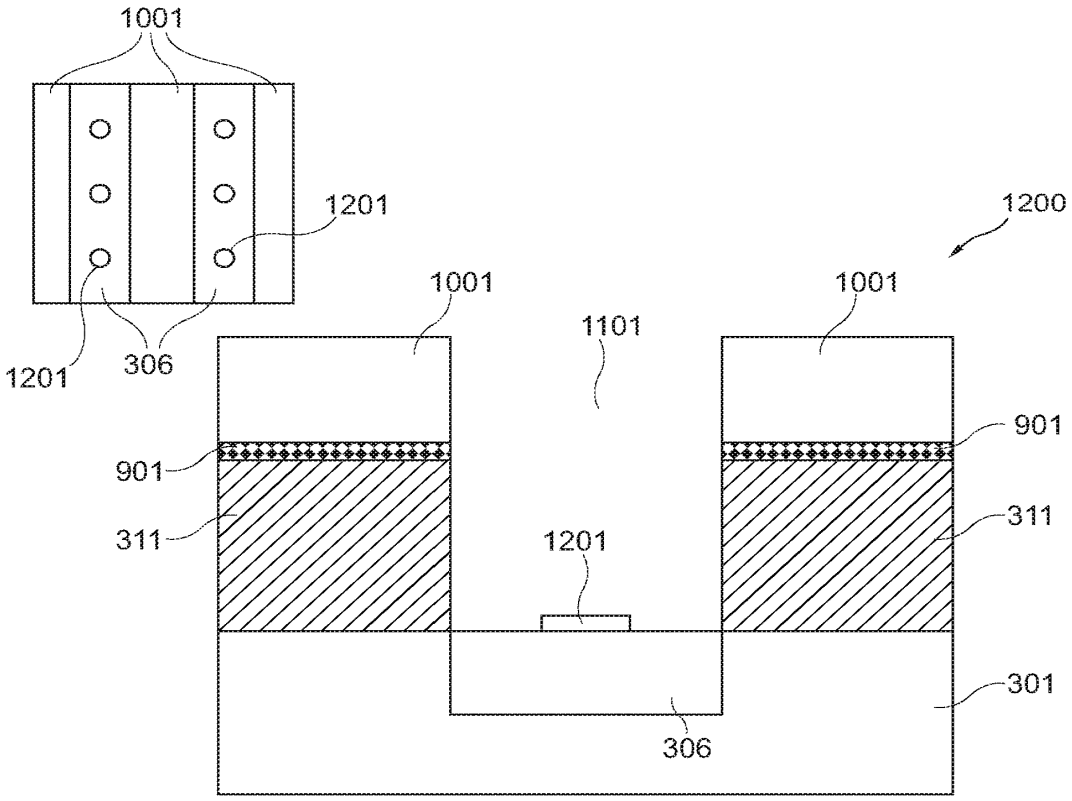

1001
1201
1200
1001
1001
1201
306
1101
901
901
311
311
1201
301
306

FIG. 12

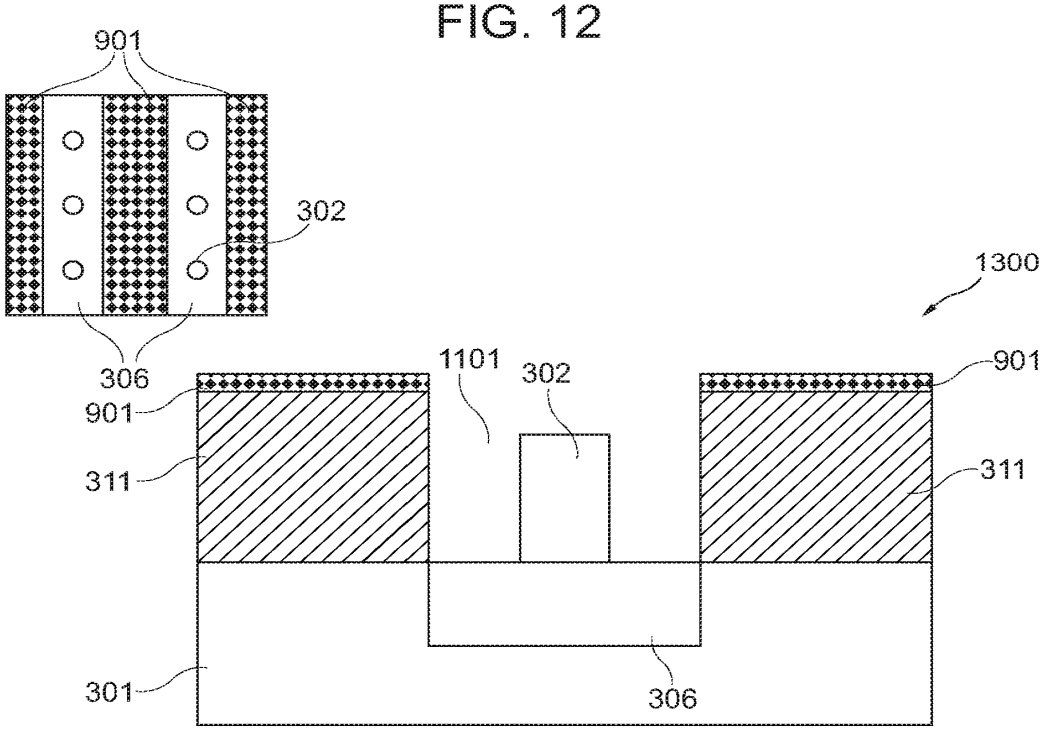

901
302
1300
306
1101
302
901
901
311
311
301
306

FIG. 13

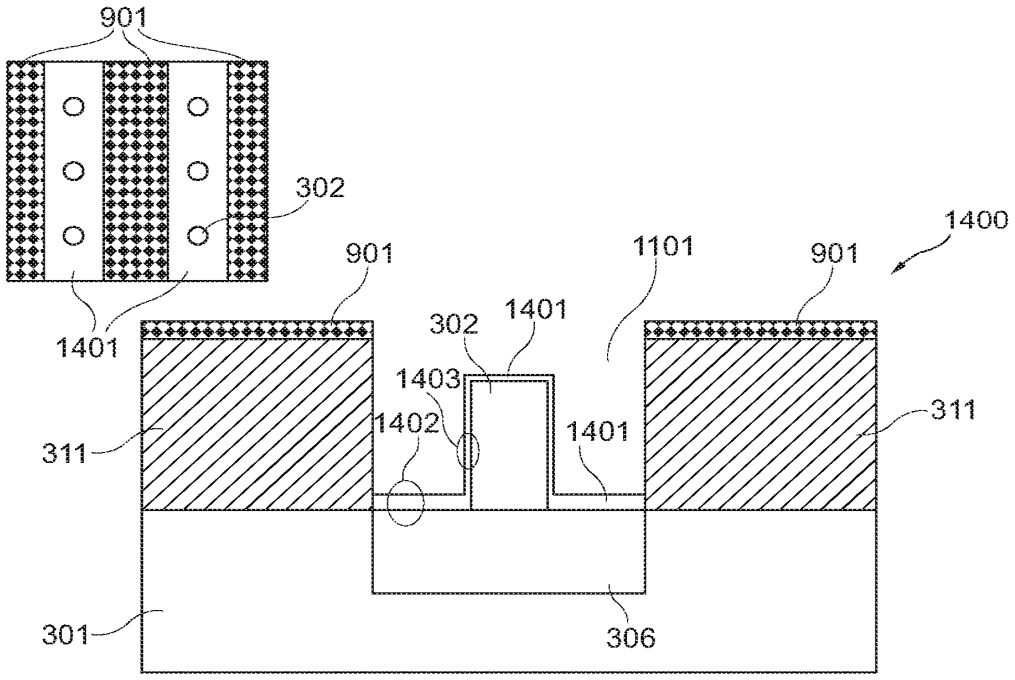

901
302
1400
901
1101
901
1401
302
1401
1403
1402
1401
311
311
301
306

FIG. 14

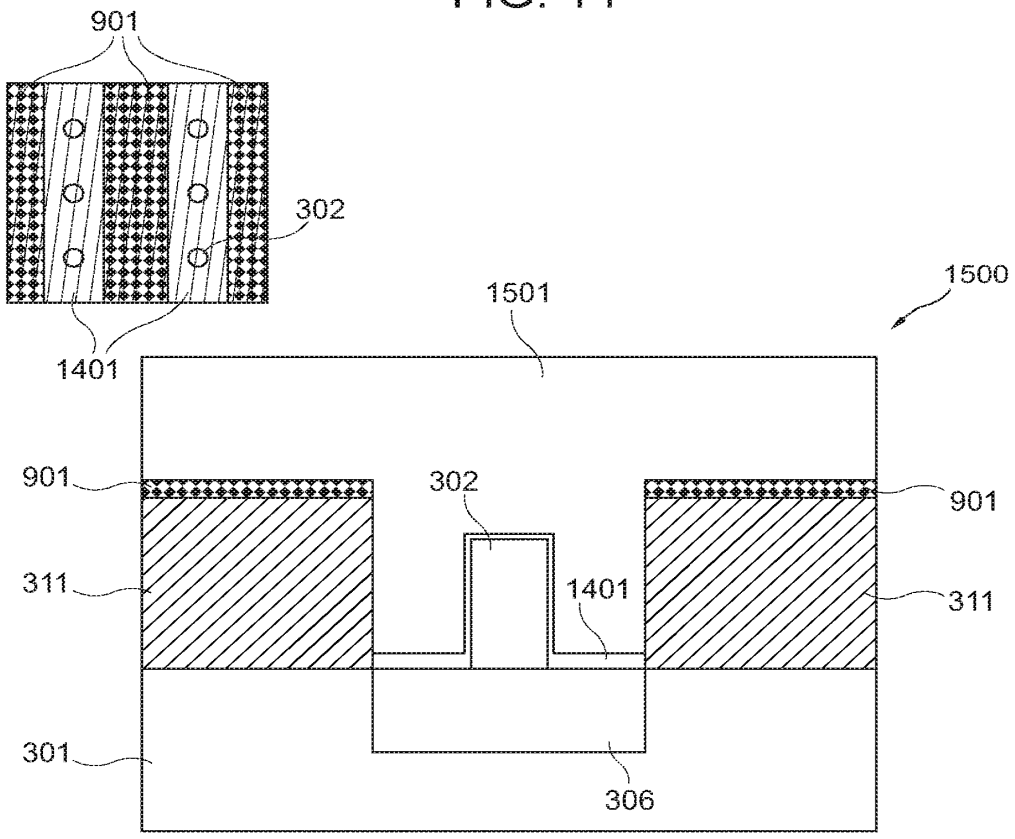

901
302
1500
1501
1401
901
302
901
311
1401
311
301
306

FIG. 15

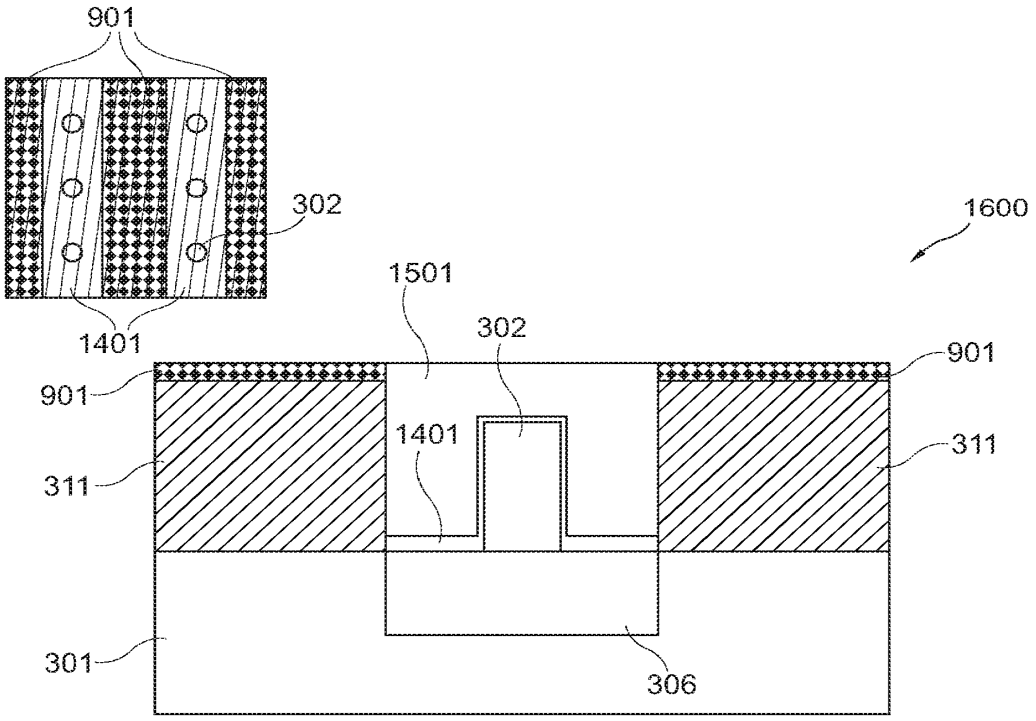

901
302
1600
1501
1401
302
901
901
1401
311
311
301
306

FIG. 16

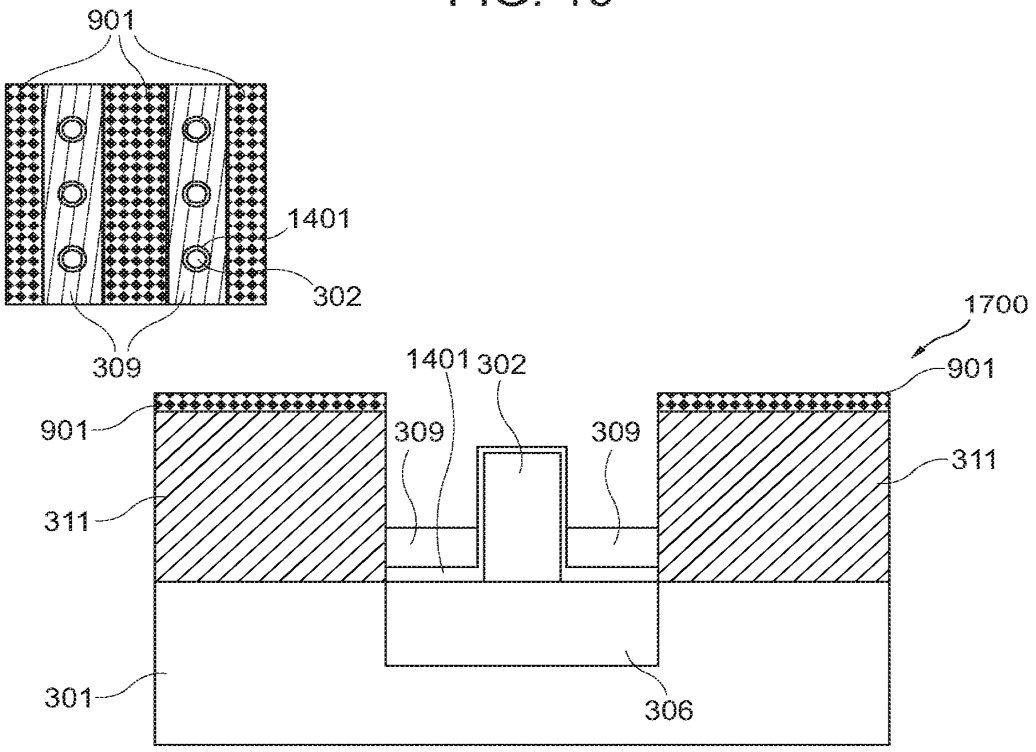

901
1401
302
1700
309
1401
302
901
901
309
309
311
311
301
306

FIG. 17

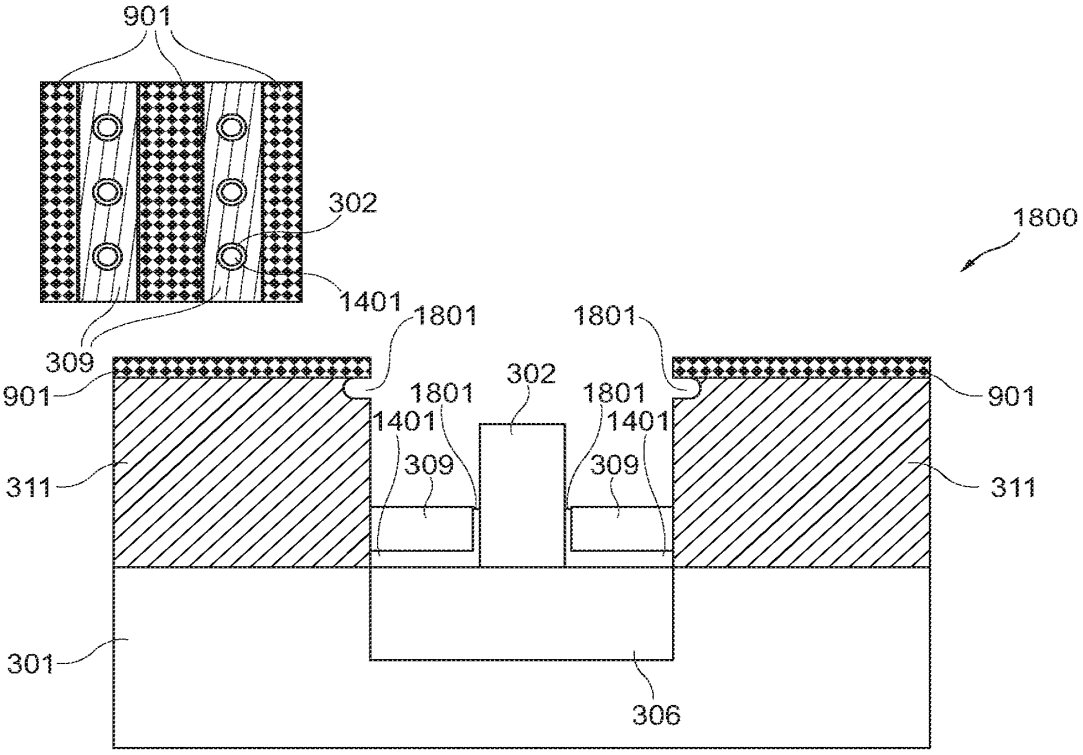

901
302
1800
1401
1801
1801
309
901
1801
302
1801
901
1401
1401
309
309
311
311
301
306

FIG. 18

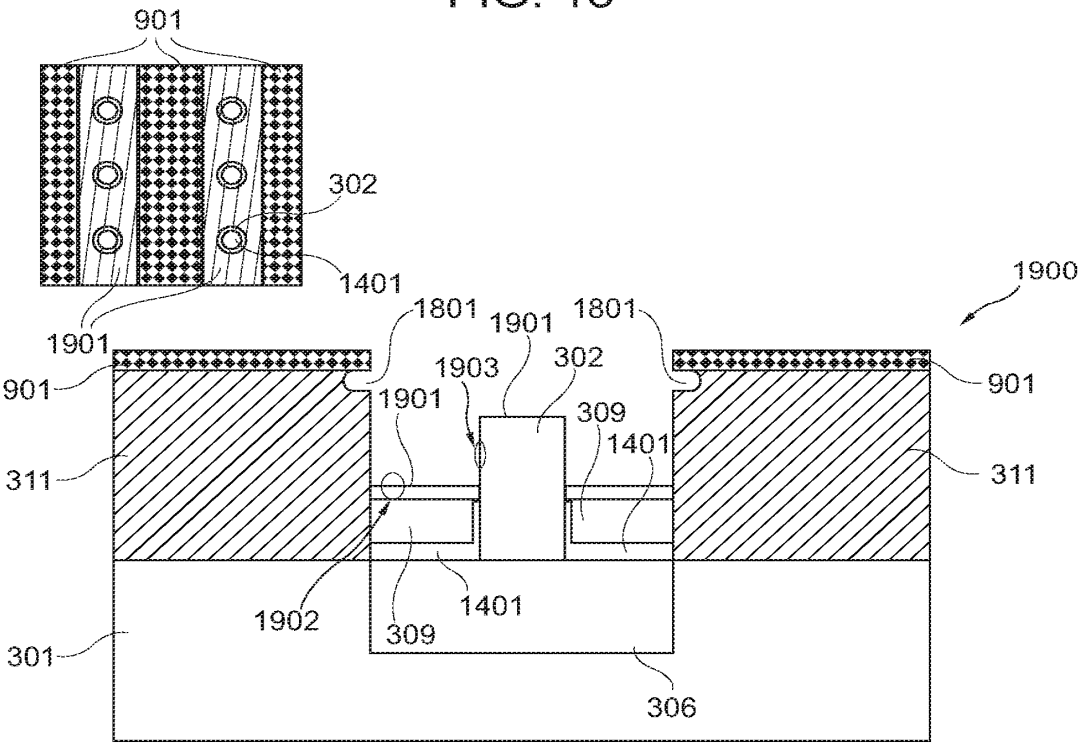

901
302
1900
1401
1801
1901
1801
1901
1901
1903
302
901
901
1901
309
1401
311
311
1902
1401
309
301
306

FIG. 19

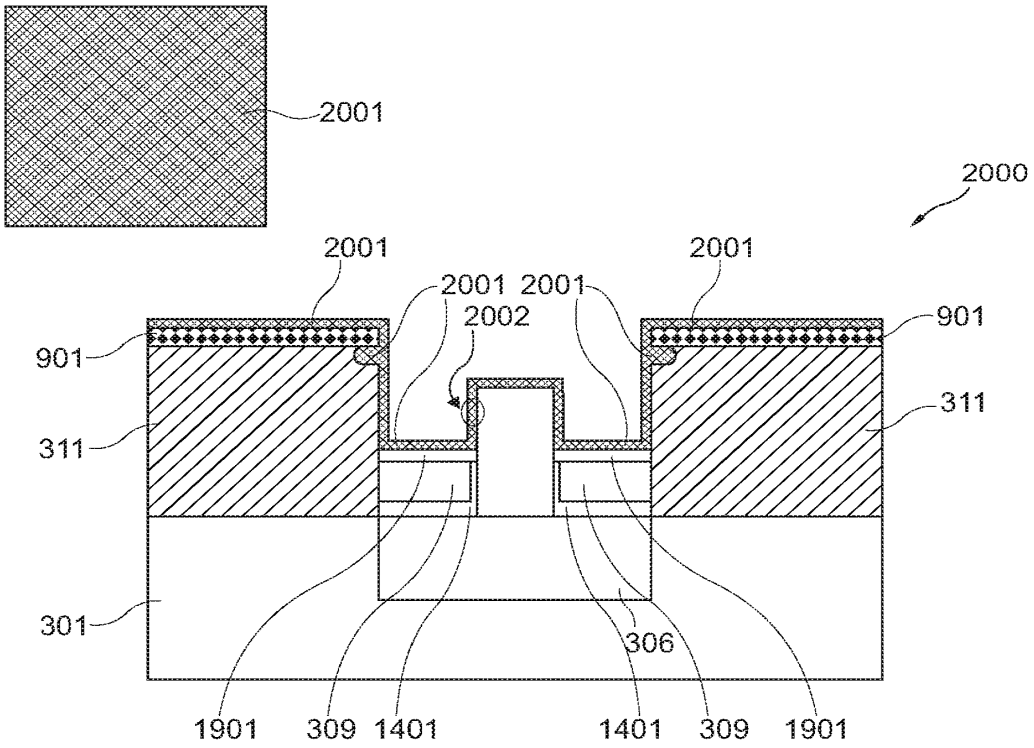

2001
2000
2001
2001 2001
2001
2002
901
901
311
311
301
306
1901
309
1401
1401
309
1901

FIG. 20

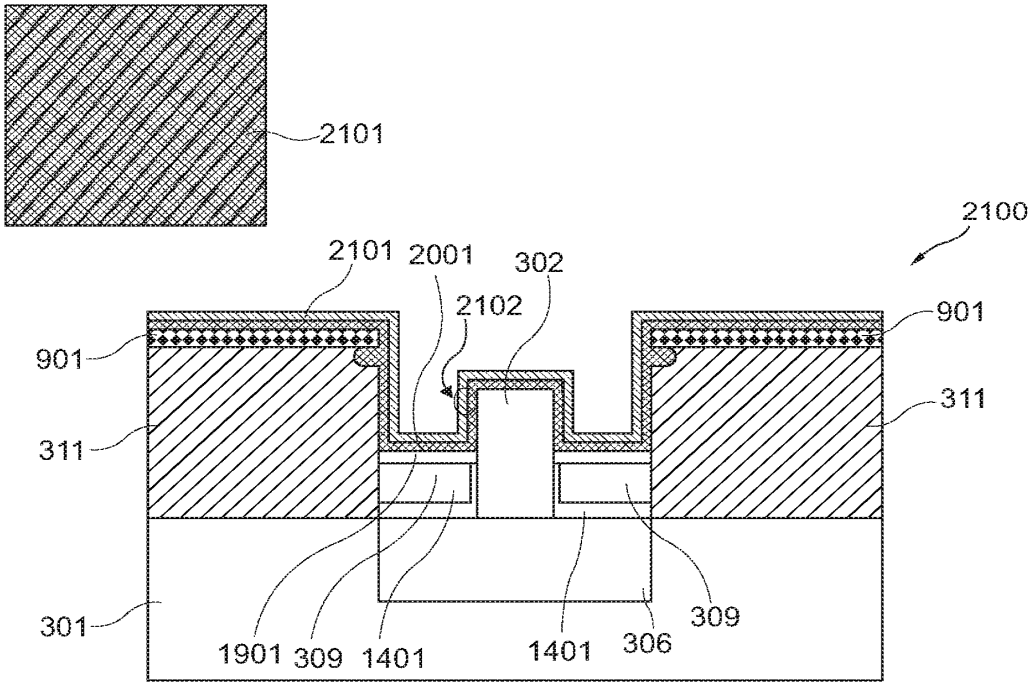

2101
2100
2101
2001
302
2102
901
901
311
311
301
309
1901
309
1401
1401
306

FIG. 21

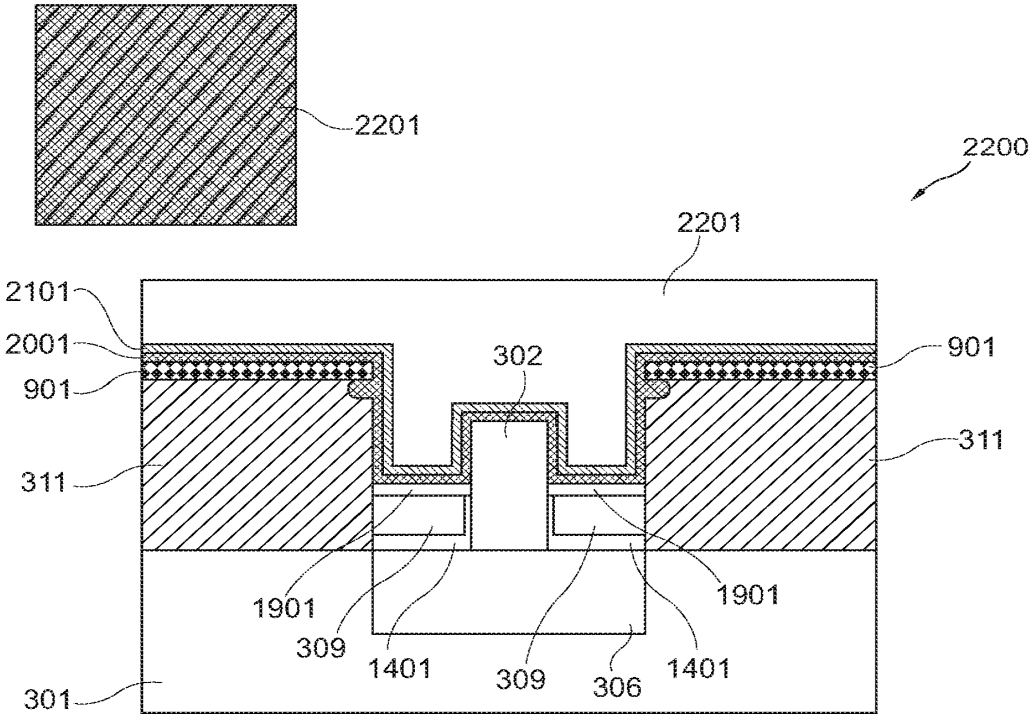

2201
2200
2201
2101
2001
901
302
901
311
311
1901
1901
309
1401
309
306
1401
301

FIG. 22

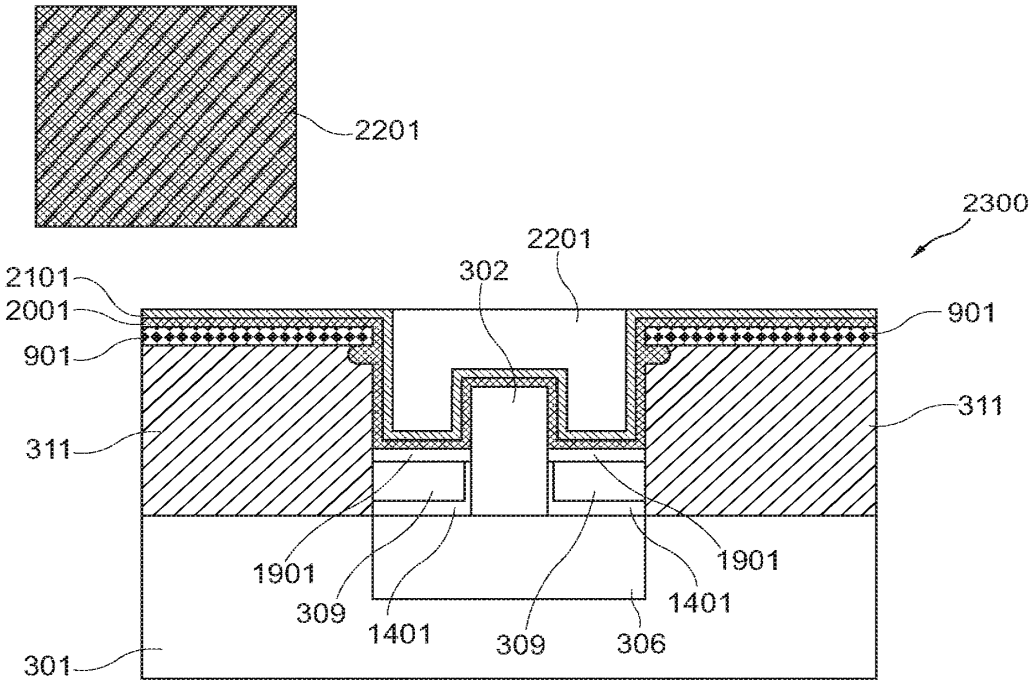

2201
2300
2201
302
2101
2001
901
901
311
311
1901
1901
309
1401
1401
309
306
301

FIG. 23

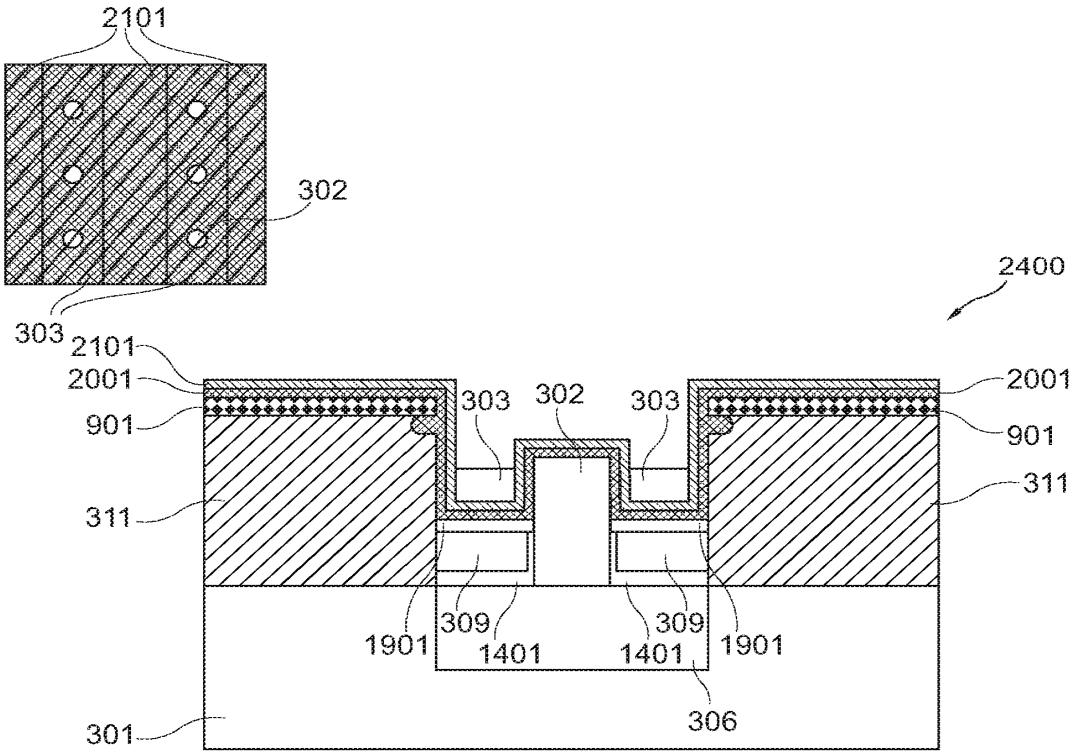

2101
302
303
2400
2101
2001
303
302
303
2001
901
901
311
311
1901
309
1401
1401
309
1901
306
301

FIG. 24

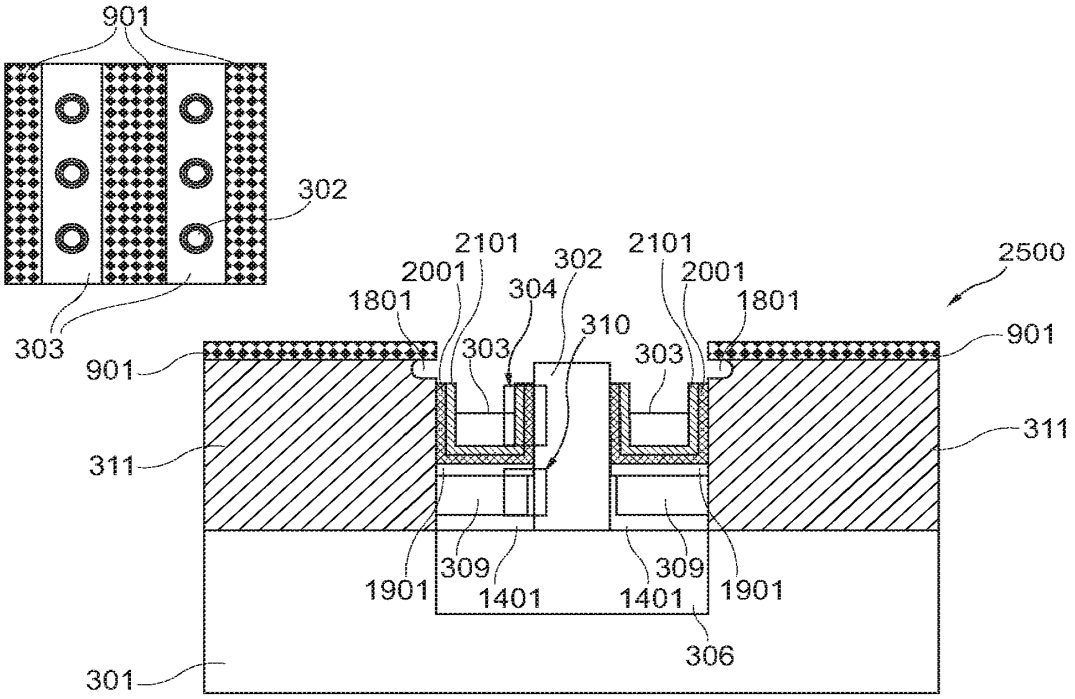

901
302
303
2101
2001
1801
304
302
310
2101
2001
1801
2500
303
303
901
901
311
311
1901
309
1401
1401
309
1901
306
301

FIG. 25

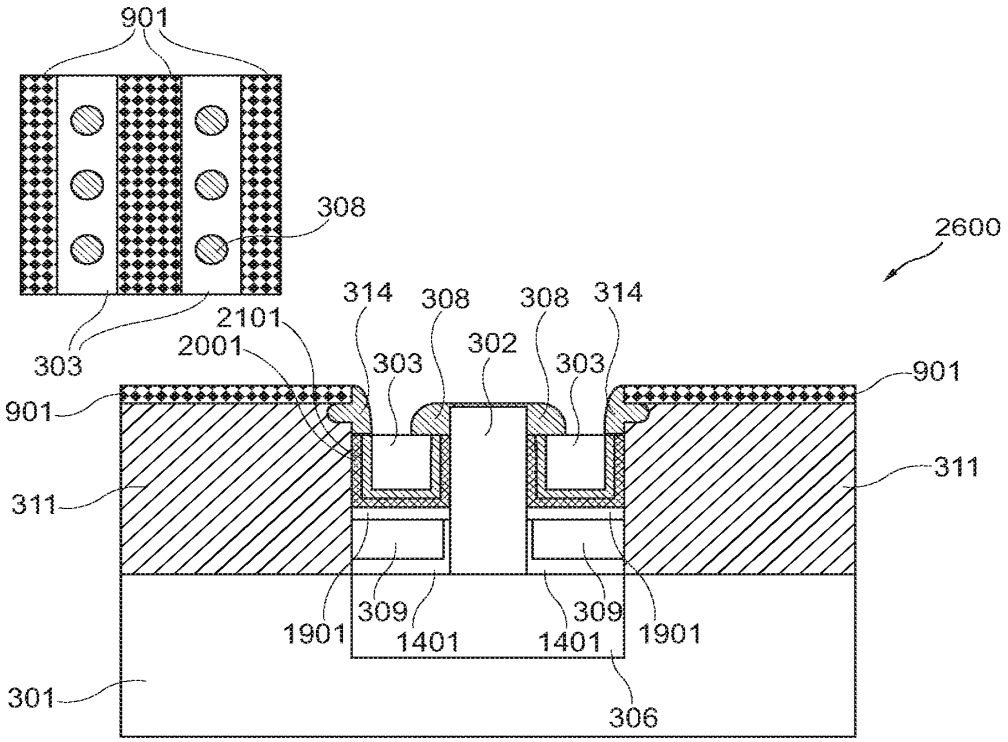

901
308
2600
314
308
308
314
2101
2001
303
302
303
303
901
901
311
311
1901
309
1401
1401
309
1901
301
306

FIG. 26

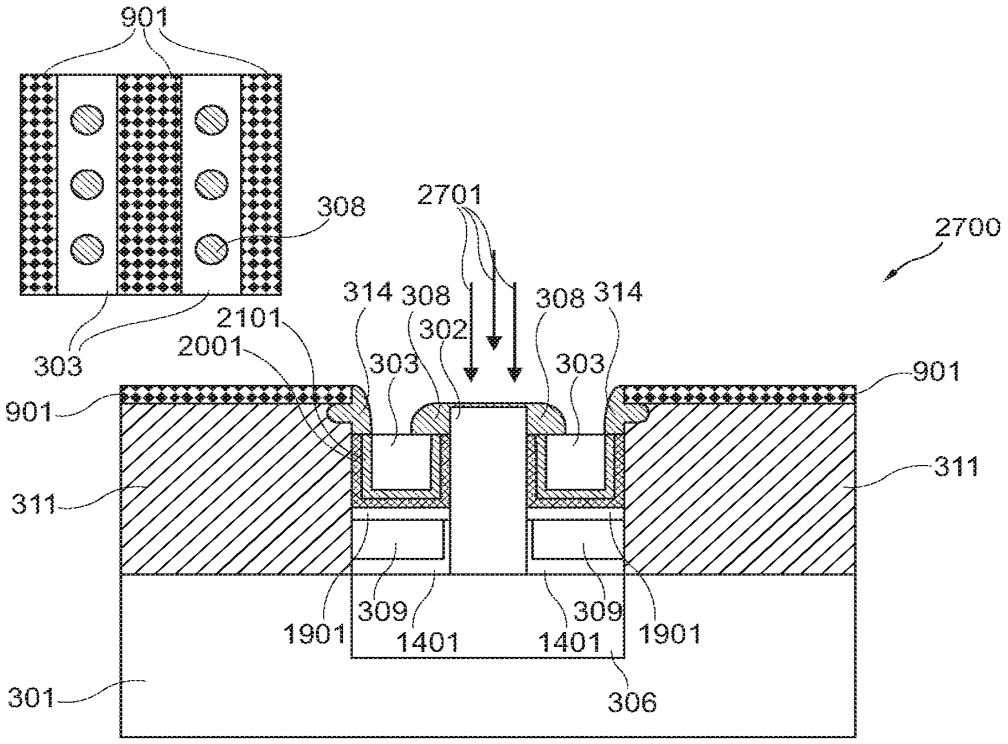

901
308
2701
2700
314
308
308
314
2101
2001
303
302
303
303
901
901
311
311
1901
309
1401
1401
309
1901
301
306

FIG. 27

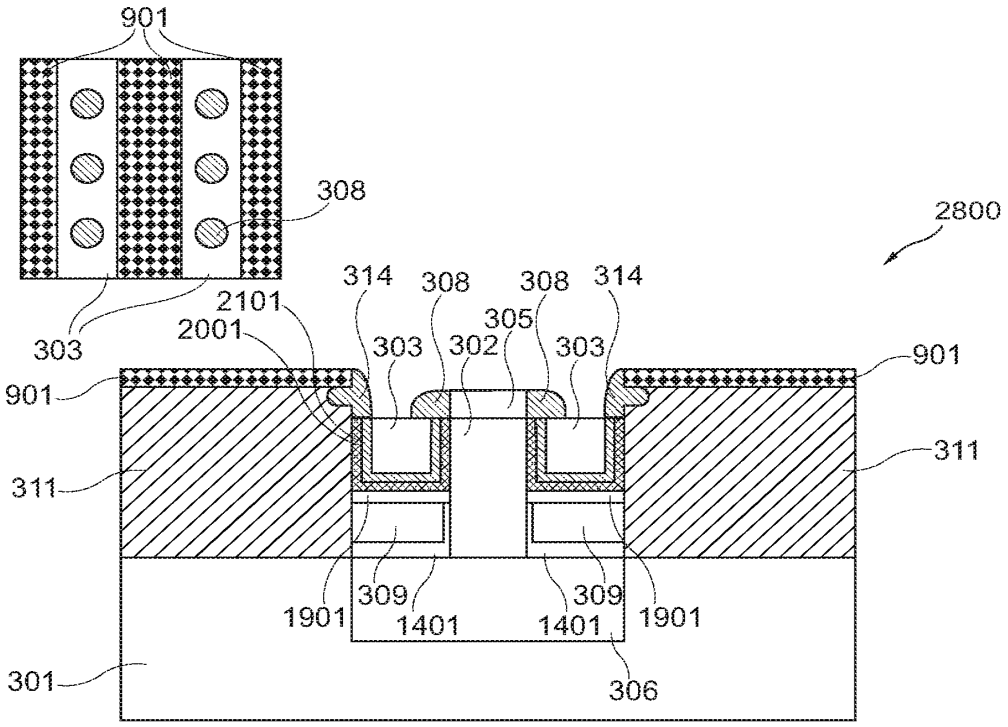

901
308
2800
314
308
308
314
2101
2001
305
303
303
302
303
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 28

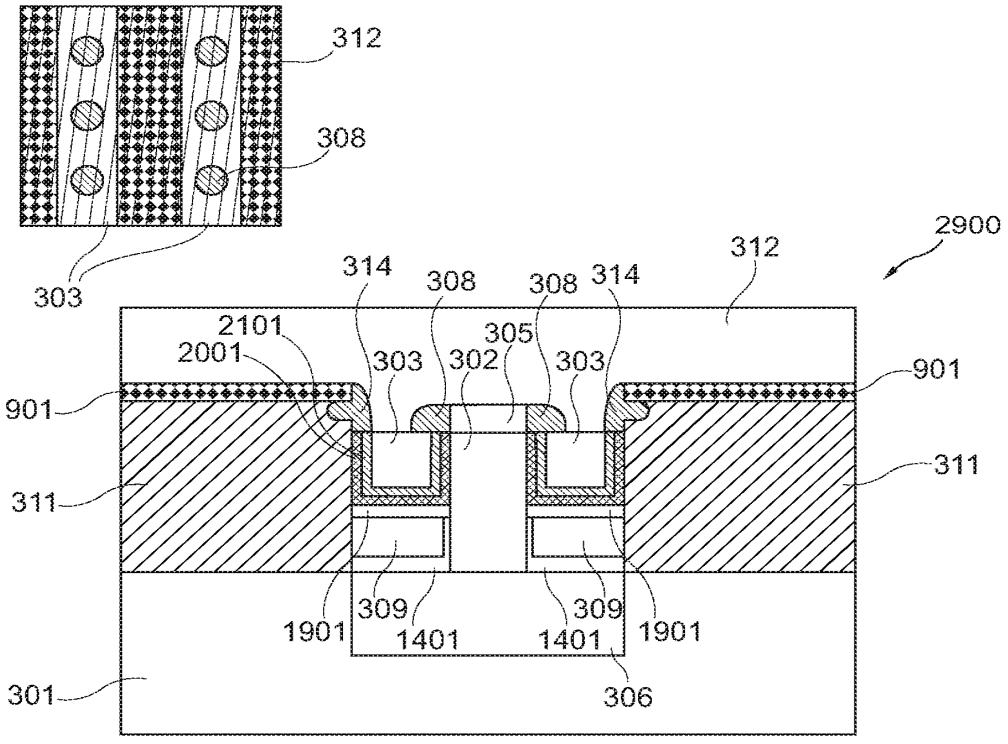

312
308
2900
303
314
308
308
314
312
2101
2001
305
303
302
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 29

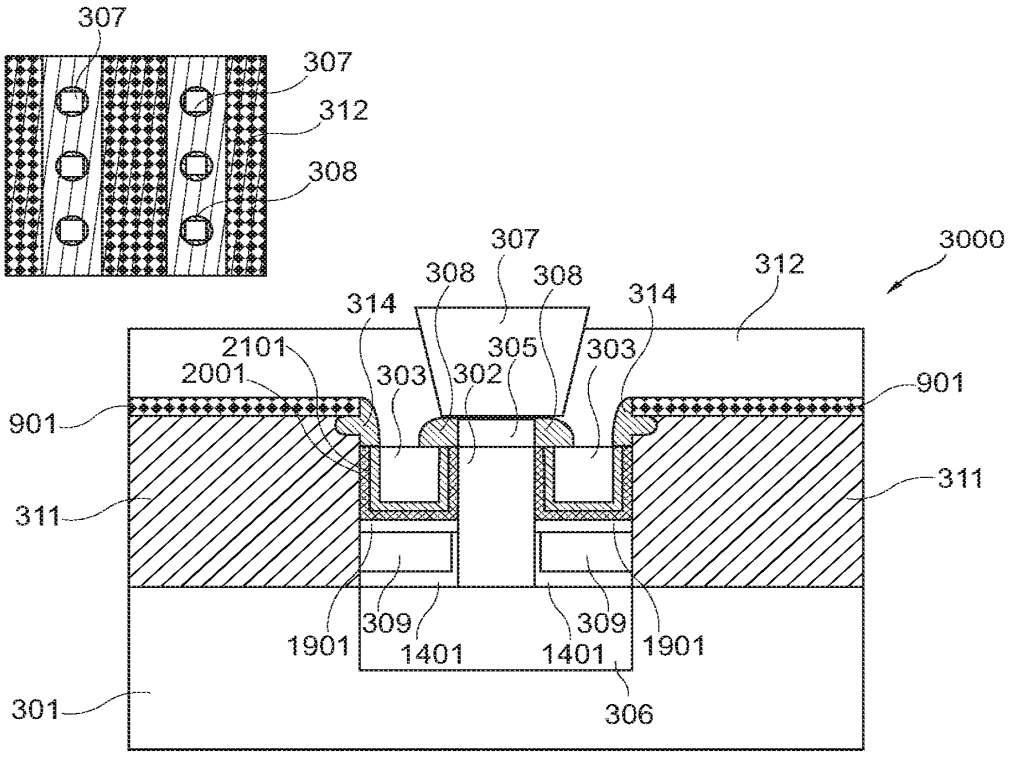

307
307
312
308
307
3000
308
308
314
314
312
2101
2001
305
303
303
302
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 30

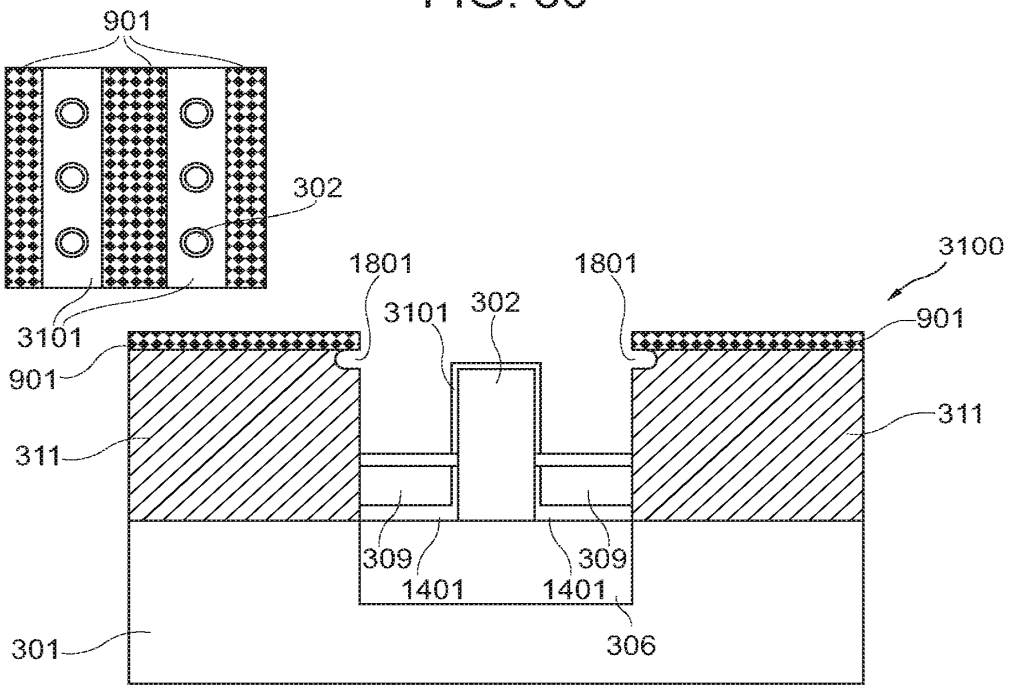

901
302
3100
1801
1801
3101
302
3101
901
901
311
311
309
309
1401
1401
301
306

FIG. 31

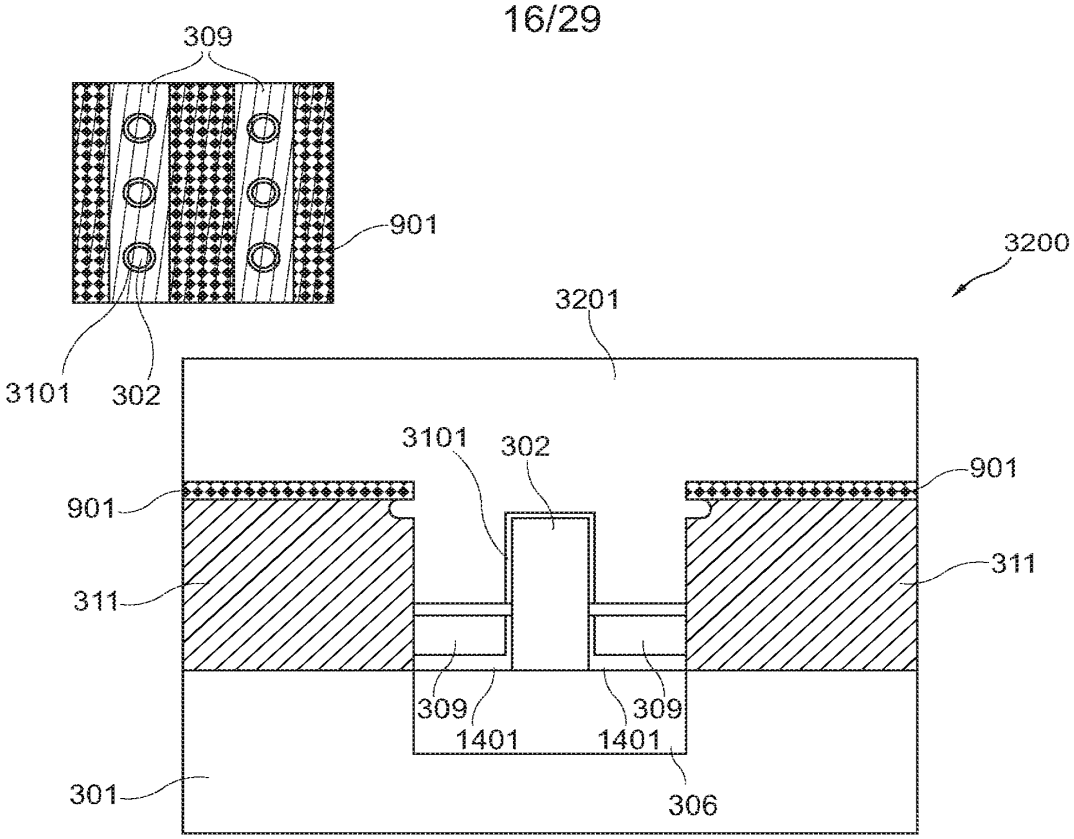

309
901
3200
3201
3101
302
3101
302
901
901
311
311
309
1401
309
1401
301
306

FIG. 32

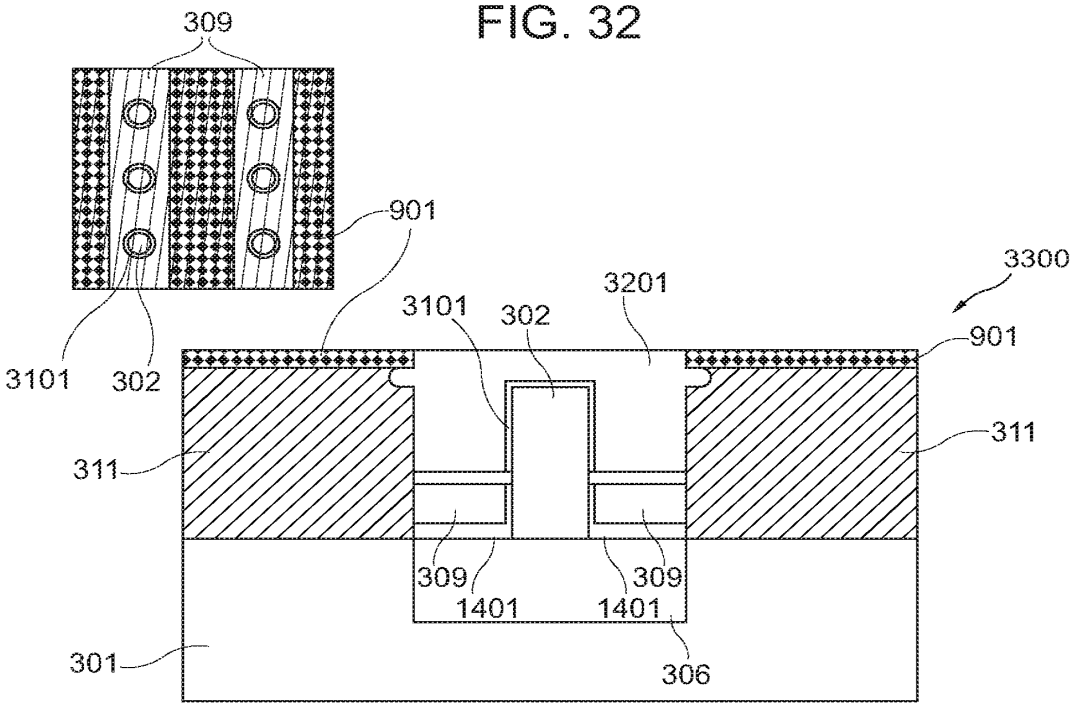

309
901
3300
3201
3101
302
3101
302
901
311
311
309
1401
309
1401
301
306

FIG. 33

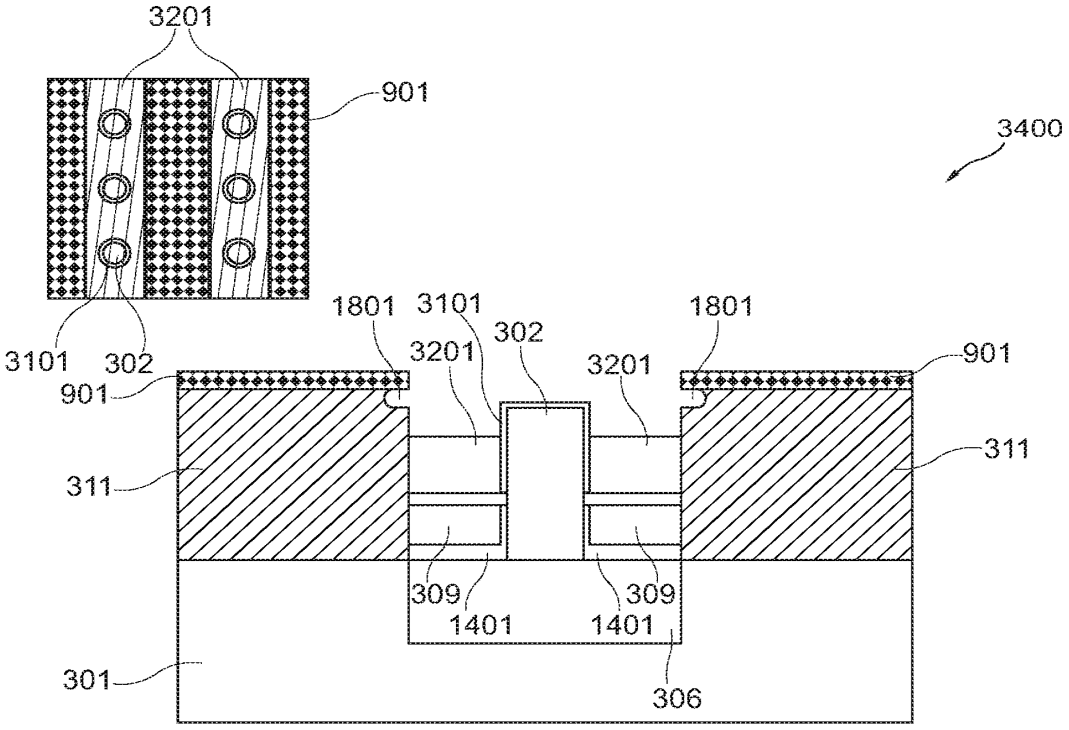

3201
901
3400
1801
3101
302
3201
3201
1801
901
3101
302
901
311
311
309
1401
1401
309
301
306

FIG. 34

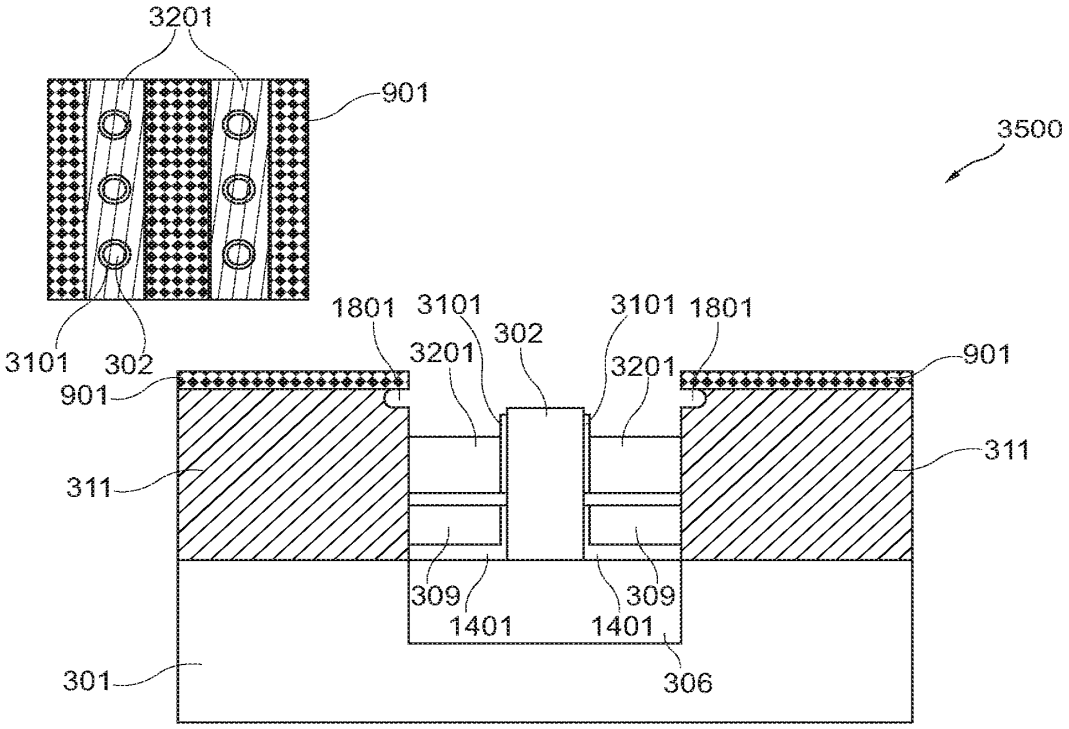

3201
901
3500
1801
3101
3101
1801
302
3201
3201
901
3101
302
901
311
311
309
1401
1401
309
301
306

FIG. 35

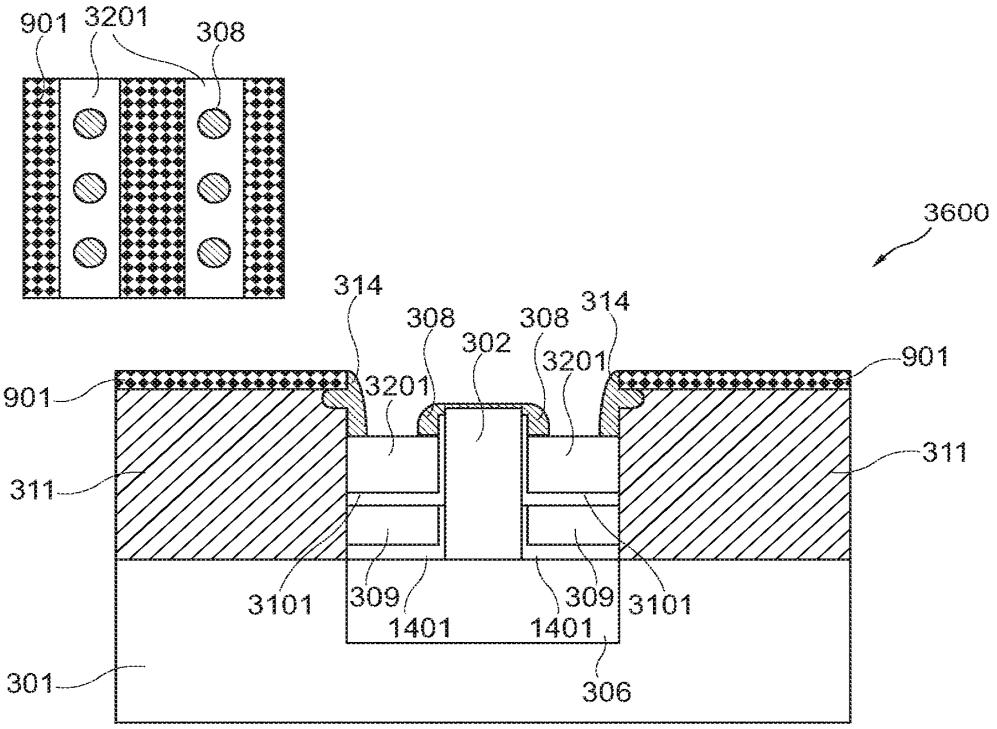

901
3201
308
3600
314
308
308
314
302
3201
901
901
3201
311
311
3101
309
309
3101
1401
1401
301
306

FIG. 36

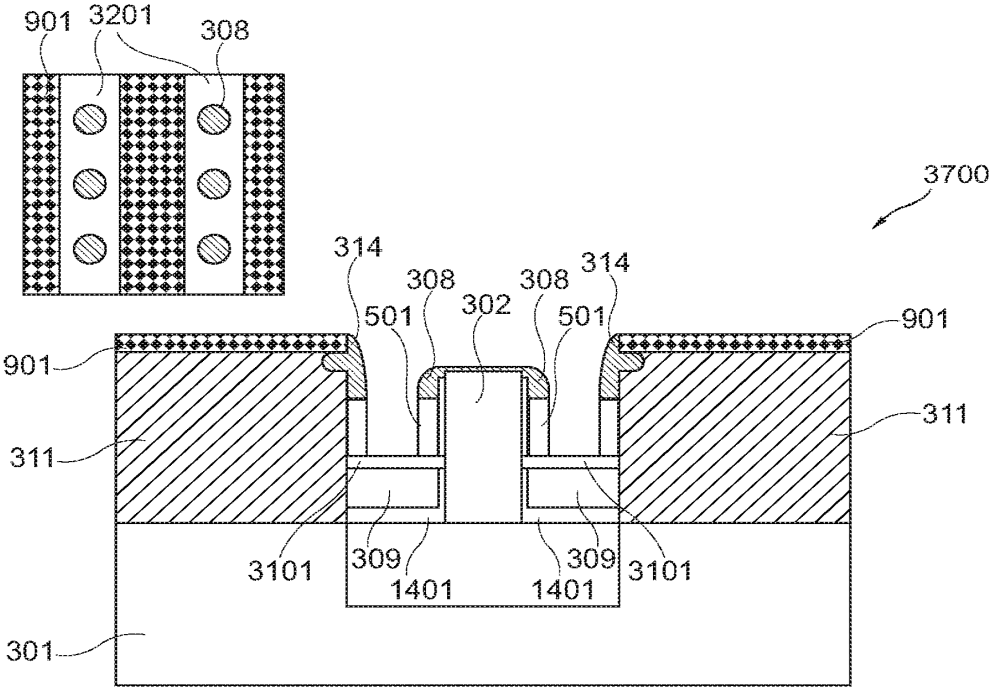

901
3201
308
3700
314
308
308
314
501
302
501
901
901
311
311
3101
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3101
1401
1401
301

FIG. 37

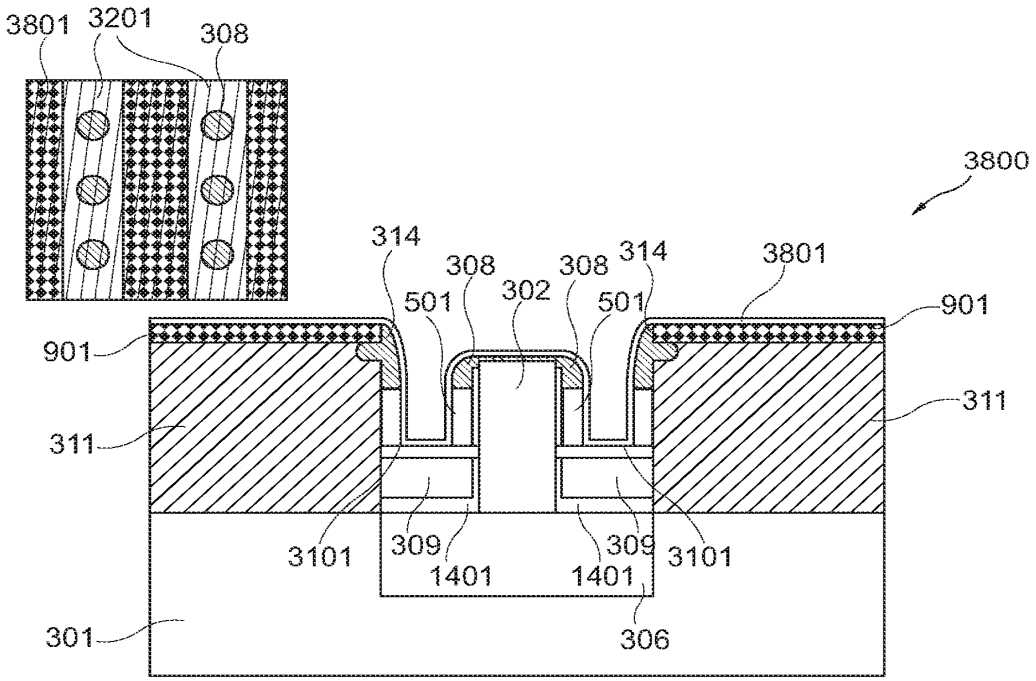

3801
3201
308
3800
314
308
308
314
3801
501
302
501
901
901
311
311
3101
309
309
3101
1401
1401
306
301

FIG. 38

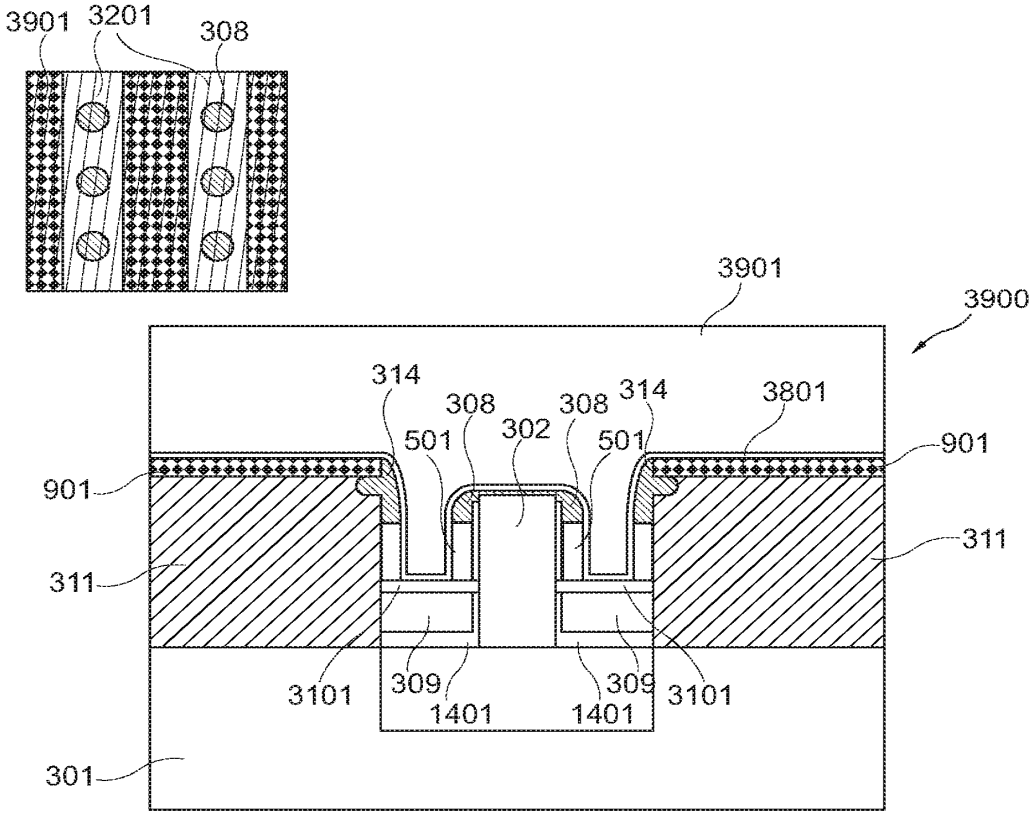

3901
3201
308
3901
3900
314
308
308
314
3801
501
302
501
901
901
311
311
3101
309
309
3101
1401
1401
301

FIG. 39

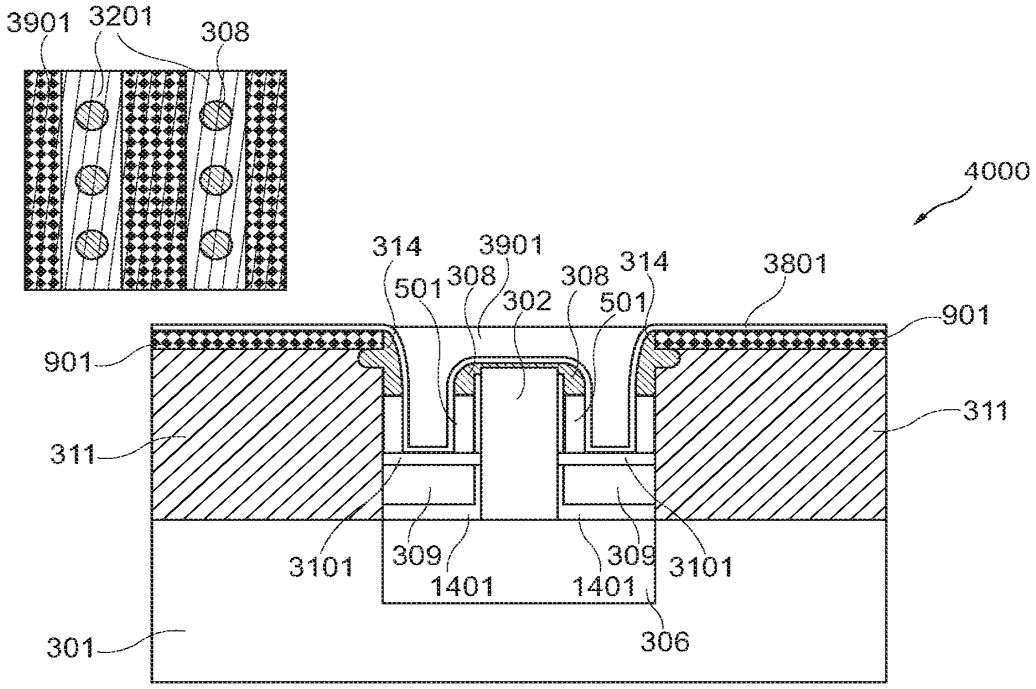

3901
3201
308
4000
314
3901
501
308
308
314
3801
302
501
901
901
311
311
3101
309
309
3101
1401
1401
306
301

FIG. 40

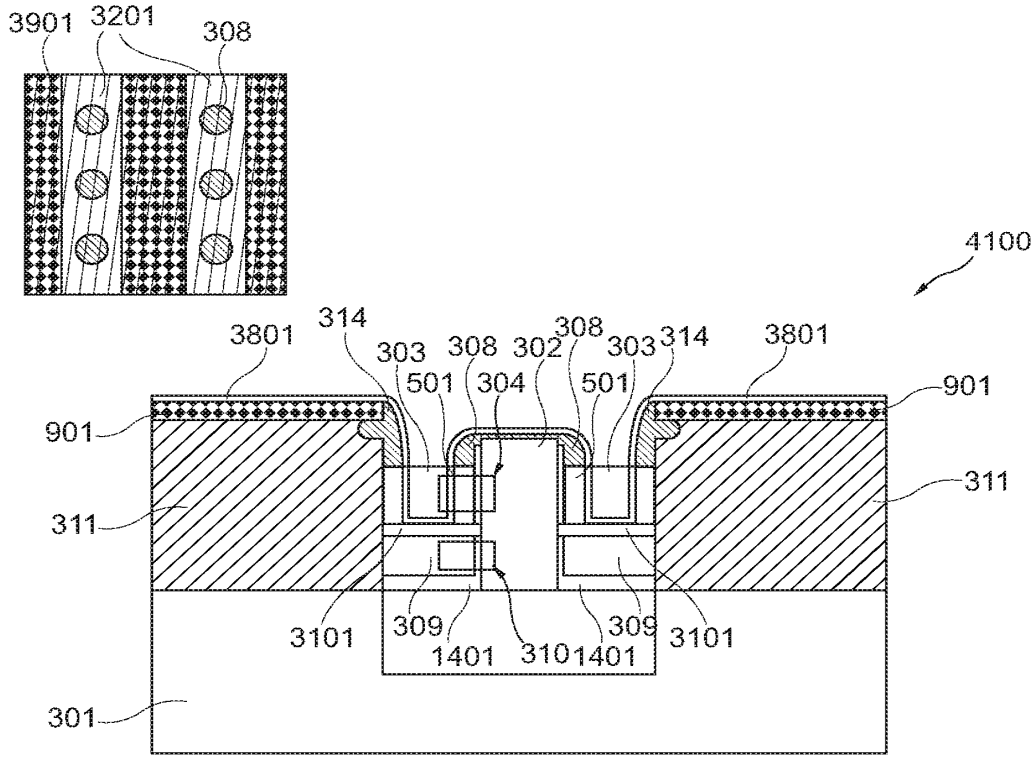

3901
3201
308
4100
3801
314
303
308
302
308
303
314
3801
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304
501
901
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311
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3101
309
309
3101
1401
310
1401
301

FIG. 41

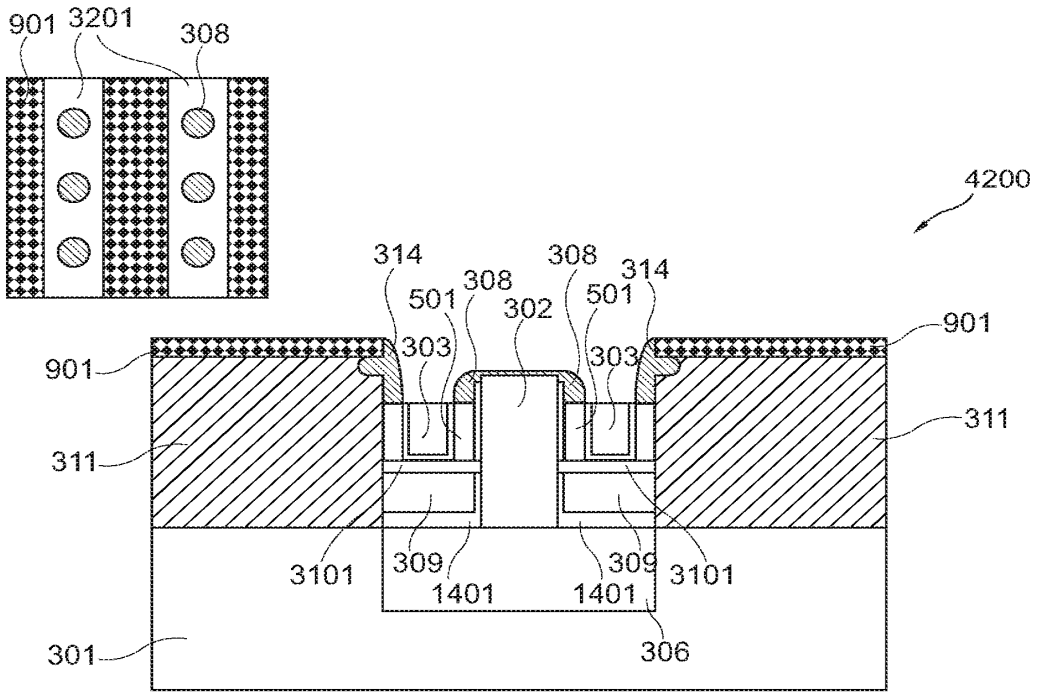

901
3201
308
4200
314
308
308
314
501
308
302
501
303
303
901
901
311
311
3101
309
309
3101
1401
1401
306
301

FIG. 42

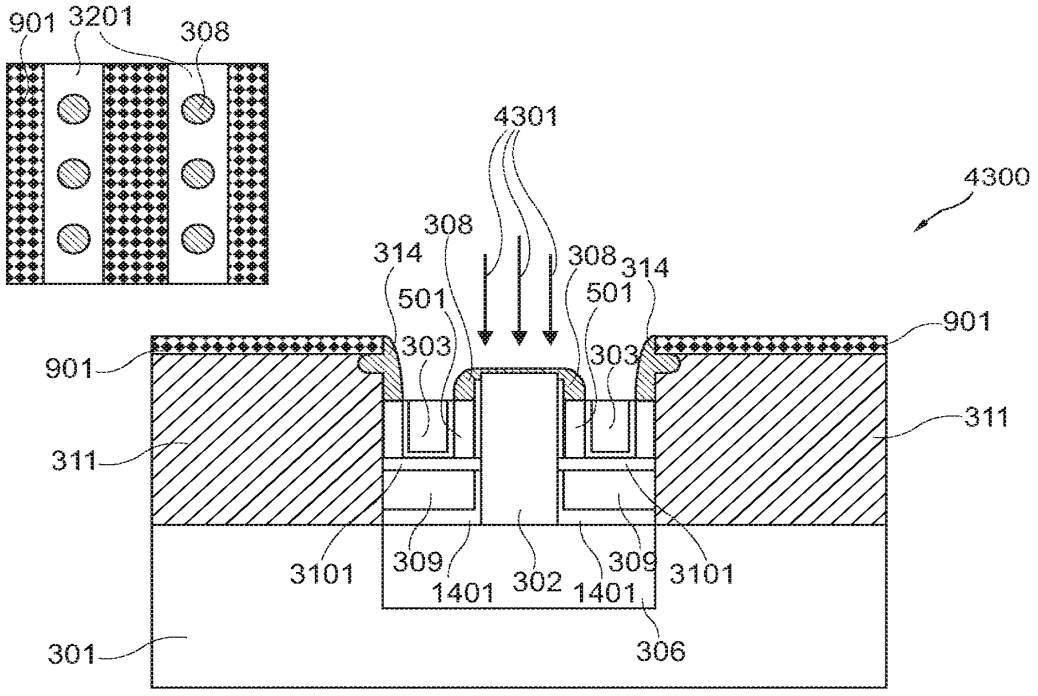

901
3201
308
4301
4300
308
314
308
314
501
501
303
303
901
901
311
311
3101
309
309
3101
1401
302
1401
306
301

FIG. 43

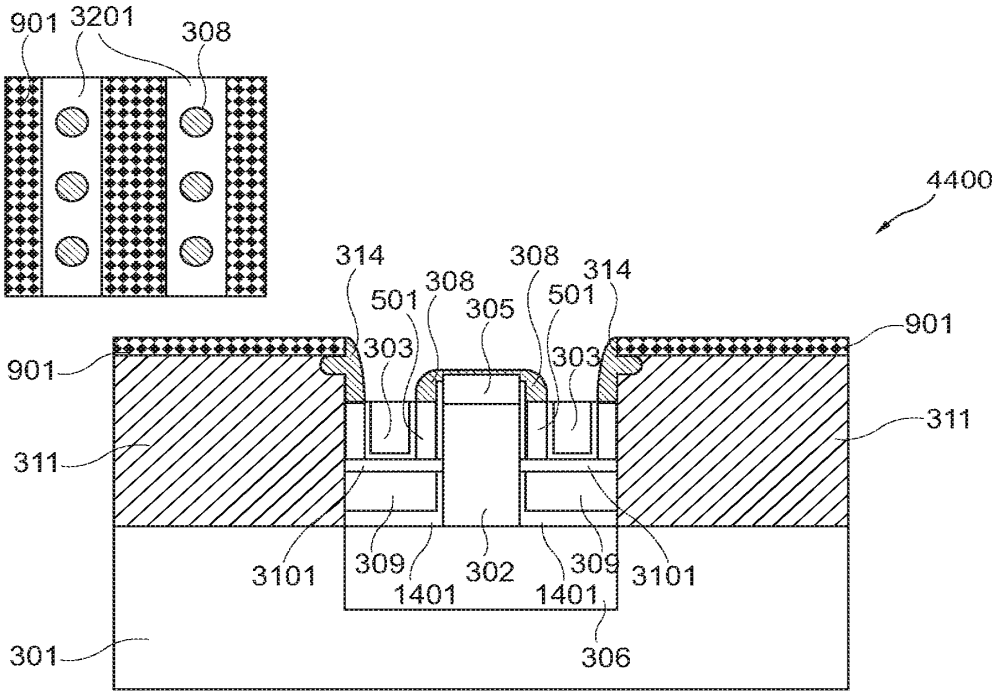

901
3201
308
4400
314
308
314
501
308
305
501
901
303
303
901
311
311
3101
309
302
309
3101
1401
1401
301
306

FIG. 44

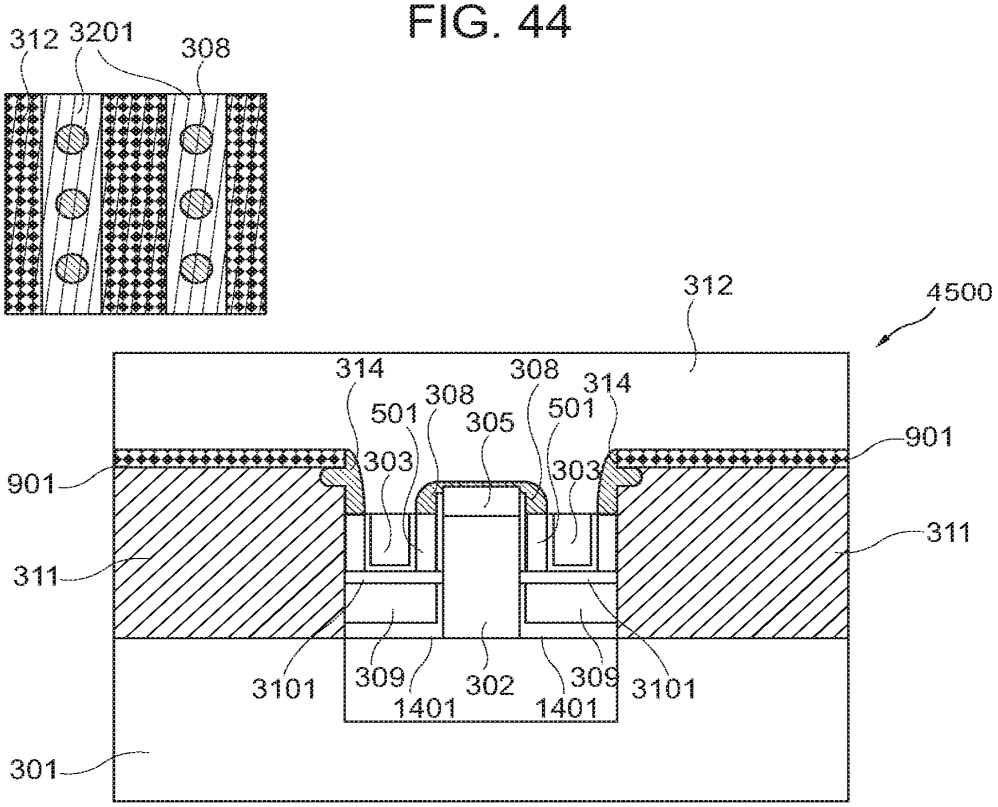

312
3201
308
4500
312
314
308
314
501
308
305
501
901
303
303
901
311
311
3101
309
302
309
3101
1401
1401
301

FIG. 45

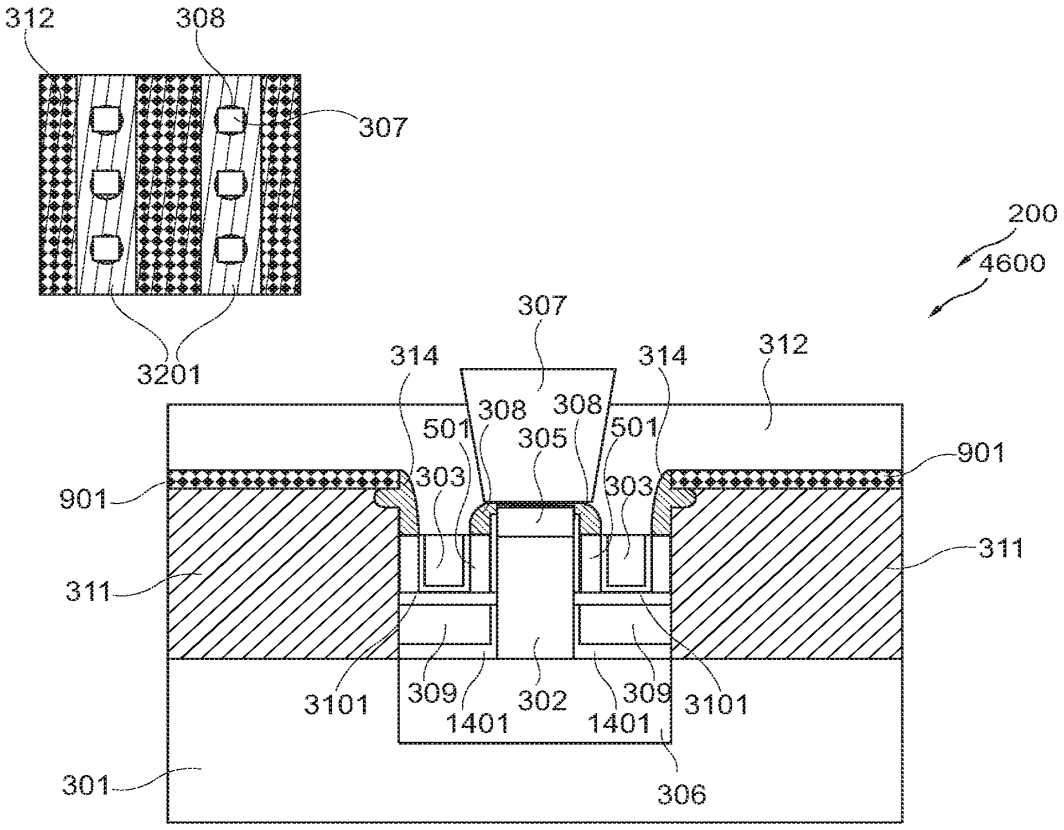

312
308
307
3201
200
4600
307
314
314
312
308
308
501
501
305
303
303
901
901
311
311
3101
309
1401
302
309
1401
3101
301
306

FIG. 46

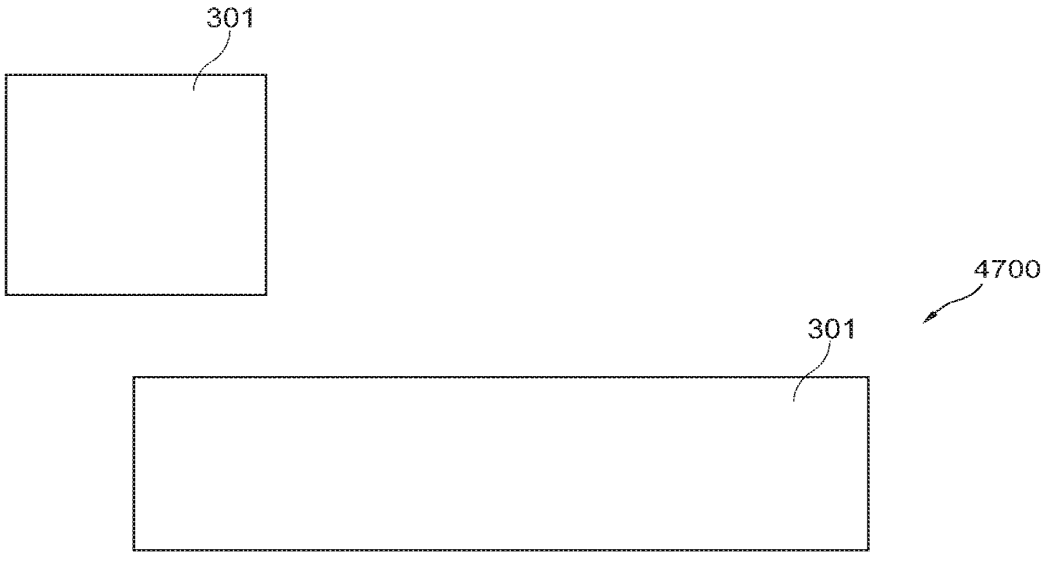

301
4700
301

FIG. 47

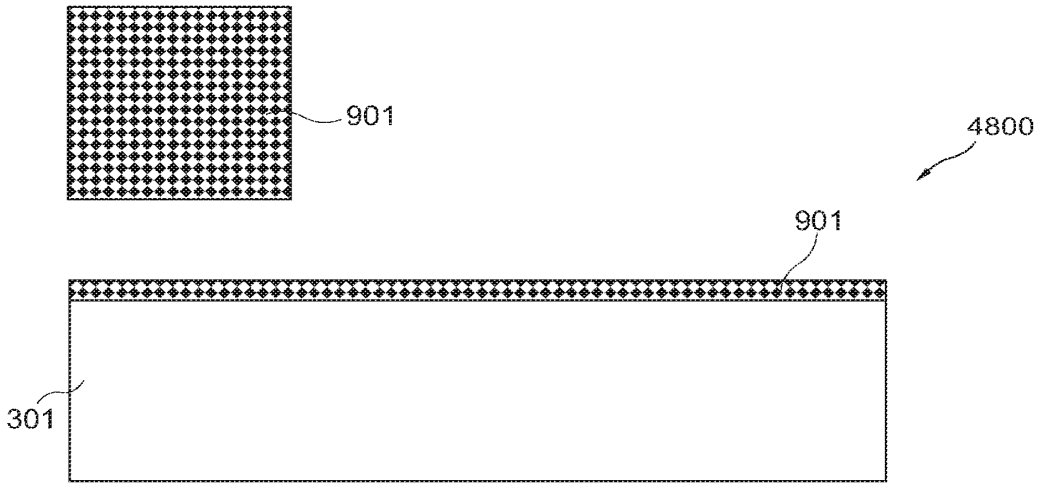


FIG. 48

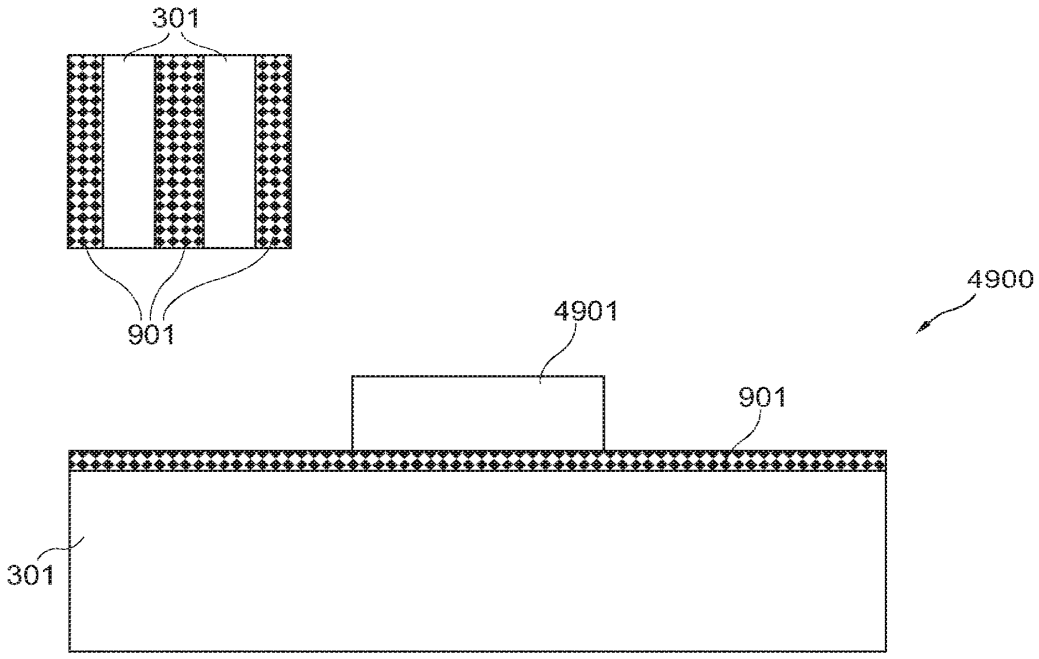


FIG. 49

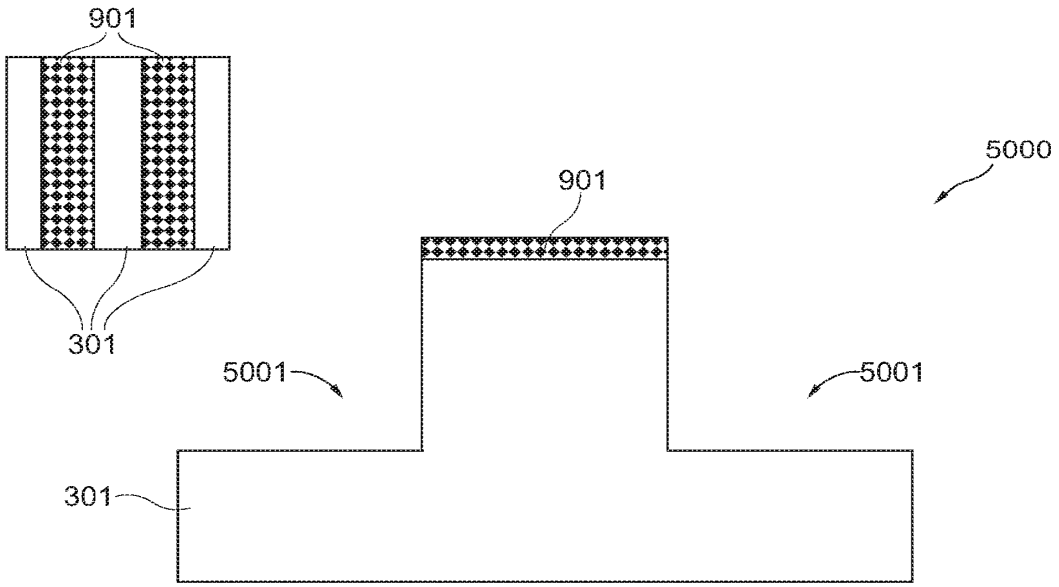


FIG. 50

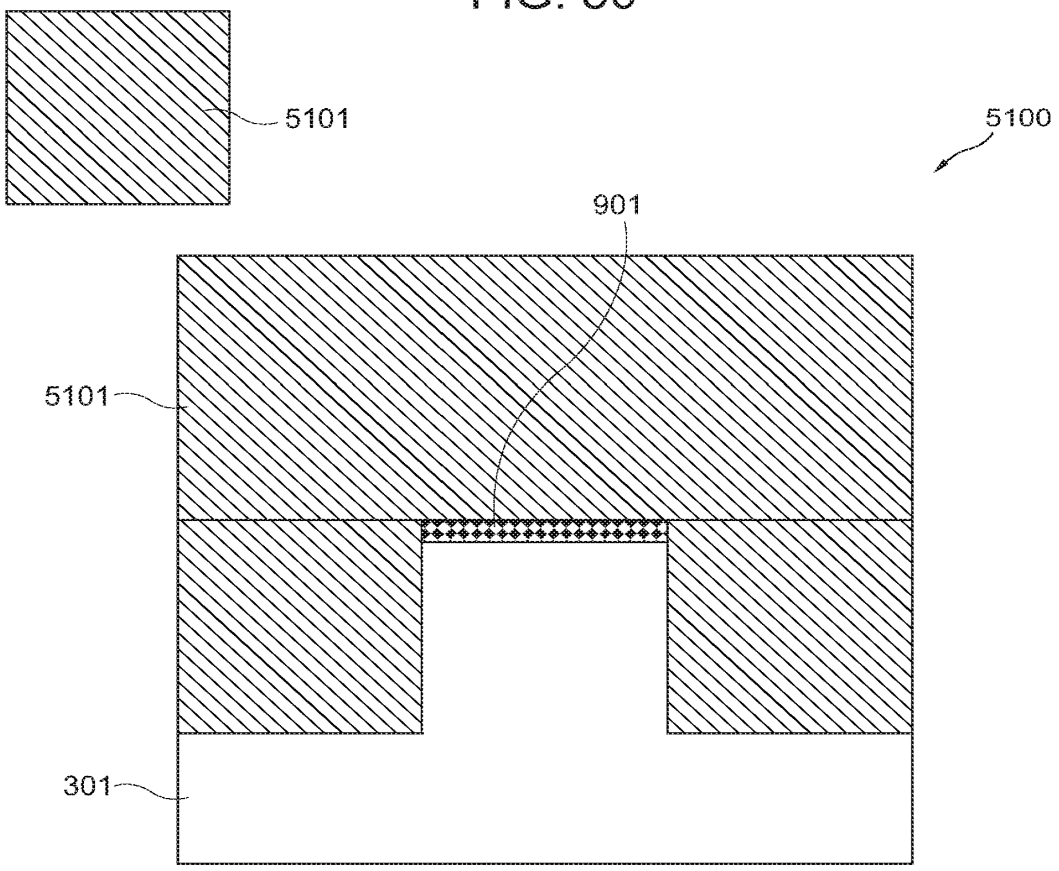


FIG. 51

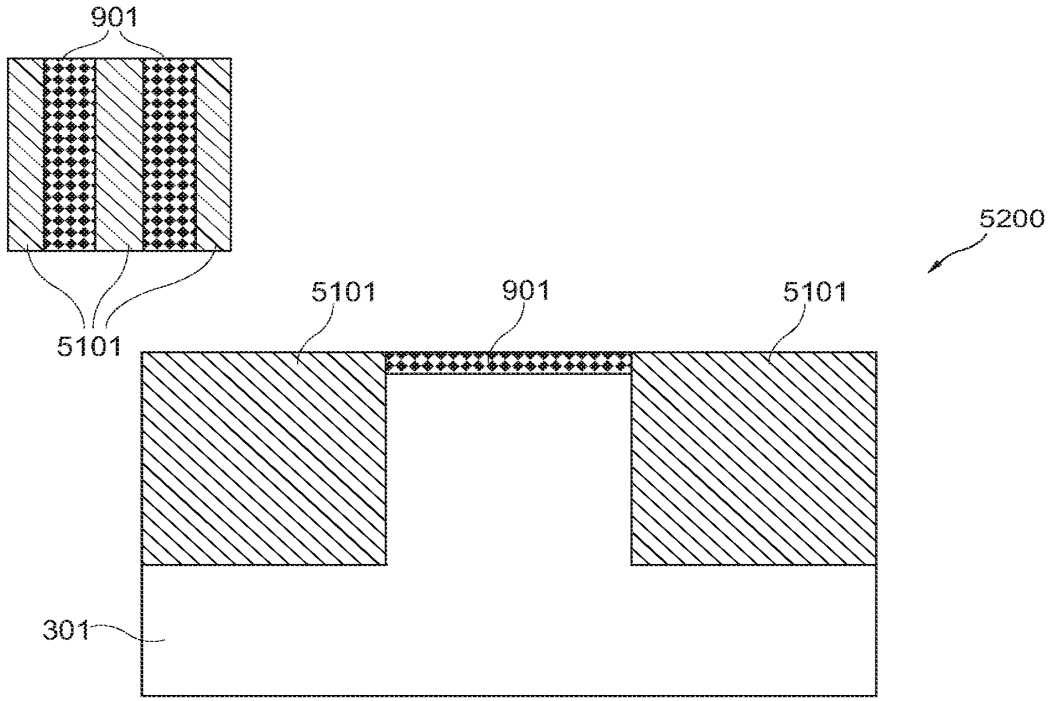

901
5200
5101
901
5101
5101
301

FIG. 52

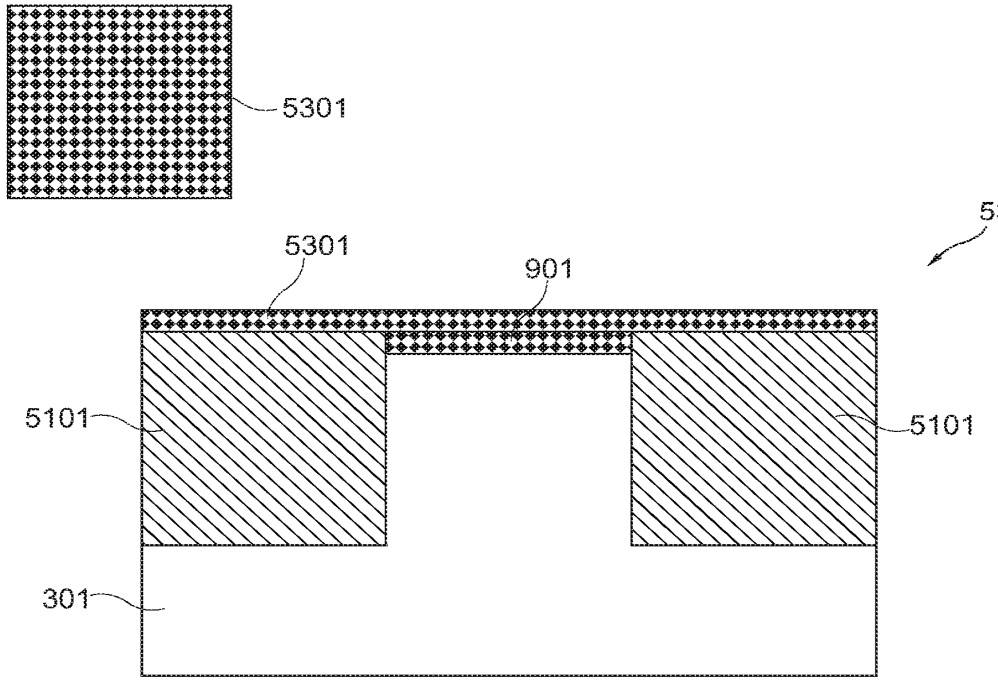

5301
5300
5301
901
5101
5101
301

FIG. 53

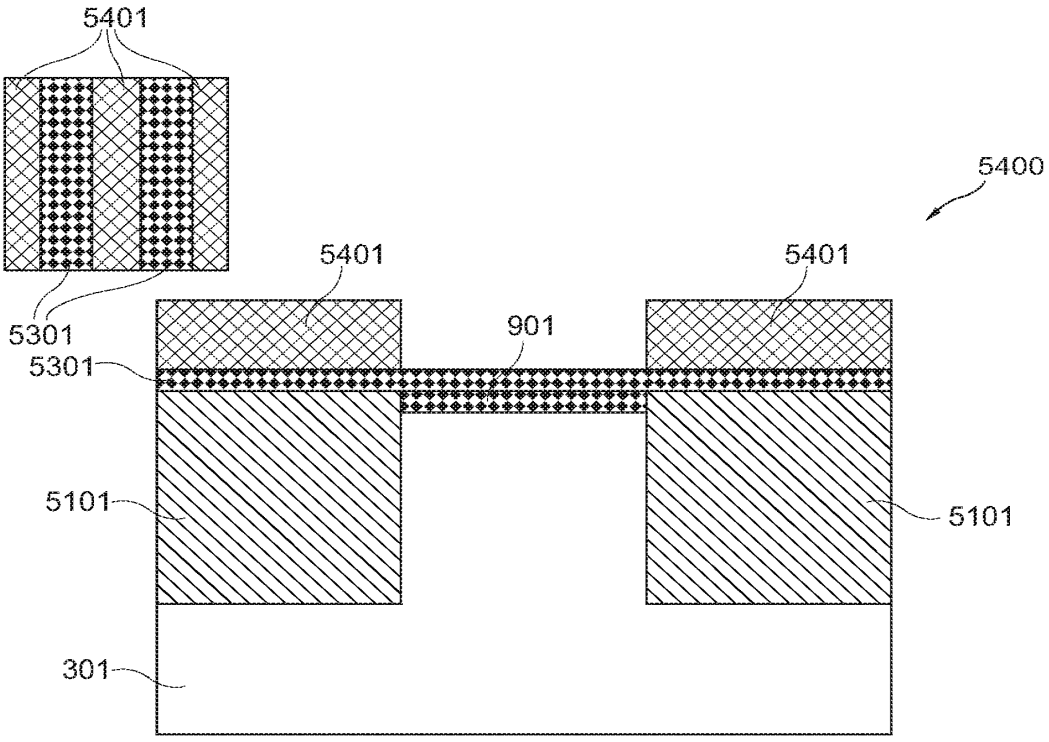

5401
5400
5401
5401
5301
901
5301
5101
5101
301

FIG. 54

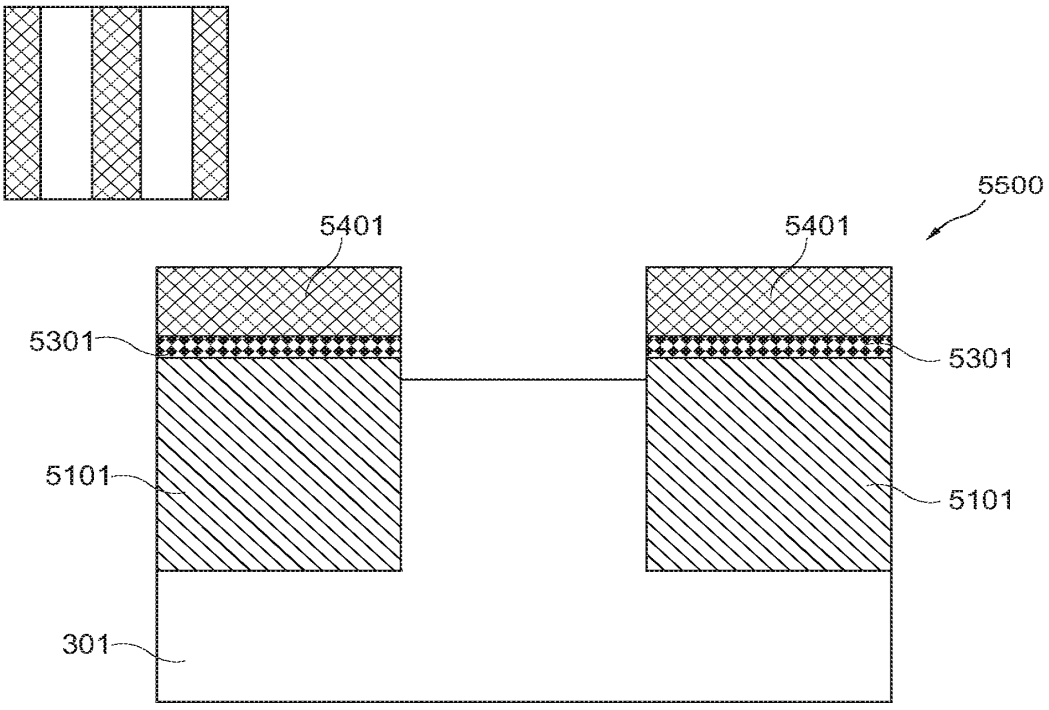

5500
5401
5401
5301
5301
5101
5101
301

FIG. 55

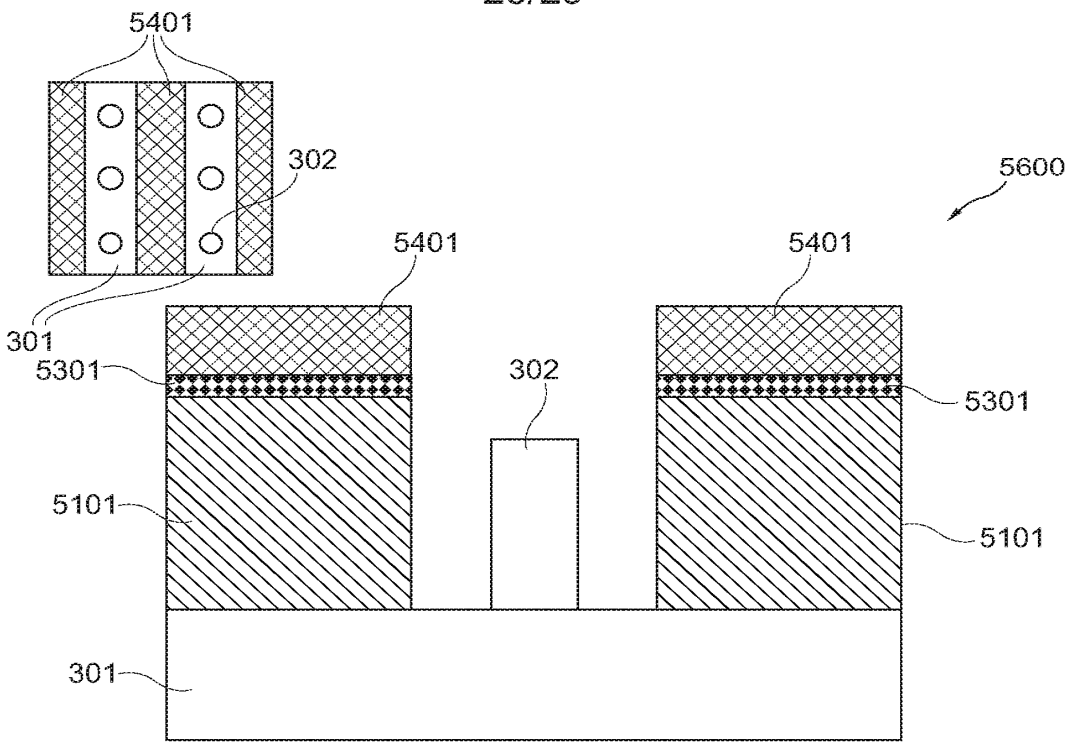

5401
302
5600
5401
5401
301
5301
302
5301
5101
5101
301

FIG. 56

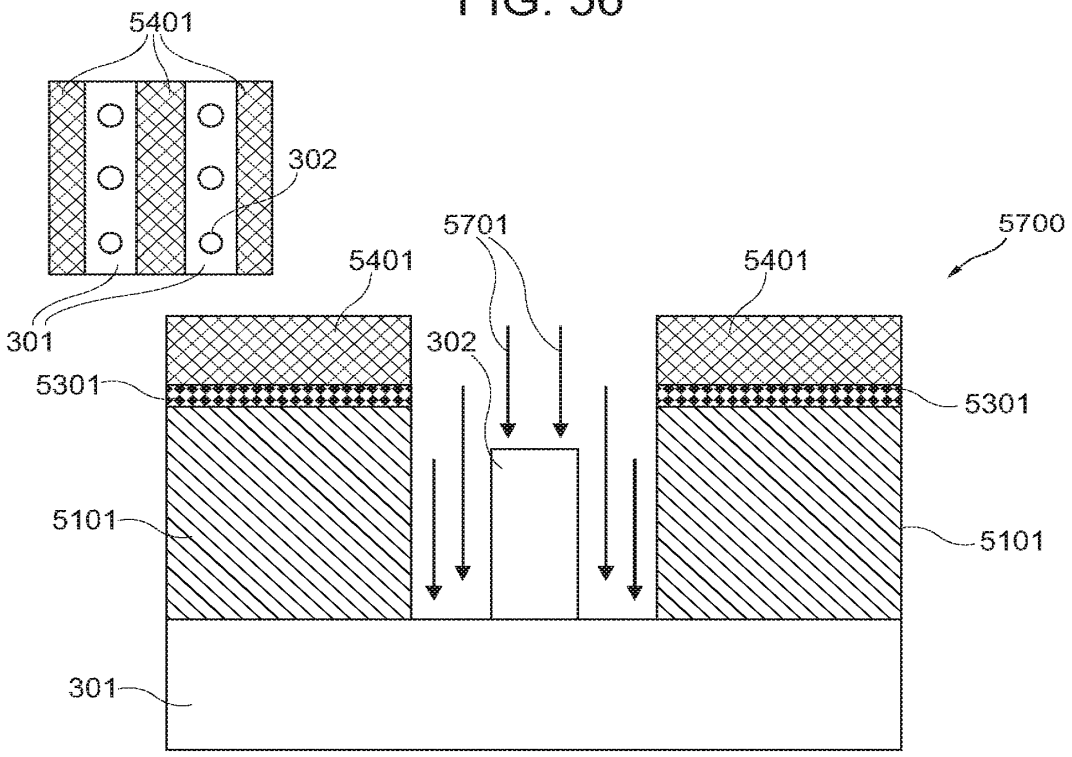

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5701
5700
5401
5401
301
302
5301
5301
5101
5101
301

FIG. 57

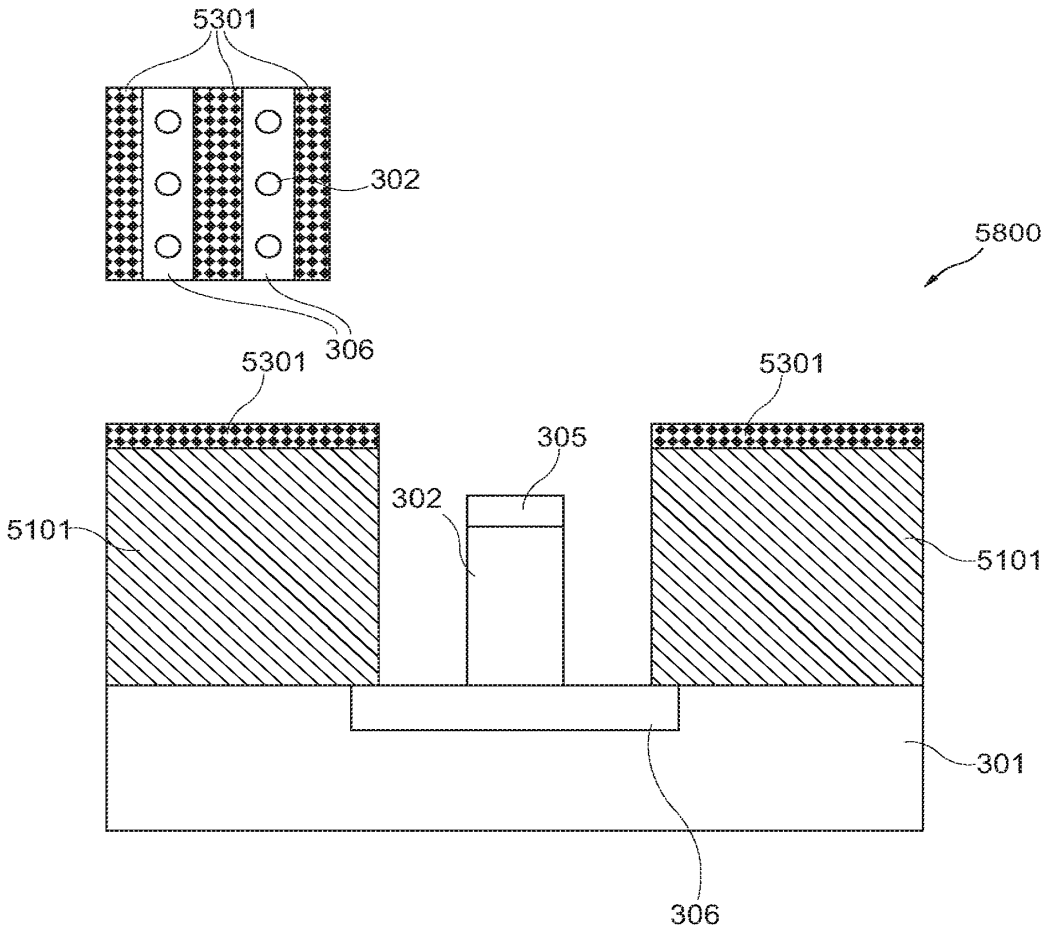


FIG. 58

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/051478

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/28 H01L21/336 H01L21/8246 H01L21/8247 H01L27/115
H01L29/788 H01L29/792 G11C16/04 H01L29/423 H01L29/06
H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PEIN H ET AL: "PERFORMANCE OF THE 3-D PENCIL FLASH EPROM CELL AND MEMORY ARRAY" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 42, no. 11, 1 November 1995 (1995-11-01), pages 1982-1991, XP000582412 ISSN: 0018-9383 the whole document	1-18
X	WO 2004/040667 A (INFINEON TECHNOLOGIES AG [DE]; GRAHAM ANDREW [DE]; HOFMANN FRANZ [DE];) 13 May 2004 (2004-05-13) the whole document	1-18
Y	EP 1 420 414 A (SAMSUNG ELECTRONICS CO LTD [KR]) 19 May 2004 (2004-05-19) the whole document	1-18

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 August 2008	18/08/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Neumann, Andreas

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/051478

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2005/124872 A (KONINKL PHILIPS ELECTRONICS NV [NL]; HIJZEN ERWIN A [BE]; BAKKERS ERIK) 29 December 2005 (2005-12-29) page 7, line 28 - page 8, line 19; figure 2	1-18
A	US 6 433 382 B1 (ORLOWSKI MARIUS [US] ET AL) 13 August 2002 (2002-08-13) column 3, line 57 - column 4, line 11; figure 1	9,10

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2008/051478

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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WO2007022359A2 VERTICAL INTEGRATED SILICON NANOWIRE FIELD EFFECT TRANSISTORS AND METHODS OF FABRICATION

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VERTICAL INTEGRATED SILICON NANOWIRE FIELD EFFECT TRANSISTORS AND METHODS OF FABRICATION

Abstract

Vertical integrated field effect transistor circuits and methods are described which are fabricated from Silicon, Germanium, or a combination Silicon and Germanium based on nanowires grown in place on the substrate. By way of example, vertical integrated transistors are formed from one or more nanowires which have been insulated, had a gate deposited thereon, and to which a drain is coupled to the exposed tips of one or more of the nanowires. The nanowires are preferably grown over a surface or according to a desired pattern in response to dispersing metal nanoclusters over the desired portions of the substrate. In one preferred implementation, SiCl4 is utilized as a gas phase precursor during the nanowire growth process. In place nanowire growth is also taught in conjunction with structures, such as trenches, while bridging forms of nanowires are also described.

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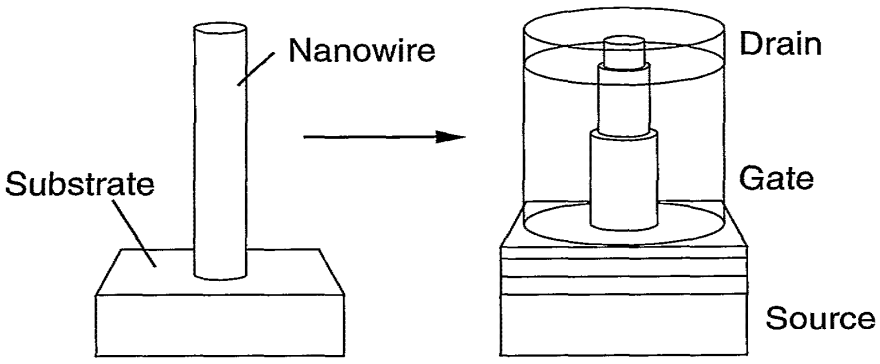
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(57) Abstract: Vertical integrated field effect transistor circuits and methods are described which are fabricated from Silicon, Germanium, or a combination Silicon and Germanium based on nanowires grown in place on the substrate. By way of example, vertical integrated transistors are formed from one or more nanowires which have been insulated, had a gate deposited thereon, and to which a drain is coupled to the exposed tips of one or more of the nanowires. The nanowires are preferably grown over a surface or according to a desired pattern in response to dispersing metal nanoclusters over the desired portions of the substrate. In one preferred implementation, SiCl4 is utilized as a gas phase precursor during the nanowire growth process. In place nanowire growth is also taught in conjunction with structures, such as trenches, while bridging forms of nanowires are also described.

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TITLE OF THE INVENTION

VERTICAL INTEGRATED SILICON NANOWIRE FIELD EFFECT TRANSISTORS AND METHODS OF FABRICATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. provisional application serial number 60/709,044 filed on August 16, 2006, incorporated herein in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] This invention was made with Government support under Grant No. DE-FG02-02ER46021, awarded by the Department of Energy. The Government has certain rights in this invention.

INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC

[0003] Not Applicable

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BACKGROUND OF THE INVENTION

1. Field of the Invention

[0006] This invention pertains generally to nanowire fabrication, and more particularly to vertical integrated transistors fabricated from nanowires.

2. Description of Related Art

[0007] As semiconductor devices are scaled into the sub 50nm regime, short-channel effects and poor sub-threshold characteristics begin to be problematic for traditional planar transistors. Novel device geometries with enhanced performance, defined by functional density, energy efficiency, scalability, and compatibility with CMOS, are required in order to push toward ever higher packing densities in devices and circuits, such as memories and logic chips, to provide ever increasing energy efficiency.

[0008] Silicon nanowires have received considerable attention as transistor components because they represent a facile route towards sub-100nm single-crystalline Si features with minimal surface roughness. Typically, silicon nanowire transistors have a horizontal planar layout with either a top or back gate geometry. However, the difficulty in reliably assembling ultra-high density planar nanowire circuits, combined with the performance limitations of the horizontal device geometry may ultimately hinder nanowire-based electronics from realizing their full potential.

[0009] Therefore, a need exists for transistor geometries and fabrication methods which are amenable to high density fabrication, the nanowire transistors and fabrication methods according to the present invention fulfill that need as well as others and overcome shortcomings with traditional nanowire fabrication.

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BRIEF SUMMARY OF THE INVENTION

[0010] The present invention comprises a vertical integrated nanowire field effect transistor (VINFET) and a method of fabricating the VINFET about a vertical nanowire. Methods are described for growing nanowires from a substrate. In one embodiment of the invention, a field effect transistor is fabricated from a vertical nanowire extending from a substrate base. The transistor comprises the nanowire coupled to the source, surrounded by a gate dielectric about which a metal gate is formed. A drain is coupled to the exposed tip of the nanowire and insulated from the conductive gate. The transistor can be fabricated with a single nanowire or any desired number of nanowires coupled between the source and a given drain region or pad.

[0011] By way of example and not limitation, in one embodiment the vertical integrated nanowire field effect transistor (VINFETs) is fabricated in place according to the following general processing procedure. First, Si nanowires are grown vertically from a Si (111) substrate. After nanowire growth, the nanoparticle catalysts are etched away and cleaned. The substrates are then oxidized to achieve the desired gate SiO_2 dielectric thickness. Cr gate metal is deposited, such as by sputtering, to achieve a conformal coating. Alternatively, LPCVD techniques can be used to deposit the desired gate materials (i.e., poly-Si, metal silicides) for threshold voltage tuning. A dielectric is then deposited for formed, for example forming a conformal low pressure chemical vapor deposition (LPCVD) SiO_2 dielectric deposited onto the substrate and nanowire. A gate pattern is then defined, such as by using standard photolithographic techniques. After developing the photoresist gate pattern, etch windows are created by plasma etching the exposed SiO_2 areas. The undesired Cr is then removed.

[0012] At this point the tips of the nanowires are still coated with the Cr gate metal. This material is then removed so as to prevent electrical shorting between the drain and gate electrodes. A combination of chemomechanical polishing and SiO_2 plasma etching techniques is suitable to expose the nanowire tips. The Cr surrounding the tips of the nanowires is then removed. A second coating of LPCVD SiO_2 is deposited onto the substrates to

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electrically isolate the gate and drain materials. Square drain pads are then photolithographically defined. The nanowire tips are subsequently exposed via SiO_2 plasma etching. SiO_2 is removed from the top of the nanowires in order to increase the contact surface area. Ni (50 nm) / Pt (30 nm) contacts are sputtered onto the drain regions, and NiSi contacts are formed after a rapid thermal annealing treatment. Before the final source contact is made, photoresist is spun onto the top device side of the substrate to protect the nanowire circuitry. Al contacts are thermally evaporated onto the backside of the substrates, after oxide removal. The device is subsequently annealed to achieve lower contact resistance.

[0013] In another embodiment, vertical integrated nanowire field effect transistors (VINFETs) are fabricated according to the following processing procedure. First, Si nanowires are grown vertically from a Si (111) substrate. After nanowire growth, the nanoparticle catalysts are etched away, for example by using aqua regia, followed by a standard water and isopropanol rinse, 7 min 300 W O_2 plasma clean. The substrates are then oxidized, for instance at 850 °C for 4-8 hours to achieve the desired gate SiO_2 dielectric thickness. Cr gate metal is preferably sputtered on to achieve a conformal coating, for example of 50-100 nm in this implementation. Alternatively, LPCVD techniques can be used to deposit the desired gate materials (i.e., poly-Si, metal silicides) for the desired threshold voltage tuning. From approximately 750 – 4000 nm of conformal low pressure chemical vapor deposition (LPCVD) SiO2 dielectric is then deposited onto the substrates. A gate pattern is then defined for example via standard photolithographic techniques. After developing the photoresist gate pattern, etch windows are created such as by performing plasma etching of the exposed SiO_2 areas using a LAM Research Corporation AutoEtch Plasma Etch System. The undesired Cr is removed, for example using Cr-7 Photomask etchant from Cyantek.

[0014] At this point the tips of the nanowires are still coated with the Cr gate metal. This material is then removed so as to prevent electrical shorting between the drain and gate electrodes. A combination of chemomechanical

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polishing and SiO_2 plasma etching techniques is suited for exposing the nanowire tips. The Cr surrounding the tips of the nanowires is then removed using Cr-7 etchant. A second dielectric coating is then formed, such as in the range of approximately 300-750 nm coating of LPCVD SiO_2 deposited onto the substrates to electrically isolate the gate and drain materials. Approximately 70 μm x 70 μm square drain pads are preferably photolithographically defined. The nanowire tips are subsequently exposed, such as via SiO_2 plasma etching. SiO_2 is removed from the top 50 nm of the nanowires in order to increase the contact surface area. Contacts are then formed, by way of example as Ni (50 nm) / Pt (30 nm) contacts sputtered onto the drain regions, and NiSi contacts formed after a two minute rapid thermal annealing treatment at 400 °C. Before the final source contact is made, photoresist is applied, such as being spun onto the top device side of the substrate to protect the nanowire circuitry. Al contacts are thermally evaporated onto the backside of the substrates, after oxide removal via SiO_2 plasma etching and 10:1 buffered HF. The device is subsequently annealed at 300 °C, to achieve lower contact resistance.

[0015] Patterned nanowire growth is described on structures, such as within channels, and channel sidewalls. In addition, bridging nanowires are described for being grown between structures. These various grown nanowires can be utilized for fabricating active or passive circuits, electromechanical devices and mechanical devices.

[0016] The invention is amenable to being embodied in a number of ways, including but not limited to the following descriptions.

[0017] One implementation according to the inventive teachings is a field effect transistor, comprising: (a) a nanowire extending from a substrate base, (i.e., in a substantially vertical direction from a horizontal substrate) and preferably grown therefrom; (b) a dielectric material surrounding at least a portion of the nanowire (e.g., vertical portion and/or circumferential portion but more preferably fully circumferentially surrounding the vertical nanowire along a portion of its length); (c) a gate material (i.e., Cr) surrounding at least a portion of the dielectric material; wherein the nanowire has an exposed tip,

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which is not covered with the dielectric material or the gate material; and (d) a drain material coupled to the exposed tip of the nanowire. The vertical integrated nanowire field effect transistor (VINFET) described can be configured for operation within any device, circuit or system.

[0018] Each vertical transistor can be formed from a single nanowire, or from a plurality of vertical nanowires, which extend from the substrate base and are coupled to the drain material of a single drain contact pad. The nanowire, or nanowires, for each vertical integrated transistor are grown from the substrate base. The growth orientation of the nanowires is preferably controlled by utilizing epitaxial crystal growth techniques. Implementations are described in which nanowires are grown according to a vapor-liquid-solid (VLS) process, or a vapor-liquid-solid epitaxy (VLSE) process. Growth proceeds utilizing SiCl4 as a gas phase precursor, without the need of separately incorporating HCl gas, during growing of the nanowire.

[0019] The nanowires are preferably grown from Si or Ge with any desired type and level of dopants. It should be appreciated that the material or dopant properties may be varied during nanowire growth to form a longitudinally patterned nanowire (i.e., modulating dopant type, level, or even material, such as between Ge and Si). Nanowire diameter is preferably controlled in response to the diameter of the alloy droplet utilized to catalyze nanowire growth from the substrate. A plurality of alloy droplets are contained within a colloidal metal (i.e., gold (Au)) which is dispersed on the surface of the substrate prior to growth of a plurality of nanowires. Nanowires grow on the substrate at sites of alloy droplets as these become overly saturated with the desired growth species. The alloy droplets are distributed across at least a portion of the substrate surface as monodispersed metal nanoclusters.

[0020] The substrate can be patterned with metal nanoclusters so that nanowires are grown only in selected areas. Patterning can be performed utilizing any desired method, for example via micro-contact printing.

[0021] An implementation can be described as a method of fabricating a vertical integrated nanowire field effect transistor, comprising: (a) growing a nanowire vertically in-place on a substrate (i.e., Si (111)); (b) etching away

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nanoparticle catalysts; (c) forming a desired gate dielectric thickness (i.e., oxidation to form SiO_2 layer); (d) depositing a gate metal (i.e., Cr) on the nanowire to achieve a conformal coating; (e) depositing a dielectric onto the substrate; (f) etching undesired gate metal wherein the nanowire has an uncoated tip; (g) depositing a dielectric onto the substrate to electrically isolate the gate and drain materials; and (h) forming a drain pad in contact with the exposed tip of said nanowire. It is also preferred that the device be annealed to lower contact resistance.

[0022] The nanowire growth phase preferably comprises: (1) dispersing metal nanoclusters of a desired diameter over one or more portions of the substrate, or within a pattern; and (2) epitaxially growing the nanowires to a desired length utilizing SiCl4 as a gas phase precursor.

[0023] Embodiments of the present invention can provide a number of beneficial aspects which can be implemented either separately or in any desired combination without departing from the present teachings.

[0024] An aspect of the invention comprises a vertical integrated nanowire field effect transistor.

[0025] Another aspect of the invention comprises devices, circuits and systems fabricated using vertical integrated nanowire field effect transistors.

[0026] Another aspect of the invention is the fabrication of vertical integrated nanowire transistors having consistent gate diameters.

[0027] Another aspect of the invention comprises growing nanowires in place from a substrate.

[0028] Another aspect of the invention comprises utilizing single nanowires, or more preferably any desired plurality of nanowires, to form channels within a single device.

[0029] Another aspect of the invention comprises controlling the diameter of nanowire growth in response to the diameter of the metal nanoclusters as seeds.

[0030] Another aspect of the invention comprises controlling the length of the nanowire in response to growth time.

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[0031] Another aspect of the invention comprises controlling distribution of metal nanoclusters by dispersing the nanoclusters such as within a colloidal metal.

[0032] Another aspect of the invention comprises growing nanowires within a trench or other structure, while retaining desired growth direction.

[0033] Another aspect of the invention comprises growing nanowire bridges between structures on a substrate.

[0034] Still another aspect of the invention is the direct integration of nanowire growth into the fabrication process, such as of vertical integrated nanowire transistors.

[0035] Further aspects of the invention will be brought out in the following portions of the specification, wherein the detailed description is for the purpose of fully disclosing preferred embodiments of the invention without placing limitations thereon.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

[0036] The invention will be more fully understood by reference to the following drawings which are for illustrative purposes only:

[0037] FIG. 1 is a schematic depicting conventional vapor-liquid-solid nanowire growth mechanisms with distributed metal catalysts, alloying, nucleation, and axial nanowire growth.

[0038] FIG. 2A - 2F are TEM images recorded during the nanowire growth process, showing Au nanoclusters in solid state at 500 C in FIG. 2A; alloying initiated at 800 C in FIG. 2B; liquid Au/Ge alloy in FIG. 2C; nucleation of a Ge nanocrystal on the alloy surface in FIG. 2D; Ge nanocrystal elongation in response to further Ge condensation in FIG. 2E; and formation of a wire in FIG. 2F.

[0039] FIG. 3A - 3B are TEM images of a vertical silicon (Si) nanowire array grown on a (111) crystal-oriented Si wafer, with monodispersed diameter, according to an aspect of the present invention.

[0040] FIG. 4 is a STEM image of two Si/Ge superlattice nanowires in the bright-field mode as grown according to an aspect of the present invention.

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[0041] FIG. 5A - 5F are schematics of vertical silicon nanowires surrounding gate transistors within different possible array and stack structures, according to an aspect of the present invention.

[0042] FIG. 6 is a schematic of a silicon nanowire vertical integrated field effect transistor, according to an aspect of the present invention.

[0043] FIG. 7A - 7C are schematics of a VINFET device fabrication process, according to an aspect of the present invention.

[0044] FIG. 8A is a scanning electron microscopy image of a VINFET device before drain contact, according to an aspect of the present invention.

[0045] FIG. 8B is a graph of ambipolar behavior of the VINFET of FIG. 8A.

[0046] FIG. 9A - 9B are images of Si Nanowires, grown according to an aspect of the present invention, showing a cross-sectional SEM image of vertically grown Si nanowires off of a Si (111) substrate in FIG. 9A; and TEM image of Si nanowire surrounded in a conformal SiO2 coating in FIG. 9B.

[0047] FIG. 10A is a schematic of VINFET device fabrication from vertical silicon nanowires, according to an aspect of the present invention.

[0048] FIG. 10B - 10D are images of VINFET fabrication as in FIG. 10A, showing top-view SEM images of a completed VINFET device in FIG. 10B; mid-section in FIG. 10C; cross-sectional image of a VINFET device in FIG. 10D.

[0049] FIG. 11A - 11D are graphs of VINFET device characteristics for devices fabricated according to the present invention.

[0050] FIG. 12A is a schematic of a VINFET inverter circuit.

[0051] FIG. 12B is a graph of VINFET characteristics for a device fabricated according to an aspect of the present invention, having multiple nanowires connected in parallel, which is shown to exhibit a substantial gain.

[0052] FIG. 13A - 13C are schematics of Si VINFET fabrication, according to an aspect of the present invention, showing Si nanowires grown in FIG. 13A, thermal oxidation to form gate oxide dielectric in FIG. 13B, and forming a Cr gate in FIG. 13C.

[0053] FIG. 14A - 14C are schematics of Si VINFET fabrication, according to an aspect of the present invention, showing LPCVD oxide deposition in FIG.

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14A; exposing nanowire tips in FIG. 14B; and etching back Cr gate material using Cr photomask etchant in FIG. 14C.

[0054] FIG. 14D - 14F are images of the Si VINFET device in response to steps shown respectively in FIG. 14A - 14C.

[0055] FIG. 15A - 15C are schematics of Si VINFET fabrication, according to an embodiment of the present invention, showing another layer of dielectric formed onto the nanowire in FIG. 15A; exposing nanowire tips in FIG. 15B; and forming drain electrode in FIG. 15C.

[0056] FIG. 16 A - 16F are images and associated size distributions for nanowire samples fabricated according to an aspect of the present invention.

[0057] FIG. 17A is a graph of SiNW growth density in relation to the relative concentration of the colloidal metal seeding solution, according to an aspect of the present invention.

[0058] FIG. 17B - 17C are images of typical nanowire growth at: 4/5 in FIG. 17B and 2/5 dilution in FIG. 17C.

[0059] FIG. 18A is a schematic of PDMS patterning of Au colloids, according to an aspect of the present invention.

[0060] FIG. 18B - 18C are SEM images of PDMS patterned SiNW growth in a side view as per FIG. 18B, and in a plan-view of the same in FIG. 18C.

[0061] FIG. 19A - 19C are images of Si nanowires grown directly in a micro-fabricated trench-channel, according to an embodiment of the present invention.

[0062] FIG. 20A is a schematic of Si nanowire bridge growth steps in micro-fabricated trenches, according to an aspect of the present invention.

[0063] FIG. 20B - 20C are images of parallel trenches formed on a SOI wafer in FIG. 20B; and of nanowire bridges grown in trenches in FIG. 20C.

[0064] FIG. 21A - 21C are SEM images of epitaxial alignment and interface cleanliness for Si nanowire growth in trenches, according to an aspect of the present invention, showing <111> crystallographic alignment in FIG. 21A, and magnifications in FIG. 21B and 21C.

[0065] FIG. 21D is a graph of X-ray photoelectron spectra of Si 2p region of FIG. 21A.

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[0066] FIG. 22A - 22D are images of connections established between Si nanowires and trench sidewalls, according to an aspect of the present invention.

[0067] FIG. 23A - 23C are images of Si nanowire bridging according to an aspect of the present invention, showing control of length in FIG. 23A, diameter in FIG. 23B; and density of bridging Si nanowires in FIG. 23C.

[0068] FIG. 24A is an SEM image of a nanowire-in-trench structure according to an embodiment of the present invention.

[0069] FIG. 24B is a graph of electrical measurements of the nanowire-in-trench structure of FIG. 24A illustrating current-voltage curves.

DETAILED DESCRIPTION OF THE INVENTION

[0070] Referring more specifically to the drawings, for illustrative purposes the present invention is embodied in the apparatus and methods generally shown in FIG. 1 through FIG. 24B. It will be appreciated that the apparatus may vary as to configuration and as to details of the parts, and that the method may vary as to the specific steps and sequence, without departing from the basic concepts as disclosed herein.

1. Silicon Nanowire Vertical integrated Surrounding-Gate FET.

[0071] As semiconductor devices are scaled into the sub 50 nm regime, short-channel effects and poor sub-threshold characteristics begin to be problematic for traditional planar transistors. Novel vertical integrated surrounding gate field-effect transistor (FET) device geometries are described which provide enhanced performance, as defined by improvements in functional density, energy efficiency, scalability, and compatibility with CMOS, are required in order to push toward ever higher packing densities with ever increasing energy efficiency, such as within memory and logic chips and circuits.

[0072] By way of example, a number of objectives are outlined below for this portion of the invention. (a) Creating a process of vertical integrated silicon nanowire array growth that provides tight control over size (such as <20 nm), uniformity (such as ± 10%), position (such as is amenable to addressability), density (such as on the order of 10^6 - 10^{12} cm^{-2}; scalability), and precise doping. (b) Demonstrate the first silicon nanowire vertical integrated

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surrounding gate transistor (Si-NW-SGT). (c) Propose the integration of Si nanowire vertical integrated surrounding gate transistors into arrays and stacks for memory and logic technologies.

[0073] In the process of transistor scaling, the introduction of several important device concepts in the past decade have been witnessed, such as: double-gate, tri-gate MOSFET, FinFET and surrounding gate MOSFET. In particular, the surrounding gate devices have the benefits of both reducing the channel effects and improving the sub-threshold characteristics, as well as providing significantly higher packing densities. The conceptual demonstration of these proposed device geometries has all been performed via the traditional top-down micro-fabrication processes (i.e., etching vertical structures into a substrate). In contrast, the current proposal relies on a bottom-up process (i.e., growing vertical structures from a substrate) to produce the precisely defined "channel" (epitaxial silicon nanowire vertical array) of the proposed surrounding gate transistors. The proposed vertical geometry also readily differentiates from the previous work on nanowire transistors, all of which adopt a lateral device geometry.

[0074] It should be appreciated that "vertical" is described herein in relation with a horizontal substrate, however, the nanowire transistors can be fabricated in a desired orientation (e.g., orthogonal, or along any given crystal orientation) which extends from a substrate surface.

[0075] Fabrication Approach.

[0076] Nanoscale one-dimensional materials have stimulated great interest due to their importance in basic scientific research and potential technology applications. Many unique and fascinating properties have been proposed and demonstrated for this class of materials, such as superior mechanical toughness, higher luminescence efficiency, and enhancement of thermoelectric figure of merit. Semiconductor nanowires are being considered as critical building blocks to assemble new generations of nanoscale electronic circuits and photonics.

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[0077] *Vapor-Liquid-Solid Epitaxial Growth of Nanowire Arrays*

[0078] One accepted mechanism of nanowire growth through a gas-phase reaction is the vapor-liquid-solid (VLS) process proposed by Wagner in 1960s during his studies of large single-crystalline whisker growth. According to this mechanism, the anisotropic crystal growth is promoted by the presence of a liquid alloy/solid interface.

[0079] FIG. 1 illustrates the process of Si nanowire growth by using Au clusters as the solvent at high temperature including seeding with a metal catalyst, followed by the three stages of alloying, nucleation and axial growth. Based on a Si-Au binary phase diagram, Si (from the decomposition of SiH_4, for example) and Au will form a liquid alloy when the temperature is higher than the eutectic point (363 C). The liquid surface has a large accommodation coefficient and is therefore a preferred deposition site for incoming Si vapor. After the liquid alloy becomes supersaturated with Si, Si nanowire growth occurs by precipitation at the solid-liquid interface.

[0080] FIG. 2A - 2F are example images taken in this lab which provide real-time observation of Ge nanowire growth conducted in a high-temperature in-situ transmission electron microscope (TEM). FIG. 2A shows Au nanoclusters in solid state at 500 C. FIG. 2B illustrates initiating of alloying at 800 C. FIG. 2C depicts liquid Au/Ge alloy, with nucleation of a Ge nanocrystal on the alloy surface shown in FIG. 2D. FIG. 2E shows Ge nanocrystal elongation in response to further Ge condensation with nanowire formation in FIG. 2F.

[0081] The results clearly show three growth stages: formation of Au-Ge alloy (FIG. 2B, 2C), nucleation of Ge nanocrystal (FIG. 2D) and elongation of Ge nanowire (FIG. 2E, 2F). These tests unambiguously demonstrate the validity of the VLS mechanism for nanowire growth. The establishment of a VLS mechanism at the nanometer scale is very important for the rational control of inorganic nanowires, since it provides the necessary underpinning for the prediction of metal solvents and optimized preparation conditions.

[0082] Based on our mechanism of nanowire growth we will demonstrate that one can achieve controlled growth of nanowires at different levels. The diameter of nanowire is determined by the size of the alloy droplet, which is in

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turn determined by the original cluster size. By using monodispersed metal nanoclusters, nanowires with a narrow diameter distribution can be synthesized. In addition, controlling the growth orientation is important for many of the proposed applications of nanowires, particularly for the vertical integrated transistor application taught herein. By applying the conventional epitaxial crystal growth technique into this VLS process, it is possible to achieve precise orientation control during the nanowire growth. The vapor-liquid-solid epitaxy (VLSE) technique is particularly powerful in controlled synthesis of nanowire arrays.

[0083] FIG. 3A - 3B are images depicting the formation of a highly uniform nanowire array. By way of example, Si is used with a (111) Si wafer as a substrate, upon which Si nanowires are grown epitaxially and vertically. The nanowires are highly uniform (in this case 60±5 nm in diameter). The length of the nanowires can be readily tuned from 1μm to 10μm by adjusting the growth time.

[0084] This VLSE method is described herein for growing silicon nanowire arrays with tight control over size (i.e., diameter <20 nm) and uniformity (i.e., < ± 10%). To demonstrate the scalability of this method the nanowire density will be controlled in the range of 10^6 - 10^{12} cm^{-2} by adjusting the initial nanocluster density on the substrates. In addition, in order to be able to address individual vertical integrated transistors, we propose to pattern the nanoclusters on the substrate to produce an ordered nanowire array, hence producing an addressable ultra-high density vertical integrated transistor array.

[0085] For the vertical integrated transistor to be functional, the precise doping within the nanowire represents a critical issue. Within the framework of VLS growth, suitable chemical vapor deposition conditions need to be mapped out so that possible surface diffusion of the dopants can be avoided. Beyond chemical doping, the VLS mechanism also allows the direct growth of longitudinal heterostructured nanowires, which should open up further technological opportunities.

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[0086] Researchers in this lab recently demonstrated the use of a hybrid pulsed laser ablation/chemical vapor deposition process for generating semiconductor nanowires with periodic longitudinal heterostructures. In this process, Si and Ge vapor sources were independently controlled and alternately delivered into the VLS nanowire growth system. As a result, single crystalline nanowires containing the Si/SiGe superlattice structure were obtained.

[0087] FIG. 4 depicts a scanning transmission electron microscopy (STEM) image of two such nanowires in the bright-field mode. Dark stripes appear periodically along the longitudinal axis of each wire, reflecting the alternating domains of Si and SiGe alloy. Since the supply of vapor sources can be readily programmed, the VLS process with modulated sources is useful for preparing a variety of heterostructures on individual nanowires in a "custom-designed" fashion. It will also enable the creation of various functional devices (e.g., p-n junctions, coupled quantum dot structures, and heterostructured unipolar and bipolar transistors) on individual nanowires. These heterostructured nanowires can be further used as important building blocks to construct nanoscale electronic circuits and light emitting devices.

[0088] *Silicon Nanowire Vertical integrated Surrounding-Gate FET*

[0089] Vertical silicon nanowire (and superlattice nanowire) arrays, when fabricated with tight control over size (< 20 nm), uniformity (± 10%), and precise doping, provide an excellent material platform for the fabrication of the vertical integrated surrounding gate transistors.

[0090] FIG. 5A - 5F illustrate silicon nanowire vertical integrated surrounding gate transistors in a variety of possible arrays and stacks. Illustrated in FIG. 5A through 5D, one can see how a circuit cell, or small structure, can be formed with integral vertical transistors coupled between conductive paths on different layers of the circuit. In addition, it should be appreciated that nanowires can be grown from any level of the circuit followed by the fabrication of VINFET transistors on those grown nanowires, wherein three-dimensional structures, such as shown in FIG. 5F, can be built up from multiple single layer two-dimensional structures as shown in FIG. 5E. It will be

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appreciated that dielectric structure fills may be present from which each succeeding layer may be built, however, these are not shown in the associated circuit structures for the sake of clarity. The vertical scalability of the process is readily seen from these diagrams additional details for which follow.

[0091] To demonstrate the device concept, we start with the fabrication of a single nanowire vertical integrated surrounding gate transistor. The substrate is patterned, such as with a low density of metal nanoclusters (10^{-6} cm^{-2}) which will be used to grow isolated nanowires. This is followed by forming a gate dielectric, for example by the use of controlled thermal oxidation of the silicon nanowires to create a dielectric oxide of suitable thickness. Alternatively, high-*k* dielectrics (such as HfO_2) can also be conformally coated on the nanowire surface, such as via atomic layer deposition. The degenerated substrate will be used as the source electrode contact. The gate electrode is then be deposited to surround the dielectric material (or at least a substantial portion thereof) which overlays the nanowire. The gating step is preferably followed with multiple steps of polishing, etching and final deposition of a drain metal electrode, for example as seen in FIG. 5A.

[0092] The present technique has been independently corroborated. A group at NASA demonstrated a vertical nanowire transistor based on the VLSE technique using isolated ZnO nanowires as based on a prior patent application of this lab. Their successful demonstration of the ZnO nanowire vertical transistor indicated that the proposed transistor may be feasible. The much more technological relevant silicon nanowire vertical integrated transistor demonstrated herein further required (1) developing a process for growing vertical silicon nanowires (which was demonstrated here); (2) developing different processes for making a silicon VINFET, and (3) controlling array distribution, density and nanowire size, such as with different diameters (60nm, 40nm, 20 nm and sub 10 nm).

[0093] Following the demonstration of fabricating a single silicon nanowire vertical integrated transistor, we synthesized high density, ordered, silicon nanowire arrays in order to create high density, addressable silicon nanowire

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vertical integrated transistor arrays and stacks (FIG. 5B-F).

2. Silicon Nanowire Vertical integrated Surrounding-Gate FET.

[0094] Semiconductor nanowires are being considered as critical building blocks to assemble new generations of nanoscale electronic circuits and photonics.

[0095] *Vapor-Liquid-Solid Epitaxial Growth of Nanowire Arrays*

[0096] Based on our mechanisms and study of nanowire growth, we have found it possible to achieve controlled growth of nanowires at different levels. The diameter of nanowires can be controlled in response to the size of the alloy droplet, which is in turn determined by the original cluster size. By using monodispersed metal nanoclusters, nanowires with a narrow diameter distribution can be synthesized. In addition, controlling the growth orientation is important in a number of proposed applications for nanowires, particularly for the vertical integrated transistor application put forth herein. By applying the conventional epitaxial crystal growth technique into this VLS process, it is possible to achieve precise orientation control during nanowire growth. This technique, vapor-liquid-solid epitaxy (VLSE), is particularly well-suited in the controlled synthesis of nanowire arrays.

[0097] An example of growing Si nanowires was shown in a preceding section relating to FIG. 3A - 3B. Using Si as an example, if a (111) Si wafer is used as a substrate, Si nanowires will grow epitaxially and vertically on the substrate and form a nanowire array as shown. The nanowires grown according to this method are highly uniform (60±5 nm in diameter). The length of the nanowires can be readily tuned from 1μm to 10μm by adjusting growth time. Aspects of the present invention utilize this VLSE technique to grow silicon nanowire arrays with tight control over size (diameter <20 nm) and uniformity (< ± 10%). To demonstrate the scalability of the proposed concept, nanowire density is also controlled in the range of from approximately 10^6 - 10^{12} cm^{-2} by adjusting the initial nanocluster density on substrates. In addition, to address individual vertical integrated transistors, patterning of the nanoclusters is demonstrated on substrates to produce ordered nanowire arrays, with the object of creating addressable ultra-high

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density vertical integrated transistor arrays.

[0098] For the vertical integrated transistor to be functional, the precise doping within the nanowire is a critical issue. Within the framework of VLS growth, suitable chemical vapor deposition conditions need to be mapped out to avoid surface diffusion of the dopants. Beyond chemical doping, the VLS mechanism also allows the direct growth of longitudinal heterostructured nanowires, which should open up further technological opportunities.

[0099] As mentioned above, researchers in this lab recently demonstrated the use of a hybrid pulsed laser ablation/chemical vapor deposition process for generating semiconductor nanowires with periodic longitudinal heterostructures. Since the supply of vapor sources can be readily programmed, the VLS process with modulated sources is useful for preparing a variety of heterostructures on individual nanowires in a "custom-designed" fashion. It will also enable the creation of various functional devices (e.g., p-n junctions, coupled quantum dot structures, and heterostructured unipolar and bipolar transistors) on individual nanowires. These heterostructured nanowires can be further used as important building blocks to construct nanoscale electronic circuits and light emitting devices.

[00100] *Silicon Nanowire Vertical integrated Surrounding-Gate FETs.*

[00101] Vertical silicon nanowire (and superlattice nanowire) arrays, with tight control over size (< 20 nm), uniformity (± 10%), and precise doping, provide an excellent material platform for the fabrication of vertical integrated surrounding gate transistors.

[00102] FIG. 6 illustrates an embodiment of a silicon nanowire vertical integrated field effect transistor having a gate that surrounds a nanowire grown from the substrate, and that is thus disposed between a source and drain.

[00103] FIG. 7A - 7C illustrate steps in the fabrication of an array of nanowire vertical integrated surrounding gate transistors (VINFET) as depicted in cross-section in FIG. 6. A substrate is patterned with a low density of metal nanoclusters (i.e., 10^{-6} cm^{-2}) for growing isolated nanowires. This is followed by controlled thermal oxidation of the silicon nanowires to create the dielectric

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oxide (i.e., SiO_2) of suitable thickness. Alternatively, high-*k* dielectrics (such as HfO_2) can also be conformally coated on the nanowire surface via atomic layer deposition. The degenerated substrate is used in this implementation as the source electrode contact, resulting in the structure shown in FIG. 7A.

[00104] The gate electrode in this case is deposited surrounding the dielectrics, as shown in FIG. 7B. Finally multiple steps of polishing, etching and final deposition of a drain metal electrode are carried out resulting in the VINFET device of FIG. 7C.

[00105] FIG. 8A and FIG. 8B depicts an SEM image of a VINFET device with a graph of its ambipolar behavior. In FIG. 8A the VINFET is shown after forming the gate electrode contact, but before the final step of drain electrode contact. With regard to the image, it should be noted that each individual bright spot in the cylindrical feature represents an individual vertical silicon nanowire channel. For the intrinsic nanowires prepared in this lab using $SiCl_4$ as sources, we found that they exhibit ambipolar behavior as can be seen from FIG. 8B. The observation of this ambipolar behavior is possibly a result of right carrier concentration within these intrinsic silicon nanowires although systematic studies should be carried forward to explore various doping conditions and optimization of VFET device performance including carrier mobility, and sub-threshold characteristics.

3. Vertical integrated Silicon Nanowire Field Effect Transistors.

[00106] Pushing the transistor geometry into the third dimension beneficially results in creating ultra-high transistor densities without the need for multi-step post-growth nanowire alignment processes. In addition, a vertical nanowire geometry promises enhanced transistor performance due to a surround-gate design. Herein the integration of vertically grown Si nanowire arrays into vertical integrated field effect transistors with a surround-gate architecture is demonstrated. These vertical integrated nanowire field-effect-transistors (VINFETs) exhibit excellent electronic properties comparable to traditional metal-oxide silicon field effect transistors (MOSFETs), suggesting that further optimization of this device structure may make them competitive with high-performance double-gate Fin field-effect transistors (FINFET) for future

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nanoelectronic devices. A VINFET based inverter demonstrates the feasibility of these devices for future logic and memory applications.

[00107] Moore's Law emphasizes the pace at which transistor sizes are reduced in order to increase the speed and density of transistors on an integrated circuit. However, conventional planar MOSFETs run into various performance limitations as gate-lengths are reduced below 50 nm. This is due to the inability of the gate electrode to effectively control source-drain current (a problem known as the short channel effect (SCE)), as well as the difficulty in proportionally scaling down gate oxide thickness and threshold voltage. These shortcomings result in significantly increased power consumption per transistor.

[00108] In order to further miniaturize the transistor while maintaining control over power consumption, alternative transistor geometries must be considered. Two such approaches are found in the use of silicon nanowire based devices and horizontal double-gate transistors. One example of horizontal double-gate transistors is known as a FINFET, whose structure is based on horizontal silicon fins sandwiched between two gate electrodes. Both of these approaches have exhibited large device mobilities and significantly reduced SCEs on the sub-100 nm scale. The FINFET has clearly demonstrated that the electrostatic efficiency of the gate electrode geometry is essential in reducing power consumption and overcoming short channel effects at this size scale. Individual silicon nanowire field-effect transistors have been shown to exhibit transistor properties that are comparable to bulk single-crystalline silicon devices. However, the transport properties of nanowire devices strongly depends on the nature of the nanowire surface. For example, hysteretic behavior of the threshold voltage is commonly observed due to the presence of surface and interface charge-trapping states on the nanowire surface. This surface dependence potentially limits transistor reliability. Additionally, the amount of energy and time required to align these nanowire components into a controlled high-density planar layout remains a significant hurdle for widespread application.

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[00109] Herein, we demonstrate that Si nanowires grown vertically from a Si (111) substrate can be used as active components in a vertical FET design featuring a surround gate geometry. In order to fabricate Si VINFETs, Si nanowires were grown in a vertical orientation on degenerately B-doped p-type (ρ <0.005 ohm-cm) Si (111) substrates as previously demonstrated. By way of example and not limitation, the wires were synthesized by the vapor-liquid-solid (VLS) growth mechanism in a CVD reactor using a $SiCl_4$ precursor, a BBr_3 dopant source, and metal nanoparticle growth-directing catalysts.

[00110] FIG. 9A is a scanning electron microscope (SEM) image of Si nanowires grown from 50 nm Au colloids. Transmission electron microscope (TEM) analysis confirms that these nanowires are single-crystalline and grow along the (111) direction off of an Si (111) substrate. Si nanowire arrays grown by the above method exhibit narrow diameter distributions with standard deviations (typically $\leq$ 9%) equal to the colloids from which they were grown.

[00111] Although the nanowires shown in FIG. 9A were grown with Au colloids, similar results have been achieved using other nanoparticle compositions such as industry-friendly Pt or Ti. Finally, positional alignment of these nanowires can be achieved by controlling the position of the nanoparticles, as well as using other methods including nanoimprint lithography and e-beam lithography. Thus, the dimensions and positioning of nanowire arrays can be accurately controlled to create suitable substrates for VINFET fabrication.

[00112] FIG. 9B is a TEM image of an Si nanowire surrounded in a conformal SiO_2 coating after dry oxidation at 850 C to form the gate dielectric. The scale bar in both FIG. 9A - 9B is 50 nm.

[00113] FIG. 10A illustrates an embodiment of a VINFET design according to the invention. These devices are fabricated using conventional very-large-scale integration (VLSI) processing, but without the need for post-growth assembly. Transistor structures having a surround gate structure have been taught and demonstrated herein to have the following advantages: (1) increased transistor density per unit area, due to the 3-dimensional device geometry; (2) a highly-efficient 'stranglehold' gate geometry resulting in

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excellent subthreshold behavior; (3) a 35% reduction of short-channel effects when compared with over double-gate devices.

[00114] It should also be appreciated that the ability to incorporate longitudinal and co-axial heterostructures into these nanowires allows future design flexibility, such as the on-chip incorporation of vertical SiGe heterostructures, for on-chip thermoelectric cooling. Furthermore, the nanowires can be embedded in a low charge trap-density SiO_2 toward reducing or eliminating hysteresis therein making transistor properties more consistent and reproducible. Si VINFETs are more readily integrated and technologically significant than prior ZnO and CuSCN VINFETs. Furthermore, the unique performance advantages demonstrated herein for the Si and Ge vertical integrated transistors due to the surround gate design have not been demonstrated in these bottom-up materials.

[00115] In this implementation, these vertically grown silicon nanowires were thermally oxidized to create uniform thermal oxides as dielectrics. A typical device in this case having a ~20-30 nm Si nanowire diameter, surrounded by approximately 30-40 nm of high-temperature gate oxide, and a Cr metal gate length of approximately 500-600 nm. More accurate values of gate-oxide thickness and nanowire channel diameter for specific devices have been obtained from TEM imaging, such as shown in FIG. 10B. Both the gate-oxide thickness and nanowire channel diameter can be easily reduced below 10 nm via conventional high-temperature thermal oxidation and SiO_2 etching chemistry. Initial VINFET devices were fabricated from nanowire arrays catalyzed by low-density nanoparticle arrays. Details about the fabrication process are described in the supplementary information. Each transistor device preferably contains a plurality of nanowires per drain contact pad, such as for example on the order of from six to many hundreds, and more preferably between approximately 8 to 269. FIG. 10B - 10D depicts images from a top-down view, perspective view and cross-sectional SEM view of a typical VINFET device according to the invention.

[00116] FIG. 11A - 11D illustrate characteristics for the fabricated VINFET devices. Typical drain-source current (I_{ds}) vs. drain-source voltage (V_{ds})

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measurements at various gate voltages (V_{gs}) indicate that B-doped VINFETs behave as accumulation-mode p-type transistors (FIG. 11A). The application of a negative (positive) V_{gs} results in an increase (decrease) of I_{ds}, due to the increase (decrease) of majority hole carriers. The V_{gs} value at which the I_{ds} is effectively turned on and accumulation begins is defined as threshold voltage (V_t). This is further demonstrated in the plot of I_{ds} vs. V_{gs} at different V_{ds} values for the same device (FIG. 11B). The average threshold voltage for 11 different devices was found to be 0.25 V ± 0.17 V (1σ). This threshold voltage is consistent with the expected values for nanowires with doping densities around 2×10^{16} cm^{-3}. Additionally, no dependence on the rate or direction of V_{gs} on the V_t was observed in any of these transistor devices. This is illustrated by the lack of hysteresis in the I_{ds} vs. V_{gs} curves when the V_{gs} is varied from negative to positive to negative values (see FIG. 11C and a more detailed section in FIG. 11D) at rates varying from 0.01-3 V s^{-1}. This is indicative of a very low number of charge-trapping states in or near the Si/SiO_2 gate oxide interface, and illustrates that consistent, reproducible transistor performance can be achieved with minimal outside ambient dependence, by embedding these devices in SiO_2.

[00117] The significant figures of merit of transistor performance include the transconductance (g_m), the device mobility (μ), on-off current ratio (I_{on}/I_{off}), subthreshold slope (S), and the drain-induced barrier lowering ($DIBL$). The transconductance is obtained from the slope of the linear region in the I_{ds} vs. V_{gs} plot at -1 V_{ds}. The g_m for all eleven devices ranged from 0.2 to 8.2 μS. Accurate comparison with other transistor devices requires normalizing the transconductance with the effective channel width (W_{eff}). Assuming W_{eff} equals the number of nanowires in each pad multiplied by the diameter of each nanowire, the normalized transconductance of these devices was found to range from 0.65 to 7.4 μS μm^{-1}. These values are comparable to those reported for thin silicon-on-insulator (SOI) MOSFET (5-12 μS μm^{-1})[26] and p-type SiNW (0.045 – 11 μS μm^{-1}) devices.

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[00118] The device mobility of an individual nanowire is extrapolated from its transconductance via the equation; $\mu = g_m * L^2 / (C\ N\ V_{ds})$, where L is the gate length, N is the number of nanowires, and C is the gate capacitance for an individual nanowire. The gate capacitance is described by the equation; $C = 2\ \pi\ \varepsilon_0\ \varepsilon_{SiO2}\ L / ln\ (r_g / r_{nw})$, where ε_{SiO2} is the dielectric constant of the gate SiO_2, r_g is the inner radius of the gate electrode, and r_{NW} is the nanowire radius. The hole mobilities, averaged from all V_{ds} values between -0.25 and -2.5 V_{ds}, range from 11-97 $cm^2\ V^{-1}s^{-1}$ with an average mobility of 35 $cm^2\ V^{-1}s^{-1}$. These hole mobilities are comparable to those reported for unfunctionalized p-type silicon nanowires (20–100 $cm^2\ V^{-1}\ s^{-1}$), and close to the best reported values of p-type SOI MOSFETs (~180 $cm^2\ V^{-1}\ s^{-1}$).

[00119] The I_{on}/I_{off}, S, and *DIBL* can be extracted upon plotting the I_{ds} vs. V_{gs} on a logarithmic scale (FIG. 11C, 11D). The I_{on}/I_{off} ratio is the ratio of I_{ds} at current saturation (I_{on}) to I_{ds} at depletion (I_{off}). I_{on}/I_{off} ranges from approximately 10^4 to 10^6 for all devices. Small *DIBL* is indicative of reduced short channel effects, and is estimated by measuring the shift in V_t at a low and high V_{ds}. The *DIBL* for a typical device is 40 mV per -1 V_{ds}, which is comparable to previously reported values for FINFETs. This figure of merit is expected to become more significant upon further reduction of the gate length. Finally, the minimization of the subthreshold slope is necessary for low power switching applications in digital electronics. The S value for a typical device having a 300 Å gate oxide shell is 120 mV/decade. Although this is approximately double the theoretical room temperature limit of 60 mV/decade, it is much smaller than typical values obtained for nanowire devices with back-gate or top-gate geometries (typically > 300 mV/decade). Further reduction of S is possible by using thinner gate oxides and high-k materials as the gate dielectric.

[00120] The full I_{ds} vs. V_{ds} curves for all devices have a small nonlinearity at negative V_{ds}, and are rectifying with a one order of magnitude decrease in current at positive V_{ds} (Inset in FIG. 11A). Such nonlinearity in the positive and negative V_{ds} is expected as there are two different Si contacts: a large

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area (~1 cm^2) source contact to the degenerately doped p-type Si substrate, and a small area (~4500 nm^2) medium-doped p-type nanowire drain contact. This nonlinearity is partly due to the large resistance of a Schottky barrier at the p-type nanowire drain. Decreasing the contact resistance will result in better transistor performance by effectively increasing g_m, I_{on}/I_{off}, and μ. The minimization of series contact resistance at the sub-20 nm scale still remains a significant challenge for the semiconductor industry.

[00121] FIG. 12A is an inverter circuit using resistor-transistor logic (RTL) to demonstrate the feasibility of using these devices for digital logic applications. This structure was fabricated by connecting a 200 MΩ resistor to one of our p-type VINFETs in series. When the input voltage is ~ -0.9 V, the output voltage switches between the source voltage (0 V) and the drain voltage (-3.5 V). A large voltage gain of approximately 28 was exhibited, as extracted through differentiating the input and output voltage (left inset in FIG. 12B), which is evidence that these are high-performance devices suitable for use in microelectronic applications. The ideal inverter resistor should have a resistance value preferably in a range between the on and off state transistor resistances. Therefore, future on-chip logic integration using properly gated VINFETs as resistors can be easily fabricated via source patterning SOI substrates.

[00122] The described Si VINFET device implementations represent a novel platform for silicon nanowire electronics that combine the epitaxial growth of silicon nanowires with aspects of top-down fabrication. These unoptimized devices already show transport properties comparable to standard planar MOSFETs. Future optimization of the processing, device geometry, doping concentration, the use of high-k dielectrics, as well as gate length reduction may competitively position these devices over high efficiency FINFETs in the sub-10nm regime.

[00123] Embodiment of VINFET Fabrication Procedure.

[00124] FIG. 13A - 13C illustrate an example embodiment of a generalized process for Si VINFET fabrication. In FIG. 13A Si nanowires are grown vertically from a Si (111) substrate. In FIG. 13B a gate dielectric layer is

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formed, for example using thermal oxidation of the Si nanowire to form SiO_2 as a gate oxide dielectric. In FIG. 13C a Cr gate material is sputtered onto the nanowires to achieve a conformal coating.

[00125] The following describes this processing in greater detail. Nanowire growth is performed as depicted in FIG. 13A. Next, the nanoparticle catalysts are etched away, such as by using aqua regia followed by a standard water and isopropanol rinse and a 7 min 300 W O_2 plasma clean. Nanowires having diameters greater than 40 nm and aspect ratios less than 40 are mechanically resilient enough to remain vertical after the standard pre-gate oxide thermal oxidation cleaning procedure despite solvent surface tension forces (smaller diameters and larger aspect ratios were not measured). The substrates were oxidized at 850°C for 4-8 hours to achieve the desired gate SiO_2 dielectric thickness as depicted in FIG. 13B.

[00126] The Cr gate metal is then formed, in this case by sputtering to achieve a conformal 50-100 nm coating, as seen in FIG. 13C. Alternatively, LPCVD techniques can be used to deposit the desired gate materials (i.e., poly-Si, metal silicides) for threshold voltage tuning.

[00127] FIG. 14A - 14F illustrates additional fabrication steps FIG. 14A - 14C and corresponding SEM images. In FIG. 14A a layer of approximately 750 - 4000 nm of conformal low pressure chemical vapor deposition (LPCVD) SiO_2 dielectric was deposited onto the gated nanowires and substrate, as depicted schematically in FIG. 14A with a corresponding SEM image shown in FIG. 14D. A gate pattern was then defined, such as via standard photolithographic techniques. After developing of the photoresist gate pattern, etch windows were created by plasma etching, and/or a combination of chemomechanical polishing and SiO_2 plasma etching techniques of the exposed SiO_2 areas, thus exposing the Cr nanowire tips as depicted in FIG. 14B and FIG. 14E. For example, plasma etching can be performed using a LAM Research Corporation AutoEtch Plasma Etch System. At this point in the process the tips of the nanowires are still coated with the Cr gate metal. This material must be removed so as to prevent electrical shorting between the drain and gate electrodes. The undesired Cr was etched-back, removed, as depicted in

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FIG. 14C and FIG. 14F. The etchant may comprise, for example, a photomask etchant, such as Cr-7 Photomask etchant from Cyantek. All SEM scale bars correspond to 1 μm, and all images are obtained at a tilt angle of 30°.

[00128] FIG. 15A - 15C illustrate another stage of VINFET fabrication. A second coating of dielectric, in the range from approximately 300-750 nm, such as LPCVD SiO_2, was deposited onto the substrates to electrically isolate the gate and drain materials as depicted in FIG. 15A. Drain pads were defined, for example 70 μm x 70 μm square drain pads, such as by photolithography methods. The nanowire tips were subsequently exposed via SiO_2 plasma etching. In addition, SiO_2 was preferably removed from the top 50 nm of the nanowires in order to increase the contact surface area, resulting in the structure depicted in FIG. 15B. Contacts are formed, in this case from Ni (50 nm) / Pt (30 nm) sputtered onto the drain regions, and NiSi contacts formed after a two minute rapid thermal annealing treatment at 400 °C which results in the structure shown in FIG. 15C. Before the final source contact is made, photoresist is preferably spun onto the top device side of the substrate to protect the nanowire circuitry. Contacts, such as Al, were thermally evaporated onto the backside of the substrates, after oxide removal, such as via SiO_2 plasma etching and 10:1 buffered HF. Preferably, the device was subsequently annealed, for example at 300°C to achieve lower contact resistance.

[00129] Threshold Voltage Analysis.

[00130] An approximate analytical function for vertical cylindrical FET devices has been previously developed by Sharma, Zaidi, Lucero, Brueck, S. R. J. & Islam, in an article entitled "N. E. Mobility and transverse electric field effects in channel conduction of wrap-around-gate nanowire MOSFETs" published in IEEE Proceedings-Circuits Devices and Systems 151, 422-430 (2004). In the case of our system, having p-type nanowires with a Cr gate electrode, the threshold voltage (V_t) can be approximated by the following formula:

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[00131]
$$V_t = V_{FB} + 2\Phi_F + \frac{qN_A r_{NW}^2}{2\varepsilon_0 \varepsilon_{SiO2}} \ln(1 + \frac{t_{OX}}{r_{NW}}) \quad (1)$$

[00132] Where V_{FB} is the flatband voltage (the voltage that is applied to the gate electrode at which the Fermi energy of the gate electrode lines up with the Fermi energy of the nanowire channel), r_{NW} is the nanowire radius, t_{Ox} is the gate oxide thickness, and N_A is the acceptor concentration in Si. The value of Φ_F is given by the formula;

[00133]
$$\Phi_F = \frac{kT}{q} \ln(\frac{N_A}{n_i}) \quad (2)$$

[00134] Where n_i is the intrinsic carrier concentration in Si. V_{FB} can be deduced by the following equation;

[00135]
$$V_{FB} = \Phi_M - \chi - \frac{E_g}{2} - \Phi_F \quad (3)$$

[00136] Where Φ_M is the gate work function, χ is the electron affinity of Si, and E_g is the band gap of silicon. Solving Eq. (1) for N_A using the average observed threshold voltages gives an average carrier concentration of 5×10^{16} cm^{-3}. More accurate analysis of the influence of carrier concentration on threshold voltage at these small length scales can be derived using drift-diffusion simulations.

4. Controlled Growth of Si Nanowire Arrays for Device Integration.

[00137] In this section silicon nanowires are synthesized in a controlled manner for their practical integration into devices. Gold colloids were utilized for nanowire synthesis by the vapor - liquid - solid (VLS) growth mechanism. Using $SiCl_4$ as the precursor gas in a chemical vapor deposition system, nanowire arrays were grown vertically aligned with respect to the substrate. By manipulating the colloid deposition on the substrate, highly controlled growth of aligned silicon nanowires was achieved. Nanowire arrays were synthesized with narrow size distributions dictated by the seeding colloids and with average diameters down to 39 nm. In these demonstrations the density of wire growth was successfully varied from approximately 0.1 - 1.8 wires / μm^2. Patterned deposition of the colloids led to confinement of the vertical

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nanowire growth to selected regions. In addition, Si nanowires were grown directly into micro-channels to demonstrate the flexibility of the deposition technique. By controlling various aspects of nanowire growth, these methods will enable their efficient and economical incorporation into devices.

[00138] Silicon nanowires (SiNWs) have been identified as useful building blocks for nanoscale electronic and thermoelectric devices. To realize their full potential in applications, however, SiNW must be integrated efficiently and economically into various device architectures. Devices have been constructed around single, or several, dispersed SiNWs, and methods have been developed to manipulate as-grown nanowires into geometries amenable to large-scale device fabrication. Alternatively, controlled growth of SiNWs in predetermined configurations would eliminate much of the processing associated with device fabrication. Furthermore, vertical growth (substantially perpendicular to the substrate) allows three-dimensional integration for more complex structures, such as vertical integrated field-effect transistor (VFET) arrays. Such arrays could afford higher transistor densities and novel three-dimensional logic or memory architectures.

[00139] The VLS growth mechanism is a synthetic technique which is particularly well-suited to controlling SiNW growth. VLS growth by chemical vapor deposition (CVD) can produce epitaxially aligned, single-crystalline wires. Specifically, SiNWs may be grown via the VLS process using gold thin films. Metal thin film, however, may not be as well suited to providing good diameter control of the resulting wires due to the randomness of the film breakup at reaction temperatures. Also, precise growth and epitaxial alignment of SiNWs has only been achieved using lithographically defined regions of SiNW growth by thin film evaporation. These methods employ expensive processing techniques with limited control over nanowire size and density.

[00140] However, gold colloids can be used to produce well-dispersed and diameter-controlled SiNWs, although simultaneous control over the size, position and epitaxial growth has not been achieved previously. Methods have been taught herein to grow vertically aligned SiNW with controlled

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dimensions and specific placement by the conventional VLS-CVD synthesis. Using a thin polyelectrolyte layer, gold colloids are electrostatically attracted and immobilized on the substrate to act as seeds for Si nanowires grown using the VLS-CVD method. The diameter of the colloids precisely controls the nanowire diameter. The concentration of the colloid solution controls the density of growth. Micro-contact printing of the polyelectrolyte layer can be used as a means to confine wire growth to patterned regions. Moreover, these versatile techniques facilitate incorporation of vertically aligned SiNWs into more complex systems, such as micro-fluidic channels.

[00141] In general, Au colloids are used to define the diameter and position of the SiNWs. Subsequent wire growth occurs along the <111> direction and is vertical due to the epitaxial growth of Si wires from the binary liquid droplet onto the underlying substrate, for example an Si (111) wafer, as previously shown. The colloids were immobilized on the wafer surface, such as adsorbing a thin layer of polyelectrolyte onto the substrate surface, for instance in response to a quick immersion in 0.1 wt% poly-L-lysine. After rinsing with DI water, the substrates were immersed in the Au nanoparticle solution (10^{10} - 10^{11} particles/mL). It should be noted that the polymer possesses a net positive charge in an aqueous solution at neutral pH and hence adsorbs onto the substrate due to its electrostatic attraction to deprotonated hydroxyl groups on the silica layer. Consequently, the polymer film presents a positively charged surface to the negatively charged Au colloids in aqueous solution, attracting them to the surface. Following a final rinse with DI water and drying, the substrates were used for nanowire growth in a CVD furnace as reported previously.

[00142] The precursor molecules utilized for SiNW growth in the CVD system was $SiCl_4$. Growth of various substrates seeded with Au colloids was conducted at temperatures between 800°C and 850°C. H_2 (10%) in Argon was used as the carrier gas to flow through the Si precursor bath and into the reaction tube. The substrates were cleaned with acetone and IPA before polymer and colloid deposition. The polymer was presumably ashed by the high reaction temperatures and a reducing H_2 environment. Gaseous HCl, a

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byproduct of $SiCl_4$ decomposition in the reaction tube, etched the oxide layer on the Si surface, presenting a clean Si crystal surface to precipitating Si from the binary liquid droplet. Epitaxial deposition of Si at this interface induced growth direction alignment of the nanowire with the crystal face of the Si wafer. Consequently, such alignment could be more difficult using other CVD precursors, such as SiH_4, without separately adding HCl gas or taking special precautions to remove the oxide layer before SiNW synthesis.

[00143] SiNWs synthesized by the above method on a Si (111) substrate yielded vertically aligned, single-crystalline wires, as observed by scanning and transmission electron microscopy (SEM and TEM). Wires aligned along the three [-111] directions were also observed, especially in synthesis using smaller colloidal catalysts, but the gas flow rate and reaction temperature were optimized to preferentially grow vertical wires for each colloid system.

[00144] FIG. 16A - 16G illustrate nanowire samples and their diameters as formed according to the following. Au colloids are well suited as seeds for controlling the SiNW diameter: The Au colloids act as the seeding metal for nanowire growth by the VLS process, and Au colloids may be synthesized, or obtained commercially, with relatively narrow size distributions. Since each colloid seeds growth for one nanowire, aligned nanowires can be grown with narrow size distributions approaching those of the seed particles. Hence, by seeding wire growth with colloids of different average size, we were able to precisely control the average diameter of the SiNW arrays, as seen in FIG. 16B, 16D and 16F. Size distributions of both colloids and nanowires were determined from TEM micrographs. SiNWs grown from Au colloids of 50 (56 $\pm$ 5.0), 30 (30 $\pm$ 3.3), and 20 (20 $\pm$ 2.1) nm diameters were 93 $\pm$ 7.4, 43 $\pm$ 4.4, and 39 $\pm$ 3.7 nm in diameter, respectively.

[00145] Extensive TEM characterization as shown in FIG. 16G indicates that these wires are single crystalline in nature. We would like to emphasize that although monodisperse silicon nanowires can be synthesized using monodispersed Au colloids as seeds, epitaxially grown, monodispersed silicon nanowires were grown in this novel chloride based CVD process.

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[00146] The SiNWs were wider than their respective seed particles due to the influx of Si into the colloids and alloy formation during the synthesis. The seed droplets swell in size until the critical supersaturation concentration is reached, at which point Si begins precipitating on the Si (111) surface below. The interface between the Au-Si droplet and the substrate determines the area of precipitation of Si, and thus the SiNW diameter. Despite their larger size, however, the nanowires have approximately the same relative standard deviation of diameter as the colloidal solutions used to seed their growth. The standard deviations of the 50, 30 and 20 nm colloids used in this study are ± 8.8%, 11%, and 11% of the average size, respectively. The standard deviations of the wires grown from these colloids are ± 7.9%, 10%, and 9.5% of the average size, respectively. This data suggests that precise diameter control of nanowires grown by this method is limited only by the size distribution of the seed particles. Hence, appropriate colloidal solutions could be used to grow monodisperse nanowire arrays.

[00147] FIG. 17A - 17C illustrate nanowire growth density in response to colloid concentration. SiNW growth density depends on the relative concentration of the seeding solution as seen in the graph of FIG. 17A. In this example, all colloid solutions were diluted from the same stock solution. The images illustrate typical nanowire growth at 4/5 in FIG. 17B and 2/5 dilution in FIG. 17C, with 1μm scale bars shown on each image.

[00148] The density of nanowire growth is critical to proper device function. By varying the concentration of the seeding solution (using 50 nm Au colloids as an example), we were able to control the seeding density on the substrate surface. The graph of FIG. 17A shows the relationship between nanowire growth density, as determined from SEM images, for example those shown in FIG. 17B and FIG. 17C, and dilution of the gold colloid stock solution. Wires were seeded with densities ranging over an order of magnitude, from approximately 0.1 - 1.8 wires/μm^2. In general, a beneficial 1-to-1 nanoparticle/nanowire ratio can be achieved although it was observed that optimal growth conditions varied slightly with nanowire seeding density.

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[00149] FIG. 18A - 18B illustrate an example of polydimethylsiloxane (PDMS) patterning of Au colloids. Spatial control over SiNW growth is achieved by patterning regions of seed particles, such as by using micro-contact printing. The steps of PDMS patterning of Au colloids is shown schematically in FIG. 18A. Briefly, a PDMS stamp is molded to the relief pattern of a photoresist master. In this example a polydimethylsiloxane (PDMS) stamp was made using a photoresist master of 2 μm lines with 2 μm separation. After curing the polymer, the stamp is removed from the master and "inked" with a solution of poly-L-lysine, such as by the same method described above for deposition on the Si substrates. The stamp pattern is transferred to the Si (111) substrate, and the pattern was transferred to the substrate, such as by placing the stamp on the substrate and heating at 70°C for 5 minutes. After this the substrate with the pattern is immersed in the Au colloid solution. For example immersion in a 50 nm Au colloid solution for a short time, such that colloids only adhere to the polyelectrolyte and not the bare Si. The colloid-patterned substrate is then grown using the conventional VLS-CVD synthesis, resulting in a corresponding pattern of SiNW arrays.

[00150] A cross-sectional SEM image of PDMS patterned SiNW growth is shown in FIG. 18B, with FIG. 18C showing a plan-view SEM image of the same. Scale bars on each image are 1μm. The resulting growth, seen in the images is strictly confined to the regions of poly-L-lysine deposition. The plan-view SEM image (FIG. 18C) shows a small portion of the pattern, which is consistent over several square millimeters, which corresponds with the extent of the stamped area that was immersed in the colloid solution.

[00151] FIG. 19A - 19C illustrate growth of SiNWs directly in a micro-channel. This colloid-seeded growth method represents a convenient way to incorporate nanowires into other systems, such as micro-fluidic systems. The micro-channels shown in FIG. 19A - 19C for this example were 8 μm deep and 40-100 μm wide. They were etched into a Si (111) wafer by deep reactive ion etching (DRIE) using SF_6/O_2 as the etchant and C_4F_8 as the sidewall passivation gas. The middle portion of a micro-channel array was covered with an O_2 plasma-treated piece of blank PDMS. The PDMS

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encloses the micro-channels by adhering to the top Si (111) surface. The colloid deposition method resembles those discussed above. First, a droplet of the poly-L-lysine solution was placed on one end of the micro-channel array, touching the PDMS. The solution was transported by capillary action to the open end of the channels. After rinsing in DI water, the PDMS was replaced and a droplet of 50 nm Au colloid solution was placed where the polymer solution had been. In the same manner as before, the solution flowed to the opposite end of the channels, and then the substrate was rinsed again. The wires were grown directly in the channels under the same conditions as previous synthesis.

[00152] FIG. 19A is a plan-view SEM image in which it is seen that nanowire growth is almost completely confined to the floor of the channel. FIG. 19B shows an approximate 45° tilt view while FIG. 19C is a cross-sectional SEM view of the same channel. Scale bars in each image are 10μm in length. As can be seen from these images, nanowire growth and vertical alignment was not affected by either the roughness of the floor of the channel, due to etching, or any changes in precursor gas flow dynamics near the channel walls. Furthermore, use of the PDMS resulted in restricting gold colloid deposition predominantly to the floor of the micro-channel. There is insignificant nanowire growth on the top surface of the substrate, so the micro-channels may be resealed with PDMS to function as a micro-fluidic device, such as for macromolecular separation based on SiNWs as diffusion barriers.

[00153] In summary, using directed colloid seeding for VLS-CVD SiNW synthesis provides precise control over nanowire diameter, growth density, and spatial distribution. At the same time, the $SiCl_4$ precursor is highly effective for the growth of vertically aligned, single-crystalline SiNWs. Moreover, these techniques facilitate the direct integration of nanowires into complex systems such as micro-fluidic devices. The versatility of the growth control methods described herein benefit from the use of $SiCl_4$ as the gas phase precursor. Other Si precursors (e.g., SiH_4) offer less flexibility of substrate preparation and vertical SiNW alignment as they require separately incorporating HCl gas. Specifically, the aligned growth of SiNWs makes this

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process well-suited for fabricating array devices, such as VINFET circuits, and two-dimensional photonic crystals. Additionally, these arrays may serve as scaffolding for the deposition of other materials for an even wider range of applications. Such in-place growth control will aid the incorporation of nanowires into devices.

5. Si Nanowire Bridges in Micro-trenches & Integration of Growth in Fabrication.

[00154] Silicon nanowires are attractive building blocks for nano-scale electronic systems due to their compatibility with existing semiconductor technology. Studies have focused on their synthesis, with considerable advances made in the control of structures, electrical and thermal properties. For practical applications, different strategies have been explored to fabricate nanowire-based devices. Pick-and-place approaches have succeeded in making individual devices such as field effect transistors (FETs), isolated thermal bridges and chemical sensors, but the approach is time-consuming and unsuitable for large scale manufacturing. The Langmuir-Blodgett technique has been utilized as a powerful and low-cost approach to align nanowires and make large scale arrays of devices, showing a significant advance towards nanowire-based integrated circuits.

[00155] However, in some circumstances, instead of following the "bottom-up synthesis first, assembly and top-down fabrication next" approach, it is more beneficial to grow nanowires precisely and rationally in pre-determined device architectures. Direct integration of nanowire growth into the fabrication process markedly simplifies procedures and avoids deterioration of nanowires in some micro-fabrication or nano-fabrication processes. In this section, Si nanowires have been grown laterally in micro-trenches pre-fabricated on silicon-on-insulator (SOI) wafers, demonstrating that nanowire growth and device fabrication can be achieved simultaneously. Lateral bridging growth was first demonstrated for GaAs nanowires and recently for Si nanowires. However, well-controlled growth and device operation were not achieved. Accordingly, in this section epitaxial growth of bridging Si nanowires and effective control of diameters, lengths, and densities is demonstrated. Electrical measurements of these Si nanowires indicates that nanowires in

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trenches could serve as versatile active components in circuits.

[00156] FIG. 20A - 20C illustrates the use of nanowires grown in trench structures to create bridging nanowires. In FIG. 20A a schematic illustration of Si nanowire bridge fabrication is shown connecting between two vertical Si{111} surfaces on (110) oriented SOI wafers. The idea of nanowire-in-trench structures is based on epitaxial growth of Si nanowires. Si nanowires grow preferentially along <111> directions. If the vertical {111} planes contained in a Si(110) wafer are exposed by vertical etching, Si nanowires can be grown laterally, bridging the two face-to-face {111} surfaces, as illustrated in FIG. 20A. In this procedure, fabrication started with a heavily doped Si(110) SOI wafer, into which trenches were micro-fabricated photolithographically, such as by proper alignment of the substrate and the pattern so that the {111} planes were exposed.

[00157] FIG. 20B shows a scanning electron microscopy (SEM) image of a group of parallel trenches. After forming these trenches, Au clusters were dispersed on the substrate as catalysts for vapor-liquid-solid (VLS) growth of nanowires carried out in a subsequent chemical vapor deposition (CVD) process using $SiCl_4$ as the precursor. It is expected that when a growing nanowire impinges into the opposite sidewall, an electrical or thermal connection is automatically made with the bridging Si nanowire being the active unit, the Si pads confine the trench as electrodes, and SiO_2 layer underneath as the insulator/dielectric barrier.

[00158] FIG. 20C shows the SEM image of such a structure. Two nanowires with diameter of approximately 80 nm have bridged the 2 μm wide $(1\ \bar{1}\ \bar{1})$ trench and one nanowire has bridged in the $(1\ \bar{1}\ 1)$ trench. Excellent epitaxy and interface cleanliness shown here are two of the advantages of the CVD process based on $SiCl_4$ precursor and Au clusters. These are crucial for obtaining devices with high quality.

[00159] FIG. 21A - 21D illustrate in greater detail epitaxial alignment and interface cleanliness for Si nanowire growth in trenches. Epitaxial growth, as the foundation of this work, is discussed first. For the samples shown, the SiO_2 mask used in photolithography to form the trenches, was removed

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before growth to allow nanowires to grow on the top exposed Si(110) surfaces. As shown in FIG. 21A, besides perpendicular growth of nanowires on the {111} vertical surfaces as expected, well aligned nanowires also grew along [1 1 $\bar{1}$] and [1 1 1] directions on the (110) top surface. It should be noted that <111> crystallographic alignment is exhibited on both Si{111} and {110} surfaces. Crystallographic geometry is illustrated by the projection of four <111> vectors. Similar results were obtained in the epitaxial growth of GaAs nanowires. Moreover, surface roughness was found to have little influence on epitaxy.

[00160] In the close-up image of the vertical {111} surface of FIG. 21C, scalloping of the surface is noticeable, which was caused by the deep reactive ion etching (DRIE) cycles during the micro-fabrication of the trenches. Nonetheless, nanowires persisted to grow along the <111> directions without much influence from the local variation of surface orientation. One can conclude that the epitaxially grown Si nanowires always align themselves with crystallographic <111> directions, with the substrate local orientation, such as due to roughness, only affecting which specific <111> direction the nanowires prefer (e.g., nanowires prefer the perpendicular [111] direction for a relative smooth (111) surface).

[00161] This alignment is believed to be driven by the energetically favorable <111> growth and facilitated by crystallization at the liquid-solid interface in the VLS process. Here, we stress the uniqueness of our $SiCl_4$-based CVD synthesis, because no epitaxial alignment as significant as that exhibited herein has been observed in other synthesis methods such as pulsed laser deposition, thermal evaporation of SiO_2 and SiH_4 CVD. This robust tendency for Si nanowires to align along the <111> directions substantially simplifies device fabrication processes, such as by reducing the requirement to perform alignment by etching (to find <111> directions precisely) and polishing of surfaces.

[00162] Thin film deposition is a process that could, for example, be performed simultaneously with VLS growth of nanowires in CVD. To prevent potential current leakage through an unintentionally deposited Si film, this film

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deposition must be minimized especially on the insulating SiO_2 surfaces. The growth conditions chosen in the present work ensure that the deposition rate of thin films is negligible during VLS growth. For example, there is no observable deposition besides nanowires on Si(110) surface in FIG. 21B, nor on Si(1 $\bar{1}$ $\bar{1}$) surface FIG. 21C.

[00163] More quantitative results were obtained by X-ray photoelectron spectroscopy (XPS), a surface sensitive characterization technique. As shown in FIG. 21D, there are no differences between the two Si 2p spectra taken from the insulating SiO_2 surface before and after a 30-minute CVD process. Only the chemically shifted Si-2p peaks characteristic of SiO_2 are observed at 103.8 eV while the Si-2p peaks of elemental Si at 99.8 eV are absent (Standard Si-2p peak is 103.3 eV for SiO_2 and 99.3 eV for Si). Basically, the large difference in deposition rates between thin films and nanowires is attributed to the catalytic action of liquid droplets in the VLS growth. Furthermore, in $SiCl_4$ CVD, thin film growth is further suppressed by the well documented etching effect of Cl species generated at high temperatures.

[00164] FIG. 22A - 22D illustrates evaluating nanowire connections between the Si nanowires and the trench sidewalls using overgrown nanowires. For device applications, it is important to ascertain the characteristics of connections formed between the Si nanowires and the sidewalls. This issue was investigated in over-grown nanowires with lengths exceeding the widths of trenches. The sample is shown in the figures in which nanowires with average lengths of 4 μm were grown in 2 μm wide trenches. Nanowires 1 and 2, as indicated on the SEM images, are located in different positions of a trench, and nanowire 3 located in another trench, were arranged together for easy comparison as seen in FIG. 22A. Nanowire 1 grew in a straight path along the [$\bar{1}$11] direction with no blockage and is used as a reference for the other two nanowires. Nanowires 2 and 3 shown in FIG. 22C-22D, which are grown along the [1 $\bar{1}$ $\bar{1}$] direction, reached the opposite ($\bar{1}$11) walls but continued to grow in a backwards direction along [$\bar{1}$ 1 $\bar{1}$] and [$\bar{1}$ $\bar{1}$ 1]. The backward growth directions were determined to still be <111> exclusively by

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extensive measurements of the angles and comparison with the nanowires grown on the (110) surface.

[00165] There are three possible backward directions for a given nanowire. Specifically, they are [111], [$\bar{1}$ 1 $\bar{1}$] (nanowire 2), and [$\bar{1}$ $\bar{1}$ 1] (nanowire 3) for a nanowire originally growing along [1 $\bar{1}$ $\bar{1}$] direction. This observation is consistent with the <111> alignment in epitaxy discussed above. The mechanism of backward growth directly indicates that nanowires should self-weld with the opposite sidewall and form solid connections as shown in FIG. 22B. The mechanical rigidity was further confirmed in the nanowire deflection experiments carried out using atomic force microscopy, which will be reported elsewhere. The nanowire-to-substrate connections shown here are different from disk formation reported previously possibly due to different growth conditions such as the precursor molecules and the temperature.

[00166] FIG. 23A - 23C depicts nanowire fabrication in which the diameters (FIG. 23A), lengths (FIG. 23B), and densities (FIG. 23C) of the nanowires are tightly controlled. Control can be achieved, such as for this example, utilizing the Au cluster catalyzed growth process. First, the lengths of nanowires can be tailored to fit in trenches of varying widths by controlling growth time. For instance, FIG. 23A depicts four bridging nanowires with similar diameters (~75 nm) having lengths of 1.5, 2.5, 4 and 10 μm respectively.

[00167] Second, the diameters of nanowires can be defined by the sizes of Au clusters. As shown in FIG. 23B, the diameters of nanowires grown from 100, 50 and 10 nm Au clusters are 140, 70 and 35 nm respectively.

[00168] Finally, the densities of nanowires in trenches can be controlled by the surface densities of Au clusters. In the example shown in FIG. 23C, densities of 1 wire/50 μm, 4 wires/50 μm and 40 wires/50 μm were obtained by using a series of diluted Au colloids. It is worth noting that nanowire diameter is not controlled independently of nanowire density in thin film catalyzed nanowire growth, where a decrease in diameter is always accompanied by a decrease in density. In contrast, in Au cluster-catalyzed growth, diameters and densities can be controlled independently.

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[00169] FIG. 24A - 24B describes testing the current flow capability of bridging nanowires. FIG. 24A depicts Si pads that were created as electrodes to provide the basis for testing the capability to pass a flow of current through the bridging nanowires, in particular applications of nanowire-in-trench structures in nano-scale electronics. In the example shown in FIG. 24A, we demonstrated the electrical connectivity of a simple network consisting of five Si pads connected by bridging nanowires.

[00170] Two tungsten probes were directly placed on top of the pads to perform electrical transport measurement. The results are shown graphically in FIG. 24B. Current-voltage (I-V) curve 1 shows the measurement between the central pad and upper pad with several nanowires in between, indicating current flow through the nanowires. Curve 2 is the I-V measured between the central pad and SiO_2 layer underneath, and curve 3 is from a measurement on a trench with no nanowires bridging. No currents were measured in these cases, consistent with the XPS results, indicating that transport occurred exclusively through nanowire bridges. Furthermore, contact problems existing in the current "fabricating electrodes after growth" approach (e.g., the deterioration of electrode-nanowire interface) are avoided here since the electrodes and nanowires are integrated into one single crystalline piece in the bridge structures. More advanced functions can be realized by further modifications on the prototype devices shown here.

[00171] In conclusion, direct integration of nanowire growth into device fabrication has been demonstrated by bridging Si nanowires in micro-fabricated trenches, which provides both growth and fabrication in a more rational and simple manner toward the creation of nanowire-based integrated circuits. The framework of devices can be pre-defined in top-down fabrication before the growth, and structures of the core units (i.e., the nanowires) can be readily realized using the Au clusters catalyzed $SiCl_4$ CVD synthesis. These new control capabilities make the nanowire-in-trench strategy desirable for various applications, such as chemical sensors, FETs and nanomechanical resonators, and so forth.

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[00172] Experimental.

[00173] *Fabrication of trenches:* (110) SOI wafers used in the study consist of 20 - 80 μm thick Si(110) layer, 0.5-2 μm thick thermally grown SiO_2 layer, and having approximately a 400 μm thick Si(100) handle layer. Thermal SiO_2 film with a thickness of from 0.5 - 1 μm was first grown on a Si(110) surface in H_2O vapor at 1050 °C. Patterns designed for trenches were made on spin-coated photoresist by photolithography and then transferred onto the SiO_2 layer by plasma etching. Using the patterned SiO_2 film as the mask, the deep reactive ion etching (DRIE) process was carried to etch the Si(110) layer to expose vertical {111} planes in an inductively-coupled plasma etcher (Surface Technology Systems). Trenches formed after etching reached the insulating SiO_2 layer of the SOI wafer.

[00174] *Growth of Si nanowires*: The SiO_2 mask was etched in 10% HF in some cases before growth, for studying the epitaxy, or for better imaging, while in some cases, it was etched after growth to remove the nanowires on the top surfaces. For dispersion of Au clusters, a drop of 0.1 wt% poly-L-lysine was first deposited on the surface of the substrate followed by rinsing with DI water and drying by N_2. Then, a drop of Au colloids was dispersed on the substrate also followed by rinsing with DI water and drying by N_2. The synthesis was carried in a horizontal hot-wall furnace at 800-850 °C. $SiCl_4$ was used as a precursor and 10% H_2 in Ar was used as both carrier gas and diluted gas.

[00175] *Characterization*: All the images were taken in a JEOL-6400 field emission scanning electron microscope (SEM). X-ray photoelectron spectra (XPS) were obtained in an ultrahigh vacuum chamber equipped with an Omicron EA125 electron energy analyzer and an Omicron DAR400 X-ray source. Binding energy values were corrected using the C-1s peak as reference.

[00176] Although the description above contains many details, these should not be construed as limiting the scope of the invention but as merely providing illustrations of some of the presently preferred embodiments of this invention. Therefore, it will be appreciated that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled

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in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. No claim element herein is to be construed under the provisions of 35 U.S.C. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

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CLAIMS

What is claimed is:

1. A field effect transistor, comprising:

a nanowire extending from a substrate base;

a dielectric material surrounding at least a portion of said nanowire;

a gate material surrounding at least a portion of said dielectric material;

said nanowire having an exposed tip, which is not covered with said dielectric material or said gate material; and

a drain material coupled to in contact with said exposed tip of said nanowire.

2. A field effect transistor as recited in claim 1, wherein a plurality of said nanowires extending from said substrate base are coupled to said drain material of a single drain contact pad.

3. A field effect transistor as recited in claim 1, wherein said nanowire extends substantially vertically from a horizontal substrate.

4. A field effect transistor as recited in claim 1, wherein said nanowire is grown from said substrate base.

5. A field effect transistor as recited in claim 4, wherein the growth orientation of said nanowire is controlled utilizing epitaxial crystal growth techniques.

6. A field effect transistor as recited in claim 4, wherein said nanowire is grown from Si or SiGe with any desired type and level of dopants.

7. A field effect transistor as recited in claim 1, wherein said nanowire is grown according to a vapor-liquid-solid (VLS) process.

8. A field effect transistor as recited in claim 7, wherein epitaxial crystal growth is used to grow the nanowire according to a vapor-liquid-solid epitaxy (VLSE)

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process.

9. A field effect transistor as recited in claim 7, wherein $SiCl_4$ is utilized as a gas phase precursor, without separately incorporating HCl gas, during growing of said nanowire.

10. A field effect transistor as recited in claim 7, wherein the material or dopant properties may be varied during nanowire growth to form a longitudinally patterned nanowire.

11. A field effect transistor as recited in claim 1, wherein the nanowire diameter is controlled in response to the diameter of an alloy droplet during nanowire growth from the substrate.

12. A field effect transistor as recited in claim 11, wherein a plurality of said alloy droplets are contained within a colloidal metal which is dispersed on the surface of said substrate prior to growth of a plurality of said nanowires.

13. A field effect transistor as recited in claim 12, wherein said colloidal metal comprises gold (Au).

14. A field effect transistor as recited in claim 1, wherein a plurality of said nanowires are grown on said substrate at sites of alloy droplets distributed across at least a portion of the substrate surface as monodispersed metal nanoclusters.

15. A field effect transistor as recited in claim 14:

wherein said substrate is patterned for growing nanowires in a pattern upon selected areas; and

wherein said pattern contains said monodispersed metal nanoclusters selectively disposed on said substrate from which said nanowires are grown.

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16. A field effect transistor as recited in claim 15, wherein said substrate is patterned utilizing micro-contact printing.

17. A field effect transistor as recited in claim 1, wherein said field effect transistor comprises a vertical integrated nanowire field-effect transistor which is configured for integration within an electrical device, circuit or system.

18 A field effect transistor, comprising:

a plurality of nanowires grown from a substrate base;

said nanowires are grown utilizing $SiCl_4$ as a gas phase precursor;

a dielectric material surrounding at least a portion of each of said nanowires;

a gate material surrounding at least a portion of said dielectric material on each of said nanowires;

wherein each of said nanowires has an exposed tip, which is not covered with said dielectric material or said gate material; and

a drain material in contact with said exposed tip of each of said nanowires.

19. A method of fabricating a vertical integrated nanowire field effect transistor, comprising:

growing a nanowire vertically in-place on a substrate;

etching away nanoparticle catalysts;

forming a gate dielectric of a desired thickness;

depositing a gate metal on the nanowire to achieve a conformal coating;

depositing a dielectric onto the substrate;

etching undesired gate metal wherein the nanowire has an uncoated tip;

depositing a dielectric onto the substrate to electrically isolate the gate and drain materials; and

forming a drain pad in contact with said uncoated tip of said nanowire.

20. A method as recited in claim 19, wherein growing of said nanowires comprises:

dispersing metal nanoclusters of a desired diameter over one or more portions

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of the substrate, or within a pattern; and

epitaxially growing said nanowire from Si to a desired length utilizing $SiCl_4$ as a gas phase precursor.

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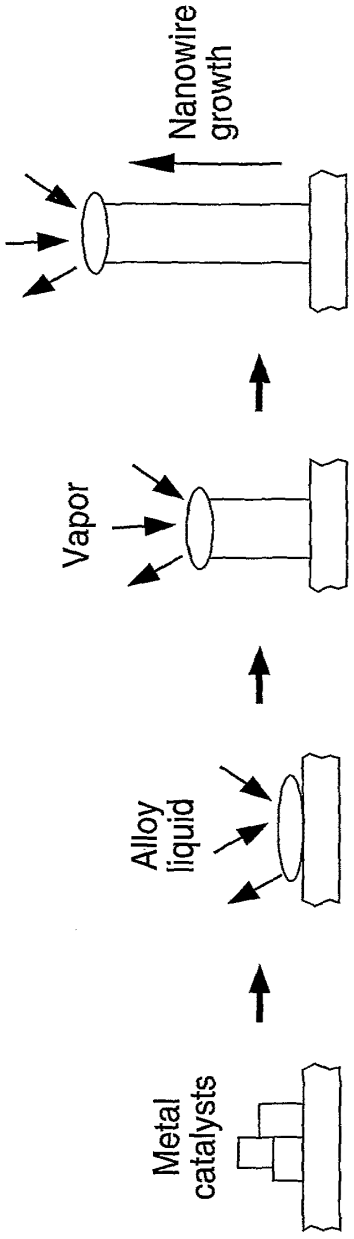


FIG. 1
(Prior Art)

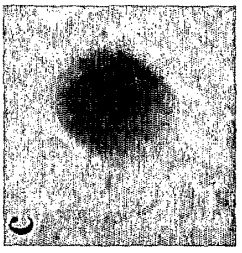


FIG. 2C

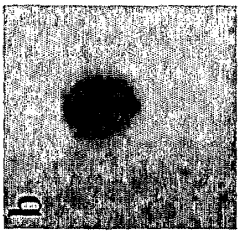


FIG. 2B

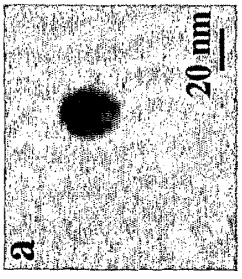


FIG. 2A

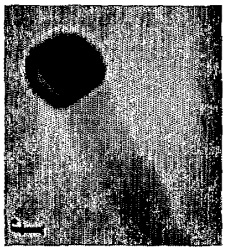


FIG. 2F

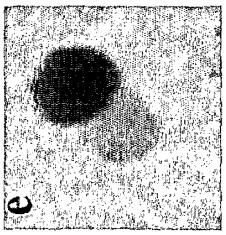


FIG. 2E

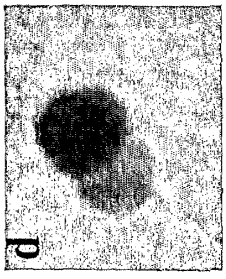


FIG. 2D

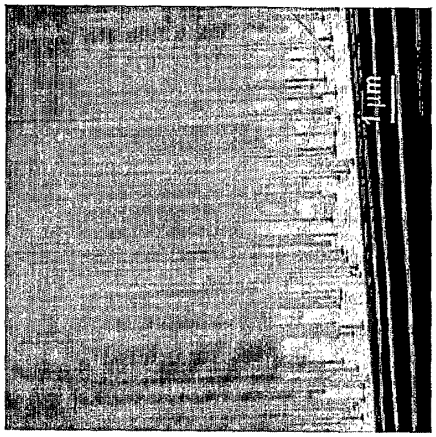


FIG. 3B

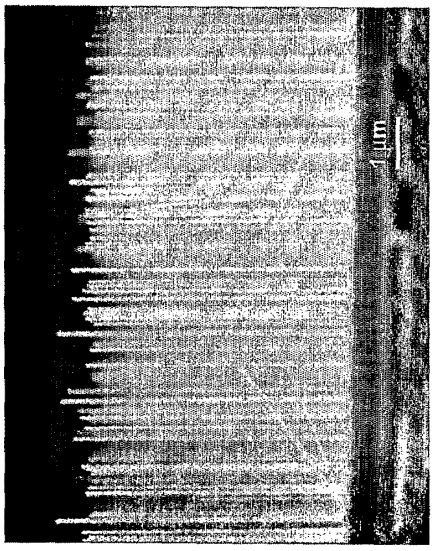


FIG. 3A

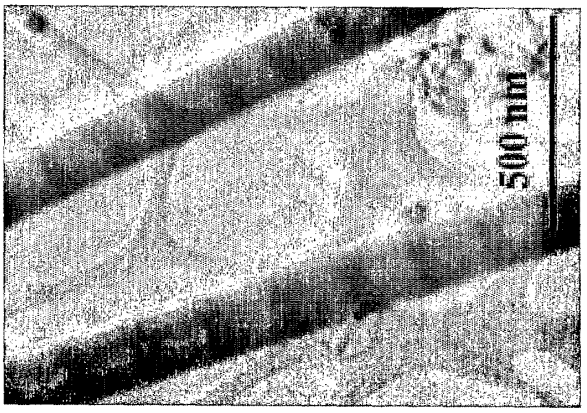


FIG. 4

FIG. 5A

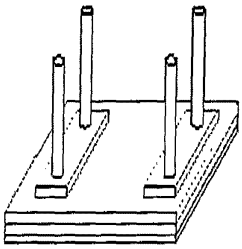


FIG. 5B

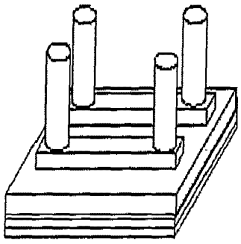


FIG. 5C

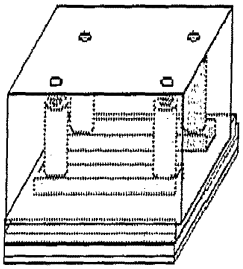
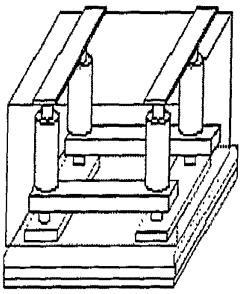


FIG. 5D



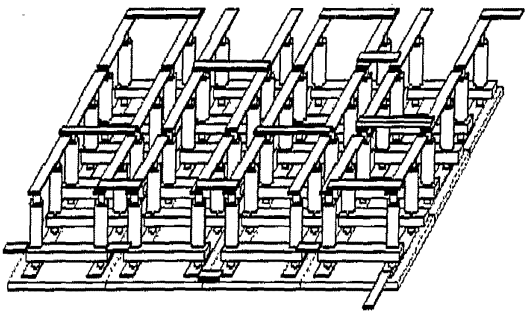


FIG. 5E

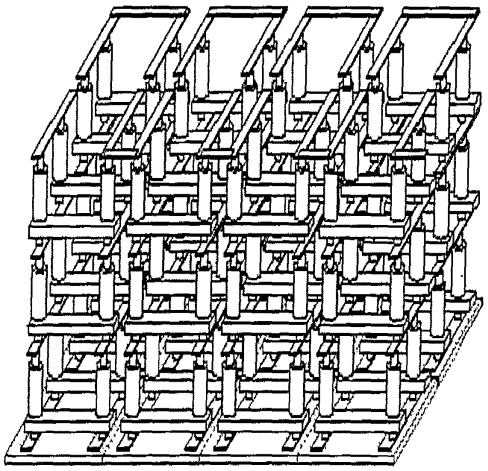
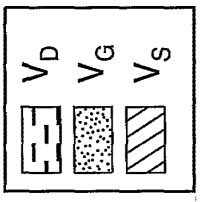


FIG. 5F



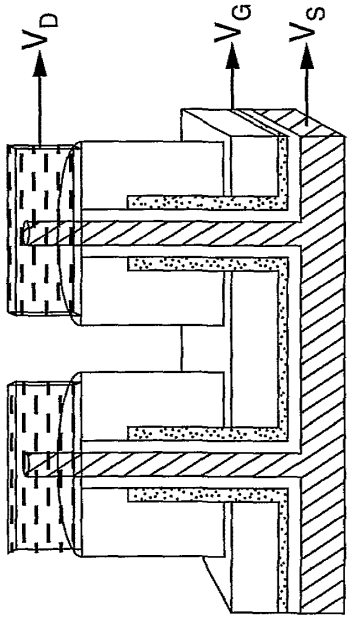


FIG. 6

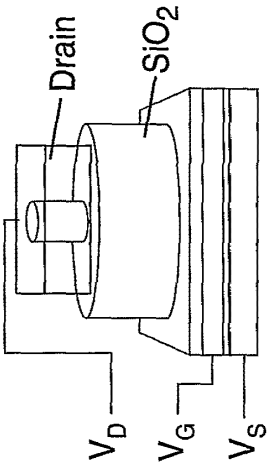


FIG. 7C

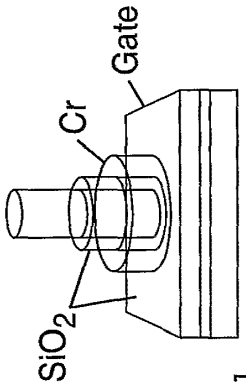


FIG. 7B

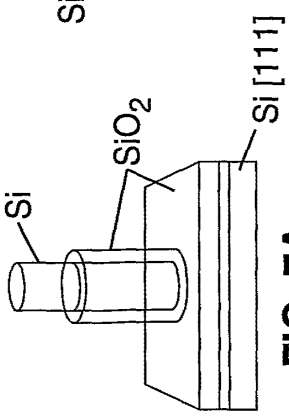


FIG. 7A

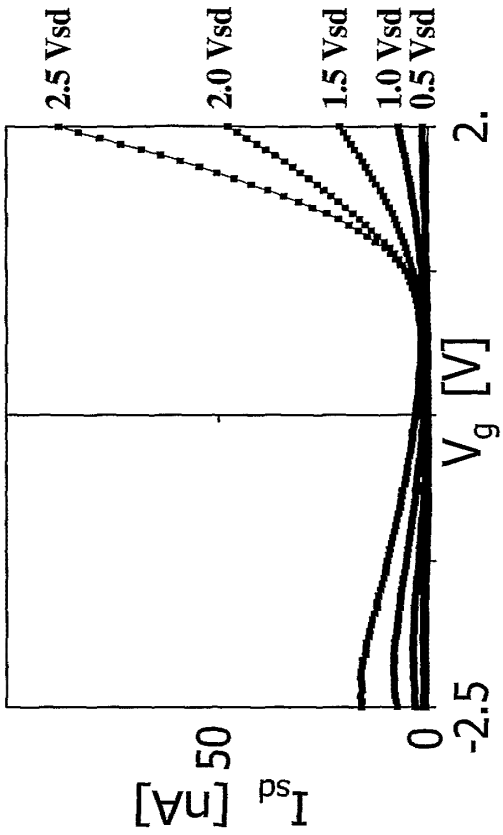


FIG. 8B

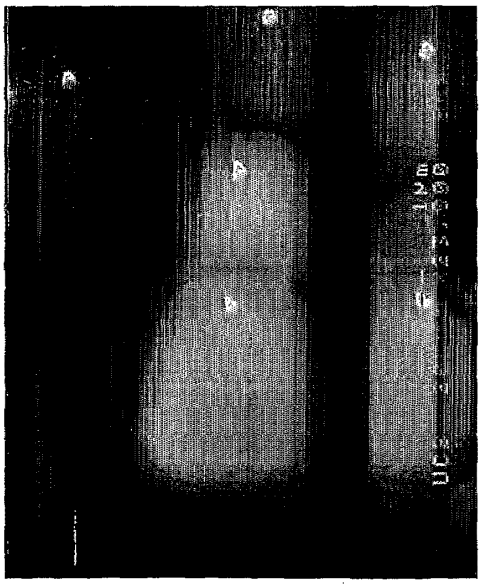


FIG. 8A

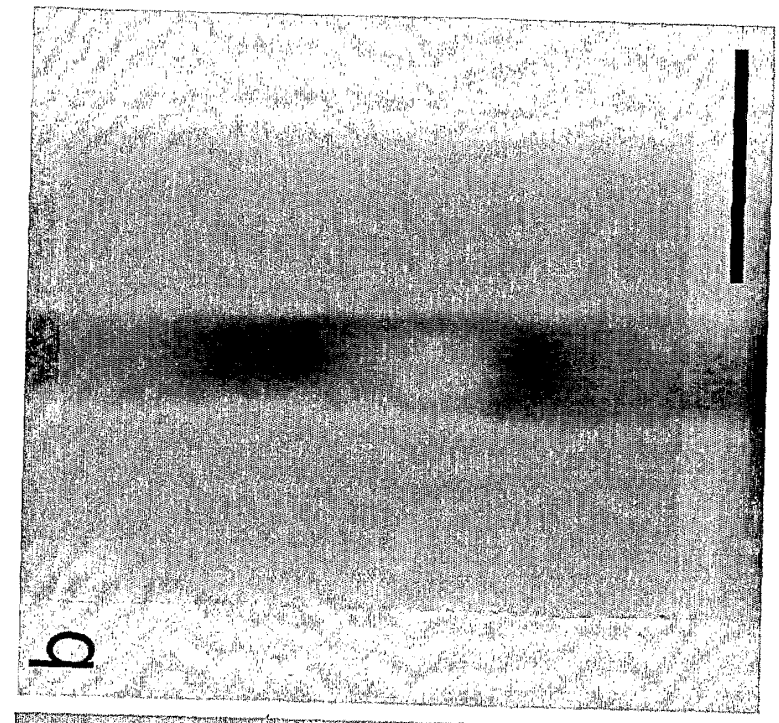


FIG. 9B

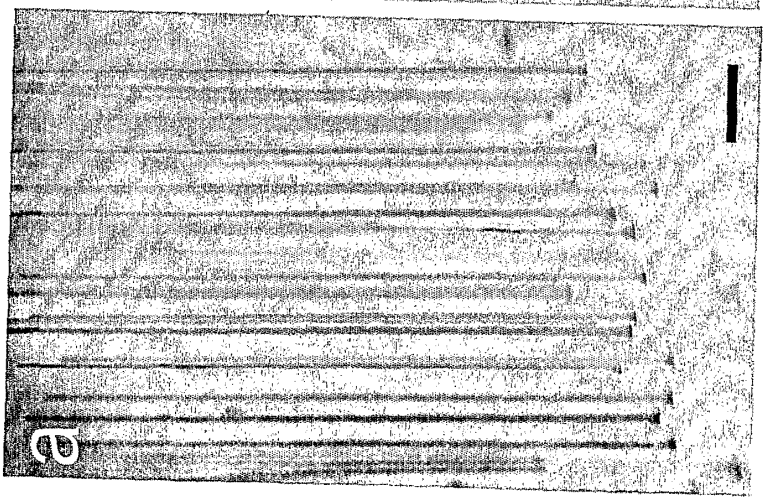


FIG. 9A

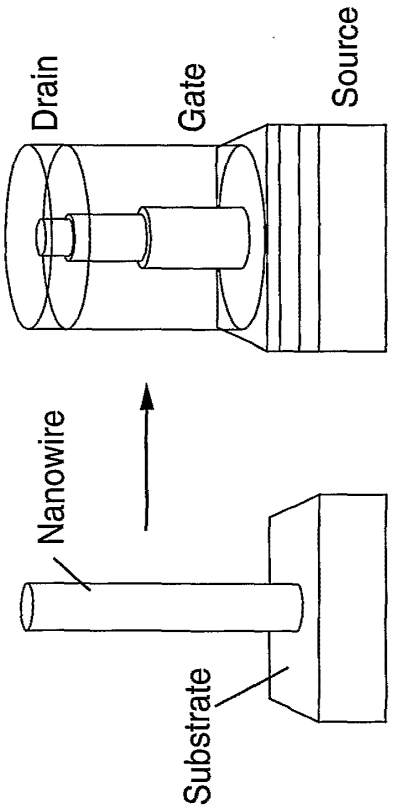


FIG. 10A

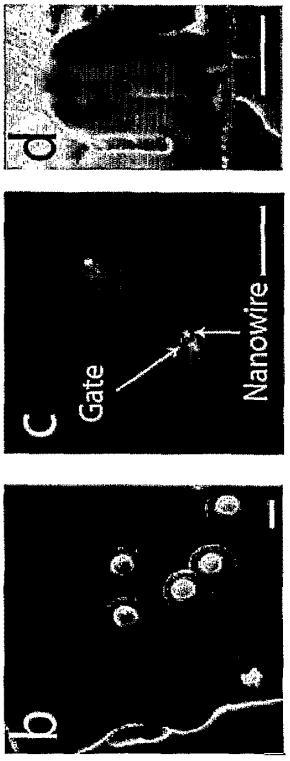


FIG. 10B

FIG. 10C

FIG. 10D

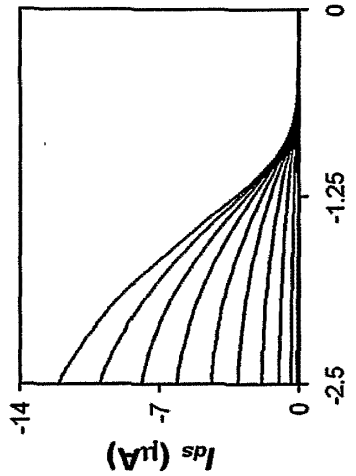


FIG. 11B

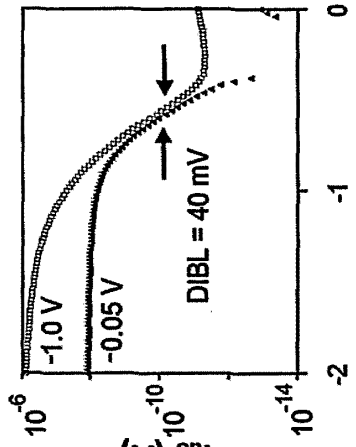


FIG. 11D

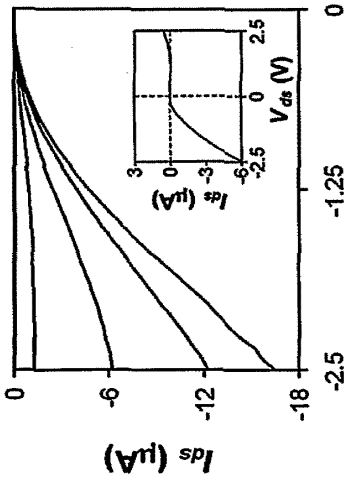


FIG. 11A

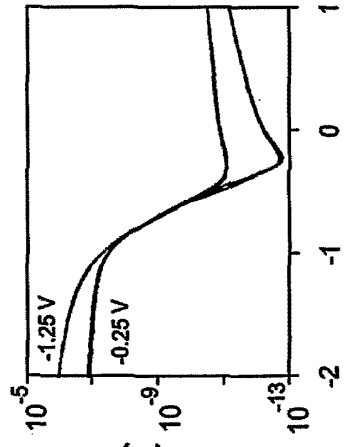


FIG. 11C

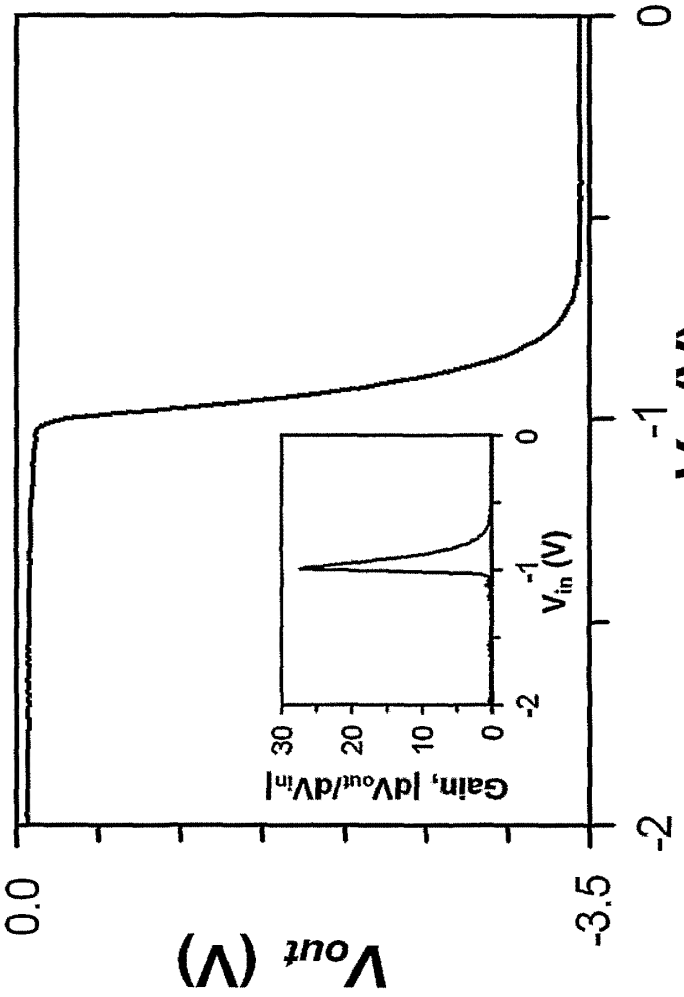


FIG. 12B

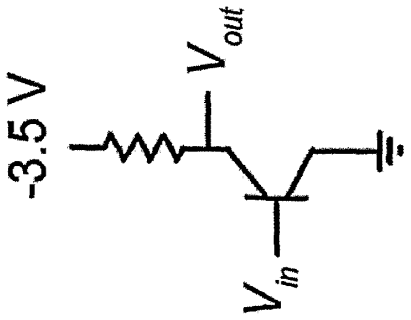


FIG. 12A

FIG. 13A

FIG. 13B

FIG. 13C

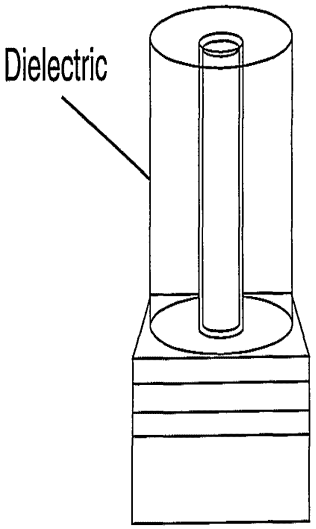


FIG. 14A

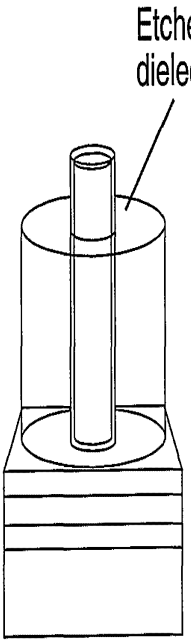


FIG. 14B

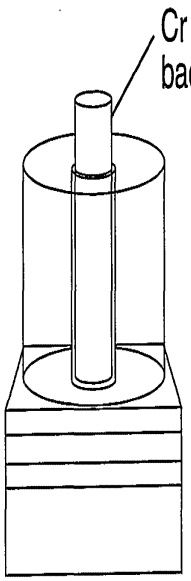


FIG. 14C

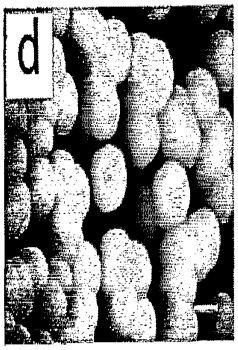


FIG. 14D

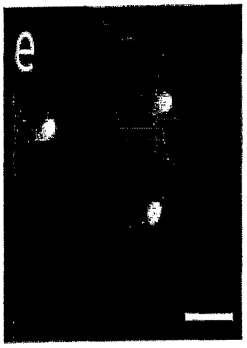


FIG. 14E

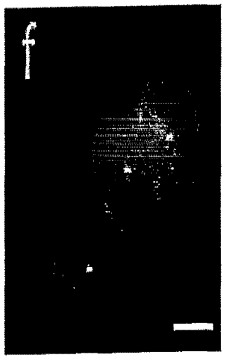


FIG. 14F

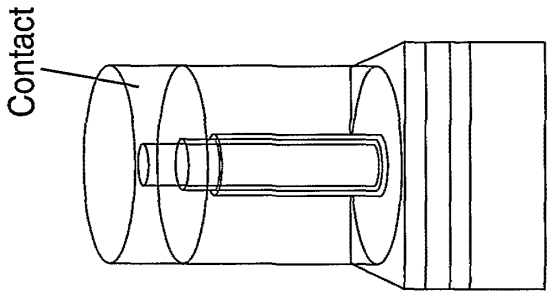


FIG. 15C

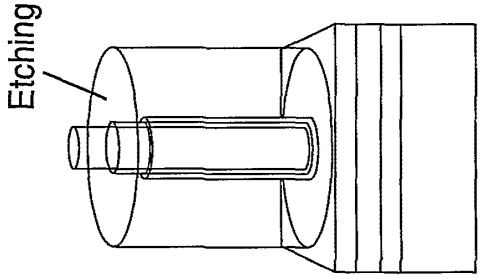


FIG. 15B

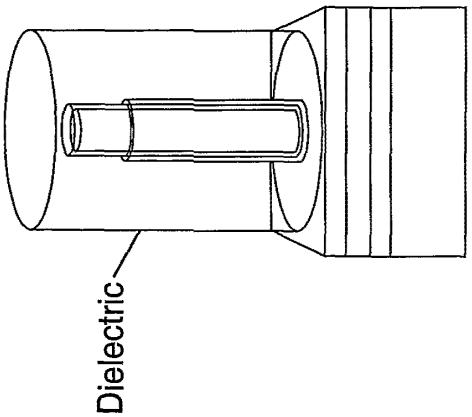


FIG. 15A

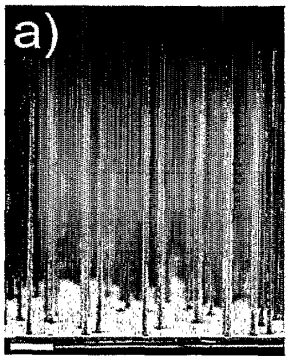


FIG. 16A

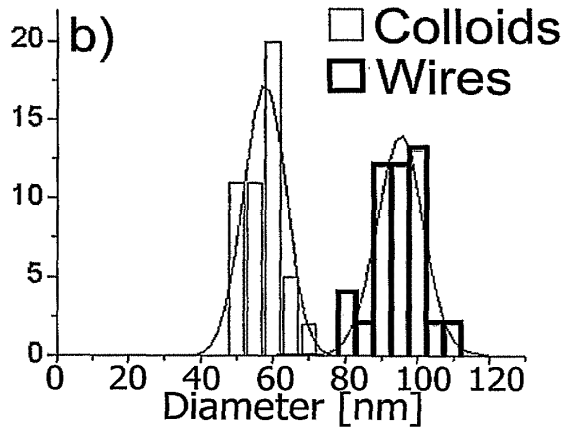


FIG. 16B



FIG. 16C

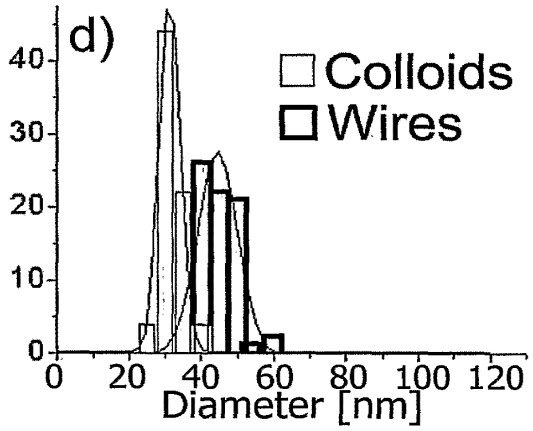


FIG. 16D

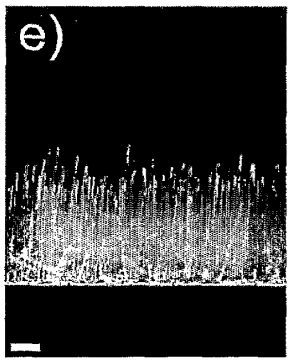


FIG. 16E

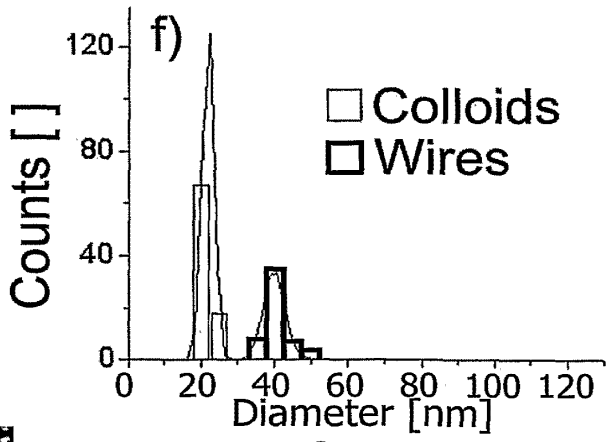


FIG. 16F

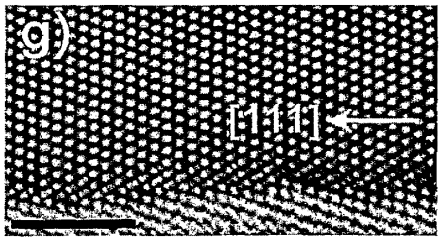


FIG. 16G

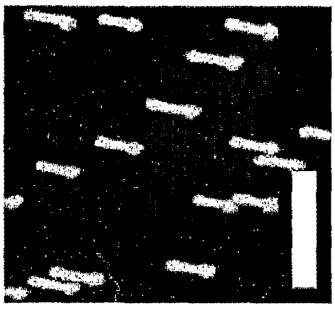


FIG. 17B

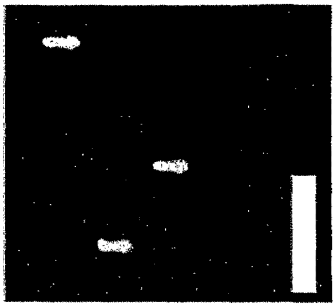


FIG. 17C

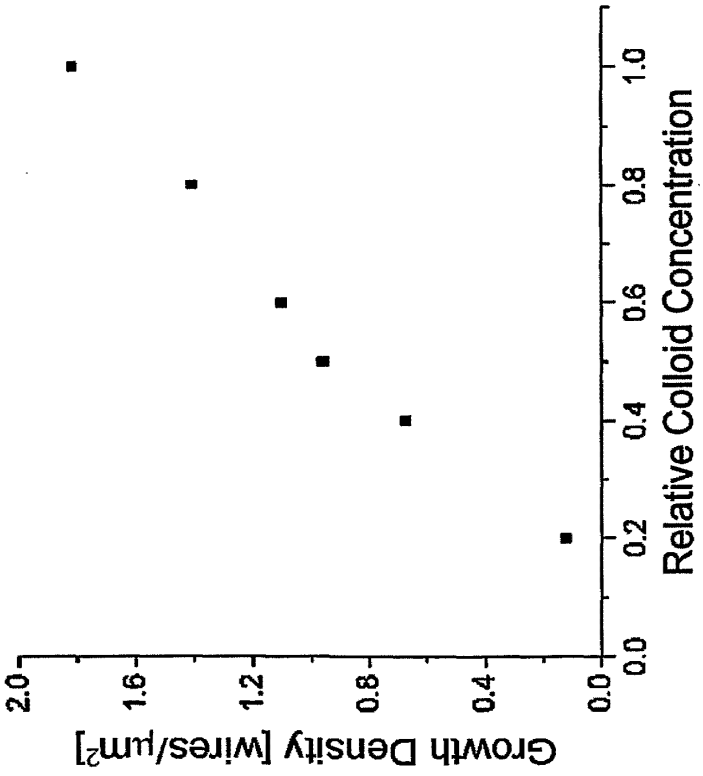


FIG. 17A

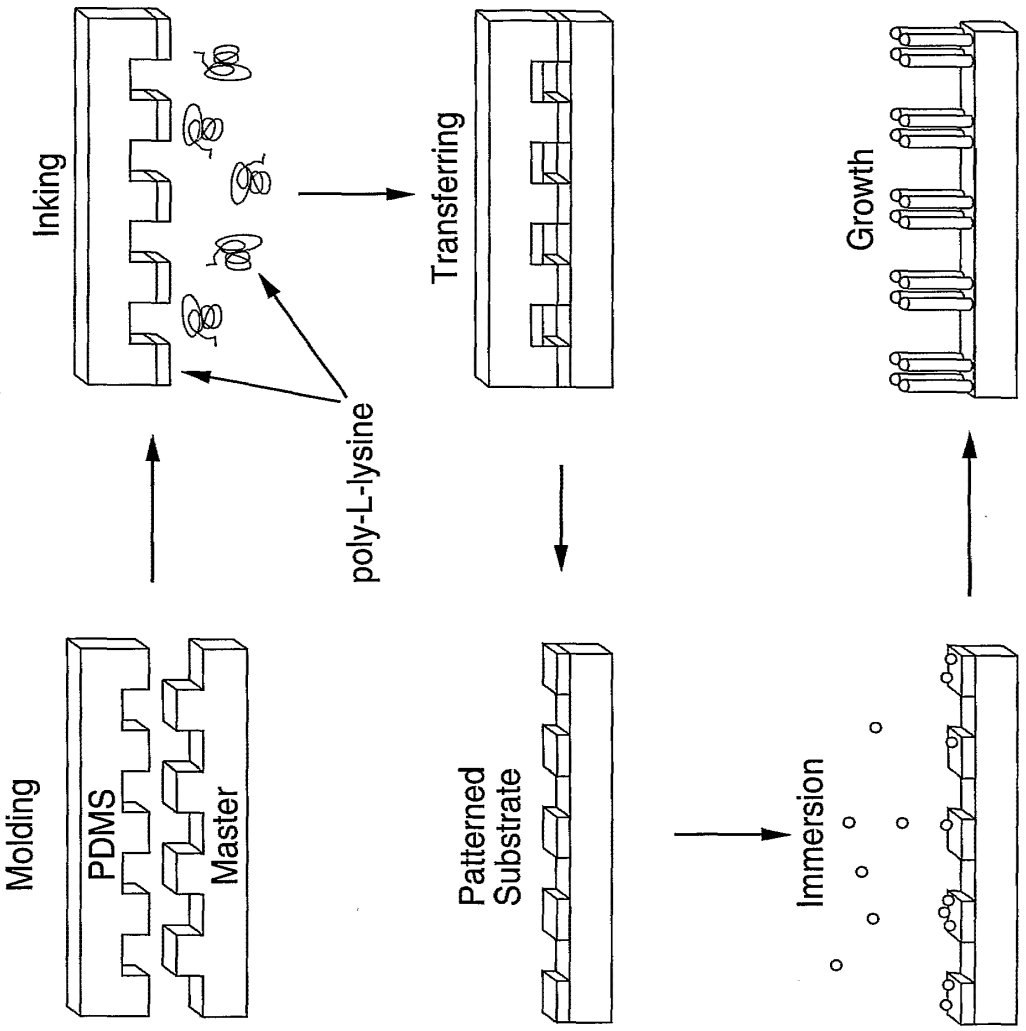

Molding
PDMS
Master
Inking
poly-L-lysine
Patterned
Substrate
Transferring
Immersion
Growth

FIG. 18A

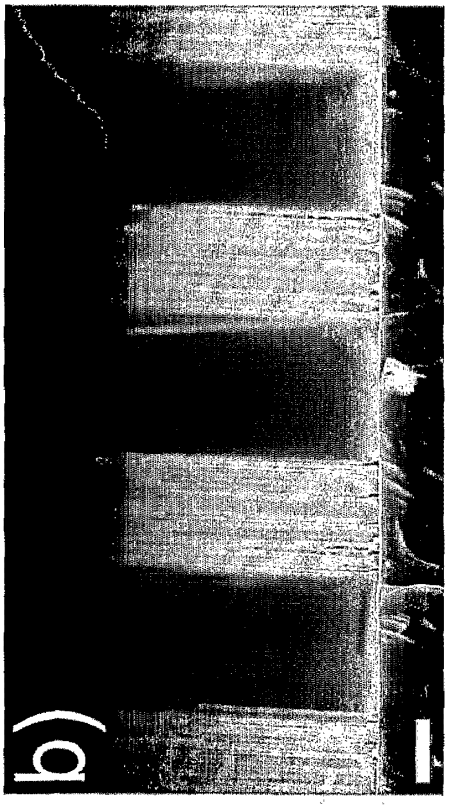


FIG. 18B

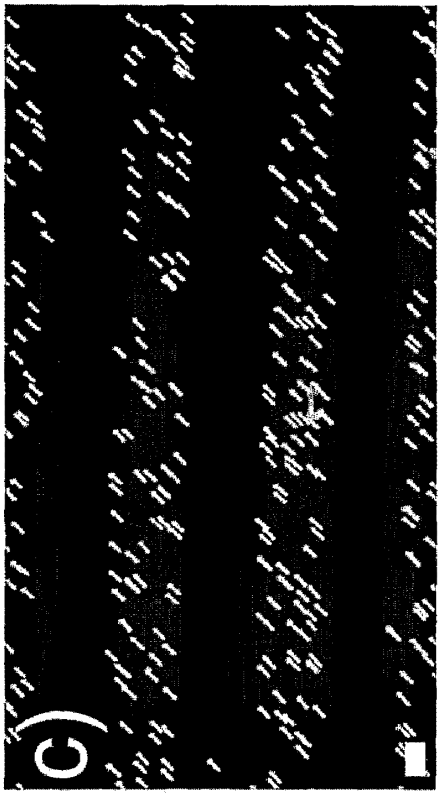


FIG. 18C

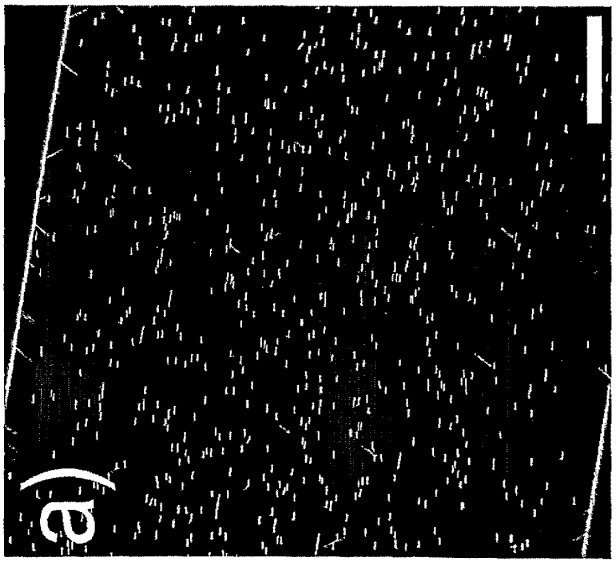


FIG. 19A

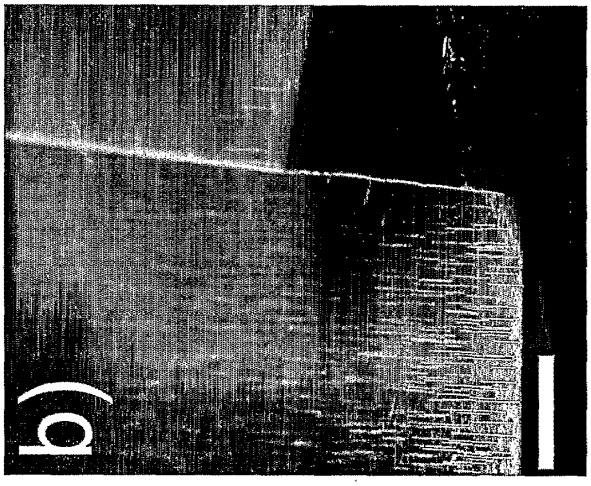


FIG. 19B

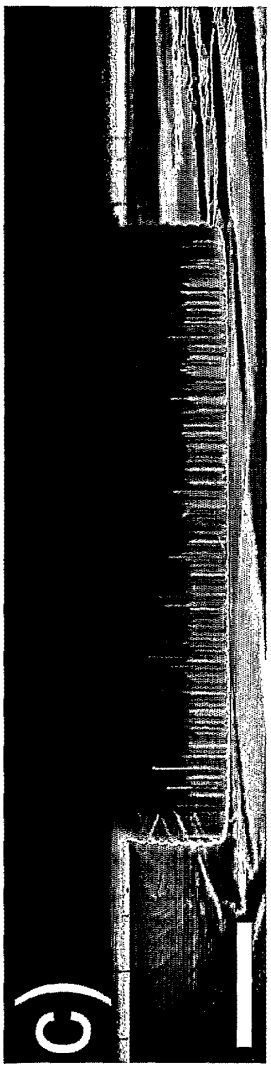


FIG. 19C

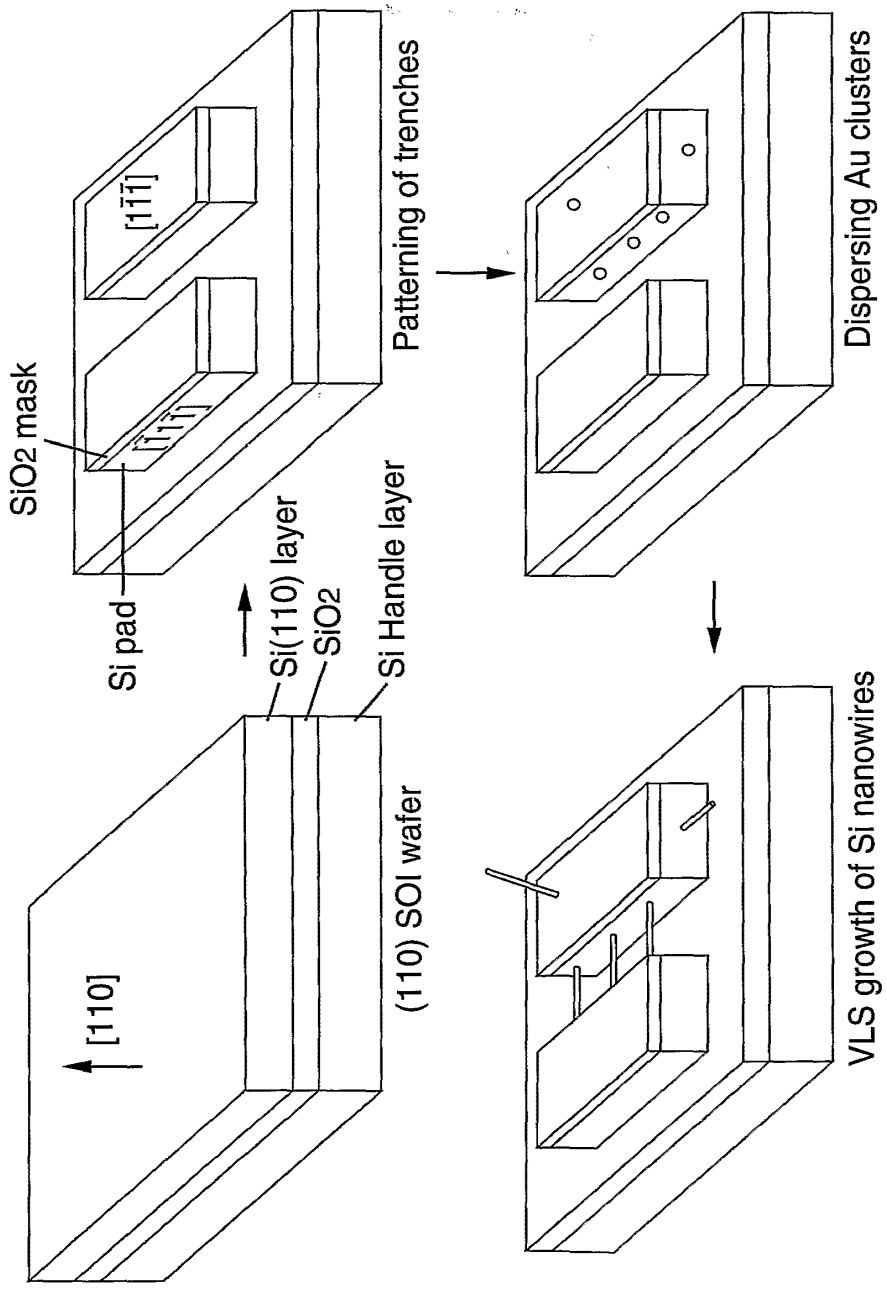

(110) SOI wafer
[110]
Si Handle layer
SiO2
Si(110) layer
Si pad
SiO2 mask
[1$\bar{1}$1]
[11$\bar{1}$]
Patterning of trenches
Dispersing Au clusters
VLS growth of Si nanowires

FIG. 20A

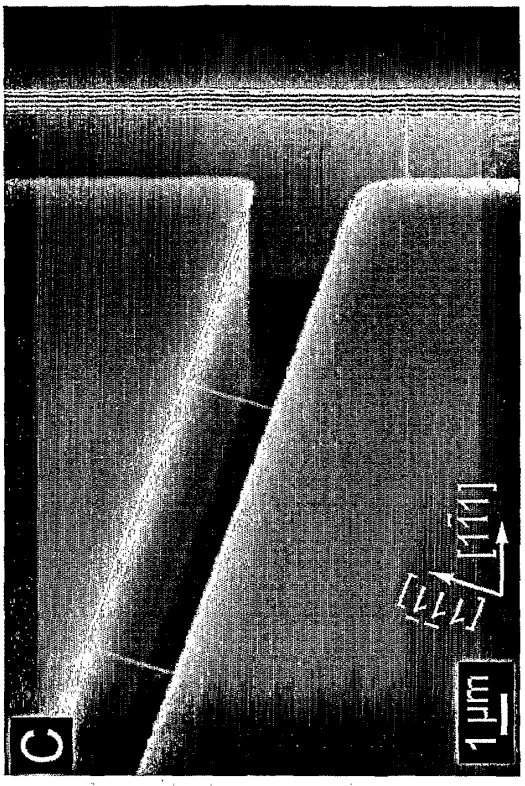


FIG. 20C

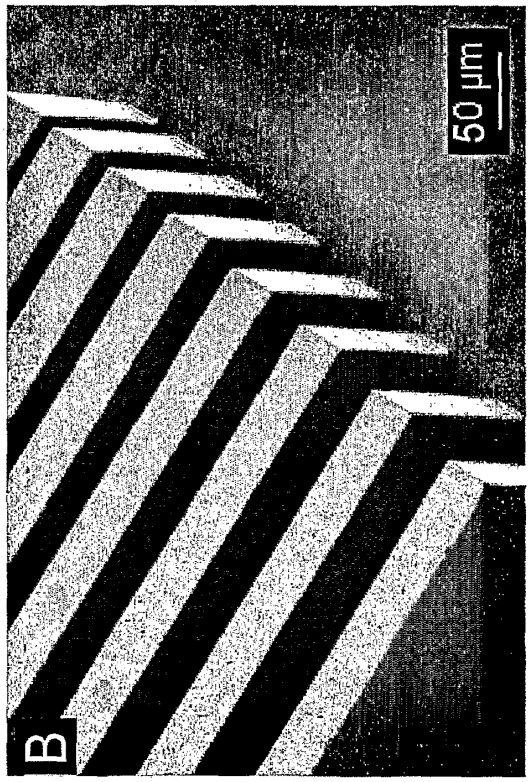


FIG. 20B

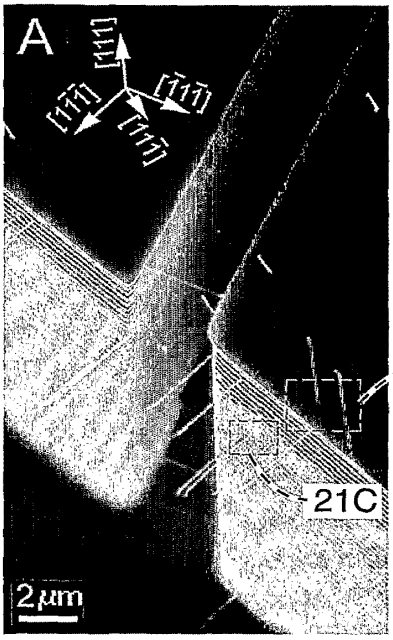


FIG. 21A

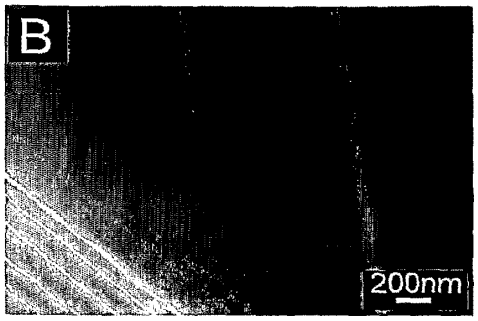


FIG. 21B

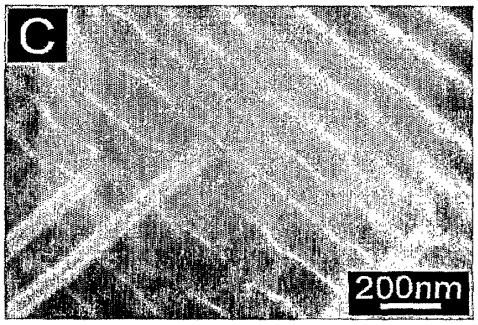


FIG. 21C

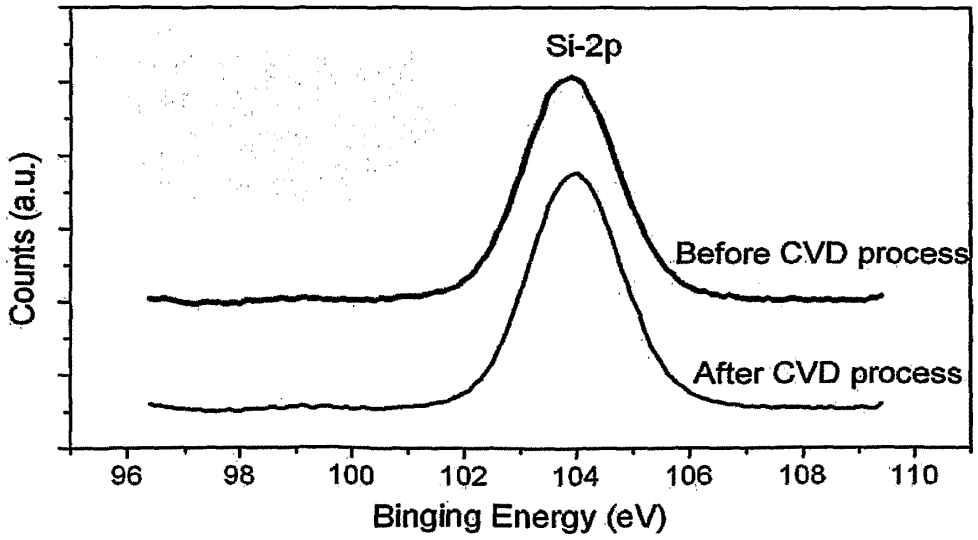


FIG. 21D

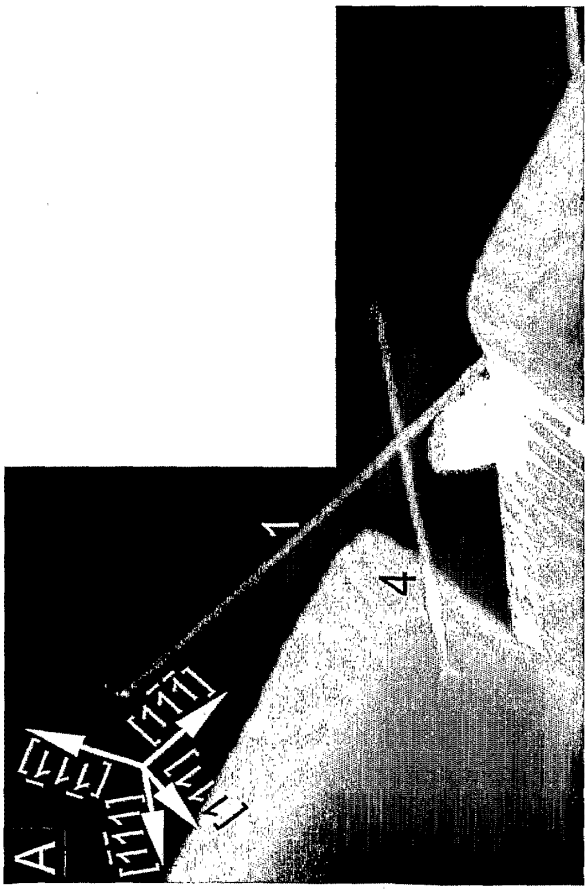


FIG. 22A

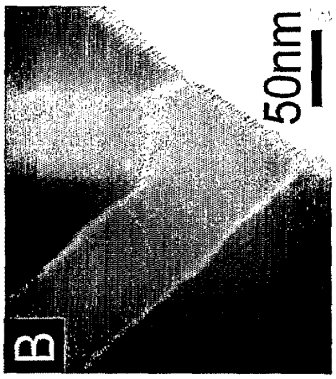


FIG. 22B

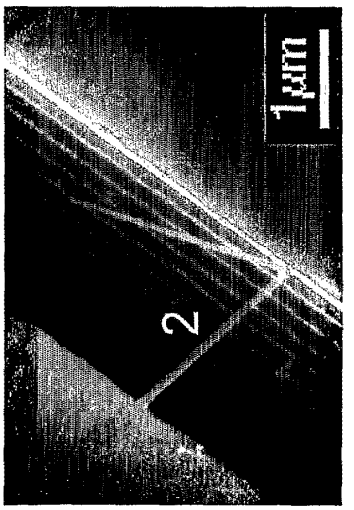


FIG. 22C

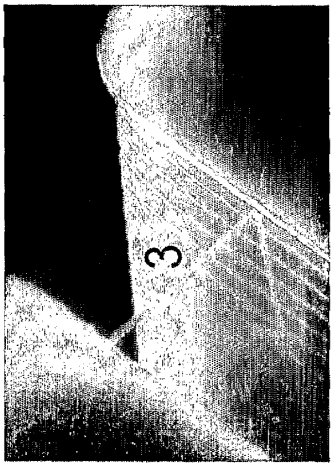


FIG. 22D

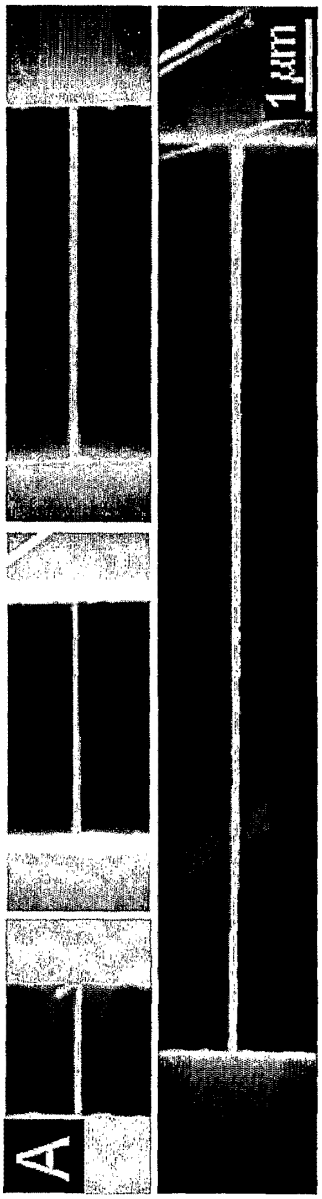


FIG. 23A

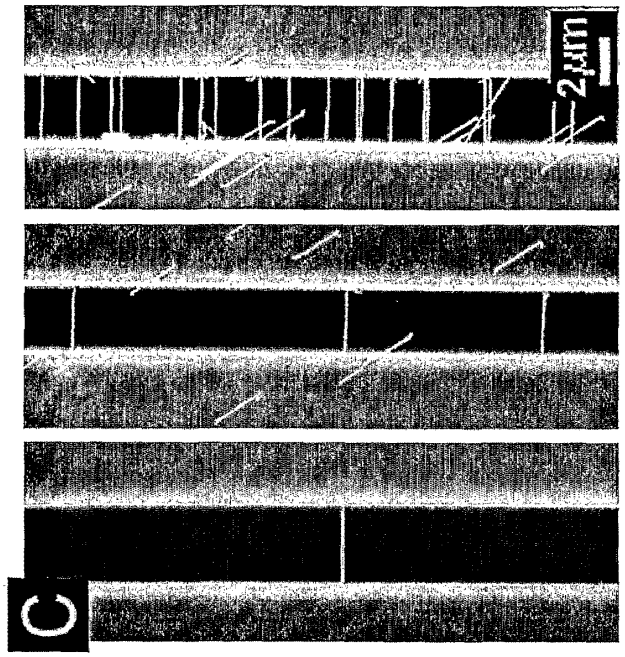


FIG. 23C

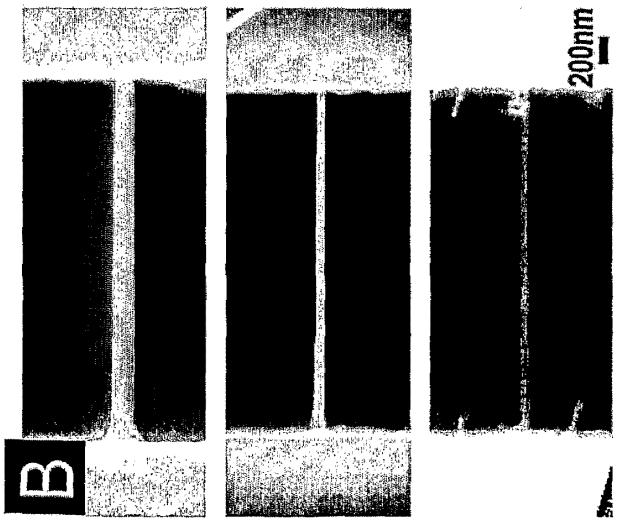


FIG. 23B

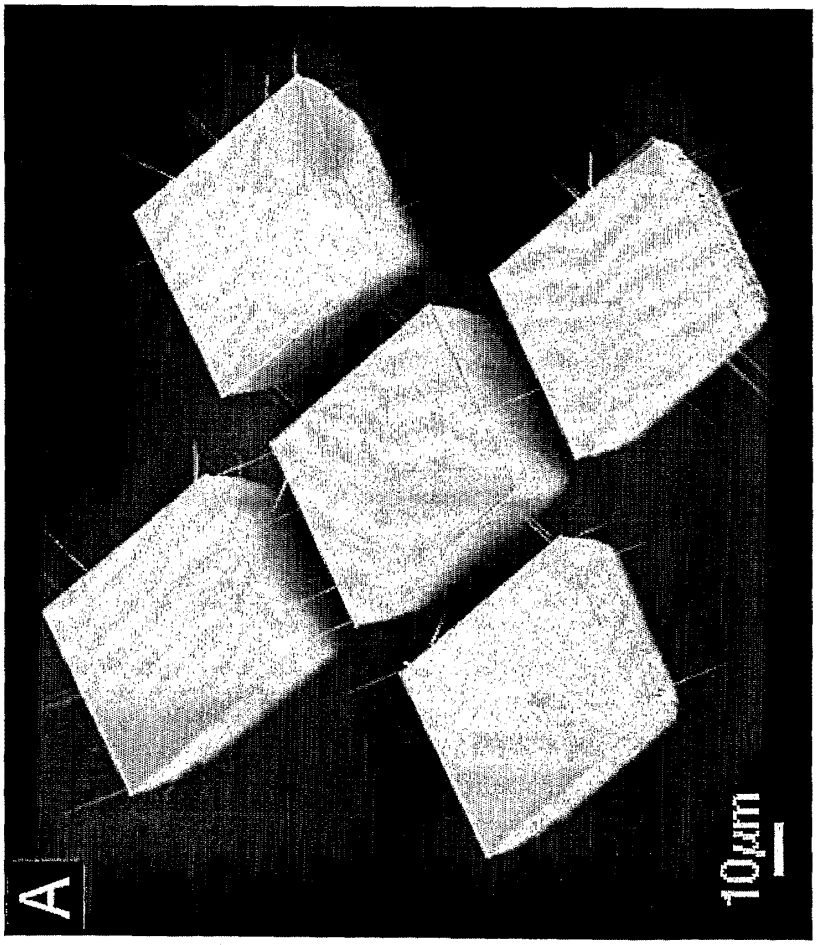


FIG. 24A

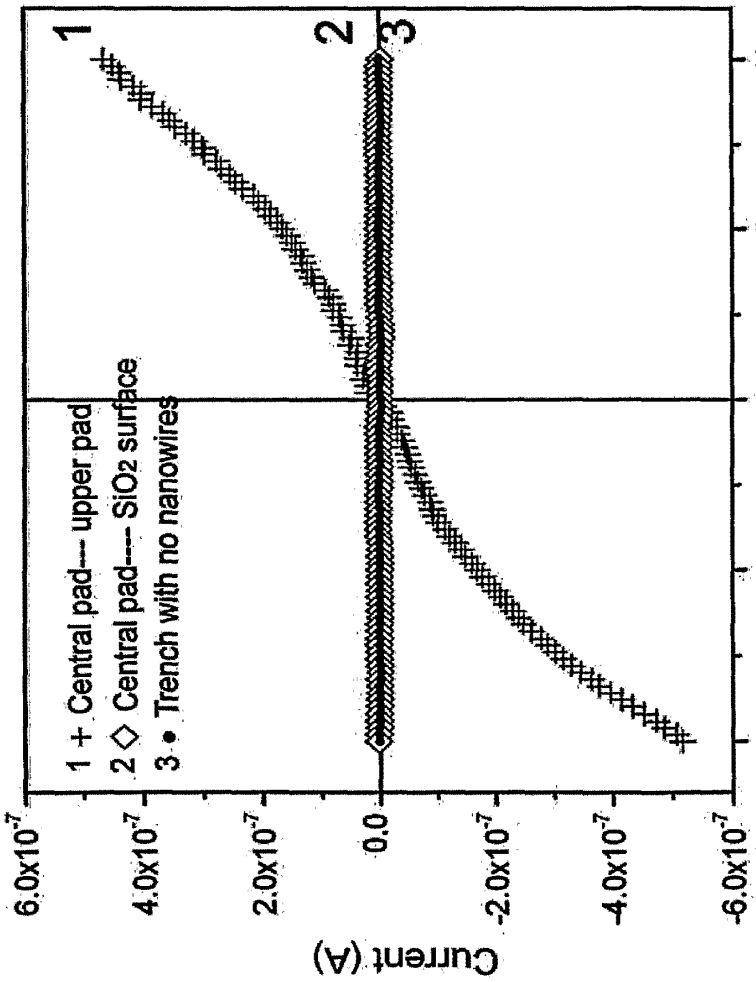

1
2
3
1 + Central pad–– upper pad
2 ◇ Central pad––– SiO2 surface
3 • Trench with no nanowires
6.0x10-7
4.0x10-7
2.0x10-7
0.0
-2.0x10-7
-4.0x10-7
-6.0x10-7
Current (A)
10
5
0
-5
-10
Voltage (V)

FIG. 24B

Espacenet

TW200847343A SONOS ONO stack scaling

Applicants: CYPRESS SEMICONDUCTOR CORP [US]

Inventors: JENNE FREDRICK B [US],LEVY SAGY [IL]

Classifications:
IPC ***H01L21/8247; H01L27/115;***

CPC **H01L21/3143 (EP,US); H01L29/40117 (EP,US); H01L29/4234 (US); H01L29/4916 (US); H01L29/512 (US); H01L29/513 (EP,US); H01L29/518 (US); H01L29/792 (EP,US);**

Priorities: US90450607A 2007-09-26; US94038407P 2007-05-25

Application: TW200847343A·2007-09-29

Publication: TW200847343A·2008-12-01

Published as: **CN101517714A; CN101517714B**; TW200847343A;**TWI436455B; US2008290400A1; US2009032863A1; US8614124B2; US8637921B2; US9349877B1; WO2008147386A1**

SONOS ONO stack scaling

Abstract

Scaling a nonvolatile trapped-charge memory device and the article made thereby. In an embodiment, scaling includes multiple oxidation and nitridation operations to provide a tunneling layer with a dielectric constant higher than that of a pure silicon dioxide tunneling layer but with a fewer hydrogen and nitrogen traps than a tunneling layer having nitrogen at the substrate interface. In an embodiment, scaling includes forming a charge trapping layer with a non-homogenous oxynitride stoichiometry. In one embodiment the charge trapping layer includes a silicon-rich, oxygen-rich layer and a silicon-rich, oxygen-lean oxynitride layer on the silicon-rich, oxygen-rich layer. In an embodiment, the method for scaling includes a dilute wet oxidation to densify a deposited blocking oxide and to oxidize a portion of the silicon-rich, oxygen-lean oxynitride layer.

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200847343

發明專利說明書

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

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※ 申請日期：96.7.20

※IPC 分類：H01L 21/8247 (2006.01)
H01L 27/115 (2006.01)

一、發明名稱：（中文/英文）

半導體-氧化物-氮化物-氧化物-半導體（SONOS）氧化物-氮化物-氧化物（ONO）堆疊縮放

SONOS ONO STACK SCALING

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姓名或名稱：（中文/英文）

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CYPRESS SEMICONDUCTOR CORPORATION

代表人：（中文/英文）

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LEVY, SAGY

國　籍：（中文/英文）

1. 美國　U.S.A.

2. 以色列 ISRAEL

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四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：　年　月　日。

☑ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☑ 有主張專利法第二十七條第一項國際優先權：

1. 美國；2007年05月25日；60/940,384

2. 美國；2007年09月26日；11/904,506

☐ 無主張專利法第二十七條第一項國際優先權：

1.

2.

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號　順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料　【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料　【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

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九、發明說明：

【發明所屬之技術領域】

本發明之實施例係關於電子學製造工業，且更特定言之係關於非揮發性捕獲電荷記憶體元件之製造。

【先前技術】

圖1為具有一半導體-氧化物-氮化物-氧化物-半導體(SONOS)閘極堆疊102之半導體元件100的中間結構之部分橫截面圖，該閘極堆疊102包括一根據習知方法形成於一半導體基板108之一表面106之上的習知氧化物-氮化物-氧化物(ONO)堆疊104。元件100通常進一步包括一或多個與閘極堆疊對準且由一通道區域112分隔之擴散區域110(諸如源極區域及汲極區域)。SONOS閘極堆疊102包括一形成於ONO堆疊104之上且與其接觸之多晶矽(poly-silicon/poly)閘極層114。多晶矽閘極114由ONO堆疊104與基板108分隔或電性隔離。ONO堆疊104通常包括一二氧化矽穿隧層116，一充當元件100之一電荷儲存或記憶層之氮化矽電荷捕獲層118，及一覆於電荷捕獲層118上之二氧化矽阻擋層120。

此等SONOS型電晶體適用於非揮發性記憶體(NVM)。電荷捕獲層儲存電荷以提供非揮發性。為程式化(亦即寫入)N型通道SONOS型元件，在源極、主體及汲極接地的同時向控制閘極施加正電壓(V_{CG})。圖2中描繪具有一通道212、氧化物穿隧層216、氮化物記憶層218及氧化物阻擋層220之習知n型通道SONOS元件在程式化期間之能帶圖、

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捕獲電荷分布及陷阱密度分布。如圖所示，正V_{CG}產生跨過SONOS堆疊之場，從而使得矽基板通道之內埋通道中一些處於導電帶能階之負電荷經歷Fowler-Nordheim穿隧穿過穿隧層(FNT)且進入電荷捕獲層。電子儲存在電荷捕獲氮化物中之具有中間能隙能階之陷阱中。如圖所說明，整個電荷捕獲層中之陷阱密度分布係大體上均勻的。如圖進一步展示，在偏壓下捕獲電荷分布為大多數捕獲電荷在電荷捕獲層(亦即記憶層)鄰近阻擋氧化物之部分中之情形。為擦除n型通道SONOS元件，向控制閘極314施加一負電壓。圖3中描繪一展示在擦除期間通道312、氧化物穿隧層316、氮化物記憶層318及氧化物阻擋層320之能帶圖。如圖所示，負V_{CG}產生跨過SONOS堆疊之場，從而吸引電洞穿隧電荷穿過穿隧層且進入電荷捕獲層。

SONOS型元件在高密度記憶體應用(諸如嵌入式NVM)中愈來愈受歡迎。工業中已知用於程式化及擦除之均勻通道Fowler-Nordheim穿隧(FNT)及/或直接穿隧(DT)產生優於其他方法之改良可靠性。此處提及FNT與DT之組合且該組合係稱作改良Fowler-Nordheim穿隧(MFNT)。目前，習知SONOS在10 V範圍內操作以達成MFNT。然而，SONOS優於其他NVM元件之優勢為電壓可縮放性。已建立理論，藉由適當縮放，SONOS中存在達成可在5伏特(V)範圍(而非習知SONOS型元件之10 V範圍或習知快閃技術之12 V至15 V範圍)中操作之記憶體技術的潛力。可在低電壓下(接近5 V)操作之SONOS型元件有利地與低電壓CMOS相容。或者，

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在經縮放之元件之特定電壓下，更快之程式化或擦除可為可能的。然而，成功縮放SONOS型元件並非無關緊要的。舉例而言，圖4描繪採用一包含一10 nm厚之二氧化矽阻擋層、一7 nm厚之氮化矽電荷捕獲層及一3 nm厚之二氧化矽穿隧層的習知ONO堆疊之習知SONOS元件的程式化時間及擦除時間。如圖所示，程式化/擦除時間在按比例降低V_{CG}時顯著增加。大體而言，短於1 ms之程式化/擦除時間合乎嵌入式記憶體應用之需要。然而，僅由+/-10 V之V_{CG}可達成習知SONOS堆疊中之此等1毫秒(ms)程式化/擦除時間。當V_{CG}降低至大約+/-9 V時習知SONOS程式化/擦除時間延長至100 ms或更久。

另外，降低程式化電壓使擦除視窗或程式化視窗(亦即記憶視窗)縮小。此係因為若在電壓降低時不按比例減小整個ONO堆疊之等效氧化物厚度(EOT)，則跨過ONO堆疊之電場降低。因為減小穿隧層厚度以允許較低外加電壓(V_{CG})下相同之擦除位準可導致擦除及程式化衰變率有害增加，故減小堆疊之EOT並非無關緊要的。類似地，若減小電荷捕獲層之厚度，則電荷重心置放於更接近基板處，從而增加向基板之電荷損失。最終，當按比例減小阻擋氧化物厚度時，電子自控制閘極之反向注入增加，從而引起對ONO堆疊之損壞及資料保存能力之損失。如圖4中進一步展示，反向注入在FNT擦除達到"飽和"之情況下顯現。此在電子以相較於其經由跨過穿隧氧化物之電洞傳輸移除更快之速度自閘極回流至記憶層時發生。因此，仍存在以

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能夠提供可在較低程式化/擦除電壓下操作之元件的方式縮放SONOS元件之ONO堆疊的需要。

【發明內容】

本文參看圖描述縮放非揮發性捕獲電荷記憶體元件之實施例。然而，特定實施例可在沒有此等特定細節中之一或多者之情況下，或與其他已知方法、材料及裝置組合來實踐。在以下描述中，陳述諸如特定材料、尺寸及製程參數等之許多特定細節以提供對本發明之全面理解。在其他情況下，熟知之半導體設計及製造技術未加以詳細描述以免不必要地混淆本發明之實施例。貫穿本說明書所提及之"一實施例"意謂所述與該實施例有關之特定特徵、結構、材料或特性包括於本發明之至少一個實施例中。因此，貫穿本說明書多處出現之片語"在一實施例中"並不一定指本發明之同一個實施例。另外，特定特徵、結構、材料或特性可以任何適宜方式組合於一或多個實施例中。

本發明之某些實施例包括一經縮放之SONOS型元件。在本發明之特定實施例中，改變穿隧層、電荷捕獲層及阻擋層以縮放SONOS型元件。在特定實施例中，經縮放之SONOS元件可在低於+/-10 V之程式化電壓及擦除電壓下操作。在某些此類實施例中，經縮放之SONOS元件係在-5 V與-9 V之間(且較佳在-5 V與-7 V之間)的擦除電壓下操作，以在該元件在攝氏-40度至攝氏95度(℃)之間的溫度下操作時在1 ms至10 ms脈衝之後提供-1 V至-3 V(且較佳-2 V至-3 V)之初始擦除電壓臨限值位準(VTE)。在其他特定實施例中

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SONOS型元件係在5 V與9 V之間(且較佳在5 V與7 V之間)的程式化電壓下操作，以在1 ms至10 ms(較佳5 ms)之程式化脈衝之後提供1 V至3 V(較佳2 V至3 V)之初始程式化電壓臨限值位準(VTP)。此等例示性經縮放之SONOS元件在85℃下操作20年且至少10,000個寫入/擦除循環(較佳100,000個循環)之後提供在1 V與2 V之間的使用壽命終結(EOL)記憶體視窗。

在某些實施例中，以具有特定氮濃度分布之經氮化之氧化物替代習知純氧(氧化物)穿隧層，從而減小該穿隧層相對於純氧穿隧層之等效氧化物厚度同時保持低介面陷阱密度。此允許降低(縮放)程式化/擦除電壓同時提供與習知未經縮放之元件同等良好或更佳之擦除電壓臨限值位準(VTP/VTE)。在特定之其他實施例中，以具有化學計量不同之至少一個頂層及底層之多層氮氧化物薄膜替代習知氮化物電荷捕獲層。在一此類實施例中，多層氮氧化物包括一富矽、貧氧之頂層用以定位且限制電荷之重心使其遠離穿隧氧化物層，由此局部增加電荷捕獲層內之陷阱密度。在特定之其他實施例中，以經再氧化之阻擋層替代習知高溫氧化物(HTO)阻擋層，從而增密阻擋氧化物且由此藉由縮放減小記憶體衰變率。此等實施例為適當記憶體視窗提供足夠淨電荷同時亦減少陷阱輔助之穿隧，從而當SONOS元件在降低之程式化/擦除電壓下操作時改良或維持程式化臨限電壓及擦除臨限電壓(VTP/VTE)。

如本文所使用之術語"在.....之上"、"在.....之下"、"介

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於……之間"及"在……上面"係指一層相對於其他層之相對位置。因此，舉例而言，一沈積或安置於另一層之上或之下之層可直接與該另一層接觸或具有一或多個介入層。此外，一沈積或安置於層之間的層可直接與該等層接觸或可具有一或多個介入層。對比而言，一在一第二層"上面"之第一層係與該第二層接觸。另外，提供一層相對於其他層之相對位置，以便在不考慮基板之絕對方位之情況下採取相對於一起始基板之沈積、修改及移除薄膜之操作。

根據本發明之一實施例，非揮發性捕獲電荷記憶體元件為SONOS型元件，其中電荷捕獲層為諸如氮化物之絕緣體層。在另一實施例中，非揮發性捕獲電荷記憶體元件為快閃型元件，其中電荷捕獲層為導體層或諸如多晶矽之半導體層。採用經氮化之氧化物穿隧層之非揮發性捕獲電荷記憶體元件可允許較低程式化或擦除電壓同時提供與習知元件同等良好或更佳之擦除電壓臨限值位準(VTP/VTE)。

【實施方式】

圖5說明具有根據本發明之一實施例之經縮放的ONO堆疊之SONOS型元件500的中間結構之橫截面側視圖。應瞭解除圖5中描繪之特定實施例以外亦可採用本文中所揭示之多個其他SONOS實施例來製造經縮放之ONO堆疊，但該等SONOS實施例仍然亦可在降低之程式化/擦除電壓下操作。因此，儘管可在整個描述中參考圖5之特徵，但本發明並不限於此特定實施例。

在圖5中展示之特定實施例中，SONOS型元件500包括一

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SONOS閘極堆疊502，閘極堆疊502包括一形成於基板508之表面506之上的ONO堆疊504。SONOS型元件500進一步包括一或多個與閘極堆疊502對準且由一通道區域512分隔之源極及汲極區域510。大體而言，經縮放之SONOS閘極堆疊502包括一形成於經縮放之ONO堆疊504及基板508之一部分之上且與其接觸之閘極層514。閘極層514由經縮放之ONO堆疊504與基板508分隔或電性隔離。

在一實施例中，基板508為一包含某種材料之單晶體之塊狀基板，該材料可包括(但不限於)矽、鍺、矽/鍺或III-V複合半導體材料。在另一實施例中，基板508包含一具有一頂部磊晶層之塊狀層。在一特定實施例中，該塊狀層包含某種材料之單晶體，該材料可包括(但不限於)矽、鍺、矽/鍺、III-V複合半導體材料及石英，同時該頂部磊晶層包含一可包括(但不限於)矽、鍺、矽/鍺、III-V複合半導體材料的單晶體層。在另一實施例中，基板508包含一在一中間絕緣體層上面之頂部磊晶層，該中間絕緣體層位於一下方塊狀層上方。頂部磊晶層可包含一可包括(但不限於)矽(亦即，以形成絕緣體上矽(SOI)半導體基板)、鍺、矽/鍺及III-V複合半導體材料的單晶體層。絕緣體層包含可包括(但不限於)二氧化矽、氮化矽及氮氧化矽之材料。該下方塊狀層包含可包括(但不限於)矽、鍺、矽/鍺、III-V複合半導體材料及石英之單晶體。基板508及因此介於源極與汲極區域510之間的通道區域512可包含雜質原子摻雜劑。在一特定實施例中，通道區域經P型摻雜且在一替代實施

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例中，通道區域經N型摻雜。

基板508中之源極及汲極區域510可為具有與通道區域512相反之導電性之任何區域。舉例而言，根據本發明之一實施例，源極及汲極區域510經N型摻雜而通道區域512經P型摻雜。在一實施例中，基板508包含具有在1×10^{15}-1×10^{19}個原子/立方公分範圍內之硼濃度的摻硼單晶矽。源極及汲極區域510包含具有在5×10^{16}-5×10^{19}個原子/立方公分範圍內之N型摻雜劑濃度的摻磷或摻砷區域。在一特定實施例中，源極及汲極區域510在基板508中之深度可在80-200奈米範圍內。根據本發明之一替代實施例，源極及汲極區域510經P型摻雜而基板508之通道區域經N型摻雜。

SONOS型元件500進一步包括一在通道區域512之上的閘極堆疊502，閘極堆疊502包括一ONO堆疊504、一閘極層514及一閘極頂蓋層525。ONO堆疊504進一步包括穿隧層516、一電荷捕獲層518及一阻擋層520。

在一實施例中，穿隧層516包括經氮化之氧化物。因為程式化電壓及擦除電壓產生跨過穿隧層之約10 MV/cm之大電場，所以程式化/擦除穿隧電流與穿隧層障壁高度之相關性高於其與穿隧層厚度之相關性。然而，在保存期間，不存在大電場且因此電荷損失與穿隧層厚度之相關性高於其與障壁高度之相關性。為在不損失電荷保存能力之情況下改良用於降低之工作電壓之穿隧電流，在一特定實施例中，穿隧層516為經氮化之氧化物。氮化藉由將氮誘導至另外純二氧化矽薄膜中來增加穿隧層之相對電容率或

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介電常數(ε)。在某些實施例中，經氮化之氧化物之穿隧層516具有與採用純氧穿隧氧化物之習知SONOS型元件相同的實際厚度。在特定實施例中，氮化提供具有在4.75與5.25之間，較佳在4.90與5.1之間(在標準溫度下)之有效(ε)的穿隧層。在一此類實施例中，氮化提供在標準溫度下具有5.07之有效(ε)之穿隧層。

在某些實施例中，經縮放之SONOS元件的經氮化之穿隧氧化物具有與採用純氧穿隧氧化物之習知未縮放SONOS元件相同之實際厚度。通常，經氮化之穿隧氧化物之較高電容率使記憶層充電更快。在此等實施例中，因為來自控制閘極之大電場跨過經氮化之穿隧氧化物下降相對較少(由於經氮化之穿隧氧化物之電容率相對較高)，所以電荷捕獲層518在程式化/擦除期間之充電速度快於同樣厚度之純氧穿隧氧化物之充電速度。此等實施例允許SONOS型元件500在降低之程式化/擦除電壓下操作同時仍然達成與習知SONOS型元件相同之程式化/擦除電壓臨限值位準(VTP/VTE)。在一特定實施例中，SONOS型元件500採用具有實際厚度在1.5 nm與3.0 nm之間，且較佳在1.9 nm與2.2 nm之間的經氮化之穿隧氧化物之穿隧層516。

在另一實施例中，穿隧層516係以特定方式氮化以減小基板介面上之陷阱密度從而改良電荷保存能力。對於經氮化之氧化物穿隧層經縮放為與純氧穿隧氧化物相同之實際厚度之特定實施例而言，電荷保存能力可大致與具有同樣厚度之純氧穿隧氧化物相同。參看圖6，描繪穿隧層616之

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一實施例內之近似氮濃度分布，朝向基板介面613氮濃度614迅速減小以限制與基板612接觸之氮化矽(Si_3N_4)層之形成。一包含極性分子之氮化矽層若存在於基板介面613上則有害地增大陷阱密度，由此減小經由陷阱至陷阱穿隧所達成之電荷保存能力。因此，藉由調整經氮化之穿隧氧化物內之氮濃度，可在不顯著降低經縮放之SONOS元件的電荷保存能力之情況下降低程式化/擦除V_{CG}。如圖4中進一步展示，穿隧層416鄰近介面413之25%厚度經氮化從而具有小於約5×10^{21}個氮原子/立方公分之氮濃度414同時穿隧層416鄰近電荷捕獲層420之25%厚度經氮化從而每立方公分具有至少5×10^{21}個氮原子。

在一實施例中，相對於純氧化物穿隧層而言，穿隧層內之氧化物之氮化降低其能量障壁且增加介電常數。如圖5中所示，出於說明之目的，以中心線517對穿隧層516加以註釋。圖6以穿隧層616鄰近基板612之一半厚度及穿隧層616鄰近電荷陷落層618之之一半厚度來描繪類似中心線617。在一特定實施例中，氮濃度614在穿隧層616之整個最初25%厚度上低於5×10^{21}個原子/立方公分且在穿隧層616之50%厚度處或在中心線617處達到大約5×10^{21}個原子/立方公分。在另一實施例中，氮濃度614在穿隧層616鄰近電荷捕獲層618之最後25%厚度內高於5×10^{21}個原子/立方公分。在一例示性實施例中，對2.2 nm之穿隧層而言，氮濃度614在穿隧層鄰近基板612之最初0.6 nm內低於5×10^{21}個原子/立方公分且在1.1 nm之穿隧層616厚度處為至少

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5×10^{21}個原子/立方公分。以此方式，可在不顯著降低經縮放之SONOS型元件之電荷保存能力的情況下增加穿隧層之電容。

圖7說明一描繪展示可歸因於根據本發明之一實施例的經氮化之氧化物穿隧層之程式化電壓降低的模擬之圖表。如圖所示，在保存電壓下，20 Å純氧化物穿隧層及40 Å氮化物電荷捕獲層之漏電流等於20 Å經氮化之氧化物穿隧層及40 Å電荷捕獲層氮化物之漏電流，同時在程式化電壓下，經氮化之氧化物穿隧層之充電電流大於純氧化物穿隧層之充電電流。因此，在9.1 V之程式化電壓或擦除電壓下，根據本發明之經氮化之氧化物穿隧層可提供與在10 V之程式化電壓或擦除電壓下及習知純氧化物穿隧層所達成之程式化擦除位準相同之程式化擦除位準。

再參看圖5，SONOS型元件500之電荷捕獲層518可進一步包括任何一般已知之電荷捕獲材料且具有適於儲存電荷之任何厚度且調變元件之臨限電壓。在某些實施例中，電荷捕獲層518為氮化矽(Si_3N_4)、富矽氮化矽或富矽氮氧化矽。富矽薄膜包括懸空矽鍵。在一特定實施例中，電荷捕獲層518在電荷捕獲層之厚度上具有不均勻化學計量。舉例而言，電荷捕獲層518可進一步包括至少兩個具有不同矽、氧及氮組成之氮氧化物層。此在電荷捕獲層內的組成不均勻性具有諸多優於具有大體上均勻組成之習知SONOS電荷捕獲層之效能優勢。舉例而言，降低習知SONOS電荷捕獲層之厚度增加陷阱至陷阱之穿隧率，導致資料保存能

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