



Selection Guide

	CY7C0430BV -133	CY7C0430BV -100
f_{MAX2} (MHz)	133	100
Max Access Time (ns) (Clock to Data)	4.7	5.0
Max Operating Current I_{CC} (mA)	750	600
Max Standby Current for I_{SB1} (mA) (All ports TTL Level)	200	150
Max Standby Current for I_{SB3} (mA) (All ports CMOS Level)	5.0	5.0

Pin Definitions

Port 1	Port 2	Port 3	Port 4	Description
$A_{0P1}-A_{15P1}$	$A_{0P2}-A_{15P2}$	$A_{0P3}-A_{15P3}$	$A_{0P4}-A_{15P4}$	Address Input/Output.
$I/O_{0P1}-I/O_{17P1}$	$I/O_{0P2}-I/O_{17P2}$	$I/O_{0P3}-I/O_{17P3}$	$I/O_{0P4}-I/O_{17P4}$	Data Bus Input/Output.
CLK_{P1}	CLK_{P2}	CLK_{P3}	CLK_{P4}	Clock Input. This input can be free running or strobed. Maximum clock input rate is f_{MAX} .
LB_{P1}	LB_{P2}	LB_{P3}	LB_{P4}	Lower Byte Select Input. Asserting this signal LOW enables read and write operations to the lower byte. For read operations both the LB and OE signals must be asserted to drive output data on the lower byte of the data pins.
UB_{P1}	UB_{P2}	UB_{P3}	UB_{P4}	Upper Byte Select input. Same function as LB , but to the upper byte.
$\overline{CE}_{0P1}, \overline{CE}_{1P1}$	$\overline{CE}_{0P2}, \overline{CE}_{1P2}$	$\overline{CE}_{0P3}, \overline{CE}_{1P3}$	$\overline{CE}_{0P4}, \overline{CE}_{1P4}$	Chip Enable Input. To select any port, both $\overline{CE}_0$ AND $\overline{CE}_1$ must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $\overline{CE}_1 \geq V_{IH}$).
$\overline{OE}_{P1}$	$\overline{OE}_{P2}$	$\overline{OE}_{P3}$	$\overline{OE}_{P4}$	Output Enable Input. This signal must be asserted LOW to enable the I/O data lines during read operations. $\overline{OE}$ is asynchronous input.
R/W_{P1}	R/W_{P2}	R/W_{P3}	R/W_{P4}	Read/Write Enable Input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
$\overline{MRST}$				Master Reset Input. This is one signal for All Ports. $\overline{MRST}$ is an asynchronous input. Asserting $\overline{MRST}$ LOW performs all of the reset functions as described in the text. A $\overline{MRST}$ operation is required at power-up.
$\overline{CNTRST}_{P1}$	$\overline{CNTRST}_{P2}$	$\overline{CNTRST}_{P3}$	$\overline{CNTRST}_{P4}$	Counter Reset Input. Asserting this signal LOW resets the burst address counter of its respective port to zero. $\overline{CNTRST}$ is second to $\overline{MRST}$ in priority with respect to counter and mask register operations.
$\overline{MKLD}_{P1}$	$\overline{MKLD}_{P2}$	$\overline{MKLD}_{P3}$	$\overline{MKLD}_{P4}$	Mask Register Load input. Asserting this signal LOW loads the mask register with the external address available on the address lines. $\overline{MKLD}$ operation has higher priority over $\overline{CNTLD}$ operation.
$\overline{CNTLD}_{P1}$	$\overline{CNTLD}_{P2}$	$\overline{CNTLD}_{P3}$	$\overline{CNTLD}_{P4}$	Counter Load Input. Asserting this signal LOW loads the burst counter with the external address present on the address pins.
$\overline{CNTINC}_{P1}$	$\overline{CNTINC}_{P2}$	$\overline{CNTINC}_{P3}$	$\overline{CNTINC}_{P4}$	Counter Increment Input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK.



Pin Definitions (continued)

Port 1	Port 2	Port 3	Port 4	Description
CNTRD _{p1}	CNTRD _{p2}	CNTRD _{p3}	CNTRD _{p4}	Counter Readback Input. When asserted LOW, the internal address value of the counter will be read back on the address lines. During CNTRD operation, both CNTLD and CNTINC must be HIGH. Counter readback operation has higher priority over mask register readback operation. Counter readback operation is independent of port chip enables. If address readback operation occurs with chip enables active ($\overline{CE}_0 = \text{LOW}$, $CE_1 = \text{HIGH}$), the data lines (I/Os) will be three-stated. The readback timing will be valid after one no-operation cycle plus t_{CD2} from the rising edge of the next cycle.
MKRD _{p1}	MKRD _{p2}	MKRD _{p3}	MKRD _{p4}	Mask Register Readback Input. When asserted LOW, the value of the mask register will be readback on address lines. During mask register readback operation, all counter and MKLD inputs must be HIGH (see Counter and Mask Register Operations truth table). Mask register readback operation is independent of port chip enables. If address readback operation occurs with chip enables active ($\overline{CE}_0 = \text{LOW}$, $CE_1 = \text{HIGH}$), the data lines (I/Os) will be three-stated. The readback will be valid after one no-operation cycle plus t_{CD2} from the rising edge of the next cycle.
CNTINT _{p1}	CNTINT _{p2}	CNTINT _{p3}	CNTINT _{p4}	Counter Interrupt flag output. Flag is asserted LOW for one clock cycle when the counter wraps around to location zero.
INT _{p1}	INT _{p2}	INT _{p3}	INT _{p4}	Interrupt flag output. Interrupt permits communications between all four ports. The upper four memory locations can be used for message passing. Example of operation: INT _{p4} is asserted LOW when another port writes to the mailbox location of Port 4. Flag is cleared when Port 4 reads the contents of its mailbox. The same operation is applicable to Ports 1, 2, and 3.
TMS				JTAG Test Mode Select Input. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK.
TCK				JTAG Test Clock Input. This can be CLK of any port or an external clock connected to the JTAG TAP.
TDI				JTAG Test Data Input. This is the only data input. TDI inputs will shift data serially in to the selected register.
TDO				JTAG Test Data Output. This is the only data output. TDO transitions occur on the falling edge of TCK. TDO normally three-stated except when captured data is shifted out of the JTAG TAP.
CLKBIST				BIST Clock Input.
GND				Thermal ground for heat dissipation.
V _{SS}				Ground Input.
V _{DD}				Power Input.
V _{SS1}				Address lines ground Input.
V _{DD1}				Address lines power Input.
V _{SS2}				Data lines ground Input.
V _{DD2}				Data lines power Input.



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to + 150°C

Ambient Temperature with

Power Applied -55°C to + 125°C

Supply Voltage to Ground Potential -0.5V to + 4.6V

DC Voltage Applied to

Outputs in High Z State -0.5V to $V_{CC}+0.5V$ DC Input Voltage -0.5V to $V_{CC}+0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >1100V

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	3.3V ± 150 mV
Industrial	-40°C to +85°C	3.3V ± 150 mV

Electrical Characteristics Over the Operating Range

Parameter	Description	CY7C0430BV						Unit
		-133			-100			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{OH}	Output HIGH Voltage (V _{CC} = Min., I _{OH} = -4.0 mA)	2.4			2.4			V
V _{OL}	Output LOW Voltage (V _{CC} = Min., I _{OH} = +4.0 mA)			0.4			0.4	V
V _{IH}	Input HIGH Voltage	2.0			2.0			V
V _{IL}	Input LOW Voltage			0.8			0.8	V
I _{OZ}	Output Leakage Current	-10		10	-10		10	μA
I _{CC}	Operating Current (V _{CC} = Max., I _{OYT} = 0 mA) Outputs Disabled, CE = V _{IL} , f = f _{max}	Indust. Com'l.	413	750		330	600	mA
I _{SB1}	Standby Current (4 Ports toggling at TTL Levels, 0 active) CE ₁₋₄ ≥ V _{IH} , f = f _{MAX}	Indust. Com'l.	80	200		60	150	mA
I _{SB2}	Standby Current (4 Ports toggling at TTL Levels, 1 active) CE ₁ CE ₂ CE ₃ CE ₄ ≤ V _{IL} , f = f _{MAX}	Indust. Com'l.	170	349		128	263	mA
I _{SB3}	Standby Current (4 Ports CMOS Level, 0 active) CE ₁₋₄ ≥ V _{IH} , f = 0	Indust. Com'l.	1.5	5		1.5	5	mA
I _{SB4}	Standby Current (4 Ports CMOS Level, 1 active and toggling) CE ₁ CE ₂ CE ₃ CE ₄ ≤ V _{IL} , f = f _{MAX}	Indust. Com'l.	110	240		83	180	mA

JTAG TAP Electrical Characteristics Over the Operating Range

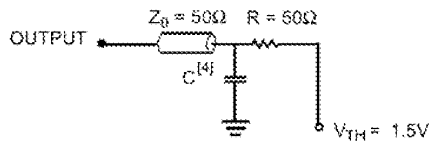
Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	$I_{OH} = -4.0 \text{ mA}$	2.4		V
V_{OL1}	Output LOW Voltage	$I_{OL} = 4.0 \text{ mA}$		0.4	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_x	Input Leakage Current	$GND \leq V_i \leq V_{DD}$	-100	100	μA

Capacitance

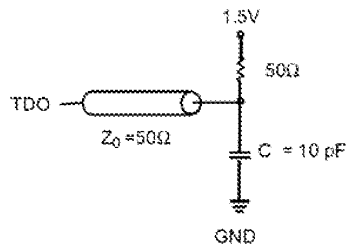
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3V$	8	pF
C_{OUT}	Output Capacitance		8	pF



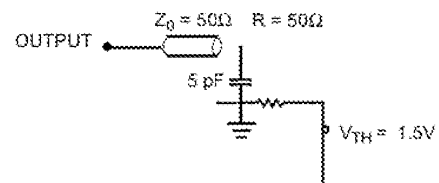
AC Test Load



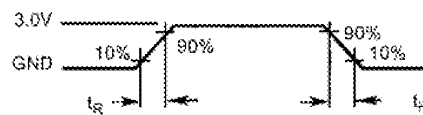
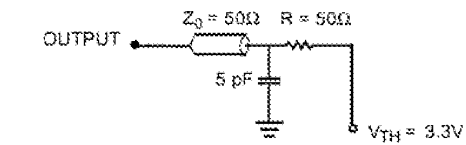
(a) Normal Load



(c) TAP Load



(b) Three-State Delay



ALL INPUT PULSES

Note:

4. Test Conditions: C = 10 pF



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Switching Characteristics Over the Industrial Operating Range ^[7]

Parameter	Description	CY7C0430BV				Unit
		-133		-100		
		Min.	Max.	Min.	Max.	
f _{MAX2}	Maximum Frequency		133		100	MHz
t _{CYC2}	Clock Cycle Time	7.5		10		ns
t _{CH2}	Clock HIGH Time	3		4		ns
t _{CL2}	Clock LOW Time	3		4		ns
t _R	Clock Rise Time		2		3	ns
t _F	Clock Fall Time		2		3	ns
t _{SA}	Address Set-up Time	2.3		3		ns
t _{HA}	Address Hold Time	0.7		0.7		ns
t _{SC}	Chip Enable Set-up Time	2.3		3		ns
t _{HC}	Chip Enable Hold Time	0.7		0.7		ns
t _{SW}	R/W Set-up Time	2.3		3		ns
t _{HW}	R/W Hold Time	0.7		0.7		ns
t _{SD}	Input Data Set-up Time	2.3		3		ns
t _{HD}	Input Data Hold Time	0.7		0.7		ns
t _{SB}	Byte Set-up Time	2.3		3		ns
t _{HB}	Byte Hold Time	0.7		0.7		ns
t _{SCLD}	CNTLD Set-up Time	2.3		3		ns
t _{HCLD}	CNTLD Hold Time	0.7		0.7		ns
t _{SCINC}	CNTINC Set-up Time	2.3		3		ns
t _{HCINC}	CNTINC Hold Time	0.7		0.7		ns
t _{SCRST}	CNTRST Set-up Time	2.3		3		ns
t _{HCRST}	CNTRST Hold Time	0.7		0.7		ns
t _{SCRD}	CNTRD Set-up Time	2.3		3		ns
t _{HCRD}	CNTRD Hold Time	0.7		0.7		ns
t _{SMLD}	MKLD Set-up Time	2.3		3		ns
t _{HMLD}	MKLD Hold Time	0.7		0.7		ns
t _{SMRD}	MKRD Set-up Time	2.3		3		ns
t _{HMRD}	MKRD Hold Time	0.7		0.7		ns
t _{OE}	Output Enable to Data Valid		6.5		8	ns
t _{OLZ} ^[6]	OE to LOW Z	1		1		ns
t _{OHZ} ^[5]	OE to HIGH Z	1	6	1	7	ns
t _{CD2}	Clock to Data Valid		4.7		5	ns
t _{CA2}	Clock to Counter Address Readback Valid		4.7		5	ns
t _{CM2}	Clock to Mask Register Readback Valid		4.7		5	ns
t _{DC}	Data Output Hold After Clock HIGH	1		1		ns
t _{CKHZ} ^[6]	Clock HIGH to Output High Z	1	4.8	1	6.8	ns
t _{CKLZ} ^[6]	Clock HIGH to Output LOW Z	1		1		ns

Note:

5. This parameter is guaranteed by design, but it is not production tested.
 6. Valid for both address and data outputs.



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Switching Characteristics Over the Industrial Operating Range (continued)^[7]

Parameter	Description	CY7C0430BV				Unit
		-133		-100		
		Min.	Max.	Min.	Max.	
t _{SINT}	Clock to INT Set Time	1	7.5	1	10	ns
t _{RINT}	Clock to INT Reset Time	1	7.5	1	10	ns
t _{SCINT}	Clock to CNTINT Set Time	1	7.5	1	10	ns
t _{RCINT}	Clock to CNTINT Reset Time	1	7.5	1	10	ns
Master Reset Timing						
t _{RS}	Master Reset Pulse Width	7.5		10		ns
t _{RSR}	Master Reset Recovery Time	7.5		10		ns
t _{ROF}	Master Reset to Output Flags Reset Time		6.5		8	ns
Port to Port Delays						
t _{CCS} ^[7]	Clock to Clock Set-up Time (time required after a write before you can read the same address location)	6.5		9		ns

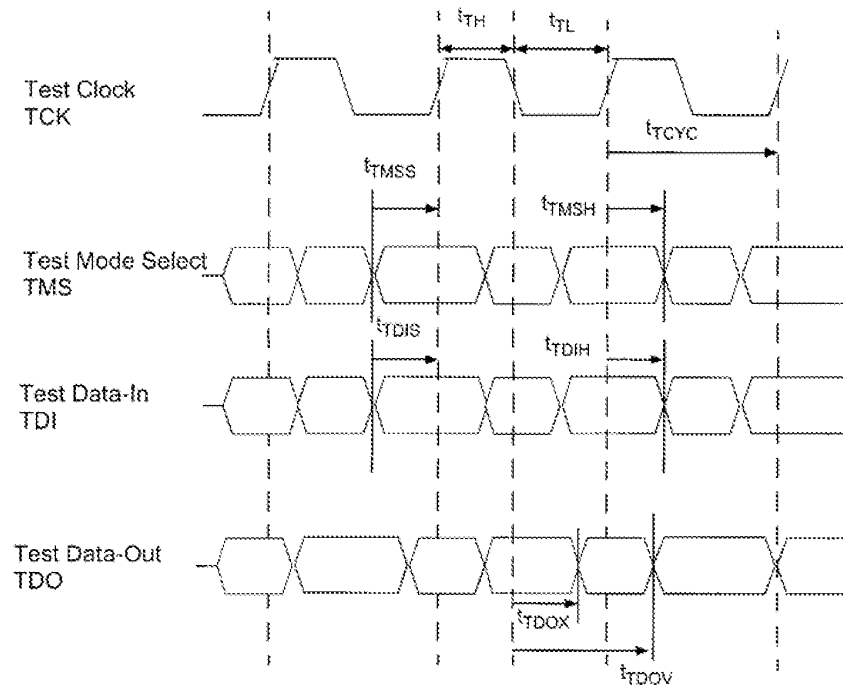
Note:

7. If data is simultaneously written and read to the same address location and t_{CCS} is violated, the data read from the address, as well as the subsequent data remaining in the address is undefined.



JTAG Timing and Switching Waveforms

Parameter	Description	CY7C0430BV				Unit
		-133		-100		
		Min.	Max.	Min.	Max.	
f _{JTAG}	Maximum JTAG TAP Controller Frequency		10		10	MHz
t _{TCYC}	TCK Clock Cycle Time	100		100		ns
t _{TH}	TCK Clock High Time	40		40		ns
t _{TL}	TCK Clock Low Time	40		40		ns
t _{TMSS}	TMS Setup to TCK Clock Rise	20		20		ns
t _{TMSH}	TMS Hold After TCK Clock Rise	20		20		ns
t _{TDis}	TDI Setup to TCK Clock Rise	20		20		ns
t _{TDIH}	TDI Hold after TCK Clock Rise	20		20		ns
t _{TDOV}	TCK Clock Low to TDO Valid		20		20	ns
t _{TDOX}	TCK Clock Low to TDO Invalid	0		0		ns
f _{BIST}	Maximum CLKBIST Frequency		50		50	MHz
t _{BH}	CLKBIST High Time	6		6		ns
t _{BL}	CLKBIST Low Time	6		6		ns





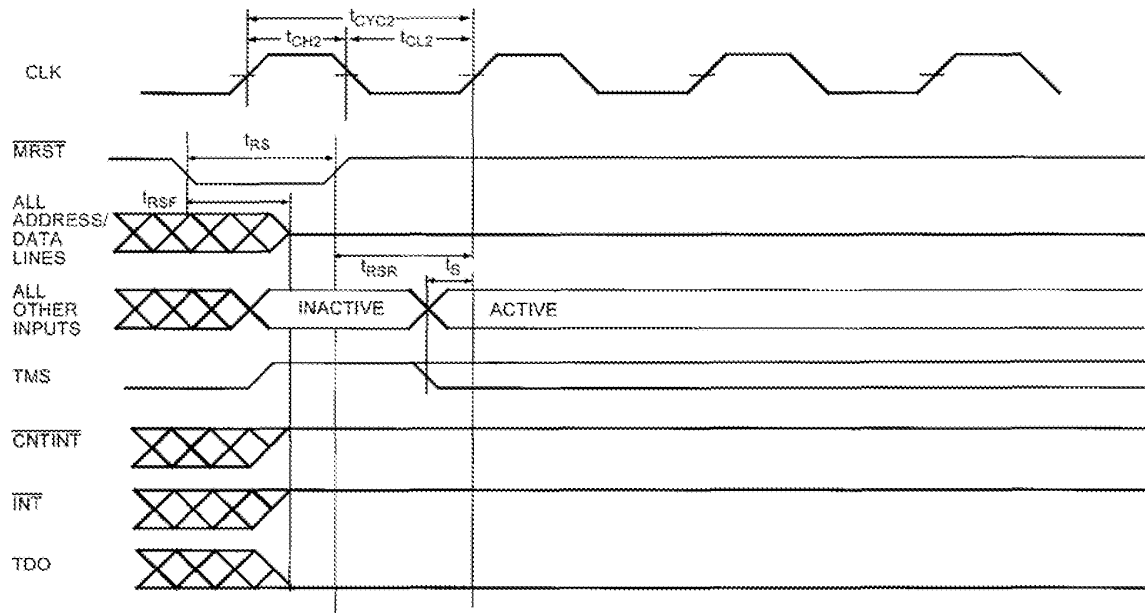
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Switching Waveforms

Master Reset^[6]



Note:

6. t_S is the set-up time required for all input control signals.

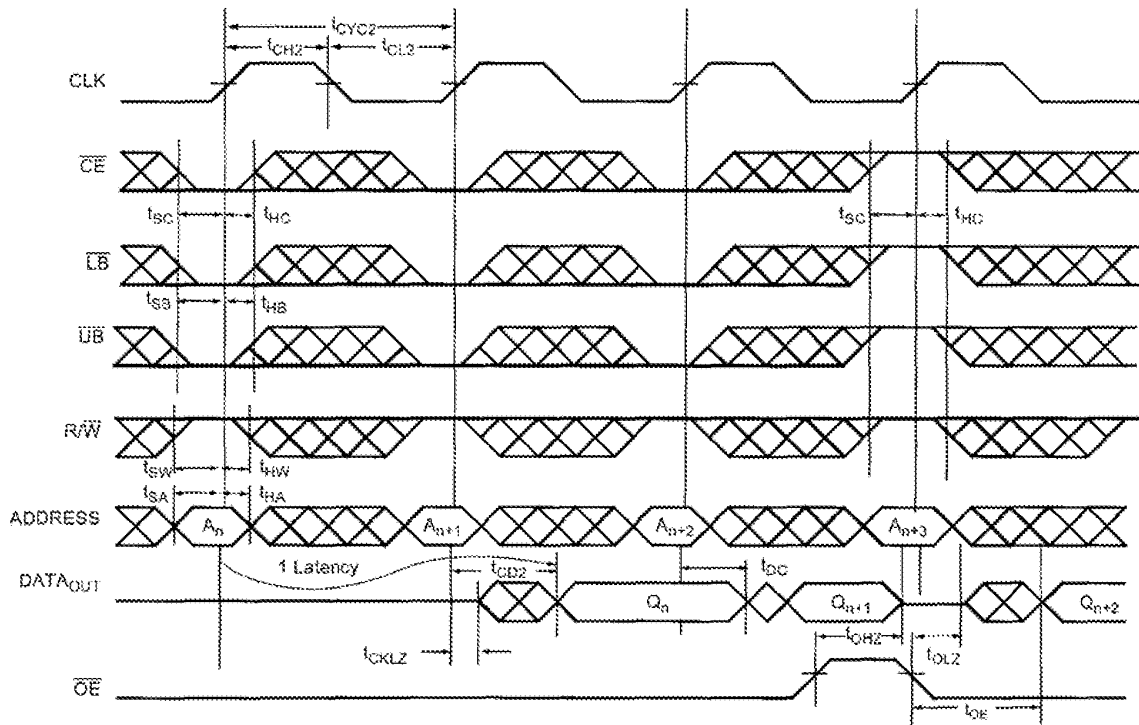


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Switching Waveforms (continued)

Read Cycle^{9, 10, 11, 12, 13}

Notes:

9. $\overline{OE}$ is asynchronously controlled; all other inputs (excluding $\overline{MRST}$) are synchronous to the rising clock edge.
10. $\overline{CNTLD} = V_{IL}$, $\overline{MRKD} = V_{IH}$, $\overline{CNTINC} = x$, and $\overline{MRST} = \overline{CNRST} = V_{IL}$.
11. The output is disabled (high-impedance state) by $\overline{CE} = V_{IH}$ following the next rising edge of the clock.
12. Addresses do not have to be accessed sequentially. Note 10 indicates that address is constantly loaded on the rising edge of the CLK. Numbers are for reference only.
13. $\overline{CE}$ is internal signal. $\overline{CE} = V_{IL}$ if $\overline{CE}_0 = V_{IL}$ and $\overline{CE}_1 = V_{IH}$.

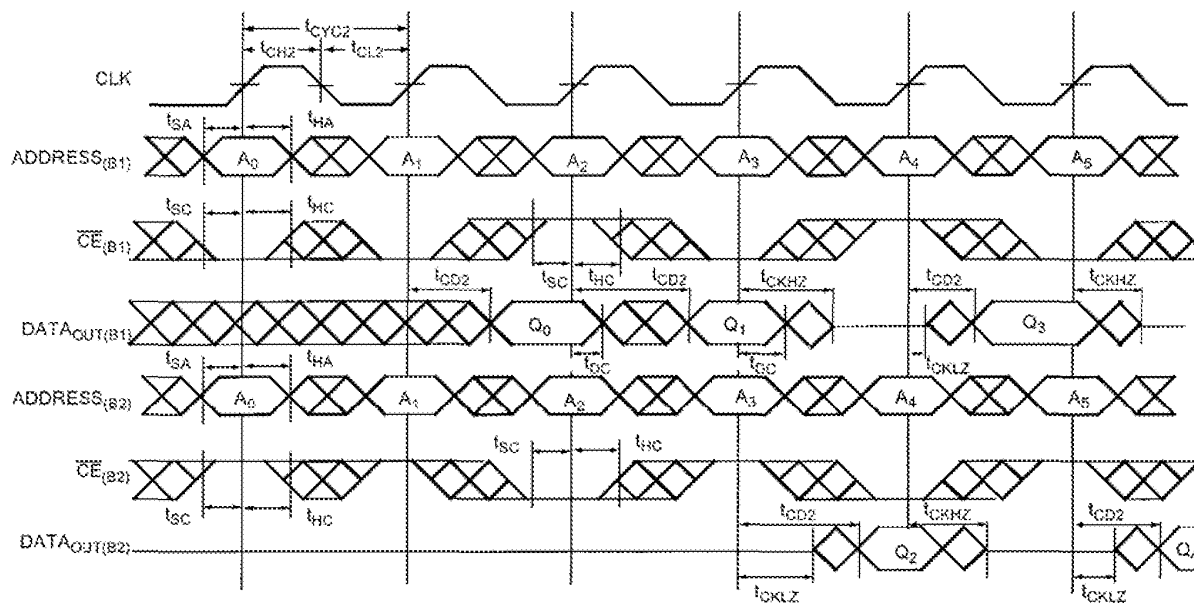
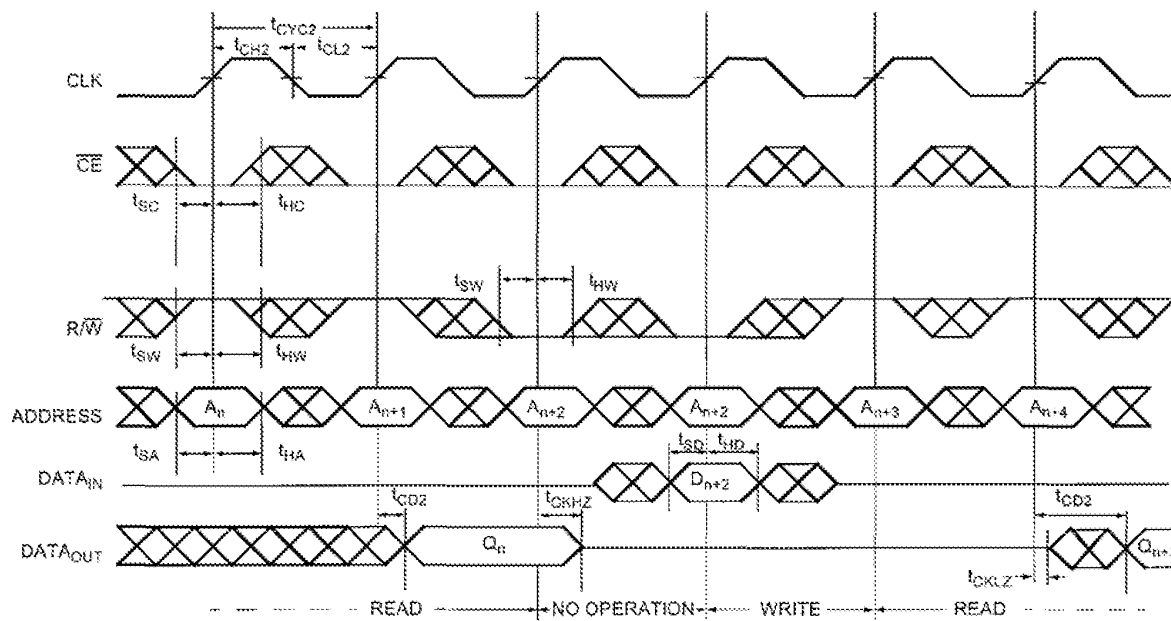


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Switching Waveforms (continued)

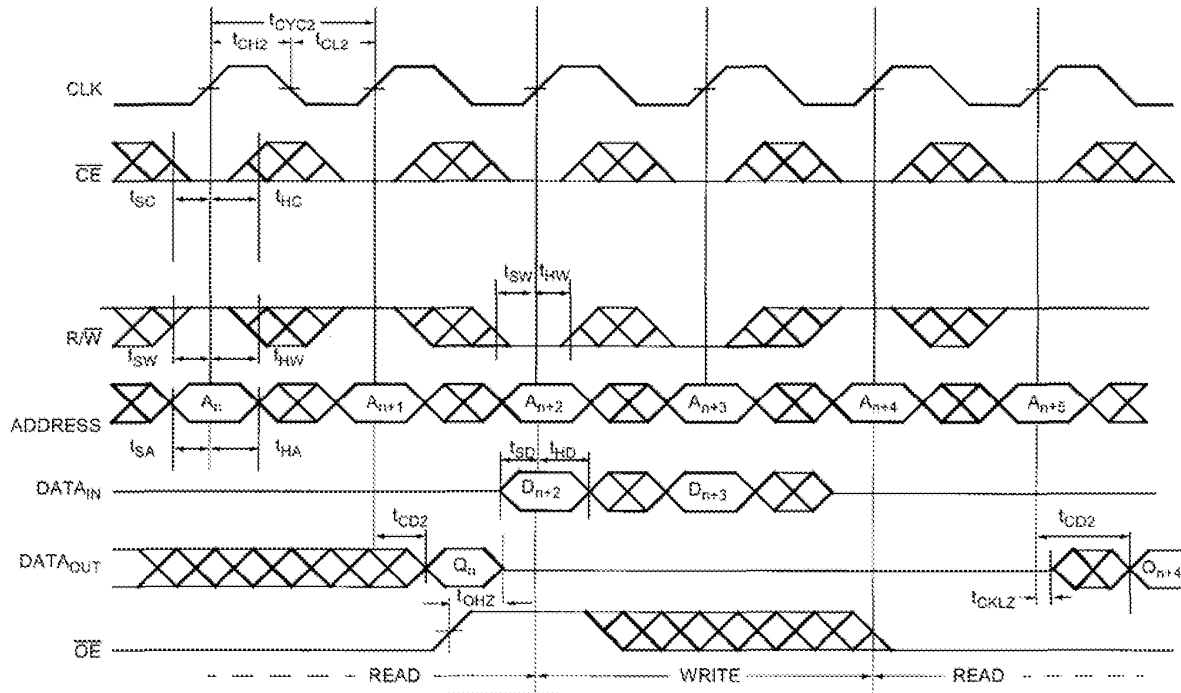
Bank Select Read^[14, 15]Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)^[16, 17, 18, 19]

Notes:

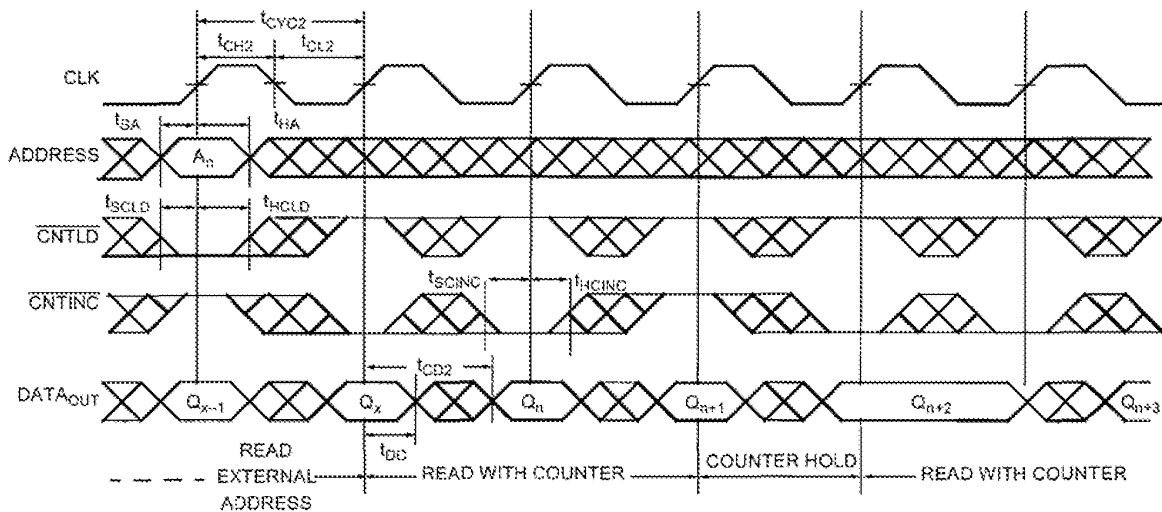
14. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress Quadport device from this data sheet.
15. $LB = UB = OE = CNTLD = V_{IL}$, $MRST = CNTRST = MKLD = V_{IL}$.
16. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
17. $LB = UB = CNTLD = V_{IL}$, $MRST = CNTRST = MKLD = V_{IL}$.
18. Addresses do not have to be accessed sequentially since $CNTLD = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference only.
19. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.



Switching Waveforms (continued)

Read-to-Write-to-Read ($\overline{OE}$ Controlled) [16, 17, 18, 19]

Read with Address Counter Advance [20, 21]



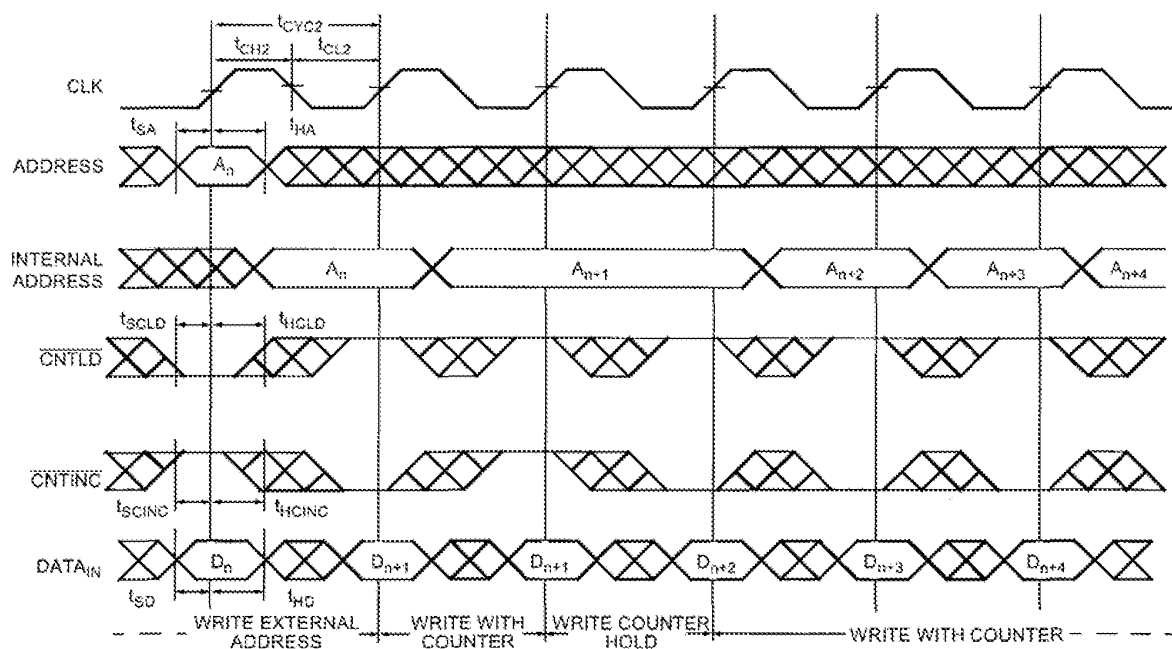
Notes:

20. $\overline{CE}_0 = \overline{OE} = \overline{CB} = \overline{UB} = V_{IL}$; $\overline{CE}_1 = \overline{RAW} = \overline{CNTRST} = \overline{MRST} = \overline{MKLD} = \overline{MKRD} = \overline{CNTRD} = V_{IH}$.21. The "Internal Address" is equal to the "External Address" when $\overline{CNTLD} = V_{IL}$.



Switching Waveforms (continued)

Write with Address Counter Advance [21, 22]



Note:

22. $CE_n = \overline{LB} = \overline{UB} = R/W = V_{IL}$; $CE_1 = \overline{CNTLD} = \overline{MRST} = \overline{MKLD} = \overline{MKRD} = \overline{CNTRD} = V_{IH}$.



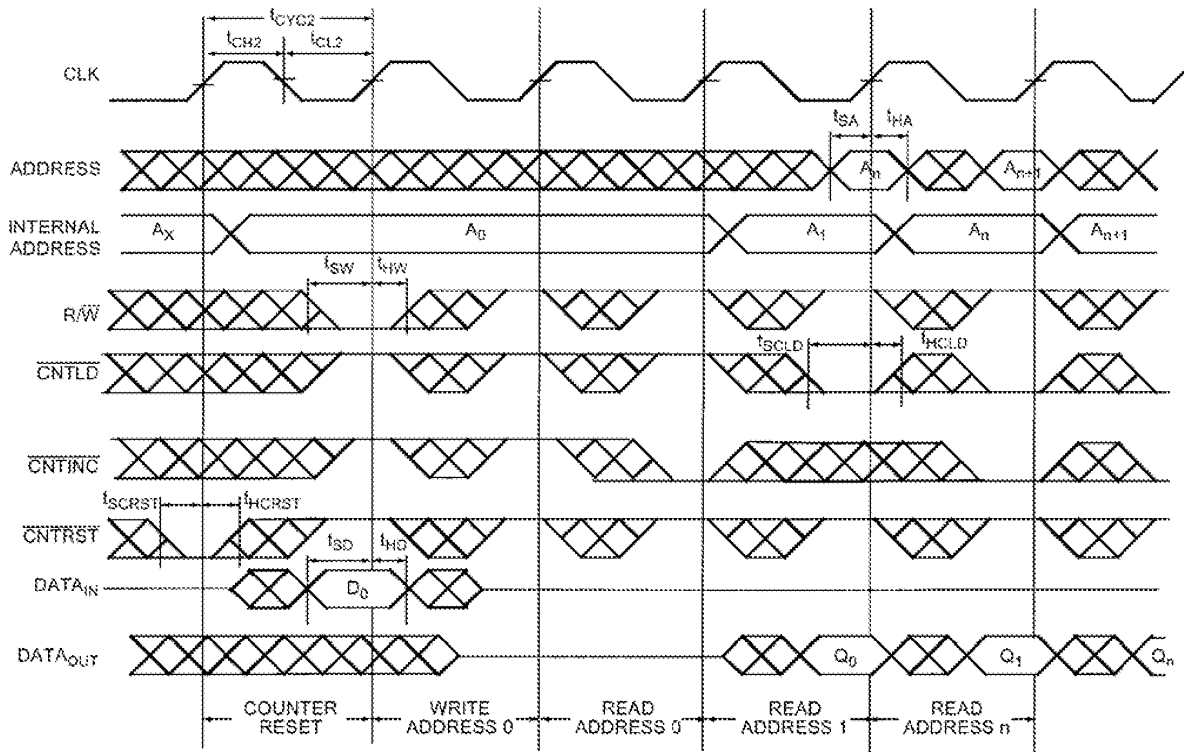
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Switching Waveforms (continued)

Counter Reset [18, 23, 24]



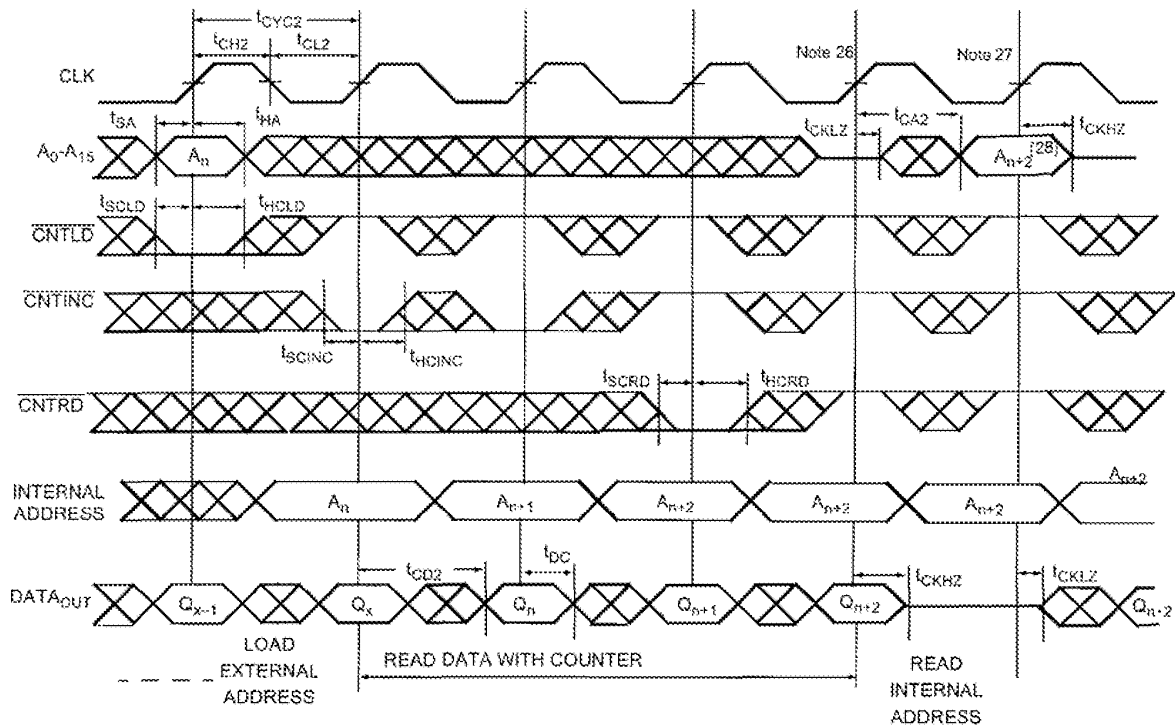
Notes:

23. $CE_0 = \overline{LB} = \overline{UB} = V_{IL}$; $CE_1 = \overline{MRST} = \overline{MKLD} = \overline{MKRD} = \overline{CNTRD} = V_{IH}$.

24. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.



Switching Waveforms (continued)

Load and Read Address Counter^[25]

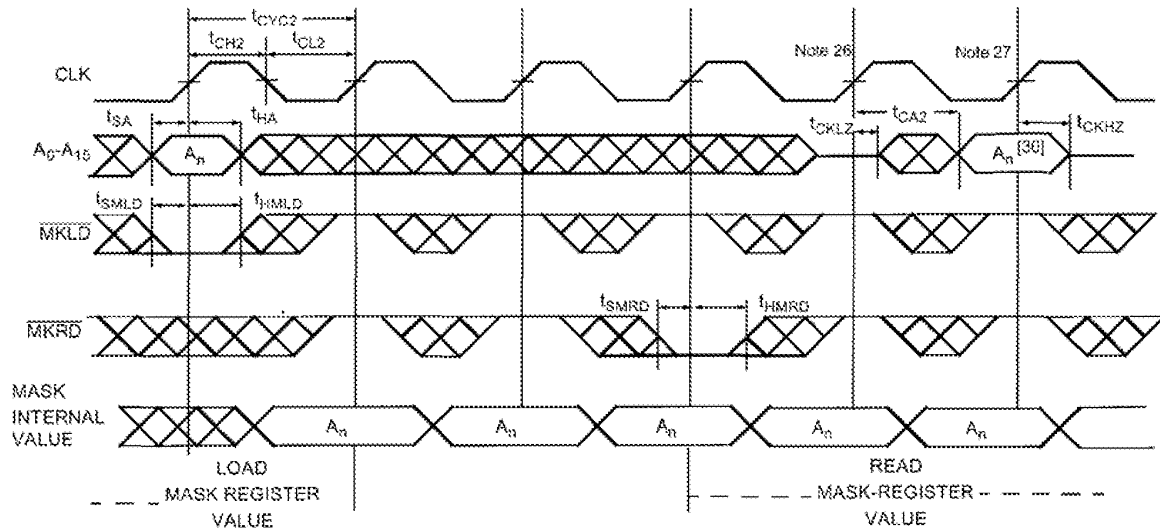
Notes:

25. $\overline{CE}_0 = \overline{CE} = \overline{LB} = \overline{UB} = V_{IL}$; $\overline{CE}_1 = R/\overline{W} = \overline{CNTRST} = \overline{MRST} = \overline{MKLD} = \overline{MKRD} = V_{IH}$.
 26. Address in output mode. Host must not be driving address bus after time t_{CRL2} in next clock cycle.
 27. Address in input mode. Host can drive address bus after t_{CKH2} .
 28. This is the value of the address counter being read out on the address lines.



Switching Waveforms (continued)

Load and Read Mask Register [29]



Notes:

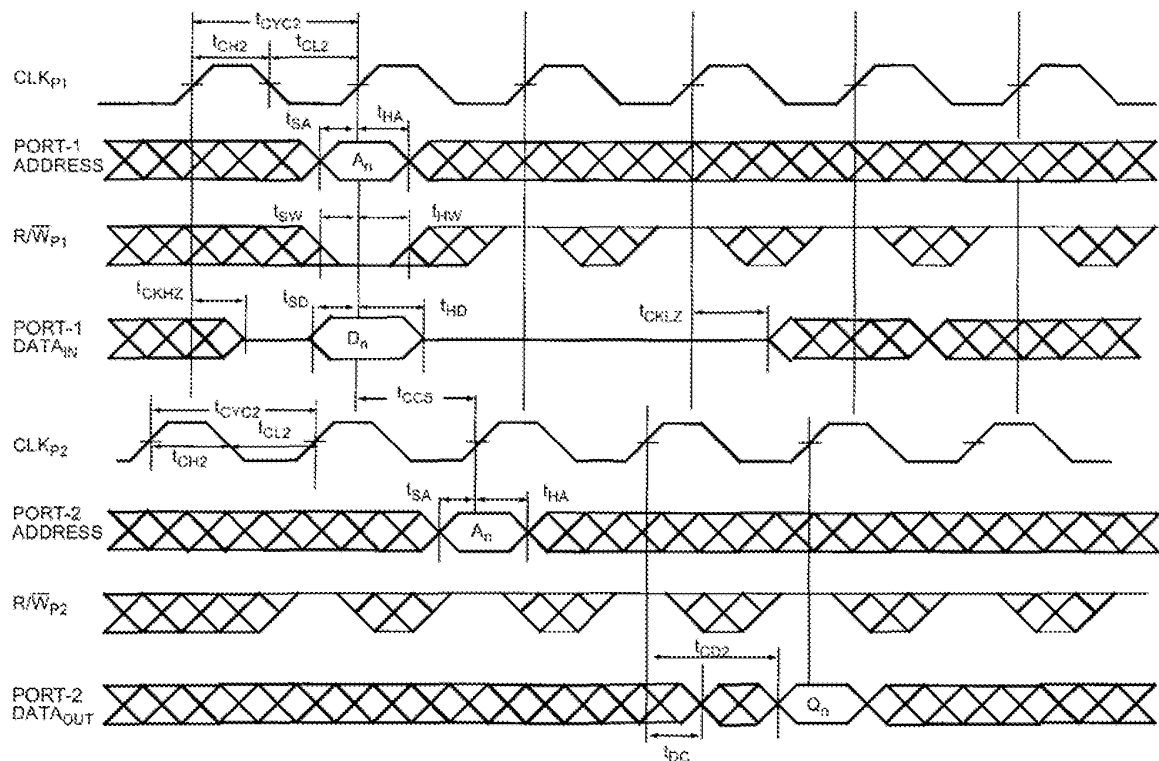
29. $\overline{CE}_0 = \overline{OE} = \overline{LE} = \overline{DE} = V_{IL}$; $\overline{CE}_1 = \overline{RW} = \overline{CNTRST} = \overline{MRST} = \overline{CNTLD} = \overline{ENTRD} = \overline{CNTINC} = V_{IH}$.

30. This is the value of the Mask Register read out on the address lines.



Switching Waveforms (continued)

Port 1 Write to Port 2 Read^[31, 32, 33]



Notes:

31. $\overline{CE_0} = \overline{OE} = \overline{CB} = \overline{UB} = \overline{CNTLD} = V_{IL}$; $\overline{CE_1} = \overline{CNTRST} = \overline{MRST} = \overline{MKLD} = \overline{MKRD} = \overline{CNTRD} = \overline{CNTINC} = V_{IH}$.
32. This timing is valid when one port is writing, and one or more of the three other ports is reading the same location at the same time. If t_{CCS} is violated, indeterminate data will be read out.
33. If $t_{CCS} <$ minimum specified value, then Port 2 will read the most recent data (written by Port 1) only ($2 \cdot t_{CYC2} + t_{CD2}$) after the rising edge of Port 2's clock. If $t_{CCS} \geq$ minimum specified value, then Port 2 will read the most recent data (written by Port 1) ($t_{CYC2} + t_{CD2}$) after the rising edge of Port 2's clock.



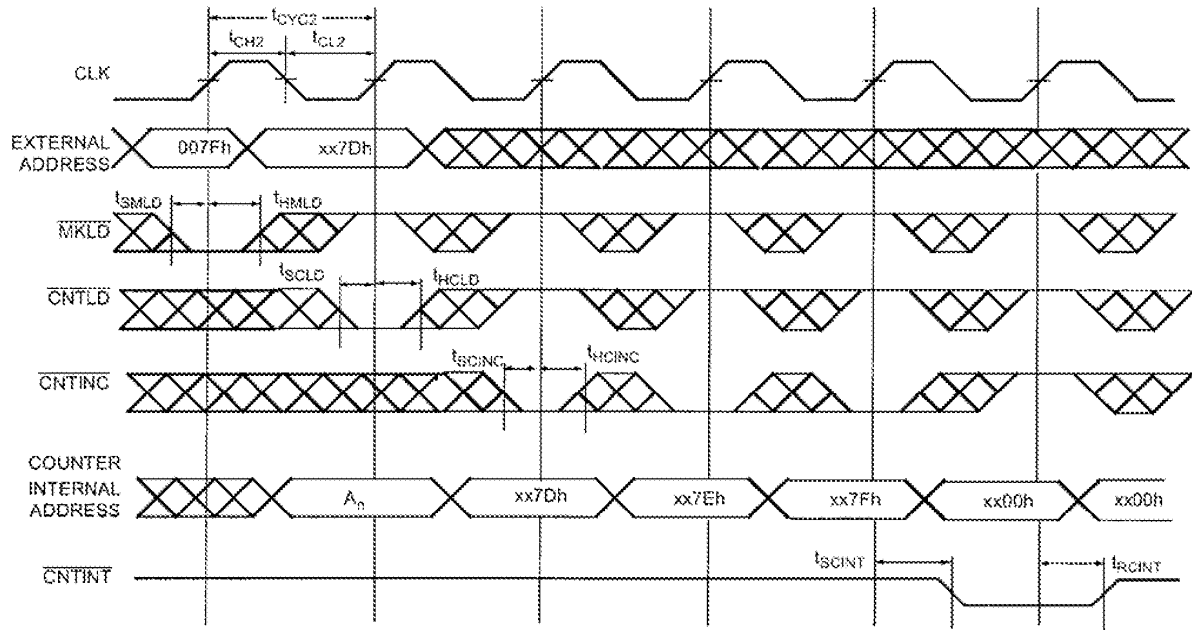
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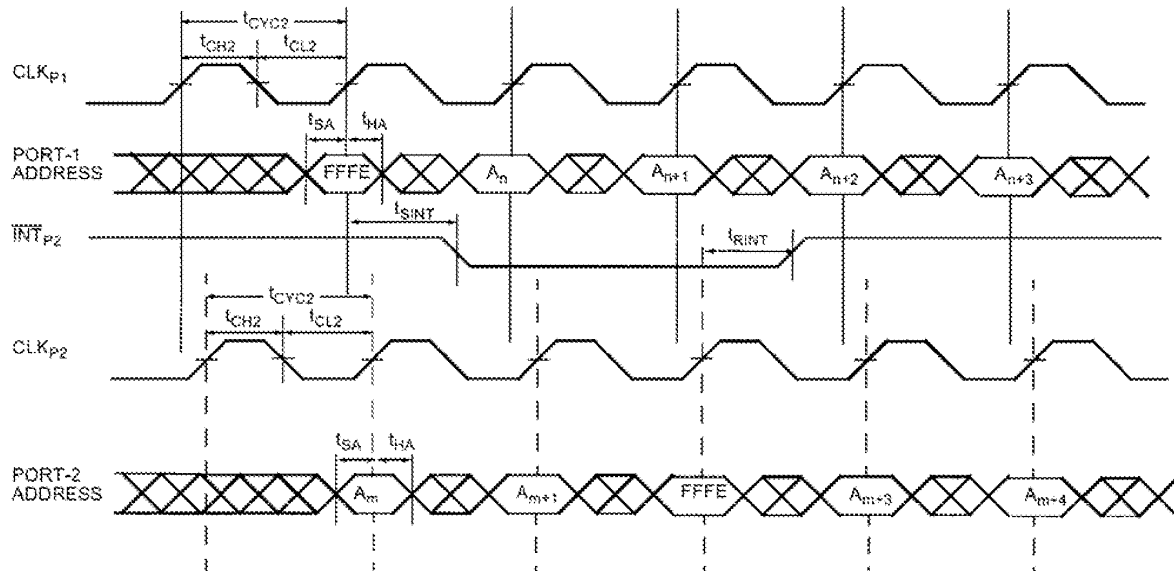
CY7C0430BV

Switching Waveforms (continued)

Counter Interrupt [34, 35, 36]



Mailbox Interrupt Timing [37, 38, 39, 40, 41]



Notes:

34. $CE_0 = CE = \overline{LB} = \overline{UB} = V_{IL}$; $CE_1 = R/\overline{W} = \overline{CNTST} = \overline{MRST} = \overline{CNTRD} = \overline{MKRD} = V_{IH}$.
35. $\overline{CNTINT}$ is always driven.
36. $\overline{CNTINC}$ goes LOW as the counter address masked portion is incremented from $xx7Fh$ to $xx00h$. The "x" is "Don't Care."
37. $CE_0 = CE = \overline{LB} = \overline{UB} = \overline{CNTLD} = V_{IL}$; $CE_1 = \overline{CNTST} = \overline{MRST} = \overline{CNTRD} = \overline{CNTINC} = \overline{MKRD} = \overline{MKLD} = V_{IH}$.
38. Address "FFFE" is the mailbox location for Port 2.
39. Port 1 is configured for Write operation, and Port 2 is configured for Read operation.
40. Port 1 and Port 2 are used for simplicity. All four ports can write to or read from any mailbox.
41. Interrupt flag is set with respect to the rising edge of the write clock, and is reset with respect to the rising edge of the read clock.



Table 1. Read/Write and Enable Operation (Any Port)^[42, 43, 44]

Inputs					Outputs	Operation
OE	CLK	CE ₀	CE ₁	R/W	I/O ₀ -I/O ₁₇	
X		H	X	X	High-Z	Deselected
X		X	L	X	High-Z	Deselected
X		L	H	L	D _{IN}	Write
L		L	H	H	D _{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

Table 2. Address Counter and Counter-Mask Register Control Operation (Any Port)^[42, 45, 46]

CLK	MRST	CNTRST	MKLD	CNTLD	CNTINC	CNTRD	MKRD	Mode	Operation
X	L	X	X	X	X	X	X	Master-Reset	Counter/Address Register Reset and Mask Register Set (resets entire chip as per reset state table)
	H	L	X	X	X	X	X	Reset	Counter/Address Register Reset
	H	H	L	X	X	X	X	Load	Load of Address Lines into Mask Register
	H	H	H	L	X	X	X	Load	Load of Address Lines into Counter/Address Register
	H	H	H	H	L	X	X	Increment	Counter Increment
	H	H	H	H	H	L	X	Read-back	Readback Counter on Address Lines
	H	H	H	H	H	H	L	Read-back	Readback Mask Register on Address Lines
	H	H	H	H	H	H	H	Hold	Counter Hold

Notes:

42. "X" = "Don't Care," "H" = V_{HH}, "L" = V_{LL}.

43. OE is an asynchronous input signal.

44. When OE changes state, deselection and read happen after one cycle of latency.

45. CE₀ = OE = V_{LL}, CE₁ = R/W = V_{HH}.

46. Counter operation and mask register operation are independent of Chip Enables.



Master Reset

The QuadPort undergoes a complete reset by taking its Master Reset (MRST) input LOW. The Master Reset input can switch asynchronously to the clocks. A Master Reset initializes the internal burst counters to zero, and the counter mask registers to all ones (completely unmasked). A Master Reset also forces the Mailbox Interrupt (INT) flags and the Counter Interrupt (CNTINT) flags HIGH, resets the BIST controller, and takes all registered control signals to a deselected read state⁴⁷. A Master Reset must be performed on the QuadPort after power-up.

Interrupts

The upper four memory locations may be used for message passing and permit communications between ports. Table 3 shows the interrupt operation for all ports. For the 1-Meg QuadPort, the highest memory location FFFF is the mailbox

for Port 1, FFFE is the mailbox for Port 2, FFFD is the mailbox for Port 3, and FFFC is the mailbox for Port 4. Table 3 shows that in order to set Port 1 INT_{P1} flag, a write by any other port to address FFFF will assert INT_{P1} LOW. A read of FFFF location by Port 1 will reset INT_{P1} HIGH. When one port writes to the other port's mailbox, the Interrupt flag (INT) of the port that the mailbox belongs to is asserted LOW. The Interrupt is reset when the owner (port) of the mailbox reads the contents of the mailbox. The interrupt flag is set in a flow-through mode (i.e., it follows the clock edge of the writing port). Also, the flag is reset in a flow-through mode (i.e., it follows the clock edge of the reading port).

Each port can read the other port's mailbox without resetting the interrupt. If an application does not require message passing, INT pins should be treated as no-connect and should be left floating. When two ports or more write to the same mailbox at the same time INT will be asserted but the contents of the mailbox are not guaranteed to be valid.

Table 3. Interrupt Operation Example

Function	Port 1		Port 2		Port 3		Port 4	
	A _{0P1-15P1}	INT _{P1}	A _{0P2-15P2}	INT _{P2}	A _{0P3-15P3}	INT _{P3}	A _{0P4-15P4}	INT _{P4}
Set Port 1 INT _{P1} Flag	X	L	FFFF	X	FFFF	X	FFFF	X
Reset Port 1 INT _{P1} Flag	FFFF	H	X	X	X	X	X	X
Set Port 2 INT _{P2} Flag	FFFE	X	X	L	FFFE	X	FFFE	X
Reset Port 2 INT _{P2} Flag	X	X	FFFE	H	X	X	X	X
Set Port 3 INT _{P3} Flag	FFFD	X	FFFD	X	X	L	FFFD	X
Reset Port 3 INT _{P3} Flag	X	X	X	X	FFFD	H	X	X
Set Port 4 INT _{P4} Flag	FFFC	X	FFFC	X	FFFC	X	X	L
Reset Port 4 INT _{P4} Flag	X	X	X	X	X	X	FFFC	H

Note:

47. During Master Reset the control signals will be set to a deselected read state: CE_{0n} = LB = UB = R/W = MKLDI = MKRDI = CNTINT = CNTINTI = CNTLDI = CNTLTI = V_{DD}; CE_{1n} = V_{IL}. The "I" suffix on all these signals denotes that these are the internal registered equivalent of the associated pin signals.

Address Counter Control Operations

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for the fast interleaved memory applications. A port's burst counter is loaded with the port's Counter Load pin (CNTLD). When the port's Counter Increment (CNTINC) is asserted, the address counter will increment on each LOW to HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until CNTINC is deasserted. Depending on the mask register state, the counter can address the entire memory array and will loop back to start. Counter Reset (CNTRST) is used to reset the Burst Counter (the Mask Register value is unaffected). When using the counter in readback mode, the internal address value of the counter will be read back on the address lines when Counter Readback Signal (CNTRD) is asserted. *Figure 1* pro-

vides a block diagram of the readback operation. *Table 2* lists control signals required for counter operations. The signals are listed based on their priority. For example, Master Reset takes precedence over Counter Reset, and Counter Load has lower priority than Mask Register Load (described below). All counter operations are independent of Chip Enables ($\overline{CE}_0$ and $\overline{CE}_1$). When the address readback operation is performed the data I/Os are three-stated (if CEs are active) and one-clock cycle (no-operation cycle) latency is experienced. The address will be read at time t_{CA2} from the rising edge of the clock following the no-operation cycle. The read back address can be either of the burst counter or the mask register based on the levels of Counter Read signal (CNTRD) and Mask Register Read signal (MKRD). Both signals are synchronized to the port's clock as shown in *Table 2*. Counter read has a higher priority than mask read.

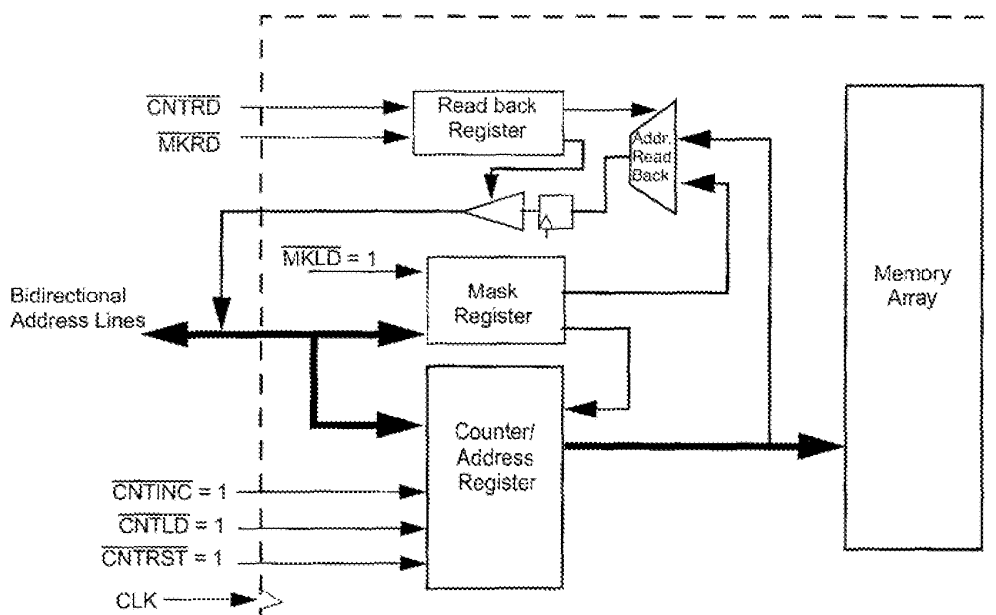
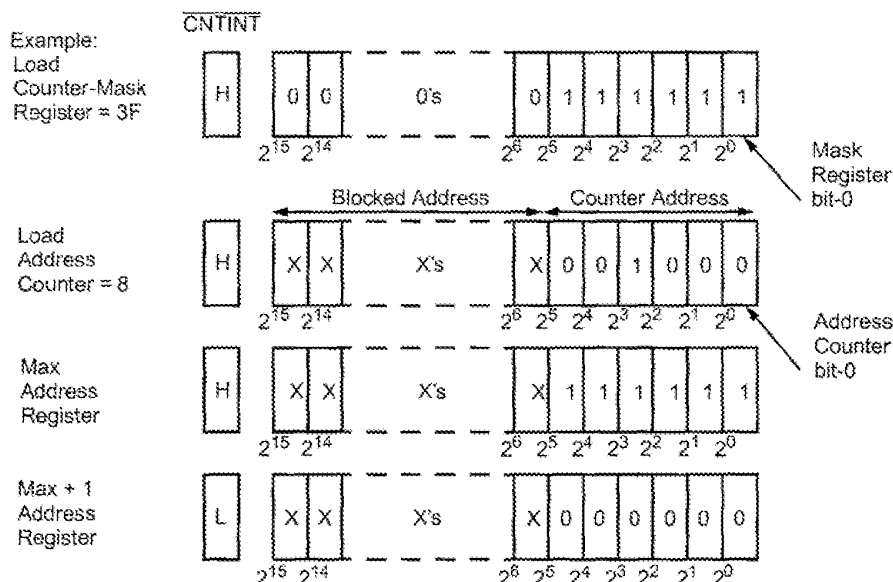


Figure 1. Counter and Mask Register Read Back on Address Lines

Counter-Mask Register



The burst counter has a mask register that controls when and where the counter wraps. An interrupt flag ($\overline{\text{CNTINT}}$) is asserted for one clock cycle when the unmasked portion of the counter address wraps around from all ones ($\overline{\text{CNTINC}}$ must be asserted) to all zeros. The example in Figure 2 shows the counter mask register loaded with a mask value of 003F unmasking the first 6 bits with bit "0" as the LSB and bit "15" as the MSB. The maximum value the mask register can be loaded with is FFFF. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of XXX8. The "blocked" addresses (in this case, the 6th address through the 15th address) are loaded with an address but do not increment once loaded. The counter address will start at address XXX8. With $\overline{\text{CNTINC}}$ asserted LOW, the counter will increment its internal address value till it reaches the mask register value of 3F and wraps around the memory block to location XXX0. Therefore, the counter uses the mask-register to define wrap-around point. The mask register of every port is loaded when $\overline{\text{MKLD}}$ (mask register load) for that port is LOW. When $\overline{\text{MKRD}}$ is LOW, the value of the mask register can be read out on address lines in a manner similar to counter read back operation (see Table 2 for required conditions).

When the burst counter is loaded with an address higher than the mask register value, the higher addresses will form the masked portion of the counter address and are called blocked addresses. The blocked addresses will not be changed or affected by the counter increment operation. The only exception is mask register bit 0. It can be masked to allow the address counter to increment by two. If the mask register bit 0 is loaded with a logic value of "0," then address counter bit 0 is masked and can not be changed during counter increment operation.

Note:

48. The "X" in this diagram represents the counter upper-bits.

If the loaded value for address counter bit 0 is "0," the counter will increment by two and the address values are even. If the loaded value for address counter bit 0 is "1," the counter will increment by two and the address values are odd. This operations allows the user to achieve a 36-bit interface using any two ports, where the counter of one port counts even addresses and the counter of the other port counts odd addresses. This even-odd address scheme stores one half of the 36-bit word in even memory locations, and the other half in odd memory locations. $\overline{\text{CNTINT}}$ will be asserted when the unmasked portion of the counter wraps to all zeros. Loading mask register bit 0 with "1" allows the counter to increment the address value sequentially.

Table 2 groups the operations of the mask register with the operations of the address counter. Address counter and mask register signals are all synchronized to the port's clock CLK. Master reset ($\overline{\text{MRST}}$) is the only asynchronous signal listed on Table 2. Signals are listed based on their priority going from left column to right column with $\overline{\text{MRST}}$ being the highest. A LOW on $\overline{\text{MRST}}$ will reset both counter register to all zeros and mask register to all ones. On the other hand, a LOW on $\overline{\text{CNRST}}$ will only clear the address counter register to zeros and the mask register will remain intact.

There are four operations for the counter and mask register:

1. Load operation: When $\overline{\text{CNTLD}}$ or $\overline{\text{MKLD}}$ is LOW, the address counter or the mask register is loaded with the address value presented at the address lines. This value ranges from 0 to FFFF (64K). The mask register load operation has a higher priority over the address counter load operation.



2. Increment: Once the address counter is loaded with an external address, the counter can internally increment the address value by asserting CNTINC LOW. The counter can address the entire memory array (depend on the value of the mask register) and loop back to location 0. The increment operation is second in priority to load operation.
3. Readback: the internal value of either the burst counter or the mask register can be read out on the address lines when CNTRD or MKRD is LOW. Counter readback has higher priority over mask register readback. A no-operation delay cycle is experienced when readback operation is performed. The address will be valid after t_{CA2} (for counter readback) or t_{CM2} (for mask readback) from the following port's clock rising edge. Address readback operation is independent of the port's chip enables ($\overline{CE}_0$ and $\overline{CE}_1$). If address readback occurs while the port is enabled (chip enables active), the data lines (I/Os) will be three-stated.
4. Hold operation: In order to hold the value of the address counter at certain address, all signals in Table 2 have to be HIGH. This operation has the least priority. This operation is useful in many applications where wait states are needed or when address is available few cycles ahead of data.

The counter and mask register operations are totally independent of port chip enables.

IEEE 1149.1 Serial Boundary Scan (JTAG) and Memory Built-In-Self-Test (MBIST)

The CY7C0430BV incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 3.3V I/O logic levels. It is composed of three input connections and one output connection required by the test logic defined by the standard. Memory BIST circuitry will also be controlled through the TAP interface. All MBIST instructions are compliant to the JTAG standard. An external clock (CLKBIST) is provided to allow the user to run BIST at speeds up to 50 MHz. CLKBIST is multiplexed internally with the ports clocks during BIST operation.

Disabling the JTAG Feature

It is possible to operate the QuadPort without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. CLKBIST must be tied LOW to disable the MBIST. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port (TAP) - Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram (FSM)). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the QuadPort and may be performed while the device is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the QuadPort test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Four-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the following JTAG/BIST Controller diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain devices. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the QuadPort with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the QuadPort. The boundary scan register is loaded with the contents of the QP Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, and SAMPLE/PRELOAD instructions can be used to capture the contents of the Input and Output ring.

**Identification (ID) Register**

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the QuadPort and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Sixteen different instructions are possible with the 4-bit instruction register. All combinations are listed in Table 6, Instruction Codes. Seven of these instructions (codes) are listed as RESERVED and should not be used. The other nine instructions are described in detail below.

The TAP controller used in this QuadPort is fully compliant to the 1149.1 convention. The TAP controller can be used to load address, data or control signals into the QuadPort and can preload the input or output buffers. The QuadPort implements all of the 1149.1 instructions except INTEST. Table 6 lists all instructions.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST allows circuitry external to the QuadPort package to be tested. Boundary-scan register cells at output pins are used to apply test stimuli, while those at input pins capture test results.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the identification register. It also places the identification register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

High-Z

The High-Z instruction causes the bypass register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all QuadPort outputs into a High-Z state.

SAMPLE / PRELOAD

SAMPLE / PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE / PRELOAD instructions loaded into the instruction register and the TAP controller in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the QuadPort clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while

in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the QuadPort signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times. Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins. If the TAP controller goes into the Update-DR state, the sampled data will be updated.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

CLAMP

The optional CLAMP instruction allows the state of the signals driven from QuadPort pins to be determined from the boundary-scan register while the BYPASS register is selected as the serial path between TDI and TDO. CLAMP controls boundary cells to 1 or 0.

RUNBIST

RUNBIST instruction provides the user with a means of running a user-accessible self-test function within the QuadPort as a result of a single instruction. This permits all components on a board that offer the RUNBIST instruction to execute their self-tests concurrently, providing a quick check for the board. The QuadPort MBIST provides two modes of operation once the TAP controller is loaded with the RUNBIST instruction:

Non-Debug Mode (Go-NoGo)

The non-debug mode is a go-nogo test used simply to run BIST and obtain pass-fail information after the test is run. In addition to that, the total number of failures encountered can be obtained. This information is used to aid the debug mode (explained next) of operation. The pass-fail information and failure count is scanned out using the JTAG interface. An MBIST Result Register (MRR) will be used to store the pass-fail results. The MRR is a 25-bit register that will be connected between TDI and TDO during the internal scan (INT_SCAN) operation. The MRR will contain the total number of fail read cycles of the entire MBIST sequence. MRR[0] (bit 0) is the Pass/Fail bit. A "1" indicates some type of failure occurred, and a "0" indicates entire memory pass.

In order to run BIST in non-debug mode, the 2-bit MBIST Control Register (MCR) is loaded with the default value "00", and the TAP controller's finite state machine (FSM), which is synchronous to TCK, transitions to Run Test/Idle state. The entire MBIST test will be performed with a deterministic number of TCK cycles depending on the TCK and CLKBIST frequency.

$$t_{CYC} = \frac{t_{CYC}[\text{CLKBIST}]}{t_{CYC}[\text{TCK}]} \times m + \text{SPC}$$

t_{CYC} is total number of TCK cycles required to run MBIST.

SPC is the Synchronization Padding Cycles (4–6 cycles)



m is a constant represents the number of read and write operations required to run MBIST algorithms (31195136).

Once the entire MBIST sequence is completed, supplying extra TCK or CLKBISt cycles will have no effect on the MBIST controller state or the pass-fail status.

Debug Mode

With the RUNBISt instruction loaded and the MCR loaded with the value of "01", and the FSM transitions to RUN_TEST/IDLE state, the MBIST goes into RUNBISt-debug mode. The debug mode will be used to provide complete failure analysis information at the board level. It is recommended that the user runs the non-debug mode first and then the debug mode in order to save test time and to set an upper bound on the number of scan outs that will be needed. The failure data will be scanned out automatically once a failure occurs using the JTAG TAP interface. The failure data will be represented by a 100-bit packet given below. The 100-bit Memory debug Register (MDR) will be connected between TDI and TDO, and will be shifted out on TDO, which is synchronized to TCK.

Figure 3 is a representation of the 100-bit MDR packet. The packet follows a 2-bit header that has a logic "1" value, and represents two TCK cycles. MDR[97:26] represent the BIST comparator values of all four ports (each port has 18 data lines). A value of "1" indicates a bit failure. The scanned out data is from LSB to MSB. MDR[25:10] represent the failing address (MSB to LSB). The state of the BIST controller is scanned out using MDR[9:4]. Bit 2 is the Test Done bit. A "0" in bit 2 means test not complete. The user has to monitor this

bit at every packet to determine if more failure packets need to be scanned out at the end of the BIST operations. If the value is "0" then BIST must be repeated to capture the next failing packet. If it is "1," it means that the last failing packets have been scanned out. A trailer similar to the header represents the end of a packet.

MCR_SCAN

This instruction will connect the Memory BIST Control Register (MCR) between TDI and TDO. The default value (upon master reset) is "00". Shift_DR state will allow modifying the MCR to extend the MBIST functionality.

MBIST Control States

Thirty-five states are listed in Table 7. Four data algorithms are used in debug mode: moving inversion (MIA), march_2 (M2A), checkerboard (CBA), and unique address algorithm (UAA). Only Port 1 can write MIA, M2A, and CBA data to the memory. All four ports can read any algorithm data from the QP memory. Ports 2, 3, and 4 will only write UAA data.

Boundary Scan Cells (BSC)

Table 9 lists all QuadPort I/Os with their associated BSC. Notice that the cells have even numbers. Every I/O has two boundary scan cells. Bidirectional signals (address lines, data-lines) require two cells so that one (the odd cell) is used to control a three-state buffer. Input only and output only signals have an extra dummy cell (odd cells) that are used to ease device layout.

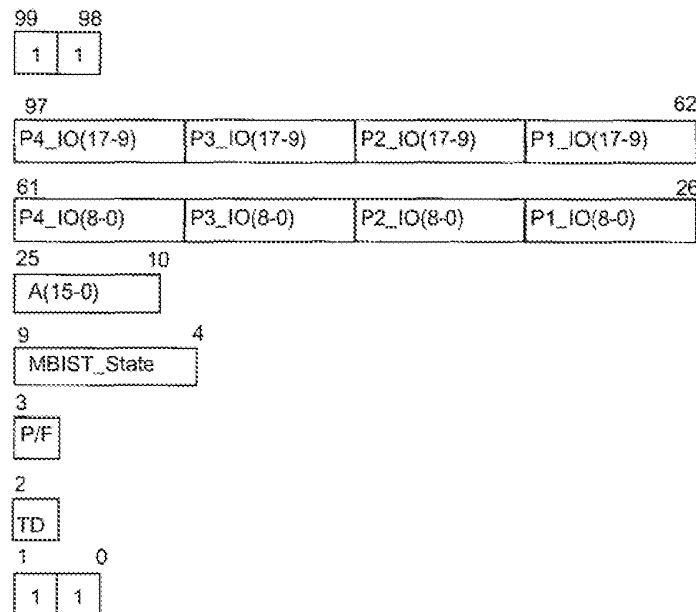
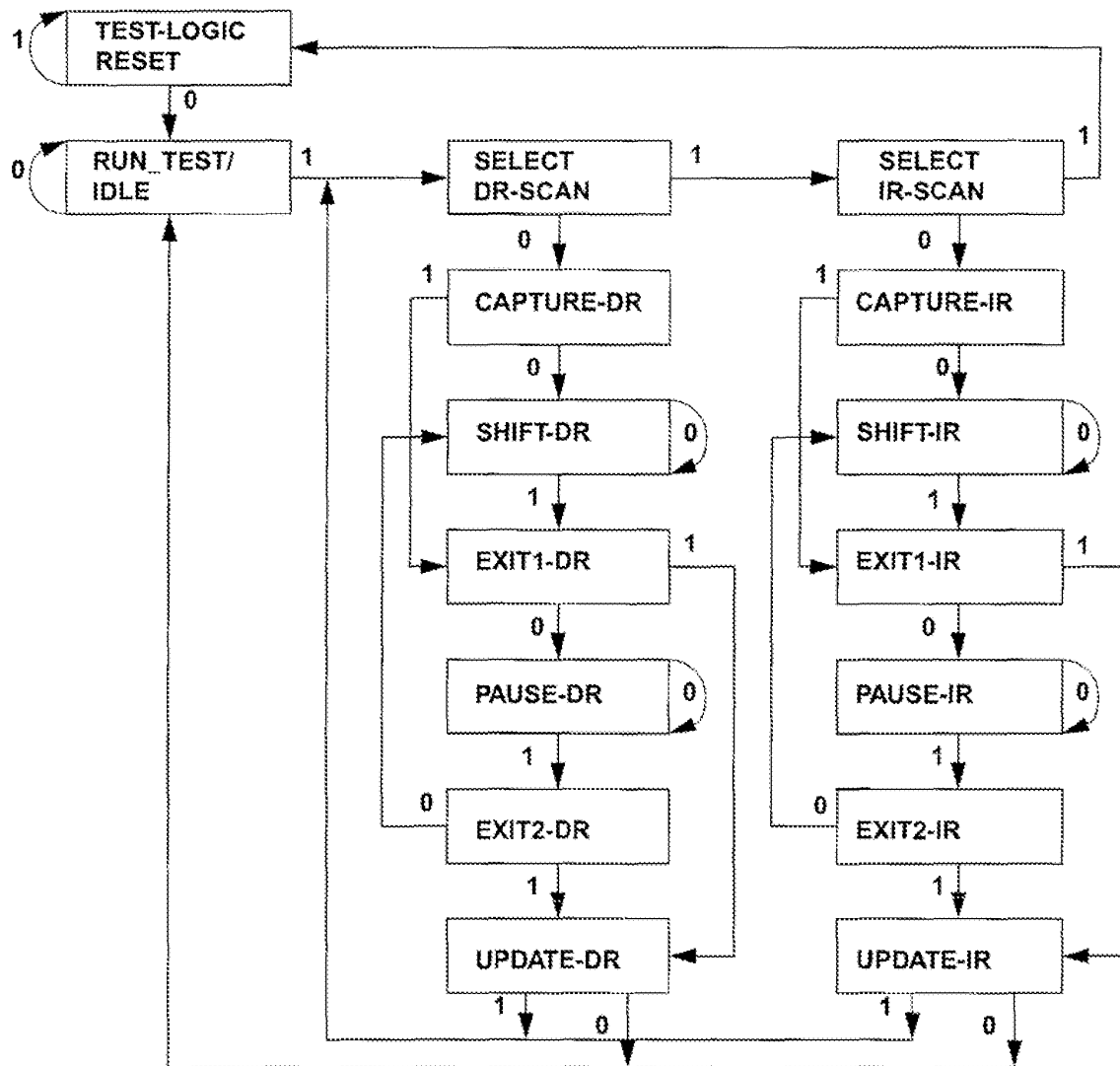


Figure 3. MBIST Debug Register Packet

TAP Controller State Diagram (FSM)^[49]**Note:**

49. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.



JTAG/BIST TAP Controller Block Diagram

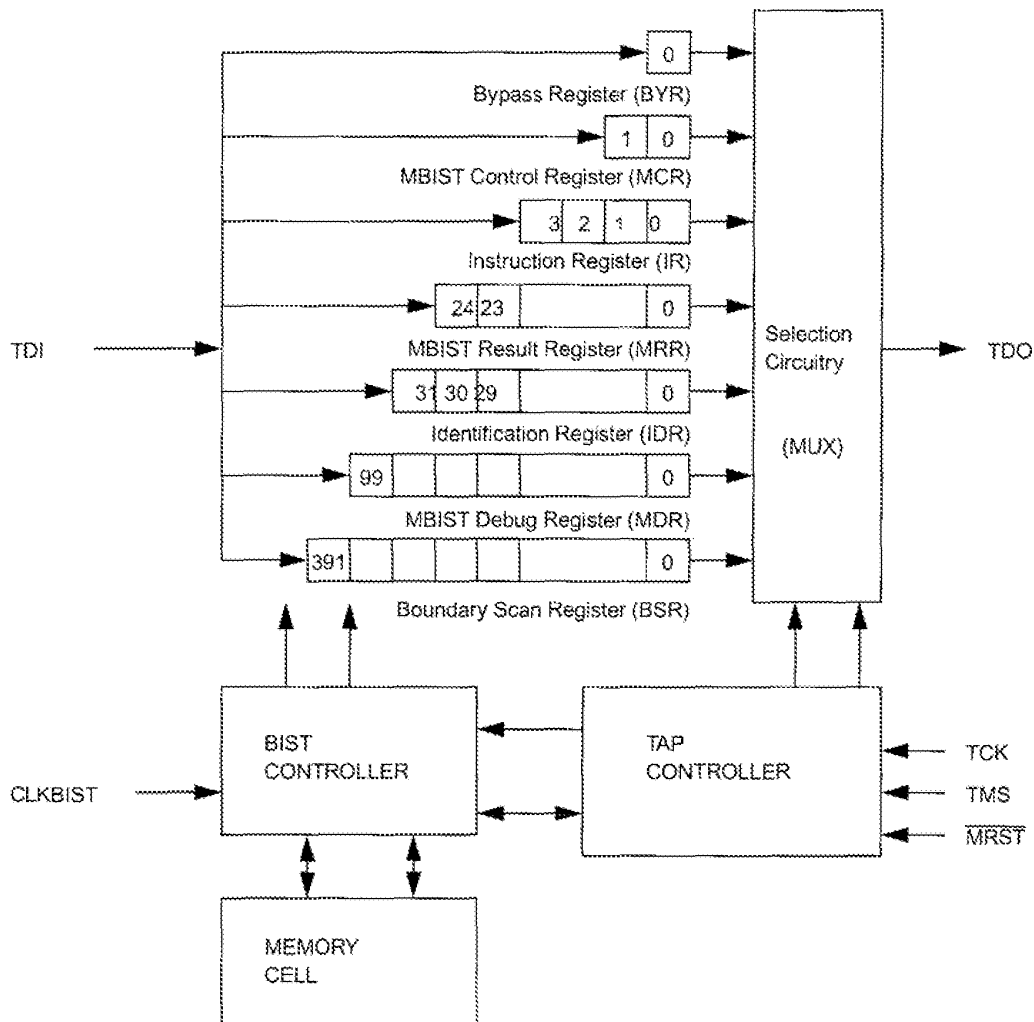


Table 4. Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	1h	Reserved for version number
Cypress Device ID (27:12)	C000h	Defines Cypress part number
Cypress JEDEC ID (11:1)	34h	Allows unique identification of QuadPort vendor
ID Register Presence (0)	1	Indicate the presence of an ID register



Table 5. Scan Registers Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
MBIST Control (MCR)	2
MBIST Result (MRR)	25
MBIST Debug (MDR)	100
Boundary Scan (BSR)	392

Table 6. Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the Input/Output ring contents. Places the boundary scan register (BSR) between the TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0111	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0110	Places the BYR between TDI and TDO. Forces all QuadPort output drivers to a High-Z state.
CLAMP	0101	Controls boundary to 1/0. Uses BYR.
SAMPLE/PRELOAD	0001	Captures the Input/Output ring contents. Places the boundary scan register (BSR) between TDI and TDO.
RUNBIST	1000	Invokes MBIST. Places the MBIST Debug register (MDR) between TDI and TDO.
INT_SCAN	0010	Scans out pass-fail information. Places MBIST Result Register (MRR) between TDI and TDO.
MCR_SCAN	0011	Presets RUNBIST mode. Places MBIST Control Register (MCR) between TDI and TDO.
RESERVED	All other codes	Seven combinations are reserved. Do not use other than the above.

Table 7. MBIST Control States

States Code	State Name	Description
000001	movi_zeros	Port 1 write all zeros to the QP memory using Moving Inversion Algorithm (MIA).
000011	movi_1_upcnt	Up count from 0 to 64K (depth of QP). All ports read 0s, then Port 1 writes 1s to all memory locations using MIA, then all ports read 1s. MIA read0_write1_read1 (MIA_r0w1r1).
000010	movi_0_upcnt	Up count from 0 to 64K. All ports read 1s, then Port 1 writes 0s, then all ports read 0s (MIA_r1w0r0).
000110	movi_1_downcnt	Down count from 64K to 0. MIA_r0w1r1.
000111	movi_0_downcnt	Down count MIA_r1w0r0.
000101	movi_read	Read all 0s.
000100	mar2_zeros	Port 1 write all zeros to memory using March2 Algorithm (M2A).
001100	mar2_1_upcnt	Up count M2A_r0w1r1.



Table 7. MBIST Control States (continued)

States Code	State Name	Description
001101	mar2_0_upcnt	Up count M2A_r1w0r0.
001111	mar2_1_downcnt	Down count M2A_r0w1r1.
001110	mar2_0_downcnt	Down count M2A_r1w0r0.
001010	mar2_read	Read all 0s.
001011	chkr_w	Port 1 writes topological checkerboard data to memory.
001001	chkr_r	All ports read topological checkerboard data.
001000	n_chkr_w	Port 1 write inverse topological checkerboard data.
011000	n_chkr_r	All ports read inverse topological checkerboard data.
011001	uaddr_zeros2	Port 2 write all zeros to memory using Unique Address Algorithm (UAA).
011011	uaddr_write2	Port 2 writes every address value into its memory location (UAA).
011010	uaddr_read2	All ports read UAA data.
011110	uaddr_ones2	Port 2 writes all ones to memory.
011111	n_uaddr_write2	Port 2 writes inverse address value into memory.
011101	n_uaddr_read2	All ports read inverse UAA data.
011001	uaddr_zeros3	Port 3 write all zeros to memory using Unique Address Algorithm (UAA).
011011	uaddr_write3	Port 3 writes every address value into its memory location (UAA).
011010	uaddr_read3	All ports read UAA data.
011110	uaddr_ones3	Port 3 writes all ones to memory.
011111	n_uaddr_write3	Port 3 writes inverse address value into memory.
011101	n_uaddr_read3	All ports read inverse UAA data.
011001	uaddr_zeros4	Port 4 write all zeros to memory using Unique Address Algorithm (UAA).
011011	uaddr_write4	Port 4 writes every address value into its memory location (UAA).
011010	uaddr_read4	All ports read UAA data.
011110	uaddr_ones4	Port 4 writes all ones to memory.
011111	n_uaddr_write4	Port 4 writes inverse address value into memory.
011101	n_uaddr_read4	All ports read inverse UAA data.
110010	complete	Test complete.

Table 8. MBIST Control Register (MCR)

MCR[1:0]	Mode
00	Non-Debug
01	Debug
10	Reserved
11	Reserved



Table 9. Boundary Scan Order

Cell #	Signal Name	Bump (Ball) ID
2	A0_P4	K20
4	A1_P4	J19
6	A2_P4	J18
8	A3_P4	H20
10	A4_P4	H19
12	A5_P4	G19
14	A6_P4	G18
16	A7_P4	F20
18	A8_P4	F19
20	A9_P4	F18
22	A10_P4	E20
24	A11_P4	E19
26	A12_P4	D19
28	A13_P4	D18
30	A14_P4	C20
32	A15_P4	C19
34	CNTINT_P4	F17
36	CNTRST_P4	K18
38	MKLD_P4	H18
40	CNTLD_P4	H17
42	CNTINC_P4	G17
44	CNTRD_P4	E17
46	MKRD_P4	E18
48	LB_P4	A20
50	UB_P4	B19
52	OE_P4	D17
54	R/W_P4	C16
56	CE1_P4	C18
58	CE0_P4	C17
60	INT_P4	K19
62	CLK_P4	K17
64	A0_P3	L20
66	A1_P3	M19
68	A2_P3	M18
70	A3_P3	N20
72	A4_P3	N19
74	A5_P3	P19
76	A6_P3	P18
78	A7_P3	R20
80	A8_P3	R19
82	A9_P3	R18

Table 9. Boundary Scan Order (continued)

Cell #	Signal Name	Bump (Ball) ID
84	A10_P3	T20
86	A11_P3	T19
88	A12_P3	U19
90	A13_P3	U18
92	A14_P3	V20
94	A15_P3	V19
96	CNTINT_P3	R17
98	CNTRST_P3	L18
100	MKLD_P3	N18
102	CNTLD_P3	N17
104	CNTINC_P3	P17
106	CNTRD_P3	T17
108	MKRD_P3	T18
110	LB_P3	Y20
112	UB_P3	W19
114	OE_P3	U17
116	R/W_P3	V16
118	CE1_P3	V18
120	CE0_P3	V17
122	INT_P3	L19
124	CLK_P3	M17
126	IO0_P4	Y15
128	IO1_P4	W15
130	IO2_P4	Y16
132	IO3_P4	W16
134	IO4_P4	Y17
136	IO5_P4	W17
138	IO6_P4	Y18
140	IO7_P4	W18
142	IO8_P4	Y19
144	IO0_P3	V12
146	IO1_P3	Y11
148	IO2_P3	W12
150	IO3_P3	Y12
152	IO4_P3	W13
154	IO5_P3	Y13
156	IO6_P3	V15
158	IO7_P3	Y14
160	IO8_P3	W14
162	IO0_P1	Y6
164	IO1_P1	W6



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CY7C0430BV

Table 9. Boundary Scan Order (continued)

Cell #	Signal Name	Bump (Ball) ID
166	IO2_P1	Y5
168	IO3_P1	W5
170	IO4_P1	Y4
172	IO5_P1	W4
174	IO6_P1	Y3
176	IO7_P1	W3
178	IO8_P1	Y2
180	IO0_P2	V9
182	IO1_P2	Y10
184	IO2_P2	W9
186	IO3_P2	Y9
188	IO4_P2	W8
190	IO5_P2	Y8
192	IO6_P2	V6
194	IO7_P2	Y7
196	IO8_P2	W7
198	A0_P2	L1
200	A1_P2	M2
202	A2_P2	M3
204	A3_P2	N1
206	A4_P2	N2
208	A5_P2	P2
210	A6_P2	P3
212	A7_P2	R1
214	A8_P2	R2
216	A9_P2	R3
218	A10_P2	T1
220	A11_P2	T2
222	A12_P2	U2
224	A13_P2	U3
226	A14_P2	V1
228	A15_P2	V2
230	CNTINT_P2	R4
232	CNTRST_P2	L3
234	MKLD_P2	N3
236	CNTLD_P2	N4
238	CNTINC_P2	P4
240	CNTRD_P2	T4
242	MKRD_P2	T3
244	LB_P2	Y1
246	UB_P2	W2

Table 9. Boundary Scan Order (continued)

Cell #	Signal Name	Bump (Ball) ID
248	OE_P2	U4
250	R/W_P2	V5
252	CE1_P2	V3
254	CE0_P2	V4
256	INT_P2	L2
258	CLK_P2	M4
260	A0_P1	K1
262	A1_P1	J2
264	A2_P1	J3
266	A3_P1	H1
268	A4_P1	H2
270	A5_P1	G2
272	A6_P1	G3
274	A7_P1	F1
276	A8_P1	F2
278	A9_P1	F3
280	A10_P1	E1
282	A11_P1	E2
284	A12_P1	D2
286	A13_P1	D3
288	A14_P1	C1
290	A15_P1	C2
292	CNTINT_P1	F4
294	CNTRST_P1	K3
296	MKLD_P1	H3
298	CNTLD_P1	H4
300	CNTINC_P1	G4
302	CNTRD_P1	E4
304	MKRD_P1	E3
306	LB_P1	A1
308	UB_P1	B2
310	OE_P1	D4
312	R/W_P1	C5
314	CE1_P1	C3
316	CE0_P1	C4
318	INT_P1	K2
320	CLK_P1	K4
322	IO9_P2	A6
324	IO10_P2	B6
326	IO11_P2	A5
328	IO12_P2	B5



Table 9. Boundary Scan Order (continued)

Cell #	Signal Name	Bump (Ball) ID
330	IO13_P2	A4
332	IO14_P2	B4
334	IO15_P2	A3
336	IO16_P2	B3
338	IO17_P2	A2
340	IO9_P1	C9
342	IO10_P1	A10
344	IO11_P1	B9
346	IO12_P1	A9
348	IO13_P1	B8
350	IO14_P1	A8
352	IO15_P1	C6
354	IO16_P1	A7
356	IO17_P1	B7
358	IO9_P3	A15
360	IO10_P3	B15
362	IO11_P3	A16
364	IO12_P3	B16
366	IO13_P3	A17
368	IO14_P3	B17
370	IO15_P3	A18
372	IO16_P3	B18
374	IO17_P3	A19
376	IO9_P4	C12
378	IO10_P4	A11
380	IO11_P4	B12
382	IO12_P4	A12
384	IO13_P4	B13
386	IO14_P4	A13
388	IO15_P4	C15
390	IO16_P4	A14
392	IO17_P4	B14



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CY7C0430BV

Ordering Information

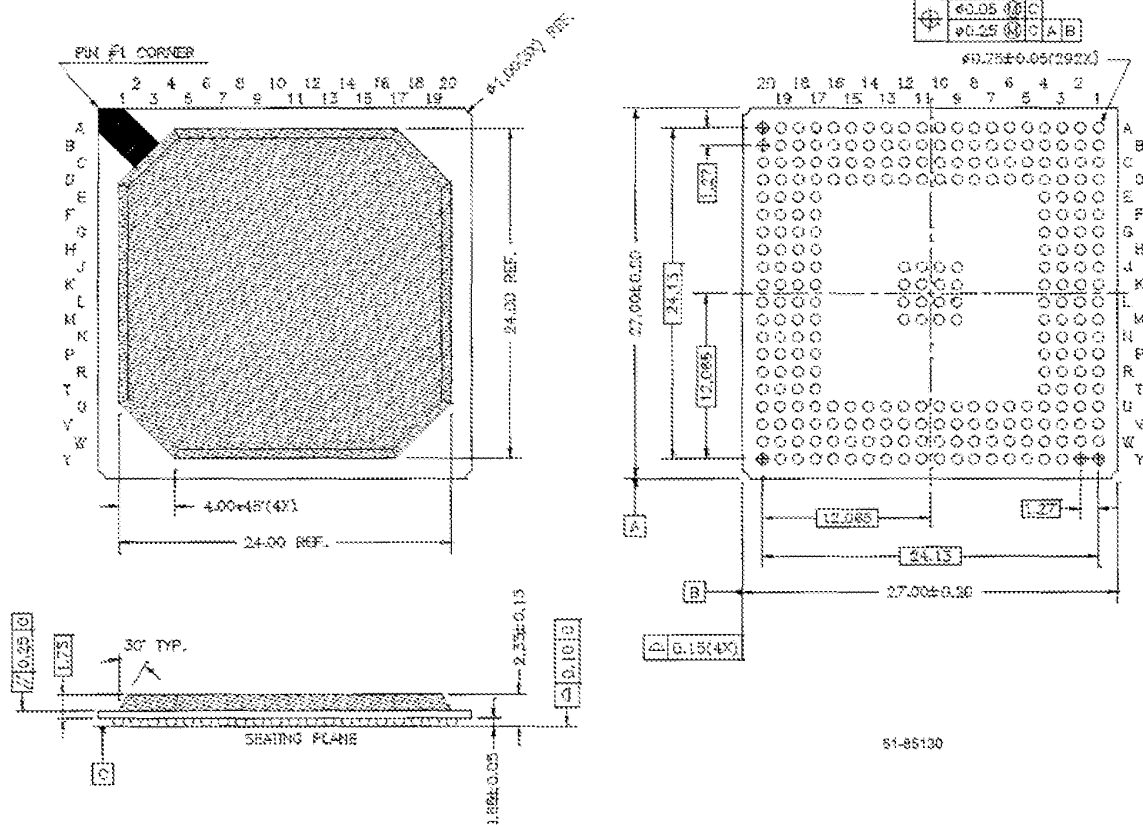
64K x 18 3.3V Synchronous QuadPort SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CY7C0430BV-133BGC	BG272	272-Ball Grid Array (BGA)	Commercial
	CY7C0430BV-133BGI	BG272	272-Ball Grid Array (BGA)	Industrial
100	CY7C0430BV-100BGC	BG272	272-Ball Grid Array (BGA)	Commercial
	CY7C0430BV-100BGI	BG272	272-Ball Grid Array (BGA)	Industrial

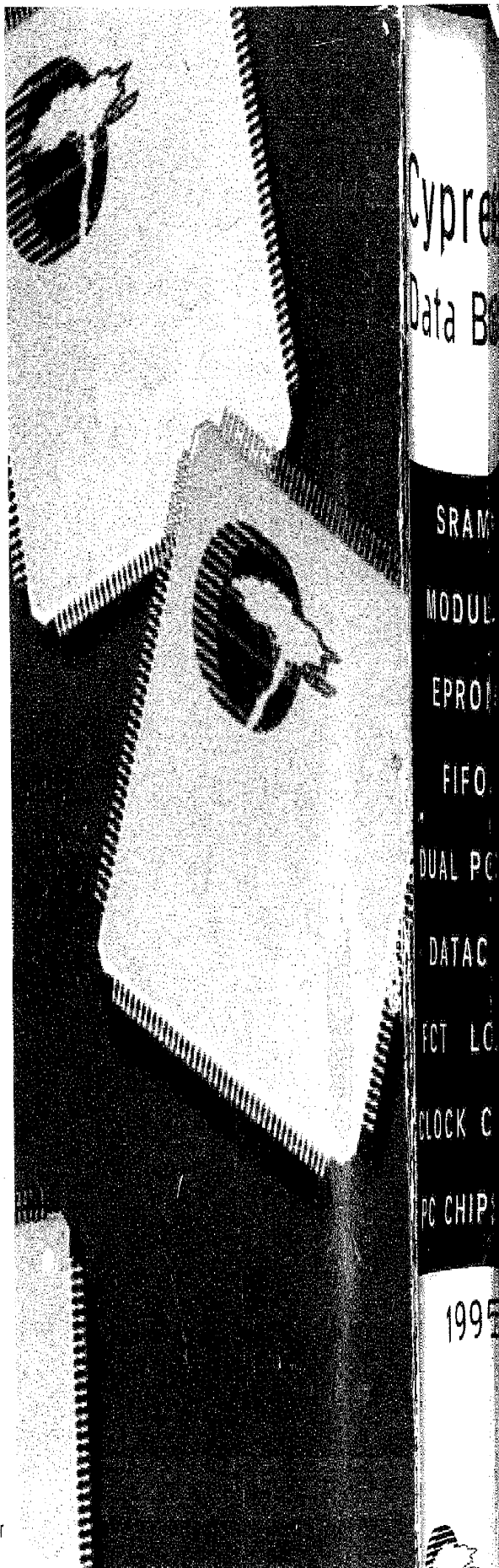
Document #: 38-01052-°C

Package Diagram

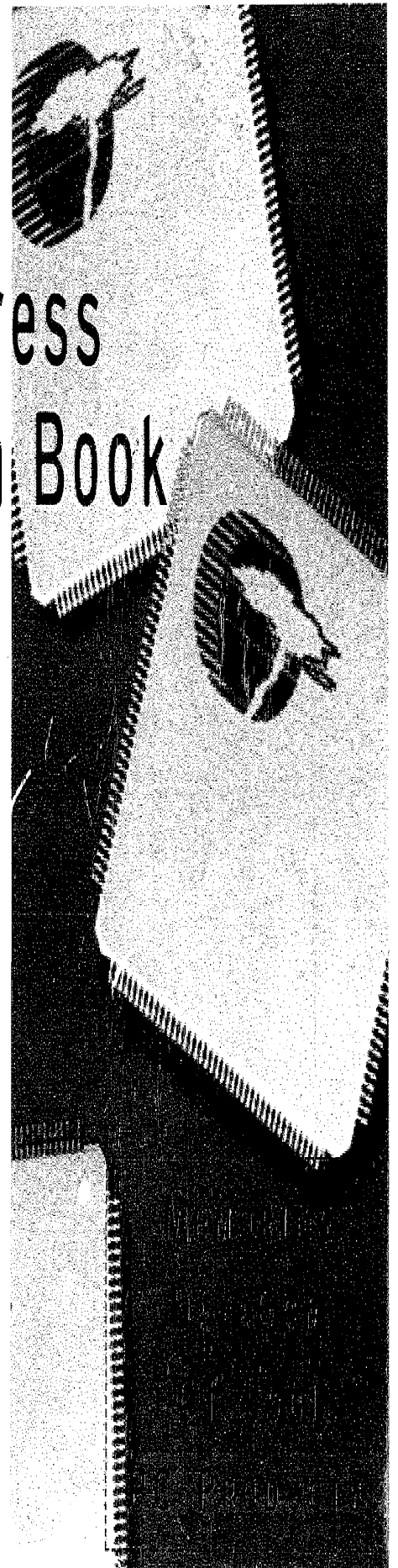
272-Lead Ball Grid Array (27 x 27 x 2.33 mm) BG272



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Cypress Data Book



Cypress Semiconductor
3901 North First Street



PRELIMINARY
CY7C006
CY7C016

16K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- CMOS for optimum speed/power
- High-speed access
—15 ns (commercial)
- Low operating power: 140 mW (typ.)
- Automatic power-down
- Fully asynchronous operation
- Master/slave select pin allows bus width expansion to 16/18 bits or more
- Busy arbitration scheme provided
- Semaphores included to permit software handshaking between ports
- INT flag for port-to-port communication
- Available in 68-pin PLCC; 80-pin (CY7C016) and 64-pin (CY7C006) TQFP
- TTL compatible
- Capable of withstanding greater than 20kV ESD
- Pin compatible and functional equivalent to TDT7006 and TDT7016

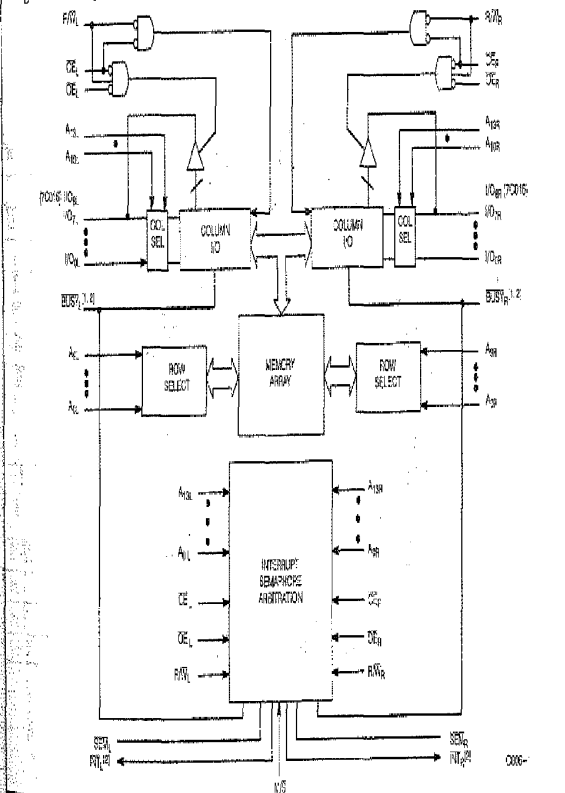
Functional Description

The CY7C006 and CY7C016 are high-speed CMOS 16K x 8 and 16K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7C006/016 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C006/016 can be utilized as a standalone 128-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16-/18-bit or wider master/slave dual-port static RAM. An MS pin is provided for implementing 16-/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable (CE), read or write enable (RW), and output enable (OE). Two flags, BUSY and INT, are provided on each port. BUSY signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag (INT) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-downs feature is controlled independently on each port by a chip enable (CE) pin or SEM pin.

The CY7C006 and CY7C016 are available in 68-pin PLCCs, and 80-pin (CY7C016) TQFP and 64-pin (CY7C006) TQFP.

Logic Block Diagram



Notes:

1. BUSY is an output in master mode, and an input in slave mode.
2. Master, post-pull output and requires no pull-up resistor.

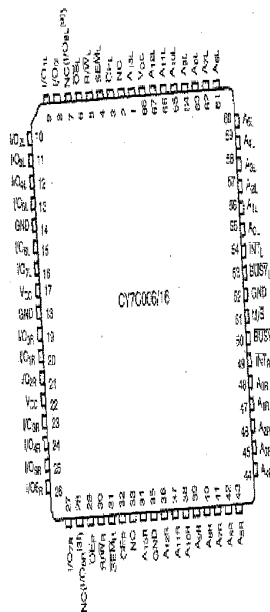


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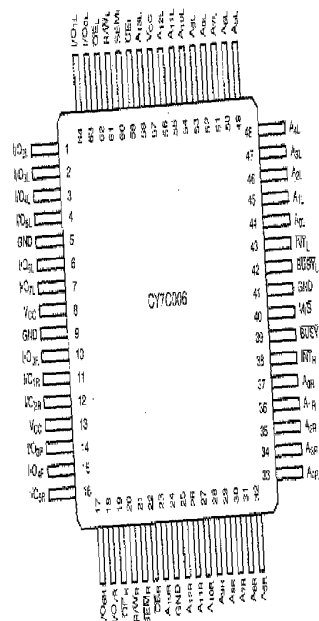
CY7C006
CY7C016

Pin Configurations

64-Pin LCC/PLCC
Top View



64-Pin TQFP
Top View



Note:
3. I/O for 7C016 only.

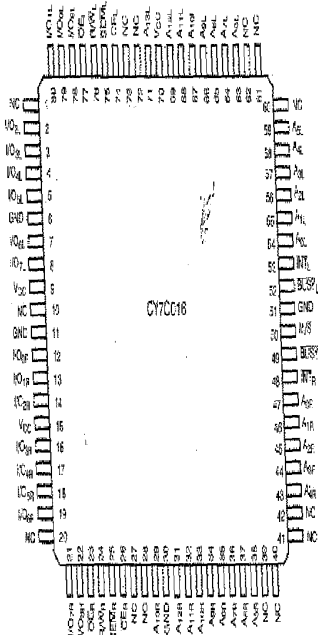


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CY7C006
CY7C016

Pin Configurations (continued)

96-Pin TQFP
Top View



006-4

Pin Definitions

Left Port	Right Port	Description
$\overline{IO}_L$ - $\overline{IO}_L$	$\overline{IO}_R$ - $\overline{IO}_R$	Data Bus Input/Output
$\overline{A}_L$ - $\overline{A}_L$	$\overline{A}_R$ - $\overline{A}_R$	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$\overline{WE}_L$	$\overline{WE}_R$	Read/Write Enable
$\overline{SEN}_L$	$\overline{SEN}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The $\overline{IO}_0$ pin is used when writing to 2 semaphores. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 3FFF and is cleared when left port reads location 3FFF. $\overline{INT}_R$ is set when left port writes location 3FFF and is cleared when right port reads location 3FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$\overline{MS}$		Master or Slave Select
V_{CC}		Power
$\overline{GND}$		Ground

Selection Guide

	7C006-15 7C016-15	7C006-25 7C016-25	7C006-35 7C016-35	7C006-55 7C016-55
Maximum Access Time (ns)	15	25	35	55
Maximum Operating Current (mA)	260	220	210	200
Maximum Standby Current for I_{KM} (mA)	70	60	50	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs in High Z State -0.5V to $+7.0\text{V}$

DC Input Voltage⁽¹⁾ -0.5V to $+7.0\text{V}$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage $>200\text{V}$
(per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{mA}$

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Industrial	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Notes:

4. Pulse width $< 20\text{ ns}$.

Electrical Characteristics Over the Operating Range⁽⁵⁾

Parameter	Description	Test Conditions	7C006-15 7C016-15			7C006-25 7C016-25			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4			2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 4.0 mA			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2			2.2			V
V _{IL}	Input LOW Voltage				0.8			0.8	V
I _{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$	-10		+10	-10		+10	μA
I _{OZ}	Output Leakage Current	Outputs Disabled, GND $\leq V_O \leq V_{CC}$	-10		+10	-10		+10	μA
I _{CC}	Operating Current	V _{CC} = Max., I _{OUP} = 0 mA Outputs Disabled	Com ¹	170	260	160	220		mA
I _{BM}	Standby Current (Both Ports TTL Levels)	CE _L and CE _R $\geq V_{IH}$ f = f _{MAX} ⁽⁶⁾	Com ¹	50	70	40	60		mA
			Ind			40	75		
I _{BS}	Standby Current (One Port TTL Level)	CE _L or CE _R $\geq V_{IH}$ f = f _{MAX} ⁽⁶⁾	Com ¹	110	170	90	130		mA
			Ind			90	150		
I _{BS}	Standby Current (Both Ports CMOS Levels)	Both Ports CE and CE _R $\geq V_{CC} - 0.2\text{V}$ V _{IN} $\geq V_{CC} - 0.2\text{V}$ or V _{IN} $\leq 0.2\text{V}$, f = 0 ⁽⁶⁾	Com ¹	3	15	3	15		mA
			Ind			3	15		
I _{BS}	Standby Current (One Port CMOS Level)	One Port CE _L or CE _R $\geq V_{CC} - 0.2\text{V}$ V _{IN} $\geq V_{CC} - 0.2\text{V}$ or V _{IN} $\leq 0.2\text{V}$, Active Port Outputs, f = f _{MAX} ⁽⁶⁾	Com ¹	100	130	80	120		mA
			Ind			80	130		

Parameter	Description	Test Conditions	7C006-25 7C016-25			7C006-35 7C016-35			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4			2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 4.0 mA			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2			2.2			V
V _{IL}	Input LOW Voltage				0.8			0.8	V
I _{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$	-10		+10	-10		+10	μA
I _{OZ}	Output Leakage Current	Outputs Disabled, GND $\leq V_O \leq V_{CC}$	-10		+10	-10		+10	μA
I _{CC}	Operating Current	V _{CC} = Max., I _{OUP} = 0 mA Outputs Disabled	Com ¹	150	210	140	200		mA
I _{BM}	Standby Current (Both Ports TTL Levels)	CE _L and CE _R $\geq V_{IH}$ f = f _{MAX} ⁽⁶⁾	Com ¹	30	50	20	40		mA
			Ind			20	55		
I _{BS}	Standby Current (One Port TTL Level)	CE _L or CE _R $\geq V_{IH}$ f = f _{MAX} ⁽⁶⁾	Com ¹	80	120	70	100		mA
			Ind			70	115		
I _{BS}	Standby Current (Both Ports CMOS Levels)	Both Ports CE and CE _R $\geq V_{CC} - 0.2\text{V}$ V _{IN} $\geq V_{CC} - 0.2\text{V}$ or V _{IN} $\leq 0.2\text{V}$, f = 0 ⁽⁶⁾	Com ¹	3	15	3	15		mA
			Ind			3	15		
I _{BS}	Standby Current (One Port CMOS Level)	One Port CE _L or CE _R $\geq V_{CC} - 0.2\text{V}$ V _{IN} $\geq V_{CC} - 0.2\text{V}$ or V _{IN} $\leq 0.2\text{V}$, Active Port Outputs, f = f _{MAX} ⁽⁶⁾	Com ¹	70	100	60	90		mA
			Ind			60	95		

Notes:

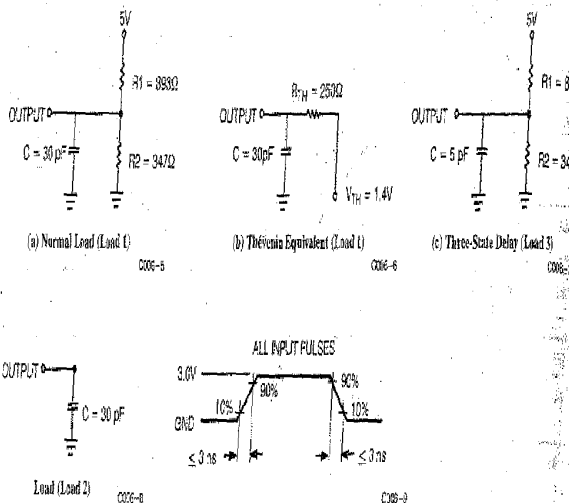
5. See the last page of this specification for Group A subgroup testing information.

6. f_{MAX} = 100c. All inputs cycling at f = 100c (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{BS}.

Capacitance⁽⁷⁾

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz	10	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0V	10	pF

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range^(5,8)

Parameter	Description	7C006-15 7C016-15		7C006-25 7C016-25		7C006-35 7C016-35		7C006-55 7C016-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	15		25		35		55		ns
t _{AA}	Address to Data Valid		15		25		35		55	ns
t _{OHA}	Output Hold From Address Change	3		3		3		3		ns
t _{ACE}	CE LOW to Data Valid		15		25		35		55	ns
t _{DCE}	OE LOW to Data Valid		10		15		20		25	ns
t _{LZOE} ^(9,10)	OE Low to Low Z	3		3		3		3		ns
t _{HZOE} ^(9,10)	OE HIGH to High Z		10		15		15		25	ns
t _{LZCE} ^(9,10)	CE LOW to Low Z	3		3		3		3		ns
t _{HZCE} ^(9,10)	CE HIGH to High Z		10		15		15		25	ns
t _{PC}	CE LOW to Power-Up	0		0		0		0		ns
t _{PD}	CE HIGH to Power-Down		15		25		35		55	ns

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 1.5V input, pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}, I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage conditions for any given device, t_{ACE} is less than t_{LZOE} and t_{HZOE} is less than t_{LZCE}.
- Test conditions used are Load 3.

Switching Characteristics Over the Operating Range^(5,8) (continued)

Parameter	Description	7C006-15 7C016-15		7C006-25 7C016-25		7C006-35 7C016-35		7C006-55 7C016-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t _{WC}	Write Cycle Time	15		25		35		55		ns
t _{DCE}	CE LOW to Write End	12		20		30		45		ns
t _{AW}	Address Set-Up to Write End	12		20		30		45		ns
t _{HA}	Address Hold From Write End	2		2		2		2		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	Write Pulse Width	12		20		25		40		ns
t _{SD}	Data Set-Up to Write End	10		15		15		25		ns
t _{HD} ⁽¹¹⁾	Data Hold From Write End	0		0		0		0		ns
t _{RWZ} ⁽¹²⁾	R/W LOW to High Z		10		15		20		25	ns
t _{LWZ} ⁽¹²⁾	R/W HIGH to Low Z	3		3		3		3		ns
t _{WD} ⁽¹²⁾	Write Pulse to Data Delay	30		50		60		80		ns
t _{WDV} ⁽¹²⁾	Write Data Valid to Read Data Valid	25		30		35		50		ns
BUSY TIMING ⁽¹³⁾										
t _{BLA}	BUSY LOW from Address Match		15		20		20		30	ns
t _{BLA}	BUSY HIGH from Address Mismatch		15		20		20		30	ns
t _{ALC}	BUSY LOW from CE LOW		15		20		20		30	ns
t _{ALC}	BUSY HIGH from CE HIGH		15		17		25		30	ns
t _{PS}	Port Set-Up for Priority	5		5		5		5		ns
t _{WB}	R/W LOW after BUSY LOW	0		0		0		0		ns
t _{WB}	R/W HIGH after BUSY HIGH	13		17		25		30		ns
t _{WDV} ⁽¹⁴⁾	BUSY HIGH to Data Valid		Note 14		Note 14		Note 14		Note 14	ns
INTERRUPT TIMING ⁽¹⁵⁾										
t _{INT}	INT Set Time		15		25		25		30	ns
t _{INT}	INT Reset Time		15		25		25		30	ns
SEMAPHORE TIMING										
t _{SEP}	SEM Flag Update Pulse (OE or SEM)	10		10		15		20		ns
t _{WRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t _{SES}	SEM Flag Contention Window	5		5		5		5		ns

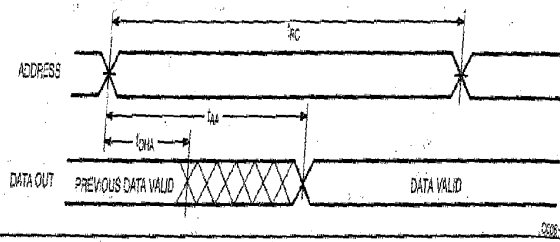
Notes:

- Must be met by the device writing to the RAM under all operating conditions.
- Test conditions used are Load 2.
- t_{WDV} is a calculated parameter and is the greater of t_{WD} - t_{PWE} (actual) or t_{WB} - t_{PS} (actual).
- For information on on-chip delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.

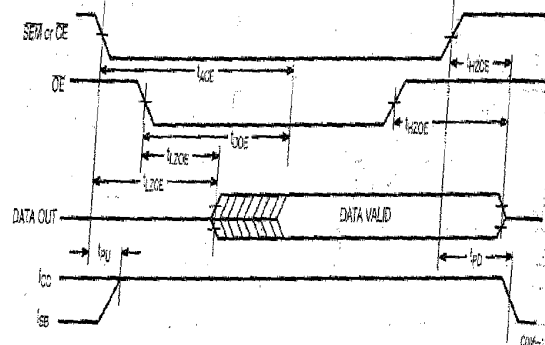


Switching Waveforms

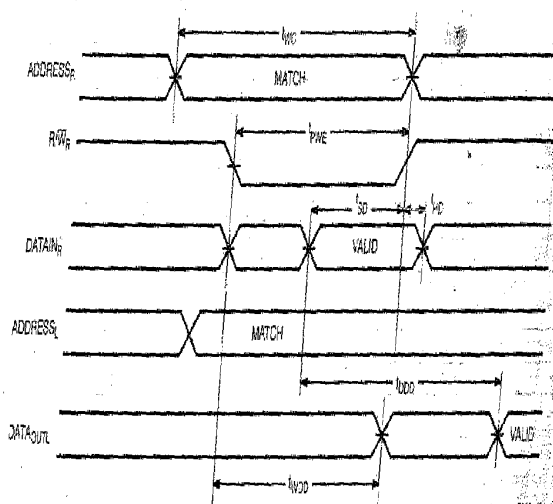
Read Cycle No. 1 (Either Port Address Access) [21, 22, 23]



Read Cycle No. 2 (Either Port CE/OE Access) [23, 23, 23]



Read Timing with Port-to-Port Delay ($M/S = L$) [23, 23]

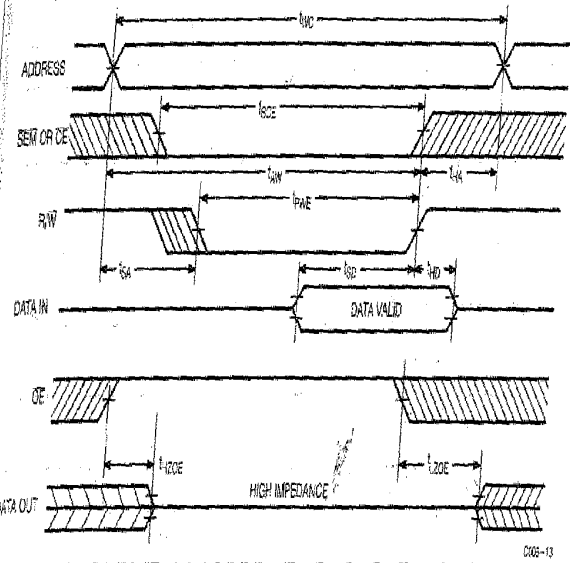


Notes

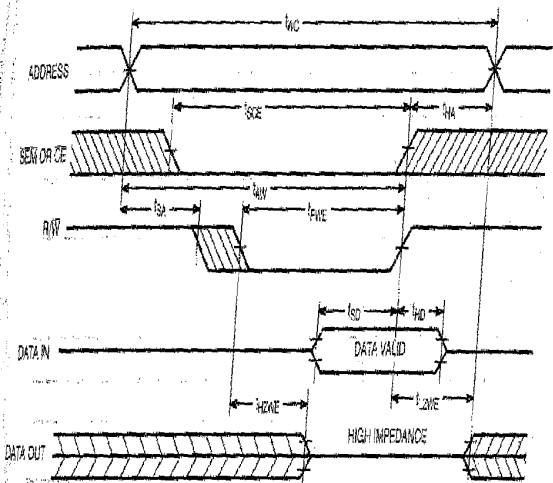
15. R/W is HIGH for read cycle.
16. Device is continuously selected $CE = LOW$ and $OE = LOW$. This waveform cannot be used for the semaphore reads.
17. Address valid prior to or coincident with CE transition LOW.
18. $CE_L = L$, $SEM = H$ when accessing RAM. $CE = H$, $SEM = L$ when accessing semaphores.
19. $BUSY = HIGH$ for the writing port.
20. $CE_L = CE_R = LOW$.

Switching Waveforms (continued)

Write Cycle No. 1: OE Three-State Data I/Os (Either Port) [21, 22, 23]

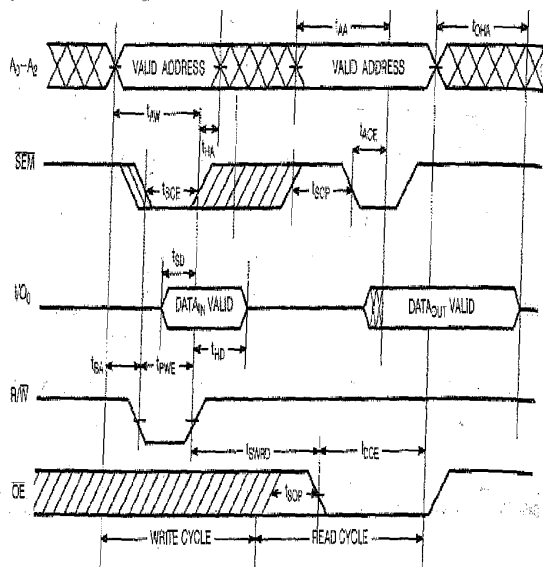


Write Cycle No. 2: R/W Three-State Data I/Os (Either Port) [21, 23, 24]

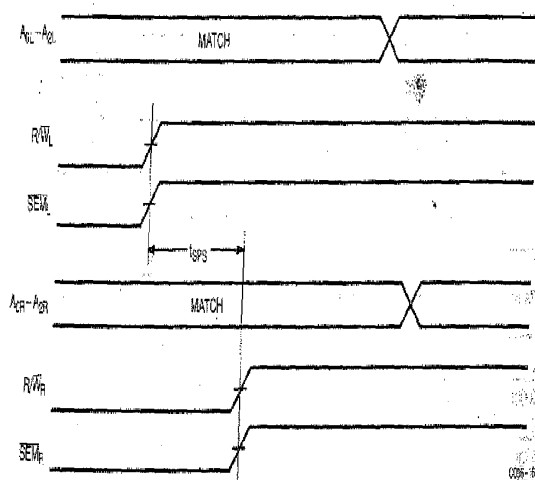


Notes

21. The internal write time of the memory is defined by the overlap of CE or SEM LOW and R/W LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{W2} or $(t_{W2W} + t_{SD})$ to allow the I/O devices to turn off, and data to be placed on the bus for the required t_{SD}. If OE is HIGH during a R/W controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{W2}.
23. R/W must be HIGH during all address transitions.
24. Data I/O pins enter high impedance when OE is held LOW during write.

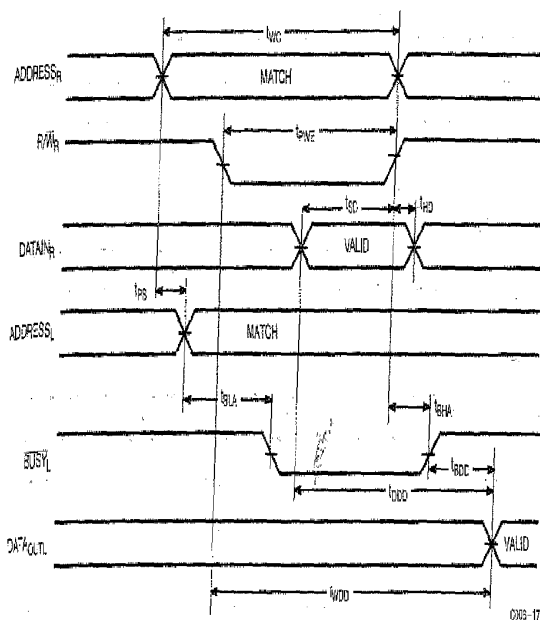
Semaphores Read After Write Timing, Either Side^[25]

276-4

Semaphore Contention^[26, 27, 28]

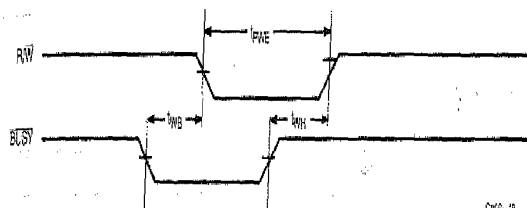
035-7

Read with $\overline{\text{BUSY}} (\text{M}/\overline{\text{S}} = \text{HIGH})^{[20]}$



0206-12

Write Timing with Busy Input ($M/\bar{S} = \text{LOW}$)



0266-3091

Notes:

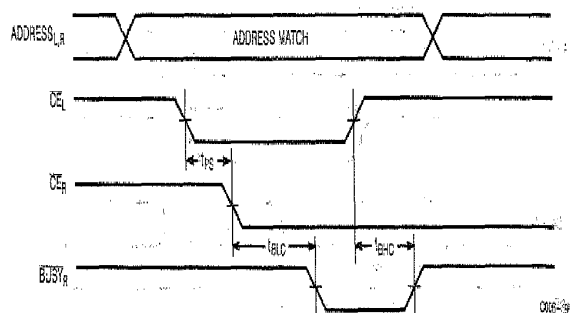
25. $\overline{C_2} = \text{HIGH}$ for the duration of the above timing (both write and read cycle).
26. $\overline{IO_R} = \overline{IO_W} = \text{LOW}$ (request semaphore). $\overline{C_2} = \overline{C_1} = \text{HIGH}$
27. Semaphores are reset (available to both parts) at each start.
28. If $\overline{IO_R}$ is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will obtain the semaphore.



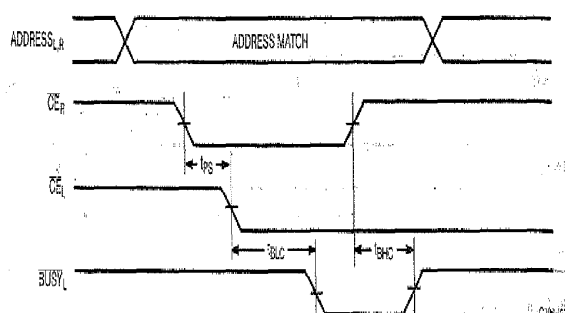
PRELIMINARY

CY7C016

Switching Waveforms (continued)

Busy Timing Diagram No. 1 (CE Arbitration)⁽²⁹⁾CE_L Valid First:

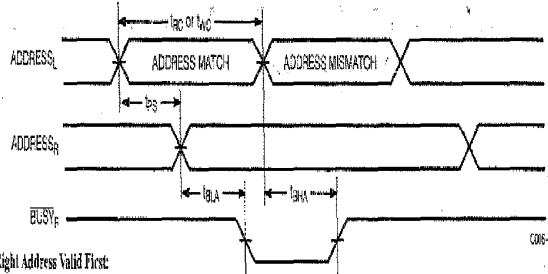
C008-29

CE_R Valid First:

C008-29

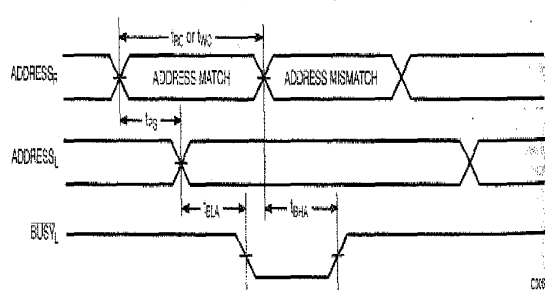
Busy Timing Diagram No. 2 (Address Arbitration)⁽³⁰⁾

Left Address Valid First:



C008-30

Right Address Valid First:



C008-30

Note:

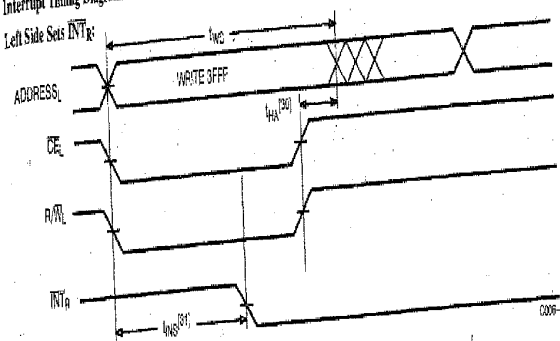
29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $BUSY$ will be asserted.
 30. t_{BHA} depends on which enable pin (CE_L or $R\overline{W}_L$) is deasserted first.



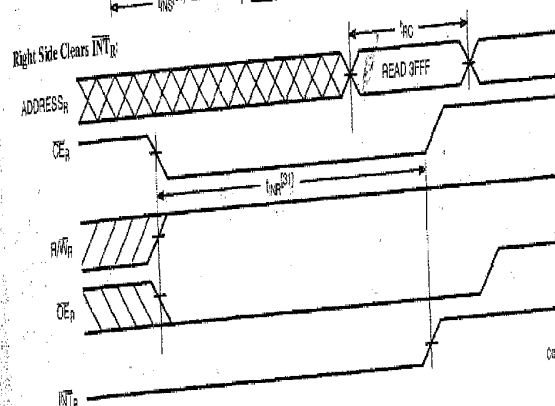
PRELIMINARY

Switching Waveforms (continued)

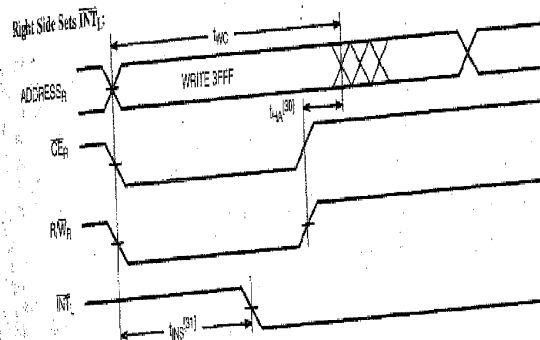
Interrupt Timing Diagrams

Left Side Sets $\overline{INT}_R$:

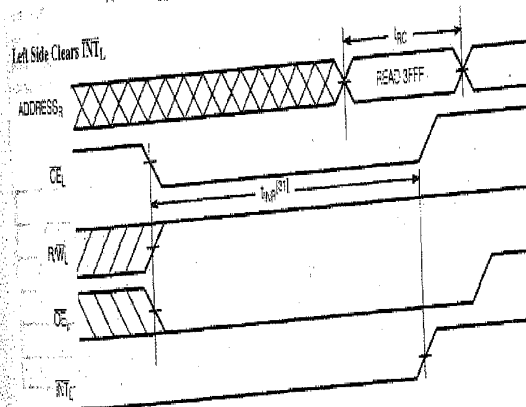
C008-23

Right Side Clears $\overline{INT}_R$:

C008-24

Right Side Sets $\overline{INT}_L$:

C008-25

Left Side Clears $\overline{INT}_L$:

C008-26

ports. When the left port writes to location 3FFE (HEX), the right port's interrupt flag (INT₂) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag (INT₁) is accomplished when the right port writes to location 3FFE (HEX). This flag is cleared when the left port reads location 3FFE (HEX). The message at 3FFE (HEX) is user-defined. See Table 2 for input requirements for INT₁, INT₂, and INT₃ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C06016 provides on-chip arbitration to alternate simultaneous memory location access (contention). If both ports' CE₁ are asserted and an address match occurs within t_{ps} of each other, the Busy logic will determine which port has access. If t_{ps} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. BUSY will be asserted (high) after an address match or t_{ps} after CE is taken LOW. BUSY₁ and BUSY₂ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/S pin is provided in order to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the BUSY input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/S pin allows the device to be used as a master and therefore the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C06016 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for t_{ps} before attempting to read the semaphore. The semaphore value will be available t_{ps} + t_{ps} after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource; otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

functions as a chip enable for the semaphore latches (CE must remain HIGH during SEM LOW). A₀₋₇ represents the semaphore address. OE and RW are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O₀ is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore.

Operations

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{ps} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All Semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 3. Semaphore Operation Example

Function	I/O ₀ Left	I/O ₀ Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Functional Description

Write Operation

Data must be set up for a duration of t_{ps} before the rising edge of RW in order to guarantee a valid write. A write operation is controlled by either the OE pin (see Write Cycle No. 1 waveform) or the RW pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{ps} after the OE is deasserted or t_{ps} after the falling edge of RW. Required inputs for non-contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output, otherwise the data read is not deterministic. Data will be valid on the port t_{ps} after the data is presented on the other port.

Table 1. Non-Contenting Read/Write

Inputs				Outputs	Operation
CE	RW	OE	SEM	I/O ₀₋₇	
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H		X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Read Operation

When reading the device, the user must assert both the OE and CE pins. Data will be available t_{ps} after CE or t_{ps} after OE is asserted. If the user of the CY7C06016 wishes to access a semaphore flag, then the SEM pin must be asserted instead of the CE pin.

Table 2. Interrupt Operation Example (assumes BUSY₁ = BUSY₂ = HIGH)

Function	Left Port					Right Port				
	RW	CE	OE	A _{0-13L}	INT	RW	CE	OE	A _{0-13R}	INT
Set Left INT	X	X	X	X	L	L	L	X	3FFE	X
Reset Left INT	X	L	L	3FFE	H	X	L	L	X	X
Set Right INT	L	L	X	3FFE	X	X	X	X	X	L
Reset Right INT	X	X	X	X	X	X	L	L	3FFE	H

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C006-15AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C006-25AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006-25AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006-25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C006-35AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006-35AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006-35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C006-55AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006-55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006-55AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006-55JI	J81	68-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C016-15AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C016-25AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016-25AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016-25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C016-35AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016-35AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016-35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C016-55AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016-55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016-55AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016-55JI	J81	68-Lead Plastic Leaded Chip Carrier	

MILITARY SPECIFICATIONS Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max	1, 2, 3
I_{IH}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SR1}	1, 2, 3
I_{SR2}	1, 2, 3
I_{SR3}	1, 2, 3
I_{SR4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{CHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCF}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUS/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{BS}	7, 8, 9, 10, 11
t_{BSS}	7, 8, 9, 10, 11
t_{BNR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{WCD}	7, 8, 9, 10, 11

Document #: 38-00163



200-MBaud HOTLink® Transceiver

Features

- Second-generation HOTLink® technology
- Fibre Channel and ESCON®-compliant 8B/10B encoder/decoder
- 10- or 12-bit pre-encoded data path (raw mode)
- 8- or 10-bit encoded data transport (using 8B/10B coding)
- Synchronous or asynchronous TTL parallel interface
- UTOPIA compatible host bus interface
- Embedded/Bypassable 256-character synchronous FIFOs
- Integrated support for daisy-chain and ring topologies
- Domain or individual destination device addressing
- 50- to 200-MBaud serial signaling rate
- Internal PLLs with no external PLL components
- Dual differential PECL-compatible serial inputs
- Dual differential PECL-compatible serial outputs
- Compatible with fiber-optic modules and copper cables
- Built-In Self-Test (BIST) for link testing
- Link Quality Indicator
- Single +5.0V $\pm 10\%$ supply
- 100-pin TQFP
- 0.35 μ m CMOS technology

Functional Description

The 200-MBaud CY7C924ADX HOTLink Transceiver is a point-to-point communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at speeds ranging between 50 and 200 MBaud. The transmit section accepts parallel data of selectable width and converts it to serial data, while the receiver section accepts serial data and converts it to parallel data of selectable width. *Figure 1* illustrates typical connections between two independent host systems and corresponding CY7C924ADX parts. As a second generation HOTLink device, the CY7C924ADX provides enhanced levels of technology, functionality, and integration over the field-proven CY7B923/933 HOTLink.

The transmit section of the CY7C924ADX HOTLink can be configured to accept either 8- or 10-bit data characters on each clock cycle, and stores the parallel data into an internal Transmit FIFO. Data is read from the Transmit FIFO and is encoded using an embedded 8B/10B encoder to improve its serial transmission characteristics. These encoded characters are then serialized and output from two Positive ECL (PECL) compatible differential transmission line drivers at a bit-rate of 10 or 12 times the character rate.

The receive section of the CY7C924ADX HOTLink accepts a serial bit-stream from one of two PECL-compatible differential line receivers and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. The recovered bit stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are reconstructed into either 8- or 10-bit data characters, written to an internal Receive FIFO, and presented to the destination host system.

The integrated 8B/10B encoder/decoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface. The embedded FIFOs may also be bypassed to create a reference-locked serial transmission link. For those systems requiring even greater FIFO storage capability, external FIFOs may be directly coupled to the CY7C924ADX device through the parallel interface without additional glue-logic.

The TTL parallel I/O interface may be configured as either a FIFO (configurable for UTOPIA emulation or for depth expansion through external FIFOs) or as a pipeline register extender. The FIFO configurations are optimized for transport of time-independent (asynchronous) 8- or 10-bit character-oriented data across a link. A Built-In Self-Test (BIST) pattern generator and checker permits at-speed testing of the high-speed serial data paths in both the transmit and receive sections, and across the interconnecting links.

HOTLink devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting workstations, backplanes, servers, mass storage, and video transmission equipment.

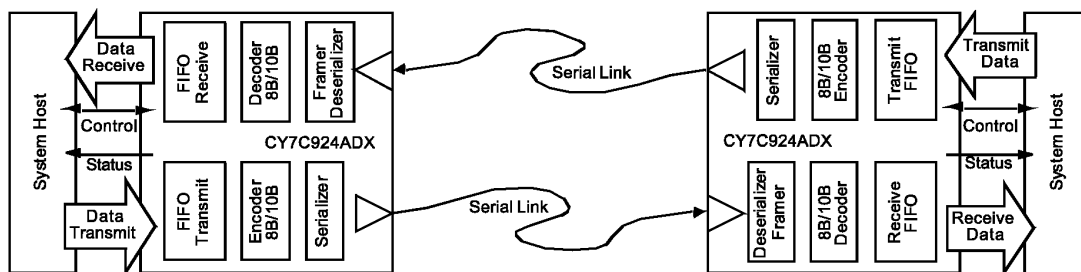
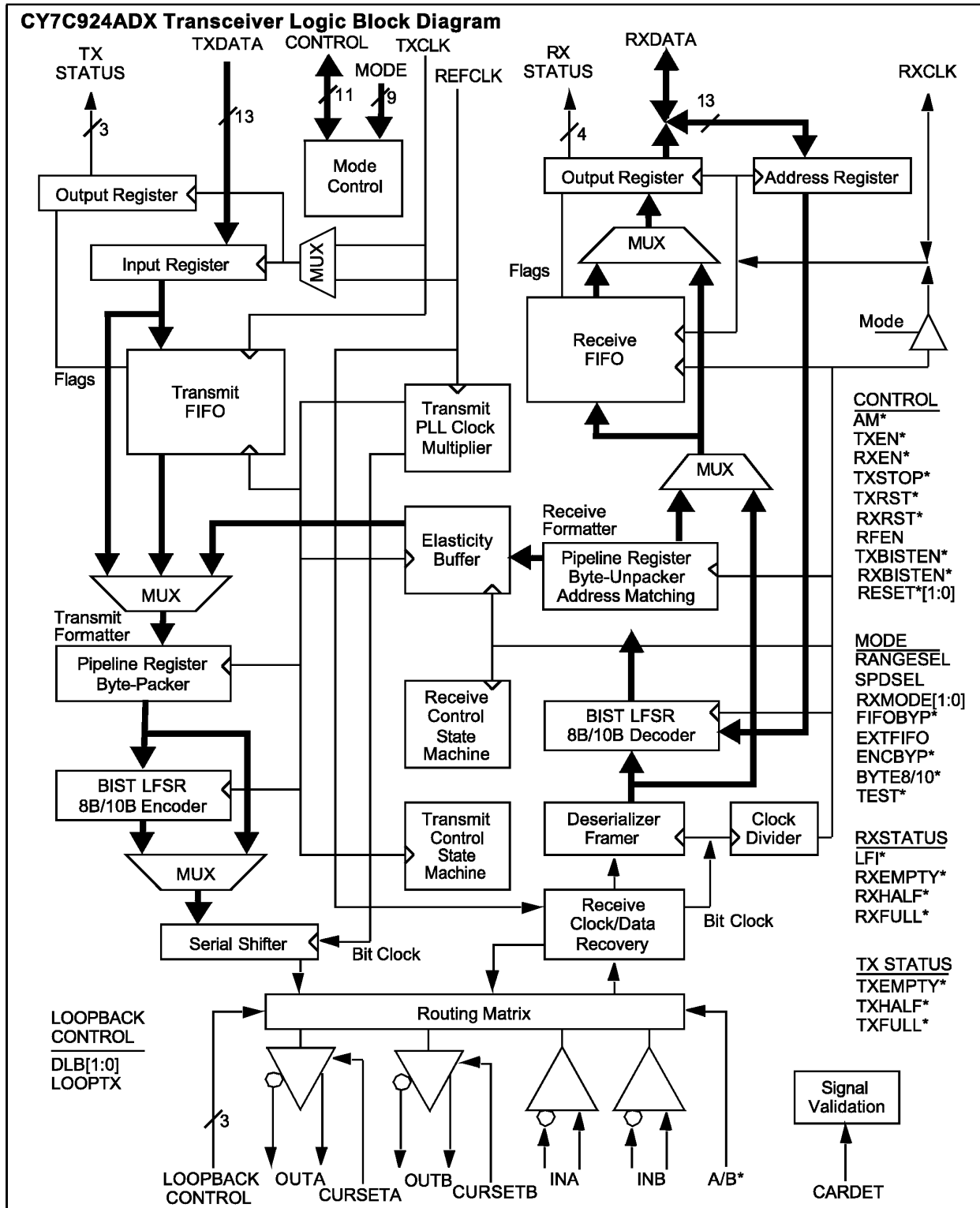
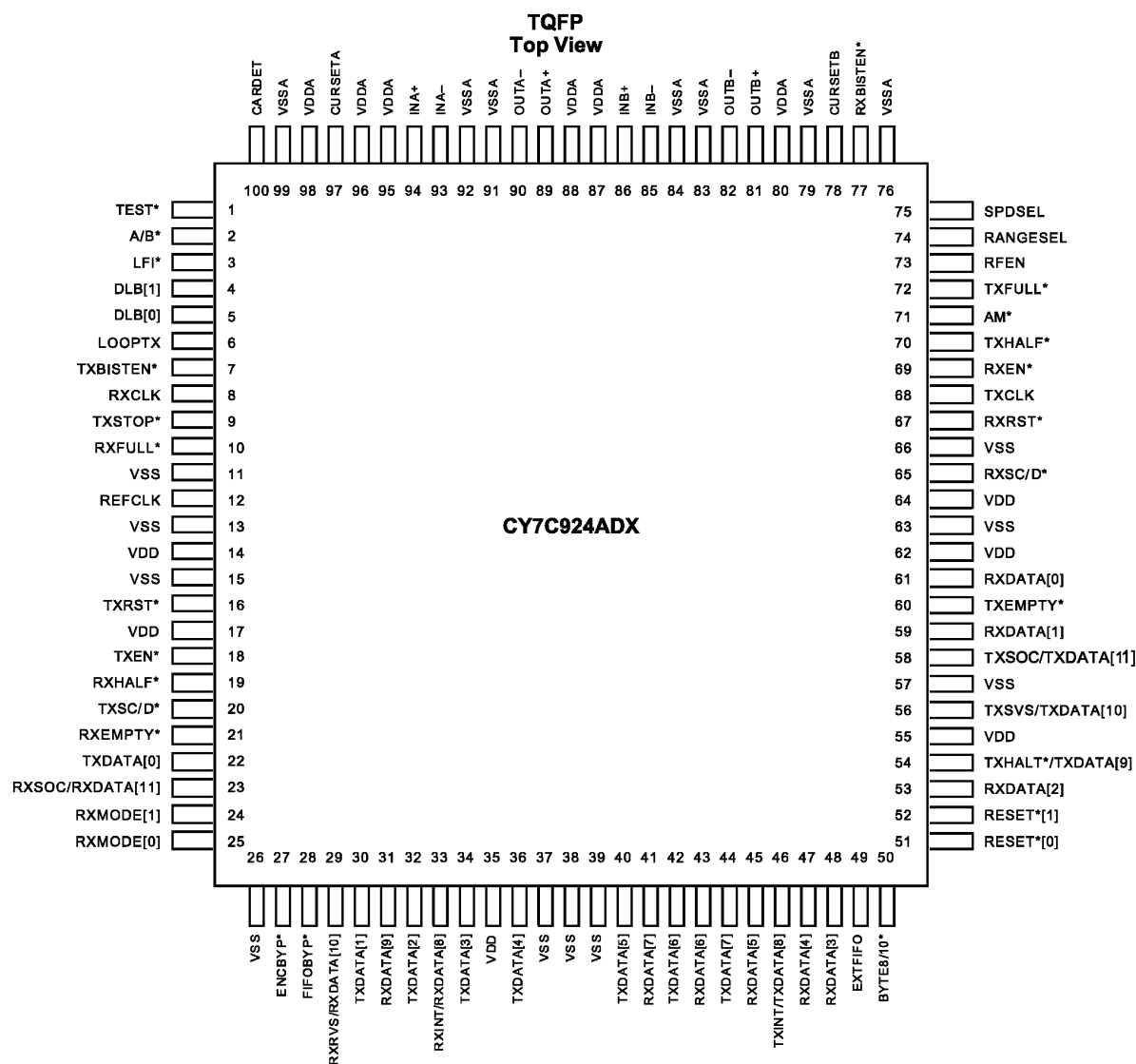


Figure 1. HOTLink System Connections





Pin Configuration





Pin Descriptions
CY7C924ADX HOTLink Transceiver

Pin #	Name	I/O Characteristics	Signal Description
Transmit Path Signals			
44, 42, 40, 36, 34, 32, 30, 22	TXDATA[7:0]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull-Up	Parallel Transmit Data Input. Bus width can be configured to accept either 8- or 10-bit characters. When the encoder is bypassed (ENCBYP* is LOW), TXDATA[7:0] functions as the least significant eight bits of the 10- or 12-bit pre-encoded transmit character.
46	TXINT/ TXDATA[8]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull-Up	Transmit Interrupt Input. This input is only interpreted if both the Transmit FIFO and Encoder are enabled (FIFOBYP* and ENCBYP* are HIGH). Upon any state-change (0→1 or 1→0) in TXINT, a character is forced into the transmit encoder and shifter prior to accessing the next Transmit FIFO contents. This signal is routed around, not through, the Transmit FIFO. When TXINT transitions from 0→1, a C0.0 (K28.0) special code is sent. When TXINT transitions from 1→0, a C3.0 (K28.3) special code is sent. These special codes force a similar signal transition on the RXINT output of an attached CY7C924ADX HOTLink Transceiver. When the Transmit FIFO is bypassed and the encoder is enabled (FIFOBYP* is LOW and ENCBYP* is HIGH), this input is ignored. When the Transmit FIFO is bypassed and the encoder is bypassed (FIFOBYP* and ENCBYP* are LOW), TXDATA[8] functions as the 9th bit of the 10- or 12-bit pre-encoded transmit character.
54	TXHALT*/ TXDATA[9]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull-Up	Transmit FIFO Halt Immediate Input. When the Transmit FIFO and the encoder are enabled (FIFOBYP* and ENCBYP* are HIGH) and TXHALT* is asserted LOW, transmission of data from the FIFO is suspended and the HOTLink transmits idle characters (K28.5). During this time, data can still be loaded into the FIFO. When TXHALT* is deasserted HIGH, normal data processing proceeds. When the encoder is bypassed (ENCBYP* is LOW), TXDATA[9] always functions as the 10th bit of the 10- or 12-bit pre-encoded transmit character. When the Transmit FIFO is bypassed and the encoder is enabled (FIFOBYP* is LOW and ENCBYP* is HIGH), this input is ignored.
56	TXSVS/ TXDATA[10]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull-Up	Transmit Send Violation Symbol Input. When the Encoder is enabled and the Transmit FIFO is enabled (ENCBYP* and FIFOBYP* are HIGH), this input is interpreted along with TXSOC and TXSC/D* (see <i>Table 2</i> for details). When the Transmit FIFO is disabled (FIFOBYP* is LOW) and the TXSVS bit is set, the character on the TXDATA is ignored and a C0.7 exception is sent instead. When the Encoder is bypassed and in 10-bit mode (ENCBYP* and BYTE8/10* are LOW), TXDATA[10] functions as the 11th bit of the 12-bit pre-encoded transmit character. When the Encoder is bypassed and in 8-bit mode (ENCBYP* is LOW and BYTE8/10* is HIGH), this input is ignored.
58	TXSOC/ TXDATA[11]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull-Up	Transmit Start of Cell Input. When the Transmit FIFO and Encoder are enabled (ENCBYP* and FIFOBYP* are HIGH), this input is used as a message frame delimiter to indicate the beginning of a data packet. It is interpreted along with TXSVS and TXSC/D* (see <i>Table 2</i> for details). When the Transmit FIFO is bypassed (FIFOBYP* is LOW) and the Encoder is enabled (ENCBYP* is HIGH) this input is ignored. When in 12-bit encoder bypass mode (ENCBYP* and BYTE8/10* are LOW), TXDATA[11] functions as the 12th bit (MSB) of the 12-bit pre-encoded transmit character. When the Encoder is bypassed and in 8-bit mode (ENCBYP* is LOW and BYTE8/10* is HIGH), this input is ignored.
20	TXSC/D*	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull-Up	Transmit Special Character or Data Select Input. When the Transmit FIFO is enabled and the encoder is enabled (FIFOBYP* and ENCBYP* are HIGH), this input is interpreted along with TXSVS and TXSOC (see <i>Table 2</i> for details). When the Transmit FIFO is bypassed and encoding is enabled (FIFOBYP* is LOW and ENCBYP* is HIGH), this signal controls whether the TXDATA[7:0] is sent as a data or control character. When the encoder is bypassed (ENCBYP* is LOW) TXSC/D* is ignored.



Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin #	Name	I/O Characteristics	Signal Description
18	TXEN*	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull-Up	Transmit Enable Input. Data enable for the TXDATA[11:0] data bus write operations. Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). When the Transmit FIFO is enabled (FIFOBYP* is HIGH) and TXEN* is asserted, data is loaded into the FIFO on every rising edge of TXCLK. When TXEN* is deasserted with TXHALT* and TXSTOP* deasserted, data continues to be read out of the Transmit FIFO and sent serially until the FIFO empties. At this time, C5.0 (K28.5) idle characters are transmitted. When the Transmit FIFO is bypassed (FIFOBYP* is LOW) and TXEN* is asserted, the parallel data on the TXDATA bus is clocked in and transmitted on every appropriate REFCLK rising edge. When TXEN* is deasserted, the parallel data bus is ignored and C5.0 sync characters are transmitted instead.
9	TXSTOP*	TTL input, sampled on TXCLK↑, Internal Pull-Up	Transmit Stop on Start_Of_Cell Input. While the Transmit FIFO and Encoder are enabled (FIFOBYP* and ENCBYP* are HIGH), this signal is used to prevent queued data characters from being serially transmitted. While TXSTOP* is deasserted, data flows through the Transmit FIFO without interruption. When TXSTOP* is asserted, data transfers continue until a TXSOC bit is detected in the character stream, at which point data transmission ceases. When transmission is stopped, C5.0 (K28.5) characters are sent instead. If data transmission is suspended due to a SOC character, pulsing TXSTOP* deasserted then asserted will allow only the next cell (delimited by SOC bits) to be transmitted. When the Transmit FIFO is bypassed (FIFOBYP* = LOW) TXSTOP* has no function. When the Transmit FIFO is enabled (FIFOBYP* is HIGH) and the Encoder is bypassed (ENCBYP* is LOW), TXDATA[9]/TXHALT* is a data input and not TXHALT*. In this mode, the TXSOC bit is not interpreted and the TXSTOP* input assumes the same operation as TXHALT*. When soon as TXSTOP* is asserted, data reads from the Transmit FIFO are suspended and alternating disparity10-bit equivalents of C5.0 are transmitted instead.
68	TXCLK	TTL clock input, Internal Pull-Up	Transmit FIFO Clock. The input clock for the parallel interface when the Transmit FIFO is enabled (FIFOBYP* is HIGH). Used to sample all Transmit FIFO related interface signals.
72	TXFULL*	3-state TTL output, changes following TXCLK↑ or REFCLK↑	Transmit FIFO Full Status Flag. Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). The TXFULL* output is enabled when AM* is asserted, otherwise it is High-Z. When the Transmit FIFO is enabled (FIFOBYP* is HIGH), TXFULL* Indicates a Transmit FIFO full condition. When TXFULL* is first asserted, the Transmit FIFO can accept up to eight additional write cycles without loss of data. When the Transmit FIFO is bypassed (FIFOBYP* is LOW), with RANGESEL HIGH or SPDSEL LOW, TXFULL* toggles at half the REFCLK rate to provide a character rate indication.
70	TXHALF*	3-state TTL output, changes following TXCLK↑ or REFCLK↑	Transmit FIFO Half-full Status Flag. The TXHALF* flag is always active LOW, regardless of the EXTFIFO* setting. When the Transmit FIFO is enabled, TXHALF* is asserted LOW when the Transmit FIFO is ≥ half full (128 characters). TXHALF* is only set to High-Z state by the assertion of RESET*[1:0] LOW.



Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin #	Name	I/O Characteristics	Signal Description
60	TXEMPTY*	3-state TTL output, changes following TXCLK↑ or REFCLK↑	Transmit FIFO Empty Status Flag. Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). The TXEMPTY* output is enabled when AM* is asserted, otherwise it is High-Z. When the Transmit FIFO is enabled (FIFOBYP* is HIGH), TXEMPTY* is asserted either when no data has been loaded into the Transmit FIFO, or when the Transmit FIFO has been emptied by either a Transmit FIFO reset or by the normal transmission of the FIFO contents. When the Transmit FIFO is bypassed (FIFOBYP* is LOW), TXEMPTY* is asserted to indicate that the transmitter can accept data. When TXBISTEN* is asserted LOW, TXEMPTY* becomes the transmit BIST-progress indicator (regardless of the logic state of FIFOBYP*). In this mode TXEMPTY* is asserted for one TXCLK or REFCLK period at the end of each transmitted BIST sequence, depending on the FIFOBYP* setting.
16	TXRST*	TTL input, internal pull-up, sampled on TXCLK↑, Internal Pull-Up	Transmit FIFO Reset. When TXRST* is sampled asserted for eight or more TXCLK cycles, a reset operation is started on the Transmit FIFO. This input is ignored when the Transmit FIFO is bypassed.
7	TXBISTEN*	TTL input, asynchronous, Internal Pull-Up	Transmitter BIST Enable. When TXBISTEN* is LOW, the transmitter generates a 511-character repeating built-in self test (BIST) sequence, that can be used to validate link integrity. The transmitter returns to normal operation when TXBISTEN* is HIGH. All Transmit FIFO read operations are suspended when BIST is active.
Receive Path Signals			
41, 43, 45, 47, 48, 53, 59, 61	RXDATA[7:0]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	Parallel Data Output and Serial Address Register Access. These outputs change following the rising edge of RXCLK, when enabled to output data (the device is addressed by AM* and selected by RXEN*). The contents of this bus are interpreted differently based on the levels present on ENCBYP*, BYTE8/10*, RXSC/D*, and when accessing the Serial Address Register. When the Decoder is bypassed (ENCBYP* is LOW), RXDATA[7:0] functions as the least significant eight bits of the 10- or 12-bit pre-encoded receive character.
33	RXINT/ RXDATA[8]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	Receive Interrupt Output. When the Receive FIFO and Decoder are enabled (FIFOBYP* and ENCBYP* are HIGH) and a C0.0 (K28.0) special code is received, RXINT is set HIGH. When a C3.0 (K28.3) special code is received RXINT is set LOW. These special codes are assumed to be generated in response to equivalent transitions on the TXINT input of an attached CY7C924ADX HOTLink transceiver. This signal is extracted prior to the Receive FIFO and (except for Receive Discard Policy 0) the associated command codes are not considered "data" to be entered into the Receive FIFO and are discarded. When the Receive FIFO is bypassed (FIFOBYP* is LOW) and the Decoder is enabled (ENCBYP* is HIGH), this output has no function. When the Decoder is bypassed (ENCBYP* is LOW), RXDATA[8] functions as the 9th bit of the 10- or 12-bit undecoded receive character.
31	RXDATA[9]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	Receive Data Output. When the Decoder is enabled in 10-bit mode (ENCBYP* is HIGH and BYTE8/10* is LOW), this output is the 10th bit (MSB) of the 10-bit decoded and unpacked data character. When the Decoder is enabled and in 8-bit mode this output is ignored. When the Decoder is bypassed (ENCBYP* is LOW), RXDATA[9] functions as the 10th bit of the 10- or 12-bit undecoded receive character.



Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin #	Name	I/O Characteristics	Signal Description
29	RXRVS/ RXDATA[10]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑, Internal Pull-Up	Received Violation Symbol Indicator. For data accesses with the Receive FIFO and Decoder are enabled (FIFOBYP* and ENCBYP* are HIGH) this signal is used as an output. It is decoded in conjunction with RXSC/D* and RXSOC, per <i>Table 6</i> to indicate the presence of specific Special Character codes in the received data stream. For data accesses with the Receive FIFO disabled and the Decoder enabled, this output indicates that a code word violation was detected on the serial inputs. When the Decoder is bypassed (ENCBYP* is LOW) and in 10-bit mode (BYTE8/10* is LOW), RXDATA[10] functions as the 11th bit of the 12-bit undecoded receive character. When in 8-bit mode this output is unused and is driven LOW RXRVS is used to report BIST pattern mismatches when RXBISTEN* is LOW. When accessing the Serial Address Register, this signal is used as a "read/write" control input. RXRVS LOW allows the host system to write the Serial Address Register (RXDATA[9:0] and RXSC/D* are inputs). RXRVS HIGH allows the host system to read the Serial Address Register (RXDATA[9:0] and RXSC/D* are outputs).
23	RXSOC/ RXDATA[11]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	Receive Start Of Cell. When the Receive FIFO and Decoder are enabled (FIFOBYP* and ENCBYP* are HIGH), this output is decoded in conjunction with RXSC/D* and RXRVS, per <i>Table 6</i> to indicate the presence of specific Special Character codes in the received data stream. When the Decoder is bypassed (ENCBYP* is LOW) and in 10-bit mode (BYTE8/10* is LOW), RXDATA[11] functions as the 12th bit (MSB) of the 12-bit undecoded receive character. When in 8-bit mode (BYTE8/10* is HIGH) this output is unused and is driven LOW.
65	RXSC/D*	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	Received Special Character or Data Indicator. For data accesses with the Receive FIFO and Decoder are enabled (FIFOBYP* and ENCBYP* are HIGH) this signal is used as an output. It is decoded in conjunction with RXSOC and RXRVS, per <i>Table 6</i> to indicate the presence of specific Special Character codes in the received data stream. For data accesses with the Receive FIFO disabled and the Decoder enabled, this output indicates that the parallel output RXDATA[7:0] is a Special Character code. When accessing the Serial Address Register, this signal is used as an input to select the addressing mode. RXSC/D* HIGH configures the Serial Address Register for Unicast address matching. RXSC/D* LOW configures the Serial Address Register for Multicast address matching. When operated with the Decoder bypassed (ENCBYP* is LOW) this pin has no function.
69	RXEN*	TTL input, sampled on RXCLK↑, Internal Pull-Up	Receive Enable. Data enable for the RXDATA[11:0] data bus write and read operations. Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). When the Receive FIFO is enabled (FIFOBYP* is HIGH) and RXEN* is asserted, data is read out of the FIFO on every rising edge of RXCLK. When RXEN* is deasserted, reads are inhibited and the RXDATA bus is not driven. When the Receive FIFO is bypassed (FIFOBYP* is LOW) and RXEN* is asserted, parallel data is clocked out Receive Output Register to the RXData bus on every RXCLK edge. When RXEN* is deasserted, the RXDATA bus is not driven. RXEN* also controls the read and write access to the Serial Address Register.
8	RXCLK	Bidirectional TTL clock, Internal Pull-Up	Receive Clock. When the Receive FIFO is enabled (FIFOBYP* is HIGH), this clock is the Receive interface <i>input</i> clock and is used to control Receive FIFO read, reset, and serial register access operations. When the Receive FIFO is bypassed (FIFOBYP* is LOW), this clock is <i>output</i> continuously at the character rate of the data being received (1/10th or 1/12th of the serial bit-rate).



Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin #	Name	I/O Characteristics	Signal Description
10	RXFULL*	3-state TTL output, changes following RXCLK↑	Receive FIFO Full Flag. Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). The RXFULL* output is enabled when AM* is asserted, otherwise it is High-Z. When the Receive FIFO is addressed (FIFOBYP* is HIGH and the device is addressed by AM* and selected by RXEN*), RXFULL* is asserted when the Receive FIFO has room for eight or fewer writes. An RXFULL* condition may indicate loss of data. When the Receive FIFO is bypassed (FIFOBYP* is LOW), RXFULL* and RXHALF* are deasserted to indicate that valid data may be present. RXFULL* is also used as a BIST progress indicator, and pulses asserted once every pass through the 511-character BIST loop. The RXFULL* output is enabled when AM* is asserted, otherwise it is High-Z.
19	RXHALF*	TTL output, changes following RXCLK↑	Receive FIFO Half-full Flag. The RXHALF* flag is always active LOW, regardless of the EXTFIFO* setting. When the Receive FIFO is enabled (FIFOBYP* is HIGH), this signal is asserted when the Receive FIFO is ≥ half full (128 characters). When the Receive FIFO is bypassed, RXHALF* is deasserted. RXHALF* is forced to the High-Z state only during a "full-chip" reset (i.e., while RESET*[1:0] are LOW).
21	RXEMPTY*	3-state TTL output, changes following RXCLK↑	Receive FIFO Empty Flag. Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). The RXFULL* output is enabled when AM* is asserted, otherwise it is High-Z. When the Receive FIFO is enabled (FIFOBYP* is HIGH), RXEMPTY* is asserted when no data remains in the Receive FIFO. Any read operation occurring when RXEMPTY* is asserted results in no change in the FIFO status, and the data from the last valid read remains on the RXDATA bus. When the Receive FIFO is bypassed but the Decoder is enabled, RXEMPTY* is used as a valid data indicator. The RXMODE[1:0] settings allow the user to determine which data is valid and allows selective flagging of idle characters. When RXEMPTY* is deasserted it indicates that a valid character (as selected by RXMODE[1:0]) is present at the RXDATA outputs. When asserted it indicates that a C5.0 (K28.5) rejected by the current RXMODE[1:0] setting is present on the RXDATA output bus. If both the Receive FIFO and the Decoder are bypassed, RXEMPTY* is deasserted to indicate that all received characters are valid. The TXFULL* output is enabled when AM* is asserted, otherwise it is High-Z.
67	RXRST*	TTL input, sampled on RXCLK↑, Internal Pull-Up	Receive FIFO Reset. When the Receive FIFO is addressed (FIFOBYP* is HIGH and device is selected by AM*) and RXRST* is sampled asserted for eight or more RXCLK cycles, a Receive FIFO reset is initiated. The RXRST* input is also asserted to access the Serial Address Register.
73	RFEN	TTL input, asynchronous, Internal Pull-Up	Reframe Enable. Used to control when the framer is allowed to adjust the character boundaries based on detection of one or more K28.5 characters in the data stream. When HIGH, the framer is allowed to adjust the character boundaries relative to the received serial data stream to match those of the remote transmitter. When LOW, the boundary is fixed.
77	RXBISTEN*	TTL input, asynchronous, Internal Pull-Up	Receiver BIST Enable. When asserted, built-in self test (BIST) is active and the receiver is configured to perform a character-for-character match of the incoming data stream with a 511-character BIST sequence. The result of character mismatches are indicated on RXRVS. Completion of each 511-character BIST loop is accompanied by an assertion pulse on the RXFULL* flag.



Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin #	Name	I/O Characteristics	Signal Description
Control Signals			
71	AM*	TTL input, sampled by TXCLK $\uparrow$, RXCLK $\uparrow$, and REFCLK $\uparrow$	Address Match. This signal is used as a qualifier for TXEN*, RXEN*, TXRST*, and RXRST*. Also controls three-state enables for the TXFULL*, TXEMPTY*, RXFULL*, and RXEMPTY* signals.
6	LOOPTX	TTL input, asynchronous, Internal Pull-Down	Serial-In to Serial-out LOOP Select. This input controls the LOOP-through function in which the serial data is recovered by the Clock/Data Recovery PLL and is then retransmitted using the Transmit PLL as the bit-rate reference. It selects between the output of the Transmit FIFO and the output of the Elasticity Buffer as the input to the Transmit Encoder. When LOW, the Transmit FIFO is the source of data for transmission. When HIGH, the Elasticity Buffer is the source of data for transmission and serial input data is reclocked and routed to the serial outputs. The LOOPTX function can only be used if the FIFOs are enabled (FIFOBYP* = HIGH).
12	REFCLK	TTL input clock	Reference Clock. This clock input is used as the timing reference for the transmit and receive PLLs. When the Transmit FIFO is bypassed, REFCLK is also used as the clock for the external transmit data interface. See <i>Table 5</i> for the relationships between REFCLK, SPDSEL, RANGESEL, FIFOBYP*, ENCBYP* and BYTE8/10*.
75	SPDSEL	Static control input TTL levels Normally wired HIGH or LOW	Speed Select. Used to select one of two operating data rate ranges for the device. When the operating symbol rate is between 100 and 200 MBaud, SPDSEL must be HIGH. When the operating symbol rate is between 50 and 100 MBaud, SPDSEL must be LOW (see <i>Table 5</i>).
74	RANGESEL	Static control input TTL levels Normally wired HIGH or LOW	Range Select. Selects the proper prescaler for the REFCLK input. See <i>Table 5</i> for the various relationships between REFCLK, SPDSEL, RANGESEL, FIFOBYP*, ENCBYP* and BYTE8/10*. When the Transmit FIFO is bypassed (FIFOBYP* is LOW) and REFCLK is a non-unity multiple of the character rate (RANGESEL HIGH or SPDSEL LOW), TXFULL* toggles at half the REFCLK rate to provide a character rate indication, and to show when data can be accepted.
49	EXTFIFO	Static control input TTL levels Normally wired HIGH or LOW	External FIFO Select. EXTFIFO indicates whether the device is used with external FIFOs and modifies the active level of the RXEN* and TXEN* inputs and the timing of the Transmitter data bus according to the interface selected. When in Utopia mode and not configured for external FIFOs (EXTFIFO is LOW), TXEN*, RXEN* and all FIFO flags are active LOW. In this mode the active data transition for the transmit data bus is within the same clock as the transmit interface is selected by TXEN*. When configured for Cascade mode where the CY7C924ADX device is cascaded with external FIFOs (EXTFIFO is HIGH), TXEN, RXEN, the Full and Empty FIFO flags are active HIGH (the Half-full flag is always active LOW). TXEN is assumed to be driven by the empty flag of an attached CY7C42X5 FIFO, and RXEN is assumed to be driven by the Almost Full flag of an attached CY7C42X5 FIFO. In this mode the active data transition for the transmit data bus is in the clock cycle following the clock edge where transmit interface is selected by TXEN*.
28	FIFOBYP*	Static control input TTL levels Normally wired HIGH or LOW	FIFO Bypass Select. When LOW, the Transmit and Receive FIFOs are bypassed. In this mode TXCLK is not used. Instead all transmit data must be synchronous to REFCLK. Transmit FIFO status flags are synchronized to REFCLK. RXCLK becomes an output at the Receive PLL recovered character clock rate. All received data and FIFO status flags are synchronized to RXCLK. When HIGH, the Transmit and Receive FIFOs are enabled. In this mode all Transmit FIFO writes are synchronized to TXCLK, and all Receive FIFO reads are synchronous to the RXCLK input.



Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin #	Name	I/O Characteristics	Signal Description
27	ENCBYP*	Static control input TTL levels Normally wired HIGH or LOW	Encoder Bypass Select. When LOW, both the Encoder and Decoder are bypassed. Data is transmitted in NRZ format, without encoding, LSB first. Received data are presented as parallel characters to the interface without decoding. When HIGH, data is passed through both the 8B/10B Encoder in the Transmit path and the Decoder in the Receive path.
24, 25	RXMODE[1:0]	Static control input TTL levels Normally wired HIGH or LOW	Receive Discard Policy Select. These inputs select between the four data handling and fill-character discard modes in the receiver. See <i>Table 7</i> .
50	BYTE8/10*	Static control input TTL levels Normally wired HIGH or LOW	Parallel Data Character Size Select. Selects the input data character width. When BYTE8/10* is HIGH and ENCBYP* is HIGH, the device is in 8-bit mode and the data is encoded using the 8B/10B code rules found in <i>Table 11</i> and <i>Table 12</i> . When BYTE8/10* is HIGH and ENCBYP* is LOW, the 10 parallel data bits are passed directly to or from the serial stream without encoding or decoding. When BYTE8/10* is LOW, the part is in 10-bit mode. If the encoder is enabled (ENCBYP* is HIGH), the part passes the 10 parallel bits to the byte stuffer and encoder. When the encoder is disabled (ENCBYP* is LOW), the 12 parallel data bits are passed directly to or from the serial stream without encoding or decoding. For affected pin groupings and function see <i>Table 1</i> and <i>Table 8</i> . If the FIFOs are BYPASSED and Encoding is enabled (FIFOBYP* = LOW and ENCBYP* = HIGH), BYTE8/10* MUST BE HIGH
52, 51	RESET*[1:0]	TTL input,	Global Logic Reset. These inputs are pulsed LOW for one or more REFCLK periods to reset the internal logic. They must be tied together or driven concurrently to ensure a valid reset.
1	TEST*	TTL input, asynchronous. Normally wired HIGH	Factory Test Mode Select. Used to force the part into a diagnostic test mode used for factory ATE test. This pin is tied HIGH during normal operation.
Analog I/O and Control			
89, 90, 81, 82	OUTA± OUTB±	PECL-compatible differential outputs	Differential Serial Data Outputs. These PECL-compatible outputs are capable of driving terminated transmission lines or commercial fiber-optic transmitter modules. An unused output pair may be powered down by leaving the outputs unconnected and strapping the associated CURSETx pin to V _{DD} .
97	CURSETA	Analog input	Current-set Resistor Input for OUTA±. A precision resistor is connected between this input and a clean ground to set the output differential amplitude and currents for the OUTA± differential driver.
78	CURSETB	Analog input	Current-set Resistor Input for OUTB±. A precision resistor is connected between this input and a clean ground to set the output differential amplitude and currents for the OUTB± differential driver.
94, 93, 86, 85	INA± INB±	PECL-compatible differential inputs	Differential Serial Data Inputs. These inputs accept the serial data stream for deserialization and decoding. Only one serial stream at a time may be fed to the receiver PLL to extract the data content. This stream is selected using the A/B* input. These inputs may also be routed to the OUTB± serial outputs using the DLB[1:0] inputs.
2	A/B*	TTL input, asynchronous, Internal Pull-Up	Receive Data Input Selector. Determines which external serial bit-stream is passed to the receiver clock and data recovery circuit.
4,5	DLB[1:0]	TTL input, asynchronous, Internal Pull-Down	Loop-back Select Inputs. Selects connections between serial inputs and outputs. Controls diagnostic loop-back and serial loop-through functions. See <i>Table 3</i> for details.

**Pin Descriptions (continued)**
CY7C924ADX HOTLink Transceiver

Pin #	Name	I/O Characteristics	Signal Description
100	CARDET	PECL-compatible input, asynchronous	Carrier Detect Input. Used to allow an external device to signify a valid signal is being presented to the high speed PECL-compatible input buffers, as is typical on an Optical Module. When CARDET is deasserted LOW, the LFI* indicator asserts LOW signifying a Link Fault. This input can be tied to V _{DD} for copper media applications.
3	LFI*	TTL output, changes following RXCLK↑	Link Fault Indication Output. Active LOW. LFI* changes synchronous with RXCLK. This output is driven LOW when the serial link currently selected by A/B* is not suitable for data recovery. This can be caused by Serial Data Amplitude is below acceptable levels. Input transition density is not sufficient for PLL clock recovery. Serial Data stream is outside an acceptable frequency range of operation. CARDET is LOW.
Power			
80, 87, 88, 95, 96, 98	V _{DDA}		Power for PECL-compatible I/O signals and internal analog circuits.
76, 79, 83, 84, 91, 92, 99	V _{SSA}		Ground for PECL-compatible I/O signals and internal analog circuits.
14, 17, 35, 55, 62, 64	V _{DD}		Power for CMOS I/O signals and internal logic circuits.
11, 13, 15, 26, 37, 38, 39, 57, 63, 66	V _{SS}		Ground for CMOS I/O signals and internal logic circuits.

CY7C924ADX HOTLink Operation**Overview**

The CY7C924ADX is designed to move parallel data across both short and long distances with minimal overhead or host system intervention. This is accomplished by converting the parallel characters into a serial bit-stream, transmitting these serial bits at high speed, and converting the received serial bits back into the original parallel data format.

The CY7C924ADX offers a large feature set, allowing it to be used in a wide range of host systems. Some of the configuration options are:

- 8-bit, 10-bit or 12-bit character size
- user definable data packet or frame structure
- 2-octave data rate range
- asynchronous (FIFOed) or synchronous data interface
- 8B/10B encoded or non-encoded (raw data)
- embedded or bypassable FIFO data storage
- multi-PHY capability
- point-to-point, point-to-multipoint, or ring data-transport.

This flexibility allows the CY7C924ADX to meet the data-transport needs of almost any system.

Transmit Data Path*Transmit Data Interface/Transmit Data FIFO*

The transmit data interface to the host system is configurable as either an asynchronous buffered (FIFOed) parallel interface or as a synchronous pipeline register. The bus itself can be configured for operation with 8-bit, 10-bit or 12-bit data.

When configured for asynchronous operation (where the host-bus interface clock operates asynchronous to the serial character and bit stream clocks), the host interface becomes that of a synchronous FIFO clocked by TXCLK. In these configurations an internal 256-character Transmit FIFO is enabled. It allows the host interface to be written at any rate from DC to 50MHz.

When configured for synchronous operation, the transmit interface is clocked by REFCLK and operates synchronous to the internal character and bit-stream clocks. The input register must be written at the character rate, but REFCLK can operate at the one, two or four times the character rate.

Both asynchronous and synchronous interface operations support two interface timing models: UTOPIA and Cascade. The UTOPIA timing model is designed to match the active levels, bus timing, and signal sequencing called out in the ATM Forum UTOPIA specification. The Cascade timing model is designed to match a host bus that resembles a synchronous FIFO. These timing models allow the CY7C924ADX to directly



couple to host systems, registers, state machines, FIFOs, etc., with minimal and in many cases no external glue logic.

Encoder

Data from the host interface or Transmit FIFO is next passed to an Encoder block. The CY7C924ADX contains an internal 8B/10B encoder that is used to improve the serial transport characteristics of the data. For those systems that contain their own encoder or scrambler, this Encoder may be bypassed.

Serializer/Line Driver

The data from the Encoder is passed to a Serializer. This Serializer operates at either 2.5, 5, or 10 times the rate of the REFCLK input (or 3, 6, or 12 times when BYTE8/10* and ENCBYP* are LOW). The serialized data is output from two PECL-compatible differential line drivers configured to drive transmission lines or optical modules.

Receive Data Path

Line Receiver/Deserializer/Framer

Serial data is received at one of two PECL-compatible differential line receivers. The data is passed to both a Clock and Data Recovery PLL (Phase Locked Loop) and to a Deseri-

alizer that converts serial data into parallel characters. The Framer adjusts the boundaries of these characters to match those of the original transmitted characters.

Decoder

The parallel characters are passed through a 10B/8B Decoder and returned to their original form. For systems that make use of external decoding or descrambling, the decoder may be bypassed.

Receive Data Interface/Receive Data FIFO

Data from the decoder is passed either to a Receive FIFO or is passed directly to the output register. The output register can be configured for operation with 8-bit, 10-bit or 12-bit data

When configured for an asynchronous buffered (FIFOed) interface, the data is passed through a 256-character Receive FIFO that allows data to be read at any rate from DC to 50MHz. When configured for synchronous operation (Receive FIFO is bypassed) data is clocked out of the Receive Output register at the byte rate, up to 20MHz. The receive interface is also configurable for both UTOPIA and Cascade timing models.

Table 1. Transmit Input Bus Signal Map

	Transmit Encoder Mode ^[1]			
	Encoded 8-bit Character Stream	Pre-encoded 10-bit Character Stream	Encoded 10-bit Character Stream	Pre-encoded 12-bit Character Stream
ENCBYP*	HIGH	LOW	HIGH	LOW
BYTE8/10*	HIGH	HIGH	LOW	LOW
TXDATA Bus Input Bit				
TXSC/D*	TXSC/D*		TXSC/D*	
TXDATA[0]	TXD[0]	TXD[0] ^[2]	TXD[0]	TXD[0] ^[2]
TXDATA[1]	TXD[1]	TXD[1]	TXD[1]	TXD[1]
TXDATA[2]	TXD[2]	TXD[2]	TXD[2]	TXD[2]
TXDATA[3]	TXD[3]	TXD[3]	TXD[3]	TXD[3]
TXDATA[4]	TXD[4]	TXD[4]	TXD[4]	TXD[4]
TXDATA[5]	TXD[5]	TXD[5]	TXD[5]	TXD[5]
TXDATA[6]	TXD[6]	TXD[6]	TXD[6]	TXD[6]
TXDATA[7]	TXD[7]	TXD[7]	TXD[7]	TXD[7]
TXINT/TXDATA[8] (FIFOBYP* = HIGH)	TXINT	TXD[8]	TXD[8]	TXD[8]
TXINT/TXDATA[8] (FIFOBYP* = LOW)		TXD[8]	TXD[8]	TXD[8]
TXHALT*/TXDATA[9] (FIFOBYP* = HIGH)	TXHALT*	TXD[9]	TXD[9]	TXD[9]
TXHALT*/TXDATA[9] (FIFOBYP* = LOW)		TXD[9]	TXD[9]	TXD[9]
TXSVS/TXDATA[10]	TXSVS		TXSVS	TXD[10]
TXSOC/TXDATA[11] (FIFOBYP* = HIGH)	TXSOC		TXSOC	TXD[11]
TXSOC/TXDATA[11] (FIFOBYP* = LOW)				TXD[11]

Notes:

1. All open cells are ignored.
2. First bit shifted out. Others follow in numerical order creating an NRZ pattern.

CY7C924ADX HOTLink Transceiver Block Diagram Description

Transmit Input/Output Register

The Transmit Input Register, shown in *Figure 2*, captures the data to be processed by the HOTLink Transmitter, and allows the input timing to be made compatible with asynchronous or synchronous host system buses. These buses can take the form of UTOPIA compliant interfaces, external FIFOs, state machines, or other control structures. Data present on the TXDATA[11:0] and TXSC/D* inputs are captured at the rising edge of the selected sample clock. The transmit data bus bit-assignments vary depending on the data encoding, and bus-width selected. These bus bit-assignments are shown in *Table 1*, and list the functional names of these different signals. Note that the function of several of these signals changes in different operating modes. The logical sense of the enable and FIFO flag signals depends on the intended interface convention and is set by the EXTIFIFO pin.

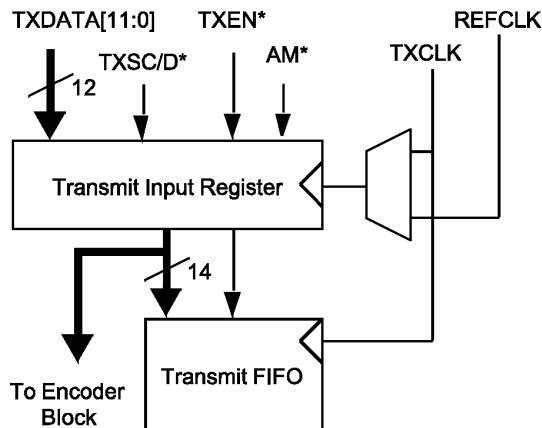


Figure 2. Transmit Input Register

The transmit interface supports both synchronous and asynchronous clocking modes, each supporting both UTOPIA (EXTIFIFO = LOW) and Cascade (EXTIFIFO = HIGH) timing models. The selection of the specific clocking mode is determined by the RANGESEL and SPDSEL inputs and the FIFO Bypass (FIFOBYP*) signal.

Synchronous Interface

Synchronous interface clocking operates the entire transmit data path synchronous to REFCLK. It is enabled by connecting FIFOBYP* LOW to disable the internal FIFOs.

Asynchronous Interface

Asynchronous interface clocking controls the writing of host bus data into the Transmit FIFO. It is enabled by setting FIFOBYP* HIGH to enable the internal FIFOs. In these configurations, all writes to the Transmit Input Register, and associated transfers to the Transmit FIFO, are controlled by TXCLK. The data is clocked out of the Transmit FIFO and through the rest of the device on REFCLK or a synthesized derivatives of REFCLK.

UTOPIA Timing Model

The UTOPIA timing model allows multiple CY7C924ADX transmitters to be addressed and accessed from a common host bus, using the protocols defined in the ATM Forum UTOPIA interface standards. It is enabled by setting EXTIFIFO LOW.

In UTOPIA timing, the TXEMPTY* and TXFULL* outputs and TXEN* input, are all active LOW signals. If the CY7C924ADX is addressed by AM*, it becomes "selected" when TXEN* is asserted LOW. Following selection, data is written into the Transmit FIFO on every clock TXCLK cycle where TXEN* remains LOW.

Cascade Timing Model

The Cascade timing model is a variation of the UTOPIA timing model. Here the TXEMPTY* and TXFULL* outputs, and TXEN input, are all active HIGH signals. Cascade timing makes use of the same address and selection sequences as UTOPIA timing, but write data accesses use a delayed write. This delayed write is necessary to allow direct coupling to external FIFOs, or to state machines that initiate a write operation one clock cycle before the data is available on the bus.

Cascade timing is enabled by setting EXTIFIFO HIGH.

When used for FIFO depth expansion, Cascade timing allows the size of the internal Transmit FIFO to be expanded to an almost unlimited depth. It allows a CY7C42x5 series synchronous FIFO to be attached to the transmit interface without any extra logic, as shown in *Figure 3*.

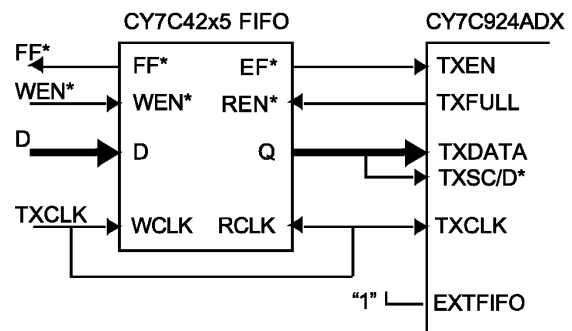


Figure 3. External FIFO Depth Expansion of the CY7C924ADX Transmit Data Path

Transmit FIFO

The Transmit FIFO is used to buffer data captured in the input register for later processing and transmission. This FIFO is sized to hold 256 14-bit characters. When the Transmit FIFO is enabled, and a Transmit FIFO write is enabled (the device is selected through AM* and TXEN* is sampled asserted), data and command are captured in the transmit input register and stored into the Transmit FIFO. All Transmit FIFO write operations are clocked by TXCLK.

The Transmit FIFO presents Full, Half-Full, and Empty FIFO flags. These flags are provided synchronous to TXCLK. When the Transmit FIFO is enabled, it allows operation with a Moore-type external controlling state machine. When configured for Cascade timing, the timing and active levels of these signals are also designed to support direct expansion to Cypress CY7C42x5 synchronous FIFOs.



The read port of the Transmit FIFO is connected to a logic block that performs data formatting and validation. All data read operations from the Transmit FIFO are controlled by a Transmit Control State Machine that operates synchronous to REFCLK.

Transmit Formatter and Validation

The Transmit Formatter and validation logic performs two primary functions:

- Data format control
- Byte-packing.

In addition to these logic functions, this block also controls the timing for the transfer of data from the Transmit Input Register, Transmit FIFO, or Elasticity Buffer.

Transmit Data Formatting

The CY7C924ADX supports a number of protocol enhancements over a raw physical-layer device. These enhancements are made possible in part through the use of the Transmit and Receive FIFOs. These FIFOs allow the CY7C924ADX to manage the data stream to a much greater extent than was possible before. In addition to the standard 8B/10B encoding used to improve serial data transmission, the CY7C924ADX also supports:

- marking of packet or cell boundaries using TXSOC
- an expanded command set
- ability to address and route packets or frames to specific receivers

All three of these capabilities are supported for both 8- and 10-bit encoded character sizes, and are made possible through use of the TXSOC bit. This bit is interpreted, along with TXSC/D* and TXSVS, in those modes where both the Transmit FIFO and the Encoder are enabled. All three bits determine how the data associated with them is processed for transmission. These operations are listed in *Table 2*.

The entries in *Table 2* where TXSOC is LOW generate the same characters in the serial data stream as a standard CY7B923 HOTLink Transmitter. The data, command, and exception character encodings are listed in the Data and Special Character code tables (*Tables 11 and 12*) found near the end of this data sheet.

Table 2. Transmit Data Formatting

TXSOC	TXSC/D*	TXSVS	Data Format Operation
0	0	0	Normal Data Encode
0	0	1	Replace Character with C0.7 Exception
0	1	0	Normal Command Encode
0	1	1	Replace Character with C0.7 Exception
1	0	0	Send Start of Cell Marker (C8.0) + Data Character
1	0	1	Replace Character with C0.7 Exception
1	1	0	Send Extended Command Marker (C9.0) + Data Character
1	1	1	Send Serial Address Marker (C10.0) + Data Character

The 001b, 011b and 101b character formats instruct the encoder to discard the associated data character and to replace it with a C0.7 Exception character.

Excepting the above 101b case, when the TXSOC bit read from the Transmit FIFO is HIGH, an extra character is inserted into the data stream. This extra character is always a Special Character code (see *Table 12*) that is used to inform the remote receiver that the immediately following character should be interpreted differently from its normal meaning. The associated character present on TXDATA[x:0] is always encoded as a data character.

The 100b combination (TXSOC=1, TXSC/D*=0, and TXSVS=0) is used as a marker for the start of a cell, frame, or packet of data being sent across the interface. When a character is read from the Transmit FIFO with this combination of bits set, a C8.0 Special Character code is sent to the Encoder prior to sending the associated data character.

The 110b character format is used to expand the command space beyond that available with the default 8B/10B code. The 8B/10B code normally supports a *data* space of 256 data characters, and a *command* (non-data) space of twelve command characters (C0.0–C11.0 in *Table 12*). For those data links where this is not sufficient, the 110b format can be used to mark the associated data as an extended command. This expands the command space to 256 commands (in addition to some of the present twelve). When a character is read from the Transmit FIFO with these bits set, a C9.0 Special Character code is sent to the Encoder prior to sending the data character.

The 111b character format is used to send a serial addresses to attached receivers. These serial addresses allow a host to direct (the following) data to a specific destination or destinations, when the CY7C924ADX devices are connected in a ring or bus topology.

The Serial Address marker may also be used to send packet identification fields, sequence numbers, or other high-level routing information for those point-to-point connections that do not require physical address capabilities, however, the reporting of the address field contents may be affected by the present receiver discard policy. This marking or tagging capability can be performed with the 100b or 110b character formats without concern for receiver discard policy.

When a character is read from the Transmit FIFO with these bits set, a C10.0 Special Character is sent to the Encoder prior to sending the associated data character.

Byte-Packer

The byte-packer is a logical construct, used to control the efficient segmentation of 10-bit source data into 8-bit characters. This conversion allows these characters to be transported using 8B/10B encoding, with the same encoding overhead (20%) as when sending 8-bit characters. Because the serializer continues to operate using 10-bit transmission characters, this encoding mode can only operate with the Transmit FIFO enabled.

The byte-packer operates by taking pieces of one or more 10-bit characters, combining them into 8-bit groups, and passing these groups to the 8B/10B encoder. It takes exactly five 8-bit characters to transport four 10-bit characters. The allocation is performed, as shown in *Figure 4*, where the low-order eight bits of the first 10-bit character (A[7:0]) are passed to the encoder on the first clock cycle. During the second clock cycle



the remaining two bits of the first character are combined with the lower six bits of the second 10-bit character ($B[5:0]+A[9:8]$). In the third clock cycle the remaining four bits of the second 10-bit character are combined with the lower four bits of the third 10-bit character ($C[3:0]+B[9:6]$). In the fourth clock cycle the remaining six bits of the third 10-bit character are combined with the lower two bits of the fourth 10-bit character ($D[1:0]+C[9:4]$). In the fifth clock cycle the remaining eight bits of the fourth 10-bit character are passed to the encoder ($D[9:2]$).

This process repeats for additional data characters present in the FIFO. If at any time the Transmit FIFO is emptied, and a portion of a 10-bit character has not yet been transmitted, the remaining bits of the 8-bit character are filled with dummy bits before that character is passed to the encoder. The 8-bit character containing these dummy bits is immediately followed by a C5.0 (K28.5) fill character, which resets the sequencer boundaries to the first character position.

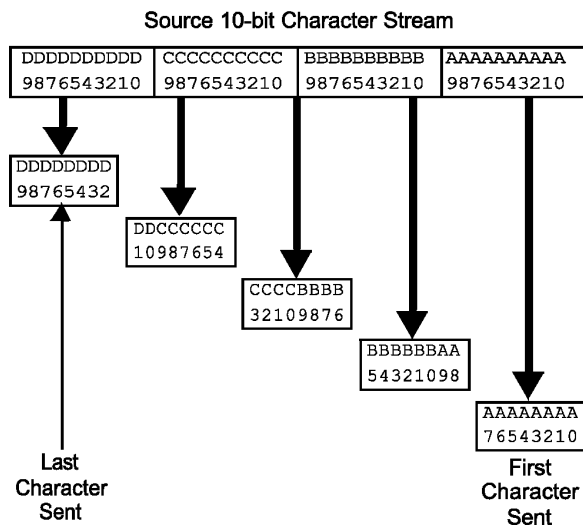


Figure 4.Byte-Packer 10-to-8 Character Mapping

Encoder Block

The Encoder logic block performs two primary functions: encoding the data for serial transmission and generating BIST (Built-In Self Test) patterns to allow at-speed link and device testing.

BIST LFSR

The Encoder logic block operates on data stored in a register. This register accepts information directly from the Transmit FIFO, the Transmit Input Register, the 10/8 Byte-Packer, or from the Transmit Control State Machine when it inserts special characters into the data stream.

This same register is converted into a Linear Feedback Shift Register (LFSR) when the Built-In Self-Test (BIST) pattern generator is enabled ($TXBISTEN^*$ is LOW). When enabled, this LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Receiver.

The specific patterns generated are described in detail in the Cypress application note "HOTLink Built-In Self-Test." The sequence generated by the CY7C924ADX is identical to that in the HOTLink CY7B923 and HOTLink II family CYP(V)15G0x0x, allowing interoperable systems to be built when used at compatible serial signaling rates.

Encoder

The data passed through the Transmit FIFO and formatter, or as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee:

- a minimum transition density (to allow the serial receiver PLL to extract a clock from the data stream)
- a DC-balance in the signaling (to prevent baseline wander)
- run-length limits in the serial data (to limit the bandwidth of the link)
- some way to allow the remote receiver to determine the correct character boundaries (framing).

The CY7C924ADX contains an integrated 8B/10B encoder that accepts 8-bit data characters and converts these into 10-bit transmission characters that have been optimized for transport on serial communications links. The 8B/10B encoder can be bypassed for those system that operate with external 8B/10B encoders, or use alternate forms of encoding or scrambling to ensure good transmission characteristics. The operation of the 8B/10B encoding algorithm is described in detail later in this data sheet, and the complete encoding tables are listed in *Tables 11 and 12*.

When the Encoder is enabled, the transmit data characters (as passed through the Transmit FIFO and formatter) are converted to either a 10-bit Data symbol or a 10-bit Special Character, depending upon the state of the $TXSC/D^*$ input. If $TXSC/D^*$ is HIGH, the data inputs represent a Special Character code and are encoded using the Special Character encoding rules in *Table 12*. If $TXSC/D^*$ is LOW, the data inputs are encoded using the Data Character encoding in *Table 11*.

If $TXSVS$ is HIGH, the respective character is replaced with an SVS (C0.7) character. This can be used to check error handling system-logic in the receiver controller or for proprietary applications.

The 8B/10B encoder is standards compliant with ANSI/NCITS ASC X3.230-1994 (Fibre Channel), IEEE 802.3z (Gigabit Ethernet), the IBM ESCON and FICON channels, and ATM Forum standards for data transport.

The 8B/10B coding function of the Encoder can be bypassed for systems that include an external coder or scrambler function as part of the controller or host system. This is performed by setting $ENCBYP^*$ LOW. With the encoder bypassed, each 10-bit or 12-bit character (as captured in the Transmit Input Register) is passed directly to the Transmit Shifter (or Transmit FIFO) without modification.

Transmit Shifter

The Transmit Shifter accepts 10-bit or 12-bit parallel data from the Encoder block once each character time, and shifts it out the serial interface output buffers using a PLL-multiplied bit-clock. This bit-clock runs at 2.5, 5, or 10 times the REFCLK rate (3, 6, or 12 times when $BYTE8/10^*$ and $ENCBYP^*$ are LOW) as selected by $RANGESEL$ and $SPDSEL$ (see *Table 4*). Timing for the parallel transfer is controlled by the counter and



dividers in the Clock Multiplier PLL and is not affected by signal levels or timing at the input pins.

Bits in each character are shifted out LSB first, as required by ANSI and IEEE standards for 8B/10B coded serial data streams.

Routing Matrix

The Routing Matrix is a set of precision multiplexors that allow various combinations of Transmit Shifter, buffered INA± or INB± serial line receiver inputs, or a reclocked serial line receiver input to be transmitted from the OUTB± serial data outputs. The signal routing for the transmit serial outputs is controlled primarily by the DLB[1:0] inputs as listed in *Table 3*.

The level-restored (10b) and reclocked (11b) settings make use of one of the transmit data outputs. When configured for level-restored or reclocked data, the selected input is retransmitted on OUTB±. The level-restored connection simply buffers the input signal allowing a “bus-like” connection to be constructed without concern for multi-drop PECL-compatible signal layout issues.

The reclocked connection buffers a PLL-filtered copy of the selected input data stream. This removes most of the high-frequency jitter that accumulates on a signal when sent over long transmission lines. Because the retransmitted data is clocked by the recovered clock, the data can suffer from jitter peaking when communicated through several PLLs.

Table 3. Transmit Data Routing Matrix

DLB[1]	DLB[0]	Data Connections
0	0	
0	1	
1	0	
1	1	

For more details on these and LOOPTX reclocking options, see the *Serial Line Receivers* section.

Serial Line Drivers

The serial interface PECL-compatible Output Drivers (ECL referenced to +5V) are the transmission line drivers for the serial media. OUTA± receives its data directly from the transmit shifter, while OUTB± receives its data from the Routing Matrix. These two outputs (OUTA± and OUTB±) are capable of direct connection to +5V optical modules, and can also directly drive DC- or AC-coupled transmission lines.

The PECL-compatible Output Drivers can be viewed as programmable current sources. The output voltage is determined by the output current and the load impedance Z_{LOAD} . The desired output voltage swing is therefore controlled by the current-set resistor R_{CURSET} associated with that driver. Different R_{CURSET} values are required for different line impedance/amplitude combinations. The output swing is designed to center around $V_{DD}-1.33V$. Each output must be externally biased to $V_{DD}-1.33V$.

When the interconnect and load are viewed as a differential transmission line, the absolute voltage V_{ODIF} and the differential load impedance are used to calculate the value of R_{CURSET} . This amplitude relationship is controlled by the load impedance on the driver, and by the resistance of the R_{CURSET} resistor for that driver, as listed in *Eq. 1*.

$$R_{CURSET} = \frac{90 \times Z_{LOAD}}{V_{ODIF}} \quad \text{Eq. 1}$$

In *Eq. 1*, V_{ODIF} is the difference in voltage levels at one output of the differential driver when that output is driving HIGH and LOW, Z_{LOAD} is the differential load between the true and complement outputs of the driver. With a known load impedance and a desired signal swing, it is possible to calculate the value of the associated CURSETA or CURSETB resistor that sets this current.

Unused differential output drivers should be left open, and can reduce their power dissipation by connecting their respective CURSETx input to V_{DD} .

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts an external clock at the REFCLK input, and multiplies that clock by 2.5, 5, or 10 (3, 6, or 12 when BYTE8/10* is LOW and the encoder is disabled) to generate a bit-rate clock for use by the transmit shifter. It also provides a character-rate clock used by the Transmit Controller state machine.

The clock multiplier PLL can accept a REFCLK input between 8.33MHz and 40MHz, however, this clock range is limited by the operation mode of the CY7C924ADX as selected by the SPDSEL and RANGESEL inputs, and to a limited extent, by the BYTE8/10*, ENCBYP* and FIFOBYP* signals. *Table 4* shows the SPDSEL and RANGESEL for the case where the FIFOs and encoding are enabled. *Table 5* provides the multiplier factors and clocking ranges for various combinations of signals.



Table 4. Speed Select and Range Select Settings, FIFOs and Encoding enabled

SPDSEL	RANGESEL	Serial Data Rate (MBaud)	REFCLK Frequency (MHz)
LOW	LOW	50–100	10–20
LOW	HIGH	50–100	20–40
HIGH	LOW	100–200	10–20
HIGH	HIGH	100–200	20–40

Transmit Control State Machine

The Transmit Control State Machine responds to multiple inputs to control the data stream passed to the encoder. It operates in response to:

- the state of the FIFOBYP* and LOOPTX inputs
- the state of the TXINT input
- the presence of data in the Transmit FIFO
- the contents of the Transmit FIFO
- the contents of the Elasticity Buffer
- the state of the transmitter BIST enable (TXBISTEN*)
- the state of external halt signals (TXHALT* and TXSTOP*)

These signals are used by the Transmit Control State Machine to control the data formatter, read access to the Transmit FIFO and Elasticity Buffer, the Byte-Packer, and BIST. They determine the content of the characters passed to the Encoder and Transmit Shifter.

When the Transmit FIFO is bypassed, the Transmit Control State Machine operates synchronous to REFCLK. In this mode, data from the TXDATA bus (or other source) is passed directly from the Input Register to the Pipeline Register. If no data is enabled into the Input register (TXEN* is deasserted) then the Transmit Control State Machine presents a C5.0 Special Character code to the Encoder to maintain link synchronization. If both the Encoder and Transmit FIFO are bypassed and no data is enabled into the Input Register, the Transmit Control State Machine injects an alternating disparity sequence of pre-encoded (10-bit) forms of the C5.0 characters. This also occurs if the Encoder is bypassed, the Transmit FIFO is enabled, and the Transmit FIFO is empty. However, since disparity tracking is part of the Encoder, the transmitted C5.0 characters may generate a running disparity error at the remote receiver. If the attached receiver has its Decoder enabled, these characters may be reported as a normal C5.0, or as a C1.7 or C2.7 (K28.5 with incorrect running disparity).

Table 5. Speed Select and Range Select Settings, all modes

FIFOBYP*	BYTE8/10*	ENCBYP*	SPDSEL	RANGESEL	REFCLK Frequency (MHz)	Serial Data Rate (MBd)	Multiplier Factor
HIGH	HIGH	X	LOW	LOW	10-20	50-100	x5
				HIGH	20-40	50-100	x2.5
			HIGH	LOW	10-20	100-200	x10
				HIGH	20-40	100-200	x5
	LOW	HIGH	LOW	LOW	10-20	50-100	x5
				HIGH	20-40	50-100	x2.5
			HIGH	LOW	10-20	100-200	x10
				HIGH	20-40	100-200	x5
		LOW	LOW	LOW	8.33-16.67	50-100	x6
				HIGH	16.67 -33.33	50-100	x3
			HIGH	LOW	8.33-16.67	100-200	x12
				HIGH	16.67 -33.33	100-200	x6
LOW	HIGH	X	LOW	LOW	10-20	50-100	x5
				HIGH	20-40	100-200	x5
			HIGH	LOW	10-20	100-200	x10
				HIGH	20-40	100-200	x5
	LOW	HIGH	LOW	LOW	10-20	50-100	x5
				HIGH	20-40	100-200	x5
			HIGH	LOW	10-20	100-200	x10
				HIGH	20-40	100-200	x5
		LOW	LOW	LOW	8.33-16.67	50-100	x6
				HIGH	16.67 -33.33	100-200	x6
			HIGH	LOW	8.33-16.67	100-200	x12
				HIGH	16.67 -33.33	100-200	x6



External Control of Data Flow

The Transmit Control State Machine supports three different types of external control:

- TXSTOP*
- TXHALT*
- TXINT

These control signal inputs are only interpreted when the Transmit FIFO is enabled. They effect the transmission of data by bringing external signals to the state machine without sending the signals through the Transmit FIFO.

TXSTOP* is used to stop transmission of the next packet or cell of data in the Transmit FIFO. When asserted (LOW) the Transmit Control State Machine continues to read and process characters in the Transmit FIFO until a location is read with the TXSOC bit set. Once a TXSOC is detected, the state machine sends out C5.0 fill characters until TXSTOP* is deasserted (HIGH) for one or more character times. When TXSTOP* is sampled deasserted it allows the next character with TXSOC set to be read from the Transmit FIFO and passed to the Encoder.

When TXSTOP* is used to control the flow of data, it is asserted (LOW) most of the time. To allow a cell or frame to pass, it only needs to be deasserted (HIGH) for one TXCLK cycle (assuming the transmit controller is at a cell boundary). Once the first character of the cell is transmitted the remainder of that cell is also processed. This allows the host system to control the transmission of data across the interface on a cell-by-cell or packet-by-packet basis.

TXHALT* (TXDATA[9]) is an immediate form of TXSTOP*. Instead of continuing to transmit data until a TXSOC is found, the assertion of TXHALT* causes character processing to stop at the next FIFO character location. No additional data is read from the Transmit FIFO until TXHALT* is deasserted (HIGH).

Note. If the Encoder is bypassed, TXDATA[9] is a data input and not TXHALT*. Since in this mode the interface does not interpret the TXSOC bit, the TXSTOP* signal assumes the same functionality as TXHALT*.

TXINT is used to send one of two interrupt characters from the local transmitter to a remote receiver. While it also bypasses the Transmit FIFO, it does not directly stop data transmission.

The Transmit Control State Machine responds to transitions on the TXINT input. When TXINT transitions from 0 → 1, a C0.0 (K28.0) Special Character code is inserted before the data character with which TXINT is associated is sent. When TXINT transitions from 1 → 0, a C3.0 (K28.3) Special Character code is sent. The reception of these characters generates an equivalent action on the attached receiver's RXINT status output.

The combination of RXHALF*, TXINT, RXINT, and TXHALT* may be used to prevent a remote FIFO overflow, which would result in lost data. This back-pressure mechanism can significantly improve data integrity in systems that cannot guarantee the full bandwidth of the host system at all times.

Elasticity Buffer

A short (8-character) FIFO is contained between the receive and transmit paths. This FIFO is used to separate the time domains of the received serial data stream and the outbound transmit data stream. This permits retransmission of received data without worry of jitter gain or jitter transfer. This allows

error-free transmission of the same data, when configured in daisy-chain or ring configurations, to an unlimited number of destinations.

This Elasticity Buffer is enabled when the LOOPTX input is asserted HIGH. This directs the receiver to place all non-C5.0 (K28.5) characters into the Elasticity Buffer. LOOPTX also directs the Transmit Control State Machine to read data from the Elasticity Buffer instead of from the Transmit FIFO.

While retransmitting data from the Elasticity Buffer, the Transmit FIFO is available for pre-loading of data to be transmitted. Once LOOPTX is deasserted (LOW), normal data transmission from the Transmit FIFO resumes.

This LOOPTX capability is only possible when sending 8-bit encoded data streams. It cannot be used with byte-packed or non-encoded data streams, and requires that the Transmit and Receive FIFOs are enabled. It also requires that the receiver be configured to process embedded commands (receiver Discard Policy cannot be 0). The reclocked connection may be required when sending non-8B/10B coded data streams, or data streams that cannot tolerate the data forwarding policies of the Elasticity Buffer.

Serial Line Receivers

Two differential line receivers, INA± and INB±, are available for accepting serial data streams, with the active input selected using the A/B* input. The DLB[1:0] inputs allow the transmit Serializer output to be selected as a third input serial stream, but this path is generally used only for diagnostic purposes. The serial line receiver inputs are all differential, and will accommodate wire interconnect with filtering losses or transmission line attenuation greater than 9dB ($V_{DIFF} \geq 200$ mV, or 400mV peak-to-peak differential) or can be directly connected to +5V fiber-optic interface modules (any ECL logic family, not limited to ECL 100K). The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages.

As can be seen in *Table 3* these inputs are configured to allow single-pin control for most applications. For those systems requiring selection of only INA± or INB±, the DLB[1:0] signals can be tied LOW, and the A/B selection can be performed using only A/B*. For those systems requiring only a single input and a local loopback, the A/B* can be tied HIGH or LOW, DLB[1] signal can be tied LOW and DLB[0] can be used for loopback control.

Signal Detect

The selected Line Receiver (that routed to the clock and data recovery PLL) is simultaneously monitored for:

- analog amplitude (>400 mV_{DIFF} pk-pk)
- transition density
- received data stream outside normal frequency range (± 400 ppm)
- and carrier detected.

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFI* (Link Fault Indicator) output, which changes synchronous to RXCLK. While link status is monitored internally at all times, it is necessary to have transitions on RXCLK to allow this signal to change externally.

**Clock/Data Recovery**

The extraction of a bit-rate clock and recovery of data bits from the received serial stream is performed within the Clock/Data Recovery (CDR) block. The clock extraction function is performed by a high-performance embedded phase-locked loop (PLL) that tracks the frequency of the incoming bit stream and aligns the phase of its internal bit-rate clock to the transitions in the serial data stream.

The CDR makes use of the clock present at the REFCLK input. It is used to ensure that the VCO (within the CDR) is operating at the correct frequency (rather than some harmonic of the bit rate), to improve PLL acquisition time, and to limit unlocked frequency excursions of the CDR VCO when no data is present at the serial inputs.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits for the range controls, the CDR PLL will track REFCLK instead of the data stream. When the frequency of the selected data stream returns to a valid frequency, the CDR PLL is allowed to track the received data stream. The frequency of REFCLK is required to be within ± 400 ppm of the frequency of the clock that drives the REFCLK signal at the remote transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the LFI* output can be used to select an alternate data stream. When an LFI* indication is detected, external logic can toggle selection of the INA $\pm$ and INB $\pm$ inputs through the A/B* input. When a port switch takes place, it is necessary for the PLL to re-acquire the new serial stream and frame to the incoming characters.

Clock Divider

This block contains the clock division logic, used to transfer the data from the Deserializer/Framer to the Decoder once every character (once every ten or twelve bits) clock. This counter is free running and generates outputs at the bit-rate divided by 10 (12 when the BYTE8/10* and ENCBYP* are LOW). When the Receive FIFO is bypassed, one of these generated clocks is driven out the RXCLK pin.

Deserializer/Framer

The CDR circuit extracts bits from the serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream looking for C5.0 (K28.5) characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

The framer operates in one of three different modes, as selected by the RFEN input. When RFEN is first asserted (HIGH), the framer is allowed to reset the internal character boundaries on any detected C5.0 character.

Random errors that occur in the serial data can corrupt some data patterns into a bit pattern identical to a K28.5, and thus cause an erroneous data-framing error. To prevent this, the CY7C924ADX provides a multi-byte framer that is enabled once RFEN has been HIGH for greater than 2048 character. This requires two C5.0 characters within a span of five characters, with both C5.0 characters located on identical 10-bit character boundary locations, before the framer is allowed to reset the internal character boundary. This multi-byte

framing option greatly reduces the possibility of erroneously reframing to an aliased K28.5 character.

If RFEN is LOW, the framer is disabled and no changes are made to character boundaries.

The framer in the CY7C924ADX operates by shifting the internal character position to align with the character clock. This ensures that the recovered clock does not contain any significant phase changes/hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other circuits using PLL-based logic elements.

Decoder Block

The decoder logic block performs two primary functions: decoding the received transmission characters back into Data and Special Character codes, and comparing generated BIST patterns with received characters to permit at-speed link and device testing.

10B/8B Decoder

The framed parallel output of the Deserializer is passed to the 10B/8B Decoder where, if the Decoder is enabled, it is transformed from a 10-bit transmission character back to the original Data and Special Character codes. This block uses the standard decoder patterns in *Tables 11* and *12* of this data sheet. Data patterns are indicated by a LOW on RXSC/D*, and Special Character codes are indicated by a HIGH. Invalid patterns or disparity errors are signaled as errors by a HIGH on RXRVS, and by specific Special Character codes.

If the Decoder is bypassed and BYTE8/10* is HIGH, the ten (10) data bits of each transmission character are passed unchanged from the framer to the Pipeline Register.

When the Decoder is bypassed and BYTE8/10* is LOW, the twelve (12) data bits of each transmission character are passed unchanged from the framer to the Pipeline Register.

BIST LFSR

The output register of the Decoder block is normally used to accumulate received characters for delivery to the Receive Formatter block. When configured for BIST mode (RXBISTEN* is LOW), this register becomes a signature pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). When enabled, this LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Transmitter. When synchronized with the received data stream, it checks each character in the Decoder with each character generated by the LFSR and indicates compare errors at the RXRVS output of the Receive Output Register.

The LFSR is initialized by the BIST hardware to the BIST loop start code of D0.0 (D0.0 is sent only once per BIST loop). Once the start of the BIST loop has been detected by the receiver, RXRVS is asserted for pattern mismatches between the received characters and the internally generated character sequence. Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXFULL* pulses asserted for one RXCLK cycle per BIST loop and can be used to check test pattern progress.

The specific patterns checked by the receiver are described in detail in the Cypress application note "HOTLink Built-In Self-Test." The sequence compared by the CY7C924ADX is



identical to that in the HOTLink CY7B933 receiver and the HOTLink II family of devices CYP(V)15G0x0x, allowing interoperable systems to be built when used at compatible serial signaling rates.

If a large number of errors are detected, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

Receive Formatter

The Receive Formatter performs three primary functions:

- Data formatting
- Address matching
- Byte-unpacking

Receive Data Formatting

The protocol enhancements of the transmit path are mirrored in the receive path logic. The majority of these enhancements require that the Receive FIFO be enabled to allow the CY7C924ADX to manage the data stream. In addition to the standard 10B/8B decoding used for character reception and recovery, the CY7C924ADX also supports:

- marking of packet or cell boundaries using RXSOC
- an expanded control/command character set
- ability to accept or discard data based on an embedded address
- the ability to filter receive data of non-essential information

All of these capabilities are supported for both 8- and 10-bit character sizes, and are made possible through use of the RXSOC bit. RXSOC is generated upon reception of the C8.0, C9.0, or C10.0 Special Character codes, in those modes where both the Receive FIFO and the Decoder are enabled.

The entries in *Table 6* show how the RXSOC, RXSC/D*, and RXRVS bits are formatted to indicate the reception of specific characters and character combinations. Normal Data and Special Character code characters are indicated by RXSOC being LOW (0). This allows the standard Special Characters codes to also be reported and output.

Table 6. Receive Data Formatting

RXSOC	RXSC/D*	RXRVS	Data Format Indication
0	0	0	Normal Data Character
0	0	1	Reserved
0	1	0	Normal Command Character
0	1	1	Received C0.7 Exception Character or Other Character Exception (as listed in <i>Table 12</i>)
1	0	0	Received Start of Cell Marker (C8.0) + Data Character
1	0	1	Received Illegal Sequence
1	1	0	Received Extended Command Marker (C9.0) + Data Character (interpreted as a command)
1	1	1	Received Serial Address Marker (C10.0) + Data Character (interpreted as an address)

Individual character errors that are not part of one of the supported sequences (Start of Cell, Extended Command, or Serial Address) are marked by the 011b (RXSOC = 0, RXSC/D* = 1, and RXRVS = 1) decode status.

Anytime RXSOC is reported HIGH (1) at least one of the C8.0, C9.0, or C10.0 characters was received as a valid character. If the immediately following character is a valid Data character, then the corresponding combination of RXSOC, RXSC/D*, and RXRVS indicate the type of information received. If the immediately following character is a Special Character code of any type (even a C5.0), then a 101b is posted to indicate an illegal sequence was received.

An illegal sequence can be caused by a remote transmitter sending incorrect information, or by receiving data corrupted during transmission. When such an error is detected, the 101b status bits are posted and the associated data field is set to the Special Character code that was received without error (C8.0, C9.0, or C10.0 reported as D8.0, D9.0, or D10.0 along with the 101b status). This information is provided to assist in debugging link or protocol faults.

The 100b indication is used to mark the associated Data character as the first character of a new frame, packet, cell, or other data construct used by the system. The Data characters and Special Character codes that follow this marker are written to the Receive FIFO (if the present address matching requirements are satisfied).

The 110b indication is used to mark the associated data character as the first character of an extended command. In reality there is no limit to the number of immediately following data characters that can be considered part of this command. The most common interpretation is based on the configured bus width, such that single-character configurations support the associated character as the extended command, providing up to 256 extended commands for 8-bit data and 1024 for 10-bit byte-packed data.

This marker is treated internally the same as the 100b Start Of Cell indication, which allows it to be used to mark the boundary of any user-specific information. As a boundary or cell marker, the immediately following data can be a data field, a header, a stream identifier, a transaction number, a packet length indicator, or any of a number of pieces of information connected to a data transfer.

Note. In reality, the 100b and 110b indicators can be used interchangeably; i.e., the 100b indication can be used to mark extended commands while the 110b indication can be used to mark the start of cells.

The 111b indication is used to mark the start of a Serial Address field. Unlike the Start Of Cell and Extended Command markers, which have no specific data-field length associated with them, the associated Serial Address is always comprised of the immediately following single data character, and supports a fixed 8-bit or 10-bit address field format in 8-bit or 10-bit byte-packed data formats.

When this serial address is received it may be passed to the Receive FIFO or discarded (see *Table 7*).

Address Matching

For those modes where address matching is enabled, the CY7C924ADX's ability to accept or discard data can be controlled by the remote transmitter. This is often useful in



configurations with one or more data sources and multiple data destinations.

Each CY7C924ADX contains an 8-bit or 10-bit Serial Address Register that is compared with the first data character received following a Serial Address marker (C10.0). This character constitutes an address, which can be configured for one of two modes for address matching. The first mode is used for multicast addresses, where a bit-wise AND is performed on each bit of the address character received, with the contents of each of the bits in the Serial Address Register. If any of the same bit locations in the register and the received data are both set to '1', a multicast address match is declared and the following data and Special Character codes are interpreted and passed to the Receive FIFO.

If the multicast address field is ever received as all 1s (FFh or 3FFh), the receiver always accepts the data. This all 1s setting is the broadcast address and is used to send data to all receivers.

This all 1s setting also has special meaning when written to the Serial Address Register. When the multicast address field is written to an all 1s (FFh or 3FFh) state, the receiver operates in promiscuous mode, and receives all data, regardless of the contents of any serial address commands received. This is also the default or power-up state of the Serial Address register.

The second mode of operation for address matching is when the Serial Address register contains a unique device address, and is compared with the character received following the C10.0 Serial Address marker. This unicast address requires an exact match between all 8 or 10 bits to declare a match found and allow the following data to pass.

When the Elasticity Buffer is enabled, all received characters (except C5.0) are written to the Elasticity Buffer, regardless of the state or configuration of any present address match. This allows one or more sources to send data to multiple receivers with the receivers connected in a ring or daisy-chain topology. By prefacing cells containing data with an address field, it is possible to have each receiver only process data specifically directed to it.

Byte-Unpacker

The Byte-Unpacker is used to re-assemble 10-bit characters from a received stream of decoded 8-bit characters. This reassembly process is designed to allow transmission of the same embedded commands, serial addresses, and Start of Cell markers that are used with 8-bit data characters. Because of the change in time per received encoded character versus delivered 10-bit data character, this unpacking process is only possible with the Receive FIFO enabled.

The byte-unpacker reverses the character segmentation shown in Figure 4. It takes five data characters and combines them into four 10-bit characters. This five-state unpacking process is re-started by the detection of any Special Character code in the Decoder, including the C5.0 (K28.5) fill character. Since usage of the Elasticity Buffer inserts and deletes C5.0 characters (as necessary) to handle the speed differences between the receive and transmit character clocks, it is not possible to send byte-packed data through the Elasticity Buffer. To send 10-bit packed data from one source to multiple destinations it is necessary to either use a star topology of interconnect, or make use of the buffered and reclocked serial input-to-output connections controlled by the Routing Matrix.

Receive Control State Machine

The Receive Control State Machine responds to multiple input conditions to control the routing and handling of received characters. It controls the staging of characters across various registers and the Receive FIFO. It also interprets all embedded Special Character codes, and converts the appropriate ones to specific bit combinations in the Receive FIFO. It controls the various discard policies and error control within the receiver, and operates in response to:

- the received character stream
- the detection and validation of serial addresses
- the room for additional data in the Receive FIFO
- the state of the receiver BIST enable (RXBISTEN*)
- the state of LOOPTX
- the state of FIFOBYP*.

These signals and conditions are used by the Receive Control State Machine to control the Receive Formatter, write access to the Receive FIFO, write access to the Elasticity Buffer, the Byte-Unpacker, the Receive Output register, and BIST. They determine the content of the characters passed to each of these destinations,

The Receive Control State Machine always operates synchronous to the recovered character clock (bit-clock/10 or bit-clock/12). When the Receive FIFO is bypassed, RXCLK becomes an output that changes synchronous to the internal character clock. RXCLK operates at the same frequency as the internal character clock.

Discard Policies

When the Receive FIFO is enabled, the Receive Control State Machine has the ability to selectively discard specific characters from the data stream that are determined by the present configuration as being unnecessary. When discarding is enabled, it reduces the host system overhead necessary to keep the Receive FIFO from overflowing and losing data.

The discard policy is configured as part of the operating mode and is set using the RXMODE[1:0] inputs. The four discard policies are listed in Table 7.

Table 7. Receiver Discard Policies

Policy #	RXMODE[1:0]	Policy Description
0	00	Keep all received characters
1	01	Process Commands, discard all but the last C5.0 character
2	10	Process Commands, discard all C5.0 characters
3	11	Process Commands, discard all C5.0 characters, discard serial addresses

Policy 0 is the simplest and also applies for all conditions where the Receive FIFO is bypassed. In this mode, every character that is received is placed into the Receive FIFO (when enabled) or into the Receive Output Register.

In discard policy 1, all Start Of Cell, extended command, and serial address commands are processed as they are received. The C5.0 character, which is automatically transmitted when no data is present in the Transmit FIFO, is treated differently here. In this mode, whenever two or more adjacent C5.0



characters are received, all of them are discarded except the last one received before any other character type. This allows these fill characters to be removed from the data stream, but does not change the data flow for protocols (like Fibre Channel) that use a single C5.0 character as a delimiter.

Policy 2 is identical to policy 1 except that all C5.0 characters are removed from the data stream.

Policy 3 is a super-set of policy 2, where the serial address is also discarded.

When the FIFOs are bypassed (FIFOBYP* LOW), no characters are actually discarded, but the receiver discard policy can be used to control external filtering of the data. The RXEMPTY* FIFO flag is used to indicate if the character on the output bus is valid or not. In discard policy 0, the RXEMPTY* flag is always deasserted to indicate that valid data is always present. In discard policy 1 when a series of C5.0 characters are received, the RXEMPTY* flag indicates an empty condition for all but the last C5.0 character before any other character is presented. In discard policies 2 or 3, the RXEMPTY* flag indicates an empty condition for all C5.0 characters. When any other character is present, this flag indicates that valid or "interesting" Data or Special Characters are present.

Receive FIFO

The Receive FIFO is used to buffer data captured from the selected serial stream for later processing by the host system. This FIFO is sized to hold 256, 14-bit characters. When the FIFO is enabled, it is written to by the Receive Control State Machine. When data is present in the Receive FIFO (as indicated by the RXFULL*, RXHALF*, and RXEMPTY* Receive FIFO status flags), it can be read from the Output Register by asserting AM* and RXEN*.

The read port on the Receive FIFO may be configured for the same two timing models as the transmit interface: UTOPIA and Cascade. Both are forms of a FIFO interface. The UTOPIA timing model (EXTFIFO = L) has active LOW, RXEMPTY* and RXFULL* status flags, and an active LOW, RXEN* enable. When configured for Cascade operation (EXTFIFO = H), these same signals are all active HIGH. The RXHALF* signal is always active LOW, regardless of EXTFIFO setting. Either timing model supports connection to various host bus interfaces, state machines, or external FIFOs for depth expansion (see Figure 5).

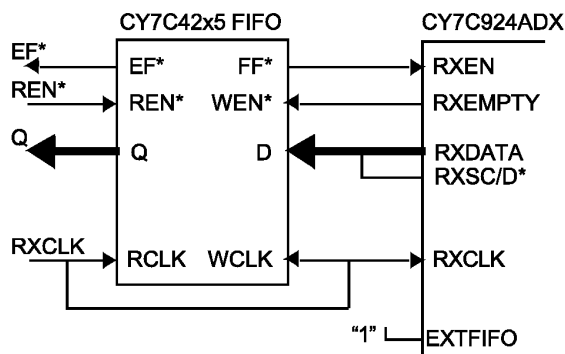


Figure 5. External FIFO Depth Expansion of the CY7C924ADX Receive Data Path

The Receive FIFO presents Full, Half-Full, and Empty FIFO status flags. These flags are provided synchronous to RXCLK to allow operation with a Moore-type external controlling state machine. When configured with the Receive FIFO enabled, RXCLK is an input. When the Receive FIFO is bypassed (FIFOBYP* is LOW), RXCLK is an output operating at the received character rate.

Receive Input Register

The input register is clocked by the rising edge of RXCLK. It samples numerous signals that control the reading of the Receive FIFO and operation of the Receive Control State Machine.

Receive Output Register

The Receive Output Register changes in response to the rising edge of RXCLK. When the Receive FIFO is enabled (FIFOBYP* = H), the FIFO status flag outputs of this register are placed in a High-Z state when the CY7C924ADX is not addressed (AM* is sampled HIGH). The RXDATA bus output drivers are enabled when the device is selected by RXEN* being asserted in the RXCLK cycle immediately following that in which the device was addressed (AM* is sampled LOW), and RXEN* being sampled by RXCLK. This initiates a Receive FIFO read cycle.

Just as with the TXDATA bus on the Transmit Input Register, the receive outputs are also mapped by the specific decoding and bus-width selected by the ENCBYP*, BYTE8/10* and FIFOBYP* inputs. These assignments are shown in Table 8.

When the Decoder and Receive FIFO are both enabled, the Receive Control State Machine interprets and discards (except in discard policy 0) received C0.0 and C3.0 command codes as set and clear directives for the RXINT output. This allows the RXINT output to duplicate the state transitions presented to the TXINT input at the source end of the link. This RXINT output can be used, along with TXHALT*, TXINT, and RXHALF*, to implement a back-pressure mechanism for the Receive FIFO, or for other time dependent signalling.

If the Receive FIFO and Decoder are bypassed, all received characters are passed directly to the Receive Output Register. If framing is enabled, and K28.5 characters have been detected meeting the present framing requirements, the output characters will appear on proper character boundaries. If framing is disabled (RFEN is LOW) or K28.5 characters have not been detected in the data stream, the received characters may not be output on their proper 10-bit boundaries. In this mode, some form of external framing and decoding/descrambling must be used to recover the original source data.

Serial Address Register

When the device is in Utopia mode (EXTFIFO = LOW), the receiver is capable of selectively accepting or discarding received data based on an address received in the data stream. The address matching capability allows for the choice of matching of either domains (multicast) or exact addresses (unicast). The 8- or 10-bit Serial Address Register represents a single character address field as shown in Figure 6.

The multicast mode is bit-specific and allows allocation of up to 8 or 10 separate domains. In the unicast address mode the match is character specific and identifies up to 256 or 1024 destination addresses. A device can either belong to one or more domains, or it can have a single unique address.

Table 8. Receive Output Bus Signal Map

	Receive Decoder Mode ^[3]			
	Decoded 10-bit Character Stream (8-bit characters)	Undecoded 10-bit Character Stream	Decoded 10-bit Byte-Packed Character Stream (10-bit characters)	Undecoded 12-bit Character Stream
ENCBYP*	HIGH	LOW	HIGH	LOW
BYTE8/10*	HIGH	HIGH	LOW	LOW
RXDATA Bus I/O Bit				
RXSC/D*	RXSC/D*		RXSC/D*	
RXDATA[0]	RXD[0]	RXD[0] ^[3]	RXD[0]	RXD[0] ^[3]
RXDATA[1]	RXD[1]	RXD[1]	RXD[1]	RXD[1]
RXDATA[2]	RXD[2]	RXD[2]	RXD[2]	RXD[2]
RXDATA[3]	RXD[3]	RXD[3]	RXD[3]	RXD[3]
RXDATA[4]	RXD[4]	RXD[4]	RXD[4]	RXD[4]
RXDATA[5]	RXD[5]	RXD[5]	RXD[5]	RXD[5]
RXDATA[6]	RXD[6]	RXD[6]	RXD[6]	RXD[6]
RXDATA[7]	RXD[7]	RXD[7]	RXD[7]	RXD[7]
RXINT/RXDATA[8] (FIFOBYP*=HIGH)	RXINT	RXD[8]	RXD[8]	RXD[8]
RXINT/RXDATA[8] (FIFOBYP*=LOW)		RXD[8]	RXD[8]	RXD[8]
RXDATA[9]	(LOW)	RXD[9]	RXD[9]	RXD[9]
RXRVS/RXDATA[10]	RXRVS		RXRVS	RXD[10]
RXSOC/RXDATA[11]	RXSOC		RXSOC	RXD[11]

When a serial address is received and a match is detected, the address, and all data following that address, is passed to the Receive FIFO (except in discard policy 3 where the address is discarded). This continues until a serial address is received that does not match the contents of the Address Register, whereupon writes to the Receive FIFO are inhibited. The Serial Address Register has a power-up default state where the multicast field set to an all ones condition (FFh or 3FFh). When set to this value the receiver accepts all data, regardless of the presence or content of any received serial address. This "promiscuous" address can also be forced by the momentary assertion of the RESET*[1:0] pair.

The Serial Address Register is only used when the receiver is operated with the Receive FIFO enabled (FIFOBYP* is HIGH) and in operating modes where the discard policy is not 0 (see Table 7 for a list of discard policies).

Serial Address Register Access

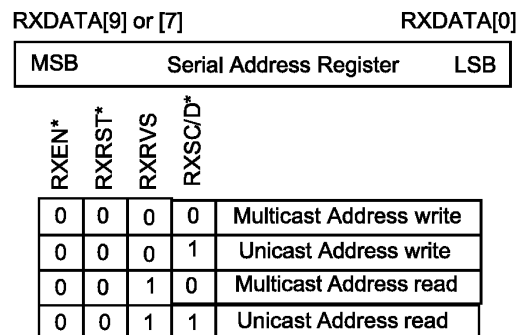
The Serial Address Register is accessed through the RXDATA bus. Both reads and writes to the register require the device to be addressed (AM* is LOW) and for RXRST* to be asserted (LOW).

Note:

- First bit shifted in. Others follow in numerical order interpreted from an NRZ pattern.

When accessed for write or read operations, the RXRVS signal is used as a read/write selector, and RXSC/D* is used to select the operating mode (multicast or unicast) of the Serial Address Register.

Address Register Content


Figure 6. Serial Address Register Format and Access



CY7C924ADX

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +6.5V

DC Voltage Applied to Outputs

in High-Z State -0.5V to $V_{DD}+0.5V$

Output Current into TTL Outputs (LOW) 30 mA

DC Input Voltage -0.5V to $V_{DD}+0.5V$

Static Discharge Voltage > 2001 V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5.0V ± 10%
Industrial	-40°C to +85°C	5.0V ± 10%

CY7C924ADX DC Electrical Characteristics Over the Operating Range

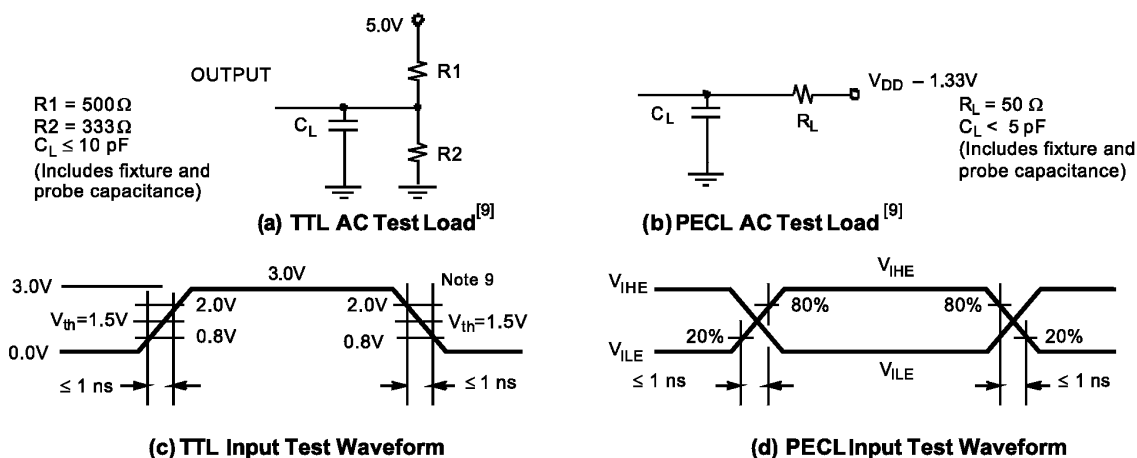
Parameter	Description	Test Conditions	Min.	Max.	Unit
TTL Outputs					
V_{OHT}	Output HIGH Voltage	$I_{OH} = -2 \text{ mA}$, $V_{DD} = \text{Min.}$	2.4		V
V_{OLT}	Output LOW Voltage	$I_{OL} = 8 \text{ mA}$, $V_{DD} = \text{Min.}$		0.4	V
I_{OST}	Output Short Circuit Current	$V_{OUT} = 0V^{[4]}$	-30	-80	mA
I_{OZL}	High-Z Output Leakage Current		-20	20	μA
TTL Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{DD}	V
V_{ILT}	Input LOW Voltage		-0.5	0.8	V
I_{IHT}	Input HIGH Current	$V_{IN} = V_{DD}$		+40	μA
I_{ILT}	Input LOW Current	$V_{IN} = 0.0V$		-40	μA
I_{IHPD}	Input HIGH Current	$V_{IN} = V_{DD}$, Pins with internal pull-down		+300	μA
I_{ILPU}	Input LOW Current	$V_{IN} = 0.0V$, Pins with internal pull-up	-300		μA
Transmitter PECL-Compatible Output Pins: OUTA+, OUTA-, OUTB+, OUTB-^[5]					
V_{OHE}	Output HIGH Voltage (V_{DD} referenced)	Load = 50Ω to $V_{DD} - 1.33V$ $R_{CURSET} = 10k$	$V_{DD} - 1.03$	$V_{DD} - 0.83$	V
V_{OLE}	Output LOW Voltage (V_{DD} referenced)	Load = 50Ω to $V_{DD} - 1.33V$ $R_{CURSET} = 10k$	$V_{DD} - 2$	$V_{DD} - 1.62$	V
V_{ODF}	Output Differential Voltage (OUT+) - (OUT-)	Load = 50Ω to $V_{DD} - 1.33V$ $R_{CURSET} = 10k$	600	1100	mV
Receiver Single-ended PECL-compatible Input Pin: CARDET					
V_{IHE}	Input HIGH Voltage (V_{DD} referenced)		$V_{DD} - 1.165$	V_{DD}	V
V_{ILE}	Input LOW Voltage (V_{DD} referenced)		2.5	$V_{DD} - 1.475$	V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHE}(\text{min.})$		+40	μA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILE}(\text{max.})$	-40		μA
Differential Line Receiver Input Pins: INA+, INA-, INB+, INB-					
V_{DIFF}	Input Differential Voltage (IN+) - (IN-)		200	2500	mV
V_{IHH}	Highest Input HIGH Voltage			V_{DD}	V
V_{ILL}	Lowest Input LOW Voltage		2.5		V
I_{IHH}	Input HIGH Current	$V_{IN} = V_{IHH} \text{ Max.}$		750	μA
$I_{ILL}^{[6]}$	Input LOW Current	$V_{IN} = V_{ILL} \text{ Min.}$	-200		μA
Miscellaneous			Typ.	Max.	
$I_{DD}^{[7]}$	Power Supply Current	Freq. = Max.	170	250	mA

Notes:

- Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
- The output current and (resulting voltage swing) is set using a single resistor between CURSETx and V_{SS} . This CURSET resistor value is calculated as $R_{CURSET} = (90 \times Z_{LOAD}) / V_{ODF}$, where Z_{LOAD} is the differential load between the true and complement outputs of the differential driver.
- To guarantee positive currents for all PECL voltages, an external pull-down resistor must be present.
- Maximum I_{DD} is measured with $V_{DD} = \text{MAX}$, RFEN = LOW, and outputs unloaded. Typical I_{DD} is measured with $V_{DD} = 5.0V$, $T_A = 25^\circ\text{C}$, RFEN = LOW, and outputs unloaded.

Capacitance^[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	$T_A = 25^\circ\text{C}$, $f_0 = 1\text{ MHz}$, $V_{DD} = 5.0\text{V}$	7	pF
C_{INPECL}	PECL-compatible input Capacitance	$T_A = 25^\circ\text{C}$, $f_0 = 1\text{ MHz}$, $V_{DD} = 5.0\text{V}$	4	pF

AC Test Loads and Waveforms

CY7C924ADX Transmitter TTL Switching Characteristics, FIFO Enabled Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{TS}	TXCLK Clock Cycle Frequency With Transmit FIFO Enabled		50	MHz
t_{TXCLK}	TXCLK Period	20		ns
t_{TXCPWH}	TXCLK HIGH Time	6.5		ns
t_{TXCPWL}	TXCLK LOW Time	6.5		ns
$t_{TXCLR}^{[8]}$	TXCLK Rise Time ^[10]	0.7	5	ns
$t_{TXCLF}^{[8]}$	TXCLK Fall Time ^[10]	0.7	5	ns
t_{TXA}	Flag Access Time From TXCLK $\uparrow$ to Output	2	15	ns
t_{TXDS}	Transmit Data Set-Up Time to TXCLK $\uparrow$	4		ns
t_{TXDH}	Transmit Data Hold Time from TXCLK $\uparrow$	1		ns
t_{TXENS}	Transmit Enable Set-Up Time to TXCLK $\uparrow$	4		ns
t_{TXENH}	Transmit Enable Hold Time from TXCLK $\uparrow$	1		ns
t_{TXRSS}	Transmit FIFO Reset (TXRST*) Set-Up Time to TXCLK $\uparrow$	4		ns
t_{TXRSH}	Transmit FIFO Reset (TXRST*) Hold Time from TXCLK $\uparrow$	1		ns
t_{TXAMS}	Transmit Address Match (AM*) Set-Up Time to TXCLK $\uparrow$	4		ns
t_{TXAMH}	Transmit Address Match (AM*) Hold Time from TXCLK $\uparrow$	1		ns
t_{TXZA}	Sample of AM* LOW by TXCLK $\uparrow$, Output High-Z to Active HIGH or LOW	0		ns
t_{TXOE}	Sample of AM* LOW by TXCLK $\uparrow$ to Output Valid	1.5	20	ns
t_{TXAZ}	Sample of AM* HIGH by TXCLK $\uparrow$ to Output in High-Z	1.5	20	ns

Notes:

8. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
9. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
10. Input/output rise and fall time is measured between 0.8V and 2.0V.

**CY7C924ADX Receiver TTL Switching Characteristics, FIFO Enabled** Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{RIS}	RXCLK Clock Cycle Frequency With Receive FIFO Enabled		50	MHz
$t_{RXCLKIP}$	RXCLK Input Period	20		ns
t_{RXCPWH}	RXCLK Input HIGH Time	6.5		ns
t_{RXCPWL}	RXCLK Input LOW Time	6.5		ns
$t_{RXCLKIR}^{[8]}$	RXCLK Input Rise Time ^[10]	0.7	5	ns
$t_{RXCLKIF}^{[8]}$	RXCLK Input Fall Time ^[10]	0.7	5	ns
t_{RXENS}	Receive Enable Set-Up Time to RXCLK $\uparrow$	4		ns
t_{RXENH}	Receive Enable Hold Time from RXCLK $\uparrow$	1		ns
t_{RXRSS}	Receive FIFO Reset (RXRXT*) Set-Up Time to RXCLK $\uparrow$	4		ns
t_{RXRSH}	Receive FIFO Reset (RXRXT*) Hold Time from RXCLK $\uparrow$	1		ns
t_{RXAMS}	Receive Address Match (AM*) Set-Up Time to RXCLK $\uparrow$	4		ns
t_{RXAMH}	Receive Address Match (AM*) Hold Time from RXCLK $\uparrow$	1		ns
$t_{RXA}^{[11]}$	Flag and Data Access Time from RXCLK $\uparrow$ to Output	1.5	15	ns
$t_{RXZA}^{[11]}$	Sample of AM* LOW by RXCLK $\uparrow$, Output High-Z to Active HIGH or LOW, or Sample of RXEN* Asserted by RXCLK $\uparrow$, Output High-Z to Active HIGH or LOW	0		ns
$t_{RXOE}^{[11]}$	Sample of AM* LOW by RXCLK $\uparrow$ to Output Valid, ^[11] or Sample of RXEN* Asserted by RXCLK $\uparrow$ to RXDATA Outputs Valid	1.5	20	ns
$t_{RXAZ}^{[11]}$	Sample of AM* HIGH by RXCLK $\uparrow$ to Output in High-Z, ^[11] or Sample of RXEN* Deasserted by RXCLK $\uparrow$ to RXDATA Outputs in High-Z	1.5	20	ns

CY7C924ADX Transmitter TTL Switching Characteristics, FIFO Bypassed Over the Operating Range

Parameter	Description	Min.	Max.	Unit
t_{TRA}	Flag Access Time From REFCLK $\uparrow$ to Output	2	15	ns
t_{REFDS}	Write Data Set-Up Time to REFCLK $\uparrow$	4		ns
t_{REFDH}	Write Data Hold Time from REFCLK $\uparrow$	2		ns
t_{REFENS}	Transmit Enable Set-Up Time to REFCLK $\uparrow$	4		ns
t_{REFENH}	Transmit Enable Hold Time from REFCLK $\uparrow$	2		ns
t_{REFAMS}	Transmit Address Match (AM*) Set-Up Time to REFCLK $\uparrow$	4		ns
t_{REFAMH}	Transmit Address Match (AM*) Hold Time from REFCLK $\uparrow$	2		ns
t_{REFZA}	Sample of AM* LOW by REFCLK $\uparrow$, Output High-Z to Active HIGH or LOW	0		ns
t_{REFOE}	Sample of AM* LOW by REFCLK $\uparrow$ to Flag Output Valid	1.5	20	ns
t_{REFAZ}	Sample of AM* HIGH by REFCLK $\uparrow$ to Flag Output High-Z	1.5	20	ns

CY7C924ADX Receiver TTL Switching Characteristics, FIFO Bypassed Over the Operating Range

Parameter	Description	Min.	Max.	Unit
$f_{ROS}^{[12]}$	RXCLK Clock Output Frequency—100 to 200 MBaud (RANGESEL is HIGH, ENCBYP* is HIGH or BYTE8/10* is HIGH)	10	20	MHz
	RXCLK Clock Output Frequency—50 to 100 MBaud (RANGESEL is LOW, ENCBYP* is HIGH or BYTE8/10* is HIGH)	5	10	MHz
	RXCLK Clock Output Frequency—100 to 200 MBaud 12-bit Encoder Bypass Operation (RANGESEL is HIGH, ENCBYP* is LOW and BYTE8/10* is LOW)	8.33	16.67	MHz
	RXCLK Clock Output Frequency—50 to 100 MBaud 10-bit Operation (RANGESEL is LOW, ENCBYP* is LOW and BYTE8/10* is LOW)	4.16	8.33	MHz
$t_{RXCLKOP}$	RXCLK Output Period	25	250	ns
$t_{RXCLKOD}$	RXCLK Output Duty Cycle	40	60	%
$t_{RXCLKOR}^{[8]}$	RXCLK Output Rise Time ^[10]	0.25	2	ns

**CY7C924ADX Receiver TTL Switching Characteristics, FIFO Bypassed** Over the Operating Range (continued)

Parameter	Description	Min.	Max.	Unit
$t_{RXCLKOF}^{[8]}$	RXCLK Output Fall Time ^[10]	0.25	2	ns
t_{RXENS}	Receive Enable Set-Up Time to RXCLK $\uparrow$	4		ns
t_{RXENH}	Receive Enable Hold Time from RXCLK $\uparrow$	1		ns
$t_{RXZA}^{[11]}$	Sample of AM* LOW by RXCLK $\uparrow$, Outputs High-Z to Active Sample of RXEN* Asserted by RXCLK $\uparrow$ to RXDATA Outputs High-Z to Active	0		ns
$t_{RXOE}^{[11]}$	Sample of AM* LOW by RXCLK $\uparrow$ to Flag Output Valid Sample of RXEN* Asserted by RXCLK $\uparrow$ to RXDATA Output Low-Z	1.5	20	ns
$t_{RXAZ}^{[11]}$	Sample of AM* HIGH by RXCLK $\uparrow$ to Flag Output High-Z Sample of RXEN* Deasserted by RXCLK $\uparrow$ to RXDATA Output High-Z	1.5	20	ns

CY7C924ADX Receiver Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
$t_B^{[15]}$	Bit Time	5.0	20.0	ns
t_{IN_J}	IN $\pm$ Peak-to-Peak Input Jitter Tolerance ^[13, 14]		0.5	UI
t_{SA}	Static Alignment ^[8, 16]		600	ps
t_{EFW}	Error Free Window ^[8, 13, 17]	0.65		UI

CY7C924ADX Transmitter Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
$t_B^{[15]}$	Bit Time	5.0	20.0	ns
t_{RISE}	PECL-compatible Output Rise Time 20–80% (PECL Test Load) ^[8]	200	1700	ps
t_{FALL}	PECL-compatible Output Fall Time 80–20% (PECL Test Load) ^[8]	200	1700	ps
t_{DJ}	Deterministic Jitter (peak-peak) ^[8, 18]		0.02	UI
t_{RJ}	Random Jitter (σ) ^[8, 19]		0.008	UI
t_{JT}	Transmitter Total Output Jitter (pk-pk) ^[8]		0.08	UI

CY7C924ADX REFCLK Input Switching Characteristics Over the Operating Range

Parameter	Description	Conditions			Min.	Max	Unit
		SPDSEL	RANGESEL	BYTE8/10*			
f_{REF}	REFCLK Clock Frequency—50 to 100 MBaud, 10-bit mode, encoder bypass, REFCLK = 2x character rate	0	0	0	8.33	16.67	MHz
	REFCLK Clock Frequency—50 to 100 MBaud, 8-bit mode, REFCLK = 2x character rate	0	0	1	10	20	MHz

Notes:

- Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.
- The period of f_{ROS} will match the period of the transmitter PLL reference (REFCLK) when receiving serial data. When data is interrupted, RXCLK may drift to REFCLK ± 2500 ppm.
- Receiver UI (Unit Interval) is calculated as $1/(\text{Serial Baud Rate})$, where Baud Rate is the rate of change of signaling.
- The specification is sum of 25% Duty Cycle Distortion (DCD), 10% Data Dependant Jitter (DDJ), 15% Random Jitter (RJ).
- The PECL switching threshold is the midpoint between the V_{OHE} and V_{OLE} specifications (approximately $V_{DD} - 1.33V$).
- Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by the absolute difference of the left and right edge shifts ($|t_{SH_L} - t_{SH_R}|$) of one bit until a character error occurs.
- Error Free Window is a measure of the time window between bit centers where a transition may occur without causing a bit sampling error. EFW is measured over the operating range, input jitter < 50% Dj.
- While sending continuous K28.5s, outputs loaded to 50Ω to $V_{DD} - 1.33V$, over the operating range.
- While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.

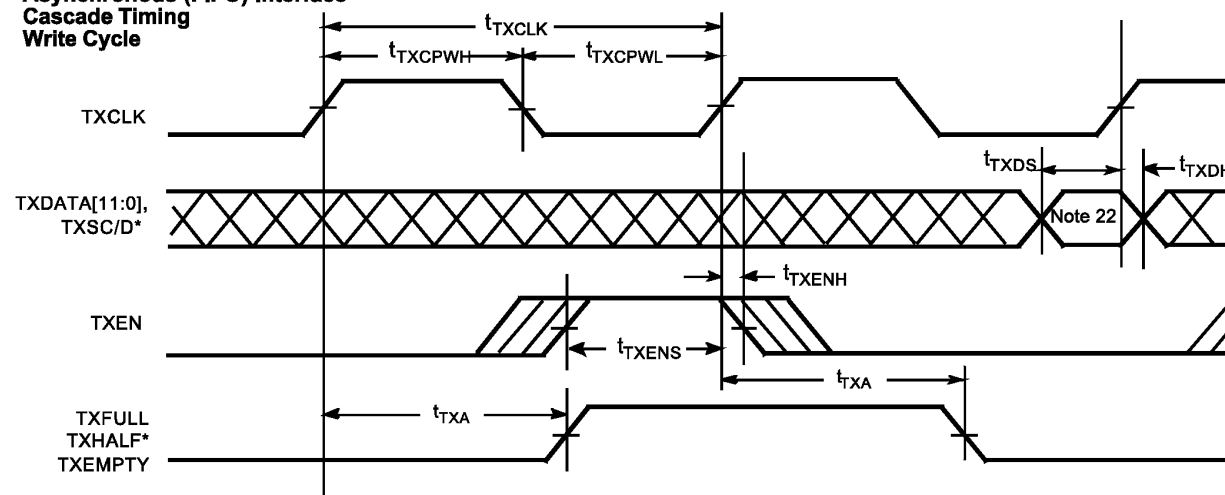


CY7C924ADX REFCLK Input Switching Characteristics Over the Operating Range

Parameter	Description	Conditions			Min.	Max	Unit
		SPDSEL	RANGESEL	BYTE8/10*			
f _{REF}	REFCLK Clock Frequency—50 to 100 MBaud, 10-bit mode, encoder bypass, REFCLK = 4x character rate	0	1 ^[20]	0	16.67	33.33	MHz
	REFCLK Clock Frequency—50 to 100 MBaud, 8-bit mode, REFCLK = 4x character rate	0	1 ^[20]	1	20	40	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 10-bit mode, encoder bypass, REFCLK = character rate	1	0	0	8.33	16.67	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 8-bit mode, REFCLK = character rate	1	0	1	10	20	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 10-bit mode, encoder bypass, REFCLK = 2x character rate	1	1	0	16.67	33.3	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 8-bit mode, REFCLK = 2x character rate	1	1	1	20	40	MHz
t _{REFCLK}	REFCLK Period				25	120	ns
t _{REFH}	REFCLK HIGH Time				6.5		ns
t _{REFL}	REFCLK LOW Time				6.5		ns
t _{REFRX}	REFCLK Frequency Referenced to Received Clock Period ^[21]				-0.04	+0.04	%

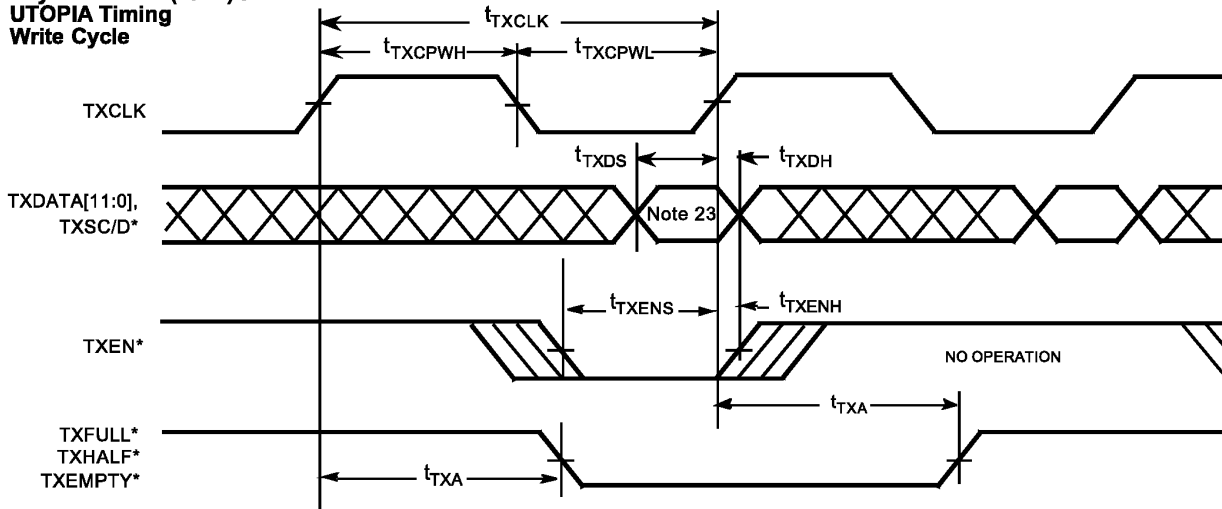
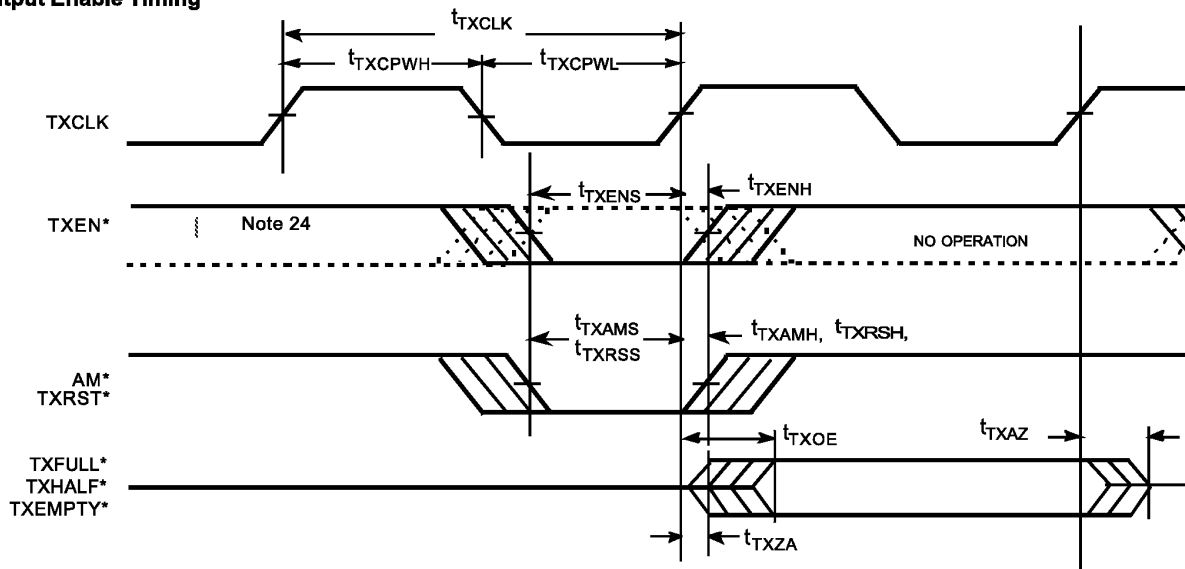
CY7C924ADX HOTLink Transmitter Switching Waveforms

**Asynchronous (FIFO) Interface
Cascade Timing
Write Cycle**



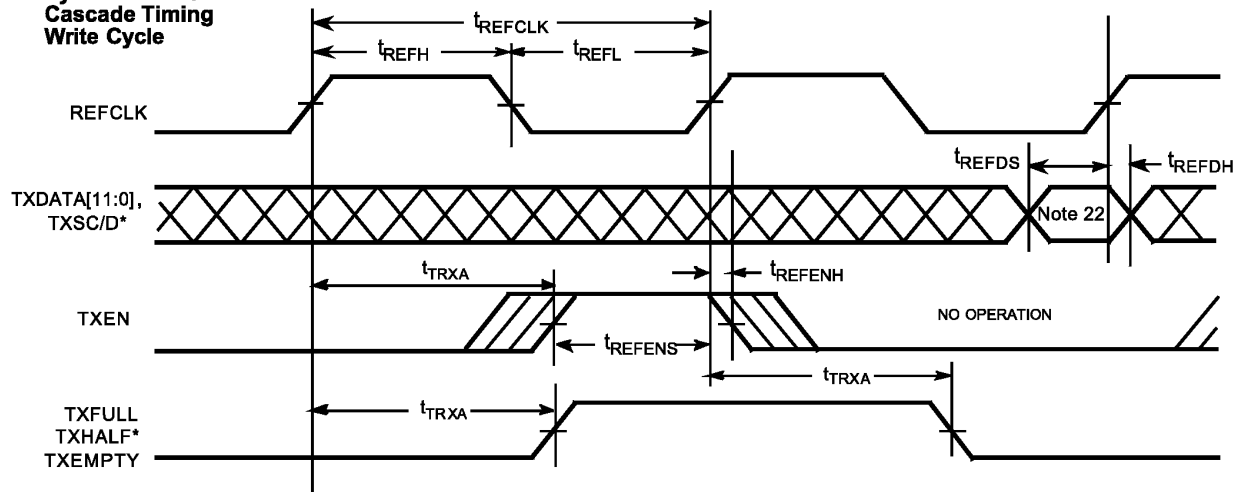
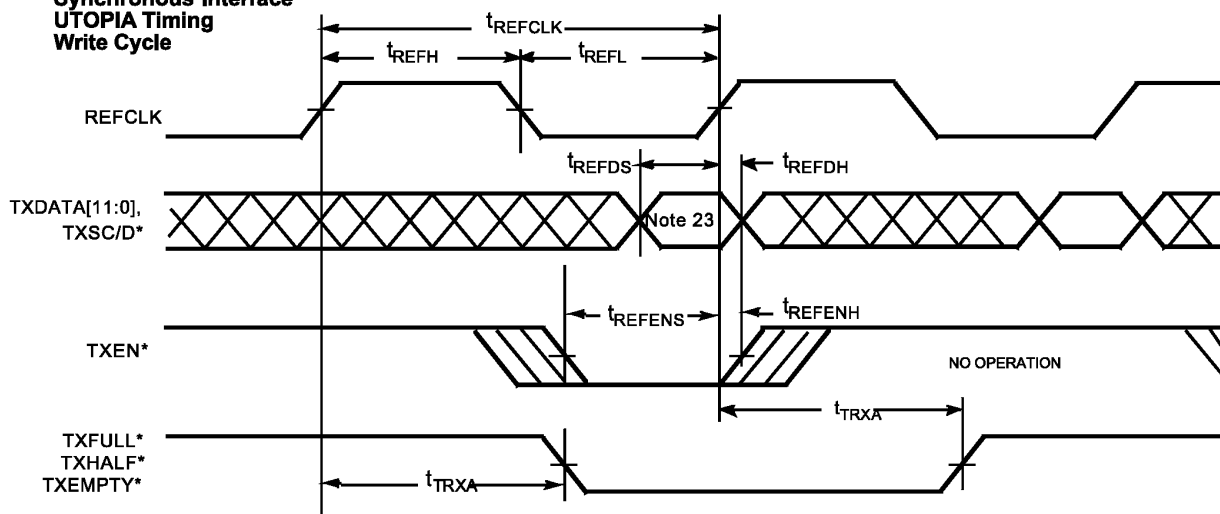
Notes:

20. When configured for synchronous operation with the FIFOs bypassed (FIFOBYP* is LOW), if RANGESEL is HIGH the SPDSEL input is ignored and operation is forced to the 100–200 MBaud range.
21. REFCLK has no phase or frequency relationship with RXCLK and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within $\pm 0.04\%$ of the transmitter PLL reference (REFCLK) frequency.
22. When transferring data to the Transmit FIFO from a depth expanded external FIFO (EXTFIFO = H), the data is captured from the external FIFO one clock cycle following the actual enable.

CY7C924ADX HOTLink Transmitter Switching Waveforms (continued)
**Asynchronous (FIFO) Interface
UTOPIA Timing
Write Cycle**

**Asynchronous (FIFO) Interface
Output Enable Timing**

Notes:

23. When writing data from a UTOPIA compliant interface (EXTFIFO = L), the write data is captured on the same clock cycle as the data.

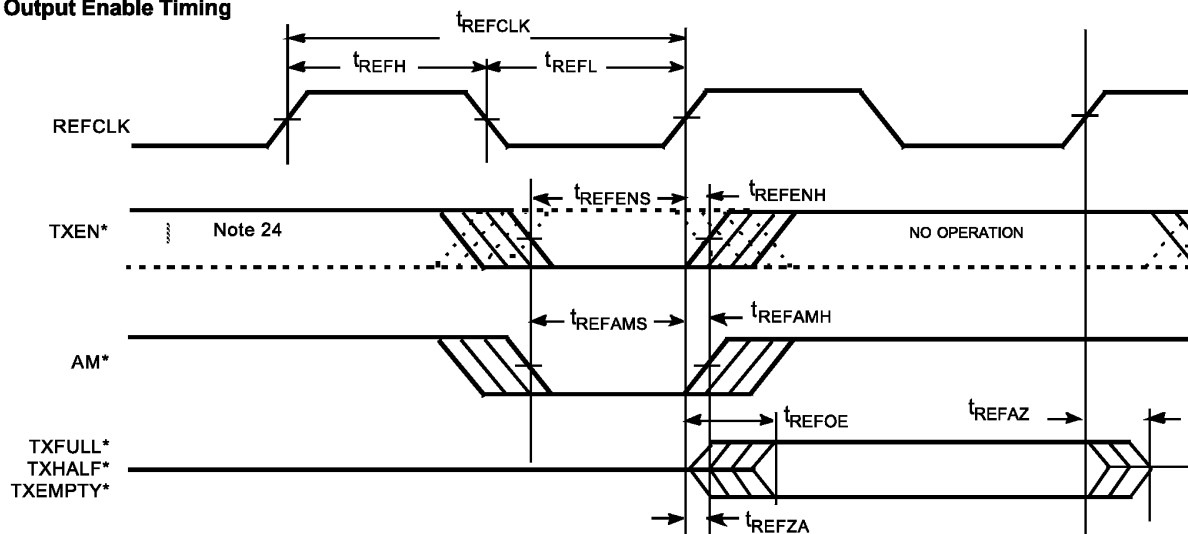
24. Signals shown as dotted lines represent the differences in timing and active state of signals when operated in Cascade Timing.

**CY7C924ADX HOTLink Transmitter Switching Waveforms** (continued)**Synchronous Interface
Cascade Timing
Write Cycle****Synchronous Interface
UTOPIA Timing
Write Cycle**



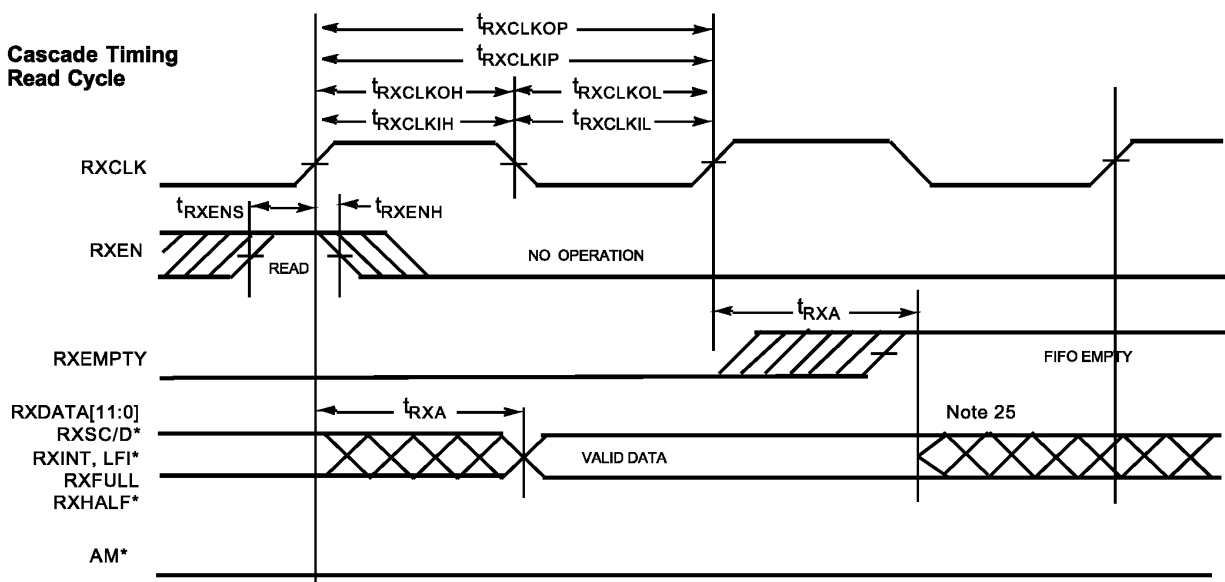
CY7C924ADX HOTLink Transmitter Switching Waveforms (continued)

Synchronous Interface Output Enable Timing



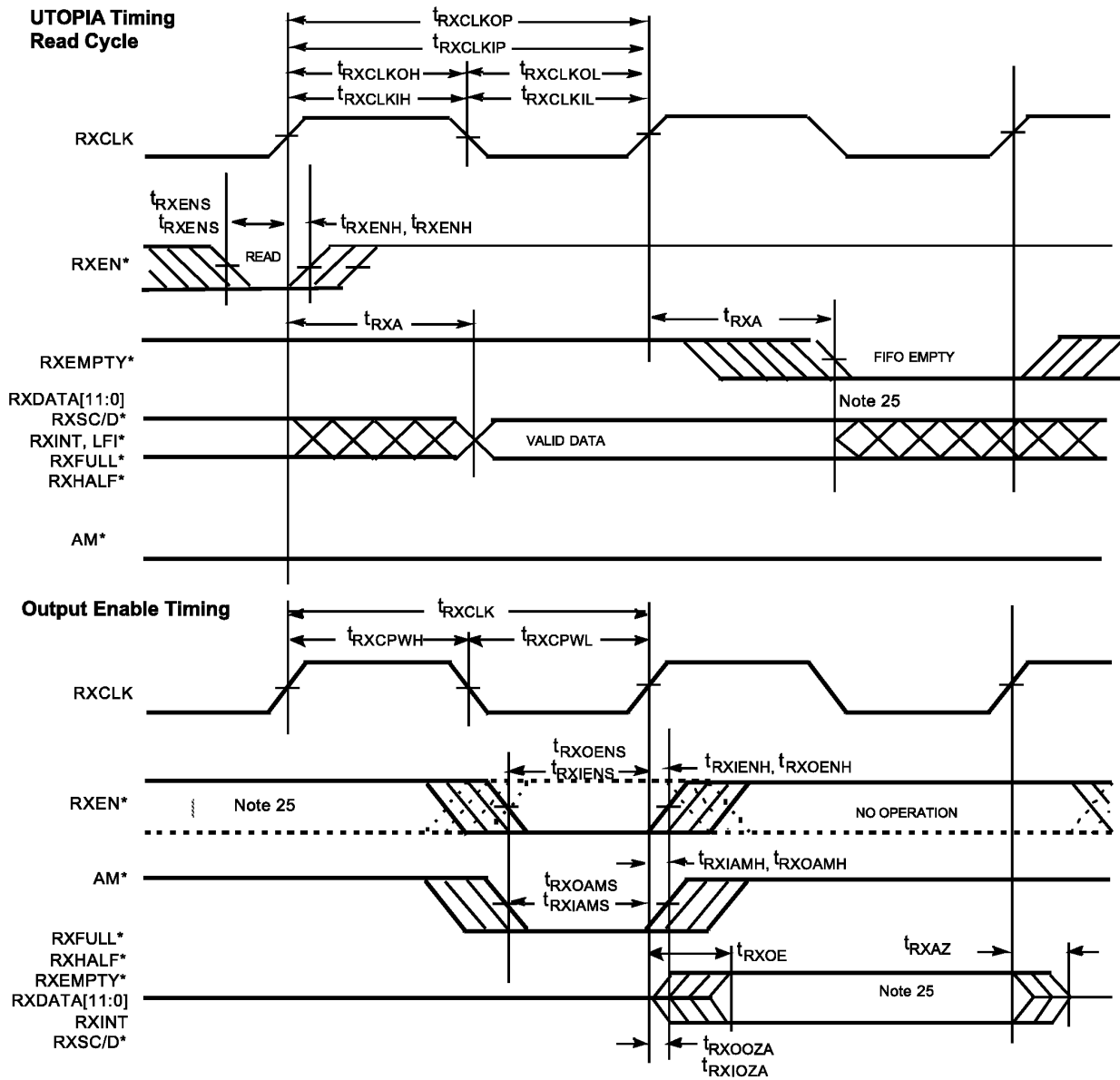
CY7C924ADX HOTLink Receiver Switching Waveforms

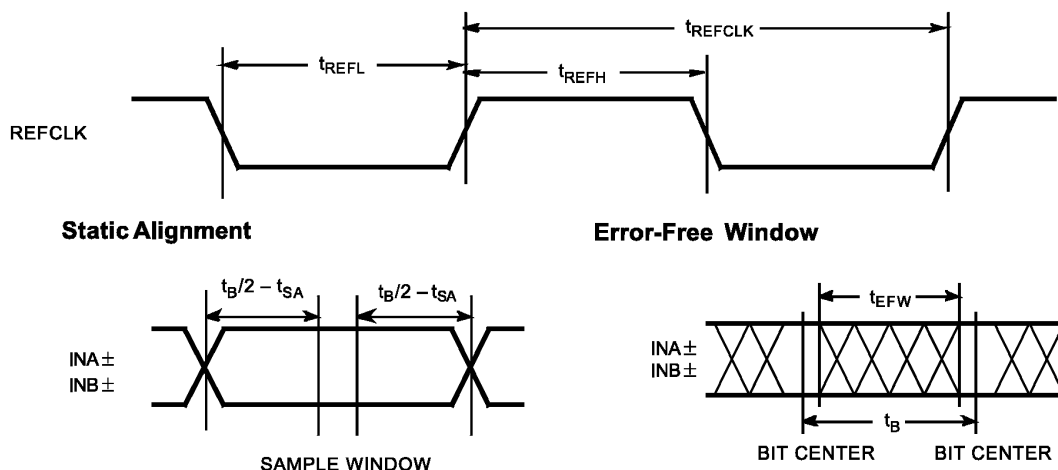
Cascade Timing Read Cycle



Note:

25. On inhibited reads when RXEN* is deasserted or BISTEN* is asserted, or if the Receive FIFO goes empty, the data outputs do not change.

CY7C924ADX HOTLink Receiver Switching Waveforms (continued)


CY7C924ADX HOTLink Receiver Switching Waveforms (continued)

CY7C924ADX HOTLink Transceiver Operation

The interconnection of two or more CY7C924ADX Transceivers form a general-purpose communications subsystem capable of transporting user data at up to 20MBytes per second over several types of serial interface media. The CY7C924ADX is highly configurable with multiple modes of operation.

In the transmit section of the CY7C924ADX, data moves from the input register, through the Transmit FIFO, to the 8B/10B Encoder. The encoded data is then shifted serially out the OUTx± differential PECL-compatible drivers. The bit-rate clock is generated internally from a 2.5x, 5x, or 10x PLL clock multiplier (3x, 6x, or 12x if BYTE8/10* and ENCBYP* are LOW). A more complete description is found in the section *CY7C924ADX HOTLink Transmit-Path Operating Mode Description*.

In the receive section of the CY7C924ADX, serial data is sampled by the receiver on one of the INx± differential line receiver inputs. The receiver clock and data recovery PLL locks onto the selected serial bit stream and generates an internal bit-rate sample clock. The bit stream is deserialized, decoded, and presented to the Receive FIFO, along with a character clock. The data in the FIFO can then be read either slower or faster than the incoming character rate. A more complete description is found in the section *CY7C924ADX HOTLink Receive-Path Operating Mode Description*.

The Transmitter and Receiver parallel interface timing and functionality can be configured to Cascade directly to external FIFOs for depth expansion, to emulate a UTOPIA interface, couple directly to registers, or couple directly to state machines. These interfaces can accept or output either:

- 8-bit characters
- 10-bit characters (for byte-packed encoded transport)
- 10-bit pre-encoded characters (pre-scrambled or pre-encoded)
- 12-bit pre-encoded characters (pre-scrambled or pre-encoded)

The bit numbering and content of the parallel transmit interface is shown in *Table 1*. When operated with the 8B/10B Encoder bypassed, the TXSC/D* and RXSC/D* bits are ignored.

The HOTLink Transceiver serial interface provides a seamless interface to various types of media. A minimal number of external passive components are required to properly terminate transmission lines and provide LVPECL loads. For power supply decoupling, a single capacitor (in the range of 0.02 μ F to 0.1 μ F) is required per power/ground pair. Additional information on interfacing these components to various media can be found in the *HOTLink Design Considerations* application note.

CY7C924ADX HOTLink Transmit-Path Operating Mode Description

The HOTLink Transmitter can be configured into several operating modes, each providing different capabilities and fitting different transmission needs. These modes are selected using the FIFOBYP*, ENCBYP* and BYTE8/10* inputs on the CY7C924ADX Transceiver. These modes can be reduced to five primary classes:

- Synchronous Encoded
- Synchronous Pre-encoded
- Asynchronous Encoded
- Asynchronous Byte-packed
- Asynchronous Pre-encoded

Synchronous Encoded

In this mode, the Transmit FIFO is bypassed, while the 8B/10B encoder is enabled. One character is accepted at the Transmit Input Register at the rising edge of REFCLK, and passed to the Encoder where it is encoded for serial transmission. The Serializer operates synchronous to REFCLK, which is multiplied by 10 or 5 to generate the serial data bit-clock. In this mode the TXSOC, TXRST*, TXINT, TXHALT*, and TXSTOP* inputs (when they are not used for data bits) are not interpreted and may be tied either HIGH or LOW. To place the CY7C924ADX into synchronous modes, FIFOBYP* must be LOW.



This mode is usually used for products that must meet specific predefined protocol requirements, and cannot tolerate the uncontrolled insertion of C5.0 fill characters. The host system is required to assert TXEN* and to provide new data at every appropriate rising edge of REFCLK to maintain the data stream. If TXEN* is not asserted, the Encoder is loaded with C5.0 (K28.5) sync characters. Because the Encoder is enabled, the transmitted C5.0 characters follow all 8B/10B encoding rules.

Input Register Mapping

In Encoded modes, the bits of the TXDATA input bus are mapped into characters (as shown in *Table 1*), including a TXSVS bit, eight or ten bits of data, and a TXSC/D* bit to select either Special Character codes or Data characters.

If the TXSVS bit is HIGH, an SVS (C0.7) character is passed to the encoder, regardless of the contents of the other TXDATA inputs. If the TXSVS bit is LOW, the associated TXDATA character is encoded per the remaining bits in that character.

The TXSC/D* bit controls the encoding of the TXDATA[7:0] or TXDATA[9:0] bits of each character. It is used to identify if the input character represents a Data Character or a Special Character code. If TXSC/D* is LOW, the character is encoded using the Data Character codes listed in *Table 11*. If TXSC/D* is HIGH, the character is encoded using the Special Character codes listed in *Table 12*.

Synchronous Pre-encoded

In synchronous pre-encoded mode (FIFOBYP* and ENCBYP* are LOW), both the Transmit FIFO and the 8B/10B encoder are bypassed, and data passes directly from the Transmit Input Register to the Serializer. The Serializer operates synchronous to REFCLK to generate the serial data bit-clock. As selected by SPDSEL and RANGESEL, the REFCLK input is multiplied by 5 or 10 when BYTE8/10* is HIGH or by 6 or 12 when BYTE8/10* is LOW. In this mode the TXINT, TXHALT*, TXSVS and TXSOC inputs are used as part of the data input bus.

This mode is usually used for products containing external encoders or scramblers, that must meet specific protocol requirements. The host system is required to assert TXEN* and to provide new data at every appropriate rising edge of the REFCLK to maintain the data stream. If TXEN* is not asserted, the Serializer is loaded with C5.0 (K28.5) sync characters. However, because the bypassed encoder is not able to track the running disparity of the previously transmitted character, the transmitted C5.0 characters may be received with a running disparity code-rule violation.

In this mode the LSB of each input character (TXDATA[0]) is shifted out first, followed sequentially by TXDATA[1] through TXDATA[9].

Asynchronous Encoded

Asynchronous Encoded mode is the most powerful operating mode of the CY7C924ADX. Both the Transmit FIFO and the Encoder are enabled (FIFOBYP* and ENCBYP* are HIGH). This allows transmission of normal data streams, while offering the added benefits of embedded cell or packet markers, an expanded command set, serial addressing, and in-band bypass-signaling (for flow control or other purposes). All characters added to the data stream to support these additional capabilities may be automatically extracted by the

Receive Control State Machine in the CY7C924ADX Receiver.

The Serializer operates synchronous to REFCLK, which is multiplied by 2.5, 5, or 10 to generate the serial data bit-clock (as selected by SPDSEL and RANGESEL). In this mode the TXSOC, TXSC/D*, TXRST*, TXSVS, TXINT/TXDATA[8], TXHALT*/TXDATA[9], and TXSTOP* inputs are interpreted.

Embedded Cell Marker

An embedded cell marker is used to mark the start of cells or frames of information passed from one end of the link to the other. This marker is set by asserting TXSOC HIGH, with TXSC/D* and TXSVS both LOW, along with the remaining data on the TXDATA bus. When the data character accompanying this marker is read from the output end of the Transmit FIFO, a C8.0 (K23.7) character is inserted into the data stream prior to the associated data character being read from the Transmit FIFO.

Expanded Commands

The standard 8B/10B Character set contains all 256 possible data characters, but only twelve special or *command* characters. To allow use of a larger selection of command codes, a Special Character code was selected to expand the command set.

An expanded command marker is used to mark the associated data as any one of 256 (2⁸) possible commands codes. This marker is generated by asserting both TXSOC and TXSC/D* HIGH, with TXSVS being LOW, along with the associated data on the TXDATA bus. When the character accompanying this marker is read from the output end of the Transmit FIFO, a C9.0 (K27.7) character is inserted into the data stream prior to the data character being read from the Transmit FIFO.

Serial Addressing

The CY7C924ADX receiver has the ability to accept or reject data based on an internal address-controlled switch. This switch is turned on when a serial address matching the receiver address settings is received. When the serial address received does not match the address programmed into the receiver, the receiver's input is ignored.

A serial address is transmitted by asserting TXSOC, TXSC/D*, and TXSVS all HIGH. When the character accompanying this marker is read from the output end of the Transmit FIFO, a C10.0 (K29.7) character is inserted into the data stream prior to the data characters being read from the Transmit FIFO. The serial address is either 8 or 10 bits depending on the level on BYTE8/10*.

In-Band Bypass-Signaling

In-band bypass-signaling allows a signal to be sent to the remote receiver without that signal having to pass through the Transmit (or Receive) FIFO. When TXINT transitions, a character is immediately inserted in the data stream at the Encoder block, delaying other data encoding for a cycle.

When TXINT transitions from 0→1, a C0.0 (K28.0) special character is sent. When TXINT transitions from 1→0, a C3.0 (K28.3) special code is sent. These special codes may be used to force a similar signal transition on the RXINT output of an attached CY7C924ADX HOTLink Receiver.

This input may be used to transport a low data rate signal (like a serial RS-232/UART signal) across the interface, without any significant impact on the actual data being transported



across the link. It may also be used to transparently propagate FIFO flow control information across the link by directly connecting the RXHALF* flag of the local receiver to the TXINT of the local transmitter. The RXINT at the remote end of the link can then be connected to the TXHALT* input to halt data transfers at the remote end of the link until the local Receive FIFO has sufficient room to continue.

Asynchronous Byte-Packed

Asynchronous byte-packed mode contains the same features as asynchronous encoded, but with support for 10-bit source data. This data is byte-packed through the 8B/10B encoder to deliver the data across the interface. This mode is enabled when FIFOBYP* and ENCBYP* are HIGH and BYTE8/10* is LOW.

When sending extended commands, the larger 10-bit character size enlarges the extended command space to 1024 (2¹⁰) possible commands codes.

Asynchronous Pre-encoded

In Asynchronous pre-encoded modes, the Transmit FIFO is enabled and the Encoder is disabled (FIFOBYP* is HIGH and ENCBYP* is LOW). This means that all words clocked into the input register are written to the Transmit FIFO before being sent to the Serializer. The Serializer operates synchronous to REFCLK to generate the serial data bit-clock. SPDSEL and RANGESEL determine whether REFCLK is multiplied by 10, 5 or 2.5 (if BYTE8/10* is HIGH) or 3, 6 or 12 (if BYTE8/10* is LOW). In this mode the TXINT and TXHALT* inputs are used as part of the 10-bit input character. TXSVS, TXSOC and TXSTOP* are still available.

These modes are usually used for products containing external encoders or scramblers, that must meet specific protocol requirements. The host system must assert TXEN* and provide new data at every rising edge of TXCLK to maintain the data stream (without overfilling the Transmit FIFO). If the Transmit FIFO ever goes empty, the Serializer is loaded with an alternating disparity string of C5.0 (K28.5) sync characters (when BYTE8/10* is HIGH) or the bit pattern 0110000100011 (when BYTE8/10* is LOW).

This insertion can be an issue for some system implementations. If the remote receiver is configured to decode 8B/10B coded characters, it will probably detect running disparity errors because the bypassed Encoder is not able to track the running disparity of the previously transmitted character. However, since these pre-encoded modes are generally used with alternate forms of scrambling or encoding, for these applications this disparity is not generally an issue.

To maintain a data stream without adding these C5.0 SYNC codes, it is necessary that the Transmit FIFO be loaded at the same speed or faster than the rate that data is read from that FIFO.

CY7C924ADX HOTLink Receive-Path Operating Mode Descriptions

The HOTLink Receiver can be configured into several operating modes, each providing different capabilities and fitting different reception needs. These modes are selected using the FIFOBYP*, ENCBYP* and BYTE8/10* inputs on the CY7C924ADX Transceiver. These modes can be reduced to five primary classes:

- Synchronous Decoded
- Synchronous Undecoded
- Asynchronous Decoded
- Asynchronous Byte-packed
- Asynchronous Undecoded.

In all these modes, serial data is received at one of the differential line receiver inputs and routed to the Deserializer and Framer. The PLL in the clock and data recovery block is used to extract a bit-rate clock from the transitions in the data stream, and uses that clock to capture bits from the serial stream. These bits are passed to the Deserializer where they are formed into 10- or 12-bit characters.

To align the incoming bit stream to the proper character boundaries, the Framer must be enabled by asserting RFEN HIGH. The Framer logic-block checks the incoming bit stream for the unique pattern that defines the character boundaries. This logic filter looks for the ANSI X3.230 symbol defined as a "Special Character Comma" (K28.5 or C5.0). Once a K28.5 is found, the Framer captures the offset of the data stream from the present character boundaries, and resets the boundary to reflect this new offset, thus framing the data to the correct character boundaries.

Since noise induced errors can cause the incoming data to be corrupted, and since many combinations of corrupt and legal data can create and aliased K28.5, the framer may also be disabled by setting RFEN LOW.

An option exists in the framer to require multiple K28.5 characters, meeting specific criteria, before the character boundaries are reset. This multi-byte mode of the Framer is enabled by keeping RFEN asserted HIGH for greater than 2048 character clock cycles. For multi-byte framing, the receiver must find a pair of K28.5 characters, both on identical 10-bit boundaries, within a 5-character span (50 bits) before it shifts its framing boundaries. This option greatly reduces the probability of framing to aliased K28.5 characters while still allowing many links to maintain synchronization.

Synchronous Decoded

In these modes, the Receive FIFO is bypassed, while the 10B/8B Decoder is enabled (FIFOBYP* is LOW and ENCBYP* is HIGH). Framed characters output from the Deserializer are decoded, and passed direct to the Receive Output Register. The Deserializer operates synchronous to the recovered bit-clock, which is divided by 10 generate the output RXCLK clock. In this mode the RXRST* input is not interpreted and may be biased either HIGH or LOW.

These modes are usually used for products that must meet specific protocol requirements. New decoded characters are provided at the RXDATA outputs once every rising edge of RXCLK. When RXEMPTY* is deasserted along with the data, it indicates that a valid character (as selected by RXMODE[1:0]) is present at the RXDATA outputs. When asserted it indicates that a C5.0 (K28.5) not kept by the current RXMODE[1:0] setting is present on the RXDATA output bus. Because the decoder is enabled, all received characters are checked for compliance to the 8B/10B decoding rules.

Output Register Mapping

The RXDATA[11:0] output bus is mapped into a character consisting of eight bits of data, one bit that carries violation information, and an RXSC/D* bit that identifies the character as either control or data.



These bits have combinations that identify the meaning of the remaining bits of the character. If RXRVS is HIGH and RXSC/D* is HIGH the decoder outputs a C0.7, C1.7, C2.7 or C4.7 in response to reception of either an SVS (C0.7) character or other invalid character.

Synchronous Undecoded

In this mode, both the Receive FIFO and the 10B/8B Decoder are bypassed (FIFOBYP* and ENCBYP* are LOW), and data passes directly from the Deserializer to the output register. The Deserializer operates synchronous to the recovered bit-clock, which is divided by 10 or 12 to generate the output RXCLK clock. In this mode the RXRST* input is not interpreted and may be biased either HIGH or LOW.

This mode is usually used for products containing external decoders or descramblers that must meet specific protocol requirements. New data is provided at the RXDATA outputs once every rising edge of RXCLK. Received characters are not checked for any specific coding requirements and no decoding errors are reported.

Asynchronous Decoded

Asynchronous Decoded mode is the most powerful operating mode of the CY7C924ADX HOTLink Receiver. Both the Receive FIFO and the Decoder are enabled (FIFOBYP* and ENCBYP* are HIGH). This allows reception of normal data streams, while offering the added benefits of embedded cell markers, an expanded command set, serial address support, and in-band bypass-signaling (for flow control or other purposes). All characters added to the data stream by the transmitter to support these additional capabilities may be automatically extracted by the Receive Control State Machine in the CY7C924ADX Transceiver.

The deserializer operates synchronous to the recovered bit-clock, which is divided by 10 to generate the Receive FIFO write clock. When the Receive FIFO is addressed by AM* and selected by RXEN*, characters are read from the FIFO using the external RXCLK input.

Asynchronous Decoded mode support the same Output Register mapping as the Synchronous Decoded mode. Because both the Receive FIFO and Decoder are enabled, the output FIFO may be read at any rate supported by the FIFO (0 to 50MHz), however, if the Receive FIFO ever indicates a full condition (RXFULL* is asserted), data may be lost.

Embedded Cell Marker

An embedded cell marker is used to mark the start of cells or frames of information passed from one end of the link to the other. When a C8.0 (K23.7) character is detected in the data stream, the next character is written to the Receive FIFO along with RXSOC set HIGH, and RXSC/D* and RXRVS set LOW. When the character accompanying this marker is read from the Receive FIFO with these same bits set, it indicates the start of a cell or frame.

Expanded Command

The standard 8B/10B Character set contains all 256 possible data characters, but only twelve Special Character codes. To allow use of a larger selection of command codes, one Special Character code was selected to expand the command set.

An Expanded Command marker is used to mark the associated data as any one of 256 (2^8) possible commands codes. When a C9.0 (K27.7) character is detected in the data stream, the following character is written to the Receive FIFO along with both RXSOC and RXSC/D* set HIGH, and RXRVS set LOW. When the character accompanying this marker is read from the Receive FIFO with these same bits set, it may be used to indicate that the data on the RXDATA bus is an Expanded Command.

Serial Addressing

The CY7C924ADX receive path can be directed to accept all characters, or to only accept that data specifically addressed to it. This address control is managed through an embedded Address Compare Register in the receiver logic. This register supports either domain (multicast) or exact-match (unicast) based compares on an address field received across the serial link. When a C10.0 (K29.7) special code is received, the immediately following data character contains the address field that is compared with the receiver Serial Address Register contents.

When the CY7C924ADX is configured for multicast address matching, the received address field is compared as an OR of a bit-wise AND with the Serial Address Register. A valid match between any of the bits sets the switch to allow the following data to be written into the Receive FIFO. If no matches are found, the data is not written to the Receive FIFO and is discarded.

When the CY7C924ADX is configured for unicast address matching, the received address field is compared for an exact match with the Serial Address Register. If an exact match is found, a switch is set in the receiver to accept all following data until the next serial address marker is found. If they do not match, the data is not written to the Receive FIFO and is discarded.

In-Band Bypass-Signaling

In-band bypass-signaling allows a signal to be received at the local receiver without that signal having to pass through the Receive FIFO.

When a C0.0 (K28.0) character is received, the RXINT output is set HIGH. When a C3.0 (K28.3) character is received, the RXINT output is set LOW. These special codes are generated by forcing similar transitions into the TXINT input of the CY7C924ADX HOTLink Transmitter sourcing the data stream.

This output may be used to transport a low data-rate signal (like a serial RS-232/UART signal) across the interface, without any significant impact on the actual data being transported across the link. It may also be used to transparently propagate FIFO flow-control information across the link by directly connecting the RXHALF* flag of the local receiver to the TXINT of the local transmitter. The RXINT at the remote end of the link can then be connected to the TXHALT* input to halt data transfers at the remote end of the link until the local Receive FIFO has sufficient room to continue.

Asynchronous Byte-Packed

Asynchronous byte-packed mode contains the same features as asynchronous decoded, but with support for 10-bit source data (BYTE8/10* is LOW). The received characters are decoded first back into 8-bit data characters, which are then reassembled into 10-bit source data.



Because of the time difference involved with the packing and unpacking operations, this mode can only be used with the internal FIFOs enabled.

When receiving extended commands, the larger 10-bit character size enlarges the extended command space to 1024 (2^{10}) possible commands codes.

When receiving a serial address, the larger 10-bit character size also increases the Serial Address Register to 10 bits. This allows up to 10 separate domains for multicast addressing or 1024 unique addresses for unicast addressing.

Asynchronous Undecoded

In Asynchronous Undecoded modes, the Receive FIFO is enabled (FIFOBYP* is HIGH and ENCBYP* is LOW). This means that all characters received from the serial interface are written to the Receive FIFO before being passed to the output register. The Deserializer operates synchronous to the recovered bit-clock, which is divided by 10 or 12 to generate the Receive FIFO write clock. Data is read from the Receive FIFO, using the RXCLK input clock, when addressed by AM* and selected by RXEN*.

These modes are usually used for products containing external decoders or descramblers, that must meet specific protocol requirements. New data may be read from the Receive FIFO any time that the FIFO status flags indicate a non-empty condition (RXEMPTY* is deasserted). To ensure that data is not lost through a FIFO overflow, the Receive FIFO must be read faster than data is loaded into the Receive FIFO.

If the receiver is to provide framed characters, it is necessary for the transmit end to include C5.0 (K28.5) characters in the data stream. This can be done by:

- operating the transmitter in encoded mode and writing C5.0 characters into the data stream
- operating the transmitter in pre-encoded mode and writing the 10-bit value for an encoded C5.0 character to the data stream (1100000101 or 0011111010)
- deasserting TXEN* when the transmitter is operated in synchronous mode
- asserting TXHALT*, or by allowing the transmit FIFO to go empty when it is operated in asynchronous mode.

BIST Operation and Reporting

The CY7C924ADX HOTLink Transceiver incorporates the same Built-In Self-Test (BIST) capability used with the HOTLink CY7B923/ CY7B933 and HOTLink II CYP(V)15G0x0x families. This link diagnostic uses a Linear Feedback Shift Register (LFSR) to generate a 511-character repeating sequence that is compared, character-for-character, at the receiver.

BIST mode is intended to check the entire high-speed serial link at full link-speed, without the use of specialized and expensive test equipment. The complete sequence of characters used in BIST are documented in the *HOTLink Built-In Self-Test* application note.

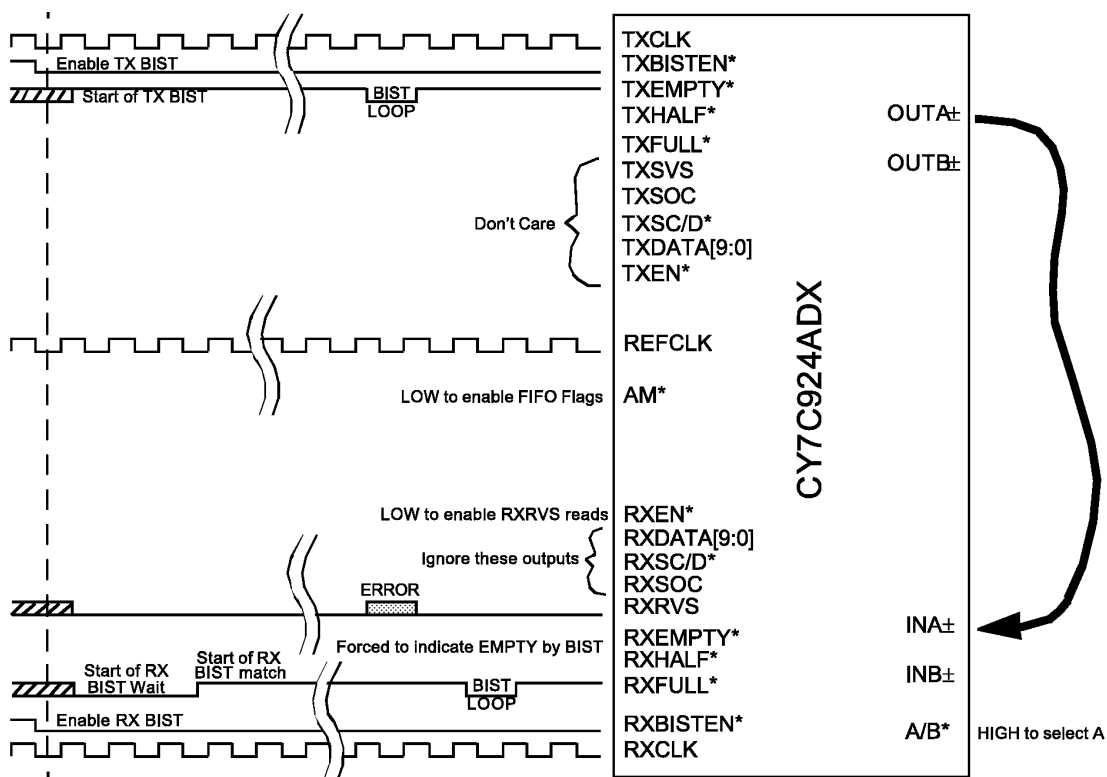


Figure 7. Built-In Self-Test Illustration, Utopia mode



BIST Enable Inputs

There are separate BIST enable inputs for the transmit and receive paths of the CY7C924ADX. These inputs are both active LOW; i.e., BIST is enabled in its respective section of the device when the BIST enable input is determined to be at a logic-0 level. Both BIST enable inputs are asynchronous; i.e., they are synchronized inside the CY7C924ADX to the internal state machines.

BIST Transmit Path

The transmit path operation with BIST is controlled by the TXBISTEN* input and overrides most other inputs (see Figure 7). When the Transmit FIFO is enabled (not bypassed) and TXBISTEN* is recognized internally, all reads from the Transmit FIFO are suspended and the BIST generator is enabled to sequence out the 511 character repeating BIST sequence. If the Transmit Control State Machine was in the middle of an atomic operation (e.g., sending an extended command) the Data Character associated with the Special Character code is transmitted prior to recognition of the TXBISTEN* signal and suspension of FIFO data processing. If the recognition occurs in the middle of a data field, the following data is not transmitted at that time, but remains in the Transmit FIFO. Once the TXBISTEN* signal is removed, the data in the Transmit FIFO is again available for transmission. To ensure proper data handling at the destination, the transmit host controller should either use TXHALT* or TXSTOP* to segment transmission of data at specific boundaries, or allow the Transmit FIFO to completely empty before enabling BIST.

With transmit BIST enabled, the Transmit FIFO remains available for loading of data. It may be written up to its normal maximum limit while the BIST operation takes place. To allow removal of stale data from the Transmit FIFO, it may also be reset during a BIST operation. The reset operation proceeds as documented, with the exception of the information presented on the TXEMPTY* FIFO status flag. Since this flag is used to present BIST loop status, it continues to reflect the state of the transmit BIST loop status until TXBISTEN* is no longer recognized internally. The completion of the reset operation may still be monitored through the TXFULL* FIFO status flag.

The TXEMPTY* flag, when used for transmit BIST progress indication, continues to reflect the active HIGH or active LOW settings determined by the UTOPIA or Cascade timing model selected by EXTIFIFO; i.e., when configured for the Cascade timing model, the TXEMPTY* and TXFULL* FIFO flags are active HIGH, when configured for the UTOPIA timing model the TXEMPTY* and TXFULL* FIFO flags are active LOW. The illustration in Figure 7 uses the UTOPIA conventions.

When TXBISTEN* is first recognized, the TXEMPTY* flag is clocked to a reset state, regardless of the addressed state of the Transmit FIFO (if AM* is LOW or not), but is not driven out of the part unless AM* has been sampled asserted (LOW). Following this, on each completed pass through the BIST loop, the TXEMPTY* flag is set for one interface clock period (TXCLK or REFCLK).

When the Transmit FIFO is enabled, the TXEMPTY* flag remains set until the interface is addressed and the state of TXEMPTY* has been observed. If the device is not addressed (AM* is not sampled LOW), the flag remains set internally regardless of the number of TXCLK clock cycles that are processed. If the device status is not polled on a sufficiently

regular basis, it is possible for the host system to miss one or more of these BIST loop indications.

A pass through the loop is defined as that condition where the Encoder generates the D0.0 state that initiates the BIST loop. Depending on the initial state of the BIST LFSR, the first pass through the loop may occur at substantially less than 511 character periods. Following the first pass, as long as TXBISTEN* remains LOW, all remaining passes are exactly 511 characters in length.

When the Transmit FIFO is bypassed, the interface is clocked by the REFCLK signal instead of TXCLK. While the active or asserted state of the TXEMPTY* signal is still controlled by the EXTIFIFO, the state of any completed BIST loops is no longer preserved. Instead, the TXEMPTY* flag reflects the dynamic state of the BIST loop progress, and is asserted only once every 511 character periods. If the interface is not addressed at the time that this occurs, then the FIFO status flags remain in a High-Z state and the loop event is lost.

BIST Receive Path

The receive path operation in BIST is similar to that of the transmit path. While the Receive FIFO is enabled and RXBISTEN* is recognized internally, all writes to the Receive FIFO are suspended. If the receiver had a previous serial address match and was accepting data, no additional characters are written to the Receive FIFO. If the receive data state machine was in the middle of processing a multi-character sequence or other atomic operation (e.g., a start of cell marker and its associated data), the characters associated with the atomic operation are discarded and not written to the Receive FIFO.

Upon internal recognition of RXBISTEN*, the serial address match flag is cleared such that once BIST has been disabled and data is again being received, all received data is rejected until a new serial address is again received that matches the address match criteria.

Note. If the CY7C924ADX is set to match all data (all 1s in the multicast match field), then it is not necessary to get an address match before receiving data following the termination of BIST. On reset or when programmed to this state, the device ignores all serial address commands and matches all data.

Any data present in the Receive FIFO when RXBISTEN* is recognized remains in the FIFO and cannot be read until the BIST operation is complete. The data in the Receive FIFO remains valid, but is NOT available for reading through the host parallel interface. This is because the error output indicator for receive BIST operations is the RXRVS signal, which is normally part of the RXDATA bus. To prevent read operations while BIST is in operation, the RXEMPTY* and RXHALF* flags are forced to indicate an Empty condition. Once RXBISTEN* has been removed and recognized internally, the Receive FIFO status flags are updated to reflect the current content status of the Receive FIFO.

To allow removal of stale data from the Receive FIFO, it may be reset during a BIST operation. The reset operation proceeds as documented, with the exception that the RXEMPTY* and RXHALF* status flags already indicate an empty condition. The RXFULL* flag is used to present BIST progress. The active state on RXFULL* and RXEMPTY* flags remain controlled by the present operating mode and interface timing model (UTOPIA or Cascade) as selected by EXTIFIFO*.



When RXBISTEN* has been recognized, RXFULL* becomes the receive BIST loop indicator, regardless of the logic state of FIFOBYP*. When RXBISTEN* is first recognized with the Receive FIFO enabled, the RXFULL* flag is clocked to a set state, regardless of the addressed state of the Receive FIFO (if AM* is sampled LOW or not). Following this, RXFULL* remains set until the receiver detects the start of the BIST pattern. Then RXFULL* is deasserted for the duration of the BIST pattern, pulsing asserted for one RXCLK period on the last symbol of each BIST loop. If 14 of 28 consecutive characters are received in error, RXFULL* returns to the set state until the start of a BIST sequence is again detected.

Just like the BIST status flag on the transmit data path, when the Receive FIFO is enabled the RXFULL* flag captures the asserted states, and keeps them until they are read. This means that if the status flag is not read on a regular basis, events may be lost.

The detection of errors is presented on the RXRVS output. Unlike the RXFULL* FIFO status flag, the active state of this output is not controlled by the EXT_FIFO input. With the Receive FIFO enabled, these outputs should operate the same as the RXFULL* flag, with respect to preserving the detection state of an error until it is read.

Unlike the RXFULL* flag, which only needs the CY7C924ADX to be addressed (AM* sampled LOW by RXCLK) to enable the RXFULL* three-state driver, and an RXCLK to "read" the flag, the RXRVS output requires a selection (assertion of RXEN* while addressed) to enable the RXDATA bus three-state drivers. The selection process is necessary to ensure that a multi-PHY implementation does not enable multiple RXRVS drivers at the same time.

When the Receive FIFO is bypassed, the interface is clocked by the RXCLK output signal. While the active or asserted state of the RXFULL* signal is still controlled by the EXT_FIFO input, the state of any completed BIST loops or detected errors are no longer preserved. Instead, the RXFULL* flag reflects the dynamic state of the BIST loop progress, and is asserted only once every 511 character periods. If the interface is not addressed at the time that this occurs, then the FIFO status flags remain in a High-Z state and the loop event is lost. This is also true of the RXRVS output, such that if the CY7C924ADX receive path is not selected to enable the RXDATA bus three-state drivers, the detection of a BIST mismatch is lost.

BIST Three-state Control

When BIST is enabled on either the transmitter or the receiver, the three-state enable signals for the BIST status flags and error indicators work the same as for normal data processing. The output drivers for the BIST status that is presented on FIFO status flags are only enabled when AM* has been sampled asserted (LOW) by the respective clock (TXCLK, RXCLK, or REFCLK).

To access the BIST error information, it is necessary to perform a read cycle of the addressed receiver. This means that AM* must be LOW to allow a receiver address match (Rx_Match) to exist, and RXEN* must then be asserted to select the device. Because the part is in BIST, no data is read from the FIFO, but the data bus is driven. This allows the RXRVS indicator to be driven onto the RXDATA bus. So long as RXEN* remains asserted, the receiver stays selected, the data bus remains driven, and RXRVS has meaning.

Bus Interfacing

The parallel transmit and receive host interfaces to the CY7C924ADX are configurable for either synchronous or asynchronous operation. Each of these configurations supports two selectable timing and control models of UTOPIA or Cascade.

All asynchronous bus configurations have the internal Transmit and Receive FIFOs enabled. This allows data to be written or read from these FIFOs at any rate up to the maximum 50-MHz clock rate of the FIFOs. All internal operations of the CY7C924ADX do not use the external TXCLK or RXCLK, but instead make use of synthesized derivatives of REFCLK for transmit path operations and a recovered character clock for receive path operations.

All synchronous bus configurations require the bus interface operations to be synchronous to REFCLK on the transmit path and the recovered clock (output as RXCLK) on the receive path. The internal FIFOs are bypassed in all synchronous modes.

The two supported timing and control models are UTOPIA and Cascade. These timing models take their name from their default configuration. The UTOPIA timing model is based on the ATM Forum UTOPIA interface standards. This timing model is that of a FIFO with active LOW FIFO status flags and read/write enables.

The Cascade timing model is a modification of the UTOPIA configuration that changes the flags and FIFO read/write enables to active HIGH. This model is present primarily to allow depth expansion of the internal FIFO by direct coupling to external CY7C42x5 synchronous FIFOs. To allow this direct coupling, the FIFO flag active levels and cycle-to-cycle timing between the transmit enable (TXEN*) and data latching are modified to ensure correct data transfer.

These four configurations of bus operation and timing/control can all be used with or without external FIFOs. Depending on the specific mode selected, the amount of external hardware necessary to properly couple the CY7C924ADX to state machines or external FIFOs is minimal in all cases, and may be zero if the proper configuration is selected.

UTOPIA Interface Background

The UTOPIA interface is defined by the ATM Forum as the bus interface between the ATM and PHY layer devices of an ATM system. This interface is defined as 8 or 16 bits wide, with the latter reserved mainly for high-speed physical interfaces (PHYs) such as 622 Mbps OC-12. Due to the limited speed range of the CY7C924, only the 8-bit interface is implemented.

UTOPIA-1 was the original UTOPIA specification (created in 1993) which covers transport of:

- 155.52 Mbps (scrambled SONET/OC-3)
- 155.52 Mbps (8B/10B block coded at 194.4 Mbaud)
- 100 Mbps (4B/5B encoded TAXI)
- 44.736 Mbps (DS-3/T3)
- 51.84 Mbps (OC-1)

The UTOPIA-1 interface has a maximum clock rate of 25 MHz. All AC-timing and pin descriptions are covered in the UTOPIA-1 Specification, Version 2.01.

UTOPIA-2 was created as an addendum to the UTOPIA-1 specification. In this revision, the parallel interface was extended to both 33MHz and 50MHz to accommodate PCI bus architectures in ATM designs. A method of addressing was added to allow multiple devices (PHYs) to share a common host bus. Also, a description of a management interface was added (not supported by this device).

The CY7C924ADX contains all pins necessary to support the UTOPIA-1 and, through use of an external address decoder, can emulate the multi-PHY capability of a UTOPIA-2 interface. The maximum bus speed supports the full 50MHz I/O rate for emerging high-performance systems.

UTOPIA Address Match and Selection

All actions on a UTOPIA-2 interface are controlled by the Address Match and selection states of the interface. These states control the read and write access to the Receive and Transmit FIFOs, access to the FIFO status flags, reset of the Transmit and Receive FIFOs, and read and write access to the Serial Address Register. The CY7C924ADX supports the concept of an "address match" through a single Address Match (AM*) input.

Address Match and FIFO Flag Access

The CY7C924ADX makes use of a single active-LOW Address Match (AM*) to generate address-match conditions. When this input is LOW it is equivalent to an ATM address compare on both the TXADDR and RXADDR buses. This allows multiple CY7C924ADX devices to share a common bus, with device output three-state controls being managed by either an address match condition (AM* sampled LOW), or by a selection state.

The Transmit and Receive FIFO flag empty and FIFO full output drivers are enabled in any TXCLK, REFCLK, or RXCLK cycle following AM* being sampled asserted (LOW) by the rising edge of the respective clock. The AM* input is sampled separately by the clocks for the transmit and receive interfaces, which allows these clocks to operate at different clock rates. An example of both Transmit and Receive FIFO flag access is shown in Figure 8.

When the Transmit FIFO is enabled (FIFOBYP* is HIGH) and AM* is sampled LOW by the rising edge of TXCLK, the output drivers for the TXFULL* and TXEMPTY* FIFO flags are

enabled. When AM* is sampled HIGH by the rising edge of TXCLK, these same output drivers are disabled.

When the Transmit FIFO is bypassed (FIFOBYP* is LOW and not in byte-packed mode) and AM* is sampled LOW by the rising edge of REFCLK, the output drivers for the TXFULL* and TXEMPTY* FIFO flags are enabled. When AM* is sampled HIGH by the rising edge of REFCLK, the FIFO flag output drivers are disabled.

When AM* is sampled LOW by the rising edge of RXCLK (input or output), the output drivers for the RXFULL* and RXEMPTY* FIFO flags are enabled. When AM* is sampled HIGH by the rising edge of RXCLK, the FIFO flag output drivers are disabled.

Device Selection

The concept of selection is used to control the access to the transmit and receive parallel-data ports of the device. There are three primary types of selection:

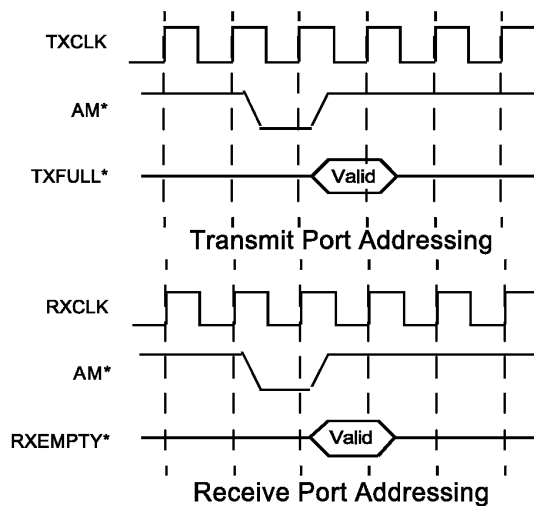


Figure 8. FIFO Flag Driver Enables

- Transmit data selection (with and without internal Transmit FIFO)
- Receive data selection (with and without internal Receive FIFO)
- Continuous selection (for either or both transmit and receive interfaces)

In addition to these normal selection types, there are two additional sequences that are used to control the internal Transmit and Receive FIFOs reset operations, and to control read/write access to the Serial Address Register:

- Transmit reset sequence
- Receive reset sequence (includes access to the Serial Address Register)

Of these operations, the transmit data selection and transmit reset sequence are mutually exclusive and cannot exist at the same time. The receive data selection and receive reset sequence are also mutually exclusive and cannot exist at the same time. Either transmit operation can exist at the same time as either receive operation.

All normal forms of selection require that an Address Match condition must exist (AM* sampled LOW) either at the same time as the selection control signal being sampled asserted, or one or more clock cycles prior to the selection control signal being sampled asserted.

Transmit Data Selection

Asynchronous With UTOPIA Timing and Control (Transmit FIFO Enabled)

When AM* is sampled LOW and TXRST* is sampled HIGH by the rising edge of TXCLK, a Tx_Match condition is generated. This Tx_Match condition continues until AM* is sampled HIGH or TXRST* is sampled LOW at the rising edge of TXCLK. When a Tx_Match (or Tx_RstMatch) condition is present, the TXEMPTY* and TXFULL* output drivers are enabled. When a Tx_Match (or Tx_RstMatch) condition is not present, these same drivers are disabled (High-Z).

The selection state of the Transmit FIFO is entered when a Tx_Match condition is present, and TXEN* transitions from HIGH to LOW. Once selected, the Transmit FIFO remains

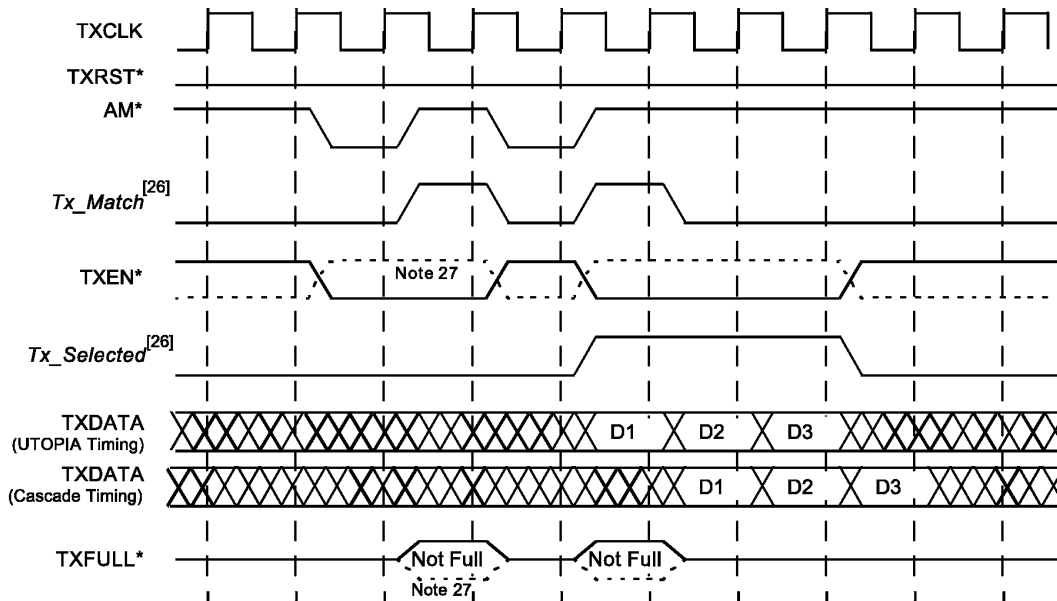


Figure 9. Transmit Selection with Transmit FIFO Enabled

selected until TXEN* is sampled HIGH by the rising edge of TXCLK. In the selected state, data present on the TXDATA inputs is captured and stored in the Transmit FIFO. This transmit interface selection process is shown in *Figure 9*. For the first TXEN* assertion, the TX_Match condition is not yet present so the Transmitter is not selected. However, the second TXEN* assertion meets this requirement and the Transmitter selection is successful.

**Synchronous With UTOPIA Timing and Control
(Transmit FIFO Bypassed)**

When the Transmit FIFO is bypassed (FIFOBYP* is LOW and not in byte-packed mode), the CY7C924ADX must still be selected to write data into the Transmit Input Register.

Parallel TXDATA is clocked in and transmitted serially when TXEN* is asserted. When TXEN* is deasserted, the TXDATA bus contents are ignored and C5.0 idle characters are sent instead.

AM* must be asserted to enable the TXFIFO flags. When AM* is deasserted, the flags are High-Z.

When AM* is deasserted while TXEN* is enabled, the Transmit TXDATA is still read in and transmitted, but the FIFO flags are no longer enabled.

When data is not written to the Transmit Input Register, the data stream is automatically padded with C5.0 (K28.5) SYNC characters. If the 8B/10B Encoder is enabled, disparity tracking allows the added C5.0 fill characters to follow all 8B/10B encoding rules. If the 8B/10B encoder is bypassed, disparity tracking is disabled, and the transition between externally encoded data and internally generated C5.0 characters may generate a running disparity error at the attached

Notes:

26. Signals labeled in *italics* are internal to the CY7C924ADX.

27. Signals shown as dotted lines represent the differences in timing and active state of signals when operated in Cascade Timing.

receiver. The same error may occur at the transition between the internal C5.0 characters and the resumption of externally encoded data. When strings of contiguous C5.0 characters are generated, each C5.0 has alternating running disparity with the previous C5.0 character.

Receive Data Selection

**Asynchronous With UTOPIA Timing and Control
(Receive FIFO Enabled)**

When AM* is sampled LOW and RXRST* is sampled HIGH by the rising edge of RXCLK input, an Rx_Match condition is generated. This Rx_Match condition continues until AM* is sampled HIGH or RXRST* is sampled LOW at the rising edge of RXCLK input. When an Rx_Match (or Rx_RstMatch) condition is present, the RXEMPTY* and RXFULL* output drivers are enabled. When an Rx_Match (or Rx_RstMatch) condition is not present, these same drivers are disabled (High-Z).

The selection state of the Receive FIFO is entered when an Rx_Match condition is present, and RXEN* transitions from HIGH to LOW. Once selected, the Receive FIFO remains selected until RXEN* is sampled HIGH by the rising edge of RXCLK input. The selected state initiates a read cycle from the Receive FIFO and enables the Receive FIFO data onto the RXDATA bus. This receive interface selection process is shown in *Figure 10*. For the first RXEN* assertion, the Rx_Match condition is not present when RXEN* is asserted so the Receiver is not selected. However, the second RXEN* assertion occurs with an Rx_Match condition present and the Receiver selection is successful.

Synchronous With UTOPIA Timing and Control (Receive FIFO Bypassed)

When the Receive FIFO is bypassed (FIFOBYP* is LOW and not in a byte-packed mode), the CY7C924ADX must still be selected to enable the output drivers for the RXDATA bus. With the Receive FIFO bypassed, RXCLK becomes a synchronous output clock operating at the character rate.

The Receive interface is selected when AM* is sampled asserted and RXEN* is asserted at least one cycle later. Once selected, it remains asserted until RXEN* is deasserted, regardless of the state of AM*.

If RXEN* is deasserted when AM* is deasserted, AM* must again be sampled LOW followed by RXEN* sampled low at least one cycle later for the Receive interface to again be selected. When the Receive interface is not selected, the RXDATA[11:0] bus is High-Z.

The Receive FIFO flags depend only on the state of AM*. When AM* is asserted, the flags are enabled. When AM* is deasserted, the flags are High-Z.)

Continuous Selection

Continuous Selection is a specialized form of selection which does not require sequenced assertion of AM* and TXEN* or RXEN* to select the device for data transfers. In this Continuous Selection mode, the AM* and associated TXEN* or RXEN* enable signal must be asserted when the device is powered up or during assertion of RESET*[1:0]. So long as these signals remain asserted, the device remains selected and data is accepted and presented on every clock cycle.

Note. The use of continuous selection makes it impossible to reset the internal FIFOs, or to access the Serial Address Register.

FIFO Reset Address Match

When AM* and TXRST* are both LOW, and this condition is sampled by the rising edge of TXCLK, a Tx_RstMatch

condition is generated. This Tx_RstMatch condition continues until AM* or TXRST* is sampled HIGH by the rising edge of TXCLK. When a Tx_RstMatch (or Tx_Match) condition is present, the TXEMPTY* and TXFULL* output drivers are enabled (just as in a normal Tx_Match condition). When AM* is not asserted, these same drivers are disabled (High-Z). The Transmit FIFO reset Address Match is shown in Figure 11. Note that although TXRST* remains LOW for more than one clock cycle, the Tx_RstMatch does not because the AM* signal is no longer asserted (LOW)

When AM* and RXRST* are both LOW, and this condition is sampled by the rising edge of RXCLK, an Rx_RstMatch condition is generated. This Rx_RstMatch condition continues until AM* or RXRST* is sampled HIGH, at the rising edge of RXCLK. When an Rx_RstMatch (or Rx_Match) condition is present, the RXEMPTY* and RXFULL* output drivers are enabled. When AM* is not asserted these same drivers are disabled (High-Z). The Receive FIFO reset Address Match is shown in Figure 12.

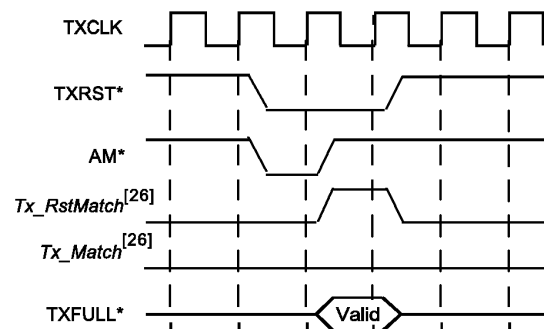


Figure 11. Transmit FIFO Reset Address Match

Note that while the FIFO flags remain asserted for more than one clock cycle, this is due to an Rx_Match condition, not a continuation of the Rx_RstMatch.

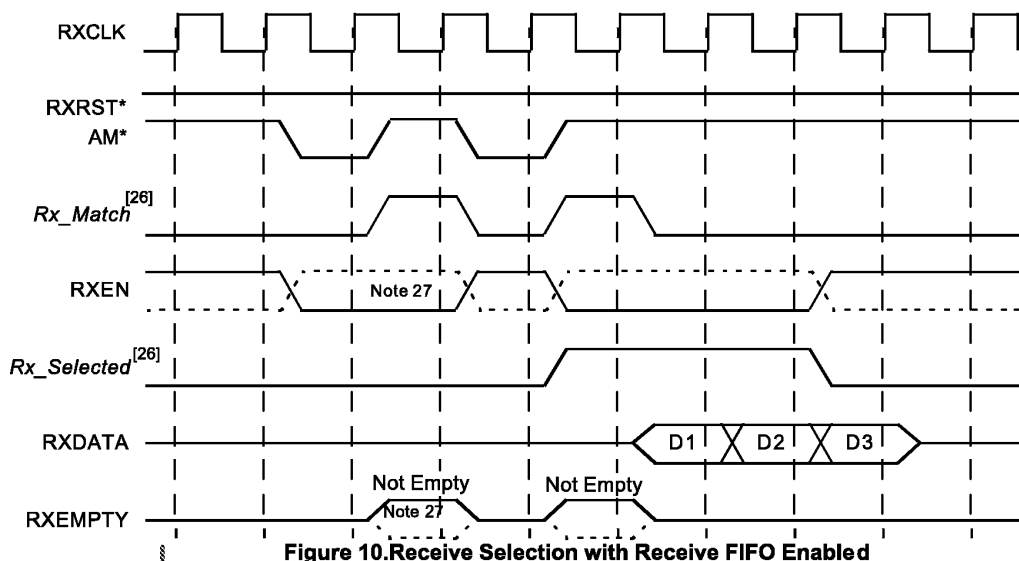


Figure 10. Receive Selection with Receive FIFO Enabled

FIFO Reset Sequence

On power-up, the Transmitter and Receiver FIFOs are cleared automatically. If the usage of the FIFOs in specific operating modes results in stale or unwanted data, this data can be cleared by resetting the respective FIFO. Data in the Transmitter FIFO will empty automatically if it is enabled to read the FIFO (assuming TXHALT* is not LOW). Stale received data can be "flushed" by reading it, or the Receive FIFO can be reset to remove the unwanted data.

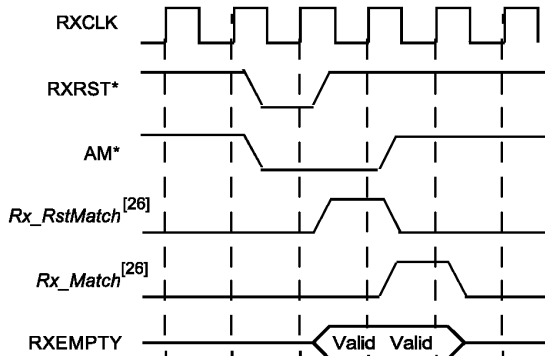


Figure 12. Receive FIFO Reset Address Match

The Transmitter and Receiver FIFOs are reset when the Tx_RstMatch or Rx_RstMatch condition remains present for eight consecutive clock cycles. Any disruption of the reset sequence prior to reaching the eight cycle count, either by removal of AM* or the respective TXRST* or RXRST* terminates the sequence and does not reset the FIFO. If the associated TXEN* or RXEN* signals are asserted during the reset, the relevant interface's reset operation is inhibited until the enable signal is deasserted. Because AM* must remain asserted during the reset sequence, the addressed FIFO flags remain driven during the entire sequence.

Transmit FIFO Reset Sequence

The Transmit FIFO reset sequence is started when TXRST* and AM* are first sampled LOW by the rising edge of TXCLK. If TXEN* is asserted (sampled HIGH for UTOPIA timing or LOW for Cascade timing), the reset sequence is inhibited until it is removed.

When a Transmit FIFO reset sequence is enabled and has been active for at least eight TXCLK cycles, a Transmit FIFO reset operation is started. To show this progress, the Transmitter FIFO flags are forced to indicate a FULL* condition (TXEMPTY* is deasserted, and both TXHALF* and TXFULL* are asserted).

Note. The FIFO Full state forced by the reset operation is different from a Full state caused by normal FIFO data writes.

For normal FIFO write operations, when Full is first asserted, the Transmit FIFO can still accept up to eight additional writes of data. When a Full state is asserted due to a Transmit FIFO reset operation, the FIFO will not accept any additional data.

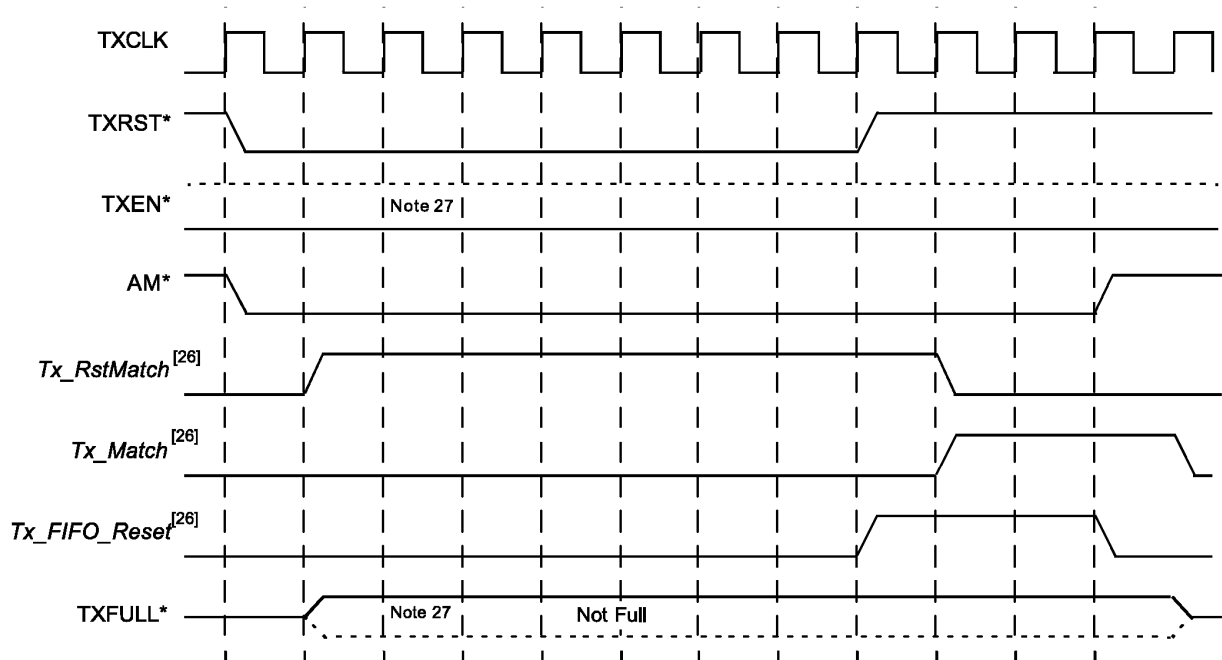
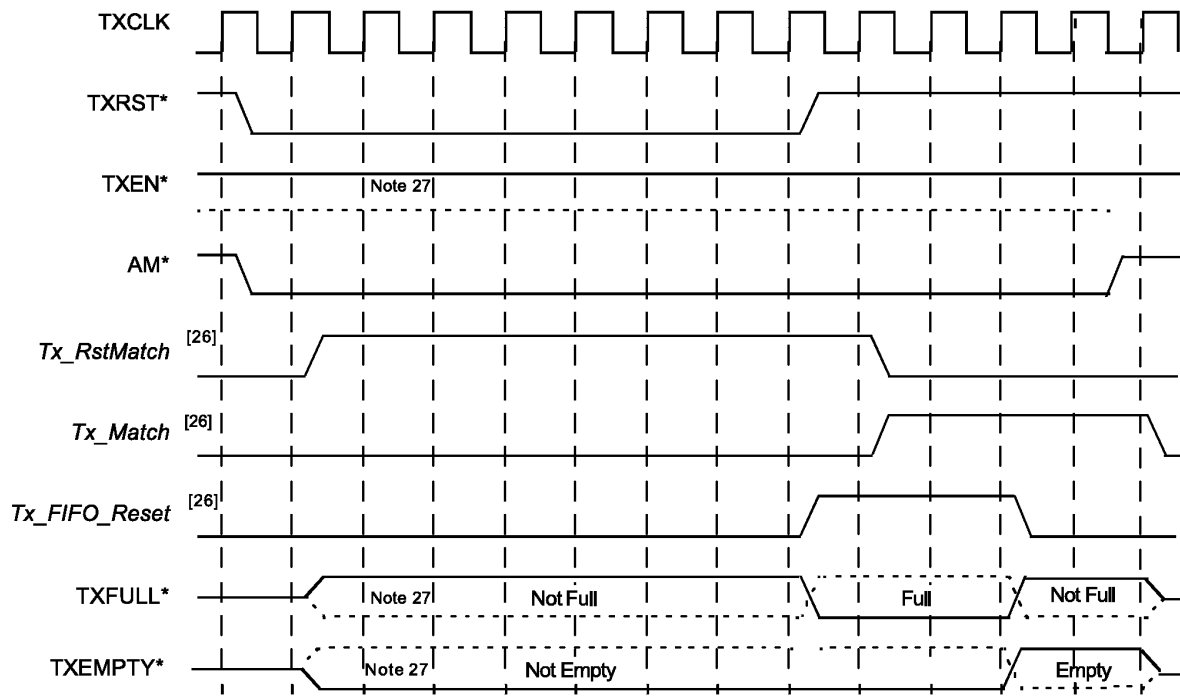
This FIFO reset operation is not allowed to progress within the device until the external reset condition is removed. This can occur by deasserting TXRST* or AM*. If AM* is deasserted (HIGH) to remove the reset condition, the Transmit FIFO flag's drivers are disabled, and the Transmit FIFO must be addressed at a later time to validate completion of the Transmit FIFO reset. If TXRST* is deasserted (HIGH) to remove the reset condition, the Tx_RstMatch is changed to a Tx_Match, and the Transmitter FIFO status flags remain driven.

The Transmit FIFO reset operation is complete when the Transmitter FIFO flags indicate an Empty state (TXEMPTY* is asserted and both TXHALF* and TXFULL* are deasserted). A valid Transmit FIFO reset sequence is shown in Figure 13. Figure 14 shows a sequence of input signals which does not produce a FIFO reset. In this case TXEN* was asserted to select the a Transmitter FIFO for data transfers. Because TXEN* remains active, the assertion of AM* and TXRST* does not initiate a reset operation. This is shown by the TXFULL* flag remaining HIGH (deasserted) following what would be the normal expiration of the eight-state reset counter.

Receive FIFO Reset Sequence

The Receive FIFO reset sequence operates similarly to the Transmitter FIFO reset sequence. The same requirements exist for the assertion state of RXRST* and selection of the interface through AM*. A sample Receive FIFO reset sequence is shown in Figure 15. Upon recognition of a Receive FIFO reset, the Receive FIFO flags are forced to indicate an Empty state to prohibit additional reads from the FIFO. Unlike the Transmitter FIFO, where the internal completion of the reset operation is shown by first going Full and later going Empty when the internal reset is complete, there is no secondary indication of the completion of the internal reset of the Receive FIFO. The Receive FIFO is usable as soon as new data is placed into it by the Receive Control State Machine.

When a Receive FIFO reset sequence is enabled and has been active for at least eight RXCLK cycles, a Receive FIFO reset operation is started. This FIFO reset operation is not allowed to progress within the device until the associated RXRST* or AM* signal is sampled deasserted. Following deassertion of RXRST* (which starts the FIFO reset operation), selection of the device for normal data transfers is inhibited during the immediately following RXCLK clock cycle. If a selection of the receive interface is attempted during this immediately following cycle (by asserting RXEN*), the selection is ignored, and the device remains unselected until RXEN* is deasserted, and reasserted in a following RXCLK cycle.



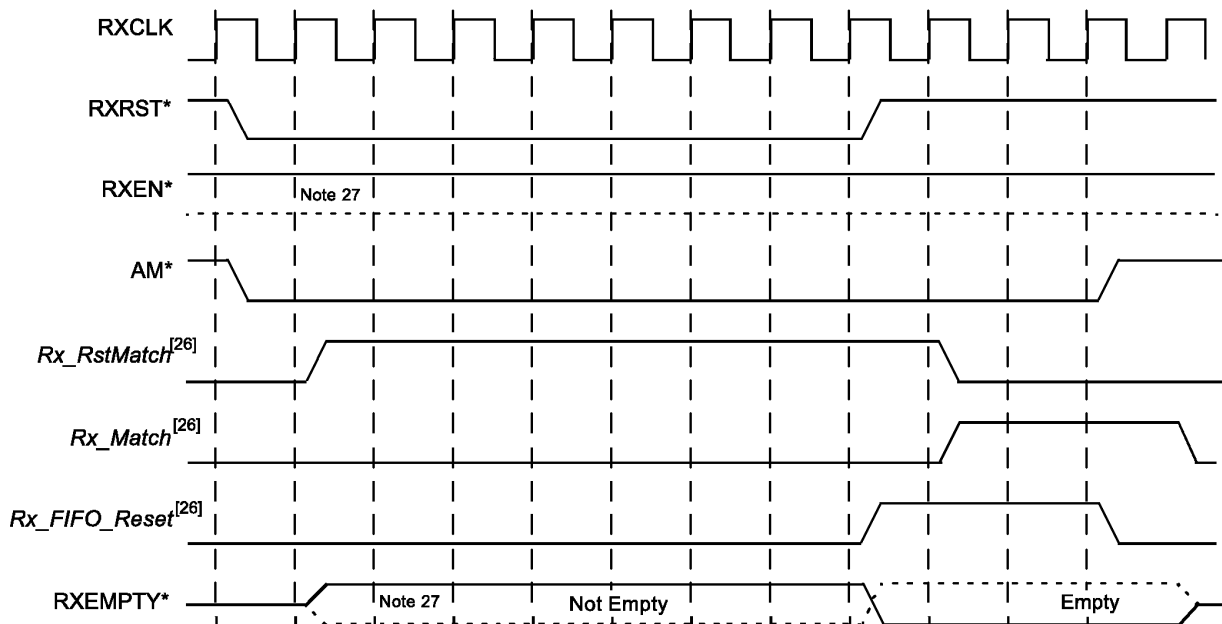


Figure 15. Receive FIFO Reset Sequence

Serial Address Register Access

The Serial Address Register in the CY7B924ADX is accessed through the RXDATA bus. This Serial Address Register can only be accessed in Utopia mode (EXTFIFO = L). This register can be both written and read, and is accessed by asserting RXRST* to address the register in the device instead of the normal Receive FIFO data. Within this alternate address space, the RXRVS signal is an input at all times, and is used to select between read (RXRVS is HIGH) and write (RXRVS is LOW) operations on the Serial Address Register.

The Serial Address Register is the same size as the 8- or 10-bit data width selected by BYTE8/10*. It can be set to match domain or multicast addresses by the level on RXSC/D*. If RXS/D* is LOW when the Serial Address Register is written, it becomes the Multicast address register and declares a match if at least one bit matches the equivalent bit in the incoming Address character. If RXSC/D* is HIGH when the Serial Address Register is written, it becomes the Unicast address register and defines a match only if all of the bits match the incoming Address character.

This register mapping is shown in *Figure 6*

Accessing Serial Address Register

To access the Serial Address Register in the CY7B924ADX, an Rx_RstMatch condition must first be generated by the

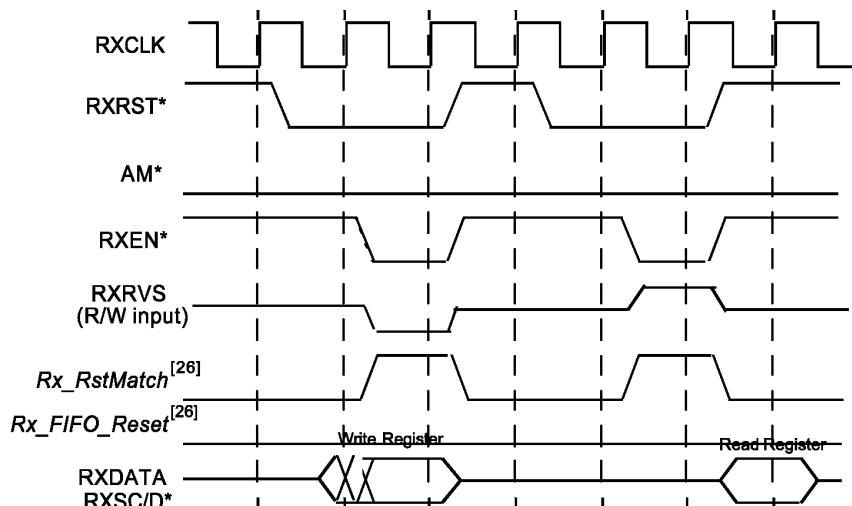
combined assertion of AM* and RXRST* and the device must be in Utopia timing mode (EXTFIFO = L). RXEN* is then used as the data strobe signal to initiate either a read or write cycle to the RXDATA bus. If RXRVS is HIGH at the time of the RXEN* data strobe, a register read operation takes place. If RXRVS is LOW at the time of the RXEN* data strobe, a register write operation takes place.

The RXSC/D* input is used in conjunction with RXDATA[9:0] or RXDATA[7:0] to select the operational mode of the Serial Address Register (Unicast or Multicast)

Register write and read operations are shown in *Figure 16*. If the serial address register write and read operations are both performed without deasserting RXRST* for at more than seven cycles, then RXRST* will still not extend to the requirement for a reset and the Receive FIFO will not be reset.

FIFO Reset, Serial Address Register Access and Continuous Selection

When configured for continuous selection (AM* asserted with TXEN* always enabled, or AM* asserted with RXEN* always enabled), it is not possible to reset the Transmit and Receive FIFOs. It is also not possible to write to the Serial Address Register without deselecting the Receive FIFO interface.


Figure 16. Serial Address Register Access

X3.230 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data (Data Characters) are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 8-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary rationale for use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard consist of a distinct and easily recognizable bit pattern (the Special Character Comma) that assists a Receiver in achieving word alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an 8-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the 8-bit byte for the raw 8-bit data, and the letters a, b, c, d, e, f, g, h, i, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown here:

FC-2 bit designation—	7	6	5	4	3	2	1	0
HOTLink TX/RX designation—	7	6	5	4	3	2	1	0
8B/10B bit designation—	H	G	F	E	D	C	B	A

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character (using 8B/10B Transmission Code notation):

```
FC-2  45
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation (note carefully that the order of bits is reversed):

```
Data Byte Name  D5.2
      Bits: ABCDE FGH
            10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
Bits: abcdeifghj
      1010010101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D, and the SC/D* pin is LOW) or a Special Character (c is set to K, and the SC/D* pin is HIGH). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7).



Note. This definition of the 10-bit Transmission Code is based on (and is in basic agreement with) the following references, which describe the same 10-bit transmission code.

A.X. Widmer and P.A. Franaszek. "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code" *IBM Journal of Research and Development*, 27, No. 5: 440-451 (September, 1983).

U.S. Patent 4,486,739. Peter A. Franaszek and Albert X. Widmer. "Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code" (December 4, 1984).

Fibre Channel Physical and Signaling Interface (ANS X3.230-1994 ANSI FC-PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22-7202).

8B/10B Transmission Code

The following information describes how the tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within the higher-level constructs specified by the standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit "a" is transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order. (Note that bit i is transmitted between bit e and bit f, rather than in alphabetical order.)

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two (not necessarily different) Transmission Characters. The two columns correspond to the current value of the running disparity ("Current RD-" or "Current RD+"). Running disparity is a binary parameter with either the value negative (-) or the value positive (+).

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Transmitter calculates a new value for its running disparity based on the contents of the transmitted character. Special Character codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3.230.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver decides whether the Transmission Character is valid or invalid according to the following rules and tables and calculates a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity are used to calculate the new running-disparity value for Transmission Characters that have been transmitted (Transmitter's running disparity) and that have been received (Receiver's running disparity).

Running disparity for a Transmission Character is calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other sub-block. Running disparity at the beginning of the 6-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the 6-bit sub-block if the 6-bit sub-block is 000111, and it is positive at the end of the 4-bit sub-block if the 4-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the 6-bit sub-block if the 6-bit sub-block is 111000, and it is negative at the end of the 4-bit sub-block if the 4-bit sub-block is 1100.
3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate encoding for the Valid Data byte or the Special Character byte into a Transmission Character is listed in the character encoding *Tables 11* and *12*. The current value of the Transmitter's running disparity is used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity is calculated. This new value is used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. *Table 9* shows naming notations and examples of valid transmission characters.

Table 9. Valid Transmission Characters

Data			
Byte Name	TX _{IN} or RX _{OUT}		Hex Value
	765	43210	
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
.	.	.	.
.	.	.	.
D5.2	010	000101	45
.	.	.	.
.	.	.	.
D30.7	111	11110	FE
D31.7	111	11111	FF



Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity is searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the associated Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's

validity, the received Transmission Character is used to calculate a new value of running disparity. The new value is used as the Receiver's current running disparity for the next received Transmission Character. Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. *Table 10* shows an example of this behavior.

Table 10. Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

Table 11. Valid Data Characters (TXSC/D* = LOW, RXSC/D* = LOW)

Data Byte Name	Bits	Current RD–		Current RD+		Data Byte Name	Bits	Current RD–		Current RD+	
	HGFEDCBA	abcdei	fghj	abcdei	fghj		HGFEDCBA	abcdei	fghj	abcdei	fghj
D0.0	000 00000	100111	0100	011000	1011	D0.1	001 00000	100111	1001	011000	1001
D1.0	000 00001	011101	0100	100010	1011	D1.1	001 00001	011101	1001	100010	1001
D2.0	000 00010	101101	0100	010010	1011	D2.1	001 00010	101101	1001	010010	1001
D3.0	000 00011	110001	1011	110001	0100	D3.1	001 00011	110001	1001	110001	1001
D4.0	000 00100	110101	0100	001010	1011	D4.1	001 00100	110101	1001	001010	1001
D5.0	000 00101	101001	1011	101001	0100	D5.1	001 00101	101001	1001	101001	1001
D6.0	000 00110	011001	1011	011001	0100	D6.1	001 00110	011001	1001	011001	1001
D7.0	000 00111	111000	1011	000111	0100	D7.1	001 00111	111000	1001	000111	1001
D8.0	000 01000	111001	0100	000110	1011	D8.1	001 01000	111001	1001	000110	1001
D9.0	000 01001	100101	1011	100101	0100	D9.1	001 01001	100101	1001	100101	1001
D10.0	000 01010	010101	1011	010101	0100	D10.1	001 01010	010101	1001	010101	1001
D11.0	000 01011	110100	1011	110100	0100	D11.1	001 01011	110100	1001	110100	1001
D12.0	000 01100	001101	1011	001101	0100	D12.1	001 01100	001101	1001	001101	1001
D13.0	000 01101	101100	1011	101100	0100	D13.1	001 01101	101100	1001	101100	1001
D14.0	000 01110	011100	1011	011100	0100	D14.1	001 01110	011100	1001	011100	1001
D15.0	000 01111	010111	0100	101000	1011	D15.1	001 01111	010111	1001	101000	1001
D16.0	000 10000	011011	0100	100100	1011	D16.1	001 10000	011011	1001	100100	1001
D17.0	000 10001	100011	1011	100011	0100	D17.1	001 10001	100011	1001	100011	1001
D18.0	000 10010	010011	1011	010011	0100	D18.1	001 10010	010011	1001	010011	1001
D19.0	000 10011	110010	1011	110010	0100	D19.1	001 10011	110010	1001	110010	1001
D20.0	000 10100	001011	1011	001011	0100	D20.1	001 10100	001011	1001	001011	1001
D21.0	000 10101	101010	1011	101010	0100	D21.1	001 10101	101010	1001	101010	1001
D22.0	000 10110	011010	1011	011010	0100	D22.1	001 10110	011010	1001	011010	1001
D23.0	000 10111	111010	0100	000101	1011	D23.1	001 10111	111010	1001	000101	1001



Table 11. Valid Data Characters (TXSC/D* = LOW, RXSC/D* = LOW) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGFEDCBA	abcdei fghj	abcdei fghj		HGFEDCBA	abcdei fghj	abcdei fghj
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011



Table 11. Valid Data Characters (TXSC/D* = LOW, RXSC/D* = LOW) (continued)

Data Byte Name	Bits HGFEDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGFEDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110



Table 11. Valid Data Characters (TXSC/D* = LOW, RXSC/D* = LOW) (continued)

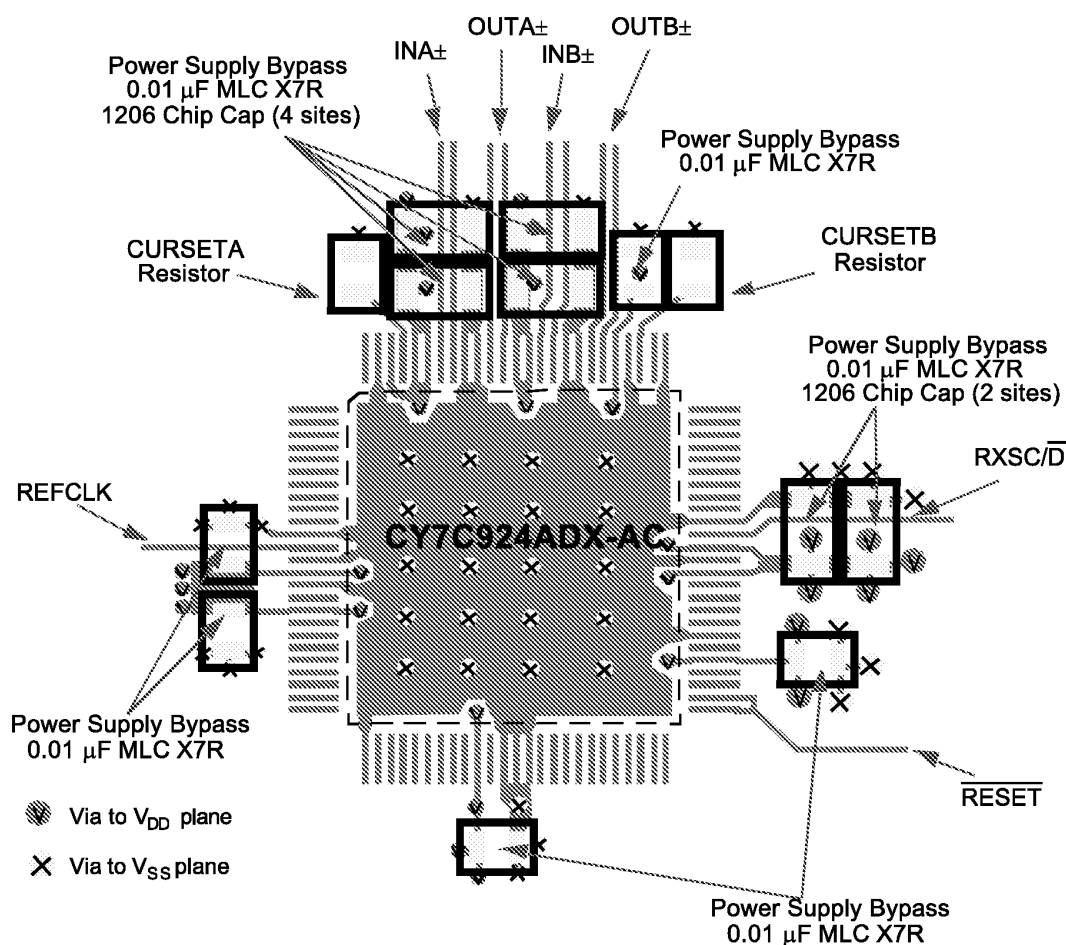
Data Byte Name	Bits HGFEDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGFEDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table 12. Valid Special Character Codes and Sequences (TXSC/D* = HIGH or RXSC/D* = HIGH)^[28, 29]

S.C. Byte Name	S.C. Code Name		Bits		Current RD–		Current RD+	
			HGF	EDCBA	abcdei	fghj	abcdei	fghj
K28.0	C0.0 ^[30]	(C00)	000	00000	001111	0100	110000	1011
K28.1	C1.0 ^[31]	(C01)	000	00001	001111	1001	110000	0110
K28.2	C2.0 ^[31]	(C02)	000	00010	001111	0101	110000	1010
K28.3	C3.0 ^[30]	(C03)	000	00011	001111	0011	110000	1100
K28.4	C4.0 ^[31]	(C04)	000	00100	001111	0010	110000	1101
K28.5	C5.0 ^[31, 32]	(C05)	000	00101	001111	1010	110000	0101
K28.6	C6.0 ^[31]	(C06)	000	00110	001111	0110	110000	1001
K28.7	C7.0 ^[31, 33]	(C07)	000	00111	001111	1000	110000	0111
K23.7	C8.0 ^[30]	(C08)	000	01000	111010	1000	000101	0111
K27.7	C9.0 ^[30]	(C09)	000	01001	110110	1000	001001	0111
K29.7	C10.0 ^[30]	(C0A)	000	01010	101110	1000	010001	0111
K30.7	C11.0	(C0B)	000	01011	011110	1000	100001	0111
End of Frame Sequence								
EOFxx	C2.1 ^[34]	(C22)	001	00010	–K28.5,Dn.xxx0		+K28.5,Dn.xxx1	
Code Rule Violation and SVS Tx Pattern								
Exception	C0.7 ^[33, 35]	(CE0)	111	00000	100111	1000	011000	0111
–K28.5	C1.7 ^[36]	(CE1)	111	00001	001111	1010	001111	1010
+K28.5	C2.7 ^[37]	(CE2)	111	00010	110000	0101	110000	0101
Running Disparity Violation Pattern								
Exception	C4.7 ^[38]	(CE4)	111	00100	110111	0101	001000	1010

Notes:

28. All codes not shown are reserved.
29. Notation for Special Character Code Name is consistent with Fibre Channel and ESCON naming conventions. Special Character Code Name is intended to describe binary information present on I/O pins. Common usage for the name can either be in the form used for describing Data patterns (i.e., C0.0 through C31.7), or in hex notation (i.e., Cnn where nn = the specified value between 00h and FFh).
30. These characters have reserved meanings when command processing is enabled. This includes all operating modes where the FIFOs are enabled and the discard policy is not 0.
31. These characters are used for control of ESCON interfaces. They can be sent as embedded commands or other markers when not operating using ESCON protocols.
32. The K28.5 character is used for framing operations by the receiver. It is also the pad or fill character transmitted to maintain the serial link when no user data is available.
33. Care must be taken when using this Special Character code. When a C7.0 or C0.7 is followed by a D11.x or D20.x, an alias K28.5 sync character is created. These sequences can cause erroneous framing and should be avoided while RFEN is HIGH.
34. C2.1 = Transmit either –K28.5+ or +K28.5– as determined by Current RD and modify the following Transmission Character by setting its least significant bit to 1 or 0. If Current RD at the start of the following character is plus (+) the LSB is set to 0, and if Current RD is minus (–) the LSB becomes 1. This modification allows construction of X3.230:1994 "EOF" frame delimiters wherein the second data byte is determined by the Current RD.
For example, to send "EOFdt" the controller could issue the sequence C2.1–D21.4– D21.4–D21.4, and the HOTLink Transmitter will send either K28.5–D21.4–D21.4–D21.4 or K28.5–D21.5– D21.4–D21.4 based on Current RD. Likewise to send "EOFdt" the controller could issue the sequence C2.1–D10.4–D21.4–D21.4, and the HOTLink Transmitter will send either K28.5–D10.4–D21.4– D21.4 or K28.5–D10.5–D21.4– D21.4 based on Current RD.
The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.
35. C0.7 = Transmit a deliberate code rule violation. The code chosen for this function follows the normal Running Disparity rules. Transmission of this Special Character has the same effect as asserting TXSVS = HIGH. The receiver outputs this Special Character only if the Transmission Character being decoded is not found in the tables.
36. C1.7 = Transmit Negative K28.5 (–K28.5+) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C1.7 if –K28.5 is received with RD+, otherwise K28.5 is decoded as C5.0 or C2.7.
37. C2.7 = Transmit Positive K28.5 (+K28.5–) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C2.7 if +K28.5 is received with RD–, otherwise K28.5 is decoded as C5.0 or C1.7.
38. C4.7 = Transmit a deliberate code rule violation to indicate a Running Disparity violation. The receiver will only output this Special Character if the Transmission Character being decoded is found in the tables, but Running Disparity does not match. This may indicate that an error occurred in a prior byte.

Printed Circuit Board Layout Suggestions


This is a typical printed circuit board layout showing example placement of power supply bypass components and other components mounted on the same side as the CY7C924ADX.

Other layouts, including cases with components mounted on the reverse side would work as well.

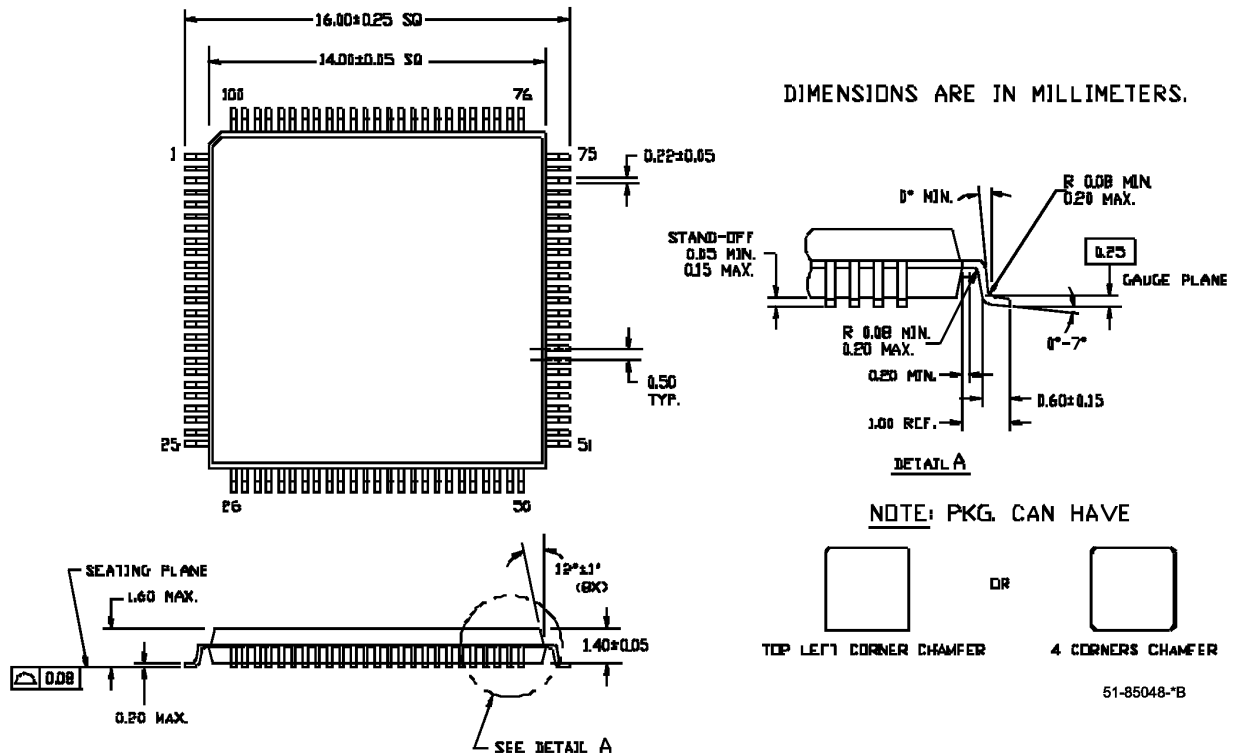
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7C924ADX-AC	A100	100-Lead Thin Quad Flat Pack	Commercial
CY7C924ADX-AI	A100	100-Lead Thin Quad Flat Pack	Industrial



Package Diagram

100-pin Thin Plastic Quad Flat Pack (TQFP) A100



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**Document History Page**

Document Title: CY7C924ADX 200-MBaud HOTLink® Transceiver Document Number: 38-02008				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	105846	03/26/01	SZV	Change from Spec number: 38-00770 to 38-02008
*A	107878	07/09/01	KET	Changed part number: CY7C924DX to CY7C924ADX
*B	118320	11/13/02	REV	Changed the mentioning of PECL inputs and outputs to PECL-compatible inputs and outputs, which is more correct. Changed the font and centered the part number in the device footprint Fixed the line wrap issue with DLB[1] and DLB[0] Changed labels on waveforms to make them more consistent with those in the tables Changed the I/O labels on the D-type flip flop Changed mentioning of PAREN to TXPAREN to make data sheet more consistent
*C	123796	01/29/03	KKV	Replaced incorrect source copy with correct source copy
D	201401	01/19/04	TNT	Removed parity Changed device selection requirements when in FIFO Bypass mode Added comprehensive table showing SPDSEL/RANGESEL and data rate mapping Cascade mode read timing description changed, receive timing diagram updated to reflect operation Serial Address Register access listed as an option for Utopia mode only Changed FIFO reset condition to show that the count is suspended, not reset, when TXEN is asserted





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17/157,350	01/25/2021	Igor Polishchuk	PM07027D1CIP1C6

CONFIRMATION NO. 6135

PUBLICATION NOTICE



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36491
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Title:MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Publication No.US-2021-0217862-A1

Publication Date:07/15/2021

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	Filing Date	2021-01-25
	First Named Inventor	Igor Polishchuk
	Art Unit	1737
	Examiner Name	
	Attorney Docket Number	PM07027D1CIP1C6

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	3	20080173928	A1	2008-07-24	Arai et al.		
	4	20120068255	A1	2012-03-22	SAMSUNG ELECTRONICS CO LTD		
	5	20080093661	A1	2008-04-24	HYNIX SEMICONDUCTOR INC [KR]		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17157350	
	Filing Date		2021-01-25	
	First Named Inventor	Igor Polishchuk		
	Art Unit	1737		
	Examiner Name			
	Attorney Docket Number	PM07027D1CIP1C6		

	6	20070158736	A1	2007-07-12	KABUSHIKI KAISHA TOSHIBA
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17157350
	Filing Date	2021-01-25
	First Named Inventor	Igor Polishchuk
	Art Unit	1737
	Examiner Name	
	Attorney Docket Number	PM07027D1CIP1C6

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Signature	/Michael L. Bartholomew/	Date (YYYY-MM-DD)	2021-08-02
Name/Print	Michael L. Bartholomew	Registration Number	60225

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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Electronic Acknowledgement Receipt

EFS ID:	43404971
Application Number:	17157350
International Application Number:	
Confirmation Number:	6135
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	36491
Filer:	Michael Lee Bartholomew
Filer Authorized By:	
Attorney Docket Number:	PM07027D1CIP1C6
Receipt Date:	02-AUG-2021
Filing Date:	25-JAN-2021
Time Stamp:	17:25:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C6_IDS.pdf	612289 ea414d297ca0398cc45e818f495c89a729862539	no	4

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	Filing Date		2021-01-25
	First Named Inventor	Igor Polishchuk	
	Art Unit	1737	
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Signature	/Michael L. Bartholomew/	Date (YYYY-MM-DD)	2021-08-18
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JP2010140997A NONVOLATILE SEMICONDUCTOR MEMORY DEVICE, AND METHOD FOR MANUFACTURING THE SAME

Applicants: TOSHIBA CORP

Inventors: OZAWA YOSHIO

Classifications:

IPC *H01L21/8247; H01L27/115; H01L29/788; H01L29/792;*CPC *H01L21/02255 (US); H01L21/02667 (US); H01L27/11582 (EP,US); H01L29/0657 (EP,US);
H01L29/40117 (EP,US); H01L29/4234 (EP,US); H01L29/66833 (EP,US); H01L29/792 (EP,US);
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Priorities: JP2008314187A 2008-12-10

Application: JP2010140997A 2008-12-10

Publication: JP2010140997A 2010-06-24

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US2010140684A1; **US2011156131A1**; **US2014357032A1**; **US2015137212A1**; **US7927953B2**; **US8841183B2**; **US8946021B2**;
US9219076B2

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE, AND METHOD FOR MANUFACTURING THE SAME

Abstract

PROBLEM TO BE SOLVED: To provide a nonvolatile semiconductor memory device such that the operating speed of a cell transistor is fast and variation in threshold is small, and to provide a method of manufacturing the nonvolatile semiconductor memory device. SOLUTION: On a silicon substrate 11 there is formed a stacked body 14 by alternately stacking a plurality of silicon oxide films 12 and silicon films 13, a trench 15 is formed in the stacked body 14, an alumina film 16, a silicon nitride film 17 and a silicon oxide film 18 are formed in this order on an inner surface of the trench 15, and a channel silicon crystalline film 20 is formed on the silicon oxide film 18. Next, a silicon oxide layer 21a is formed at an interface between the silicon oxide film 18 and the channel silicon crystalline film 20 by performing thermal treatment in an oxygen gas atmosphere. COPYRIGHT: (C)2010,JPO&INPIT

(19) 日本国特許庁(JP)

(12) 公開特許公報(A)

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(22) 出願日	平成20年12月10日 (2008.12.10)		株式会社東芝
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			東芝内
		Fターム(参考)	5F083 EP18 EP22 EP48 EP49 EP50
			EP76 GA01 GA06 GA10 GA11
			GA21 JA03 JA05 JA19 PR03
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			PR40
			5F101 BA45 BA47 BA53 BB02 BD16
			BD30 BD34 BD35 BF02 BF03
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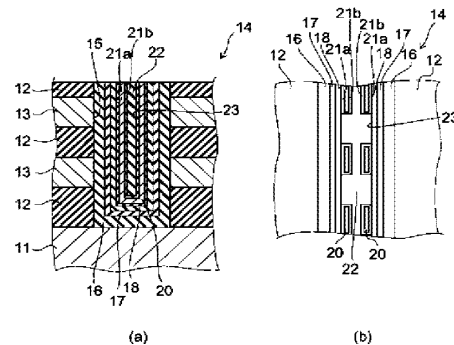
(54) 【発明の名称】 不揮発性半導体記憶装置及びその製造方法

(57) 【要約】

【課題】セルトランジスタの動作速度が速く、しきい値の変動が小さい不揮発性半導体記憶装置及びその製造方法を提供する。

【解決手段】シリコン基板11上にそれぞれ複数のシリコン酸化膜12及びシリコン膜13を交互に積層して積層体14を形成し、積層体14にトレンチ15を形成し、トレンチ15の内面上にアルミナ膜16、シリコン窒化膜17、シリコン酸化膜18をこの順に形成し、シリコン酸化膜18上にチャネルシリコン結晶膜20を形成する。次に、酸素ガス雰囲気中で熱処理を行い、シリコン酸化膜18とチャネルシリコン結晶膜20との界面にシリコン酸化物層21aを形成する。

【選択図】 図6



【特許請求の範囲】

【請求項 1】

ゲート電極上に、電荷蓄積膜、トンネル絶縁膜及びシリコン結晶からなるチャネル膜をこの順に形成する工程と、

酸素ガス雰囲気中で熱処理を行い、前記トンネル絶縁膜と前記チャネル膜との界面にシリコン酸化物層を形成する工程と、

を備えたことを特徴とする不揮発性半導体記憶装置の製造方法。

【請求項 2】

ゲート電極上に、電荷蓄積膜、トンネル絶縁膜及びシリコン結晶からなるチャネル膜をこの順に形成する工程と、

一酸化窒素ガス雰囲気中で熱処理を行い、前記トンネル絶縁膜と前記チャネル膜との界面にシリコン酸窒化物層を形成する工程と、

を備えたことを特徴とする不揮発性半導体記憶装置の製造方法。

【請求項 3】

基板上にそれぞれ複数の層間絶縁膜及び前記ゲート電極を交互に積層して積層体を形成する工程と、

前記積層体にトレンチを形成する工程と、

をさらに備え、

前記電荷蓄積膜、前記トンネル絶縁膜及び前記チャネル膜は、前記トレンチの内面上に形成し、

前記熱処理を行うときに、前記トレンチ内に、前記トレンチの外部に通じ、内面に前記チャネル膜が露出した空洞が形成されていることを特徴とする請求項 1 または 2 に記載の不揮発性半導体記憶装置の製造方法。

【請求項 4】

前記熱処理の後、前記空洞の内面において前記チャネル膜を露出させる工程と、

前記空洞内にシリコンを埋め込む工程と、

をさらに備えたことを特徴とする請求項 3 に記載の不揮発性半導体記憶装置の製造方法。

【請求項 5】

基板と、

前記基板上に設けられ、それぞれ複数の層間絶縁膜及びゲート電極が交互に積層され、トレンチが形成された積層体と、

前記トレンチの内面上に設けられた電荷蓄積膜と、

前記電荷蓄積膜上に設けられたトンネル絶縁膜と、

前記トンネル絶縁膜上に設けられ、シリコン結晶からなるチャネル膜と、

を備え、

前記トンネル絶縁膜と前記チャネル膜との界面に、シリコン酸化物層又はシリコン酸窒化物層が形成されていることを特徴とする不揮発性半導体記憶装置。

【発明の詳細な説明】

【技術分野】

【0001】

本発明は、不揮発性半導体記憶装置及びその製造方法に関し、特に、絶縁膜上にシリコンからなるチャネル膜を形成した不揮発性半導体記憶装置及びその製造方法に関する。

【背景技術】

【0002】

近年、平面型の不揮発性半導体記憶装置に替わって、複数の MONOS (Metal-Oxide-Nitride-Oxide-Silicon) 型メモリセルを 3 次元的に積層させた不揮発性半導体記憶装置が開発されている (例えば、特許文献 1 参照。)。この不揮発性半導体記憶装置を製造する際には、基板上にゲート電極及び層間絶縁膜を交互に形成して積層体を形成し、この積層体に積層方向に延びる貫通ホールを形成し、貫通ホールの内面上に電荷ブロック膜、電荷蓄積膜及びトンネル絶縁膜をこの順に形成し、その後、例えば CVD 法 (Chemical Vap

or Deposition法：化学気相成長法）によりシリコンを堆積させている。これにより、貫通ホール内に垂直方向に延びるシリコンピラーが埋設され、これがメモリセルのチャンネルとなる。

【0003】

しかしながら、この製造方法では、トンネル絶縁膜上にシリコンを堆積させてシリコンピラーを形成しているため、トンネル絶縁膜とシリコンピラーとの界面に欠陥が高密度に導入され、この欠陥が界面準位や固定電荷を形成してしまう。これにより、メモリセルを構成するセルトランジスタの動作速度が遅くなり、また、長期間の使用によってセルトランジスタのしきい値が変動し、誤動作が発生する。

【0004】

【特許文献1】特開2008-171918号公報

【発明の開示】

【発明が解決しようとする課題】

【0005】

本発明の目的は、セルトランジスタの動作速度が速く、しきい値の変動が小さい不揮発性半導体記憶装置及びその製造方法を提供することである。

【課題を解決するための手段】

【0006】

本発明の一態様によれば、ゲート電極上に、電荷蓄積膜、トンネル絶縁膜及びシリコン結晶からなるチャンネル膜をこの順に形成する工程と、酸素ガス雰囲気中で熱処理を行い、前記トンネル絶縁膜と前記チャンネル膜との界面にシリコン酸化物層を形成する工程と、を備えたことを特徴とする不揮発性半導体記憶装置の製造方法が提供される。

【0007】

本発明の他の一態様によれば、ゲート電極上に、電荷蓄積膜、トンネル絶縁膜及びシリコン結晶からなるチャンネル膜をこの順に形成する工程と、一酸化窒素ガス雰囲気中で熱処理を行い、前記トンネル絶縁膜と前記チャンネル膜との界面にシリコン酸窒化物層を形成する工程と、を備えたことを特徴とする不揮発性半導体記憶装置の製造方法が提供される。

【0008】

本発明のさらに他の一態様によれば、基板と、前記基板上に設けられ、それぞれ複数の層間絶縁膜及びゲート電極が交互に積層され、トレンチが形成された積層体と、前記トレンチの内面上に設けられた電荷蓄積膜と、前記電荷蓄積膜上に設けられたトンネル絶縁膜と、前記トンネル絶縁膜上に設けられ、シリコン結晶からなるチャンネル膜と、を備え、前記トンネル絶縁膜と前記チャンネル膜との界面に、シリコン酸化物層又はシリコン酸窒化物層が形成されていることを特徴とする不揮発性半導体記憶装置が提供される。

【発明の効果】

【0009】

本発明によれば、セルトランジスタの動作速度が速く、しきい値の変動が小さい不揮発性半導体記憶装置及びその製造方法を実現することができる。

【発明を実施するための最良の形態】

【0010】

以下、図面を参照しつつ、本発明の実施形態について説明する。

まず、本発明の第1の実施形態について説明する。

図1(a)及び(b)乃至図6(a)及び(b)は、本実施形態に係る不揮発性半導体記憶装置の製造方法を例示する図であり、各図の(a)は工程断面図であり、各図の(b)は工程平面図である。

【0011】

まず、図1(a)及び(b)に示すように、シリコン基板11上に、例えばCVD法により、層間絶縁膜となるシリコン酸化膜12と、ゲート電極となる不純物をドーピングしたシリコン膜13とを交互に堆積させて、積層体14を形成する。シリコン酸化膜12及びシリコン膜13の厚さは、例えばそれぞれ50nm(ナノメートル)とする。なお、図

1 (a) には、シリコン膜 13 が 2 枚のみ図示されているが、本実施形態はこれに限定されず、シリコン膜 13 は何枚でもよい。

【0012】

次に、図 2 (a) 及び (b) に示すように、積層体 14 上にレジストマスク (図示せず) を形成し、これをマスクとして R I E (Reactive Ion Etching: 反応性イオンエッチング) を施し、シリコン酸化膜 12 及びシリコン膜 13 を選択的に除去して、積層体 14 にトレンチ 15 を形成する。トレンチ 15 の形状は溝状であり、その幅は例えば 70 nm 程度である。トレンチ 15 の側面には、層間絶縁膜であるシリコン酸化膜 12 及びゲート電極であるシリコン膜 13 が露出する。また、トレンチ 15 の底面にはシリコン基板 11 が露出する。

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【0013】

次に、図 3 (a) 及び (b) に示すように、A L D (Atomic Layer Deposition: 原子層蒸着) 法により、トレンチ 15 の内面上に、電荷ブロック膜となる厚さが例えば 10 nm のアルミナ膜 16、電荷蓄積膜となる厚さが例えば 5 nm のシリコン窒化膜 17、トンネル絶縁膜となる厚さが例えば 5 nm のシリコン酸化膜 18 をこの順に堆積させる。

【0014】

次に、C V D 法により、シリコン酸化膜 18 上に、不純物をドーピングした非晶質シリコン膜を例えば 10 nm の厚さに堆積させる。このとき、C V D の原料ガスには、例えばシラン (SiH_4) を用いる。また、非晶質シリコン膜はトレンチ 15 内を完全には埋め込まずに、トレンチ 15 内に空洞が残る。その後、温度が例えば 500 °C 以上の熱処理を施し、この非晶質シリコン膜を結晶化させ、多結晶シリコン膜 19 とする。なお、C V D の成膜温度を調整すれば、シリコン酸化膜 18 上に多結晶シリコンを堆積させることにより、多結晶シリコン膜 19 を形成することもできる。

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【0015】

次に、図 4 (a) 及び (b) に示すように、積層体 14 上にレジストマスク (図示せず) を形成し、これをマスクとして R I E を施し、多結晶シリコン膜 19 を選択的に除去する。これにより、多結晶シリコン膜 19 をトレンチ 15 が延びる方向に沿って分断し、複数本の U 字形のチャネルシリコン結晶膜 20 とする。このとき、トレンチ 15 内におけるアルミナ膜 16、シリコン窒化膜 17、シリコン酸化膜 18 及びチャネルシリコン結晶膜 20 が設けられていない部分は、空洞 23 となる。空洞 23 はトレンチ 15 の外部に通じ、内面にチャネルシリコン結晶膜 20 が露出している。なお、図 4 (b) においては、チャネルシリコン結晶膜 20 が 3 本のみ図示されているが、本実施形態はこれに限定されず、何本でもよい。

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【0016】

次に、図 5 (a) 及び (b) に示すように、酸素ガス (O_2) 雰囲気中で熱酸化処理を行う。この熱酸化処理の条件は、温度を例えば 700 ~ 1200 °C とし、時間を例えば 1 分 ~ 1 時間とする。これにより、チャネル膜 (チャネルシリコン結晶膜 20) とトンネル絶縁膜 (シリコン酸化膜 18) との界面に、厚さが例えば 0.2 ~ 2 nm 程度のシリコン酸化物層 21 a が形成される。なお、この熱酸化処理により、チャネルシリコン結晶膜 20 の露出面にもシリコン酸化物層 21 b が形成される。シリコン酸化物層 21 b の厚さは、チャネルシリコン結晶膜 20 の厚さと熱処理条件に依存するが、概ね、シリコン酸化物層 21 a の厚さの 1.5 ~ 3 倍程度となる。

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【0017】

次に、図 6 (a) 及び (b) に示すように、全面にシリコン酸化物を堆積又は塗布して、空洞 23 内にシリコン酸化物 22 を埋め込む。シリコン酸化物 22 は素子分離絶縁膜を形成する。次に、C M P (Chemical Mechanical Polishing: 化学的機械研磨) を行い、積層体 14 の上面上からシリコン酸化物 22 及びシリコン酸化物層 21 b を除去し、チャネルシリコン結晶膜 20 の上面を露出させる。これにより、シリコン基板 11 上にメモリアレイ部が形成される。メモリアレイ部においては、U 字形のチャネルシリコン結晶膜 20 ごとに N A N D ストリングが構成されており、各 N A N D ストリングにおいては、チャ

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ネルシリコン結晶膜 20 が延びる方向に沿って複数の MONOS 型メモリセルトランジスタが配列され、直列に接続されている。その後、周知の技術により、選択ゲートトランジスタ、配線層及び周辺素子（いずれも図示せず）等を形成し、3次元積層構造の不揮発性半導体製造装置を製造する。

【0018】

図 6 (a) 及び (b) に示すように、この不揮発性半導体記憶装置においては、シリコン基板 11 上に、それぞれ複数の層間絶縁膜（シリコン酸化膜 12）及びゲート電極（シリコン膜 13）が交互に積層された積層体 14 が設けられており、積層体 14 にはトレンチ 15 が形成されている。また、トレンチ 15 の内面上には、電荷ブロック膜（アルミナ膜 16）、電荷蓄積膜（シリコン窒化膜 17）、トンネル絶縁膜（シリコン酸化膜 18）がこの順に設けられており、トンネル絶縁膜（シリコン酸化膜 18）上にはシリコン結晶からなるチャネルシリコン結晶膜 20 が設けられている。そして、トンネル絶縁膜（シリコン酸化膜 18）とチャネル膜（チャネルシリコン結晶膜 20）との界面には、シリコン酸化物層 21a が形成されている。

【0019】

次に、本実施形態の作用効果について説明する。

本実施形態においては、3次元積層型の不揮発性半導体記憶装置を効率よく製造するために、層間絶縁膜（シリコン酸化膜 12）とゲート電極（シリコン膜 13）を交互に堆積させて積層体 14 を形成した後、トレンチ 15 を形成し、トレンチ 15 の内面上に電荷ブロック膜（アルミナ膜 16）、電荷蓄積膜（シリコン窒化膜 17）、トンネル絶縁膜（シリコン酸化膜 18）を成膜し、その上にチャネル膜（チャネルシリコン結晶膜 20）を形成している。すなわち、図 3 (a) 及び (b) に示す工程において、シリコン酸化膜 18 上に、CVD 法により非晶質シリコン膜を堆積させている。このとき、シリコン酸化膜 18 と非晶質シリコン膜との界面には、CVD の原料ガス（例えばシラン）に起因する水酸基が残留したり、未結合手が発生したりして、欠陥が発生する。この欠陥は、非晶質シリコン膜が結晶化され、加工されてチャネルシリコン結晶膜 20 となったときに、シリコン酸化膜 18 とチャネルシリコン結晶膜 20 との界面に残留し、界面準位や固定電荷を発生させる。

【0020】

そこで、本実施形態においては、図 5 (a) 及び (b) に示す工程において、酸素ガス雰囲気中で熱処理を行っている。結晶状態のシリコンからなるチャネルシリコン結晶膜 20 を酸素ガス雰囲気中に晒した状態で熱処理を行うと、チャネルシリコン結晶膜 20 の露出面にシリコン酸化物層 21b が生成されると共に、その反対面、すなわち、シリコン酸化膜 18 との界面にもシリコン酸化物層 21a が形成される。これは、酸素ガスはシリコン膜内では解離しにくく、拡散してシリコン膜の反対側の面に到達し、そこで解離して酸化反応が起こるためと考えられる。そして、シリコン酸化膜 18 とチャネルシリコン結晶膜 20 との界面にシリコン酸化物層 21a が形成されることにより、シリコン酸化膜 18 とチャネルシリコン結晶膜 20 との界面に発生していた欠陥がシリコン酸化物層 21a 内に取り込まれ、界面準位及び固定電荷が大幅に低減する。一例では、界面準位及び固定電荷の密度は、シリコン酸化物層 21a を形成しない場合には $1 \times 10^{12} \text{ cm}^{-2}$ 以上であるが、シリコン酸化物層 21a を形成すると $1 \times 10^{11} \text{ cm}^{-2}$ 以下まで減少する。

【0021】

このように、本実施形態によれば、トンネル絶縁膜であるシリコン酸化膜 18 とチャネル膜であるチャネルシリコン結晶膜 20 との界面の状態が大幅に改善されるため、セルトランジスタの動作速度が向上する。また、長期間使用してもセルトランジスタのしきい値が変動しにくくなり、メモリの信頼性が向上する。

【0022】

また、本実施形態においては、図 5 (a) 及び (b) に示す熱処理を行うときに、トレンチ 15 内に、トレンチ 15 の外部に通じ、内面にチャネルシリコン結晶膜 20 が露出した空洞 23 が形成されている。このため、雰囲気中の酸素ガスが空洞 23 を介してチャネ

ルシリコン結晶膜 20 の全体に効率的に供給され、シリコン酸化膜 18 とチャネルシリコン結晶膜 20 との界面全体にシリコン酸化物層 21 a が形成される。

【0023】

なお、上述の例では、非晶質シリコン膜を結晶化させて多結晶シリコン膜 19 とし、分割加工してチャネルシリコン結晶膜 20 とした後、酸素ガス雰囲気中で熱処理を行いシリコン酸化物層 21 a を形成しているが、本実施形態はこれには限定されず、酸素ガス雰囲気中での熱処理の前に、シリコン膜が結晶化されていればよい。例えば、非晶質シリコン膜を分割加工した後、結晶化させ、その後、酸素ガス雰囲気中の熱処理を行ってもよく、非晶質シリコン膜を結晶化させ、酸素ガス雰囲気中で熱処理した後、分割加工してもよい。但し、分割加工の後に酸素ガス雰囲気中の熱処理を行った方が、酸素ガスの供給効率が高いため、シリコン酸化物層 21 a が形成されやすく、また、分割加工時のダメージを回復させることができるため、望ましい。

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【0024】

次に、本発明の第 2 の実施形態について説明する。

図 7 (a) 及び (b) 乃至図 8 (a) 及び (b) は、本実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、各図の (b) は、(a) に示す領域 R の一部拡大図である。

【0025】

まず、前述の第 1 の実施形態と同様な方法により、図 4 (a) 及び (b) に示す構造体を作製する。次に、図 7 (a) に示すように、一酸化窒素ガス (NO) 雰囲気中で熱酸化処理を行う。この熱酸化処理の条件は、温度を例えば 700 ~ 1200 °C とし、時間を例えば 1 分 ~ 1 時間とする。なお、一酸化窒素ガス雰囲気とは、一酸化窒素ガスのみを含む雰囲気には限定されず、一酸化窒素ガスを含む雰囲気であればよい。

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【0026】

この熱酸化処理により、チャネルシリコン結晶膜 20 とシリコン酸化膜 18 との界面に、厚さが例えば 0.2 ~ 2 nm 程度のシリコン酸窒化物層 24 a が形成される。なお、このとき、チャネルシリコン結晶膜 20 の露出面にもシリコン酸窒化物層 24 b が形成される。このシリコン酸窒化物層 24 b の厚さは、チャネルシリコン結晶膜 20 の厚さと熱処理条件に依存するが、概ね、シリコン酸窒化物層 24 a の厚さの 1.5 ~ 3 倍程度となる。チャネルシリコン結晶膜 20 の露出面だけでなくシリコン酸化膜 18 との界面にもシリコン酸窒化物層が形成される理由は、一酸化窒素ガスはシリコン膜内では解離しにくく、露出面からシリコン膜内に拡散してシリコン膜の反対面に到達し、そこで解離して酸化反応と窒化反応が起こるためであると考えられる。

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【0027】

また、このとき、図 7 (b) に示すように、シリコン酸窒化物層 24 a 及び 24 b においては、層厚方向で組成が傾斜する。すなわち、シリコン酸窒化物層 24 a 及び 24 b のそれぞれにおいて、チャネルシリコン結晶膜 20 側には窒素濃度が相対的に高い窒素リッチ層 24 N が形成され、チャネルシリコン結晶膜 20 から遠い側には酸素濃度が相対的に高い酸素リッチ層 24 O が形成される。これは、熱酸化処理によりシリコン膜の表面にシリコン酸窒化物層を形成する過程で、シリコン酸窒化物層中の窒素原子はシリコン膜とシリコン酸窒化物層との界面に偏析しやすいためであると考えられる。

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【0028】

次に、図 8 (a) 及び (b) に示すように、前述の第 1 の実施形態と同様に、空洞 23 内に素子分離絶縁膜としてシリコン酸化物 22 を埋め込む。次に、CMP を行って積層体 14 の上面上からシリコン酸化物 22 及びシリコン酸窒化物層 24 b を除去し、チャネルシリコン結晶膜 20 の上面を露出させる。この結果、シリコン基板 11 上にメモリアレイ部が形成される。その後、400 °C ~ 1000 °C 程度の温度で熱アニール処理を行って、シリコン酸化物 22 を緻密化する。これにより、シリコン酸化物 22 のリーク電流を低減し、メモリ誤動作の発生頻度を低減できる。その後、選択ゲートトランジスタ、配線層及び周辺素子 (いずれも図示せず) 等を形成し、3 次元積層構造の不揮発性半導体製造装置

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を製造する。

【0029】

本実施形態に係る不揮発性半導体記憶装置においては、前述の第1の実施形態と比較して、トンネル絶縁膜（シリコン酸化膜18）とチャネル膜（チャネルシリコン結晶膜20）との界面には、シリコン酸化物層21a（図6参照）の代わりに、シリコン酸窒化物層24aが形成されている。

【0030】

次に、本実施形態の作用効果について説明する。

本実施形態においては、図7（a）及び（b）に示す工程において、一酸化窒素ガス雰囲気中で熱酸窒化処理を行っている。これにより、チャネルシリコン結晶膜20とシリコン酸化膜18との界面に、シリコン酸窒化物層24aが形成される。そして、シリコン酸窒化物層24aは、チャネルシリコン結晶膜20側に形成された窒素リッチ層24Nと、シリコン酸化膜18側に形成された酸素リッチ層24Oとの積層膜となる。

【0031】

この結果、シリコン酸化膜18とチャネルシリコン結晶膜20との界面に発生した欠陥が、窒素リッチ層24N内に取り込まれ、界面準位及び固定電荷が大幅に低減する。一例では、界面準位及び固定電荷の密度は、シリコン酸窒化物層24aを形成しない場合には $1 \times 10^{12} \text{ cm}^{-2}$ 以上であるが、シリコン酸窒化物層24aを形成すると $1 \times 10^{11} \text{ cm}^{-2}$ 以下まで減少する。これにより、セルトランジスタの動作速度が向上する。また、窒素リッチ層24Nがチャネルシリコン結晶膜20に接して設けられているため、メモリセルに対してデータの書込／消去を繰り返し行っても、界面準位の増大のような界面状態の劣化が抑制されて、セルトランジスタの信頼性が飛躍的に向上する。

【0032】

また、本実施形態によれば、シリコン酸化物22を緻密化するための熱アニール処理の際に、チャネルシリコン結晶膜20の表面がシリコン酸窒化物層24a及び24bによって覆われているため、チャネルシリコン結晶膜20が酸化されて体積が減少することを抑制できる。これにより、セルトランジスタの誤動作の発生頻度を大幅に低減することができ、装置の信頼性が向上する。更に、チャネルシリコン結晶膜20の両界面に窒素リッチ層24Nが設けられているため、熱アニール時にチャネルシリコン結晶膜20が凝集して変形することを防止できる。

【0033】

なお、本実施形態においては、図7（a）及び（b）に示す工程において、一酸化窒素ガス雰囲気の代わりに亜酸化窒素ガス雰囲気中で熱処理を行っても、同様な効果を得ることができる。この場合には、チャネルシリコン結晶膜20の露出面に形成されるシリコン酸窒化物層24bの膜厚が厚くなる傾向があるため、チャネルシリコン結晶膜20の仕上がり膜厚を薄くしたい場合に好適である。

【0034】

次に、本発明の第3の実施形態について説明する。

図9（a）及び（b）乃至図14（a）及び（b）は、本実施形態に係る不揮発性半導体記憶装置の製造方法を例示する図であり、各図の（a）は工程断面図であり、各図の（b）は工程平面図である。

本実施形態は、前述の第1の実施形態と比較して、トレンチの形状が溝形ではなく円柱形であること、及び、チャネルシリコン結晶層をシリコン基板に到達させることが異なっている。

【0035】

まず、図9（a）及び（b）に示すように、前述の第1の実施形態と同様な方法により、シリコン基板11上に積層体14を形成する。

次に、図10（a）及び（b）に示すように、レジストマスク（図示せず）を用いてR1Eを行い、積層体14に複数本のトレンチ25を形成する。トレンチ25の形状は積層体14の積層方向に延びる円柱形とし、その内径は例えば70nmとする。また、積層体

14の積層方向から見て、トレンチ25は例えばマトリクス状に配列させる。更に、各トレンチ25の底面にはシリコン基板11を露出させる。なお、図示の便宜上、各図には1本のトレンチ25のみを示しているが、実際には多数のトレンチ25を形成する。

【0036】

次に、図11(a)及び(b)に示すように、ALD法により、トレンチ25の内面上に、アルミナ膜16、シリコン窒化膜17、シリコン酸化膜18をこの順に堆積させる。これらの膜の厚さは、例えば、それぞれ10nm、5nm、5nmとする。装置の完成後、これらの膜は、それぞれ、電荷ブロック膜、電荷蓄積膜、トンネル絶縁膜として機能する。

【0037】

次に、図12(a)及び(b)に示すように、積層体14上にレジストマスク(図示せず)を形成し、これをマスクとしてRIEを行うことにより、トレンチ25の底面上からシリコン酸化膜18、シリコン窒化膜17、アルミナ膜16を選択的に除去し、シリコン基板11を露出させる。このとき、シリコン基板11の上面が少し掘り込まれる。

【0038】

次に、CVD法により、トレンチ25の内面上に、不純物をドーピングした非晶質シリコン膜を例えば10nmの厚さに堆積させる。その後、温度が例えば500℃以上の熱処理を施して、この非晶質シリコン膜を結晶化させ、チャンネルシリコン結晶膜30とする。チャンネルシリコン結晶膜30の下端部はシリコン基板11に接触する。また、チャンネルシリコン結晶膜30の形状は、底部が閉じた円筒形となり、その内部は空洞33となる。すなわち、空洞33はトレンチ25の外部に通じ、内面にチャンネルシリコン結晶膜30が露出する。なお、CVDの成膜温度を調整すれば、トレンチ25の内面上に多結晶シリコンを堆積させることにより、チャンネルシリコン結晶膜30を形成することもできる。

【0039】

次に、図13(a)及び(b)に示すように、酸素ガス(O₂)雰囲気中で熱酸化処理を行う。この熱酸化処理の条件は、温度を例えば700～1200℃とし、時間を例えば1分～1時間とする。これにより、チャンネルシリコン結晶膜30とシリコン酸化膜18等との界面に、シリコン酸化物層31aが形成される。シリコン酸化物層31aの厚さは、例えば0.2～2nm程度となる。なお、この熱酸化処理により、チャンネルシリコン結晶膜30の露出面にもシリコン酸化物層31bが形成される。このシリコン酸化物層31bの厚さは、チャンネルシリコン結晶膜30の厚さと熱処理条件に依存するが、概ね、シリコン酸化物層31aの厚さの1～2倍程度となる。一方、チャンネルシリコン結晶膜30とシリコン基板11との界面には、シリコン酸化物層はほとんど形成されない。

【0040】

次に、図14(a)及び(b)に示すように、前述の第1の実施形態と同様な方法により、空洞33内にシリコン酸化物22を埋め込む。そして、CMPを行って積層体14の上面からシリコン酸化物層30bを除去し、チャンネルシリコン結晶膜30の上面を露出させる。これにより、シリコン基板11上にメモリアレイ部が形成される。その後、選択ゲートトランジスタ、配線層及び周辺素子(いずれも図示せず)等を形成し、3次元積層構造の不揮発性半導体製造装置を製造する。

【0041】

図14(a)及び(b)に示すように、本実施形態において製造される不揮発性半導体記憶装置においては、シリコン基板11上に、それぞれ複数の層間絶縁膜(シリコン酸化膜12)及びゲート電極(シリコン膜13)が交互に積層された積層体14が設けられており、積層体14には円柱形のトレンチ25が形成されている。トレンチ25の側面上には、電荷ブロック膜(アルミナ膜16)、電荷蓄積膜(シリコン窒化膜17)、トンネル絶縁膜(シリコン酸化膜18)がこの順に設けられており、トレンチ25の内部には、底部が閉じた円筒形のチャンネルシリコン結晶膜30が設けられており、シリコン基板11に接続されている。チャンネルシリコン結晶膜30の内部は上部が開いた空洞33となっており、その内部にはシリコン酸化物22が埋め込まれている。そして、トンネル絶縁膜(シ

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リコン酸化膜 18) とチャネル膜 (チャネルシリコン結晶膜 30) との界面にはシリコン酸化物層 31a が形成されており、素子分離絶縁膜 (シリコン酸化物 22) とチャネル膜 (チャネルシリコン結晶膜 30) との界面にはシリコン酸化物層 31b が形成されている。

【0042】

次に、本実施形態の作用効果について説明する。

本実施形態によれば、メモリセルトランジスタのチャネルがシリコン基板 11 に接続された 3 次元積層型の不揮発性半導体記憶装置を製造することができる。

また、本実施形態においては、前述の第 1 の実施形態と比較して、熱酸化処理条件が同じであれば、シリコン酸化物層 31a の厚さに対するシリコン酸化物層 31b の厚さの比を小さくすることができる。例えば、前述の第 1 の実施形態においては、この比は 1.5 ~ 3 であるが、本実施形態においては、1 ~ 2 とすることができる。これは、チャネルシリコン結晶膜 30 の形状が円筒形であり、シリコン酸化膜 18 と接する外側面は凸型の曲面であり、熱酸化処理時に露出面である内側面は凹型の曲面であるため、酸化反応の進行に伴って発生する応力が、外側面よりも内側面の方が大きいためであると考えられる。これにより、シリコン酸化物層 31b が厚くなることを抑制し、熱酸化処理後のチャネルシリコン結晶膜 30 の厚さを確保して、所望のチャネル電流を得ることが可能となる。また、所望の厚さのシリコン酸化物層 31a を形成するための熱酸化処理温度を低くできるため、元素の熱拡散を抑制することができる。この結果、メモリアレイ部の構造を高精度化することができ、メモリ誤動作が少ない不揮発性半導体記憶装置を製造することができる。

【0043】

本実施形態における上記以外の作用効果は、前述の第 1 の実施形態と同様である。すなわち、本実施形態においても、トンネル絶縁膜 (シリコン酸化膜 18) とチャネル膜 (チャネルシリコン結晶膜 30) との界面にシリコン酸化物層 31a を形成することにより、この界面の界面準位及び固定電荷を低減し、セルトランジスタが高速でしきい値変動が少ない不揮発性半導体記憶装置を製造することができる。本実施形態においても、前述の第 1 の実施形態と同様に、酸素ガス雰囲気中の熱処理により、界面準位及び固定電荷の密度を、例えば $1 \times 10^{12} \text{ cm}^{-2}$ 以上から $1 \times 10^{11} \text{ cm}^{-2}$ 以下まで低減することができる。

【0044】

なお、本実施形態においては、前述の第 1 の実施形態と同様に、酸素ガス雰囲気中で熱処理を行ってチャネルシリコン結晶膜 30 の表面を酸化する例を示したが、前述の第 2 の実施形態と同様に、一酸化窒素ガス雰囲気中で熱処理を行ってチャネルシリコン結晶膜 30 の表面を酸窒化してもよい。これにより、前述の第 2 の実施形態と同様な作用効果を得ることができる。

【0045】

次に、本発明の第 4 の実施形態について説明する。

図 15 (a) 及び (b) 並びに図 16 (a) 及び (b) は、本実施形態に係る不揮発性半導体記憶装置の製造方法を例示する図であり、各図の (a) は工程断面図であり、各図の (b) は工程平面図であり、

図 17 は、本実施形態に係る不揮発性半導体記憶装置を例示する斜視図である。

なお、図 17 においては、図示の便宜上、シリコン基板 11 及びシリコン酸化膜 12 は図示を省略している。

【0046】

本実施形態は、前述の第 3 の実施形態と比較して、円筒形のチャネルシリコン結晶膜 30 の内部に、シリコン酸化物 22 (図 14 参照) ではなく多結晶シリコンを埋め込む点が異なっている。

【0047】

先ず、前述の第 3 の実施形態と同様な方法により、図 13 (a) 及び (b) に示す構造

体を作製する。そして、図15(a)及び(b)に示すように、希フッ酸溶液を用いてウェットエッチングを行い、チャンネルシリコン結晶膜30の露出面に形成されたシリコン酸化物層31bを除去する。なお、一酸化窒素ガスを含む雰囲気中で熱酸化処理を行い、チャンネルシリコン結晶膜30の露出面にシリコン酸化物層を形成した場合は、リン酸溶液を用いたウェットエッチングにより、このシリコン酸化物層を除去する。これにより、空洞33の内面において、チャンネルシリコン結晶膜30が露出する。

【0048】

次に、図16(a)及び(b)に示すように、全面に不純物をドーピングした非晶質シリコンを堆積させて、空洞33の内部に埋め込む。その後、CMPを行い、積層体14上に堆積された非晶質シリコンを除去し、チャンネルシリコン結晶膜30の上面を露出させる。次に、例えば500℃以上の温度で熱アニールを施し、非晶質シリコンを結晶化させ、多結晶シリコン32とする。その後、選択ゲートトランジスタ、配線層及び周辺素子(いずれも図示せず)等を形成し、3次元積層構造の不揮発性半導体製造装置を製造する。

【0049】

図16(a)及び(b)並びに図17に示すように、本実施形態に係る不揮発性半導体記憶装置においては、トレンチ25の側面上に形成された円筒形のチャンネルシリコン結晶膜30と、その内部に埋め込まれた多結晶シリコン32とにより、シリコン基板11に接続され、垂直方向に伸びるシリコンピラーが構成される。そして、このシリコンピラーがセルトランジスタのチャンネルとして機能する。

【0050】

次に、本実施形態の作用効果について説明する。

本実施形態においては、前述の第3の実施形態と比較して、チャンネルとなるシリコンピラーの断面積が大きくなるため、大きなセル電流を流すことができる。この結果、セルトランジスタの動作速度が大きく向上する。本実施形態における上記以外の作用効果は、前述の第3の実施形態と同様である。

【0051】

次に、第4の実施形態の比較例について説明する。

図18は、本比較例に係る不揮発性半導体記憶装置を例示する断面図である。

図18に示すように、本比較例においても、前述の第4の実施形態と同様に、積層体14にトレンチ25を形成し、トレンチ25の内面上に、アルミナ膜16、シリコン窒化膜17及びシリコン酸化膜18をこの順に成膜する。次に、シリコン酸化膜18上にCVDにより非晶質シリコン膜を形成し、結晶化させて、円柱状のチャンネルシリコン結晶膜40とする。但し、本比較例においては、非晶質シリコン膜の形成後、酸素ガス雰囲気中又は一酸化窒素ガス雰囲気中における熱処理は行わず、従って、シリコン酸化膜18とチャンネルシリコン結晶膜40との界面に、シリコン酸化物層又はシリコン酸窒化物層が形成されない。

【0052】

本比較例においては、シリコン酸化膜18上に非晶質シリコン膜を堆積させたときに導入された欠陥が最後まで残り、シリコン酸化膜18とチャンネルシリコン結晶膜40との界面に界面準位及び固定電荷が発生する。この結果、セルトランジスタの動作速度が遅くなり、また、長期間の使用によるしきい値変動が顕著となって、メモリセルに誤動作が生じる。これに対して、前述の第1乃至第4の実施形態によれば、酸素ガス雰囲気中又は一酸化窒素ガス雰囲気中において熱処理を行い、トンネル絶縁膜を構成するシリコン酸化膜とチャンネル膜を構成するチャンネルシリコン結晶膜との界面にシリコン酸化物層又はシリコン酸窒化物層を形成しているため、この界面における界面準位及び固定電荷を減らすことができる。

【0053】

以上、実施形態を参照して本発明を説明したが、本発明はこれらの実施形態に限定されるものではない。例えば、前述の各実施形態に対して、当業者が適宜、構成要素の追加、削除若しくは設計変更を行ったもの、又は、工程の追加、省略若しくは条件変更を行った

ものも、本発明の要旨を備えている限り、本発明の範囲に含有される。

【図面の簡単な説明】

【0054】

【図1】(a)は本発明の第1の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図2】(a)は第1の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図3】(a)は第1の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図4】(a)は第1の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

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【図5】(a)は第1の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図6】(a)は第1の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図7】(a)は本発明の第2の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)は(a)に示す領域Rの一部拡大図である。

【図8】(a)は第2の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)は(a)に示す領域Rの一部拡大図である。

【図9】(a)は本発明の第3の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

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【図10】(a)は第3の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図11】(a)は第3の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図12】(a)は第3の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図13】(a)は第3の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図14】(a)は第3の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

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【図15】(a)は本発明の第4の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図16】(a)は第4の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程断面図であり、(b)はその工程平面図である。

【図17】第4の実施形態に係る不揮発性半導体記憶装置を例示する斜視図である。

【図18】第4の実施形態の比較例に係る不揮発性半導体記憶装置を例示する断面図である。

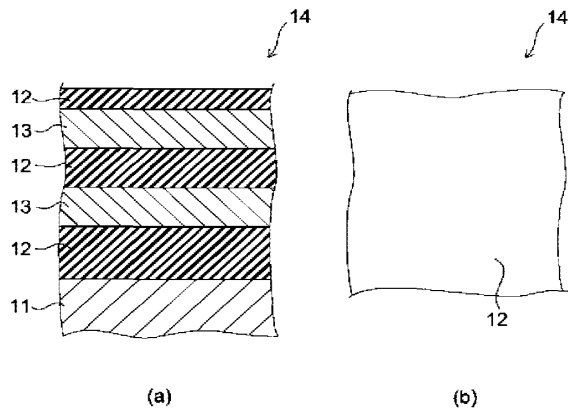
【符号の説明】

【0055】

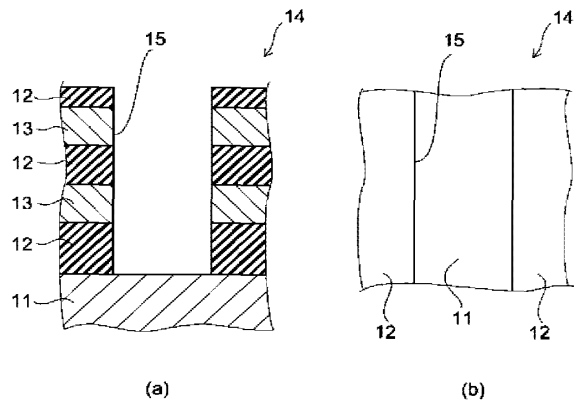
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11 シリコン基板、12 シリコン酸化膜、13 シリコン膜、14 積層体、15 トレンチ、16 アルミナ膜、17 シリコン窒化膜、18 シリコン酸化膜、19 多結晶シリコン膜、20 チャネルシリコン結晶膜、21a、21b シリコン酸化物層、22 シリコン酸化物、23 空洞、24a、24b シリコン酸窒化物層、24N 窒素リッチ層、24O 酸素リッチ層、25 トレンチ、30 チャネルシリコン結晶膜、31a、31b シリコン酸化物層、32 多結晶シリコン、33 空洞、40 チャネルシリコン結晶膜、R 領域

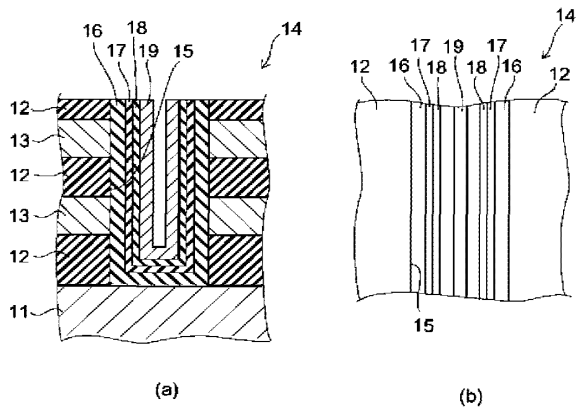
【図 1】



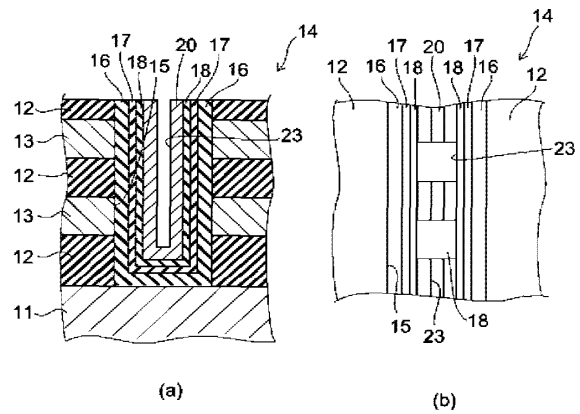
【図 2】



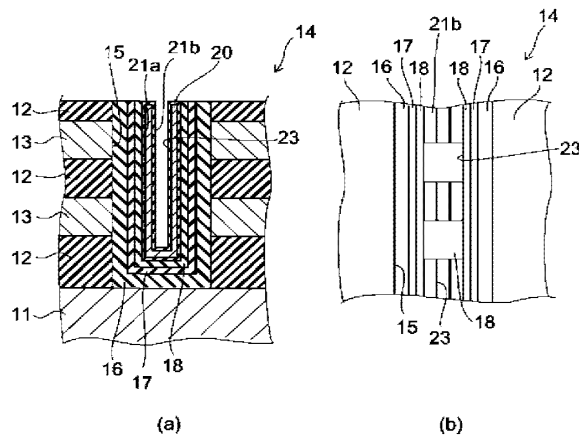
【図 3】



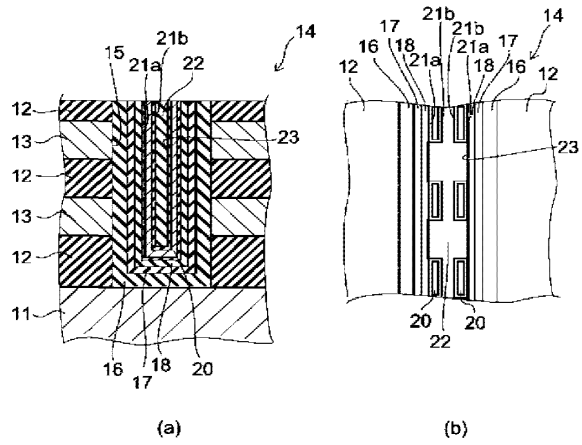
【図 4】



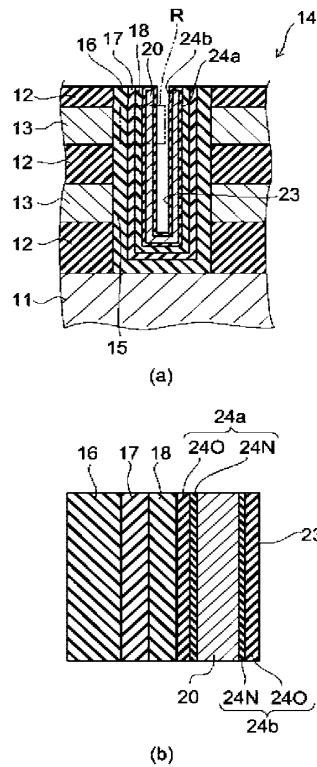
【図 5】



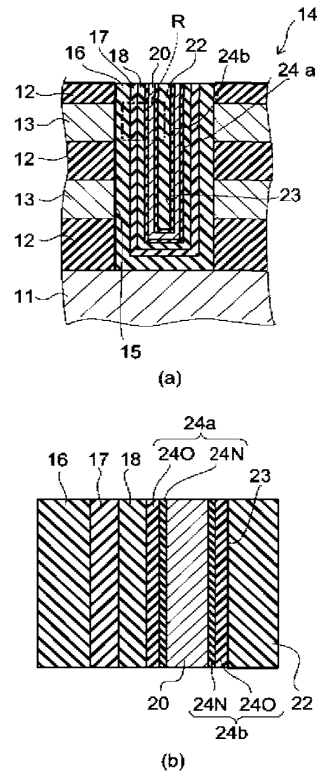
【図 6】



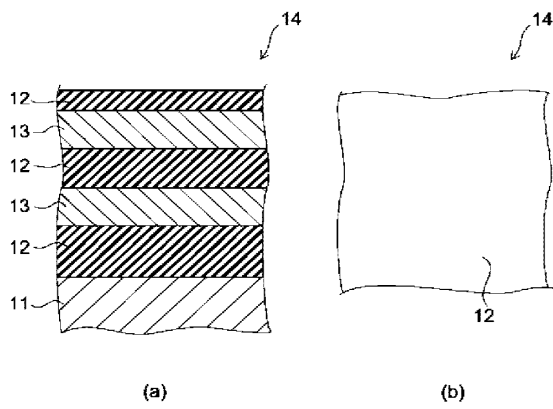
【図 7】



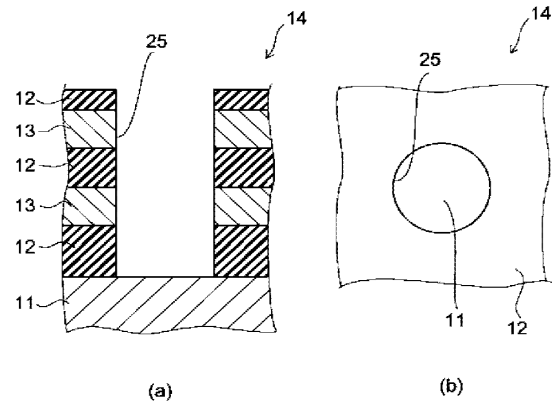
【図 8】



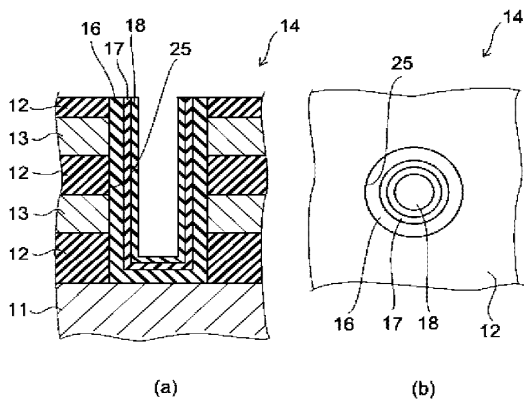
【図 9】



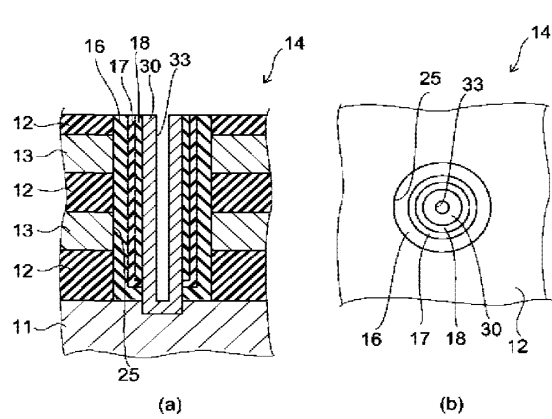
【図 10】



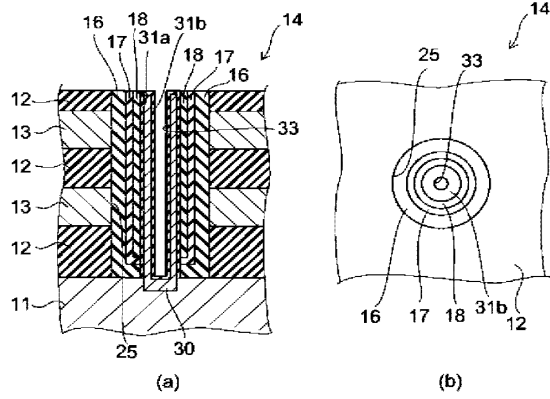
【図 11】



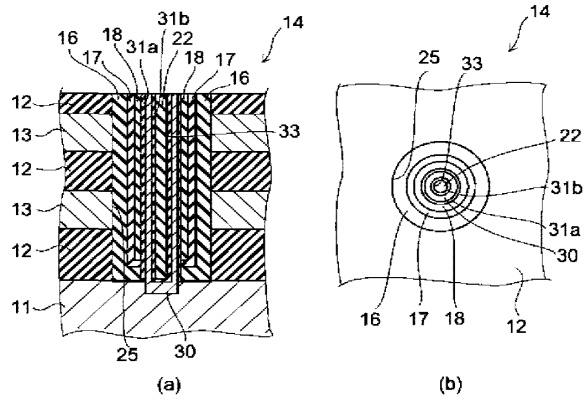
【図 12】



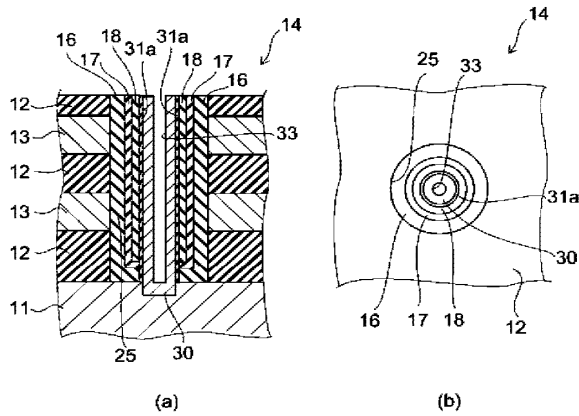
【図 1 3】



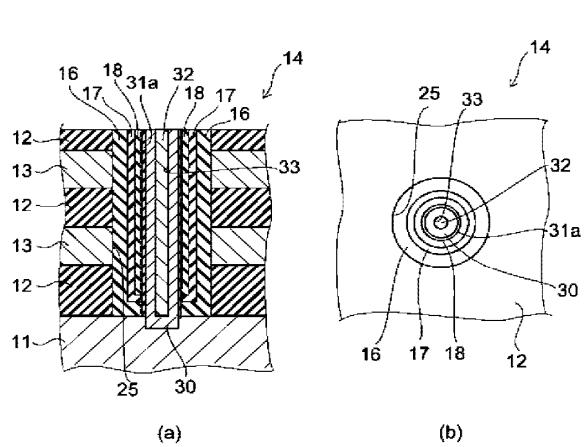
【図 1 4】



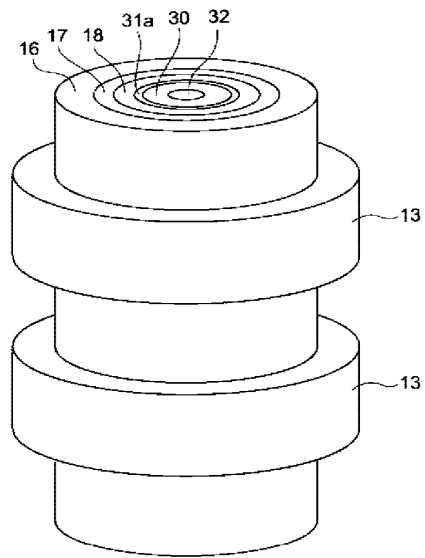
【図 1 5】



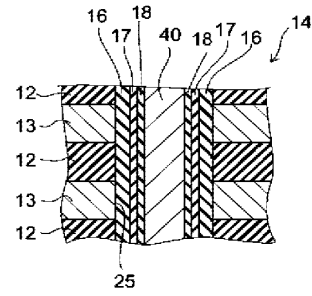
【図 1 6】



【図 17】



【図 18】





Espacenet

JP2011035228A NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND METHOD FOR MANUFACTURING THE SAME

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NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND METHOD FOR MANUFACTURING THE SAME

Abstract

PROBLEM TO BE SOLVED: To provide a nonvolatile semiconductor storage device, reducing the resistance of a selection gate electrode and having high response characteristic in a selection gate transistor for selecting a semiconductor pillar, and also to provide a method for manufacturing the device. **SOLUTION:** The nonvolatile semiconductor storage device is equipped with: a lamination structure ML including a plurality of electrode films WL and a plurality of interelectrode insulating films 14 which are alternately laminated in a first direction; a selection gate electrode SG laminated on the lamination structure ML in the first direction; a semiconductor pillar SP pierced into the lamination structure ML and the selection gate electrode SG in the first direction; a storage part formed on an intersection part between respective electrode films WL and the semiconductor pillar SP; and a selection gate insulating film SGI formed between the semiconductor pillar SP and the selection gate electrode SG. The selection gate electrode SG has a first silicide layer 51 formed on the surface of the selection gate electrode SG, the surface which is vertical to the first direction of the selection gate. **COPYRIGHT: (C)2011,JPO&INPIT**

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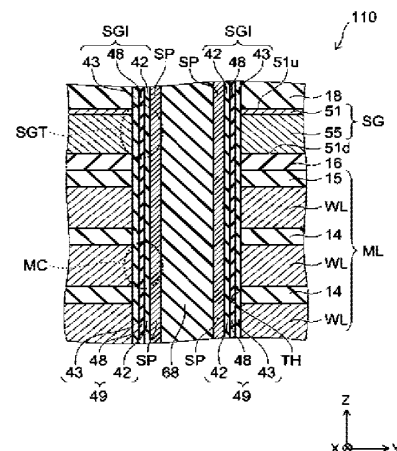
(54) 【発明の名称】 不揮発性半導体記憶装置及びその製造方法

(57) 【要約】

【課題】選択ゲート電極を低抵抗化し、半導体ピラーを選択する選択ゲートトランジスタの応答特性が良好な不揮発性半導体記憶装置及びその製造方法を提供する。

【解決手段】第1方向に交互に積層された複数の電極膜WLと複数の電極間絶縁膜14とを有する積層構造体MLと、前記第1方向において積層構造体MLに積層された選択ゲート電極SGと、積層構造体MLと選択ゲート電極SGとを前記第1方向に貫通する半導体ピラーSPと、電極膜WLのそれぞれと半導体ピラーSPとの交差部に設けられた記憶部と、半導体ピラーSPと選択ゲート電極SGとの間に設けられた選択ゲート絶縁膜SGIと、を備えた不揮発性半導体記憶装置が提供される。選択ゲート電極SGは、選択ゲート電極SGの前記第1方向に対して垂直な面上に設けられた第1シリサイド層51を有する。

【選択図】 図 1



【特許請求の範囲】

【請求項 1】

第 1 方向に交互に積層された複数の電極膜と複数の電極間絶縁膜とを有する積層構造体と、

前記第 1 方向において前記積層構造体に積層された選択ゲート電極と、
前記積層構造体と前記選択ゲート電極とを前記第 1 方向に貫通する半導体ピラーと、
前記電極膜のそれぞれと前記半導体ピラーとの交差部に設けられた記憶部と、
前記半導体ピラーと前記選択ゲート電極との間に設けられた選択ゲート絶縁膜と、
を備え、

前記選択ゲート電極は、前記選択ゲート電極の前記第 1 方向に対して垂直な面上に設けられた第 1 シリサイド層を有することを特徴とする不揮発性半導体記憶装置。

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【請求項 2】

前記選択ゲート電極は、前記第 1 シリサイド層に前記第 1 方向で積層されたシリコン層をさらに有することを特徴とする請求項 1 記載の不揮発性半導体記憶装置。

【請求項 3】

前記選択ゲート電極は、前記選択ゲート電極の前記第 1 方向に対して平行な面上に設けられた第 2 シリサイド層をさらに有することを特徴とする請求項 1 または 2 に記載の不揮発性半導体記憶装置。

【請求項 4】

基板をさらに備え、

前記積層構造体及び前記選択ゲート電極は、前記基板の上に設けられ、

前記第 1 方向に対して垂直な前記面は、前記選択ゲート電極の上側の面であることを特徴とする請求項 1～3 のいずれか 1 つに記載の不揮発性半導体記憶装置。

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【請求項 5】

第 1 方向に交互に積層された複数の電極膜と複数の電極間絶縁膜とを有する積層構造体と、

前記第 1 方向において前記積層構造体に積層された選択ゲート電極と、
前記積層構造体と前記選択ゲート電極とを前記第 1 方向に貫通する半導体ピラーと、
前記電極膜のそれぞれと前記半導体ピラーとの交差部に設けられた記憶部と、
前記半導体ピラーと前記選択ゲート電極との間に設けられた選択ゲート絶縁膜と、
を有する不揮発性半導体記憶装置の製造方法であって、

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前記積層構造体と、前記選択ゲート電極の少なくとも一部となる選択ゲート電極膜と、
を前記第 1 方向に積層し、

前記選択ゲート電極膜の前記第 1 方向に対して垂直な面をシリサイド化することを特徴とする不揮発性半導体記憶装置の製造方法。

【発明の詳細な説明】

【技術分野】

【0001】

本発明は、不揮発性半導体記憶装置及びその製造方法に関する。

【背景技術】

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【0002】

不揮発性半導体記憶装置（メモリ）の記憶容量の増加のために、一括加工型 3 次元積層メモリが提案されている（例えば、特許文献 1 参照）。この方法によれば積層数によらず、積層メモリを一括して形成することが可能なため、コストの増加を抑えることが可能となる。

【0003】

この一括加工型 3 次元積層メモリにおいては、絶縁膜と、ワード線となる電極膜と、を交互に積層させて積層構造体を形成し、この積層構造体に貫通ホールを一括して形成する。そして、貫通ホールの側面に電荷蓄積層（記憶層）を形成し、貫通ホールの内部に半導体を埋め込み、半導体ピラーを形成する。これにより、各電極膜と半導体ピラーとの交差

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部分にメモリセルが形成され、半導体ピラーに沿ってメモリストリングが形成される。

【0004】

そして、メモリストリングとなる半導体ピラーを選択するために、電極膜と平行に選択ゲート電極が設けられ、この選択ゲート電極と半導体ピラーとにより選択ゲートトランジスタが形成される。選択ゲートトランジスタの応答特性を向上させるために、選択ゲート電極の低抵抗化が望まれている。

【先行技術文献】

【特許文献】

【0005】

【特許文献1】特開2007-266143号公報

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【発明の概要】

【発明が解決しようとする課題】

【0006】

本発明は、選択ゲート電極を低抵抗化し、半導体ピラーを選択する選択ゲートトランジスタの応答特性が良好な不揮発性半導体記憶装置及びその製造方法を提供する。

【課題を解決するための手段】

【0007】

本発明の一態様によれば、第1方向に交互に積層された複数の電極膜と複数の電極間絶縁膜とを有する積層構造体と、前記第1方向において前記積層構造体に積層された選択ゲート電極と、前記積層構造体と前記選択ゲート電極とを前記第1方向に貫通する半導体ピラーと、前記電極膜のそれぞれと前記半導体ピラーとの交差部に設けられた記憶部と、前記半導体ピラーと前記選択ゲート電極との間に設けられた選択ゲート絶縁膜と、を備え、前記選択ゲート電極は、前記選択ゲート電極の前記第1方向に対して垂直な面上に設けられた第1シリサイド層を有することを特徴とする不揮発性半導体記憶装置が提供される。

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【0008】

本発明の他の一態様によれば、第1方向に交互に積層された複数の電極膜と複数の電極間絶縁膜とを有する積層構造体と、前記第1方向において前記積層構造体に積層された選択ゲート電極と、前記積層構造体と前記選択ゲート電極とを前記第1方向に貫通する半導体ピラーと、前記電極膜のそれぞれと前記半導体ピラーとの交差部に設けられた記憶部と、前記半導体ピラーと前記選択ゲート電極との間に設けられた選択ゲート絶縁膜と、を有する不揮発性半導体記憶装置の製造方法であって、前記積層構造体と、前記選択ゲート電極の少なくとも一部となる選択ゲート電極膜と、を前記第1方向に積層し、前記選択ゲート電極膜の前記第1方向に対して垂直な面をシリサイド化することを特徴とする不揮発性半導体記憶装置の製造方法が提供される。

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【発明の効果】

【0009】

本発明によれば、選択ゲート電極を低抵抗化し、半導体ピラーを選択する選択ゲートトランジスタの応答特性が良好な不揮発性半導体記憶装置及びその製造方法が提供される。

【図面の簡単な説明】

【0010】

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【図1】第1の実施形態に係る不揮発性半導体記憶装置の構成を例示する模式的断面図である。

【図2】第1の実施形態に係る不揮発性半導体記憶装置の全体構成を例示する模式的断面図である。

【図3】第1の実施形態に係る不揮発性半導体記憶装置の全体構成を例示する模式的斜視図である。

【図4】第1の実施形態に係る不揮発性半導体記憶装置の電極膜の構成を例示する模式的平面図である。

【図5】第1の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

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【図 6】第 1 の実施形態に係る別の不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

【図 7】第 1 の実施形態に係る別の不揮発性半導体記憶装置の構成を例示する模式的断面図である。

【図 8】第 1 の実施形態に係る別の不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

【図 9】第 1 の実施形態に係る別の不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

【図 10】第 1 の実施形態に係る別の不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

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【図 11】第 1 の実施形態に係る別の不揮発性半導体記憶装置の構成を例示する模式的断面図である。

【図 12】第 1 の実施形態に係る別の不揮発性半導体記憶装置の構成を例示する模式的断面図である。

【図 13】第 1 の実施形態に係る別の不揮発性半導体記憶装置の構成を例示する模式的断面図である。

【図 14】第 1 の実施形態に係る別の不揮発性半導体記憶装置の構成を例示する模式的斜視図である。

【図 15】第 2 の実施形態に係る不揮発性半導体記憶装置の製造方法を例示するフローチャート図である。

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【発明を実施するための形態】

【0011】

以下に、本発明の各実施の形態について図面を参照しつつ説明する。

なお、図面は模式的または概念的なものであり、各部分の厚みと幅との関係、部分間の大きさの比係数などは、必ずしも現実のものと同じとは限らない。また、同じ部分を表す場合であっても、図面により互いの寸法や比係数が異なって表される場合もある。

また、本願明細書と各図において、既出の図に関して前述したものと同様の要素には同一の符号を付して詳細な説明は適宜省略する。

【0012】

(第 1 の実施の形態)

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図 1 は、第 1 の実施形態に係る不揮発性半導体記憶装置の構成を例示する模式的断面図である。

図 2 及び図 3 は、第 1 の実施形態に係る不揮発性半導体記憶装置の全体構成を例示する、それぞれ、模式的断面図及び模式的斜視図である。

なお、図 3 においては、図を見易くするために、導電部分のみを示し、絶縁部分は図示を省略している。

図 4 は、第 1 の実施形態に係る不揮発性半導体記憶装置の電極膜の構成を例示する模式的平面図である。

本実施形態に係る不揮発性半導体記憶装置 110 は、一括加工型 3 次元積層フラッシュメモリである。不揮発性半導体記憶装置 110 は、U 字形状のメモリストリングを有する例である。

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まず、図 2 及び図 3 により、不揮発性半導体記憶装置 110 の構成の概要を説明する。

【0013】

図 2 に表したように、不揮発性半導体記憶装置 110 においては、例えば、メモリ部 MU と制御部 C T U とが設けられる。これらメモリ部 MU 及び制御部 C T U は、例えば単結晶シリコンからなる基板 11 の主面 11 a の上に設けられる。

【0014】

基板 11 においては、例えば、メモリセルが設けられるメモリアレイ領域 MR と、メモリアレイ領域 MR の例えば周辺に設けられた周辺領域 PR と、が設定される。周辺領域 PR においては、基板 11 の上に、各種の周辺領域回路 P R 1 が設けられる。

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【0015】

メモリアレイ領域MRにおいては、基板11の上に例えば回路部CUが設けられ、回路部CUの上にメモリ部MUが設けられる。なお、回路部CUは必要に応じて設けられ、省略可能である。回路部CUとメモリ部MUとの間には、例えば酸化シリコンからなる層間絶縁膜13が設けられる。

【0016】

例えば、制御部CTUの少なくとも一部は、例えば、上記の周辺領域回路PR1及び回路部CUの少なくともいずれかに設けることができる。

【0017】

メモリ部MUは、複数のメモリセルトランジスタを有するマトリクスメモリセル部MU1と、マトリクスメモリセル部MU1の配線を接続する配線接続部MU2と、を有する。

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【0018】

図3は、マトリクスメモリセル部MU1の構成を例示している。

すなわち、図2においては、マトリクスメモリセル部MU1として、図3のA-A'断面と、図3のB-B'線断面と、に相当する部分が例示されている。

【0019】

図2及び図3に表したように、マトリクスメモリセル部MU1においては、基板11の主面11a上に、積層構造体MLが設けられる。積層構造体MLは、主面11aに対して垂直な方向に交互に積層された複数の電極膜WLと複数の電極間絶縁膜14とを有する。

【0020】

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ここで、基板11の主面11aに対して垂直な方向をZ軸方向（第1方向）とする。そして、主面11aに対して平行な平面内の1つの方向をY軸方向（第2方向）とする。そして、Z軸方向とY軸方向とに垂直な方向をX軸方向（第3方向）とする。

【0021】

積層構造体MLにおける電極膜WL及び電極間絶縁膜14の積層方向は、Z軸方向である。電極膜WLは、例えば、消去ブロック単位で分断される。

【0022】

図1は、マトリクスメモリセル部MU1の構成を例示しており、例えば図3のB-B'線断面の一部に相当する。

図1に表したように、不揮発性半導体記憶装置110のメモリ部MUは、第1方向（Z軸方向）に交互に積層された複数の電極膜WLと複数の電極間絶縁膜14とを有する積層構造体MLと、Z軸方向において積層構造体MLに積層された選択ゲート電極SGと、積層構造体MLと選択ゲート電極SGとをZ軸方向に貫通する半導体ピラーSP（第1半導体ピラーSP1）と、電極膜WLのそれぞれと半導体ピラーSPとの交差部に設けられた記憶部（メモリセルMC）と、半導体ピラーSPと選択ゲート電極SGとの間に設けられた選択ゲート絶縁膜SGI（第1選択ゲート絶縁膜）と、を有する。

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【0023】

本具体例では、記憶部（メモリセルMC）は、例えば、電極膜WLのそれぞれと半導体ピラーSP（第1半導体ピラーSP1）との間に設けられた記憶層48（第1記憶層）と、記憶層48（第1記憶層）と半導体ピラーSPとの間に設けられた内側絶縁膜42（第1内側絶縁膜）と、電極膜WLのそれぞれと記憶層48（第1記憶層）との間に設けられた外側絶縁膜43（第1外側絶縁膜）と、を含む。

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【0024】

そして、本具体例では、半導体ピラーSPはZ軸方向に延在する管状の形状を有し、半導体ピラーSPの内側には、絶縁性の芯材部68が設けられている。

【0025】

すなわち、積層構造体ML及び選択ゲート電極SGをZ軸方向に貫通する貫通ホールTHの内側の壁面に、外側絶縁膜43、記憶層48、内側絶縁膜42、及び、半導体ピラーSPとなる膜、がこの順番で形成され、その残余の空間に絶縁性の芯材部68が埋め込まれている。

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【0026】

ただし、本発明はこれに限らず、後述するように、芯材部68が設けられず、貫通ホールTHの内側の外側絶縁膜43、記憶層48及び内側絶縁膜42の内側に、柱状の半導ピラーSPが形成される構成であっても良い。以下では、芯材部68が設けられる場合として説明する。

【0027】

積層構造体MLの電極膜WLと、半導体ピラーSPと、の交差部に、記憶層48を有するメモリトランジスタを含むメモリセルMCが3次元マトリクス状に設けられ、この記憶層48に電荷を蓄積させることにより、各メモリセルトランジスタがデータを記憶する。

【0028】

電極膜WLは、このメモリセルトランジスタのゲート電極として機能する。電極膜WLには所定の電気信号が印加され、電極膜WLは、不揮発性半導体記憶装置110のワード線となる。

【0029】

内側絶縁膜42は、メモリセルトランジスタにおけるトンネル絶縁膜として機能する。一方、外側絶縁膜43は、メモリセルトランジスタにおけるブロック絶縁膜として機能する。電極間絶縁膜14は、電極膜WLどうしを絶縁する層間絶縁膜として機能する。

【0030】

一方、選択ゲート電極SGと半導体ピラーSPとが交差する部分において、半導体ピラーSPを選択するための選択ゲートトランジスタSGTが形成される。選択ゲート電極SG、選択ゲート絶縁膜SGI及び半導体ピラーSPは、この選択ゲートトランジスタSGTの、それぞれ、ゲート電極、ゲート絶縁膜及びチャネル層として機能する。

【0031】

電極膜WLには、任意の導電材料を用いることができる。本具体例では、不純物が導入されて導電性が付与されたアモルファスシリコンまたはポリシリコンが用いられる。すなわち、半導体ピラーSPと交差する部分に形成されるメモリセルトランジスタのしきい値特性が所望の値に設定され易いように、電極膜WLには、アモルファスシリコンまたはポリシリコンが用いられることが望ましい。

【0032】

選択ゲート電極SGの材料及びその構成に関しては後述する。

【0033】

電極間絶縁膜14、内側絶縁膜42、外側絶縁膜43及び選択ゲート絶縁膜SGIには、例えばシリコン酸化膜を用いることができる。なお、電極間絶縁膜14、内側絶縁膜42、外側絶縁膜43及び選択ゲート絶縁膜SGIは、単層膜でも良く、また積層膜でも良い。

【0034】

記憶層48には、例えばシリコン窒化膜を用いることができ、半導体ピラーSPと電極膜WLとの間に印加される電界によって、電荷を蓄積または放出し、情報を記憶する部分として機能する。記憶層48は、単層膜でも良く、また積層膜でも良い。

【0035】

芯材部68には、例えばシリコン窒化膜を用いることができる。

【0036】

なお、後述するように電極間絶縁膜14、内側絶縁膜42、記憶層48、外側絶縁膜43、選択ゲート絶縁膜SGI及び芯材部68には、上記に例示した材料に限らず、任意の材料を用いることができる。

【0037】

なお、図2及び図3においては、積層構造体MLが電極膜WLを4層有している場合が例示されているが、積層構造体MLにおいて、設けられる電極膜WLの数は任意である。以下では、電極膜WLが4枚である場合として説明する。

【0038】

本具体例においては、2本の半導体ピラーSPは接続部CPによって接続されている。

すなわち、不揮発性半導体記憶装置110のメモリ部MUは、第2半導体ピラーSP2と、第1接続部CP1（接続部CP）と、をさらに有する。第2半導体ピラーSP2は、半導体ピラーSPに含まれる。

第2半導体ピラーSP2は、例えばY軸方向において第1半導体ピラーSP1と隣接し、積層構造体ML及び選択ゲート電極SGをZ軸方向に貫通する。

記憶層48は、電極膜WLのそれぞれと第2半導体ピラーSP2との間にも設けられる。内側絶縁膜42は、第2半導体ピラーSP2と記憶層48との間にも設けられる。外側絶縁膜43は、電極膜WLと、第2半導体ピラーにおける記憶層48と、の間にも設けられる。

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【0039】

第1接続部CP1は、第1半導体ピラーSP1と第2半導体ピラーSP2とをZ軸方向における同じ側（この例では基板11の側）で電氣的に接続する。第1接続部CP1は、Y軸方向に延在して設けられる。第1接続部CP1には、第1及び第2半導体ピラーSP1及びSP2と同じ材料が用いられる。

【0040】

すなわち、基板11の主面11aの上に、層間絶縁膜13を介してバックゲートBG（接続部導電層）が設けられる。そして、バックゲートBGの第1及び第2半導体ピラーSP1及びSP2に対向する部分に溝が設けられ、溝の内部に、外側絶縁膜43、記憶層48及び内側絶縁膜42が形成され、その内側に接続部CPとなる半導体の膜が形成され、残余の空間に接続部芯材部68CPが埋め込まれる。なお、溝における外側絶縁膜43、記憶層48、内側絶縁膜42、接続部CP及び接続部芯材部68CPの形成は、貫通ホールTHにおける外側絶縁膜43、記憶層48、内側絶縁膜42、半導体ピラーSP及び芯材部68の形成と同時に、一括して行われる。このように、バックゲートBGは、接続部CPに対向して設けられる。

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【0041】

これにより、第1及び第2半導体ピラーSP1及びSP2と、接続部CPと、によって、U字形状の半導体ピラーが形成され、これが、U字形状のNANDストリングとなる。

【0042】

図2及び図3に表したように、第1半導体ピラーSP1の第1接続部CP1とは反対の端は、ビット線BLに接続され、第2半導体ピラーSP2の第1接続部CP1とは反対の端は、ソース線SLに接続されている。なお、半導体ピラーSPとビット線BLとはビアV1及びビアV2により接続される。

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【0043】

本具体例では、ビット線BLは、Y軸方向に延在し、ソース線SLは、X軸方向に延在する。

【0044】

そして、積層構造体MLとビット線BLとの間において、第1半導体ピラーSP1に対向して、ドレイン側選択ゲート電極SGD（第1選択ゲート電極SG1）が設けられ、第2半導体ピラーSP2に対向して、ソース側選択ゲート電極SGS（第2選択ゲート電極SG2）が設けられる。これにより、任意の半導体ピラーSPの任意のメモリセルMCに所望のデータを書き込み、また読み出すことができる。なお、上記の第1選択ゲート電極SG3及び第2選択ゲート電極SG4は、選択ゲート電極SGに含まれる。

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【0045】

本具体例では選択ゲート電極SGは、Y軸方向に分断され、X軸方向に沿って延在する帯状の形状を有している。

【0046】

なお、図2に表したように、積層構造体MLの最上部（基板11から最も遠い側）には、層間絶縁膜15が設けられている。そして、積層構造体MLの上に層間絶縁膜16が設けられ、その上に選択ゲート電極SGが設けられ、選択ゲート電極SGどうしの間には層

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間絶縁膜 17 が設けられている。なお、層間絶縁膜 15 が省略され、積層構造体 M L の一番上が、電極間絶縁膜 14 または電極膜 W L であり、そのような積層構造体 M L の上に層間絶縁膜 16 が設けられていても良い。さらに、場合によっては、層間絶縁膜 15 及び層間絶縁膜 16 が省略され、積層構造体 M L の一番上が電極間絶縁膜 14 であり、その上に選択ゲート電極 S G が設けられていても良い。また、層間絶縁膜 16 が省略され、積層構造体 M L の電極間絶縁膜 14 または層間絶縁膜 15 の上に選択ゲート電極 S G が設けられていても良い。以下では、層間絶縁膜 15 及び層間絶縁膜 16 が設けられる場合として説明する。

【0047】

そして、層間絶縁膜 17 の上に層間絶縁膜 18 が設けられ、その上に、ソース線 S L とビア 22 (ビア V 1、V 2) が設けられ、ソース線 S L の周りには層間絶縁膜 19 が設けられている。そして、ソース線 S L の上に層間絶縁膜 23 が設けられ、その上にビット線 B L が設けられている。ビット線 B L は、Y 軸に沿った帯状の形状を有している。

なお、層間絶縁膜 15、16、17、18、19 及び 23 には、例えば酸化シリコンを用いることができる。

【0048】

なお、ここで、不揮発性半導体記憶装置 110 において複数設けられる半導体ピラーに関し、半導体ピラーの全体または任意の半導体ピラーを指す場合には、「半導体ピラー S P」と言い、半導体ピラーどうしの関係を説明する際などにおいて、特定の半導体ピラーを指す場合に、「第 n 半導体ピラー S P n」(n は 1 以上の任意の整数)とすることにす

【0049】

図 4 に表したように、電極膜 W L においては、0 以上の整数である m において、n が ($4m+1$) 及び ($4m+4$) である半導体ピラー S P ($4m+1$) 及び S P ($4m+4$) に対応する電極膜が共通に接続され電極膜 W L A となり、n が ($4m+2$) 及び ($4m+3$) である半導体ピラー S P ($4m+2$) 及び ($4m+3$) に対応する電極膜が共通に接続され電極膜 W L B となる。すなわち、電極膜 W L は、X 軸方向に対向して櫛歯状に互いに組み合わされた電極膜 W L A 及び電極膜 W L B の形状を有している。

【0050】

図 4 に表したように、電極膜 W L は、絶縁層 I L によって分断され、電極膜 W L は、第 1 領域 (電極膜 W L A) 及び第 2 領域 (電極膜 W L B) に分かれている。

【0051】

そして、図 2 に例示した配線接続部 M U 2 のように、X 軸方向における一方の端において、電極膜 W L B は、ビアプラグ 31 によってワード配線 32 に接続され、例えば基板 11 に設けられる駆動回路と電氣的に接続される。そして、同様に、X 軸方向における他方の端において、電極膜 W L A は、ビアプラグによってワード配線に接続され、駆動回路と電氣的に接続される。すなわち、Z 軸方向に積層された各電極膜 W L (電極膜 W L A 及び電極膜 W L B) の X 軸方向における長さが階段状に変化させられ、X 軸方向の一方の端では電極膜 W L A によって駆動回路との電氣的接続が行われ、X 軸方向の他方の端では、電極膜 W L B によって駆動回路との電氣的接続が行われる。

【0052】

そして、図 3 に表したように、メモリ部 M U は、第 3 半導体ピラー S P 3 と、第 4 半導体ピラー S P 4 と、第 2 接続部 C P 2 と、をさらに有することができる。第 3 半導体ピラー S P 3 及び第 4 半導体ピラー S P 4 は、半導体ピラー S P に含まれ、第 2 接続部 C P 2 は、接続部 C P に含まれる。

【0053】

第 3 半導体ピラー S P 3 は、Y 軸方向において、第 2 半導体ピラー S P 2 の第 1 半導体ピラー S P 1 とは反対の側で第 2 半導体ピラー S P 2 と隣接し、積層構造体 M L 及び選択ゲート電極 S G を Z 軸方向に貫通する。第 4 半導体ピラー S P 4 は、Y 軸方向において、第 3 半導体ピラー S P 3 の第 2 半導体ピラー S P 2 とは反対の側で第 3 半導体ピラー S P

3と隣接し、積層構造体M L及び選択ゲート電極S GをZ軸方向に貫通する。

【0054】

第2接続部C P 2は、第3半導体ピラーS P 3と第4半導体ピラーS P 4とをZ軸方向における同じ側（第1接続部C P 1と同じ側）で電氣的に接続する。第2接続部C P 2は、Y軸方向に延在して設けられ、バックゲートB Gに対向している。

【0055】

記憶層4 8は、電極膜W Lのそれぞれと第3及び第4半導体ピラーS P 3及びS P 4との間、並びに、バックゲートB Gと第2接続部C P 2との間、にも設けられる。内側絶縁膜4 2は、第3及び第4半導体ピラーS P 3及びS P 4と記憶層4 8との間、並びに、記憶層4 8と第2接続部C P 2との間、にも設けられる。外側絶縁膜4 3は、電極膜W Lのそれぞれと、第3及び第4半導体ピラーS P 3及びS P 4の記憶層4 8との間、並びに、第2接続部C P 2の記憶層4 8とバックゲートB Gとの間、にも設けられる。

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【0056】

そして、ソース線S Lは、第3半導体ピラーS P 3の第2接続部C P 2とは反対の側の第3端部と接続される。そして、ビット線B Lは、第4半導体ピラーS P 4の第2接続部C P 2とは反対の側の第4端部と接続される。

【0057】

そして、第3半導体ピラーS P 3に対向して、ソース側選択ゲート電極S G S（第3選択ゲート電極S G 3）が設けられ、第4半導体ピラーS P 4に対向して、ドレイン側選択ゲート電極S G D（第4選択ゲート電極S G 4）が設けられる。ソース側選択ゲート電極S G Sと第3半導体ピラーS P 3との間、及び、ドレイン側選択ゲート電極S G Dと第4半導体ピラーS P 4との間にも、選択ゲート絶縁膜S G Iが設けられる。なお、上記の第3選択ゲート電極S G 3及び第4選択ゲート電極S G 4は、選択ゲート電極S Gに含まれる。

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【0058】

図1に表したように、このような構成を有する不揮発性半導体記憶装置1 1 0においては、選択ゲート電極S Gは、Z軸方向に対して垂直な面上に設けられた第1シリサイド層5 1を有する。ここで、このZ軸方向に対して垂直な面は、例えば、選択ゲート電極S GのZ軸方向に対して垂直な面である上面5 1 u及び下面5 1 dの少なくともいずれかとすることができる。

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【0059】

本具体例では、第1シリサイド層5 1は選択ゲート電極S Gの上面5 1 uの側に設けられている。すなわち、不揮発性半導体記憶装置1 1 0においては、基板1 1が設けられ、積層構造体M Lは、基板1 1の上に設けられ、選択ゲート電極S Gは、積層構造体M Lの基板1 1とは反対の側に設けられ、第1シリサイド層5 1は、選択ゲート電極S Gの積層構造体M Lとは反対の側の面に沿って設けられている。第1シリサイド層5 1が設けられるZ軸に対して垂直な上記の面は、選択ゲート電極S Gの上側の面（上面5 1 u）である。

【0060】

そして、本具体例では、選択ゲート電極S Gは、第1シリサイド層5 1にZ軸方向で積層されたシリコン層5 5をさらに有する。すなわち、選択ゲート電極S Gは、シリコン層5 5と、シリコン層5 5に積層された第1シリサイド層5 1と、の積層構造を有している。

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【0061】

シリコン層5 5は、例えば、導電性が付与されたアモルファスシリコンまたはポリシリコンを含む。

【0062】

このように、選択ゲート電極S Gの上面5 1 u及び下面5 1 dの少なくともいずれかに、シリコン層5 5よりも抵抗が低い第1シリサイド層5 1を設けることで、選択ゲート電極S Gが低抵抗化でき、選択ゲートトランジスタS G Tの応答特性を向上できる。

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【0063】

さらに、本具体例では、選択ゲート電極SGの一部として、アモルファスシリコンまたはポリシリコンを含むシリコン層55を用いることで、選択ゲート電極SGと半導体ピラーSPとが交差する部分に形成される選択ゲートトランジスタSGTのしきい値特性が所望の値に設定され易くなり、不揮発性半導体記憶装置110の動作上有利となる。

【0064】

ただし、本発明はこれに限らず、選択ゲート電極SGが第1シリサイド層51を含めば良く、例えば、選択ゲート電極SGの全てが第1シリサイド層51であっても良い。この場合も、選択ゲート電極SGは、Z軸方向に対して垂直な面上に設けられた第1シリサイド層51を有するものとされる。

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【0065】

上記の第1シリサイド層51として、例えば、タングステン、モリブデン、チタン、コバルト、ニッケル、タンタル、バナジウム及びニオブよりなる群から選択された少なくともいずれかを含むシリサイドを用いることができる。

【0066】

以下、不揮発性半導体記憶装置110の製造方法の一例について説明する。

図5は、第1の実施形態に係る不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

すなわち、同図は、選択ゲート電極SGの製造方法に関する工程順模式的断面図である。

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【0067】

まず、例えば、シリコンからなる基板11の上に、層間絶縁膜13を形成した後、バックゲートBGとなる導電膜（例えば不純物が添加されたアモルファスシリコンまたはポリシリコン等）を形成し、この導電膜に、リソグラフィ及びRIE（Reactive Ion Etching）を用いて、接続部CPが形成される溝パターンを形成し、この溝パターン中にシリコン窒化膜からなる犠牲層を埋め込む。

その上に、電極間絶縁膜14と電極膜WLとを、交互に所望の繰り返しの数で堆積させ、その上に層間絶縁膜15を堆積させ、積層構造体MLを形成する。

【0068】

その後、図5（a）に表したように、積層構造体MLの上に、層間絶縁膜16、及び、選択ゲート電極SGとなる選択ゲート電極膜SGfを形成した後、その上に、CMP（Chemical Mechanical Polishing）加工のストッパとなるストッパ膜ST1を形成する。選択ゲート電極膜SGfには、例えば不純物が添加されたアモルファスシリコン膜を用い、ストッパ膜ST1には、例えばシリコン窒化膜を用いる。なお、後述するように、選択ゲート電極膜SGfは、選択ゲート電極SGの少なくとも一部となる膜であれば良い。

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【0069】

そして、図5（b）に表したように、フォトリソグラフィとRIEにより、ストッパ膜ST1と選択ゲート電極膜SGfとを加工して、X軸方向に延在する溝TR1を形成する。

【0070】

そして、図5（c）に表したように、溝TR1の中にNSG（Nondoped Silica Glass）などの絶縁材料を埋め込み、CMP処理を行い、層間絶縁膜17を形成する。

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【0071】

そして、図5（d）に表したように、例えばRIEにより、ストッパ膜ST1を除去する。

【0072】

そして、図5（e）に表したように、露出した選択ゲート電極膜SGf、及び、層間絶縁膜17の上に、例えばタングステン膜を形成する。そして、例えば熱処理を行うことで、選択ゲート電極膜SGfの上面の側にタングステンシリサイドからなる第1シリサイド層51が形成され、選択ゲート電極膜SGfの第1シリサイド層51以外の部分がシリコ

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ン層 55 となる。そして、不要なタングステン膜を除去し、層間絶縁膜 17 を露出させる。このように、第 1 シリサイド層 51 は、選択ゲート電極 SG (選択ゲート電極膜 SGf) に対して自己整合的に形成される。

【0073】

そして、図 5 (f) に表したように、第 1 シリサイド層 51 及び層間絶縁膜 17 の上に、層間絶縁膜 18 を形成し、層間絶縁膜 18、第 1 シリサイド層 51、シリコン層 55、層間絶縁膜 16、図示しない積層構造体 ML 及び図示しない層間絶縁膜 13 を貫通し、接続部 CP が形成される上記の溝パタン中の犠牲層に到達する貫通ホール TH を形成し、犠牲層を除去する。

【0074】

そして、図 5 (g) に表したように、貫通ホール TH 及び溝の内壁面に、外側絶縁膜 43、記憶層 48 及び内側絶縁膜 42 となる積層膜 49 を形成し、その内側に半導体ピラー SP 及び接続部 CP となる半導体ピラー膜 SPf を形成し、残余の空間に、芯材部 68 及び接続部芯材部 68 CP となる芯材部膜 68 f を埋め込む。そして、例えば RIE によりエッチバックして貫通ホール TH の上部の芯材部膜 68 f を除去し、それにより形成された空間にコンタクト用のアモルファスシリコン層 SPf1 を埋め込む。

【0075】

そして、図 5 (h) に表したように、貫通ホール TH の内部に埋め込まれた各種の膜、及び、層間絶縁膜 18 の上に層間絶縁膜 19 を形成する。

【0076】

この後、適宜、層間絶縁膜 19 を加工して、ソース線 SL、ビア 22、層間絶縁膜 23、及びビット線 BL を形成し、図 1 ~ 図 4 に例示した不揮発性半導体記憶装置 110 が形成できる。

【0077】

なお、シリサイド層を選択ゲート電極 SG の側面のみに設ける比較例の場合は、選択ゲート電極膜 SGf の側面のみにタングステンなどの金属膜を形成して、その側面にシリサイド層を形成することになる。これに対し、本実施形態に係る不揮発性半導体記憶装置 110 においては、第 1 シリサイド層 51 が Z 軸方向に対して垂直な面上、すなわち、本具体例では選択ゲート電極 SG の上面 51 u の側に設けられ、この場合は、選択ゲート電極膜 SGf の上面に金属膜を形成するので、側面への金属膜の形成の比較例よりも、より均一に金属膜を形成できる。この結果、第 1 シリサイド層 51 がより均一に形成でき、選択ゲート電極 SG をより安定して低抵抗化できるメリットがある。

【0078】

図 6 は、第 1 の実施形態に係る別の不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

すなわち、同図は、本実施形態に係る別の不揮発性半導体記憶装置 110 a の製造方法を例示している。不揮発性半導体記憶装置 110 a においては、選択ゲート電極 SG の下面 51 d (積層構造体 ML の側の面) の側に第 1 シリサイド層 51 a が設けられている。図 6 は、選択ゲート電極 SG の部分に関する製造方法を例示している。

【0079】

まず、不揮発性半導体記憶装置 110 と同様に、例えば、シリコンからなる基板 11 の上に、層間絶縁膜 13、バックゲート BG となる導電膜、導電膜の溝パタン、及び、溝パタン中の犠牲層を形成し、その上に、積層構造体 ML を形成する。

【0080】

そして、図 6 (a) に表したように、積層構造体 ML の上に層間絶縁膜 16 を形成し、その上に、薄いタングステン膜 51 a f を形成する

その後、図 6 (b) に表したように、タングステン膜 51 a f の上にアモルファスシリコンからなる選択ゲート電極膜 SGf を形成し、必要に応じて熱処理を行うことで、タングステンシリサイド層が形成でき、フォトリソグラフィと RIE により選択ゲート電極膜 SGf とタングステンシリサイド層を加工して、X 軸方向に延在する溝 TR1 を形成する

。これにより、タングステンシリサイド層からなる第1シリサイド層51aと、その上に積層されたシリコン層55と、有する選択ゲート電極SGが形成される。

【0081】

そして、図6(c)に表したように、溝TR1の中にNSGなどの絶縁材料を埋め込み、CMP処理を行い、層間絶縁膜17を形成する。

【0082】

そして、図6(d)に表したように、シリコン層55及び層間絶縁膜17の上に層間絶縁膜18を形成した後、層間絶縁膜18、シリコン層55、第1シリサイド層51a、層間絶縁膜16、図示しない積層構造体ML及び図示しない層間絶縁膜13を貫通し、接続部CPが形成される上記の溝パタン中の犠牲層に到達する貫通ホールTHを形成し、犠牲層を除去する。

【0083】

そして、図6(e)に表したように、貫通ホールTHの内壁面に、積層膜49、半導体ピラー膜SPf及び芯材部膜68fを埋め込み、上部の芯材部膜f68を除去し、その上部にアモルファスシリコン層SPf1を埋め込む。

【0084】

そして、図6(f)に表したように、貫通ホールTHの内部に埋め込まれた各種の膜、及び、層間絶縁膜18の上に層間絶縁膜19を形成する。

【0085】

この後、適宜、層間絶縁膜19を加工して、ソース線SL、ビア22、層間絶縁膜23、及びビット線BLを形成し、不揮発性半導体記憶装置110aが形成できる。

【0086】

不揮発性半導体記憶装置110aにおいても、選択ゲート電極SGの下面51dにシリコン層55よりも抵抗が低い第1シリサイド層51aを設けることで、選択ゲート電極SGが低抵抗化でき、選択ゲートトランジスタSGTの応答特性を向上できる。

【0087】

なお、選択ゲート電極の上面51uの側の第1シリサイド層51と、下面51dの側の第1シリサイド層51aと、を同時に設けても良い。

【0088】

なお、図6(a)及び(b)に例示した工程において、層間絶縁膜16の上に選択ゲート電極SGの一部となる、例えばアモルファスシリコンからなる下層選択ゲート電極膜を形成し、下層選択ゲート電極膜を選択ゲート電極SGのパタン形状に加工し、その上に、例えばタングステン膜を形成し、例えば熱処理を行うことで、下層選択ゲート電極膜のパタン形状の第1シリサイド層51aを形成し、さらに、その上に選択ゲート電極SGの他の一部となる上層選択ゲート電極膜を形成し、上層選択ゲート電極膜を加工し、これによりシリコン層55を形成して、下面51dの側に設けられた第1シリサイド層51aと、その上に積層されたシリコン層55と、有する選択ゲート電極SGを形成しても良い。

【0089】

なお、この工程において、下層選択ゲート電極膜の厚さを厚くすることで、下層選択ゲート電極膜の下面側が下側シリコン層であり、上面側が第1シリサイド層である積層構造が形成でき、結果として、層間絶縁膜16の側から順に、下側シリコン層、第1シリサイド層及びシリコン層が積層された構造を有する選択ゲート電極SGを形成することもできる。このように、第1シリサイド層は、Z軸に対して垂直な面上に設けられれば良く、選択ゲート電極SGの上面51u及び下面51dの少なくともいずれかだけでなく、選択ゲート電極SGの厚さ方向の中間に設けられていても良い。また、複数の第1シリコン層と複数のシリコン層とが、Z軸方向に積層されていても良い。

【0090】

図7は、第1の実施形態に係る別の不揮発性半導体記憶装置の構成を例示する模式的断面図である。

すなわち、同図は、選択ゲート電極SGの部分に関する部分的な模式的断面図である。

【0091】

図7に表したように、本実施形態に係る別の不揮発性半導体記憶装置111においては、選択ゲート電極SGは、その側面に設けられた第2シリサイド層52をさらに有する。これ以外は、不揮発性半導体記憶装置110と同様とすることができるので説明を省略する。

【0092】

第2シリサイド層52は、Z軸方向（第1方向）に対して平行な面上に設けられている。

【0093】

このように、不揮発性半導体記憶装置111の選択ゲート電極SGは、上面51uの側に第1シリサイド層51を有し、さらに、側面に第2シリサイド層52を有することで、選択ゲート電極SGをさらに低抵抗化でき、選択ゲートトランジスタSGTの応答特性をさらに向上できる。

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【0094】

なお、この場合も、選択ゲート電極SGの一部として、シリコン層55を用いることで、選択ゲート電極SGと半導体ピラーSPとが交差する部分に形成される選択ゲートトランジスタSGTのしきい値特性が所望の値に設定され易くなり、動作上有利となる。

【0095】

以下、不揮発性半導体記憶装置111の製造方法の例について説明する。

図8は、第1の実施形態に係る別の不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

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すなわち、同図は、選択ゲート電極SGの製造方法に関する工程順模式的断面図である。

【0096】

まず、例えば、シリコンからなる基板11の上に、層間絶縁膜13、バックゲートBGとなる導電膜、導電膜の溝パタン、及び、溝パタン中の犠牲層を形成し、その上に積層構造体MLを形成する。

【0097】

その後、図8（a）に表したように、積層構造体MLの上に、層間絶縁膜16及び選択ゲート電極SGとなる選択ゲート電極膜SGfを形成する。

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【0098】

そして、図8（b）に表したように、フォトリソグラフィとRIEにより、選択ゲート電極膜SGfを加工して、X軸方向に延在する溝TR1を形成する。

【0099】

そして、図8（c）に表したように、露出した選択ゲート電極膜SGfの上面及び側面に、例えばタングステン膜を形成する。そして、例えば熱処理を行うことで、選択ゲート電極膜SGfの上面の側に第1シリサイド層51が形成され、側面に第2シリサイド層52が形成され、選択ゲート電極膜SGfの第1シリサイド層51及び第2シリサイド層52以外の部分がシリコン層55となる。そして、不要なタングステン膜を除去し、層間絶縁膜16を露出させる。このように、第1シリサイド層51及び第2シリサイド層52は、選択ゲート電極SG（選択ゲート電極膜SGf）に対して自己整合的に形成される。

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【0100】

そして、図8（d）に表したように、層間絶縁膜16、第1シリサイド層51及び第2シリサイド層52を覆うように、例えばNSGなどの層間絶縁膜18aを形成し、層間絶縁膜17及び層間絶縁膜18を形成する。

【0101】

そして、図8（e）に表したように、層間絶縁膜18、第1シリサイド層51、シリコン層55、層間絶縁膜16、図示しない積層構造体ML及び図示しない層間絶縁膜13を貫通し、接続部CPが形成される上記の溝パタン中の犠牲層に到達する貫通ホールTHを形成し、犠牲層を除去する。

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【0102】

そして、図8(f)に表したように、貫通ホールTHの内壁面に、積層膜49、半導体ピラー膜SPf、芯材部膜68fを形成し、例えばRIEによりエッチバックして上部の芯材部膜68fを除去し、それにより形成された空間にコンタクト用のアモルファスシリコン層SPf1を埋め込む。

【0103】

その後、層間絶縁膜19、ソース線SL、ビア22、層間絶縁膜23、及びビット線BLを形成し、図7に例示した不揮発性半導体記憶装置111が形成できる。

【0104】

このような製造方法は、図5に関して説明した製造方法に比べ、工程が省略でき、生産性がさらに高い。

【0105】

また、不揮発性半導体記憶装置111の場合、選択ゲート電極膜SGfの上面及び側面の両方に金属膜を形成する際に、上面への金属膜の形成が均一に行われるので、側面への金属膜の形成の均一性への要求が緩和され、選択ゲート電極SGを安定してさらに低抵抗化できる。

【0106】

以下、上面の側にシリサイド層を有する選択ゲート電極SGを有する不揮発性記憶装置の製造方法の変形例について説明する。

図9は、第1の実施形態に係る別の不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

すなわち、同図は、選択ゲート電極SGの製造方法に関する工程順模式的断面図である。

【0107】

まず、例えば、シリコンからなる基板11の上に、層間絶縁膜13、バックゲートBGとなる導電膜、導電膜の溝パタン、及び、溝パタン中の犠牲層を形成し、その上に積層構造体MLを形成する。

【0108】

その後、図9(a)に表したように、積層構造体MLの上に、層間絶縁膜16、選択ゲート電極SGとなる選択ゲート電極膜SGf、及び、層間絶縁膜18bを形成する。層間絶縁膜18bには、例えばシリコン酸化膜を用いることができる。

【0109】

そして、図9(b)に表したように、フォトリソグラフィとRIEにより、層間絶縁膜18b、選択ゲート電極膜SGf、層間絶縁膜16、図示しない積層構造体ML及び図示しない層間絶縁膜13を貫通し、接続部CPが形成される上記の溝パタン中の犠牲層に到達する貫通ホールTHを形成し、犠牲層を除去する。

【0110】

そして、図9(c)に表したように、貫通ホールTHの内壁面に、積層膜49、半導体ピラー膜SPf、芯材部膜68fを形成し、例えばRIEによりエッチバックして上部の芯材部膜68fを除去し、それにより形成された空間にコンタクト用のアモルファスシリコン層SPf1を埋め込む。

【0111】

そして、図9(d)に表したように、層間絶縁膜18bを例えばフッ酸などを用いた処理により除去して、選択ゲート電極膜SGfの上面を露出させる。

【0112】

そして、図9(e)に表したように、露出した選択ゲート電極膜SGf、及び、貫通ホールTHに埋め込まれた層の上に、例えばタングステン膜を形成し、例えば熱処理を行う。これにより、選択ゲート電極膜SGfの上面の側にタングステンシリサイドからなる第1シリサイド層51が形成され、選択ゲート電極膜SGfの第1シリサイド層51以外の部分がシリコン層55となる。そして、貫通ホールTHに埋め込まれたアモルファスシリ

コン層 S P f 1 の上側には、タングステンシリサイドからなる第 3 シリサイド層 5 3 が形成される。なお、この場合も、第 1 シリサイド層 5 1 は、選択ゲート電極 S G (選択ゲート電極膜 S G f) に対して自己整合的に形成される。

【0113】

そして、図 9 (f) に表したように、フォトリソグラフィと R I E により、第 1 シリサイド層 5 1 とシリコン層 5 5 とを加工して、X 軸方向に延在する溝 T R 2 を形成する。

【0114】

そして、図 9 (g) に表したように、溝 T R 2 の内部を埋め込み、第 1 シリサイド層 5 1、貫通ホール T H に埋め込まれた層、及び、第 3 シリサイド層 5 3 を覆うように、層間絶縁膜 1 8 c を形成する。層間絶縁膜 1 8 c には例えばシリコン酸化膜を用いることができ、層間絶縁膜 1 8 c は、図 2 に例示した層間絶縁膜 1 7、1 8 及び 1 9 となる。

【0115】

その後、ソース線 S L、ビア 2 2、層間絶縁膜 2 3、及びビット線 B L を形成し、変形例の不揮発性半導体記憶装置 1 1 2 が形成できる。

【0116】

なお、本具体例では、貫通ホール T H によって形成された半導体ピラー S P の上部にもシリサイド層 (第 3 シリサイド層 5 3) が形成され、この第 3 シリサイド層 5 3 は、第 1 シリサイド層 5 1 と一括して形成される。

【0117】

以下、上面 5 1 u 及び側面にシリサイド層を有する選択ゲート電極 S G を有する不揮発性記憶装置の製造方法の変形例の 1 つについて説明する。

図 1 0 は、第 1 の実施形態に係る別の不揮発性半導体記憶装置の製造方法を例示する工程順模式的断面図である。

すなわち、同図は、選択ゲート電極 S G の製造方法に関する工程順模式的断面図である。本具体例においては、図 9 (a) ~ (d) に関して説明した工程までは同じであるので、それ以降の工程について説明する。

【0118】

貫通ホール T H の内壁面に、積層膜 4 9、半導体ピラー膜 S P f 及び芯材部膜 6 8 f を形成し、その上部にアモルファスシリコン層 S P f 1 を形成し、選択ゲート電極膜 S G f の上面を露出させた後、図 1 0 (a) に表したように、フォトリソグラフィと R I E により、選択ゲート電極膜 S G f を加工して、X 軸方向に延在する溝 T R 3 を形成する。

【0119】

そして、図 1 0 (b) に表したように、露出した選択ゲート電極膜 S G f の上面及び側面、並びに、貫通ホール T H に埋め込まれた層の上に、例えばタングステン膜を形成し、例えば熱処理を行う。これにより、選択ゲート電極膜 S G f の上面及び側面に、それぞれ、タングステンシリサイドからなる第 1 シリサイド層 5 1 及び第 2 シリサイド層 5 2 が形成され、選択ゲート電極膜 S G f の第 1 シリサイド層 5 1 及び第 2 シリサイド層 5 2 以外の部分がシリコン層 5 5 となる。そして、貫通ホール T H に埋め込まれたアモルファスシリコン層 S P f 1 の上に、タングステンシリサイドからなる第 3 シリサイド層 5 3 が形成される。なお、この場合も、第 1 シリサイド層 5 1 及び第 2 シリサイド層 5 2 は、選択ゲート電極 S G (選択ゲート電極膜 S G f) に対して自己整合的に形成される。

【0120】

そして、図 1 0 (c) に表したように、溝 T R 3 の残余の空間を埋め込み、第 1 シリサイド層 5 1、第 2 シリサイド層 5 2、貫通ホール T H に埋め込まれた層、及び、第 3 シリサイド層 5 3 を覆うように、層間絶縁膜 1 8 d を形成する。層間絶縁膜 1 8 d には例えばシリコン酸化膜を用いることができ、層間絶縁膜 1 8 d は、図 2 に例示した層間絶縁膜 1 7、1 8 及び 1 9 となる。

【0121】

その後、ソース線 S L、ビア 2 2、層間絶縁膜 2 3、及びビット線 B L を形成し、変形例の不揮発性半導体記憶装置 1 1 3 が形成できる。

【0122】

なお、本具体例では、貫通ホールTHによって形成された半導体ピラーSPの上部にもシリサイド層（第3シリサイド層53）が形成され、この第3シリサイド層53は、第1シリサイド層51及び第2シリサイド層52と一括して形成される。

【0123】

図11は、第1の実施形態に係る別の不揮発性半導体記憶装置の構成を例示する模式的断面図である。

図11に表したように、本実施形態に係る別の不揮発性半導体記憶装置115aにおいては、積層構造体MLを貫通している半導体ピラーSPの部分と、電極膜WLと、の間の構造が、選択ゲート電極SGを貫通している半導体ピラーSPの部分と、選択ゲート電極SGと、の間の構造と、が互いに異なっている。

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【0124】

すなわち、半導体ピラーSPの部分と電極膜WLとの間には、既に説明したように、外側絶縁膜43、記憶層48及び内側絶縁膜42の積層膜49が設けられているが、半導体ピラーSPと選択ゲート電極SGとの間には、積層膜49とは異なる絶縁膜である選択ゲート絶縁膜SGIが設けられている。この選択ゲート絶縁膜SGIにはシリコン酸化膜を用いることができる。このように、選択ゲート絶縁膜SGIの構成は、各種の変形が可能である。

【0125】

図12は、第1の実施形態に係る別の不揮発性半導体記憶装置の構成を例示する模式的断面図である。

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図12(a)に表したように、本実施形態に係る別の不揮発性半導体記憶装置115bにおいては、不揮発性半導体記憶装置110に対して、芯材部68が設けられず、半導体ピラーSPが管状ではなく、柱状となっている。これ以外は、不揮発性半導体記憶装置110と同様である。

【0126】

また、図12(b)に表したように、本実施形態に係る別の不揮発性半導体記憶装置115cにおいては、不揮発性半導体記憶装置115aに対して、芯材部68が設けられず、半導体ピラーSPが管状ではなく、柱状となっている。これ以外は、不揮発性半導体記憶装置115aと同様である。

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このように、半導体ピラーSPの構成は、各種の変形が可能である。

【0127】

図13及び図14は、第1の実施形態に係る別の不揮発性半導体記憶装置の構成を例示する、それぞれ模式的断面図及び模式的斜視図である。

なお、図14においては、図を見易くするために、導電部分のみを示し、絶縁部分は図示を省略している。

【0128】

図13及び図14に表したように、本実施形態に係る不揮発性半導体記憶装置120においては、半導体ピラーSPはU字形状に接続されておらず、それぞれの半導体ピラーSPが独立している。すなわち、不揮発性半導体記憶装置120においては、直線状のNANDストリングが設けられる。そして、積層構造体MLの上に上部選択ゲート電極USG（例えばドレイン側選択ゲート電極SGDとなる）が設けられ、積層構造体MLの下に下部選択ゲート電極LSG（例えばソース側選択ゲート電極SGSとなる）が設けられている。これらの上部選択ゲート電極USG及び下部選択ゲート電極LSGは、選択ゲート電極SGに含まれる。

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【0129】

上部選択ゲート電極USGと半導体ピラーSPとの間には、例えば酸化シリコンからなる上部選択ゲート絶縁膜USGIが設けられ、下部選択ゲート電極LSGと半導体ピラーSPとの間には、例えば酸化シリコンからなる下部選択ゲート絶縁膜LSGIが設けられる。これら上部選択ゲート絶縁膜USGI及び下部選択ゲート絶縁膜LSGIは、選択ゲ

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ート絶縁膜 SGI に含まれる。

【0130】

そして、下部選択ゲート電極 LSG の下側に、ソース線 SL が設けられている。ソース線 SL の下に層間絶縁膜 13a が設けられ、ソース線 SL と下部選択ゲート電極 LSG との間に層間絶縁膜 13b が設けられている。

【0131】

下部選択ゲート電極 LSG の下方において半導体ピラー SP はソース線 SL に接続され、上部選択ゲート電極 USG の上方において半導体ピラー SP はビット線 BL に接続されている。そして、上部選択ゲート電極 USG と下部選択ゲート電極 LSG との間の積層構造体 ML においてメモリセル MC が形成され、半導体ピラー SP が、直線状の 1 つの NAND ストリングとして機能する。

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【0132】

上部選択ゲート電極 USG 及び下部選択ゲート電極 LSG は、Y 軸方向に分断されており、X 軸方向に沿って延在する帯状の形状を有している。

【0133】

一方、半導体ピラー SP の上部に接続されるビット線 BL、及び、半導体ピラー SP の下部に接続されるソース線 SL は、Y 軸方向に延在する帯状の形状を有している。

そして、この場合は、電極膜 WL は、X-Y 平面に平行な板状の導電膜である。

【0134】

このような構造の不揮発性半導体記憶装置 120 においても、上部選択ゲート電極 USG 及び下部選択ゲート電極 LSG の少なくともいずれかは、Z 軸方向に対して垂直な面上に設けられた第 1 シリサイド層 51 を有する。ここで、Z 軸方向に対して垂直な面は、例えば、上部選択ゲート電極 USG 及び下部選択ゲート電極 LSG の少なくともいずれかの Z 軸方向に対して垂直な面である上面及び下面の少なくともいずれかとすることができる。

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【0135】

そして、この場合には、第 1 シリサイド層 51 が形成される上部選択ゲート電極 USG 及び下部選択ゲート電極 LSG の少なくともいずれかは、第 1 シリサイド層 51 に Z 軸方向で積層されたシリコン層 55 をさらに有する。すなわち、上部選択ゲート電極 USG 及び下部選択ゲート電極 LSG の少なくともいずれかは、シリコン層 55 と、シリコン層 55 に積層された第 1 シリサイド層 51 と、の積層構造を有している。

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【0136】

この場合もシリコン層 55 は、例えば、導電性が付与されたアモルファスシリコンまたはポリシリコンを含む。

【0137】

このように、上部選択ゲート電極 USG 及び下部選択ゲート電極 LSG の少なくともいずれかの上面及び下面の少なくともいずれかに、シリコン層 55 よりも抵抗が低い第 1 シリサイド層 51 を用いることで、選択ゲート電極 SG が低抵抗化でき、選択ゲートトランジスタ SGT の応答特性を向上できる。

【0138】

そして、この場合も、上部選択ゲート電極 USG 及び下部選択ゲート電極 LSG の少なくともいずれかは、Z 軸方向（第 1 方向）に対して平行な面上に設けられる第 2 シリサイド層 52 をさらに有していても良い。

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これにより、選択ゲート電極 SG をさらに低抵抗化でき、選択ゲートトランジスタ SGT の応答特性をさらに向上できる。

【0139】

なお、上部選択ゲート電極 USG の上面の側に第 1 シリサイド層 51 が設けられる場合には、上部選択ゲート電極 USG は、積層構造体 ML の基板 11 とは反対の側に設けられており、第 1 シリサイド層 51 は、上部選択ゲート電極 USG の積層構造体 ML とは反対の側の面に沿って設けられる。

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【0140】

一方、下部選択ゲート電極LSGの上面の側に第1シリサイド層51が設けられる場合には、下部選択ゲート電極LSGは、基板11と積層構造体MLとの間に設けられており、第1シリサイド層51は、下部選択ゲート電極LSGの積層構造体MLの側の面に沿って設けられる。

【0141】

(第2の実施の形態)

本発明の第2の実施形態に係る不揮発性半導体記憶装置の製造方法は、上記の実施形態に係る不揮発性半導体記憶装置及びその変形の不揮発性半導体記憶装置の製造方法である。すなわち、第1方向(例えばZ軸方向)に交互に積層された複数の電極膜WLと複数の電極間絶縁膜14とを有する積層構造体MLと、前記第1方向において積層構造体MLに積層された選択ゲート電極SGと、積層構造体MLと選択ゲート電極SGとを前記第1方向に貫通する半導体ピラーSPと、電極膜WLのそれぞれと半導体ピラーSPとの交差部に設けられた記憶部(メモリセルMC)と、半導体ピラーSPと選択ゲート電極SGとの間に設けられた選択ゲート絶縁膜SGIと、を有する不揮発性半導体記憶装置の製造方法である。以下では、本実施形態の特徴である選択ゲート電極SGの形成方法について説明する。

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【0142】

図15は、第2の実施形態に係る不揮発性半導体記憶装置の製造方法を例示するフローチャート図である。

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図15に表したように、本実施形態に係る製造方法においては、まず、積層構造体MLと、選択ゲート電極SGの少なくとも一部となる選択ゲート電極膜SGfと、を第1方向(Z軸方向)に積層する(ステップS110)。すなわち、積層構造体MLと選択ゲート電極膜SGfとを、例えば、基板11の主面11aの上に形成する。例えば、図5(a)に関して説明した処理を実施する。また、例えば、図6(a)に例示した処理を実施する場合は、この場合は、上記の選択ゲート電極SGは、図6(a)に例示した下層選択ゲート電極膜SGf1である。

【0143】

そして、選択ゲート電極膜SGfの前記第1方向に対して垂直な面をシリサイド化する(ステップS120)。例えば、図5(e)や図6(a)に関して説明した処理を実施する。

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【0144】

これにより、例えば、選択ゲート電極SGの上面51u及び下面51dの少なくともいずれかに、シリコン層55よりも抵抗が低い第1シリサイド層51が形成でき、選択ゲート電極SGが低抵抗化でき、選択ゲートトランジスタSGTの応答特性を向上できる。

【0145】

なお、ステップS120においては、選択ゲート電極膜SGfの第1方向に対して平行な面(すなわち、選択ゲート電極膜SGfの側面)を、さらにシリサイド化しても良い。すなわち、図8(c)または図10(b)に関して説明した処理を行う。これにより、選択ゲート電極SGの抵抗をさらに低下できる。

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【0146】

なお、本発明の実施形態に係る不揮発性半導体記憶装置において、電極間絶縁膜14、内側絶縁膜42、外側絶縁膜43、選択ゲート絶縁膜SGI及び芯材部68には、酸化シリコン、窒化シリコン、酸窒化シリコン、酸化アルミニウム、酸窒化アルミニウム、ハフニア、ハフニウム・アルミネート、窒化ハフニア、窒化ハフニウム・アルミネート、ハフニウム・シリケート、窒化ハフニウム・シリケート、酸化ランタン及びランタン・アルミネートよりなる群から選択されたいずれかの単層膜、または、前記群から選択された複数からなる積層膜を用いることができる。

【0147】

また、記憶層48には、窒化シリコン、酸窒化シリコン、酸化アルミニウム、酸窒化ア

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ルミニウム、ハフニア、ハフニウム・アルミネート、窒化ハフニア、窒化ハフニウム・アルミネート、ハフニウム・シリケート、窒化ハフニウム・シリケート、酸化ランタン及びランタン・アルミネートよりなる群から選択されたいずれかの単層膜、または、前記群から選択された複数からなる積層膜を用いることができる。

【0148】

なお、本願明細書において、「垂直」及び「平行」は、厳密な垂直及び厳密な平行だけでなく、例えば製造工程におけるばらつきなどを含むものであり、実質的に垂直及び実質的に平行であれば良い。

【0149】

以上、具体例を参照しつつ、本発明の実施の形態について説明した。しかし、本発明は、これらの具体例に限定されるものではない。例えば、不揮発性半導体記憶装置を構成する基板、電極膜、絶縁膜、絶縁層、積層構造体、記憶層、電荷蓄積層、半導体ピラー、ワード線、ビット線、ソース線、配線、メモリセルトランジスタ、選択ゲートトランジスタ等、各要素の具体的な構成に関しては、当業者が公知の範囲から適宜選択することにより本発明を同様に実施し、同様の効果を得ることができる限り、本発明の範囲に包含される。

また、各具体例のいずれか2つ以上の要素を技術的に可能な範囲で組み合わせたものも、本発明の要旨を包含する限り本発明の範囲に含まれる。

【0150】

その他、本発明の実施の形態として上述した不揮発性半導体記憶装置及びその製造方法を基にして、当業者が適宜設計変更して実施し得る全ての不揮発性半導体記憶装置及びその製造方法も、本発明の要旨を包含する限り、本発明の範囲に属する。

【0151】

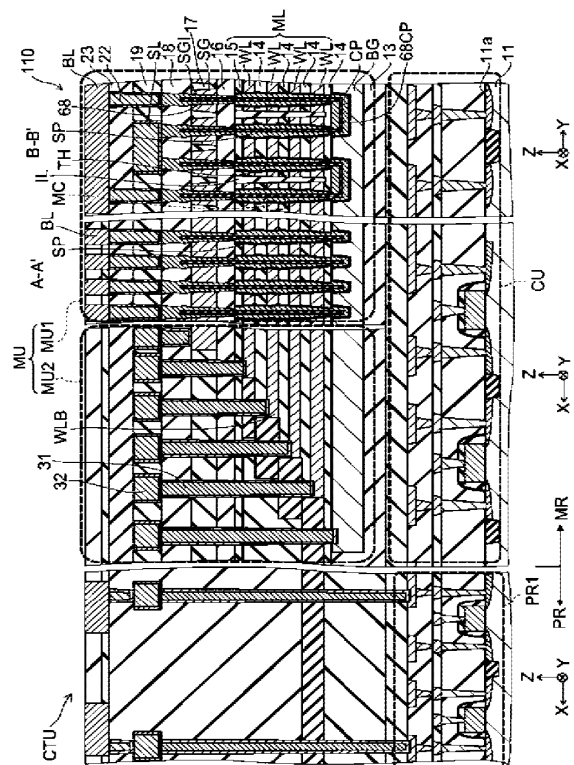
その他、本発明の思想の範疇において、当業者であれば、各種の変更例及び修正例に想到し得るものであり、それら変更例及び修正例についても本発明の範囲に属するものと了解される。例えば、前述の各実施形態に対して、当業者が適宜、構成要素の追加、削除若しくは設計変更を行ったもの、又は、工程の追加、省略若しくは条件変更を行ったものも、本発明の要旨を備えている限り、本発明の範囲に含有される。

【符号の説明】

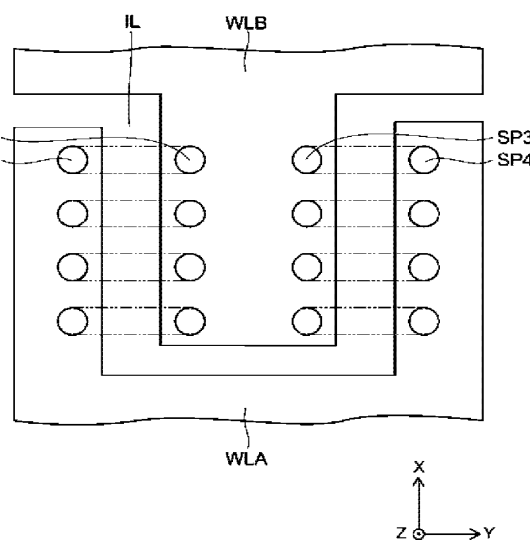
【0152】

11…基板、11a…主面、13、13a、13b、15、16、17、18、18a～18d、19、23…層間絶縁膜、14…電極間絶縁膜、22…ビア、31…ビアプラグ、32…ワード配線、42…内側絶縁膜、43…外側絶縁膜、48…記憶層、49…積層膜、51、51a…第1シリサイド層、51d…下面、51u…上面、52…第2シリサイド層、53…第3シリサイド層、55…シリコン層、68…芯材部、68CP…接続部芯材部、110、110a、111、112、113、115a～c、120…不揮発性半導体記憶装置、BG…バックゲート、BL…ビット線、CP…接続部、CP1、CP2…第1及び第2接続部、CTU…制御部、CU…回路部、IL…絶縁層、LSG…下部選択ゲート電極、LSGI…下部選択ゲート絶縁膜、MC…メモリセル（記憶部）、ML…積層構造体、MR…メモリアレイ領域、MU…メモリ部、MU1…マトリクスメモリセル部、MU2…配線接続部、PR…周辺領域、PR1…周辺領域回路、SG…選択ゲート電極、SG1～SG4…第1～第4選択ゲート電極、SGD…ドレイン側選択ゲート電極、SGI…選択ゲート絶縁膜、SGS…ソース側選択ゲート電極、SGT…選択ゲートトランジスタ、SGf…選択ゲート絶縁膜、SL…ソース線、SP…半導体ピラー、SP1～SP4…第1～第4半導体ピラー、SPf…半導体ピラー膜、SPf1…アモルファスシリコン層、ST1…ストッパ膜、TH…貫通ホール、TR1～TR3…溝、USG…上部選択ゲート電極、USGI…上部選択ゲート絶縁膜、V1、V2…ビア、WL、WLA、WLB…電極膜

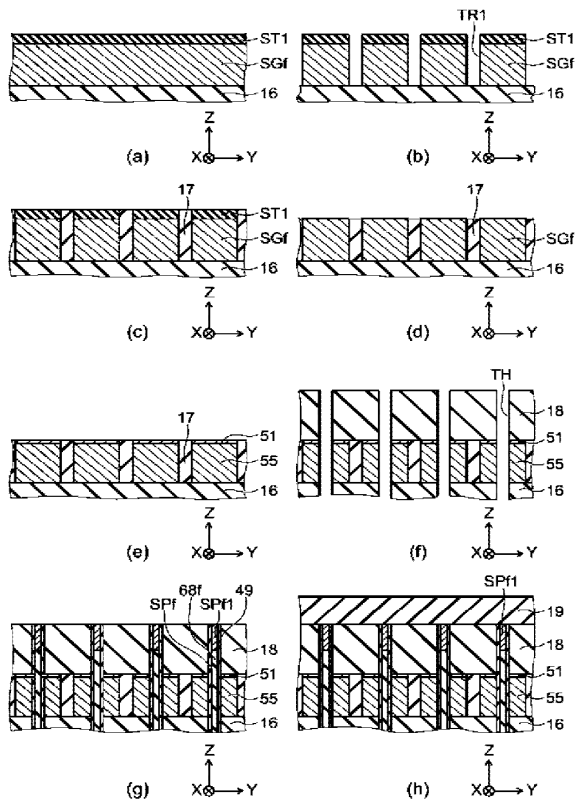
【图 2】



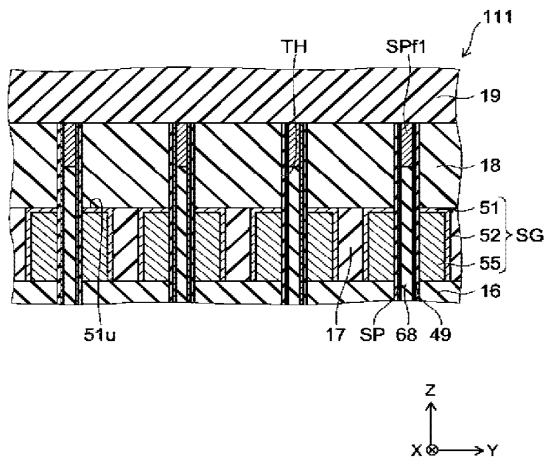
【图 4】



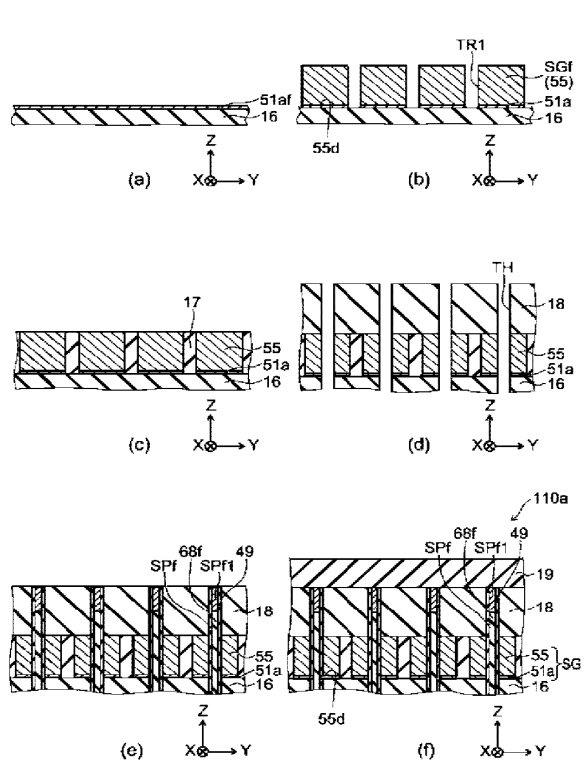
【図 5】



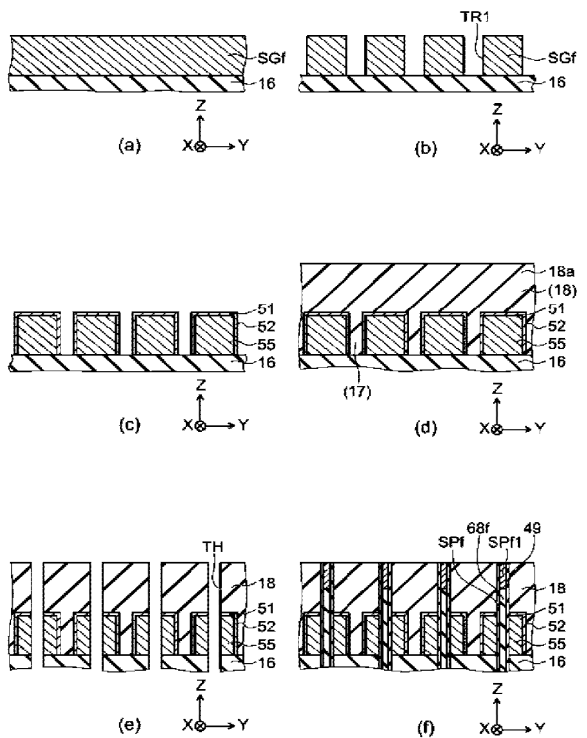
【図 7】



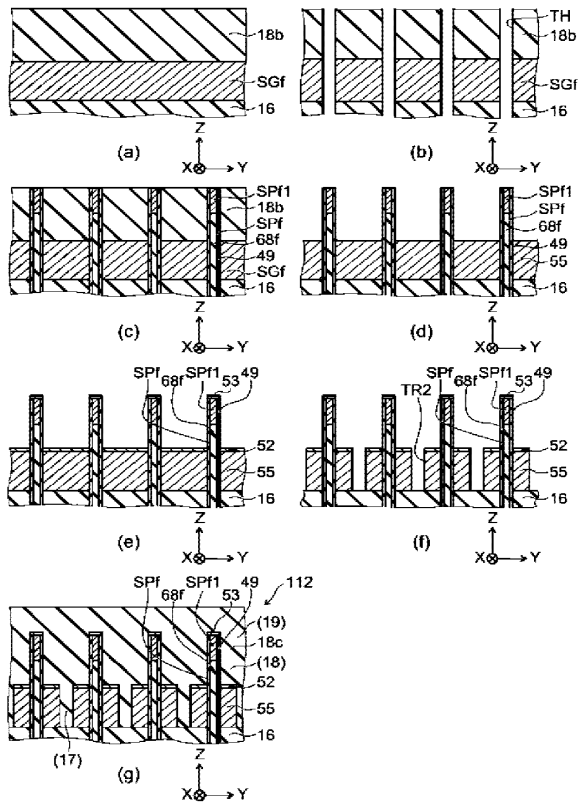
【図 6】



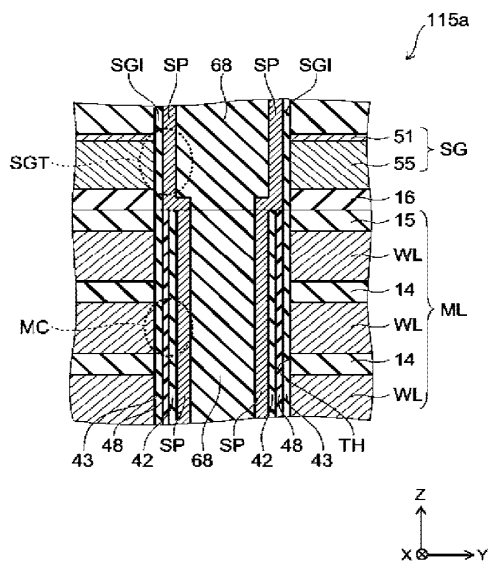
【図 8】



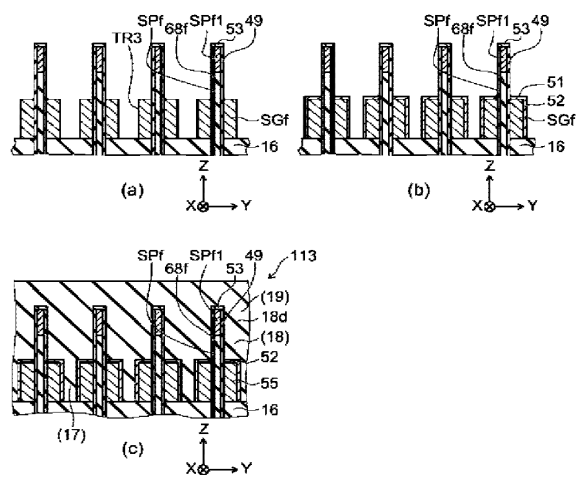
【図 9】



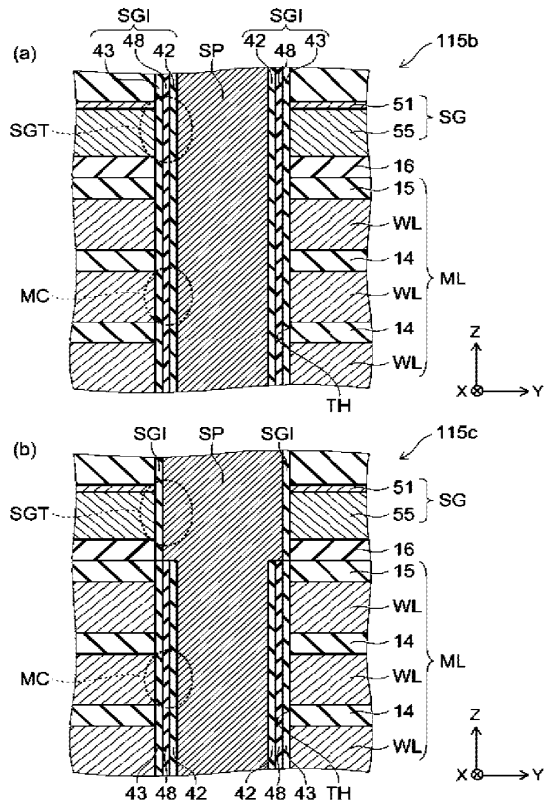
【図 11】



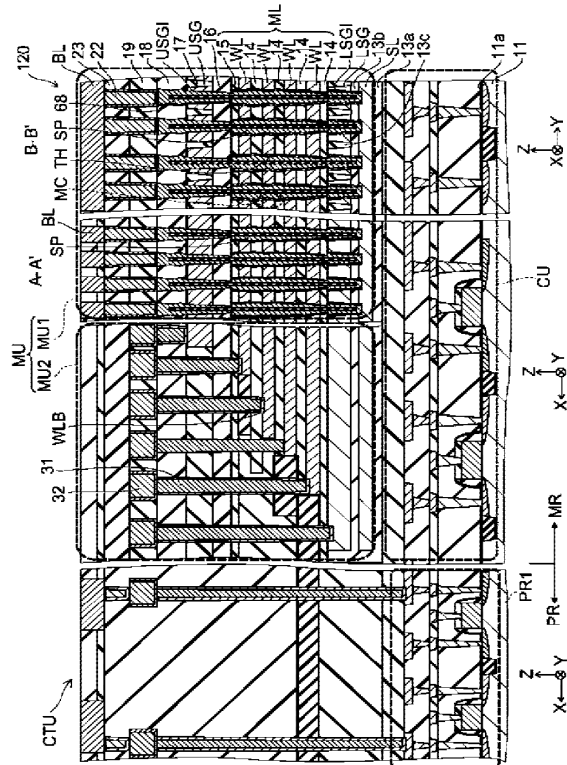
【図 10】



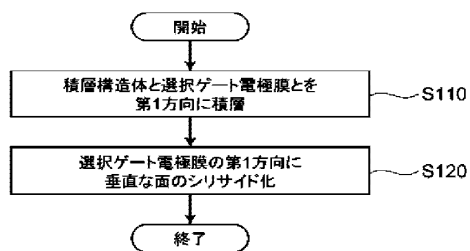
【図 12】



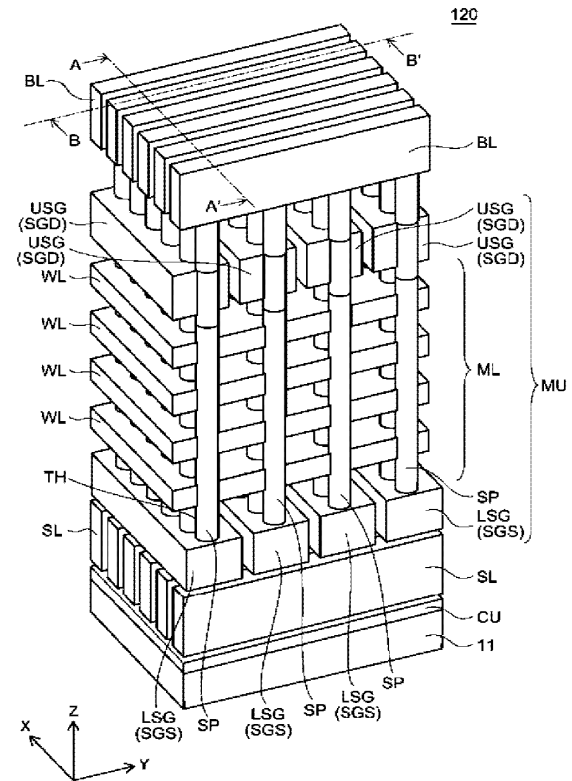
【図 1 3】



【図 1 5】



【図 1 4】



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5F101 BA42 BA45 BA47 BB02 BD16 BD22 BD30 BD34

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PATENT

Docket No. PM07027D1CIP1C6 (3430.2.388US6CIP1)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Igor Polishchuk et al.

Serial No.: 17/157,350

Filed: January 25, 2021

Title: MEMORY TRANSISTOR WITH MULTIPLE
CHARGE STORING LAYERS AND A HIGH WORK
FUNCTION GATE ELECTRODE

Examiner: Not assigned

Group Art
Unit: 2893

PRELIMINARY AMENDMENT

TO THE COMMISSIONER FOR PATENTS:

Before examination, please amend the above-identified patent application as follows.

Amendments to the Claims begin on page 2.

Remarks begin on page 9 of this paper.

AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Canceled)
2. (New) A method comprising:
 - forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;
 - forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate;
 - forming on sidewalls of the opening a blocking dielectric layer;
 - forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region;
 - forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and
 - forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.
3. (New) The method of claim 2, further comprising the step of etching the sacrificial layer to form a second opening.
4. (New) The method of claim 3, further comprising the step of depositing a gate electrode in the second opening.
5. (New) The method of claim 4, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.

6. (New) The method of claim 4, wherein the deposited gate electrode is a high work function gate electrode.
7. (New) The method of claim 2, wherein the vertical channel formed includes an annular region.
8. (New) The method of claim 7, wherein at least a portion of the vertical channel is formed of polysilicon.
9. (New) The method of claim 7, wherein the vertical channel formed includes an outer layer of semiconductor material.
10. (New) The method of claim 9, wherein the outer layer of semiconductor material is formed of polysilicon.
11. (New) The method of claim 7, wherein the vertical channel formed includes a layer of semiconductor material surrounding a cylinder of filler material.
12. (New) The method of claim 2, further comprising the step of forming a second diffusion region such that the vertical channel connects the first and second diffusion regions.
13. (New) The method of claim 2, further comprising forming a layer of semiconductor material including a second doped diffusion region over a top surface of the stack of layers and the opening, wherein the vertical channel electrically couples the first doped diffusion region to the second doped diffusion region.
14. (New) The method of claim 2, wherein the second dielectric layer separates the sacrificial layer from an overlying memory transistor.

15. (New) The method of claim 2, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.
16. (New) The method of claim 15, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.
17. (New) The method of claim 15, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.
18. (New) The method of claim 7, wherein the blocking dielectric layer is formed in a substantially annular shape.
19. (New) The method of claim 18, wherein the multi-layer charge storing region is formed in a substantially annular shape.
20. (New) The method of claim 19, wherein the tunnel dielectric layers is formed in a substantially annular shape.
21. (New) The method of claim 2, wherein the blocking dielectric layer includes a high K dielectric.
22. (New) The method of claim 18, wherein the blocking dielectric layer includes a high K dielectric.
23. (New) The method of claim 4, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.
24. (New) A method comprising:
forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from

the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;

forming an opening extending through the stack of layers towards the substrate;

forming on sidewalls of the opening an annular shaped blocking dielectric layer;

forming on an inside sidewall of the blocking dielectric layer an annular shaped multi-layer charge storing region;

forming on an inside sidewall of the multi-layer charge storing region an annular shaped tunnel dielectric layer; and

forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layers.

25. (New) The method of claim 24, further comprising the step of etching the sacrificial layer to form a second opening.

26. (New) The method of claim 25, further comprising the step of depositing a gate electrode in the second opening.

27. (New) The method of claim 26, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.

28. (New) The method of claim 26, wherein the deposited gate electrode is a high work function gate electrode.

29. (New) The method of claim 24, wherein the second dielectric layer separates the sacrificial layer from an overlying memory transistor.

30. (New) The method of claim 24, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.

31. (New) The method of claim 30, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.
32. (New) The method of claim 31, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.
33. (New) The method of claim 26, wherein the blocking dielectric layer includes a high K dielectric.
34. (New) The method of claim 33, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.
35. (New) The method of claim 34, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.
36. (New) A semiconductor memory device, comprising:
a semiconductor substrate,
a channel region oriented substantially perpendicular to the semiconductor substrate,
the channel region formed in a substantially annular shape,
a tunnel dielectric layer surrounding the channel region, the tunnel dielectric layer formed in a substantially annular shape,
a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape,
a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and
a gate electrode surrounding the blocking dielectric layer.
37. (New) The semiconductor memory device of claim 36, wherein the multi-layer charge storing region includes a first oxygen-lean nitride layer and a second oxygen-rich nitride layer.

38. (New) The semiconductor memory device of claim 37, wherein the first oxygen-lean nitride layer and the second oxygen-rich nitride layer both include silicon, nitrogen and oxygen components.
39. (New) The semiconductor memory device of claim 38, wherein the first oxygen-lean nitride layer is formed on an inside sidewall of the blocking dielectric layer and wherein the second oxygen-rich nitride layer is formed on the inside sidewall of the first oxygen-lean nitride layer.
40. (New) The semiconductor memory device of claim 39, wherein the blocking dielectric layer includes a high K dielectric.
41. (New) The semiconductor memory device of claim 36, including a stack of layers formed over the substrate.
42. (New) The semiconductor memory device of claim 41, wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer, wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer.
43. (New) The semiconductor memory device of claim 42, wherein the channel region is formed in an opening extending through the stack of layers.
44. (New) The semiconductor memory device of claim 42, wherein the second dielectric layer separates the gate layer from an overlying memory transistor.
45. (New) The semiconductor memory device of claim 36, wherein the blocking dielectric layer includes a high K dielectric.

46. (New) The semiconductor memory device of claim 36, wherein the gate electrode is a high work function gate electrode.

REMARKS

The Applicant respectfully submits that the Application is in condition for allowance. If the Examiner notes any further matters that may be resolved by a telephone interview or Examiner's amendment, the Examiner is encouraged to contact the Applicant using the contact information listed below.

Respectfully submitted,

/Michael L. Bartholomew/_____
Michael L. Bartholomew
Reg. No. 60,225
Attorney for Applicant

Date: November 1, 2021
50 W. Broadway, 10th Floor
Salt Lake City, UT 84111
Telephone (801) 994-4646
Fax (801) 531-1929

Electronic Patent Application Fee Transmittal				
Application Number:		17157350		
Filing Date:		25-Jan-2021		
Title of Invention:		MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
First Named Inventor/Applicant Name:		Igor Polishchuk		
Filer:		Michael Lee Bartholomew		
Attorney Docket Number:		PM07027D1CIP1C6		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	25	100	2500
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2500

Electronic Acknowledgement Receipt

EFS ID:	44175412
Application Number:	17157350
International Application Number:	
Confirmation Number:	6135
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	36491
Filer:	Michael Lee Bartholomew
Filer Authorized By:	
Attorney Docket Number:	PM07027D1CIP1C6
Receipt Date:	01-NOV-2021
Filing Date:	25-JAN-2021
Time Stamp:	17:34:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$2500
RAM confirmation Number	E2021A1H35184268
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		3430-2-388US6CIP1_PreliminaryAmendment.pdf	104208	yes	9
			e0f3e48ae79d0723ce4ef3082698597cfee1fc10		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Preliminary Amendment		1	1	
	Claims		2	8	
	Applicant Arguments/Remarks Made in an Amendment		9	9	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	38097	no	2
			97b7eacd15c007541050b72ff83f8b992636ded6f		
Warnings:					
Information:					
Total Files Size (in bytes):			142305		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 17/157,350		Filing Date 01/25/2021		☐ To be Mailed		
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO										
APPLICATION AS FILED - PART I										
		(Column 1)	(Column 2)							
FOR		NUMBER FILED	NUMBER EXTRA	RATE (\$)		FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A	N/A						
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A	N/A						
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A	N/A						
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 = *		x \$100 =						
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 = *		x \$480 =						
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL						
APPLICATION AS AMENDED - PART II										
AMENDMENT	11/01/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 45	Minus	** 45	= 0	x \$100 =		0		
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	x \$480 =		0		
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		0		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =				
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =				
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE				
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE				
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/TERRANCE R LAWRENCE/				
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".										
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

36491 7590 07/20/2022
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

EXAMINER

YUSHIN, NIKOLAY K

ART UNIT

PAPER NUMBER

2893

DATE MAILED: 07/20/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/157,350	01/25/2021	Igor Polishchuk	PM07027D1CIPIC6	6135

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	10/20/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

36491 7590 07/20/2022
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/157,350	01/25/2021	Igor Polishchuk	PM07027D1CIP1C6	6135

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	10/20/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

- ☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. **NOTE:** If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/157,350	01/25/2021	Igor Polishchuk	PM07027D1CIP1C6	6135
36491	7590	07/20/2022	EXAMINER	
Kunzler Bean & Adamson			YUSHIN, NIKOLAY K	
50 W. Broadway			ART UNIT	
Suite 1000			PAPER NUMBER	
Salt Lake City, UT 84101			2893	
DATE MAILED: 07/20/2022				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/157,350	Applicant(s) Polishchuk et al.	
	Examiner NIKOLAY K YUSHIN	Art Unit 2893	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Application filed on 01/25/2021.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2-46. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>See Continuation Sheet</u> .	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	

/NIKOLAY K YUSHIN/ Primary Examiner, Art Unit 2893	
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Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 05/25/2021; 05/25/2021; 08/02/2021; 08/18/2021

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Status of Claims

Claims 2 - 46 are under consideration in this Office Action.

Allowable Subject Matter

Claims 2 - 46 are allowed.

The following is an examiner's statement of reasons for allowance:

In re Claim 2, prior-art fails to disclose a method comprising steps of "forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate; forming on sidewalls of the opening a blocking dielectric layer; forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region; forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers" Therefore, the claimed method differs from prior art methods on this point and there is no evidence it would have been obvious to make this change.

In re Claim 24, prior-art fails to disclose a method comprising steps of "forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layer." Therefore, the claimed method differs from prior art methods on this point and there is no evidence it would have been obvious to make this change.

In re Claim 36, prior-art fails to disclose a semiconductor memory device, comprising a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape, a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and a gate electrode surrounding the blocking dielectric layer.” Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY K YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached Monday-Friday (7-7 PST).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Yara B. Green can be reached on 5712703075. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY K YUSHIN/
Primary Examiner, Art Unit 2893

Issue Classification 	Application/Control No. 17/157,350	Applicant(s)/Patent Under Reexamination Polishchuk et al.	
	Examiner NIKOLAY K YUSHIN	Art Unit 2893	

CPC						
Symbol				Type	Version	
H01L	/	29	/	4234	F	2013-01-01
H01L	/	29	/	40117	I	2019-08-01
H01L	/	29	/	792	I	2013-01-01
H01L	/	29	/	513	I	2013-01-01
H01L	/	29	/	518	I	2013-01-01
H01L	/	29	/	66833	I	2013-01-01
H01L	/	29	/	7926	I	2013-01-01
B82Y	/	10	/	00	I	2013-01-01
H01L	/	27	/	11526	I	2013-01-01
G11C	/	16	/	0466	I	2013-01-01
H01L	/	27	/	11563	I	2013-01-01
H01L	/	29	/	4916	I	2013-01-01
H01L	/	29	/	511	I	2013-01-01
H01L	/	21	/	0214	I	2013-01-01
H01L	/	21	/	02532	I	2013-01-01
H01L	/	21	/	02595	I	2013-01-01
H01L	/	29	/	0676	I	2013-01-01
H01L	/	29	/	66795	I	2013-01-01
H01L	/	27	/	11568	I	2013-01-01
H01L	/	27	/	11573	I	2013-01-01
H01L	/	27	/	11575	I	2013-01-01
H01L	/	29	/	0649	I	2013-01-01
H01L	/	29	/	42344	I	2013-01-01
H01L	/	29	/	512	I	2013-01-01

CPC Combination Sets					
Symbol			Type	Set	Ranking
	/				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	45	
/NIKOLAY K YUSHIN/ Primary Examiner, Art Unit 2893	24 June 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	36	10C&10D

Issue Classification 	Application/Control No. 17/157,350	Applicant(s)/Patent Under Reexamination Polishchuk et al.
	Examiner NIKOLAY K YUSHIN	Art Unit 2893

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L	/	21	/ 02
H01L	/	27	/ 11563
H01L	/	29	/ 00
G11C	/	16	/ 04
NON-CLAIMED			
/	/	/	/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

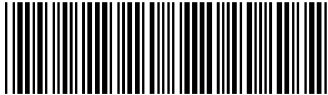
NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	45	
/NIKOLAY K YUSHIN/ Primary Examiner, Art Unit 2893 (Primary Examiner)	24 June 2022 (Date)	O.G. Print Claim(s) 36	O.G. Print Figure 10C&10D

Issue Classification 	Application/Control No. 17/157,350	Applicant(s)/Patent Under Reexamination Polishchuk et al.
	Examiner NIKOLAY K YUSHIN	Art Unit 2893

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☐ T.D.
 ☐ R.1.47

CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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1	2	16	11	22	20	24	29	39	38						
9	3	2	12	5	21	25	30	40	39						
10	4	3	13	20	22	26	31	41	40						
11	5	4	14	13	23	27	32	42	41						
12	6	6	15	23	24	32	33	43	42						
14	7	7	16	28	25	33	34	44	43						
15	8	8	17	29	26	34	35	45	44						
17	9	19	18	30	27	35	36	36	45						

NONE	Total Claims Allowed:	
(Assistant Examiner)	(Date)	45
/NIKOLAY K YUSHIN/ Primary Examiner, Art Unit 2893	24 June 2022	O.G. Print Claim(s)
(Primary Examiner)	(Date)	36
		O.G. Print Figure
		10C&10D

<i>Search Notes</i> 	Application/Control No. 17/157,350	Applicant(s)/Patent Under Reexamination Polishchuk et al.
	Examiner NIKOLAY K YUSHIN	Art Unit 2893

CPC - Searched*		
Symbol	Date	Examiner
B82Y10/00; B82Y40/00	06/24/2022	NY
G11C16/0466; G11C16/02; G11C16/3459; G11C16/379	06/24/2022	NY
H01L21/02532; H01L21/0214; H01L21/02595	06/24/2022	NY
H01L27/11526; H01L27/11573; H01L27/11563; H01L27/11575; H01L27/11568	06/24/2022	NY
H01L29/511; H01L29/4916; H01L29/66833; H01L29/0649; H01L29/42344; H01L29/7926; H01L29/518; H01L29/40117; H01L29/66795; H01L29/792; H01L29/0676; H01L29/513; H01L29/512; H01L29/4234	06/24/2022	NY

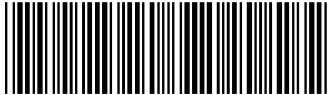
CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Keyword, inventor names, assignee searching - see search history	06/24/2022	NY

/NIKOLAY K YUSHIN/ Primary Examiner, Art Unit 2893	
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<i>Search Notes</i> 	Application/Control No. 17/157,350	Applicant(s)/Patent Under Reexamination Polishchuk et al.
	Examiner NIKOLAY K YUSHIN	Art Unit 2893

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
B82Y10	00	06/24/2022	NY
B82Y40	00	06/24/2022	NY
G11C16	0466; 02; 3459; 379	06/24/2022	NY
H01L21	02532; 0214; 02595	06/24/2022	NY
H01L27	11526; 11573; 11563; 11575; 11568	06/24/2022	NY
H01L29	511; 4916; 66833; 0649; 42344; 7926; 518; 40117; 66795; 792; 0676; 513; 512; 4234	06/24/2022	NY

/NIKOLAY K YUSHIN/ Primary Examiner, Art Unit 2893	
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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	27	((("LONGITUDE") near3 ("FLASH") near3 ("MEMORY") near3 ("SOLUTIONS") near3 ("LTD"))).AS,AANM.	(USPAT)	OR	ON	ON	2022/06/23 05:58 PM
L2	176	((("LONGITUDE") near3 ("FLASH") near3 ("MEMORY") near3 ("SOLUTIONS") near3 ("LTD"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/23 05:58 PM
L3	356	((("POLISHCHUK") near3 ("Igor")) OR ((("LEVY") near3 ("Sagy")) OR ((("RAMKUMAR") near3 ("Krishnaswamy"))).INV	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/06/23 05:58 PM
L4	658	((("POLISHCHUK") near3 ("Igor")) OR ((("LEVY") near3 ("Sagy")) OR ((("RAMKUMAR") near3 ("Krishnaswamy"))).INV	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/23 05:59 PM
L5	80	L4 AND L2	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO)); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/23 05:59 PM
L6	40	L4 AND L2	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/23 05:59 PM
L7	20	L4 AND L2	(USPAT)	OR	ON	ON	2022/06/23 05:59 PM
L8	1	17/157350	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/23 06:01 PM
L9	30	16/429464;15/864832; 16/429464; 15/335180; 14/811346; 14/159315; 13/539466; 13/288919; 12/152518	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/23 06:04 PM
L10	21	16/429464;15/864832; 16/429464; 15/335180; 14/811346; 14/159315;	(USPAT)	OR	ON	ON	2022/06/23 06:05 PM

L11	93	13/539466; 13/288919; 12/152518 ("5408115" "6025267" "6114734" "6127227" "6153543" "20060017092" "20060228907" "7060594" "7927951" "20090065849" "5348903" "5464783" "5972804" "6174774" "6277683" "2005245034" "2006220106" "20080290398" "6001713" "8008713" "7425491" "6462370" "20050062098" "20100270609" "4395438" "4543707" "4870470" "5861347" "6020606" "6214689" "20060051880" "20070029625" "20060284236" "6174758" "5405791" "5500816" "5550078" "5573963" "5939333" "5972765" "6074915" "6147014" "7279740" "7692246" "8163660" "20080272424" "5543336" "20020048893" "6136654" "6140187" "6268299" "6297173" "6321134" "6348380" "2006113627" "20100252877" "5773343" "20060113586" "7576386" "20100178759" "20020048200" "5937323" "6162700" "6217658" "6335288" "2005093054" "6717860" "7646041" "20060008959" "20070232007" "6573149" "4843023" "5793089" "6015739" "6150286" "6157426" "20060081331" "20070272971" "20080087942" "20080237684" "2008237694" "20090206385" "6596590" "4257832" "4490900" "5404791" "5817170" "5847411" "6023093" "6218700" "6287913" "6297096" "20070012988" "200815003" "20090227116" "4667217" "6518113" "2008290400" "20100006922" "5179038").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/23 06:37 PM
L14	97446956	(semiconductor memory	(US-PGPUB; USPAT;	OR	ON	ON	2022/06/23

L15	39	substrate channel annular (tunnel ADJ dielectric) layer (multilayer OR multi\$layer) charge storing (block\$4 ADJ dielectric) (gate nADJ electrode))	USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	07:06 PM
L16	45	(semiconductor memory substrate channel annular (tunnel ADJ dielectric) layer (multilayer OR multi\$layer) charge storing (block\$4 ADJ dielectric) (gate ADJ electrode))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:06 PM
L17	45	(semiconductor memory substrate channel annular (tunnel ADJ dielectric) layer (multilayer OR multi\$layer) charge stor\$4 (block\$4 ADJ dielectric) (gate ADJ electrode))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:07 PM
L18	158	(memory substrate channel annular (tunnel ADJ dielectric) layer (multilayer OR multi\$layer) charge stor\$4 (block\$4 ADJ dielectric) (gate ADJ electrode))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:07 PM
L19	37	(memory substrate channel (circ\$4 OR annular) (tunnel ADJ dielectric) layer (multilayer OR multi\$layer) charge stor\$4 (block\$4 ADJ dielectric) (gate ADJ electrode))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:08 PM
L20	37	L18 AND (B82Y10/00; B82Y40/00).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:08 PM
		L18 AND (B82Y\$/00).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU,	AND	ON	ON	2022/06/23 07:10 PM

L21	62	L18 AND (G11C16/0466; G11C16/02).CPC.	SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:10 PM
L22	97	L18 AND (G11C16/\$).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:11 PM
L23	67	L18 AND (G11C16/0466; G11C16/02; G11C16/3459; G11C16/379).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:12 PM
L24	14	L18 AND (H01L21/02532; H01L21/0214; H01L21/02595).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:12 PM
L25	95	L18 AND (H01L27/11526; H01L27/11573; H01L27/11563; H01L27/11575; H01L27/11568).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:13 PM
L26	130	L18 AND (H01L29/511; H01L29/4916; H01L29/66833; H01L29/0649; H01L29/42344; H01L29/7926; H01L29/518; H01L29/40117; H01L29/66795; H01L29/792; H0 L29/0676; H01L29/513; H01L29/512; H01L29/4234).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 07:13 PM

L27	70	L18 AND (H01L29/511; H01L29/4916; H01L29/66833; H01L29/0649; H01L29/42344; H01L29/7926; H01L29/518; H01L29/40117; H01L29/66795; H01L29/792; H0 L29/0676; H01L29/513; H01L29/512; H01L29/4234).CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 07:13 PM
L28	61	L18 AND (H01L27/11526; H01L27/11573; H01L27/11563; H01L27/11575; H01L27/11568).CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 07:15 PM
L29	13	L18 AND (H01L21/02532; H01L21/0214; H01L21/02595).CPC.	(US-PGPUB; USPAT; DERWENT)	AND	ON	ON	2022/06/23 07:15 PM
L30	21	L18 AND (B82Y\$/00)CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 07:17 PM
L31	56	L4 AND (B82Y\$/00)CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 11:54 PM
L32	114	L4 AND (B82Y10/00; B82Y40/00).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 11:54 PM
L33	0	L4 AND (B82Y40/00).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 11:54 PM
L34	0	L2 AND (B82Y40/00).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 11:54 PM
L35	0	L3 AND (B82Y40/00).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR,	AND	ON	ON	2022/06/23 11:55 PM

L36	28564	(B82Y40/00).CPC.	GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/23 11:55 PM
L37	28546	(B82Y40/00).CPC.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2022/06/23 11:55 PM
L38	11512	(B82Y40/00).CPC. AND (B82Y10/00).CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 11:56 PM
L39	4	(B82Y40/00).CPC. AND (B82Y10/00).CPC. AND (G11C16/0466; G11C16/02; G11C16/3459; G11C16/379).CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 11:56 PM
L45	26999	(G11C16/0466; G11C16/02; G11C16/3459; G11C16/379).CPC.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/24 12:01 AM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	0	(memory substrate channel (circl\$4 OR annular) (tunnel ADJ dielectric) layer (multilayer OR multi\$layer) charge stor\$4 (block\$4 ADJ dielectric) (gate ADJ electrode)).clm.	(US-PGPUB; USPAT)	SAME	ON	ON	2022/06/23 07:42 PM
N2	0	(memory substrate channel (circl\$4 OR annular) (tunnel ADJ dielectric) layer (multilayer OR multi\$layer) charge stor\$4 (block\$4 ADJ dielectric) (gate ADJ electrode))	(US-PGPUB; USPAT)	SAME	ON	ON	2022/06/23 07:42 PM
N3	90	(memory substrate channel (circl\$4 OR annular) (tunnel ADJ dielectric) layer (multilayer OR multi\$layer) charge	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 07:42 PM

N4	21	stor\$4 (block\$4 ADJ dielectric) (gate ADJ electrode)) N3 AND (B82Y10/00; B82Y40/00).CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 07:43 PM
N5	50	N3 AND (G11C16/0466; G11C16/02; G11C16/3459; G11C16/379).CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 07:43 PM
N6	13	N3 AND (H01L21/02532; H01L21/0214; H01L21/02595).CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 07:44 PM
N7	61	N3 AND (H01L27/11526; H01L27/11573; H01L27/11563; H01L27/11575; H01L27/11568).CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 07:44 PM
N8	70	N3 AND (H01L29/511; H01L29/4916; H01L29/66833; H01L29/0649; H01L29/42344; H01L29/7926; H01L29/518; H01L29/40117; H01L29/66795; H01L29/792; H01L29/0676; H01L29/513; H01L29/512; H01L29/4234).CPC.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/23 07:44 PM

Bibliographic Data

Application No: 17/157,350

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

/NIKOLAY K YUSHIN/

Examiner's Signature

Initials

Title:

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING
LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/25/2021	257	2893	PM07027D1CIP1C6
RULE			

APPLICANTS

LONGITUDE FLASH MEMORY SOLUTIONS LTD., Dublin, IRELAND

INVENTORS

Igor Polishchuk, Fremont, CA, UNITED STATES

Sagy Charel Levy, Zichron Yaakov, ISRAEL

Krishnaswamy Ramkumar, San Jose, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 16429464 06/03/2019 PAT 10903325

16429464 is a CON of 15864832 01/08/2018 PAT 10312336

15864832 is a CON of 15335180 10/26/2016 PAT 9929240

15335180 is a CON of 14811346 07/28/2015 PAT 9502543

14811346 is a CON of 14159315 01/20/2014 PAT 9093318

14159315 is a CON of 13539466 07/01/2012 PAT 8633537

13539466 is a CIP of 13288919 11/03/2011 PAT 8859374

13288919 is a DIV of 12152518 05/13/2008 PAT 8063434

12152518 has PRO of 60940160 05/25/2007

FOREIGN APPLICATIONS

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02/04/2021

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Salt Lake City, UT 84101
UNITED STATES

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\$1,980

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

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	Filing Date	2021-01-25
	First Named Inventor	Igor Polishchuk
	Art Unit	1737
	Examiner Name	
	Attorney Docket Number	PM07027D1CIP1C6

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	2	2011035228	JP	A	2011-02-17	TOSHIBA CORP		
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Signature	/Michael L. Bartholomew/	Date (YYYY-MM-DD)	2021-08-18
Name/Print	Michael L. Bartholomew	Registration Number	60225

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Doc description: Information Disclosure Statement (IDS) Filed

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	Examiner Name	Not Yet Assigned
	Attorney Docket Number	PM07027D1CIP1C6

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	1	20080293255	A1	2008-11-27	Krishnaswamy Ramkumar		
	2	20080296664	A1	2008-12-04	Ramkumar et al.		
	3	20090011609	A1	2009-01-08	Ramkumar et al.		
	4	20090039414	A1	2009-02-12	Lue et al.		
	5	20090039416	A1	2009-02-12	Lai et al.		

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Examiner Name	Not Yet Assigned
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6	20090045452	A1	2009-02-19	Lue et al.
7	20090065849	A1	2009-03-12	Kosei Noda
8	20090152618	A1	2009-06-18	Matsuo et al.
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15	20090294836	A1	2009-12-03	Masahiro Kiyotoshi
16	20090294844	A1	2009-12-03	Tanaka et al.

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17	20090302365	A1	2009-12-10	Arup Bhattacharyya
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24	20100178759	A1	2010-07-15	Kim et al.
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26	20100270609	A1	2010-10-28	Olsen et al.
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28	20100295118	A1	2010-11-25	Arup Bhattacharyya
29	20110018053	A1	2011-01-27	Lo et al.
30	20110163371	A1	2011-07-07	Song et al.
31	20110233512	A1	2011-09-29	Yang et al.
32	20110237060	A1	2011-09-29	Lee et al.
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34	20120007167	A1	2012-01-12	Hung et al.
35	20120061744	A1	2012-03-15	Hwang et al.
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37	20120068250	A1	2012-03-22	Ino et al.
38	20130175604	A1	2013-07-11	Polishchuk et al.

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	39	20130309826	A1	2013-11-21	Ramkumar et al.	
	40	20140264551	A1	2014-09-18	Polishchuk et al.	
	41	20160300724	A1	2016-10-13	Levy et al.	
	42	20180366563	A1	2018-12-20	Levy et al.	

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Name/Print	Michael L. Bartholomew	Registration Number	60225

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	1	20060255399	A1	2006-11-16	Kim et al.		
	2	20060180851	A1	2006-08-17	SAMSUNG ELECTRONICS CO LTD		
	3	20080173928	A1	2008-07-24	Arai et al.		
	4	20120068255	A1	2012-03-22	SAMSUNG ELECTRONICS CO LTD		
	5	20080093661	A1	2008-04-24	HYNIX SEMICONDUCTOR INC [KR]		

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	6	20070158736	A1	2007-07-12	KABUSHIKI KAISHA TOSHIBA	
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17157350
Filing Date	2021-01-25
First Named Inventor	Igor Polishchuk
Art Unit	1737
Examiner Name	
Attorney Docket Number	PM07027D1CIP1C6

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Michael L. Bartholomew/	Date (YYYY-MM-DD)	2021-08-02
Name/Print	Michael L. Bartholomew	Registration Number	60225

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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	2	4395438	A	1983-07-26	Ping-Wang Chiang	
	3	4490900	A	1985-01-01	Te-Long Chiu	
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Application Number	17157350
Filing Date	2021-01-25
First Named Inventor	Igor Polishchuk
Art Unit	1737
Examiner Name	Not Yet Assigned
Attorney Docket Number	PM07027D1CIP1C6

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Michael L. Bartholomew/	Date (YYYY-MM-DD)	2021-05-25
Name/Print	Michael L. Bartholomew	Registration Number	60225

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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To: docket@kba.law,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
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Jul 20, 2022 04:53:56 AM

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Salt Lake City, UT 84101
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Application	Document	Mailroom Date	Attorney Docket No.
17157350	NOA	07/20/2022	PM07027D1CIP1C6
	1449	07/20/2022	PM07027D1CIP1C6
	1449	07/20/2022	PM07027D1CIP1C6
	1449	07/20/2022	PM07027D1CIP1C6
	1449	07/20/2022	PM07027D1CIP1C6

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

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Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

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36491 7590 07/20/2022
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Michael L. Bartholomew	(Typed or printed name)
/Michael L. Bartholomew/	(Signature)
2022-08-17	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/157,350	01/25/2021	Igor Polishchuk	PM07027D1CIP1C6	6135

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	10/20/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 Kunzler Bean & Adamson

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

LONGITUDE FLASH MEMORY SOLUTIONS LTD. Dublin, IRELAND

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

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5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29☐ Applicant asserting small entity status. See 37 CFR 1.27☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Michael L. Bartholomew/

Date 2022-08-17

Typed or printed name Michael L. Bartholomew

Registration No. 60225

Electronic Patent Application Fee Transmittal				
Application Number:		17157350		
Filing Date:		25-Jan-2021		
Title of Invention:		MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
First Named Inventor/Applicant Name:		Igor Polishchuk		
Filer:		Michael Lee Bartholomew/Mary Keshishian		
Attorney Docket Number:		PM07027D1CIP1C6		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	46428489
Application Number:	17157350
International Application Number:	
Confirmation Number:	6135
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	36491
Filer:	Michael Lee Bartholomew
Filer Authorized By:	
Attorney Docket Number:	PM07027D1CIP1C6
Receipt Date:	17-AUG-2022
Filing Date:	25-JAN-2021
Time Stamp:	13:24:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$1200
RAM confirmation Number	E20228GD25103108
Deposit Account	
Authorized User	

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Fee-Transmittal_PM07027D1CIP1C6.pdf	85307	no	1
			99ee734e025d99afe0bac4e7f055852678783572		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	38058	no	2
			9fab5e82608861448e3d44a3be34fc26e1150427		
Warnings:					
Information:					
Total Files Size (in bytes):			123365		
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17157350
Filing Date	2021-01-25
First Named Inventor	Igor Polishchuk
Art Unit	1737
Examiner Name	
Attorney Docket Number	PM07027D1CIP1C6

Change(s) applied

to document, /J.T./ 7/28/2022	6	20070158736	A1	2007-07-12	~~KABUSHIKI KAISHA TOCHIBA~~ Arai et al.
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If you wish to add additional U.S. Published Application citation information please click the Add button. **FOREIGN PATENT DOCUMENTS**

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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Examiner Signature	/NIKOLAY K YUSHIN/	Date Considered	06/23/2022
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0851-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17157350
	Filing Date	2021-01-25
	First Named Inventor	Igor Polishchuk
	Art Unit	1737
	Examiner Name	
	Attorney Docket Number	PM07027D1CIP1C6

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Change(s) applied to document, /J.T./ 7/28/2022	1	20060255399	A1	2006-11-16	Kim et al.	
	2	20060180851	A1	2006-08-17	~~SAMSUNG ELECTRONICS CO LTD~~ Lee et al.	
	3	20080173928	A1	2008-07-24	Arai et al.	
	4	20120068255	A1	2012-03-22	~~SAMSUNG ELECTRONICS CO LTD~~ Lee et al.	
	5	20080093661	A1	2008-04-24	~~HYNIX SEMICONDUCTOR INC (KR)~~ Joo et al.	



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/157,350	09/27/2022	11456365	PM07027D1CIP1C6	6135

36491 7590 09/07/2022
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 117 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional inventors):

Igor Polishchuk, Fremont, CA;
Sagy Charel Levy, Zichron Yaakov, ISRAEL;
Krishnaswamy Ramkumar, San Jose, CA;

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

LONGITUDE FLASH MEMORY SOLUTIONS LTD., Dublin, IRELAND

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To: docket@kba.law,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 36491

Sep 08, 2022 03:27:04 AM

Dear PAIR Customer:

Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101
UNITED STATES

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17157350	ISSUE.NTF	09/07/2022	PM07027D1CIP1C6

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