

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Sandisk Technologies, Inc.,
Petitioner,

v.

Longitude Flash Memory Solutions Ltd.,
Patent Owner.

Case No. IPR2025-01281

U.S. Patent No. 11,456,365

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,456,365**

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 11,456,365 to Polishchuk et al. (“the ’365 patent”)
1002	Certified Prosecution file history for the ’365 patent (“Prosecution History”)
1003	Declaration of Jack C. Lee
1004	U.S. Patent Application Publication No. 2012/0068255 to Changhyun Lee, et al. (“Lee ’255”)
1005	Korean Patent Publication No. 2011-0118961 to Gi Hong Lee et al. and Certified English Translation of Korean Patent Publication No. 2011-0118961 to Gi Hong Lee et al. (“Lee ’961”)
1006	U.S. Patent Application Publication No. 2006/0065919A1 to Ichiro Fujiwara (“Fujiwara”)
1007	L. Lukasiak and A. Jakubowski, <i>History of Semiconductors</i> , Journal of Telecommunications and Information Technology, Vol. 3 (2010) (“Lukasiak”)
1008	U.S. Patent No. 4,203,158 to Dov Frohman-Bentchkowsky, et al. (“Frohman-Bentchkowsky”)
1009	U.S. Patent Application Publication No. 2006/0255399 to Ju-Hyung Kim, et al. (“Kim ’399”)
1010	U.S. Patent Application Publication No. 2003/0122204 to Kazumasa Nomoto, et al. (“Nomoto”)
1011	U.S. Patent Application Publication No. 2009/0179253 to Levy, et al. (“Levy”)
1012	U.S. Patent Application Publication No. 2011/0045647 to Jin-Hwa Heo, et al. (“Heo”)
1013	U.S. Patent Application Publication No. 2011/0281429 to Udayan Ganguly, et al. (“Ganguly”)
1014	U.S. Patent Application Publication No. US 2006/0113586 to Szu-Yu Wang (“Wang ’586”)

Exhibit No.	Description
1015	U.S. Patent No. 6,897,533 to Jean Yee-Mei Yang, et al. (“Yang ’533”)
1016	U.S. Patent Application Publication No. 2006/0198189 to Hang-Ting Lue, et al. (“Lue ’189”)
1017	U.S. Patent Application Publication No. 2009/0059676 to Shen Chih Lai, et al. (“Lai ’676”)
1018	Erh-Kun Lai, et al., <i>A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory</i> , Proceedings of the 2006 International Electron Devices Meeting (IEEE Dec. 2006) (“Lai Article”)
1019	U.S. Patent Application Publication No. 2005/0006696A1 to Mitsuhiro Noguchi, et al. (“Noguchi”)
1020	Antonio Arreghini, et al., <i>Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells</i> , IEEE Transactions on Electron Devices, Vol. 55, No. 5 (May 2008) (“Arreghini”)
1021	U.S. Patent Application Publication No. 2010/0157680A1 to Masaaki Higuchi, et al. (“Higuchi”)
1022	U.S. Patent Application Publication No. 2008/0128790 to Jin-Hyo Jung (“Jung”)
1023	U.S. Patent Application Publication No. 2003/0198106 to Jeong-Hyuk Choi (“Choi”).
1024	U.S. Patent Application Publication No. 2009/0026460 to Tien-Fan Ou, et al. (“Ou”)
1025	Falong Zhou, et al., <i>VNDROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications</i> , Proceeding of 2006 European Solid-State Device Research Conference (IEEE Sept. 2006) (“VDNROM”)
1026	H. Tanaka, et al., <i>Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory</i> , 2007 IEEE Symposium on VLSI Technology (June 2007) (“Tanaka”)

Exhibit No.	Description
1027	Toshiba Press Release, Toshiba Develops New NAND Flash Technology (June 12, 2007) (“Toshiba PR”)
1028	U.S. Patent Application Publication No. 2010/0178759A1 to JinGyun Kim, et al. (“Kim ’759”)
1029	Moon Kyung Kim, et al., <i>A Comparison of N+ Type and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories</i> , Material Research Society Symposium Proceedings, Vol. 997 (MRS 2007) (“Kim Article”)
1030	U.S. Patent Application Publication No. 2006/0118858 to Sang-hun Jeon (“Jeon”)
1031	U.S. Patent Application Publication No. 2005/0237809 to Yen-Hao Shih, et al. (“Shih”)
1032	U.S. Patent Application Publication No. 2012/0276696 to Jun-Kyu Yang, et al. (“Yang ’696”)
1033	U.S. Patent Application Publication No. 2013/0270625 to Byong-hyun Jang, et al. (“Jang”)
1034	U.S. Patent Application Publication No. 2012/0068247 to Changhyun Lee, et al. (“Lee ’247”)
1035	U.S. Patent Application Publication No. 2012/0299086 to Jaegoo Lee (“Lee ’086”)
1036	U.S. Patent Application Publication No. 2011/0316064 to Jung Ho Kim, et al. (“Kim ’064”)
1037	U.S. Provisional Application No. 60/940,160 (“’160 Provisional App.”)
1038	Prosecution file history for the ’434 patent (U.S. Application No. 12/152,518) (“’434 Pros. Hist.”)
1039	Prosecution file history for the ’374 patent (U.S. Application No. 13/288,919) (“’374 Pros. Hist.”)
1040	Prosecution file history for the ’537 patent (U.S. Application No. 13/539,466) (“’537 Pros. Hist.”)
1041	U.S. Patent No. 6,912,163 to Wei Zheng, et al. (“Zheng”)

Exhibit No.	Description
1042	S.M. Sze and K. Ng, <i>Physics of Semiconductor Devices</i> (3 rd Ed. Wiley-Interscience 2007) (“Sze”)
1043	U.S. Patent Application Publication No. 2010/0019312 to Katsuyuki Sekine, et al. (“Sekine”)
1044	U.S. Patent No. 7,450,423 to Erh-Kun Lai, et al. (Lai ’423)
1045	Declaration of June Munford
1046	IEEE Declaration of Gordon MacPherson

Petitioner respectfully requests that the Board institute *inter partes* review and cancel claims 1-3, 5-12, 14-23, and 25-45 (the “Challenged Claims”) of U.S. Patent No. 11,456,365 (the ’365 patent).

I. TECHNICAL BACKGROUND

The ’365 patent is directed generally to non-volatile memory (or “NVM”), which is a type of computer memory that can retain stored information even after power is removed. Ex. 1001 (’365 patent), 1:32-36; Ex. 1003, ¶¶42-43. More specifically, the ’365 patent purports to improve the data retention capabilities of silicon–oxide–nitride–oxide–silicon (“SONOS”) flash memory devices. Ex. 1001 (’365 patent), 2:5-14, 2:45-57; Ex. 1003, ¶¶18-19, 50. As discussed below, SONOS-type flash memory devices were well-known at the time of the application for the ’365 patent.

A. Floating Gate Flash Memory

Flash memory is a type of semiconductor NVM that was invented in the 1980s. Ex. 1003, ¶44. Early flash memory devices were based on a “floating gate” metal–oxide–semiconductor field-effect transistor (MOSFET) design. *Id.*, ¶45. The design included an electrically insulated gate that “floats” between two oxide layers, as shown here:

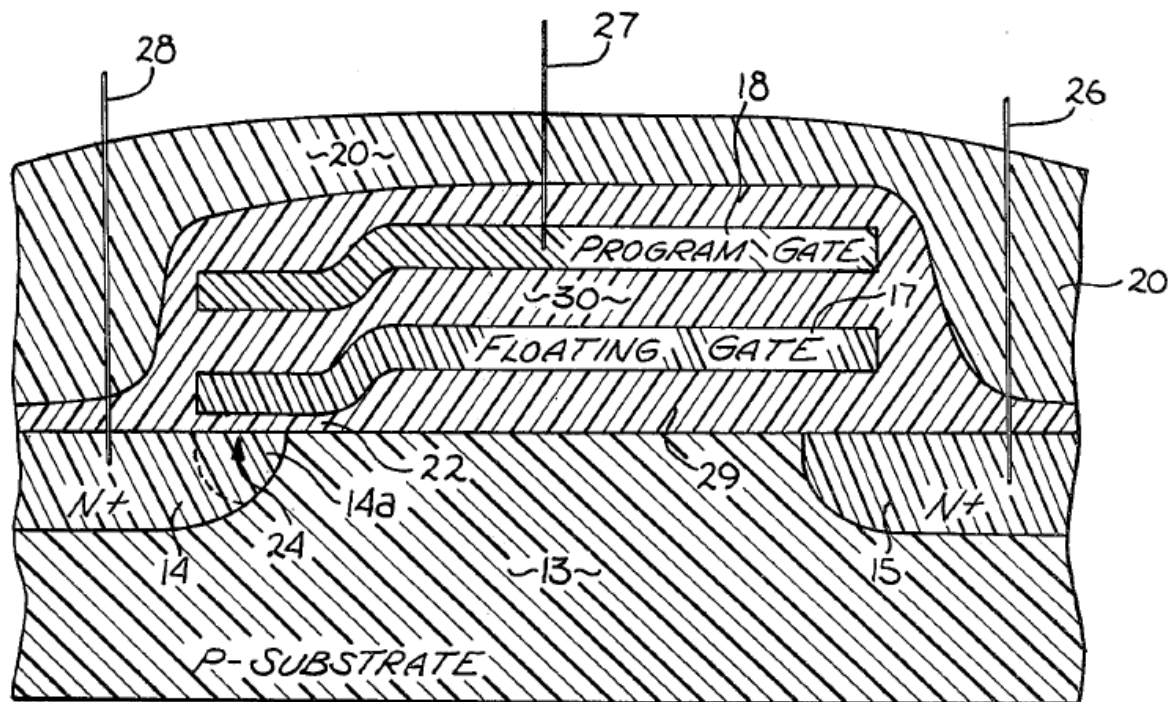
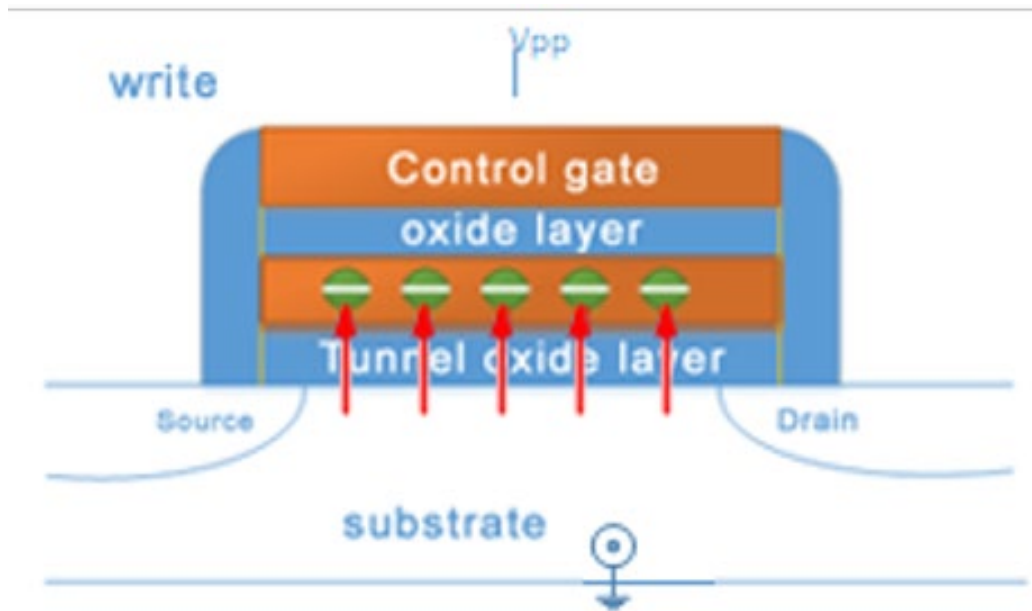


Fig. 1

Ex. 1008 (Frohman-Bentchkowsky), Fig. 1; *see also id.*, 4:1-31; Ex. 1003, ¶45.

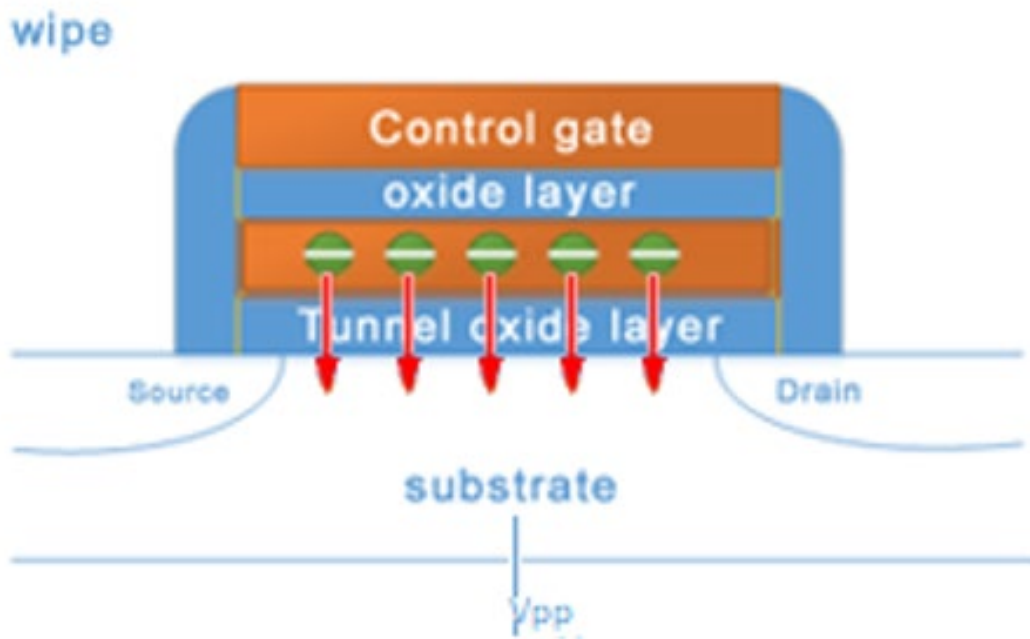
Because the floating gate is electrically isolated, any electron placed in the gate will be trapped there after voltage is removed. *See, e.g.*, Ex. 1008 (Frohman-Bentchkowsky), 1:18-23, 3:55-57, 5:5-7; Ex. 1003, ¶46. This allows a floating gate transistor to function as NVM. In the simplest example, the presence of sufficient electrons in the floating gate will cause the memory to be read as a “1,” while the absence of electrons in the floating gate will cause the memory to be read as a “0.” *Id.*, 1:20-23.

During a program/write operation, electrons can be placed in the floating gate using a “tunneling” procedure, where an electric field is applied that causes electrons from the substrate to “tunnel” through an oxide layer to the floating gate:



Ex. 1003, ¶47.

During an erase/wipe operation, the opposite electric field is applied, causing the electrons trapped in the control gate to “tunnel” back to the substrate:

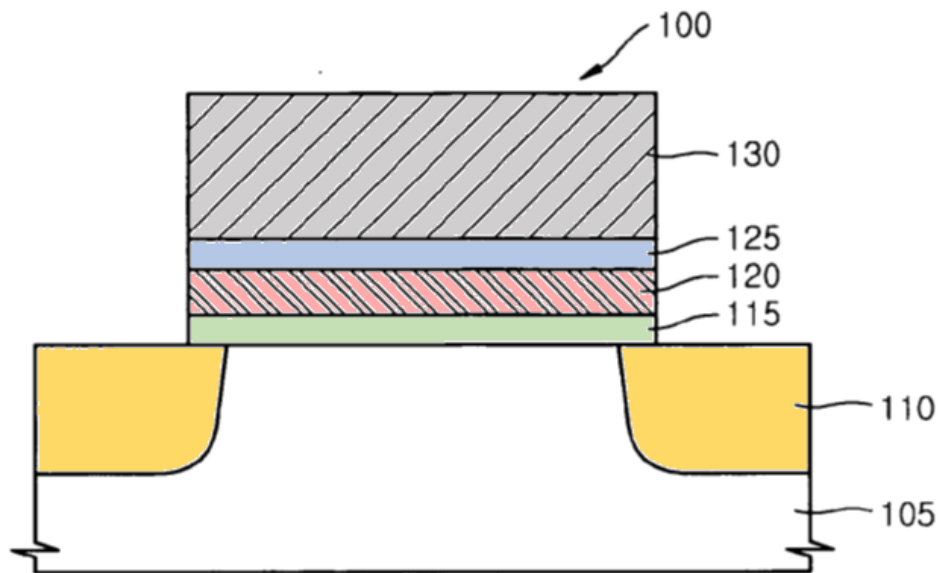


Ex. 1003, ¶48.

B. SONOS-Type Flash Memory

By the early 2000s, flash memory devices were commonly designed to use charge-trapping SONOS technology. *See, e.g.,* Ex. 1010 (Nomoto), Fig. 3H, [0032]-[0038]; Ex. 1003, ¶49. As noted above, “SONOS” is a reference to the layers of the NVM device: silicon-oxide-nitride-oxide-silicon. SONOS-type flash memory is similar to floating gate memory except that a non-conductive silicon nitride layer is used to trap charges rather than the floating gate. Ex. 1003, ¶50. An example of a “conventional” SONOS memory device is provided in Kim ’399 (Ex. 1009), which was filed on February 15, 2006:

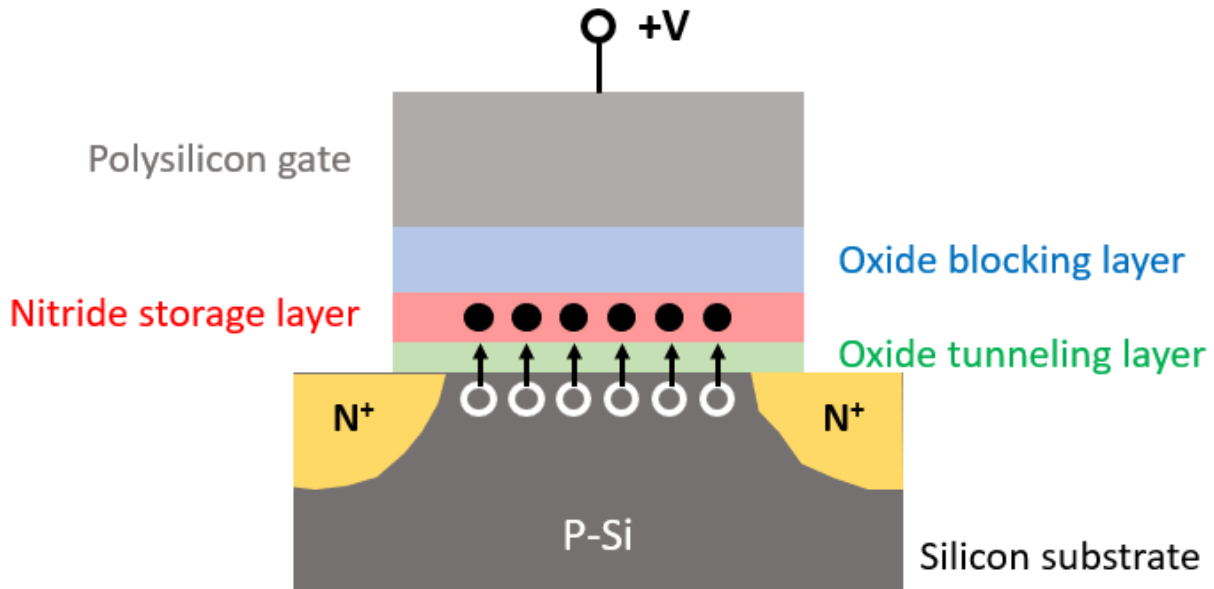
FIG. 1 (CONVENTIONAL ART)



Ex. 1009 (Kim '399), Fig. 1, [0006]-[0008].

As reflected above, a conventional SONOS memory device in 2006 included: (i) silicon semiconductor substrate 105 with source/drain regions 110; (ii) oxide tunnel insulating film 115 (green); (iii) nitride charge trapping film 120 (red); (iv) silicon oxide blocking insulating film 125 (blue); and (v) silicon control gate 130 (gray). Ex. 1003, ¶¶50-51.

Like floating gate memory, SONOS charge trap memory transistors work by “tunneling” electrons into and out of the nitride charge trapping layer. Ex. 1003, ¶52. During a programming step, a positive voltage is applied to the gate, which causes electrons from the substrate to tunnel through the tunnel oxide and into the nitride storage layer:



Ex. 1003, ¶52.

When the voltage is removed, the electrons remain in the nitride storage layer. Ex. 1003, ¶52. To perform an erase/clear step, a negative voltage is applied to the gate, which causes electrons to tunnel from the nitride storage layer back through the tunnel oxide into the silicon substrate. *Id.*, ¶53.

C. Well-Known Configurations of SONOS-Type Flash Memory

Prior to July 2012, a person of ordinary skill in the art (a “POSITA”) would have been familiar with several routine configurations of SONOS-type flash memory devices and the predictable benefits of those configurations. *See* Ex. 1003, Parts III.C.4-8. For example, a POSITA would have been familiar with:

- Configuring SONOS devices to include multiple charge storage layers, such as SONNOS configurations. Ex. 1003, ¶¶54-60 (discussing Ex.

- 1011 (Levy), Ex. 1010 (Nomoto), Ex. 1012 (Heo), Ex. 1009 (Kim '399), Ex. 1013 (Ganguly), and Ex. 1014 (Wang '586)).
- Configuring SONOS devices to include an intermediate oxide layer between two nitride layers, such as SONONOS configurations. Ex. 1003, ¶¶61-66 (discussing Ex. 1016 (Lue '189), Ex. 1015 (Yang '533), Ex. 1017 (Lai '676), Ex. 1018 (Lai Article), Ex. 1019 (Noguchi), and Ex. 1020 (Arreghini)).
 - Using high work function materials for the gate electrodes of SONOS/SONNOS/SONONOS devices. Ex. 1003, ¶¶82-84 (discussing Ex. 1029 (Kim Article), Ex. 1016 (Lue '189), Ex. 1017 (Lai '676), Ex. 1012 (Heo), Ex. 1030 (Jeon), and Ex. 1031 (Shih)).
 - Arranging SONOS/SONNOS/SONONOS devices to have vertical configurations. Ex. 1003, ¶¶67-81 (discussing Ex. 1021 (Higuchi), Ex. 1028 (Kim '759), Ex. 1023 (Choi), Ex. 1024 (Ou), Ex. 1022 (Jung), Ex. 1025 (VDNROM), Ex. 1026 (Tanaka), and Ex. 1027 (Toshiba PR)).
 - Fabricating SONOS/SONNOS/SONONOS devices using “gate-first” and “gate-last” methodologies. Ex. 1003, ¶¶85-97 (discussing Ex. 1028 (Kim '759), Ex. 1021 (Higuchi), Ex. 1032 (Yang '696), Ex. 1033 (Jang), Ex. 1034 (Lee '247), Ex. 1035 (Lee '086), and Ex. 1036 (Kim '064)).

II. THE '365 PATENT

A. Overview of Alleged Invention

The '365 patent issued on September 27, 2022 from an application filed on January 25, 2021. *See* Ex. 1001 ('365 patent), p. 1. The '365 patent purports to

improve the data retention capabilities of SONOS memory devices using an “oxide-nitride-nitride-oxide (ONNO) stack” with a “multi-layer charge-trapping region.” Ex. 1001 (’365 patent), 2:5-14, 2:45-57; Ex. 1003, ¶¶18-19, 49. Figure 4A, annotated below, depicts one embodiment of the ONNO stack of the ’365 patent:

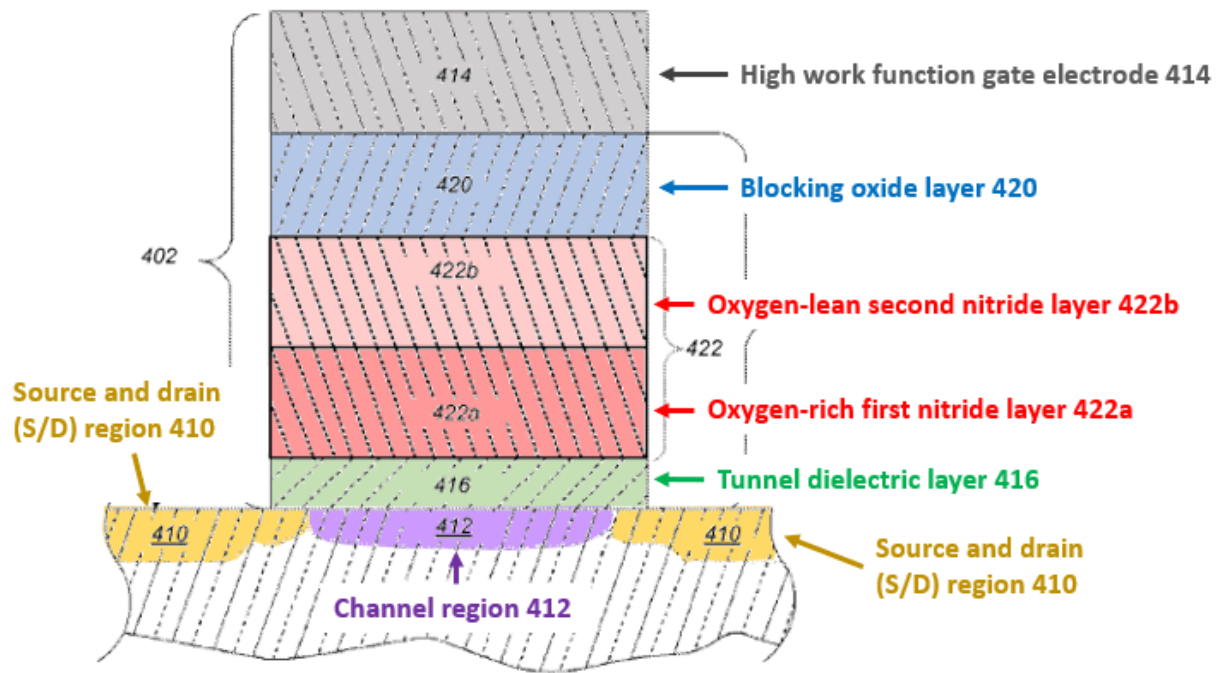


FIG. 4A

Ex. 1001 (’365 patent), Fig. 4A; *see also* Ex. 1003 ¶¶20-21.

Figure 4A includes “one or more diffusion regions 410” (gold) that are “separated by a channel region 412” (purple). Ex. 1001 (’365 patent), 8:59-62; Ex. 1003, ¶22. In this figure, the ONNO stack is aligned above the channel region in a horizontal configuration. *Id.* The stack includes “tunnel dielectric layer 416”

(green), “multi-layer charge trapping region 422” (red), “blocking dielectric layer 420” (blue), and “high work function gate electrode 414” (gray). Ex. 1001 (’365 patent), 8:52-10:15; Ex. 1003, ¶22.

The ’365 patent further states that the ONNO stack may be modified to have an intermediate oxide layer between the two nitride layers, forming an ONONO structure. Ex. 1001 (’365 patent), Fig. 4B, 10:8-15; Ex. 1003, ¶24. An example of this configuration, with the intermediate oxide layer annotated in orange, is shown in figure 4B:

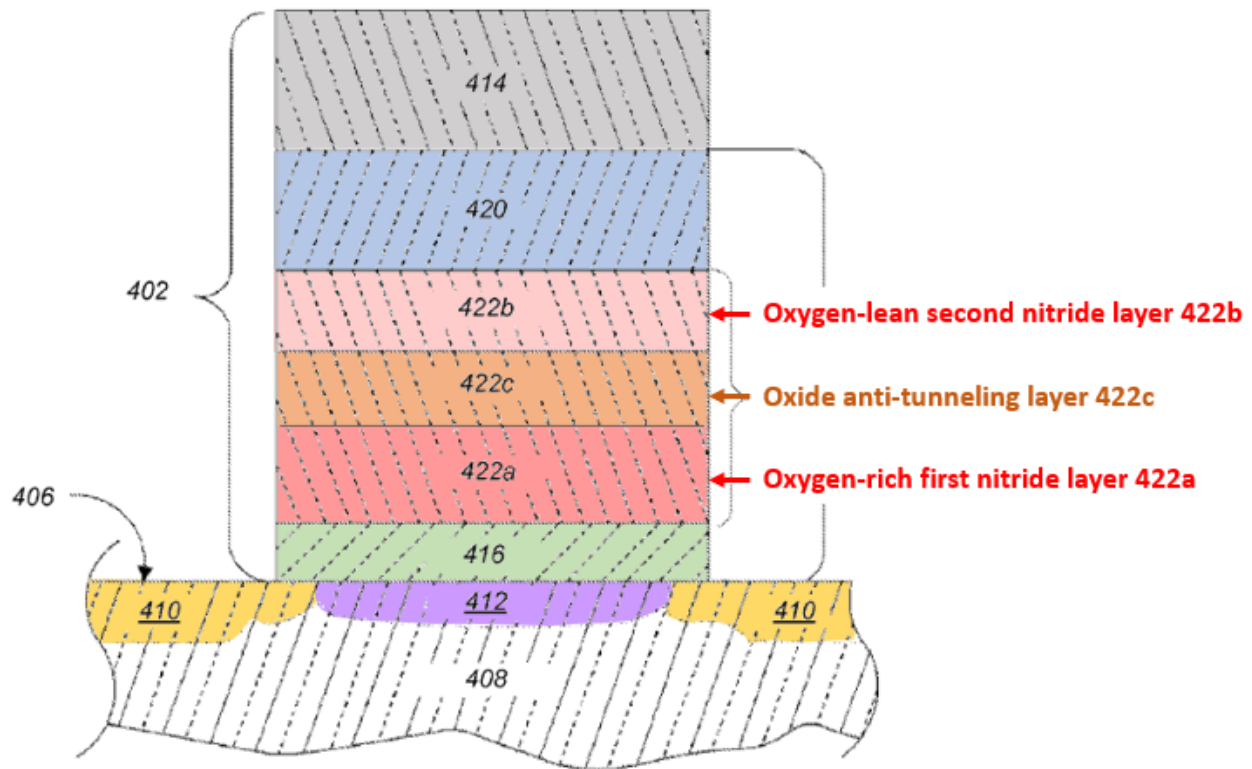
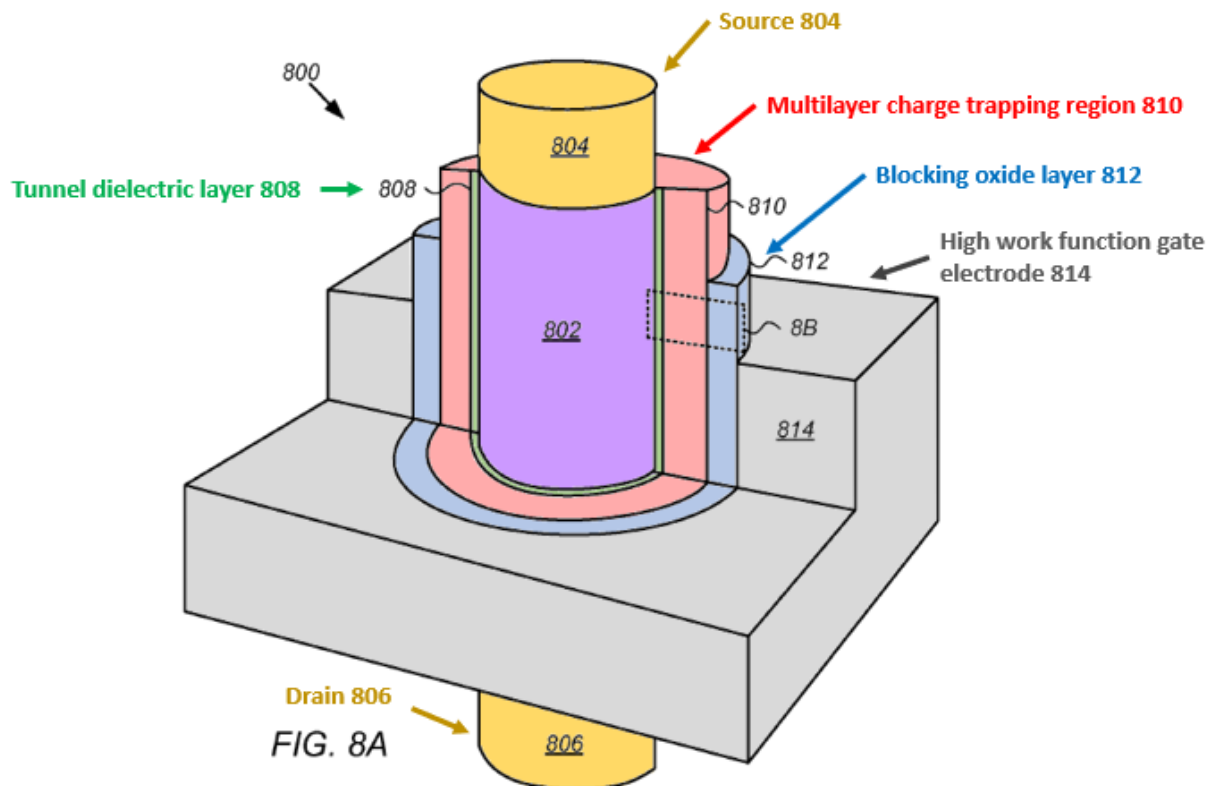


FIG. 4B

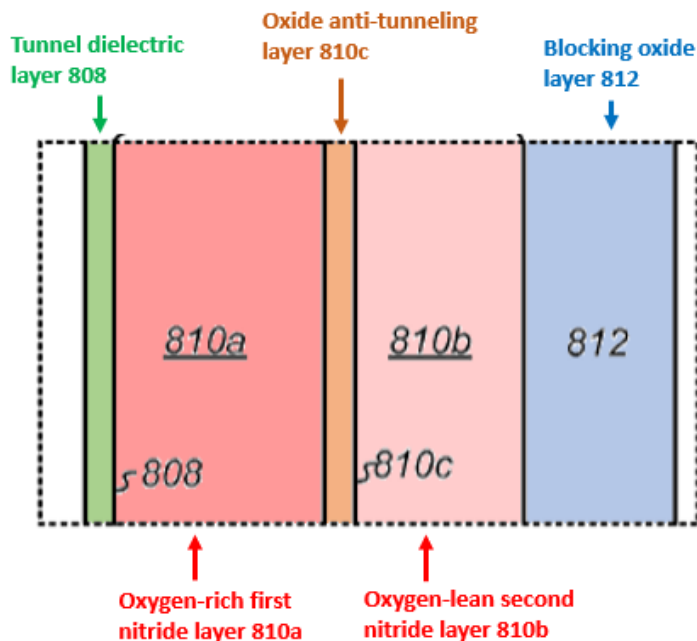
Ex. 1001 (’365 patent), Fig. 4B; Ex. 1003, ¶24.

While figures 4A and 4B depict horizontally-oriented memory transistors, the '365 patent states that there are alternative implementations of the ONNO (or ONONO) stack. Ex. 1001 ('365 patent), 8:51-20:7; Ex. 1003, ¶¶26-29. For example, figures 8A and 8B are directed to a vertically-oriented (“three-dimensional” or “3D”) memory transistor structure with an ONONO stack. Ex. 1001 ('365 patent), Figs. 8-10, 17:17-20:7; Ex. 1003, ¶¶30-31. Figure 8A shows a transistor with a channel region (purple) that extends vertically between diffusion regions (gold):



Ex. 1001 ('365 patent), Fig. 8A, 17:17-18:14; Ex. 1003, ¶30.

Figure 8B depicts a magnified view of the cross section of the ONONO stack from figure 8A:



Ex. 1001 ('365 patent), Fig. 8B, 17:55-63; ¶¶32-33.

Figures 9 and 10 depict methods of fabricating vertical channel memory devices, including a “gate first” method (figure 9) and “gate last” method (figure 10). Ex. 1001 ('365 patent), 3:36-38, 18:15-19:19; Ex. 1003, ¶¶34-35.

As discussed below, the Challenged Claims are each directed to vertically-oriented SONOS-type memory transistors or methods of fabricating the same.

B. Prosecution History

Igor Polishchuk, Sagy Charel Levy, and Krishnaswamy Ramkumar (collectively, “the Applicants”) filed the application for the '365 patent on January 25, 2021 with only one claim. Ex. 1002 (Pros. Hist.), 000065-78. Subsequently,

the Applicants submitted information disclosure statements listing more than 300 prior art references (*id.*, 001802-11, 001898-1947) and amended the application to replace original claim 1 with new claims 2-46 (*id.*, 001856-64). The Examiner allowed application claims 2-46 without rejection. Ex. 1002 (Pros. Hist.), 001871-79. The Examiner did not explicitly compare the limitations of claims 2-46 to any specific prior art reference. *See generally id.* In providing the reasons for allowance, the Examiner stated the following elements were absent from the prior art:

- “[F]orming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate; forming on sidewalls of the opening a blocking dielectric layer; forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region; forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.” Ex. 1002 (Pros. Hist.), 1877 (regarding issued claim 1).
- “[F]orming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layer.” *Id.* (regarding issued claim 23).
- “[A] semiconductor memory device, comprising a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer

charge storing region formed in a substantially annular shape, a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and a gate electrode surrounding the blocking dielectric layer.” *Id.*, 16 (regarding issued claim 35); *see also* Ex. 1003, ¶¶37-41.

C. Priority Date

The earliest possible priority date for the Challenged Claims of the ’365 patent is **July 1, 2012**, the date of the filing of U.S. Patent Application No. 13/539,466, which issued as U.S. Patent No. 8,633,573.

On its face, the ’365 patent purports to claim priority to provisional patent application filed on May 25, 2007 through a chain of related applications represented in the following chart:

	App No.	Filing Date	Patent No.	Relationship
A	60/940,160	5/25/2007	n/a	
B	12/152,518	5/13/2008	8,063,434	
C	13/288,919	11/3/2011	8,859,374	Divisional of B
D	13/539,466	7/1/2012	8,633,537	Continuation-in-Part of C
E	14/159,315	1/20/2014	9,093,318	Continuation of D
F	14/811,346	7/28/2015	9,502,543	Continuation of E
G	15/335,180	10/26/2016	9,929,240	Continuation of F
H	15/864,832	1/8/2018	10,312,336	Continuation of G
I	16/429,464	6/2/2019	10,903,325	Continuation of H

	App No.	Filing Date	Patent No.	Relationship
J	17/157,350	1/25/2021	11,456,365	Continuation of I

Ex. 1001 ('365 patent), 1:8-29; Ex. 1003, ¶¶100-101.

To obtain the benefit of the filing date of the earlier related applications, the Challenged Claims must have written description support those applications. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010); *Augustine Med., Inc. v. Gaymar Indus., Inc.*, 181 F.3d 1291, 1302-03 (Fed. Cir. 1999) (“A CIP application contains subject matter from a prior application and may also contain additional matter not disclosed in the prior application. Different claims of such an application may therefore receive different effective filing dates.”). The written description support must have “sufficient detail that one skilled in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought.” *Anascope, Ltd. v. Nintendo of Am., Inc.*, 601 F.3d 1333, 1335 (Fed. Cir. 2010). The question is whether the subject matter is disclosed in the specification, not whether the subject matter would have been obvious. *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1571-1572 (Fed. Cir. 1997).

Here, every Challenged Claim requires a vertically oriented semiconductor memory device or a method of fabricating the same. Ex. 1003, ¶103. Claims 1 and 23 require forming “a vertical channel” or “an annular shaped vertical

channel,” respectively. Ex. 1001 (’365 patent), claims 1, 23. Claim 35 requires “a channel region oriented substantially perpendicular to the semiconductor substrate, the channel region formed in a substantially annular shape.” *Id.*, claim 35.

The three earliest applications in the priority chain of the ’365 patent—the ’160 Provisional Application (filed May 25, 2007), the ’518 Application (filed May 13, 2008), and the ’919 Application (filed November 3, 2011) (collectively, the “Earlier Applications”)—do not provide written description support for a vertical channel or a “channel region oriented substantially perpendicular to the semiconductor substrate.” *See* Ex. 1037 (’160 Provisional App.); Ex. 1038 (’434 Pros. Hist.); Ex. 1039 (’374 Pros. Hist.); Ex. 1003, ¶¶102, 104-106. Rather, the Earlier Applications exclusively disclose horizontally-oriented semiconductor devices. *See, e.g.*, Ex. 1038 (’434 Pros. Hist.), 000139; Ex. 1003, ¶105. The Applicants first added subject matter concerning vertically-oriented memory devices—e.g., figures 8-10 of the ’365 patent—on July 1, 2012 in connection with a continuation-in-part application that later issued as the ’537 patent. *See* Ex. 1040 (’537 Pros. Hist.), 000218-278; *compare id. with* Ex. 1038 (’434 Pros. Hist.), 000111-139; Ex. 1039 (’374 Pros. Hist.), 000158-199; Ex. 1003, ¶105.

Because features of the independent claims of the ’365 patent (claims 1, 23, and 35) are not disclosed in any of the Earlier Applications, the earliest possible priority date for the ’365 patent is July 1, 2012.

III. FIELD AND LEVEL OF ORDINARY SKILL

The '365 patent is in the field of non-volatile semiconductor memory. *See, e.g.,* Ex. 1001 ('365 patent), 1:31-36; Ex. 1003, ¶107. Each of the Challenged Claims is directed to either a “semiconductor memory device” (*see id.*, claim 35) or method of fabricating the same (*see id.*, claims 1, 23).

A POSITA in the relevant field as of July 1, 2012 would have had at least (1) a master's degree in electrical engineering, materials science, physics, or a related degree, and at least 3-5 years of experience in semiconductor devices and fabrication technologies; or (2) a bachelor's degree in electrical engineering, materials science, physics, or a related degree, and at least 5-6 years of experience in semiconductor devices and fabrication technologies. Ex. 1003, ¶¶108-109.

In view of the types of problems encountered in the art and prior art solutions to those problems, a POSITA in the relevant timeframe above would have been familiar with:

- Floating gate flash memory technology (*see* Ex. 1003, ¶¶44-48, 110);
- The structure and composition of SONOS-type memory devices (*see id.*, ¶¶40-53, 110);
- SONNOS and SONONOS configurations of SONOS-type memory devices (*see id.*, ¶¶54-66, 110);
- Vertically-oriented configurations of SONOS-type memory transistors, including 3D NAND structures (*see id.*, ¶¶67-81, 110);

- The use of high work function materials, such as p+ doped polysilicon, to form gate electrodes for SONOS-type memory devices (*see id.*, ¶¶82-84, 110); and
- Fabrication processes for both horizontal and vertical flash memories, including gate-first and gate-last methodologies (*see id.*, ¶¶85-97, 110).

IV. CLAIM CONSTRUCTION

A. “oxygen-rich nitride” and “oxygen-lean nitride”

Dependent claims 6-8, 25-27, 34, 38, 39, and 40 recite “oxygen-lean” and “oxygen-rich” nitride layers. The ’365 patent does not provide a general definition of these terms, but does provide an example of “oxygen-rich” and “oxygen-lean” in connection with the embodiment depicted in figure 6:

By oxygen-rich it is meant wherein a concentration of oxygen in the oxygen-rich first nitride layer 616a is from about 15 to about 40%, whereas a concentration of oxygen in [an] oxygen-lean second nitride layer 616b is less than about 5%.

Ex. 1001 (’365 patent), 13:57-31; Ex. 1003, ¶112.

Based on this statement, a POSITA would have understood that (i) a nitride layer with about 5% or less oxygen is within the bounds of “oxygen-lean”; and (ii) a nitride layer with about 15% or more oxygen is within the bounds of “oxygen-rich.” Ex. 1003, ¶113.

B. “high work function gate electrode”

Dependent claims 12, 31, and 37 of the '365 patent require “a high work function gate electrode.” This term was well-known to a POSITA prior to July 2012. Ex. 1003, ¶¶82-84, 114. The '365 patent uses “high work function gate electrode” according to its ordinary meaning: “[b]y high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased.” Ex. 1001 ('365 patent), 4:7-9. The '365 patent states that polysilicon doped with p-type impurities (e.g., boron) is an example of a high work function gate material. Ex. 1001 ('365 patent), 7:31-43; Ex. 1003, ¶115. Again, this is consistent with a POSITA's understanding of the term prior to July 2012. Ex. 1003, ¶¶115, 181-183; Ex. 1012 (Heo), [0046]; Ex. 1017 (Lai '676), [0067], [0072]; Ex. 1041 (Zheng), 5:36-37, 5:52-62.

A POSITA thus would have understood “high work function gate electrode” in the context of the '365 patent to have its ordinary meaning, which encompasses gate electrodes comprised of, for example, polysilicon doped with p-type impurities and other materials known as high work function materials. Ex. 1003, ¶¶116, 181-183; Ex. 1012 (Heo), [0046]; Ex. 1017 (Lai '676), [0067], [0072]; Ex. 1041 (Zheng), 5:36-37, 5:52-62.

C. “the [second] oxygen-rich nitride layer is formed on the inside sidewall of the [first] oxygen-lean nitride layer”

Claims 7, 26, and 40 require that “the [second] oxygen-rich nitride layer is formed on the inside sidewall of the [first] oxygen-lean nitride layer.” A POSITA would have understood, in the context of the ’365 patent, that “formed on” does not require direct contact. Ex. 1003, ¶117. Rather, an oxygen-rich layer may be “formed on” the inside sidewall of an oxygen-lean layer even when there is an intermediate oxide layer between the oxygen-rich layer and the oxygen lean layer. *Id.*

A POSITA would have understood this to be the proper construction of “formed on” in the context of the ’365 patent due to the claims of the ’365 patent—particularly the interaction of claims 26 and 27. Ex. 1003, ¶118. Claim 26 requires the oxygen-rich nitride layer to be “formed on” the sidewall of the oxygen-lean nitride layer. Ex. 1001 (’365 patent), claim 26. Claim 27 depends from claim 26 and further requires “forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.” *Id.*, claim 27. Taken together, a POSITA would understand that the oxygen-rich nitride layer can be both “formed on” the sidewall of the oxygen-lean nitride layer (claim 26) and, at the same time, have an anti-tunneling layer “between” the oxygen-rich and oxygen-lean nitride layers (claim 27). Ex. 1003, ¶118.

D. Dependent Claim 43

Claim 43 recites a semiconductor memory device, “wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer, wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer **by a sacrificial layer.**” Claim 43 thus recites a “stack of layers” that has both a “gate layer” and “sacrificial layer.” But the ’365 patent teaches that, in fabricating a memory device, sacrificial layers are replaced by gate material. Ex. 1001 (’365 patent), Fig. 10, 19:20-20:8; Ex. 1003, ¶120. Thus, a POSITA would have understood that the reference to “a sacrificial layer” in claim 43 is a typographical error and would have understood the wherein clause as follows: “wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the gate ~~a sacrificial~~ layer.” *Id.*

V. IDENTIFICATION OF CHALLENGE

A. Statutory Grounds

Petitioner requests *inter partes* review and cancelation of the Challenged Claims on the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1	1-3, 5, 9-12, 14-23, 28-33, 35-37, and 42-45	§ 103 Obviousness	Lee '255, Lee '961
2	6-8, 25-27, 34, 38-41	§ 103 Obviousness	Lee '255, Lee '961, Fujiwara

Under 35 U.S.C. § 103, a party may not obtain a patent “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious” to a POSITA at the time of the invention. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). “The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *Id.* As discussed below, the challenged claims of the ’365 patent are obvious under § 103.

B. Relied-Upon Prior Art¹

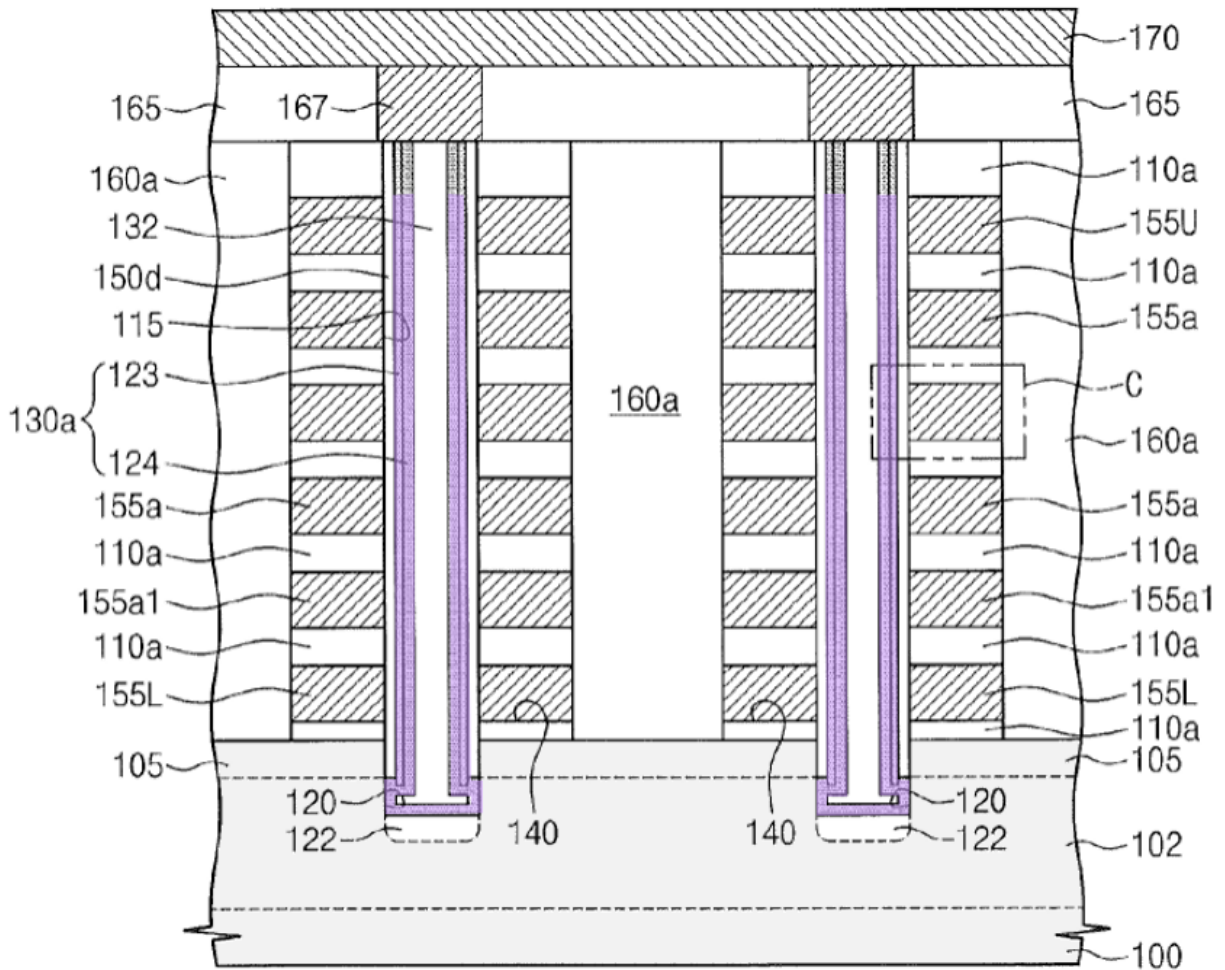
1. Lee ’255 (Ex. 1004)

Lee ’255 is a U.S. Patent Application Publication that was published on March 22, 2012 from an application filed on August 29, 2011. Ex. 1004 (Lee ’255), p.1. Lee ’255 is prior art under pre-AIA § 102(a) and §102(e) because the invention was described in a U.S. patent application that was filed and published before July 1, 2012. Ex. 1003, ¶122.

¹ Pre-AIA 35 U.S.C. §102 applies. *See* MPEP §2159.02.

Lee '255 was listed on an information disclosure statement submitted during prosecution of the '365 patent, along with more than 300 other prior art references. The Examiner, however, did not cite or apply Lee '255 in any Office Action, nor provide any substantive analysis of Lee '255 in allowing the claims of the '365 patent. Ex. 1003, ¶123.

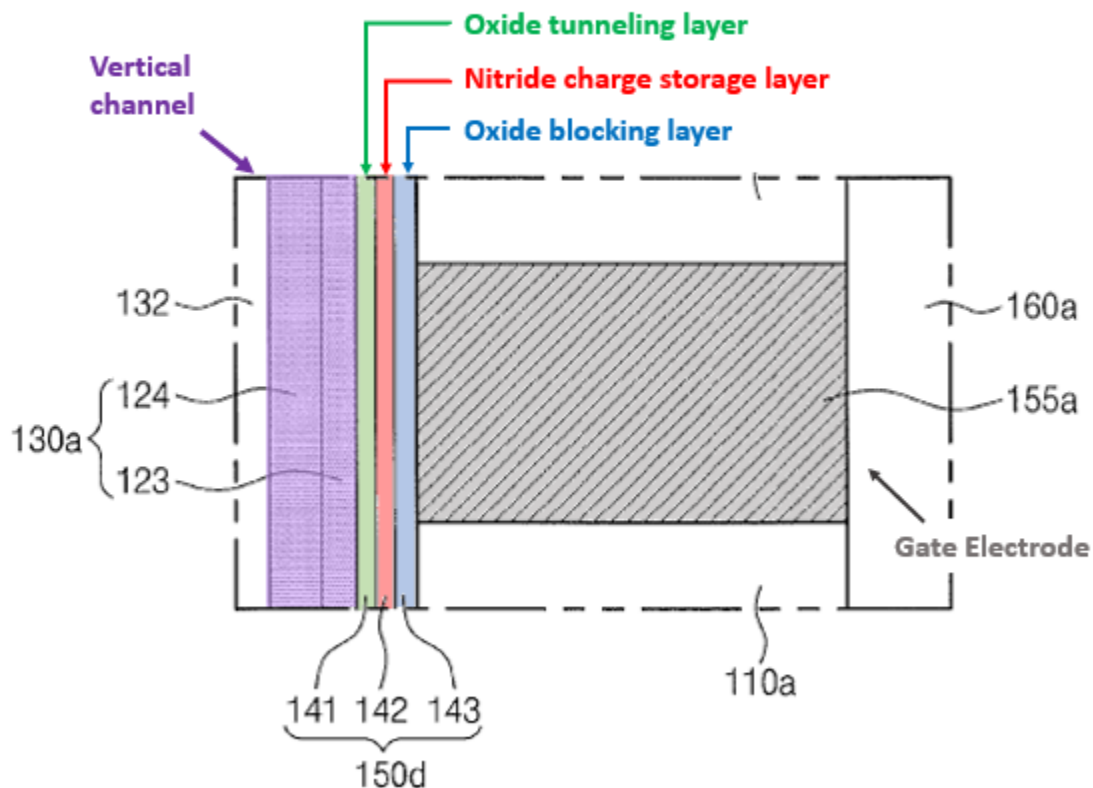
Lee '255 teaches “a three-dimensional (3D) semiconductor memory device” and method for fabricating the same. Ex. 1004 (Lee), [0002]-[0004]; Ex. 1003, ¶124. For example, figure 4A of Lee '255 depicts a 3D memory device with a vertical channel 130a (purple) that passes through a stack of layers (110a, 155L, 155a, 155U) formed over a substrate 100 (light gray):



Ex. 1004 (Lee '255), Fig. 4A, [0052]-[0054], [0063]; Ex. 1003, ¶124.

To store charges, Lee teaches an oxide-nitride-oxide gate dielectric layer 150d formed in an annular shape surrounding the vertical channel 130a. Ex. 1004 (Lee '255), Fig. 4B, 5A, [0057], [0074]; Ex. 1003, ¶125. The gate dielectric layer 150d includes an oxide tunneling layer 141 (green), a nitride charge storage layer 142 (red), and an oxide blocking layer 143 (blue), as shown in this annotated version of figure 4B:

Fig. 4B



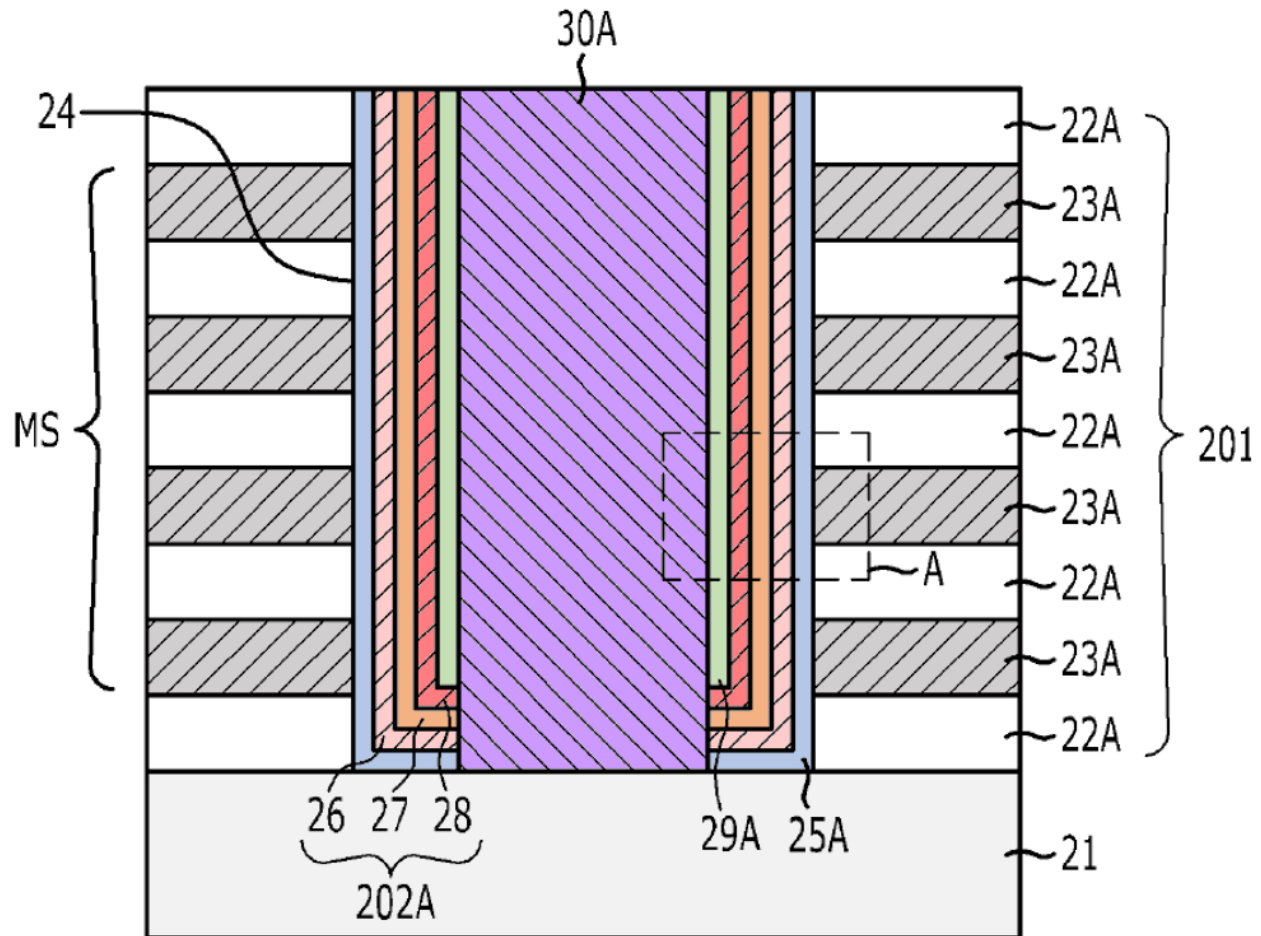
Ex. 1004 (Lee '255), Fig. 4B, [0057], [0074]; Ex. 1003, ¶125.

Lee '255 is analogous art to the '365 patent because it teaches improvements to NVM devices generally, and charge trap memory devices specifically. Ex. 1003, ¶126.

2. Lee '961 (Ex. 1005)

Lee '961 is a Korean Patent Publication. *See* Ex. 1005 (Korean language original and certified English translation of same). Lee '961 is prior art under pre-AIA § 102(a) because Lee '961 was published on November 2, 2011. Lee '961 was not cited or considered during prosecution of the '365 patent.

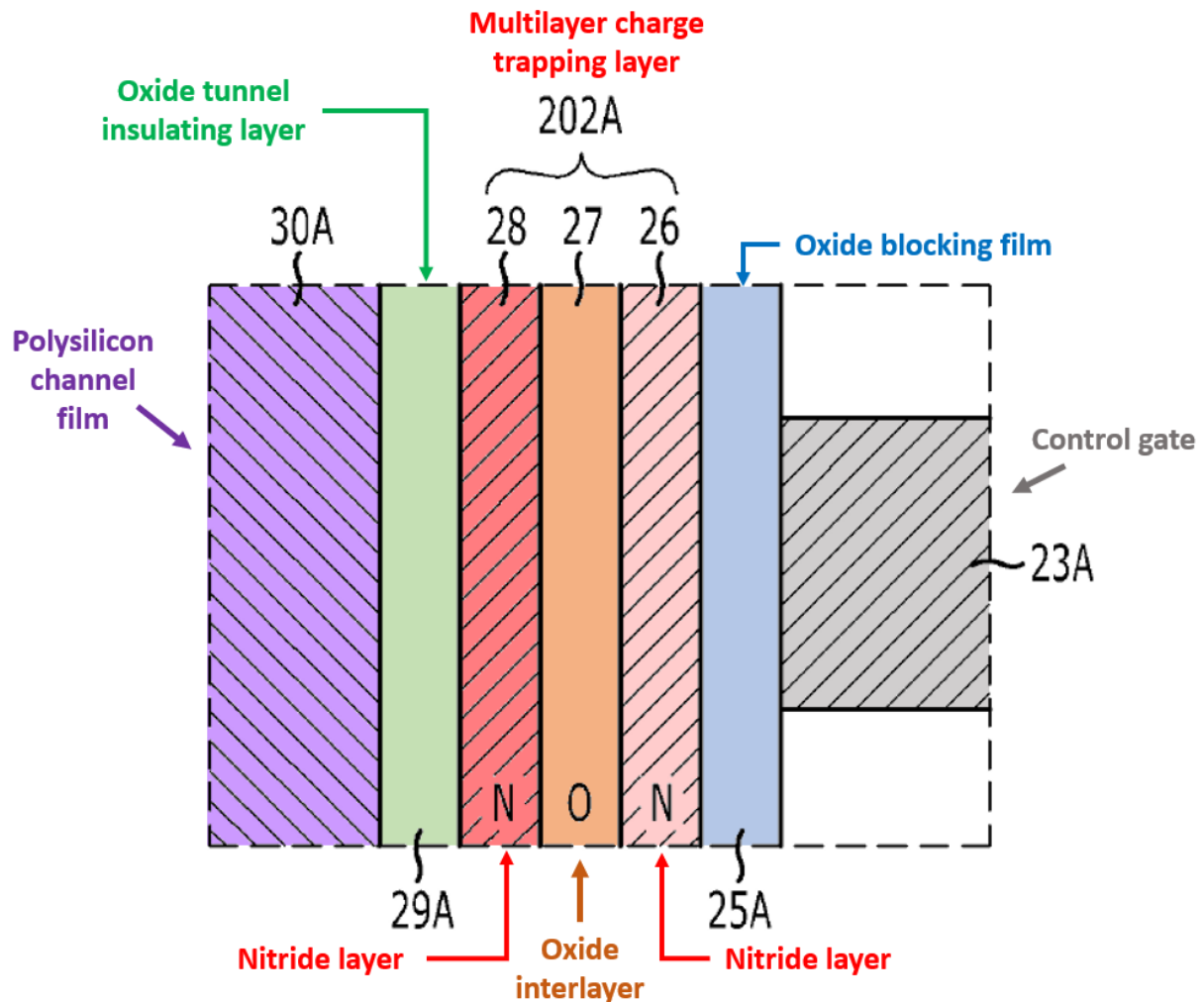
Lee '961 teaches a 3D charge trap memory device with a stack of layers (201) formed over a substrate (21) as shown in annotated figure 2a below. The stack includes alternating insulating layers (22A) and gate electrodes (23A):



Ex. 1005 (Lee '961), Fig. 2a, [0017]-[0019]; Ex. 1003, ¶129.

Lee '961 teaches a vertical 3D structure where a polysilicon channel is surrounded by oxide tunnel insulating layer 29A, multilayered charge trap layer 202A, and oxide blocking film 25A. Ex. 1005 (Lee '961), [0017]-[0019]; Ex.

1003, ¶130. As shown in annotated figure 2b below, multilayer charge trap layer 202A includes nitride layer 28, oxide interlayer 27, and nitride layer 26:



Ex 1005 (Lee '961), Fig. 2b, [0020]; Ex. 1003, ¶130.

Like Lee '255, Lee '961 is analogous art to the '365 patent because it teaches improvements to NVM devices generally, and charge trap memory devices specifically. Ex. 1003, ¶131.

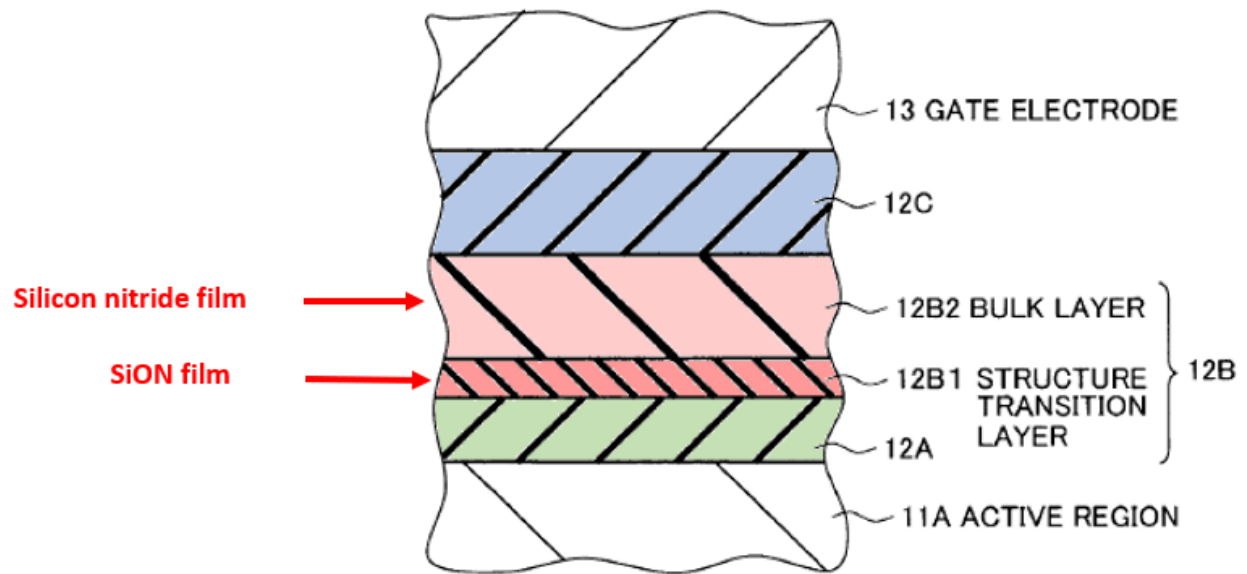
3. Fujiwara (Ex. 1006)

Fujiwara is a U.S. Patent Application Publication that was published on March 30, 2006 from an application filed on September 16, 2005. Ex. 1006 (Fujiwara), p. 1. Fujiwara is prior art under pre-AIA §102(b) because it was published more than one year before July 1, 2012. Ex. 1003, ¶132.

Fujiwara was listed on an information disclosure statement submitted during prosecution of the '365 patent, along with more than 300 other prior art references. The Examiner did not cite or apply Fujiwara in any Office Action, nor provide any substantive analysis of Fujiwara in allowing the claims of the '365 patent. Ex. 1003, ¶133.

Fujiwara teaches a charge-trapping memory transistor with multiple nitride layers. Ex. 1006 (Fujiwara), [0037]-[0038], [0197], [0220]; Ex. 1003, ¶¶134-135. Fujiwara teaches that a silicon nitride charge storage layer 12B can be made of two nitride layers—an upper silicon nitride (SiN_x) “bulk” layer 12B2 and a lower silicon oxynitride (SiON) “transition” layer 12B1:

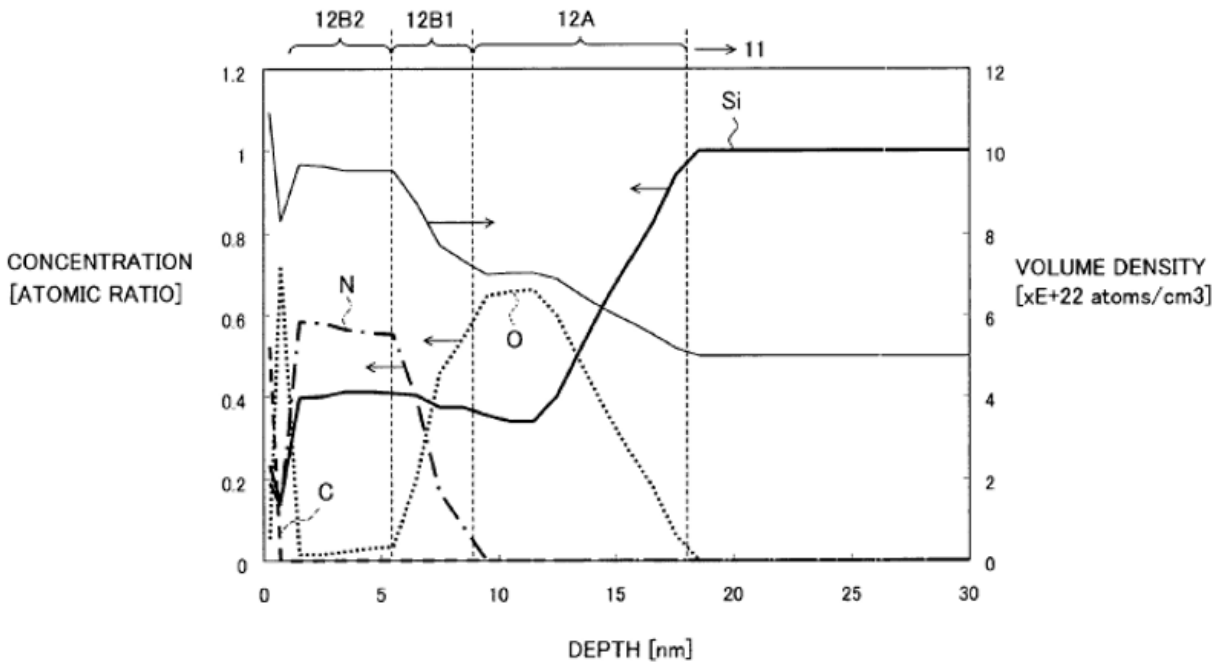
FIG. 21



Ex. 1006 (Fujiwara), Fig. 21, [0197]-[0208]; Ex. 1003, ¶136.

Fujiwara also teaches the relative oxygen (O), nitrogen (N), and silicon (Si) concentrations in each layer in figure 22:

FIG. 22



Ex. 1006 (Fujiwara), Fig. 22, [0200]; Ex. 1003, ¶137.

As reflected above, Fujiwara teaches that layer 12B2 is oxygen-lean (e.g., less than about 5% throughout its thickness), while layer 12B1 is oxygen-rich, with atomic concentrations reaching about 50%. Ex. 1006 (Fujiwara), Fig. 22, [0200]; Ex. 1003, ¶137.

As with Lee '255 and Lee '961, Fujiwara is analogous art to the '365 patent because it teaches improvements to NVM devices generally, and charge trap memory devices specifically.

VI. INVALIDITY GROUNDS

A. Ground 1: Obviousness over Lee '255 in view of Lee '961

A POSITA would have found claims 1-3, 5, 9-12, 14-23, 28-33, 35-37, and 42-45 of the '365 patent obvious over the teachings of Lee '255 in view of Lee '961. Ex. 1003 ¶¶140-278.

1. Overview of combination

Lee '255 teaches a 3D vertical SONOS charge trap-type NVM device. Ex. 1004 (Lee '255), Figs. 4A, 4B, [0003]. Lee '255 teaches most of the limitations of Challenged Claims, including, (i) a substrate with a stack of alternating dielectric and gate layers thereon; (ii) a vertical, pipe-shaped (annular) channel passing through the stack of layers and perpendicular to the substrate; (iii) an ONO stack around and along the vertical channel that includes a tunneling oxide layer, a nitride charge trapping layer, and a blocking oxide layer; and (iv) a series of gate electrodes around the ONO stack forming a vertical array of individual memory transistors. Ex. 1003, ¶141; Ex. 1004 (Lee '255), Figs. 4A, 4B, 5A, [0050]-[0063].

Lee '961 also teaches a 3D vertical SONOS charge trap-type NVM device. Ex. 1005 (Lee '961), [0002]-[0006]. Lee '961 teaches that prior art 3D memory devices similar to the device taught in Lee '255 can suffer from leakage of charges. *Id.*, Fig. 1, [0006]. To provide improved data retention properties, Lee '961 teaches modifying prior art devices to include a SONONOS configuration with a

“multilayered charge trap layer.” Ex. 1005 (Lee ’961), [0010]; *see also id.*, [0012], [0015], [0017], [0020]; Ex. 1003, ¶142.

As discussed below, a POSITA would have been motivated to modify the nitride charge trapping layer of Lee ’255 to incorporate the “multilayered charge trap layer” configuration disclosed in Lee ’961. Ex. 1003, ¶¶143, 163-168.

The combination of Lee ’255 and Lee ’961 differs from prior art considered during prosecution. Ex. 1003, ¶144. In allowing claims 1, 23, and 35, the Examiner did not analyze Lee ’255 or Lee ’961, individually or in combination. *See generally*, Ex. 1002 (Pros. Hist.). Lee ’961 was not of record. While Lee ’255 was listed on an information disclosure statement, the Examiner never applied that reference. Had the Examiner considered the combination of Lee ’255 and Lee ’961, he would have determined that the references teach the features that he found missing from the prior art, including an annularly-shaped multi-layer charge trapping region surrounding a vertical channel. Ex. 1002 (Pros. Hist.), 001877-78. Ex. 1003, ¶144.

2. Independent claim 35

For ease of analysis and efficiency, Petitioner will address independent device claim 35 first before turning to address independent claims 1 and 23, which teach methods of fabricating devices.

[35pre] A semiconductor memory device, comprising:

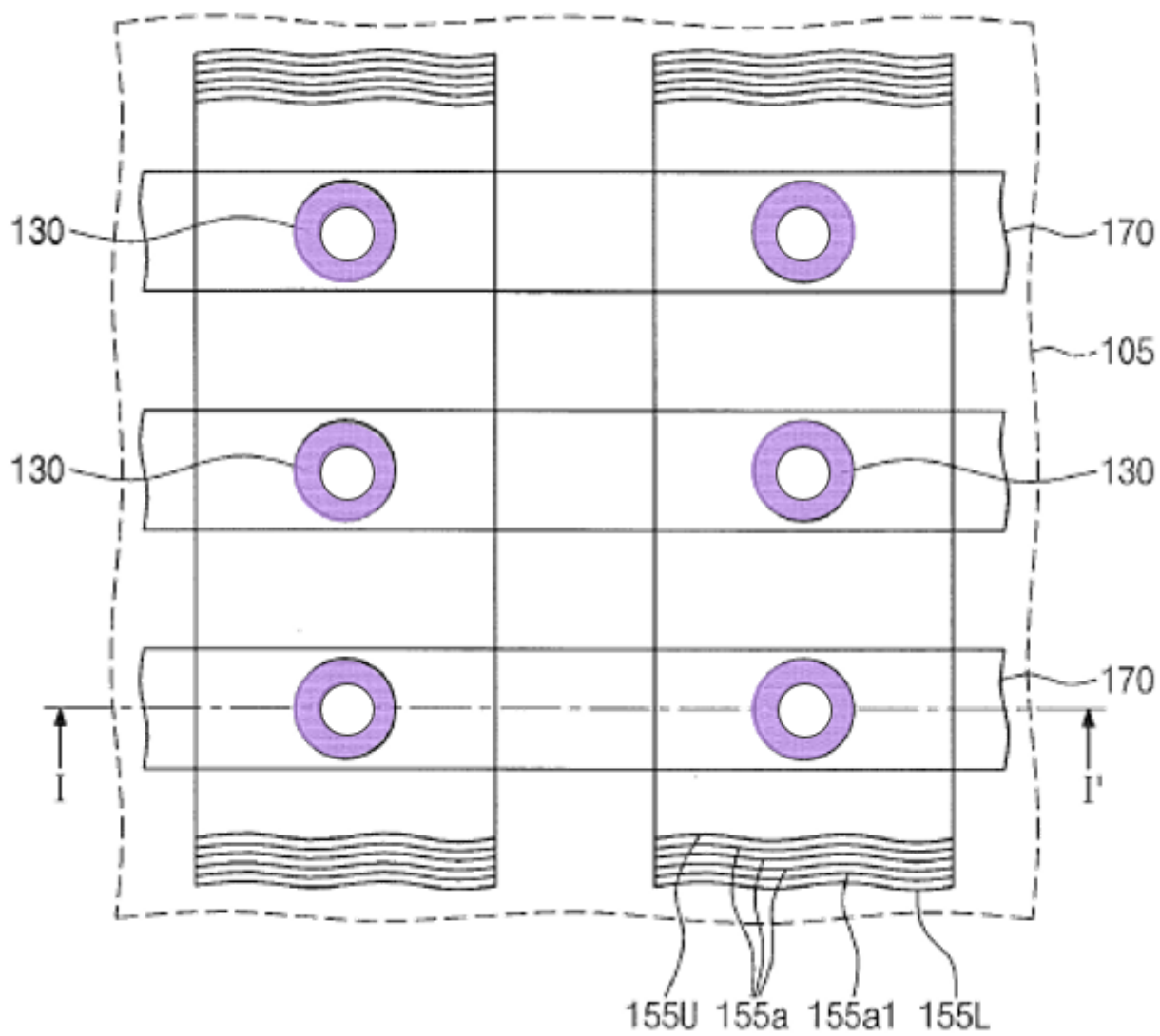
Lee '255 teaches “a three-dimensional (3D) **semiconductor memory device** and a method of fabricating the same.” Ex. 1004 (Lee '255), [0002] (emphasis added); *see also, e.g., id.*, Abstract, Figs. 1A-5B, [0074]; Ex. 1003, ¶147.

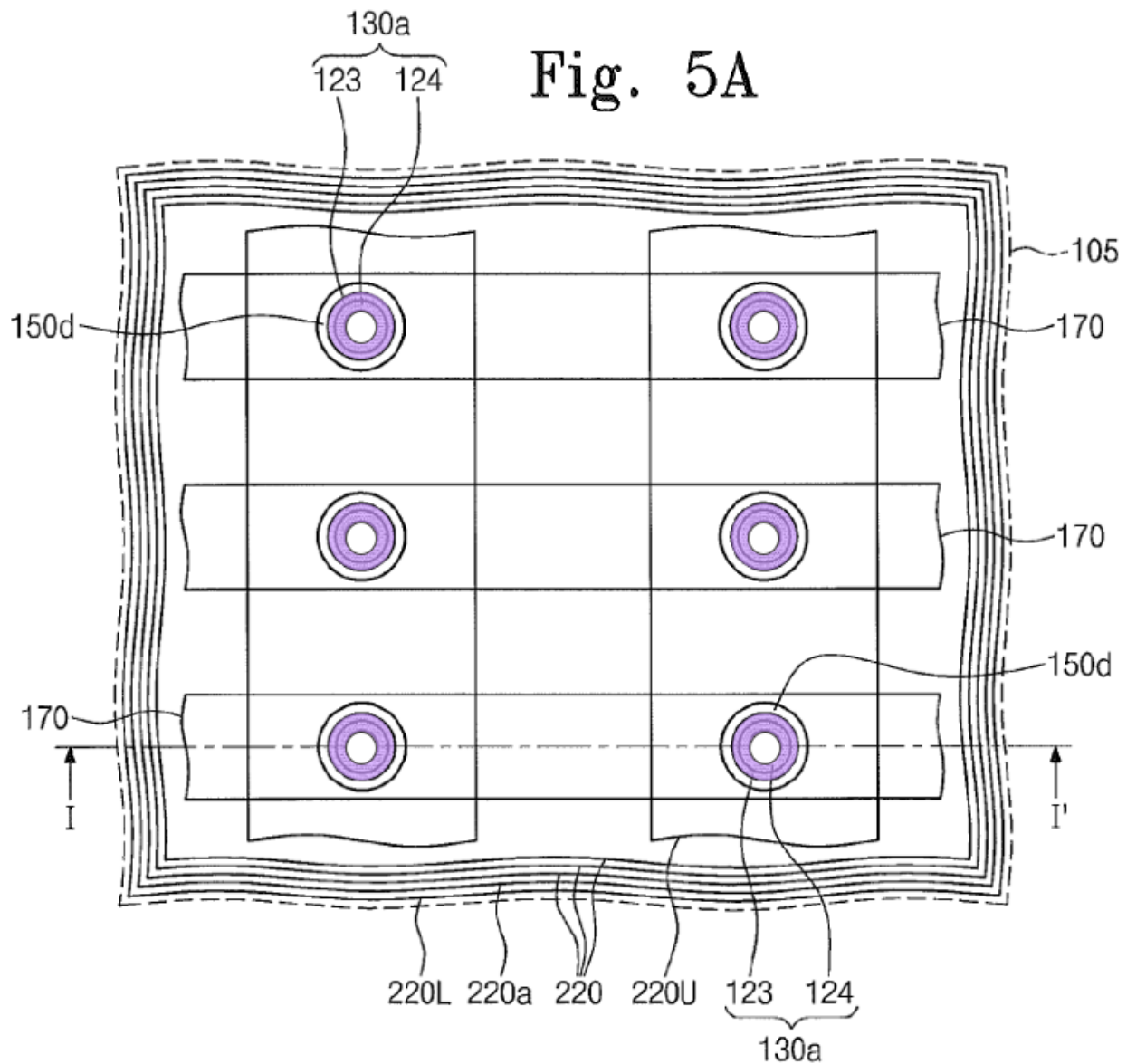
[35a] a semiconductor substrate,

Lee '255 teaches limitation [35a] because Lee '255 teaches forming 3D memory devices on “**a semiconductor substrate 100**” made of, for example, silicon. Ex. 1004 (Lee '255), [0050] (emphasis added); *see also id.*, [0005], [0009]. Lee '255 provides an example of its *semiconductor substrate*² in figure 4A (highlighted in light gray):

² Petitioner uses italics throughout the analysis of the invalidity grounds to identify claim language and distinguish claim language from quotations to the prior art.

Fig. 1A



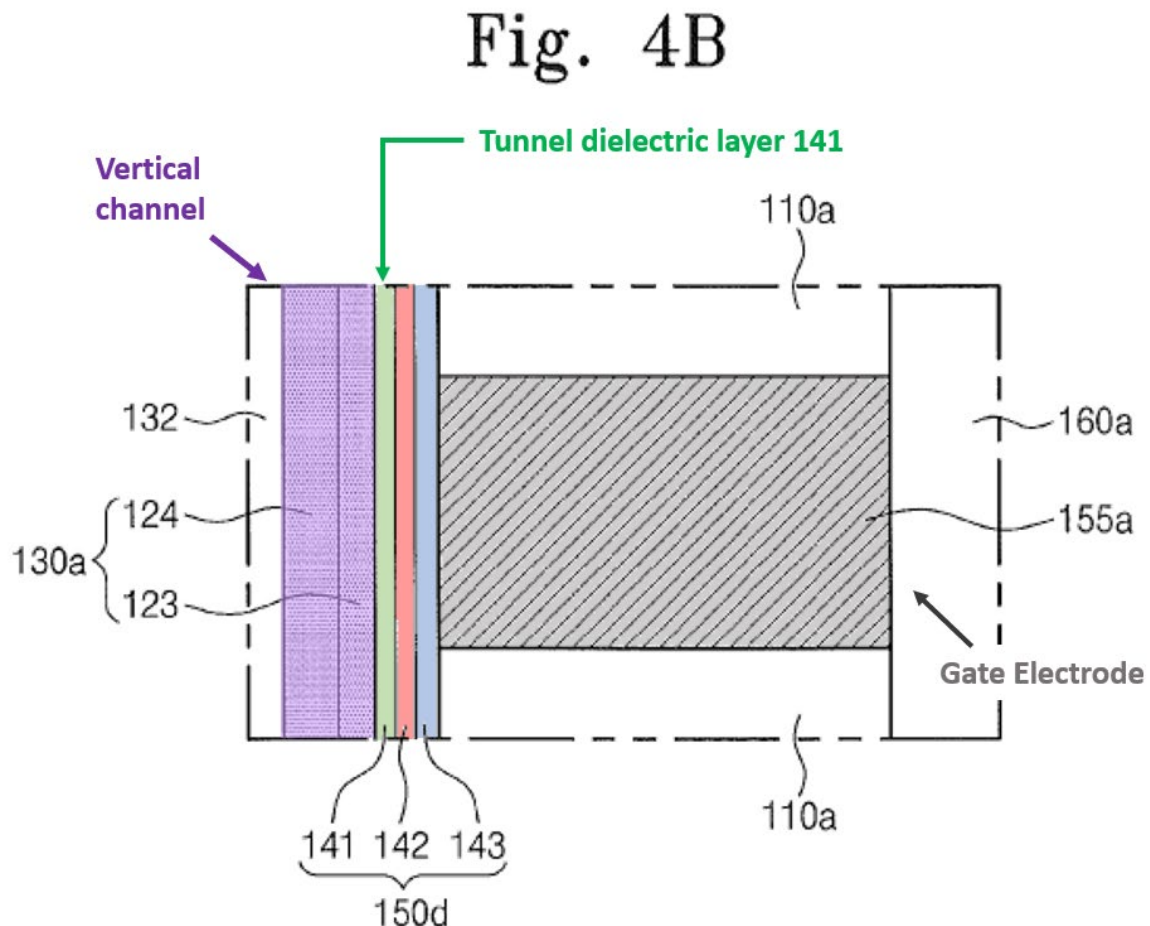


Ex. 1004 (Lee '255), Figs. 1A, 5A, [0054]; *see also id.*, [0074]; Ex. 1003, ¶150.

[35c] a tunnel dielectric layer surrounding the channel region, the tunnel dielectric layer formed in a substantially annular shape,

Lee '255 teaches limitation [35c] because it teaches a “gate dielectric layer 150d” disposed around and along the vertical active pattern 130/130a (the *channel region*) that includes “tunnel dielectric layer 141.” Ex. 1004 (Lee '255), Fig.

4A/B, [0055]-[0057]; Ex. 1003, ¶151. Figure 4B depicts the *tunnel dielectric layer* (annotated here in green):

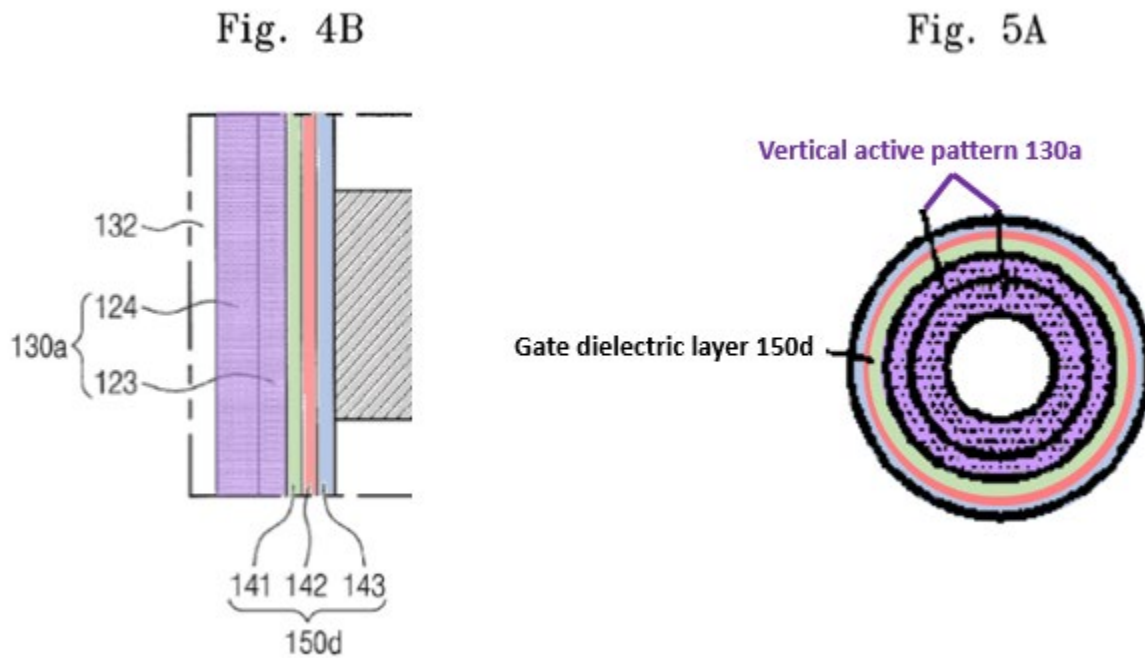


Ex. 1004 (Lee '255), Figs. 4B; Ex. 1003, ¶151.

Lee '255 also teaches that the tunnel dielectric layer is *formed in a substantially annular shape, surrounding the channel region*. As discussed above, Lee '255 teaches that the vertical active pattern (the *channel region*) may be formed in the shape of a pipe (i.e., *annularly*). See Limitation [35b]. Lee '255 further teaches that gate dielectric layer 150d, which includes tunnel dielectric

layer 141, is “disposed between” the vertical active pattern and “each of the gate patterns.” Ex. 1004 (Lee ’255), [0055]; Ex. 1003, ¶152.

Lee ’255 teaches the composition and relative positioning of gate dielectric layer 150d in figure 4B, with the tunneling layer 141 abutting the vertical channel. Lee ’255 teaches that gate dielectric layer 150d has an annular shape surrounding the channel region in figure 5A:



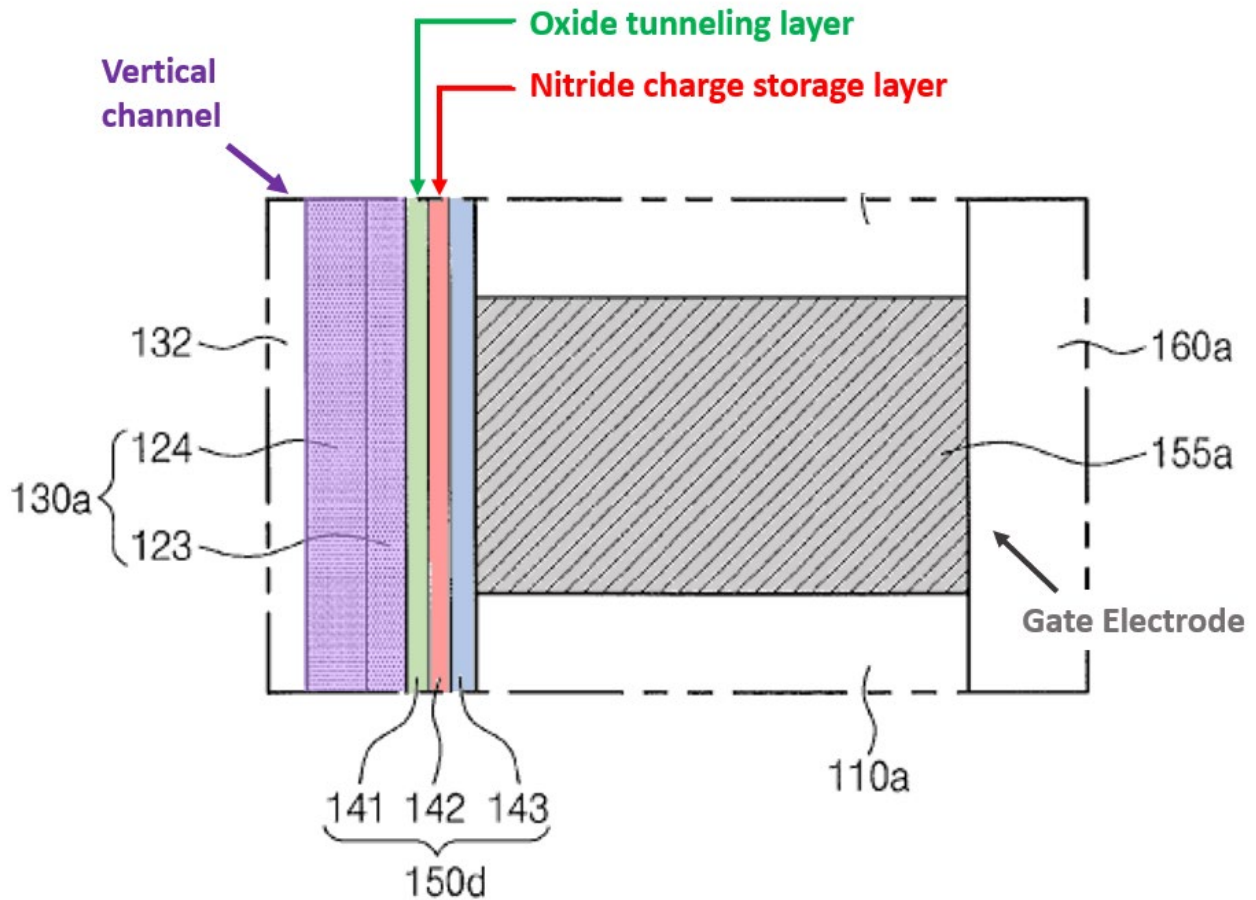
Ex. 1004 (Lee ’255), Figs. 4B, 5A (excerpted and annotated); Ex. 1003, ¶¶153-154.

[35d]	a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape,
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The combination of Lee '255 and Lee '961 teaches limitation [35d]. Ex. 1003, ¶¶ 155-168. As discussed below, Lee '255 teaches a *charge storing region surrounding the tunnel dielectric layer, the . . . charge storing region formed in a substantially annular shape*. Lee '961 teaches a *multi-layer charge storage region* to improve the operation of memory devices such as those taught in Lee '255. A POSITA would have been motivated to modify the charge storing region of Lee '255 based on Lee '961's teachings regarding a multi-layer charge storing region.

Lee '255 teaches a *charge storage region* because Lee '255 teaches that gate dielectric layer 150d includes a nitride “charge storage layer” 142 (annotated in red):

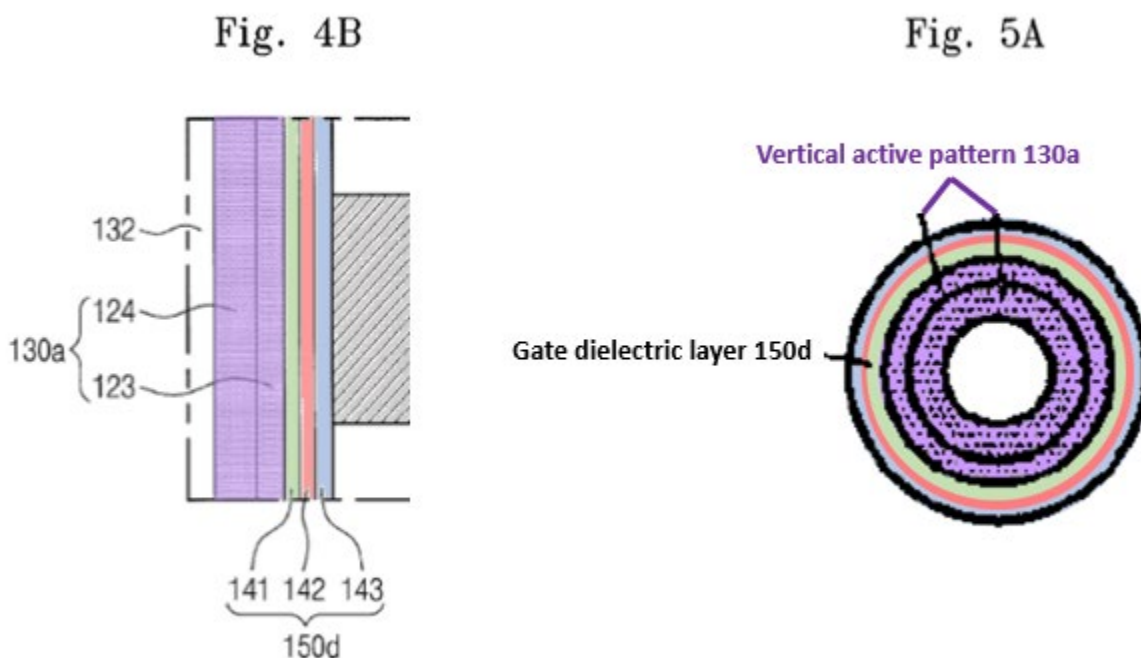
Fig. 4B



Ex. 1004 (Lee '255), Figs. 4B, *see also id.*, [0055]-[0057], [0074]-[0075]; Ex. 1003, ¶156.

Lee '255 teaches that nitride charge storage layer 142 is *formed in a substantially annular shape that is surrounding the tunnel dielectric layer*. As explained above, Lee '255 teaches that the gate dielectric layer 150d is formed in an *annular shape* surrounding the channel region. *See* Limitation [35c]. Lee '255 teaches that the annularly-shaped gate dielectric layer 150d has three sub-layers that are formed in concentric circles—tunnel dielectric layer 141 (green),

surrounded by charge storage layer 142 (red), surrounded by blocking dielectric layer 143 (blue). Thus, a POSITA would have understood that Lee '255 teaches a *substantially annular* charge storing region (charge storage layer 142) *surrounding the tunnel dielectric layer* (tunneling oxide layer 141):



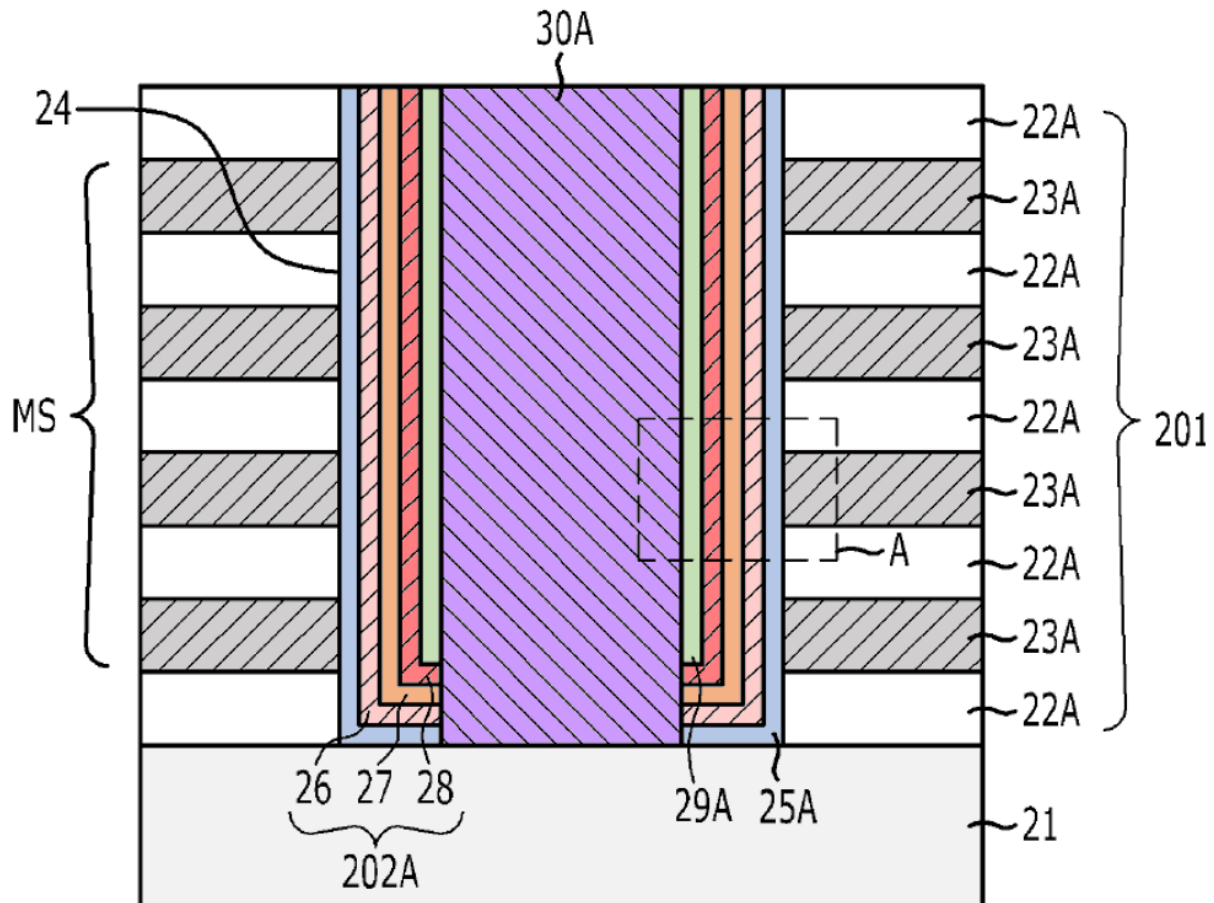
Ex. 1004 (Lee '255), Figs. 4B, 5A (excerpted and annotated); Ex. 1003, ¶¶157-158.

While figure 4B of Lee '255 depicts a “gate dielectric layer 150d” with only three layers, Lee '255 also teaches that the structure is compatible with additional oxide or oxynitride layers. Ex. 1004 (Lee '255), [0057]; Ex. 1003, ¶159.

Lee '961 teaches a 3D SONOS device similar to the device of Lee '255, but with a *multi-layer charge storing region*—a “multilayered charge trap layer” 202A

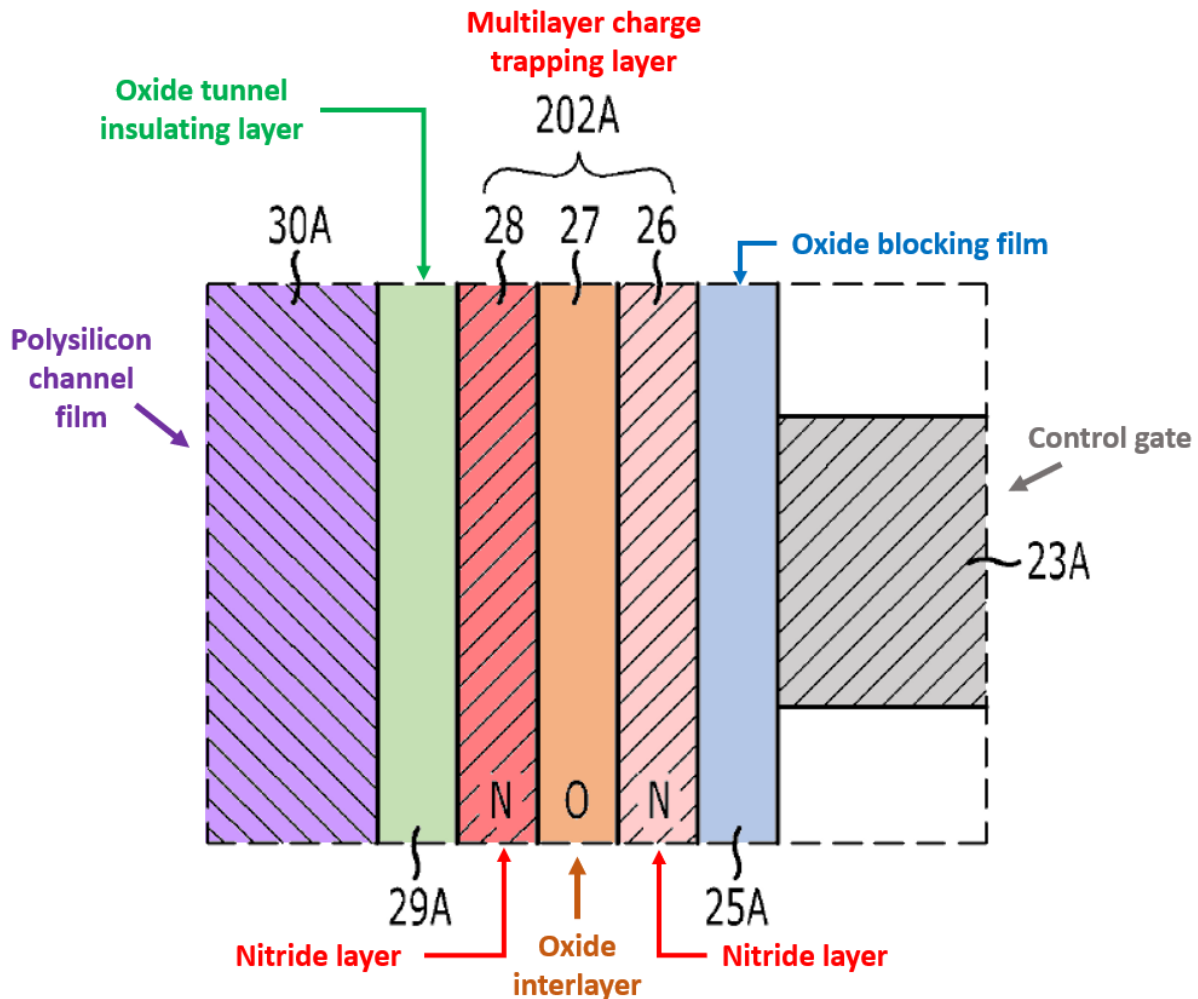
that “improv[es] the data retention properties of non-volatile memory devices.”

Ex. 1005 (Lee '961), [0008], [0010]. Figure 2a of Lee '961 depicts the vertical structure of the 3D memory device, including layer 202A:



Ex. 1005 (Lee '961), FIG. 2a; Ex. 1003, ¶160.

Lee '961's *multi-layer charge storing region* (multilayered charge trap layer 202A) is further depicted in figure 2b:



Ex. 1005 (Lee '961), Figures 2b, [0013], [0018]-[0020]; Ex. 1003, ¶161.

Like Lee '255, Lee '961 teaches that the charge trapping region is positioned between a tunneling dielectric layer (green) and a blocking oxide layer (blue). Ex. 1005 (Lee '961), FIGS. 2a, 2b, [0017]-[0019]; Ex. 1003, ¶162. Lee '961 teaches that “[t]he charge trap layer 202A has a multilayer structure” (*a multi-layer charge storing region*). Ex. 1005 (Lee '961), [0020]. For example, the multilayer charge trap layer 202A may include a nitride first trap layer 26, an oxide interlayer 27, and

a nitride second trap layer 28. Ex. 1005 (Lee '961), [0020]; *see also id.*, [0015]; Ex. 1003, ¶162.

a. Motivation to combine Lee '255 and Lee '961 and expectation of success

A POSITA would have been motivated to modify Lee '255's charge trapping layer to incorporate a multi-layer charge trapping region based on the teachings of Lee '961. Ex. 1003, ¶¶163-168, ¶¶218-223.

As an initial matter, it would have been obvious for a POSITA to consult the teachings of Lee '961 in seeking to improve the memory transistor configuration of Lee '255 because both Lee '961 and Lee '255 are directed to improving the operation of SONOS-type charge trapping memory transistors. Ex. 1003, ¶164. Indeed, Lee '255 mirrors the type of devices that Lee '961 seeks to improve. *Compare* Ex. 1004 (Lee '255), Fig. 4A *with* Ex. 1005 (Lee '961), Fig. 1. Moreover, Lee '255 specifically teaches that its structure is compatible with additional nitride and oxide layers. Ex. 1004 (Lee '255), [0057]; Ex. 1003, ¶159.

A POSITA would also have been motivated to apply Lee '961's ONONO stack teachings to the ONO stack of Lee '255 based on the express teachings, suggestion, and motivation to combine found in Lee '961. Ex. 1003, ¶165. Specifically, Lee '961 teaches that SONOS configurations such as Lee '255's suffered from poor charge retention due to lateral spreading of charges in the single silicon nitride trapping film. Ex. 1005 (Lee '961), [0004]-[0006]. Lee '961

teaches that a solution to this problem is the multilayered charge trap layer (202A), which improves data retention. Ex. 1005 (Lee '961), [0010].

The data retention benefits of using the multilayer charge trapping region of Lee '961 also would have been predictable to a POSITA prior to July 2012. Ex. 1003, ¶166. Using multilayer charge trapping structures was already a conventional strategy for improving retention prior to July 2012. *See* Ex. 1003, ¶¶54-81, 166; *see also* Ex. 1010 (Nomoto), [0035], [0044]-[0045], [0073]-[0088]; Ex. 1011 (Levy), [0025]-[0026]; Ex. 1012 (Heo), [0058]-[0068]; Ex. 1006 (Fujiwara), Fig. 21, [0197]-[0208]; Ex. 1009 (Kim '399), [0034], [0046]-[0047]; Ex. 1013 (Ganguly), [0020], [0048]-[0049]; Ex. 1017 (Lai '676), [0015], [0068]-[0077]; Ex. 1021 (Higuchi) [0007], [0133]-[0134], [0141]-[0142]; Ex. 1014 (Wang '586), [0006], [0022], [0031]-[0032]; Ex. 1020 (Arreghini), 000003 (Fig. 3), 000006. As such, applying the multilayer charge trapping region of Lee '961 to modify the charge trapping layer of Lee '255 would have amounted to (i) combining prior art elements according to known methods to yield predictable results; and (ii) use of known techniques to improve a similar device in the same way. Ex. 1003, ¶166. It also would have been obvious to try a multilayer charge trapping region with the device of Lee '255 prior to July 2012. *Id.*, ¶167.

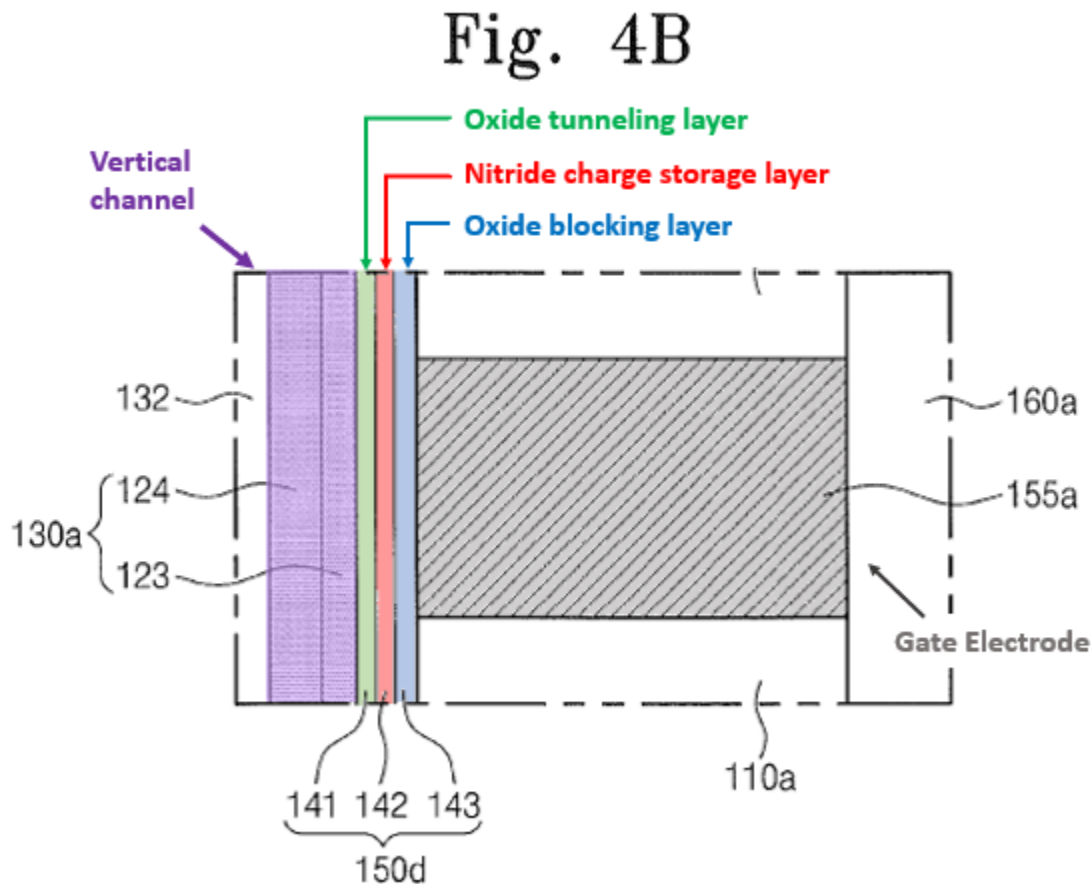
A POSITA also would have had a reasonable expectation of success in modifying the memory device of Lee '255 based on the teachings of Lee '961. Ex.

1003, ¶168. Both Lee '255 and Lee '961 are directed to very similar 3D charge trap memory devices with common features: vertical channels, stacks of insulating and gate layers, tunneling oxides, charge trap layers, and blocking oxides, and annular configuration. The memory structures in both references use similar materials and layouts, and address similar technical challenges. Indeed, Lee '961 expressly aims to improve the type of memory architecture used in Lee '255 by introducing a multilayer charge trap structure. Ex. 1005 (Lee '961), Fig. 1, [0002]-[0010]. Applying Lee '961's teachings of a multilayer charge trapping region to the structure of Lee '255 would have amounted to depositing additional layers as part of the fabrication process. Ex. 1003, ¶168. This is an alternative that Lee '255 already contemplates. *See* Ex. 1004 (Lee '255), [0057]. Further, a POSITA would have understood that depositing these additional layer would involve using established techniques for material selection, layer formation, and stack integration that were routine and well-known to a POSITA prior to July 2012. Ex. 1003, ¶¶168, 218-223 (describing compatibility of processes of Lee '255 and Lee '961).

[35e]	a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and
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Lee '255 teaches limitation [35e] because it teaches that the “gate dielectric layer 150d” includes an oxide “blocking dielectric layer 143” (*a blocking dielectric layer*). Ex. 1004 (Lee '255), Fig. 4B, [0055]-[0057]; Ex. 1003, ¶169. The relative

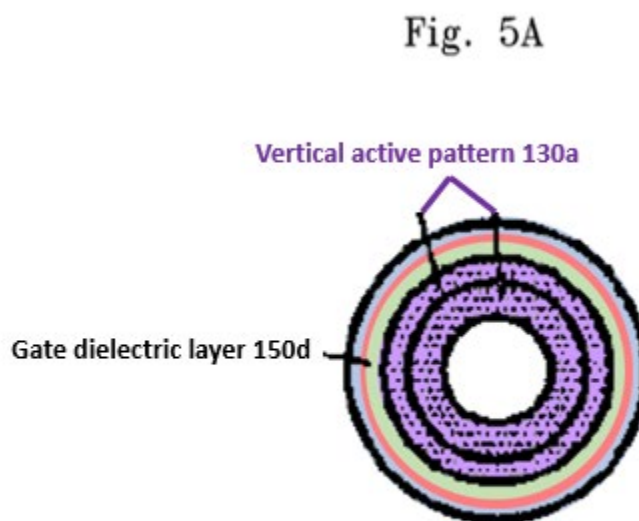
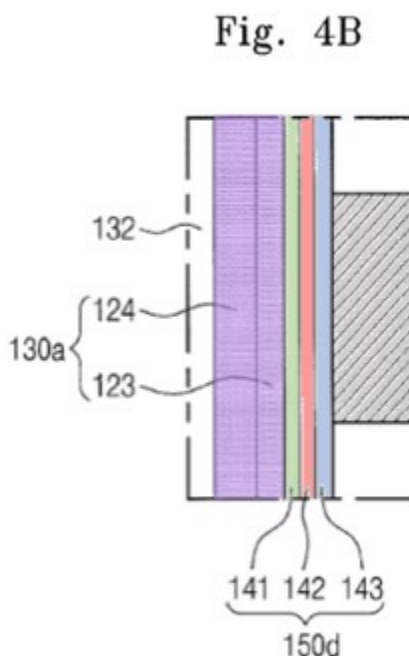
position of the blocking dielectric layer 143 (blue), is shown in this annotated version of figure 4B:



Ex. 1004 (Lee '255), Fig. 4B.

Lee '255 further teaches that blocking dielectric layer 143 (*blocking dielectric layer*) is *formed in a substantially annular shape* and positioned so that it is *surrounding the . . . charge storing region*. As explained above, Lee '255 teaches that the gate dielectric layer 150d is formed in an *annular shape* surrounding the channel region. See Limitations [35c], [35d]. The blocking

dielectric layer 143 is positioned on the outside of the ONO stack such that it surrounds the charge storage region:

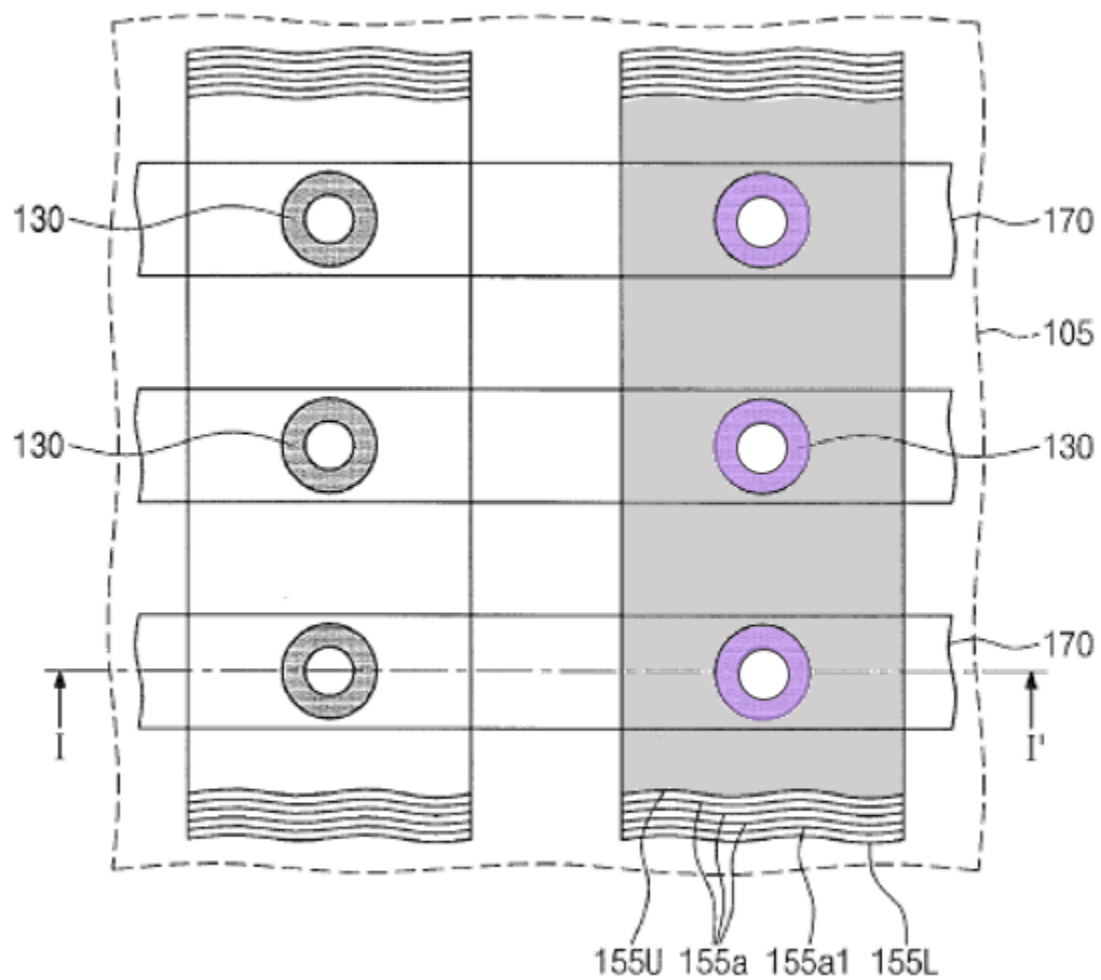


Ex. 1004 (Lee '255), Figs. 4B, 5A (excerpted and annotated); *see also id.*, [0055]-[0057]; Ex. 1003, ¶¶170-171. Modifying the charge storage layer of Lee '255 based on the teachings of Lee '961 (*see* Limitation [35d]) would not alter the relative positioning of that layer to the tunneling or blocking layers because both Lee '255 and Lee '961 teach that the charge trapping region (whether a single layer or multiple layers) is positioned between the tunnel layer and the blocking layer. Ex. 1003, ¶172.

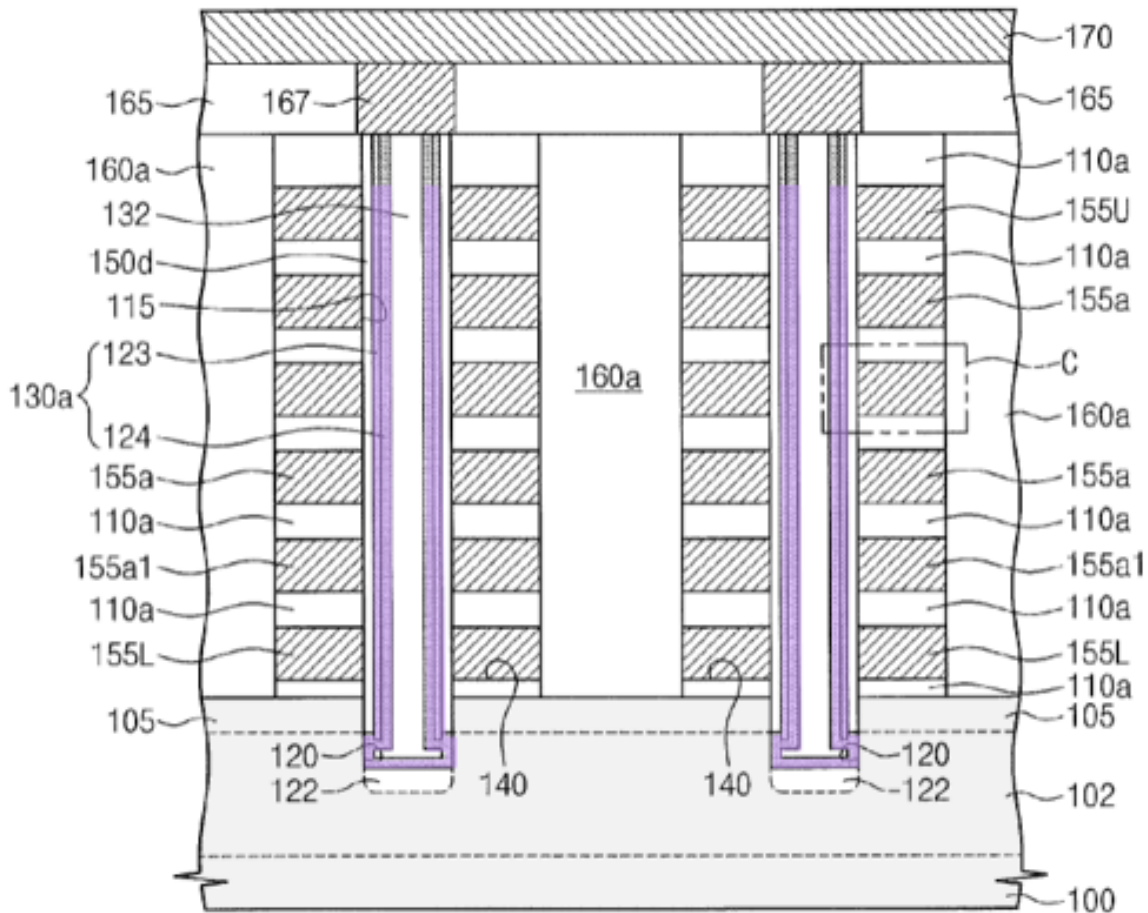
[35f] a gate electrode surrounding the blocking dielectric layer.

Lee '255 teaches limitation [35f] because it teaches gate electrodes 155a (each *a gate electrode*) that are positioned *surrounding* oxide blocking dielectric layer 143 (*the blocking dielectric layer*). Ex. 1004 (Lee '255), Figs. 1A, 4A, 4B, and 5A, [0055]-[0062]; Ex. 1003, ¶173.

Lee '255 teaches that the 3D memory device is comprised of a “stack-structure, including insulation patterns 110a and gate patterns 155L, 155a1, 155a, and 155U that are stacked alternately and repeatedly.” Ex. 1004 (Lee '255), [0051]. “A plurality of vertical active patterns 130”—i.e., vertical *channel regions*—“may pass through each of the stack-structures.” *Id.*, [0061]. This is shown, for example, in figures 1A (plan view) and 4A (cross section of figure 1A along axis I – I’):



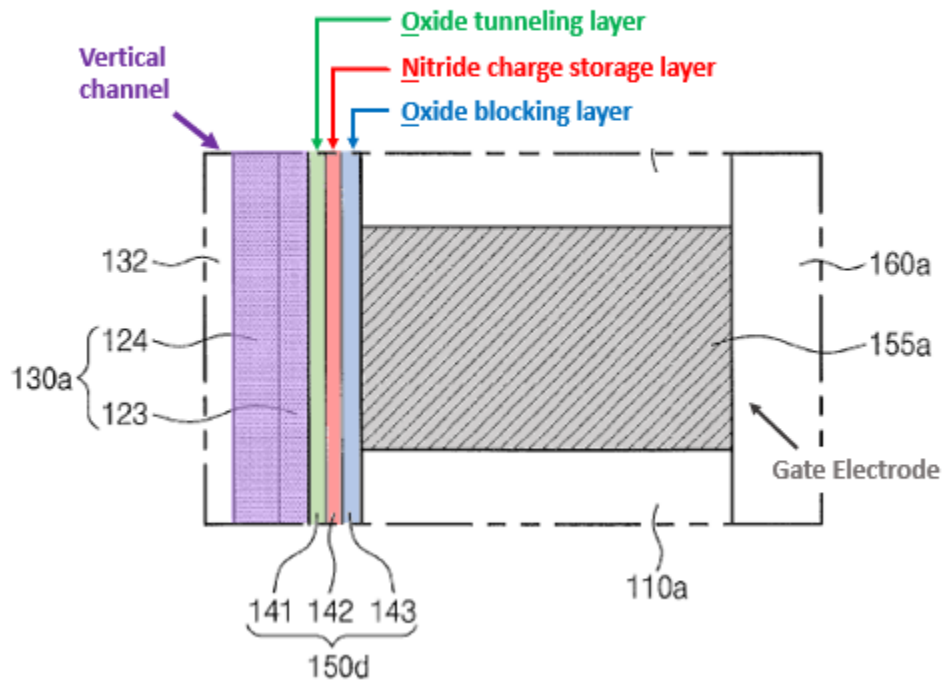
Ex. 1004 (Lee '255), Fig. 1A.



Ex. 1005 (Lee '255), Fig. 4A, [0051], [0061]; Ex. 1003, ¶174.

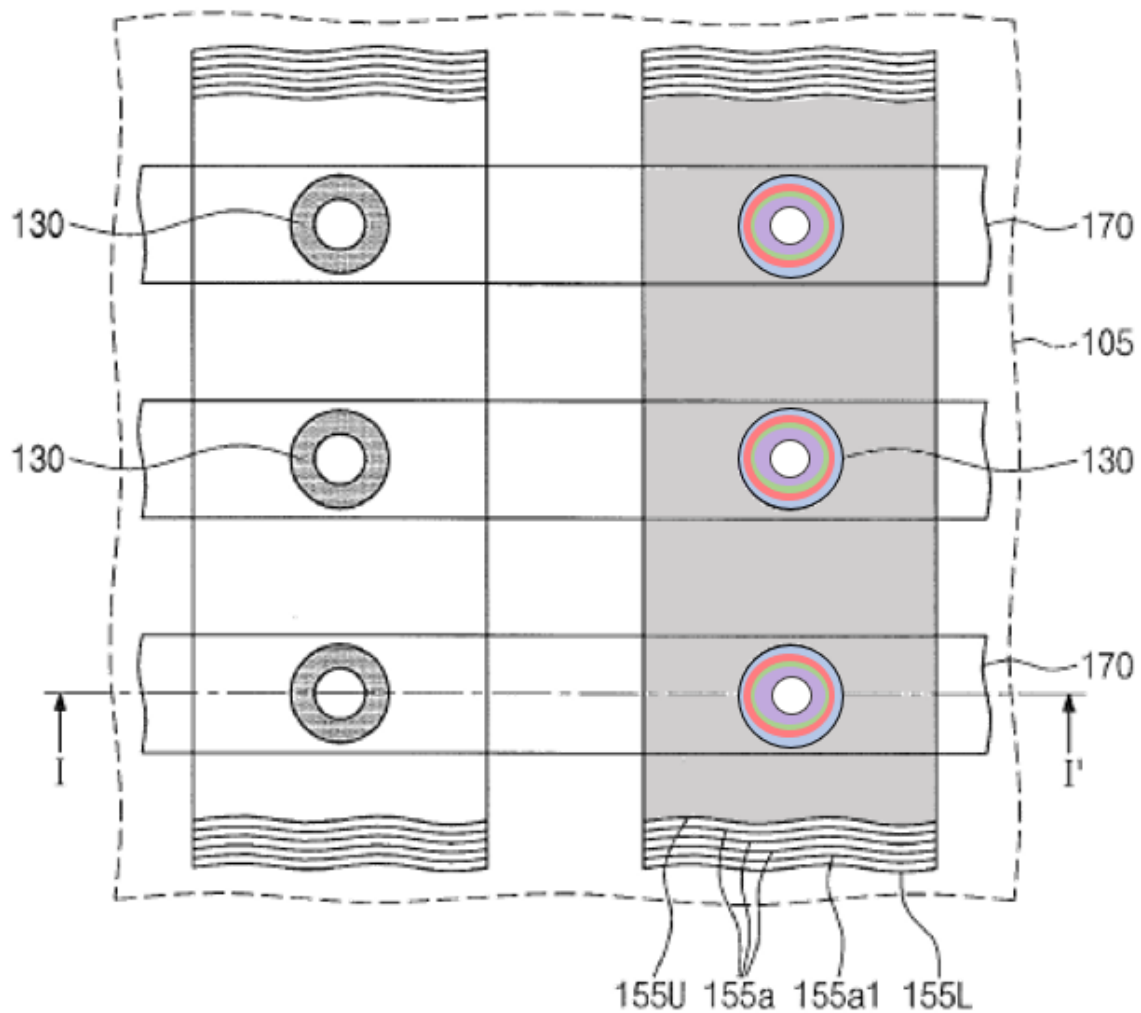
Lee '255 teaches that the “blocking dielectric layer 143” is part of gate dielectric layer 150d. Ex. 1004 (Lee), [0056]; Ex. 1003, ¶175. “[T]he blocking dielectric layer 143” is on the outside of the gate dielectric layer 150d and “may be adjacent to each of the gate patterns 155L, 155a1, 155a, and 155U.” *Id.*, [0056]. This is shown in figure 4B, where gate electrode 155a (gray) is shown in a abutting blocking dielectric layer 143 (blue):

Fig. 4B



Ex. 1004 (Lee '255), Fig. 4B; Ex. 1003, ¶175.

Blue lines have been added to the below annotation of figure 4A to more clearly illustrate the position of the blocking dielectric layer 143 within gate dielectric layer 150d:



Ex. 1004 (Lee '255), Figs. 1A, 4B, 5A, [0074], [0077]; Ex. 1003, ¶177.

3. Dependent claims 36, 37, 42-44

Claims 36, 37, and 42-44, which depend from claim 35, are also obvious based on the teachings of Lee '255 in view of Lee '961.

36. The semiconductor memory device of claim 35, wherein the blocking dielectric layer includes a high K dielectric.

Lee '255 teaches the additional limitation of claim 36 because it teaches that the “blocking dielectric layer 143 may include a high-k dielectric layer having a dielectric constant higher than that of the tunnel dielectric layer 141.” Ex. 1004 (Lee '255), [0057]; Ex. 1003, ¶¶178-179.

37. The semiconductor memory device of claim 35, wherein the gate electrode is a high work function gate electrode.

Lee '255 teaches the additional limitations of claim 37 because Lee '255 teaches its gates 155a “include a conductive material” such as doped silicon, tantalum, or tantalum nitride. Ex. 1004 (Lee '255), [0062]. A POSITA would have understood that doped silicon and tantalum nitride are both *high work function* materials. Ex. 1003, ¶181; Ex. 1001 (the '365 patent), 7:31-43 (doped polysilicon used for high work function gate electrodes); Ex. 1012 (Heo), [0046]; Ex. 1017 (Lai '676), [0067], [0072]; Ex. 1041 (Zheng), 5:52-62, 6:32-59.

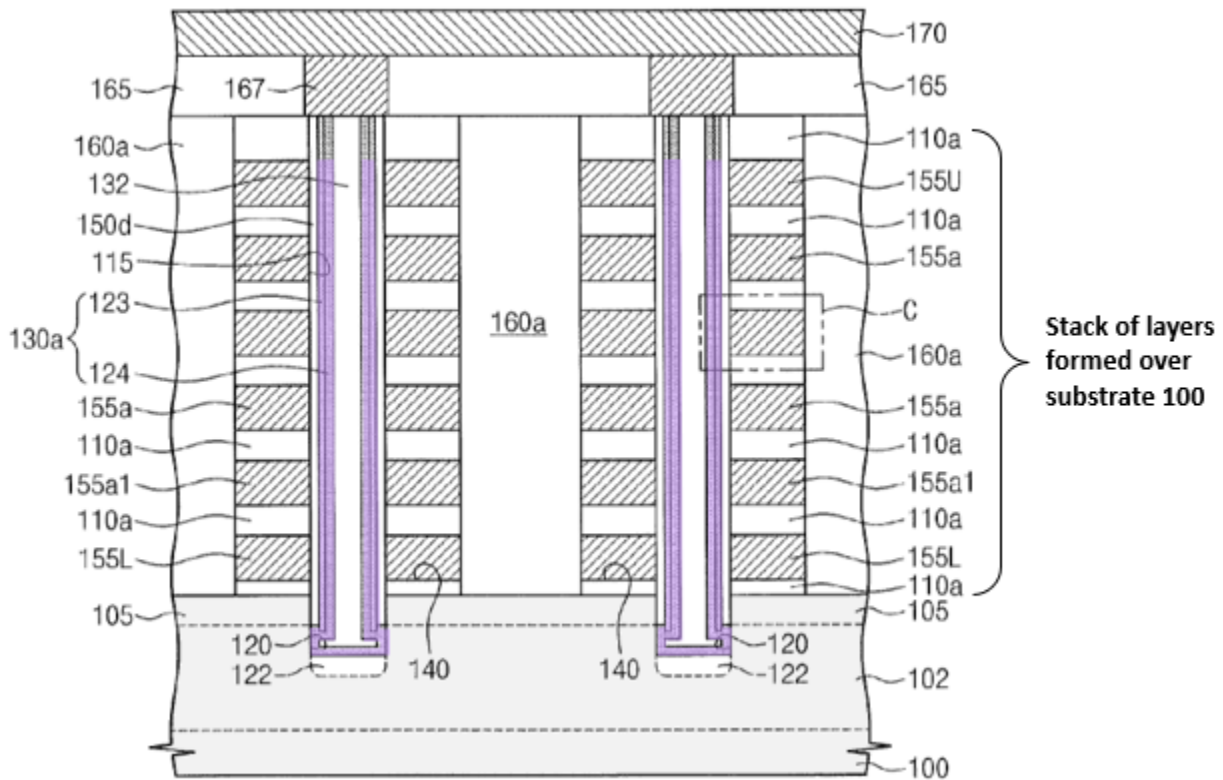
To the extent patent owner argues that the gate materials taught in Lee '255 are not *high work function* materials, a POSITA would have found it obvious to use a *high work function gate electrode* based on the teachings of Lee '961. Ex. 1003, ¶¶182-183. Lee '961 teaches gates made of polysilicon doped with P-type impurities. Ex. 1005 ('961), [0018]. A POSITA would have understood based on the examples of *high work function gate electrodes* provided in the '365 patent (*see*

Ex. 1001 ('365 patent), 7:31-43) that polysilicon doped with p-type impurities is an example of a *high work function* gate material. See Part IV.B, *supra*; see also Ex. 1041 (Zheng) 5:36-37, 5:60-62, Ex. 1012 (Heo), [0046]; Ex. 1017 (Lai '676), [0067], [0072].

A POSITA would have been motivated to apply the high work function gate electrode of Lee '961 to the memory device of Lee '255, and expected success in doing so, because the use of such material would have amounted to (i) combining prior art elements according to known methods to yield predictable results; and (ii) use of known techniques to improve a similar device in the same way. Ex. 1003, ¶183; Ex. 1029 (Kim Article), Fig. 7, 000005; Ex. 1030 (Jeon), Fig. 1, [0009]; Ex. 1016 (Lue '189), [0084], [0086]; Ex. 1012 (Heo), [0064]; 1031 (Shih), [0071]; Ex. 1041 (Zheng), 1:14-18.

42. The semiconductor memory device of claim 35, including a stack of layers formed over the substrate.
--

Lee '255 teaches the additional limitations of claim 42 because it teaches *a stack of layers*—the “stack-structure, including insulation patterns 110a and gate patterns 155L, 155a1, 155a and 155U that are stacked alternately and repeatedly”—that is *formed over the substrate* (substrate 100). Ex. 1004 (Lee '255), Fig. 4A, [0051], [0074]; Ex. 1003, ¶¶184-185. This *stack of layers formed over the substrate* is shown in Figure 4A:



Ex. 1004 (Lee '255), Fig. 4A.

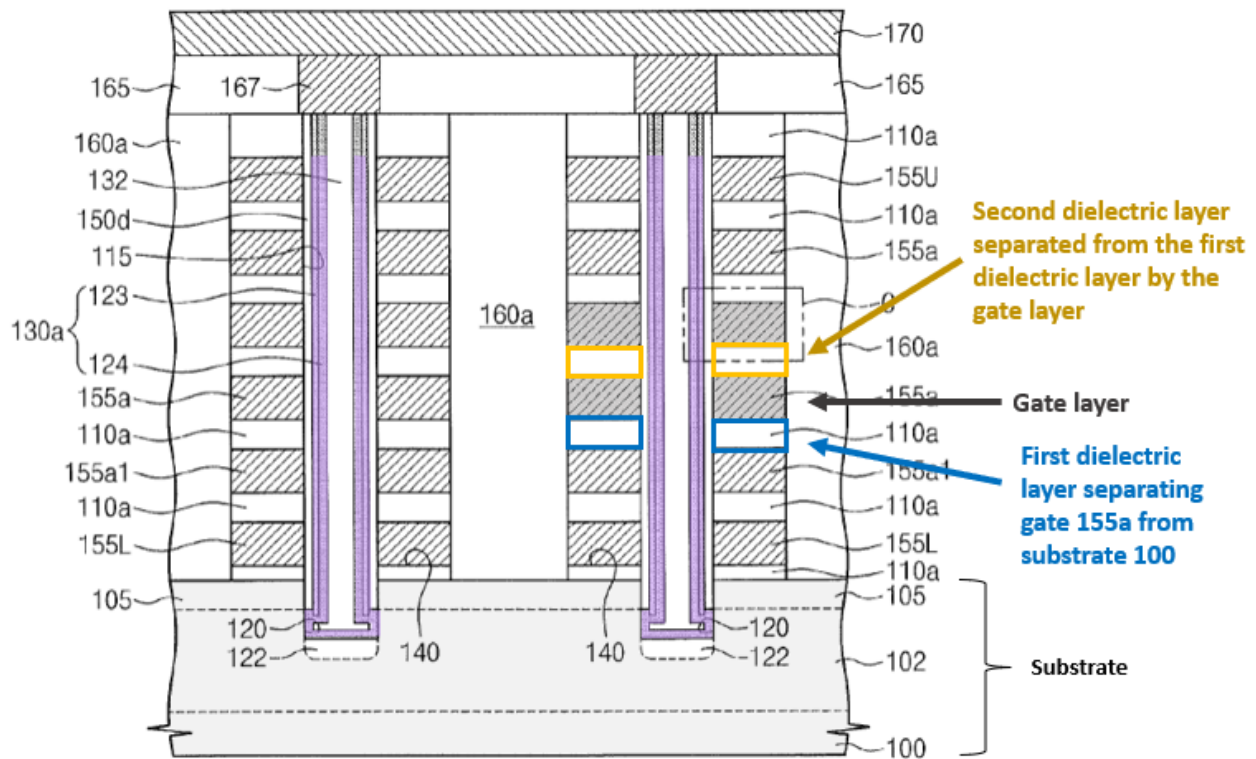
43. The semiconductor memory device of claim 42, wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer, wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer.

As an initial matter, the wherein clause of claim 43 includes a typographical error and should be construed as: “wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the gate ~~a sacrificial~~ layer.” See Part IV.D, above.

Lee '255 teaches a *stack of layers* because Lee '255 teaches a “stack-structure.” See Claim 42; Ex. 1004 (Lee '255), Fig. 4A, [0051], [0074]; Ex. 1003,

¶¶186, 188. Lee '255 teaches the stack of layers includes *a first dielectric layer, a gate layer and a second dielectric layer* because Lee '255 teaches that the stack structure includes multiple “insulation patterns 110a” (dielectric layers) that are adjacent to gate patterns 155a (gate layers). Ex. 1004 (Lee '255), Fig. 4A, [0055], [0060]; Ex. 1003, ¶¶189-190; Ex. 1045 (Lai '423), 2:46-59.

Lee '255 teaches *wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by [the gate] layer* because the insulating patterns 110a (dielectric layers) and the gate patterns 155a (gate layers) are “stacked alternately” with insulating layers separating gate layers from the substrate and gate layers positioned between (and therefore separating) the dielectric layers:



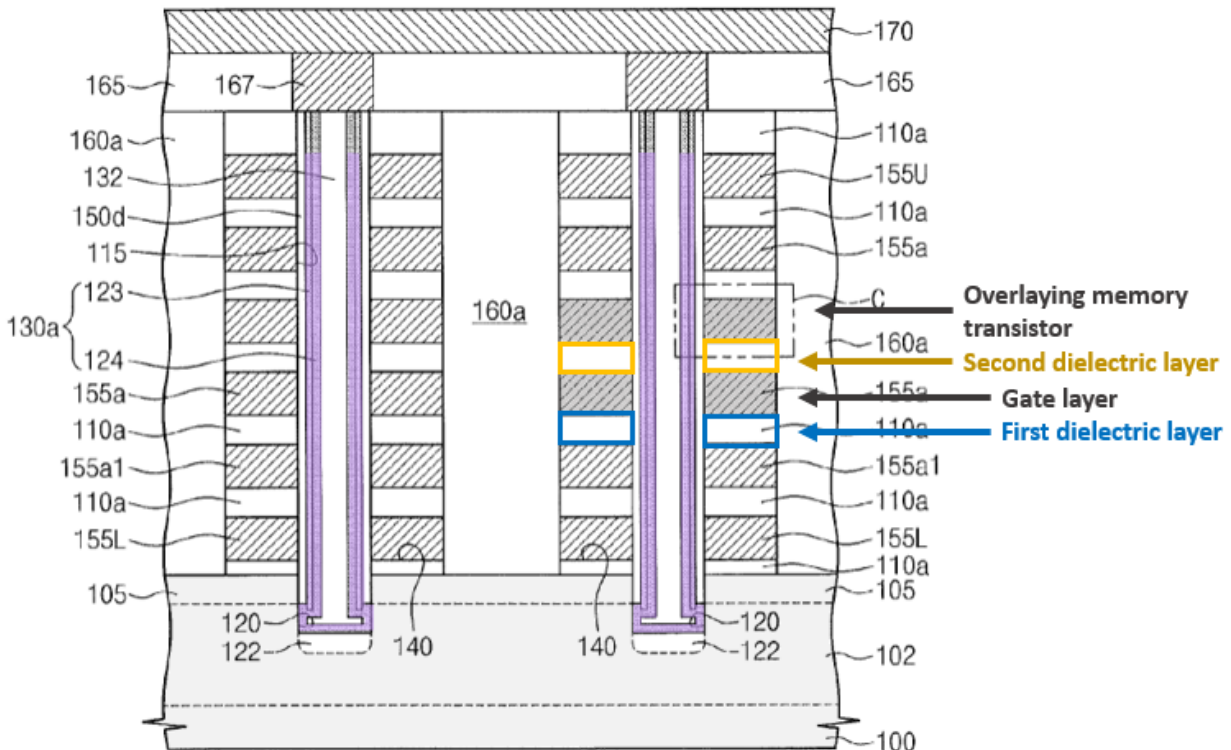
Ex. 1004 (Lee '255), Fig. 4A, [0051]; Ex. 1003, ¶191.

44. The semiconductor memory device of claim 43, wherein the channel region is formed in an opening extending through the stack of layers.

For the reasons set forth above, Lee '255 teaches a *channel region* (vertical active pattern 130/130a) and a *stack of layers* (the “stack-structure” of insulating patterns 110a and gate patterns 155). See Limitation [35b], claims 42, 43; Ex. 1003, ¶193.

Lee '255 further teaches the *channel region* (active pattern 130/130a) is *formed in an opening* (“opening 115”) that is *extending through the stack of layers* (insulation patterns 110a and gate patterns 155), as depicted in figure 4A (see green and purple highlights):

97 (explaining 3D NAND fabrication); Ex. 1026 (Tanaka), 00001. The following annotation of figure 4A provides one example of Lee '255's teachings of a *second dielectric layer* that separates the gate layer from an overlying memory transistor:



Ex. 1004 (Lee '255), Fig. 4A; Ex. 1003, ¶¶197.

4. Independent claim 1

Claim 1 is also obvious based on the teachings of Lee '255 in view of Lee '961.

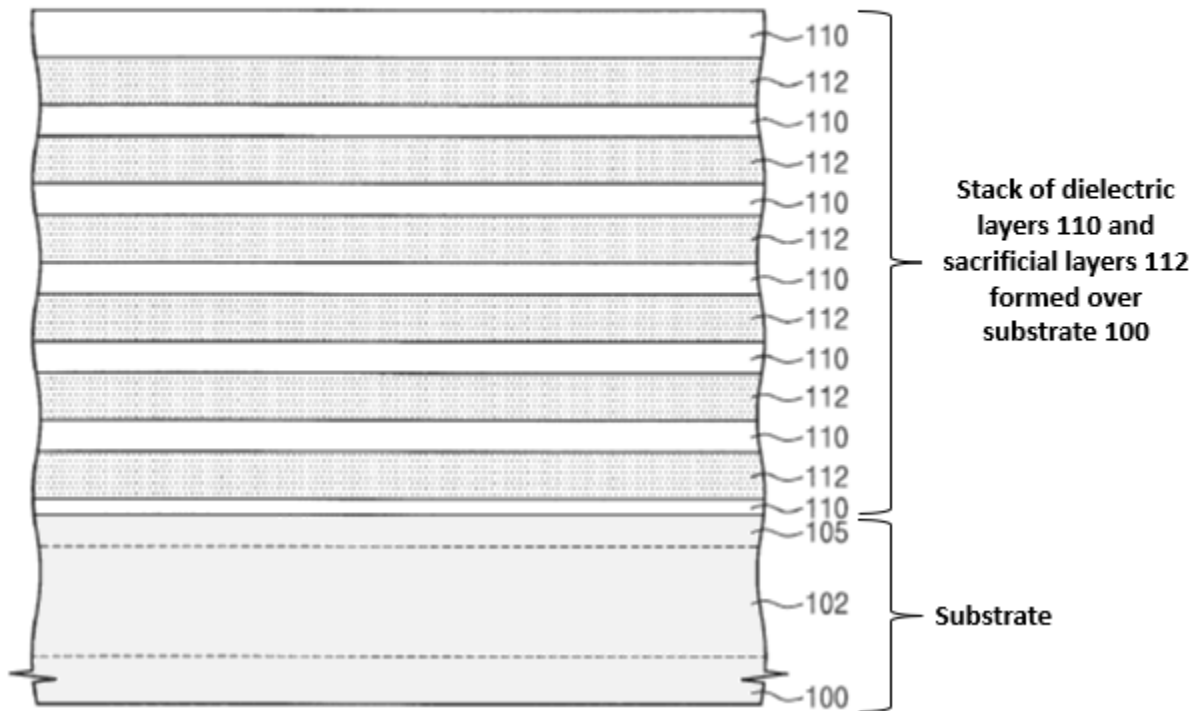
[1pre] A method comprising:

Lee '255 teaches “a method of fabricating 3D semiconductor memory” devices. *See, e.g.*, Ex. 1004 (Lee '255), [0080]; *see also id.*, FIGS. 6A-10C, 13A-16B, [0131]; Ex. 1003, ¶198.

[1a1] forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;

Lee '255 teaches *forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer* because Lee '255 teaches “[i]nsulation layers 110 and sacrificial layers 112 may be alternately and repeatedly stacked on the common source region 105 [of substrate 100].” Ex. 1004 (Lee '255), [0080]; *see also id.*, [0077] (common source region 105 is part of the substrate). Ex. 1003, ¶¶199-200. This is depicted in figure 6A:

Fig. 6A



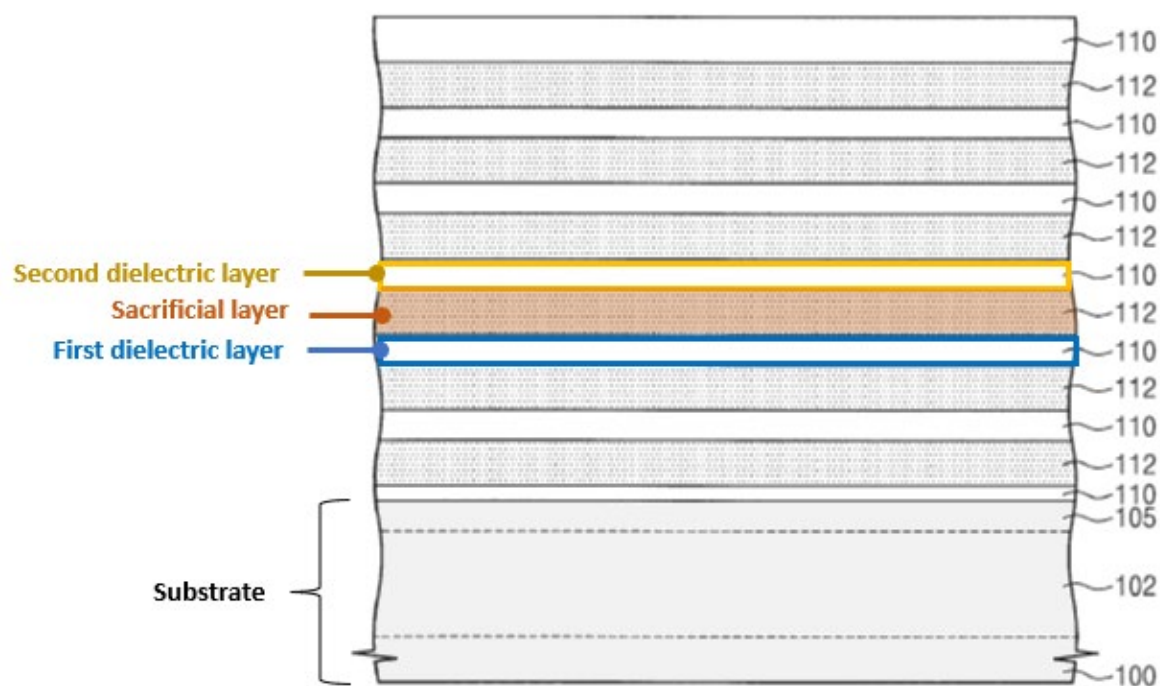
Ex. 1004 (Lee '255), Fig. 6A, [0080]; Ex. 1003, ¶200.

As reflected above, Lee '255 teaches forming a *first* and a *second* dielectric layer because Lee '255 teaches that there are multiple insulation layers 110. Ex. 1004 (Lee '255), [0080]; Ex. 1003, ¶201; *see also* claim 43, *supra*.

Lee '255 teaches *the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer* because Lee '255 teaches that there are insulating layers 110 formed on either side of multiple sacrificial layers 112, all above substrate 100. For example, figure 6A teaches a first dielectric layer 110

(blue border) separates a sacrificial layer 112 (orange) from substrate 100 (light gray). Lee '255 further teaches that the same sacrificial layer separates the same first dielectric layer from a second dielectric layer 110 (yellow border):

Fig. 6A

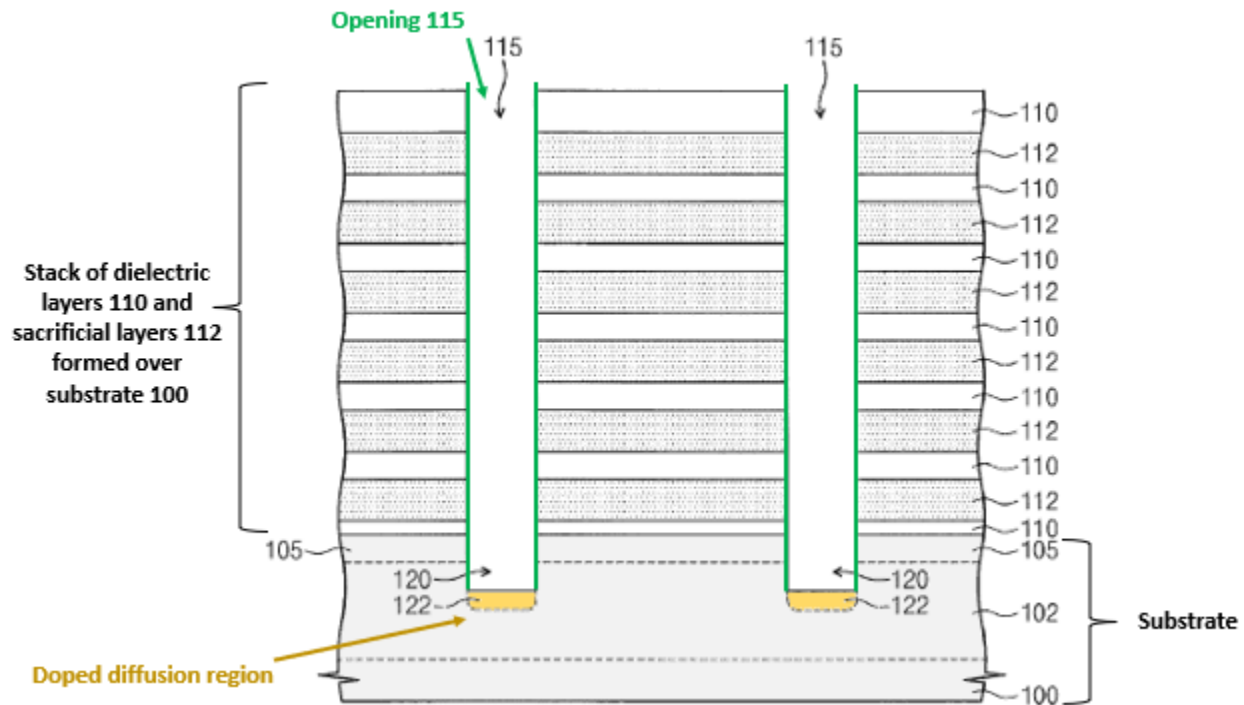


Ex. 1004 (Lee '255), Fig. 6A; Ex. 1003, ¶¶202-203.

[1a2] forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate;

Lee '255 teaches *forming an opening* (opening 115) that *extend[s] through the stack of layers* (the stack of the insulation layers 110 and sacrificial layers 112)

to a first doped diffusion region formed on the substrate (high concentration region 122):

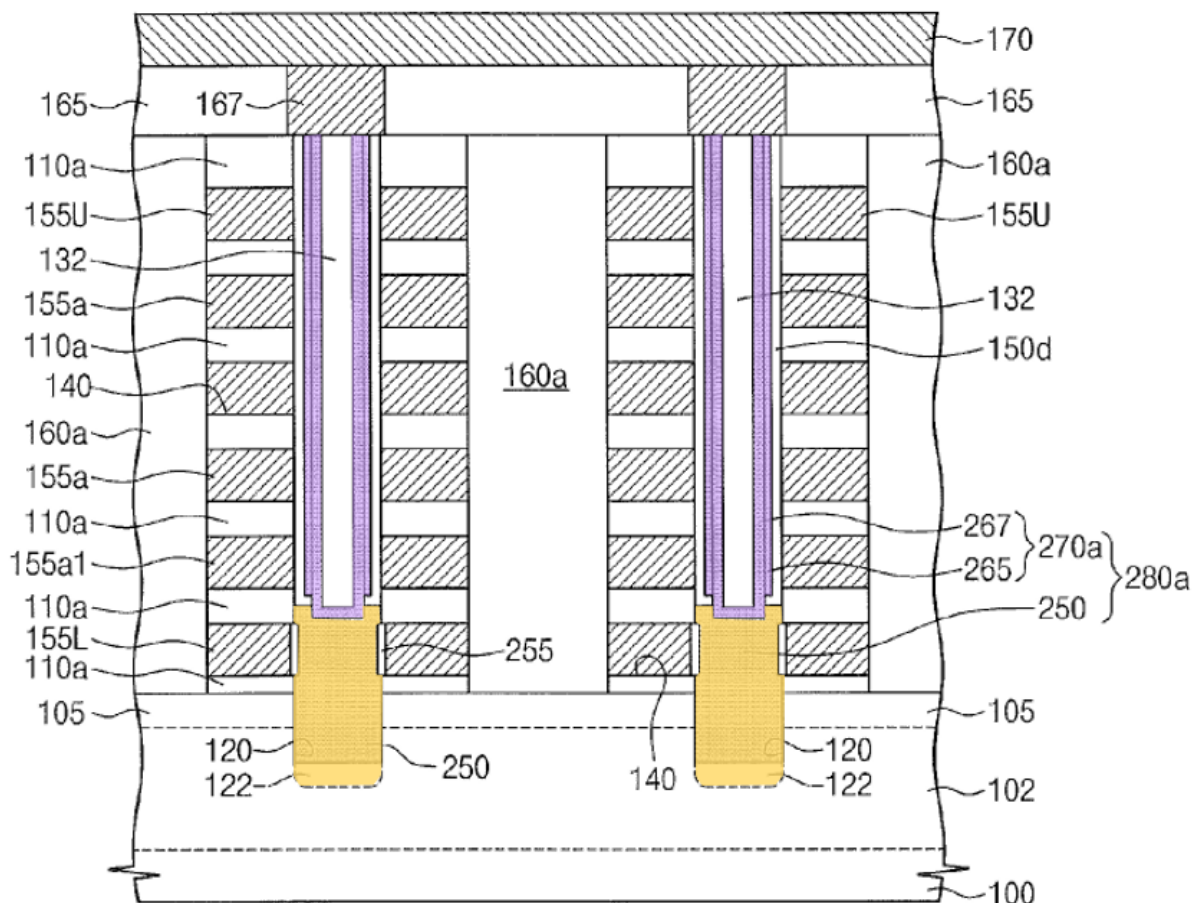


Ex. 1004 (Lee '255), Fig. 6B, [0081]; Ex. 1003, ¶¶204-205.

A POSITA would have understood that “high concentration region 122” is a *first doped diffusion region* because Lee '255 teaches that it is doped with conductive dopants. Ex. 1004 (Lee '255), [0081]; Ex. 1003, ¶206. Further, figure 6B shows that high concentration region 122 is *formed on the substrate*. Ex. 1004 (Lee '255), Fig. 6B; *compare id. with* Ex. 1001 ('365 patent), Fig. 9E (showing diffusion region 904 in a similar position); Ex. 1003, ¶207. Alternatively, if Patent Owner argues that high concentration region 122 is not *formed on the substrate*, Lee '255 teaches another embodiment in which high concentration region 122 is

combined with a doped “lower active pattern 250” formed on (and extending above) the upper surface of substrate 100:

Fig. 12E



Ex. 1004 (Lee '255), Fig. 12E, [01130, [0114], [0133]; Ex. 1003, ¶208.

A POSITA would have found it obvious to employ such doped lower active pattern 250 in combination with high concentration region 122 because Lee '255 teaches that it is an alternative configuration within its inventive concept that

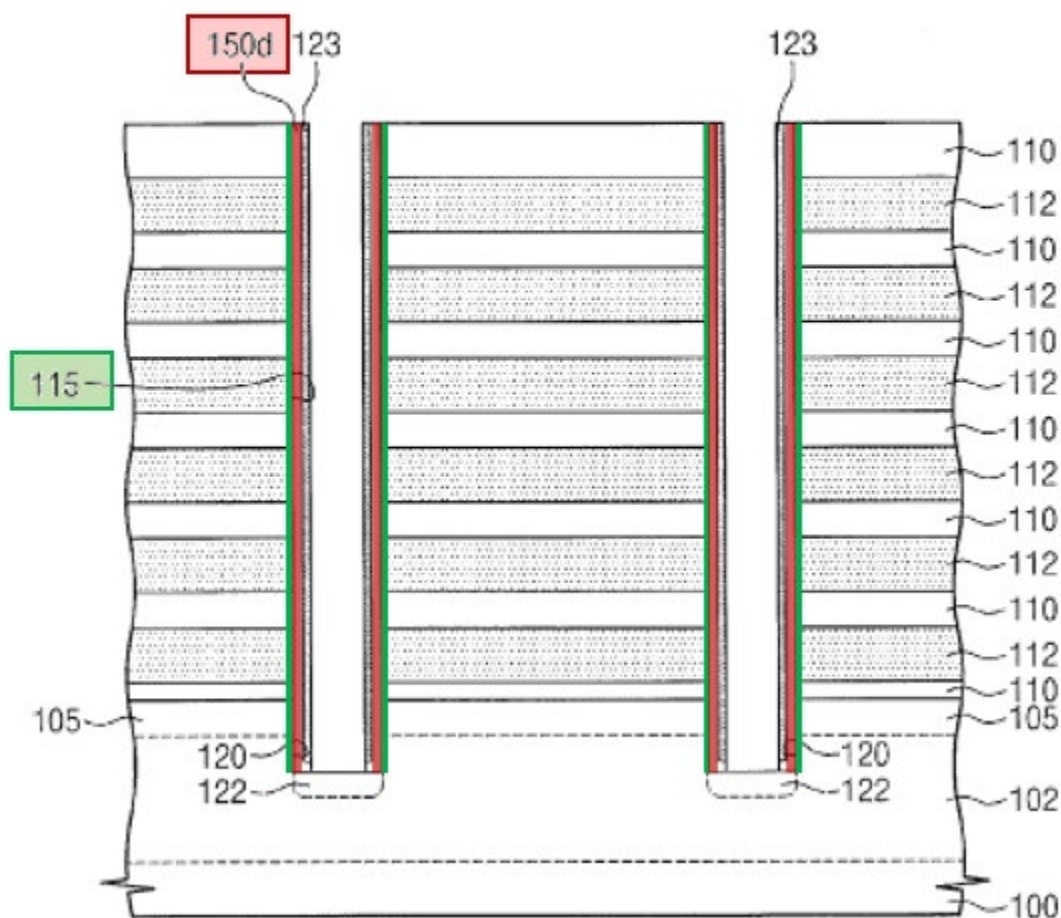
provides improved reliability. Ex. 1004 (Lee '255), [0113], [0118]; Ex. 1003, ¶209.

[1b]	forming on sidewalls of the opening a blocking dielectric layer;
[1c]	forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region;
[1d]	forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and

Lee '255 teaches [1b] *forming on sidewalls of the opening a blocking dielectric layer*; [1c] *forming on an inside sidewall of the blocking dielectric layer a . . . charge storing region*; and [1d] *forming on an inside sidewall of the . . . charge storing region a tunnel dielectric layer* because Lee '255 teaches forming a dielectric gate layer 150d in opening 115, with successive blocking, charge-trapping, and tunneling sub-layers in the sequence and relative position required by limitations [1b], [1c], and [1d]. *See, e.g.*, Ex. 1004 (Lee '255), Figs. 4A, 4B, 5A, 5B, [0055], [0056], [0077]; Ex. 1003, ¶211.

Lee '255 teaches that gate dielectric layer 150d is formed on “the inner sidewall of an opening 115.” Ex. 1004 (Lee '255), [0077]. This is depicted, for example, in figure 9A (with green annotations highlighting the sidewalls of opening 115 and maroon annotations highlighting gate dielectric layer 150d):

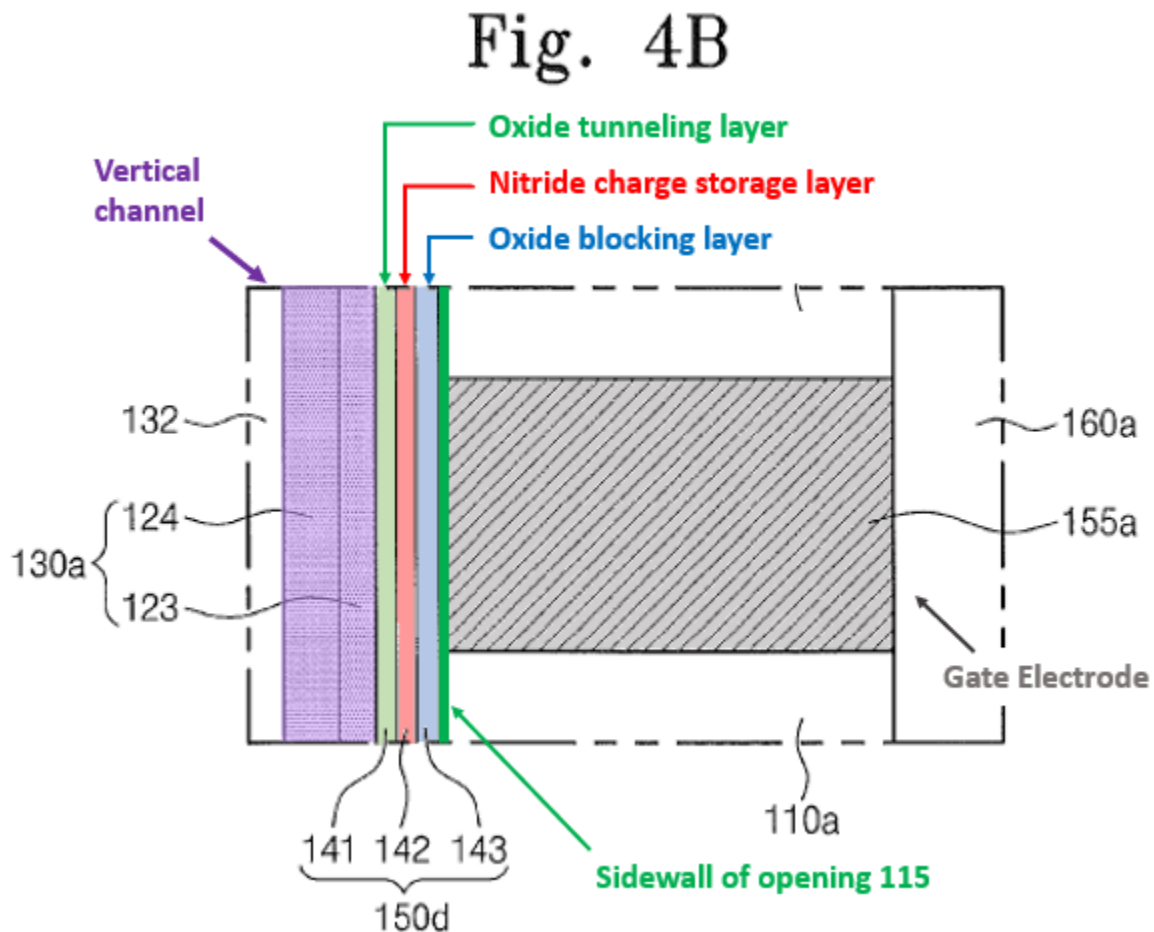
Fig. 9A



Ex. 1004 (Lee '255), Fig. 9A; *see also id.*, Fig. 4A; Ex. 1003, ¶¶212-213.

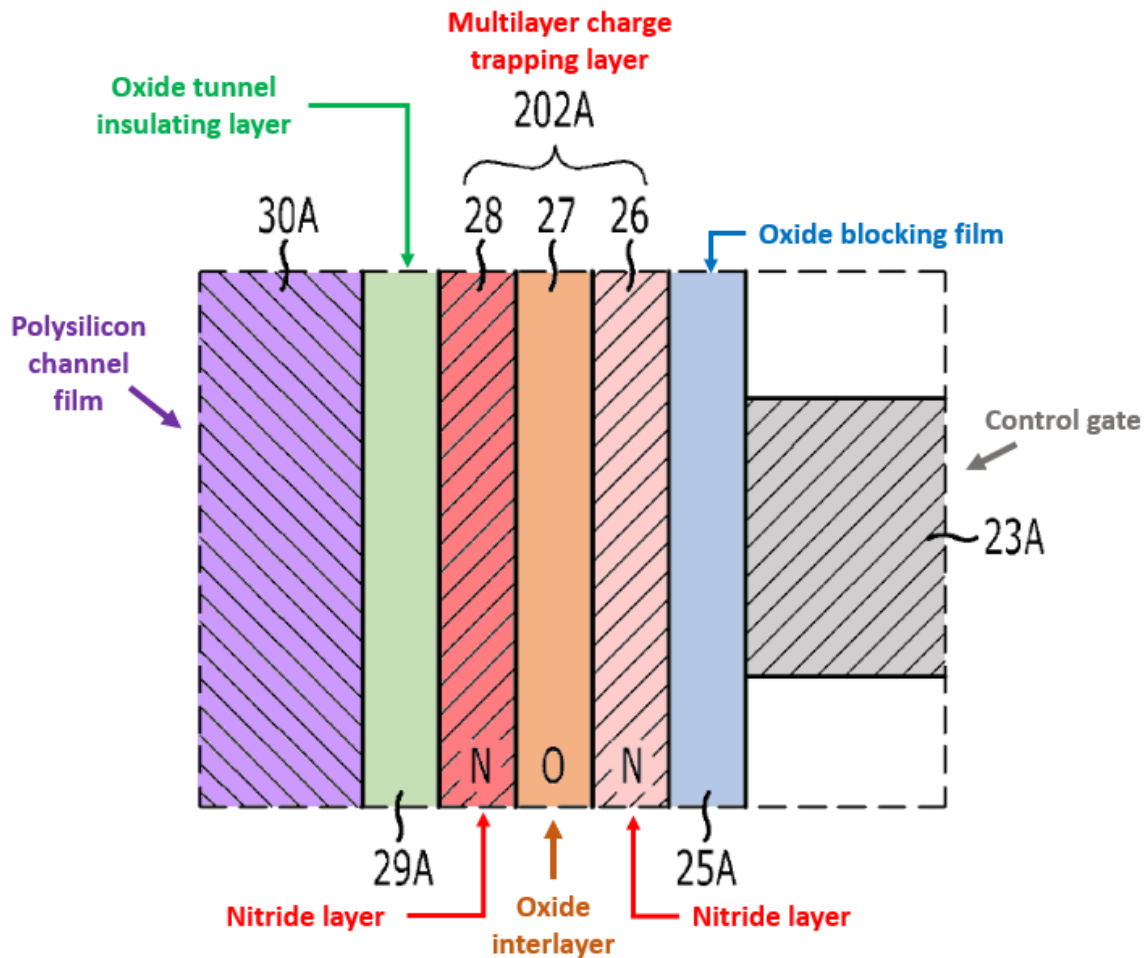
Figure 4B provides further details on the layers of gate dielectric layer 150b, showing that (i) blocking dielectric layer 143 (*a blocking dielectric layer*) (blue) is *form[ed] on the sidewalls of the opening* (opening 115) (green); (ii) charge storage layer 142 (*a . . . charge storage region*) (red) is *form[ed] on an inside sidewall of the blocking dielectric layer* (blue); and (iii) tunneling layer 141 (*a tunnel*

dielectric layer) (light green) is form[ed] on the sidewall of the . . . charge storing region (red):



Ex. 1004 (Lee '255), Fig. 4B, [0056], [0074]; Ex. 1003, ¶¶214-215.

A POSITA would have been motivated to modify the charge storage layer 142 of Lee '255 based on the teachings of Lee '961. *See* Limitation [35d], above; Ex. 1003, ¶216. This modification would have resulted in a multilayer charge storage region in Lee '255, modeled on region 202A of Lee '961:



As reflected above, modifying the charge storage layer of Lee '255 based on the teachings of Lee '961 would not have changed the position of that layer relative to the blocking and tunneling layers. The modified charge storage layer would be formed *on an inside sidewall of the blocking dielectric layer* (blue). Further, the tunneling layer (green) would be formed *on an inside sidewall of the multi-layer charge storing region*. Ex. 1003, ¶¶217-222.

[1e]	forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.
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Lee '255 teaches a *vertical channel* because Lee '255 teaches forming vertical active pattern 130/130a. *See* Limitation [35b]; Ex. 1003, ¶225.

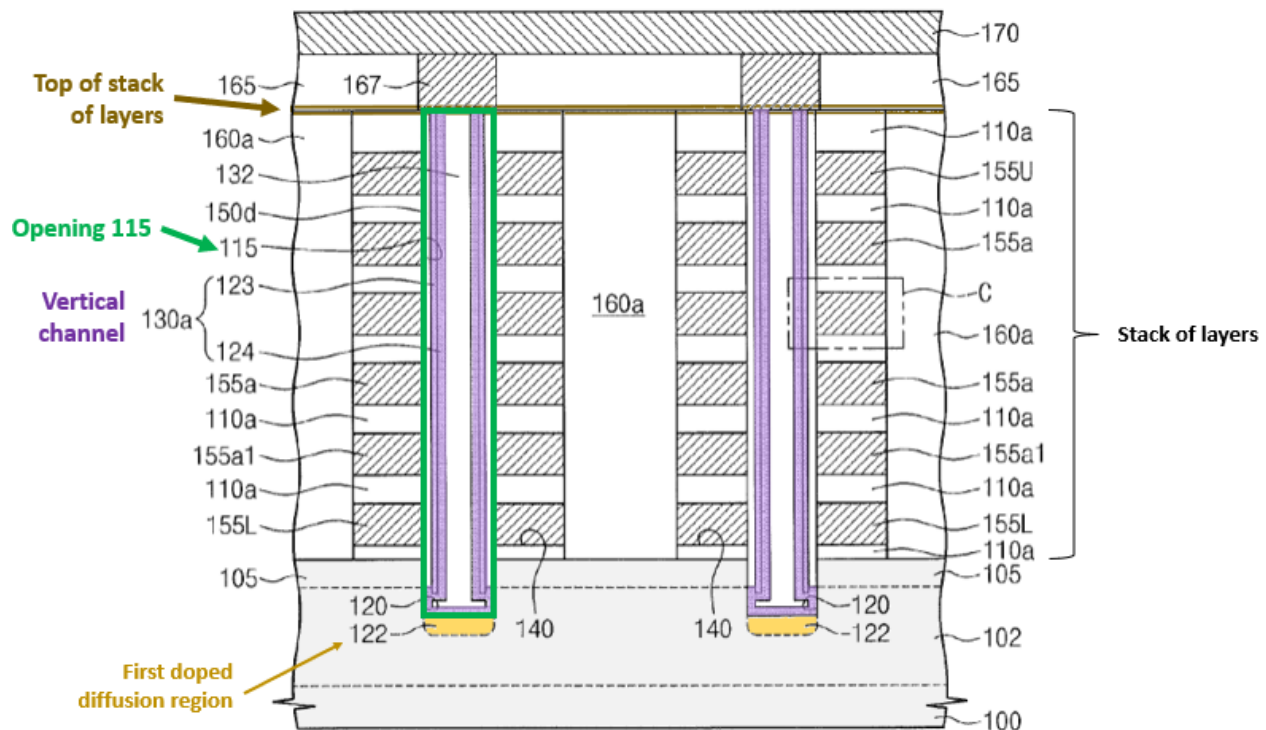
Lee '255 teaches that vertical active pattern 130/130a (the *vertical channel*) *ha[s] semiconductor material* because Lee '255 teaches “the vertical active pattern 130 may include the same semiconductor material as that of substrate 100”—e.g., silicon—and “may have a polycrystalline state or a single crystalline state.” Ex. 1004 (Lee '255), [0062], [0050]; Ex. 1003, ¶226.

Lee '255 teaches that the vertical active pattern 130/130a is *form[ed] on an inside sidewall of the tunnel dielectric layer* because Lee '255 teaches that “[t]he tunnel dielectric layer 141 may be adjacent to the sidewall of the vertical active pattern 130.” Ex. 1004 (Lee '255), [0056]; *see also id.*, [0105]; Ex. 1003, ¶227.

The position of the *vertical channel* (purple) on *an inside sidewall of the tunnel dielectric layer* (light green) is further taught in figure 4B:

A cross-sectional view of a semiconductor device. A vertical channel (130a) is formed in a substrate (110a). The channel is lined with an oxide tunneling layer (123) and a nitride charge storage layer (124). An oxide blocking layer (125) is located on the sidewall of the opening (115). The channel is capped with a gate electrode (160a). The device is surrounded by a gate electrode (155a). The substrate (110a) is shown with a dashed line indicating the bottom of the channel. The channel is labeled with 132, 124, 123, 141, 142, 143, and 150d. The gate electrode is labeled with 160a, 155a, and 110a. The sidewall of the opening is labeled with 115.

Lee '255 teaches the vertical active pattern 130/130a *extend[s] from the first doped diffusion region through the opening to a top of the stack of layers* because Lee '255 teaches that the vertical active pattern 130 extends through opening 115 (*the opening*) from “[t]he high concentration region 122 of the first conductive dopant” (*the first doped diffusion region*) and “may pass through the stack-structure” (*the stack of layers*). Ex. 1004 (Lee '255), Figs. 1A, 4A, [0052]; [0053], [0077], [0081]. This is also depicted in figure 4B:



Ex. 1004 (Lee '255), Fig. 4B; Ex. 1003, ¶228.

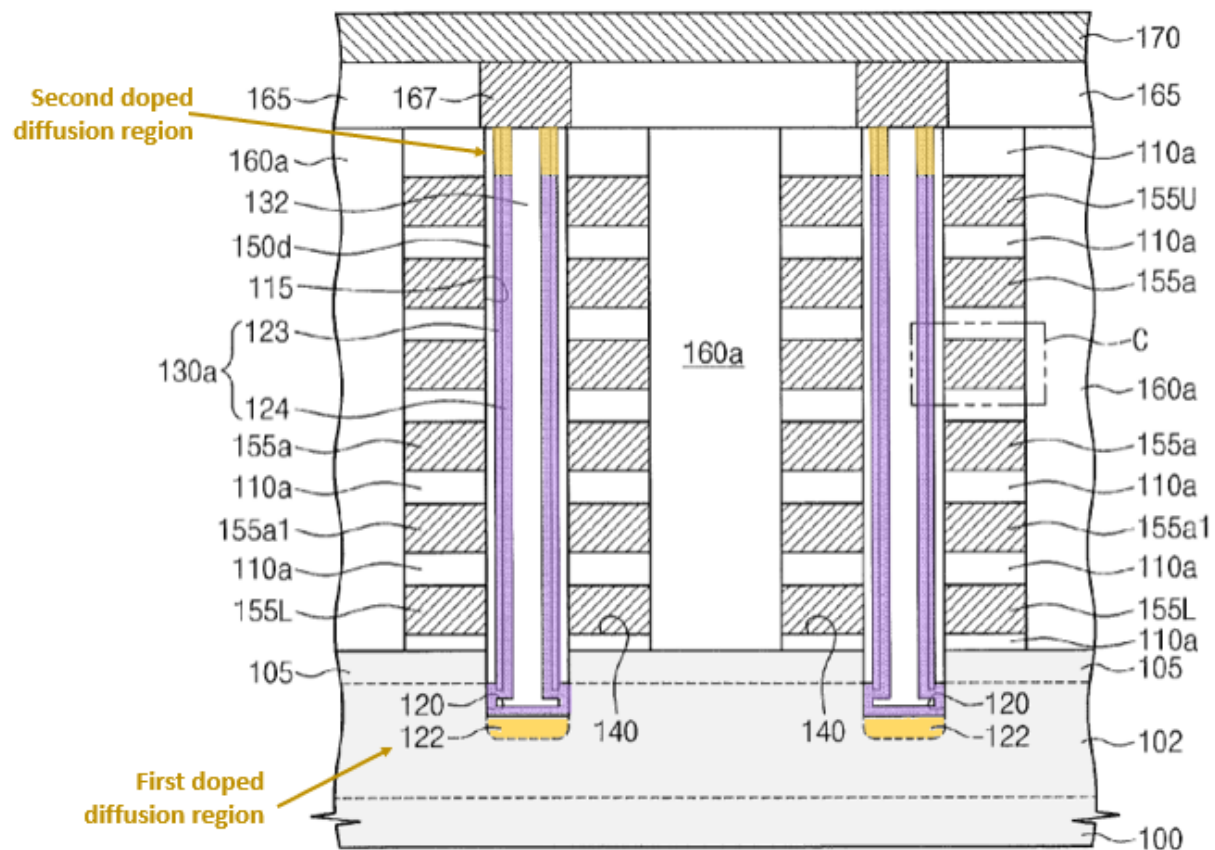
5. Dependent claims 2, 3, 5, 9-12, 14-22

Claims 2, 3, 5, 9-12, and 14-22, which depend from claim 1, are also obvious based on the teachings of Lee '255 in view of Lee '961.

2. The method of claim 1, further comprising the step of forming a second diffusion region such that the vertical channel connects the first and second diffusion regions.

Lee '255 teaches the additional limitations of claim 2 because Lee '255 teaches that a “drain being doped with the second conductive dopant may be formed in the upper portion of the vertical active pattern 130. A lower surface of the drain may be disposed on a level adjacent to an upper surface of the uppermost

gate pattern 155U” (*forming a second diffusion region*). Ex. 1004 (Lee ’255), [0063]; Ex. 1003, ¶¶229-231; Ex. 1001 (’365 patent), 8:59-62 (identifying a drain region is an example of a diffusion region). This drain region is identified in annotated FIG. 4A below.



Ex. 1004 (Lee ’255), Fig. 4A; Ex. 1003, ¶230.

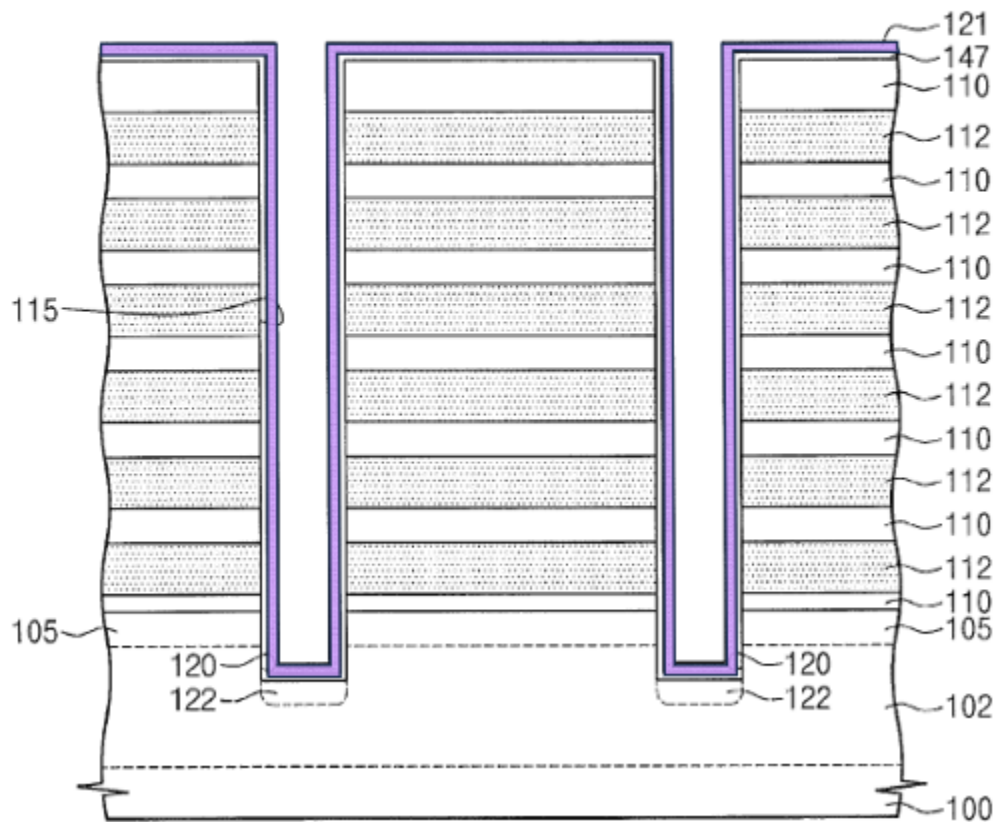
Lee ’255 further teaches that the vertical active pattern 130/130a (*the vertical channel*) connects the upper drain region (*the second diffusion region*) and high concentration region 122 (*the first diffusion region*) because Lee ’255 teaches that the high concentration region 122, the active pattern 130/130a, and the drain

are all physically connected. *See* Ex. 1004 (Lee '255), Fig. 4A, above; Ex. 1003, ¶232. Lee '255 also teaches that the vertical active pattern 130/130a electrically connects the two diffusion regions. Ex. 1004 (Lee '255), [0053], [0063]-[0064]; Ex. 1003, ¶233.

3. The method of claim 1, further comprising forming a layer of semiconductor material including a second doped diffusion region over a top surface of the stack of layers and the opening, wherein the vertical channel electrically couples the first doped diffusion region to the second doped diffusion region.
--

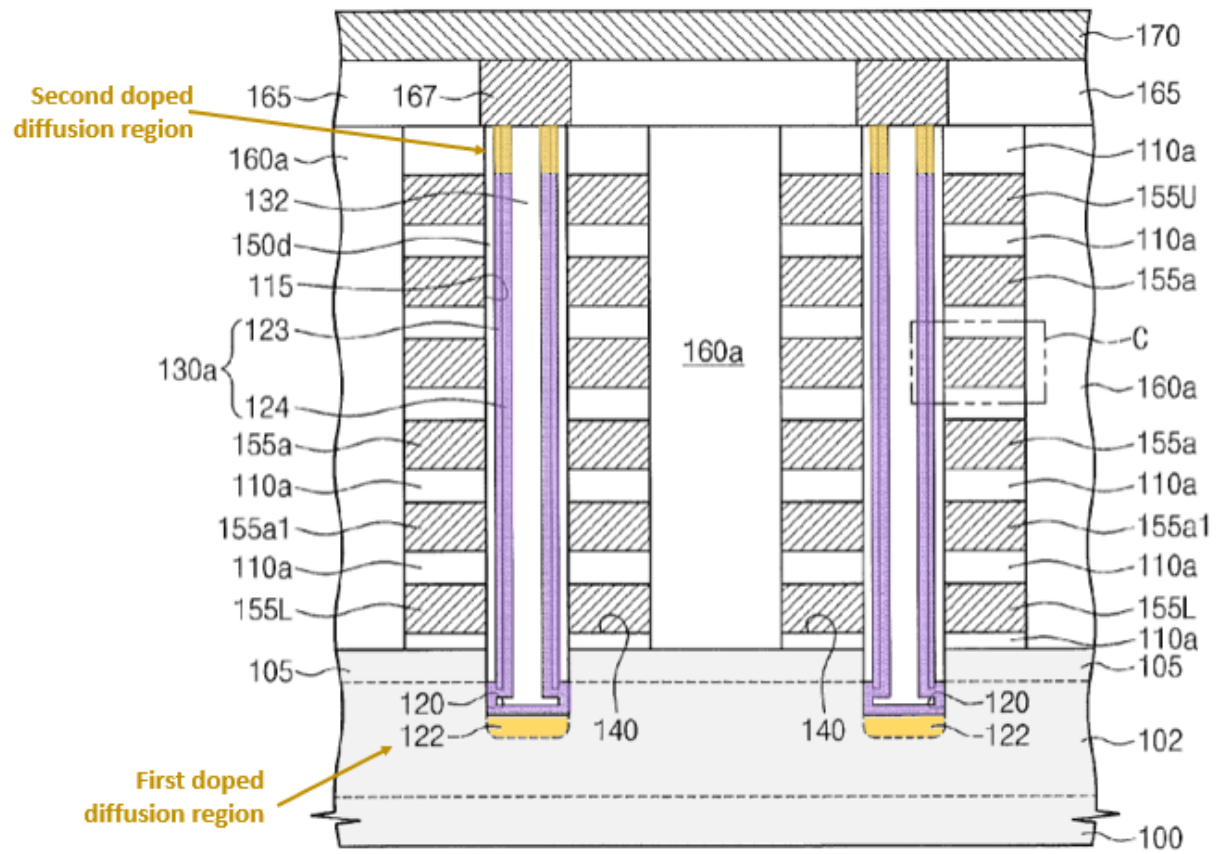
Lee '255 teaches *forming a layer of semiconductor material ... over a top surface of the stack of layers and the opening* because Lee '255 teaches that the first and second semiconductor patterns 123 and 124 (*layers of semiconductor material*) are “conformally formed.” Ex. 1004 (Lee '255), [0105], [0106]; Ex. 1003, ¶¶234-236. A POSITA would have understood that “conformally formed” means that the semiconductor layers are formed over the entire upper surface of the layer stack and along the walls of opening 115 before the layers are etched. Ex. 1003, ¶¶237-239. Lee '255 gives an example of the process of “conformally forming” with respect to semiconductor layer 121 in Fig. 8A and a POSITA would have understood that the “conformally forming” process would have been the same for semiconductor patterns 123 and 124 of figure 9:

Fig. 8A



Ex. 1004 (Lee '255), Fig. 8A, [0099]-[0100]; Ex. 1003, ¶¶236-238.

Lee '255 teaches that, once the semiconductor layers are conformally formed and etched, the semiconductor material *include[es] a second doped diffusion region*, as shown in this annotated version of figure 4A:



Ex. 1004 (Lee '255), Fig. 4A; Ex. 1003, ¶240; *see also* claim 2, *supra*.

Lee '255 teaches that vertical channel 130/130a *electrically couples the first doped diffusion region to the second doped diffusion region* for the reasons set forth above. *See* claim 2; Ex. 1003, ¶241.

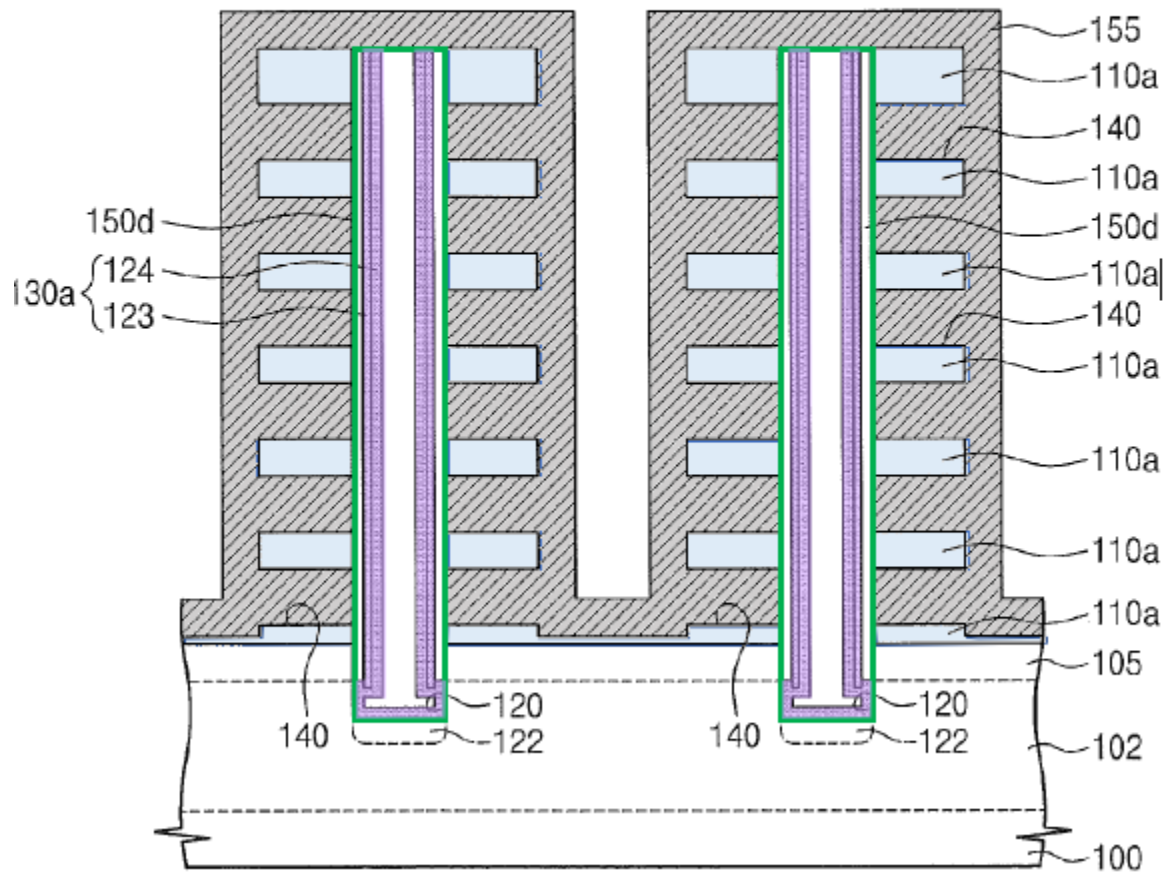
5. The method of claim 1, wherein the blocking dielectric layer includes a high K dielectric.
20. The method of claim 19, wherein the blocking dielectric layer includes a high K dielectric.

See claim 36, *supra*. Ex. 1003, ¶¶242-245.

- | |
|---|
| <p>9. The method of claim 1, further comprising the step of etching the sacrificial layer to form a second opening.</p> <p>10. The method of claim 9, further comprising the step of depositing a gate electrode in the second opening.</p> |
|---|

Lee '255 teaches the additional limitations of claims 9 and 10 because Lee '255 teaches removing sacrificial layers 112a (*the sacrificial layer*) to form “empty regions” 140 (*a second opening*) that are then filled with gate conductive layer 155 (*depositing a gate electrode*). Ex. 1004 (Lee '255), Figs. 8E, 9B-9D, [0103], [0106]-[0108]; Ex. 1003, ¶¶246-252. For example, figure 9C shows the sacrificial layers etched and replaced with gate layer 155:

Fig. 9C



Ex. 1004 (Lee '255), Fig. 9C, [0107]; Ex. 1003, ¶¶247-251.

- 11. The method of claim 10, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.**

See claim 45, *supra*. Ex. 1003, ¶¶253-254.

- 12. The method of claim 10, wherein the deposited gate electrode is a high work function gate electrode.**

See claim 37, *supra*. Ex. 1003, ¶¶255-256.

14. The method of claim 1, wherein the vertical channel formed includes an annular region.

19. The method of claim 14, wherein the blocking dielectric layer is formed in a substantially annular shape.

21. The method of claim 19, wherein the multi-layer charge storing region is formed in a substantially annular shape.

22. The method of claim 21, wherein the tunnel dielectric layers is formed in a substantially annular shape.

See claim 35, Limitations [35b]-[35e], supra. Ex. 1003, ¶¶257-259.

15. The method of claim 14, wherein at least a portion of the vertical channel is formed of polysilicon.

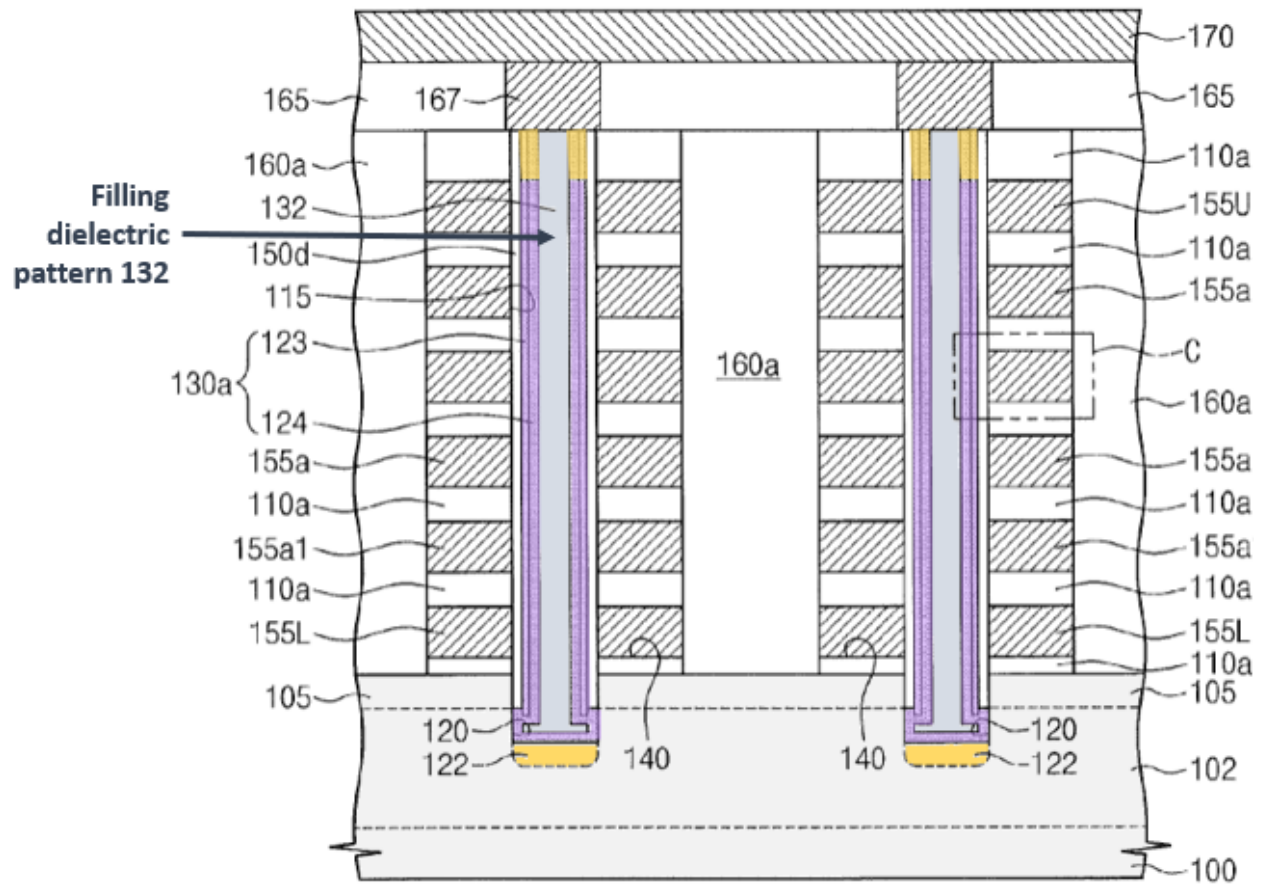
16. The method of claim 14, wherein the vertical channel formed includes a layer of semiconductor material surrounding a cylinder of filler material.

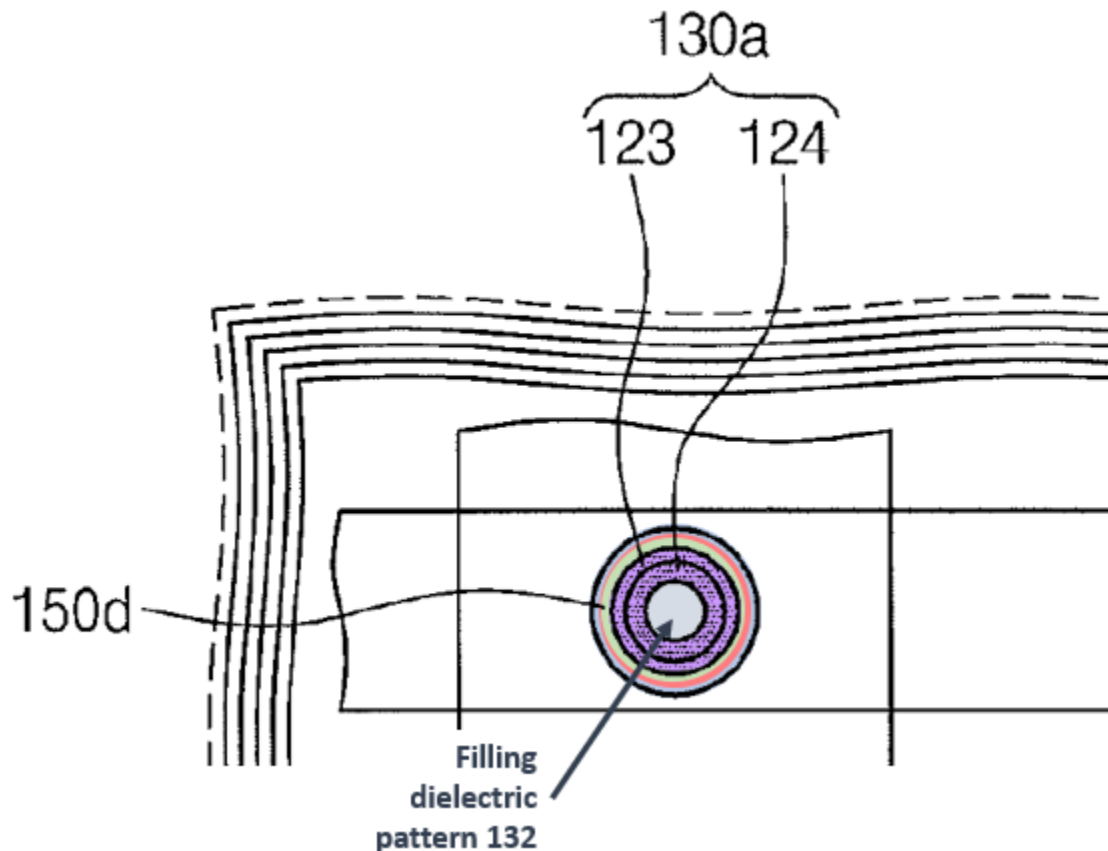
17. The method of claim 14, wherein the vertical channel formed includes an outer layer of semiconductor material.

18. The method of claim 17, wherein the outer layer of semiconductor material is formed of polysilicon.

Lee '255 teaches the additional limitations of claims 15, 16, 17, and 18 because Lee '255 teaches that: (i) vertical active pattern 130/130a (*the vertical channel*) may be formed of silicon (*a semiconductor material*) in “a polycrystalline state” (*formed of polysilicon*) (Ex. 1004 (Lee '255), [0062], [0114]); and (ii) the vertical channel “may have a hollow pipe shape ... [and] [t]he inside of the vertical active pattern 130 may be filled with a filling dielectric pattern 132” (*an outer layer of semiconductor material surrounding a cylinder of filler*

material) (*id.*, [0054]). Ex. 1003, ¶¶260-262. This is depicted in figures 4A and 5A:





Ex. 1004 (Lee '255), Figs. 4A, 5A; see also *id.*, Fig. 5B, [0075].

6. Independent claim 23

[23pre] A method comprising:

See claim 1, Limitation [1pre], supra. Ex. 1003, ¶263.

[23a1] forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;

See claim 1, Limitation [1a1], supra. Ex. 1003, ¶264.

[23a2]	forming an opening extending through the stack of layers towards the substrate;
---------------	--

See claim 1, Limitation [1a2], *supra*. Ex. 1003, ¶265.

[23b]	forming on sidewalls of the opening an annular shaped blocking dielectric layer;
[23c]	forming on an inside sidewall of the blocking dielectric layer an annular shaped multi-layer charge storing region;
[23d]	forming on an inside sidewall of the multi-layer charge storing region an annular shaped tunnel dielectric layer; and
[23e]	forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layers.

See claim 1, Limitations [1b]-[1e] (forming layers), and claim 35, Limitations [35b]-[35e] (layers with annular shapes), *supra*. Ex. 1003, ¶266.

7. Dependent claims 28-33

Claims 28-33, which depend from claim 23, are also obvious based on the teachings of Lee '255 in view of Lee '961.

28. The method of claim 23, further comprising the step of etching the sacrificial layer to form a second opening.

See claim 9, *supra*. Ex. 1003, ¶¶267-268.

29. The method of claim 28, further comprising the step of depositing a gate electrode in the second opening.
--

See claim 10, *supra*. Ex. 1003, ¶¶269-270.

30. The method of claim 29, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.

See claim 11, supra. Ex. 1003, ¶¶271-272.

31. The method of claim 29, wherein the deposited gate electrode is a high work function gate electrode.

See claim 37, supra. Ex. 1003, ¶¶273-274.

32. The method of claim 29, wherein the blocking dielectric layer includes a high K dielectric.

See claim 36, supra. Ex. 1003, ¶¶275-276.

33. The method of claim 32, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.

See claim 45, supra. Ex. 1003, ¶¶277-278.

B. Ground 2: Obviousness over Lee '255, Lee '961, and Fujiwara

A POSITA would have found claims 6-8, 25-27, 34, and 38-41 of the '365 patent obvious over the teachings of Lee '255 in view of Lee '961. Ex. 1003 ¶¶279-312.

1. Overview of combination

As set forth above, a POSITA would have been motivated to modify the charge storage layer of Lee '255 based on Lee 961's teachings regarding a multi-layer charge storage layer configuration that improves data retention of nonvolatile memory devices.

Fujiwara, like Lee '961, teaches a NVM device with a multi-layer charge storage region. Ex. 1006 (Fujiwara), Fig. 21, [0003], [0197], [0205]; Ex. 1003, ¶281. Fujiwara additionally teaches the optimal oxygen concentrations for the multiple charge storage layers—using an oxygen-rich lower nitride layer and an oxygen-lean upper nitride layer to further promote charge retention. Ex. 1006 (Fujiwara), [0197]-[0218], Figs. 21, 22.

As discussed below, a POSITA would have found it obvious to further modify the combination of Lee '255 and Lee '961 in view of Fujiwara's teachings concerning optimized oxygen concentrations. Ex. 1003, ¶282. This combination of Lee '255, Lee '961, and Fujiwara differs from the prior art the Examiner considered during prosecution because the combination teaches the limitations the Examiner found missing from the prior art. Ex. 1003, ¶ 283.

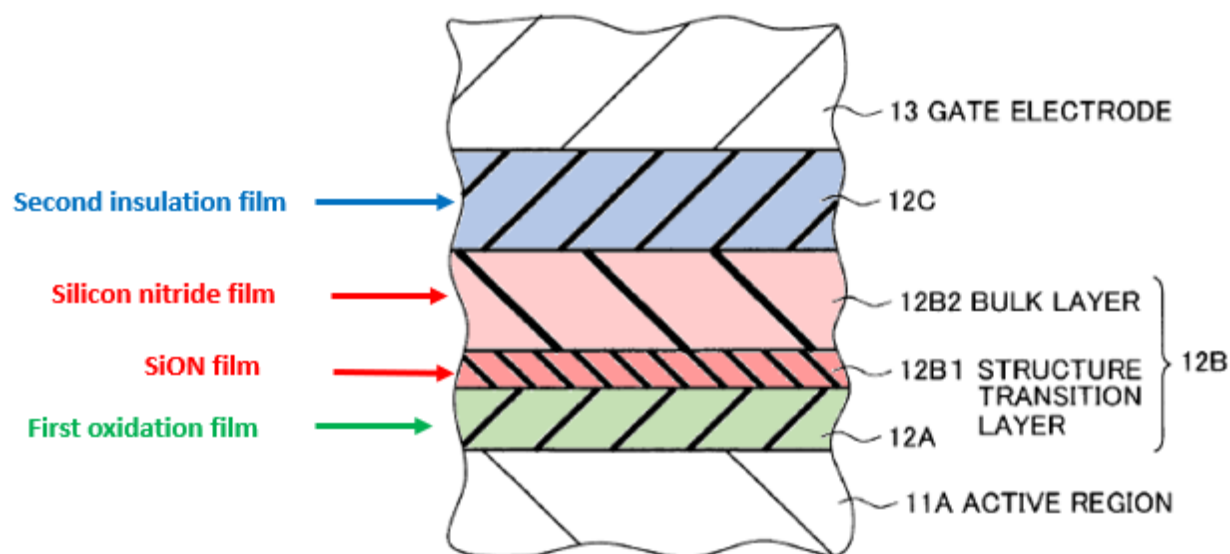
2. Dependent claims 6-8, 25-27, 34, and 38-41

- 6. The method of claim 1, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.
- 25. The method of claim 23, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.
- 34. The method of claim 33 wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.
- 38. The semiconductor memory device of claim 35, wherein the multi-layer charge storing region includes a first oxygen-lean nitride layer and a second oxygen-rich nitride layer.

The combination of Lee '255, Lee '961, and Fujiwara teaches the additional limitations of claims 6, 25, 34, and 38. Ex. 1003, ¶¶284-301.

As set forth above, the combination of Lee '255 and Lee '961 teaches a *multi-layer charge storing region*. See Limitation [35d]; Ex. 1003, ¶286. Fujiwara also teaches a multi-layer charge storing region that includes a silicon nitride “bulk layer” 12B2 (a [*first*] *oxygen-lean nitride layer*) and a silicon oxynitride (SiON) “transition layer” 12B1 (a [*second*] *oxygen-rich nitride layer*), as shown in figure 21:

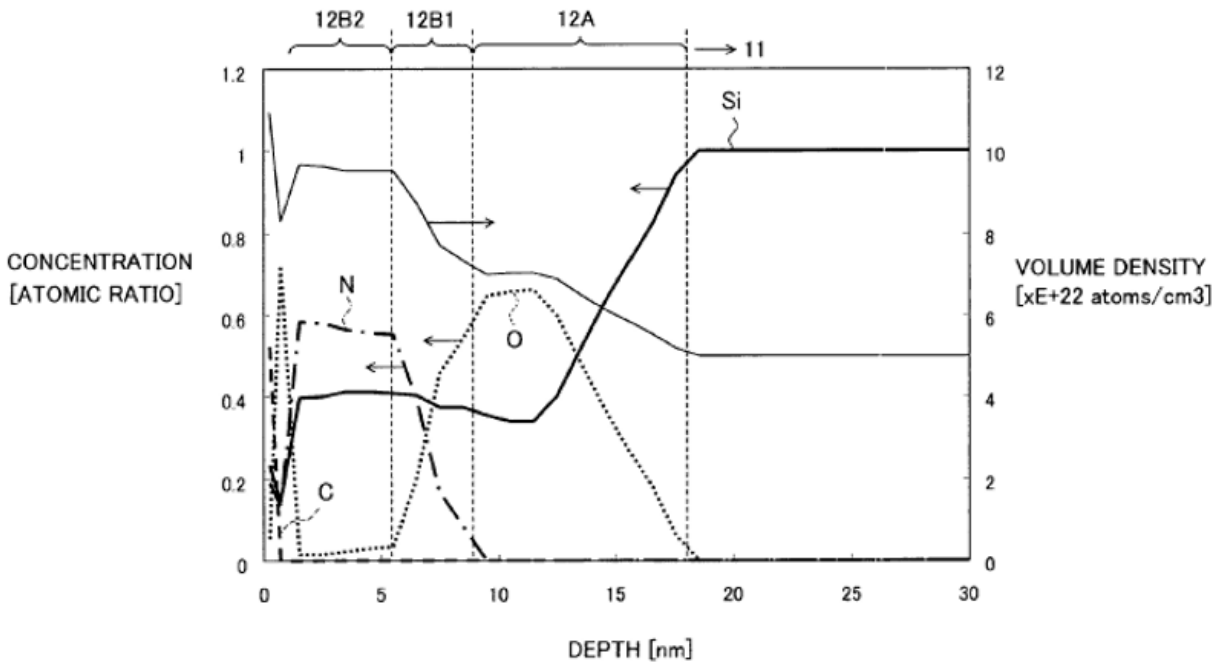
FIG. 21



Ex. 1006 (Fujiwara), Fig. 21; *see also id.*, Fig. 2, [0074], [0198]–[0201], [0212], [0215]–[0218]; Ex. 1003, ¶¶289-292.

In figure 22, Fujiwara provides atomic composition profiles for the layers, showing: (i) the upper nitride layer (12B2) is *oxygen-lean* (with less than about 5% oxygen throughout); and (ii) the lower nitride layer (12B1) is *oxygen-rich* (peaking at about 50% oxygen):

FIG. 22



Ex. 1006 (Fujiwara), Fig. 22 (dotted line representing “O”); *see also id.*, [0200];

Ex. 1003, ¶¶293-295.

With respect to layer 12B1, a POSITA would have understood that layer qualifies as *oxygen-rich* because the oxygen concentrations exceed about 15% atomic concentration for the vast majority of the layer. Ex. 1003, ¶294. Figure 23 of Fujiwara also confirms the *oxygen-rich* nature of layer 12B1 because it shows that layer 12B1 has a refractive index of up to ~2.10, which shows that the layer reaches an atomic oxygen concentration between 60-67%. *Id.*

- a. **Motivation to combine Fujiwara with Lee '255 and Lee '961 and expectation of success**

A POSITA would have been motivated to further modify the combination of Lee '255 and Lee '961 to apply the teachings of Fujiwara to optimize the oxygen concentrations of the nitride layers of the multi-layer charge-trapping region. Ex. 1003, ¶¶296-300.

As an initial matter, it would have been obvious for a POSITA to consult the teachings of Fujiwara to improve the memory transistor configuration of Lee '255 and Lee '961 because Fujiwara is directed to improving the configuration of SONOS-type charge trapping memory transistors. Ex. 1006 (Fujiwara), FIG. 1, [0010]-[0013]; Ex. 1003, ¶297. Additionally, Fujiwara's teaching of optimizing oxygen concentrations in nitride layers to improve charge retention is complementary to the combination of Lee '961 and Lee '255, which also has the goal of improving data retention. Ex. 1003, ¶297; *compare* Ex. 1005 (Lee '961), [0008], [0010] *with* Ex. 1006 (Fujiwara), [0197], [0205].

A POSITA also would have understood that Fujiwara provides an express teaching and suggestion to combine because Fujiwara teaches using the oxygen-rich/oxygen-lean configuration to improve the charge retention characteristics of a SONOS NVM device, which is also one of the goals of Lee '961. Ex. 1006 (Fujiwara), [0197]; Ex. 1003, ¶298. As such, a POSITA would have understood that the combination of Fujiwara with Lee '255 and Lee '961 amounts to applying

the teachings of Fujiwara for their intended purpose to improve similar devices in the same way. Ex. 1003, ¶298.

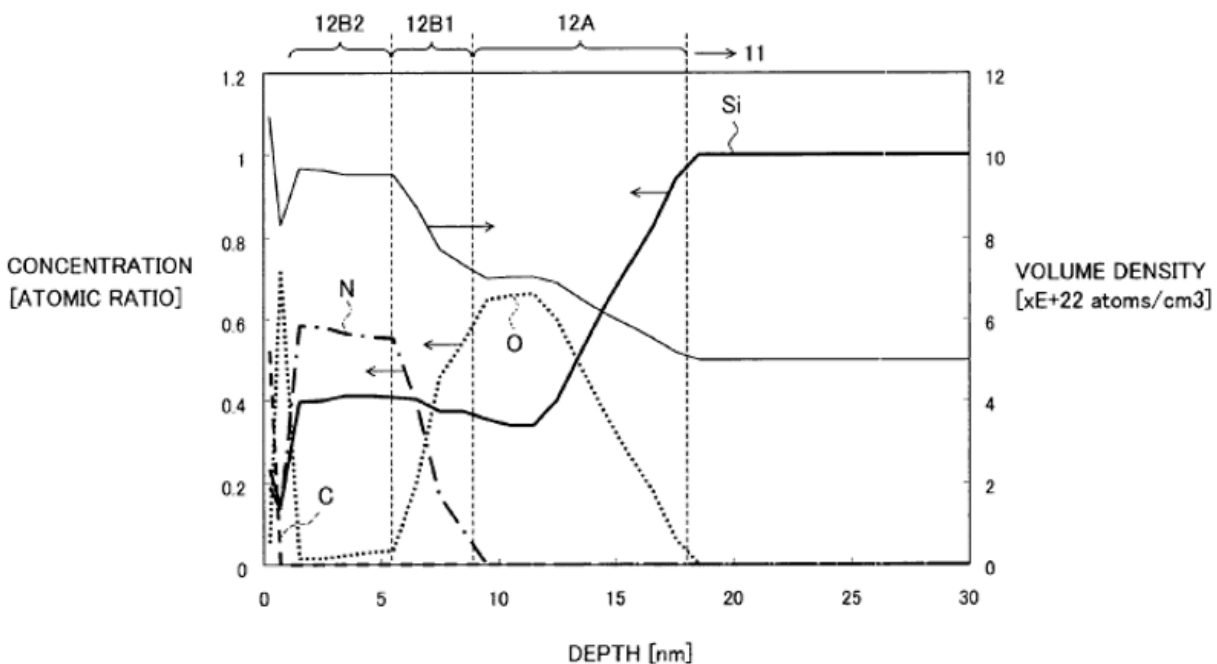
Applying the teachings of Fujiwara to Lee '255/Lee '961 also would have amounted to combining prior art elements according to known methods to obtain predictable benefits. Ex. 1003, ¶299. Indeed, prior to July 2012, it was a routine design choice to use an oxygen-rich first nitride layer and a silicon-rich, oxygen-lean second nitride layer to improve charge retention characteristics in both SONNOS and SONONOS configurations. *Id.* (citing Ex. 1012 (Heo), [0058]-[0068]; Ex. 1017 (Lai '676), [0015], [0068]-[0077]; Ex. 1011 (Levy), [0025]-[0026]; Ex. 1013 (Ganguly), Fig. 3, [0048]-[0050]; and Ex. 1021 (Higuchi) [0007], [0133]-[0134], [0141]-[0142]).

A POSITA also would have expected success in applying Fujiwara's teachings concerning optimized oxygen concentrations to the multilayer charge trapping region of Lee '255 / Lee '961 because the underlying materials, equipment, and processes are all mainstream. Ex. 1003, ¶300. A POSITA would reasonably predict that implementing Fujiwara's teaching of oxygen-rich and oxygen-lean nitride layers in the existing Lee '255 / Lee '961 stack framework could be achieved with routine process-tuning and would deliver the same data-retention benefits without introducing new reliability risks. *Id.*

39. The semiconductor memory device of claim 38, wherein the first oxygen-lean nitride layer and the second oxygen-rich nitride layer both include silicon, nitrogen and oxygen components.

The combination of Lee '255, Lee '961, and Fujiwara teaches the additional limitations of claim 39 because Fujiwara teaches that both nitride layers 12B2 and 12B1 have silicon, nitrogen, and oxygen components in the concentration profile set forth in figure 22 (*see* "O," "N," and "Si" lines):

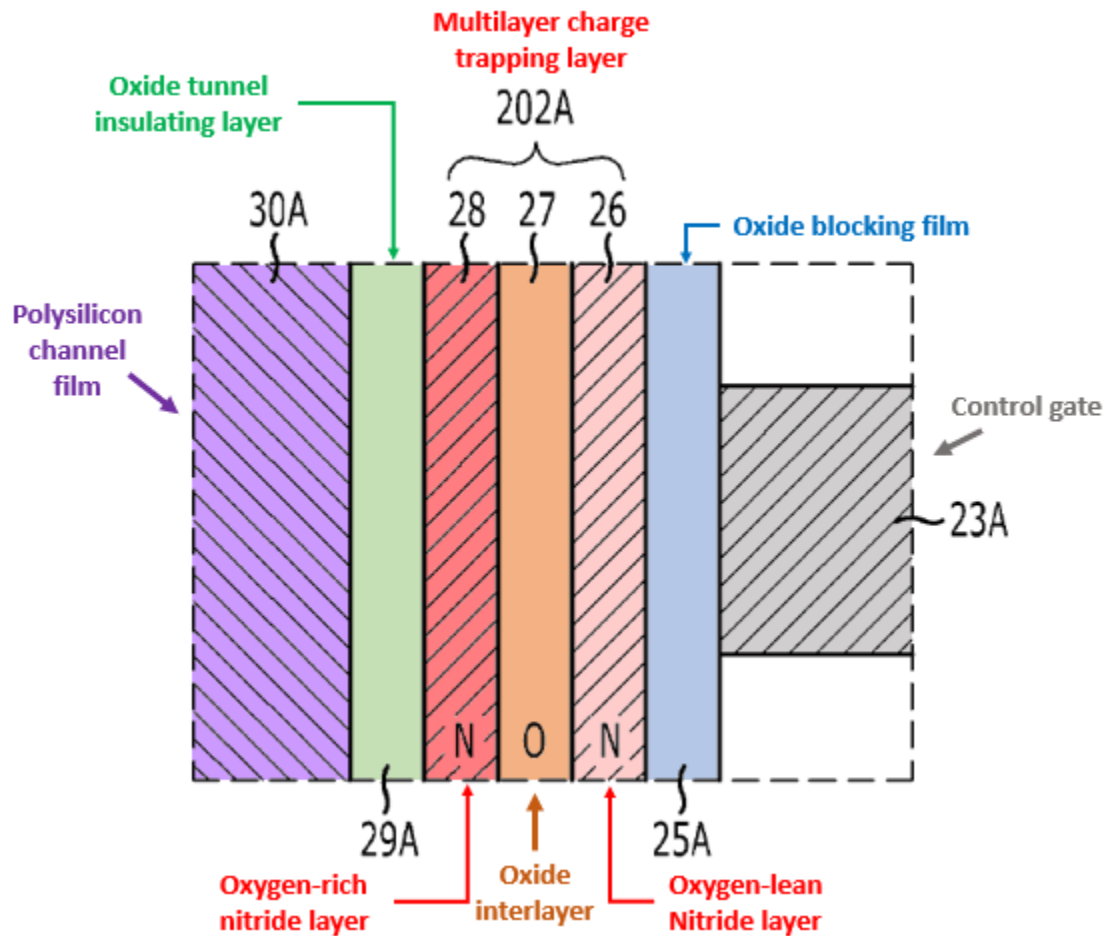
FIG. 22



Ex. 1006 (Fujiwara), Fig. 22, [0200]; Ex. 1003, ¶¶301-302.

- | |
|---|
| <p>7. The method of claim 6, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.</p> <p>26. The method of claim 25, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.</p> <p>40. The semiconductor memory device of claim 39, wherein the first oxygen-lean nitride layer is formed on an inside sidewall of the blocking dielectric layer and wherein the second oxygen-rich nitride layer is formed on the inside sidewall of the first oxygen-lean nitride layer.</p> |
|---|

The combination of Lee '255, Lee '961, and Fujiwara also teaches the additional limitations of claims 7, 26, and 40. Ex. 1003, ¶¶303-306. Fujiwara teaches that (i) the oxygen-rich nitride layer is positioned near the tunneling layer; and (ii) the oxygen-lean nitride layer is positioned near the blocking layer. Ex. 1006 (Fujiwara), Figs. 21, 22; *see also id.*, [0212], [0215], [0218]. A POSITA would have found it obvious to retain the same relative positioning when applying the teachings of Fujiwara to further modify the combination of Lee '255 and Lee '961. Ex. 1003, ¶305. As modified based on Fujiwara, the oxygen-rich and oxygen lean layers of the multilayer charge trapping layer would be arranged as follows:



Ex. 1005 (Lee '961), Fig. 2b (as modified based on Fujiwara); Ex. 1003, ¶305.

As reflected above, the resultant *[first] oxygen-lean nitride layer* (layer 26) *is formed on the inside sidewall of the blocking dielectric layer*. Meanwhile, the *[second] oxygen-rich nitride layer* (layer 28) *is formed on the inside sidewall of the oxygen-lean nitride layer*, but with an intermediate oxide layer (layer 27). As set forth in the claim construction section, above, a POSITA would have understood that, even though there is an intervening oxide interlayer 27 between nitride first

trap layer 26 and nitride second trap layer 28, layer 28 is still understood to be “formed on” the sidewall of layer 26. Ex. 1003, ¶306.

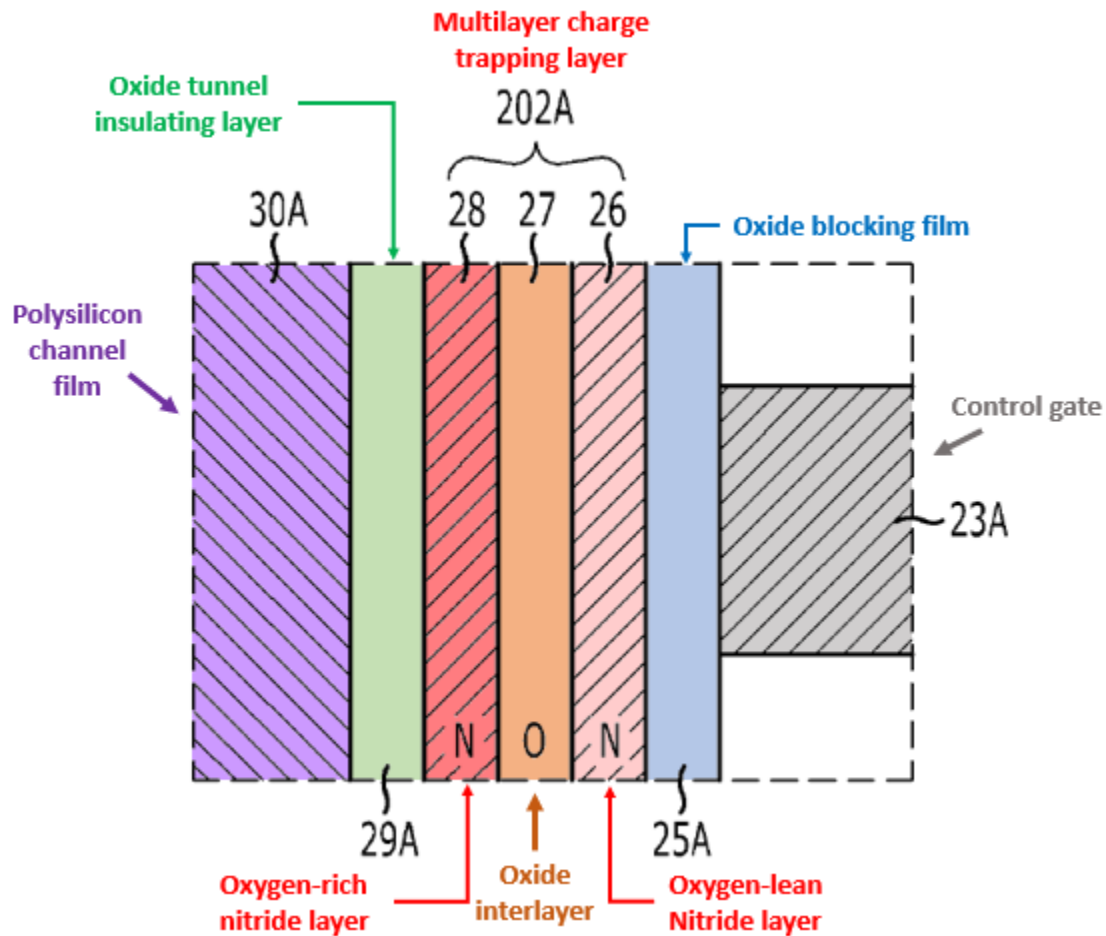
41. The semiconductor memory device of claim 40, wherein the blocking dielectric layer includes a high K dielectric.

See claim 36, supra. Ex. 1003, ¶¶307-308.

8. The method of claim 6, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.

27. The method of claim 26, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.

The combination of Lee '255, Lee '961, and Fujiwara teaches the additional limitations of claims 8 and 27 because Lee '961 teaches the arrangement of oxide interlayer 27 (*anti-tunneling layer*) *between* its nitride first trap layer 26 (*oxygen-lean nitride layer*) and nitride second trap layer 28 (*oxygen-rich nitride layer*), as shown in the annotated version of figure 2b below:



Ex. 1005 (Lee '961), Fig. 2b, [0020]; Ex. 1003, ¶¶309-310.

A POSITA would have understood oxide interlayer 27 is the *anti-tunneling layer* because Lee '916 teaches that the interlayer prevents the loss (leakage) of charges that would otherwise accumulate at an interface region. Ex. 1005 (Lee '961), [0031]-[0033]; Ex 1003, ¶311. This understanding aligns with the function of the anti-tunneling layer of the '365 patent—to lower the leakage of current. Ex. 1001 ('365 patent), 10:26-31.

VII. CONCLUSION

For the foregoing reasons, Petitioner requests *inter partes* review and that the claims 1-3, 5-12, 14-23, and 25-45 of the '365 patent be canceled as unpatentable.

VIII. STANDING

Petitioner certifies that Petitioner is not barred or estopped from requesting this *inter partes* review and the '365 patent is eligible for it.

IX. MANDATORY NOTICES AND FEES

Real Party In Interest: The real parties-in-interests here are Sandisk Technologies, Inc. and SanDisk Corporation. No other parties directed, controlled, or funded this Inter Partes Review proceeding (IPR).

Related Matters: The '365 patent is the subject of the following civil actions and administrative proceedings:

- *Sandisk Corp. v. IPValue Management, Inc., et al.*, 5:25-cv-02389 (N.D. Cal.).
- *IPValue Management, Inc., et al. v. Western Digital Corp., et al.*, 8:25-cv-00119 (C.D. Cal.).

Lead and Backup Counsel: Pursuant to 37 C.F.R. §42.8(b)(3) and 42.10(a), Petitioner designates Harper Batts (Reg. No. 56,160) as lead counsel and Jeffrey Liang (Reg. No. 69,043), Chris Ponder (Reg. No. 77,167) and Jonathan DeFosse

(provisionally recognized PTAB attorney, *pro hac vice* requested) as back-up counsel, each of Sheppard, Mullin, Richter & Hampton LLP.

Service Information: Petitioner consents to service by electronic mail addressed to:

hbatts@sheppardmullin.com,
cponder@sheppardmullin.com,
jliang@sheppardmullin.com,
jdefosse@sheppardmullin.com, and
LegalTM-Sandisk-LFMS-IPRs@sheppardmullin.com

Petitioner's counsel may also be served by mail or hand delivery at Sheppard, Mullin, Richter & Hampton LLP, 1540 El Camino Real, Suite 120, Menlo Park, CA 94025. Petitioner's counsel may be reached by telephone at (650) 815-2673 and by facsimile at (650) 815-4668.

Fees: The Office is authorized to charge fees for this Petition to Deposit Account 50-4561, Ref. 104X-409022.

Respectfully submitted,

SHEPPARD, MULLIN,
RICHTER & HAMPTON LLP

/Harper Batts/
Harper Batts (Reg. No. 56,160)

CLAIM APPENDIX

Claim 1	
[1pre]	A method comprising:
[1a1]	forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;
[1a2]	forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate;
[1b]	forming on sidewalls of the opening a blocking dielectric layer;
[1c]	forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region;
[1d]	forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and
[1e]	forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.
Claim 2	
2	The method of claim 1, further comprising the step of forming a second diffusion region such that the vertical channel connects the first and second diffusion regions.
Claim 3	
3	The method of claim 1, further comprising forming a layer of semiconductor material including a second doped diffusion region over a top surface of the stack of layers and the opening, wherein the vertical channel electrically couples the first doped diffusion region to the second doped diffusion region.

Claim 5	
5	The method of claim 1, wherein the blocking dielectric layer includes a high K dielectric.
Claim 6	
6	The method of claim 1, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.
Claim 7	
7	The method of claim 6, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.
Claim 8	
8	The method of claim 6, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.
Claim 9	
9	The method of claim 1, further comprising the step of etching the sacrificial layer to form a second opening.
Claim 10	
10	The method of claim 9, further comprising the step of depositing a gate electrode in the second opening.
Claim 11	
11	The method of claim 10, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.

Claim 12	
12	The method of claim 10, wherein the deposited gate electrode is a high work function gate electrode.
Claim 14	
14	The method of claim 1, wherein the vertical channel formed includes an annular region.
Claim 15	
15	The method of claim 14, wherein at least a portion of the vertical channel is formed of polysilicon.
Claim 16	
16	The method of claim 14, wherein the vertical channel formed includes a layer of semiconductor material surrounding a cylinder of filler material.
Claim 17	
17	The method of claim 14, wherein the vertical channel formed includes an outer layer of semiconductor material.
Claim 18	
18	The method of claim 17, wherein the outer layer of semiconductor material is formed of polysilicon.
Claim 19	
19	The method of claim 14, wherein the blocking dielectric layer is formed in a substantially annular shape.
Claim 20	
20	The method of claim 19, wherein the blocking dielectric layer includes a high K dielectric.

Claim 21	
21	The method of claim 19, wherein the multi-layer charge storing region is formed in a substantially annular shape.
Claim 22	
22	The method of claim 21, wherein the tunnel dielectric layers is formed in a substantially annular shape.
Claim 23	
[23pre]	A method comprising:
[23a1]	forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;
[23a2]	forming an opening extending through the stack of layers towards the substrate;
[23b]	forming on sidewalls of the opening an annular shaped blocking dielectric layer;
[23c]	forming on an inside sidewall of the blocking dielectric layer an annular shaped multi-layer charge storing region;
[23d]	forming on an inside sidewall of the multi-layer charge storing region an annular shaped tunnel dielectric layer; and
[23e]	forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layers.

Claim 25	
25	The method of claim 23, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.
Claim 26	
26	The method of claim 25, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.
Claim 27	
27	The method of claim 26, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.
Claim 28	
28	The method of claim 23, further comprising the step of etching the sacrificial layer to form a second opening.
Claim 29	
29	The method of claim 28, further comprising the step of depositing a gate electrode in the second opening.
Claim 30	
30	The method of claim 29, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.
Claim 31	
31	The method of claim 29, wherein the deposited gate electrode is a high work function gate electrode.

Claim 32	
32	The method of claim 29, wherein the blocking dielectric layer includes a high K dielectric.
Claim 33	
33	The method of claim 32, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.
Claim 34	
34	The method of claim 33 wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.
Claim 35	
[35pre]	A semiconductor memory device, comprising:
[35a]	a semiconductor substrate,
[35b]	a channel region oriented substantially perpendicular to the semiconductor substrate, the channel region formed in a substantially annular shape,
[35c]	a tunnel dielectric layer surrounding the channel region, the tunnel dielectric layer formed in a substantially annular shape,
[35d]	a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape,
[35e]	a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and
[35f]	a gate electrode surrounding the blocking dielectric layer.

Claim 36	
36	The semiconductor memory device of claim 35, wherein the blocking dielectric layer includes a high K dielectric.
Claim 37	
37	The semiconductor memory device of claim 35, wherein the gate electrode is a high work function gate electrode.
Claim 38	
38	The semiconductor memory device of claim 35, wherein the multi-layer charge storing region includes a first oxygen-lean nitride layer and a second oxygen-rich nitride layer.
Claim 39	
39	The semiconductor memory device of claim 38, wherein the first oxygen-lean nitride layer and the second oxygen-rich nitride layer both include silicon, nitrogen and oxygen components.
Claim 40	
40	The semiconductor memory device of claim 39, wherein the first oxygen-lean nitride layer is formed on an inside sidewall of the blocking dielectric layer and wherein the second oxygen-rich nitride layer is formed on the inside sidewall of the first oxygen-lean nitride layer.
Claim 41	
41	The semiconductor memory device of claim 40, wherein the blocking dielectric layer includes a high K dielectric.
Claim 42	
42	The semiconductor memory device of claim 35, including a stack of layers formed over the substrate.

Claim 43	
43	The semiconductor memory device of claim 42, wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer, wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer.
Claim 44	
44	The semiconductor memory device of claim 43, wherein the channel region is formed in an opening extending through the stack of layers.
Claim 45	
45	The semiconductor memory device of claim 43, wherein the second dielectric layer separates the gate layer from an overlying memory transistor.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on September 3, 2025, true and correct copies of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 11,456,365 and Exhibits 1001-1046 were served in its entirety on the Patent Owner at the following address of record as listed on Patent Center via Priority Mail Express® or Express Mail:

Kunzler Bean & Adamson
50 W. Broadway, Suite 1000
Salt Lake City, UT 84101

The undersigned certifies that true and correct copies of the Petition for *Inter Partes* Review of U.S. Patent No. 11,456,365 and Exhibits 1001-1046 were also sent via electronic mail to the attorneys of record for Plaintiff in the concurrent litigation matters:

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Date: September 3, 2025

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**CERTIFICATE OF COMPLIANCE WITH
TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS,
AND TYPE STYLE REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 12,300 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman.

Respectfully submitted,

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Date: September 3, 2025

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