

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Sandisk Technologies, Inc.,
Petitioner,

v.

Longitude Flash Memory Solutions Ltd.,
Patent Owner.

Case No. IPR2025-01281

U.S. Patent No. 11,456,365

**DECLARATION OF JACK C. LEE IN SUPPORT
OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 11,456,365**

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I, Jack C. Lee, declare as follows:

1. I have been retained as an independent expert on behalf of Sandisk Technologies, Inc. in connection with the above-captioned Petition for *Inter Partes* Review. In this declaration, I give my opinions as to whether certain claims of U.S. Patent No. 11,456,365 (the '365 patent) are unpatentable. I provide technical bases for these opinions as appropriate.

2. This declaration contains statements of my opinions formed to date and the bases and reasons for those opinions. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

I. BACKGROUND AND QUALIFICATIONS

A. Summary of Relevant Experience and Qualifications

3. My curriculum vitae ("CV") is attached hereto as Appendix 1 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

4. I am an expert in the field of semiconductor process technology and semiconductor design with more than 40 years' experience as a researcher, educator, and consultant. The opinions below draw on my education, training and experience.

5. I earned a B.S. with highest honors (1980) and M.S. (1981) in Electrical Engineering, from University of California, Los Angeles, and a Ph.D. in Electrical Engineering (1988) from University of California, Berkeley.

6. From 1979 to 1984, I served as a Member of Technical Staff at the TRW Microelectronics Center, where I worked on high-speed bipolar device/circuit design, fabrication, and testing and was promoted to Engineering Group Leader in 1983.

7. While at UC Berkeley I received several academic honors, including the 1988 IEEE International Reliability Physics Symposium Best Paper Award and a competitive Lectureship with dedicated teaching assistantship.

8. After completing my doctorate, I joined the faculty at The University of Texas at Austin in August 1988. I have taught undergraduate and graduate courses in semiconductor device fabrication and design, supervised more than forty Ph.D. students, and since 2000 have held the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering. I became Professor Emeritus level in September 2023.

9. My current research and teaching interests include advanced MOSFETs such as FinFETs, memory devices including non-volatile NAND structures, high-K gate dielectrics and high work function gate electrodes, ultra-thin dielectrics such as silicon nitride, tunneling and blocking oxides, reliability

physics, and modeling, packaging, photovoltaic technologies, and alternative channel materials.

10. I have been invited to present tutorials, short courses and plenary talks various topics including high-K gate stacks in leading conferences such as the Symposium on VLSI Technology and the IEEE International Electron Devices Meeting (IEDM). My research group at UT Austin was among the first to develop hafnium-based high-K for nanoscale MOSFETs, and I have published extensively on HfO₂, HfSiON, hafnium silicate, interfacial engineering, and dielectric reliability.

11. My research has been supported by the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, among others.

12. I have authored more than 600 journal and conference papers, co-authored eight book or book chapters, and am a named inventor on nine U.S. patents. My work has received multiple best-paper and inventor awards.

13. In 2002, I was elected an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices,” and I served as an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

14. I regularly consult for semiconductor companies and consortia, teach industrial short courses, and organize international conferences, including the International Symposium on VLSI Technologies and IEDM.

B. Compensation

15. For my efforts in connection with the preparation of this declaration, I have been compensated at my standard rate for this type of consulting activity. My compensation is in no way contingent on the results of these or any other proceeding relating to the above-captioned patent.

C. Materials and Other Information Considered

16. I have considered information from various sources in forming my opinions. I have reviewed and considered each of the exhibits listed in the attached Appendix 2 (Materials Considered) in forming my opinions, along with any other documents or information otherwise identified herein.

II. UNDERSTANDING OF THE LAW

17. I am not an attorney. In forming my opinions herein, I applied the relevant legal principles provided to me by counsel, summarized in Appendix 4.

III. BACKGROUND

A. Overview of the '365 Patent

18. I understand that the '365 patent issued on September 27, 2022 from an application filed on January 25, 2021. *See* Ex. 1001 ('365 patent), p. 1. It is directed to alleged improvements in the design and fabrication of non-volatile

semiconductor memory devices. *See* Ex. 1001 ('365 patent), 1:33-36. While the '365 patent acknowledges that such devices were already “widely used” at the time of its filing (Ex. 1001 ('365 patent), 1:40-44), it asserts that existing designs had “poor or decreasing data retention over time, limiting the useful transistor lifetime” (Ex. 1001 ('365 patent), 2:5-14) and that processes for fabricating conventional memory transistors were “incompatible with those used for fabricating logic transistors” (*Id.*, 2:24-31).

19. The '365 patent states that designing a memory transistor to include an “oxide-nitride-nitride-oxide (ONNO) stack” (with a “multi-layer charge-trapping region”) and a “high work function gate electrode” provides a solution to the problems with conventional memory transistors:

Generally, the device includes a memory transistor comprising a polysilicon channel region electrically connecting a source region and a drain region formed in a substrate, an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, and a high work function gate electrode formed over a surface of the ONNO stack. In one embodiment, the ONNO stack includes a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer. In another embodiment, the multi-layer charge trapping region further includes an oxide anti-tunneling layer

separating the first nitride layer from the second nitride layer.

Ex. 1001 ('365 patent), 2:45-57.

20. Figure 3 of the '365 patent depicts an embodiment of the alleged invention. *See* Ex. 1001 ('365 patent), 8:14-18. It shows a semiconductor device with a memory transistor (304) and a logic transistor (302). *Id.*, 3:13-17. The memory transistor includes: a channel region (312) extending horizontally between source/drain diffusion regions (314); an ONNO stack (310) disposed above the channel region with (i) an oxide tunneling layer (316) (one of the “O” layers of the ONNO stack); (ii) a “multi-layer charge storage layer” (318A, 318B) (the two “N” layers of the ONNO stack); and (iii) a blocking oxide layer (320) (the other “O” layer of the ONNO stack); and a high work function gate electrode (308). *Id.*, 8:18-35. The logic transistor (302) has an oxide layer (326) and a high work function gate electrode (324). *Id.*, 8:36-44. I have annotated figure 3 here:

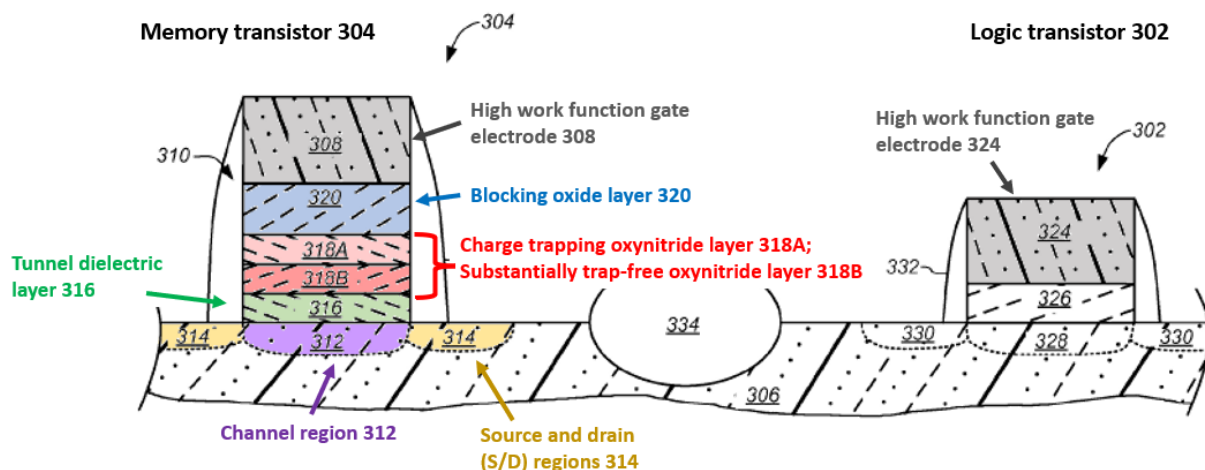


FIG. 3

Ex. 1001 ('365 patent), Fig. 3.

21. Figure 4A provides a larger cross-sectional view of a memory transistor according to the alleged invention, showing an ONNO structure with multi-layer charge-trapping region 422 made up of nitride layers 422a and 422b.

Ex. 1001 ('365 patent), 3:18-19. Again, I have annotated figure 4A here:

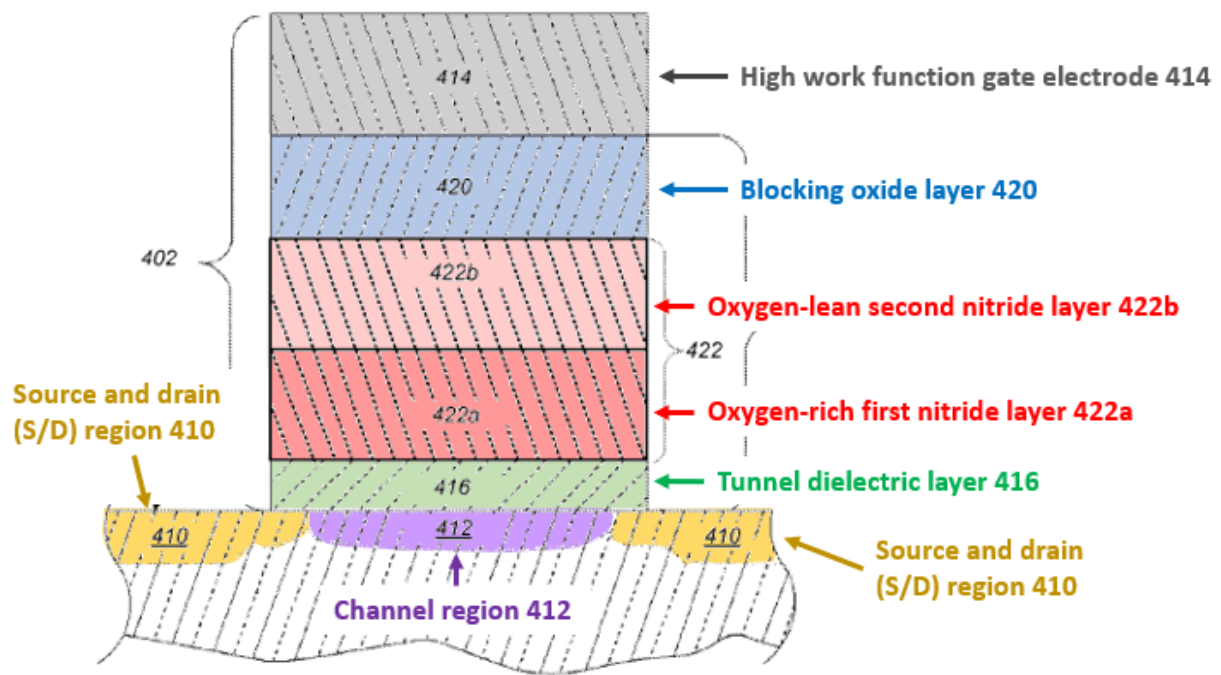


FIG. 4A

Ex. 1001 ('365 patent), Fig. 4A.

22. The '365 patent provides additional details concerning the above-annotated features of the alleged invention:

- **Diffusion (Source/Drain) Regions 314/410 (Gold).** The memory transistor includes “one or more diffusion regions 410, such as source

and drain regions.” Ex. 1001 (’365 patent), 8:59-62; *see also id.*, 8:23-24 (“heavily doped source and drain (S/D) regions 314”).

- **Channel Region 312/412 (Purple).** Electric current flows through a “channel region 312” between the source and drain. Ex. 1001 (’365 patent), 8:22-24. The channel region may be formed of polysilicon. *Id.*, 9:5-10.
- **ONNO Stack (Green/Red/Blue).** The memory transistor includes an oxide-nitride-nitride-oxide (ONNO) stack comprising (i) an oxide “tunnel dielectric layer” (316/416) (green); (ii) a nitride “multi-layer charge storage layer” (318/422) (red); and (iii) a “blocking oxide layer” (320/420) (blue). Ex. 1001 (’365 patent), 8:24-29; 8:58-9:4.
- **Oxygen Concentrations in the “Multilayer Charge Trapping Layer” (Red).** The “multilayer charge trapping layer” (red) includes an “oxygen-rich first nitride layer” (318B/422a) and a “silicon rich, nitrogen-rich, oxygen-lean second nitride layer” (318A/422b). Ex. 1001 (’365 patent), 8:22-35; 8:57-9:4; 10:4-15. “Either or both” of the “charge trapping” nitride layers “can include silicon nitride or silicon oxynitride.” *Id.*, 14:11-14.
- **High Work Function Gate Electrode (Gray).** The memory transistor includes a “high work function gate electrode 308” (Ex. 1001 (’365 patent), 8:18-22), meaning “that the minimum energy needed to remove an electron from the gate electrode is increased” (*Id.*, 4:7-9). The high work function gate electrode, for example, may be formed of polysilicon that is “doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV.” *Id.*, 9:21-25.

23. ONNO configurations like those of Figures 3 and 4A were well-known by July 2012 (*see* Part III.C.4), as was the use of high work function gate electrodes (*see* Part III.C.7).

24. Figure 4B depicts an alternative embodiment of the alleged invention where the multi-layer charge trapping layer includes an intermediate oxide anti-tunneling layer (422c) (orange) separating the two nitride layers of the charge trapping region (oxygen-rich nitride layer 422a, oxygen-lean nitride layer 422b) (red). Ex. 1001 ('365 patent), 10:8-15. This results in an ONONO variation of the ONNO stack. *Id.* Again, I have annotated figure 4B here:

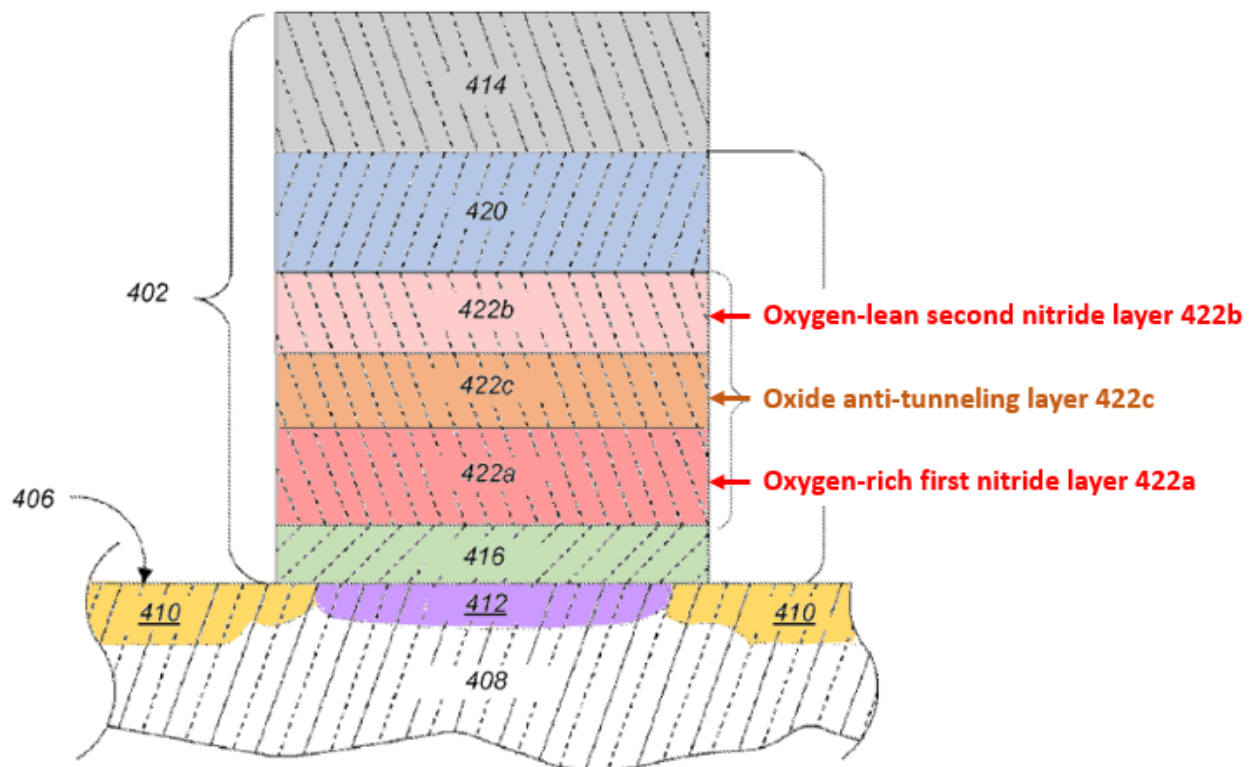


FIG. 4B

25. ONONO configurations like that of Figure 4B were well-known by July 2012. *See* Part III.C.5.

26. The '365 patent includes a lengthy section entitled "Implementations and Alternatives" that discloses different ways to arrange the features of the alleged invention discussed above (e.g., diffusion regions, channel region, ONNO or ONONO stack, high work function gate electrode) in designing a memory transistor. Ex. 1001 ('365 patent), 8:51-20:7.

27. Figures 4A and 4B (annotated above) depict a memory transistor similar to figure 3, where a channel region extends horizontally between diffusion regions and the ONNO or ONONO stack is disposed above the channel region.

28. Figures 6A, 6B, 7A, and 7B are also directed to horizontal channels between diffusion regions, but with an ONONO stack surrounding the channel region. Ex. 1001 ('365 patent), 12:64-17:16. For example, figures 6A and 6B are annotated here using the same colors to represent the diffusion regions (gold), channel region (purple), ONONO stack (green/red/orange/red/blue), and high work function gate electrode (gray):

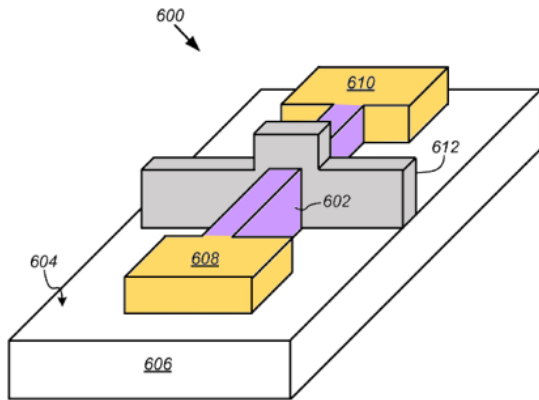


FIG. 6A

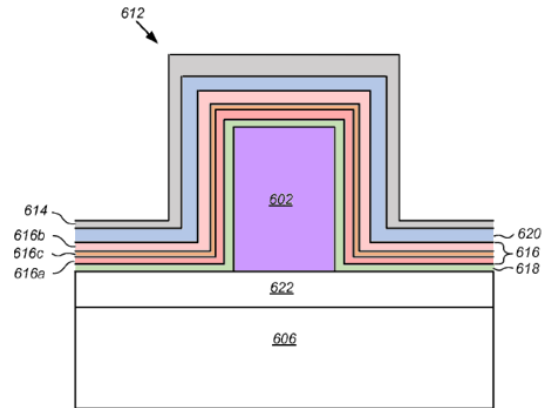
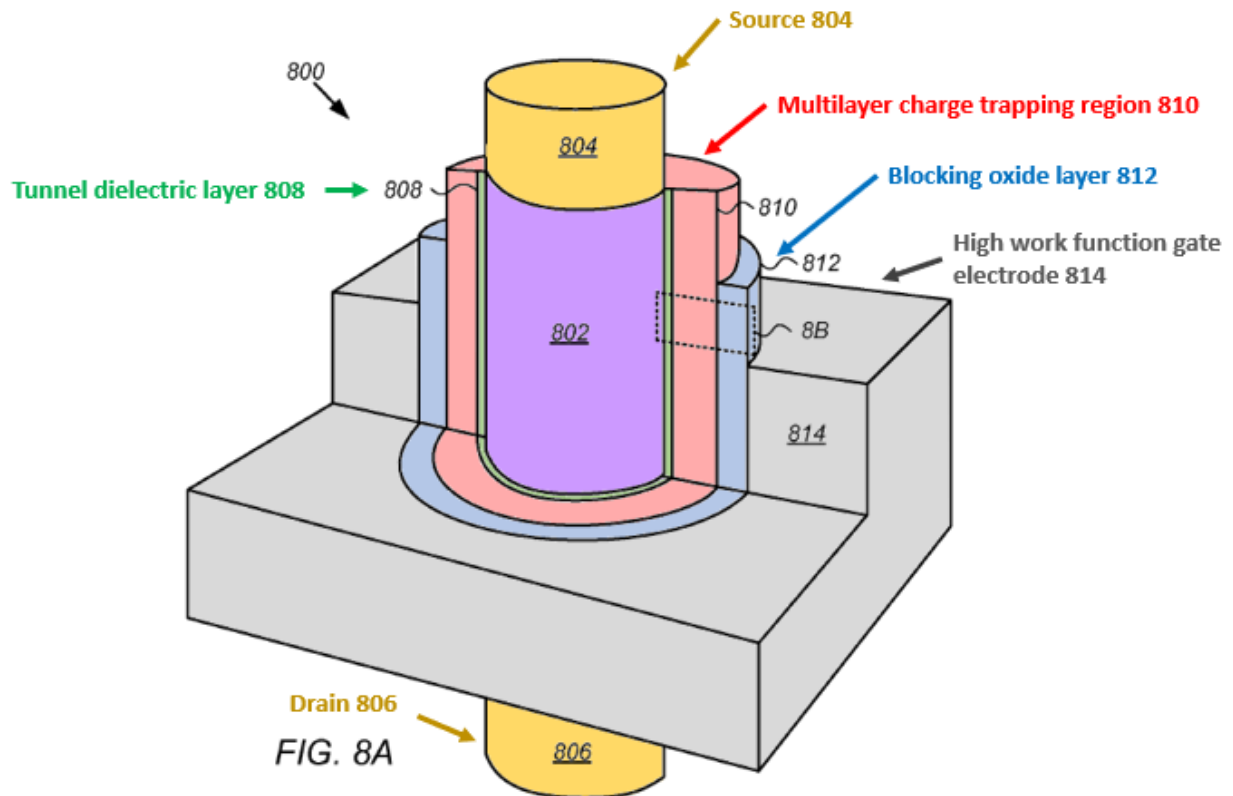


FIG. 6B

Ex. 1001 ('365 patent), Figs. 6A, 6B.

29. A POSITA would have understood that the above figures illustrate a “fin” SONOS configuration that was well-known by July 2012. *See* Part III.C.6.

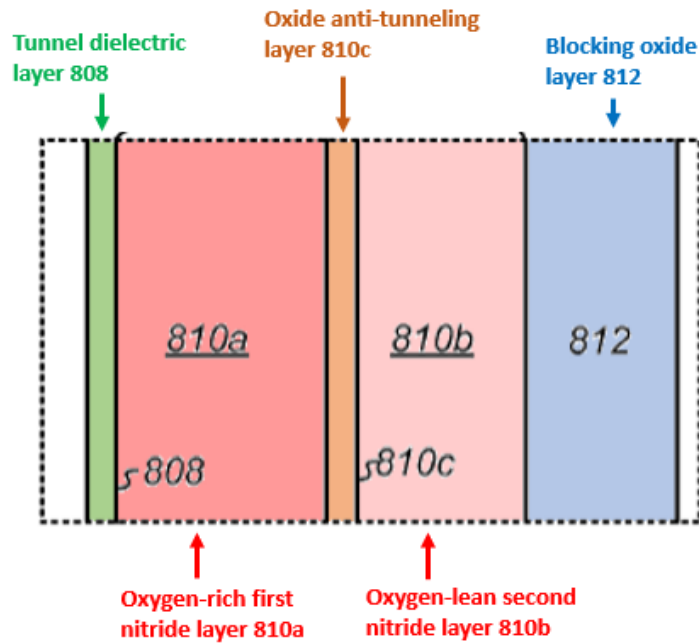
30. Figures 8-10 are directed to vertically-oriented memory transistors. Ex. 1001 ('365 patent), 17:17-20:7. For example, figure 8A shows a transistor where the channel region (802) extends vertically between diffusion regions (806) and (804) and the ONONO stack (808/810/812) is disposed about the channel region (802). Ex. 1001 ('365 patent), 17:17-18:14. I have annotated figure 8 here with the same colors as above:



See Ex. 1001 ('365 patent), Fig. 8A.

31. A POSITA would have understood that figure 8A depicts a three-dimensional ("3D") SONOS configuration, which was well-known by July 2012. *See* Part III.C.6.

32. Figure 8B depicts a cross section of the ONONO stack from figure 8A (see hashed line in figure 8A referring to "8B"):



Ex. 1001 ('365 patent), Fig. 8B.

33. The '365 patent describes the ONONO stack of figure 8 as follows:

In some embodiments, such as that shown in FIG. 8B, the multi-layer charge trapping region 810 includes at least an inner or oxygen-rich first nitride layer 810a closest to the tunnel dielectric layer 808, and an outer or oxygen-lean second nitride layer 810b. Optionally, as in the embodiment shown, the oxygen-rich first nitride layer 810a and the oxygen-lean second nitride layer 810b are separated by an intermediate oxide or anti-tunneling layer 810c comprising oxide.

Ex. 1001 ('365 patent), 17:55-63.

34. Lastly, figures 9 and 10 depict vertical channel manufacturing processes, including a “gate first” method in figure 9 and “gate last” method in

figure 10. Ex. 1001 ('365 patent), 3:36-38. In either case, figures 9 and 10 show vertical channels as they are made according to the alleged invention in relationship to the surrounding structure. Ex. 1001 ('365 patent), 18:15-19:19.

35. In short, the '365 patent's contribution is limited to known gate-first and gate-last fabrication methods and conventional SONOS/SONONOS structures, i.e., ONNO and ONONO stacks, oxygen-rich and oxygen-lean nitride layering, optional anti-tunneling oxide, and high-work-function gates, applied across planar, fin-type, and vertical transistor configurations. Each of these elements and process flows was already well-known by July 2012, as discussed below. *See* Part III.C.9.

B. Prosecution History of the '365 Patent

36. I understand that Igor Polishchuk, Sagy Charel Levy, and Krishnaswamy Ramkumar (collectively, "the Applicants") filed the application for the '365 patent (U.S. Application No. 17/157,350) on January 25, 2021. Ex. 1002 (Pros. Hist.), 000065-78. I understand that the original application included only one claim. I understand that Applicants submitted information disclosure statements during prosecution listing large numbers of prior art references (more than 300 references in total). Ex. 1002 (Pros. Hist.), 001802-11, 001898-1947. Then, on November 1, 2021, I understand that Applicants filed a preliminary amendment replacing original claim 1 with new claims 2-46. Ex. 1002 (Pros. Hist.), 001856-64.

37. I understand that the Examiner allowed application claims 2-46 without rejection. Ex. 1002 (Pros. Hist.), 001871-79. The Examiner did not explicitly compare the limitations of claims 2-46 to any specific prior art reference. In the statement of reasons for allowance, the Examiner identified claim limitations that he believed were missing from the prior art, as discussed below.

38. Regarding application claim 2 (issued claim 1), the Examiner stated the prior art does not disclose “forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate; forming on sidewalls of the opening a blocking dielectric layer; forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region; forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.” Ex. 1002 (Pros. Hist.), 001877.

39. Regarding application claim 24 (issued claim 23), the Examiner stated the prior art fails to disclose “forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layer.” Ex. 1002 (Pros. Hist.), 001877.

40. Regarding application claim 36 (issued claim 35), the Examiner stated the prior art fails to disclose “a semiconductor memory device, comprising a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape, a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and a gate electrode surrounding the blocking dielectric layer.” Ex. 1002 (Pros. Hist.), 001878.

C. Technical Background Relevant to the '365 Patent

41. As I set forth in Part V, below, I understand that July 1, 2012 is the earliest possible priority date for the claims of the '365 patent. In this section, I provide technical background relevant to understanding the general knowledge of a person of ordinary skill in the art (a “POSITA”) as of that date.¹ I also cross-reference and rely on this technical background in explaining my opinions that certain claims of the '365 patent would have been obvious to a POSITA as of July 2012.

1. Non-Volatile Memory

42. Non-volatile memory (or “NVM”) is a type of computer memory that can retain stored information even after power is removed. In contrast, volatile

¹ I provide my understanding of the level of ordinary skill in the art in Part VI, below.

memory needs constant power to retain data. Well-known examples of non-volatile memory include hard disk drives (HDDs) and read-only memory (ROM) chips.

43. Regardless of the specific technology, every NVM cell incorporates a physical “state holder” that is energetically stable at room temperature, i.e., it takes substantial energy (more than ambient thermal noise) to disturb it. In magnetic disks that state is the orientation of magnetic domains; in phase-change memories, it is whether a chalcogenide bit-line segment has crystallized; in flash and other charge-trap devices, it is a packet of electrons parked behind an insulating barrier. Writing data to a NVM applies a stimulus (e.g., magnetic field, heat pulse, high electric field, etc.) strong enough to flip the state. Reading data stored in the NVM senses the state through resistance, capacitance, or another indicator. When external power is removed, the barrier remains, so the state—and thus the data—persists for years.

2. Floating Gate Flash Memory

44. “Flash memory” is a common type of semiconductor NVM. Flash memory was invented in the 1980s and is based on metal–oxide–semiconductor field-effect transistor (MOSFET) technology. MOSFETs are typically composed of a semiconductor material with a source, drain, and gate, as shown in the following basic example:

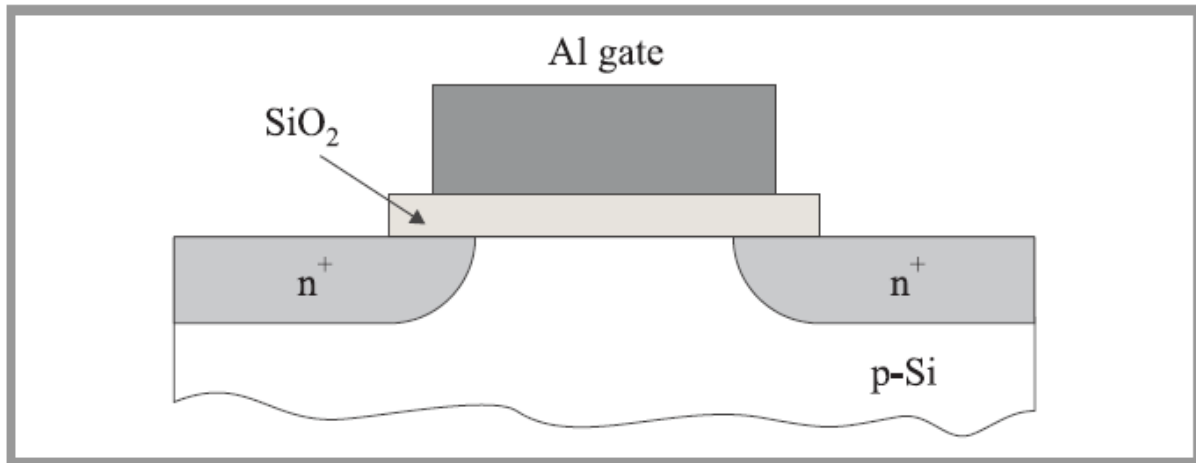


Fig. 4. A cross section of a metal-oxide-semiconductor transistor.

Ex. 1007 (Lukasiak), p. 6, Fig. 4.

45. Early flash memory devices dating back to the 1980s were based on a “floating gate” MOSFET design, sometimes referred to as “FGMOS.” The design was similar to the regular MOSFET above except FGMOS devices have an additional electrically insulated gate that “floats” between two oxide layers, as shown here:

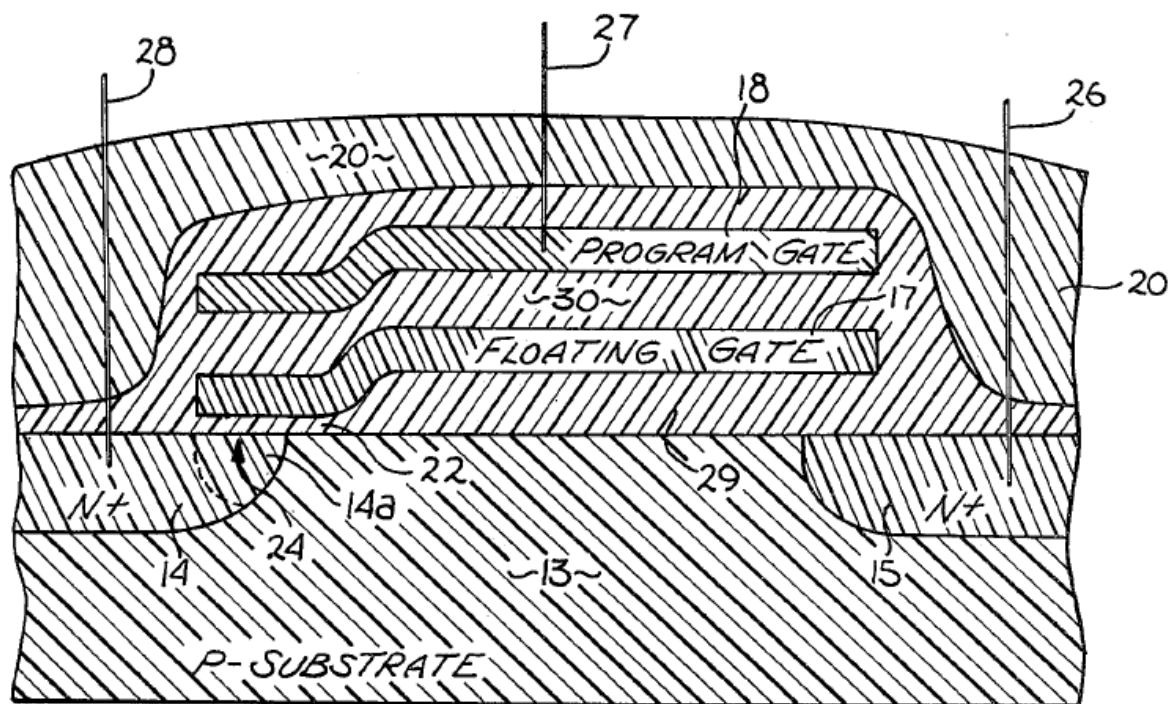


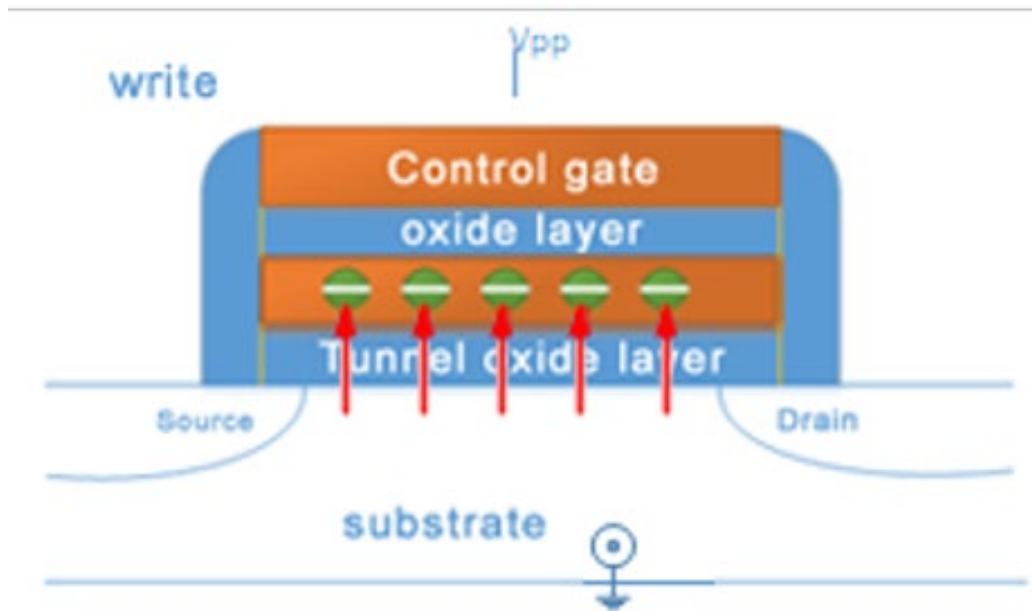
Fig. 1

Ex. 1008 (Frohman-Bentchkowsky), Fig. 1; *see also id.*, 4:1-31.

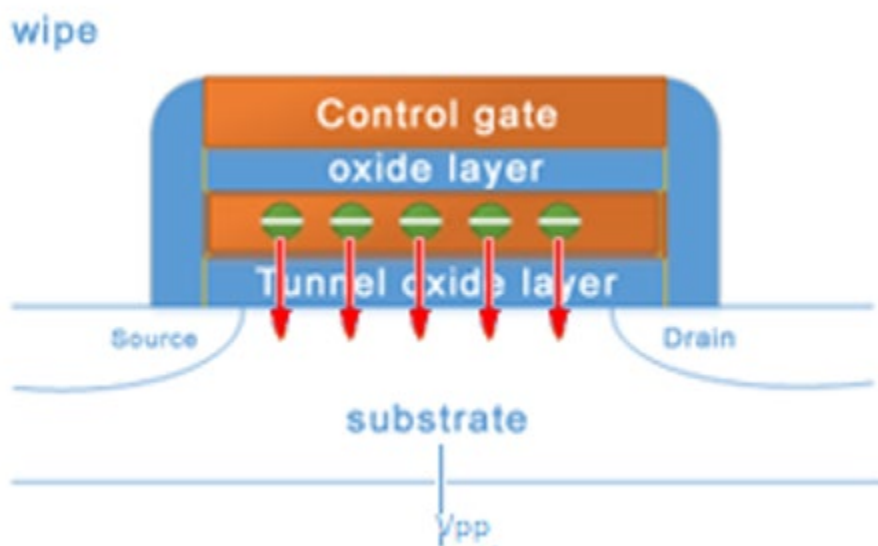
46. Because the floating gate is electrically isolated, any electron placed in the gate will be trapped there—even after voltage is removed. *See, e.g.*, Ex. 1008 (Frohman-Bentchkowsky), 1:18-23, 3:55-57, 5:5-7. This property is what allows the floating gate transistor to function as a non-volatile memory. In the simplest example, the presence of sufficient electrons in the floating gate will cause the memory to be read as a “1,” while the absence of electrons in the floating gate will cause the memory to be read as a “0.” *Id.*, 1:20-23.

47. Electrons can be placed in the floating gate by various methods, including by “tunneling,” where an electric field is applied between the substrate

and control gate that causes electrons from the substrate to “tunnel” through the tunnel oxide layer and move into the floating gate. This is called a program/write operation and is depicted here:



48. The electrons can be removed from the floating gate by applying an opposite electric field, which will cause the electrons trapped in the control gate to “tunnel” back to the substrate through the tunnel oxide layer. This is called a clear/erase/wipe operation and is shown here:

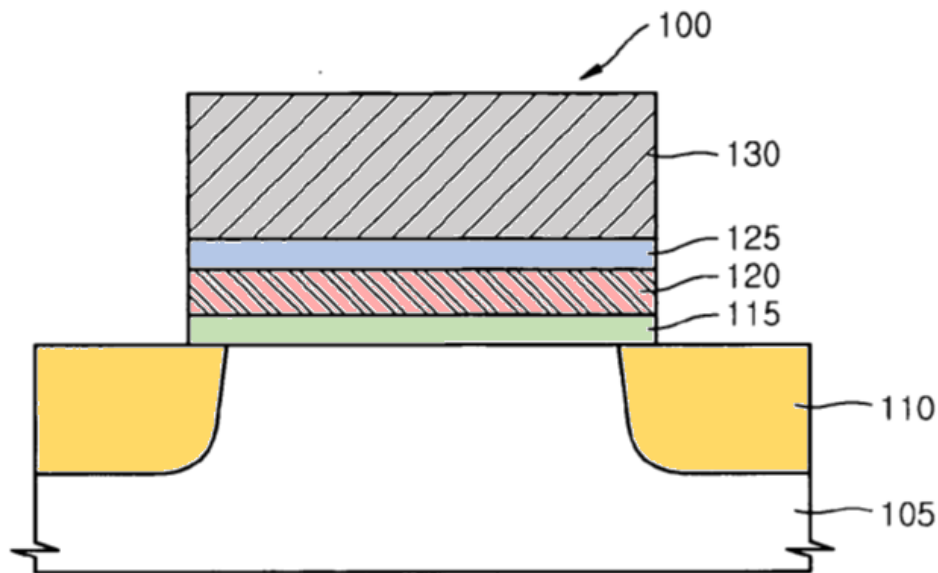


3. “SONOS” Flash Memory

49. By the early 2000s, flash memory devices were also fabricated using charge-trap “SONOS” (silicon–oxide–nitride–oxide–silicon) transistors. The ’365 patent is directed to SONOS-type devices.

50. SONOS-type flash memory is similar to floating gate memory except that the floating gate is replaced with a non-conductive silicon nitride layer containing a large number of charge trapping sites. An example of a SONOS memory device is provided in Kim ’399 (Ex. 1009), which was filed on February 15, 2006:

FIG. 1 (CONVENTIONAL ART)

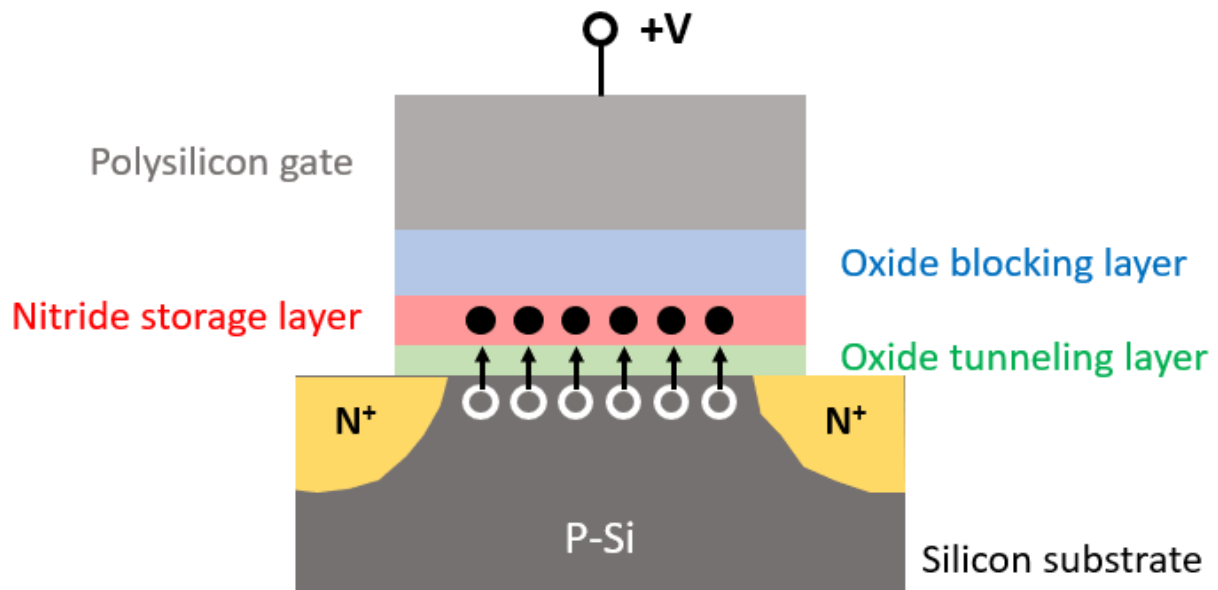


Ex. 1009 (Kim '399), Fig. 1, [0006]-[0008].

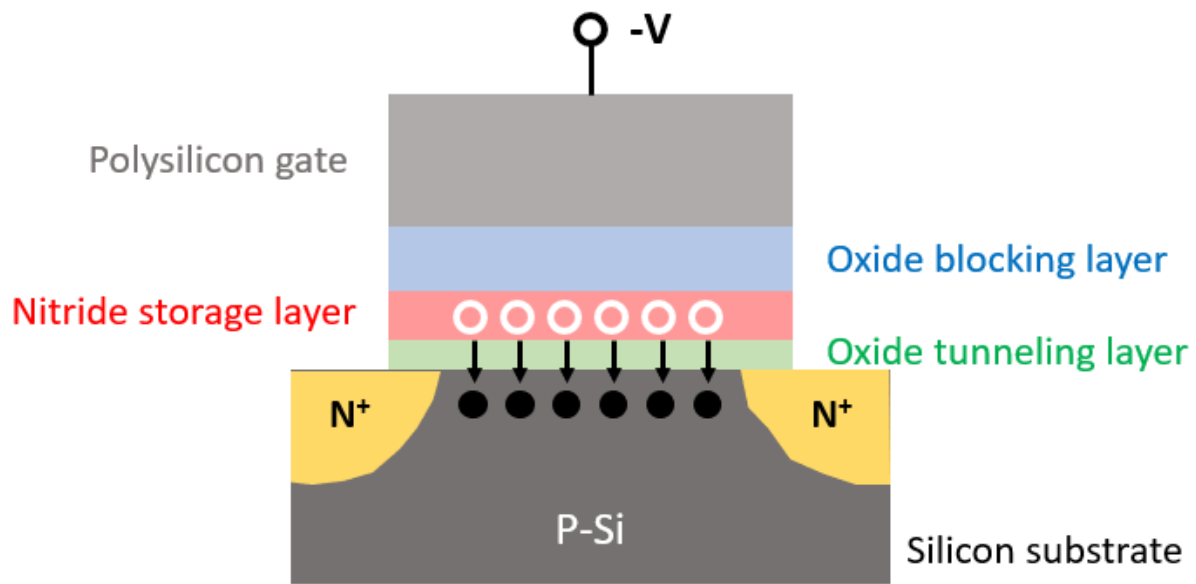
51. As reflected above, the conventional SONOS memory device shown in figure 1 of Kim '399 includes: (i) silicon semiconductor substrate 105 with source/drain regions 110; (ii) oxide tunnel insulating film 115 (green); (iii) nitride charge trapping film 120 (red); (iv) silicon oxide blocking insulating film 125 (blue); and (v) polysilicon control gate 130 (gray).

52. Like floating gate memory, SONOS charge trap memory transistors work by moving electrons, representing data bits (i.e., 1s and 0s), into and out of the nitride charge trapping layer by “tunneling.” During a writing/programming step, a positive voltage is applied to the gate, which causes electrons from the substrate to tunnel through the tunnel oxide and into the nitride storage layer. When the voltage is removed, the electrons remain in the nitride storage layer

(even when power to the device is turned off), prevented from moving by the structure of the nitride storage layer and the tunneling and blocking oxides on either side. This is shown in the following figure:



53. To perform an erase/clear step, a negative voltage is applied to the gate, which causes electrons to tunnel from the nitride storage layer back through the tunnel oxide into the silicon substrate. This is shown in the following figure:

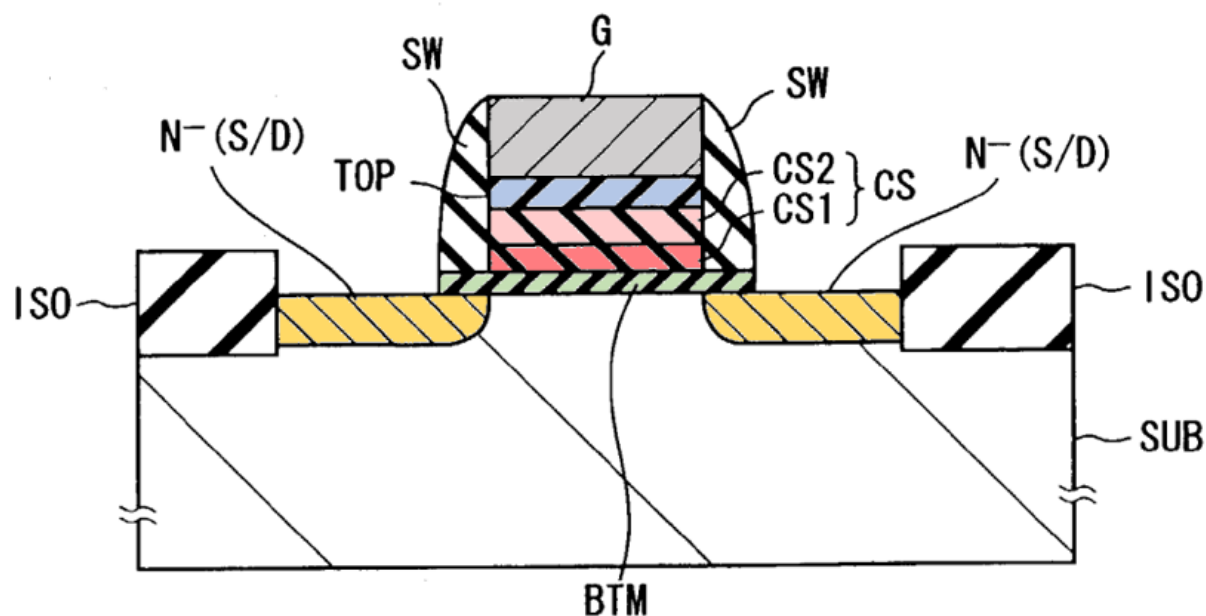


4. SONNOS configurations

54. With the conventional SONOS structure well-established by the mid-2000s, the industry turned to engineering alternative configurations of the SONOS “stack” to optimize performance. For example, a POSITA would have been very familiar prior to July 2012 with a variation that added a second nitride layer to the conventional SONOS stack to create a SONNOS device.

55. It was well understood prior to July 2012 that making the two N layers of different compositions and trap densities, such as by making the lower layer of oxynitride (SiO_xN_y) and the top layer of nitride, could improve charge storage by preventing electron leakage from the top nitride layer. Nomoto (Ex. 1010), a 2003 U.S. patent application publication, reflects one such device:

FIG.3H



Ex. 1010 (Nomoto), Fig. 3H.

56. As reflected above, Nomoto's FIG. 3H depicts a SONNOS structure:

- (i) silicon substrate ("SUB") with source and drain ("S/D");
- (ii) a silicon dioxide (SiO_2) bottom dielectric film ("BTM");
- (iii) a first nitride film ("CS1");
- (iv) second nitride film ("CS2");
- (v) silicon dioxide (SiO_2) top dielectric film ("TOP");
- and (vi) doped polycrystalline silicon gate electrode ("G").

Ex. 1010 (Nomoto), [0032]-[0038]. Nomoto teaches that the two nitride layers have different compositions (*id.*, [0035], [0044]-[0045]) so that the charge trap density of CS2 is higher than CS1 (*id.*, [0073]-[0088]). Nomoto teaches that the top nitride film (CS2) acts as the primary charge storage layer, while the lower nitride film (CS1) acts as a barrier

that reduces leakage of charges from CS2. Ex. 1010 (Nomoto), [0035]; *see also id.*, [0088] (explaining benefits of two nitride layers).

57. To achieve nitride layers with different trap densities (as in Nomoto), it was well-understood prior to July 2012 to employ (i) an oxygen-lean nitride top layer primarily responsible for storing charges; and (ii) an oxygen-rich nitride bottom layer to prevent electron leakage from the oxygen-lean top layer. For example, Levy (Ex. 1011), reflects this configuration:

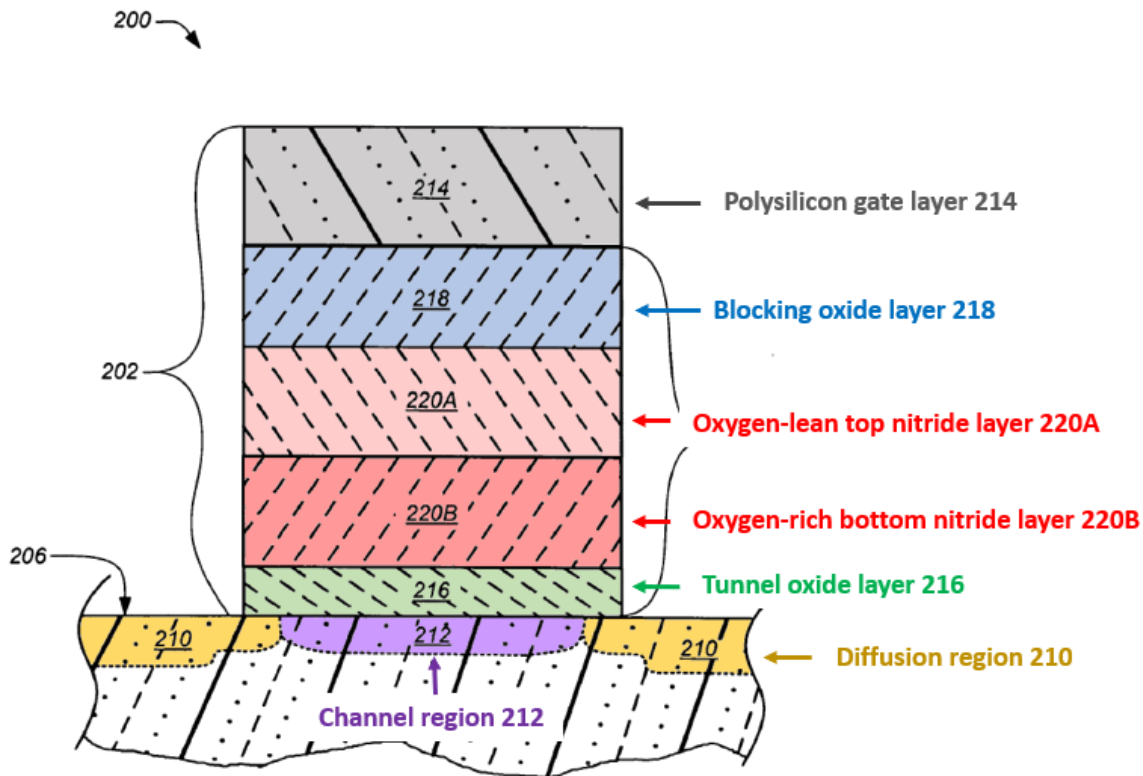
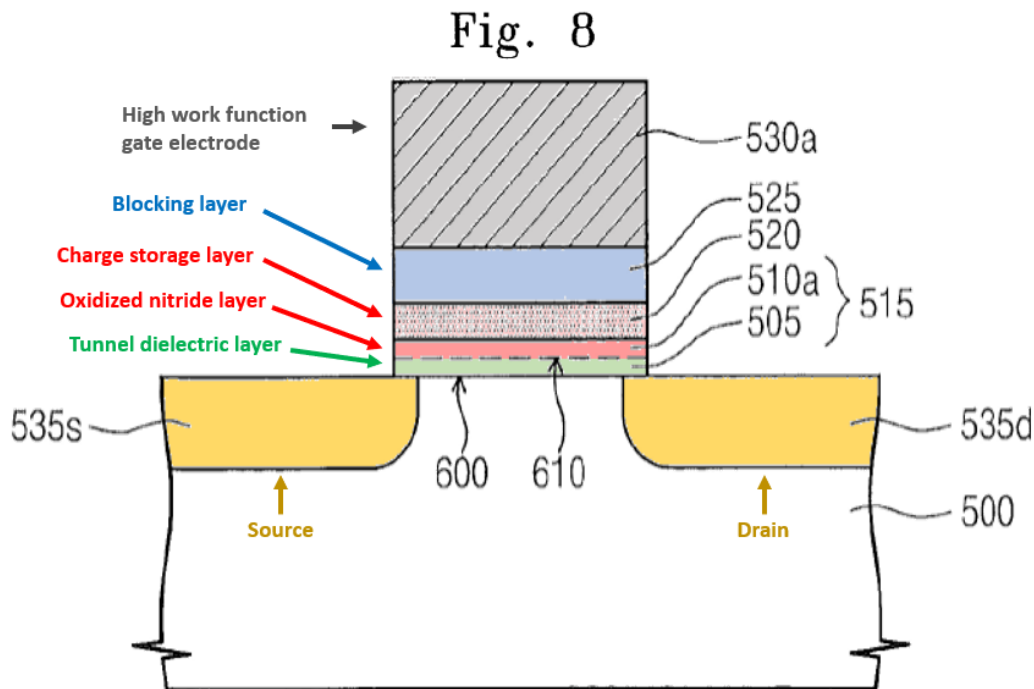


FIG. 2

Ex. 1011 (Levy), Fig. 2; *see also id.*, [0021], [0025]-[0027].

58. Consistent with Nomoto, Levy teaches that “a silicon-rich, oxygen-rich, bottom oxynitride layer” decreases the charge loss rate after programming and erase.” Ex. 1011 (Levy), [0025].²

59. Heo (Ex. 1012) teaches a similar configuration, where an “oxidized nitride layer” is arranged adjacent the nitride charge storage layer to prevent charge leakage, as shown in annotated Figure 8:



² I understand that Levy is a 2009 publication of a 2007 U.S. Patent Application that shares two inventors with the '365 patent—Sagy Levy and Krishnaswamy Ramkumar. I understand that Levy is prior art to the '365 patent because it was published more than one year before the earliest possible priority date of the claims of the '365 patent (July 1, 2012). *See* Part V, below. As reflected above, figure 2 of Levy mirrors figure 4A of the '365 patent.

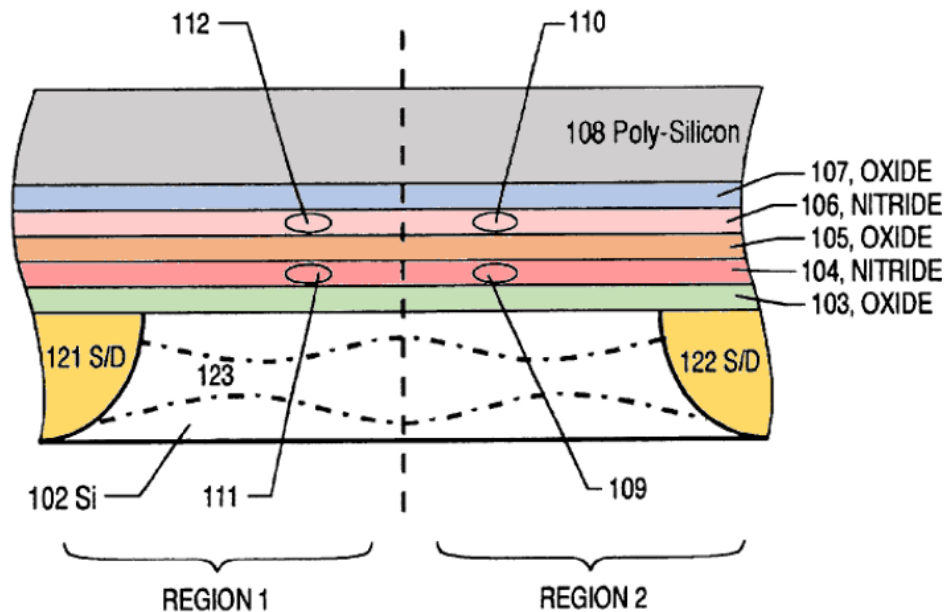
Ex. 1012 (Heo), [0030], [0068].

60. A POSITA would have been aware of numerous other prior art references reflecting SONNOS structures similar to Nomoto, Levy, and Heo—i.e., two nitride layers having differing oxygen concentrations to promote charge retention. *See, e.g.*, Ex. 1009 (Kim '399), Fig. 3 (showing SONOS-type device with multiple nitride layers), [0034] (teaching bottom nitride layer may be silicon oxynitride and top layer may be silicon nitride), [0046]-[0047] (teaching that use of multiple nitride layers suppresses charge loss); Ex. 1013 (Ganguly), Fig. 3, [0048]-[0050] (teaching first nitride layer is oxygen-rich and engineered to have a lower charge trap density in order to promote charge retention in the second nitride layer); and Ex. 1014 (Wang '586), [0031]-[0032] (teaching multi-layer charge storage structures including a silicon oxynitride bottom and nitrided silicon oxynitride top (FIG. 5) or a silicon oxynitride bottom and nitride top (FIG. 6)).

5. SONONOS configurations

61. Another well-known variation of SONOS-type memory devices prior to July 2012 was inserting an intermediate oxide layer between two nitride layers to form a SONONOS structure. For example, Yang '533 (Ex. 1015) is a U.S. Patent filed in 2002 and issued in 2005 that teaches a SONONOS structure for a memory cell/transistor 100 having: (i) a substrate with source 121, drain 122, and channel 123; (ii) oxide layer 103; (iii) charge trapping nitride layer 104; (iv) oxide

layer 105; (v) charge trapping nitride layer 106; (vi) oxide layer 107; and (vii) poly gate 108. 1:60-2:3, 2:64-3:8. Each nitride layer has one or more storage regions. Ex. 1015 (Yang '533), 3:9-29.



Ex. 1015 (Yang '533), Fig. 1.

62. Another example can be found in Ex. 1016 (Lue '189), filed and published in 2006, which teaches SONOS cells having: (i) substrates 101/201 with source 102/202 and drain 104/204 and channel 106/206; (ii) lower/first oxide layer 122/222; (iii) first/small hole-tunneling-barrier height nitride layer 124/224; (iv) second/upper oxide layer 126/226; (v) second/charge-trapping (or charge storage) nitride layer 130/230; (vi) third/insulating oxide layer 140/240; and (vii) polysilicon gate 150/2550. Ex. 1016 (Lue '189), [0057]-[0060].

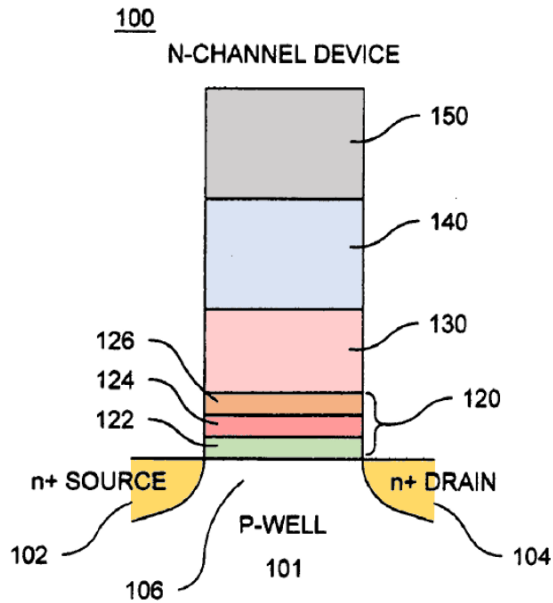


Fig. 1a

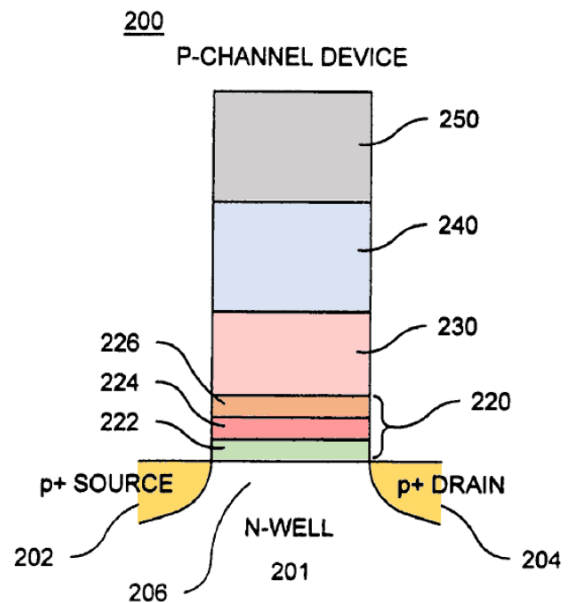
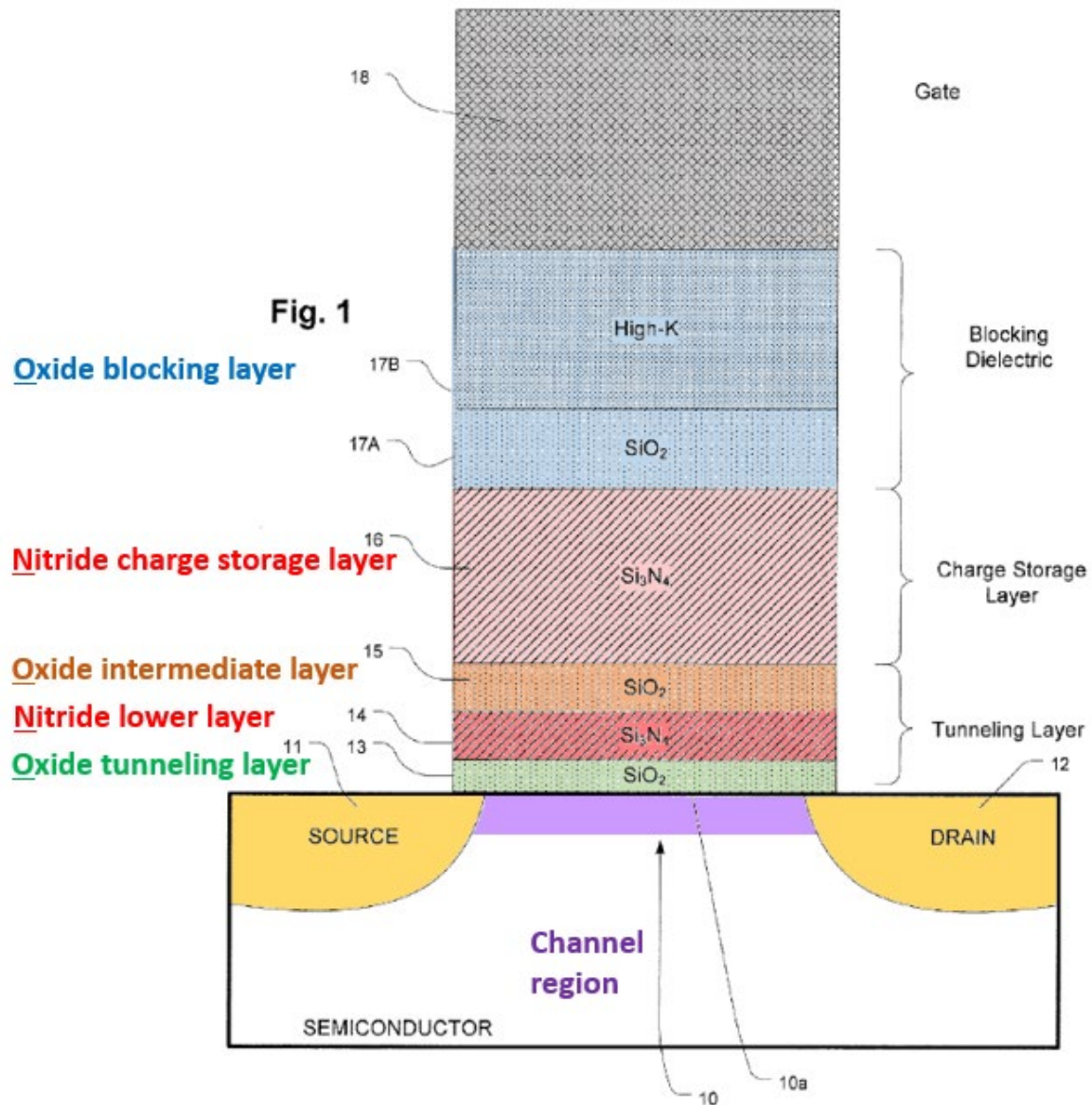


Fig. 1b

Ex. 1016 (Lue '189), Figs. 1a, 1b.

63. Lue '189 teaches that the O1/N1/O2 tunneling dielectric structure 120 allows hole tunneling from the substrate to the charge-storage layer during an erase/reset operation of the memory device and preferably does not trap charges during memory operations. Ex. 1016 (Lue '189), [0059]. This allows fast erase speeds while improving charge retention. Ex. 1016 (Lue '189), [0055], [0061].

64. Lai '676 (Ex. 1017) teaches a similar configuration that is intended to provide improved data retention. Ex. 1017 (Lai '676), [0003], [0015]. In particular, Lai '676 teaches using a SONOS configuration for trapping charges in its figure 1:



Ex. 1017 (Lai '676), Fig. 1.

65. As reflected above, Lai '676's SONOS configuration includes a silicon dioxide tunneling layer 13 (green), silicon oxynitride band offset layer 14 (red), silicon dioxide isolation layer 15 (orange), a silicon nitride charge trapping layer 16 (pink), silicon dioxide blocking dielectric layer 17A/B (blue), and doped

polysilicon or metal high work function gate 18 (gray). Ex. 1017 (Lai '676), [0067]-[0069], [0074], [0075]-[0077].

66. In addition to Yang '533, Lue '189, and Lai '676, many other references reflect a POSITA's general knowledge prior to July 2012 of SONONOS memory transistors—i.e., SONOS-type memory transistors with an oxide layer separating two nitride layers—and the benefits of using such structures. *See, e.g.*, Ex. 1018 (Lai Article), p. 1 (col. 1-2), Table 1, Fig. 1 (teaching SONONOS configuration to provide good data retention); Ex. 1019 (Noguchi), Fig. 1, [0068]-[0069], [0072], [0241]; Ex. 1020 (Arreghini), p. 1213 (Fig. 3), p. 1216 (SONONOS devices “show a faster programming and erasing compared with SONOS cells”).

6. Vertically-oriented SONOS-type memory transistors

67. As reflected in Figure 1 of Kim '399 (Ex. 1009), early SONOS-type memory transistors typically had ONO stacks formed above channels extending horizontally between sources and drains.

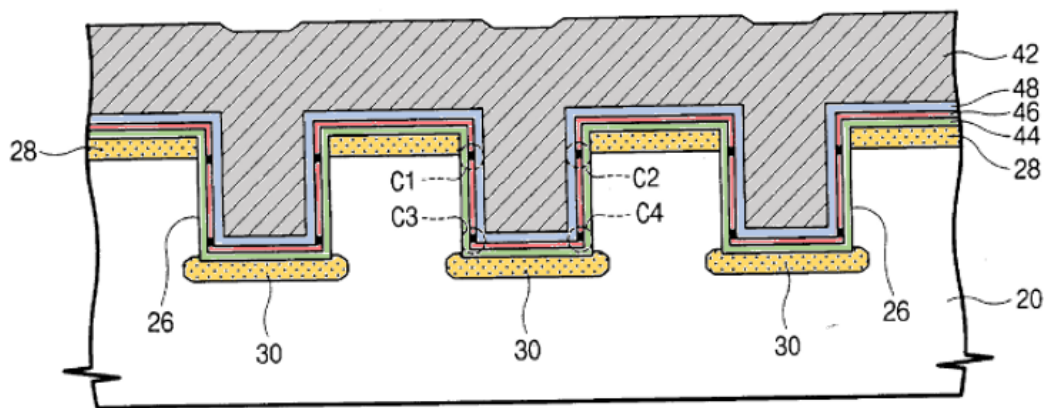
68. By the mid-2000s, a POSITA would have been aware of SONOS-type memory transistors with vertical structures —i.e., transistors with a channel extending vertically (perpendicular to the substrate), where the ONO stack is arranged along the sides of the vertical channel. A POSITA would have understood that this vertical structure could increase the storage capacity of the

memory device because electrons can be stored in the layers on both sides of the channel, rather than in just one horizontal layer above a channel.

69. Despite the difference in channel orientation, a POSITA would have understood that the vertical SONOS memory transistors operate using the same charge trapping principles as the horizontal SONOS memory transistors. This is reflected in numerous references—like the '365 patent itself—that apply the same charge-trapping layers in both vertically-oriented and horizontally-oriented devices. *See, e.g.*, Higuchi (Ex. 1021), Figs. 1A, 1B, 18A, 18B; Ex. 1022 (Jung), Figs. 1-3; Ex. 1025 (VDNROM), pp. 226-27 (“[T]he fabrication of this VDNROM device is basically compatible with planar CMOS technology”); Ex. 1028 (Kim '759), Figs. 1, 2 (horizontal embodiments), [0070] (vertically stacked ONO structure using same processes as horizontal embodiments); Ex. 1043 (Sekine), [0176]-[0181] (teaching planar structures of figures 1-36 may be applied to vertical 3D memory arrangements of figures 37-61).

70. A POSITA's general knowledge of vertically-oriented SONOS memory transistors prior to July 2012 is reflected, for example, in Choi (Ex. 1023), filed and published in 2003, which teaches a SONOS/SONNOS “trench” memory:

Fig. 9A



Ex. 1023 (Choi), Fig. 9A.

71. Choi teaches that the memory device includes: (i) substrate 20 with grooves 26 and diffusion areas 28 and 30 forming a vertical channel; (ii) silicon oxide tunnel insulating layer 44; (iii) charge trap insulating layer 46 with “at least one silicon nitride layer”; (iv) silicon oxide blocking insulating layer 48; and (v) doped polysilicon or metal gate conductive layer 42. Ex. 1023 (Choi), [0025], [0031]-[0033]. Choi teaches that this configuration is an improvement over the horizontal prior art because it may include more data storage “in the same horizontal dimensions as the conventional art.” *Id.*, [0034], [0005], [0006], [0025].

72. Ou (Exhibit 1024), filed in 2007 and published in 2009, provides further reflection of a POSITA’s knowledge of vertically-oriented SONOS-type

memory transistors prior to July 2012. Figure 4A of Ou depicts, for example, a SONONOS memory device with a vertical channel:

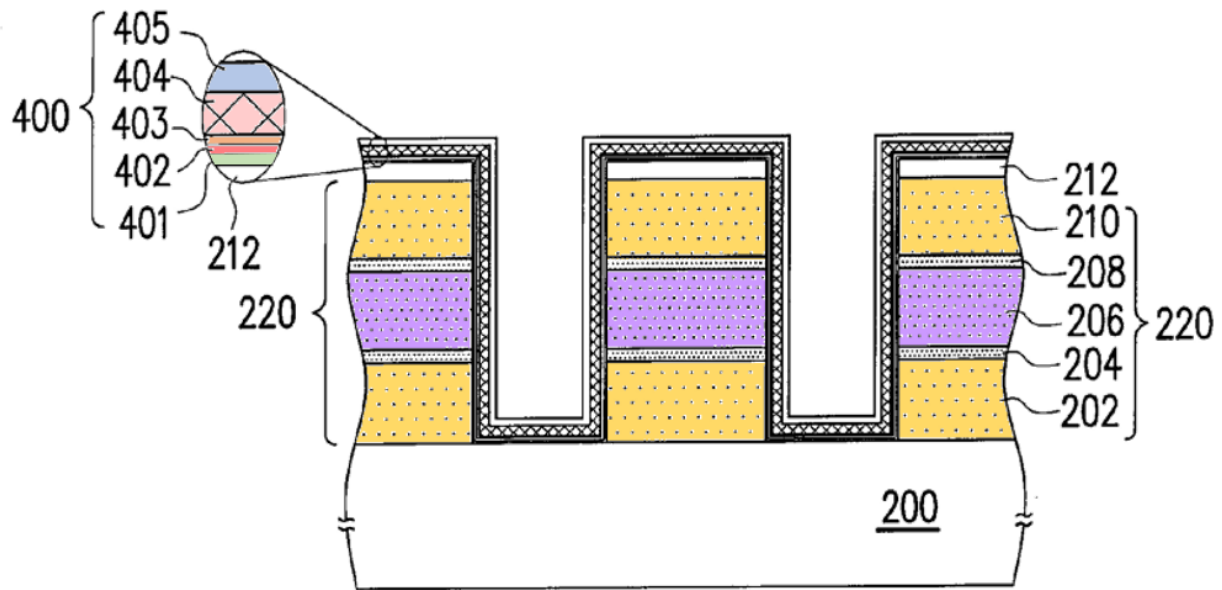
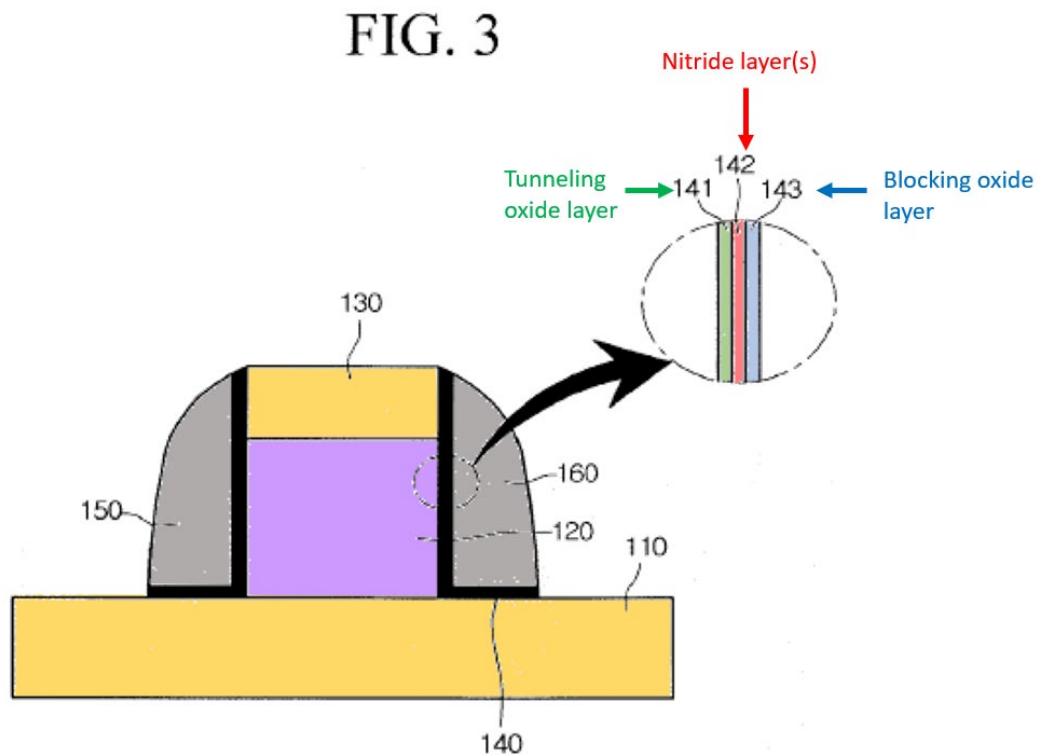


FIG. 4A

Ex. 1024 (Ou), Fig. 4A.

73. This embodiment has semiconductor layers (202, 206, and 210) that act as a source, channel, and drain (*id.*, [0068]); (ii) a first oxide layer (O1) 401 (green); (iii) a first nitride layer (N1) 402 (red); (iv) a second oxide layer (O2) 403 (orange); (v) a second nitride layer (N2) 404 (red); (vi) a third oxide layer (O3) 405 (blue). *Id.*, Fig. 4A, [0066]; *see also id.*, Fig. 4B, [0067] (teaching doped polysilicon gate formed abutting third oxide layer).

74. Jung (Exhibit 1022), filed in 2007 and published in 2008, shows another type of vertically-oriented SONOS-type memory in its figure 3 (annotated below), with a vertical polysilicon channel projecting up from a substrate that utilizes either an ONO stack 140 as shown in figure 3, or an ONONO stack of $\text{SiO}_2\text{—Si}_3\text{N}_4\text{—SiO}_2\text{—Si}_3\text{N}_4\text{—SiO}_2$ as identified in paragraph [0015]. Ex. 1022 (Jung), Figs. 3, 8, [0011]-[0015], [0025], [0026].



Ex. 1022 (Jung), Fig. 3.

75. VDNROM (Ex. 1025), published in 2006, is similar. Figure 1 of VDNROM (annotated below) depicts a vertically-oriented projecting channel surrounded by an ONONO stack:

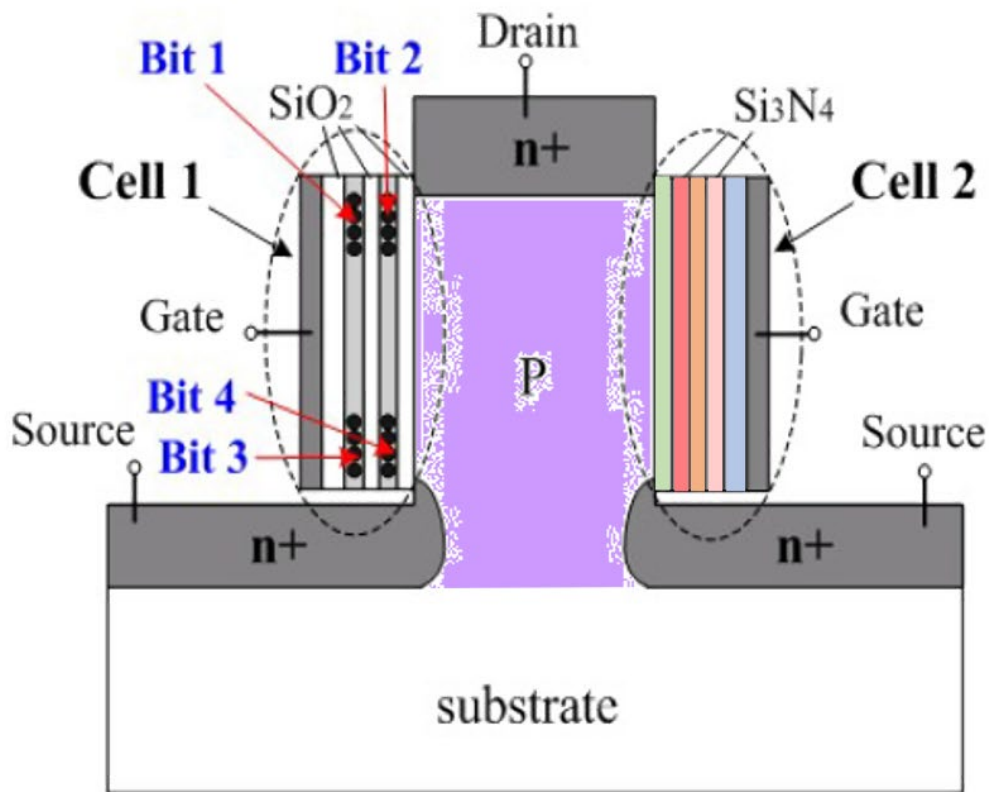
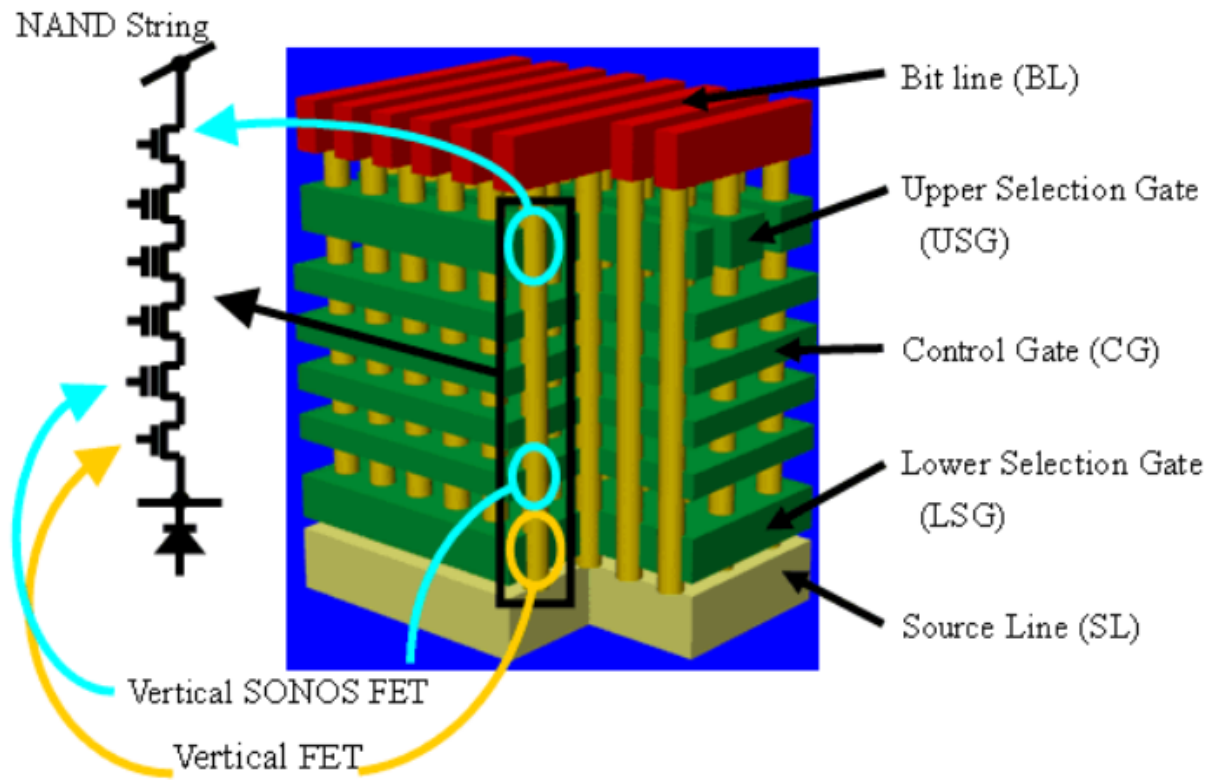


Fig. 1 Schematic cross sectional view of the proposed 4 bits/cell VDNROM flash memory.

Ex. 1025 (VDNROM), p. 226, Fig. 1.

76. By the mid-2000s, a POSITA would also have been aware of three-dimensional flash memory configurations (“3D NAND strings”) with vertical channels. For example, Toshiba announced its Bit Cost Scalable (“BiCS”) 3D NAND technology in 2007. Ex. 1026 (Tanaka), p.14 (Abstract); Ex. 1027 (Toshiba PR). In a press release announcing details of its vertical SONOS structure, Toshiba provided a figure showing the 3D NAND architecture:

The structure of the new memory cell



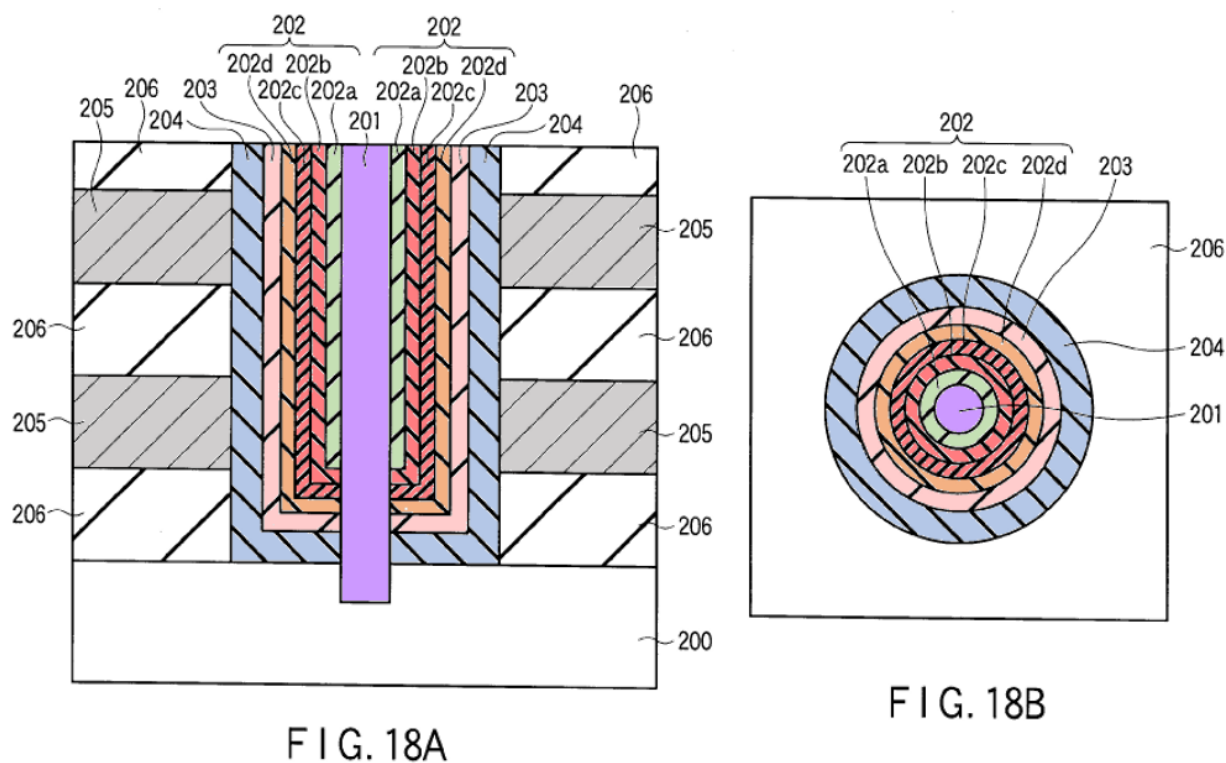
Ex. 1027 (Toshiba PR) (“Toshiba’s new method has a SONOS structure—silicon-oxide-nitride-oxide-silicon—and the electrical charge is held in a silicon-nitride film, which is formed inside gate holes.”).³

77. Higuchi (Ex. 1021), a June 2010 U.S. patent application publication, is also representative of a POSITA’s knowledge of the vertical 3D NAND

³ The ’365 patent describes “Bit-Cost Scalable or BiCS architecture” as part of the alleged invention. *See* Ex. 1001 (’365 patent), 17:3-16. I understand that the portions of the ’365 patent referring to BiCS were first added on July 1, 2012, more than five years after Toshiba announced BiCS architecture in June 2007. *See* Ex. 1026 (Tanaka); Ex. 1027 (Toshiba PR).

structure prior to July 2012. Higuchi teaches that its invention is an improvement over conventional horizontal SONOS structures, and provides inventive embodiments of both horizontal (e.g., Figs. 1-16) and vertical (e.g., Figs. 17-26) traps, demonstrating that the teachings are equally applicable to either configuration.

78. For example, Higuchi teaches a vertical 3D NAND memory transistor with a SONOS configuration in figure 18:



Ex. 1021 (Higuchi), Figs. 18A, 18B, [0131]-[0142].

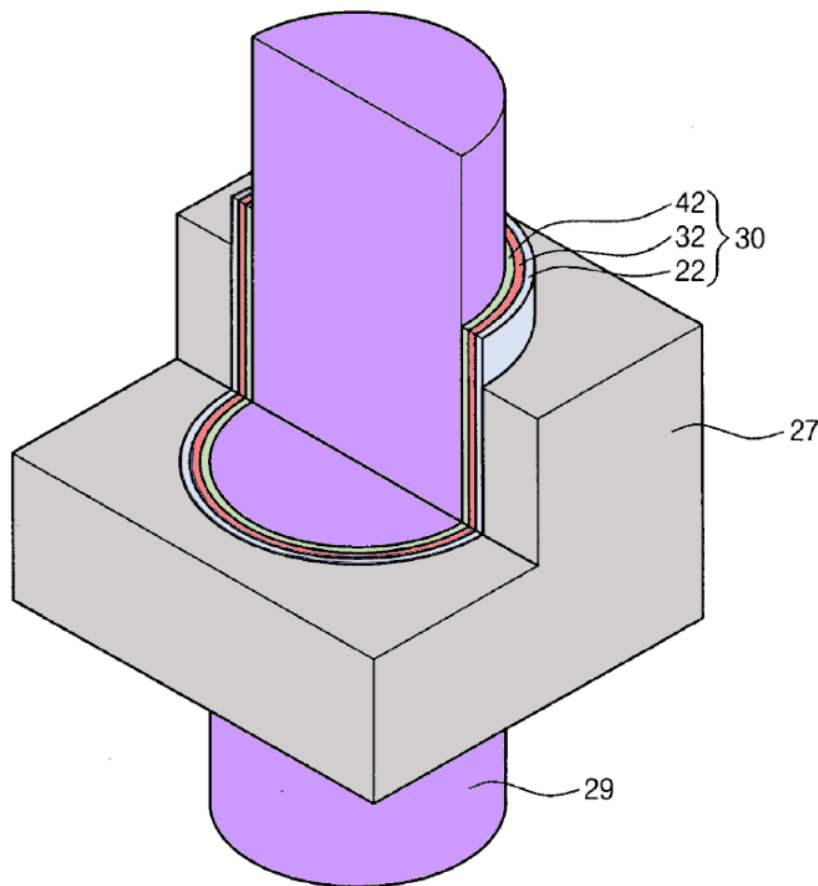
79. Higuchi explains that this vertical SONOS structure includes: (i) semiconductor region (silicon region) 201; (ii) oxide film 202a (silicon oxide); (iii) nitride film 202b (silicon nitride); (iv) oxynitride film 202c; (v) oxide film 202d

(silicon oxide); (vi) nitride charge-storage insulating film 203; (vii) block insulating film 204; and (viii) control gate electrode 205. Ex. 1021 (Higuchi), [0133]-[0134].

80. Kim '759 (Ex. 1028), a July 2010 U.S. patent application publication, is also representative of a POSITA's knowledge of vertical SONOS memory structures prior to July 2012. For example, Kim '759 teaches a vertical NAND memory transistor in its figure 5 that is similar to figure 8A of the '365 patent:

Fig. 5

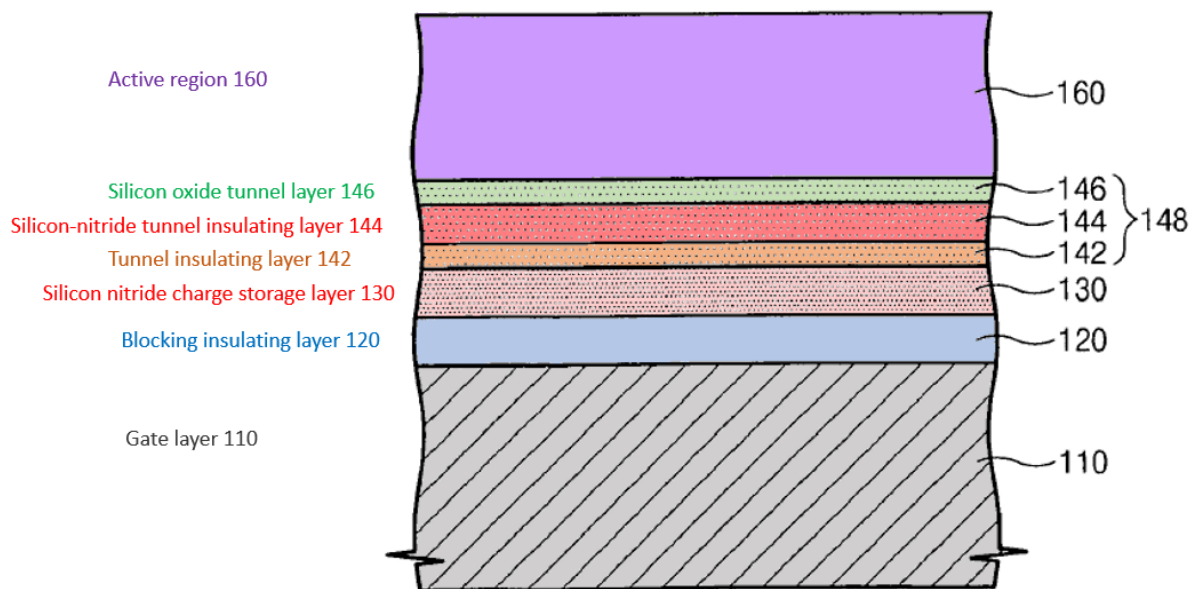
28



Ex. 1028 (Kim '759), Fig. 5; *compare id. with* Ex. 1001 ('365 patent), Fig. 8A.

81. Kim '759 teaches that the vertical SONOS memory device may be configured with a SONONOS structure with a stack comprising an oxide blocking layer (120), a silicon nitride charge storage layer (130), two tunnel insulating layers (142 and 144), and an oxide tunneling layer (146):

Fig. 2C



Ex. 1028 (Kim '759), Fig. 2C, [0037]-[0048]; *compare id. with* Ex. 1001 ('365 patent), Fig. 8B.

7. High work function gate electrodes

82. A POSITA also would have had general knowledge of the use of high work function gate electrodes with SONOS-type memory transistors prior to July 2012.

83. For example, the Kim Article (Ex. 1029), a 2007 article entitled, “A Comparison of N⁺ Type and P⁺ Type Polysilicon Gate in High Speed Non-Volatile Memories,” teaches that the use of a boron-doped p⁺ polysilicon gate in a SONOS memory device provides improved erase speed as compared to a n⁺ polysilicon gate, due to the p⁺ polysilicon gate having a higher work function. *See, e.g.,* Ex. 1029 (Kim Article), 000005 (“The erase speed of p⁺ polysilicon gate memory is much faster than that of n⁺ polysilicon gate memory.”), Fig. 7.

84. Beyond the Kim Article, there are many other representative examples of a POSITA’s general knowledge of the routine use of high work function gate electrodes with SONOS memory transistors. *See, e.g.,* Ex. 1016 (Lue ’189), [0084] (in preferred embodiments, high work function gates can be formed of metals, metal nitrides, or P⁺ polysilicon), [0086] (“High work function gate materials suppress gate electron injection into the trapping layer. . . . [T]he memory cells according to high work function gate material embodiments of the present invention are particularly suitable for use in NAND applications where elevated threshold voltages in the erased/reset state can be undesirable.”); Ex. 1017

(Lai '676), [0007], [0052] (“higher work-function metal gate has lower erase saturation”), [0067] (“For some applications, it is preferable to use materials having work functions higher than 4 eV, preferably higher than 4.5 eV”), [0124] (“A high work-function metal gate (such as Pt) is necessary to suppress the gate injection for these type cells.”); Ex. 1012 (Heo), [0064] (teaching the use of a high work function gate electrode to improve the efficiency and ease of operation of the flash memory); Ex. 1030 (Jeon), Fig. 1, [0009] (“The control gate 14 includes either N⁺ polysilicon with a work function of 4.1 eV or p⁺ polysilicon with a work function of 5.1 eV.”); Ex. 1031 (Shih), [0071] (“In some embodiments, the gate comprises a material having a work function greater than the intrinsic work function of n-type silicon. . . for example, greater than about 5 eV. Representative gate materials include p-type poly TiN, Pt, and other high work function metals and materials.”).

8. 3D NAND Fabrication

85. Prior to July 2012, a POSITA would have understood that 3D NAND devices could be fabricated using “gate first” processes and “gate last” processes.

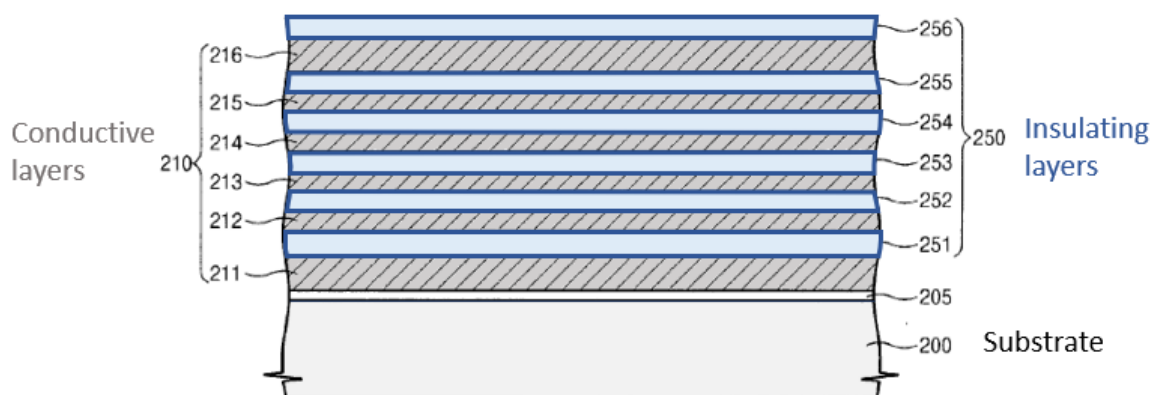
(a) Gate First Methodology

86. In a gate-first process, a 3D NAND device is fabricated by forming a series of alternating gate and dielectric layers on a substrate, creating holes through the layers down to the substrate, forming the charge trap structures (e.g., ONO,

ONNO, or ONONO) on the inner surface of the holes, and then forming a vertical channel in the middle of the hole.

87. An example of “gate first” methodology is shown in Kim ’759’s (Exhibit 1028) Figures 7A-7D. As shown in FIG. 7A, alternating conductive layers 211, 212, 213, 214, 215, and 216 (which form gates in the finished structure) and insulating layers 251, 252, 253, 254, 255, and 256 may be deposited on substrate 200:

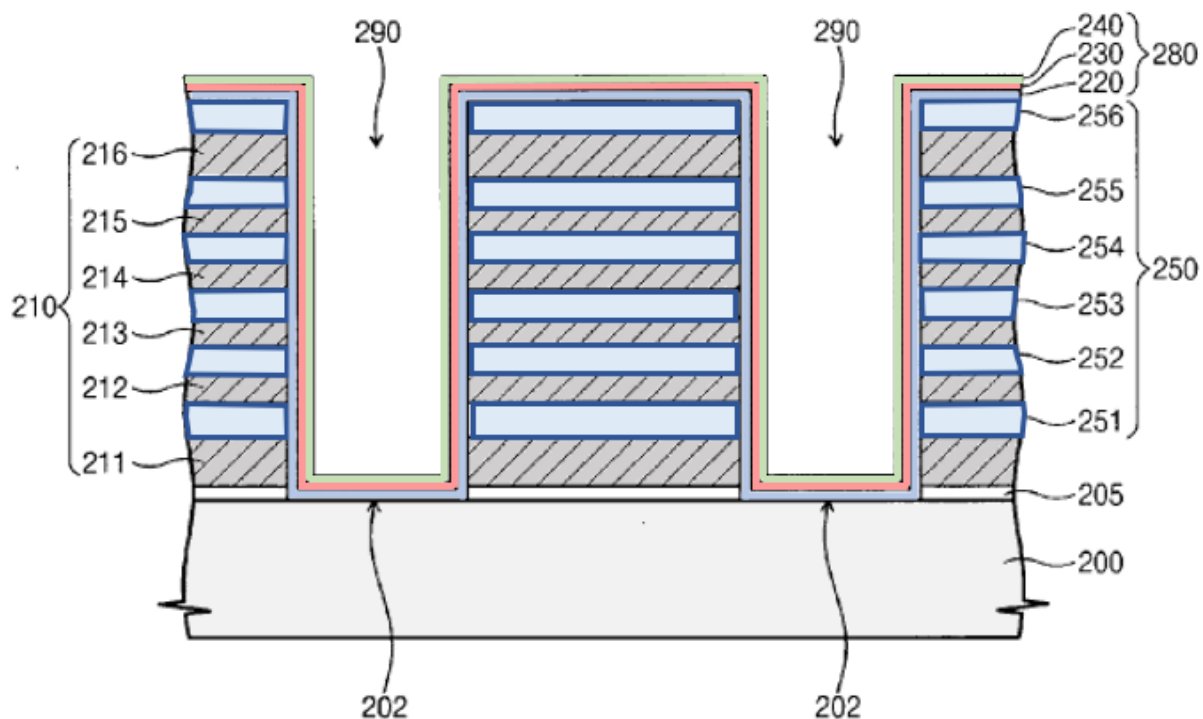
Fig. 7A



Ex. 1028 (Kim ’759), Fig. 7A, [0065]-[0068.]

88. Next, as shown in Fig. 7B, openings 290 may be formed, after which blocking insulating layer 220, charge storage layer 230, and tunnel insulating layer 240 may be formed.

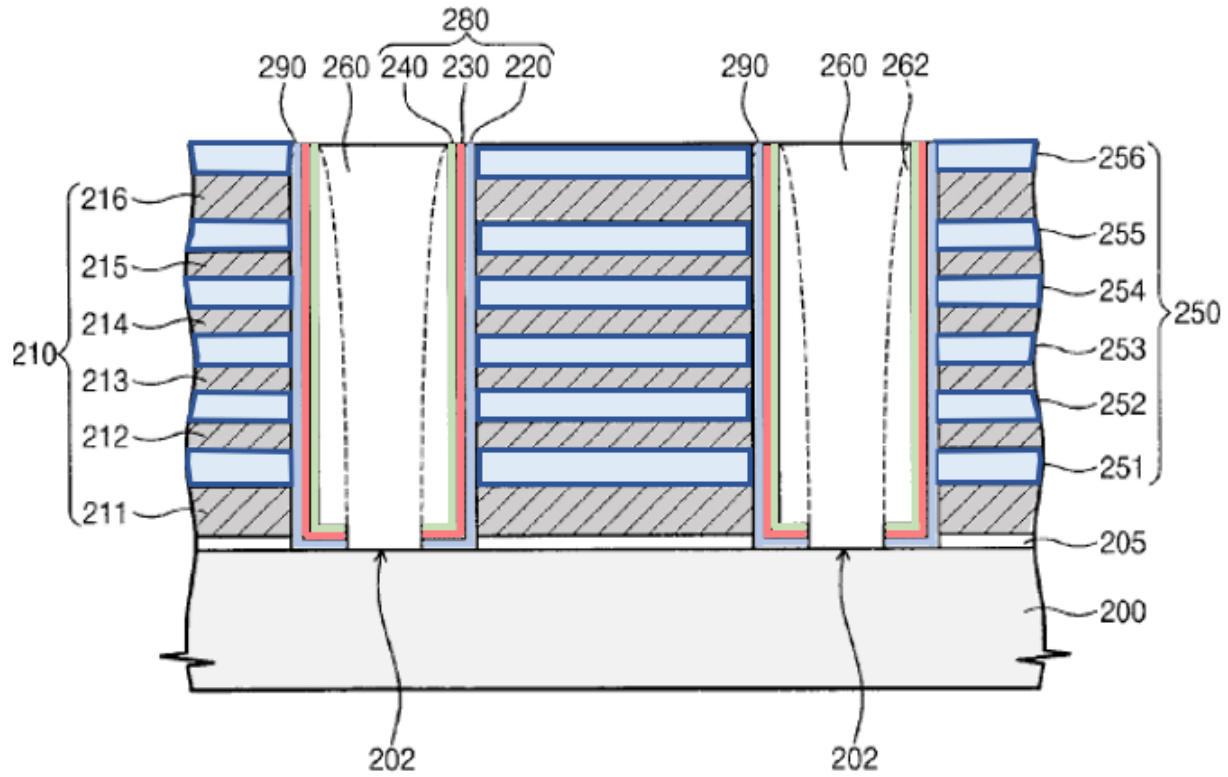
Fig. 7B



Ex. 1028 (Kim '759), Fig. 7B, [0069].

89. Next, as shown in Fig. 7C, the top of substrate 200 is exposed by etching away layers 220/230/240 at the base of opening 290 and active portion 260 is filled in opening 290 to form a vertical silicon channel.

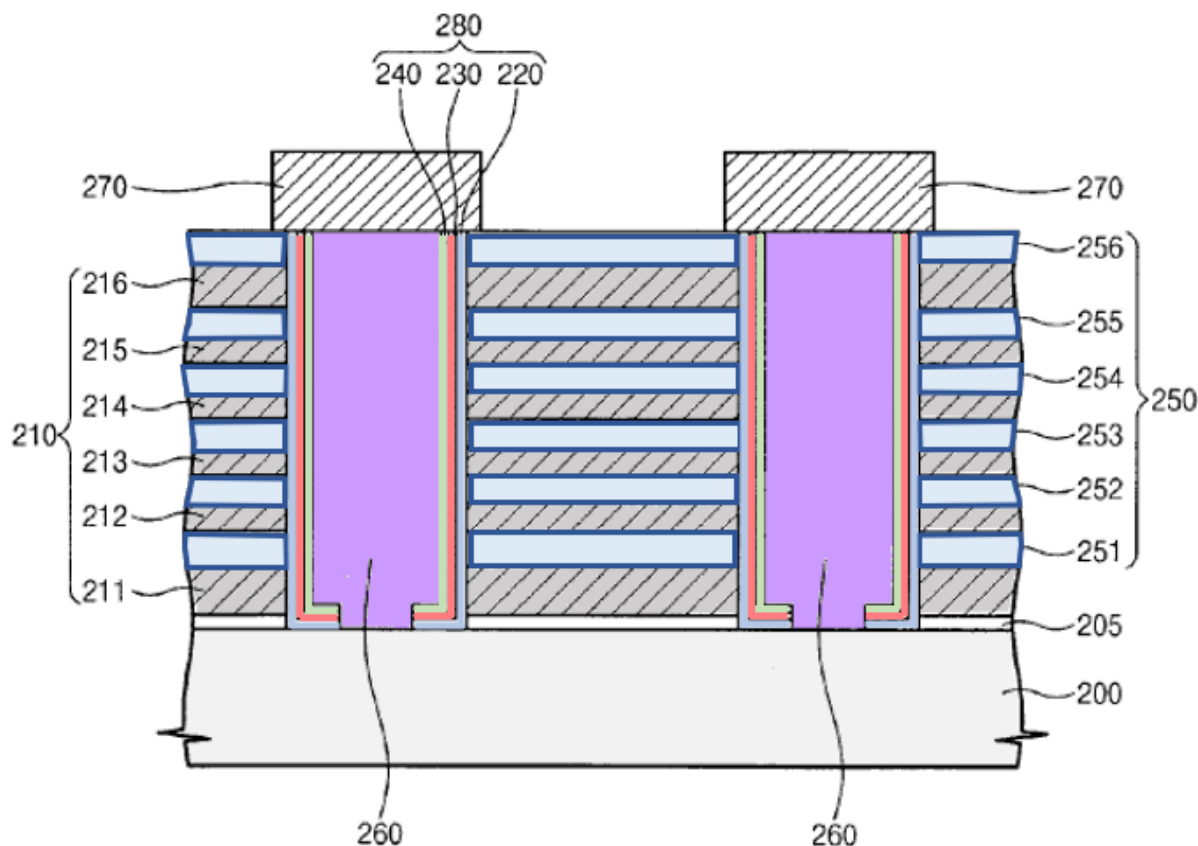
Fig. 7C



Ex. 1028 (Kim '759), Fig. 7C, [0071]-[0072].

90. Finally, as shown in Fig. 7D, bit lines are formed atop the active portions 260.

Fig. 7D



Ex. 1028 (Kim '759), Fig. 7D, [0073].

91. Higuchi's (Ex. 1021) provides a similar example of a gate first methodology in Figures 18-21.

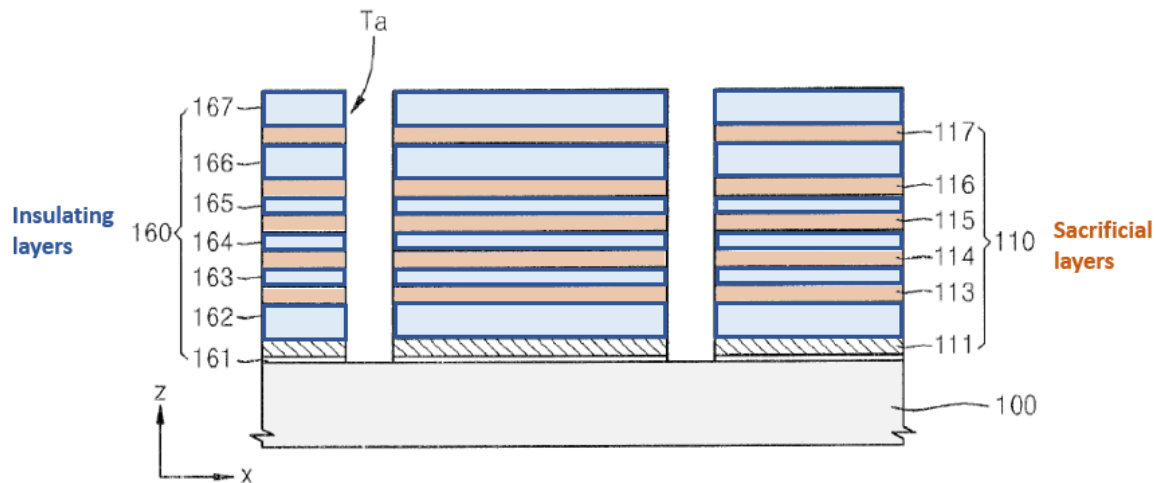
(b) Gate Last Methodology

92. The second way to fabricate 3D NAND devices is a "gate last" process where, instead of starting with a series of gate and dielectric layers formed on a substrate (the "gate first" process), a series of sacrificial and dielectric layers

are formed. Next, like the “gate first” process, holes are created through the layers down to the substrate, the charge trap structures (e.g., ONO, ONNO, or ONONO) are formed on the inner surface of the holes, and the vertical channel is then formed in the middle of the hole. Finally, the sacrificial layers are removed and replaced with gate electrodes.

93. An example of the gate last methodology is shown in Figures 4A-4N of Yang '696 (Ex 1032), a patent publication filed in 2012. Yang teaches providing a stack of insulating (161 to 167) and sacrificial (111 to 117) layers on substrate 100 and forming openings (Ta' and Ta) through the layers:

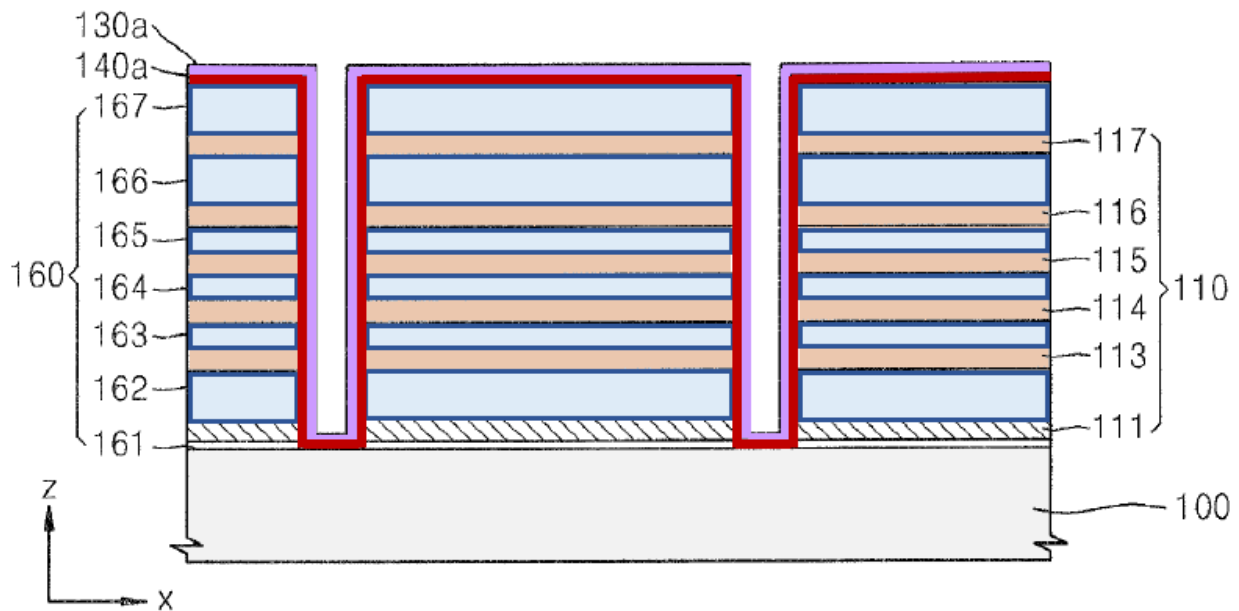
FIG. 4C



Ex. 1032 (Yang '696), Figs. 4A-4C, [0062]-[0073].

94. Yang then teaches forming gate dielectric layer 140a (including a blocking insulating layer, a charge storage layer, and a tunneling insulating layer) and a first polysilicon or single crystalline silicon channel layer 130a.

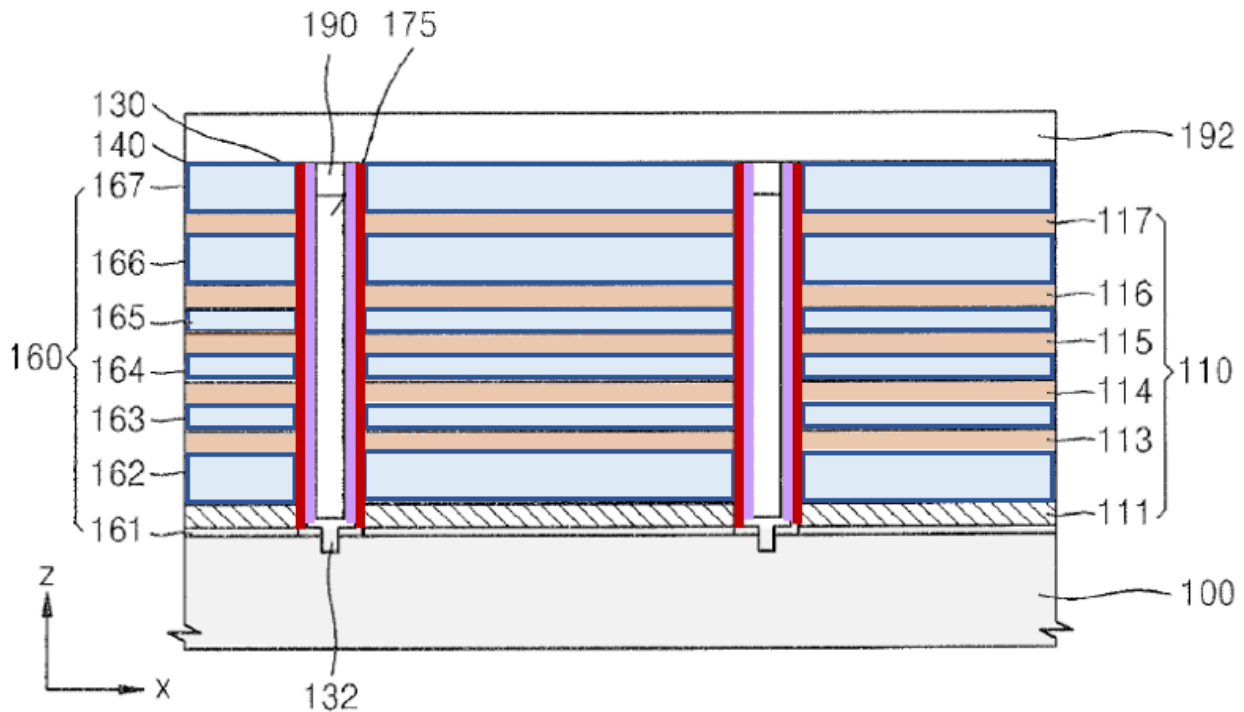
FIG. 4E



Ex. 1032 (Yang '696), FIGS. 4D-4F, [0074]-[0076].

95. Yang '696 next teaches forming contact portion 132, channel region 130, insulating layer 175, conductive layer 190, and insulating layer 192:

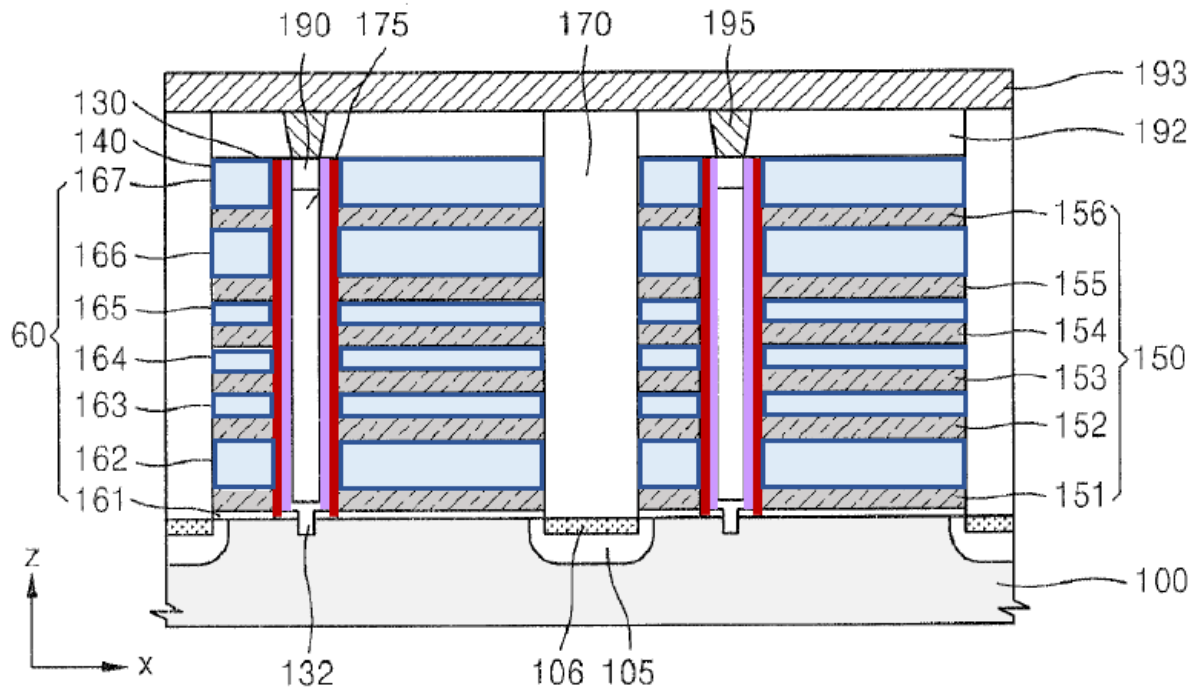
FIG. 4I



Ex. 1032 (Yang '696), Figs. 4G-4I, [0078]-[0082].

96. Yang '696 next teaches, in Figs. 4J-4L, etching second openings Tb and then etching away sacrificial layers 111 and 113-117 to form lateral openings T2 and T1. Ex. 1032 (Yang '696), Figs. 4J-4L, [0083]-[0091]. Then, conductive material is filled into lateral openings T1 and T2 to form gate electrodes 150. Ex. 1032 (Yang '696), Fig. 4M, [0092]-[0094]. Finally, impurity region 105, common source line CSL 106, insulating region 170, bitline contact plugs 195, and bitlines 193 are formed.

FIG. 4N



Ex. 1032 (Yang '696), Fig. 4N, [0095]-[0098].

97. Many additional examples of the gate last methodology using sacrificial layers would have been known to a POSITA prior to July 2012. *See, e.g.,* Ex. 1033 (Jang), Figs. 6-14; Ex. 1034 (Lee '247), Figs. 2-9; Ex. 1035 (Lee '086), Figs. 8-17; Ex. 1036 (Kim '064), Figs. 4-12.

IV. CHALLENGED CLAIMS

98. I understand that Petitioners are challenging the validity of claims 1-3, 5-12, 14-23, and 25-45 of the '365 patent (the "Challenged Claims"), which are

reproduced in Appendix 3. In forming my opinions, I have considered all of the claims of the '365 patent, as well as portions of the prosecution history.

V. PRIORITY DATE OF CHALLENGED CLAIMS

99. In performing my analysis, I have used July 1, 2012—the filing date of the application for U.S. Patent No. 8,633,537 (the '537 patent)—as the relevant priority date for the reasons set forth below.

100. On its face, the '365 patent identifies nine related U.S. patent applications:

	App No.	Filing Date	Patent No.	
A	60/940,160	5/25/2007	n/a	“the '160 provisional”
B	12/152,518	5/13/2008	8,063,434	“the '434 patent”
C	13/288,919	11/3/2011	8,859,374	“the '374 patent,” divisional of B
D	13/539,466	7/1/2012	8,633,537	“the '537 patent,” continuation-in-Part of C
E	14/159,315	1/20/2014	9,093,318	“the '318 patent,” continuation of D
F	14/811,346	7/28/2015	9,502,543	“the '543 patent,” continuation of E
G	15/335,180	10/26/2016	9,929,240	“the '240 patent,” continuation of F
H	15/864,832	1/8/2018	10,312,336	“the '336 patent,” continuation of G
I	16/429,464	6/2/2019	10,903,325	“the '325 patent,” continuation of H
J	17/157,350	1/25/2021	11,456,365	“the '365 patent,” continuation of I

101. I understand that a patent cannot claim priority to earlier applications if, from the perspective of an ordinary artisan, the patent claims include new matter not present in those earlier applications. *See* Appendix 4 (Understanding of the Law).

102. To determine the earliest possible priority date for the claims of the '365 patent, I reviewed the three earliest-filed applications—the '160 provisional application (filed May 25, 2007), the application for the '434 patent (filed May 13, 2008), and the application for the '374 patent (filed November 3, 2011) (collectively, the “Earlier Applications”). *See* Ex. 1037 ('160 Provisional App.); Ex. 1038 ('434 Pros. Hist.); Ex. 1039 ('374 Pros. Hist.). In my opinion, from the point of view of an ordinary artisan, these Earlier Applications do not support the claims of the '365 patent.

103. Each of the independent claims of the '365 patent requires a vertically oriented semiconductor memory device or a method of fabricating the same. Claim 1 requires, for example, “forming on an inside sidewall of the tunnel dielectric layer a **vertical channel** having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.” Ex. 1001 ('365 patent), claim 1. Claim 23 similarly requires “forming on an inside sidewall of the tunnel dielectric layer an annular shaped **vertical channel** having a semiconductor material extending from the substrate through the opening towards a top of the stack of layers.” *Id.*, claim 23. Claim 35 requires “a channel region oriented substantially perpendicular to the semiconductor substrate, the channel region formed in a substantially annular shape.” *Id.*, claim 35.

104. The Earlier Applications are silent as to any “vertical channel” or “channel region oriented substantially perpendicular to the semiconductor substrate.” Rather, the memory transistors disclosed in the Earlier Applications are exclusively horizontally-oriented (i.e., the channels extend horizontally between diffusion regions parallel to a substrate). For example, horizontal channel 312 of Figure 3 of the application for the ’434 patent—which is the same as figure 3 of the application for the ’374 patent and figure 3 of the ’365 patent—is representative of the horizontal channel disclosed in the prior related applications:

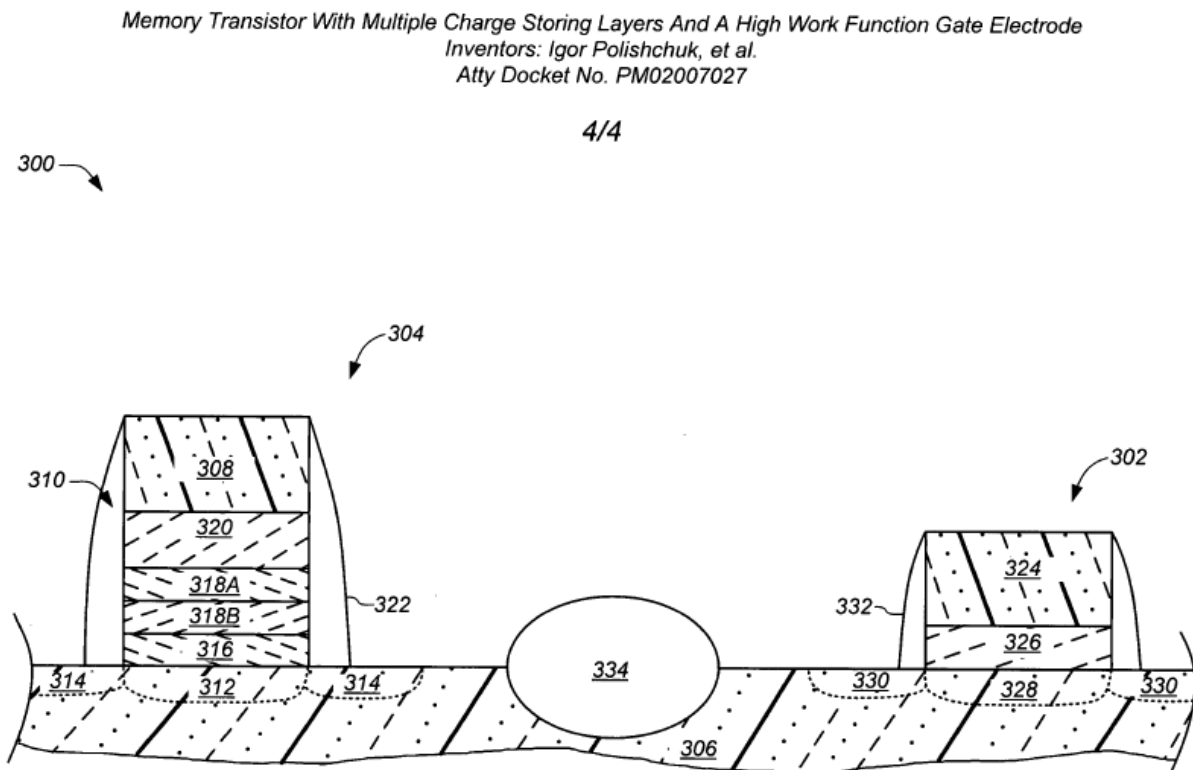


FIG. 3

Ex. 1038 (’434 Pros. Hist.), 000139.

105. The Earlier Applications do not include any of the vertical channel embodiments of the '365 patent, which are found in figures 8A-8B, 9A-9F and 10A-10F and the accompanying written description (*see* Ex. 1001 ('365 patent), 17:17-20:7). Rather, those figures and the accompanying written description of the vertical channel embodiments were first added in the continuation-in-part application for the '537 patent, which was filed on July 1, 2012. *See* Ex. 1040 ('537 Pros. Hist.), 000218-278; *compare id. with* Ex. 1038 ('434 Pros. Hist.), 000111-139; Ex. 1039 ('374 Pros. Hist.), 000158-199.

106. Because features of the independent claims of the '365 patent (claims 1, 23, and 35) are not disclosed in any of the Earlier Applications, I understand that the earliest possible priority date for the claims of the '365 patent (claims 1-45) is July 1, 2012—the date the application for the '537 patent was filed.

VI. LEVEL OF ORDINARY SKILL IN THE ART

107. The '365 patent is in the field of non-volatile semiconductor memory. *See, e.g.*, Ex. 1001 ('365 patent), 1:31-36. Each of the Challenged Claims is directed to either a “semiconductor memory device” (*see id.*, claim 35) or method of fabricating the same (*see id.*, claims 1, 23). In determining the characteristics of a hypothetical person of ordinary skill in the art (a “POSITA”) in the area of the '365 patent as of July 1, 2012, I considered several things, including various prior art techniques relating to the structure and fabrication of memory transistors

and the rapidity with which innovations were made in those areas. I also considered the sophistication of the technologies involved, and the educational background and experience of those actively working in the field at the time. I also considered the level of education that would be necessary to understand the '365 patent. Finally, I placed myself back in the relevant period of time and considered the engineers that I have worked with in the field of non-volatile semiconductor memory.

108. I am familiar with the knowledge and capability that a POSITA would have possessed in the field of the '365 patent as of July 1, 2012 based on my personal experience with semiconductor devices and fabrication in relation to both academia and industry. It is my opinion that a POSITA as of July 1, 2012 would have had at least (1) a master's degree in electrical engineering, materials science, physics, or a related degree, and at least 3-5 years of experience in semiconductor devices and fabrication technologies; or (2) a bachelor's degree in electrical engineering, materials science, physics, or a related degree, and at least 5-6 years of experience in semiconductor devices and fabrication technologies.

109. As reflected in my curriculum vitae (attached as Appendix 1), my expertise met or exceeded a POSITA's as of July 2012.

110. In view of the types of problems encountered in the art and prior art solutions to those problems, it is my opinion that a POSITA with the level of skill described above would have been familiar with the following:

- Floating gate flash memory technology (*see* Part III.C.2);
- The structure and composition of SONOS-type memory devices (*see* Part III.C.3, above);
- SONNOS and SONONOS configurations of SONOS-type memory devices (*see* Parts III.C.4 and 5, above);
- Vertically-oriented configurations of SONOS-type memory transistors, including 3D NAND structures (*see* Part III.C.6);
- The use of high work function materials, such as p+ doped polysilicon, to form gate electrodes for SONOS-type memory devices (*see* Part III.C.7); and
- Fabrication processes for both horizontal and vertical flash memories, including gate-first and gate-last methodologies (*see* Part II.C.8).

VII. CLAIM CONSTRUCTION

111. For purposes of this declaration, I have considered the claim language, specification, and prosecution history to determine the meaning of the claim language as it would have been understood by a POSITA at the time of the invention.

A. “oxygen-rich nitride” and “oxygen-lean nitride”

112. Dependent claims 6, 7, 8, 25, 26, 27, 34, 38, 39, and 40 each refer to “oxygen-lean” and “oxygen-rich” nitride layers. The ’365 patent does not

expressly define the boundaries of when a nitride layer is “oxygen-rich” or “oxygen-lean.” But the ’365 patent states with respect to the figure 6 embodiment only that:

By oxygen-rich it is meant wherein a concentration of oxygen in the oxygen-rich first nitride layer 616a is from about 15 to about 40%, whereas a concentration of oxygen in [an] oxygen-lean second nitride layer 616b is less than about 5%.

Ex. 1001 (’365 patent), 13:57-61.

113. Regardless of the outer boundaries of “oxygen-lean” and “oxygen-rich,” a POSITA would have understood, based on the figure 6 embodiment, that (i) a nitride layer with about 5% or less oxygen is within the bounds of “oxygen-lean”; and (ii) a nitride layer with about 15% or more oxygen is within the bounds of “oxygen-rich.”

B. “high work function gate electrode”

114. Dependent claims 12, 31, and 37 of the ’365 patent require “a high work function gate electrode.” This term was well-known to a POSITA prior to July 2012. *See* Part III.C.7 (providing numerous examples of “high work function” gate electrodes, including p⁺ doped polysilicon and metal gates).

115. The ’365 patent does not define “high work function gate” in a way that departs from the common understanding of that term. To the contrary, the

specification confirms that, “[b]y high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased.” Ex. 1001 (’365 patent), 4:7-9. The ’365 patent also gives the following examples of “high work function”:

In one embodiment, the polysilicon layer 216 is doped following the growth or formation in the LPCVD process using ion implantation process. For example, the polysilicon layer 216 can be doped by implanting boron (B^+) or BF_2 ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about $1e14\text{ cm}^{-2}$ to about $1e16\text{ cm}^{-2}$ to form an N-type (NMOS) SONOS memory transistor and, preferably, a P-type (PMOS) logic transistor having high work function gate electrodes.

Ex. 1001 (’365 patent), 7:31-43.

116. As such, POSITA would have understood “high work function gate electrode” in the context of the ’365 patent to have its ordinary meaning and encompass gate electrodes comprised of, for example, polysilicon doped with p-type impurities, such as boron, as well as other materials known as high work function materials in the prior art. *See* Part III.C.7.

C. “the [second] oxygen-rich nitride layer is formed on the inside sidewall of the [first] oxygen-lean nitride layer”

117. Claims 7, 26, and 40 require that “the [second] oxygen-rich nitride layer is formed on the inside sidewall of the [first] oxygen-lean nitride layer.” A POSITA would have understood, in the context of the ’365 patent, that “formed on” does not require direct contact. Rather, an oxygen-rich layer may be “formed on” the inside sidewall of an oxygen-lean layer even when there is an intermediate oxide layer between the oxygen-rich layer and the oxygen lean layer.

118. A POSITA would have understood this to be the proper construction of “formed on” in the context of the ’365 patent due to the claims of the ’365 patent—particularly the interaction of claims 26 and 27. Claim 26 requires the oxygen-rich nitride layer to be “formed on” the sidewall of the oxygen-lean nitride layer. Ex. 1001 (’365 patent), claim 26. Claim 27 depends from claim 26 and further requires “forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.” *Id.*, claim 27. Taken together, a POSITA would understand that the oxygen-rich nitride layer can be both “formed on” the sidewall of the oxygen-lean nitride layer (claim 26) and, at the same time, have an anti-tunneling layer “between” the oxygen-rich and oxygen-lean nitride layers.

D. Dependent Claim 43

119. Claim 43 recites a semiconductor memory device, “wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer,

wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer **by a sacrificial layer.**”

120. Claim 43 thus recites a “stack of layers” that has both a “gate layer” and “sacrificial layer.” But the ’365 patent teaches that, in fabricating a memory device, sacrificial layers are replaced by gate material. Ex. 1001 (’365 patent), Fig. 10, 19:20-20:8. Thus, a POSITA would have understood that the reference to “a sacrificial layer” in claim 43 is a typographical error and would have understood the wherein clause to mean: “wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the gate ~~a sacrificial~~ layer.” This is what is illustrated in, for example, figure 9F of the ’365 patent (reproduced below), where gate layer 908 separates first/lower dielectric layer 902 and second/upper dielectric layer 910:

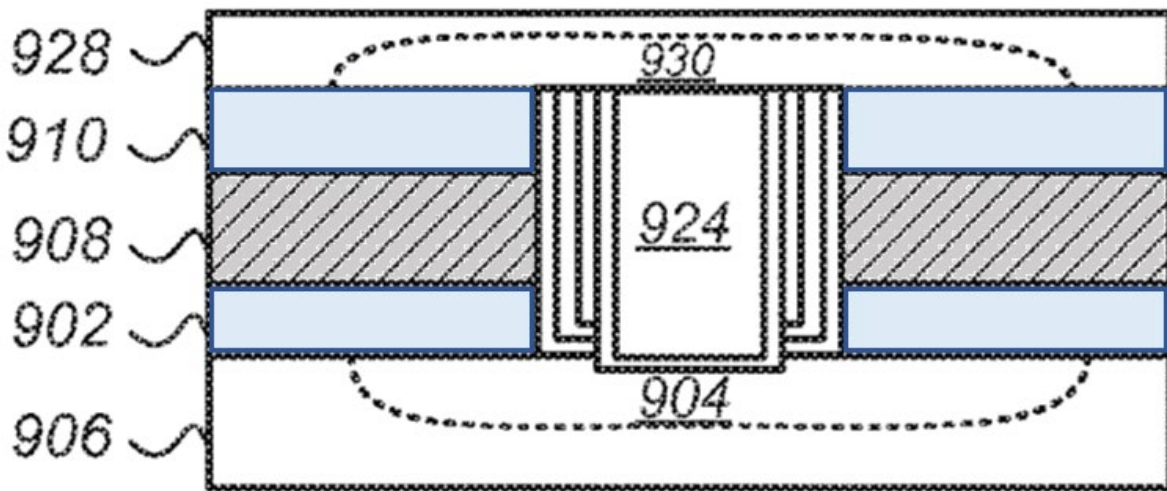


FIG. 9F

Ex. 1001 ('365 patent), Fig. 9F, 18:15-19:19.

VIII. SUMMARY OF ASSERTED PRIOR ART

121. As is evident from the background provided above, there are many prior art patents and publications that teach the features of the '365 patent.

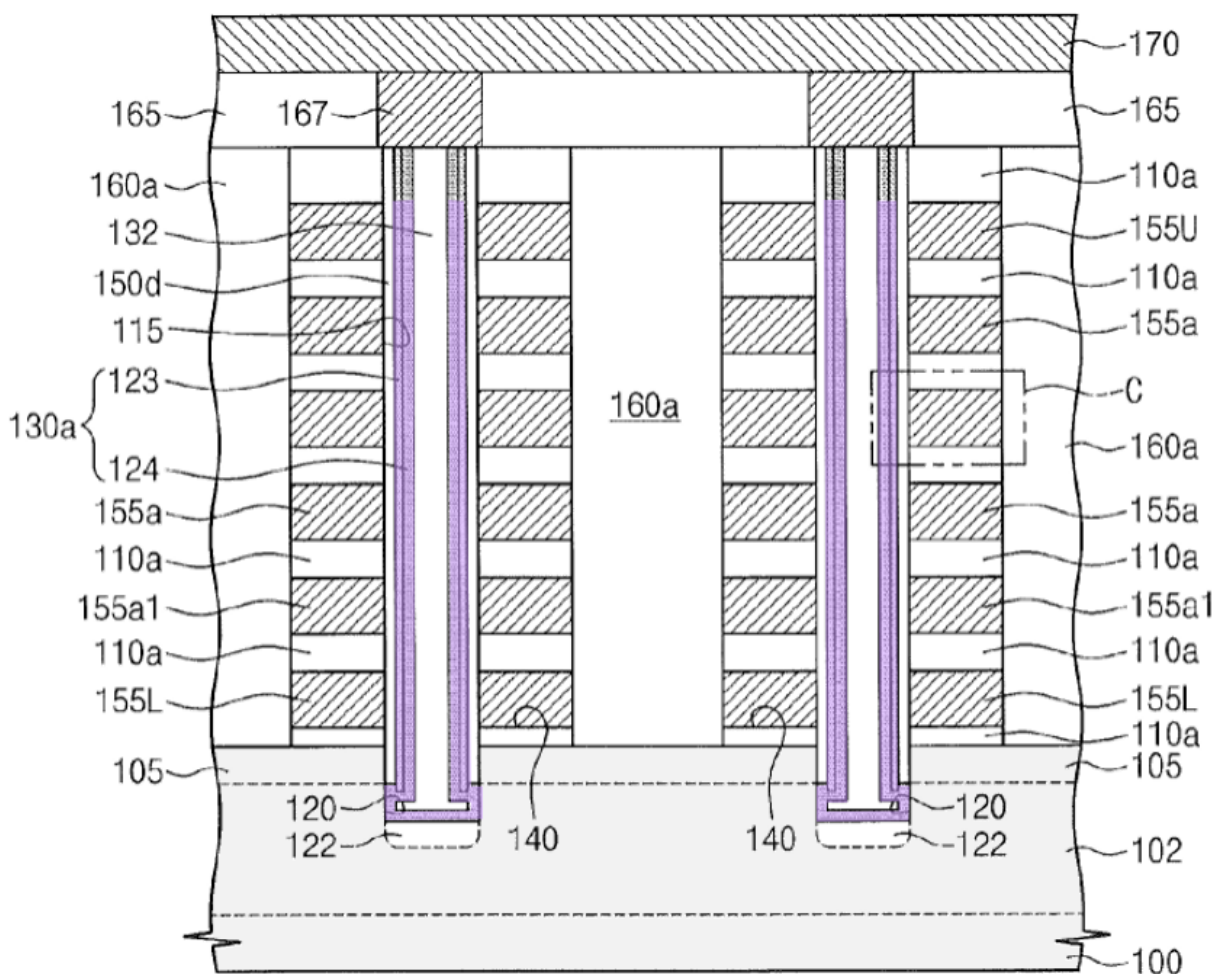
Multiple pre-2012 references already taught ONNO/ONONO stacks, oxygen-rich and oxygen-lean nitride layering, anti-tunneling oxides, and high-work-function gates, all as routine techniques for balancing retention, program/erase speed, and CMOS compatibility. Along with the materials discussed in the background and listed in Appendix 2, I have reviewed and considered the following prior art in forming my opinions in this matter.

A. Lee '255 (Exhibit 1004)

122. Lee '255 (Exhibit 1004) is a copy of U.S. Patent Application Publication 2012/0068255, entitled “Three-Dimensional Semiconductor Memory Devices.” Lee was published on March 22, 2012 from an application filed on August 29, 2011. Lee identifies three inventors: Changhyun Lee, Byoungkeun Son, and Hyejin Cho. I understand that Lee '255 is considered prior art to the challenged claims because it was filed by another and published before July 1, 2012.

123. I understand that Applicants listed Lee '255 on an information disclosure statement submitted during the prosecution of the '365 patent, along with more than 300 other references Applicants listed on such statements. I understand that the Examiner did not cite or apply Lee '255 in any Office Action, nor provide any substantive analysis of Lee '255 in allowing the claims of the '365 patent. *See* Part III.C.

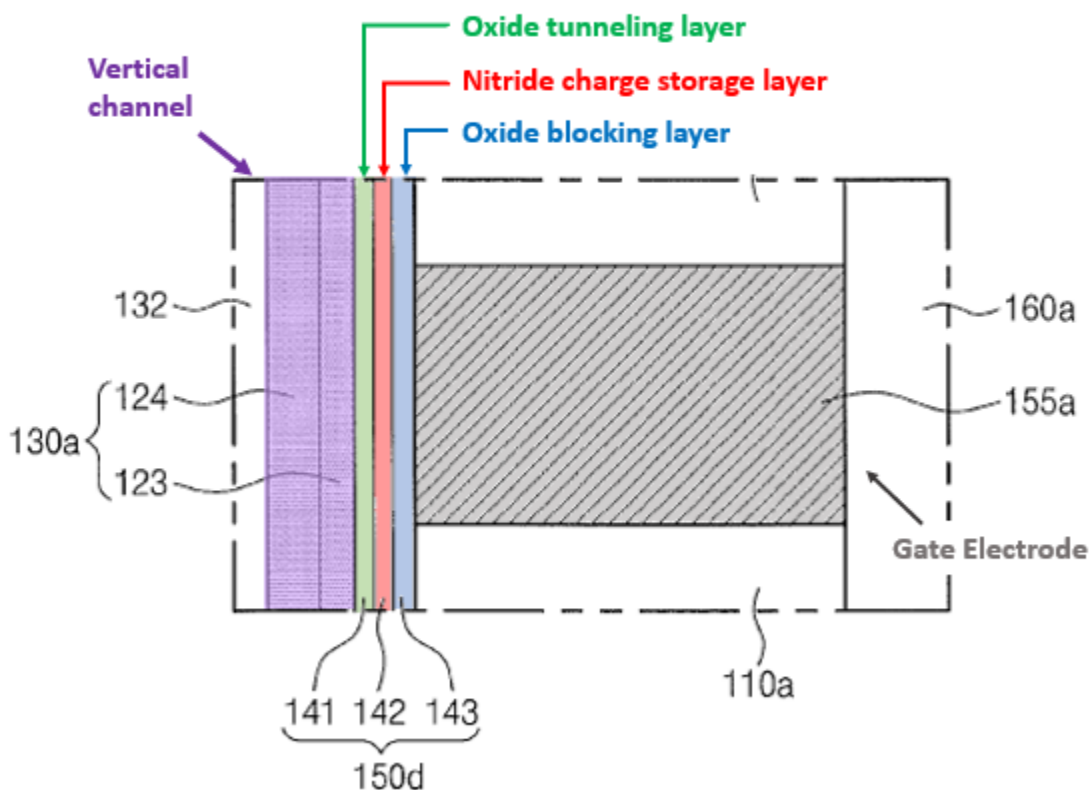
124. Lee '255 teaches “a semiconductor device and a method of fabricating the same and, more particularly, . . . a three-dimensional (3D) semiconductor memory device.” Ex. 1004 (Lee), [0002]-[0004]. For example, the 3D memory device depicted in figure 4A (annotated below) includes a vertical channel 130a (purple) that passes through a stack of layers (110a, 155L, 155a, 155U) formed over a substrate 100 (gray). *Id.*, [0052]-[0054], [0063].



Ex. 1004 (Lee), Fig. 4A.

125. To store charges, Lee teaches that a gate dielectric layer 150d is formed to surround the vertical channel 130a. The gate dielectric layer 150d includes an oxide tunneling layer 141 (green), a nitride charge storage layer 142 (red), and an oxide blocking layer 143 (blue), as shown in this annotated version of figure 4B:

Fig. 4B



Ex. 1004 (Lee '255), Fig. 4B, [0057], [0074].

126. A POSITA would have understood that Lee '255 is analogous art to the '365 patent because it teaches improvements to non-volatile memory devices generally, and charge trap memory devices specifically.

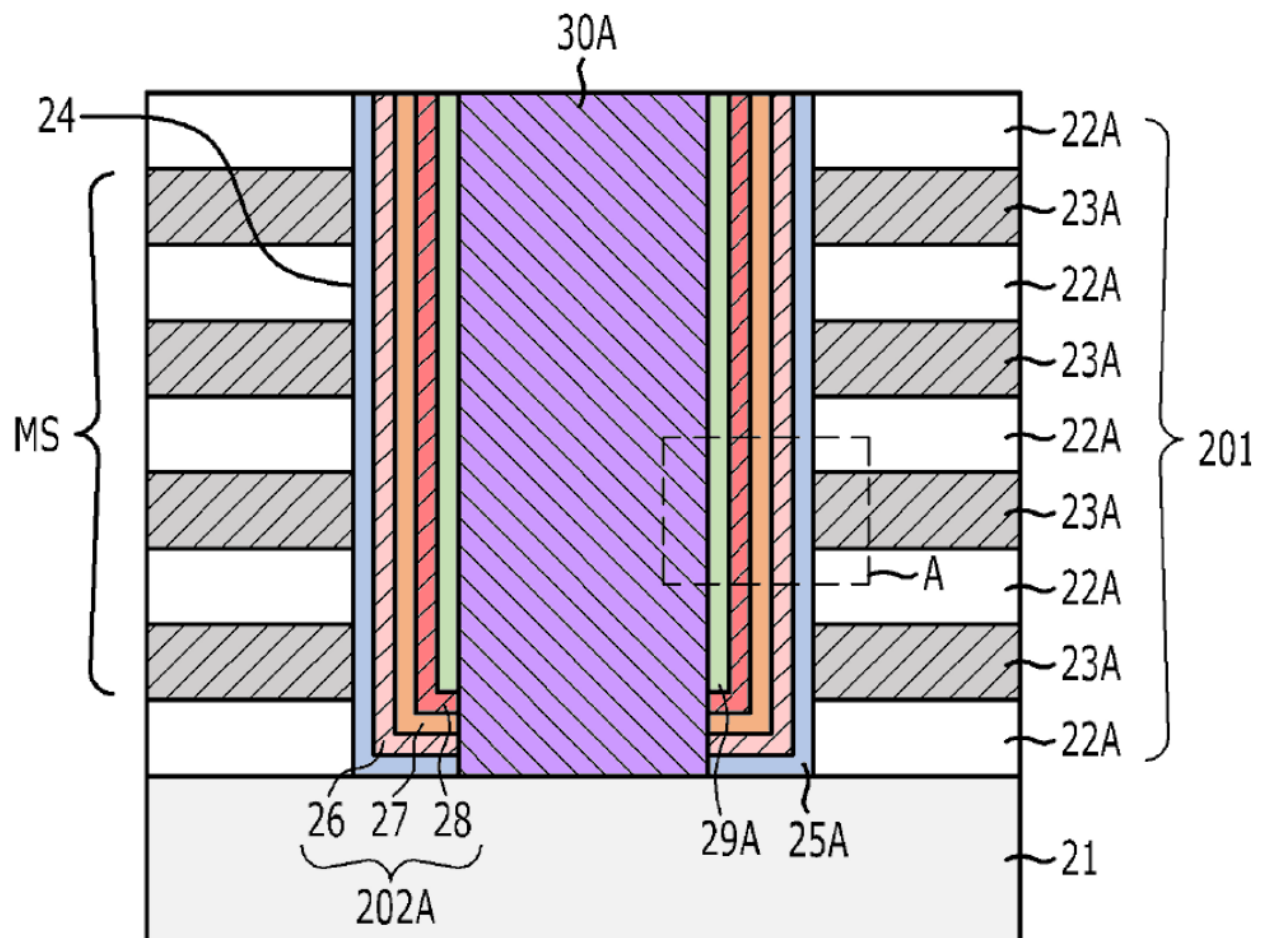
B. Lee '961 (Exhibit 1005)

127. Lee '961 (Exhibit 1005) is a copy of Korean Patent Publication No. 2011-0118961, entitled "Non-Volatile Memory Devices and Methods of Making Them," and the certified English translation of the same. Lee '961 was published on November 2, 2011 from an application filed on April 26, 2010. Lee '961

identifies three inventors: Gi Hong Lee, Jae Hyung Koo, and Beom Yong Kim. I understand that Lee '961 is considered prior art to the challenged claims because it was published before July 1, 2012.

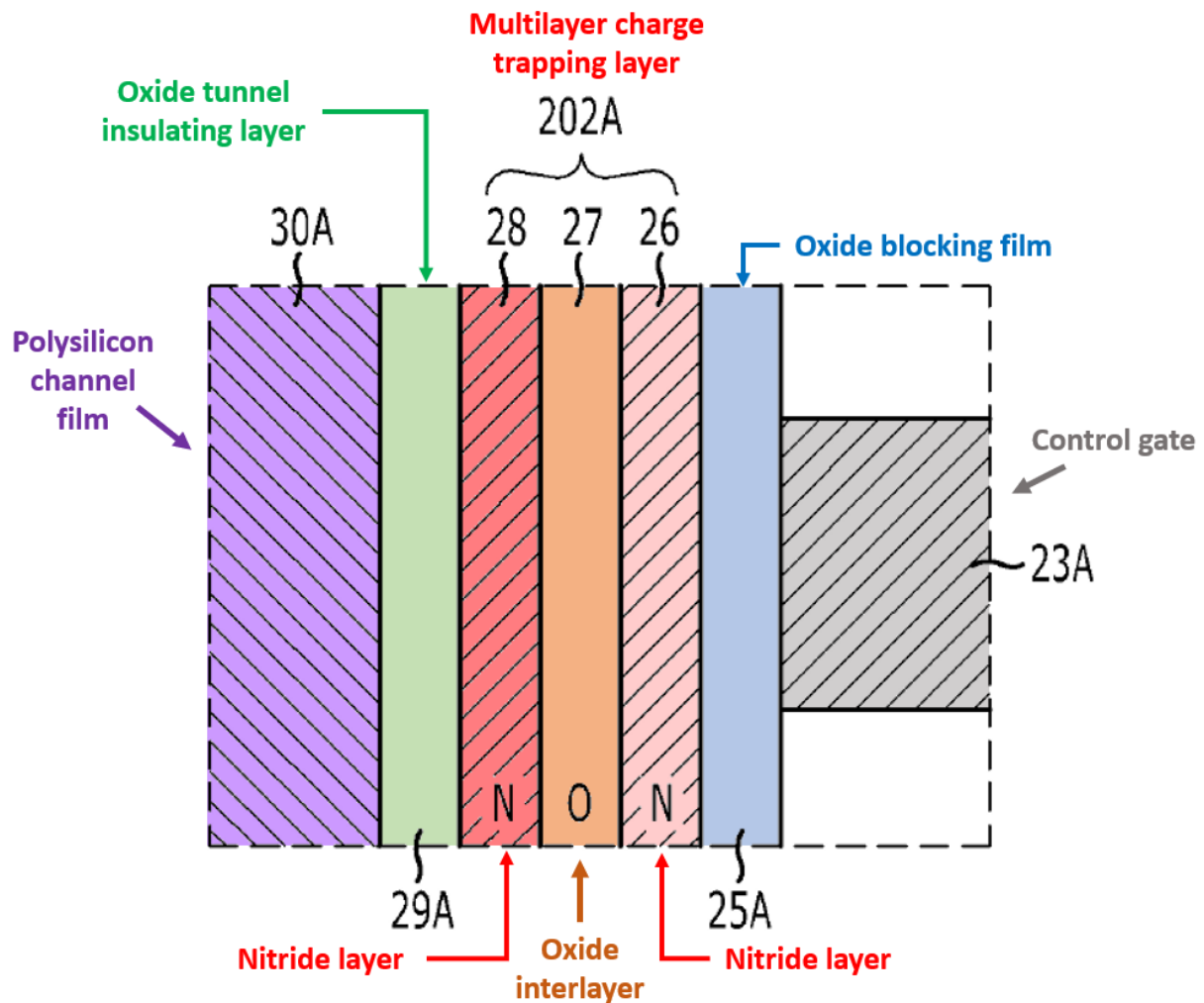
128. I understand that Lee '961 was not cited or considered during prosecution of the '365 patent.

129. Lee '961 teaches a 3D charge trap memory device with a stack of layers (201) formed over a substrate (21) as shown in annotated figure 2a below. The stack including alternating insulating layers (22A) and gate electrodes (23A):



Ex. 1005 (Lee '961), Fig. 2a, [0017]-[0019].

130. As reflected above, Lee '961 teaches a vertical 3D structure where a polysilicon channel is surrounded by a tunnel insulating layer 29A (silicon oxide), multilayered charge trap layer 202A, and blocking film 25A (silicon oxide). Ex. 1005 (Lee '961), [0017]-[0019]. As shown in annotated figure 2b below, multilayer charge trap layer 202A includes nitride layer 28, oxide interlayer 27, and nitride layer 26:



Ex 1005 (Lee '961), Fig. 2b, [0020].

131. A POSITA would have understood that Lee '961 is analogous art to the '365 patent because it teaches improvements to non-volatile memory devices generally, and charge trap memory devices specifically.

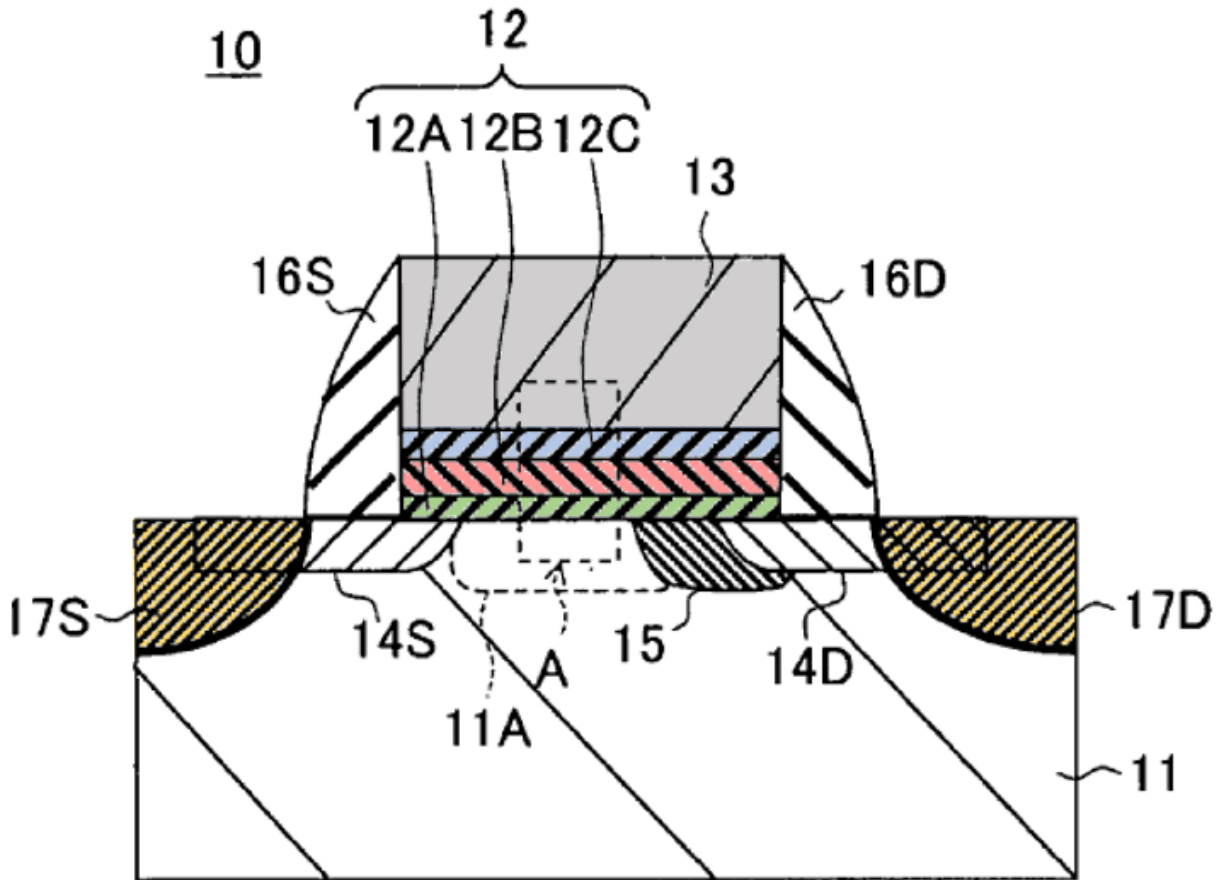
C. Fujiwara (Exhibit 1006)

132. Fujiwara (Exhibit 1006) is a copy of U.S. Patent Publication 2006/0065919 A1, entitled “Nonvolatile Memory Device and Method for Producing the Same.” Fujiwara was published on March 30, 2006 from an application filed on September 16, 2005. Fujiwara identifies a single inventor, Ichiro Fujiwara. I understand that Fujiwara is considered prior art to the challenged claims because it was published more than one year prior to July 1, 2012.

133. I understand that Applicants listed Fujiwara on an information disclosure statement submitted during the prosecution of the '365 patent, along with more than 300 other references Applicants listed on such statements. I understand that the Examiner did not cite or apply Fujiwara in any Office Action, nor provide any substantive analysis of Fujiwara in allowing the claims of the '365 patent. *See* Part III.C.

134. Fujiwara teaches a charge-trapping memory transistor with multiple nitride layers that provide improved data retention characteristics. Ex. 1006 (Fujiwara), [0037]-[0038], [0197], [0220].

135. For example, in figures 2, 21, and 22, Fujiwara teaches a memory transistor with: (i) semiconductor substrate 11 with source 17S and drain 17D; (ii) first/bottom silicon oxide film 12A; (iii) silicon nitride charge storage layer 12B; (iv) second/top silicon oxide film 12C; and (v) gate 13.

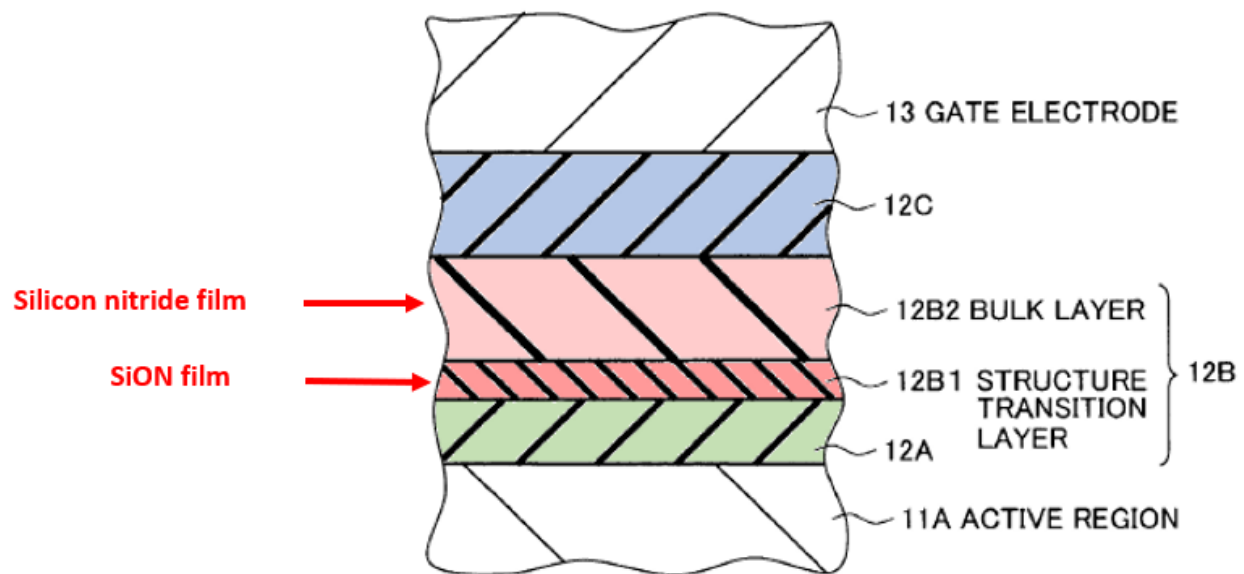


Ex. 1006 (Fujiwara), Fig. 2, [0072]-[0084], [0146]-[0154].

136. In figure 21, Fujiwara teaches that the silicon nitride charge storage layer 12B can be made of two nitride layers – a lower silicon oxynitride (SiON) “transition” layer 12B1 and upper silicon nitride (SiN_x) “bulk” layer 12B2, where

the SiON transition layer 12B1 is provided to: (i) improve the film quality of layer 12B; and (ii) improve data retention characteristics.

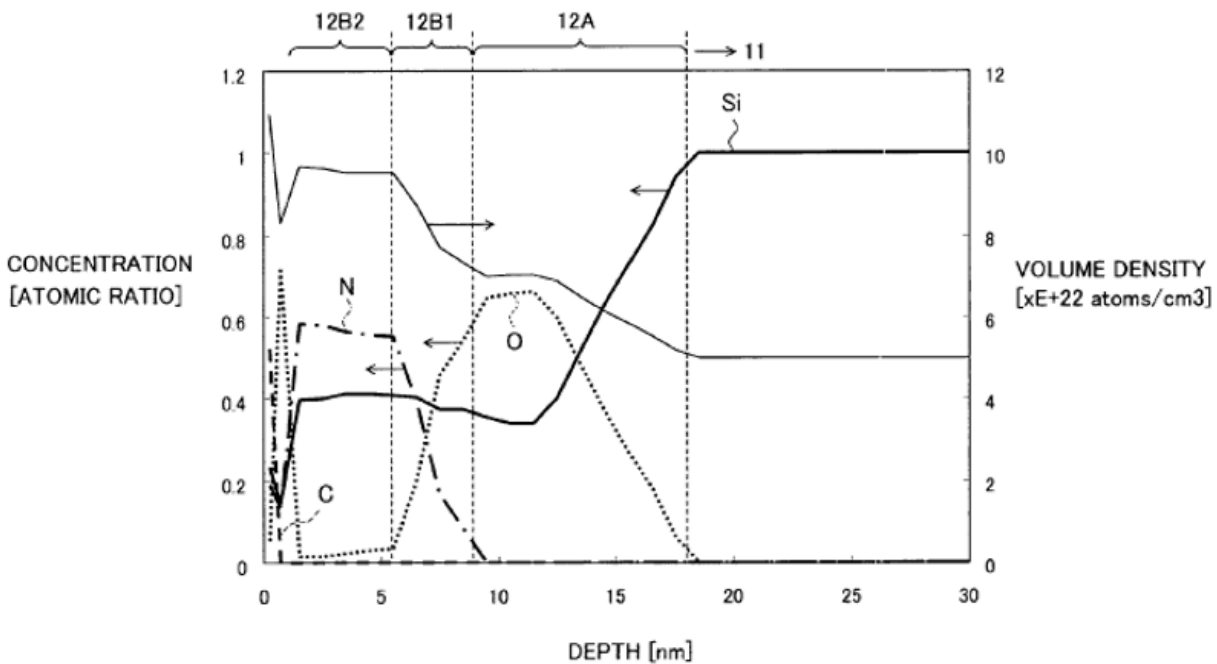
FIG. 21



Ex.1006 (Fujiwara), Fig. 21, [0197]-[0208].

137. Figure 22 of Fujiwara teaches the relative oxygen (O), nitrogen (N), and silicon (Si) concentrations in each layer. Figure 22 teaches that layer 12B2 is silicon-rich (e.g., ~40% concentration through its thickness) and oxygen lean (e.g., less than about 5% throughout its thickness). Figure 22 further teaches that layer 12B1 is oxygen-rich, with atomic concentrations reaching about 50%.

FIG. 22



Ex. 1006 (Fujiwara), Fig. 22, [0200].

138. A POSITA would have understood that Fujiwara is analogous art to the '365 patent because it teaches improvements to non-volatile memory devices generally, and charge trap memory devices specifically.

IX. ANALYSIS OF INVALIDITY GROUNDS

139. Based on my review and analysis of the materials cited herein, my opinions regarding the understanding of a POSITA before July 1, 2012, and my training and experience, it is my opinion that the challenged claims of the '365 patent are invalid based on the following grounds:

Ground	Claims	Basis	Prior Art
1	1-3, 5, 9-12, 14-23, 28-33, 35-37, and 42-45	§ 103 Obviousness	Lee '255, Lee '961
2	6-8, 25-27, 34, 38-41	§ 103 Obviousness	Lee '255, Lee '961, Fujiwara

A. Ground 1: Obviousness over Lee '255 and Lee '961

140. It is my opinion that claims 1-3, 5, 9-12, 14-23, 28-33, 35-37, and 42-45 of the '365 patent are rendered obvious based on the teachings of Lee '255 and Lee '961.

141. Lee '255 teaches a 3D vertical SONOS charge trap-type nonvolatile memory device. Ex. 1004 (Lee '255), Figs. 4A, 4B, [0003]. As discussed below, Lee '255 teaches most of the limitations of the challenged claims, including, (i) a substrate with a stack of alternating dielectric and gate layers thereon; (ii) a vertical pipe-shaped (annular) channel passing through the layers perpendicular to the substrate; (iii) an ONO stack around and along the vertical channel that includes a tunneling oxide layer, a nitride charge trapping layer, and a blocking oxide layer; and (iv) a series of gate electrodes around the ONO stack forming a vertical array of individual memory transistors. *See id.*, [0050]-[0063].

142. Lee '961 also teaches a 3D vertical SONOS charge trap-type nonvolatile memory device. Ex. 1005 (Lee '961), [0002]-[0006]. Lee '961 teaches

that prior art 3D memory devices similar to the device taught in Lee '255 can suffer from leakage of charges. *Id.*, Fig. 1, [0006]. To provide improved data retention properties, Lee '961 teaches modifying prior art devices to include a SONOS configuration with a “multilayered charge trap layer”—“[t]he present invention described above has the effect of improving data retention properties of non-volatile memory devices by applying a multilayered charge trap layer comprising a plurality of trap layers and interlayers.” Ex. 1005 (Lee '961), [0010]; *see also id.*, [0012], [0015], [0017], [0020].

143. It is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 1-3, 5, 9-12, 14-23, 28-33, 35-37, and 42-45 of the '365 patent. As discussed below, a POSITA would have been motivated to modify the nitride charge trapping layer of Lee '255 to incorporate the “multilayered charge trap layer” configuration disclosed in Lee '961 to achieve the performance benefits that Lee '961 expressly attributes to that structure—namely, improved data retention and suppression of charge spreading. The motivation to combine these references is clear from their shared focus on vertical charge-trap memory architectures and their use of compatible materials and fabrication techniques. A POSITA also would have expected success in implementing the multilayer charge-trap structure of Lee '961 in the stack of Lee '255 because this combination could be accomplished with routine process

modifications, using well-established deposition tools and parameters. I provide further details on this motivation and expectation of success in connection with specific claim limitations below.

144. The combination of Lee '255 and Lee '961 presents a materially different teaching from the prior art considered during prosecution of the '365 patent. Based on my review of the file history, I understand that the Examiner allowed claims 1, 23, and 35 (application claims 2, 24, and 36), without rejection, based on his understanding that none of the prior art references of record disclosed an annularly-shaped multi-layer charge trapping region surrounding a vertical channel. Ex. 1002 (Pros. Hist.), 001877-78. However, as I explain in more detail below, the combination of Lee '255, which was not applied during prosecution, and Lee '961, which was neither of record nor applied during prosecution, clearly teaches the structural features that the Examiner found missing. Together, these references disclose a multilayer charge-trapping region arranged annularly around a vertical semiconductor channel, precisely as claimed in the '365 patent.

1. Ordering and grouping of claims

145. In performing my analysis, I have begun with independent device claim 35 and the claims that depend from claim 35 (claims 36, 37, 42-45) because I believe it is most efficient to address the device claims before addressing the independent method claims (claims 1 and 23).

146. For efficiency, I have also grouped claims together throughout my analysis where the claims have similar substantive requirements.

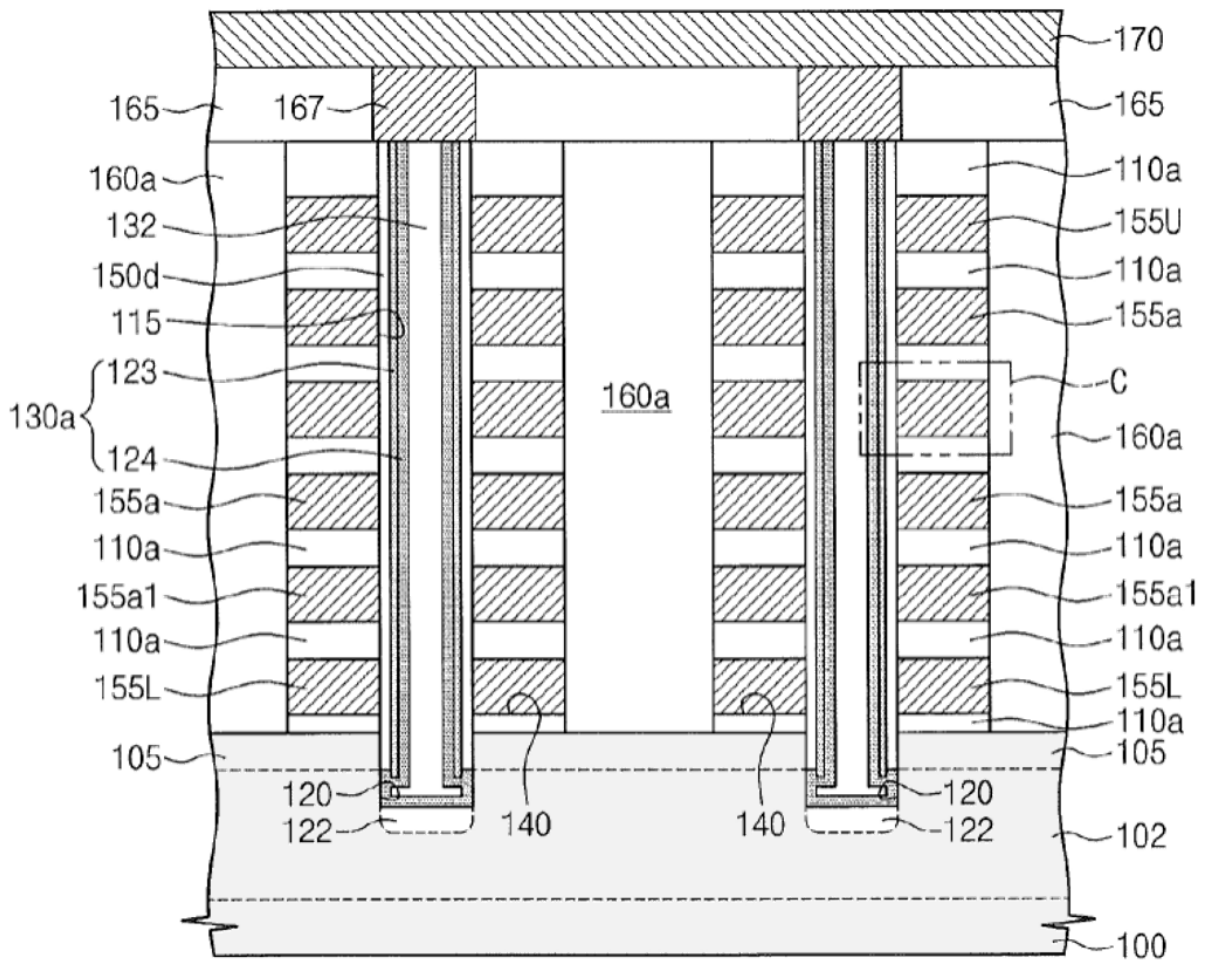
2. Independent Claim 35

[35pre] A semiconductor memory device, comprising:

147. I understand that a preamble does not always limit the claim. *See* Appendix 4. To the extent Patent Owner argues this preamble is limiting, it is my opinion that Lee '255 teaches *a semiconductor memory device* because Lee '255 teaches “a three-dimensional (3D) semiconductor memory device and a method of fabricating the same.” *See, e.g.*, Ex. 1004 (Lee '255), [0002]; *see also, e.g., id.*, Abstract, Figs. 1A-5B, [0074] (teaching “3D semiconductor memory device”).

[35a] a semiconductor substrate,

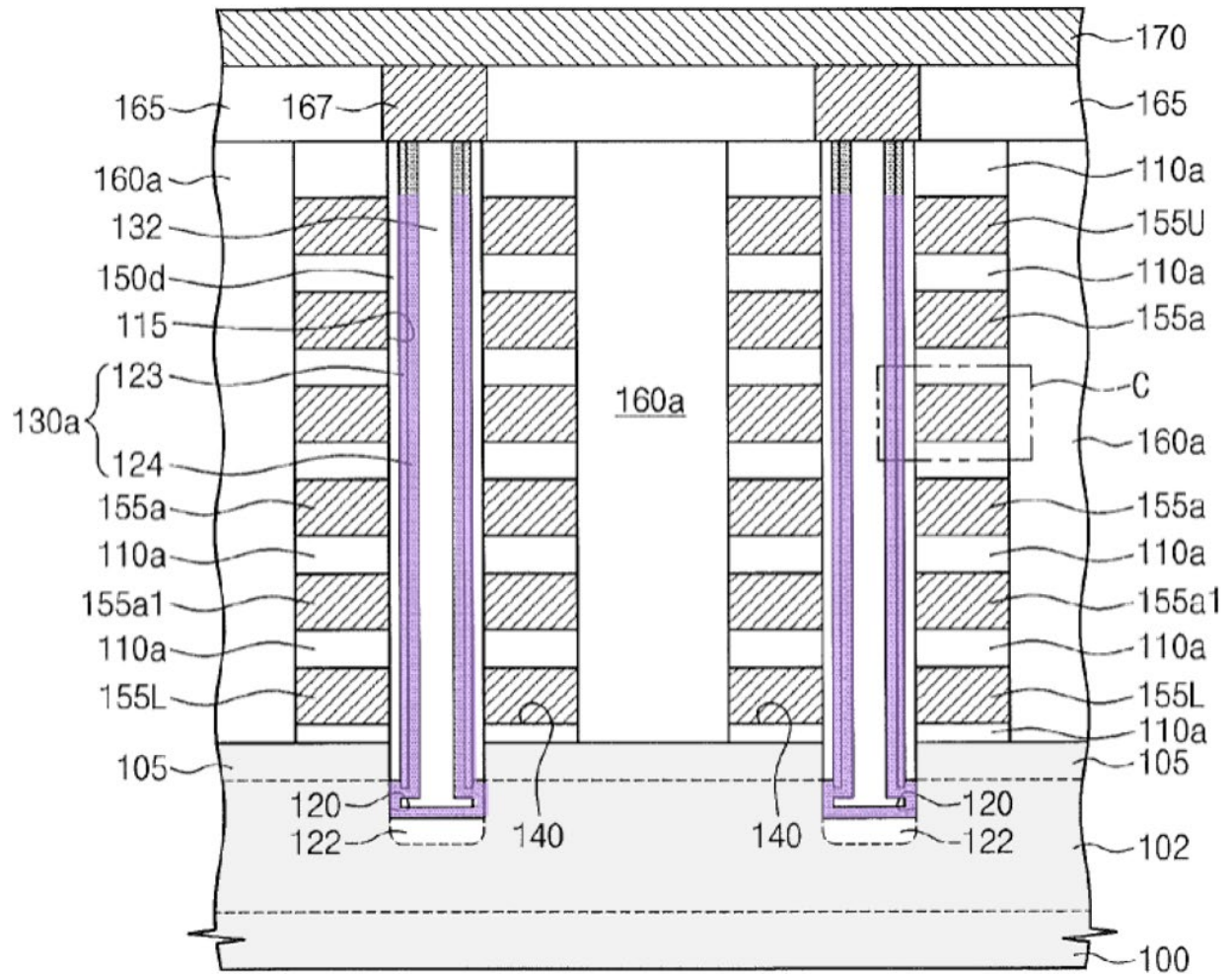
148. It is my opinion that Lee '255 teaches limitation [35a] because it teaches forming 3D memory devices on “a semiconductor substrate 100” made of, for example, silicon. Ex. 1004 (Lee '255), [0050]; *see also id.*, [0005], [0009]. Lee '255 provides an example of its *semiconductor substrate* in figure 4A, which I have annotated here, showing substrate 100 in light gray:



Ex. 1004 (Lee '255), Fig. 4A, [0050], [0074].

[35b] a channel region oriented substantially perpendicular to the semiconductor substrate, the channel region formed in a substantially annular shape,

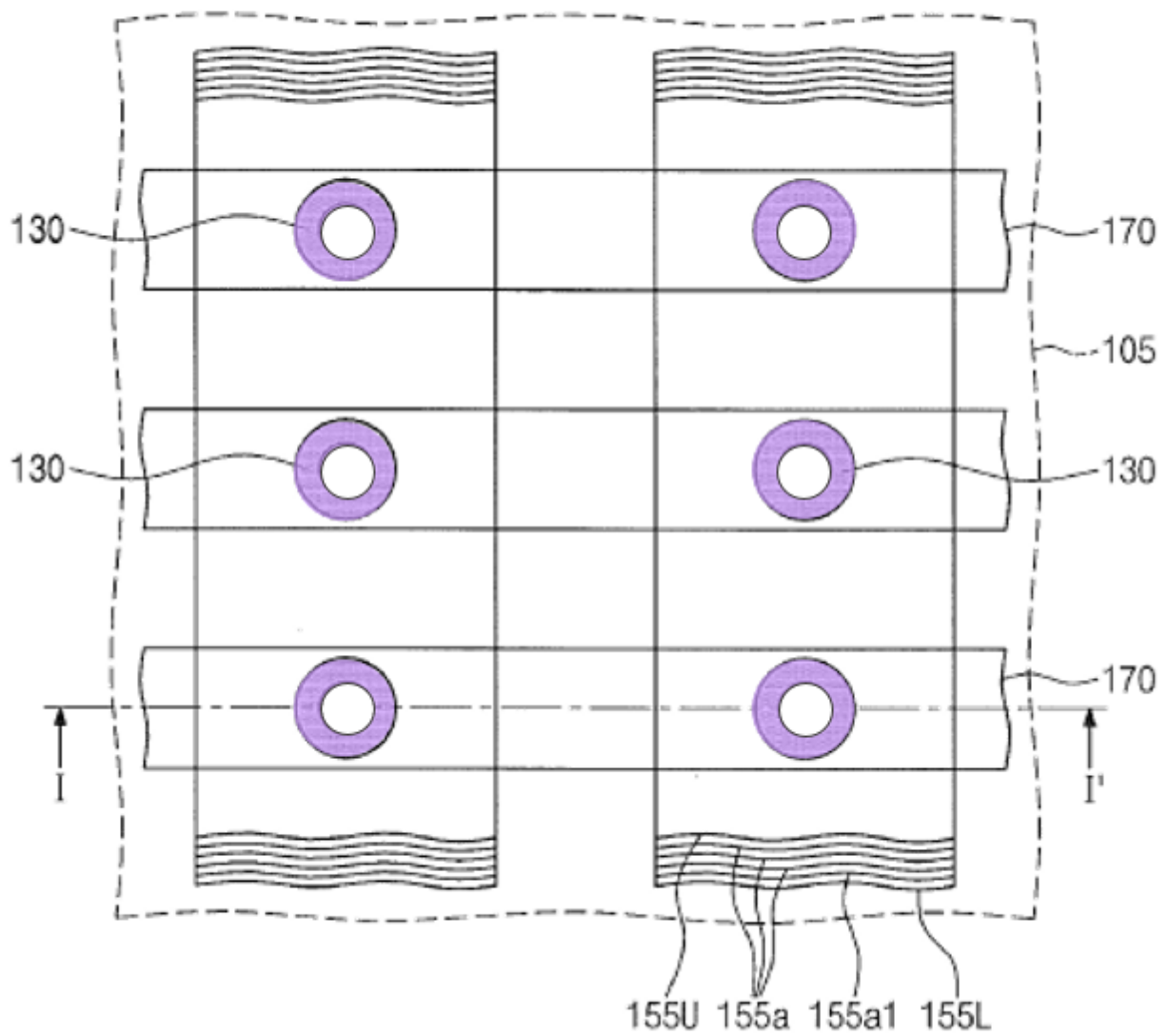
149. It is my opinion that Lee '255 teaches limitation [35b] because it teaches “vertical channel regions that are defined in the sidewall of vertical active pattern” 130/130a. Ex. 1004 (Lee '255), [0059], [0058]. As shown in figure 4A, Lee teaches that the “vertical active pattern” 130/130a (the *channel region*) is *oriented substantially perpendicular to the semiconductor substrate* (substrate 100):

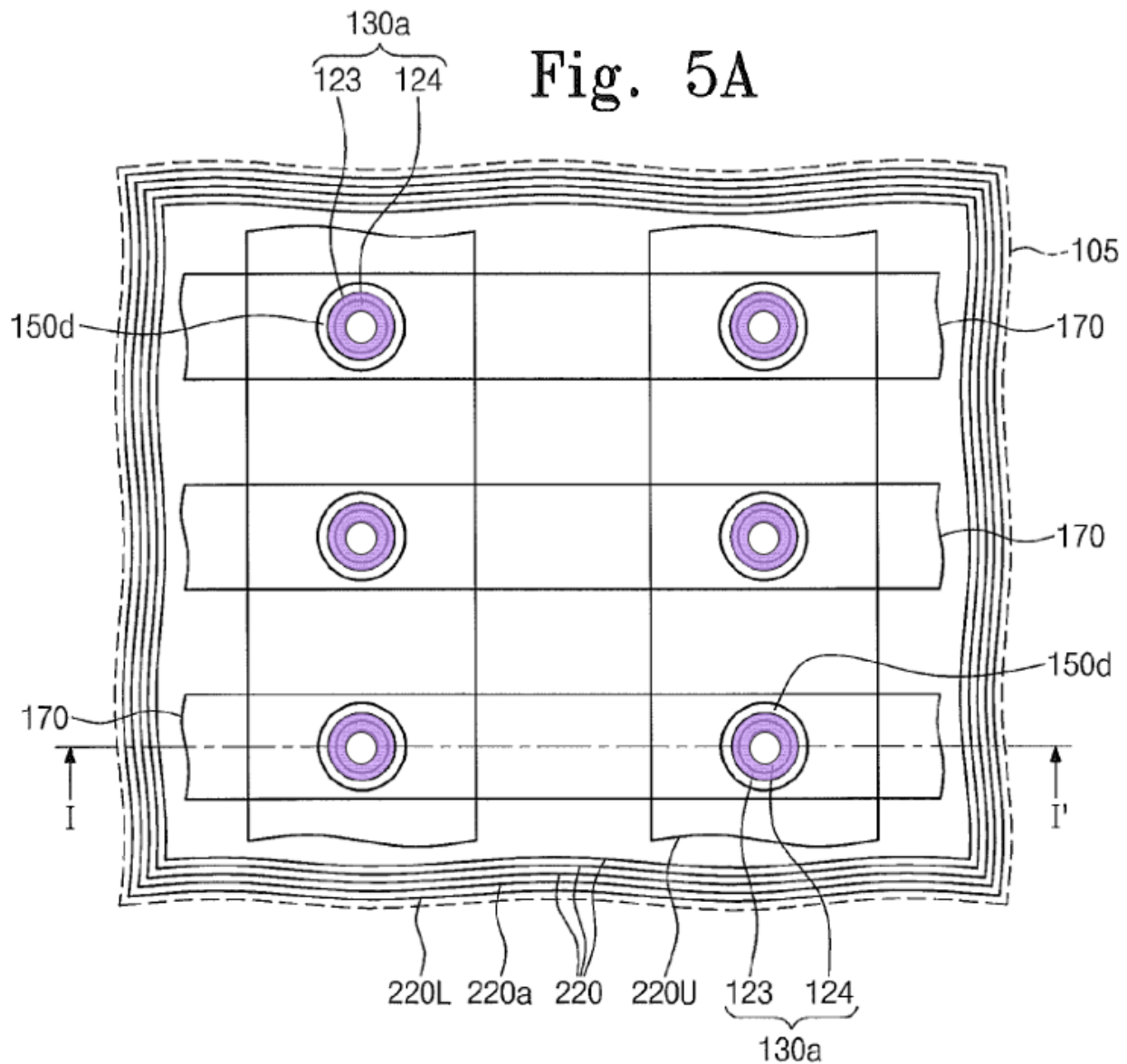


Ex. 1004 (Lee '255), Fig. 4A; *see also id.*, [0052].

150. Lee '255 further teaches that the vertical active pattern 130/130a (the *channel region*) is *formed in a substantially annular shape* because the vertical active pattern 130/130a may have “a hollow pipe shape.” Ex. 1004 (Lee '255), [0054]. This *annular shape* is depicted, for example, in Figures 1A and 5A:

Fig. 1A





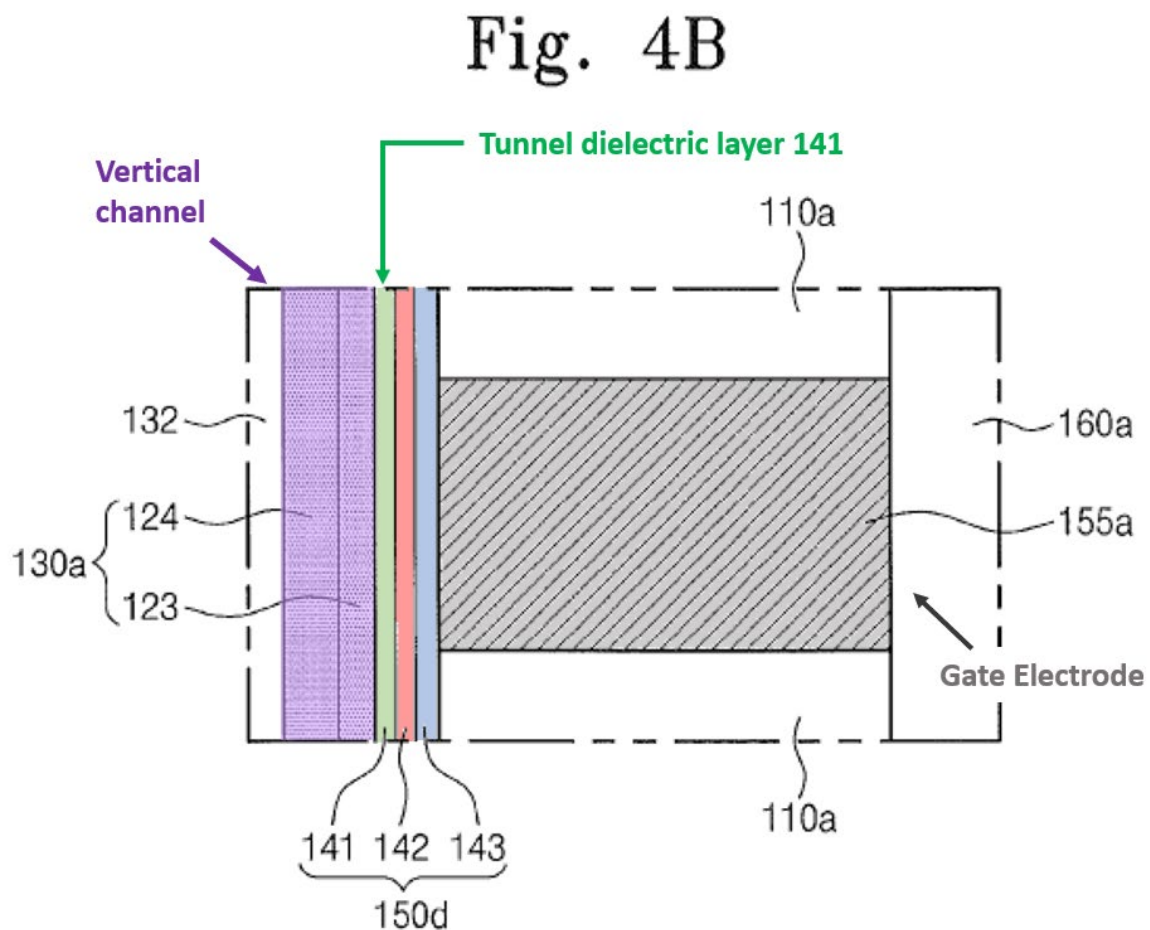
Ex. 1004 (Lee '255), Figs. 1A, 5A, [0054]; *see also id.*, [0074] (“FIG. 4A is a cross-sectional view taken along line I-I’ of FIG. 1A.”).

[35c] a tunnel dielectric layer surrounding the channel region, the tunnel dielectric layer formed in a substantially annular shape,

151. It is my opinion that Lee '255 teaches limitation [35c] because it teaches a “gate dielectric layer 150d” disposed around and along the vertical active

pattern 130/130a (the *channel region*) that includes “tunnel dielectric layer 141.”

Ex. 1004 (Lee '255), Fig. 4A/B, [0055]-[0057]. I have annotated the *tunnel dielectric layer* (“tunnel dielectric layer 141”) in green the following version of Lee '255's figure 4B:

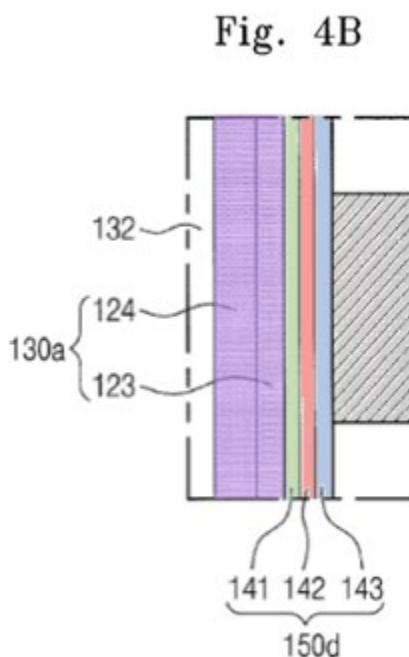
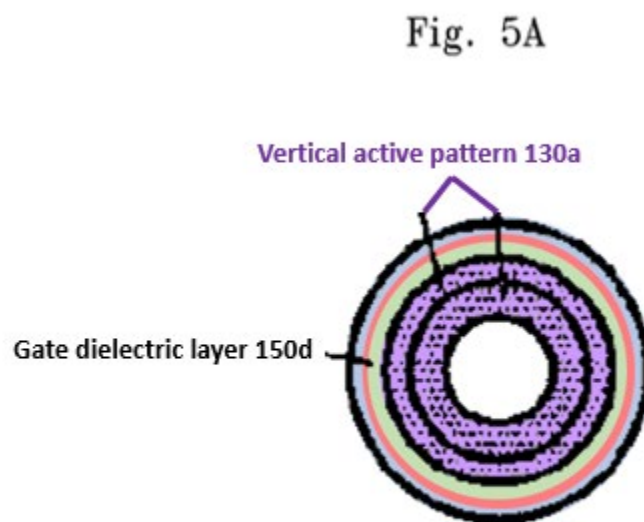


Ex. 1004 (Lee '255), Figs. 4B.

152. Lee '255 further teaches that the tunnel dielectric layer is *formed in a substantially annular shape and surrounding the channel region*. As discussed above, Lee '255 teaches that the vertical active pattern (the *channel region*) may be

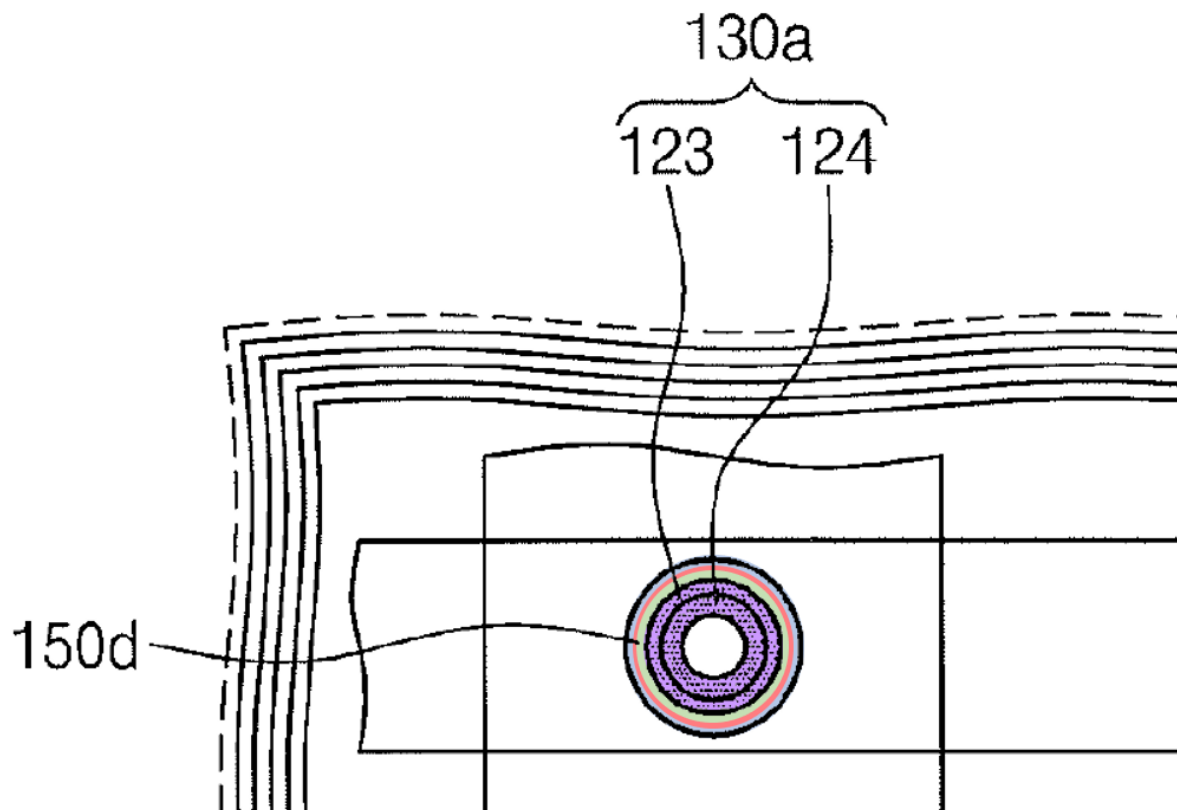
formed in the shape of a pipe (i.e., *annularly*). Lee '255 further teaches that gate dielectric layer 150d, which includes tunnel dielectric layer 141 (see above), is “disposed between” the vertical active pattern and “each of the gate patterns.” Ex. 1004 (Lee '255), [0055].

153. Lee '255 teaches the relative positioning of the channel and dielectric layers in figure 4B, while the shape of the layers is taught in figure 5A. I have excerpted and annotated those figures here, adding the layers of dielectric gate layer 150d shown in figure 4B to figure 5A, which shows that dielectric gate layer 150d, but does not include details on the individual sub-layers of the dielectric gate layer:



Ex. 1004 (Lee '255), Figs. 4B, 5A (excerpted and annotated).⁴

154. As shown in the below annotated excerpt from figure 5A of Lee '255, this results in gate dielectric layer 150d, including the tunnel dielectric layer 141 (green), forming an annular shape that surrounds the channel region (130a) (purple):



⁴ A POSITA would have understood that showing the annular shape of gate dielectric layer 150d with further details concerning the individual sub-layers of gate dielectric layer 150d in a separate figure was common. For example, the '365 patent uses a similar disclosure concerning the shape of the layers in figure 8A with further details on the composition of the layers in figure 8B. *See* Ex. 1001 ('365 patent), Figs. 8A, 8B.

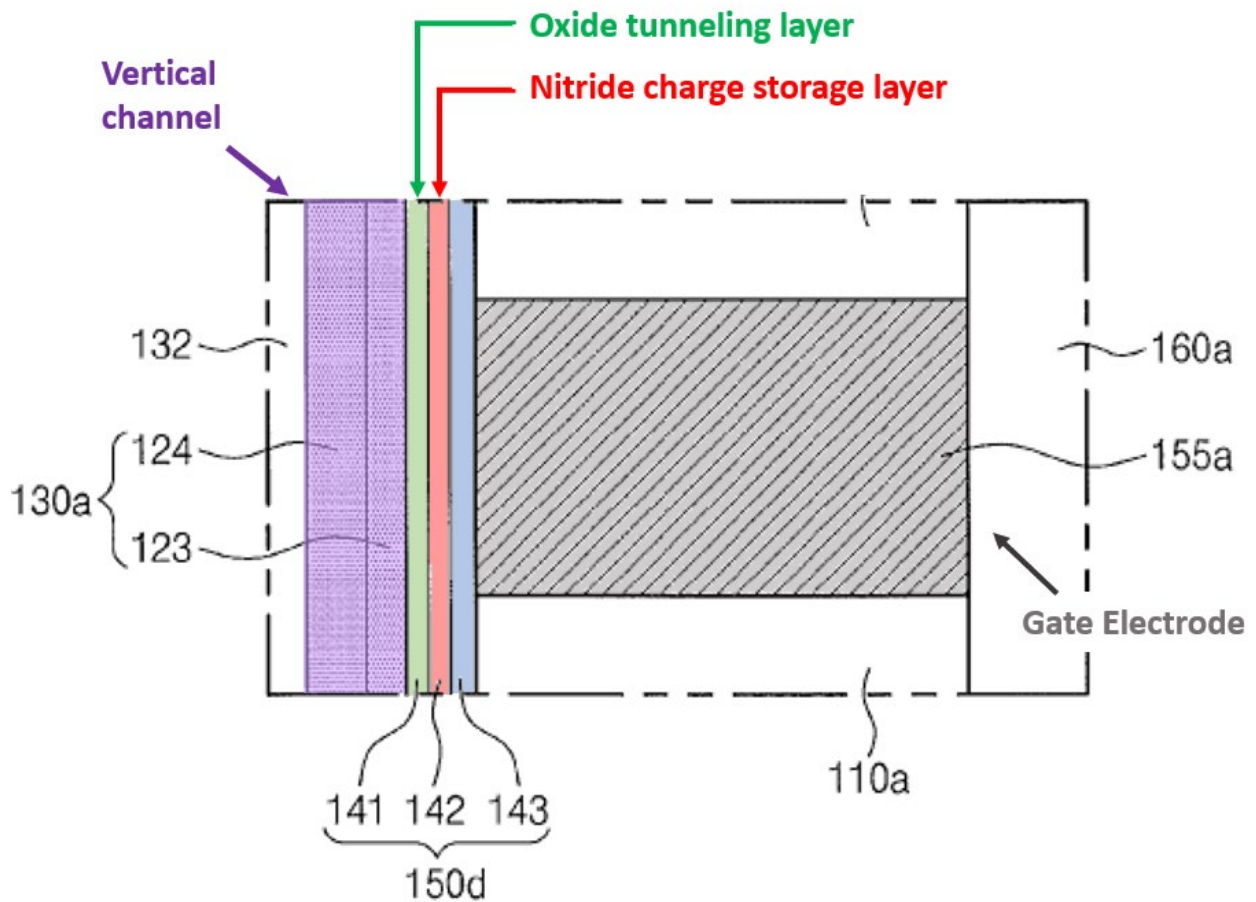
Ex. 1004 (Lee '255), Fig. 5A; *see also id.*, [0055]-[0057], [0074]-[0075].

[35d] a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape,

155. It is my opinion that the combination of Lee '255 and Lee '961 teaches limitation [35d]. As discussed below, Lee '255 teaches a *charge storing region surrounding the tunnel dielectric layer, the . . . charge storing region formed in a substantially annular shape*. Lee '961 teaches a *multi-layer charge storage region* to improve the operation of memory devices such as those taught in Lee '255. A POSITA would have been motivated to modify the charge storing region of Lee '255 based on Lee '961's teachings regarding a multi-layer charge storing region.

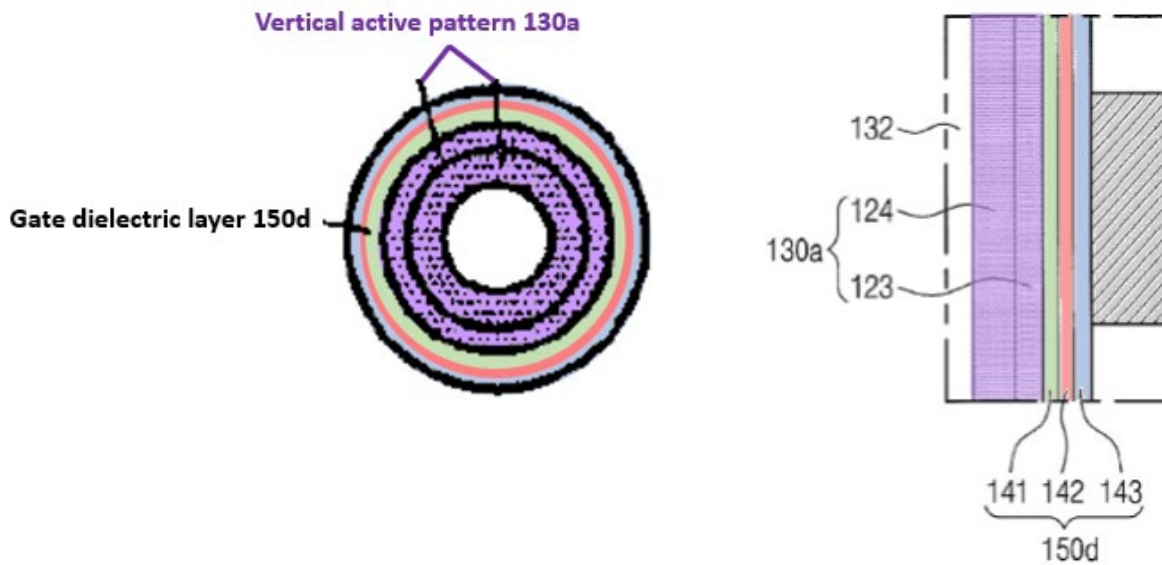
156. Lee '255 teaches a *charge storage region* because Lee '255 teaches that the gate dielectric layer 150d includes a nitride "charge storage layer 142." Ex. 1004 (Lee '255), Fig. 4B, [0055]-[0057]. This nitride charge storage layer 142 is depicted in figure 4B, which I have annotated here:

Fig. 4B



Ex. 1004 (Lee '255), Figs. 4B, *see also id.*, [0055]-[0057], [0074]-[0075].

157. Lee '255 further teaches that nitride charge storage layer 142 is *formed in a substantially annular shape that is surrounding the tunnel dielectric layer*. As I explained above (*see limitation [35c]*), Lee '255 teaches that the gate dielectric layer 150d is formed in an *annular shape* surrounding the channel region:



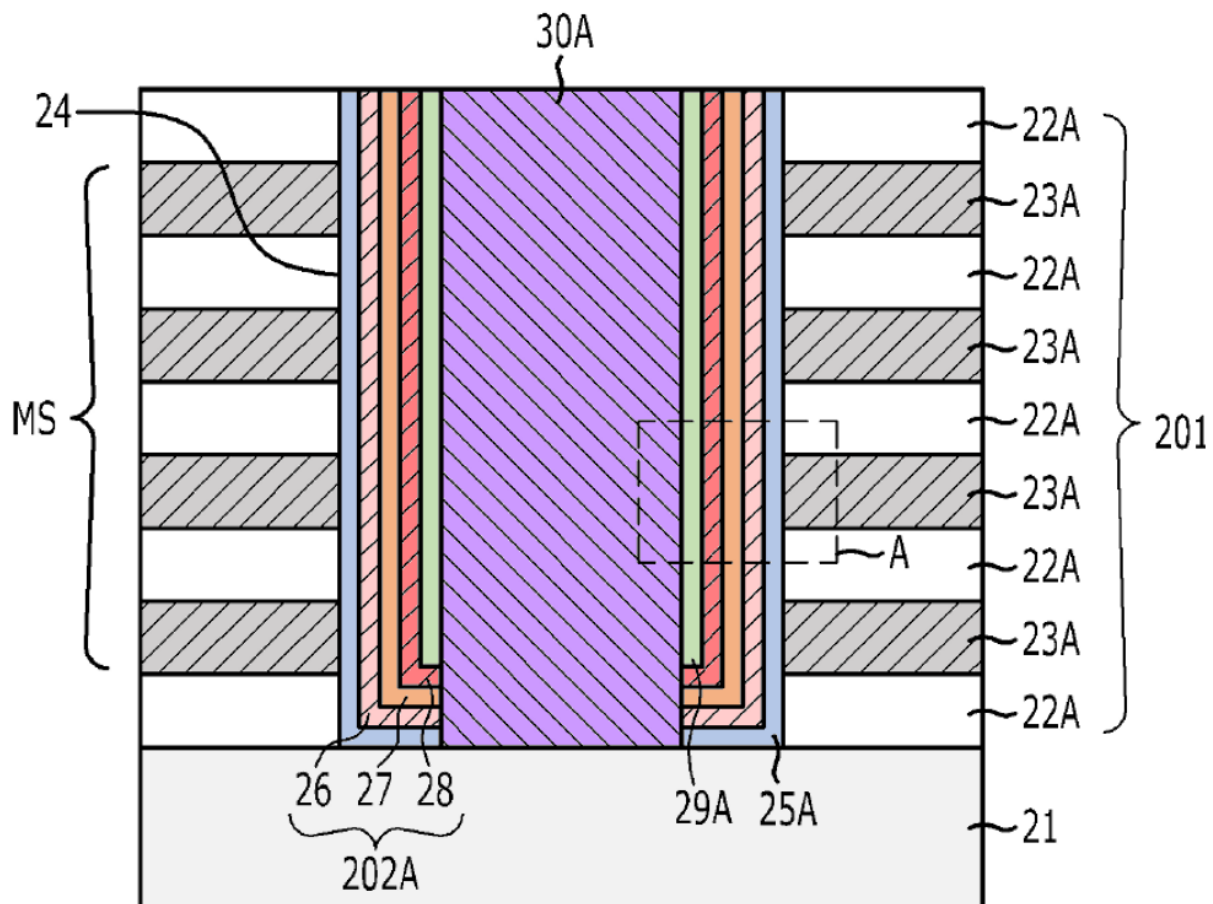
Ex. 1004 (Lee '255), Figs. 4B, 5A (excerpted and annotated).

158. I added the sub-layers of dielectric gate layer 150d to the excerpt from figure 5A based on the teachings of figure 4B, which shows the relative positions of the sub-layers to the vertical channel. As depicted above, the gate dielectric layer has three sub-layers that a POSITA would have understood to form concentric circles—tunnel dielectric layer 141 (green), surrounded by charge storage layer 142 (red), surrounded by blocking dielectric layer 143 (blue). Thus, a POSITA would have understood that Lee '255 teaches a *substantially annular* charge storing region (charge storage layer 142) *surrounding the tunnel dielectric layer* (tunneling oxide layer 141).

159. While figure 4B of Lee '255 depicts a “gate dielectric layer 150d” with three layers, Lee '255 teaches that the structure is compatible with additional

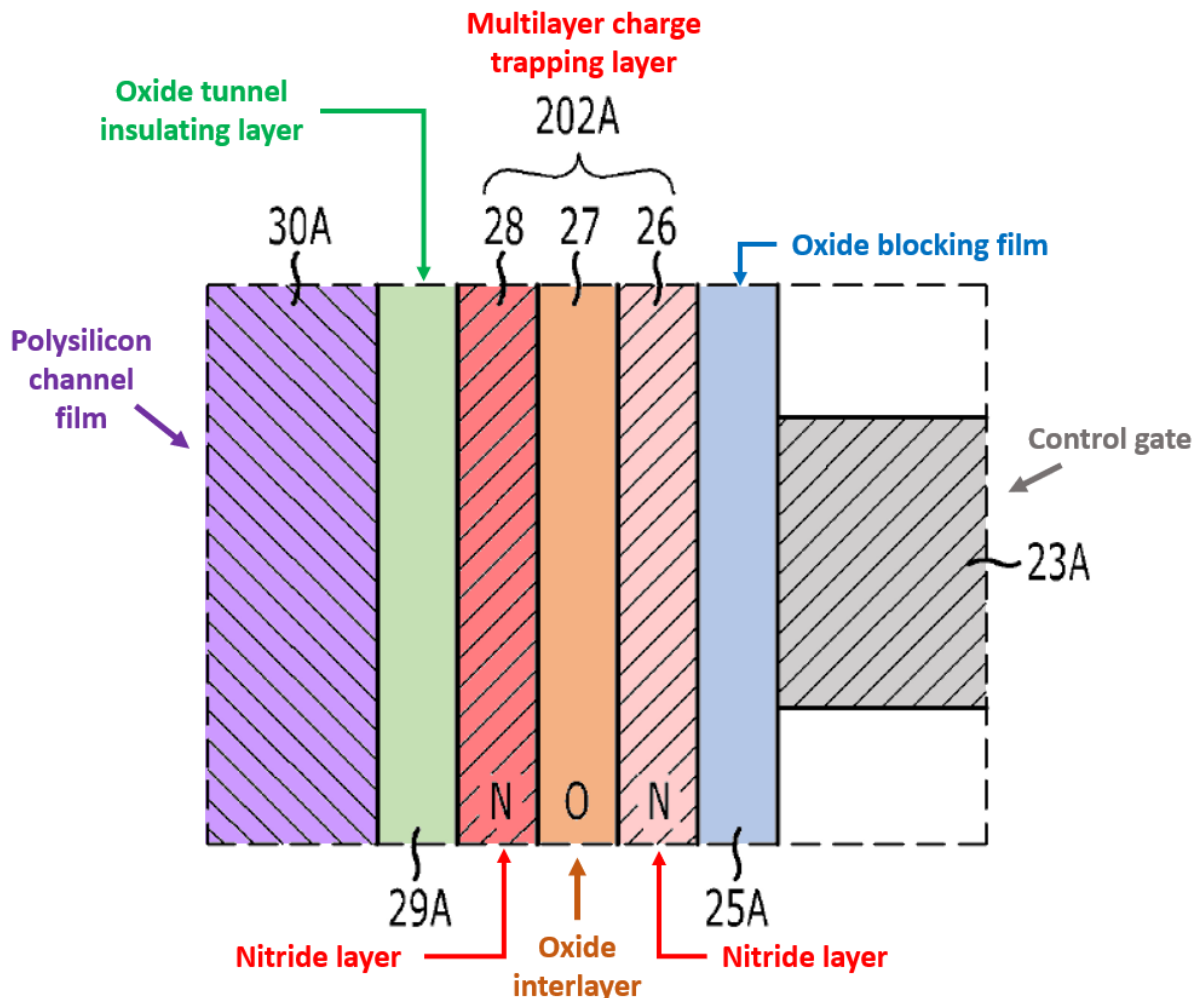
layers. For example, Lee '255 teaches incorporating additional oxide or oxynitride layers. Ex. 1004 (Lee '255), [0057].

160. Lee '961 teaches a “multilayered charge trap layer” 202A (*a multi-layer charge storing region*) that “improv[es] the data retention properties of non-volatile memory devices” such as the device of Lee '255. Ex. 1005 (Lee '961), [0008], [0010]. Figure 2a of Lee '961 depicts the vertical structure of the 3D memory device:



Ex. 1005 (Lee '961), FIG. 2a.

161. Lee '961's *multi-layer charge storing region* (multilayered charge trap layer 202A) is further depicted in figure 2b, which is a magnified view of box "A" from figure 2a:



Ex. 1005 (Lee '961), Figures 2b, [0013], [0018]-[0020].

162. Like Lee '255, Lee '961 teaches that the charge trapping region is positioned between a tunneling dielectric layer (green) and a blocking oxide layer (blue). Ex. 1005 (Lee '961), FIGS. 2a, 2b, [0017]-[0019]. Lee '961 teaches that "[t]he charge trap layer 202A has a multilayer structure" (*a multi-layer charge*

storing region). Ex. 1005 (Lee '961), [0020]. For example, the multilayer charge trap layer 202A may include a nitride first trap layer 26, an oxide interlayer 27, and a nitride second trap layer 28. Ex. 1005 (Lee '961), [0020]; *see also id.*, [0015].

163. A POSITA would have been motivated to modify Lee '255's charge trapping layer to incorporate a multilayer charge trapping region based on the teachings of Lee '961.

164. It would have been obvious for a POSITA to consult the teachings of Lee '961 in seeking to improve the memory transistor configuration of Lee '255 because both Lee '961 and Lee '255 are directed to improving the operation of SONOS-type charge trapping memory transistors. Indeed, Lee '255 mirrors the type of devices that Lee '961 seeks to improve. *Compare* Ex. 1004 (Lee '255), Fig. 4A *with* Ex. 1005 (Lee '961), Fig. 1.

165. A POSITA would also have been motivated to apply Lee '961's ONONO stack teachings to the ONO stack of Lee '255 based on the express teachings, suggestion, and motivation to combine found in Lee '961. Specifically, Lee '961 teaches that SONOS configurations such as Lee '255's suffered from poor charge retention due to lateral spreading of charges in the single silicon nitride trapping film. Ex. 1005 (Lee '961), [0004]-[0006]. Lee '961 teaches that a solution to this problem is the multilayered charge trap layer (202A), which improves data retention. Ex. 1005 (Lee '961), [0010] ("The present invention

described above has the effect of improving the data retention properties of non-volatile memory devices by applying a multilayered charge trap layer comprising a plurality of trap layers and interlayers.”).

166. The data retention benefits of using the multilayer charge trapping region of Lee '961 also would have been predictable to a POSITA prior to July 2012. As set forth above in Parts III.C.4-6, using multilayer charge trapping structures was already a conventional strategy for improving retention prior to July 2012. *See* Parts III.C.4-6, above; *see also, e.g.*, Ex. 1010 (Nomoto), [0035], [0044]-[0045], [0073]-[0088] (teaching that a multi-layer charge trap with two nitride layers having different compositions (CS1, CS2) provides improved retention); Ex. 1011 (Levy), [0025]-[0026] (a multi-layer charge trap with an oxygen-lean top nitride layer and oxygen-rich bottom nitride layer “decrease[s] the charge loss rate after programming and after erase”); Ex. 1012 (Heo), [0058]-[0068] (teaching that using a bottom oxidized nitride layer with a top nitride layer improves “the data retention properties and/or durability of the non-volatile memory device”); Ex. 1006 (Fujiwara), Fig. 21, [0197]-[0208] (explaining retention benefits of using two nitride charge trapping layers); Ex. 1009 (Kim '399), [0034], [0046]-[0047] (teaching that use of bottom silicon oxynitride layer and top silicon nitride layer suppresses charge loss); Ex. 1013 (Ganguly), [0020], [0048]-[0049] (teaching that having lower nitride layer with up to 50%

oxygen and an upper “silicon-rich silicon nitride” results in “increased retention”); Ex. 1017 (Lai ’676), [0015], [0068]-[0077] (teaching that an NON charge trapping region with an upper silicon nitride layer 16, middle oxide layer 15, and lower silicon oxynitride layer 14 improves retention); Ex. 1021 (Higuchi) [0007], [0133]-[0134], [0141]-[0142] (teaching that an NON charge trapping region with an upper silicon nitride layer 203, middle oxide layer 202d, and lower silicon oxynitride layer 203c improves retention); Ex. 1014 (Wang ’586), [0006], [0022], [0031]-[0032] (teaching multi-layer charge storage structures including a silicon oxynitride bottom and nitrated silicon oxynitride top (FIG. 5) or a silicon oxynitride bottom and nitride top (FIG. 6) provides improved retention); Ex. 1020 (Arreghini), 000003 (Fig. 3), 000006 (teaching benefits of multi-layer charge trapping region). As such, applying the multilayer charge trapping region of Lee ’961 to modify the charge trapping layer of Lee ’255 would have amounted to (i) combining prior art elements according to known methods to yield predictable results; and (ii) use of known techniques to improve a similar device in the same way.

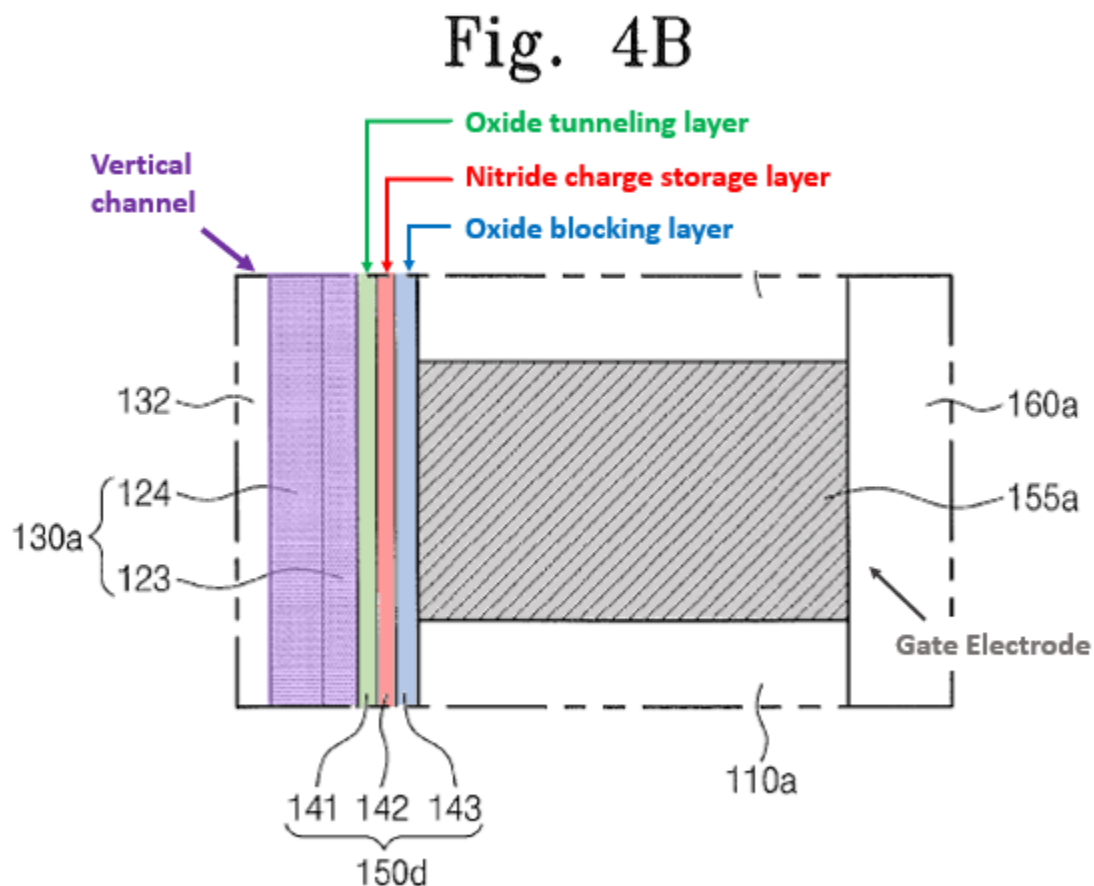
167. Applying the multilayer charge trap of Lee ’961 to the memory device of Lee ’255 also would have been obvious to try prior to July 2012. The selection of various trap configurations (e.g., ONO, ONNO, or ONONO) were routine design choices. *See* Part III.A.3-6. These alternatives represented a finite number

of predictable options available to a POSITA to optimize charge trap memory devices.

168. A POSITA would have also had a reasonable expectation of success in modifying the memory device of Lee '255 based on the teachings of Lee '961 to incorporate a multilayer charge trapping region. Both Lee '255 and Lee '961 are directed to very similar 3D charge trap memory devices with common features: vertical channels, stacks of insulating and gate layers, tunneling oxides, charge trap layers, and blocking oxides, and annular configuration. The memory structures in both references use similar materials and layouts, and address similar technical challenges. As I noted above, Lee '961 expressly aims to improve the type of memory architecture used in Lee '255 by introducing a multilayer charge trap structure. Ex. 1005 (Lee '961), Fig. 1, [0002]-[0010]. Applying Lee '961's teachings of a multilayer charge trapping region to the structure of Lee '255 would have amounted to depositing additional layers as part of the fabrication process. This is an alternative that Lee '255 already contemplates. *See* Ex. 1004 (Lee '255), [0057]. Moreover, a POSITA would have understood that applying the teachings of Lee '961 to Lee '255 would involve using established techniques for material selection, layer formation, and stack integration that were routine and well-known to a POSITA prior to July 2012.

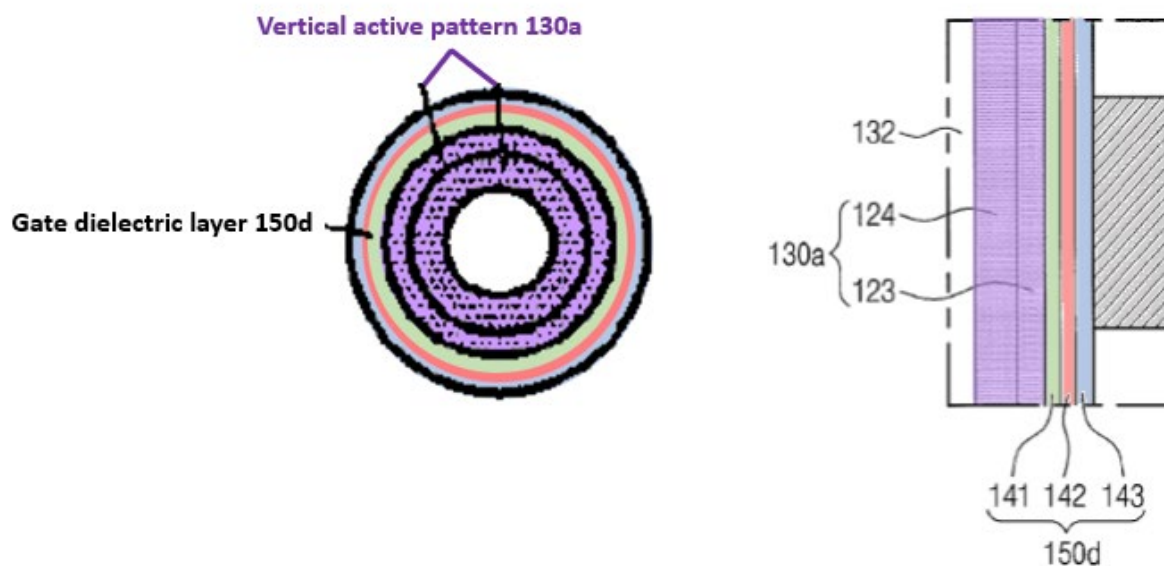
[35e] a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and

169. It is my opinion that Lee '255 teaches limitation [35e] because it teaches that the “gate dielectric layer 150d” includes an oxide “blocking dielectric layer 143” (*a blocking dielectric layer*). Ex. 1004 (Lee '255), Fig. 4B, [0055]-[0057]. The relative position of the blocking dielectric layer 143 (blue), is shown in this annotated version of figure 4B:



Ex. 1004 (Lee '255), Fig. 4B.

170. Lee '255 further teaches that blocking dielectric layer 143 (*blocking dielectric layer*) is *formed in a substantially annular shape* and positioned so that it is *surrounding the . . . charge storing region*. As I explained above (see limitations [35c], [35d]), Lee '255 teaches that the gate dielectric layer 150d, including the blocking dielectric layer, is formed in an *annular shape* surrounding the channel region. Lee '255 teaches the relative positioning of the channel and dielectric layers in figure 4B, while the shape of the layers is taught in figure 5A. I have excerpted and annotated those figures again here:



Ex. 1004 (Lee '255), Figs. 4B, 5A (excerpted and annotated); *see also id.*, [0055]-[0057].

171. As shown above, a POSITA would have understood that Lee '255 teaches a *substantially annular blocking dielectric layer* (blocking dielectric layer

143) that is positioned *surrounding the . . . charge storing region* (charge storage layer 142).

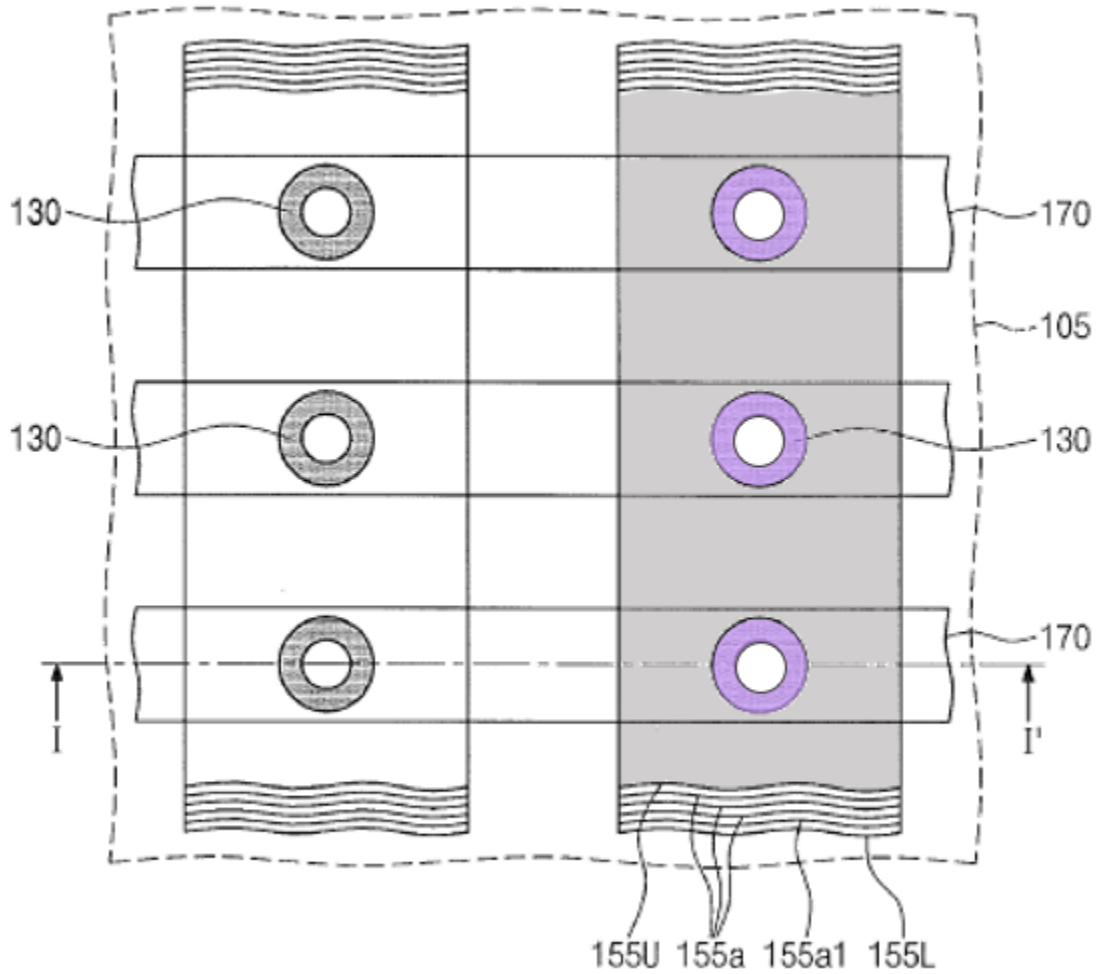
172. As I explained in connection with limitation [35d], above, a POSITA would have been motivated to modify the single-layer charge storage region of Lee '255 based on Lee '961's teachings regarding a multilayer charge storage region. The resulting multilayer charge storage region would maintain its position between the tunneling layer and blocking dielectric layer in the combination of Lee '255 and Lee '961. This placement of the charge trapping layer is taught in both Lee '255 (*see* Ex. 1004 (Lee '255), FIG. 4B) and Lee '961 (*see* Ex. 1005 (Lee '961), FIG. 2b).

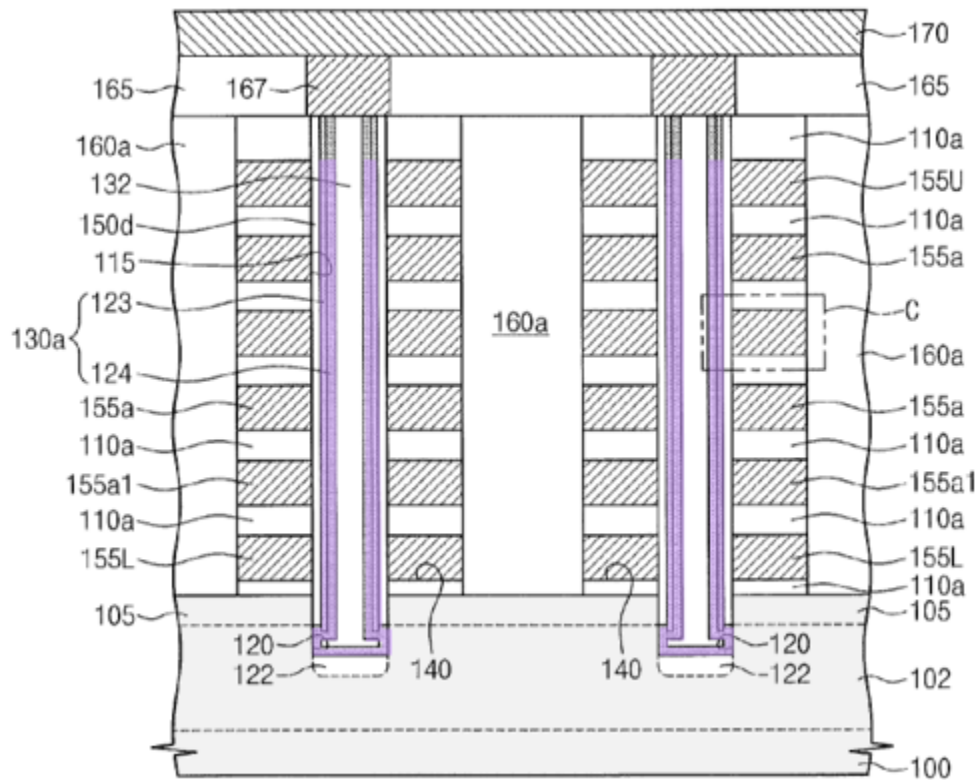
[35f] a gate electrode surrounding the blocking dielectric layer.

173. It is my opinion that Lee '255 teaches limitation [35f] because it teaches gate electrodes 155a (each *a gate electrode*) that are positioned *surrounding* oxide blocking dielectric layer 143 (*the blocking dielectric layer*). Ex. 1004 (Lee '255), Figs. 1A, 4A, 4B, and 5A, [0055]-[0062].

174. Lee '255 teaches that the 3D memory device is comprised of a “stack-structure, including insulation patterns 110a and gate patterns 155L, 155a1, 155a, and 155U that are stacked alternately and repeatedly.” Ex. 1004 (Lee '255), [0051]. “A plurality of vertical active patterns 130”—i.e., vertical *channel regions*—“may pass through each of the stack-structures.” *Id.*, [0061]. This is

shown, for example, in figures 1A (plan view) and 4A (cross section of figure 1A along axis I – I’):

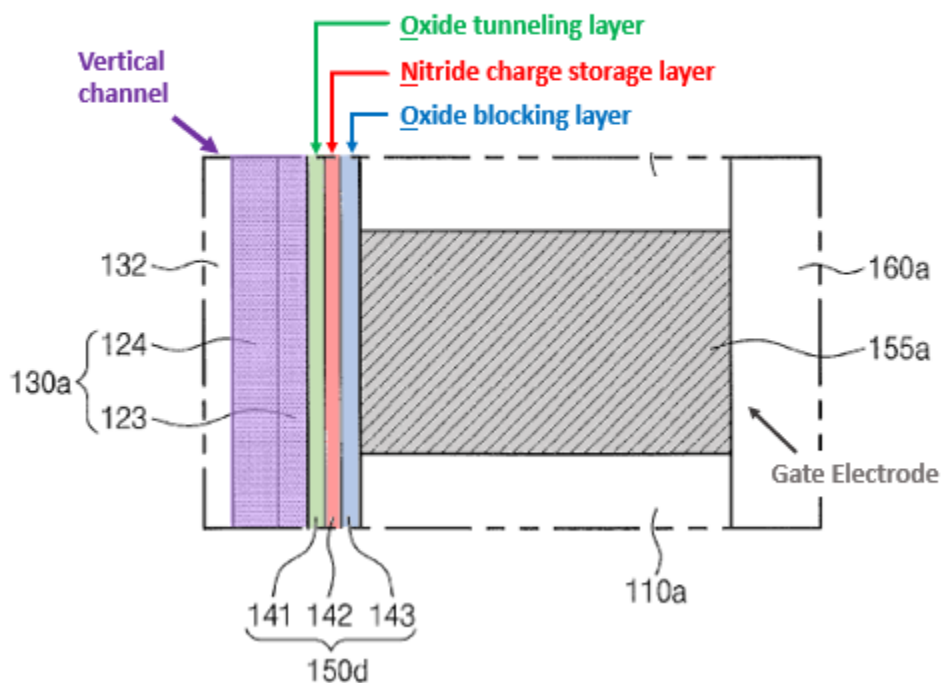




Ex. 1005 (Lee '255), Figs. 1A, 4A, [0051], [0061].

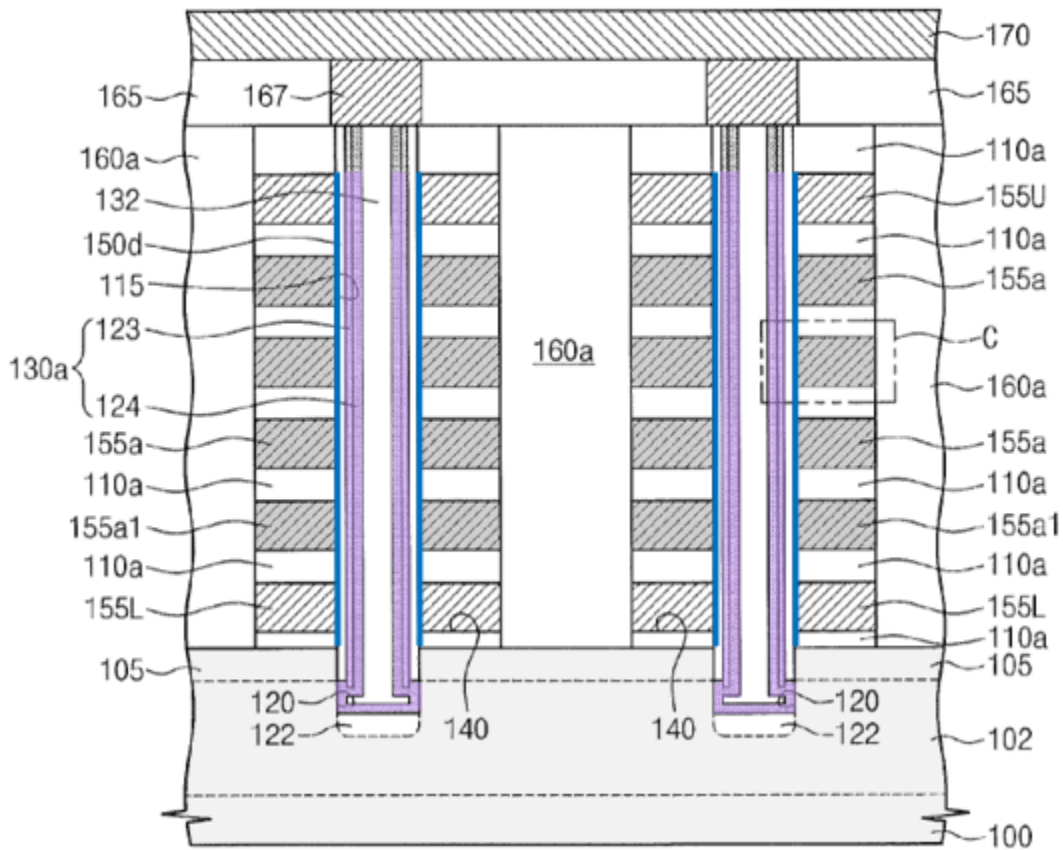
175. Lee '255 teaches that the “blocking dielectric layer 143” is part of gate dielectric layer 150d. Ex. 1004 (Lee), [0056]. “[T]he blocking dielectric layer 143” is on the outside of the gate dielectric layer 150d and “may be adjacent to each of the gate patterns 155L, 155a1, 155a, and 155U.” *Id.*, [0056]. This is shown in figure 4B, where gate electrode 155a (gray) is shown in a abutting blocking dielectric layer 143 (blue):

Fig. 4B



Ex. 1004 (Lee '255), Fig. 4B.

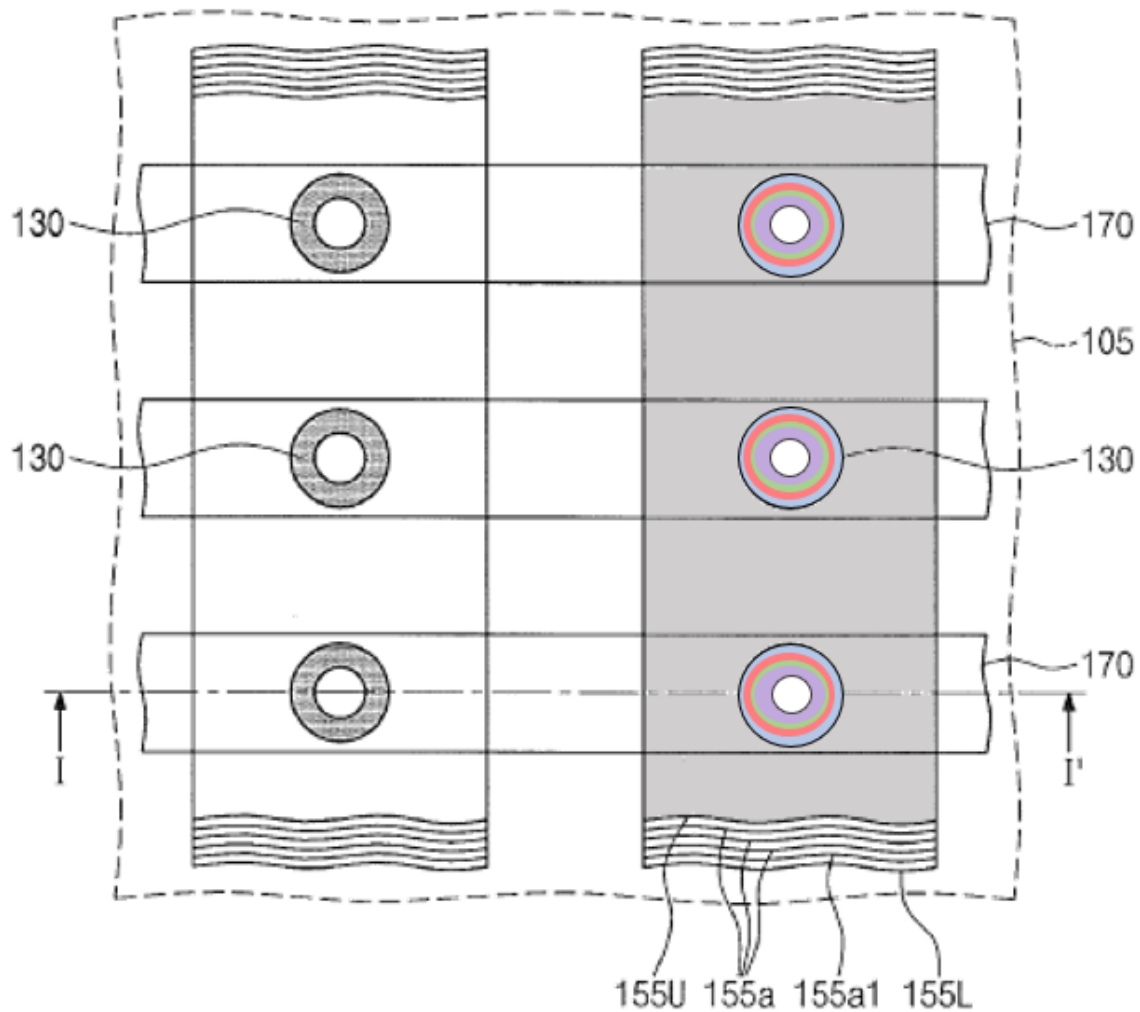
176. I have added blue lines to figure 4A to more clearly illustrate the position of the blocking dielectric layer 143:



Ex. 1004 (Lee '255), Fig. 4A.

177. While Lee '255 does not provide a top view of figure 4A, a POSITA would have understood that the top view would have had the gate stack structure of as shown in figure 1A (gates 155L, 155a1, 155a, and 155U) with the active pattern (130a) and gate dielectric layer (150d) depicted in figure 5A. *See* Ex. 1004 (Lee '255), [0074] ("FIG. 4A is a cross-sectional view taken along the line I-I' of FIG. 1A."), [0077] (FIG 5A includes "the gate dielectric layer 150d" and "vertical active pattern 130a"), [0079] ("The elements of the above-described modification examples may be combined or replaced."). I have combined the elements of

figures 1A (position of the gate electrode), 4B (layers of the gate dielectric layer), and 5B (position of the gate dielectric layer from top view) to illustrate why a POSITA would have understood Lee '255 to teach that gate electrode 155a (gray) is positioned *surrounding the blocking dielectric layer* (blue):



Ex. 1004 (Lee '255), Figs. 1A, 4B, 5A, [0074], [0077].

36. The semiconductor memory device of claim 35, wherein the blocking dielectric layer includes a high K dielectric.

178. I understand that claim 36 depends from claim 35 and therefore has all of the requirements of claim 35. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claim 35.

179. It is my opinion that Lee '255 teaches the additional limitation of claim 36 because it teaches that the “blocking dielectric layer 143 may include a high-k dielectric layer having a dielectric constant higher than that of the tunnel dielectric layer 141.” Ex. 1004 (Lee '255), [0057].

37. The semiconductor memory device of claim 35, wherein the gate electrode is a high work function gate electrode.

180. I understand that claim 37 depends from claim 35 and therefore has all of the requirements of claim 35. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claim 35.

181. It is my opinion that Lee '255 teaches the additional limitations of claim 37 because Lee '255 teaches its gates 155a “include a conductive material” such as doped silicon, tantalum, or tantalum nitride. Ex. 1004 (Lee '255), [0062]. In the context of the SONOS configuration disclosed by the combination of Lee '255 and Lee '961 described above, a POSITA would have understood that

doped silicon and tantalum nitride are *high work function* materials. *See, e.g.*, Ex. 1001 (the '365 patent), 7:31-43 (doped polysilicon used for high work function gate electrodes); Ex. 1012 (Heo), [0046] (P-type silicon, tantalum (Ta), and tantalum nitride (TaN) are examples of materials for high work function gate electrodes); Ex. 1017 (Lai '676), [0067], [0072] (p⁺ polysilicon and tantalum nitride are high work function materials); Ex. 1041 (Zheng), 5:52-62 (P⁺ polysilicon is “particularly well suited” for use in high work function gate electrodes); *id.*, 6:32-59 (tantalum and tantalum nitride used for high work function gate electrodes).

182. To the extent patent owner argues that the gate materials taught in Lee '255 are not *high work function* materials, a POSITA would have found it obvious to use a *high work function gate electrode* based on the teachings of Lee '961. In particular, Lee '961 teaches “[t]he control gate electrode (23A) includes a polysilicon film, particularly **a doped polysilicon film doped with N-type impurities or P-type impurities.**” Ex. 1005 ('961), [0018]. As I explained in the claim construction section, above (see Part VII.C), a POSITA would have understood—based on the examples of *high work function gate electrodes* provided in the '365 patent—that polysilicon doped with p-type impurities is an example of a *high work function* gate material. *See* Ex. 1001 ('365 patent), 7:31-43; *see also* Ex. 1041 (Zheng) 5:36-37 (“For each [] memory device 12, one of the

word lines 14 functions as a gate electrode.”); *id.*, 5:60-62 (“Materials that are particularly well suited for the word lines 14 include P⁺ polysilicon (having a work function of about 5.1 eV to about 5.2 eV.”); Ex. 1012 (Heo), [0046]; Ex. 1017 (Lai ’676), [0067], [0072].

183. A POSITA would have been motivated to apply the high work function gate electrode of Lee ’961 to the memory device of Lee ’255, and expected success in doing so, because the use of such material would have amounted to (i) combining prior art elements according to known methods to yield predictable results; and (ii) use of known techniques to improve a similar device in the same way. As I explained in Part III.C.7, the use of high work function gate electrodes in SONOS-type memory devices was well-established and the benefits of such a design choice were widely recognized. *See, e.g.*, Ex. 1029 (Kim Article), Fig. 7, 000005 (“The erase speed of p⁺ polysilicon gate memory is much faster than that of n⁺ polysilicon gate memory.”); Ex. 1030 (Jeon), Fig. 1, [0009] (“The control gate 14 includes either N⁺ polysilicon with a work function of 4.1 eV or p⁺ polysilicon with a work function of 5.1 eV.”); Ex. 1016 (Lue ’189), [0084] (in preferred embodiments, high work function gates can be formed of metals, metal nitrides, or P⁺ polysilicon), [0086] (“High work function gate materials suppress gate electron injection into the trapping layer. . . . [T]he memory cells according to high work function gate material embodiments of the present invention are

particularly suitable for use in NAND applications where elevated threshold voltages in the erased/reset state can be undesirable.”); Ex. 1012 (Heo), [0064] (teaching the use of a high work function gate electrode to improve the efficiency and ease of operation of the flash memory); 1031 (Shih), [0071] (“In some embodiments, the gate comprises a material having a work function greater than the intrinsic work function of n-type silicon. . . for example, greater than about 5 eV. Representative gate materials include p-type poly TiN, Pt, and other high work function metals and materials.”); Ex. 1041 (Zheng), 1:14-18 (high work function gate electrode enhances data retention).

42. The semiconductor memory device of claim 35, including a stack of layers formed over the substrate.
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184. I understand that claim 42 depends from claim 35 and therefore has all of the requirements of claim 35. As I have explained above, it is my opinion that the combination of Lee ’255 and Lee ’961 teaches each and every limitation of claim 35.

185. It is my opinion that Lee ’255 teaches the additional limitations of claim 42 because it teaches *a stack of layers*— the “stack-structure, including insulation patterns 110a and gate patterns 155L, 155a1, 155a and 155U that are stacked alternately and repeatedly”—that is *formed over the substrate* (substrate

187. As set forth above in the claim construction section, above, a POSITA would have understood the wherein clause of claim 43 to include a typographical error as follows: “wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the gate a sacrificial layer.”

Stack of layers formed over substrate 100

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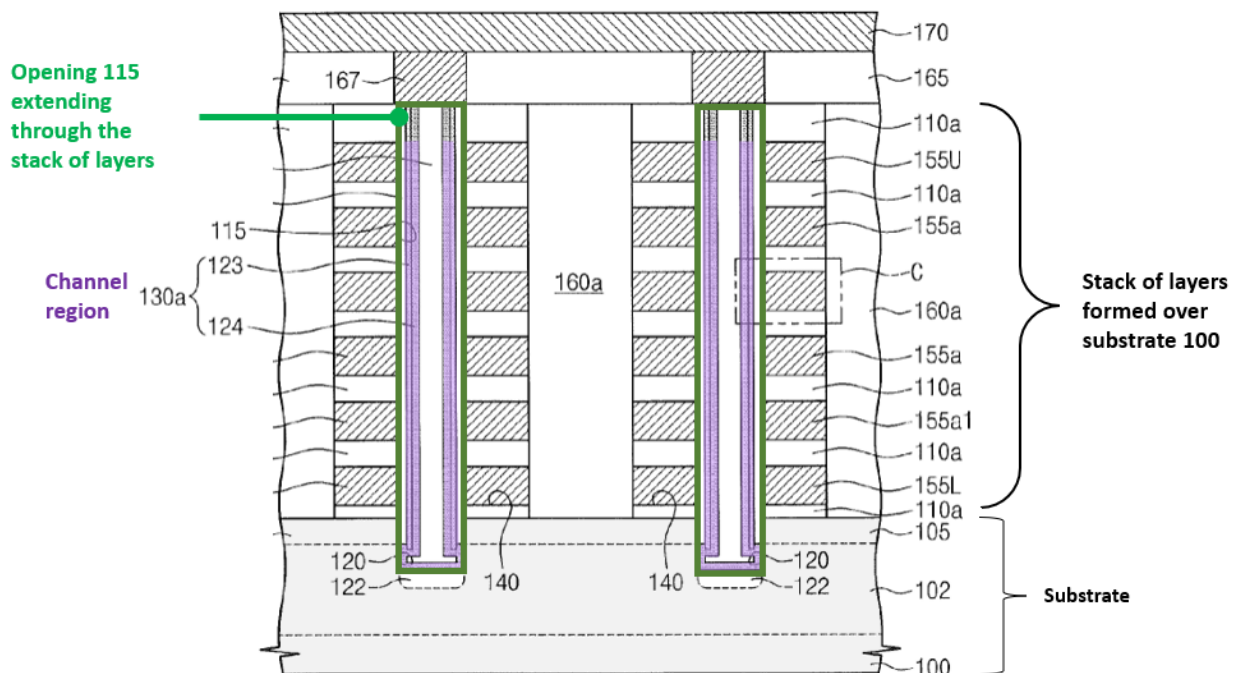
189. Lee '255 teaches *the stack of layers includes a first dielectric layer and a second dielectric layer* because Lee '255 teaches that the stack structure includes “insulation pattern 110a adjacent to each of the gate patterns.” E.g., Ex. 1004 (Lee '255), Fig. 4A, [0055], [0060]. A POSITA would have understood that an insulation layer, such as “insulation pattern 110a” is a *dielectric layer* because a POSITA would have understood that a dielectric layer is a layer that provides electrical insulation. See, e.g., Ex. 1044 (Lai '423), 2:46-59. Further, a POSITA would have understood that insulation pattern 110a is a dielectric layer because it “may include oxide” or “be formed as oxide layers,” which a POSITA would have understood to act as insulators and thereby qualify as *dielectric layers*. Ex. 1004 (Lee '255), [0062], [0080].

190. Lee '255 teaches *a gate layer* because Lee '255 teaches gate patterns 155a. See, e.g., Ex. 1004 (Lee '255), Fig. 4A, [0062].

191. Lee '255 teaches *wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by [the gate] layer* because the insulating patterns 110a and the gate patterns 155a are “stacked alternately” as part of the stack structure, with insulating layers separating gate layers from the substrate. Ex. 1004 (Lee '255), Fig. 4A, [0051]. Further, the gate layers are positioned between the dielectric layers, thus separating the dielectric layers from each other. I have

193. Lee '255 teaches a *channel region* (vertical active pattern 130/130a) as set forth in limitation [35b] and a *stack of layers* (the “stack-structure” of insulating patterns 110a and gate patterns 155) as set forth in claims 42 and 43.

194. As shown in Figure 4A, Lee '255 teaches the *channel region* (active pattern 130/130a) is *formed in an opening* (“opening 115”) that is *extending through the stack of layers* (insulation patterns 110a and gate patterns 155L, 155a1, 155a and 155U). I have highlighted opening 115 in green:



Ex. 1004 (Lee '255), Fig. 4A, [0077].

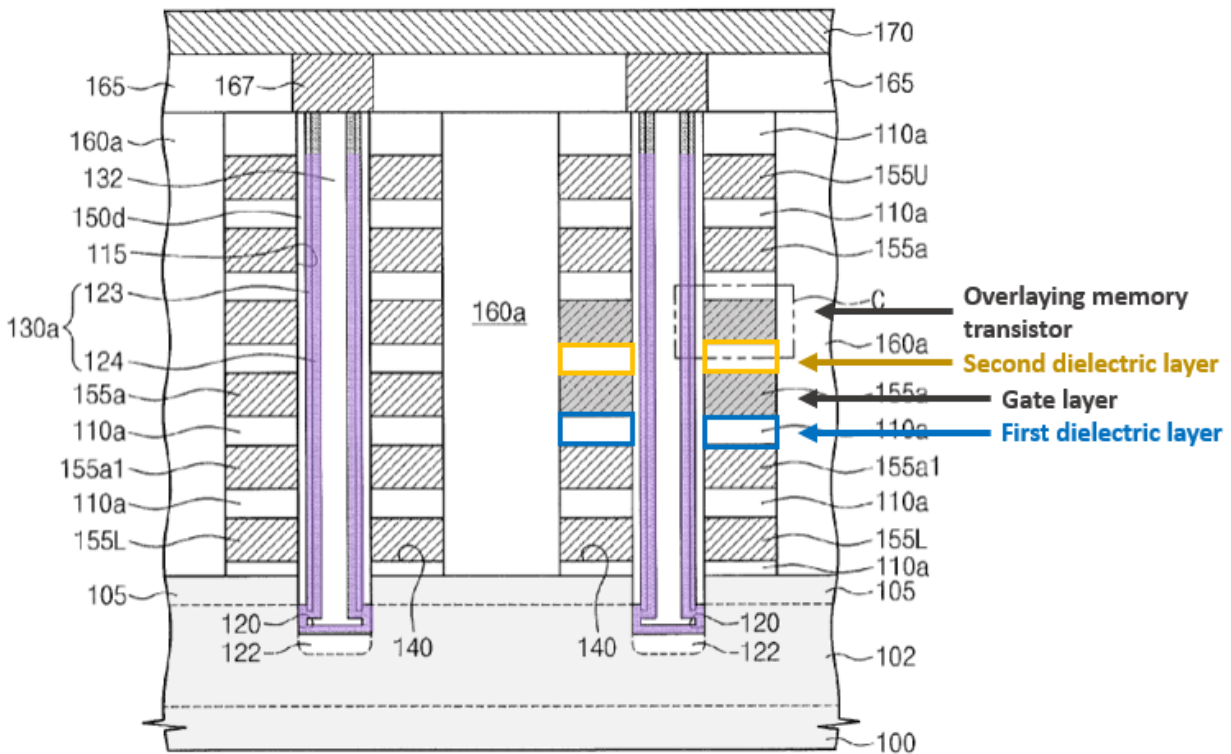
45. The semiconductor memory device of claim 43, wherein the second dielectric layer separates the gate layer from an overlying memory transistor.

195. I understand that claim 45 depends from claims 35, 42, and 43. As I have explained above, it is my opinion that the combination of Lee '255 and

Lee '961 teaches each and every limitation of claim 35 and the additional limitations of claims 42 and 43. In my opinion, Lee '255 also teaches the additional limitations of claim 45.

196. First, a POSITA would have understood, and Lee '255 expressly teaches, that each gate pattern (e.g., 155a) is representative of an individual *memory transistor*. Ex. 1004 (Lee '255), [0058]-[0060] (“cell transistors includ[e] the cell gates” 155a). Further, a POSITA would have understood that the nature of the 3D NAND devices, such as those taught in Lee '255, is to create a vertical stack multiple memory transistors to form an array. *See* Parts III.C.6 and 8; *see also* Ex. 1026 (Tanaka), 00001 (“One solution to avoid such situation is three dimensionally stacked array structures as reported in previous papers [1] [2], in which planar NAND structures are simply stacked.”).

197. Second, as set forth in connection with claim 43, any one of the three-layer stacks of dielectric layers 110a and gate layers 155a teaches *a first dielectric layer, a gate layer and a second dielectric layer*, including the example three-layer stack identified in the annotated Figure 4A for claim 43. Using the same example three-layer stack, I have annotated figure 4A to reflect one of the places where Lee '255 teaches *the second dielectric layer separates the gate layer from an overlying memory transistor*:



Ex. 1004 (Lee '255), Fig. 4A.

3. Independent Claim 1

[1pre] A method comprising:

198. I understand that a preamble does not always limit the claim. *See* Appendix 4. To the extent Patent Owner argues this preamble is limiting, it is my opinion that Lee '255 teaches *a method* of making semiconductor memory devices. *See, e.g.,* Ex. 1004 (Lee '255), FIGS. 6A-10C, 13A-16B, [0080] (“FIGS. 6A to 6H are cross-sectional views taken along line I-I’ of FIG. 1A for describing a method of fabricating [a] 3D semiconductor memory device according to an embodiment of the inventive concept.”), [0131].

[1a1]	forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;
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199. It is my opinion that Lee '255 teaches limitation [1a1] because Lee '255 teaches forming an alternating stack of insulating and sacrificial layers over the substrate. *See* Ex. 1004 (Lee '255), Fig. 6A, [0080].

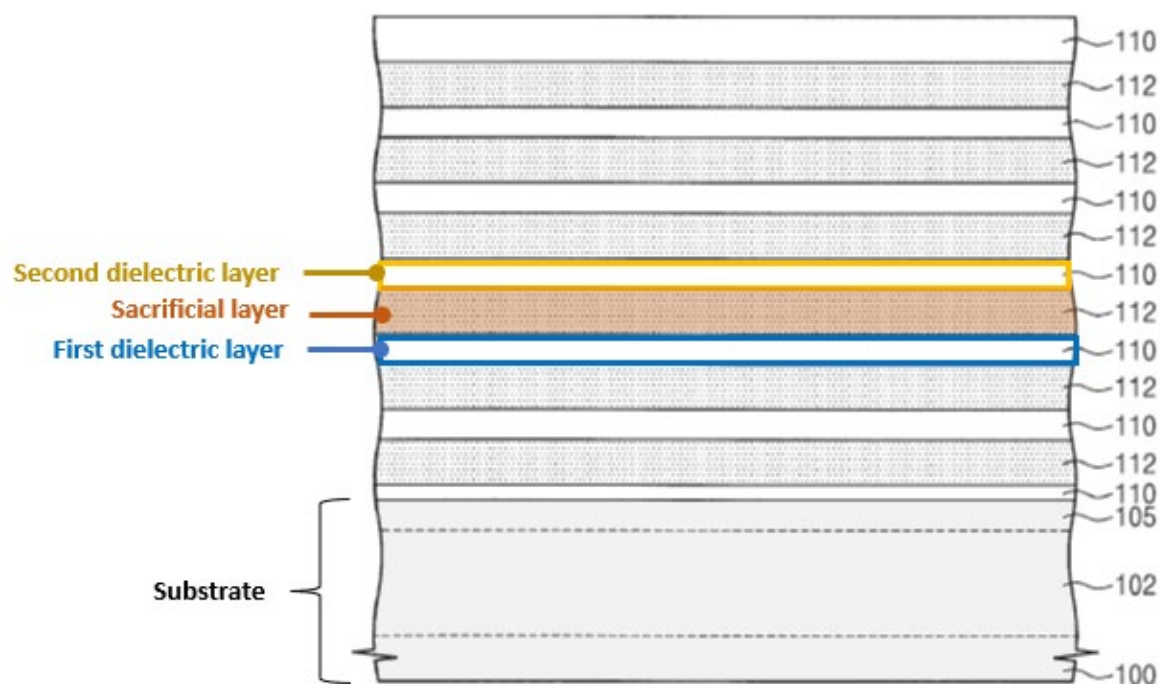
200. Lee '255 teaches *forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer* because Lee '255 teaches “[i]nsulation layers 110 and sacrificial layers 112 may be alternately and repeatedly stacked on the common source region 105 [of substrate 100].” Ex. 1004 (Lee '255), [0080]; *see also id.*, [0077] (common source region 105 is part of the substrate).⁵ Forming this stack of layers over a substrate is depicted, for example, in figure 6A:

⁵ As discussed below, sacrificial layers 112 are later removed to form the gate patterns 155L, 155a1, 155a and 155U in the finished FIG. 4A device discussed above.

A cross-sectional view of a substrate 100. The substrate 100 is a solid layer at the bottom. Above it is a stack of alternating layers: dielectric layers 110 (represented by horizontal lines) and sacrificial layers 112 (represented by stippled patterns). The stack consists of eight pairs of these layers. The topmost layer is a dielectric layer 110. Below the stack is a dashed line representing an interface 102. The entire structure is labeled with a bracket as "Stack of dielectric layers 110 and sacrificial layers 112 formed over substrate 100".

201. As reflected above, Lee '255 teaches forming a *first* and a *second* dielectric layer because Lee '255 teaches that there are multiple insulation layers 110. Lee '255 further teaches that insulation layers 110 “may be formed as oxide layers” and “sacrificial layers 112 may be formed of materials having an etch selectivity.” Ex. 1004 (Lee '255), [0080]. For example, “sacrificial layers 112 may be formed as nitride layers.” Ex. 1004 (Lee '255), [0080]. A POSITA would have understood that an oxide insulation layer is a *dielectric layer*. See, e.g., Ex. 1042 (Sze), 000013.

Fig. 6A

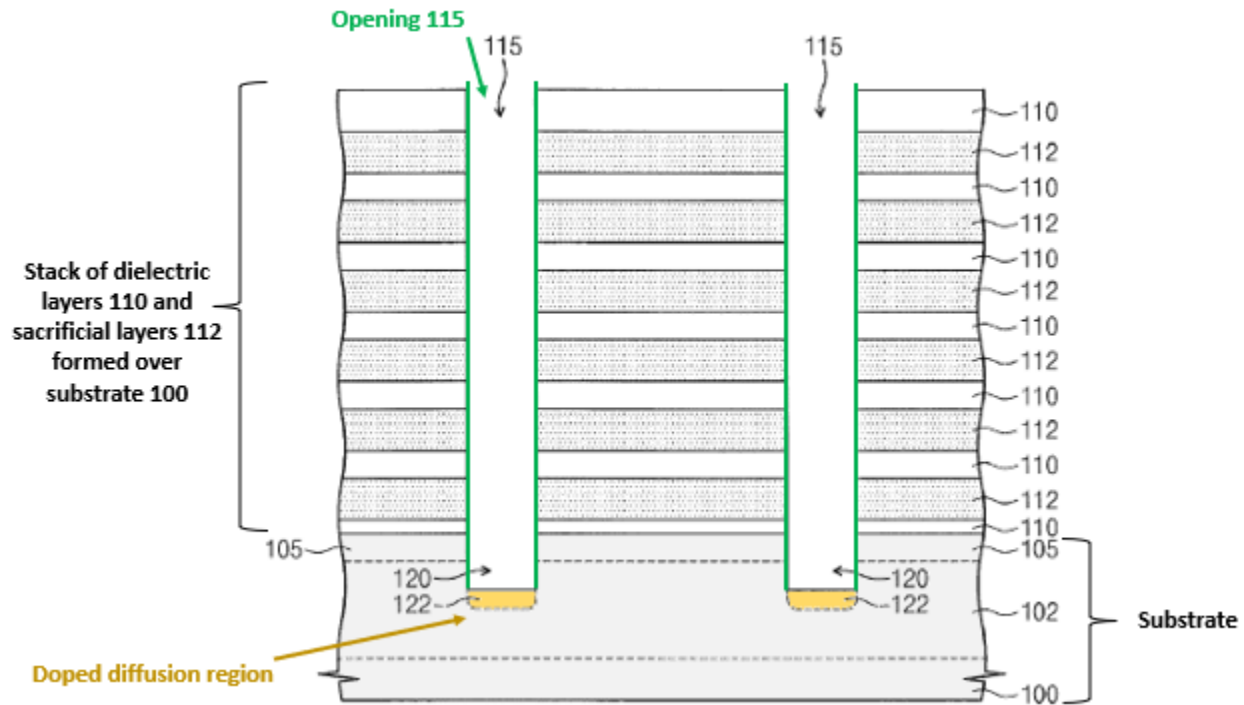


203. As reflected above, Lee '255 teaches that a first dielectric layer 110 (blue border) separates a sacrificial layer 112 (orange) from substrate 100 (light

gray). Lee '255 further teaches that the same sacrificial layer 112 (orange) separates the same first dielectric layer 110 (blue border) from a second dielectric layer 110 (yellow border).

[1a2]	forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate;
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204. It is my opinion that Lee '255 teaches limitation [1a2] because Lee '255 teaches *forming an opening* (opening 115) that *extend[s] through the stack of layers* (the stack of the insulation layers 110 and sacrificial layers 112) *to a first doped diffusion region formed on the substrate* (high concentration region 122). Ex. 1004 (Lee '255), [0081] (“The opening 115 may pass through the insulation layers 110 and sacrificial layers 112.”). This process is depicted in figure 6B, which I have annotated here:



Ex. 1004 (Lee '255), Fig. 6B.

205. As shown in figure 6B above, Lee '255 teaches that opening 115 extends to high concentration region 122 on substrate 100 (*an opening extending through the stack of layers to a first doped diffusion region formed on the substrate*). Ex. 1004 (Lee '255), Fig. 4A, 6B, [0081].

206. Lee '255 teaches that high concentration region 122 is a *first doped diffusion region* because Lee '255 teaches that “high concentration region 122 may be formed by providing the first conductive dopant into the well region 102 through the bottom surface of the recess region 120. The high concentration region 122 of the first conductive dopant may be higher than another portion of the well region 102.” Ex. 1004 (Lee '255), [0081]. And, more generally, a POSITA would

have understood that *diffusion regions*—e.g., sources and drains—are regions doped with conductive dopants so that charge carriers (electrons or holes) flow to or from those regions through a channel. *See, e.g.*, Ex. 1042 (Sze), 000016. The '365 patent confirms this understanding. *See, e.g.*, Ex. 1001 ('365 patent), 8:33-35 (diffusion regions are a source and drain separated from each other by a channel), 7:63-64 (identifying the source and drain regions as “heavily doped” and separated by the channel).

207. Lee '255 further teaches that high concentration region 122 is formed *on the substrate* as shown in figure 6B, above. Ex. 1004 (Lee '255), FIG. 6B. A POSITA would have understood that the positioning of the *first doped diffusion region* of Lee '255 in this regard mirrors the positioning of the first diffusion region 904 in figures 9A-9E of the '365 patent (as shown in my annotated version of figure 9E below), which is the only vertical channel embodiment of the '365 patent that identifies diffusion regions *vis-à-vis* a substrate.

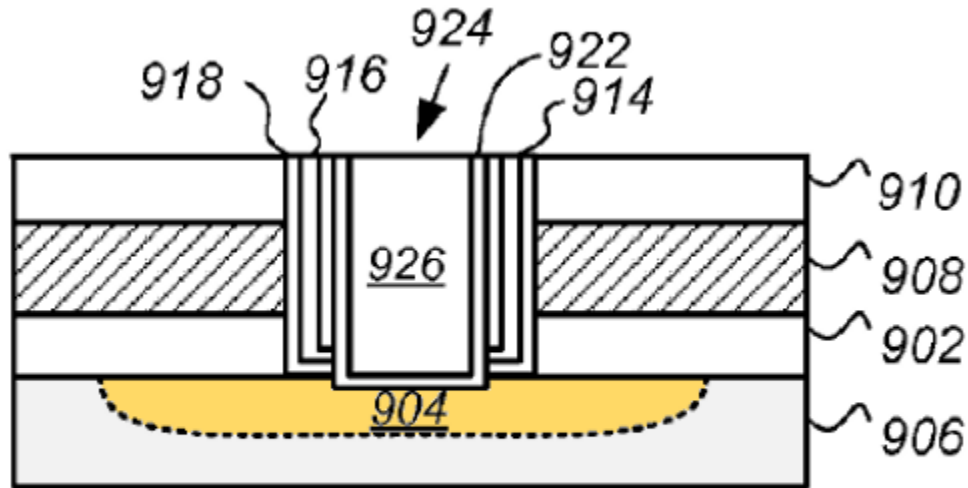
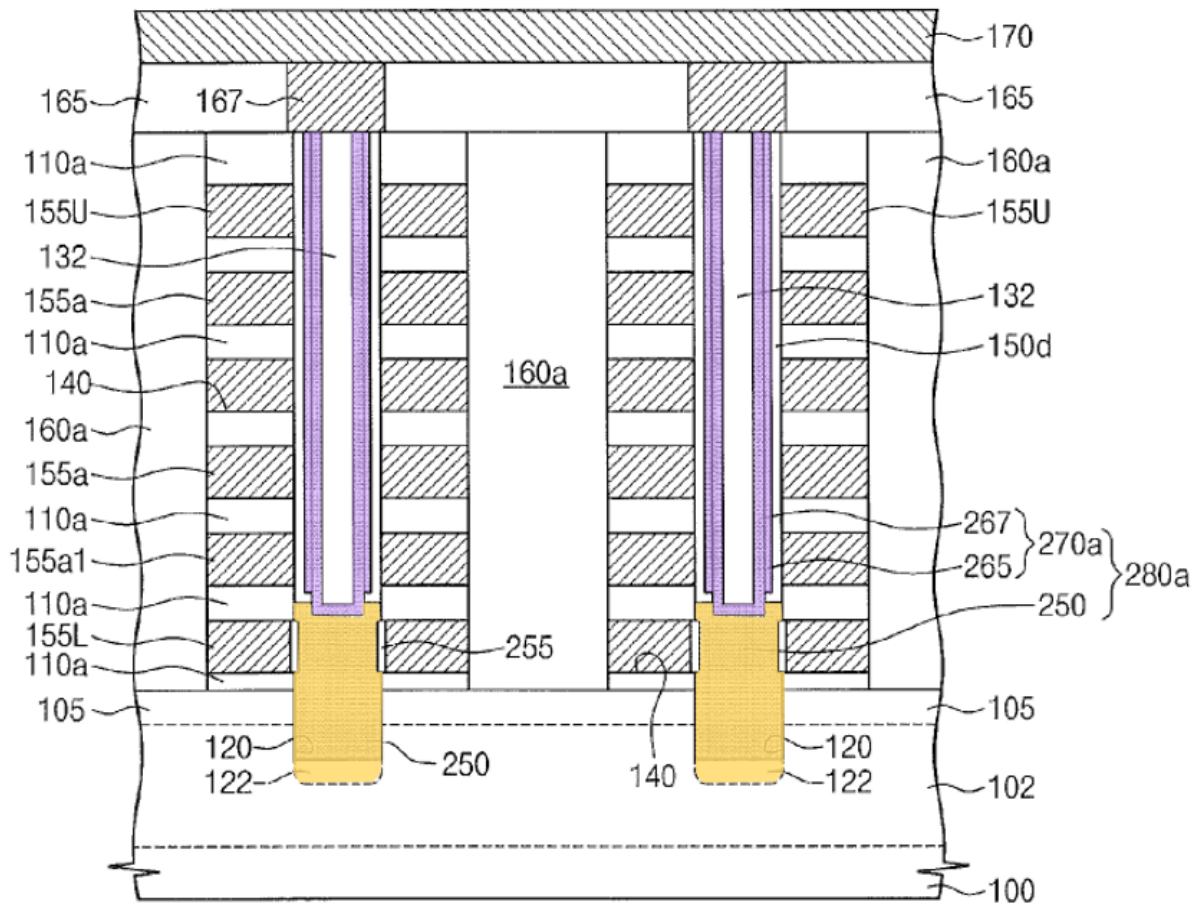


FIG. 9E

Ex. 1001 ('365 patent), Fig. 9E.

208. Alternatively, Lee '255 teaches in, for example, its FIG. 11 and 12A-12F embodiments, the use of doped lower active pattern 250. Ex. 1004 (Lee '255), Figs. 11, 12A-12F, [0133]. A POSITA would have understood that doped lower active pattern 250 and portion 122 together (or pattern 250 alone) would form a diffusion region for the reasons above that extends on and above substrate 100 where it connects with the bottom of vertical channel 130:

Fig. 12E



Ex. 1004 (Lee '255), FIGS. 11 and 12A-12F, [0113], [0114], [0133].

209. It would have been obvious to a POSITA to employ such doped lower active pattern 250 in combination with high concentration region 122 because Lee '255 teaches that it is an alternative configuration within its inventive concept that provides improved reliability. Ex. 1004 (Lee '255), [0113], [0118].

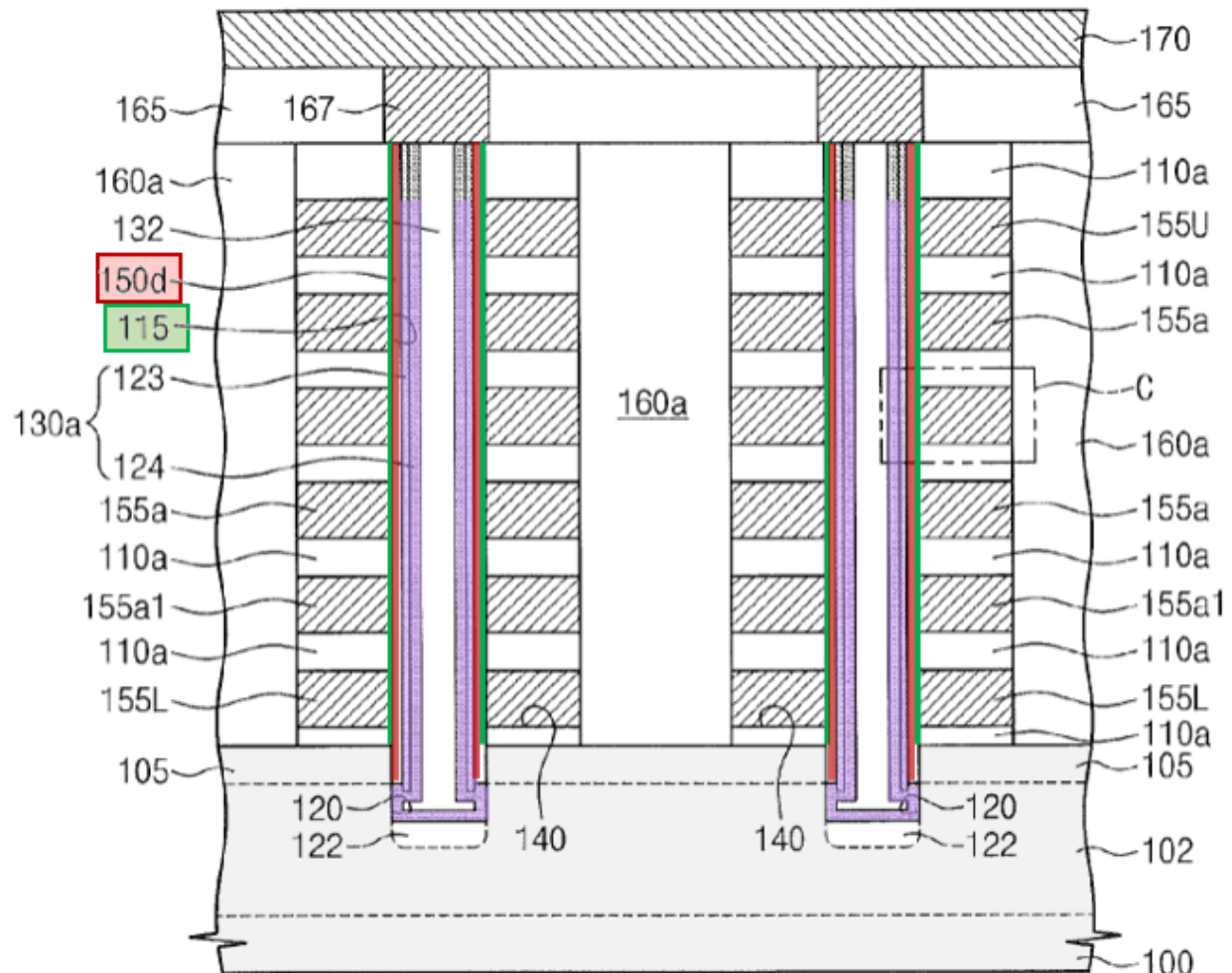
[1b]	forming on sidewalls of the opening a blocking dielectric layer;
[1c]	forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region;
[1d]	forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and

210. It is my opinion that the combination of Lee '255 and Lee '961 teaches limitations [1b]-[1d] for the following reasons.

211. Lee '255 teaches [1b] *forming on sidewalls of the opening a blocking dielectric layer*; [1c] *forming on an inside sidewall of the blocking dielectric layer a . . . charge storing region*; and [1d] *forming on an inside sidewall of the . . . charge storing region a tunnel dielectric layer* because Lee '255 teaches forming a dielectric gate layer 150d in opening 115, with successive blocking, charge-trapping, and tunneling sub-layers in the sequence and relative position required by limitations [1b], [1c], and [1d]. *See, e.g.*, Ex. 1004 (Lee '255), Figs. 4A, 4B, 5A, 5B, [0055], [0056], [0077].

212. As a threshold matter, Lee '255 teaches that dielectric gate layer 150d is formed on the sidewalls of opening 115. Ex. 1004 (Lee '255), [0077] (“[T]he gate dielectric layer 150d may be disposed between the vertical active pattern 130a and the inner sidewall of an opening 115 passing through the stack structure.”). This is depicted, for example, in figure 4A, where I have used green to identify the

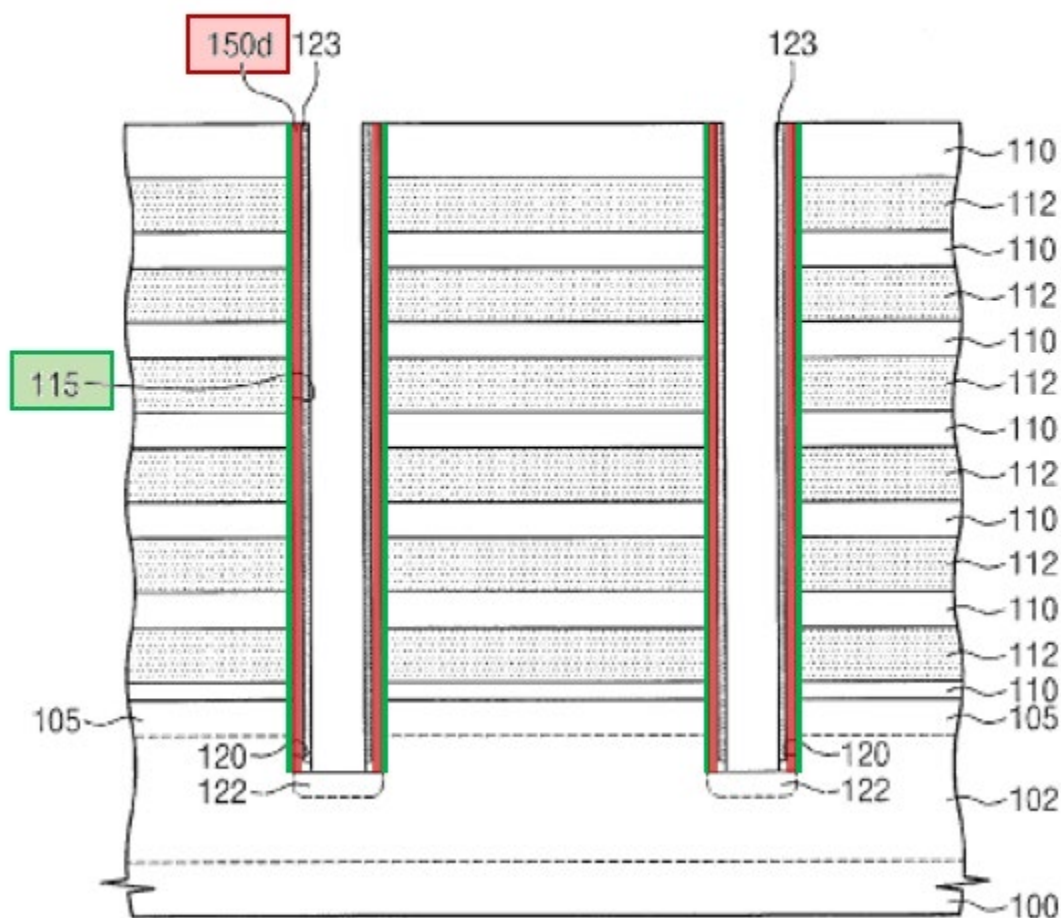
sidewalls of the stack of layers along opening 115 and maroon to mark the location of gate dielectric layer 150d:



Ex. 1004 (Lee '255), Fig. 4A.

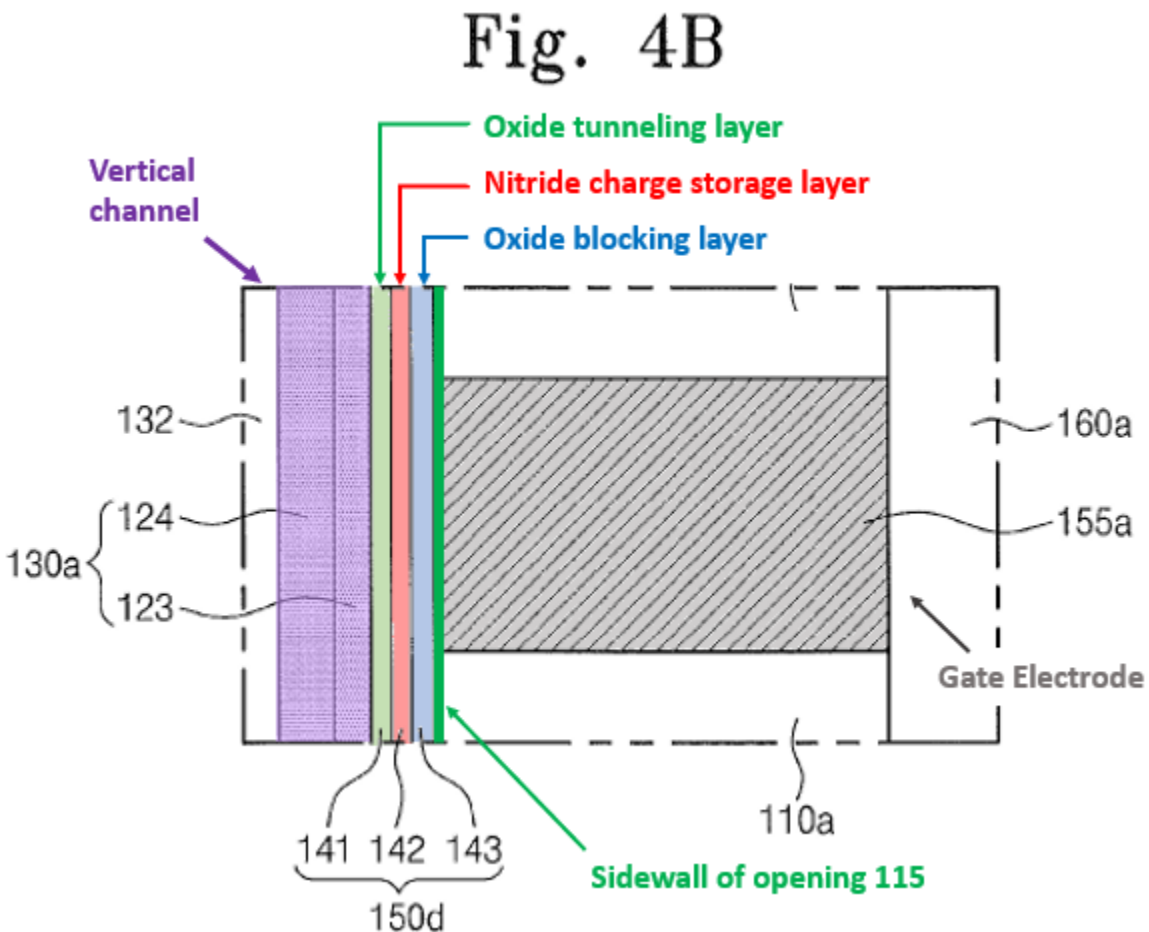
213. Figure 9A of Lee '255 also shows that the gate dielectric layer 150d is formed on the sidewalls of opening 115. I have again annotated the figure to show the sidewalls of opening 115 in green and the gate dielectric layer in maroon:

Fig. 9A



Ex. 1004 (Lee '255), Fig. 9A, [0105] (“the gate dielectric layer 150d may also be restrictively disposed in the opening 115”), [0111] (“In other words, the 3D semiconductor memory device of FIGS. 4A and 4B may be implemented in the method that has been described above with reference to FIGS. 9A to 9D or a modified method of a portion of the fabricating method of FIGS. 10A to 10C.”).

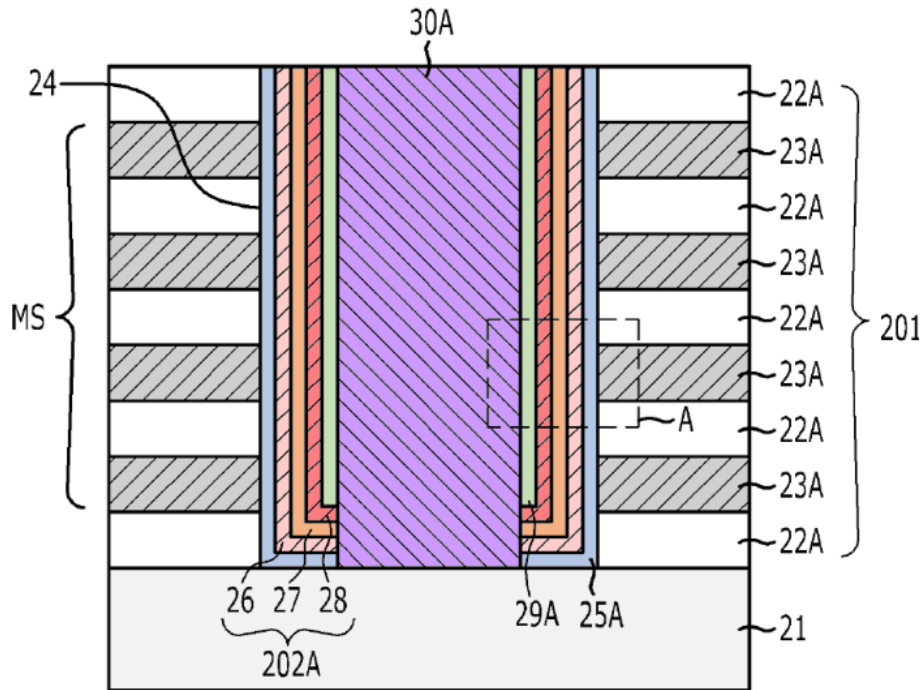
214. Figure 4B provides a magnified view showing the position of the layers of the gate dielectric layer 150d. Lee '255 teaches that (i) blocking dielectric layer 143 (*a blocking dielectric layer*) is *form[ed] on the sidewalls of the opening* (opening 115); (ii) charge storage layer 142 (*a . . . charge storage region*) is *form[ed] on an inside sidewall of the blocking dielectric layer*; and (iii) tunneling layer 141 (*a tunnel dielectric layer*) is *form[ed] on the sidewall of the . . . charge storing region*:



Ex. 1004 (Lee '255), Fig. 4B, [0056], [0074].

215. As reflected above, Lee '255 teaches that the layers are positioned as required in limitations [1b]-[1d]. In particular, blocking dielectric layer 143 (blue) is formed on the sidewall of opening 115 (green) as required in limitation [1b]. Next, charge trapping layer 142 (red) is formed on the inner sidewall of blocking dielectric layer 143 (blue), as required in limitation [1c]. Next, tunneling layer 141 (green) is formed on the sidewall of charge trapping layer 142 (red), as required in limitation [1d].

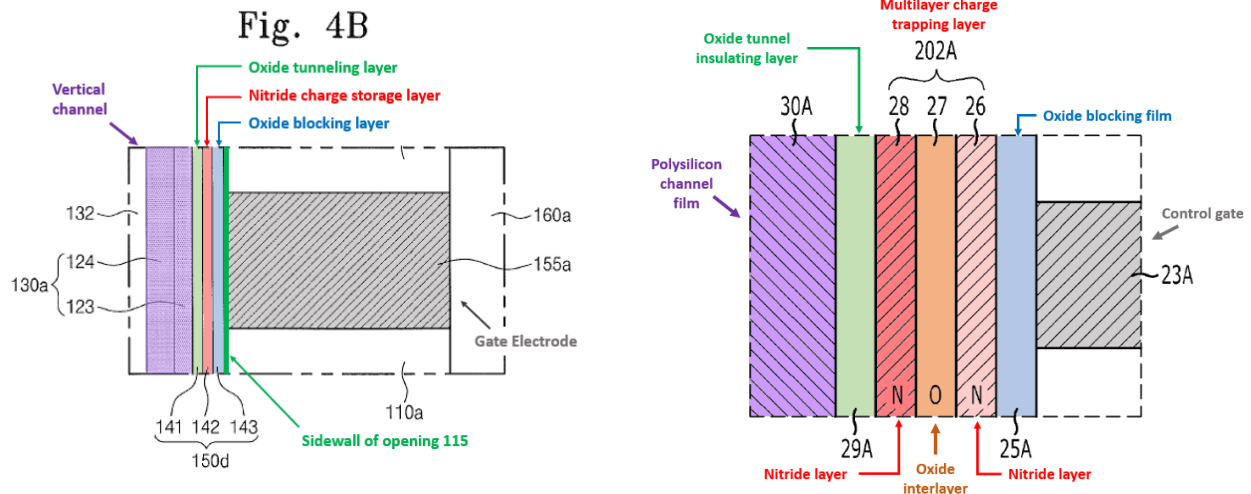
216. As I explained in connection with Limitation [35d], above, a POSITA would have been motivated to modify the charge storage layer 142 of Lee '255 based Lee '961's teachings of a multilayer charge storage region and it would have been a straight-forward process to deposit an additional layer in connection with the device of Lee '255. *See* Limitation [35d], above. This modification would have resulted in a multilayer charge storage region in Lee '255, modeled on region 202A depicted in figures 2a and 2b of Lee '961:



217. A POSITA would have understood that the position of the modified charge trapping region in Lee '255 would have remained the same—i.e., it would be formed on the sidewall of the blocking dielectric layer (blue) and separate that layer from the tunneling layer (green), as is shown in both figure 4B of Lee '255 (charge storage layer 142) and figure 2b of Lee '961 (multilayer charge trapping layer 202A):

Lee '255 – Figure 4B

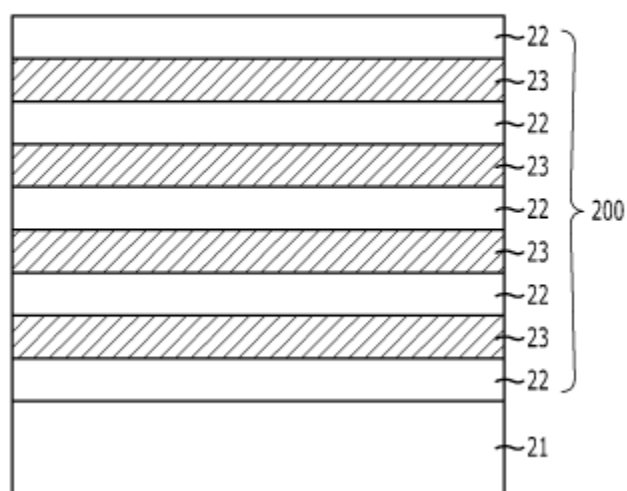
Lee '961 – Figure 2b



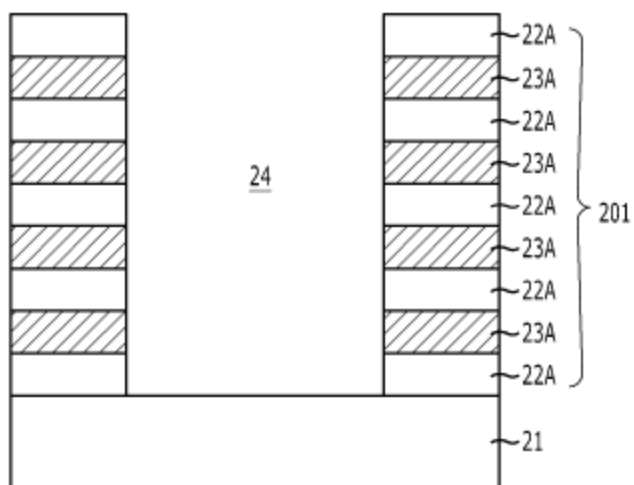
Ex. 1004 (Lee '255), Fig. 4B; Ex. 1005 (Lee '961), Fig. 2b.

218. A POSITA would have expected success in modifying the charge storage layer of Lee '255 based on the multilayer charge storing layer of Lee '961 because the two references teach similar processes for forming the layers in the positions required by Limitations [1b], [1c], and [1d]. In particular, Lee '961 teaches forming an opening in a stack of layers (hole 24). Ex. 1005 (Lee '961), [0025]. Lee '961 then teaches that “a blocking film (25), a multilayer charge trap layer 202, and a tunnel insulating layer (29) are sequentially stacked onto the memory cell stack.” Ex. 1005 (Lee '961), [0026]. The formation of these layers is shown in figures 3a -3c:

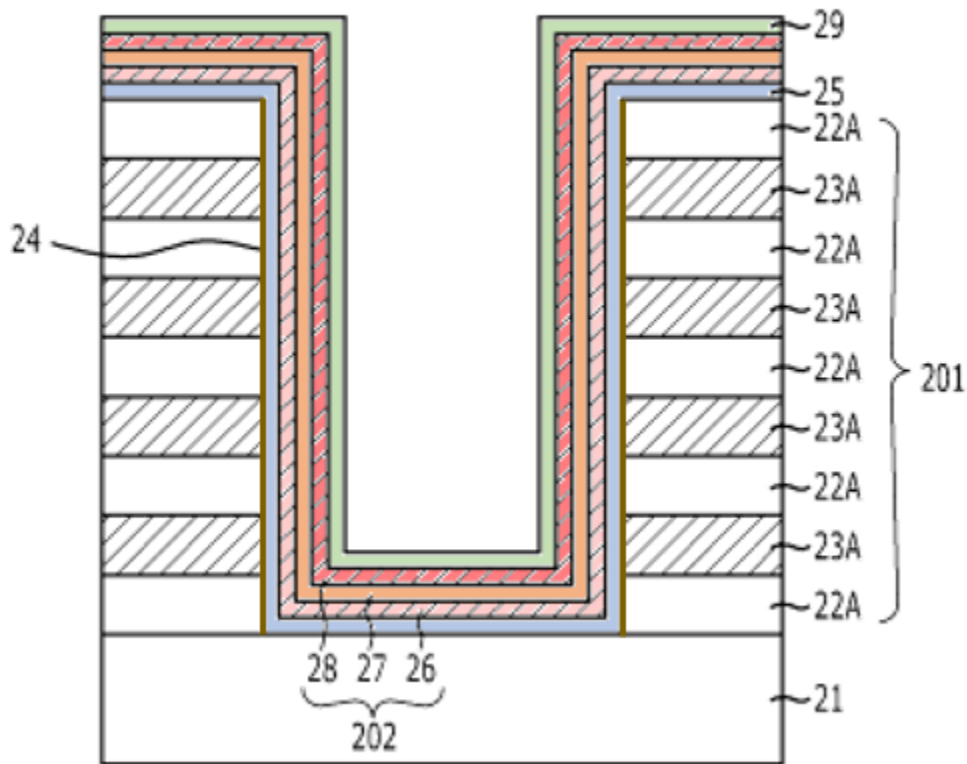
도면3a



도면3b



도면3c



Ex. 1005 (Lee '961), FIG. 3c, [0026].

219. Based on this teaching, a POSITA would have understood that the constituent layers of the Lee '255 / Lee '961 combination would have been formed sequentially, one on top of another, from the outermost layer to the innermost to result in the completed device configuration shown in FIGS. 4A/B.

220. Specifically, a POSITA would have understood that Lee '255's oxide blocking dielectric layer 143 (*blocking dielectric layer*) would first be formed on the inner sidewall of opening 115, which is its position in FIG. 4B (*forming on sidewalls of the opening a blocking dielectric layer*).

221. Next, the *multi-layer charge storing region* taught by the Lee '255 / Lee '961 combination would be formed (instead of Lee '255's nitride charge storage layer 142) on the inner surface of oxide blocking dielectric layer 143, which is the position of layer 142 in FIG. 4B (*forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region*). The multiple layers of Lee '961's *multi-layer charge storing region* would also be successively formed in a similar manner.

222. Finally, Lee '255's tunneling oxide layer 141 (*tunnel dielectric layer*) would be formed on the inner surface of the nitride charge storage layer 142 (*forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer*).

223. The foregoing teaches all of the limitations [1b]-[1d].

[1e]	forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.
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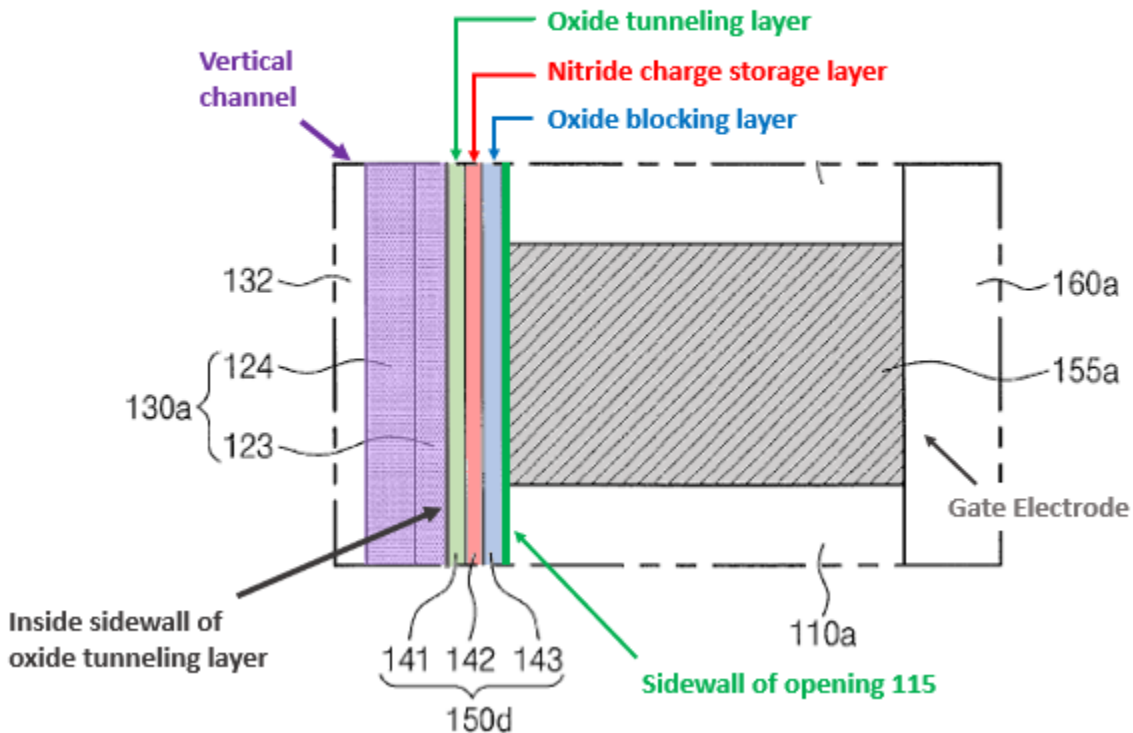
224. It is my opinion that Lee '255 teaches limitation [1e] for at least the following reasons.

225. As set forth in connection with limitation [35b], Lee '255 teaches a *vertical channel* because Lee '255 teaches forming vertical active pattern 130/130a. See analysis of Limitation [35b], above.

226. Lee '255 teaches that vertical active pattern 130/130a (the *vertical channel*) *has* semiconductor material because Lee '255 teaches “the vertical active pattern 130 may include the same semiconductor material as that of substrate 100”—e.g., silicon—and “may have a polycrystalline state or a single crystalline state.” Ex. 1004 (Lee '255), [0062], [0050].

227. Lee '255 teaches that the vertical active pattern 130/130a is *formed* on an inside sidewall of the tunnel dielectric layer because Lee '255 teaches that “[t]he tunnel dielectric layer 141 may be adjacent to the sidewall of the vertical active pattern 130.” Ex. 1004 (Lee '255), [0056]; *see also id.*, [0105] (“A first semiconductor layer may be conformally formed on the gate dielectric layer 150d”). The position of the vertical active pattern (*vertical channel*) of Lee '255 on an inside sidewall of the tunnel dielectric layer is further taught in figure 4B of Lee '255, which shows that the vertical channel (purple) is formed on the inside sidewall of the tunnel dielectric layer 141 (green):

Fig. 4B



Ex. 1004 (Lee '255), Fig. 4B; *see also* Figs. 9A/9B (showing the formation of vertical active pattern 130a on gate dielectric layer 150d), [0106] (“Referring to FIG. 9B, subsequently, a second semiconductor may be conformally formed over the substrate 100 ... The first and second semiconductor patterns 123 and 124 may configure a vertical active pattern 130”).

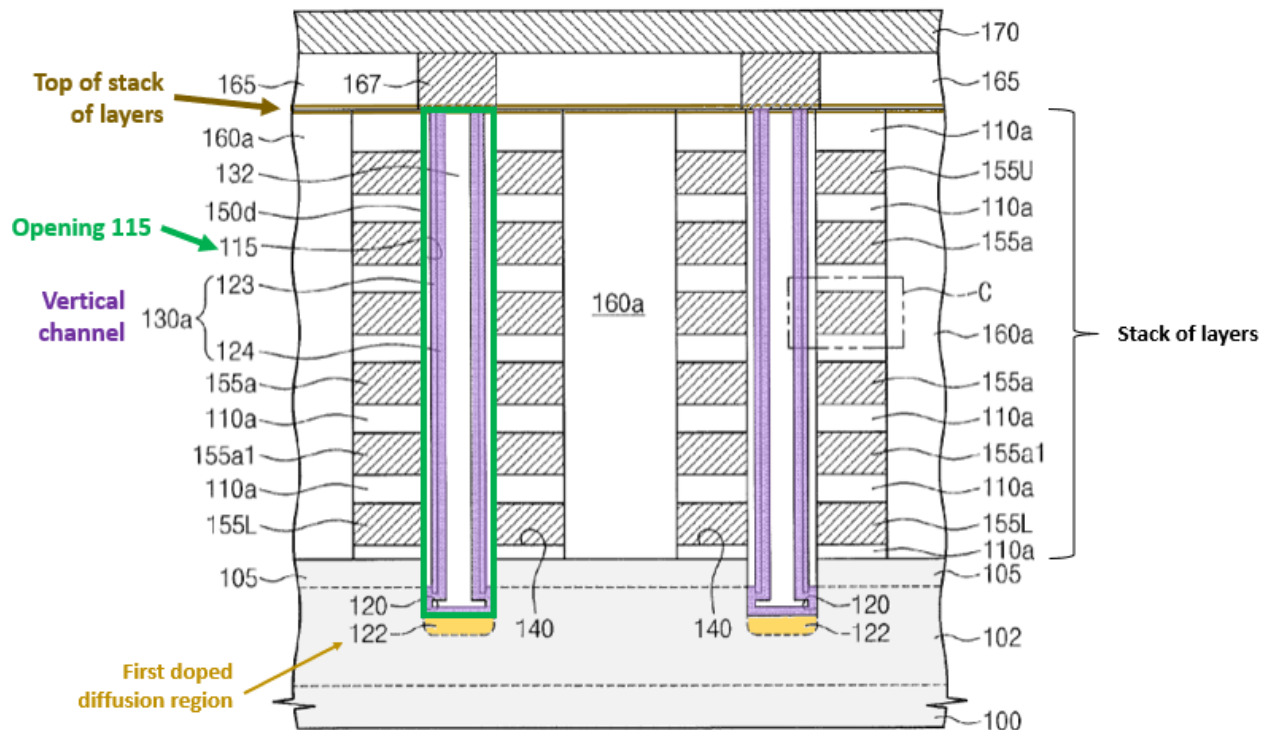
228. Lee '255 teaches the vertical active pattern 130/130a *extend[s] from the first doped diffusion region through the opening to a top of the stack of layers* because Lee '255 teaches that the vertical active pattern 130 extends through opening 115 (*the opening*) from “[t]he high concentration region 122 of the first conductive dopant” (*the first doped diffusion region*) and “may pass through the

stack-structure” (*the stack of layers*). Ex. 1004 (Lee ’255), Figs. 1A, 4A, [0052]

(“The vertical active pattern 130 may be extended into a recess region 120”); [0053]

(high concentration region 122 is at bottom of recess region 120), [0077], [0081].

Figure 4B provides a further teaching of the position of the vertical channel relative to the stack of layers, showing the vertical channel extends through opening 115 to the top of the stack of layers:



Ex. 1004 (Lee ’255), Fig. 4B.

2. The method of claim 1, further comprising the step of forming a second diffusion region such that the vertical channel connects the first and second diffusion regions.

229. I understand that claim 2 depends from claim 1 and therefore has all of the requirements of claim 1. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claim 1.

230. It is my opinion that Lee '255 teaches the additional limitations of claim 2 because Lee '255 teaches that a “drain being doped with the second conductive dopant may be formed in the upper portion of the vertical active pattern 130. A lower surface of the drain may be disposed on a level adjacent to an upper surface of the uppermost gate pattern 155U” (*forming a second diffusion region*). Ex. 1004 (Lee '255), [0063]. This drain region is identified in annotated FIG. 4A below.

that the high concentration region 122, the active pattern 130/130a, and the drain are all physically connected.

233. To the extent *connects* is interpreted to mean electrically connects or couples, Lee '255 teaches that the high concentration region 122, the active pattern 130/130a and the drain are formed of conductive materials and are connected for current flow. Ex. 1004 (Lee '255), [0064] (“a current flowing through the vertical active pattern 130”), [0053] (“the first **conductive** dopant concentration of the portion 122”), [0063] (“a drain being doped with the second **conductive** dopant”). A POSITA also would have understood these elements to be electrically connected because that is how a charge trapping memory device functions—i.e., electrons must flow in the vertical channel between the diffusion regions to permit tunneling of the electrons into the charge capture layers. *See, e.g.*, Ex. 1008 (Frohman-Bentchkowsky), 4:32-45; *see also* Part III.C.3 (explaining the operation of SONOS memory transistors).

3. The method of claim 1, further comprising forming a layer of semiconductor material including a second doped diffusion region over a top surface of the stack of layers and the opening, wherein the vertical channel electrically couples the first doped diffusion region to the second doped diffusion region.

234. I understand that claim 3 depends from claim 1 and therefore has all of the requirements of claim 1. As I have explained above, it is my opinion that

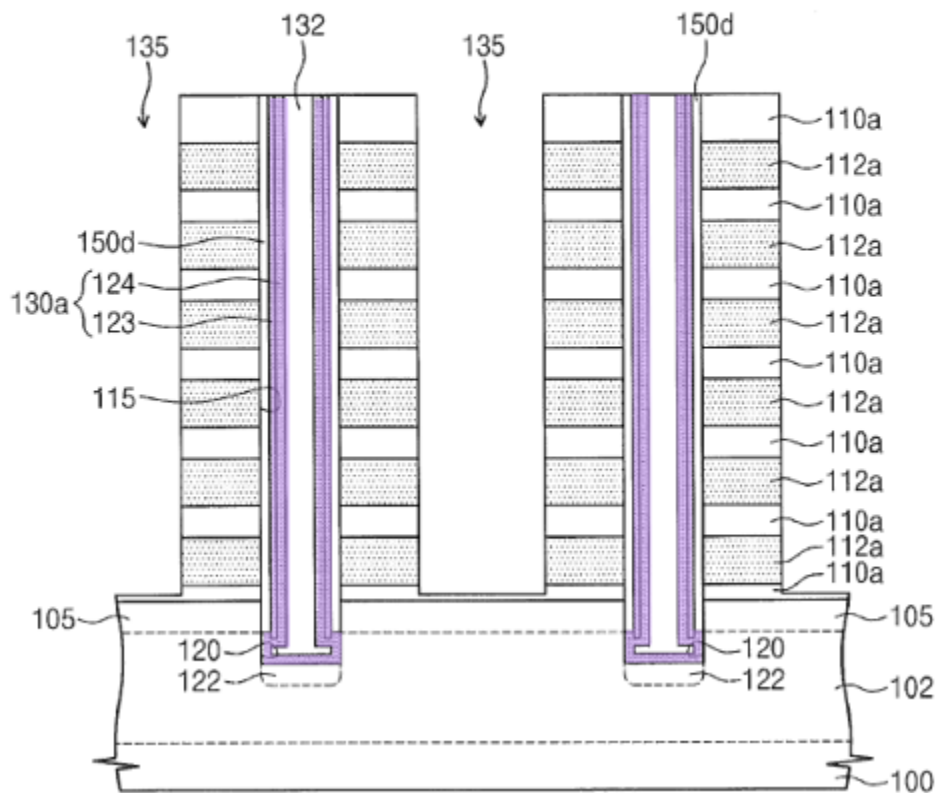
the combination of Lee '255 and Lee '961 teaches each and every limitation of claim 1.

235. It is my opinion that Lee '255 teaches the additional limitations of claim 3.

236. First, Lee '255 teaches *forming a layer of semiconductor material ... over a top surface of the stack of layers and the opening* because it teaches the successive deposition of first and second semiconductor layers 123 and 124 (*layers of semiconductor material*) over both the top surface of the stack of layers and along the inner surfaces of opening 115 (*over a top surface of the stack of layers and the opening*) to thereby form the vertical channels 130/130a described above. Ex. 1004 (Lee '255), [0105] (“A first semiconductor layer may be **conformally formed** on the gate dielectric layer 150d.”); [0106] (“subsequently, a second semiconductor may be **conformally formed over the substrate 100**”).

237. A POSITA would have understood “conformally formed” to mean that the first and second semiconductor layers 123 and 124 are both deposited over the entire upper surface of the layer stack and along the walls of opening 115, before the portions on the upper surface of the layer stack are removed to arrive at the construction shown in Figure 9B:

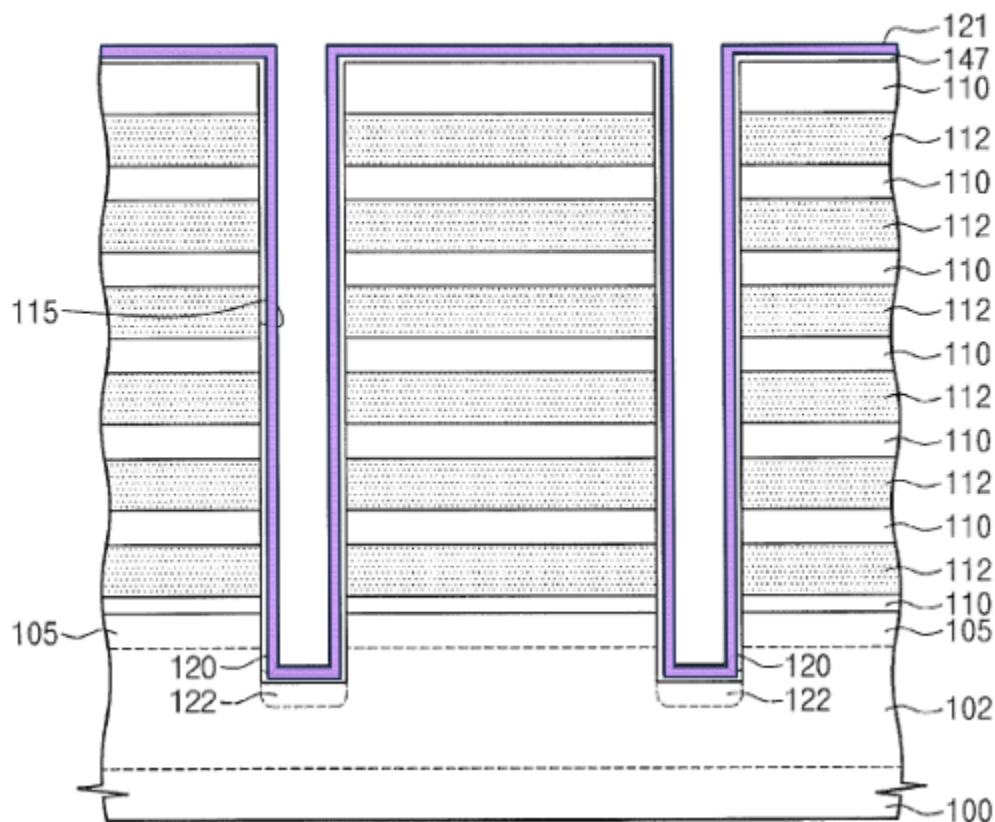
Fig. 9B



Ex. 1004 (Lee '255), Fig. 9B.

238. While this process is not explicitly portrayed with respect to Figure 9B, it is in the related procedure shown in Figures 8A and 8B, where first semiconductor layer 121 is “conformally formed” *over a top surface* of the layer stack and in opening 155 in Fig. 8A and a POSITA would have understood that the same process would have applied to semiconductor layers 123/124 (see Fig. 9B, above):

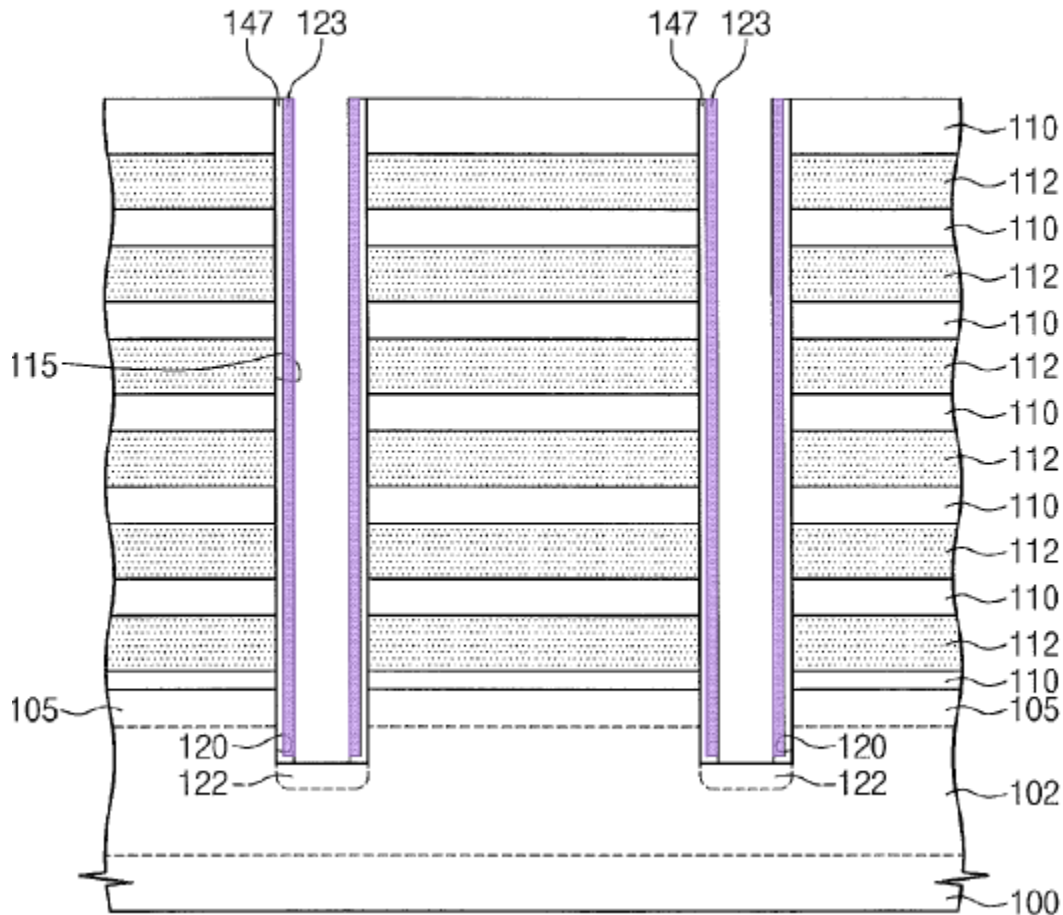
Fig. 8A



Ex. 1004 (Lee '255), Fig. 8A, [0099]-[0100].

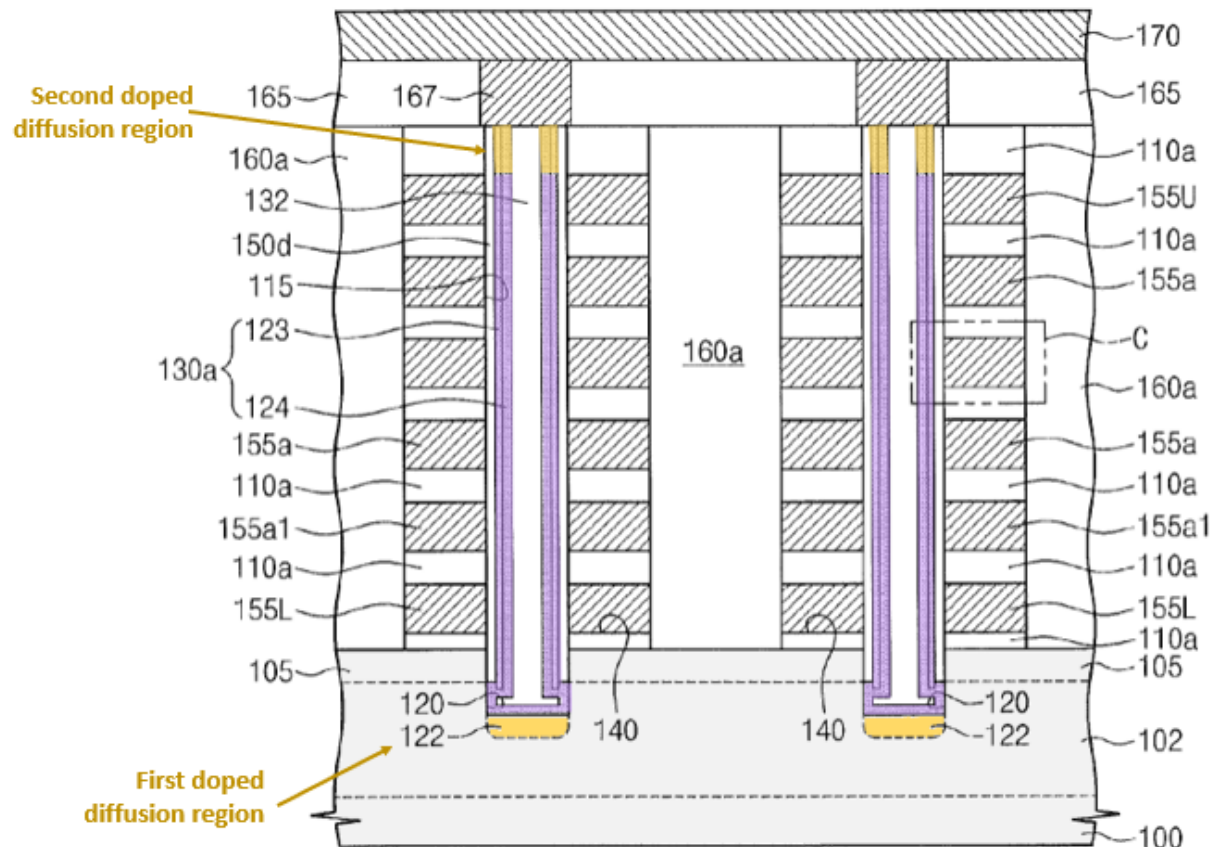
239. The portion of the semiconductor layer formed over the top surface is later removed by etching, as shown in Fig. 8B.

Fig. 8B



Ex. 1004 (Lee '255), Fig. 8B, [0099]-[0100].

240. Second, Lee '255 teaches that its deposited semiconductor material *include[es] a second doped diffusion region* because the first and second semiconductor layers 123 and 124 configure (after processing) a vertical active pattern 130a with second diffusion regions for the reasons set forth in claim 2. *See* claim 2, above.



Ex. 1004 (Lee '255), Fig. 4A.

241. Third, Lee '255 teaches: (i) vertical channels 130/130a with drain regions formed therein (*second doped diffusion region*) extending between the drain region to high concentration region 122 (the *first doped diffusion region*) as set forth in limitation [1a2]; and (ii) that *the vertical channel electrically couples the first doped diffusion region to the second doped diffusion region* for the reasons set forth in claim 2.

5. The method of claim 1, wherein the blocking dielectric layer includes a high K dielectric.

20. The method of claim 19, wherein the blocking dielectric layer includes a high K dielectric.

242. I understand that claim 5 depends from claim 1 and therefore has all of the requirements of claim 1. I understand that claim 20 depends from claims 1, 14, and 19 and therefore has all of the requirements of those claims.

243. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claim 1.

244. As I explain below, it is my opinion that Lee '255 and Lee '961 teach the additional limitations of claims 14 and 19.

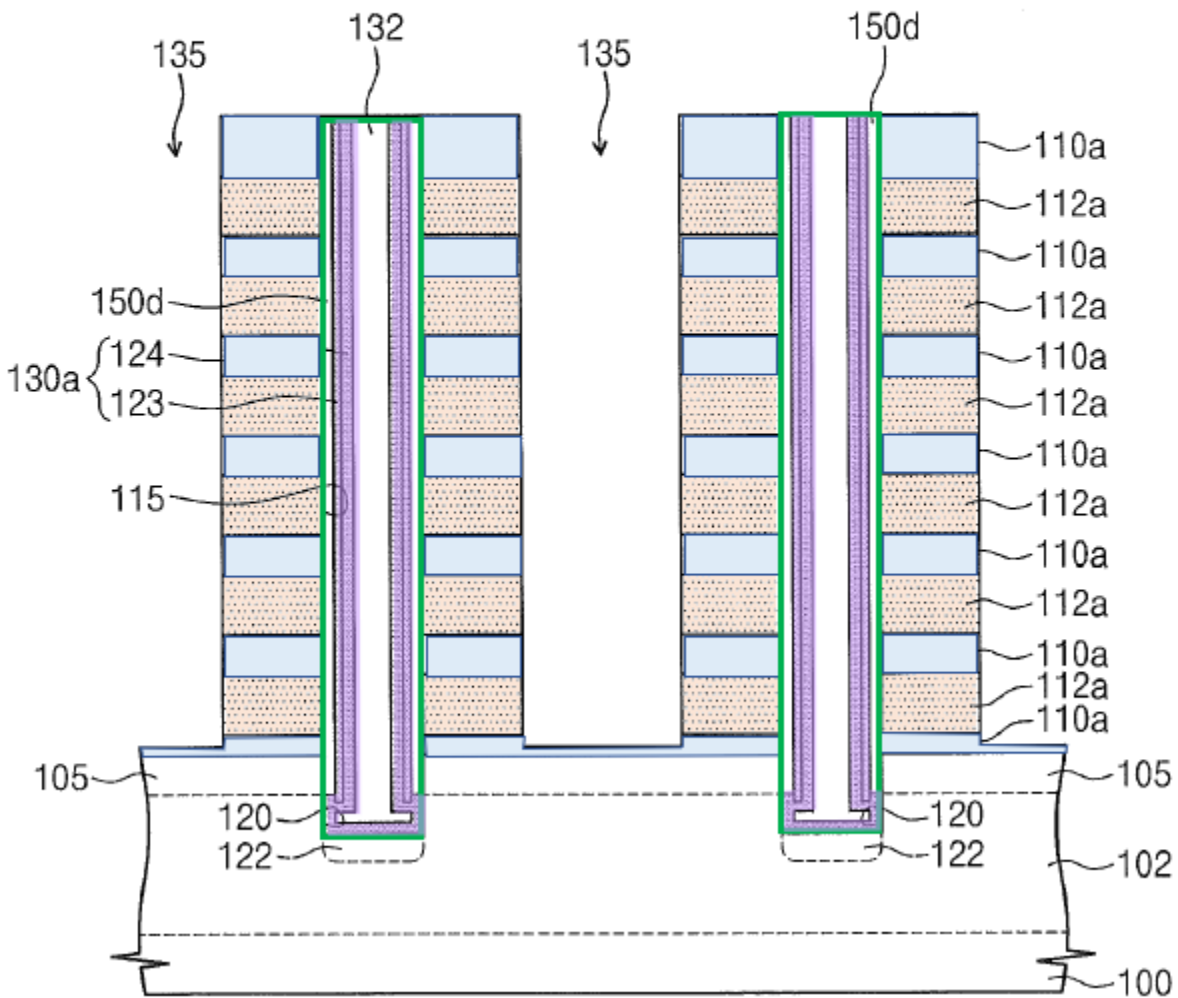
245. The additional limitations of claims 5 and 20 are the same as those of claim 36. As a result, it is my opinion that Lee '255 and Lee '961 teach the additional limitations of claims 5 and 20 for the same reasons set forth in connection with claim 36, above.

9. The method of claim 1, further comprising the step of etching the sacrificial layer to form a second opening.

10. The method of claim 9, further comprising the step of depositing a gate electrode in the second opening.

246. I understand that claim 9 depends from claim 1 and therefore has all of the requirements of claim 1. I understand that claim 10 depends from claims 1 and 9 and therefore has all of the requirements of those claims. As I have explained

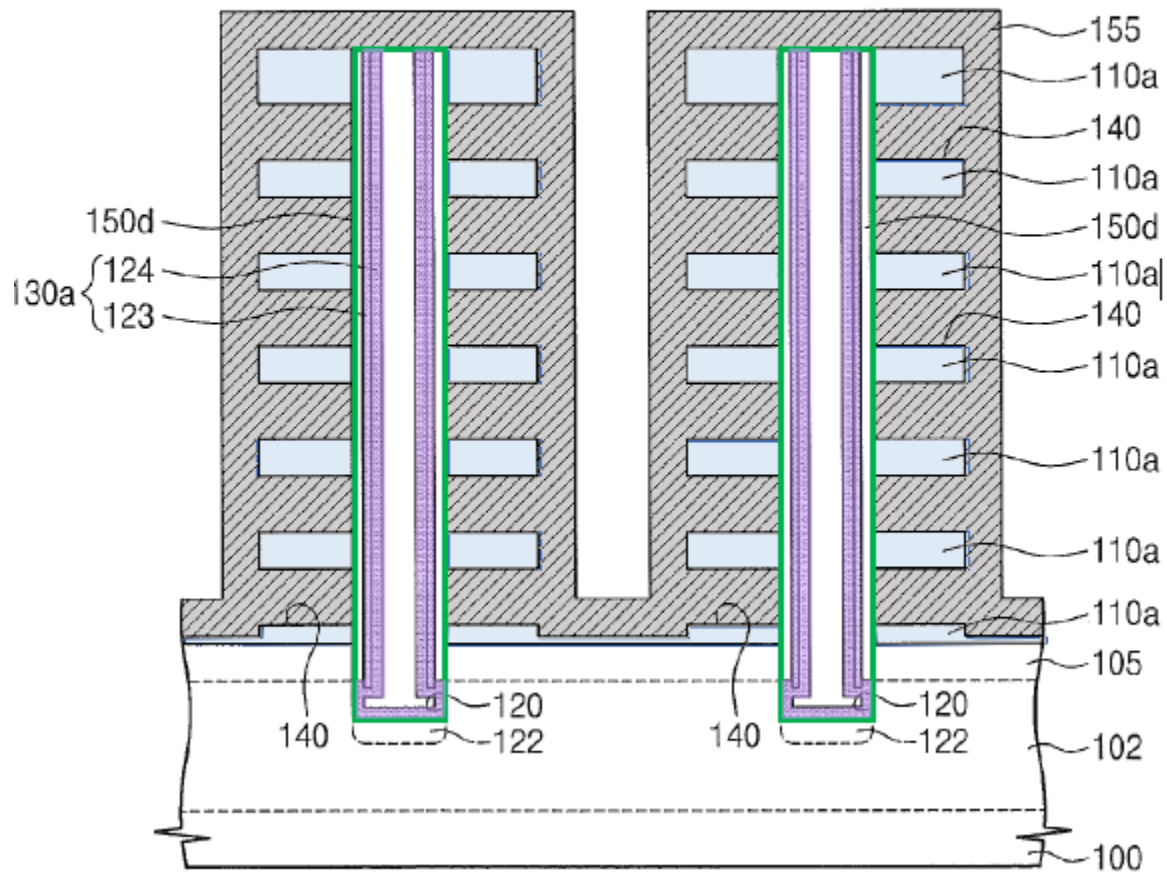
Fig. 9B



Ex. 1004 (Lee '255), Fig. 9B, [0106].

249. Next, in Fig. 9C, Lee '255 teaches that “empty regions 140 may be formed by removing the sacrificial patterns 112a” and the empty regions 140 are then filled with gate conductive layer 155 (gray):

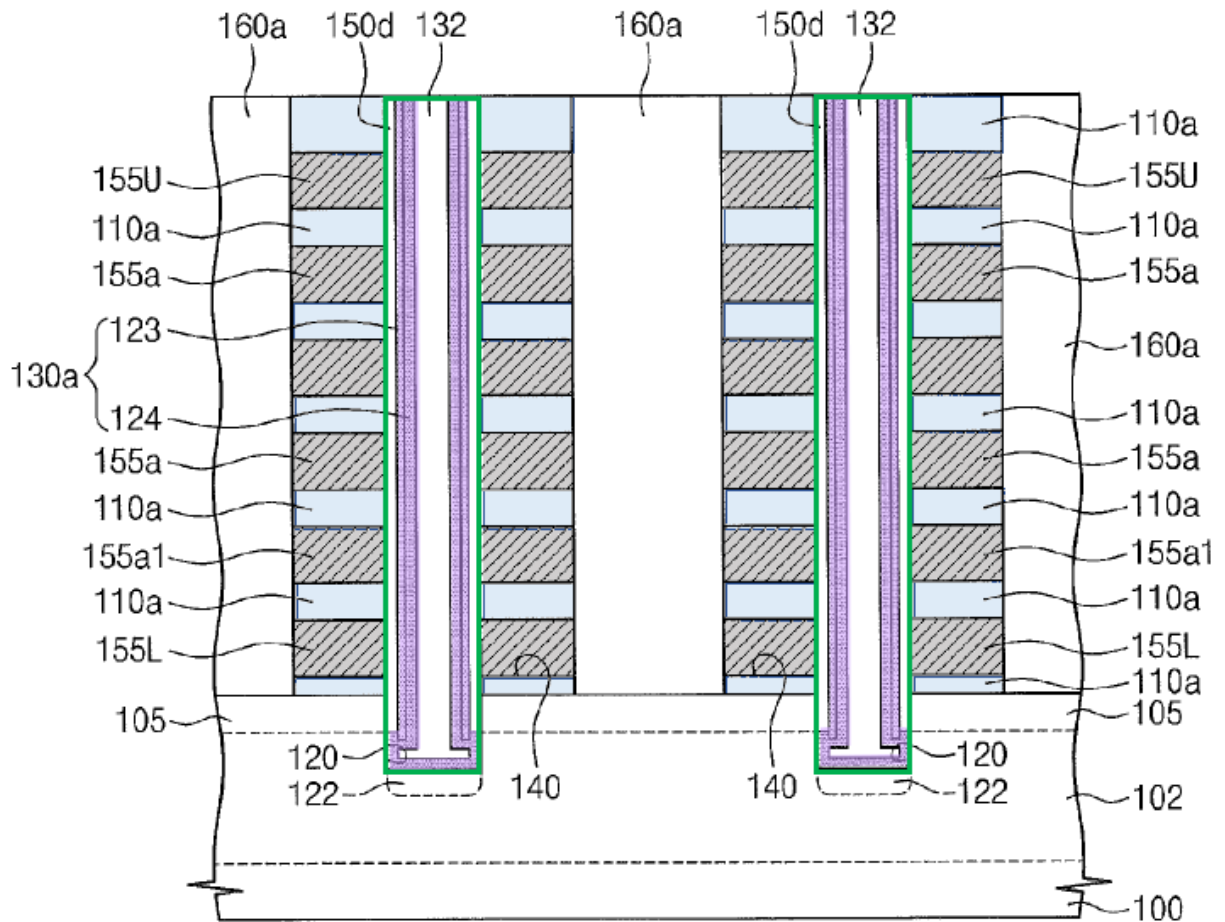
Fig. 9C



Ex. 1004 (Lee '255), Fig. 9C, [0107].

250. Finally, in Fig. 9D, device isolation pattern 160a is formed:

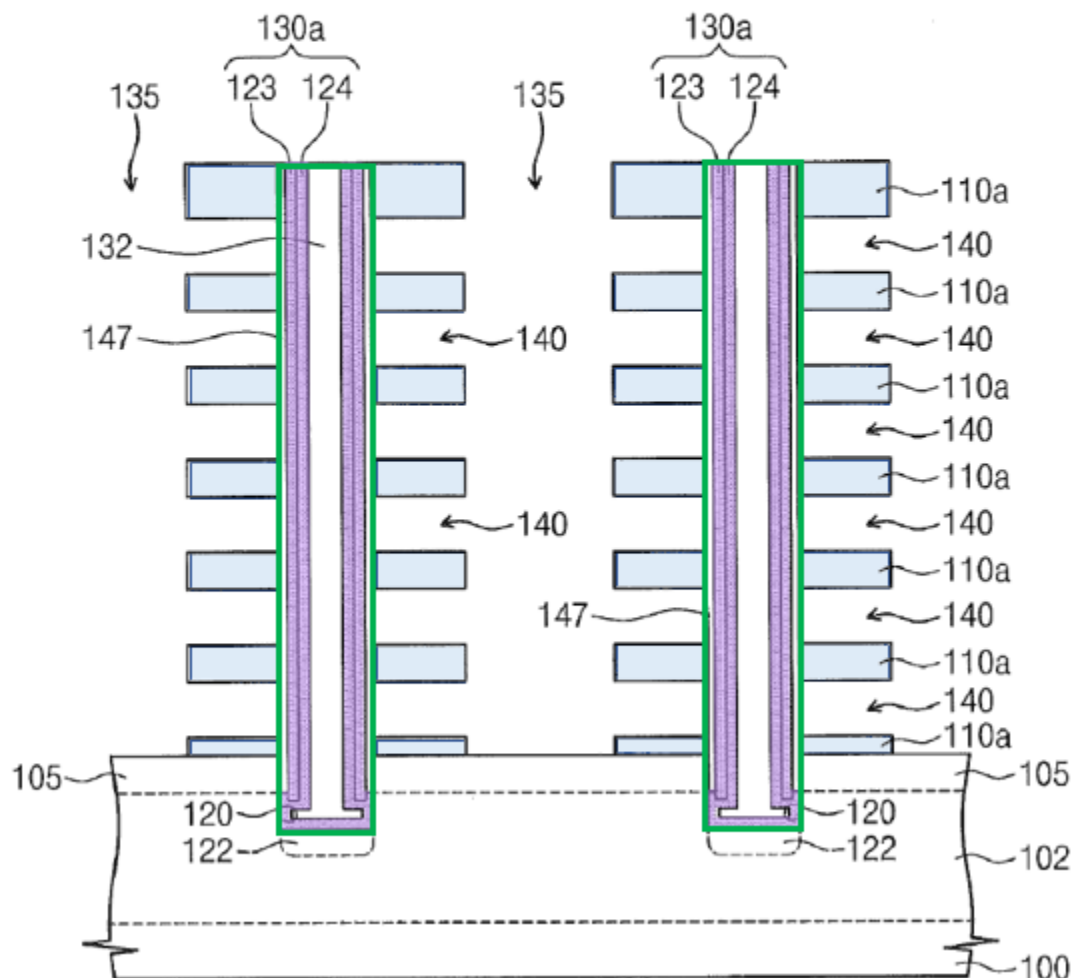
Fig. 9D



Ex. 1004 (Lee '255), Fig. 9D, [0108].

251. While the process portrayed in Figs. 9A-9D teaches that “empty regions 140” are created by removal of the sacrificial patterns 112a and are then filled by “gate conductive layer 155,” the figures do not show empty regions 140 in an unfilled state. Fig. 8E (reproduced below) shows, in a similar process, empty regions 140 in an unfilled state after sacrificial patterns 112a are removed.

Fig. 8E



Ex. 1004 (Lee '255), Fig. 8E, [0103] (“[t]he empty regions 140 may be formed by removing the sacrificial patterns 112. At this point, the empty regions 140 may expose some portions of the first sub-layer 147, respectively.”)

252. In view of the above, Lee '255 teaches *the step of etching the sacrificial layer to form a second opening* because Lee '255 teaches etching away the sacrificial layers 112 to form empty regions 140. Ex. 1004 (Lee '255), Figs. 8E,

9C, [0106]. Lee '255 further teaches *the step of depositing a gate electrode in the second opening* because Lee '255 teaches filling of empty regions 140 with gate conductive layers 155. *Id.*, Figs. 9C, 9D, [0107].

11. The method of claim 10, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.
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253. I understand that claim 11 depends from claims 1, 9, and 10. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 1, 9, and 10.

254. The additional limitations of claim 11 are identical to the additional limitations of claim 45, which I addressed above. As such, claim 11 is obvious based on the teachings of Lee '255 and Lee '961 for the same reasons set forth above in connection with claim 45.

12. The method of claim 10, wherein the deposited gate electrode is a high work function gate electrode.

255. I understand that claim 12 depends from claims 1, 9, and 10. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 1, 9, and 10.

256. The additional limitations of claim 12 are identical to the additional limitations of claim 37, which I addressed above. As such, claim 12 is obvious based on the teachings of Lee '255 and Lee '961 for the same reasons set forth above in connection with claim 37.

14. The method of claim 1, wherein the vertical channel formed includes an annular region.

19. The method of claim 14, wherein the blocking dielectric layer is formed in a substantially annular shape.

21. The method of claim 19, wherein the multi-layer charge storing region is formed in a substantially annular shape.

22. The method of claim 21, wherein the tunnel dielectric layers is formed in a substantially annular shape.

257. I understand that claim 14 depends from claim 1. I understand that claim 19 depends from claims 1 and 14. I understand that claim 21 depends from claims 1, 14, and 19. I understand that claim 22 depends from claims 1, 14, 19, and 21. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claim 1. It is further my opinion that the combination of Lee '255 and Lee '961 teaches the additional limitations of claims 14, 19, 21, and 22.

258. Claims 14, 19, 21, and 22 are each directed to elements of the memory device having an *annular* shape—the vertical channel (claim 14), the blocking dielectric layer (claim 19), the multi-layer charge storage region (claim 21), and the tunnel dielectric layer (claim 22).

259. As I have explained above in connection with Limitations [35b] – [35d], Lee '255 teaches that its vertical channel, blocking dielectric layer, multi-layer charge storing region, and tunnel dielectric layer are annularly shaped. In my

opinion, claims 14, 19, 21, and 22 are obvious for the same reasons set forth above in connection with in limitations [35b]-[35e].

15. The method of claim 14, wherein at least a portion of the vertical channel is formed of polysilicon.

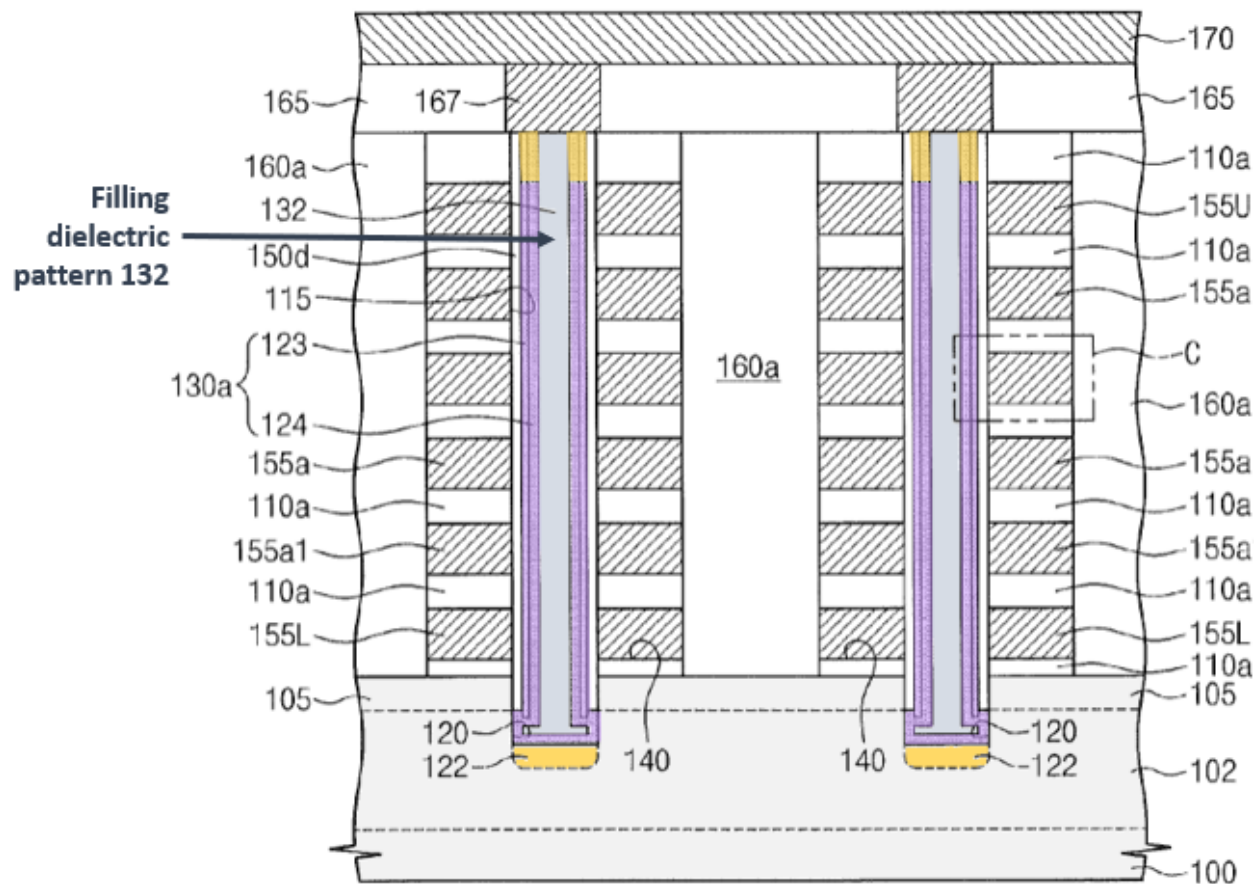
16. The method of claim 14, wherein the vertical channel formed includes a layer of semiconductor material surrounding a cylinder of filler material.

17. The method of claim 14, wherein the vertical channel formed includes an outer layer of semiconductor material.

18. The method of claim 17, wherein the outer layer of semiconductor material is formed of polysilicon.

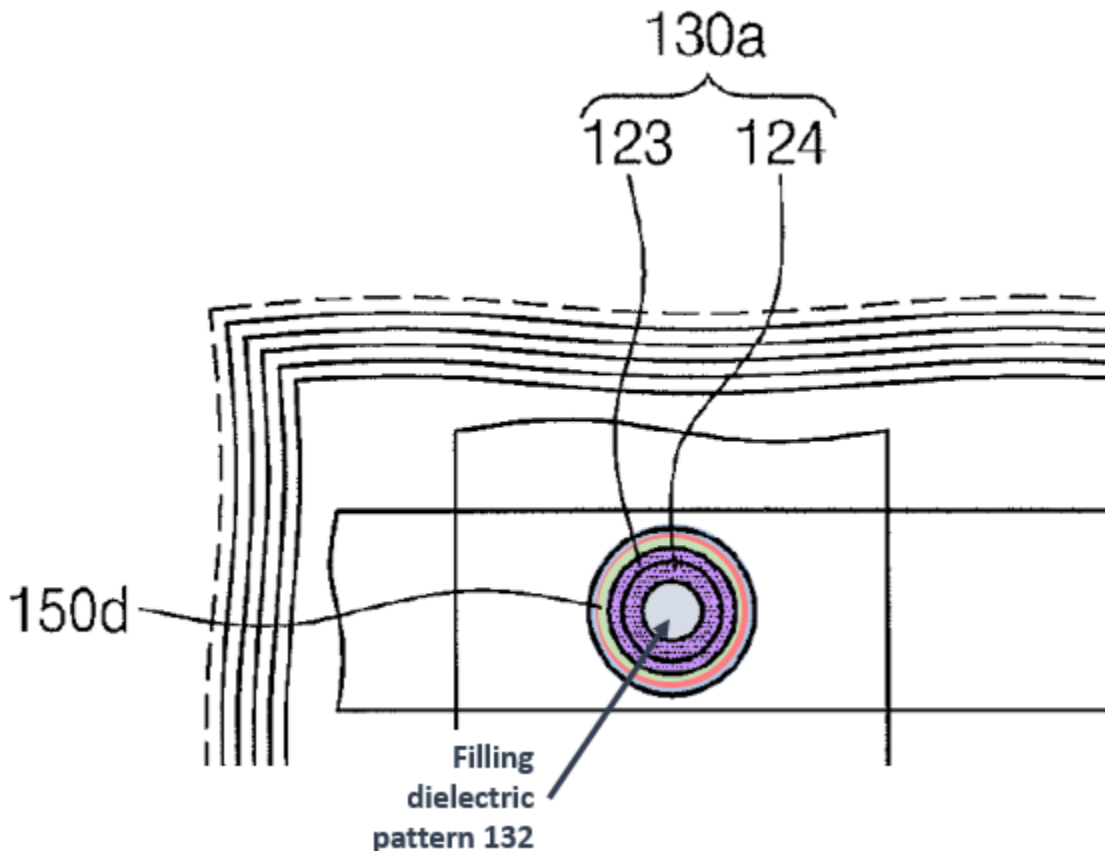
260. I understand that claims 15, 16, and 17 each depend from claims 1 and 14. I also understand that claim 18 depends from claims 1, 14, and 17. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 1 and 14. It is further my opinion that the combination of Lee '255 and Lee '961 teaches the additional limitations of claims 15, 16, 17, and 18. In particular, Lee '255 teaches the additional limitations of claims 15, 16, 17, and 18 because Lee '255 teaches that: (i) "the vertical active pattern 130 may have a hollow pipe shape ... [and] [t]he inside of the vertical active pattern 130 may be filled with a filling dielectric pattern 132 (Ex. 1004 (Lee '255), [0054], Fig. 4A); and (ii) vertical active pattern 130/130a may be comprised of a semiconductor material, such as silicon, that has "a poly-crystalline state." Ex. 1004 (Lee '255), [0062], [0114] (stating that active patterns may

include silicon). The cylinder of filler material (filling dielectric pattern 132) is depicted in figure 4A:



Ex. 1004 (Lee '255), Fig. 4A.

261. As I explained in connection with limitation [35b]-[35e], the vertical active pattern 130/130a and surrounding gate dielectric layer 150d of Lee '255 has the shape of a pipe. I have annotated an excerpt from figure 5A to illustrate where a POSITA would have understood the filling dielectric pattern 132 to be positioned from a top view of the device:



See Ex. 1004 (Lee '255), Fig. 5A; see also Fig. 5B, [0075].

262. For the reasons set forth above, it is my opinion that Lee '255 teaches *a portion of the vertical channel* (active vertical pattern 130/130a) *is formed of polysilicon* (poly-crystalline silicon) and *surrounding a cylinder of filler material* (filling dielectric pattern 132). Lee further teaches that *the vertical channel* (active vertical pattern 130/130a) may include *an outer layer of semiconductor material* (semiconductor pattern 123) that is *formed of polysilicon* (poly-crystalline silicon).

4. Independent Claim 23

[23pre]	A method comprising:
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263. This limitation is the same as limitation [1pre] and is obvious for the reasons discussed for limitation [1pre].

[23a1]	forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;
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264. This limitation is the same as limitation [1a1] and is obvious for the reasons discussed for that limitation.

[23a2]	forming an opening extending through the stack of layers towards the substrate;
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265. This Limitation is similar to Limitation [1a2]. In particular, Limitation [23a2] requires that the opening extend *through the stack of layers towards the substrate*, while Limitation [1a2] more specifically requires that the opening extend *through the stack of layers to a first doped diffusion region formed on the substrate*. In either case, the opening must extend through the stack of layers towards the substrate. As such, it is my opinion that Lee '255 and Lee '961 teach limitation [23a2] for the same reasons set forth above in connection with limitation [1a2], which I incorporate here by reference.

[23b]	forming on sidewalls of the opening an annular shaped blocking dielectric layer;
[23c]	forming on an inside sidewall of the blocking dielectric layer an annular shaped multi-layer charge storing region;
[23d]	forming on an inside sidewall of the multi-layer charge storing region an annular shaped tunnel dielectric layer; and
[23e]	forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layers.

266. These Limitations of claim 23 are almost identical to Limitations [1b]-[1e] of claim 1, except that limitations [23b] – [23e] recite that each element has an *annular shape*. Limitations [23b] – [23e] are obvious for the same reasons set forth in connection with limitations [1b]-[1e] and limitations [35b]-[35e], which explain why Lee '255 and Lee '961 teach that the blocking dielectric layer, multi-layer charge storage region, tunnel dielectric layer, and vertical channel each have an annular shape.

28. The method of claim 23, further comprising the step of etching the sacrificial layer to form a second opening.

267. I understand that claim 28 depends from claim 23. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claim 23.

268. The additional limitations of claim 28 are the same as the additional limitations of claim 9. In my opinion, claim 28 is obvious based on the teachings

of Lee '255 and Lee '961 for the same reasons I set forth in connection with claim 9.

29. The method of claim 28, further comprising the step of depositing a gate electrode in the second opening.

269. I understand that claim 29 depends from claims 23 and 28. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 23 and 28.

270. The additional limitations of claim 29 are the same as the additional limitations of claim 10. In my opinion, claim 29 is obvious based on the teachings of Lee '255 and Lee '961 for the same reasons I set forth in connection with claim 10.

30. The method of claim 29, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.

271. I understand that claim 30 depends from claims 23, 28, and 29. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 23, 28 and 29.

272. The additional limitations of claim 30 are the same as the additional limitations of claim 11. In my opinion, claim 30 is obvious based on the teachings of Lee '255 and Lee '961 for the same reasons I set forth in connection with claim 11.

31. The method of claim 29, wherein the deposited gate electrode is a high work function gate electrode.

273. I understand that claim 31 depends from claims 23, 28, and 29. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 23, 28 and 29.

274. The additional limitations of claim 31 are the same as the additional limitations of claim 37. In my opinion, claim 31 is obvious based on the teachings of Lee '255 and Lee '961 for the same reasons I set forth in connection with claim 37.

32. The method of claim 29, wherein the blocking dielectric layer includes a high K dielectric.

275. I understand that claim 32 depends from claims 23, 28, and 29. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 23, 28 and 29.

276. The additional limitations of claim 32 are the same as the additional limitations of claim 36. In my opinion, claim 32 is obvious based on the teachings of Lee '255 and Lee '961 for the same reasons I set forth in connection with claim 36.

33. The method of claim 32, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.
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277. I understand that claim 33 depends from claims 23, 28, 29, and 32. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 23, 28, 29, and 32.

278. The additional limitations of claim 33 are similar to the additional limitations of claim 45. In my opinion, claim 33 is obvious based on the teachings of Lee '255 and Lee '961 for the same reasons I set forth in connection with claim 45.

B. Ground 2: Obviousness over Lee '255, Lee '961, and Fujiwara

279. It is my opinion that claims 6-8, 25-27, 34, 38-41 of the '365 patent are rendered obvious based on the teachings of Lee '255, Lee '961, and Fujiwara.

280. I have already reviewed the teachings of Lee '255 and Lee '961 above and explained why a POSITA would have been motivated to modify the charge storage layer of Lee '255 based on Lee 961's teachings regarding a multilayer charge storage layer configuration that improves data retention of nonvolatile memory devices.

281. Fujiwara, like Lee '255 and Lee '961, relates to SONOS charge trapping-type nonvolatile memory devices. Ex. 1006 (Fujiwara), [0003] ("The present invention relates to a nonvolatile memory device provided with a metal-

oxide-nitride-oxide semiconductor (MONOS) type”).⁶ Fujiwara, like Lee ’961, teaches that retention in charge-trapping type memory devices can be improved by using the multilayer charge storage layer configuration shown in its figure 21. Ex. 1006 (Fujiwara), [0197], [0205]. In particular, Fujiwara teaches that using an oxygen-rich lower nitride layer and an oxygen-lean upper nitride layer promotes charge retention. Ex. 1006 (Fujiwara), [0197]-[0218], Figs. 21, 22.

282. It is my opinion that the combination of Lee ’255, Lee ’961, and Fujiwara teaches each and every limitation of claims 6-8, 25-27, 34, 38-41 of the ’365 patent for the reasons discussed in detail below. Further, it is my opinion that a POSITA would have been motivated to further modify the combination of Lee ’255 and Lee ’961 in view of Fujiwara’s teachings concerning optimized oxygen concentrations when using multiple nitride layers in a charge-trapping nonvolatile memory device. A POSITA also would have expected success in applying the teachings of Fujiwara to further modify the combination of Lee ’255 and Lee ’961. I have provided further details of my motivation to combine and expectation of success analysis in connection with specific claim limitations below.

⁶ A POSITA would have understood that “MONOS” (Metal-Oxide-Nitride-Oxide-Silicon) and “SONOS” (Silicon-Oxide-Nitride-Oxide-Silicon) are equivalent types of metal-oxide-semiconductor field effect transistors (MOSFET) with the primary distinction being the material used for the gate electrode (metal versus silicon). *See, e.g.*, Ex. 1007 (Lukasiak), p. 6.

283. As I have already explained above, the combination of Lee '255 and Lee '961 differs from the prior art the Examiner considered during prosecution of the '365 patent. That analysis also applies to the further combination of Lee '255 and Lee '961 with Fujiwara.

6. The method of claim 1, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.

25. The method of claim 23, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.

34. The method of claim 33 wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.

38. The semiconductor memory device of claim 35, wherein the multi-layer charge storing region includes a first oxygen-lean nitride layer and a second oxygen-rich nitride layer.

284. I understand that claim 6 depends from claim 1 of the '365 patent. I understand that claim 25 depends from claim 23 of the '365 patent. I understand that claim 34 depends from claims 23, 28, 29, 32, and 33 of the '365 patent. I understand that claim 38 depends from claim 35 of the '365 patent. As I have explained above, it is my opinion that the combination of Lee '255 and Lee '961 teaches each and every limitation of claims 1, 23, 28, 29, 32, 33, and 35 of the '35 patent and I incorporate that analysis herein.

285. It is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches the additional limitations of claims 6, 25, 34, and 38.

286. The combination of Lee '255 and Lee '961 teaches a *multi-layer charge storing region* for the reasons set forth in limitation [35d], which I incorporate herein. By way of summary, Lee '961 teaches a multilayer charge trap layer 202A (*multi-layer charge storing region*) that includes silicon nitride first trap layer 26, oxide interlayer 27, and silicon nitride second trap layer 28. Ex. 1005 (Lee '961), Figures 2a, 2b, [0020]. As set forth above, the goal of Lee '961's multilayer charge storage region is to improve charge retention by adding additional layers below the single nitride charge trap layer of the prior art. *Id.*, [0010], [0032][0033] (teaching that, as compared to the prior art SONOS construction, "applying a multilayered charge trap layer (202) may disperse the electric field as the charge is separated by a plurality of trap layers and weaken the driving force by which the charge is spread in the lateral direction"). A POSITA would have been motivated to modify the charge storage layer of Lee '255 to incorporate a multilayer charge storage layer based on the teachings of Lee '961. *See* analysis of limitation [35d], above.

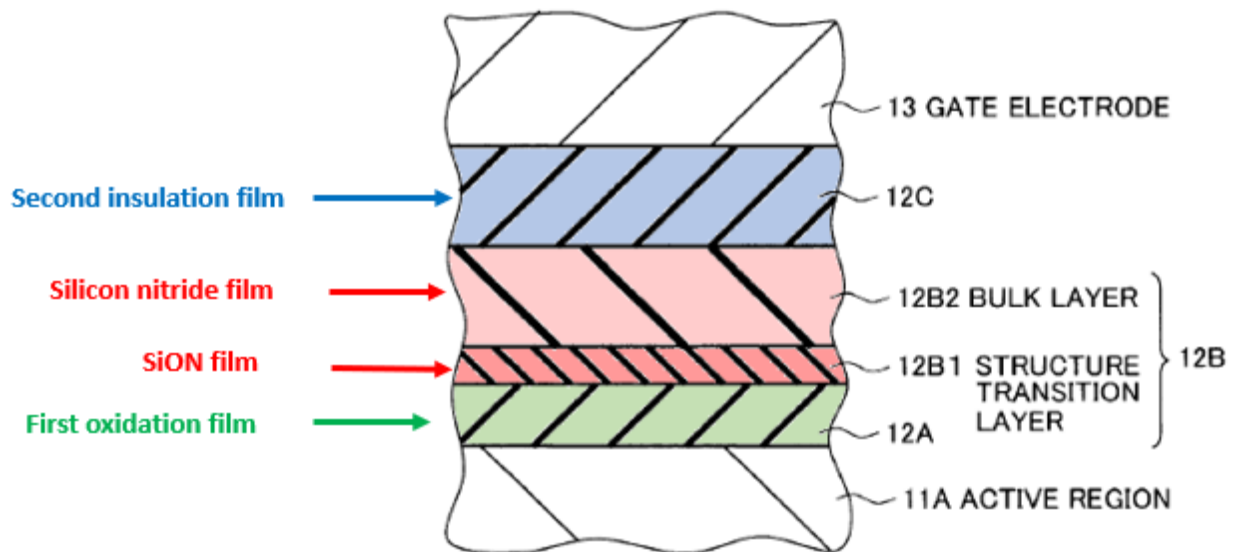
287. A POSITA would have considered it obvious prior to July 2012 to modify the multi-layer charge storage region of Lee '255 / Lee '961 to make nitride layer 26 of Lee '961 oxygen-lean and nitride layer 28 of Lee '961 oxygen-rich to further improve charge retention, as this was a well-known design strategy to achieve those goals. *See* Part III.C.4-5.

288. In particular, a POSITA would have considered it obvious to provide such an arrangement based on the teachings of Fujiwara, which teaches, like Lee '961, that using a multilayer charge storage layer configuration improves charge retention. Ex. 1006 (Fujiwara), [0197].

289. Fujiwara teaches a multi-layer charge storing region that *includes an oxygen-lean nitride layer and an oxygen-rich nitride layer* because Fujiwara teaches a charge trapping structure that includes two nitride layers—a silicon oxynitride (SiON) “transition layer” 12B1 (*oxygen-rich nitride layer*) and a silicon nitride “bulk layer” 12B2 (*an oxygen-lean nitride layer*). *Id.*, Fig. 2, Fig. 21, [0074], [0198]-[0201], [0212], [0215]-[0217].

290. This arrangement is shown in annotated Figure 21 below, where the silicon oxynitride (SiON) “transition layer” 12B1 (*oxygen-rich nitride layer*) is shaded in darker red and the silicon nitride “bulk layer” 12B2 (*an oxygen-lean nitride layer*) is shaded in lighter red.

FIG. 21



Ex. 1006 (Fujiwara), Fig. 21; *see also id.*, Fig. 2, [0212], [0215], [0218].

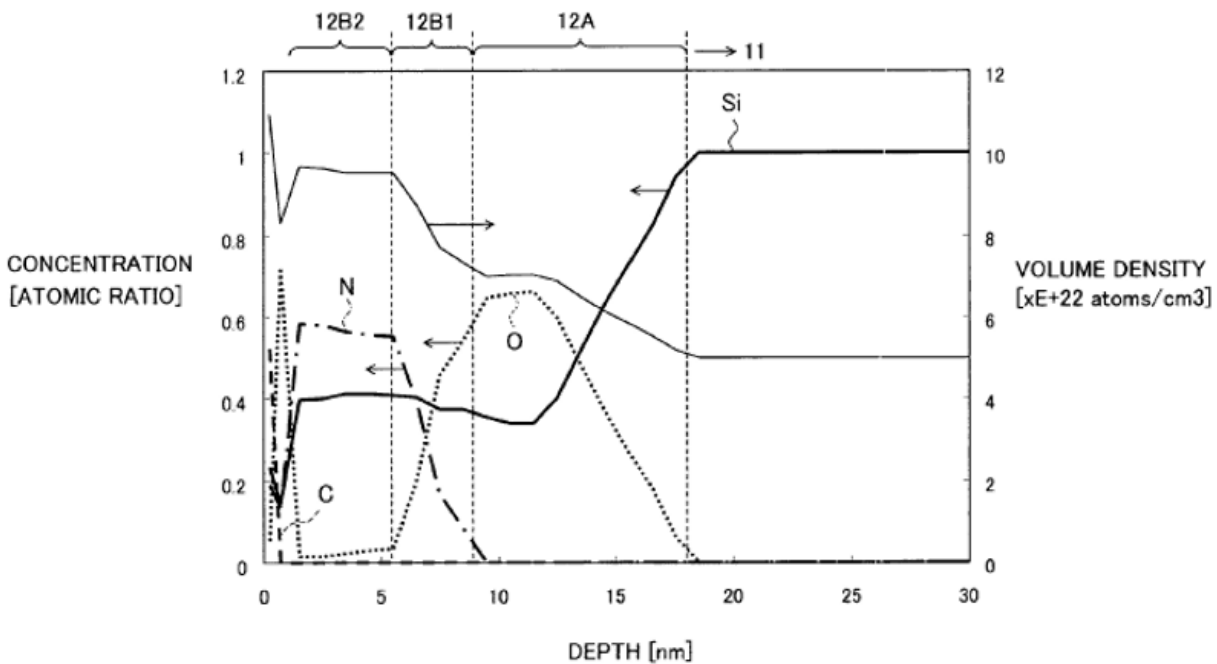
291. A POSITA would have understood that “transition layer (SiON) film” 12B1 is an *oxygen-rich nitride layer* and nitride “bulk layer” 12B2 is an *oxygen-lean nitride layer*.

292. Indeed, Fujiwara characterizes the upper (oxygen-lean) nitride layer (12B2) as the “main structure of the charge storage layer.” Ex. 1006 (Fujiwara), [0215], [0199]. The lower (oxygen-rich) nitride layer (12B1) is a silicon oxynitride transition layer chosen because it is “low in the charge trap and high in the data retention characteristic.” *Id.*, [0205], [0201], [0210]. These teachings mirror those of the ’365 patent, which states that the upper, oxygen-lean nitride is designed to trap charges, while the lower, oxygen-rich nitride is substantially trap-

free and designed to reduce charge loss. *See* Ex. 1001 ('365 patent), 6:7-14; 8:27-30 (“lower, substantially trap free oxynitride layer 318B”); *see also id.*, 6:3-10 (same); 10:16-18 (“It has been found that an oxygen-rich, first nitride layer 422a decreases the charge loss rate after programming and after erase.”); 13:45-57 (the oxygen-rich layer is designed “to reduce the number of charge traps therein”). These properties of oxygen-rich and oxygen-lean nitride layers were also widely known by POSITAs prior to July 2012. *See* Part III.C.4-6.

293. Beyond the foregoing, Fujiwara also explicitly teaches that the upper nitride layer (12B2) is *oxygen-lean* and the lower nitride layer (12B1) is *oxygen-rich*, based on the disclosed atomic composition profiles of those layers depicted in figure 22:

FIG. 22



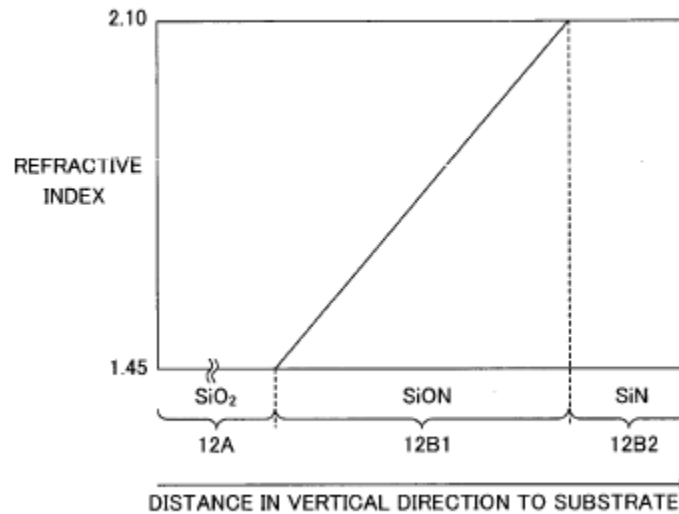
Ex. 1006 (Fujiwara), Fig. 22, [0200].⁷

294. As reflected above, layer 12B1 (SiON transition layer) is an *oxygen-rich nitride layer* because it peaks at approximately 50 atomic % oxygen in its interior. Layer 12B2 (Si₃N₄ bulk layer), by contrast, is a silicon-rich, *oxygen-lean nitride layer* because it holds approximately 40 atomic % silicon throughout, with less than approximately 5 atomic % oxygen throughout. With respect to layer 12B1, the oxygen concentration varies across its depth, with oxygen concentrations

⁷ At the left of the graph of figure 22, the oxygen concentration increases. A POSITA would understand that this occurs as the MONOS stack transitions to the top oxide insulating layer. This is also reflected by the brackets at the top of the chart that show where the bulk nitride layer (12B2) ends/transitions.

exceeding about 15% for the vast majority of the layer. While the oxygen concentration drops below 15% as a transition is made from layer 12B1 to 12B2, a POSITA would have recognized this as a common variation during CVD or oxidation processes when one layer (e.g., a SiON layer) transitions to another layer (e.g., a SiN layer). Having an oxygen concentration lower than 15% at the transition from layer 12B1 to layer 12B2 would not alter a POSITA's understanding that layer 12B1 is an *oxygen-rich nitride layer* (SiON film) as a whole. When assessing whether a *nitride layer* is *oxygen-rich*, a POSITA would evaluate the composition across the full layer (e.g., the entire SiON film), not at an isolated interface. In Fujiwara, a vast majority of layer 12B1 (by depth) contains more than 15% oxygen, with portions exceeding 50%. A POSITA would not have required each boundary segment to exceed 15% oxygen, given the well-recognized nature of graded SiON transition films. This conclusion is reinforced by Fujiwara figure 23, which shows the refractive index of 12B1 grading up to about 2.10, which a POSITA would have understood to represent about 60–67 atomic % O. A POSITA would have recognized refractive index as a standard optical proxy for oxygen incorporation in SiON films. Thus, figure 23 independently confirms the same conclusion as figure 22: even with a graded profile, 12B1 is an *oxygen-rich* first nitride layer.

FIG. 23



Ex. 1006 (Fujiwara), Fig. 23.

295. As such, Fujiwara teaches that layer 12B1 is *oxygen-rich* because the percentage of oxygen in layer 12B1 exceeds 15%. *See* Part VII.B (construction of oxygen-rich and oxygen-lean). Similarly, Fujiwara teaches that layer 12B2 is *oxygen-lean* because the percentage of oxygen is less than 5%. *See id.*

296. It is my opinion that a POSITA would have been motivated to further modify the combination of Lee '255 and Lee '961 to apply the teachings of Fujiwara to optimize the oxygen concentrations of the nitride layers of the multi-layer charge-trapping region.

297. It would have been obvious for a POSITA to consult the teachings of Fujiwara in seeking to improve the memory transistor configuration of Lee '255 and Lee '961 because Fujiwara is also directed to improving the configuration of

SONOS-type charge trapping memory transistors such as those taught in Lee '255 and Lee '961. Ex. 1006 (Fujiwara), FIG. 1 (teaching a SONOS stack), [0010]-[0013] (teaching that SONOS retention characteristics need improvement). Fujiwara's teaching of optimizing oxygen concentrations in nitride layers to improve charge retention is complementary to the combination of Lee '961 and Lee '255, which also has the goal of improving data retention. Ex. 1003, ¶297; *compare* Ex. 1005 (Lee '961), [0008], [0010] *with* Ex. 1006 (Fujiwara), [0197], [0205].

298. A POSITA would have been motivated to apply Fujiwara's layer composition teachings to the Lee '255 / Lee '961 charge trapping region to obtain the benefit expressly taught in Fujiwara—to improve the retention characteristic of the charge storage layer of the resultant stack. Ex. 1006 (Fujiwara), [0197] (stating that the oxygen-rich/oxygen-lean embodiment “further improve[s] the charge retention characteristics”). A POSITA would have understood that this combination of Fujiwara with Lee '255 and Lee '961 amounts to applying the teachings of Fujiwara for their intended purpose to improve similar devices in the same way.

299. Further, the benefit of using an oxygen-rich first nitride layer and a silicon-rich, oxygen-lean nitride second layer in a SONOS memory transistor would have been predictable to a POSITA prior to July 2012. In addition to

Fujiwara, many other prior art references show that it was a routine design choice to use an oxygen-rich first nitride layer and a silicon-rich, oxygen-lean second nitride layer to obtain improved charge retention characteristics in both SONNOS and SONONOS configurations. *See, e.g.*, Ex. 1012 (Heo), [0058]-[0068] (teaching that using a bottom oxidized nitride layer with a top nitride layer improves “the data retention properties and/or durability of the non-volatile memory device”); Ex. 1017 (Lai ’676), [0015], [0068]-[0077] (teaching that an NON charge trapping region with an upper silicon nitride layer 16, middle oxide layer 15, and lower silicon oxynitride layer 14 improves retention); Ex. 1011 (Levy), [0025]-[0026] (using an oxygen-rich bottom nitride layer “decrease[s] the charge loss rate after programming and after erase”); Ex. 1013 (Ganguly), Fig. 3, [0048]-[0050] (teaching first nitride layer is up to 50% oxygen and engineered to have a lower charge trap density in order to promote charge retention in the second nitride layer); and Ex. 1021 (Higuchi) [0007], [0133]-[0134], [0141]-[0142] (teaching that an NON charge trapping region with an upper silicon nitride layer 203, middle oxide layer 202d, and lower silicon oxynitride layer 202c improves retention).

Accordingly, applying the teachings of Fujiwara to the Lee ’255/Lee ’961 stack would have amounted to combining prior art elements according to known methods to obtain predictable results.

300. A POSITA also would have expected success in applying Fujiwara's teachings concerning optimized oxygen concentrations to the multi-layer charge-trapping region of Lee '255 / Lee '961 framework the underlying materials, equipment, and process knobs are all mainstream. Even without Fujiwara, Lee '255 and Lee '961 already provide a multi-layer charge trap; Fujiwara merely teaches adjusting the compositions of the layers. Indeed, Lee '961's intermediate oxide layer already suggests a natural location for Fujiwara's oxygen-rich transition film, further confirming the compatibility of the two disclosures. In conventional LPCVD or PECVD reactors that adjustment is routine: the operator varies O₂/N₂ (or N₂O/NH₃) flow, tweaks chamber pressure or RF power, or performs a brief in-situ O₂ anneal. Standard run sheets already relate gas-phase O₂ percentage to the resulting atomic-percent oxygen in SiON, so, for example, setting ~50 at. % O in the 1–2 nm transition layer and $\lesssim$ 5 at. % O in the overlying Si₃N₄ bulk layer is a matter of selecting recipe parameters, not inventing new chemistry. Fujiwara further points out that the transition film remains amorphous, avoiding lattice-mismatch penalties, and that both layers tolerate subsequent high- κ caps and metal gates up to about 750 °C—a thermal window already assumed in Lee '255 and Lee '961. Because the retention improvement scales smoothly with the oxygen gradient, a POSITA would reasonably predict that implementing Fujiwara's teaching of oxygen-rich and oxygen-lean nitride layers in the existing Lee '255 /

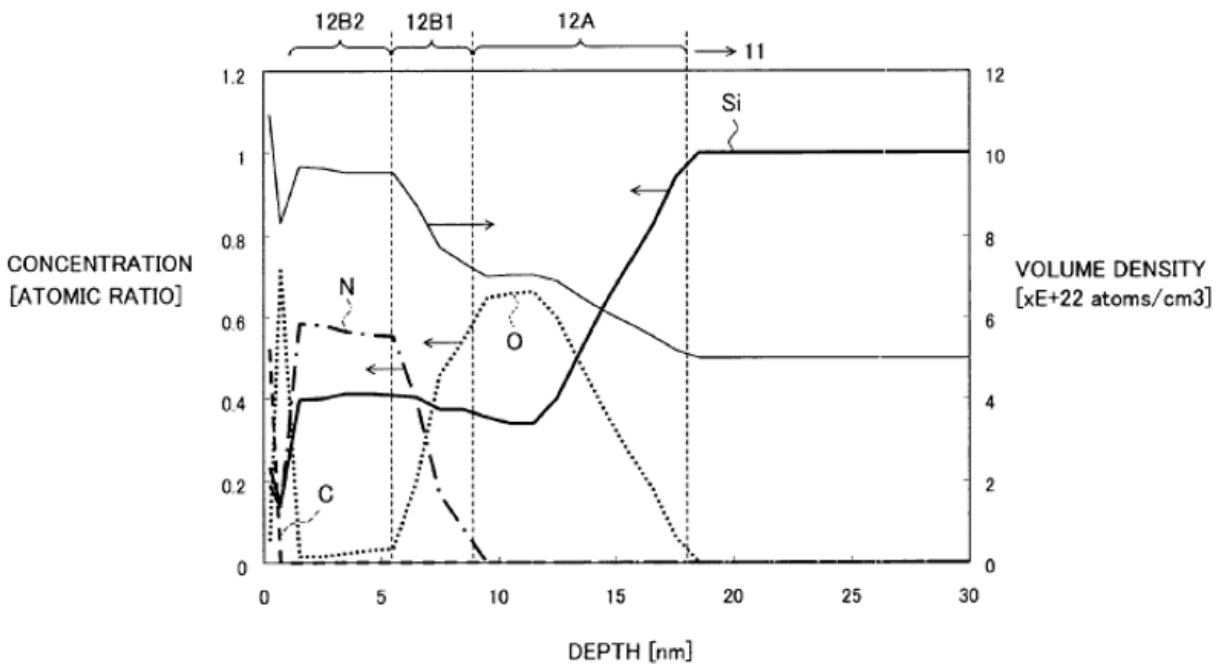
Lee '961 stack framework could be achieved with routine process-tuning and would deliver the same data-retention benefits without introducing new reliability risks. Thus, applying Fujiwara's approach in framework of Lee '255 / Lee '961 would involve routine adjustments to deposition parameters—such as gas flow, chamber pressure, or in-situ oxidation—all using standard tools like LPCVD or PECVD.

39. The semiconductor memory device of claim 38, wherein the first oxygen-lean nitride layer and the second oxygen-rich nitride layer both include silicon, nitrogen and oxygen components.

301. I understand that claim 39 depends from claims 38 and 35. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claims 35 and 38 and I incorporate that analysis herein.

302. It is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches the additional limitations of claim 39 because Fujiwara teaches that both nitride layers 12B2 and 12B1 have silicon, nitrogen, and oxygen components in the concentration profile set forth in Fig. 22 (below).

FIG. 22



Ex. 1006 (Fujiwara), Fig. 22, [0200].

7. The method of claim 6, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.

26. The method of claim 25, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.

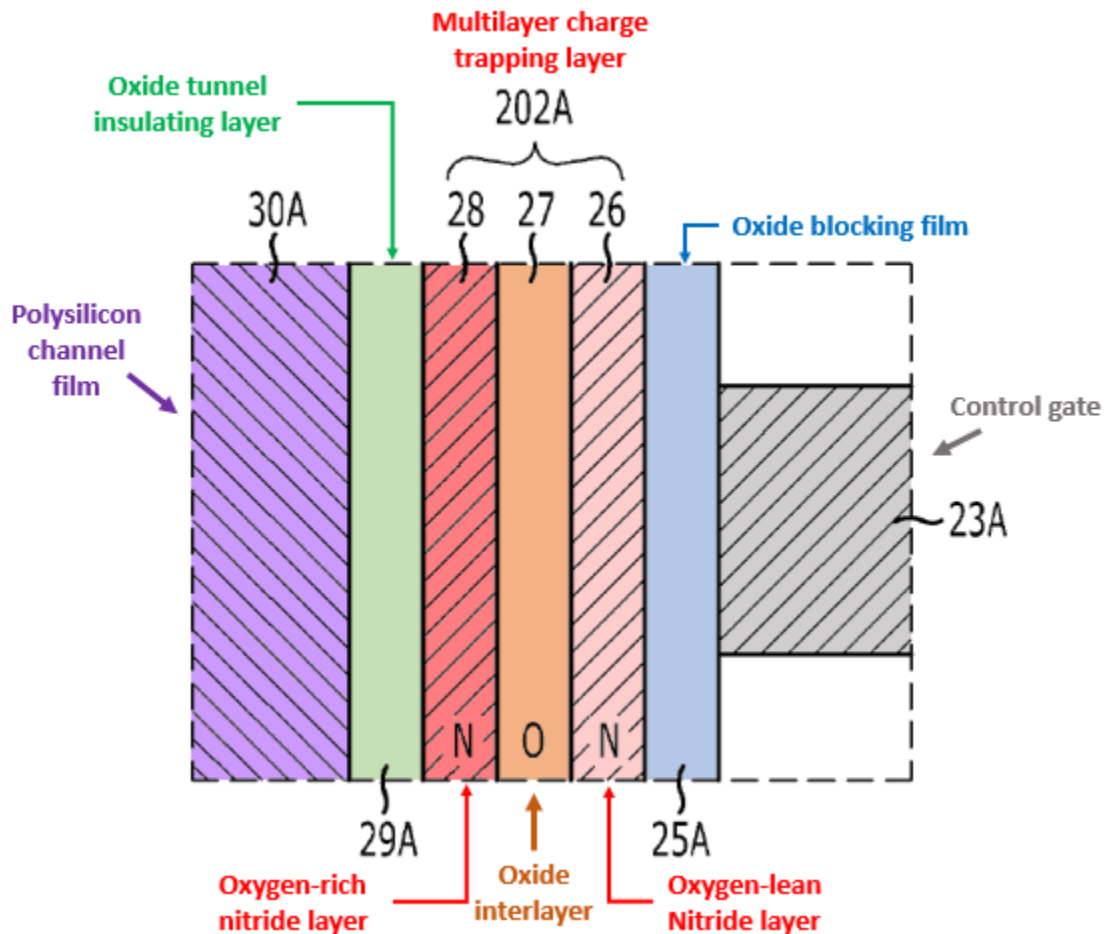
40. The semiconductor memory device of claim 39, wherein the first oxygen-lean nitride layer is formed on an inside sidewall of the blocking dielectric layer and wherein the second oxygen-rich nitride layer is formed on the inside sidewall of the first oxygen-lean nitride layer.

303. I understand that claim 7 depends on claims 1 and 6; claim 26 depends on claims 23 and 25; and claim 40 depends on claims 35, 38, and 39. As I

have explained above, it is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claims 1, 6, 23, 25, 35, 38, and 39, and I incorporate that analysis herein.

304. It is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches the additional limitations of claims 7, 26, and 40.

305. Fujiwara teaches that (i) the oxygen-rich nitride layer is positioned near the tunneling layer; and (ii) the oxygen-lean nitride layer is positioned near the blocking layer. Ex. 1006 (Fujiwara), Figs. 21, 22; *see also id.*, [0212], [0215], [0218]. A POSITA would have found it obvious to retain the same relative positioning when applying the teachings of Fujiwara to further modify the combination of Lee '255 and Lee '961. As modified based on Fujiwara, the oxygen-rich and oxygen-lean layers of the multilayer charge trapping layer would be arranged as follows:



Ex. 1005 (Lee '961), Fig. 2b (as modified based on Fujiwara).

306. As reflected above, the resultant *[first] oxygen-lean nitride layer* (layer 26) is *formed on the inside sidewall of the blocking dielectric layer*. Meanwhile, the *[second] oxygen-rich nitride layer* (layer 28) is *formed on the inside sidewall of the oxygen-lean nitride layer*, but with an intermediate oxide layer (layer 27). As set forth in the claim construction section, above, a POSITA would have understood that, even though there is an intervening oxide interlayer 27 between nitride first trap layer 26 and nitride second trap layer 28, layer 28 is still understood to be “formed on” the sidewall of layer 26.

41. The semiconductor memory device of claim 40, wherein the blocking dielectric layer includes a high K dielectric.

307. I understand that claim 41 depends from claims 35, 38, 39, and 40. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claims 35, 38, 39, and 40, and I incorporate that analysis herein.

308. The additional limitations of claim 41 are the same as the additional limitations of claim 5. In my opinion, claim 41 is obvious based on the teachings of Lee '255 and Lee '961 for the same reasons I set forth in connection with claim 5.

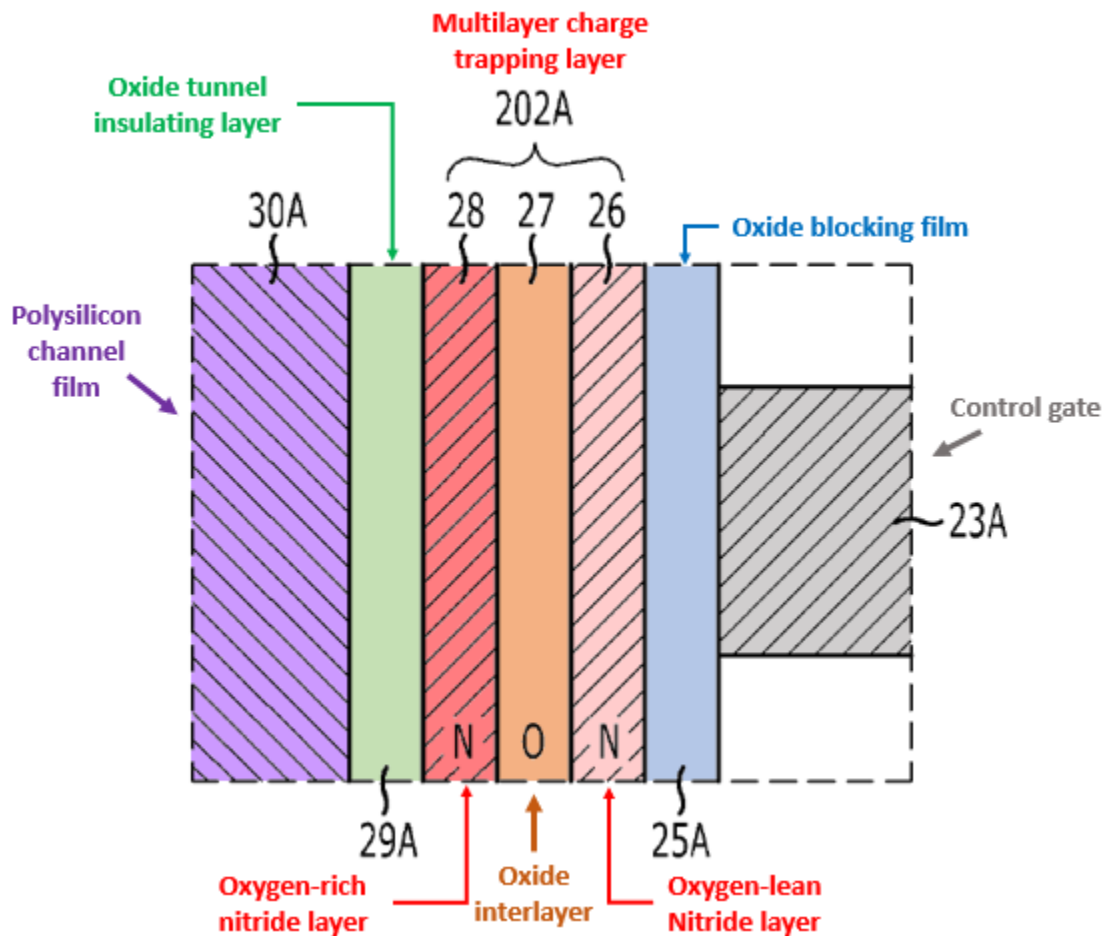
8. The method of claim 6, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.

27. The method of claim 26, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.

309. I understand that claim 8 depends from claims 1 and 6. I understand that claim 27 depends from claims 23, 25, and 26. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claims 1, 6, 23, 25, and 26, and I incorporate that analysis herein.

310. It is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches the additional limitations of claims 8 and 27 because Lee '961 teaches the arrangement of oxide interlayer 27 (*anti-tunneling layer*) *between* its

nitride first trap layer 26 (*oxygen-lean nitride layer*) and nitride second trap layer 28 (*oxygen-rich nitride layer*), as shown in the annotated version of figure 2b below:



Ex. 1005 (Lee '961), Fig. 2b, [0020].

311. A POSITA would have understood oxide interlayer 27 is the *anti-tunneling layer* because Lee '916 teaches that the interlayer prevents the loss (leakage) of charges that would otherwise accumulate at an interface region. Ex. 1005 (Lee '961), [0031]-[0033]. This understanding aligns with the function of the anti-tunneling layer of the '365 patent: "It has further been found the anti-tunneling

layer 422c substantially reduces the probability of electron charge that accumulates at the boundaries of the oxygen-lean second nitride layer 422b during programming from tunneling into the first nitride layer 422a, **resulting in lower leakage current** than for a conventional non-volatile memory transistor.” Ex. 1001 (’365 patent), 10:26-31.

X. CONCLUSION

312. I declare that all statements made herein are true to the best of my knowledge, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on September 2, 2025

By:



Jack C. Lee

APPENDIX 1: CURRICULUM VITAE OF JACK C. LEE

Jack C. Lee
Professor Emeritus
Electrical and Computer Engineering Department
The University of Texas at Austin

Current Status

Professor Emeritus
Department of Electrical and Computer Engineering
The University of Texas at Austin

Research / teaching experience and expertise:

- Integrated circuits manufacturing
- Photovoltaic/solar cell technologies
- Alternative channel devices
- Dielectric and passivation processes
- Display technologies
- Semiconductor memory devices

Education

9/84 – 8/88 Ph.D., Electrical Engineering, University of California at Berkeley
9/80 – 12/81 M.S., Electrical Engineering, University of California at Los Angeles
9/76 – 6/80 B.S., Electrical Engineering (with highest honors),
University of California at Los Angeles

Professional Career

9/23 – present Professor Emeritus
Department of Electrical and Computer Engineering
The University of Texas at Austin
9/00 – 8/23 Cullen Trust for Higher Education Endowed Professorship in Engineering #4
Department of Electrical and Computer Engineering
The University of Texas at Austin
9/96 – 8/23 Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin
9/92 – 8/96 Associate Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin
9/88 – 8/92 Assistant Professor, Department of Electrical and Computer Engineering
The University of Texas at Austin
1/88 – 6/88 Lecturer, Electrical Engineering and Computer Science Department
University of California at Berkeley
6/79 – 8/84 Member of Technical Staff, High-Speed Bipolar Device Program
TRW Microelectronics Center, Redondo Beach, CA

Honors and Awards

IEEE Electron Devices Society Distinguished Lecturer, 2004 - 2016.
Fellow, The Institute of Electrical and Electronic Engineers (IEEE), 2002 “For
contributions to the understanding and development of ultra-thin dielectrics and their
application to silicon devices”
Gordon Lepley IV Endowed Memorial Teaching Award, ECE Department, The
University of Texas at Austin, 2004

Cullen Trust For Higher Education Endowed Professorship in Engineering, 2000-present
 Dean's Fellow, College of Engineering, The University of Texas at Austin, 1999, 2003
 Lockheed Fort-Worth Division Award for Excellence in Engineering Teaching,
 College of Engineering, The University of Texas at Austin, 1996
 Award of Excellence, Halliburton Foundation, 1993
 Departmental Teaching Award, College of Engineering, The University of Texas at
 Austin, 1993
 SRC Inventor Recognition Award, Semiconductor Research Corporation, 1991
 Hughes Aircraft Company Endowed Faculty Fellowship in Engineering,
 The University of Texas at Austin, 1991- 2000
 Outstanding Engineering Teaching by an Assistant Professor, College of Engineering,
 The University of Texas at Austin, 1991
 Best Paper Award, SEMATECH Centers of Excellence Coordination Meeting, 1990.
 Dow Outstanding Young Faculty Award, American Society for Engineering Education,
 1990
 Engineering Research Initiation Award, Engineering Foundation of the United
 Engineering Trustees, 1989
 Best Paper Award, IEEE International Reliability Physics Symposium, 1988

Litigation Experience as Testifying Experts

The following is a list of cases in which I have provided expert testimony, including through a declaration, report or testimony at deposition or trial since 2016

- Marlin Semiconductor Limited v. TSMC
 April 2025 –
 (Representing defendant, TSMC)
- Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Mfg. Co. Ltd
 October 2024 –
 (Representing defendant, TSMC)
- Yangtze Memory Technologies v. Micron
 January 2024 –
 (Representing defendant, Micron)
- BeSang v. Micron
 March 2023 –
 (Representing defendant, Micron)
- The Trustees of Purdue University v. Wolfspeed, Inc.
 February 2022 – March 2025
 (Representing defendant, Wolfspeed)
- GlobalFoundries - IPR
 March 2021 –
 (Representing petitioner and filed an IPR declaration)

- HD Silicon Solutions LLC v. Microchip Technology Inc.
January 2021 – February 2025
(Representing defendant, Microchip Technology Inc.)
- Longitude Licensing Limited vs Western Digital
March 2023 – January 2024
(Representing defendant, Western Digital)
- Impinj, Inc. v. NXP USA, Inc.
September 2019 – July 2023
(Representing defendant, NXP USA, Inc.)
- Monterey Research, LLC v. Qualcomm Inc.
February 2020 – May 2022
(Representing defendant, Qualcomm)
- Bell Semiconductor, LLC v. Texas Instruments Incorporated
July 2020 – March 2021
(Representing defendant, Texas Instruments)
- Greenthread LLC v. Samsung
February 2020 – July 2020
(Representing plaintiff, Greenthread LLC)
- MLC Intellectual Property LLC vs. Micron Technology, Inc.,
June 2016 – January 2021
(Representing plaintiff, MLC Intellectual Property LLC)
- Hanwha v. LONGi Solar Technology
April 2019 – June 2020
(Representing defendant LONGi Solar Technology)
- Vista Peak Ventures, LLC v. Innolux Corp.
January 2019 – March 2019
(Representing IPR Petitioner, Innolux Corp.)
- Home Semiconductor Corp. v. Samsung
August 2018 – June 2020
(Representing plaintiff, Home Semiconductor Corp.)
- Mariner IC Inc. v. Asustek Computer Inc.
May 2018 – August 2019
(Representing plaintiff, Mariner IC Inc.)
- Godo Kaisha IP Bridge 1 v. OmniVision Technologies, Inc.

January 2018 – December 2018
(Representing defendant, OmniVision Technologies, Inc.)

- Macronix v. Toshiba
May 2017 – February 2018
(Representing defendant, Toshiba)
- University of Illinois v. Micron Technology
September 2009 – November 2017
(Representing plaintiff, Univ. of Illinois)
- Silicon Genesis v. Soitec
October 2016 – March 2017
(Representing plaintiff, Silicon Genesis)

Non-Litigation Consulting

- Applied Materials, Inc.
Teaching short courses on semiconductor physics, devices, design/layout, and fabrication technologies (2-3 courses per year).

Jack C. Lee is a Professor Emeritus of the Electrical and Computer Engineering Department. He held the Cullen Trust for Higher Education Endowed Professorship in Engineering # 4 at The University of Texas at Austin from 2000-2023. He received the B.S. and M.S. degrees in electrical engineering from University of California, Los Angeles, in 1980 and 1981, respectively; and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1988. From 1979 to 1984, he was a Member of Technical Staff at the TRW Microelectronics Center, CA, in the High-Speed Bipolar Device Program. He worked on bipolar device and circuit design, fabrication and testing. In 1988, he joined the faculty of The University of Texas at Austin. His current research interests include semiconductor devices including 3D structures such as FinFETs, fabrication processes, characterization and modeling, dielectric process, characterization and reliability, high-K gate dielectrics and electrode, semiconductor memory applications, alternative channel materials, display technologies and photovoltaic/solar cell technologies. Dr. Lee has over 40 years of experience in semiconductor technology and dielectric processing. He has published over 600 journal publications and conference proceedings and 9 patents; and co-authored 8 book and book chapters. He has also been

recognized with many teaching and research awards. Dr. Lee is a Fellow of IEEE and had been a Distinguished Lecturer for the IEEE Electron Devices Society.

Publications

Jack C. Lee

Refereed Journal Publications

1. J. Lee, K. Mayaram and C. Hu, "A Theoretical Study of Gate/Drain Offset in LDD MOSFET's," IEEE Electron Device Letters, vol. EDL-7, no. 3, p. 152 - 154, March 1986.
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APPENDIX 2: MATERIALS CONSIDERED IN THE PREPARATION OF THIS DECLARATION

Exhibit No.	Description
1001	U.S. Patent No. 11,456,365 to Polishchuk et al. (“the ’365 patent”)
1002	Certified Prosecution file history for the ’365 patent (“Prosecution History”)
1004	U.S. Patent Application Publication No. 2012/0068255 to Changhyun Lee, et al. (“Lee ’255”)
1005	Korean Patent Publication No. 2011-0118961 to Gi Hong Lee et al. and Certified English Translation of Korean Patent Publication No. 2011-0118961 to Gi Hong Lee et al. (“Lee ’961”)
1006	U.S. Patent Application Publication No. 2006/0065919A1 to Ichiro Fujiwara (“Fujiwara”)
1007	L. Lukasiak and A. Jakubowski, <i>History of Semiconductors</i> , Journal of Telecommunications and Information Technology, Vol. 3 (2010) (“Lukasiak”)
1008	U.S. Patent No. 4,203,158 to Dov Frohman-Bentchkowsky, et al. (“Frohman-Bentchkowsky”)
1009	U.S. Patent Application Publication No. 2006/0255399 to Ju-Hyung Kim, et al. (“Kim ’399”)
1010	U.S. Patent Application Publication No. 2003/0122204 to Kazumasa Nomoto, et al. (“Nomoto”)
1011	U.S. Patent Application Publication No. 2009/0179253 to Levy, et al. (“Levy”)
1012	U.S. Patent Application Publication No. 2011/0045647 to Jin-Hwa Heo, et al. (“Heo”)
1013	U.S. Patent Application Publication No. 2011/0281429 to Udayan Ganguly, et al. (“Ganguly”)
1014	U.S. Patent Application Publication No. US 2006/0113586 to Szu-Yu Wang (“Wang ’586”)

Exhibit No.	Description
1015	U.S. Patent No. 6,897,533 to Jean Yee-Mei Yang, et al. (“Yang ’533”)
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1021	U.S. Patent Application Publication No. 2010/0157680A1 to Masaaki Higuchi, et al. (“Higuchi”)
1022	U.S. Patent Application Publication No. 2008/0128790 to Jin-Hyo Jung (“Jung”)
1023	U.S. Patent Application Publication No. 2003/0198106 to Jeong-Hyuk Choi (“Choi”).
1024	U.S. Patent Application Publication No. 2009/0026460 to Tien-Fan Ou, et al. (“Ou”)
1025	Falong Zhou, et al., <i>VNDROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications</i> , Proceeding of 2006 European Solid-State Device Research Conference (IEEE Sept. 2006) (“VDNROM”)
1026	H. Tanaka, et al., <i>Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory</i> , 2007 IEEE Symposium on VLSI Technology (June 2007) (“Tanaka”)

Exhibit No.	Description
1027	Toshiba Press Release, Toshiba Develops New NAND Flash Technology (June 12, 2007) (“Toshiba PR”)
1028	U.S. Patent Application Publication No. 2010/0178759A1 to JinGyun Kim, et al. (“Kim ’759”)
1029	Moon Kyung Kim, et al., <i>A Comparison of N+ Type and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories</i> , Material Research Society Symposium Proceedings, Vol. 997 (MRS 2007) (“Kim Article”)
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1032	U.S. Patent Application Publication No. 2012/0276696 to Jun-Kyu Yang, et al. (“Yang ’696”)
1033	U.S. Patent Application Publication No. 2013/0270625 to Byong-hyun Jang, et al. (“Jang”)
1034	U.S. Patent Application Publication No. 2012/0068247 to Changhyun Lee, et al. (“Lee ’247”)
1035	U.S. Patent Application Publication No. 2012/0299086 to Jaegoo Lee (“Lee ’086”)
1036	U.S. Patent Application Publication No. 2011/0316064 to Jung Ho Kim, et al. (“Kim ’064”)
1037	U.S. Provisional Application No. 60/940,160 (“’160 Provisional App.”)
1038	Prosecution file history for the ’434 patent (U.S. Application No. 12/152,518) (“’434 Pros. Hist.”)
1039	Prosecution file history for the ’374 patent (U.S. Application No. 13/288,919) (“’374 Pros. Hist.”)
1040	Prosecution file history for the ’537 patent (U.S. Application No. 13/539,466) (“’537 Pros. Hist.”)
1041	U.S. Patent No. 6,912,163 to Wei Zheng, et al. (“Zheng”)
1042	S.M. Sze and K. Ng, <i>Physics of Semiconductor Devices</i> (3 rd Ed.

Exhibit No.	Description
	Wiley-Interscience 2007) (“Sze”)
1043	U.S. Patent Application Publication No. 2010/0019312 to Katsuyuki Sekine, et al. (“Sekine”)
1044	U.S. Patent No. 7,450,423 to Erh-Kun Lai, et al. (Lai ’423)

APPENDIX 3: CHALLENGED CLAIMS

1. [pre] A method comprising:

[1a1] forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;

[1a2] forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate;

[1b] forming on sidewalls of the opening a blocking dielectric layer;

[1c] forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region;

[1d] forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and

[1e] forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.

2. The method of claim 1, further comprising the step of forming a second diffusion region such that the vertical channel connects the first and second diffusion regions.

3. The method of claim 1, further comprising forming a layer of semiconductor material including a second doped diffusion region over a top surface of the stack of layers and the opening, wherein the vertical channel electrically couples the first doped diffusion region to the second doped diffusion region.

5. The method of claim 1, wherein the blocking dielectric layer includes a high K dielectric.

6. The method of claim 1, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.

7. The method of claim 6, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.

8. The method of claim 6, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.

9. The method of claim 1, further comprising the step of etching the sacrificial layer to form a second opening.

10. The method of claim 9, further comprising the step of depositing a gate electrode in the second opening.

11. The method of claim 10, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.

12. The method of claim 10, wherein the deposited gate electrode is a high work function gate electrode.

14. The method of claim 1, wherein the vertical channel formed includes an annular region.

15. The method of claim 14, wherein at least a portion of the vertical channel is formed of polysilicon.

16. The method of claim 14, wherein the vertical channel formed includes a layer of semiconductor material surrounding a cylinder of filler material.

17. The method of claim 14, wherein the vertical channel formed includes an outer layer of semiconductor material.

18. The method of claim 17, wherein the outer layer of semiconductor material is formed of polysilicon.

19. The method of claim 14, wherein the blocking dielectric layer is formed in a substantially annular shape.

20. The method of claim 19, wherein the blocking dielectric layer includes a high K dielectric.

21. The method of claim 19, wherein the multi-layer charge storing region is formed in a substantially annular shape.

22. The method of claim 21, wherein the tunnel dielectric layers is formed in a substantially annular shape.

23. [pre] A method comprising:

[23a1] forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;

[23a2] forming an opening extending through the stack of layers towards the substrate;

[23b] forming on sidewalls of the opening an annular shaped blocking dielectric layer;

[23c] forming on an inside sidewall of the blocking dielectric layer an annular shaped multi-layer charge storing region;

[23d] forming on an inside sidewall of the multi-layer charge storing region an annular shaped tunnel dielectric layer; and

[23e] forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layers.

25. The method of claim 23, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.

26. The method of claim 25, wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.

27. The method of claim 26, further comprising forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.

28. The method of claim 23, further comprising the step of etching the sacrificial layer to form a second opening.

29. The method of claim 28, further comprising the step of depositing a gate electrode in the second opening.

30. The method of claim 29, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.

31. The method of claim 29, wherein the deposited gate electrode is a high work function gate electrode.

32. The method of claim 29, wherein the blocking dielectric layer includes a high K dielectric.

33. The method of claim 32, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.

34. The method of claim 33 wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.

35. [pre] A semiconductor memory device, comprising:

[35a] a semiconductor substrate,

[35b] a channel region oriented substantially perpendicular to the semiconductor substrate, the channel region formed in a substantially annular shape,

[35c] a tunnel dielectric layer surrounding the channel region, the tunnel dielectric layer formed in a substantially annular shape,

[35d] a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape, [35e] a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and [35f] a gate electrode surrounding the blocking dielectric layer.

36. The semiconductor memory device of claim 35, wherein the blocking dielectric layer includes a high K dielectric.

37. The semiconductor memory device of claim 35, wherein the gate electrode is a high work function gate electrode.

38. The semiconductor memory device of claim 35, wherein the multi-layer charge storing region includes a first oxygen-lean nitride layer and a second oxygen-rich nitride layer.

39. The semiconductor memory device of claim 38, wherein the first oxygen-lean nitride layer and the second oxygen-rich nitride layer both include silicon, nitrogen and oxygen components.

40. The semiconductor memory device of claim 39, wherein the first oxygen-lean nitride layer is formed on an inside sidewall of the blocking dielectric layer and wherein the second oxygen-rich nitride layer is formed on the inside sidewall of the first oxygen-lean nitride layer.

41. The semiconductor memory device of claim 40, wherein the blocking dielectric layer includes a high K dielectric.

42. The semiconductor memory device of claim 35, including a stack of layers formed over the substrate.

43. The semiconductor memory device of claim 42, wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer, wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer.

44. The semiconductor memory device of claim 43, wherein the channel region is formed in an opening extending through the stack of layers.

45. The semiconductor memory device of claim 43, wherein the second dielectric layer separates the gate layer from an overlying memory transistor.

APPENDIX 4: UNDERSTANDING OF THE LAW

I have applied the following legal principles provided to me by counsel in arriving at the opinions shown in this report.

Legal Standard for Prior Art

I am not an attorney. I have been informed by attorneys of the relevant legal principles and have applied them to arrive at the opinions shown in this declaration.

I understand that the Petition in an *inter partes* review proceeding may challenge the validity of one or more patent claims and request the cancellation of those claims based on the grounds available under 35 U.S.C. § 102 and 35 U.S.C. § 103 using prior art that consists of patents and printed publications.

Anticipation and Prior Art

I understand that § 102 specifies when a challenged claim is invalid for lacking novelty over the prior art, and that this concept is also known as “anticipation.” I understand that a prior art reference anticipates a challenged claim, and thus renders it invalid by anticipation, if all elements of the challenged claim are disclosed in the prior art reference. I understand the disclosure in the prior art reference can be either explicit or inherent, meaning it is necessarily present or implied. I understand that the prior art reference does not have to use the same words as the challenged claim, but all of the requirements of the claim

must be disclosed so that a person of ordinary skill in the art could make and use the claimed subject-matter.

In addition, I understand that § 102 also defines what is available for use as a prior art reference to a challenged claim.

Under § 102(a), a challenged claim is anticipated if it was patented or described in a printed publication in the United States or a foreign country before the challenged claim's date of invention.

Under § 102(b), a challenged claim is anticipated if it was patented or described in a printed publication in the United States or a foreign country more than one year prior to the challenged patent's filing date.

Under § 102(e), a challenged claim is anticipated if it was described in a published patent application that was filed by another in the United States before the challenged claim's date of invention, or was described in a patent granted to another that was filed in the United States before the challenged claim's date of invention.

I understand that a challenged claim's date of invention is presumed to be the challenged patent's filing date. I also understand that the patent owner may establish an earlier invention date and "swear behind" prior art defined by § 102(a) or § 102(e) by proving (with corroborated evidence) the actual date on which the

named inventors conceived of the subject matter of the challenged claim and proving that the inventors were diligent in reducing the subject matter to practice.

I understand that the filing date of a patent is generally the filing date of the application filed in the United States that issued as the patent. However, I understand that a patent may be granted an earlier effective filing date if the patent owner properly claimed priority to an earlier patent application.

I understand that when a challenged claim covers several structures, either generically or as alternatives, the claim is deemed anticipated if any of the structures within the scope of the claim is found in the prior art reference.

I understand that when a challenged claim requires selection of an element from a list of alternatives, the prior art teaches the element if one of the alternatives is taught by the prior art.

Legal Standard for Obviousness

I understand that even if a challenged claim is not anticipated, it is still invalid if the differences between the claimed subject matter and the prior art are such that the claimed subject matter would have been obvious to a person of ordinary skill in the pertinent art at the time the alleged invention.

I understand that obviousness must be determined with respect to the challenged claim as a whole.

I understand that one cannot rely on hindsight in deciding whether a claim is obvious.

I also understand that an obviousness analysis includes the consideration of factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the challenged claim, (3) the level of ordinary skill in the pertinent art, and (4) “secondary” or “objective” evidence of non-obviousness.

Secondary or objective evidence of non-obviousness includes evidence of: (1) a long felt but unmet need in the prior art that was satisfied by the claimed invention; (2) commercial success or the lack of commercial success of the claimed invention; (3) unexpected results achieved by the claimed invention; (4) praise of the claimed invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the claimed invention; and (7) contemporaneous and independent invention by others. However, I understand that there must be a relationship between any secondary evidence of non-obviousness and the claimed invention.

I understand that a challenged claim can be invalid for obviousness over a combination of prior art references if a reason existed (at the time of the alleged invention) that would have prompted a person of ordinary skill in the art to combine elements of the prior art in the manner required by the challenged claim. I understand that this requirement is also referred to as a “motivation to combine,”

“suggestion to combine,” or “reason to combine,” and that there are several rationales that meet this requirement.

I understand that the prior art references themselves may provide a motivation to combine, but other times simple common sense can link two or more prior art references. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may come from market forces.

I understand obviousness to include, for instance, scenarios where known techniques are simply applied to other devices, systems, or processes to improve them in an expected or known way. I also understand that practical and common-sense considerations should be applied in a proper obviousness analysis. For instance, familiar items may have obvious uses beyond their primary purposes.

I understand that the combination of familiar elements according to known methods is obvious when it yields predictable results. For instance, obviousness bars patentability of a predictable variation of a technique even if the technique originated in another field of endeavor. This is because design incentives and other market forces can prompt variations of it, and predictable variations are not the product of innovation, but rather ordinary skill and common sense.

I understand that a particular combination may be obvious if it was obvious to try the combination. For example, when there is a design need or market

pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. This would result in something obvious because the result is the product not of innovation but of ordinary skill and common sense. However, I understand that it may not be obvious to try a combination when it involves unpredictable technologies.

It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

It is my understanding that the Manual of Patent Examining Procedure §2143 sets forth the following as exemplary rationales that support a conclusion of obviousness:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

- Choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

A person of ordinary skill in the art looking to overcome a problem will often use the teachings of multiple publications together like pieces of a puzzle, even though the prior art does not necessarily fit perfectly together. Therefore, I understand that references for obviousness need not fit perfectly together like puzzle pieces. Instead, I understand that obviousness analysis takes into account inferences, creative steps, common sense, and practical logic and applications that a person of ordinary skill in the art would employ under the circumstances.

I understand that a claim can be obvious in light of a single reference, if the elements of the challenged claim that are not explicitly or inherently disclosed in the reference can be supplied by the common sense of one of skill in the art.

I understand that obviousness also bars the patentability of applying known or obvious design choices to the prior art. One cannot patent merely substituting one prior art element for another if the substitution can be made with predictable

results. Likewise, combining prior art techniques that are interoperable with respect to one another is generally obvious and not patentable.

In order for a claim to be found invalid based upon a modification or combination of the prior art, there must be reasonable expectation that a person of ordinary skill would have successfully modified or combined the prior art to arrive at the claimed arrangement. This does not mean that it must be certain that a person of ordinary skill would have been successful – the law only requires that the person of ordinary skill in the art would have perceived a reasonable expectation of success in modifying or combining the prior art to arrive at the claimed invention.

In sum, my understanding is that obviousness invalidates claims that merely recite combinations of, or obvious variations of, prior art teachings using understanding and knowledge of one of skill in the art at the time and motivated by the general problem facing the inventor at the time. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of or attempting obvious variations on prior art references in the claimed manner.

Legal Standard for Claiming the Benefit of the Filing Date of an Earlier-Filed Patent Application

I understand that an invention described in a patent may claim the benefit of, or priority to, a prior application filed in the United States or in a foreign country. I understand that, to claim the benefit of an earlier-filed application, the later-filed

application must contain a specific reference to the earlier-filed application. In addition, I understand that the later-filed application must be an application for a patent for an invention which is also disclosed in the prior application. I understand that the disclosure in the prior application and the later-filed application must be sufficient to comply with the written description and enablement requirements of 35 U.S.C. § 112(a), which provides for two requirements: (1) a written description, which must allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed; and (2) enablement, meaning that the patent must teach an ordinary artisan to make and use the invention without undue experimentation. I understand that a patent cannot claim priority to earlier applications if the later patent includes new matter not present in those earlier disclosures. For example, I understand that a claim in a continuation-in-part application is entitled only to the filing date of the continuation-in-part application when the claim recites a feature which was not disclosed or adequately supported by a proper disclosure under 35 U.S.C. 112 in the earlier-filed parent application.

Legal Standard for Claim Construction

I understand that before any invalidity analysis can be properly performed, the scope and meaning of the challenged claims must be determined by claim construction.

I understand that a patent may include two types of claims, independent claims and dependent claims. I understand that an independent claim stands alone and includes only the limitations it recites. I understand that a dependent claim depends from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to the limitations recited in the claim (or claims) from which it depends.

In comparing the challenged claims to the prior art, I have carefully considered the patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

I understand that to determine how a person of ordinary skill would have understood a claim term, one should look to sources available at the time of the alleged invention that show what a person of skill in the art would have understood disputed claim language to mean. It is my understanding that this may include what is called “intrinsic” evidence as well as “extrinsic” evidence.

I understand that, in construing a claim term, one should primarily rely on intrinsic patent evidence, which includes the words of the claims themselves, the remainder of the patent specification, and the prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient. I understand that extrinsic evidence may include

principles, concepts, terms, and other resources available to those of skill in the art at the time of the invention.

I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else or something more specific. I understand that to determine whether a term has special meaning, the claims, the patent specification, and the prosecution history are particularly important, and may show that the inventor gave a term a particular definition or intentionally disclaimed, disavowed, or surrendered claim scope.

I understand that the claims of a patent define the scope of the rights conferred by the patent. I understand that because the claims point out and distinctly claim the subject matter which the inventors regard as their invention, claim construction analysis must begin with and is focused on the claim language itself. I understand that the context of the term within the claim as well as other claims of the patent can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, how a term is used in one claim can often inform the meaning of the same term in other claims. Differences among claims or claim terms can also be a useful guide in understanding the meaning of particular claim terms.

I understand that a claim term should be construed not only in the context of the particular claim in which the disputed term appears, but in the context of the

entire patent, including the entire specification. I understand that because the specification is a primary basis for construing the claims, a correct construction must align with the specification.

I understand that the prosecution history of the patent as well as art incorporated by reference or otherwise cited during the prosecution history are also highly relevant in construing claim terms. For instance, art cited by or incorporated by reference may indicate how the inventor and others of skill in the art at the time of the invention understood certain terms and concepts. Additionally, the prosecution history may show that the inventors disclaimed or disavowed claim scope, or further explained the meaning of a claim term.

With regard to extrinsic evidence, I understand that all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical dictionaries may indicate how one of skill in the art used or understood the claim terms. However, I understand that extrinsic evidence is considered to be less reliable than intrinsic evidence, and for that reason is generally given less weight than intrinsic evidence.

I understand that in general, a term or phrase found in the introductory words or preamble of the claim, should be construed as a limitation if it recites essential structure or steps, or is necessary to give meaning to the claim. For

instance, I understand preamble language may limit claim scope: (i) if dependence on a preamble phrase for antecedent basis indicates a reliance on both the preamble and claim body to define the claimed invention; (ii) if reference to the preamble is necessary to understand limitations or terms in the claim body; or (iii) if the preamble recites additional structure or steps that the specification identifies as important.

On the other hand, I understand that a preamble term or phrase is not limiting where a challenged claim defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. I understand that to make this determination, one should review the entire patent to gain an understanding of what the inventors claim they invented and intended to encompass in the claims.

I understand that 35 U.S.C. § 112 ¶ 6 created an exception to the general rule of claim construction called a “means plus function” limitation. These types of terms and limitations should be interpreted to cover only the corresponding structure described in the specification, and equivalents thereof. I also understand that a limitation is presumed to be a means plus function limitation if (a) the claim limitation uses the phrase “means for”; (b) the “means for” is modified by functional language; and (c) the phrase “means for” is not modified by sufficient structure for achieving the specified function.

I understand that a structure is considered structurally equivalent to the corresponding structure identified in the specification only if the differences between them are insubstantial. For instance, if the structure performs the same function in substantially the same way to achieve substantially the same result. I further understand that a structural equivalent must have been available at the time of the issuance of the claim.