

EXHIBIT D: P.R. 3-1(B) CHART FOR U.S. PATENT NO. 11,456,365

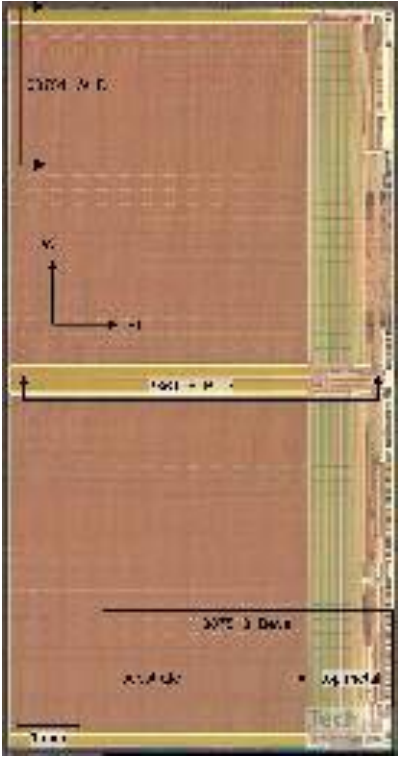
Declaratory judgment defendants IPValue Management, Inc. and Longitude Flash Memory Solutions Ltd. (collectively “IPValue”) provides this chart based upon information that is presently available to them. IPValue has not had access to the accused infringers’ confidential design documents or to other materials that may become available during discovery. IPValue reserves the right to change or provide more detail to the infringement theories set forth below, based upon information that it learns during this case, subject to the Court’s rules and orders.

Definitions:

The term ‘365 Accused Instrumentalities is defined in Section I.B of IPValue’s Disclosure of Asserted Claims and Infringement Contentions. As shown in the chart below, the structure of the memory transistors is similar across each of the 64L, 96L, 112L, 162L, and 218L 3D NAND products. Any reference to any specific accused product in the chart below is representative of all ‘365 Accused Instrumentalities.

<i>Claim Element</i>	<i>’365 Accused Instrumentalities</i>
1. A method comprising:	The ‘365 Accused Instrumentalities are manufactured using the claimed method. For example, the WDS960G2G0C SSD contains a semiconductor die containing 112-Layer 3D NAND Flash Memory¹: 

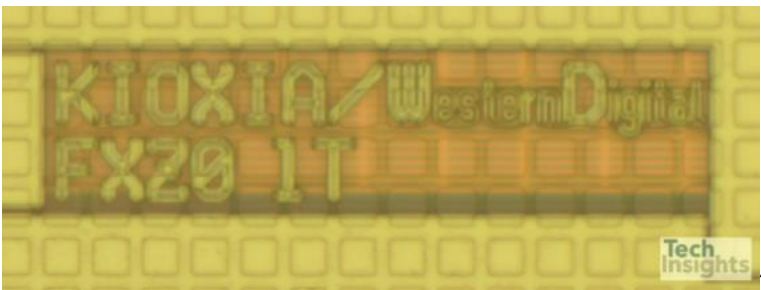
¹ TechInsights, Kioxia/Western Digital WDS960G2G0C SSD, SanDisk 060946 1T00 (FXH8 512G Die), 112-Layer 3D NAND Flash Memory, 18 nm Process Node, Advanced Memory Essentials, AME-2106-802, Published: November 19, 2021 (“TechInsights 112L Report”)

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	A microscopic image of a semiconductor die, likely a NAND flash memory die. The die is rectangular and has a brownish-gold color. It features a grid of memory cells. There are several markings on the die, including "3070 3 Data" and "3070 3 Data" in the upper left and lower right areas. A small "T" is visible in the bottom left corner. The die is mounted on a green substrate. Die markings on this and other '365 Accused Instrumentalities indicate that they are each made by a joint venture owned by Toshiba/Kioxia and Sandisk/Western Digital:

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	 12 Package Optical - Package X-ray - Die Optical\TH58LJT0T24BADE_FST0_256G_336534_DieMik-100X.png ²  ³

² Image of Western Digital Green SSD (P/N WDS480G2G0A) (96L)

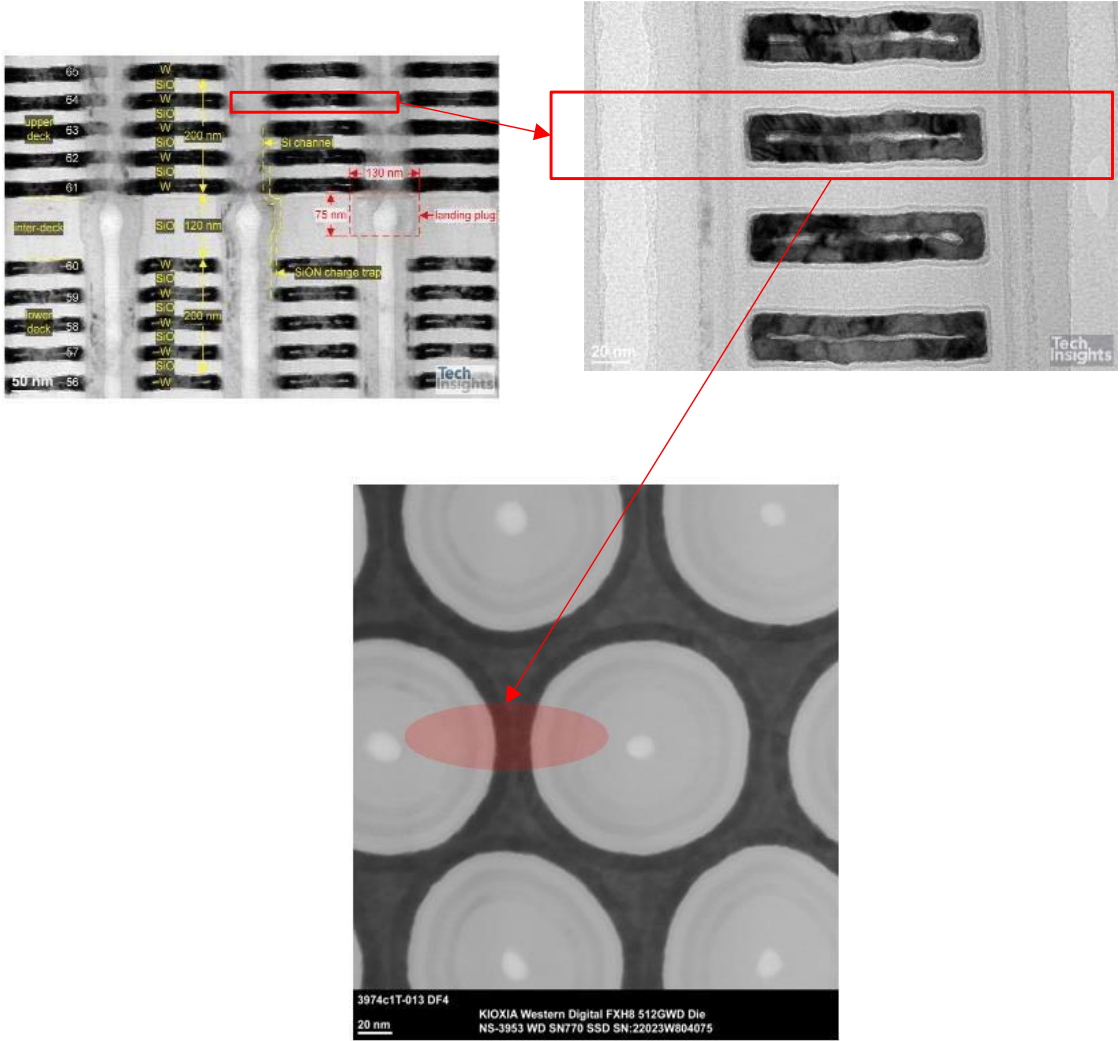
³ TechInsights 112L Report

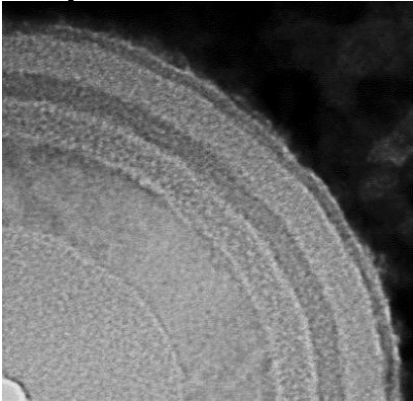
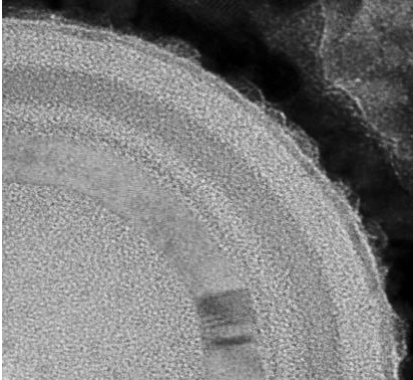
Claim Element	'365 Accused Instrumentalities
	 4  5 The following images each show multiple memory transistors, in different cross sections of a 112L accused product⁶:

⁴ TechInsights, Toshiba TH58LKT3B46BA8S (KIOXIA/Western Digital Corp. FXZ0_1T die), 162-Layer 3D NAND Flash Memory, Advanced Memory Essentials, AME-2310-803, Published: February 29, 2024 (“TechInsights 162L Report”)

⁵ TechInsights, KIOXIA/WDC FYU6_1T 218L (BiCS8), Triple-Level Cell (TLC) 1 Tb 3D NAND Flash, Advanced Memory Essentials, AME-2407-801, Published: November 29, 2024 (“TechInsights 218L Report”)

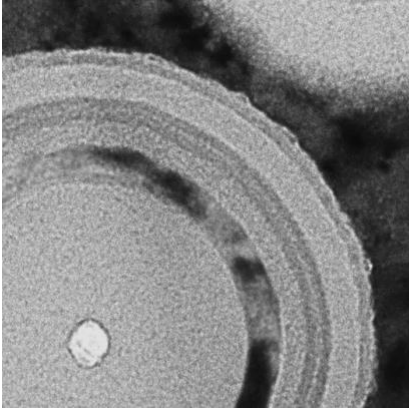
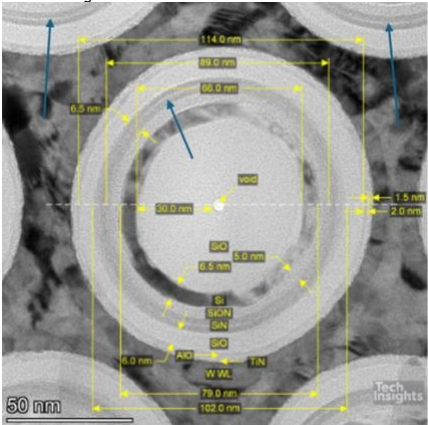
⁶ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	Similar memory transistor structures are present in each of the '365 Accused Instrumentalities, as shown in the following cross section images. 64-layer⁷:  96-layer⁸: 

⁷ TechInsights, Memory DRAM & NAND Tri-Annual Briefing #1, 2022, Report ID: BRF-2112-810, May 2022, p. 47,

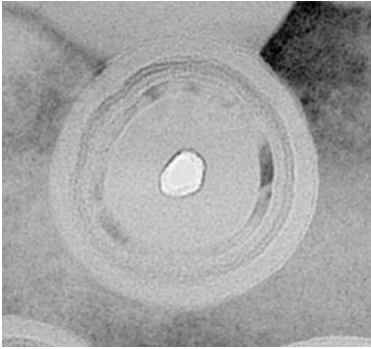
⁸ *Id.*

Claim Element	'365 Accused Instrumentalities
	112-layer⁹:  162-layer¹⁰:  218-layer¹¹:

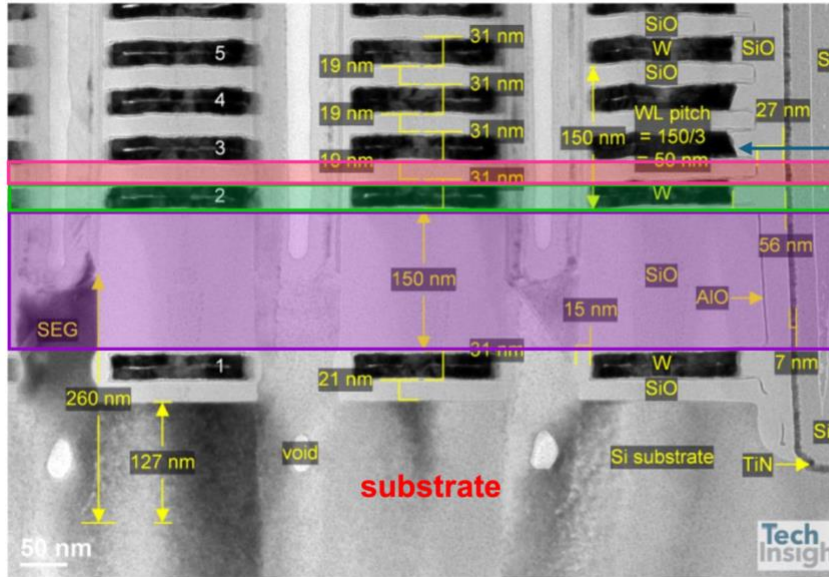
⁹ *Id.*

¹⁰ TechInsights 162L Report

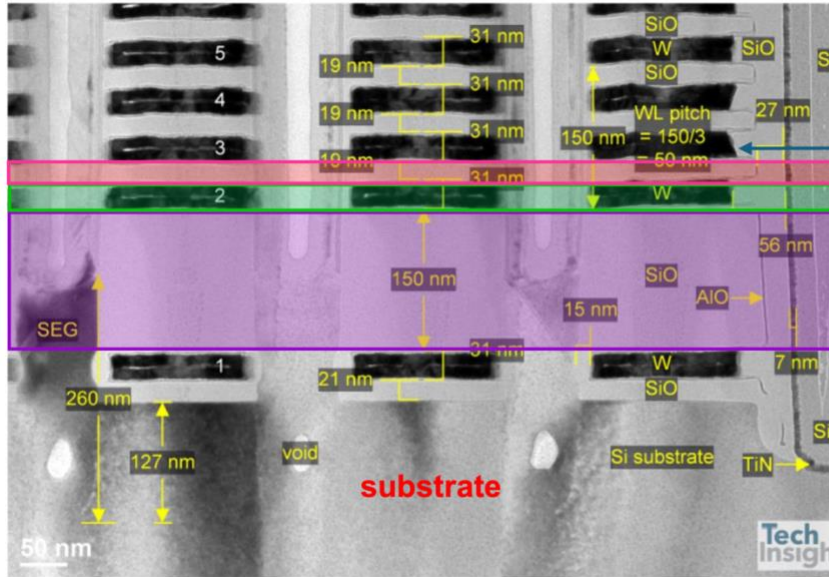
¹¹ TechInsights 218L Report

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	
[1a] forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer,	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer. For example, a first dielectric layer, a sacrificial layer, and a second dielectric layer are formed over a silicon substrate ¹² :

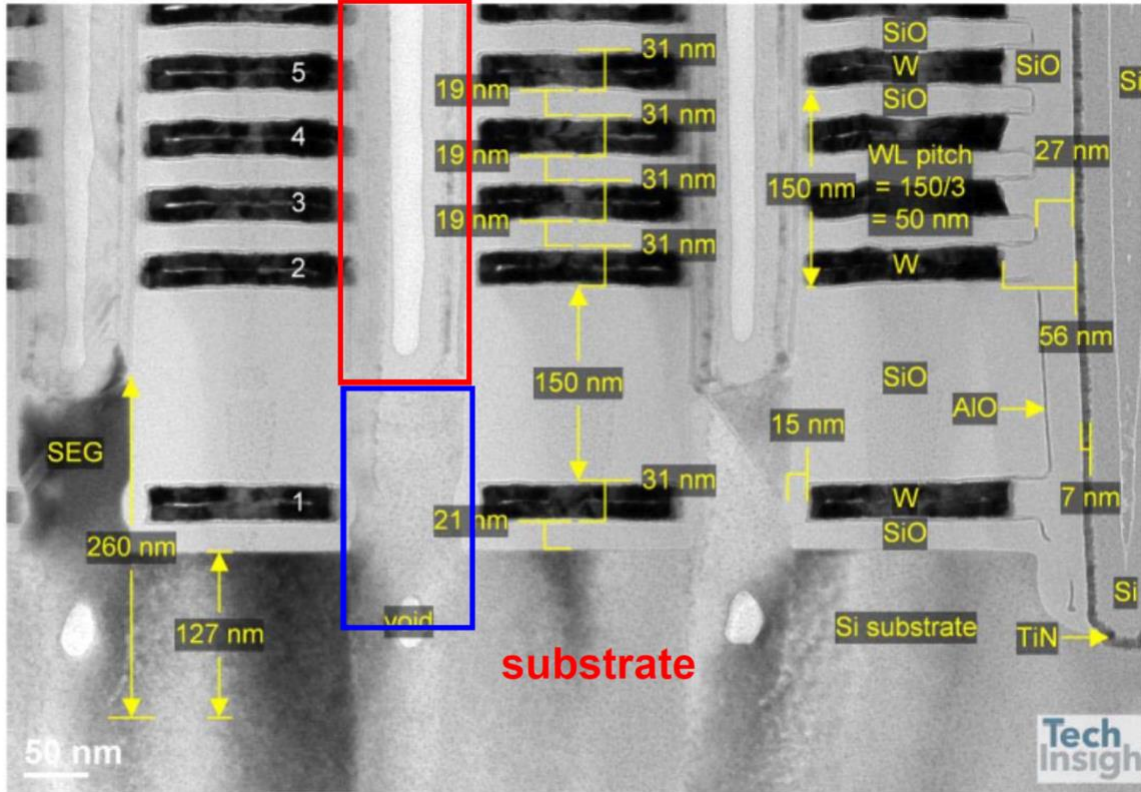
¹² TechInsights 112L Report

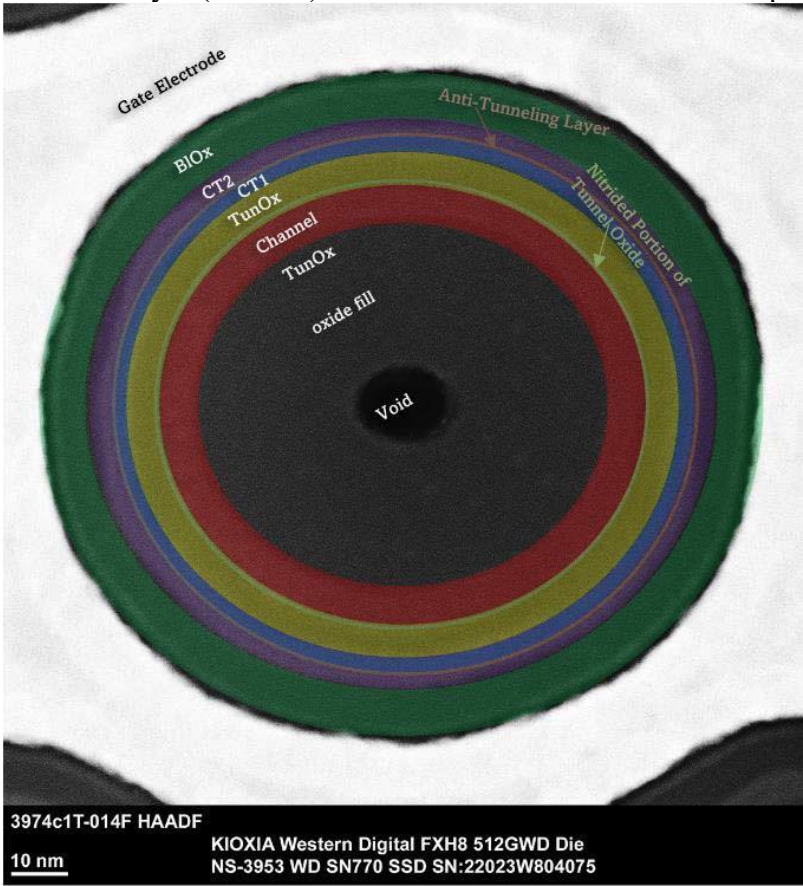
<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	 The image is a cross-sectional SEM micrograph of a semiconductor device. It shows a substrate at the bottom, labeled 'substrate' in red. Above the substrate is a 'first dielectric layer' (purple), which is separated from the substrate by a 'sacrificial layer' (green). Above the sacrificial layer is a 'second dielectric layer' (pink), which is separated from the first dielectric layer by the sacrificial layer. The second dielectric layer contains a 'memory transistor' (blue). The device structure includes various layers and dimensions: 5, 4, 3, 2, 1, 19 nm, 31 nm, 150 nm, 27 nm, 56 nm, 7 nm, 21 nm, 31 nm, 15 nm, 127 nm, 260 nm, 50 nm, SiO, W, Si, SEG, void, Si substrate, TiN. A scale bar of 50 nm is shown at the bottom left. The Tech Insign logo is at the bottom right.
[1b] wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;	In the method of manufacturing the '365 Accused Instrumentalities the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer. For example, the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer ¹³:

¹³ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 The image is a cross-sectional SEM of a semiconductor device. It shows a stack of layers on a substrate. Key features and labels include: Layers and Dimensions: - Top layer: 5, 4, 3, 2, 1 (numbered layers). - Layer 1: 260 nm thick. - Layer 2: 127 nm thick. - Layer 3: 19 nm thick. - Layer 4: 31 nm thick. - Layer 5: 31 nm thick. - Layer 6: 19 nm thick. - Layer 7: 31 nm thick. - Layer 8: 10 nm thick. - Layer 9: 31 nm thick. - Layer 10: 150 nm thick. - Layer 11: 27 nm thick. - Layer 12: 56 nm thick. - Layer 13: 15 nm thick. - Layer 14: 7 nm thick. - Layer 15: 21 nm thick. - Layer 16: 31 nm thick. - Layer 17: 150 nm thick. - Layer 18: 50 nm thick. - Layer 19: 150 nm thick. - Layer 20: 150 nm thick. - Layer 21: 150 nm thick. - Layer 22: 150 nm thick. - Layer 23: 150 nm thick. - Layer 24: 150 nm thick. - Layer 25: 150 nm thick. - Layer 26: 150 nm thick. - Layer 27: 150 nm thick. - Layer 28: 150 nm thick. - Layer 29: 150 nm thick. - Layer 30: 150 nm thick. - Layer 31: 150 nm thick. - Layer 32: 150 nm thick. - Layer 33: 150 nm thick. - Layer 34: 150 nm thick. - Layer 35: 150 nm thick. - Layer 36: 150 nm thick. - Layer 37: 150 nm thick. - Layer 38: 150 nm thick. - Layer 39: 150 nm thick. - Layer 40: 150 nm thick. - Layer 41: 150 nm thick. - Layer 42: 150 nm thick. - Layer 43: 150 nm thick. - Layer 44: 150 nm thick. - Layer 45: 150 nm thick. - Layer 46: 150 nm thick. - Layer 47: 150 nm thick. - Layer 48: 150 nm thick. - Layer 49: 150 nm thick. - Layer 50: 150 nm thick. - Layer 51: 150 nm thick. - Layer 52: 150 nm thick. - Layer 53: 150 nm thick. - Layer 54: 150 nm thick. - Layer 55: 150 nm thick. - Layer 56: 150 nm thick. - Layer 57: 150 nm thick. - Layer 58: 150 nm thick. - Layer 59: 150 nm thick. - Layer 60: 150 nm thick. - Layer 61: 150 nm thick. - Layer 62: 150 nm thick. - Layer 63: 150 nm thick. - Layer 64: 150 nm thick. - Layer 65: 150 nm thick. - Layer 66: 150 nm thick. - Layer 67: 150 nm thick. - Layer 68: 150 nm thick. - Layer 69: 150 nm thick. - Layer 70: 150 nm thick. - Layer 71: 150 nm thick. - Layer 72: 150 nm thick. - Layer 73: 150 nm thick. - Layer 74: 150 nm thick. - Layer 75: 150 nm thick. - Layer 76: 150 nm thick. - Layer 77: 150 nm thick. - Layer 78: 150 nm thick. - Layer 79: 150 nm thick. - Layer 80: 150 nm thick. - Layer 81: 150 nm thick. - Layer 82: 150 nm thick. - Layer 83: 150 nm thick. - Layer 84: 150 nm thick. - Layer 85: 150 nm thick. - Layer 86: 150 nm thick. - Layer 87: 150 nm thick. - Layer 88: 150 nm thick. - Layer 89: 150 nm thick. - Layer 90: 150 nm thick. - Layer 91: 150 nm thick. - Layer 92: 150 nm thick. - Layer 93: 150 nm thick. - Layer 94: 150 nm thick. - Layer 95: 150 nm thick. - Layer 96: 150 nm thick. - Layer 97: 150 nm thick. - Layer 98: 150 nm thick. - Layer 99: 150 nm thick. - Layer 100: 150 nm thick. Labels: SEG, void, Si substrate, TiN, SiO, W, SiO, WL pitch = 150/3 = 50 nm, memory transistor, second dielectric layer, sacrificial layer, first dielectric layer. Dimensions: 50 nm scale bar. Source: Tech Insign.
[1c] forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate;	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate. For example, an opening (corresponding to the red rectangle below) is formed extending through the stack of layers to a first doped diffusion region (blue rectangle below) on the silicon substrate¹⁴:

¹⁴ TechInsights 112L Report

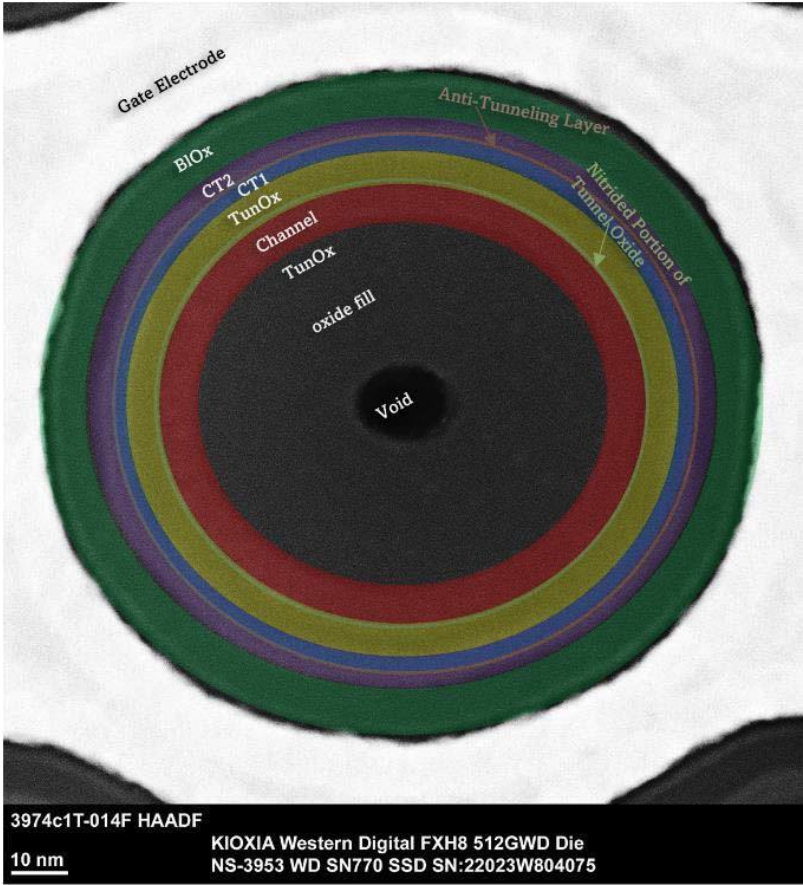
Claim Element	'365 Accused Instrumentalities
	 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.

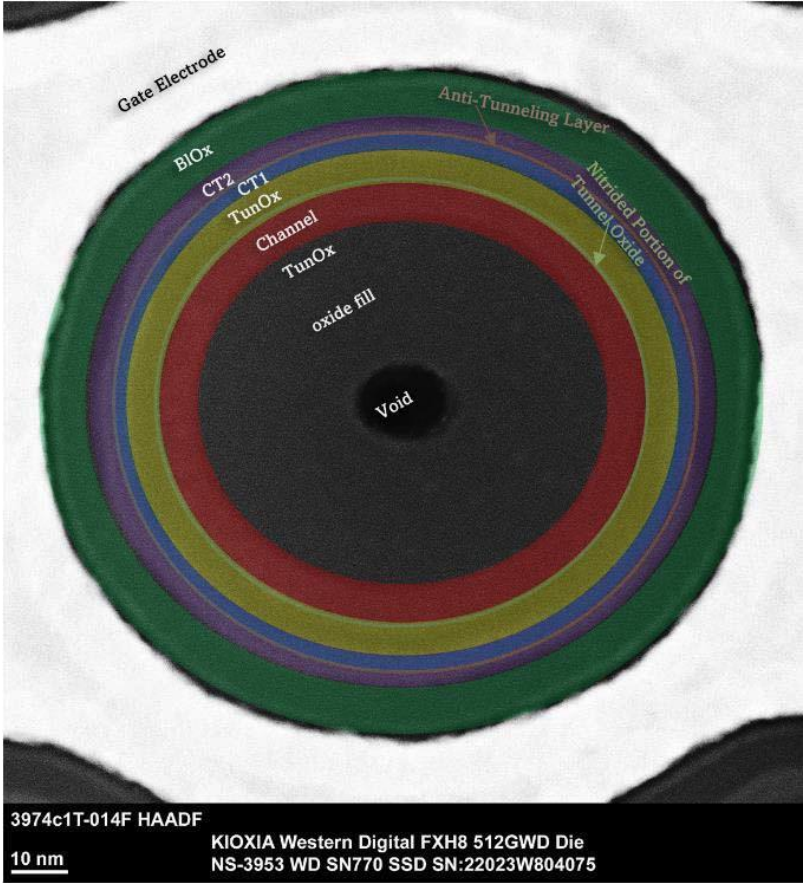
Claim Element	'365 Accused Instrumentalities
[1d] forming on sidewalls of the opening a blocking dielectric layer;	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming on sidewalls of the opening a blocking dielectric layer. For example, a blocking dielectric layer ("BIOx") is formed on the sidewalls of the opening ¹⁵:  The diagram is a cross-sectional view of a memory cell, likely a NAND flash. It shows a central 'Void' surrounded by concentric layers. From the center outwards, the layers are: 'oxide fill', 'TunOx', 'Channel', 'TunOx', 'CT1', 'CT2', 'BIOx', and 'Gate Electrode'. A 'Nitrided Portion of Tunnel Oxide' is also indicated. The diagram is labeled with '3974c1T-014F HAADF' and '10 nm' scale bar. Below the diagram, it says 'KIOXIA Western Digital FXH8 512GWD Die' and 'NS-3953 WD SN770 SSD SN:22023W804075'.

¹⁵ TechInsights 112L Report

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[1e] forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region;	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region. For example, the multi-layer charge storing region (“CT1,” “Anti-Tunneling Layer,” “CT2”) is formed on an inside sidewall of the blocking dielectric layer (“BIOx”) ¹⁶ .

¹⁶ TechInsights 112L Report

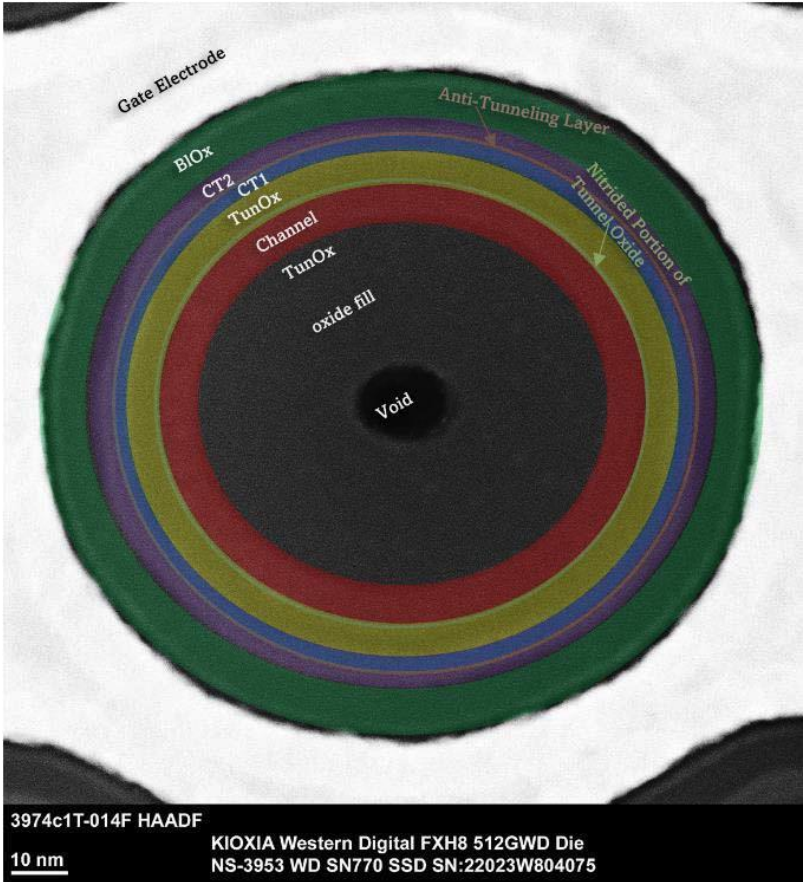
Claim Element	'365 Accused Instrumentalities
	 The diagram shows a cross-section of a memory cell. At the center is a dark circular region labeled 'Void'. Surrounding this is a thick grey ring labeled 'oxide fill'. The next layer is a red ring labeled 'TunOx'. Above this is a thin yellow ring labeled 'Channel'. This is followed by a blue ring labeled 'TunOx', then a green ring labeled 'CT1', and another blue ring labeled 'CT2'. The outermost layer is a thick green ring labeled 'BIOx'. Above the BIOx layer is a thin grey layer labeled 'Gate Electrode'. To the right of the central structure, there is a label 'Anti-Tunneling Layer' pointing to a thin blue layer, and 'Nitrided Portion of Tunnel Oxide' pointing to a thin yellow layer within the TunOx region. 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.

Claim Element	'365 Accused Instrumentalities
[1f] forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer. For example, the tunnel dielectric layer (yellow "TunOx") is formed on an inside sidewall of the multi-layer charge storing region ("CT1," "Anti-Tunneling Layer," "CT2")¹⁷:  The diagram is a cross-sectional view of a multi-layer charge storing region. It shows a central "Void" surrounded by a "oxide fill" layer. Above the oxide fill is a "Channel" layer, which is flanked by "TunOx" (yellow) layers. Above the TunOx layers are "CT1" and "CT2" layers. The outermost layer is the "Gate Electrode". A "Nitrided Portion of Tunnel Oxide" is also indicated. The diagram is labeled with "3974c1T-014F HAADF" and "10 nm" scale bar. Below the diagram, it says "KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075".

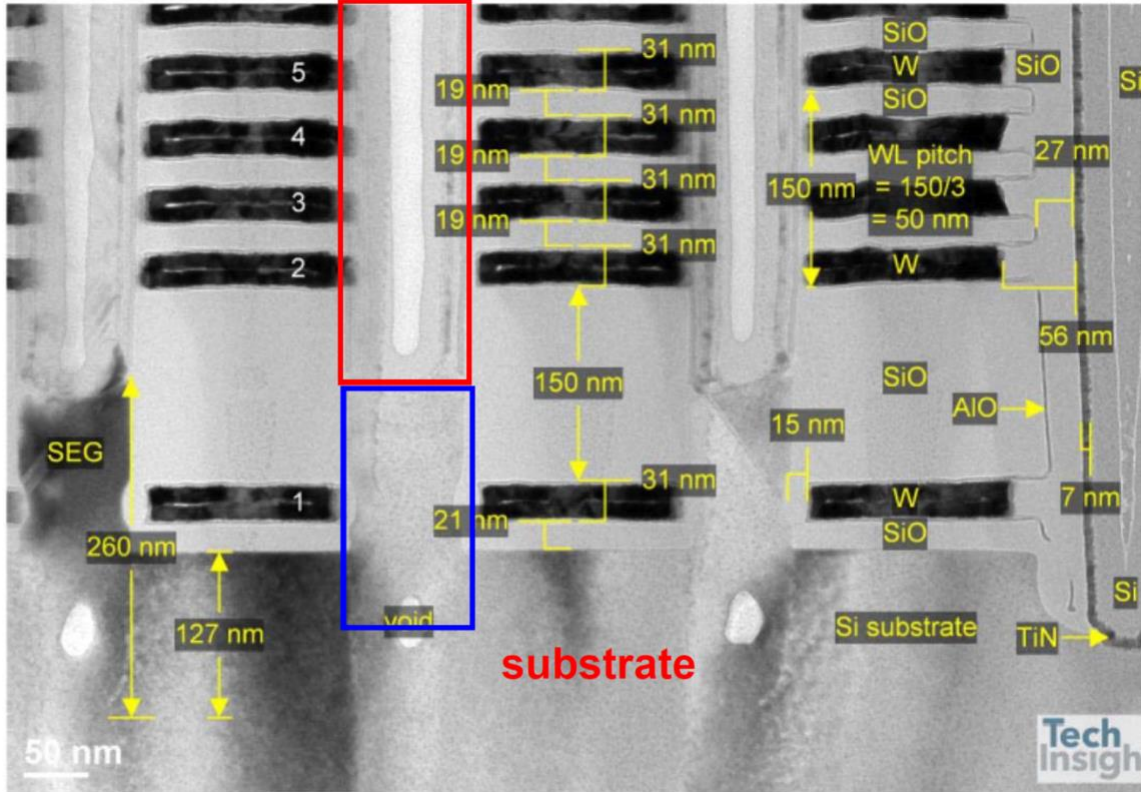
¹⁷ TechInsights 112L Report

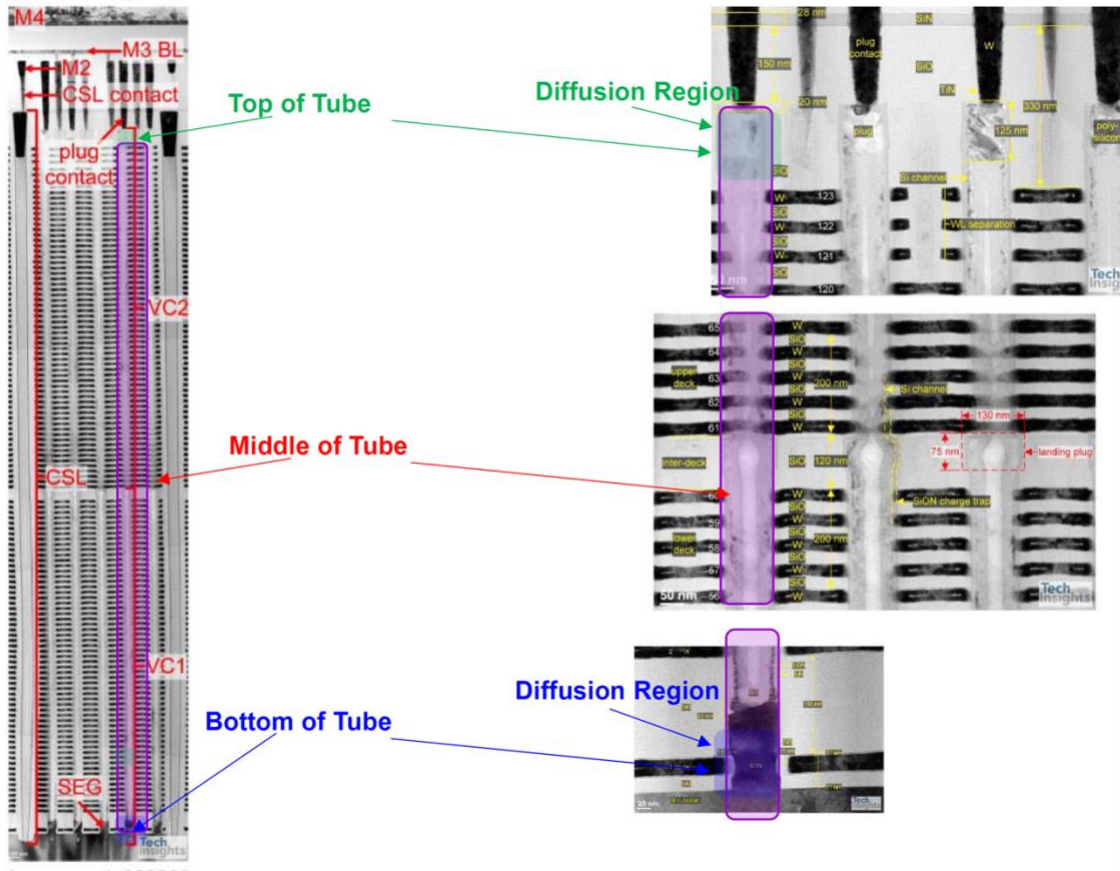
<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[1g] forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers. For example, the silicon channel ("Channel") is formed on an inside sidewall of the tunnel dielectric layer (yellow "TunOx") ¹⁸ :

¹⁸ *Id.*

Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 The channel extends from the first doped region (blue rectangle”) through the opening to the top of the stack of layers¹⁹:

¹⁹ TechInsights 112L Report

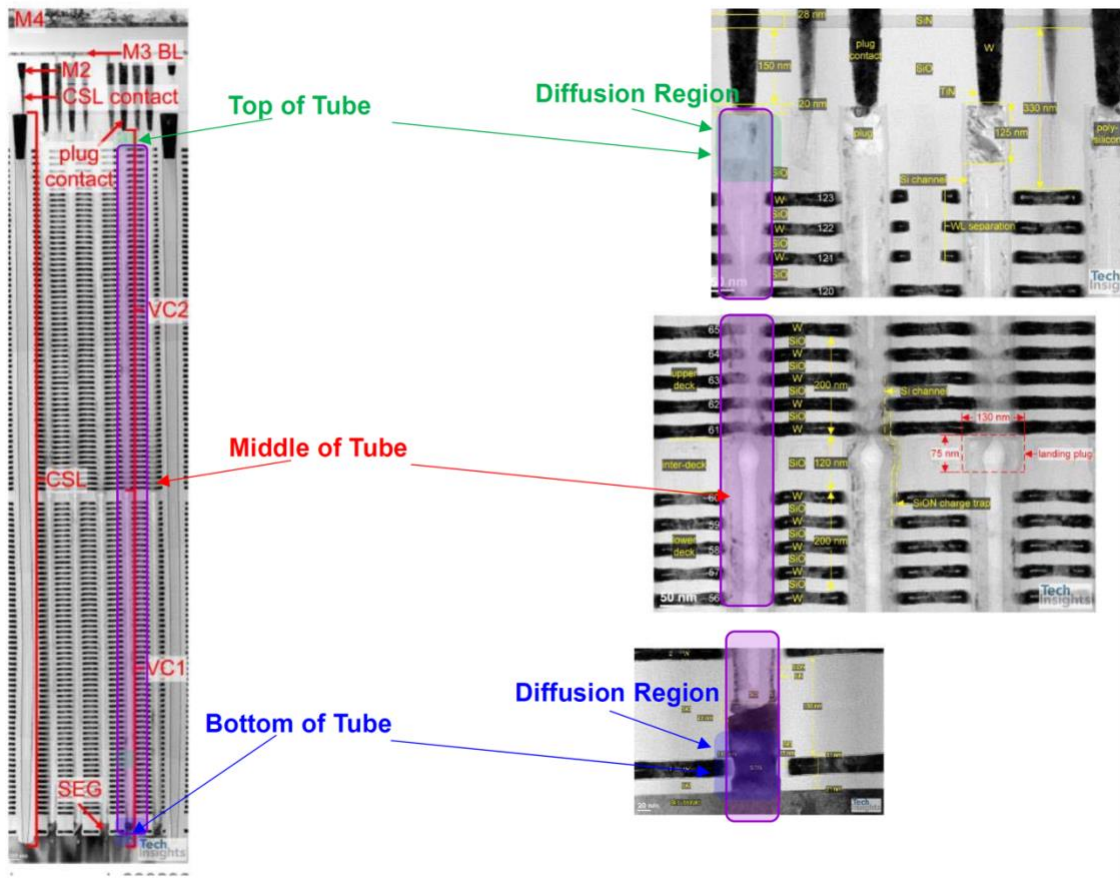
Claim Element	'365 Accused Instrumentalities
	 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
2. The method of claim 1, further comprising the step of forming a second diffusion region such that the	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming a second diffusion region such that the vertical channel connects the first and

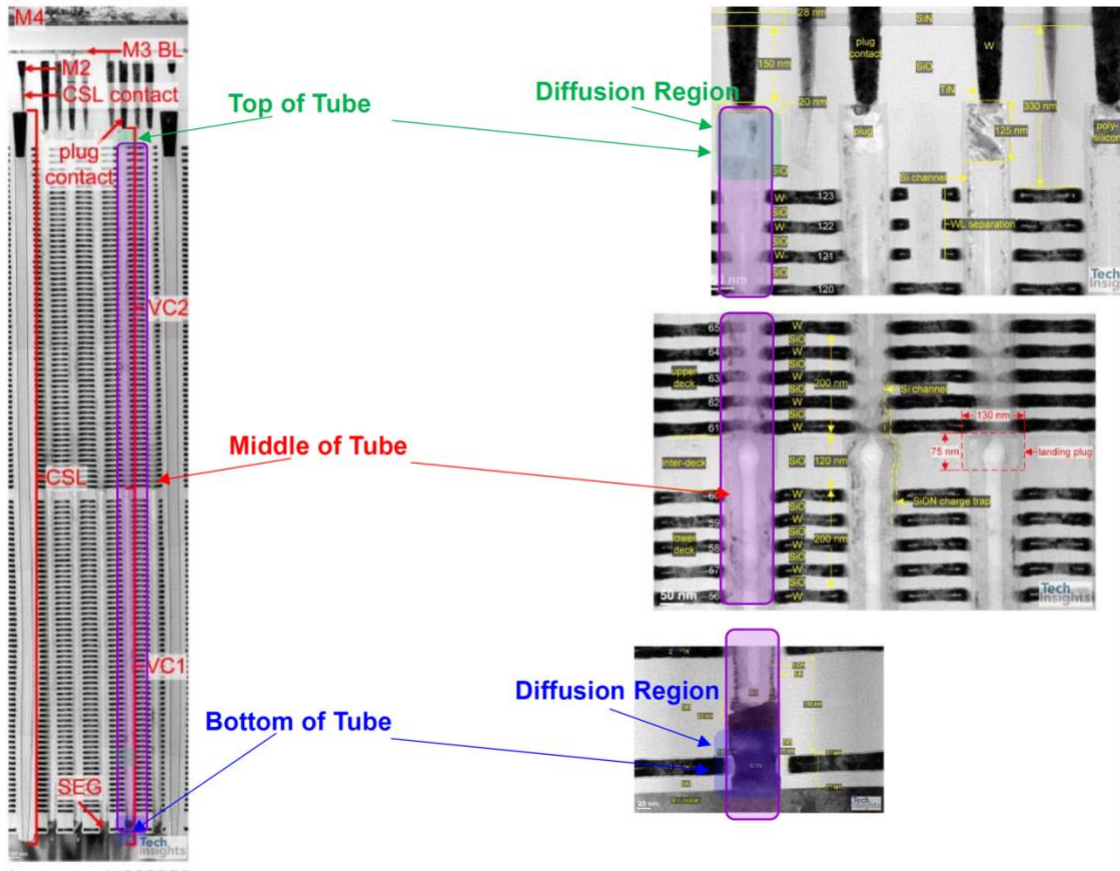
Claim Element	'365 Accused Instrumentalities
vertical channel connects the first and second diffusion regions.	second diffusion regions. For example, the top second diffusion region is formed, such that the tube shaped vertical channel connects the first and second diffusion regions²⁰: 

²⁰ TechInsights 112L Report

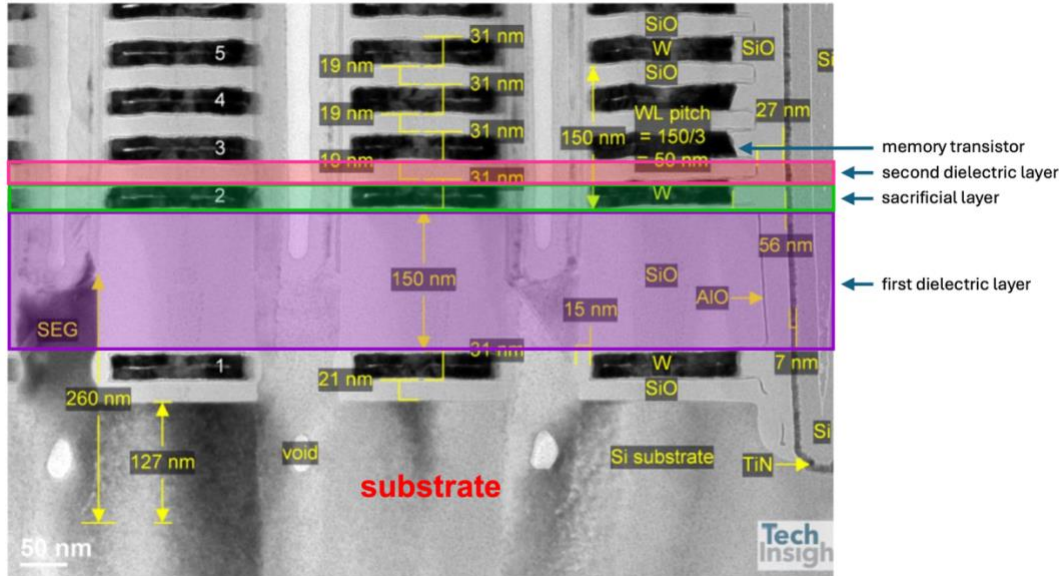
<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
3. The method of claim 1,	
[3a] further comprising forming a layer of semiconductor material including a second doped diffusion region over a top surface of the stack of layers and the opening,	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming a layer of semiconductor material including a second doped diffusion region over a top surface of the stack of layers and the opening. For example, the top second doped diffusion region is formed over a top surface of the stack of layers and the opening ²¹ :

²¹ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[3b] wherein the vertical channel electrically couples the first doped	In the method of manufacturing the '365 Accused Instrumentalities the vertical channel electrically couples the first doped diffusion region to the second doped diffusion region.

Claim Element	'365 Accused Instrumentalities
diffusion region to the second doped diffusion region.	For example, the tube-shaped vertical channel electrically couples the bottom first doped diffusion region to the top second doped diffusion region²²: 

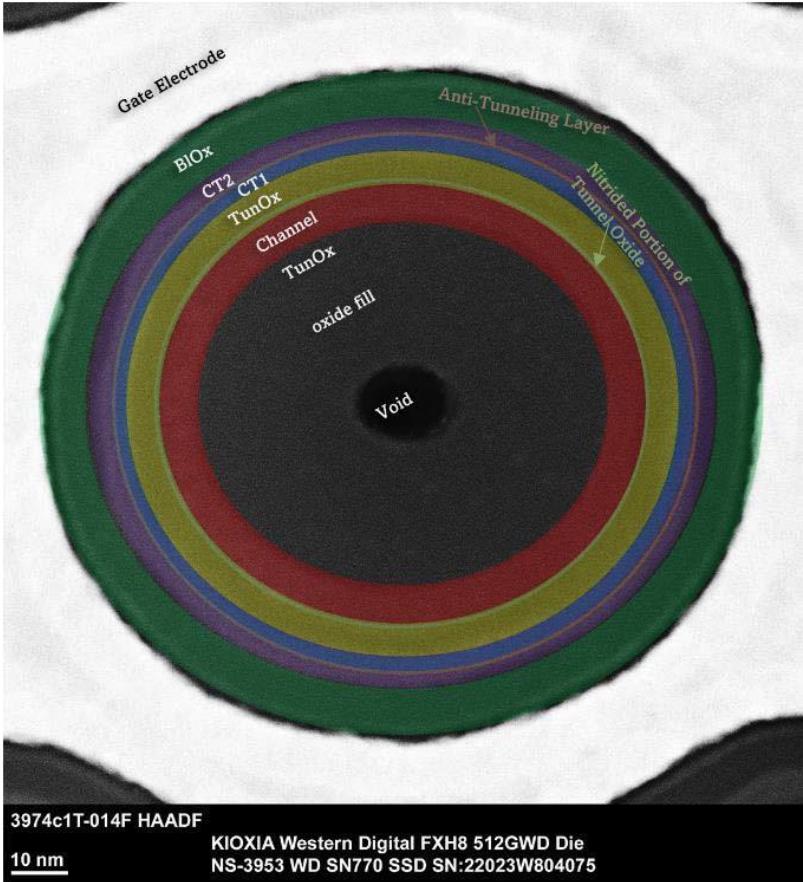
²² TechInsights 112L Report

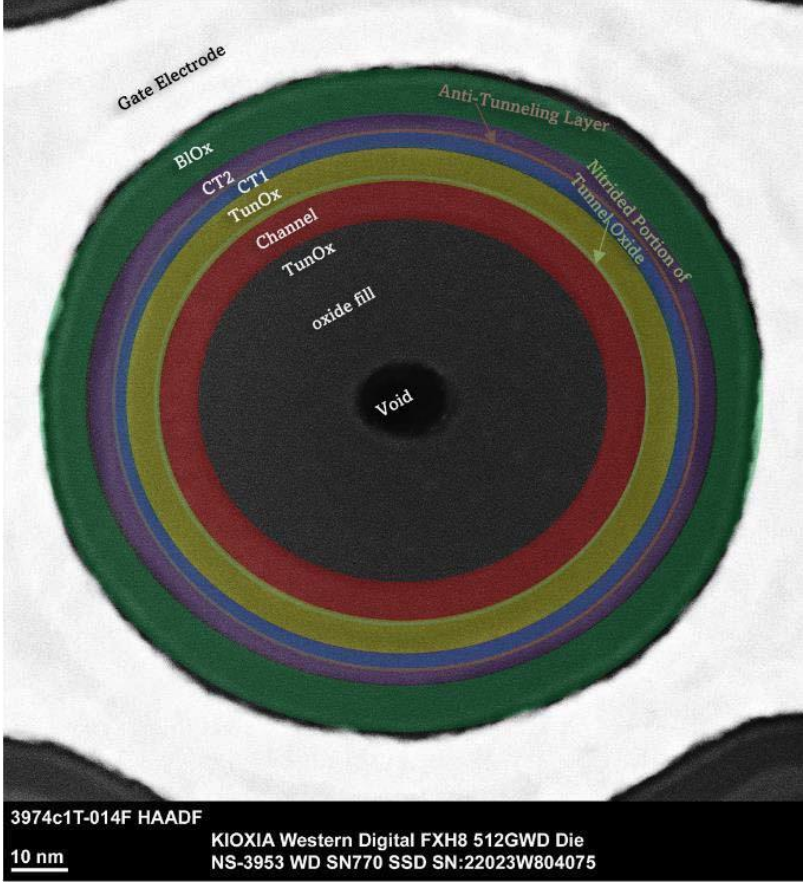
Claim Element	'365 Accused Instrumentalities
4. The method of claim 1, wherein the second dielectric layer separates the sacrificial layer from an overlying memory transistor.	In the method of manufacturing the '365 Accused Instrumentalities the second dielectric layer separates the sacrificial layer from an overlying memory transistor. For example, the second dielectric layer separates the sacrificial layer from an overlying memory transistor²³:  The diagram illustrates a cross-section of a memory array. It shows a substrate at the bottom, followed by a TiN layer, a Si substrate, and a SiO₂ layer. Above these is a W layer, followed by a SiO₂ layer, a 7 nm layer, and a 15 nm layer. A large purple region represents the first dielectric layer, which is 150 nm thick. Above this is a green layer representing the sacrificial layer, which is 150 nm thick. Above the sacrificial layer is a red layer representing the second dielectric layer, which is 150 nm thick. Above the second dielectric layer is a memory transistor, which is 150 nm thick. The memory transistor is composed of a SiO₂ layer, a W layer, and a SiO₂ layer. The WL pitch is 150 nm, which is equal to 150/3 = 50 nm. The diagram also shows a SEG layer, a void, and a 50 nm scale bar. The Tech Insign logo is in the bottom right corner.
5. The method of claim 1, wherein the blocking dielectric layer includes a high K dielectric.	In the method of manufacturing the '365 Accused Instrumentalities the blocking dielectric layer includes a high K dielectric. For example, the blocking dielectric layer (“BLOx”) comprises aluminum oxide, a high K high temperature oxide.

²³ TechInsights 112L Report

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
6. The method of claim 1, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.	In the method of manufacturing the '365 Accused Instrumentalities the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer. For example, the multi-layer charge storing region includes an oxygen-lean nitride layer ("CT2" or "CT1") and an oxygen-rich nitride layer ("CT1" or "CT2") ²⁴ :

²⁴ TechInsights 112L Report

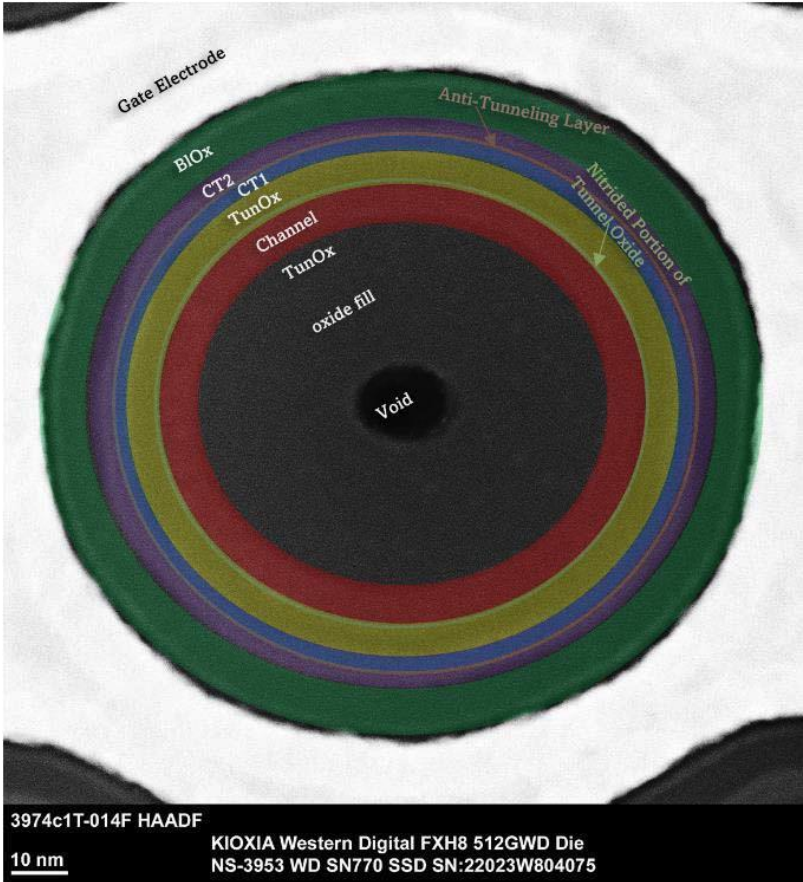
Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
7. The method of claim 6,	
[7a] wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and	In the method of manufacturing the '365 Accused Instrumentalities the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer. For example, the

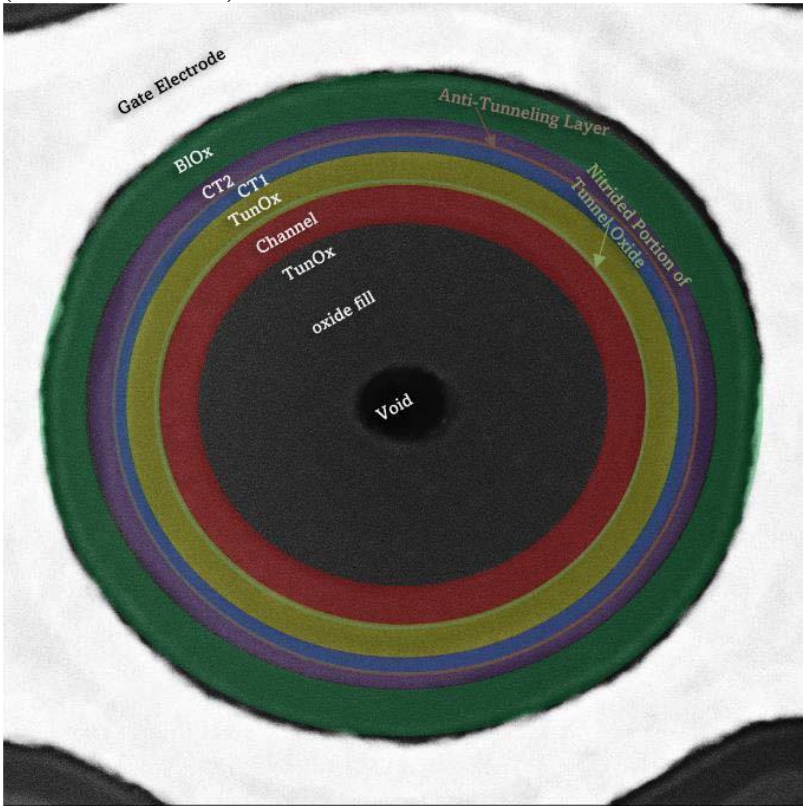
Claim Element	'365 Accused Instrumentalities
	oxygen-lean nitride layer ("CT2") is formed on the inside sidewall of the blocking dielectric layer ("BlOx")²⁵:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

²⁵ TechInsights 112L Report

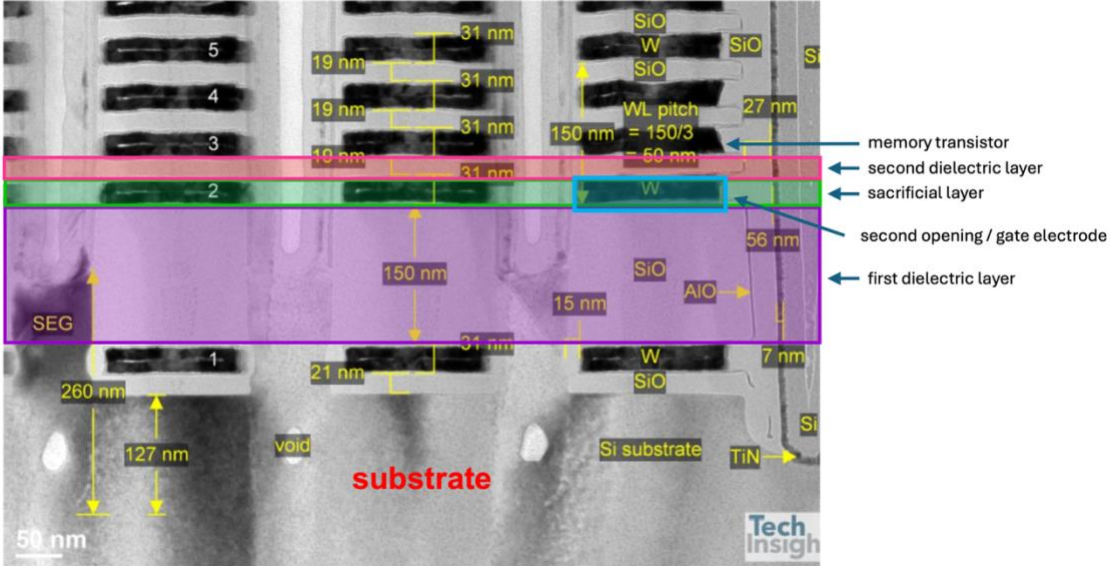
<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[7b] wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.	In the method of manufacturing the '365 Accused Instrumentalities the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer. For example, the oxygen-rich nitride layer ("CT1") is formed on the inside sidewall of the oxygen-lean nitride layer ("CT2") ²⁶ :

²⁶ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
8. The method of claim 6, further comprising forming an anti-tunneling	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich

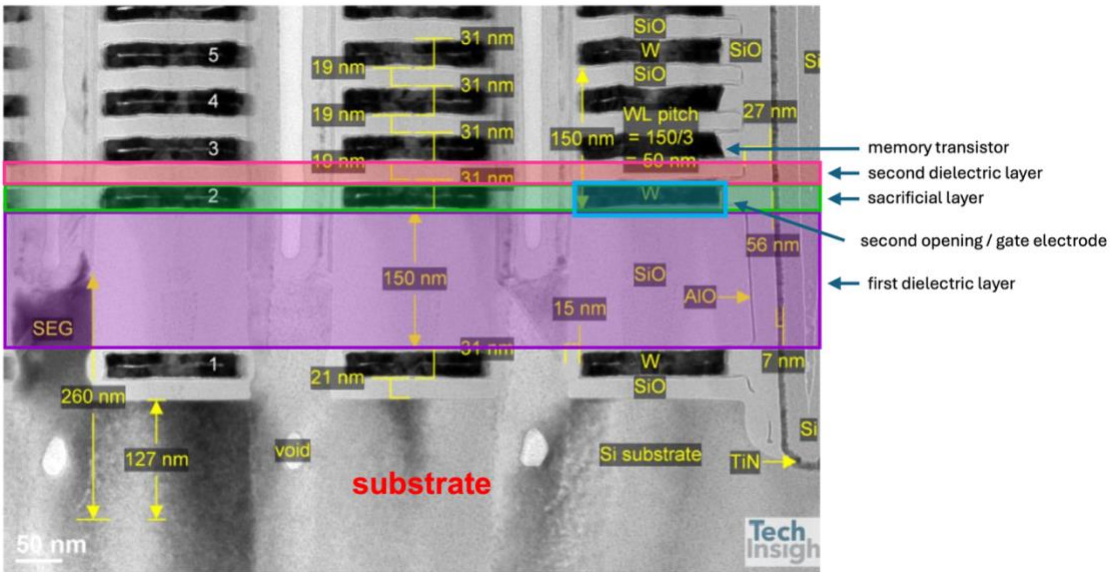
Claim Element	'365 Accused Instrumentalities
layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.	nitride layer. For example, an anti-tunneling layer (“Anti-Tunneling Layer”) is formed between the oxygen-lean nitride layer (“CT2” or “CT1”) and the oxygen-rich nitride layer (“CT1” or “CT2”) ²⁷:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

²⁷ TechInsights 112L Report

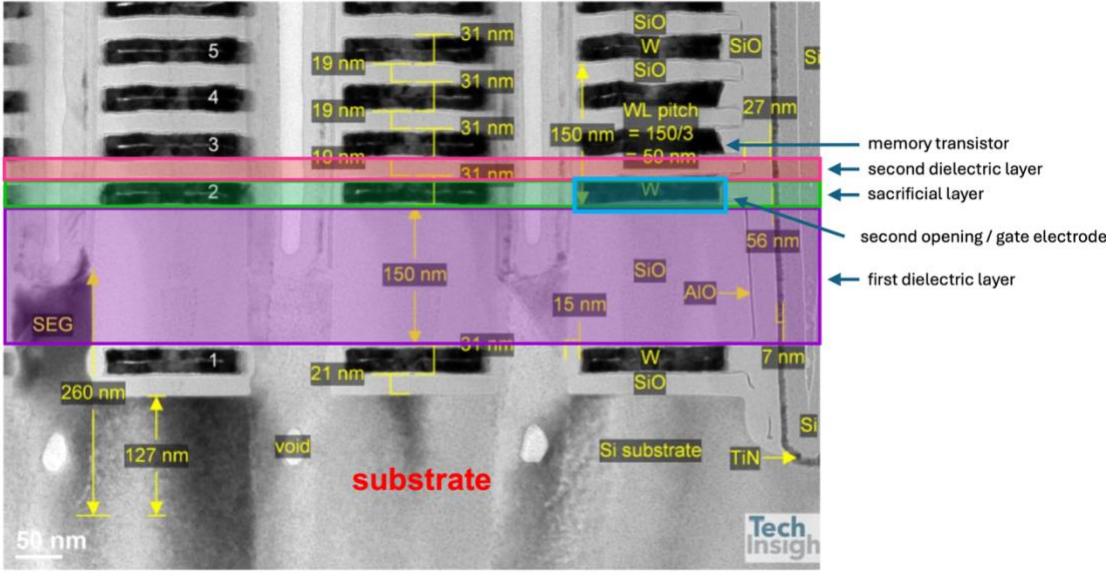
Claim Element	'365 Accused Instrumentalities
9. The method of claim 1, further comprising the step of etching the sacrificial layer to form a second opening.	The method of manufacturing the '365 Accused Instrumentalities includes a step of etching the sacrificial layer to form a second opening. For example, the sacrificial layer is etched to form a second opening where a tungsten gate will be deposited²⁸:  The diagram illustrates a cross-section of a memory transistor. Key layers and dimensions include: a Si substrate at the base; a TiN layer (7 nm) on the substrate; a first dielectric layer (SiO₂, 15 nm) with an AlO_x layer (56 nm) on top; a second opening / gate electrode (W, 150 nm) filled with tungsten; a sacrificial layer (SiO₂, 19 nm) above the gate; a second dielectric layer (SiO₂, 31 nm) above the sacrificial layer; and a memory transistor (W, 31 nm) on top. Other dimensions shown are 260 nm, 127 nm, 21 nm, 31 nm, 19 nm, 27 nm, and 150 nm. A scale bar indicates 50 nm. Labels include SEG, void, Si substrate, TiN, and TechInsights.
10. The method of claim 9, further comprising the step of depositing a gate electrode in the second opening.	The method of manufacturing the '365 Accused Instrumentalities includes a step of depositing a gate electrode in the second opening. For example, a gate electrode (tungsten) is deposited in the second opening²⁹:

²⁸ TechInsights 112L Report

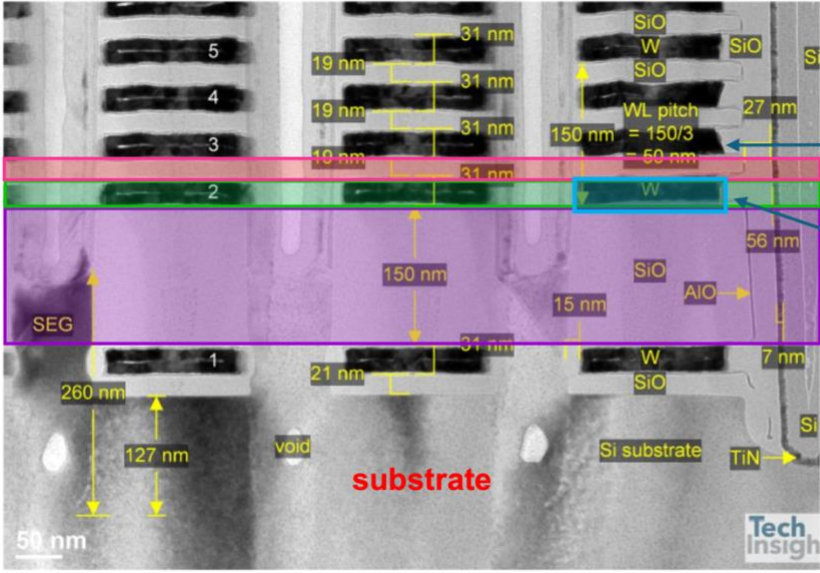
²⁹ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 The diagram shows a cross-section of a memory device. From bottom to top, the layers are: a Si substrate with a TiN layer (7 nm), a first dielectric layer (56 nm), a second opening / gate electrode (15 nm), a sacrificial layer (150 nm), a second dielectric layer (150 nm), and a memory transistor (150 nm). The transistor has a WL pitch of 150 nm, which is divided into three 50 nm segments. Other dimensions include 31 nm, 19 nm, 27 nm, 21 nm, 260 nm, and 127 nm. Labels include SEG, void, Si substrate, TiN, SiO, W, and AIO. A 50 nm scale bar is present. The TechInsights logo is in the bottom right corner.
11. The method of claim 10, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.	In the method of manufacturing the '365 Accused Instrumentalities the second dielectric layer separates the gate electrode from an overlying memory transistor. For example, the second dielectric layer separates the gate electrode from an overlying memory transistor³⁰:

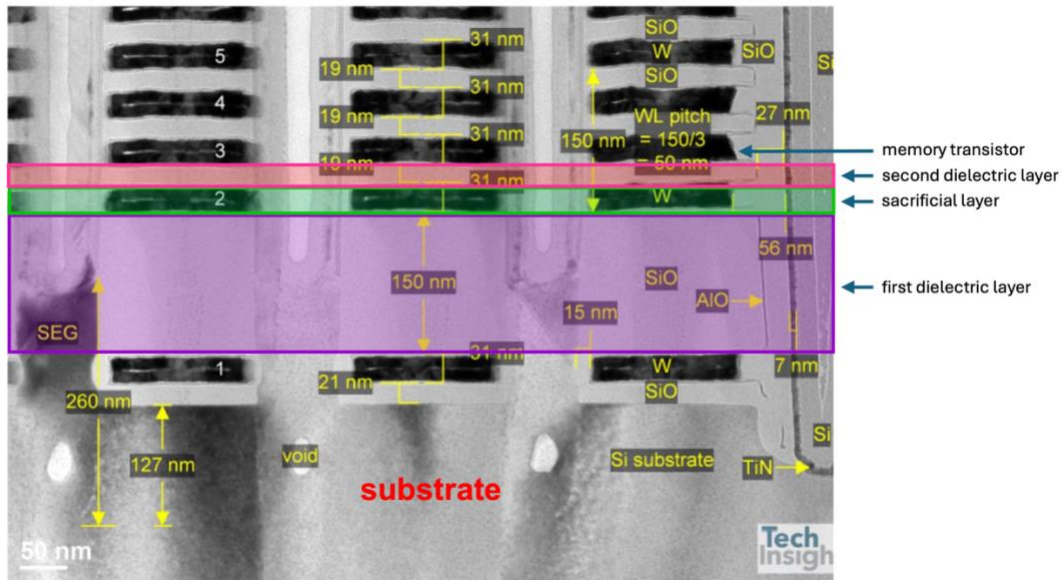
³⁰ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 The diagram shows a cross-section of a memory device. From top to bottom, the layers are: a memory transistor (5 nm), a second dielectric layer (19 nm), a sacrificial layer (31 nm), a second opening / gate electrode (19 nm), and a first dielectric layer (31 nm). The gate electrode is labeled 'W' (tungsten) and has a width of 150 nm. The dielectric layers are labeled 'SiO' and 'Si'. The substrate is labeled 'Si substrate' and 'TiN'. Other dimensions include 27 nm, 150 nm, 50 nm, 56 nm, 15 nm, 7 nm, 21 nm, 31 nm, 127 nm, and 260 nm. A 'void' is indicated in the substrate. The 'SEG' (source/drain extension gate) is also shown. A scale bar of 50 nm is provided. The TechInsights logo is in the bottom right corner.
12. The method of claim 10, wherein the deposited gate electrode is a high work function gate electrode.	In the method of manufacturing the '365 Accused Instrumentalities the deposited gate electrode is a high work function gate electrode. For example, the deposited gate electrode is tungsten, a high work function material ³¹ :

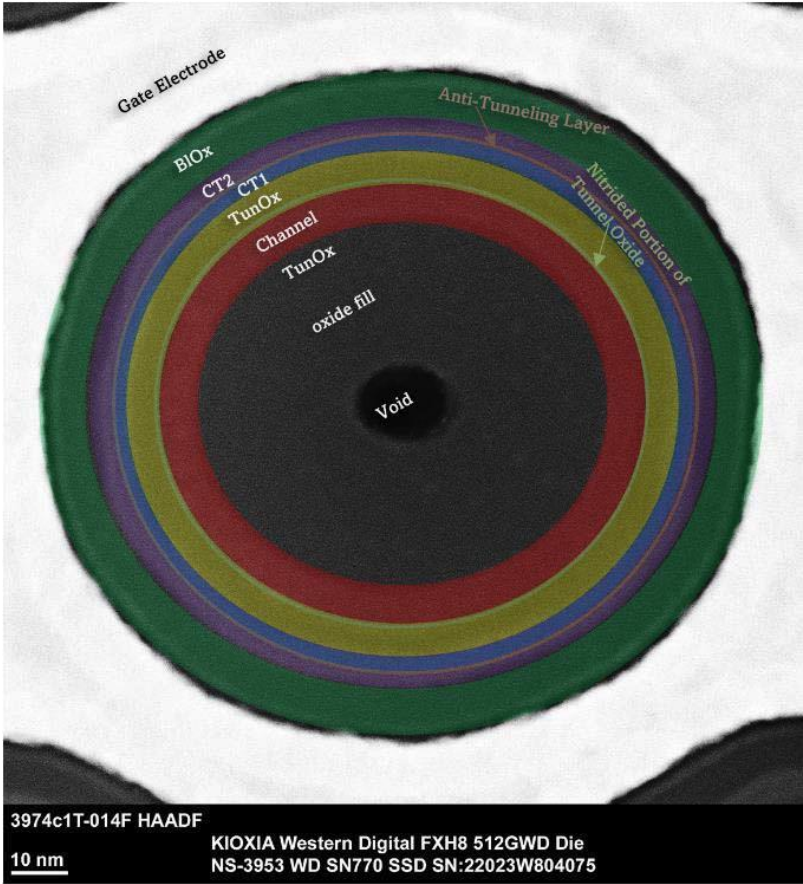
³¹ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 The diagram shows a cross-section of a memory device. Key layers and dimensions include: a Si substrate at the base; a TiN layer (7 nm); a first dielectric layer (56 nm); a second opening / gate electrode (15 nm); a second dielectric layer (150 nm); a sacrificial layer (31 nm); a memory transistor (19 nm); and a WL pitch (150 nm = 150/3 = 50 nm). Other labels include SEG, void, and SiO₂. A 50 nm scale bar is present.
13. The method of claim 4, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.	In the method of manufacturing the '365 Accused Instrumentalities the second dielectric layer separates the gate electrode from an overlying memory transistor. For example, the second dielectric layer separates the gate electrode from an overlying memory transistor³²:

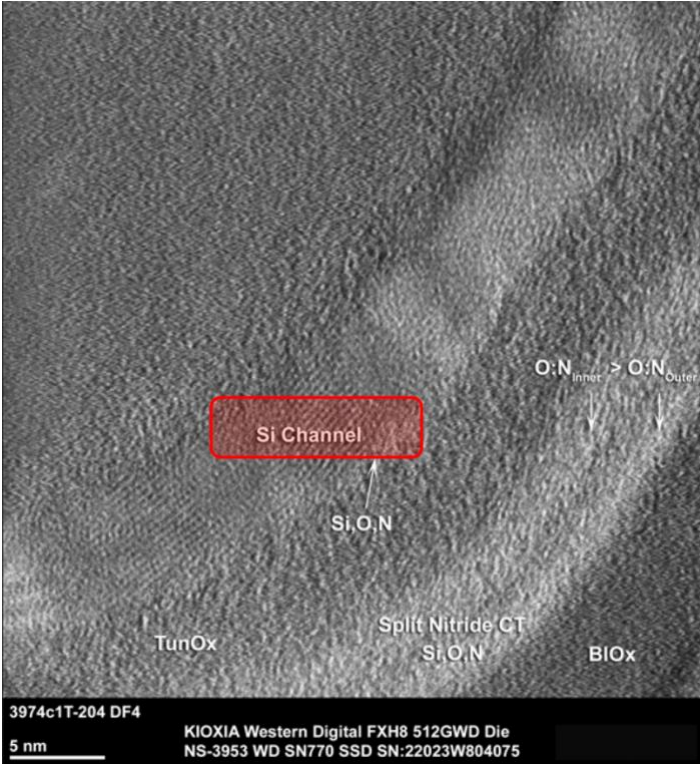
³² TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 The diagram shows a cross-section of a memory device. Key layers and dimensions include: a Si substrate at the base; a TiN layer (7 nm); a SiO₂ layer; a W layer; a SiO₂ layer; a WL pitch of 150 nm (divided into 150/3 = 50 nm); a 27 nm layer; a 150 nm layer; a 31 nm layer; a 19 nm layer; a 10 nm layer; a 31 nm layer; a 150 nm layer; a 56 nm layer; a 15 nm layer; a 31 nm layer; a 21 nm layer; a 260 nm layer; a 127 nm layer; a void; a SEG layer; and a substrate. The structure is divided into five horizontal regions labeled 1 through 5. A 50 nm scale bar is shown at the bottom left. The TechInsights logo is at the bottom right. Labels on the right side of the diagram: - memory transistor - second dielectric layer - sacrificial layer - first dielectric layer
14. The method of claim 1, wherein the vertical channel formed includes an annular region.	In the method of manufacturing the '365 Accused Instrumentalities the vertical channel formed includes an annular region. For example, the vertical channel formed includes an annular region ("Channel") ³³ :

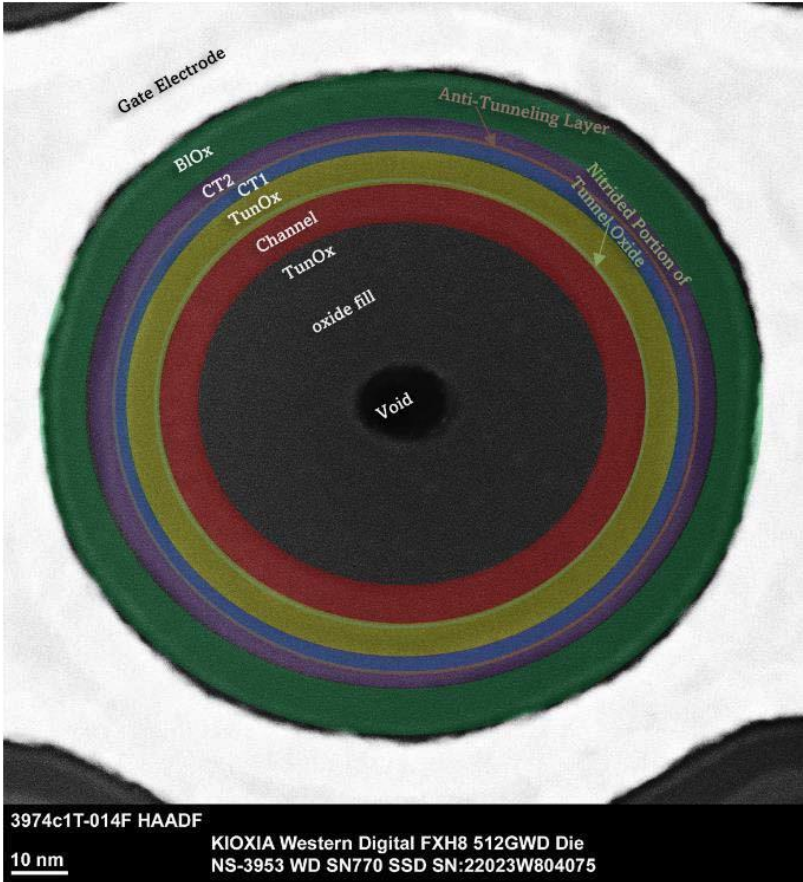
³³ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
15. The method of claim 14, wherein at least a portion of the vertical channel is formed of polysilicon.	In the method of manufacturing the '365 Accused Instrumentalities at least a portion of the vertical channel is formed of polysilicon. For example, at least a portion of the "Si Channel" is polysilicon³⁴:

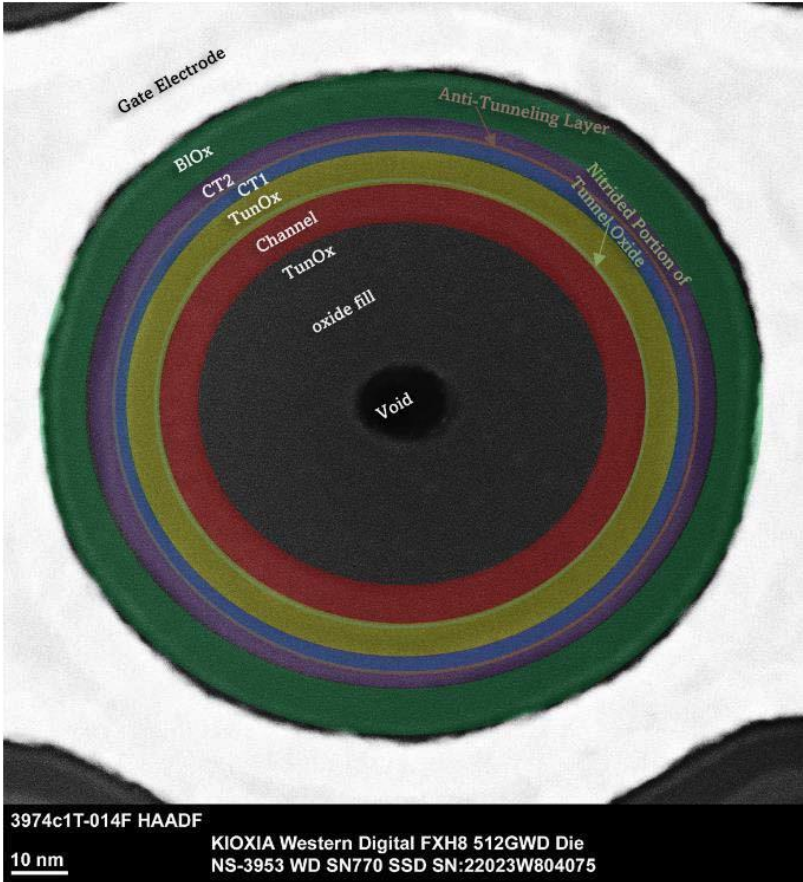
³⁴ *Id.*

Claim Element	'365 Accused Instrumentalities
	
16. The method of claim 14, wherein the vertical channel formed includes a layer of semiconductor material surrounding a cylinder of filler material.	In the method of manufacturing the '365 Accused Instrumentalities the vertical channel formed includes a layer of semiconductor material surrounding a cylinder of filler material. For example, the vertical channel formed includes a layer of semiconductor material ("Channel") surrounding a cylinder of filler material ("oxide fill")³⁵:

³⁵ TechInsights 112L Report

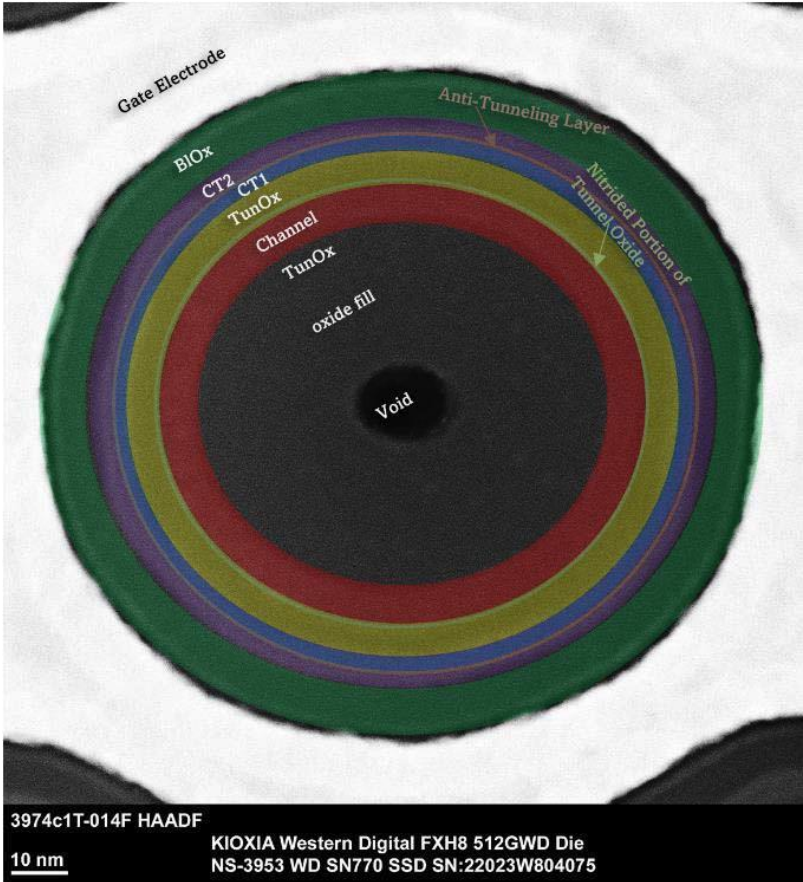
Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
19. The method of claim 14, wherein the blocking dielectric layer is formed in a substantially annular shape.	In the method of manufacturing the '365 Accused Instrumentalities the blocking dielectric layer is formed in a substantially annular shape. For example, the blocking dielectric layer ("BLOx") is formed in a substantially annular shape³⁶:

³⁶ TechInsights 112L Report

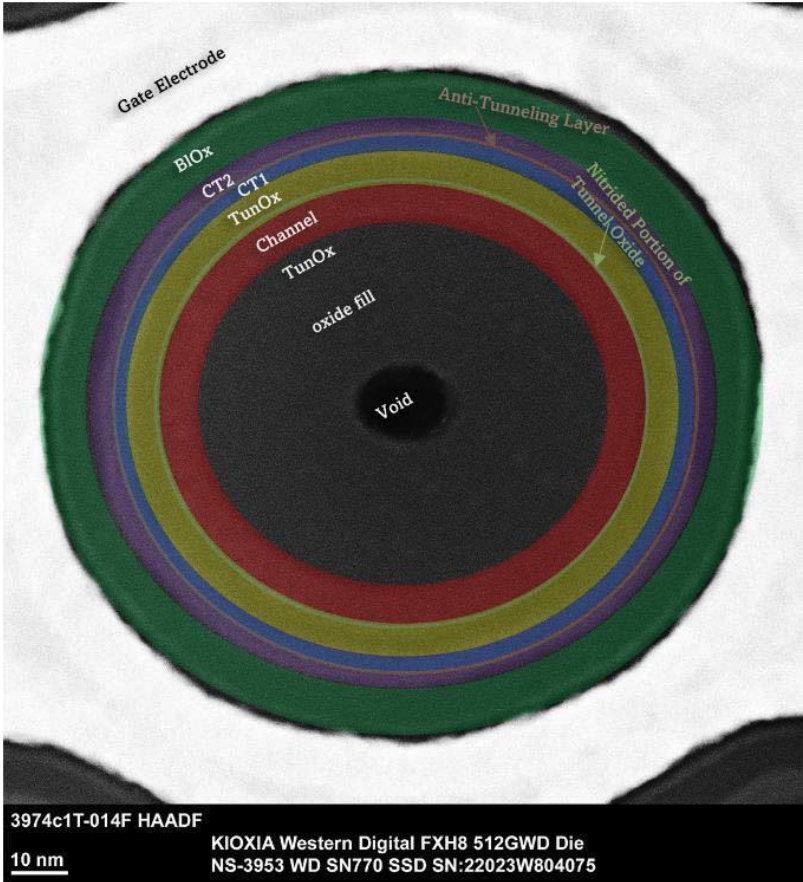
Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
20. The method of claim 19, wherein the blocking dielectric layer includes a high K dielectric.	In the method of manufacturing the '365 Accused Instrumentalities the blocking dielectric layer includes a high K dielectric. For example, the blocking dielectric layer ("BLOx") comprises aluminum oxide, a high K high temperature oxide.

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
21. The method of claim 19, wherein the multi-layer charge storing region is formed in a substantially annular shape.	In the method of manufacturing the '365 Accused Instrumentalities the multi-layer charge storing region is formed in a substantially annular shape. For example, the multi-layer charge storing region ("CT1," "Anti-Tunneling Layer," "CT2") is formed in a substantially annular shape ³⁷ :

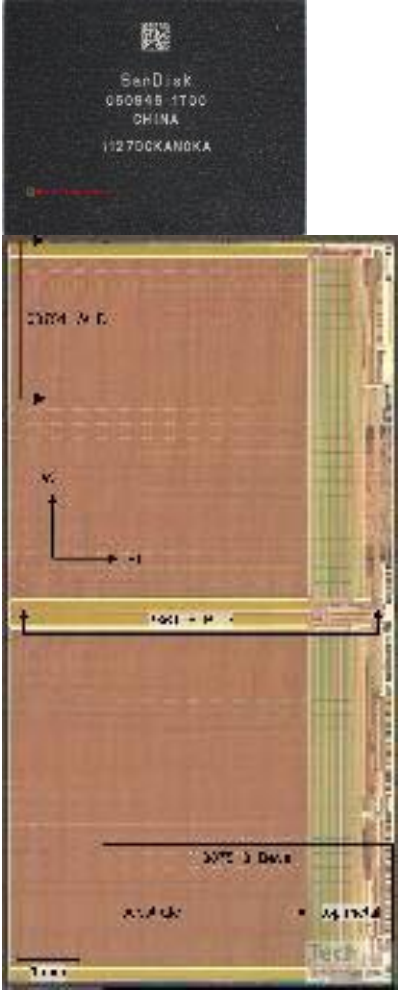
³⁷ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
22. The method of claim 21, wherein the tunnel dielectric layers is formed in a substantially annular shape.	In the method of manufacturing the '365 Accused Instrumentalities the tunnel dielectric layers is formed in a substantially annular shape. For example, the tunnel dielectric layers ("TunOx") is formed in a substantially annular shape³⁸:

³⁸ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
23. A method comprising:	The '365 Accused Instrumentalities are manufactured using the claimed method. For example, the WDS960G2G0C SSD contains a semiconductor die containing 112-Layer 3D NAND Flash Memory ³⁹ :

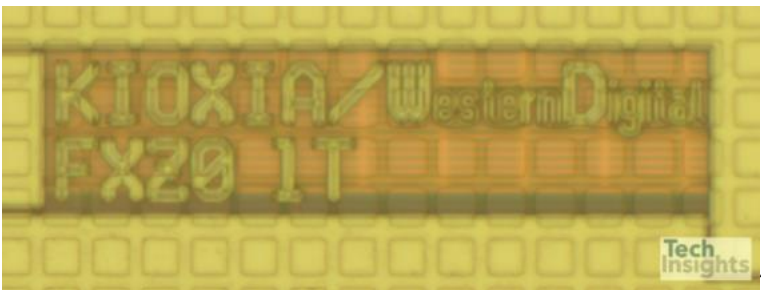
³⁹ TechInsights, Kioxia/Western Digital WDS960G2G0C SSD, SanDisk 060946 1T00 (FXH8 512G Die), 112-Layer 3D NAND Flash Memory, 18 nm Process Node, Advanced Memory Essentials, AME-2106-802, Published: November 19, 2021 ("TechInsights 112L Report")

Claim Element	'365 Accused Instrumentalities
	 Die markings on this and other '365 Accused Instrumentalities indicate that they are each made by a joint venture owned by Toshiba/Kioxia and Sandisk/Western Digital:

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	 TOSHIBA/SANDISK FST0 256G Tech Insights 12 Package Optical - Package X-ray - Die Optical\TH58LJT0T24BADE_FST0_256G_336534_DieMik-100X.png 40  KIOXIA/Umicore FXH9 S12G Tech Insights 41

⁴⁰ Image of Western Digital Green SSD (P/N WDS480G2G0A) (96L)

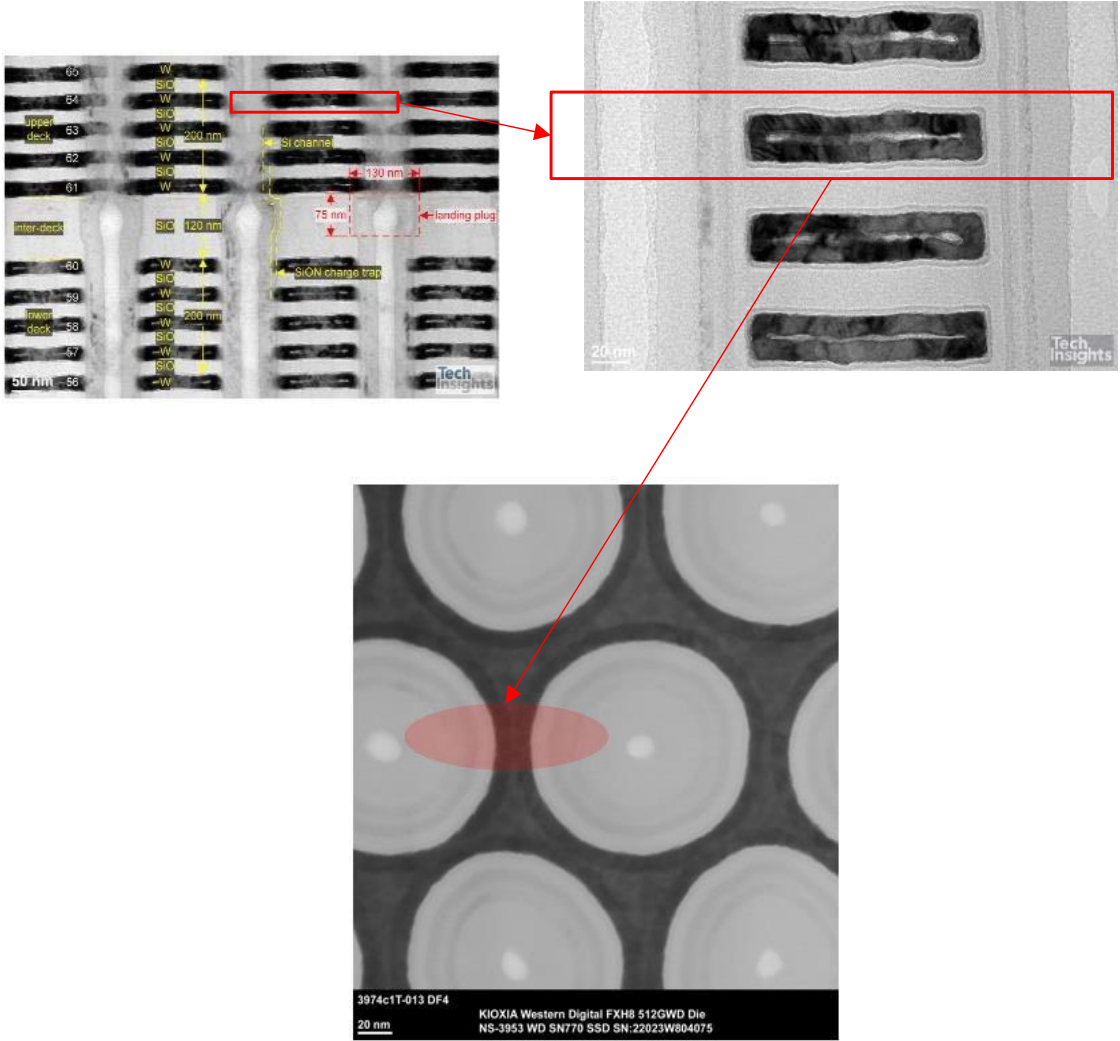
⁴¹ TechInsights 112L Report

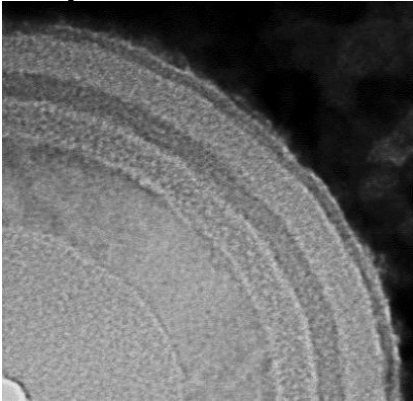
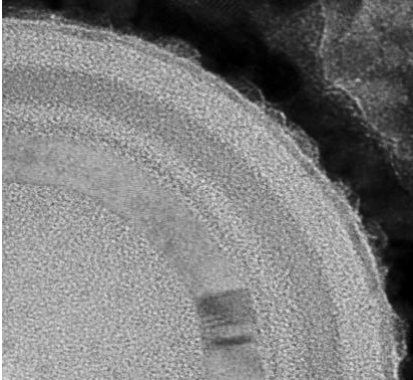
Claim Element	'365 Accused Instrumentalities
	 42  43 The following images each show multiple memory transistors, in different cross sections of a 112L accused product⁴⁴:

⁴² TechInsights, Toshiba TH58LKT3B46BA8S (KIOXIA/Western Digital Corp. FXZ0_1T die), 162-Layer 3D NAND Flash Memory, Advanced Memory Essentials, AME-2310-803, Published: February 29, 2024 (“TechInsights 162L Report”)

⁴³ TechInsights, KIOXIA/WDC FYU6_1T 218L (BiCS8), Triple-Level Cell (TLC) 1 Tb 3D NAND Flash, Advanced Memory Essentials, AME-2407-801, Published: November 29, 2024 (“TechInsights 218L Report”)

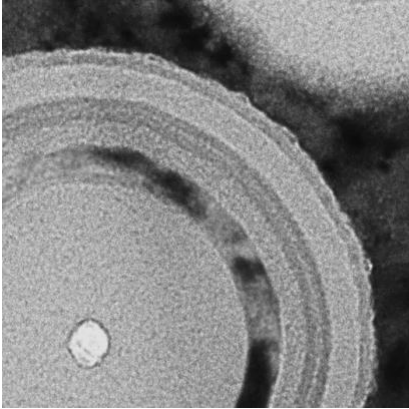
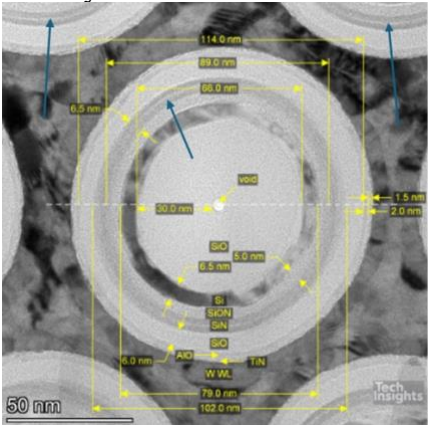
⁴⁴ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	Similar memory transistor structures are present in each of the '365 Accused Instrumentalities, as shown in the following cross section images. 64-layer⁴⁵:  96-layer⁴⁶: 

⁴⁵ TechInsights, Memory DRAM & NAND Tri-Annual Briefing #1, 2022, Report ID: BRF-2112-810, May 2022, p. 47,

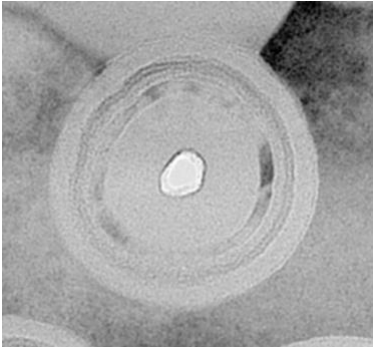
⁴⁶ *Id.*

Claim Element	'365 Accused Instrumentalities
	112-layer⁴⁷:  162-layer⁴⁸:  218-layer⁴⁹:

⁴⁷ *Id.*

⁴⁸ TechInsights 162L Report

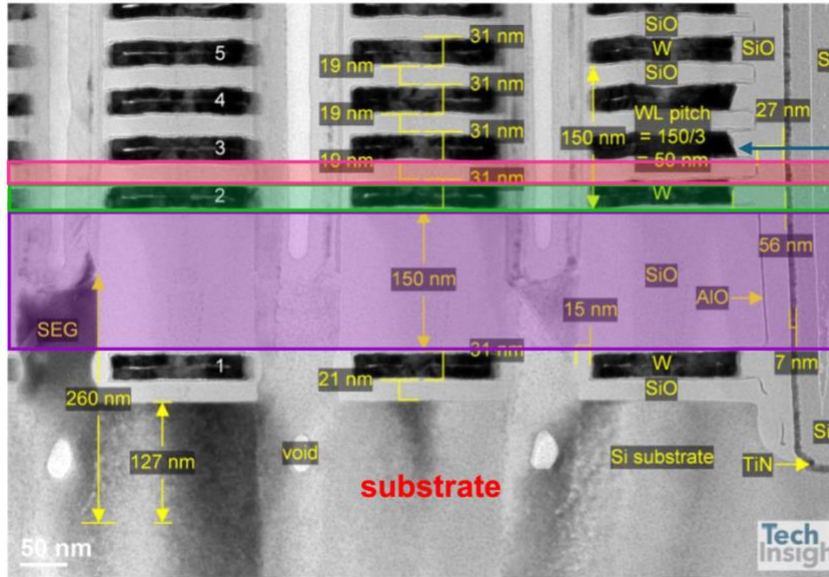
⁴⁹ TechInsights 218L Report

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	
[23a] forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer,	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer. For example, a first dielectric layer, a sacrificial layer, and a second dielectric layer are formed over a silicon substrate⁵⁰:

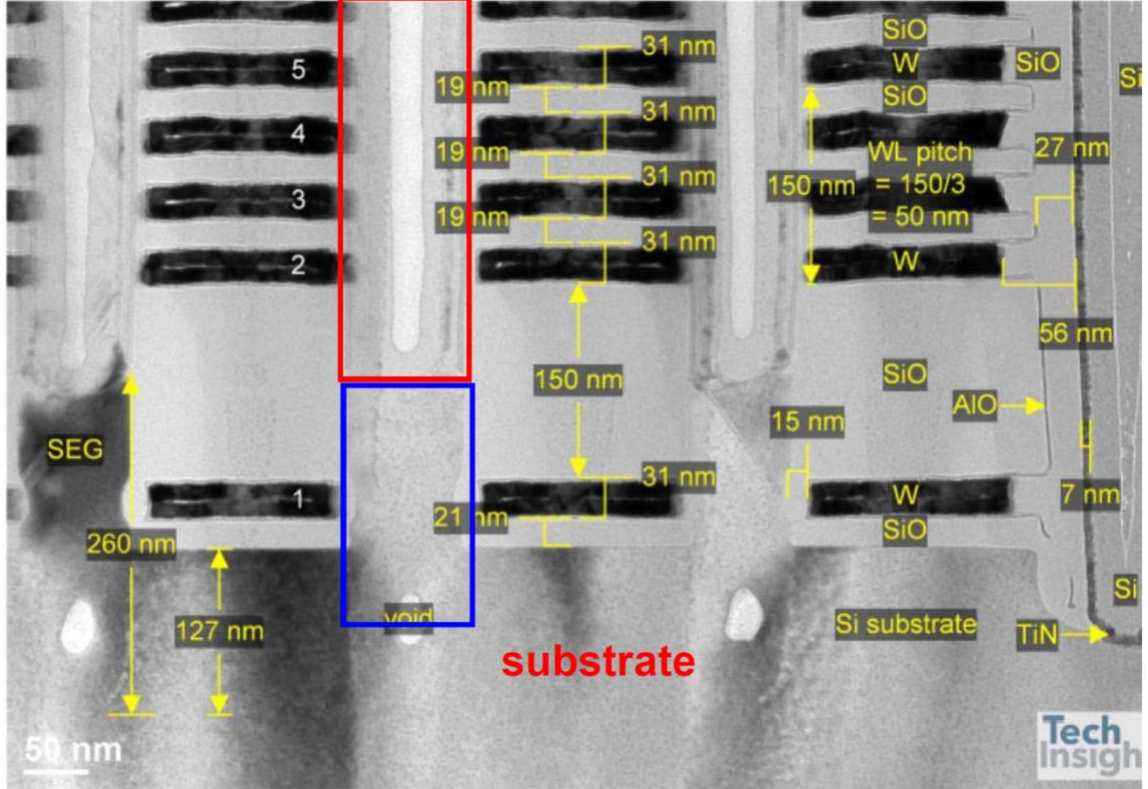
⁵⁰ TechInsights 112L Report

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	The image shows a cross-section of a semiconductor device. At the base is a "substrate" (red label) with a "TiN" layer (7 nm) and "SiO₂". Above this is a stack of layers: "W", "SiO₂", "AIO" (15 nm), "SiO₂", "SEG", "void", and another "SiO₂" layer (127 nm). Horizontal lines representing gates or contacts are labeled 1 through 5. Dimensions include 260 nm, 21 nm, 31 nm, 19 nm, 31 nm, 150 nm, 27 nm, 56 nm, and 7 nm. Labels on the right indicate "memory transistor", "second dielectric layer", "sacrificial layer", and "first dielectric layer". A scale bar of 50 nm is shown at the bottom left.
[23b] wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;	In the method of manufacturing the '365 Accused Instrumentalities the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer. For example, the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer ⁵¹ :

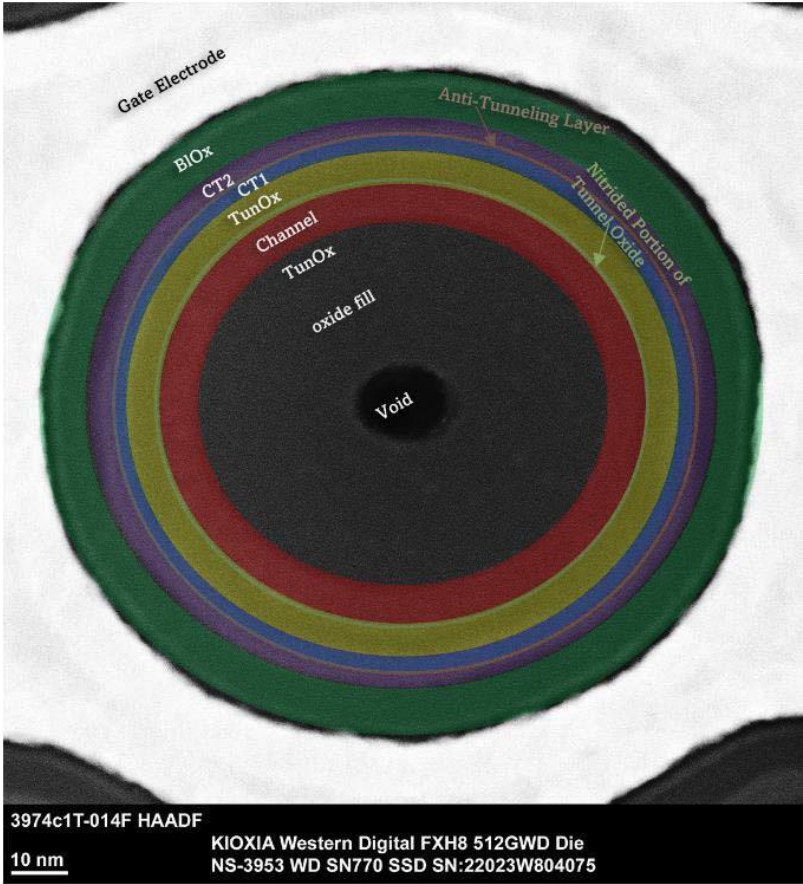
⁵¹ TechInsights 112L Report

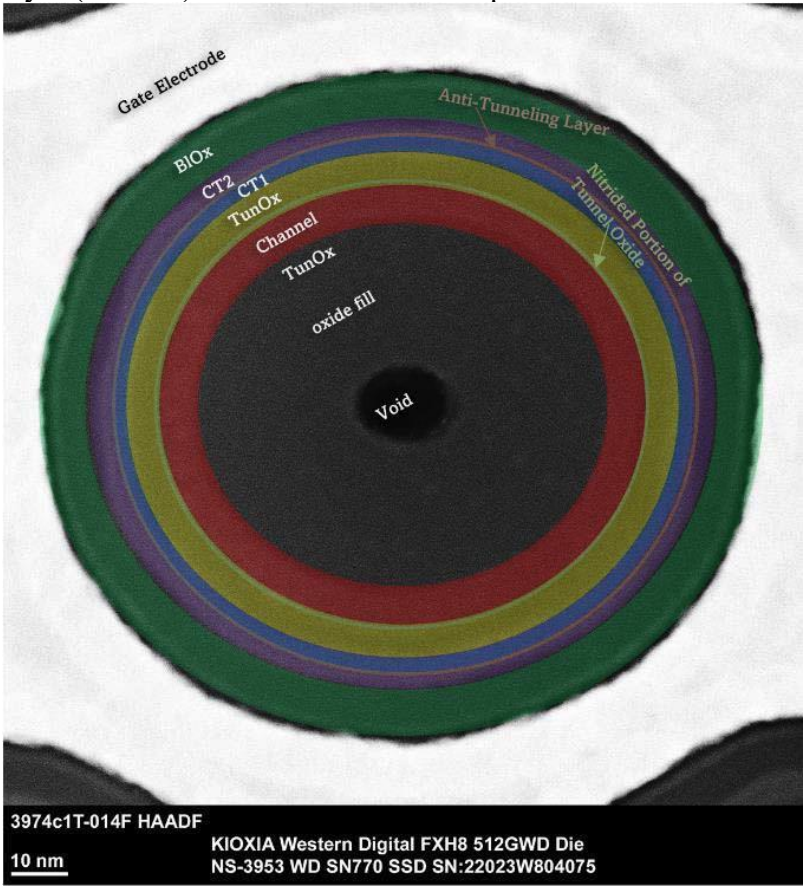
Claim Element	'365 Accused Instrumentalities
	
[23c] forming an opening extending through the stack of layers towards the substrate;	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming an opening extending through the stack of layers towards the substrate. For example, an opening (corresponding to the red rectangle below) is formed extending through the stack of layers to a first doped diffusion region (blue rectangle below) on the silicon substrate⁵²:

⁵² TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	
[23d] forming on sidewalls of the opening an annular shaped blocking dielectric layer;	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming on sidewalls of the opening an annular shaped blocking dielectric layer. For example, an annular shaped blocking dielectric layer ("BIOx") is formed on the sidewalls of the opening⁵³:

⁵³ *Id.*

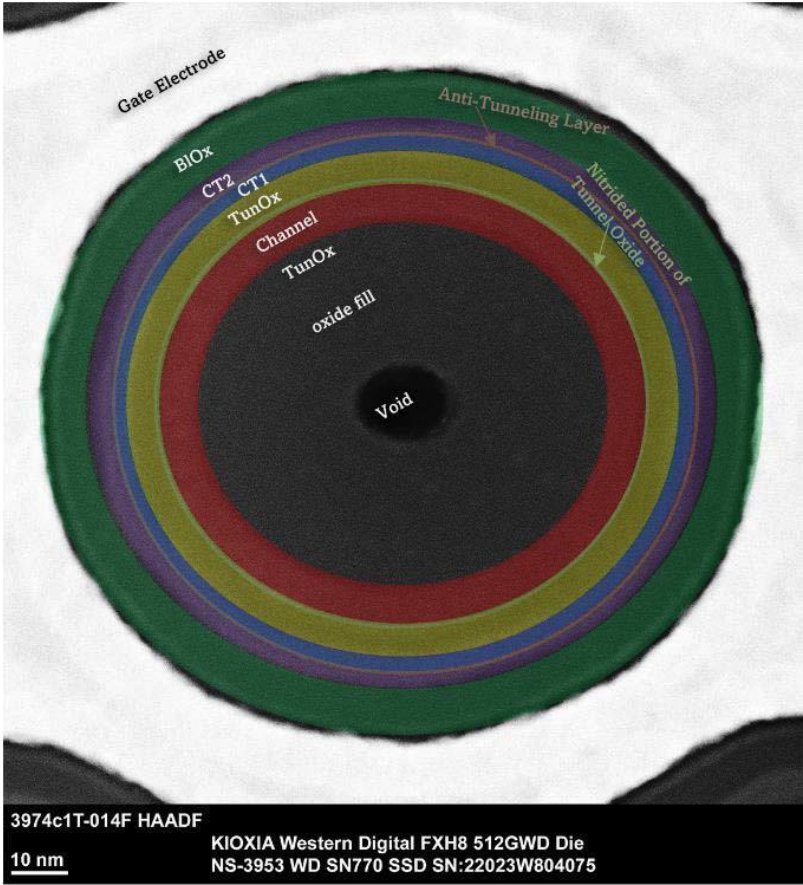
Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[23e] forming on an inside sidewall of the blocking dielectric layer an annular	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming on an inside sidewall of the blocking dielectric layer an annular shaped multi-

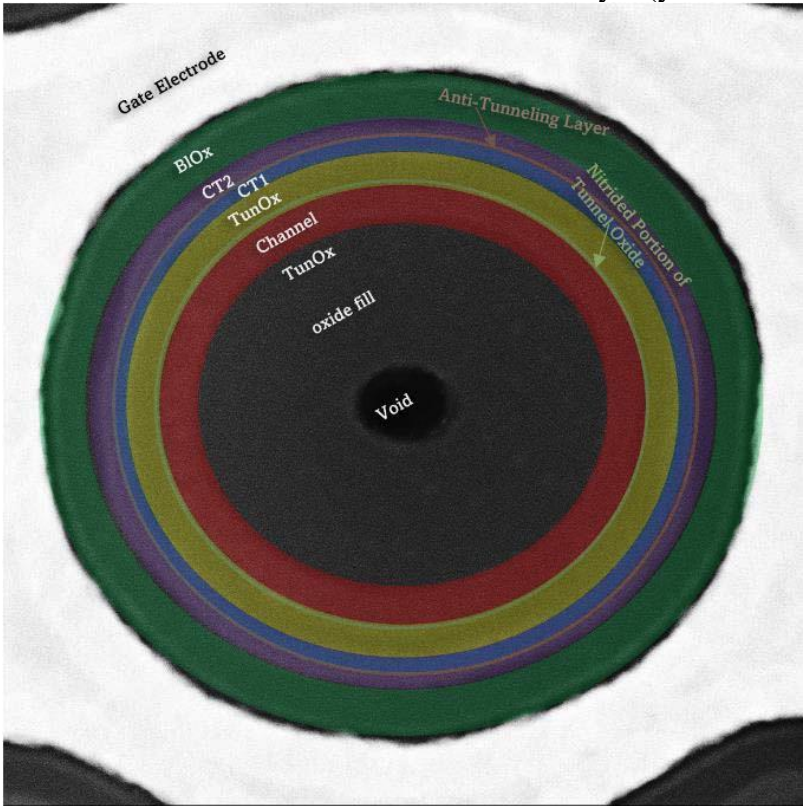
Claim Element	'365 Accused Instrumentalities
shaped multi-layer charge storing region;	layer charge storing region. For example, the multi-layer charge storing region (“CT1,” “Anti-Tunneling Layer,” “CT2”) is formed on an inside sidewall of the blocking dielectric layer (“BIOx”) and has an annular shape ⁵⁴: 

⁵⁴ *Id.*

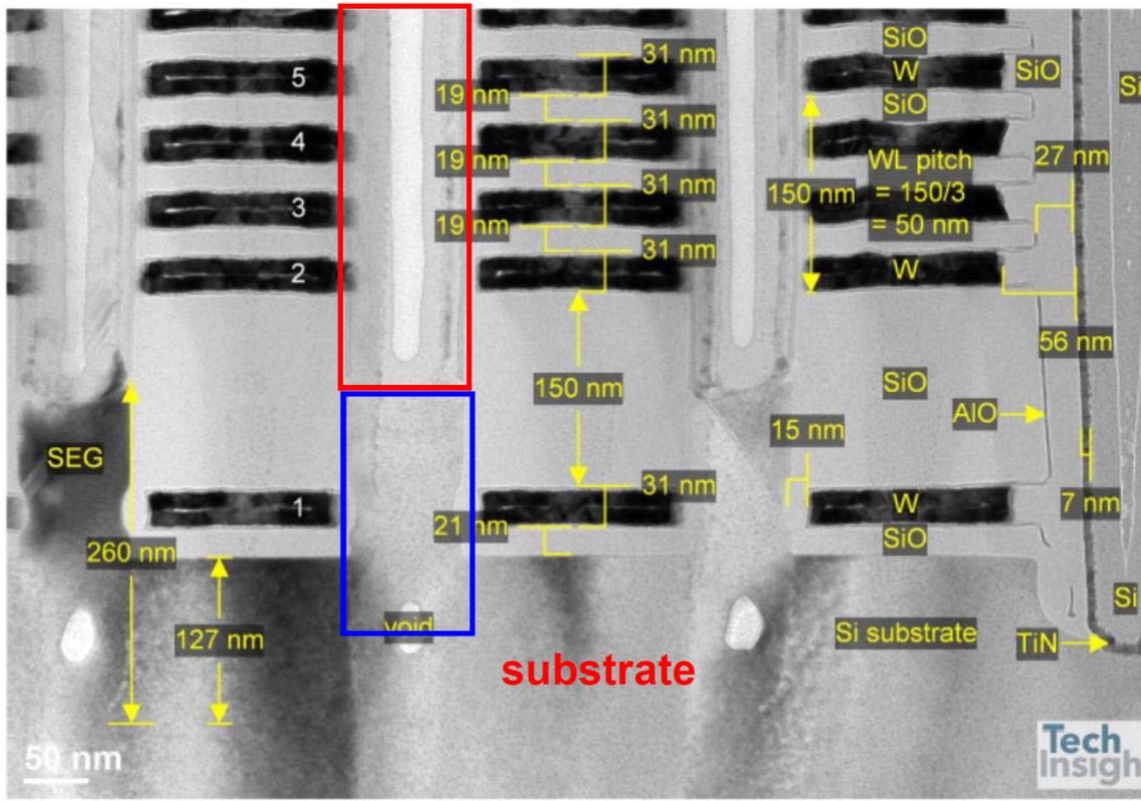
<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[23f] forming on an inside sidewall of the multi-layer charge storing region an annular shaped tunnel dielectric layer; and	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming on an inside sidewall of the multi-layer charge storing region an annular shaped tunnel dielectric layer. For example, the tunnel dielectric layer (yellow "TunOx") is formed on an inside sidewall of the multi-layer charge storing region ("CT1," "Anti-Tunneling Layer," "CT2") and has an annular shape ⁵⁵ :

⁵⁵ *Id.*

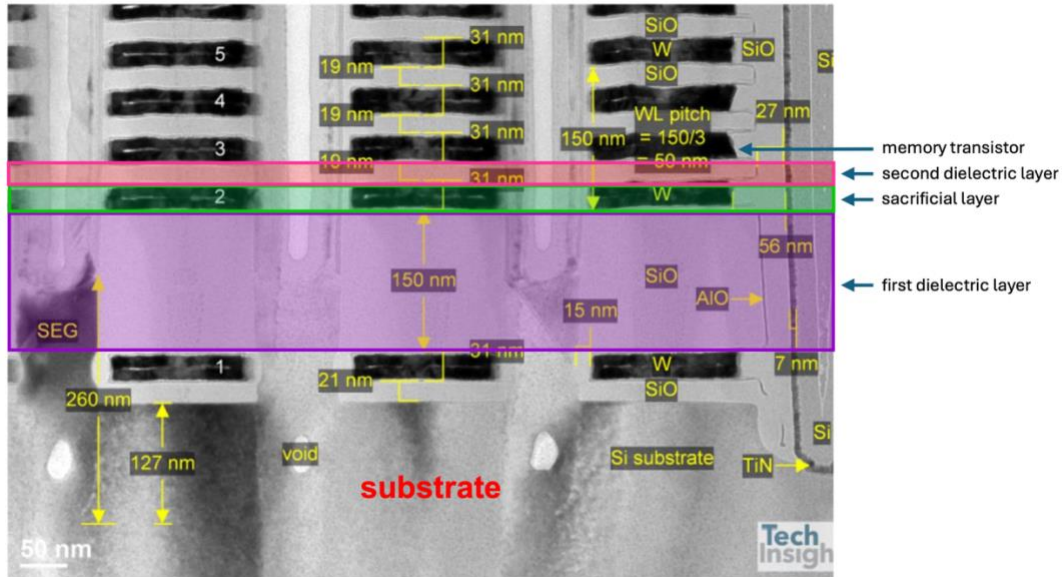
Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[23g] forming on an inside sidewall of the tunnel dielectric layer an annular	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical

Claim Element	'365 Accused Instrumentalities
shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layers.	channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layers. For example, the silicon channel (“Channel”) is formed on an inside sidewall of the tunnel dielectric layer (yellow “TunOx”) ⁵⁶:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

⁵⁶ *Id.*

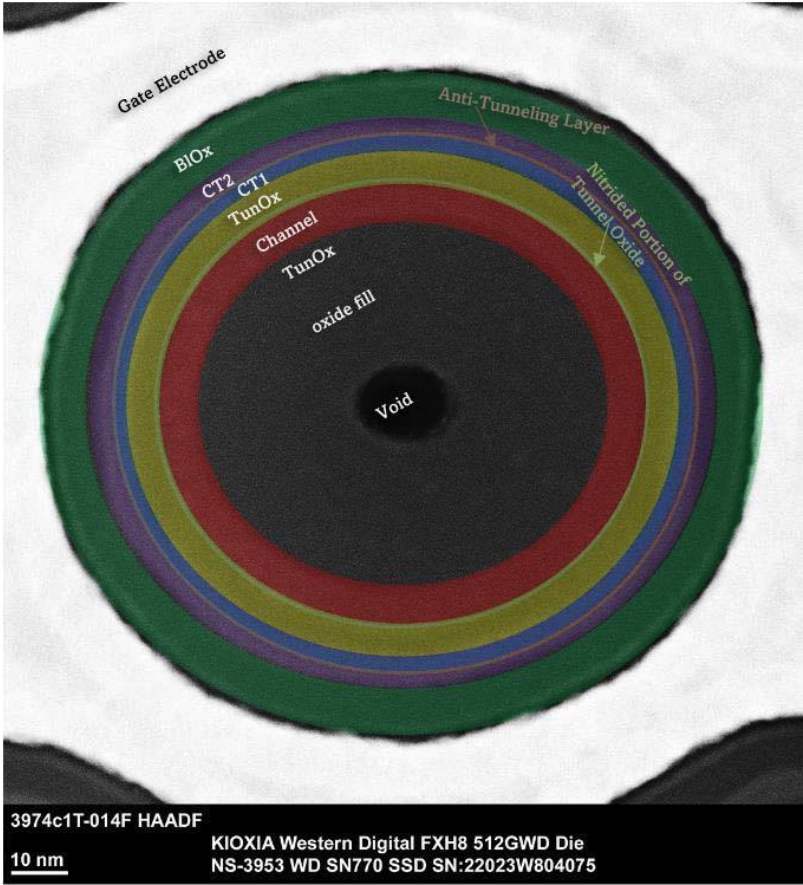
Claim Element	'365 Accused Instrumentalities
	The channel extends from the substrate through the opening to the top of the stack of layers⁵⁷:  As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.

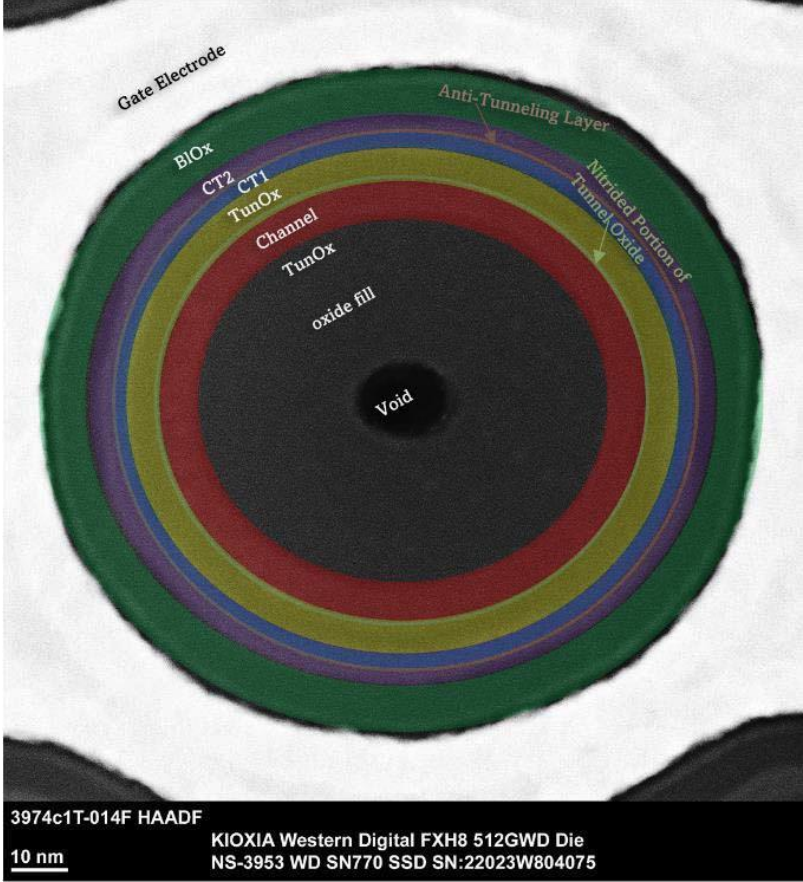
⁵⁷ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
24. The method of claim 23, wherein the second dielectric layer separates the sacrificial layer from an overlying memory transistor.	In the method of manufacturing the '365 Accused Instrumentalities the second dielectric layer separates the sacrificial layer from an overlying memory transistor⁵⁸:  The diagram is a cross-sectional view of a memory device. It shows a substrate at the bottom, labeled 'substrate' in red. Above the substrate is a 'Si substrate' layer. A 'TIN' layer is shown on the right. A 'void' is indicated in the center. A 'SEG' (Source Electrode Gate) is on the left. The structure includes a 'memory transistor' at the top, which is separated from a 'sacrificial layer' by a 'second dielectric layer'. The 'first dielectric layer' is below the sacrificial layer. Various layers are labeled with their thicknesses: 5, 4, 3, 2, 1, 31 nm, 19 nm, 10 nm, 150 nm, 27 nm, 56 nm, 15 nm, 7 nm, 21 nm, 31 nm, 260 nm, 127 nm, 50 nm. A 'WL pitch' is indicated as 150 nm = 150/3. A 'W' layer is shown. The diagram is credited to 'Tech Insights'.
25. The method of claim 23, wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.	In the method of manufacturing the '365 Accused Instrumentalities the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer. For example, the multi-layer charge storing region includes an oxygen-lean nitride layer ("CT2" or "CT1") and an oxygen-rich nitride layer ("CT1" or "CT2")⁵⁹:

⁵⁸ TechInsights 112L Report

⁵⁹ TechInsights 112L Report

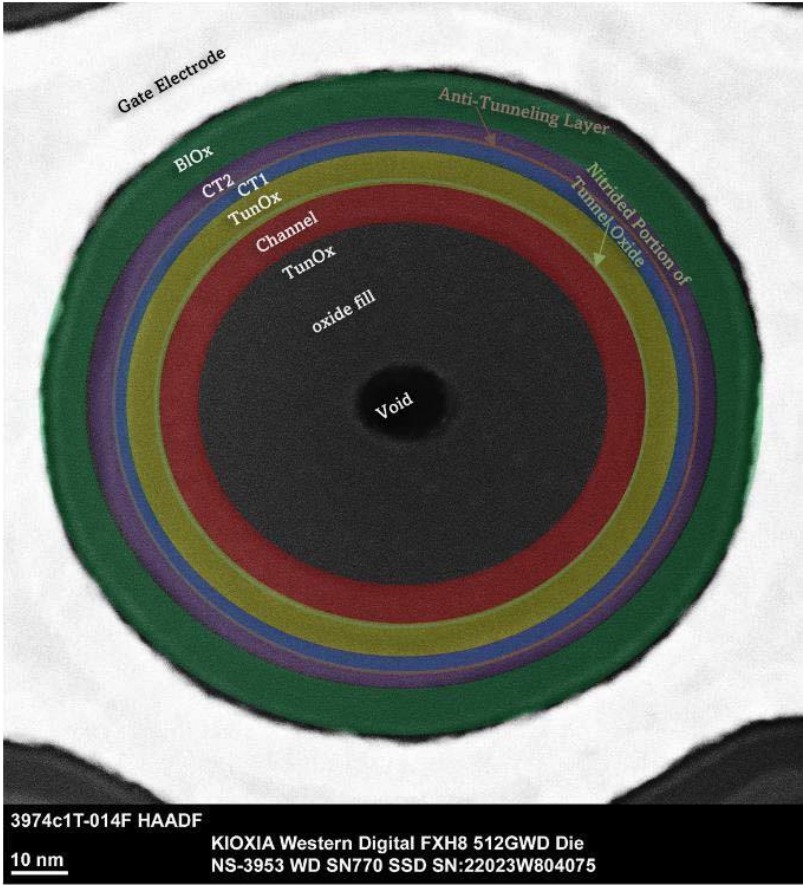
Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
26. The method of claim 25,	
[26a] wherein the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer and	In the method of manufacturing the '365 Accused Instrumentalities the oxygen-lean nitride layer is formed on the inside sidewall of the blocking dielectric layer. For example, the

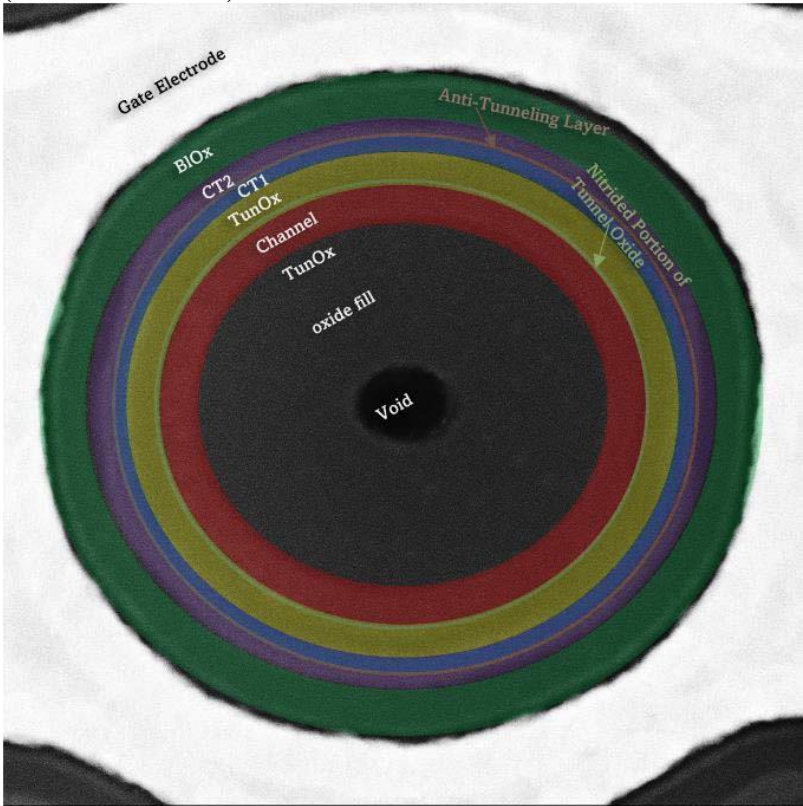
Claim Element	'365 Accused Instrumentalities
	oxygen-lean nitride layer (“CT2”) is formed on the inside sidewall of the blocking dielectric layer (“BlOx”) ⁶⁰:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

⁶⁰ TechInsights 112L Report

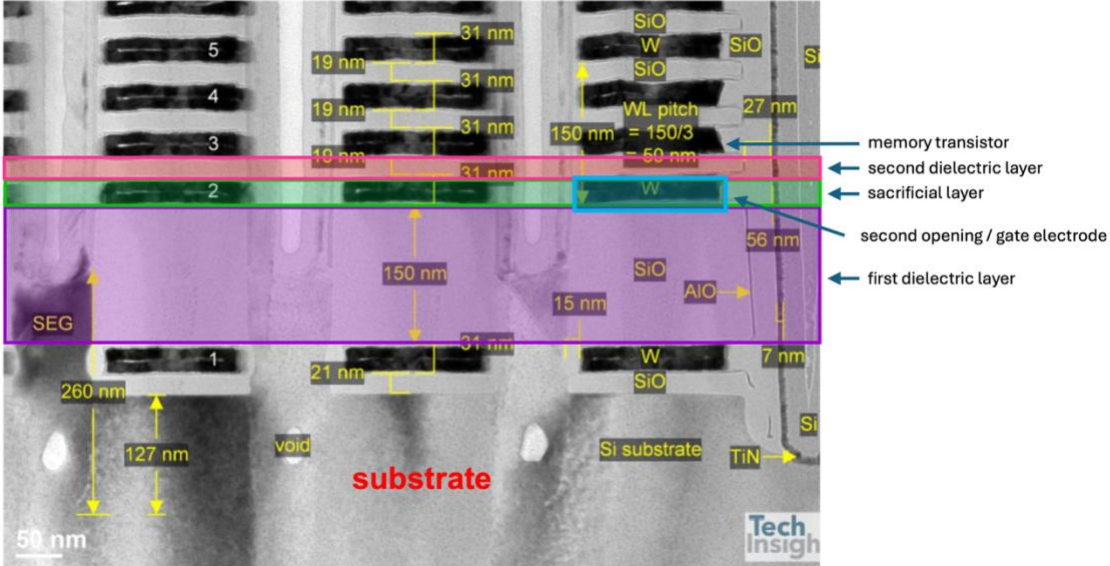
<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[26b] wherein the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer.	In the method of manufacturing the '365 Accused Instrumentalities the oxygen-rich nitride layer is formed on the inside sidewall of the oxygen-lean nitride layer. For example, the oxygen-rich nitride layer ("CT1") is formed on the inside sidewall of the oxygen-lean nitride layer ("CT2") ⁶¹ :

⁶¹ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
27. The method of claim 26, further comprising forming an anti-tunneling	The method of manufacturing the '365 Accused Instrumentalities includes a step of forming an anti-tunneling layer between the oxygen-lean nitride layer and the oxygen-rich

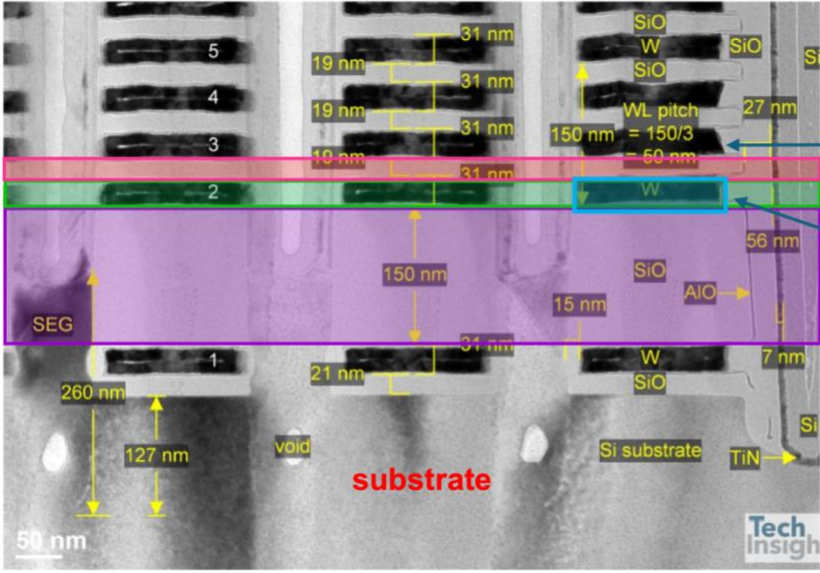
Claim Element	'365 Accused Instrumentalities
layer between the oxygen-lean nitride layer and the oxygen-rich nitride layer.	nitride layer. For example, an anti-tunneling layer (“Anti-Tunneling Layer”) is formed between the oxygen-lean nitride layer (“CT2” or “CT1”) and the oxygen-rich nitride layer (“CT1” or “CT2”) ⁶²:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

⁶² TechInsights 112L Report

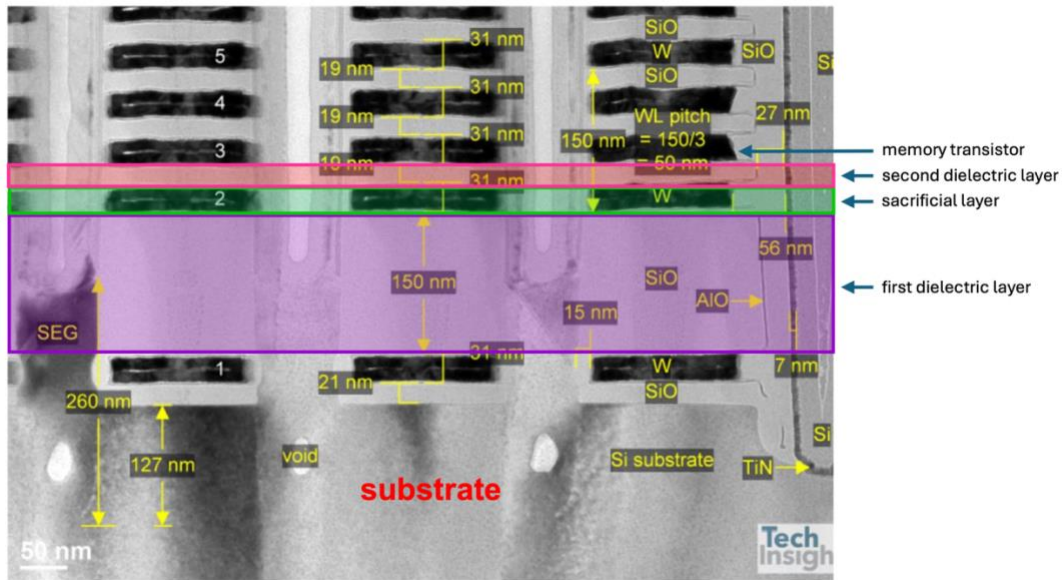
Claim Element	'365 Accused Instrumentalities
28. The method of claim 23, further comprising the step of etching the sacrificial layer to form a second opening.	The method of manufacturing the '365 Accused Instrumentalities includes a step of etching the sacrificial layer to form a second opening. For example, the sacrificial layer is etched to form a second opening where a tungsten gate will be deposited⁶³:  The diagram illustrates a cross-section of a memory transistor. Key layers and dimensions are labeled: Substrate: Si substrate at the base. First Dielectric Layer: A layer above the substrate, with a thickness of 15 nm. Second Dielectric Layer: A layer above the first dielectric, with a thickness of 56 nm. Sacrificial Layer: A layer above the second dielectric, with a thickness of 19 nm. Second Opening / Gate Electrode: An opening in the sacrificial layer, with a width of 150 nm. Memory Transistor: The main structure, with a width of 150 nm. W (Tungsten): A layer within the second opening, with a thickness of 7 nm. SiO₂: Various layers with thicknesses of 31 nm, 19 nm, and 27 nm. WL pitch: 150 nm, which is equal to 150/3 = 50 nm. SEG: A layer on the left side, with a thickness of 260 nm. Void: A void in the substrate, with a diameter of 127 nm. TiN: A layer on the right side, with a thickness of 7 nm.
29. The method of claim 28, further comprising the step of depositing a gate electrode in the second opening.	The method of manufacturing the '365 Accused Instrumentalities includes a step of depositing a gate electrode in the second opening. For example, a gate electrode (tungsten) is deposited in the second opening⁶⁴:

⁶³ TechInsights 112L Report

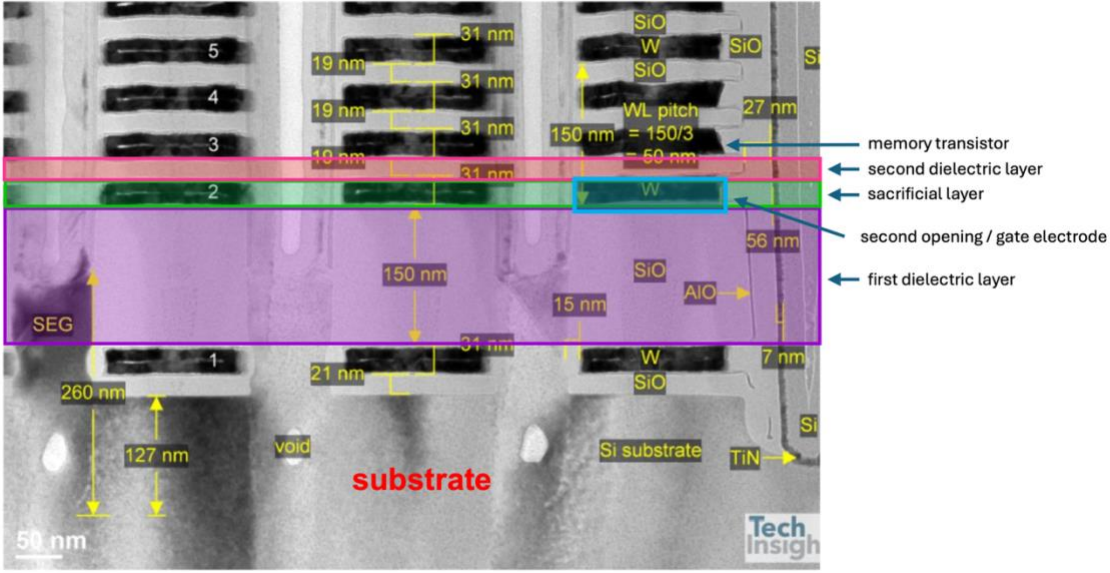
⁶⁴ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 The diagram shows a cross-section of a memory device. Key layers and dimensions include: a Si substrate at the base; a TiN layer (7 nm); a first dielectric layer (56 nm); a second opening / gate electrode (15 nm); a second dielectric layer (150 nm); a sacrificial layer (31 nm); a memory transistor (19 nm); and a WL pitch (150 nm = 150/3 = 50 nm). Other labels include SEG, void, and SiO₂. A 50 nm scale bar is present.
30. The method of claim 29, wherein the second dielectric layer separates the gate electrode from an overlying memory transistor.	In the method of manufacturing the '365 Accused Instrumentalities the second dielectric layer separates the gate electrode from an overlying memory transistor. For example, the second dielectric layer separates the gate electrode from an overlying memory transistor⁶⁵:

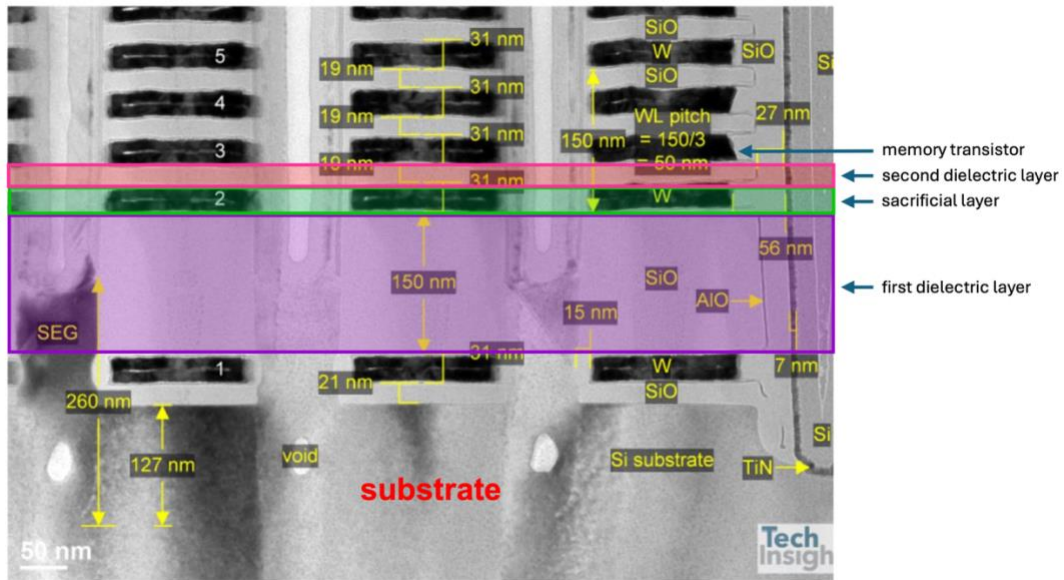
⁶⁵ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 The diagram is a cross-sectional view of a memory device. It shows a substrate at the bottom, labeled 'substrate' in red. Above the substrate is a 'SEG' (source/drain gate electrode) layer. The structure includes several layers: a 'first dielectric layer' (purple), a 'sacrificial layer' (green), a 'second dielectric layer' (pink), and a 'memory transistor' (blue). Dimensions are indicated for various layers: 260 nm, 127 nm, 21 nm, 31 nm, 19 nm, 31 nm, 150 nm, 27 nm, 56 nm, 7 nm, 15 nm, 50 nm, and 150 nm. Materials labeled include SiO, W, Si, AIO, TiN, and void. A 'WL pitch = 150/3 = 50 nm' is noted. A 50 nm scale bar is present at the bottom left. The TechInsights logo is at the bottom right.
31. The method of claim 29, wherein the deposited gate electrode is a high work function gate electrode.	In the method of manufacturing the '365 Accused Instrumentalities the deposited gate electrode is a high work function gate electrode. For example, the deposited gate electrode is tungsten, a high work function material⁶⁶:

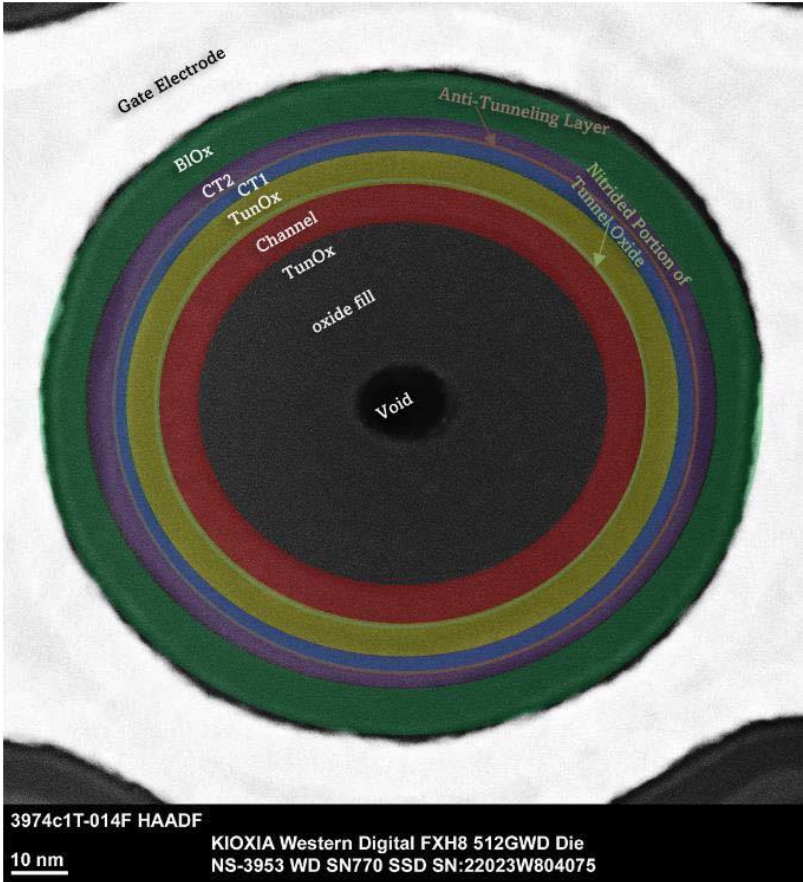
⁶⁶ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 The diagram illustrates a cross-sectional view of a memory device structure. Key components and dimensions include: Layers and Features: SiO₂, W, WL pitch, memory transistor, second dielectric layer, sacrificial layer, second opening / gate electrode, first dielectric layer, SEG, void, substrate, and TiN. Dimensions (nm): 5, 4, 3, 2, 1, 19, 31, 150, 27, 50, 56, 15, 7, 260, 127, 21, 31, 150, 50, 7, 50. Labels: SEG, void, substrate, TiN, Si substrate, SiO₂, W, WL pitch, memory transistor, second dielectric layer, sacrificial layer, second opening / gate electrode, first dielectric layer.
32. The method of claim 29, wherein the blocking dielectric layer includes a high K dielectric.	In the method of manufacturing the '365 Accused Instrumentalities the blocking dielectric layer includes a high K dielectric. For example, the blocking dielectric layer ("BIOx") comprises aluminum oxide, a high K high temperature oxide. As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
33. The method of claim 32, wherein the second dielectric layer separates the	In the method of manufacturing the '365 Accused Instrumentalities the second dielectric layer separates the gate electrode from an overlying memory transistor. For example, the second dielectric layer separates the gate electrode from an overlying memory transistor⁶⁷:

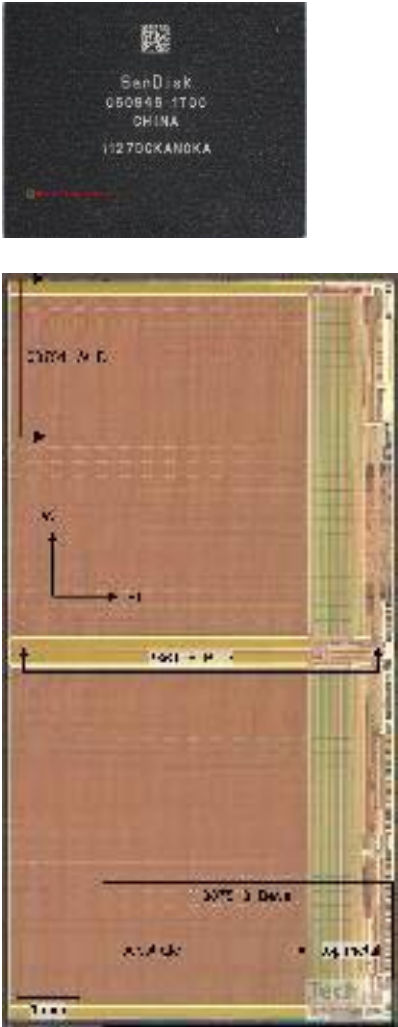
⁶⁷ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
gate electrode from an overlying memory transistor.	 The diagram is a cross-sectional view of a memory device. It shows a substrate at the bottom, labeled 'substrate' in red. Above the substrate is a 'SEG' (source/drain extension) layer. The structure includes several layers of SiO₂, W (tungsten), and Si. Dimensions are indicated in nm: 260 nm, 127 nm, 21 nm, 31 nm, 19 nm, 31 nm, 150 nm, 27 nm, 56 nm, 15 nm, 7 nm, and 50 nm. A 'void' is shown in the center. A 'Si substrate' and 'TiN' layer are also labeled. A 'memory transistor' is indicated by a blue arrow pointing to a specific layer. A 'second dielectric layer' and 'sacrificial layer' are also labeled. A 'first dielectric layer' is indicated by a blue arrow pointing to a layer. The 'WL pitch' is noted as 150/3 = 50 nm. The 'Tech Insights' logo is in the bottom right corner.
34. The method of claim 33 wherein the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer.	In the method of manufacturing the '365 Accused Instrumentalities the multi-layer charge storing region includes an oxygen-lean nitride layer and an oxygen-rich nitride layer. For example, the multi-layer charge storing region includes an oxygen-lean nitride layer ("CT2" or "CT1") and an oxygen-rich nitride layer ("CT1" or "CT2")⁶⁸:

⁶⁸ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
35. A semiconductor memory device, comprising:	To the extent the preamble is deemed limiting, the '365 Accused Instrumentalities comprise a semiconductor memory device. For example, the WDS960G2G0C SSD contains a semiconductor die containing 112-Layer 3D NAND Flash Memory⁶⁹:

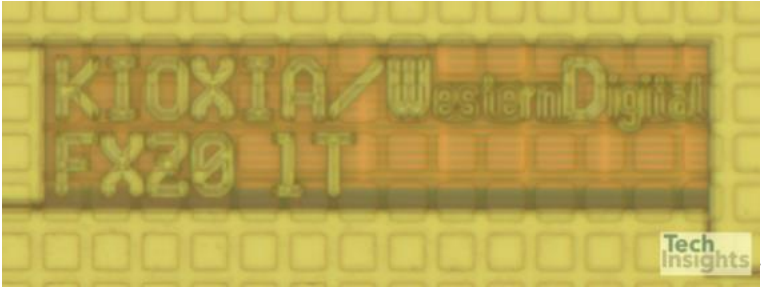
⁶⁹ TechInsights, Kioxia/Western Digital WDS960G2G0C SSD, SanDisk 060946 1T00 (FXH8 512G Die), 112-Layer 3D NAND Flash Memory, 18 nm Process Node, Advanced Memory Essentials, AME-2106-802, Published: November 19, 2021 ("TechInsights 112L Report")

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	

Claim Element	'365 Accused Instrumentalities
	Die markings on this and other '365 Accused Instrumentalities indicate that they are each made by a joint venture owned by Toshiba/Kioxia and Sandisk/Western Digital: 70 71

⁷⁰ Image of Western Digital Green SSD (P/N WDS480G2G0A) (96L)

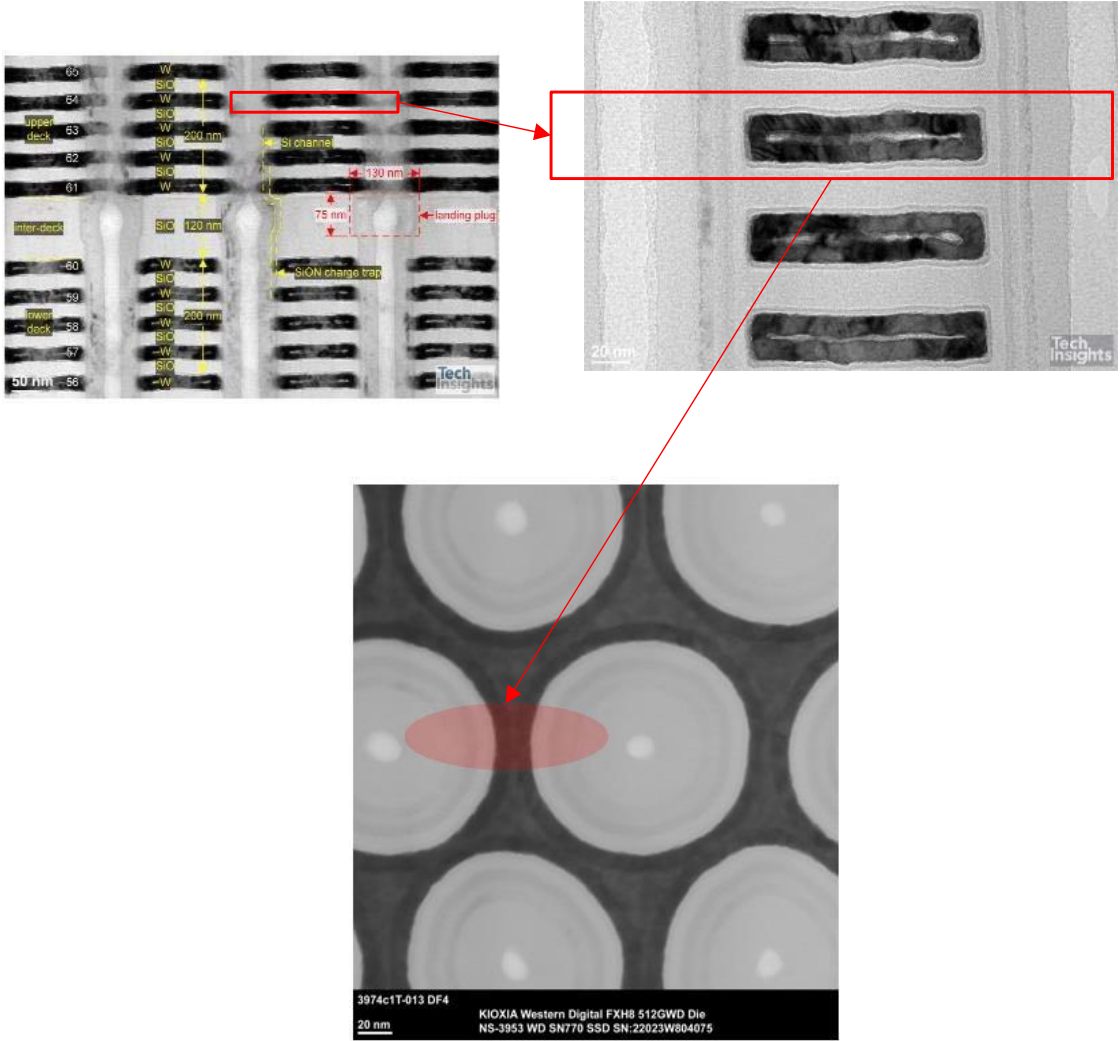
⁷¹ TechInsights 112L Report

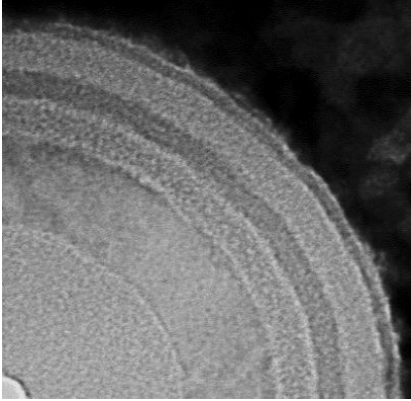
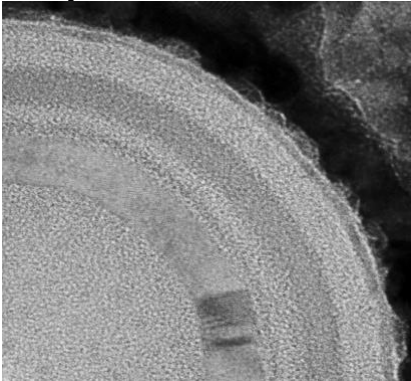
Claim Element	'365 Accused Instrumentalities
	 72  73 The following images each show multiple memory transistors, in different cross sections of a 112L accused product⁷⁴:

⁷² TechInsights, Toshiba TH58LKT3B46BA8S (KIOXIA/Western Digital Corp. FXZ0_1T die), 162-Layer 3D NAND Flash Memory, Advanced Memory Essentials, AME-2310-803, Published: February 29, 2024 (“TechInsights 162L Report”)

⁷³ TechInsights, KIOXIA/WDC FYU6_1T 218L (BiCS8), Triple-Level Cell (TLC) 1 Tb 3D NAND Flash, Advanced Memory Essentials, AME-2407-801, Published: November 29, 2024 (“TechInsights 218L Report”)

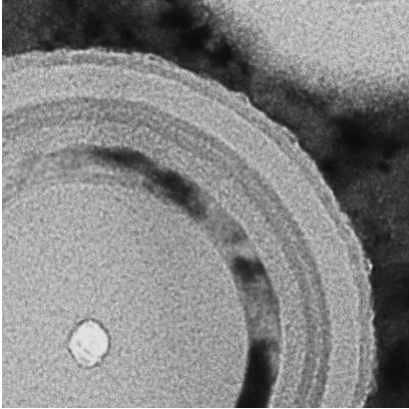
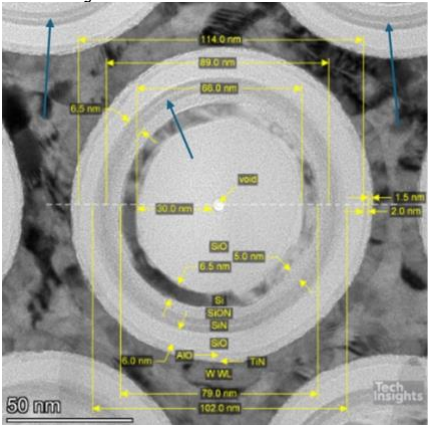
⁷⁴ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 3974c1T-013 DF4 20 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	Similar memory transistor structures are present in each of the '365 Accused Instrumentalities, as shown in the following cross section images. 64-layer⁷⁵:  96-layer⁷⁶: 

⁷⁵ TechInsights, Memory DRAM & NAND Tri-Annual Briefing #1, 2022, Report ID: BRF-2112-810, May 2022, p. 47,

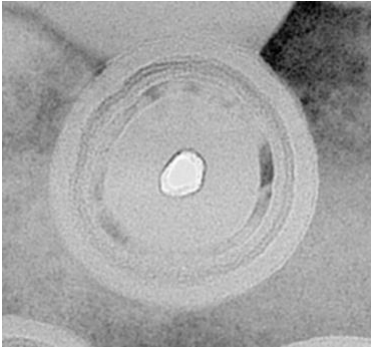
⁷⁶ *Id.*

Claim Element	'365 Accused Instrumentalities
	112-layer⁷⁷:  162-layer⁷⁸:  218-layer⁷⁹:

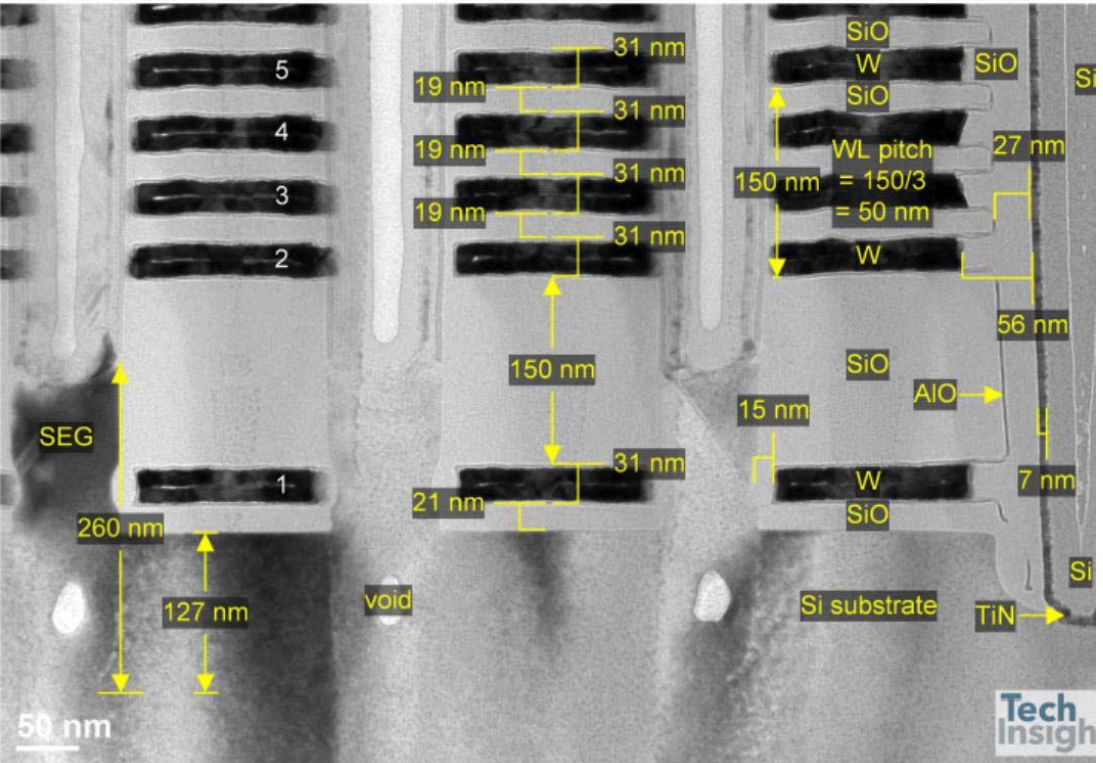
⁷⁷ *Id.*

⁷⁸ TechInsights 162L Report

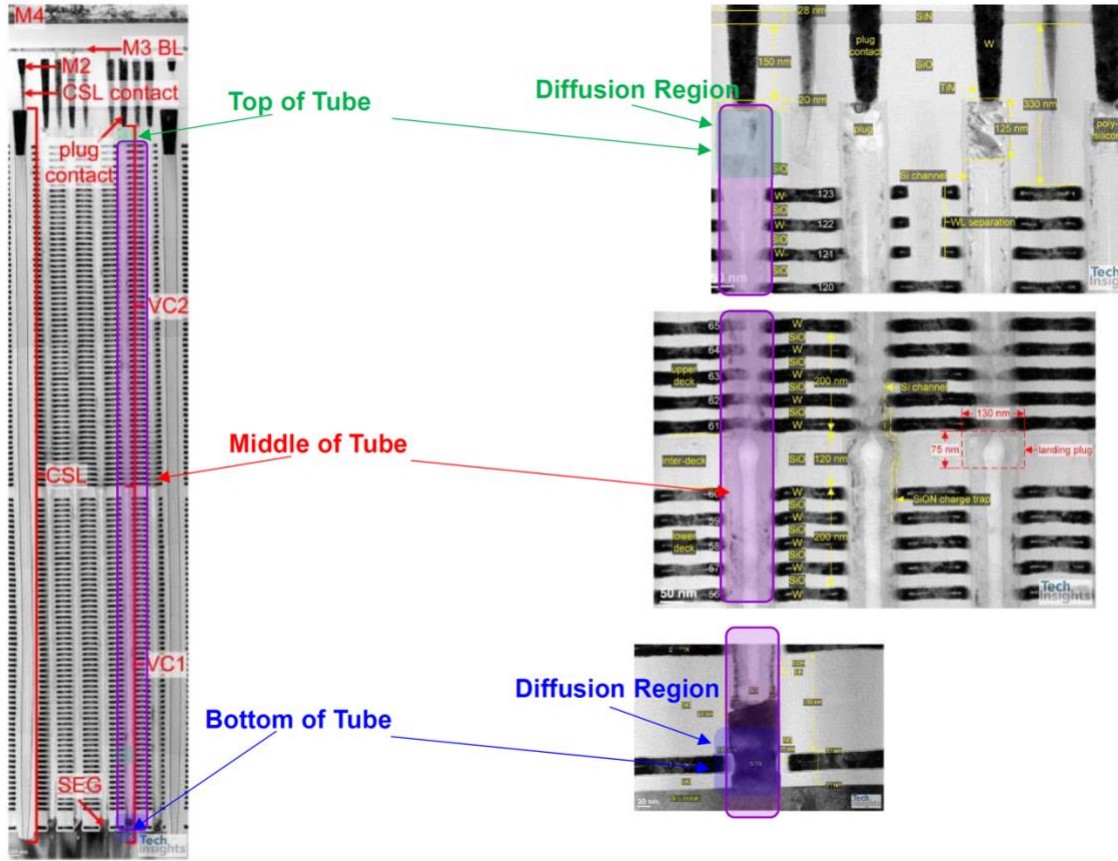
⁷⁹ TechInsights 218L Report

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	
[35a] a semiconductor substrate,	The '365 Accused Instrumentalities comprise a semiconductor substrate. For example, these products include a silicon substrate ⁸⁰ :

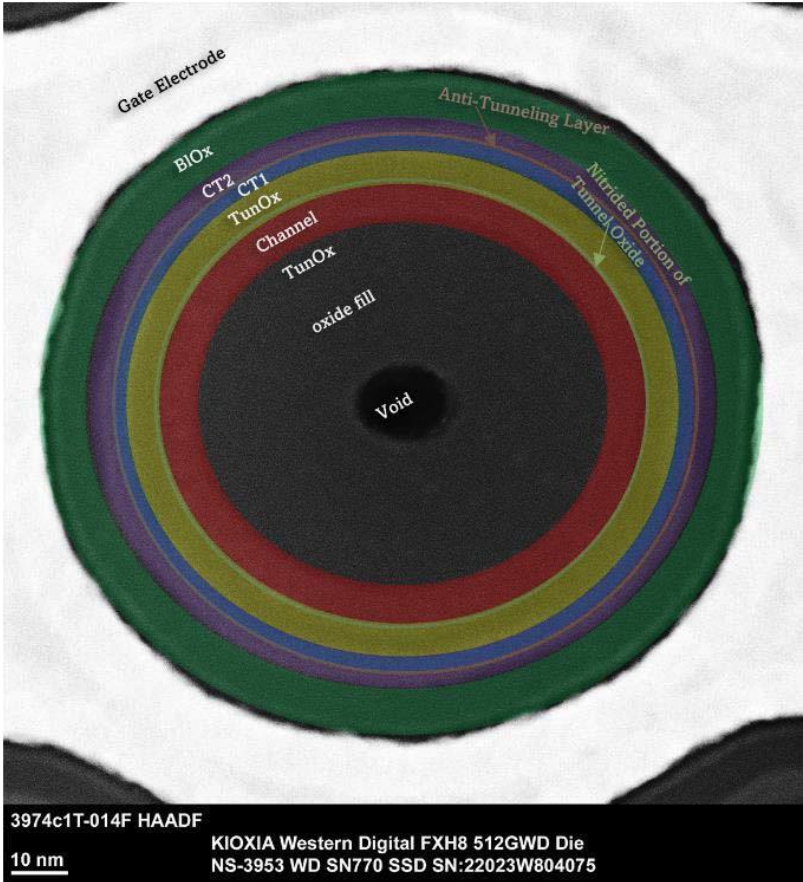
⁸⁰ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
	 The image is a cross-sectional scanning electron micrograph (SEM) of a semiconductor device. It shows several layers and structures with various dimensions labeled in nanometers (nm). On the left, a series of horizontal bars are numbered 1 through 5. Bar 1 is 260 nm wide and 127 nm high. A label 'SEG' points to a region. In the center, a 'void' is indicated. To the right, a stack of layers is shown with dimensions: 19 nm, 31 nm, 31 nm, 31 nm, 31 nm, 150 nm, 31 nm, 21 nm. Further right, another stack of layers is shown with dimensions: 150 nm, 27 nm, 56 nm, 15 nm, 7 nm. Labels include 'SiO', 'W', 'WL pitch = 150/3 = 50 nm', 'SiO', 'AIO', 'W', 'SiO', 'Si substrate', and 'TiN'. A scale bar at the bottom left indicates 50 nm. The 'Tech Insignia' logo is in the bottom right corner.
[35b] a channel region oriented substantially perpendicular to the semiconductor substrate, the channel region formed in a substantially annular shape,	The '365 Accused Instrumentalities comprise a channel region oriented substantially perpendicular to the semiconductor substrate, the channel region formed in a substantially annular shape. For example, the '2365 Accused Instrumentalities contain vertical tube structures⁸¹:

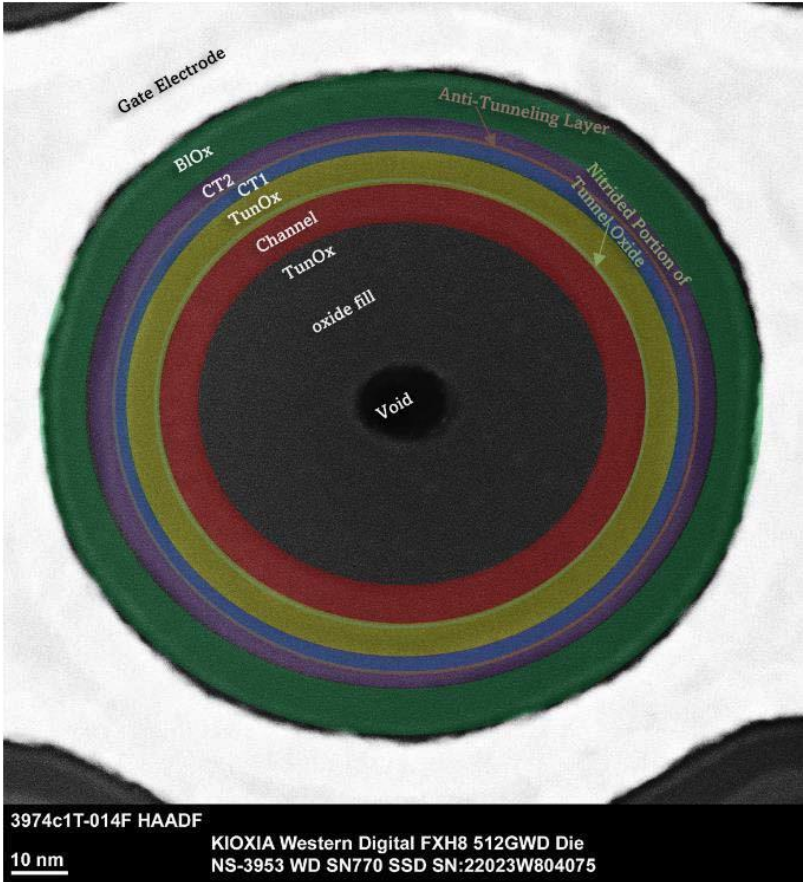
⁸¹ TechInsights 112L Report

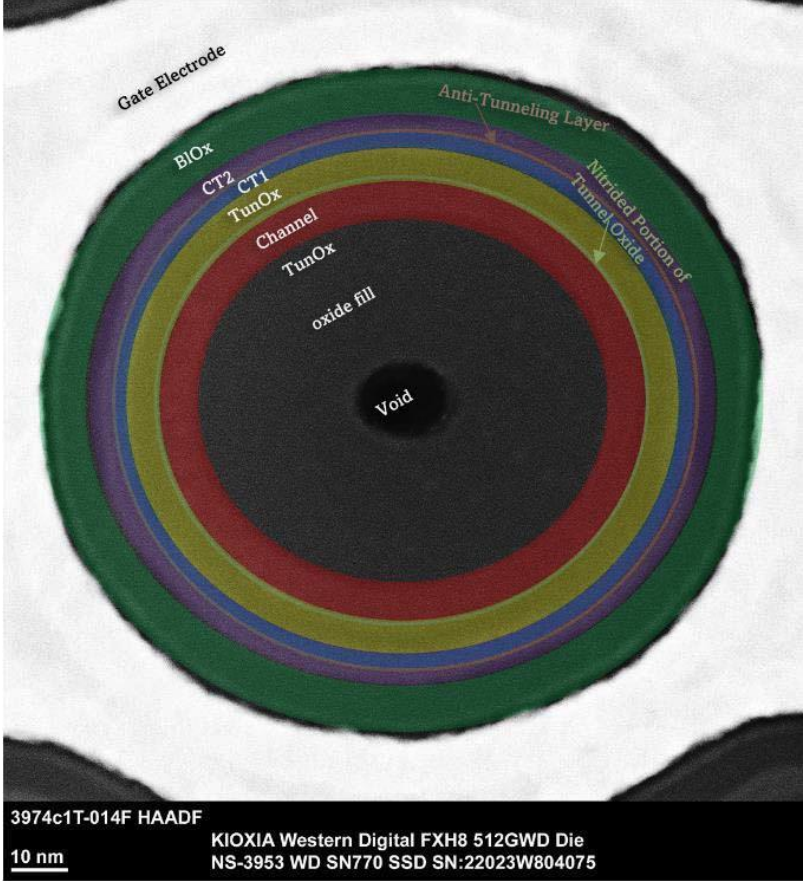
Claim Element	'365 Accused Instrumentalities
	 The vertical tubes contain a silicon channel (“Channel”) which is substantially annular in shape⁸²:

⁸² TechInsights 112L Report

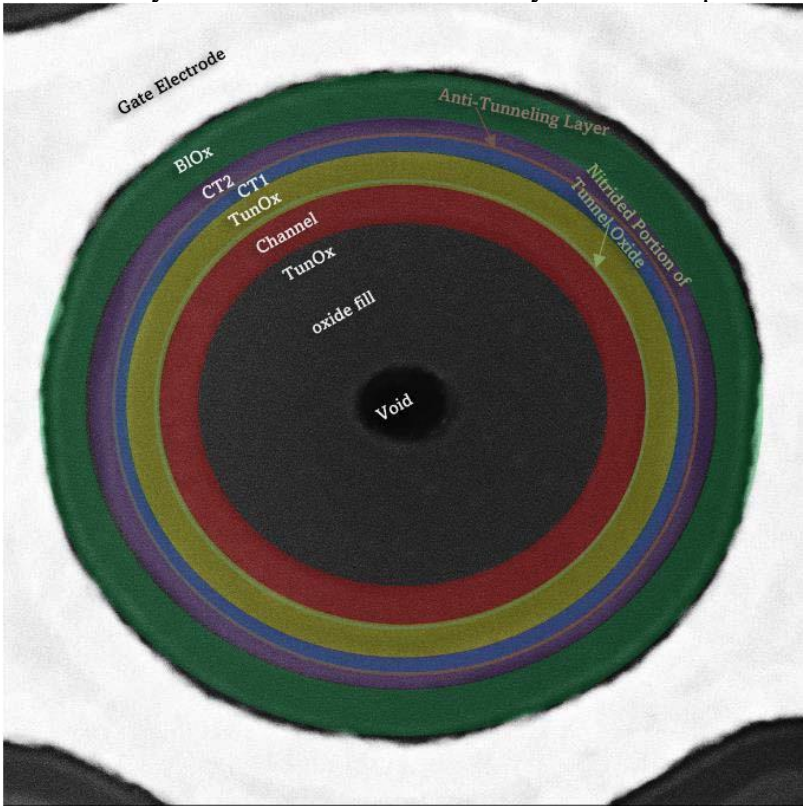
Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
[35c] a tunnel dielectric layer surrounding the channel region, the tunnel dielectric layer formed in a substantially annular shape,	The '365 Accused Instrumentalities comprise a tunnel dielectric layer surrounding the channel region, the tunnel dielectric layer formed in a substantially annular shape. For example, the tunnel dielectric layer ("TunOx") surrounds the channel region ("Channel"), and the tunnel dielectric layer is formed in a substantially annular shape⁸³:

⁸³ TechInsights 112L Report

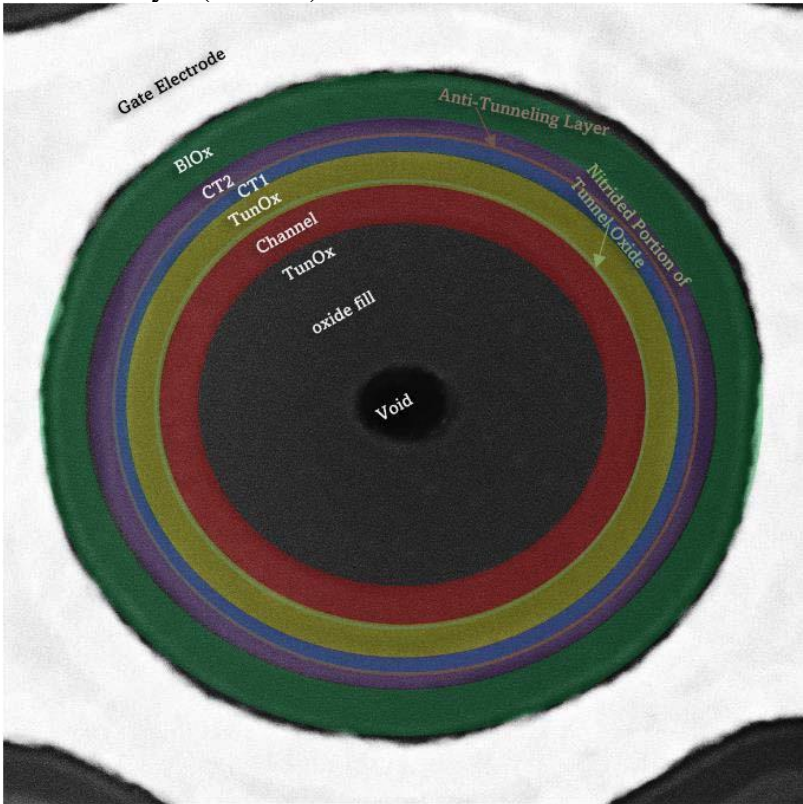
Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
[35d] a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape,	The '365 Accused Instrumentalities comprise a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape. For example, multi-layer charge storing region ("CT1," "Anti-

Claim Element	'365 Accused Instrumentalities
	Tunnelling Layer,” “CT2”) surrounds the tunnel dielectric layer (“TunOx”), and the multi-layer charge storing region is formed in a substantially annular shape ⁸⁴:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
[35e] a blocking dielectric layer surrounding the multi-layer charge	The '365 Accused Instrumentalities comprise a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially

⁸⁴ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
storing region, the blocking dielectric layer formed in a substantially annular shape, and	annular shape. For example, a blocking dielectric layer (“BIOx”) surrounds the multi-layer charge storing region (“CT1,” “Anti-Tunnelling Layer,” “CT2”), and the blocking dielectric layer is formed in a substantially annular shape ⁸⁵:  The diagram illustrates a cross-section of a memory cell with concentric layers. From the center outwards, the layers are: a central 'Void', followed by 'oxide fill', 'TunOx', 'Channel', 'TunOx', 'CT1', 'CT2', 'BIOx', 'Anti-Tunneling Layer', 'Nitrided Portion of Tunnel Oxide', and an outer 'Gate Electrode'. The layers are color-coded: Void (black), oxide fill (dark grey), TunOx (light grey), Channel (red), TunOx (yellow), CT1 (green), CT2 (blue), BIOx (purple), Anti-Tunneling Layer (orange), Nitrided Portion of Tunnel Oxide (light blue), and Gate Electrode (dark blue). 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

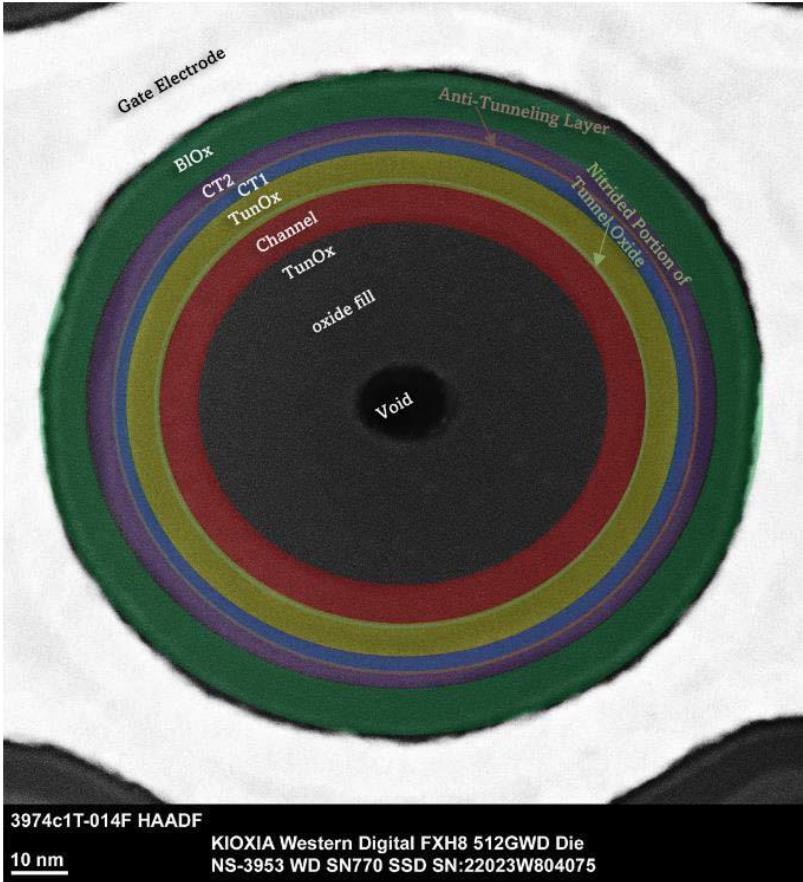
⁸⁵ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
[35f] a gate electrode surrounding the blocking dielectric layer.	The '365 Accused Instrumentalities comprise a gate electrode surrounding the blocking dielectric layer. For example, the gate electrode ("Gate Electrode") surrounds the blocking dielectric layer ("BIOx")⁸⁶:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

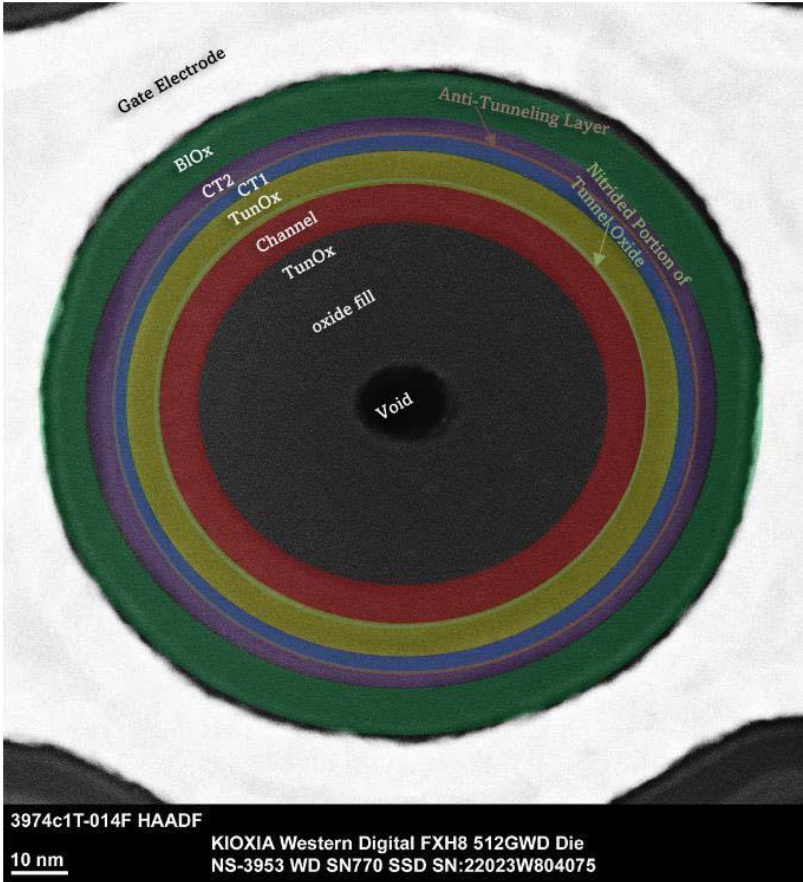
⁸⁶ TechInsights 112L Report

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
36. The semiconductor memory device of claim 35, wherein the blocking dielectric layer includes a high K dielectric.	In the '365 Accused Instrumentalities the blocking dielectric layer includes a high K dielectric. For example, the blocking dielectric layer (“BIOx”) comprises aluminum oxide, a high K high temperature oxide. As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
37. The semiconductor memory device of claim 35, wherein the gate electrode is a high work function gate electrode.	In the '365 Accused Instrumentalities the gate electrode is a high work function gate electrode. For example, the gate electrode (“Gate Electrode”) is formed from tungsten, a high work function material ⁸⁷ :

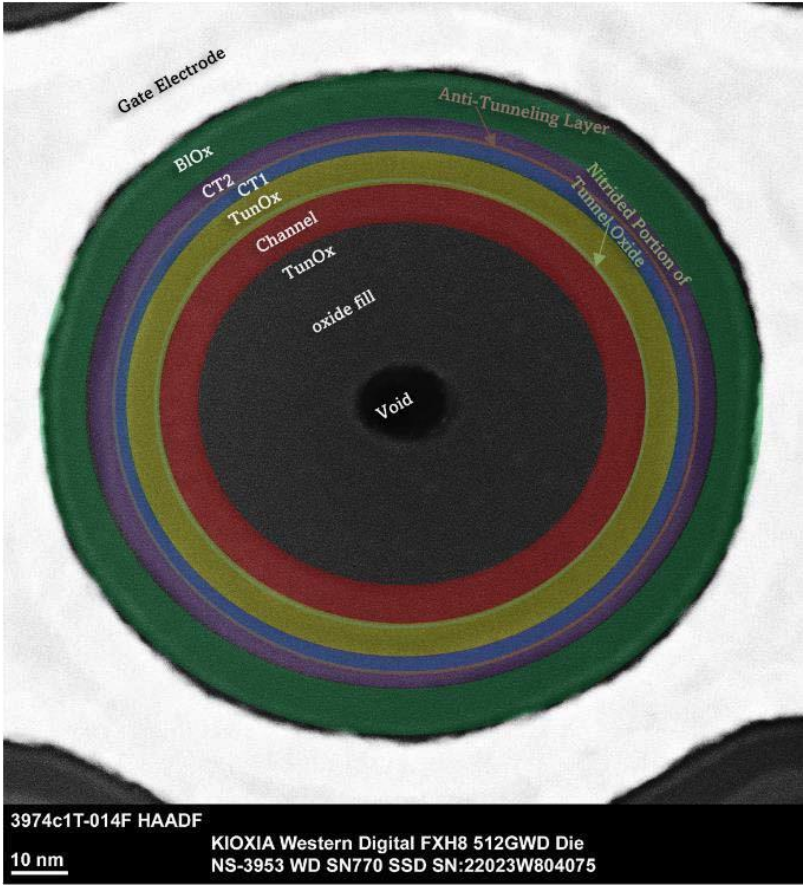
⁸⁷ TechInsights 112L Report

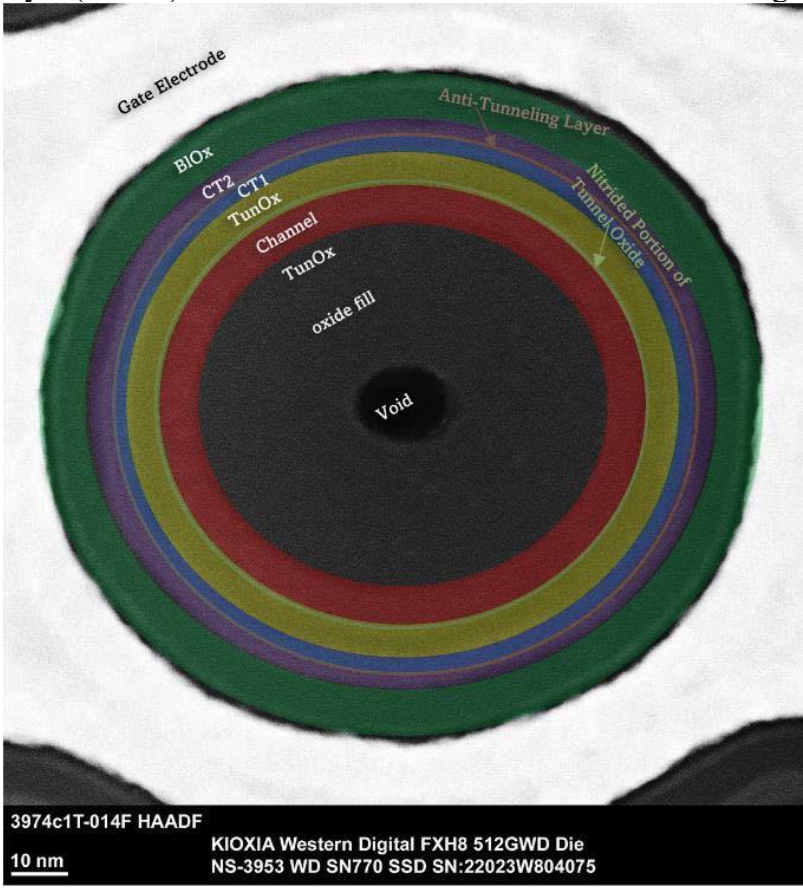
Claim Element	'365 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
38. The semiconductor memory device of claim 35, wherein the multi-layer charge storing region includes a first	In the '365 Accused Instrumentalities the multi-layer charge storing region includes a first oxygen-lean nitride layer and a second oxygen-rich nitride layer. For example, the multi-layer charge storing region includes an oxygen-lean nitride layer ("CT2") and an oxygen-rich nitride layer ("CT1")⁸⁸:

⁸⁸ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
oxygen-lean nitride layer and a second oxygen-rich nitride layer.	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
39. The semiconductor memory device of claim 38, wherein the first oxygen-lean nitride layer and the second oxygen-rich nitride layer both include silicon, nitrogen and oxygen components.	In the '365 Accused Instrumentalities the first oxygen-lean nitride layer and the second oxygen-rich nitride layer both include silicon, nitrogen and oxygen components. For example, the first oxygen-lean nitride layer ("CT2" or "CT1") and the second oxygen-rich nitride layer ("CT1" or "CT2") both include silicon, nitrogen and oxygen components ⁸⁹ :

⁸⁹ TechInsights 112L Report

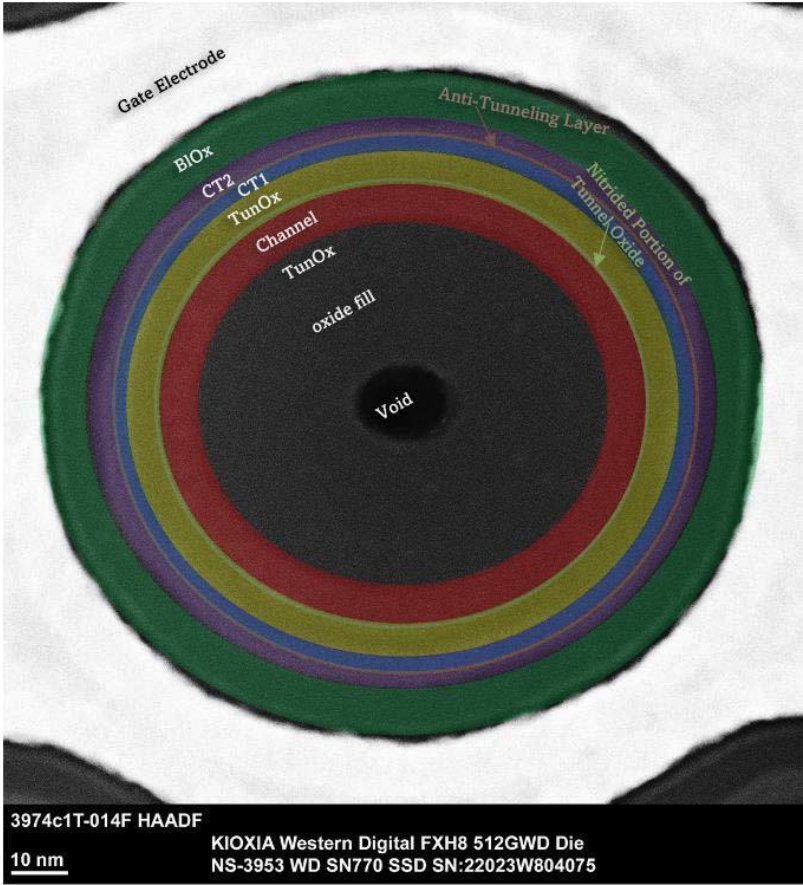
Claim Element	'365 Accused Instrumentalities
silicon, nitrogen and oxygen components.	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
40. The semiconductor memory device of claim 39,	

Claim Element	'365 Accused Instrumentalities
[40a] wherein the first oxygen-lean nitride layer is formed on an inside sidewall of the blocking dielectric layer and	In the '365 Accused Instrumentalities the first oxygen-lean nitride layer is formed on an inside sidewall of the blocking dielectric layer. For example, the first oxygen-lean nitride layer ("CT2") is formed on an inside sidewall of the blocking dielectric layer ("BIOx")⁹⁰:  The diagram is a cross-sectional view of a memory cell, likely a NAND flash, showing concentric layers. From the outside in, the layers are: Gate Electrode (dark green), BIOx (light green), CT2 (purple), CT1 (blue), TunOx (yellow), Channel (red), TunOx (orange), oxide fill (dark grey), and a central Void (black). A Nitrided Portion of Tunnel Oxide is indicated on the right side. The diagram is labeled with '3974c1T-014F HAADF' and '10 nm' scale bar. Below the diagram, it says 'KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075'.

⁹⁰ TechInsights 112L Report

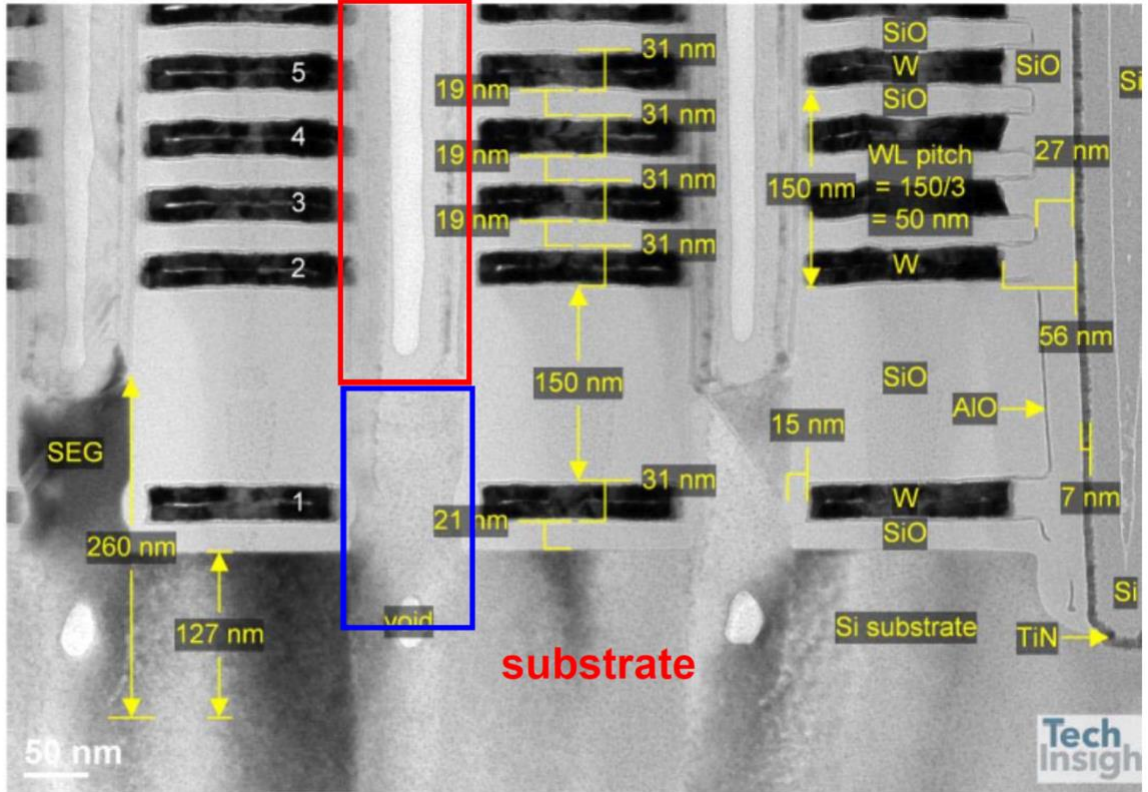
<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[40b] wherein the second oxygen-rich nitride layer is formed on the inside sidewall of the first oxygen-lean nitride layer.	In the '365 Accused Instrumentalities the second oxygen-rich nitride layer is formed on the inside sidewall of the first oxygen-lean nitride layer. For example, the second oxygen-rich nitride layer ("CT1") is formed on the inside sidewall of the first oxygen-lean nitride layer ("CT2") ⁹¹ :

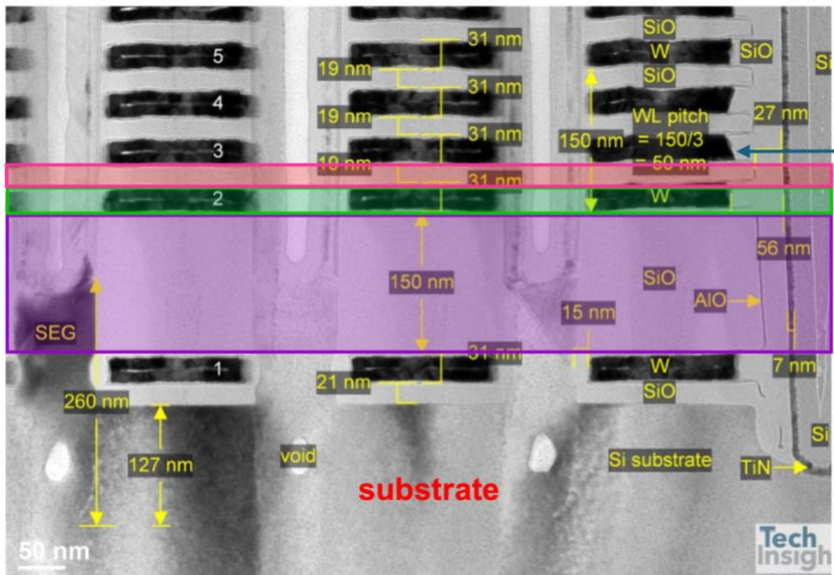
⁹¹ TechInsights 112L Report

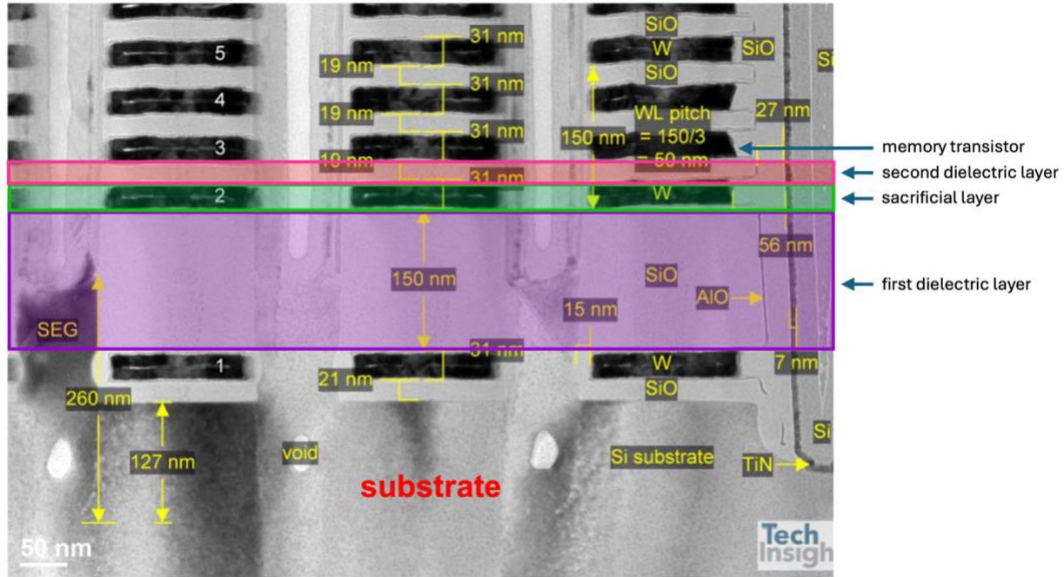
Claim Element	'365 Accused Instrumentalities
	 The diagram shows a cross-section of a memory cell. At the center is a dark circular region labeled 'Void'. Surrounding this is a thick grey ring labeled 'oxide fill'. The next layer is a red ring labeled 'TunOx'. Above this is a thin yellow ring labeled 'Channel'. This is followed by a blue ring labeled 'TunOx', then a green ring labeled 'CT1', and finally a dark green outer ring labeled 'CT2'. The topmost layer is a thin black line labeled 'Gate Electrode'. On the right side, there is a label 'Anti-Tunneling Layer' pointing to a thin blue layer, and 'Nitrided Portion of Tunnel Oxide' pointing to a thin yellow layer within the blue layer. At the bottom left of the diagram, there is a scale bar labeled '10 nm' and text identifying the sample as '3974c1T-014F HAADF' and 'KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075'. As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.

<i>Claim Element</i>	<i>'365 Accused Instrumentalities</i>
41. The semiconductor memory device of claim 40, wherein the blocking dielectric layer includes a high K dielectric.	In the '365 Accused Instrumentalities the blocking dielectric layer includes a high K dielectric. For example, the blocking dielectric layer (“BIOx”) comprises aluminum oxide, a high K high temperature oxide. As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
42. The semiconductor memory device of claim 35, including a stack of layers formed over the substrate.	The '365 Accused Instrumentalities include a stack of layers formed over the substrate. For example, the devices include a stack of layers formed over the silicon substrate ⁹²:

⁹² TechInsights 112L Report

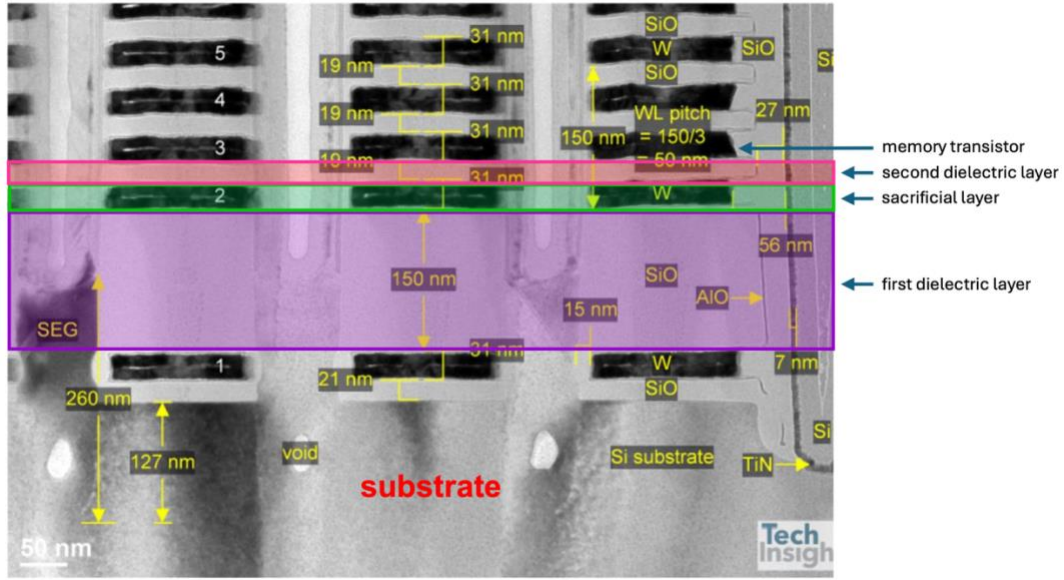
Claim Element	'365 Accused Instrumentalities
	
43. The semiconductor memory device of claim 42,	
[43a] wherein the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer,	In the '365 Accused Instrumentalities the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer. For example, the stack of layers includes a first dielectric layer, a gate layer and a second dielectric layer as annotated below:

Claim Element	'365 Accused Instrumentalities
	 The image is a cross-sectional scanning electron micrograph (SEM) of a memory transistor structure. It shows multiple layers and dimensions. Key features include: Substrate: Labeled in red at the bottom. SEG (Source/Drain Extension Gate): A layer on the left side. Gate Stack: Consists of a first dielectric layer (purple), a sacrificial layer (green), and a second dielectric layer (pink). Memory Transistor: Indicated by a blue arrow pointing to the gate stack. Dimensions: Various thicknesses and widths are labeled in nanometers (nm), such as 260 nm, 127 nm, 150 nm, 31 nm, 19 nm, 10 nm, 27 nm, 56 nm, 15 nm, 7 nm, 21 nm, and 34 nm. Materials: Labels include SiO₂, W (tungsten), Si, AIO, TiN, and voids. Scale Bar: 50 nm is shown at the bottom left. Logo: Tech Insign is visible at the bottom right.
[43b] wherein the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer.	In the '365 Accused Instrumentalities the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer. For example, the gate layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by a sacrificial layer:

Claim Element	'365 Accused Instrumentalities
	
44. The semiconductor memory device of claim 43, wherein the channel region is formed in an opening extending through the stack of layers.	In the '365 Accused Instrumentalities the channel region is formed in an opening extending through the stack of layers. For example, the channel region is formed in an opening (purple rectangle) extending through the stack of layers ⁹³:

⁹³ TechInsights 112L Report

Claim Element	'365 Accused Instrumentalities
45. The semiconductor memory device of claim 43, wherein the second dielectric layer separates the gate layer from an overlying memory transistor.	In the '365 Accused Instrumentalities the second dielectric layer separates the gate layer from an overlying memory transistor. For example, the second dielectric layer separates the gate layer from an overlying memory transistor:

Claim Element	'365 Accused Instrumentalities
	 The diagram shows a cross-sectional view of a memory device structure. Key layers and dimensions are labeled: Substrate: Si substrate (bottom layer). SEG (Source Electrode Gate): A layer on the left side. First dielectric layer: A thick layer (56 nm) above the substrate. Sacrificial layer: A thin layer (15 nm) above the first dielectric layer. Second dielectric layer: A thin layer (150 nm) above the sacrificial layer. Memory transistor: A structure (150 nm) above the second dielectric layer. Other layers: SiO, W, SiO, WL pitch, 27 nm, 31 nm, 19 nm, 10 nm, 21 nm, 7 nm, TiN, void, 260 nm, 127 nm, 50 nm. The diagram includes a 50 nm scale bar and a Tech Insign logo.