

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC.,
Petitioner,

v.

LONGITUDE FLASH MEMORY SOLUTIONS LTD.,
Patent Owner.

Case IPR2025-01281
U.S. Patent No. 11,456,365

PATENT OWNER'S PRELIMINARY RESPONSE

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TABLE OF AUTHORITIES

Cases

<i>In re Oetiker</i> , 977 F.2d 1443 (Fed. Cir. 1992)	13
<i>KSR In'l Co. v. Teleflex Inv.</i> , 550 U.S. at 398 (2007).....	13

PATENT OWNER'S EXHIBIT LIST

<i>Exhibit</i>	<i>Description</i>
2001	<i>Complaint, Sandisk Corp. v. IPValue Management, Inc., et al., 5:25-cv-02389 (N.D. Cal.), March 7, 2025.</i>
2002	<i>Case Management Order, Sandisk Corp. v. IPValue Management, Inc., et al., 5:25-cv-02389 (N.D. Cal.), Sept. 2, 2025.</i>
2003	<i>Invalidity Contentions, Sandisk Corp. v. IPValue Management, Inc., et al., 5:25-cv-02389 (N.D. Cal.), Nov. 14, 2025.</i>
2004	<i>Order on Discovery Dispute, Sandisk Corp. v. IPValue Management, Inc., et al., 5:25-cv-02389 (N.D. Cal.), Sept. 29, 2025.</i>
2005	<i>Order Denying Motion to Dismiss, Sandisk Corp. v. IPValue Management, Inc., et al., 5:25-cv-02389 (N.D. Cal.), Oct. 7, 2025.</i>
2006	<i>Order, Sandisk Corp. v. IPValue Management, Inc., et al., 5:25-cv-02389 (N.D. Cal.), Oct. 20, 2025.</i>

I. Introduction

The Petition does not demonstrate a reasonable likelihood of prevailing because it fails to show that at least one limitation of each of the independent claims would have been obvious to a person of skill in the art.

Only the Petition's first ground challenges the independent claims of the '365 Patent. It relies primarily on Lee '255 as rendering the claims obviousness. The Petition admits, as it must, that Lee '255 was cited in an IDS filed during the prosecution of the '365 patent. Moreover, the Petition does not allege any error by the examiner during prosecution. Instead, the Petition alleges that this reference in combination with the Lee '961 reference that was not before the examiner renders the claims obvious.

As explained below the Petition fails to show that Lee '255 discloses or renders obvious at least the "annular shaped" limitation of claim [35d], the "formed on" limitations of claim [1b], [1c], and [1d], and the similar limitations of claim 23. Moreover, the Petition does not assert that Lee '961 discloses these limitations, even assuming that a POSITA would be motivated to combine their teaching. Accordingly, as to the limitations of the independent claims, the Petition presents no reason to deviate from the examiner's decision that the claims are patentable.

As the Petition fails to show that the independent claims of the '365 Patent are obvious, the Petition's Ground 1 fails. Moreover, as Ground 2 challenges only

claims that depend on claims 1, 23, and 35—and because it relies upon the added Fujiwara reference solely to address limitations of additional dependent claims—Ground 2 necessarily fails as well. While Patent Owner only addresses certain claim limitations in this preliminary response, it reserves the right to address additional issues in a Patent Owner Response should a proceeding be instituted on the Petition.

Petitioner’s request for institution should be denied.

II. Background

A. Sandisk’s Petition

Petitioner Sandisk Technologies, Inc. (“Petitioner” or “Sandisk”) challenges claims 1-3, 5-12, 14-23, and 25-45 of the ’365 Patent. The Petition’s two asserted grounds for unpatentability are structured as follows:

- Ground 1: Obviousness of claims 1-3 5, 9-12, 14-23, 28-33, 35-37, and 42-45 over Lee ’255 and Lee ’961; and
- Ground 2: Obviousness of claims 6-8, 25-27, 34, and 38-41 over Lee ’255, Lee ’961, and Fujiwara.

All challenged dependent claims depend from claims 1, 23, and 35. These independent claims are challenged only in the Petition’s Ground 1, and the Fujiwara reference added in Ground 2 is relied upon solely to address added limitations of the dependent claims. Accordingly, this Preliminary Response need only address the Petition’s arguments in Ground 1 as it relates to claims 1, 23, and 35. Institution

must be denied unless the Petition establishes a reasonable likelihood of prevailing with respect to those independent claims as set forth in Ground 1.

As the Petition points out, both Lee '255 and Fujiwara were included among the references in an IDS filed during the prosecution of the '365 patent. Petition at 29, 34. But the Petition does not attempt to show that Lee '255 or Fujiwara, or any combination of those references with any of the other references of record in prosecution should have led to the rejection of any of the challenged claims. Rather, the Petition relies on a different reference—Lee '961—that was not before the examiner. Petition at 31. The Petition expressly argues that its obviousness grounds are based upon art that is different from that before the examiner and thus does not seek to show that the examiner overlooked teachings of the art before him or made errors in analyzing that art. Petition at 38 (“The combination of Lee '255 and Lee '961 differs from prior art considered during prosecution. . . . Lee '961 was not of record.”), 92 (“This combination of Lee '255, Lee '961, and Fujiwara differs from the prior art the Examiner considered during prosecution because the combination teaches the limitations the Examiner found missing from the prior art.”). However, as shown below, the Petition fails to establish anything in Lee '961 that would lead to a different result.

B. Overview of the '365 Patent

The '365 patent was filed on January 25, 2021, and issued on September 27, 2022. It is one of a series of continuations and continuations-in-part of U.S. Patent No. 8,063,434, filed on May 13, 2008, which in turn claimed priority to provisional application 60/940,160, filed on May 25, 2007. Ex. 1001 at 2.

The patent is directed to NAND flash non-volatile memory transistors whose gate stacks include multiple charge-storing layers, and their manufacture. Such transistors are at the heart of flash memories used in solid state drives, hard drives, USB flash drives, and other non-volatile memory-based storage. In the embodiments described, a tunnel dielectric overlies a semiconductor channel, a blocking dielectric lies beneath the gate, and between them is a multi-layer charge-trapping region that includes nitride layers of different oxygen content separated by an oxide anti-tunneling layer, all disposed under a gate electrode. Ex. 1001 at 2:41–57, 3:43–52, 4:37–49, 10:4–15, 12:25–46.

The specification explains that conventional charge-trap flash memories with Si-rich trapping layers provide a large initial program/erase window but experience rapid window collapse and limited data retention, while “high-quality” nitride layers offer only moderate improvement in retention and start from a smaller initial window, and that existing memory processes can be incompatible with CMOS logic processes used in embedded and system-on-chip designs. Ex. 1001 at 1:63–2:37. As

described in the Background and Summary, the disclosed multi-layer charge-trapping architecture, combined with the high work-function gate, is presented as a solution intended to improve data retention and transistor lifetime while remaining compatible with standard logic process flows, thereby providing the advance over prior structures identified in the patent itself. *Id.*

The '365 Patent contains 3 independent claims: claim 35, a system claim and claims 1 and 23, which are method claims. Claim 35 recites:

35. A semiconductor memory device, comprising:

a semiconductor substrate,

a channel region oriented substantially perpendicular to the semiconductor substrate, the channel region formed in a substantially annular shape,

a tunnel dielectric layer surrounding the channel region, the tunnel dielectric layer formed in a substantially annular shape,

a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a substantially annular shape,

a blocking dielectric layer surrounding the multi-layer charge storing region, the blocking dielectric layer formed in a substantially annular shape, and a gate electrode surrounding the blocking dielectric layer.

Ex. 1001 at 22:22-38. Claim 1 recites:

1. A method comprising:

forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;

forming an opening extending through the stack of layers to a first doped diffusion region formed on the substrate;

forming on sidewalls of the opening a blocking dielectric layer;

forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region;

forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and

forming on an inside sidewall of the tunnel dielectric layer a vertical channel having a semiconductor material extending from the first doped diffusion region through the opening to a top of the stack of layers.

Ex. 1001 at 20:26-45. Claim 23 recites:

23. A method comprising:

forming over a substrate a stack of layers including at least a first dielectric layer, a sacrificial layer and a second dielectric layer, wherein the sacrificial layer is separated from the substrate by the first dielectric layer and the second dielectric layer is separated from the first dielectric layer by the sacrificial layer;

forming an opening extending through the stack of layers towards the substrate;

forming on sidewalls of the opening an annular shaped blocking dielectric layer;

forming on an inside sidewall of the blocking dielectric layer an annular shaped multi-layer charge storing region;

forming on an inside sidewall of the multi-layer charge storing region an annular shaped tunnel dielectric layer; and

forming on an inside sidewall of the tunnel dielectric layer an annular shaped vertical channel having a semiconductor material extending from the substrate through the opening towards a top of the stack of layers.

Ex. 1001 at 21:36-57.

III. Level of Ordinary Skill in the Art

The Petition proposes that a person of ordinary skill in the art in the field of the '365 Patent “would have had at least (1) a master’s degree in electrical engineering, materials science, physics, or a related degree, and at least 3-5 years of experience in semiconductor devices and fabrication technologies; or (2) a bachelor’s degree in electrical engineering, materials science, physics, or a related degree, and at least 5-6 years of experience in semiconductor devices and fabrication technologies.” Pet. at 23. For purposes of this Preliminary Response only, Patent Owner does not challenge that definition.

IV. Claim Construction

The Petition proposes claim constructions for terms found only in certain of the dependent claims. Pet. at 24-27. Petitioner does not propose constructions for any terms found solely in independent claims 1, 23, and 35. As this Preliminary

Response only address the challenges to the independent claims set forth in Ground 1, Patent Owner does not address the Petition's proposed claim constructions at this time. Patent Owner reserves the right to challenge these claim constructions, and propose additional constructions, in any later proceedings.

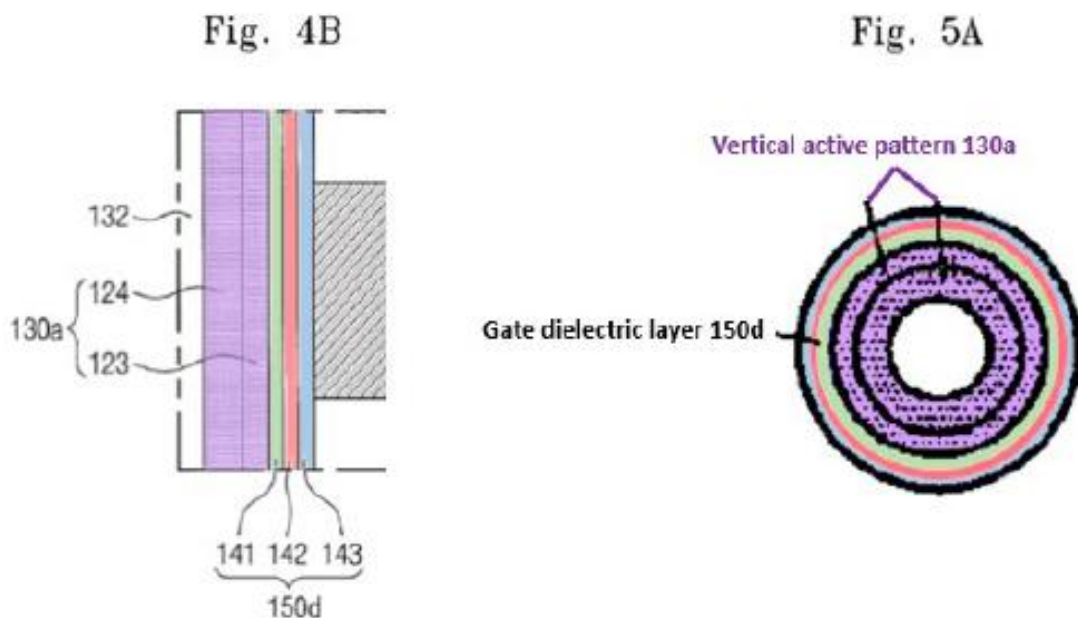
V. The Petition's Ground 1 Challenges Fail.

A. Lee '255 and Lee '961 do not disclose the claimed annular shaped multi-layer charge storing region of Claim 35

Claim [35d] of the '365 Patent recites “a multi-layer charge storing region surrounding the tunnel dielectric layer, the multi-layer charge storing region formed in a *substantially annular shape*.” Contrary to the allegations of the Petition, Lee '255 does not teach that what Petitioner identifies as the multi-layer charge storing region is of “substantially annular shape.”

The Petition asserts that “tunnel dielectric layer” 141, “charge storage layer” 142, and “blocking dielectric layer” 143 which are contained within Gate dielectric 150d of Lee '255 satisfy the multi-layer charge storing region limitation. Pet. at 46-49. Lee '255 does not teach that any of these layers have annular shape. Instead, Lee '255 teaches only that “Gate dielectric layer 150d” is annularly shaped. See Lee '255, Fig. 5A. It teaches nothing concerning the *shape* of “tunnel dielectric layer” 141, “charge storage layer” 142, or “blocking dielectric layer” 143, which are contained within Gate dielectric 150d.

The Petition wrongly asserts that “tunnel dielectric layer” 141, “charge storage layer” 142, or “blocking dielectric layer” 143 are of annular shape by relying solely on Fig. 4B and 5A of Lee ’255. Pet. at 48. *See also* Ex. 003, ¶159 (declaration of Dr. Lee similarly relying only on Figs. 4B and 5A). These figures are reproduced below as annotated by Petitioner:



Ex. 1004 (Lee ’255), Figs. 4B, 5A (excerpted and annotated); Ex. 1003, ¶¶157-158.

Pet. at 48. Petitioner does not cite to anything beyond the figures of Lee ’255 to support its argument that the shape of these layers is annular. Indeed, nothing in the teaching of Lee ’255 supports the Petition’s decision to draw the red, green and blue lines in Fig. 5A as circles (annular shapes). Instead, Lee ’255 teaches only that

“tunnel dielectric layer” 141, “charge storage layer” 142, or “blocking dielectric layer” 143 are “substantially extended vertically”:

Referring to FIGS. 4A and 4B, the entirety of a gate dielectric layer 150d between the vertical active pattern 130a and each of the gate patterns 155L, 155al, 155a and 155U may be substantially extended vertically. That is, ***the tunnel dielectric layer 141, charge storage layer 142 and blocking dielectric layer 143 of the gate dielectric layer 150d may be substantially extended vertically.***

Ex. 1004 at [0074]. Lee '255 makes this clarification to distinguish the Fig. 4B embodiment from other embodiments such as that of Fig. 1C where 141, 142 and 143 have multiple ninety-degree angles and horizontal portions. *See id.* [0056], Fig. 1C. However, nothing in this disclosure would lead a POSITA to understand that 141, 142, and 143 have annular shape.

Moreover, the Petition is devoid of any reasoning as to why a POSITA would understand the teaching of Lee '255 above to render the annular shape limitations obvious. Such arguments are an example of prohibited hindsight-based analysis. *See KSR In'l Co. v. Teleflex Inv.*, 550 U.S. at 398, 421 (2007) (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”). *In re Oetiker*, 977 F.2d 1443, 1447 (Fed. Cir. 1992) (“The combination of elements from non-analogous sources, in a manner that reconstructs the applicant's invention only with the benefit of hindsight, is insufficient to present a prima facie case of obviousness.”).

Petitioner's proposed combination with Lee '961 does not solve this problem. The Petition does not contend that Lee '961 teaches the annular shape limitation. Pet. at 48-50. Instead, the Petition relies on Lee '961 only as providing further support for the charge-storing region consisting of multiple layers. Pet. at 48-49. Indeed, the Petition concedes that Lee '961 only teaches a vertical orientation of the layers of the multi-layer charge storing region. Pet. at 49 ("Figure 2a of Lee '961 depicts the vertical structure of the 3D memory device").¹

Accordingly, the Petition fails to show a reasonable likelihood of prevailing on the grounds that Lee '255 and Lee '961, alone or combination, render claim 35 of the '365 Patent obvious.

B. Lee '255 and Lee '961 do not disclose a blocking dielectric layer formed on sidewalls of the opening, a multi-layer charge storage region formed on an inside sidewall of the block dielectric layer or a tunnel dielectric layer formed on an inside sidewall of the multi-layer charge storing region as required by claim 1

Claim 1 of the '365 Patent recites:

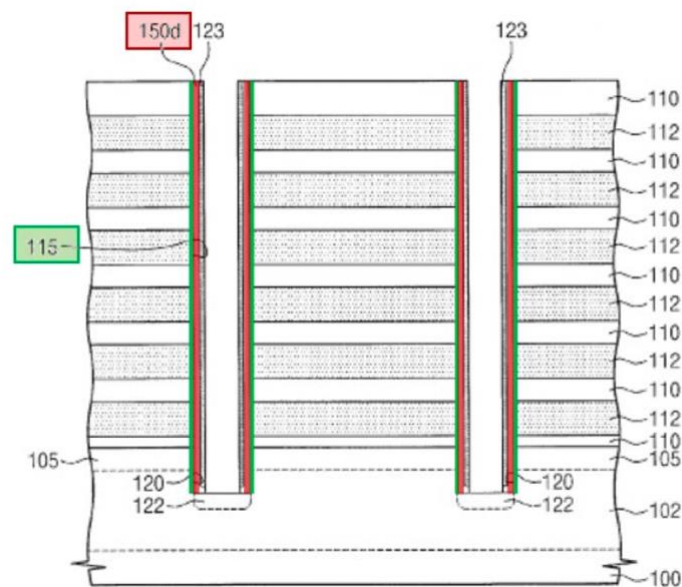
[1b] forming on sidewalls of the opening a blocking dielectric layer;

¹ As the Petition does not rely on the combination of Lee '265 and Lee '961 to teach the "annular shape" of the multi-layer charge storing region, Patent Owner does not need to respond the Petition's arguments concerning motivation to combine at this time. See Pet. at 51-53.

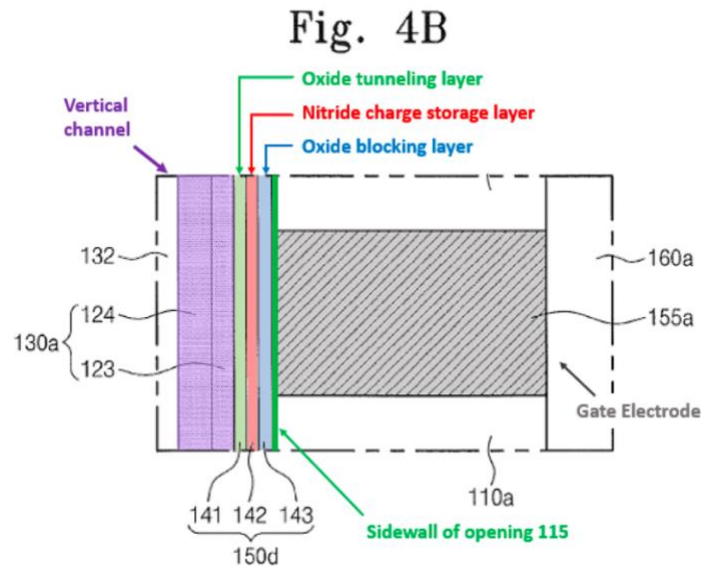
- [1c] forming on an inside sidewall of the blocking dielectric layer a multi-layer charge storing region;
- [1d] forming on an inside sidewall of the multi-layer charge storing region a tunnel dielectric layer; and

According to the Petition, the claim “require[s]” the following “sequence and relative position” “forming a dielectric gate layer 150d in opening 115, with successive blocking, charge-trapping, and tunneling sub-layers.” Petition at 74. The Petition fails to show that Lee ‘255 teaches this order of formation or renders such a sequence obvious.

The Petition notes that Lee ‘255 “teaches forming a dielectric gate layer 150d in opening 115.” Pet. at 74. It goes on to annotate Fig. 9A of Lee ‘255 to show how gate layer 150d is formed on the sidewalls of opening 115:



Pet. 75. The Petition, however, does not contend that gate layer 150d is the claimed “blocking dielectric layer” of limitation [1b]. Instead, it contends that “blocking dielectric layer 143” *contained within* gate layer 150d is the claimed “blocking dielectric layer.” Pet. at 75. Likewise, it contends that two other layers contained within gate layer 150d—charge storage layer 142 and tunneling layer 141—are the multi-layer charge storing region of limitation [1c] and the tunnel dielectric layer of limitation [1d], respectively. Pet. at 75-76 (“Figure 4B provides further details on the layers of gate dielectric layer 150b, showing that (i) blocking dielectric layer 143 (a blocking dielectric layer) (blue) is form[ed] on the sidewalls of the opening (opening 115) (green); (ii) charge storage layer 142 (a . . . charge storage region) (red) is form[ed] on an inside sidewall of the blocking dielectric layer (blue); and (iii) tunneling layer 141 (a tunnel dielectric layer) (light green) is form[ed] on the sidewall of the . . . charge storing region (red)).”). The Petition makes this point clear with its annotated version of Fig. 4B of Lee ’255



Pet. at 76.

The problem for Petitioner, is that Lee '255 does not disclose the “sequence and relative position” of layers 141, 142, and 143. The Petition’s claim that Paragraphs [0056] and [0074] of Lee '255 provide this disclosure is incorrect. Pet. at 76. Instead, these paragraphs at most teach that the layers are located within gate layer 150d – they do not disclose the order or sequence in which they are formed:

[0056] The gate dielectric layer 150 will be described below in more detail with reference to FIG. 1C. Referring to FIG. 1C, according to an embodiment of the inventive concept, the gate dielectric layer 150 may include a tunnel dielectric layer 141, a charge storage layer 142 and a blocking dielectric layer 143. The tunnel dielectric layer 141 ***may be adjacent to the sidewall*** of the vertical active pattern 130, and the blocking dielectric layer 143 ***may be adjacent*** to each of the gate patterns 155L, 155aL, 155a and 155U. The charge storage layer 142 ***may be disposed*** between the tunnel dielectric layer 141 and the blocking dielectric layer 143. According to an embodiment of the inventive concept, as illustrated in FIG. 1C, the entirety of the gate dielectric layer 150 (i.e., the tunnel dielectric layer 141, the charge storage layer 142

and the blocking dielectric layer 143) may be extended to cover the upper and lower surfaces of each of the gate patterns 155L, 155al, 155a and 155U.

Ex. 1004 at [0056] (emphasis added).

[0074] FIG. 4A is a cross-sectional view taken along line I-I' of FIG. 1A for describing further modification example of a 3D semiconductor memory device according to an embodiment of the inventive concept. FIG. 4B is a magnified view of a portion C of FIG. 4A. Referring to FIGS. 4A and 4B, the entirety of a gate dielectric layer 150d between the vertical active pattern 130a and each of the gate patterns 155L, 155al, 155a and 155U may be substantially extended vertically. That is, the tunnel dielectric layer 141, charge storage layer 142 and blocking dielectric layer 143 of the gate dielectric layer 150d ***may be substantially extended vertically***. An extended portion of the gate dielectric layer 150d may be disposed between the vertical active pattern 130a and the insulation pattern 110a. The stack-structure of FIGS. 1A and 1B may have a line shape that is extended in the first direction. Unlike this, the stack-structure may include gate patterns having a flat plate shape. This will be described below with reference to the accompanying drawings.

Ex. 1004 at [0074] (emphasis added). Petitioner does not provide any explanation, evidence or other argument as to why a POSITA would understand the “formed on” limitations to be obvious based on this teaching. Pet. at 74-76. Noteworthy, Dr. Lee, Petitioner’s expert, opines only that the layers are “***positioned***” as required by the claims, not “formed” in sequence as Petitioner asserts is required by the claims. *See, e.g.,* Ex. 1003, ¶¶ 215.

Petitioner’s proposed combination with Lee ‘961 likewise fails to disclose any sequence or ordering as to how they layers are formed. Petitioner relies on Lee ’961

for teaching of including additional layers in the multi-layer charge storage region. Pet. at 76-77. Although Petitioner's expert contends that Lee '961 provides teaching about the order in which its layers are formed, Ex. 1003, ¶¶218, the proposed combination still requires "Lee '255's oxide blocking dielectric layer 143 (blocking dielectric layer) [to] *first* be formed on the inner sidewall of opening 115" and "Lee '255's tunneling oxide layer 141 (tunnel dielectric layer) [to] be formed on the inner surface of the nitride charge storage layer 142" *last*. Ex. 1003, ¶¶220, 222. As discussed above, Lee '255 does not disclose or render obvious any such ordering.

Accordingly, the Petition's challenge to claim 1 fails.

C. Lee '255 and Lee '961 do not disclose a blocking dielectric layer formed on sidewalls of the opening, a multi-layer charge storage region formed on an inside sidewall of the block dielectric layer or a tunnel dielectric layer formed on an inside sidewall of the multi-layer charge storing region or the "annular" shape requirements of claim 23

The Petition's challenge to claim 23 incorporates by reference its arguments as to claim 35 and 1. *See* Pet. at 89-90. These arguments fail for the same reasons. Specifically, the Petition fails show that Lee '255 and Lee '961 disclose the "annular shaped multi-layer charge storing region" limitations of [23c] for the same reasons that they do not disclose the similar limitation in [35d]. Likewise, the references,

alone or in combination, do not disclose the “formed on” limitations of [23b], [23c], and [23d] for the same reasons they do not disclose the similar limitations of [1b], [1c], and [1d].

VI. Conclusion

Because the Petition fails to establish invalidity of independent claims 1, 23, and 35, and the claims that depend thereon, its Ground 1 fails. As Ground 1 fails, the Petition’s Ground 2, which only challenges dependent claims likewise fails. For this reason, Petitioner’s request for institution should be denied.

Date: December 16, 2025

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CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 3,546 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on December 16, 2025, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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