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METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application Number 14/811,346, filed July 28, 2015, which is a continuation of U.S. Patent Application Number 14/159,315, filed on January 20, 2014, now Patent Number 9,093,318, issued on July 28, 2015which is a continuation of U.S. Patent Application number 13/539,466, filed on July 1, 2012, now Patent Number 8,633,537, issued on January 21, 2014, which is a continuation-in-part of Patent Application Number 13/288,919, filed November 3, 2011, now Patent Number 8,859,374, issued on October 14, 2014, which is a divisional of U.S. Patent Number 12/152,518, filed May 13,2008, now U.S. Patent Number 8,063,434, issued November 22, 2011, which claims the benefit of priority to U.S. Provisional Patent Application Number 60/940,160, filed May 25, 2007, all of which application are hereby incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] The present invention relates generally to semiconductor devices, and more particularly to integrated circuits including non-volatile semiconductor memories and methods of fabricating the same.

BACKGROUND

[0003] Non-volatile semiconductor memories are devices that can be electrically erased and reprogrammed. One type of non-volatile memory that is widely used for general storage and transfer of data in and between computers and other electronic devices is flash memory, such as a split gate flash memory. A split gate flash memory transistor has an

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architecture similar to that of a conventional logic transistor, such as Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), in that it also includes a control gate formed over a channel connecting a source and drain in a substrate. However, the memory transistor further includes a memory or charge trapping layer between the control gate and the channel and insulated from both by insulating or dielectric layers. A programming voltage applied to the control gate traps a charge on the charge trapping layer, partially canceling or screening an electric field from the control gate, thereby changing a threshold voltage (V_T) of the transistor and programming the memory cell. During read-out, this shift in V_T is sensed by the presence or absence of current flow through the channel with application of a predetermined read-out voltage. To erase the memory transistor, an erase voltage is applied to the control gate to restore, or reverse the shift in V_T.

[0004] An important measure of merit for flash memories is data retention time, which is the time for which the memory transistor can hold charge or remain programmed without the application of power. The charge stored or trapped in the charge trapping layer decreases over time due to leakage current through the insulating layers, thereby reducing the difference between a programmed threshold voltage (VTP) and an erased threshold voltage (VTE) limiting data retention of the memory transistor.

[0005] One problem with conventional memory transistors and methods of forming the same is that the charge trapping layer typically has poor or decreasing data retention over time, limiting the useful transistor lifetime. Referring to FIG. 1A, if the charge trapping layer is silicon (Si) rich there is a large, initial window or difference between VTP, represented by graph or line 102, and the VTE, represented by line 104, but the window

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collapse very rapidly in retention mode to an end of life (EOL 106) of less than about 1.E+07 seconds.

[0006] Referring to FIG. 1B, if on the other hand the charge trapping layer is if a high quality nitride layer, that is one having a low stoichiometric concentration of Si, the rate of collapse of the window or Vt slope in retention mode is reduced, but the initial program-erase window is also reduced. Moreover, the slope of Vt in retention mode is still appreciably steep and the leakage path is not sufficiently minimized to significantly improve data retention, thus EOL 106 is only moderately improved.

[0007] Another problem is that increasingly semiconductor memories combine logic transistors, such as MOSFET's, with memory transistors in integrated circuits (ICs) fabricated on a common substrate for embedded memory or System-On-Chip (SOC) applications. Many of the current processes for forming performance of memory transistors are incompatible with those used for fabricating logic transistors.

[0008] Accordingly, there is a need for memory transistors and methods of forming the same that provides improved data retention and increased transistor lifetime. It is further desirable that the methods of forming the memory device are compatible with those for forming logic elements in the same IC formed on a common substrate.

SUMMARY OF THE INVENTION

[0009] The present invention provides a solution to these and other problems, and offers further advantages over conventional memory cells or devices and methods of fabricating the same.

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[0010] Generally, the device includes a memory transistor comprising a polysilicon channel region electrically connecting a source region and a drain region formed in a substrate, an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, and a high work function gate electrode formed over a surface of the ONNO stack. In one embodiment, the ONNO stack includes a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer. In another embodiment, the multi-layer charge-trapping region further includes an oxide anti-tunneling layer separating the first nitride layer from the second nitride layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] These and various other features and advantages of the present invention will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

[0012] FIG. 1A is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a large initial difference between programming and erase voltages but which loses charge quickly;

[0013] FIG. 1B is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a smaller initial difference between programming and erase voltages;

[0014] FIGs. 2A through 2D are partial cross-sectional side views of a semiconductor device illustrating a process flow for forming a semiconductor device

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including a logic transistor and non-volatile memory transistor according to an embodiment of the present invention;

[0015] FIG. 3 is a partial cross-sectional side view of a semiconductor device including a logic transistor and non-volatile memory transistor comprising high work function gate electrodes according to an embodiment of the present invention;

[0016] FIGs. 4A and 4B illustrates a cross-sectional view of a non-volatile memory device including an ONONO stack;

[0017] FIG. 5 depicts a flowchart representing a series of operations in a method for fabricating a non-volatile charge trap memory device including an ONONO stack, in accordance with an embodiment of the present invention;

[0018] FIG. 6A illustrates a non-planar multigate device including a multi-layer charge-trapping region;

[0019] FIG. 6B illustrates a cross-sectional view of the non-planar multigate device of FIG. 6A;

[0020] FIGs. 7A and 7B illustrate a non-planar multigate device including a multi-layer charge-trapping region and a horizontal nanowire channel;

[0021] FIG. 7C illustrates a cross-sectional view of a vertical string of non-planar multigate devices of FIG. 7A;

[0022] FIGs. 8A and 8B illustrate a non-planar multigate device including a multi-layer charge-trapping region and a vertical nanowire channel;

[0023] FIGs. 9A through 9F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 8A; and

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[0024] FIGs. 10A through 10F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 8A.

DETAILED DESCRIPTION

[0025] The present invention is directed generally to non-volatile memory transistor including a multi-layer charge storage layer and high work function gate electrode to increase data retention and/or to improve programming time and efficiency. The structure and method are particularly useful for embedded memory or System-On-Chip (SOC) applications in which a semiconductor device includes both a logic transistor and non-volatile memory transistor comprising high work function gate electrodes formed on a common substrate.

[0026] In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures, and techniques are not shown in detail or are shown in block diagram form in order to avoid unnecessarily obscuring an understanding of this description.

[0027] Reference in the description to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification do not necessarily all refer to the same embodiment. The term "to couple" as used herein may include both to directly connect and to indirectly connect through one or more intervening components.

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[0028] Briefly, a non-volatile memory transistor according to the present invention includes a high work function gate electrode formed over an oxide-nitride-oxide (ONO) dielectric stack. By high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased.

[0029] In certain preferred embodiments, the high work function gate electrode comprises a doped polycrystalline silicon or polysilicon (poly) layer, the fabrication of which can be can be readily integrated into standard complementary metal-oxide-semiconductor (CMOS) process flows, such as those used fabricate metal-oxide-semiconductor (MOS) logic transistors, to enable fabrication of semiconductor memories or devices including both memory and logic transistors. More preferably, the same doped polysilicon layer can also be patterned to form a high work function gate electrode for the MOS logic transistor, thereby improving the performance of the logic transistor and increasing the efficiency of the fabrication process. Optionally, the ONO dielectric stack includes a multi-layer charge storage or charge trapping layer to further improve performance, and in particular data retention, of the memory transistor.

[0030] A semiconductor device including a non-volatile memory transistor comprising a high work function gate electrode and methods of forming the same will now be described in detail with reference to FIGs. 2A through 2D, which are partial cross-sectional side views of intermediate structures illustrating a process flow for forming a semiconductor device including both memory and logic transistors. For purposes of clarity, many of the details of semiconductor fabrication that are widely known and are not relevant to the present invention have been omitted from the following description.

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[0031] Referring to FIG. 2, fabrication of the semiconductor device begins with formation of an ONO dielectric stack 202 over a surface 204 of a wafer or substrate 206. Generally, the ONO dielectric stack 202 includes a thin, lower oxide layer or tunneling oxide layer 208 that separates or electrically isolates a charge trapping or storage layer 210 from a channel region (not shown) of the memory transistor in the substrate 206, and a top or blocking oxide layer 212. Preferably, as noted above and as shown in FIGs. 2A-2D, the charge storage layer 210 is a multi-layer charge storage layer including at least a top, charge trapping oxynitride layer 210A and a lower, substantially trap free oxynitride layer 210B.

[0032] Generally, the substrate 206 may include any known silicon-based semiconductor material including silicon, silicon-germanium, silicon-on-insulator, or silicon-on-sapphire substrate. Alternatively, the substrate 206 may include a silicon layer formed on a non-silicon-based semiconductor material, such as gallium-arsenide, germanium, gallium-nitride, or aluminum-phosphide. Preferably, the substrate 206 is a doped or undoped silicon substrate.

[0033] The lower oxide layer or tunneling oxide layer 208 of the ONO dielectric stack 202 generally includes a relatively thin layer of silicon dioxide (SiO_2) of from about 15 angstrom (Å) to about 22 Å, and more preferably about 18 Å. The tunneling oxide layer 208 can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using chemical vapor deposition (CVD). In a preferred embodiment, the tunnel dielectric layer is formed or grown using a steam anneal. Generally, the process includes a wet-oxidizing method in which the substrate 206 is placed in a deposition or processing chamber, heated to a temperature from about 700°C to about 850°C, and exposed to a wet vapor for a predetermined period of time selected based on a

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desired thickness of the finished tunneling oxide layer 208. Exemplary process times are from about 5 to about 20 minutes. The oxidation can be performed at atmospheric or at low pressure.

[0034] In a preferred embodiment, the oxynitride layers 210A, 210B, of the multi-layer charge storage layer 210 are formed or deposited in separate steps utilizing different processes and process gases or source materials, and have an overall or combined thickness of from about 70 Å to about 150 Å, and more preferably about 100 Å. The lower, trap free oxynitride layer 210B can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a process gas including a silicon source, such as silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane (SiH_2Cl_2), tetrachlorosilane ($SiCl_4$), a nitrogen source, such as nitrogen (N_2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas, such as oxygen (O_2) or N_2O. In one embodiment the trap free oxynitride layer 210B is deposited in a low pressure CVD process using a process gas including dichlorosilane, NH_3 and N_2O, while maintaining the chamber at a pressure of from about 5 millitorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm).

[0035] The top, charge trapping oxynitride layer 210A can be deposited over the bottom oxynitride layer 210B in a CVD process using a process gas including Bis-

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TertiaryButylAminoSilane (BTBAS). It has been found that the use of BTBAS increases the number of deep traps formed in the oxynitride by increasing the carbon level in the charge trapping oxynitride layer 210A. Moreover, these deep traps reduce charge losses due to thermal emission, thereby further improving data retention. More preferably, the process gas includes BTBAS and ammonia (NH_3) mixed at a predetermined ratio to provide a narrow band gap energy level in the oxynitride charge trapping layer. In particular, the process gas can include BTBAS and NH_3 mixed in a ratio of from about 7:1 to about 1:7. For example, in one embodiment the charge trapping oxynitride layer 210A is deposited in a low pressure CVD process using BTBAS and ammonia NH_3 at a chamber pressure of from about 5 mT to about 500 mT, and at a substrate temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes.

[0036] It has been found that an oxynitride layer produced or deposited under the above conditions yields a trap-rich oxynitride layer 210A, which improves the program and erase speed and increases of the initial difference (window) between program and erase voltages without compromising a charge loss rate of the memory transistor, thereby extending the operating life (EOL) of the device. Preferably, the charge trapping oxynitride layer 210A has a charge trap density of at least about 1E10/cm^2, and more preferably from about 1E12/cm^2 to about 1E14/cm^2.

[0037] Alternatively, the charge trapping oxynitride layer 210A can be deposited over the bottom oxynitride layer 210B in a CVD process using a process gas including BTBAS and substantially not including ammonia (NH_3). In this alternative embodiment of the method, the step of depositing the top, charge trapping oxynitride layer 210A is

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followed by a thermal annealing step in a nitrogen atmosphere including nitrous oxide (N_2O), NH_3, and/or nitrogen oxide (NO).

[0038] Preferably, the top, charge trapping oxynitride layer 210A is deposited sequentially in the same CVD tool used to form the bottom, trap free oxynitride layer 210B, substantially without breaking vacuum on the deposition chamber. More preferably, the charge trapping oxynitride layer 210A is deposited substantially without altering the temperature to which the substrate 206 was heated during deposition of the trap free oxynitride layer 210B.

[0039] A suitable thickness for the lower, trap free oxynitride layer 210B has been found to be from about 10 Å to about 80 Å, and a ratio of thicknesses between the bottom layer and the top, charge trapping oxynitride layer has been found to be from about 1:6 to about 6:1 , and more preferably at least about 1:4.

[0040] The top oxide layer 212 of the ONO dielectric stack 202 includes a relatively thick layer of SiO_2 of from about 20 Å to about 70 Å, and more preferably about 45 Å. The top oxide layer 212 can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using CVD. In a preferred embodiment, the top oxide layer 212 is a high-temperature-oxide (HTO) deposited using CVD process. Generally, the deposition process includes exposing the substrate 306 to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-containing gas, such as O_2 or N_2O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

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[0041] Preferably, the top oxide layer 212 is deposited sequentially in the same tool used to form the oxynitride layers 210A, 210B. More preferably, the oxynitride layers 210A, 210B, and the top oxide layer 212 are formed or deposited in the same tool used to grow the tunneling oxide layer 208. Suitable tools include, for example, an ONO AVP, commercially available from AVIZA technology of Scotts Valley, California.

[0042] Referring to FIG. 2B, in those embodiments in which the semiconductor device is to further include a logic transistor, such as a MOS logic transistor, formed on the surface of the same substrate the ONO dielectric stack 202 is removed from a region or area of the surface 204 in which the logic transistor is to be formed, and an oxide layer 214 the formed thereon.

[0043] Generally, the ONO dielectric stack 202 is removed from the desired region or area of the surface 204 using standard photolithographic and oxide etch techniques. For example, in one embodiment a patterned mask layer (not shown) is formed from a photo-resist deposited on the ONO dielectric stack 202, and the exposed region etched or removed using a low pressure radiofrequency (RF) coupled or generated plasma comprising fluorinated hydrocarbon and/or fluorinated carbon compounds, such as $C_2H_2F_4$ commonly referred to as Freon®. Generally, the processing gas further includes argon (Ar) and nitrogen (N_2) at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

[0044] The oxide layer 214 of the logic transistor can include a layer of SiO_2 having a thickness of from about 30 to about 70 Å, and can be thermally grown or deposited using CVD. In one embodiment, the oxide layer 214 is thermally grown using a steam oxidation process, for example, by maintaining the substrate 206 in a steam atmosphere at a

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temperature of from about 650°C to about 850°C for a period of from about 10 minutes to about 120 minutes.

[0045] Next, a doped polysilicon layer is formed on a surface of the ONO dielectric stack 202 and, preferably, the oxide layer 214 of the logic transistor. More preferably, the substrate 206 is a silicon substrate or has a silicon surface on which the ONO dielectric stack is formed to form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a SONOS memory transistor.

[0046] Referring to FIG. 2C, forming of the doped polysilicon layer begins with the deposition of a conformal polysilicon layer 216 having a thickness of from about 200 Å to about 2000 Å over the ONO dielectric stack 202 and the oxide layer 214. The polysilicon layer 216 can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a silicon source or precursor. In one embodiment the polysilicon layer 216 is deposited in a low pressure CVD process using a silicon containing process gas, such as silane or dichlorosilane, and N_2, while maintaining the substrate 206 in a chamber at a pressure of from about 5 to 500 mT, and at a temperature of from about 600°C to about 1000°C for a period of from about 20 minutes to about 100 minutes to a substantially undoped polysilicon layer. The polysilicon layer 216 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or difluoroborane (BF_2) to the CVD chamber during the low pressure CVD process.

[0047] In one embodiment, the polysilicon layer 216 is doped following the growth or formation in the LPCVD process using ion implantation process. For example, the polysilicon layer 216 can be doped by implanting boron (B^+) or BF_2 ions at an energy of

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from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) SONOS memory transistor and, preferably, a P-type (PMOS) logic transistor having high work function gate electrodes. More preferably, the polysilicon layer 216 is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV.

[0048] Alternatively, the polysilicon layer 216 can be doped by ion implantation after patterning or etching the polysilicon layer and the underlying dielectric layers. It will be appreciated that this embodiment includes additional masking steps to protect exposed areas of the substrate 206 surface 204 and/or the dielectric layers from receiving undesired doping. However, generally such a masking step is included in existing process flows regardless of whether the implantation occurs before or after patterning.

[0049] Referring to FIG. 2D, the polysilicon layer 216 and the underlying dielectric stack 202 and oxide layer 214 are patterned or etched to form high work function gate electrodes 218 of the memory transistor 220 and logic transistor 222. In one embodiment polysilicon layer 216 can be etched or patterned using a plasma comprising hydrobromic acid (HBr), chlorine (CL_2) and/or oxygen (O_2) at a pressure of about 25 mTorr, and a power of about 450 W. The oxide layers 208, 212, 214, and oxynitride layers 210A, 210B, can be etched using standard photolithographic and oxide etch techniques as described. For example, in one embodiment the patterned polysilicon layer 216 is used as a mask, and the exposed oxide layers 208, 212, 214, and oxynitride layers 210A, 210B, etched or removed using low pressure RF plasma. Generally, the plasma is formed from a processing gas comprising a fluorinated hydrocarbon and/or fluorinated carbon compounds, and further

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including Ar and N_2 at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

[0050] Finally, the substrate is thermal annealed with a single or multiple annealing steps at a temperature of from about 800 °C to about 1050 °C for a time of from about 1second to about 5 minutes to drive in ions implanted in the polysilicon layer 216, and to repair damage to the crystal structure of the polysilicon layer caused by ion implantation. Alternatively, advanced annealing techniques, such as flash and laser, can be employed with temperatures as high as 1350 °C and anneal times as low as 1 millisecond.

[0051] A partial cross-sectional side view of a semiconductor device 300 including a logic transistor 302 and non-volatile memory transistor 304 comprising high work function gate electrodes according to an embodiment of the present invention is shown in FIG. 3. Referring to FIG. 3, the memory transistor 304 is formed on a silicon substrate 306 and comprises a high work function gate electrode 308 formed from a doped polysilicon layer overlying a dielectric stack 310. The dielectric stack 310 overlies and controls current through a channel region 312 separating heavily doped source and drain (S/D) regions 314. Preferably, the dielectric stack 310 includes a tunnel dielectric layer 316, a multi-layer charge storage layer 318A, 318B, and a top or blocking oxide layer 320. More preferably, the multi-layer charge storage layer 318A, 318B, includes at least a top, charge trapping oxynitride layer 318A and a lower, substantially trap free oxynitride layer 318B. Optionally, as shown in FIG. 3, the memory transistor 304 further includes one or more sidewall spacers 322 surrounding the gate stack to electrically insulate it from contacts (not shown) to the S/D regions 320 and from other transistors in the semiconductor device formed on the substrate 306.

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[0052] The logic transistor 302 comprises a gate electrode 324 overlying an oxide layer 326 formed over a channel region 328 separating heavily doped source and drain regions 330, and, optionally, can include one or more sidewall spacers 332 surrounding the gate electrically insulate it from contacts (not shown) to the S/D regions. Preferably, as shown in FIG. 3, the gate electrode 324 of the logic transistor 302 also comprises a high work function gate electrode formed from a doped polysilicon layer.

[0053] Generally, the semiconductor device 300 further includes a number of isolation structures 334, such as a local oxidation of silicon (LOCOS) region or structure, a field oxidation region or structure (FOX), or a shallow trench isolation (STI) structure to electrically isolate individual transistors formed on the substrate 306 from one another.

Implementations and Alternatives

[0054] In one aspect the present disclosure is directed to semiconductor devices including memory transistors with a high work function gate electrode and a multi-layer charge-trapping region. FIG. 4A is a block diagram illustrating a cross-sectional side view of an embodiment of one such memory transistor 400. The memory transistor 400 includes a ONNO stack 402 including an ONNO structure 404 formed over a surface 406 of a substrate 408. Substrate 408 includes one or more diffusion regions 410, such as source and drain regions, aligned to the gate stack 402 and separated by a channel region 412. Generally, the ONNO stack 402 includes a high work function gate electrode 414 formed upon and in contact with the ONNO structure 404. The high work function gate electrode 414 is separated or electrically isolated from the substrate 408 by the ONNO structure 404. The ONNO structure 404 includes a thin, lower oxide layer or tunnel dielectric layer 416

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that separates or electrically isolates the ONNO stack 402 from the channel region 412, a top or blocking dielectric layer 420, and a multi-layer charge-trapping region 422.

[0055] The nanowire channel region 412 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 412 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[0056] The high work function gate electrode 414 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. As noted above, the polysilicon layer of the high work function gate electrode 414 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or difluoroborane (BF_2) to the CVD chamber during the low pressure CVD process, or can be doped following the growth or formation in the CVD process using an ion implantation process. In either embodiment, the polysilicon layer of the high work function gate electrode 414 is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 414 is doped by implanting boron (B^+) or BF_2 ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) memory transistor.

[0057] The tunnel dielectric layer 416 may be any material and have any thickness suitable to allow charge carriers to tunnel into the multi-layer charge-trapping region 422 under an applied gate bias while maintaining a suitable barrier to leakage when the memory

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transistor 400 is unbiased. In one embodiment, the tunnel dielectric layer 416 is formed by a thermal oxidation process and is composed of silicon dioxide or silicon oxy-nitride, or a combination thereof. In another embodiment, the tunnel dielectric layer 416 is formed by chemical vapor deposition (CVD) or atomic layer deposition (ALD) and is composed of a dielectric layer which may include, but is not limited to, silicon nitride, hafnium oxide, zirconium oxide, hafnium silicate, hafnium oxy-nitride, hafnium zirconium oxide and lanthanum oxide. In a specific embodiment, the tunnel dielectric layer 416 has a thickness in the range of 1-10 nanometers. In a particular embodiment, the tunnel dielectric layer 416 has a thickness of approximately 2 nanometers.

[0058] In one embodiment, the blocking dielectric layer 420 comprises a high temperature oxide (HTO). The higher quality HTO oxide enables the blocking dielectric layer 420 to be scaled in thickness. In an exemplary embodiment, the thickness of the blocking dielectric layer 420 comprising a HTO oxide is between 2.5 nm and 10.0 nm.

[0059] In another embodiment, the blocking dielectric layer 420 is further modified to incorporate nitrogen. In one such embodiment, the nitrogen is incorporated in the form of an ONO stack across the thickness of the blocking dielectric layer 420. Such a sandwich structure in place of the conventional pure oxygen blocking dielectric layer advantageously reduces the EOT of the entire stack 402 between the channel region 412 and high work function gate electrode 414 as well as enable tuning of band offsets to reduce back injection of carriers. The ONO stack blocking dielectric layer 420 can then be incorporated with the tunnel dielectric layer 416 and the multi-layer charge trapping layer 422 comprising an oxygen-rich first nitride layer 422a, an oxygen-lean second nitride layer 422b and an anti-tunneling layer 422c.

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[0060] The multi-layer charge-trapping region 422 generally includes at least two nitride layers having differing compositions of silicon, oxygen and nitrogen, including an oxygen-rich, first nitride layer 422a, and a silicon-rich, nitrogen-rich, and oxygen-lean second nitride layer 422b, a silicon-rich. In some embodiments, such as that shown in FIG. 4B, the multi-layer charge-trapping region further includes an anti-tunneling layer 422c comprising an oxide, such as silicon dioxide, separating the oxygen-lean second nitride layer 422b from the oxygen-rich, first nitride layer 422a, to provide a ONONO stack 402 including an ONONO structure 404.

[0061] It has been found that an oxygen-rich, first nitride layer 422a decreases the charge loss rate after programming and after erase, which is manifested in a small voltage shift in the retention mode, while a silicon-rich, nitrogen-rich, and oxygen-lean second nitride layer 422b improves the speed and increases of the initial difference between program and erase voltage without compromising a charge loss rate of memory transistors made using an embodiment of the silicon-oxide-oxynitride-oxide-silicon structure, thereby extending the operating life of the device.

[0062] It has further been found the anti-tunneling layer 422c substantially reduces the probability of electron charge that accumulates at the boundaries of the oxygen-lean second nitride layer 422b during programming from tunneling into the first nitride layer 422a, resulting in lower leakage current than for a conventional non-volatile memory transistor.

[0063] The multi-layer charge-trapping region can have an overall thickness of from about 50 Å to about 150 Å, and in certain embodiments less than about 100 Å, with

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the with the thickness of the anti-tunneling layer 422c being from about 5 Å to about 20 Å, and the thicknesses of the nitride layers 404b, 404a, being substantially equal.

[0064] A method or forming or fabricating a semiconductor device including a memory transistor with a high work function gate electrode and a multi-layer charge-trapping region according to one embodiment will now be described with reference to the flowchart of FIG. 5.

[0065] Referring to FIG. 5, the method begins with forming a tunnel dielectric layer, such as a first oxide layer, over a silicon containing layer on a surface of a substrate (500). The tunnel dielectric layer can be formed or deposited by any suitable means, including a plasma oxidation process, In-Situ Steam Generation (ISSG) or a radical oxidation process. In one embodiment, the radical oxidation process involves flowing hydrogen (H_2) and oxygen (O_2) gas into a processing chamber or furnace to effect growth of a the tunnel dielectric layer by oxidation consumption of a portion of the substrate.

[0066] Next, an oxygen-rich first nitride layer of the multi-layer charge-trapping region is formed on a surface of the tunnel dielectric layer (502). In one embodiment, the oxygen-rich first nitride layer is formed or deposited in a low pressure CVD process using a silicon source, such as silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane or DCS (SiH_2Cl_2), tetrachlorosilane ($SiCl_4$) or Bis-TertiaryButylAmino Silane (BTBAS), a nitrogen source, such as nitrogen (N_2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas, such as oxygen (O_2) or N_2O. Alternatively, gases in which hydrogen has been replaced by deuterium can be used, including, for example, the substitution of deuterated-ammonia (ND_3) for NH_3. The substitution of deuterium for hydrogen advantageously passivates Si dangling bonds at the silicon-oxide

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interface, thereby increasing an NBTI (Negative Bias Temperature Instability) lifetime of the devices.

[0067] For example, the lower or oxygen-rich first nitride layer can be deposited over the tunnel dielectric layer by placing the substrate in a deposition chamber and introducing a process gas including N_2O, NH_3 and DCS, while maintaining the chamber at a pressure of from about 5 milliTorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700 degrees Celsius to about 850 degrees Celsius and in certain embodiments at least about 760 degrees Celsius, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm). It has been found that an oxynitride layer produced or deposited under these condition yields a silicon-rich, oxygen-rich first nitride layer.

[0068] Next, an anti-tunneling layer is formed or deposited on a surface of the first nitride layer (504). As with the tunnel dielectric layer, the anti-tunneling layer can be formed or deposited by any suitable means, including a plasma oxidation process, In-Situ Steam Generation (ISSG) or a radical oxidation process. In one embodiment, the radical oxidation process involves flowing hydrogen (H_2) and oxygen (O_2) gas into a batch-processing chamber or furnace to effect growth of the anti-tunneling layer by oxidation consumption of a portion of the first nitride layer.

[0069] The top or oxygen-lean second nitride layer of the multi-layer charge-trapping region is then formed on a surface of the anti-tunneling layer (506). The oxygen-

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lean second nitride layer can be deposited over the anti-tunneling layer in a CVD process using a process gas including N_2O, NH_3 and DCS, at a chamber pressure of from about 5 mT to about 500 mT, and at a substrate temperature of from about 700 degrees Celsius to about 850 degrees Celsius and in certain embodiments at least about 760 degrees Celsius, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 20 sccm. It has been found that a nitride layer produced or deposited under these condition yields a silicon-rich, nitrogen-rich, and oxygen-lean second nitride layer, which improves the speed and increases of the initial difference between program and erase voltage without compromising a charge loss rate of memory transistors made using an embodiment of the silicon-oxide-oxynitride-oxide-silicon structure, thereby extending the operating life of the device.

[0070] In some embodiments, the oxygen-lean second nitride layer can be deposited over the anti-tunneling layer in a CVD process using a process gas including BTBAS and ammonia (NH_3) mixed at a ratio of from about 7:1 to about 1:7 to further include a concentration of carbon selected to increase the number of traps therein. The selected concentration of carbon in the second oxynitride layer can include a carbon concentration of from about 5% to about 15%.

[0071] Next, a top, blocking oxide layer or blocking dielectric layer is formed on a surface of the oxygen-lean second nitride layer of the multi-layer charge-trapping region (508). As with the tunnel dielectric layer and the anti-tunneling layer the blocking dielectric

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layer can be formed or deposited by any suitable means, including a plasma oxidation process, In-Situ Steam Generation (ISSG) or a radical oxidation process. In one embodiment, the blocking dielectric layer comprises a high-temperature-oxide (HTO) deposited using CVD process. Generally, the deposition process includes exposing the substrate 306 to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-containing gas, such as O_2 or N_2O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

[0072] Alternatively, the blocking dielectric layer is formed using an ISSG oxidation process. In one embodiment, the ISSG is performed in an RTP chamber, such as the ISSG chamber from Applied Materials described above, at pressures of from about 8 to 12 Torr and a temperature of about 1050 °C with an oxygen rich gas mixture hydrogen to which from about 0.5% to 33% hydrogen has been added.

[0073] It will be appreciated that in either embodiment the thickness of the second nitride layer may be adjusted or increased as some of the oxygen-lean second nitride layer will be effectively consumed or oxidized during the process of forming the blocking dielectric layer.

[0074] Finally, a high work function gate electrode is formed upon and in contact with the blocking dielectric layer (510). The high work function gate electrode includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. As noted above, the polysilicon layer of the high work function gate electrode can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or

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difluoroborane (BF_2) to the CVD chamber during the low pressure CVD process, or can be doped following the growth or formation in the CVD process using an ion implantation process. In either embodiment, the polysilicon layer of the high work function gate electrode is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode is doped by implanting boron (B^+) or BF_2 ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) memory transistor.

[0075] With the completion of the gate stack fabrication, further processing may occur as known in the art to conclude fabrication of a SONOS-type memory device.

[0076] In another aspect the present disclosure is also directed to multigate or multigate-surface memory transistors including charge-trapping regions overlying two or more sides of a channel region formed on or above a surface of a substrate, and methods of fabricating the same. Multigate devices include both planar and non-planar devices. A planar multigate device (not shown) generally includes a double-gate planar device in which a number of first layers are deposited to form a first gate below a subsequently formed channel region, and a number of second layers are deposited thereover to form a second gate. A non-planar multigate device generally includes a horizontal or vertical channel region formed on or above a surface of a substrate and surrounded on three or more sides by a gate.

[0077] FIG. 6A illustrates one embodiment of a non-planar multigate memory transistor including with a high work function gate electrode. Referring to FIG. 6A, the

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memory transistor 600, commonly referred to as a finFET, includes a channel region 602 formed from a thin film or layer of semiconducting material overlying a surface 604 on a substrate 606 connecting a source region 608 and a drain region 610 of the memory transistor. The channel region 602 is enclosed on three sides by a fin which forms a gate 612 of the device. The thickness of the gate 612 (measured in the direction from source region to drain region) determines the effective channel region length of the device. As with the embodiments described above, the channel region 602 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 602 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[0078] In accordance with the present disclosure, the non-planar multigate memory transistor 600 of FIG. 6A can include a high work function gate electrode and a multi-layer charge-trapping region. FIG. 6B is a cross-sectional view of a portion of the non-planar memory transistor of FIG. 6A including a portion of the substrate 606, channel region 602 and the gate 612 illustrating a high work function gate electrode 614 and a multi-layer charge-trapping region 616. The gate 612 further includes a tunnel dielectric layer 618 overlying a raised channel region 602, and a blocking dielectric layer 620 overlying the blocking dielectric layer to form a control gate of the memory transistor 600. The channel region 602 and gate 612 can be formed directly on substrate 606 or on an insulating or dielectric layer 622, such as a buried oxide layer, formed on or over the substrate.

[0079] As with the embodiments described above, the high work function gate electrode 614 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. The polysilicon

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layer of the high work function gate electrode 614 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, and is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 614 is doped to a concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2}.

[0080] Referring to FIG. 6B, the multi-layer charge-trapping region 616 includes at least one lower or bottom oxygen-rich first nitride layer 616a including nitride closer to the tunnel dielectric layer 618, and an upper or top oxygen-lean second nitride layer 616b overlying the oxygen-rich first nitride layer. Generally, the oxygen-lean second nitride layer 616b includes a silicon-rich, oxygen-lean nitride layer and includes a majority of a charge traps distributed in the multi-layer charge-trapping region, while the oxygen-rich first nitride layer 616a includes an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the oxygen-lean second nitride layer to reduce the number of charge traps therein. By oxygen-rich it is meant wherein a concentration of oxygen in the oxygen-rich first nitride layer 616a is from about 15 to about 40%, whereas a concentration of oxygen in oxygen-lean second nitride layer 616b is less than about 5%.

[0081] In one embodiment, the blocking dielectric 620 also includes an oxide, such as an HTO, to provide an ONNO structure. The channel region 602 and the overlying ONNO structure can be formed directly on a silicon substrate 606 and overlaid with a high work function gate electrode 614 to provide a SONNOS structure.

[0082] In some embodiments, such as that shown in FIG. 6B, the multi-layer charge-trapping region 616 further includes at least one thin, intermediate or anti-tunneling

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layer 616c including a dielectric, such as an oxide, separating the oxygen-lean second nitride layer 616b from the oxygen-rich first nitride layer 616a. As noted above, the anti-tunneling layer 616c substantially reduces the probability of electron charge that accumulates at the boundaries of the oxygen-lean second nitride layer 616b during programming from tunneling into the first nitride layer 616a.

[0083] As with the embodiments described above, either or both of the oxygen-rich first nitride layer 616a and the oxygen-lean second nitride layer 616b can include silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The oxygen-lean second nitride layer 616b has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the oxygen-rich first nitride layer 616a, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

[0084] In those embodiments including an intermediate or anti-tunneling layer 616c including oxide, the anti-tunneling layer can be formed by oxidation of the bottom oxynitride layer, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100 degrees Celsius using a single wafer tool, or 800-900 degrees Celsius using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor

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using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0085] Finally, in those embodiments including a blocking dielectric 620 including oxide the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of the blocking dielectric 620 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric 620 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the top nitride thickness may be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer. A third option is to oxidize the second nitride layer to a chosen depth using radical oxidation.

[0086] A suitable thickness for the oxygen-rich first nitride layer 616a may be from about 30Å to about 160Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 616c. A suitable thickness for the oxygen-lean second nitride layer 616b may be at least 30Å. In certain embodiments, the oxygen-lean second nitride layer 616b may be formed up to 130Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric 620. A ratio of thicknesses between the oxygen-rich first nitride layer 616a and oxygen-lean second nitride layer 616b is approximately 1:1 in some embodiments, although other ratios are also possible.

[0087] In other embodiments, either or both of the oxygen-lean second nitride layer 616b and the blocking dielectric 620 may include a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

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[0088] In another embodiment, shown in FIGs. 7A and 7B, the memory transistor can include a nanowire channel region formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source region and a drain region of the memory transistor. By nanowire channel region it is meant a conducting channel region formed in a thin strip of crystalline silicon material, having a maximum cross-sectional dimension of about 10 nanometers (nm) or less, and more preferably less than about 6 nm.

[0089] Referring to FIG. 7A, the memory transistor 700 includes a horizontal nanowire channel region 702 formed from a thin film or layer of semiconducting material on or overlying a surface on a substrate 706, and connecting a source region 708 and a drain region 710 of the memory transistor. In the embodiment shown, the device has a gate-all-around (GAA) structure in which the nanowire channel region 702 is enclosed on all sides by a gate 712 of the device. The thickness of the gate 712 (measured in the direction from source region to drain region) determines the effective channel region length of the device. As with the embodiments described above, the nanowire channel region 702 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 702 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[0090] In accordance with the present disclosure, the non-planar multigate memory transistor 700 of FIG. 7A can include a high work function gate electrode and a multi-layer charge-trapping region. FIG. 7B is a cross-sectional view of a portion of the non-planar memory transistor of FIG. 7A including a portion of the substrate 706, nanowire channel region 702 and the gate 712 illustrating a high work function gate electrode 714 and a

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multi-layer charge-trapping region 716a-716c. Referring to FIG. 7B, the gate 712 further includes a tunnel dielectric layer 718 overlying the nanowire channel region 702, and a blocking dielectric layer 720.

[0091] As with the embodiments described above, the high work function gate electrode 714 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. The polysilicon layer of the high work function gate electrode 714 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, and is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 714 is doped to a concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2}.

[0092] The multi-layer charge-trapping region 716a-716c includes at least one inner oxygen-rich first nitride layer 716a comprising nitride closer to the tunnel dielectric layer 718, and an outer oxygen-lean second nitride layer 716b overlying the oxygen-rich first nitride layer. Generally, the outer oxygen-lean second nitride layer 716b comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in the multi-layer charge-trapping region, while the oxygen-rich first nitride layer 716a comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the outer oxygen-lean second nitride layer to reduce the number of charge traps therein.

[0093] In some embodiments, such as that shown, the multi-layer charge-trapping region 716 further includes at least one thin, intermediate or anti-tunneling layer 716c

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comprising a dielectric, such as an oxide, separating outer oxygen-lean second nitride layer 716b from the oxygen-rich first nitride layer 716a. The anti-tunneling layer 716c substantially reduces the probability of electron charge that accumulates at the boundaries of outer oxygen-lean second nitride layer 716b during programming from tunneling into the oxygen-rich first nitride layer 716a, resulting in lower leakage current.

[0094] As with the embodiment described above, either or both of the oxygen-rich first nitride layer 716a and the outer oxygen-lean second nitride layer 716b can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The outer oxygen-lean second nitride layer 716b has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the oxygen-rich first nitride layer 716a, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

[0095] In those embodiments including an intermediate or anti-tunneling layer 716c comprising oxide, the anti-tunneling layer can be formed by oxidation of the oxygen-rich first nitride layer 716a, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100 degrees Celsius using a single wafer tool, or 800-900 degrees Celsius using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15

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Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0096] Finally, in those embodiments in which the blocking dielectric 720 comprises oxide, the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of blocking dielectric layer 720 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric layer 720 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the thickness of the outer oxygen-lean second nitride layer 716b may need to be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer.

[0097] A suitable thickness for the oxygen-rich first nitride layer 716a may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 716c. A suitable thickness for the outer oxygen-lean second nitride layer 716b may be at least 30Å. In certain embodiments, the outer oxygen-lean second nitride layer 716b may be formed up to 70Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric layer 720. A ratio of thicknesses between the oxygen-rich first nitride layer 716a and the outer oxygen-lean second nitride layer 716b is approximately 1:1 in some embodiments, although other ratios are also possible.

[0098] In other embodiments, either or both of the outer oxygen-lean second nitride layer 716b and the blocking dielectric layer 720 may comprise a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO,

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Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0099] Figure 7C illustrates a cross-sectional view of a vertical string of non-planar multigate devices 700 of FIG. 7A arranged in a Bit-Cost Scalable or BiCS architecture 726. The architecture 726 consists of a vertical string or stack of non-planar multigate devices 700, where each device or cell includes a channel region 702 overlying the substrate 706, and connecting a source region and a drain region (not shown in this figure) of the memory transistor, and having a gate-all-around (GAA) structure in which the nanowire channel region 702 is enclosed on all sides by a gate 712. The BiCS architecture reduces number of critical lithography steps compared to a simple stacking of layers, leading to a reduced cost per memory bit.

[00100] In another embodiment, the memory transistor is or includes a non-planar device comprising a vertical nanowire channel region formed in or from a semiconducting material projecting above or from a number of conducting, semiconducting layers on a substrate. In one version of this embodiment, shown in cut-away in FIG. 8A, the memory transistor 800 comprises a vertical nanowire channel region 802 formed in a cylinder of semiconducting material connecting a source region 804 and drain region 806 of the device. The channel region 802 is surrounded by a tunnel dielectric layer 808, a multi-layer charge-trapping region 810, a blocking dielectric layer 812 and a high work function gate electrode 814 overlying the blocking dielectric layer to form a control gate of the memory transistor 800. The channel region 802 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or can include an annular layer formed over a cylinder of dielectric filler material. As with the horizontal nanowires

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described above, the channel region 802 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 802 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[00101] As with the embodiments described above, the high work function gate electrode 814 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. The polysilicon layer of the high work function gate electrode 814 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, and is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 814 is doped to a concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2}.

[00102] In some embodiments, such as that shown in FIG. 8B, the multi-layer charge-trapping region 810 includes at least an inner or oxygen-rich first nitride layer 810a closest to the tunnel dielectric layer 808, and an outer or oxygen-lean second nitride layer 810b. Optionally, as in the embodiment shown, the oxygen-rich first nitride layer 810a and the oxygen-lean second nitride layer 810b are separated by an intermediate oxide or anti-tunneling layer 810c comprising oxide.

[00103] Either or both of the oxygen-rich first nitride layer 810a and the oxygen-lean second nitride layer 810b can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures

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in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer.

[00104] Finally, either or both of the oxygen-lean second nitride layer 810b and the blocking dielectric layer 812 may comprise a high K dielectric, such as HfSiON, HfSiO, HfO, ZrSiON, ZrSiO, ZrO, or Y_2O_3.

[00105] A suitable thickness for the oxygen-rich first nitride layer 810a may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 820. A suitable thickness for the oxygen-lean second nitride layer 810b may be at least 30Å, and a suitable thickness for the blocking dielectric layer 812 may be from about 30-70Å.

[00106] The memory transistor 800 of FIG. 8A can be made using either a gate first or a gate last scheme. FIGs. 9A-F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 8A. FIGs. 20A-F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 8A.

[00107] Referring to FIG. 9A, in a gate first scheme a first or lower dielectric layer 902, such as an oxide, is formed over a first, doped diffusion region 904, such as a source region or a drain region, in a substrate 906. A high work function gate electrode 908 is formed over the first dielectric layer 902 to form a control gate of the device, and a second or upper dielectric layer 910 formed thereover. As with embodiments described above, the high work function gate electrode 908 can be formed by depositing and/or doping polysilicon layer having a thickness of from about 200 Å to about 2000 Å and a dopant concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2} so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about

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5.3 eV. The polysilicon layer can be deposited in a low pressure CVD process as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, or can be doped using an ion implantation process following deposition.

[00108] The first and second dielectric layers 902, 910, can be deposited by CVD, radical oxidation or be formed by oxidation of a portion of the underlying layer or substrate. Generally the thickness of the high work function gate electrode 908 is from about 40-50Å, and the first and second dielectric layers 902, 910, from about 20- 80Å.

[00109] Referring to FIG. 9B, a first opening 912 is etched through the overlying high work function gate electrode 908, and the first and second dielectric layers 902, 910, to the diffusion region 904 in the substrate 906. Next, layers of a tunneling oxide 914, charge-trapping region 916, and blocking dielectric 918 are sequentially deposited in the opening and the surface of the upper dielectric layer 910 planarized to yield the intermediate structure shown in FIG. 9C.

[00110] Although not shown, it will be understood that as in the embodiments described above the charge-trapping region 916 can include a multi-layer charge-trapping region comprising at least one lower or oxygen-rich first nitride layer closer to the tunnel dielectric layer 914, and an upper or oxygen-lean second nitride layer overlying the oxygen-rich first nitride layer. Generally, the oxygen-lean second nitride layer comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in the multi-layer charge-trapping region, while the oxygen-rich first nitride layer comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the oxygen-lean second nitride layer to reduce the number of charge traps therein. In some embodiments, the multi-layer charge-trapping region 916 further includes at least one thin,

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intermediate or anti-tunneling layer comprising a dielectric, such as an oxide, separating the oxygen-lean second nitride layer from the oxygen-rich first nitride layer.

[00111] Next, a second or channel region opening 920 is anisotropically etched through tunneling oxide 914, charge-trapping region 916, and blocking dielectric 918, FIG. 9D. Referring to FIG. 9E, a semiconducting material 922 is deposited in the channel region opening to form a vertical channel region 924 therein. The vertical channel region 924 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or, as shown in FIG. 9E, can include a separate, layer semiconducting material 922 surrounding a cylinder of dielectric filler material 926.

[00112] Referring to FIG. 9F, the surface of the upper dielectric layer 910 is planarized and a layer of semiconducting material 928 including a second, doped diffusion region 930, such as a source region or a drain region, formed therein deposited over the upper dielectric layer to form the device shown.

[00113] Referring to FIG. 10A, in a gate last scheme a dielectric layer 1002, such as an oxide, is formed over a sacrificial layer 1004 on a surface on a substrate 1006, an opening etched through the dielectric and sacrificial layers and a vertical channel region 1008 formed therein. As with embodiments described above, the vertical channel region 1008 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material 1010, such as polycrystalline or monocrystalline silicon, or can include a separate, layer semiconducting material surrounding a cylinder of dielectric filler material (not shown). The dielectric layer 1002 can comprise any suitable dielectric material, such as a silicon oxide, capable of electrically isolating the subsequently formed

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high work function gate electrode of the memory transistor 800 from an overlying electrically active layer or another memory transistor.

[00114] Referring to Figure 10B, a second opening 1012 is etched through the etched through the dielectric and sacrificial layers 1002, 1004, to the substrate 1006, and the sacrificial layer 1004 at least partially etched or removed. The sacrificial layer 1004 can comprise any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 1002, substrate 1006 and vertical channel region 1008. In one embodiment the sacrificial layer 1004 comprises an oxide that can be removed by Buffered Oxide Etch (BOE etch).

[00115] Referring to Figure 10C and 10D, a tunnel dielectric layer 1014, a multi-layer charge-trapping region 1016A-C, and a blocking dielectric layer 1018 are sequentially deposited in the opening, and the surface of the dielectric layer 1002 planarized to yield the intermediate structure shown in Figure 10C. As in the embodiments described above, the multi-layer charge trapping layer 1016A-C is a split multi-layer charge trapping layer including at least an inner oxygen-rich first nitride layer 1016A closest to the tunnel dielectric layer 1014, and an outer, oxygen-lean second nitride layer 1016B. Optionally, the first and second charge trapping layers can be separated by an intermediate oxide or anti-tunneling layer 1016C.

[00116] Next, a high work function gate electrode 1022 is deposited into the second opening 1012 and the surface of the upper dielectric layer 1002 planarized to yield the intermediate structure illustrated in Figure 10E. As with the embodiments described above, the high work function gate electrode 1022 includes a doped polysilicon layer having a dopant concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2} so that the minimum

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energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. The polysilicon layer of the high work function gate electrode 1022 is grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, to the CVD process. Finally, an opening 1024 is etched through the gate layer 1022 to form control gates of separate memory devices 1026A and 1026B.

[00117] The foregoing description of specific embodiments and examples of the invention have been presented for the purpose of illustration and description, and although the invention has been described and illustrated by certain of the preceding examples, it is not to be construed as being limited thereby. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications, improvements and variations within the scope of the invention are possible in light of the above teaching. It is intended that the scope of the invention encompass the generic area as herein disclosed, and by the claims appended hereto and their equivalents. The scope of the present invention is defined by the claims, which includes known equivalents and unforeseeable equivalents at the time of filing of this application.

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IN THE CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a memory transistor including:

a channel region electrically connecting a source region and a drain region formed in a substrate, the channel region comprising polysilicon;

an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer; and

a high work function gate electrode formed over a surface of the ONNO stack.

2. The semiconductor device of claim 1, wherein the channel comprises a silicon nanowire.

3. The semiconductor device of claim 1, wherein the channel region comprises recrystallized polysilicon.

4. The semiconductor device of claim 3, the high work function gate electrode comprises a P+ doped polysilicon layer.

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5. The semiconductor device of claim 4, wherein the ONNO stack further includes a blocking dielectric layer disposed above the multi-layer charge-trapping region, and wherein the blocking dielectric layer comprises a dielectric comprises a high K High Temperature Oxide (HTO).

6. The semiconductor device of claim 1, further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode.

7. The semiconductor device of claim 6, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a N+ doped polysilicon layer to form an P-type (PMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a N-type (NMOS) logic transistor.

8. The semiconductor device of claim 6, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a P+ doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (NMOS) logic transistor.

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9. The semiconductor device of claim 6, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor are formed from a single, patterned doped polysilicon layer.

10. The semiconductor device of claim 1, wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer.

11. A semiconductor device comprising:

a memory transistor including:

a channel region electrically connecting a source region and a drain region formed in a substrate, the channel region comprising polysilicon;

an oxide-nitride-nitride-oxide (ONONO) stack disposed above the channel region, the ONONO stack comprising:

a tunnel dielectric layer disposed above the channel region;

a multi-layer charge-trapping region including an oxygen-rich first nitride layer disposed above the tunnel dielectric layer, an oxygen-lean second nitride layer disposed above the first nitride layer, and an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer; and

a blocking dielectric layer disposed above the multi-layer charge-trapping region; and

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a high work function gate electrode disposed above a surface of the ONONO stack.

12. The semiconductor device of claim 11, wherein the channel region comprises recrystallized polysilicon.

13. The semiconductor device of claim 12, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.

14. The semiconductor device of claim 13, wherein the blocking dielectric layer comprises a dielectric comprises a high K High Temperature Oxide (HTO).

15. The semiconductor device of claim 11, wherein the channel comprises a silicon nanowire.

16. The semiconductor device of claim 11, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.

17. The semiconductor device of claim 11 further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode.

18. A semiconductor device comprising:

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a memory transistor including:

a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region;

an oxide-nitride-nitride-oxide (ONNO) stack disposed about the vertical channel, the ONNO stack comprising:

a tunnel dielectric layer abutting the vertical channel;

a multi-layer charge-trapping region including a first nitride layer comprising an oxygen-rich nitride abutting the tunnel dielectric layer, and a second nitride layer comprising a silicon-rich, oxygen-lean nitride overlying the first nitride layer; and

a blocking dielectric layer overlying the multi-layer charge-trapping region; and

a high work function gate electrode disposed about the ONONO stack, abutting the blocking dielectric layer.

19. The semiconductor device of claim 18, further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode.

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20. The semiconductor device of claim 18, wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer.

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ABSTRACT

A semiconductor devices including non-volatile memories and methods of fabricating the same to improve performance thereof are provided. Generally, the device includes a memory transistor comprising a polysilicon channel region electrically connecting a source region and a drain region formed in a substrate, an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, and a high work function gate electrode formed over a surface of the ONNO stack. In one embodiment the ONNO stack includes a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer. Other embodiments are also disclosed.

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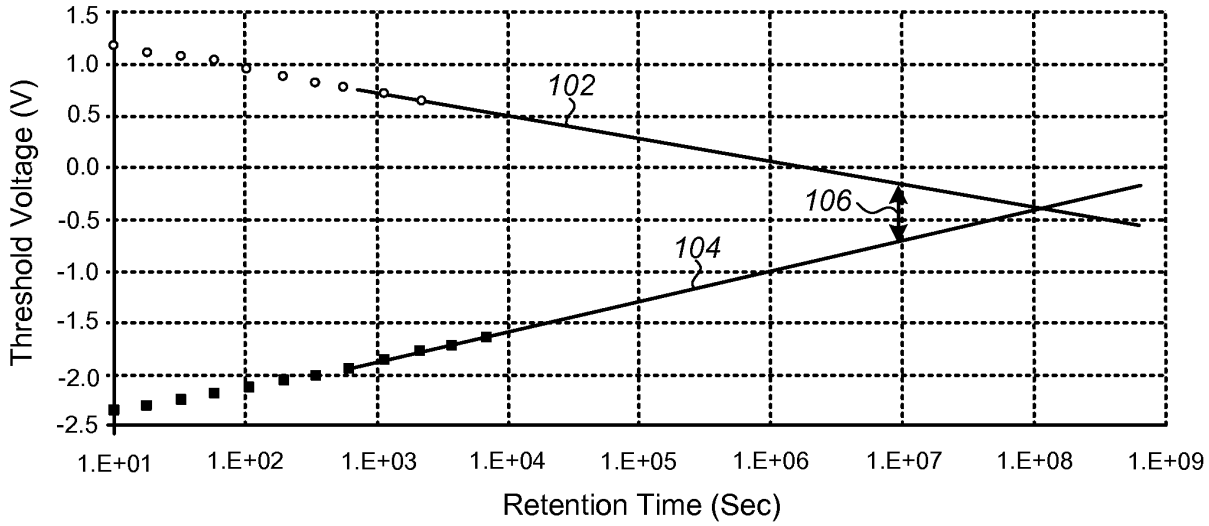

1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
Threshold Voltage (V)
102
106
104
1.E+01
1.E+02
1.E+03
1.E+04
1.E+05
1.E+06
1.E+07
1.E+08
1.E+09
Retention Time (Sec)

FIG. 1A

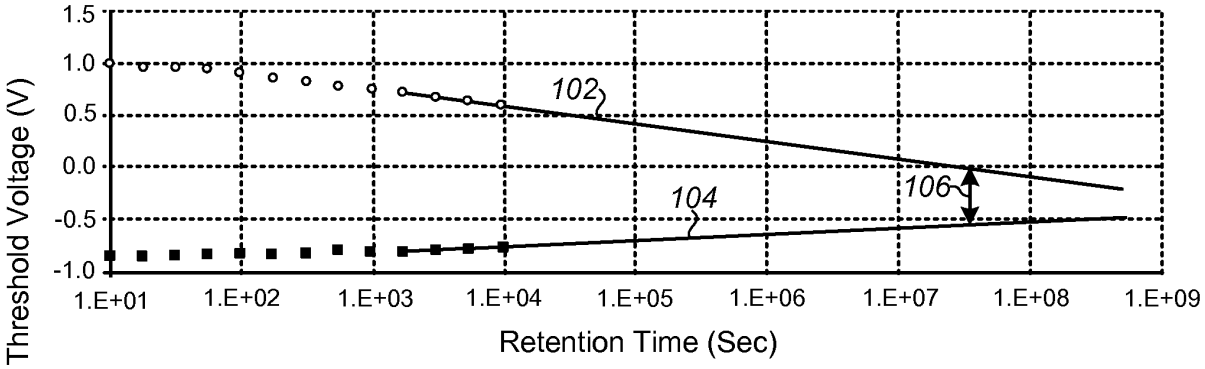

1.5
1.0
0.5
0.0
-0.5
-1.0
Threshold Voltage (V)
102
104
106
1.E+01
1.E+02
1.E+03
1.E+04
1.E+05
1.E+06
1.E+07
1.E+08
1.E+09
Retention Time (Sec)

FIG. 1B

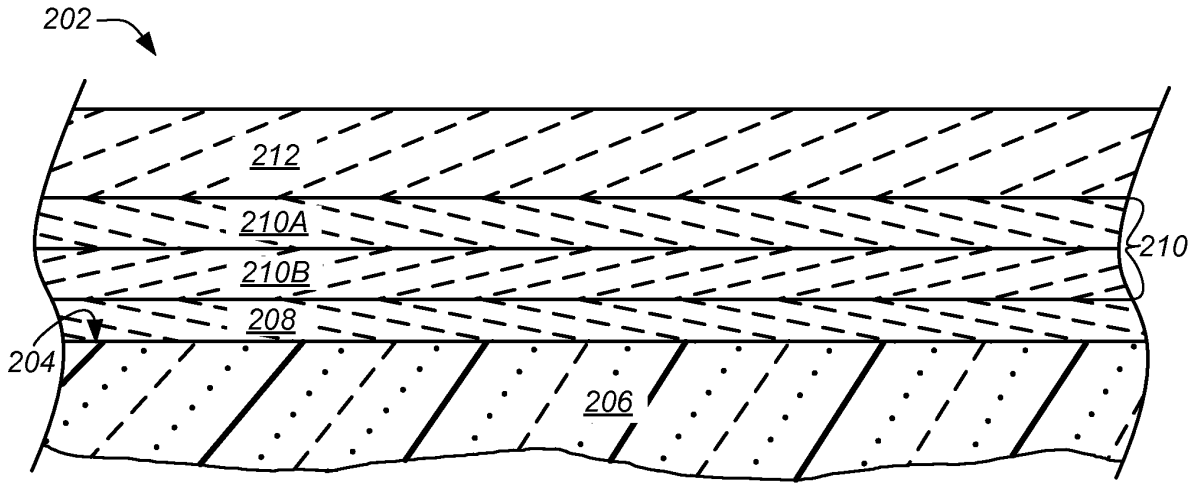

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FIG. 2A

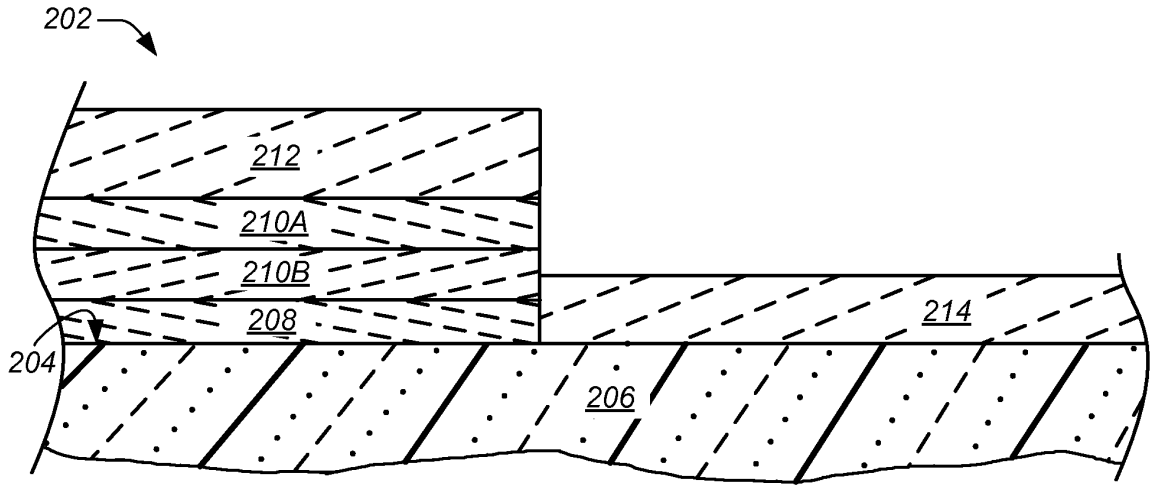

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FIG. 2B

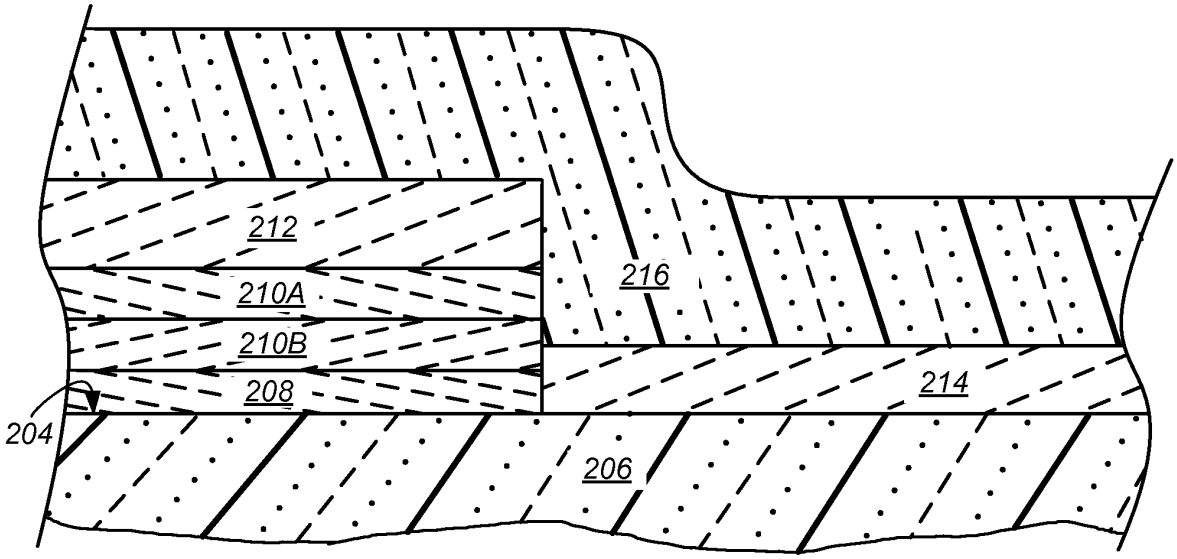

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FIG. 2C

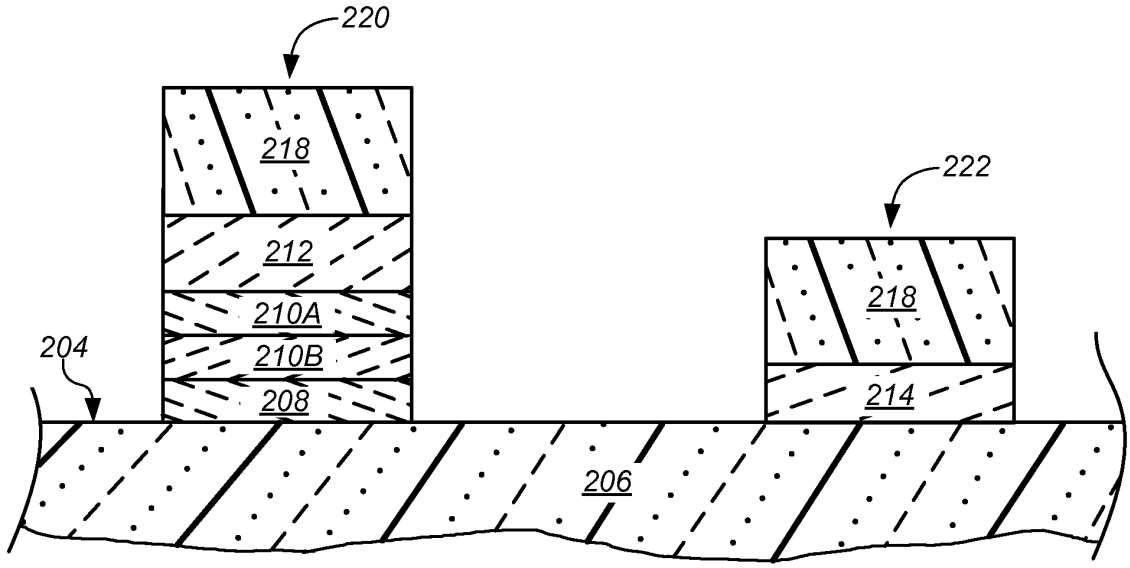

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FIG. 2D

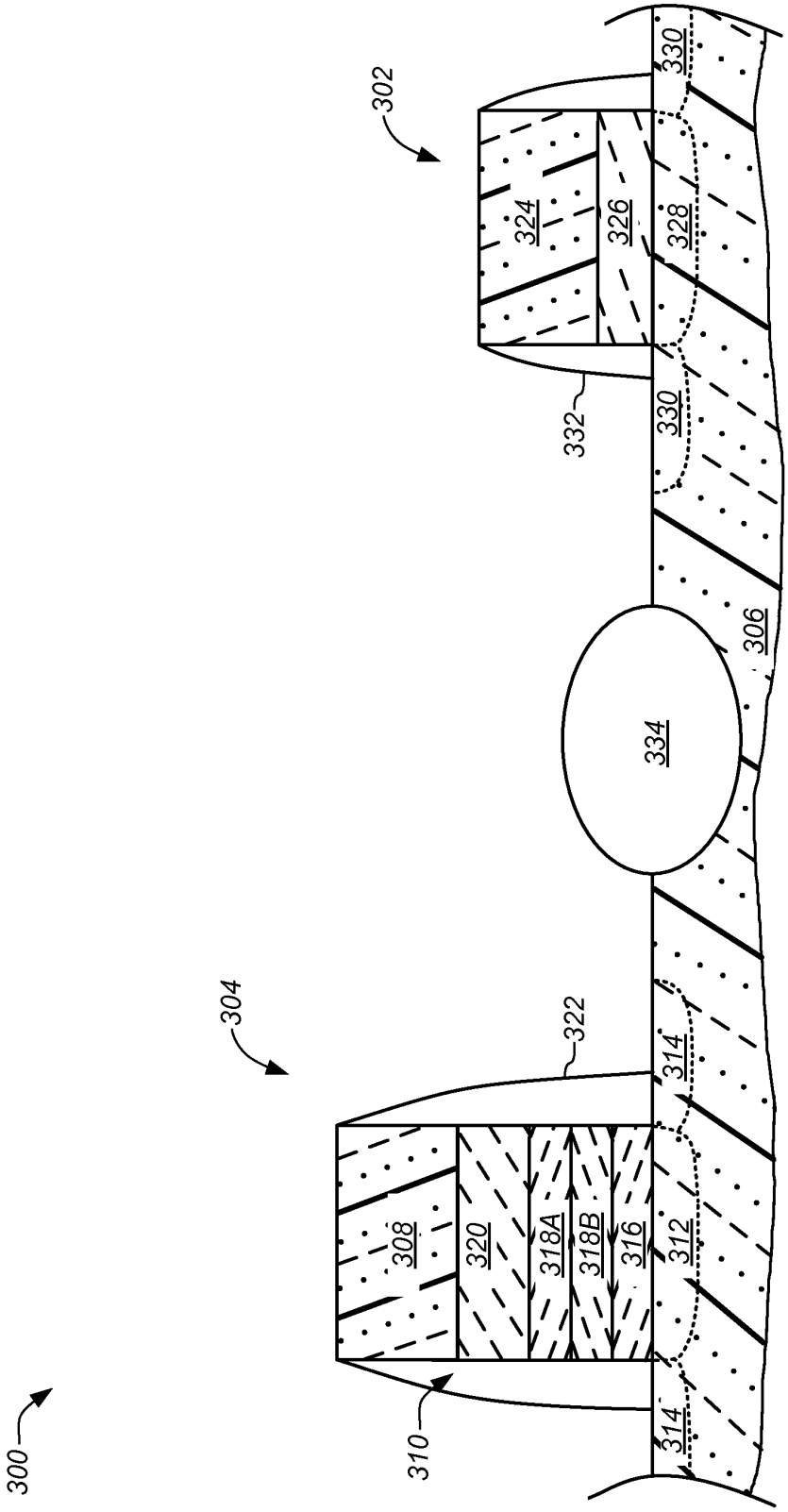

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FIG. 3

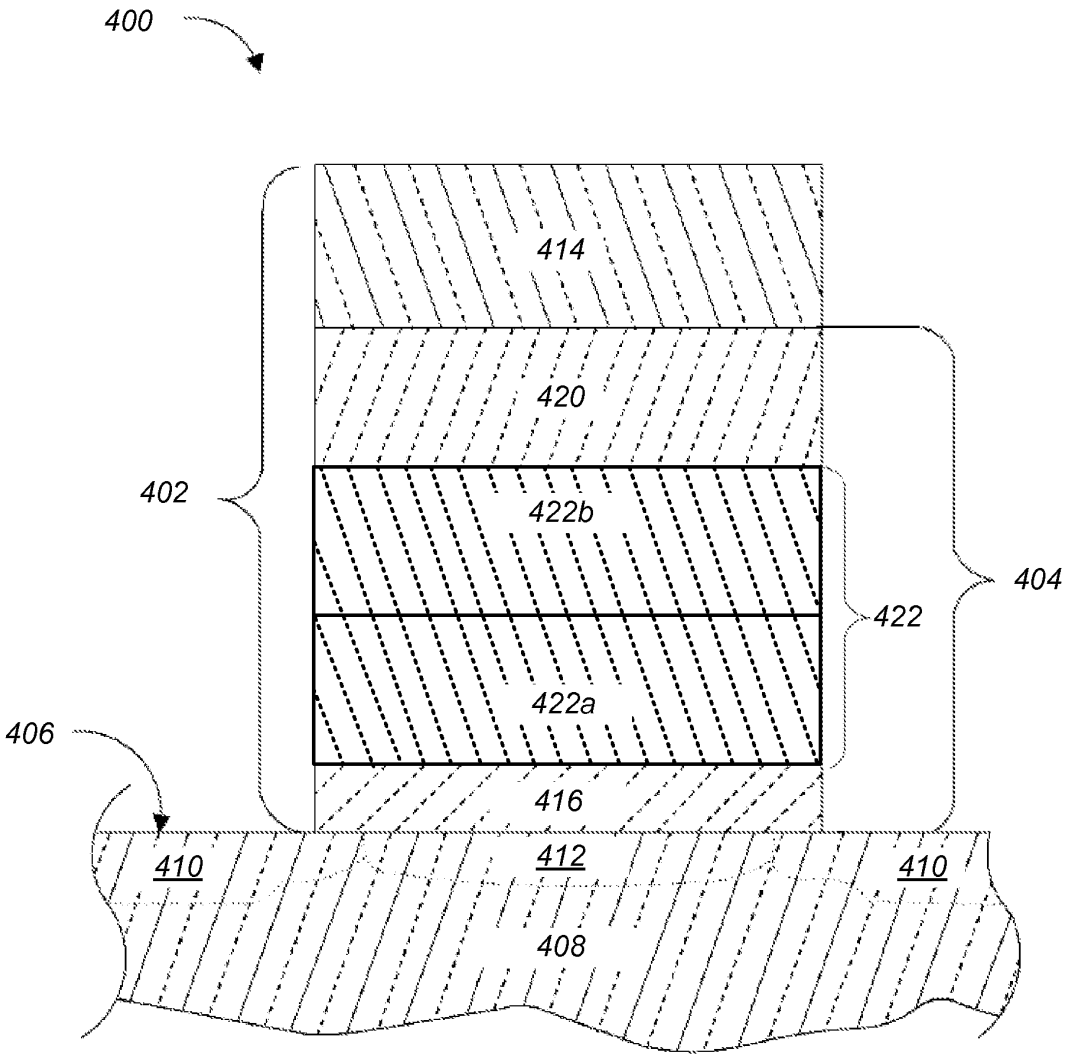


FIG. 4A

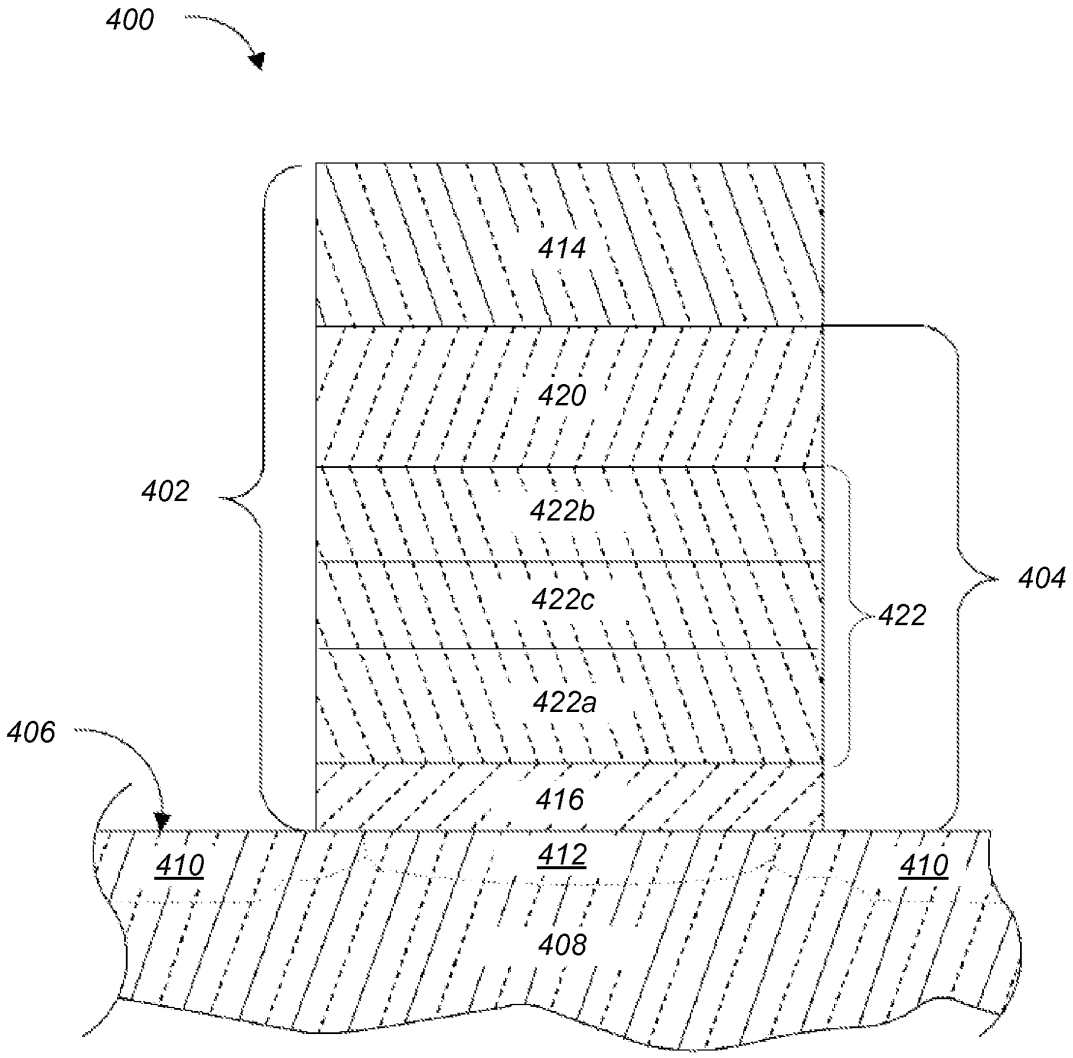


FIG. 4B

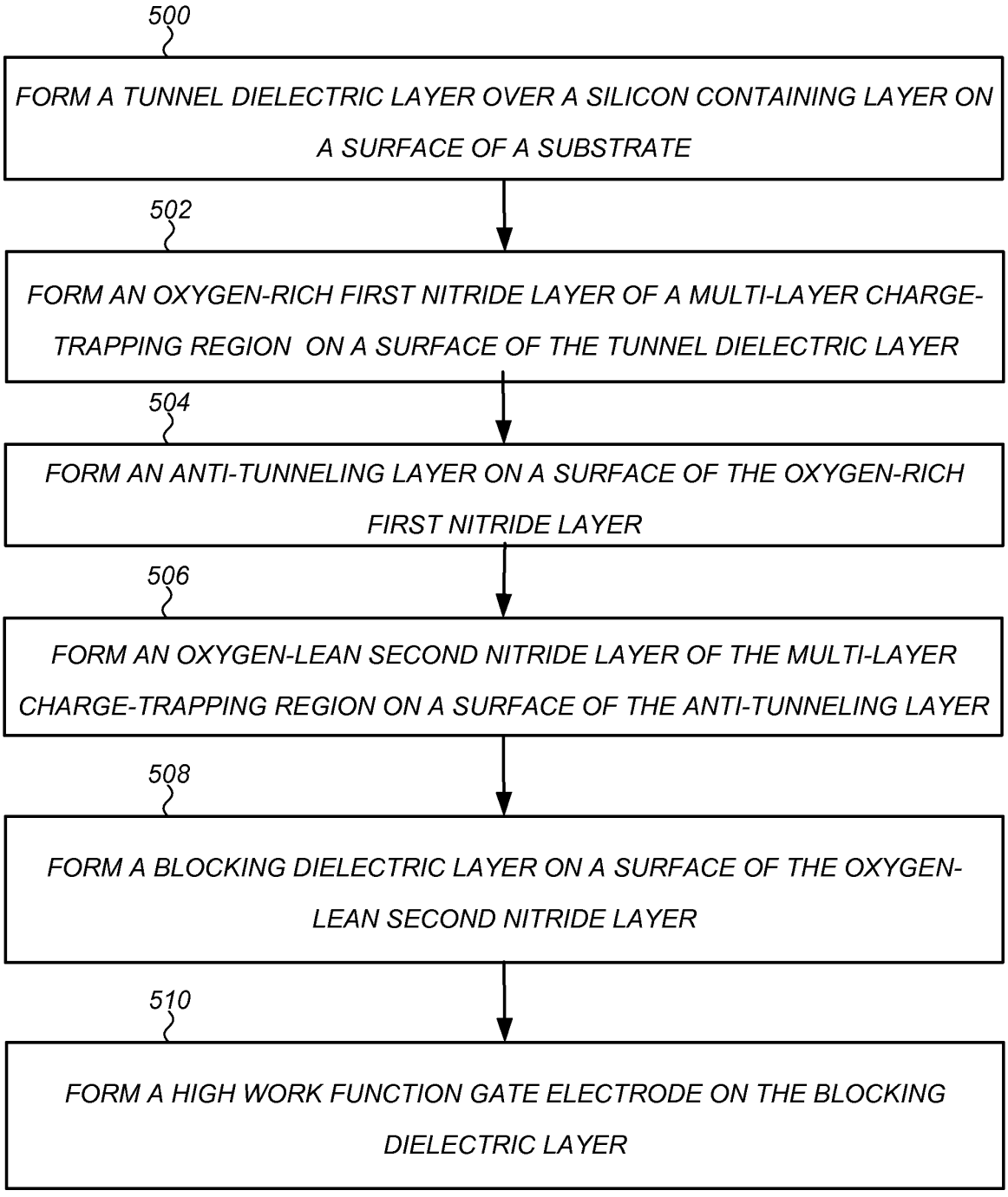

500
FORM A TUNNEL DIELECTRIC LAYER OVER A SILICON CONTAINING LAYER ON A SURFACE OF A SUBSTRATE
502
FORM AN OXYGEN-RICH FIRST NITRIDE LAYER OF A MULTI-LAYER CHARGE-TRAPPING REGION ON A SURFACE OF THE TUNNEL DIELECTRIC LAYER
504
FORM AN ANTI-TUNNELING LAYER ON A SURFACE OF THE OXYGEN-RICH FIRST NITRIDE LAYER
506
FORM AN OXYGEN-LEAN SECOND NITRIDE LAYER OF THE MULTI-LAYER CHARGE-TRAPPING REGION ON A SURFACE OF THE ANTI-TUNNELING LAYER
508
FORM A BLOCKING DIELECTRIC LAYER ON A SURFACE OF THE OXYGEN-LEAN SECOND NITRIDE LAYER
510
FORM A HIGH WORK FUNCTION GATE ELECTRODE ON THE BLOCKING DIELECTRIC LAYER

FIG. 5

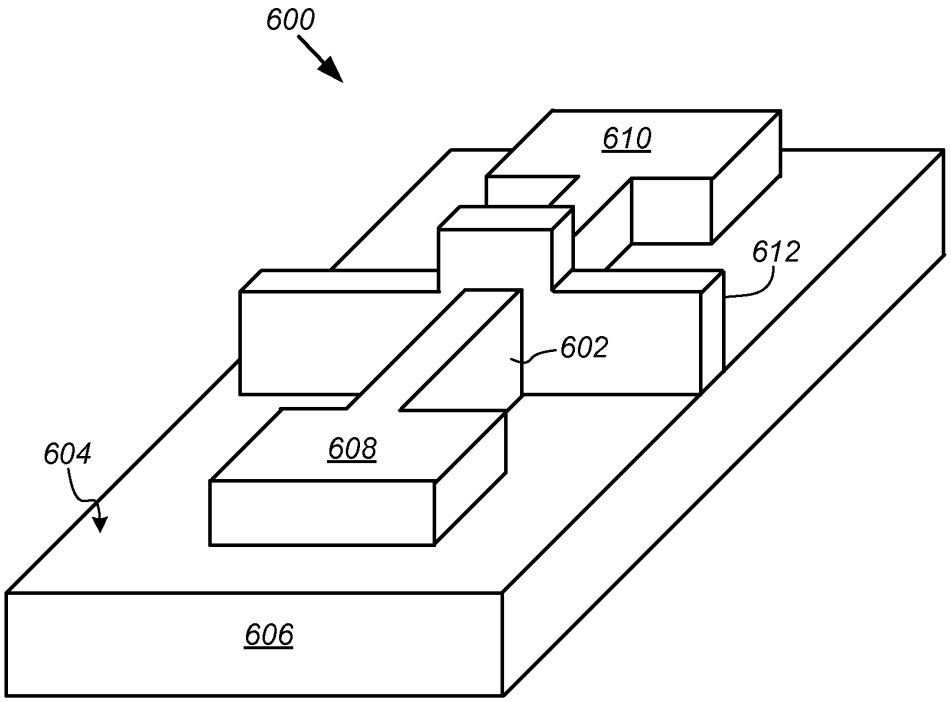


FIG. 6A

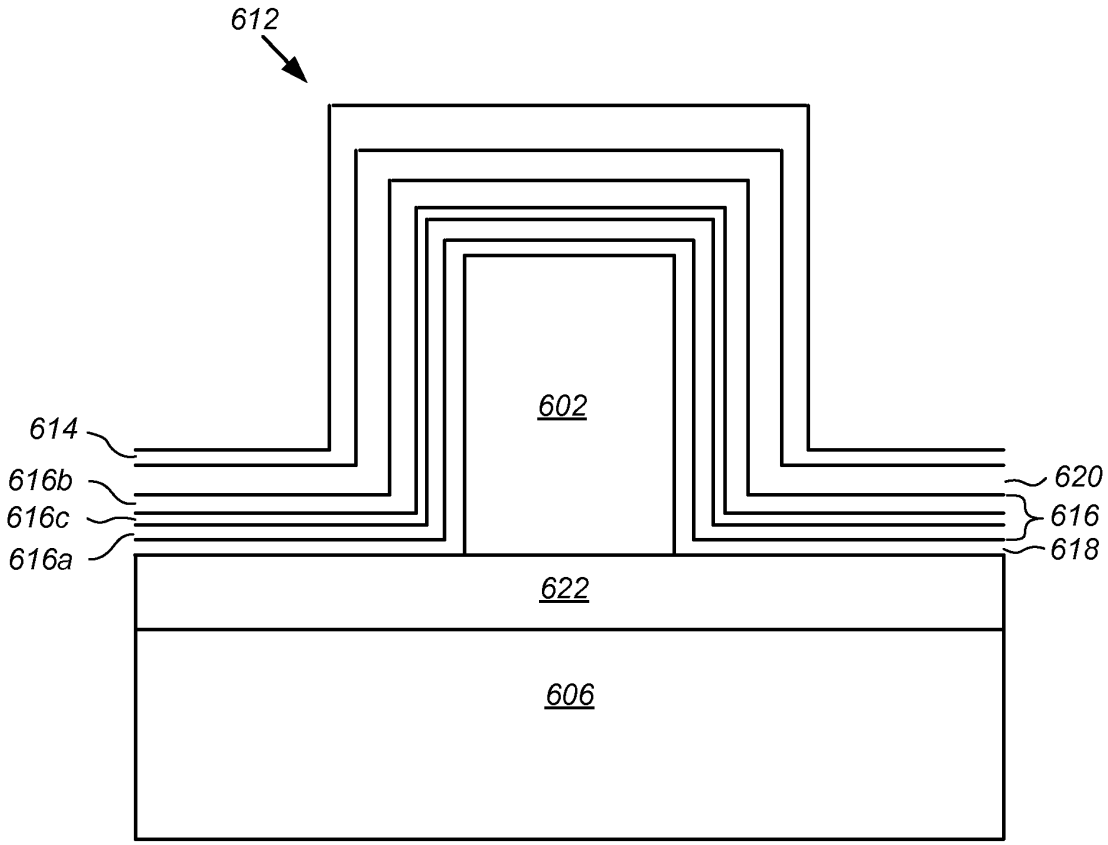


FIG. 6B

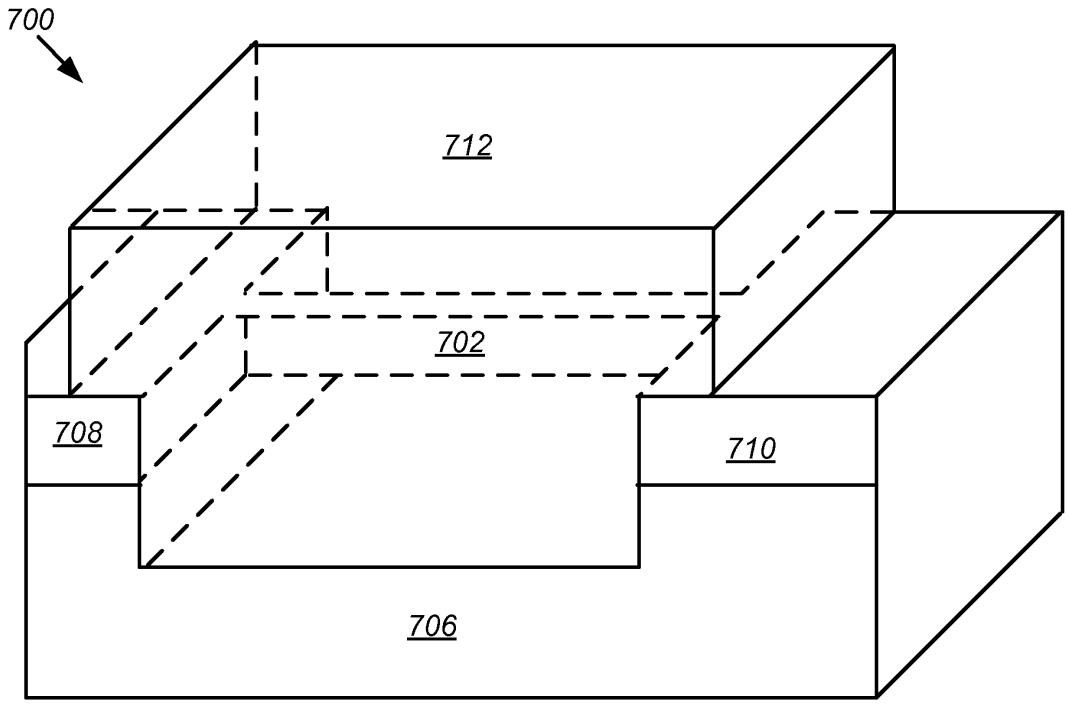


FIG. 7A

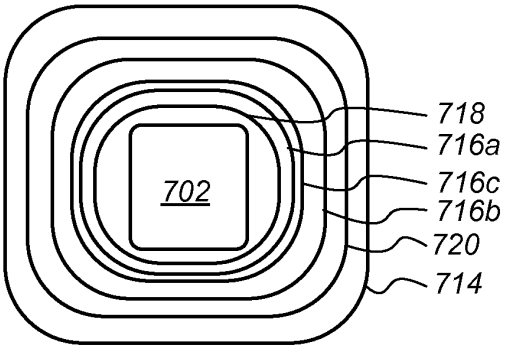


FIG. 7B

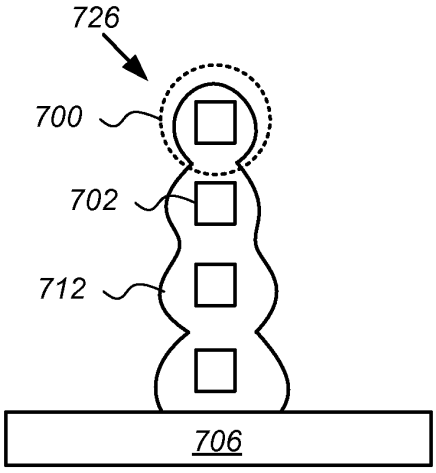


FIG. 7C

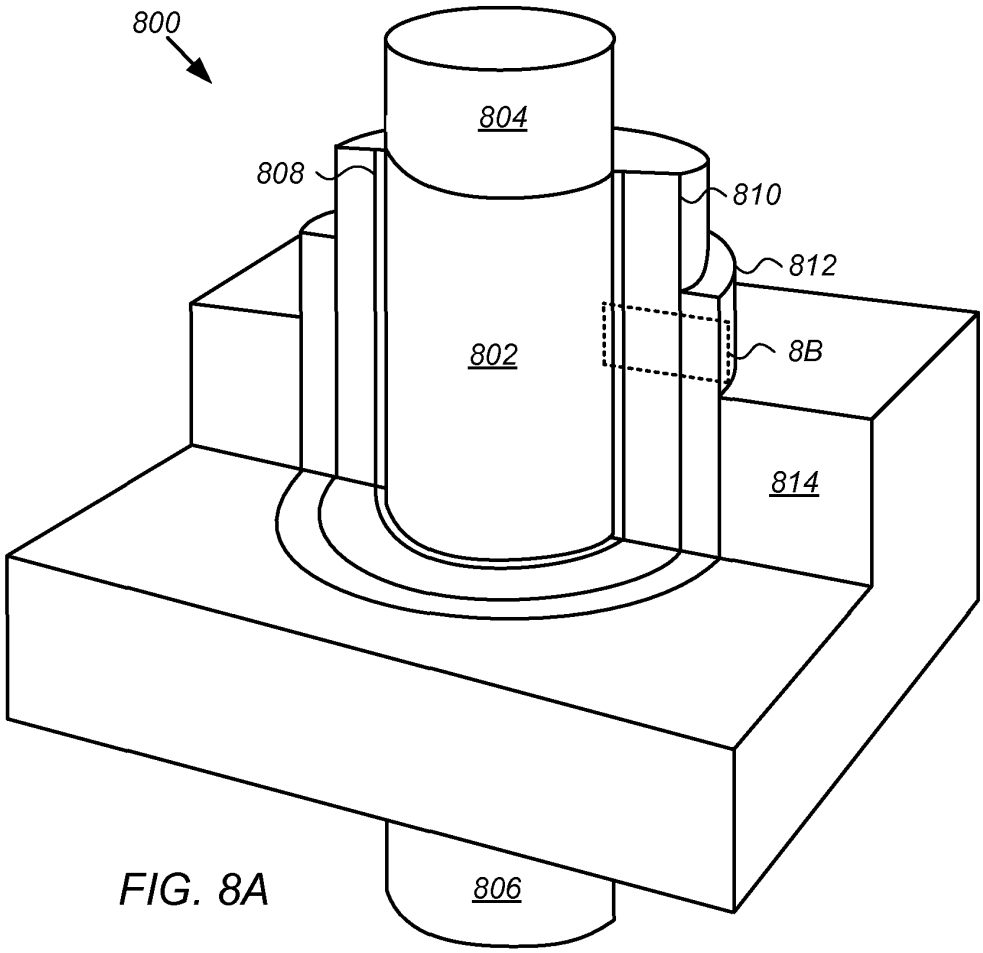


FIG. 8A

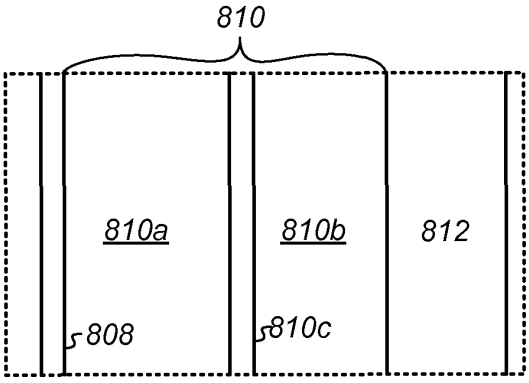


FIG. 8B

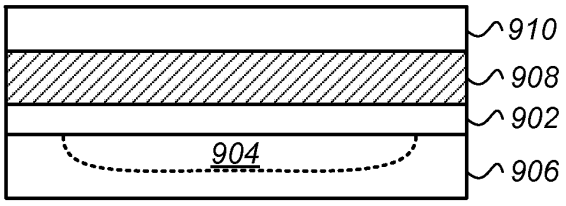


FIG. 9A

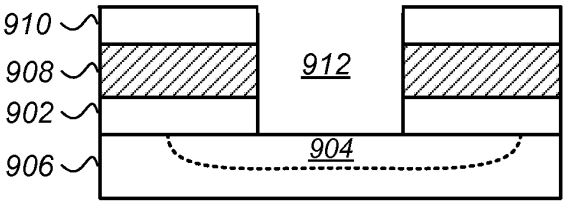


FIG. 9B

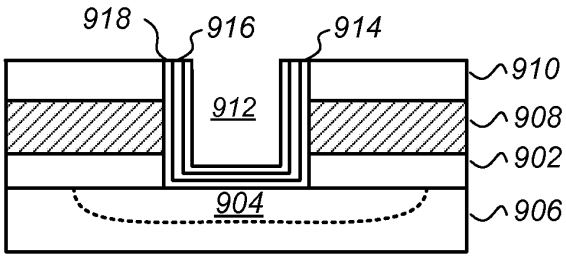


FIG. 9C

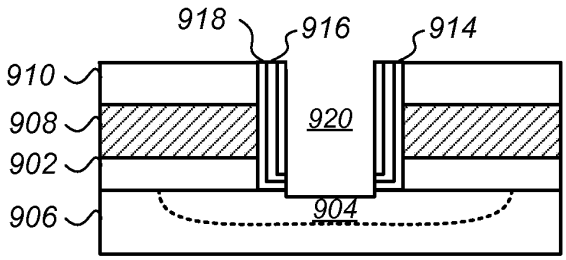


FIG. 9D

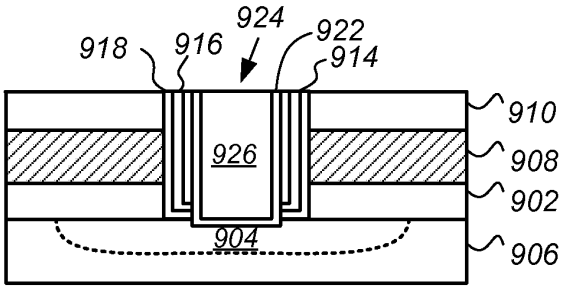


FIG. 9E

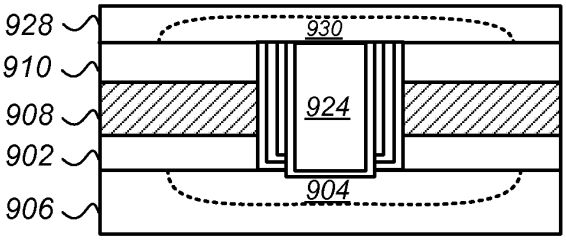


FIG. 9F

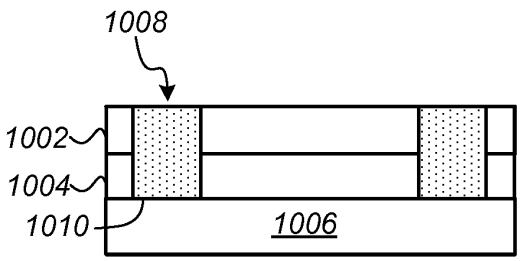


FIG. 10A

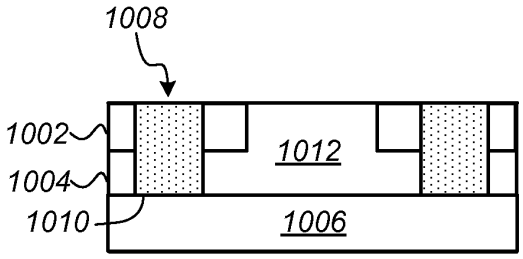


FIG. 10B

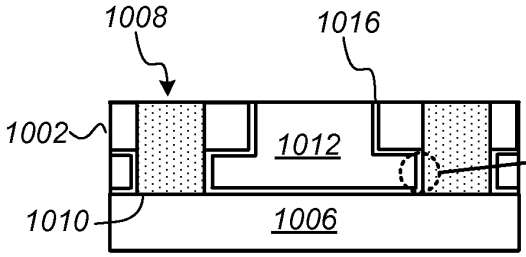


FIG. 10C

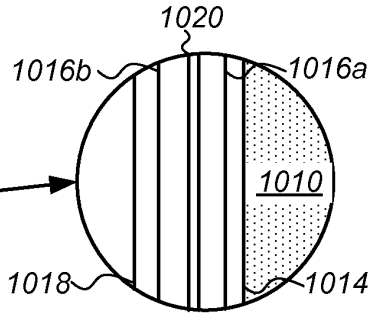


FIG. 10D

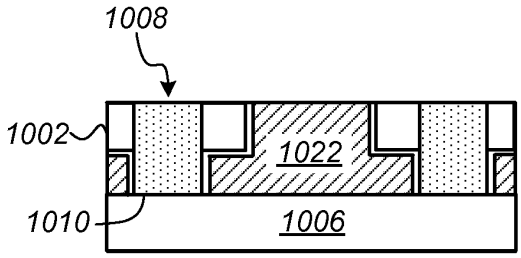


FIG. 10E

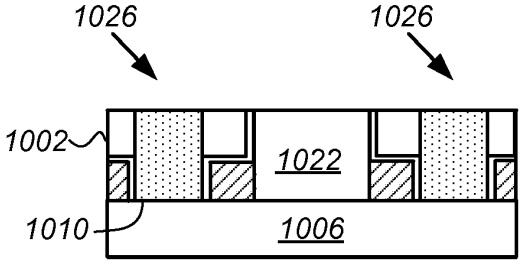


FIG. 10F

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Country	US

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Legal Name

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State/Province	
Postal Code	03900
Country	IL

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Krishnaswamy		Ramkumar	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Residence Information (Select One) (•) US Residency ( ) Non US Residency Active US Military Service

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Address 2			
City	San Jose	**State/Province**	CA
Postal Code	95129	**Country**	US

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Application Information:

Title of the Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
Attorney Docket Number	PM07027D1CIP1C3	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	60909		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending			Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
	Continuation of	14811346	2015-07-28	

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14811346	Continuation of	14159315	2014-01-20	9093318	2015-07-28

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14159315	Continuation of	13539466	2012-07-01	8633537	2014-01-21

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13539466	Continuation in part of	13288919	2011-11-03	8859374	2014-10-14

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13288919	Division of	12152518	2008-05-13	8063434	2011-11-22
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12152518	Claims benefit of provis	60940160	2007-05-25		

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Cypress Semiconductor Corporation		
Mailing Address Information For Applicant:			
Address 1	198 Champion Ct.		
Address 2			
City	San Jose	**State/Province**	CA
Country	US	Postal Code	95134
Phone Number	408-943-2600	Fax Number	
Email Address	patents@cypress.com, pbjtmp2@cypress.com, kalk@cypress.com		

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature				Date (YYYY-MM-DD)	2016-10-26
First Name	Kin Hung	Last Name	Lai	Registration Number	69251

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	27333044
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Shellie Woodman
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	26-OCT-2016
Filing Date:	
Time Stamp:	17:44:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Specification	PM07027D1CIP1C3_Spec.pdf	263254 77f8032100311568029 7d7a57cd5c6a86a2cd89f	no	47

Warnings:

Information:					
2	Drawings-only black and white line drawings	PM07027D1CIP1C3_Drawings.pdf	850306 8393a7ffcb293243de9b1d7f992bf487013d9b3e	no	13
Warnings:					
Information:					
3	Application Data Sheet	PM07027D1CIP1C3_ADS_10262016.pdf	1874772 0b8aa9351f6da63be3e5507f59bc0119c9a58558	no	9
Warnings:					
Information:					
		Total Files Size (in bytes):	2988332		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3

CONFIRMATION NO. 6223

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

FORMALITIES LETTER

OC000000087009451

Date Mailed: 11/08/2016

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- The inventor's oath or declaration or an application data sheet (ADS) naming each inventor has not been submitted. An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor, or a properly executed ADS in compliance with 37 CFR 1.76 identifying each inventor by his or her legal name, mailing address, and residence (if an inventor lives at a location which is different from where the inventor customarily receives mail) is required. If an ADS as set forth above is provided, the filing of the inventor's oath or declaration may be postponed until the application is otherwise in condition for allowance. See 37 CFR 1.53(f).
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

Sandisk Technologies, Inc. - Ex. 1002, Page 000073

- $ **280** basic filing fee.
- $ **140** surcharge.
- $ **600** search fee.
- $ **720** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1740** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- The ADS received on 10/26/2016 was not properly signed. Therefore, the Office will treat it only as a transmittal letter. See 37 CFR 1.76(e). Inventorship has not been set by this document and any foreign priority or domestic benefit claims contained therein are ineffective. See 37 CFR 1.55 or 37 CFR 1.78.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/cvorachack/

Sandisk Technologies, Inc. - Ex. 1002, Page 000074

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/335,180	10/26/2016	2827	0.00	PM07027D1CIP1C3	20	3

CONFIRMATION NO. 6223

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

FILING RECEIPT

OC000000087009450

Date Mailed: 11/08/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Igor Polishchuk, Fremont, CA;
Sagy Charel Levy, Zichron Yaakov, ISRAEL;
Krishnaswamy Ramkumar, San Jose, CA;

Applicant(s)

Igor Polishchuk, Fremont, CA;
Sagy Charel Levy, Zichron Yaakov, ISRAEL;
Krishnaswamy Ramkumar, San Jose, CA;

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Sandisk Technologies, Inc. - Ex. 1002, Page 000075

If Required, Foreign Filing License Granted: 11/03/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/335,180**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

Sandisk Technologies, Inc. - Ex. 1002, Page 000076

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/335,180

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3

CONFIRMATION NO. 6223

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

OC000000087009454

Date Mailed: 11/08/2016

Improper Submission of Authorization to Permit Access to Application by Participating Offices under 37 CFR 1.14(h)(1) (Priority Document Exchange)

The Authorization to Permit Access to Application-As-Filed by Participating Offices under 37 CFR 1.14(h)(1) (authorization to permit access to application via priority document exchange) submitted on 10/26/2016 in the above-identified application is not accepted because:

- It was not signed. If applicant still wishes to provide authorization to permit access under 37 CFR 1.14(h)(1), applicant must submit a properly signed authorization (e.g., PTO/SB/39).

Any authorization should be submitted prior to filing a subsequent foreign application with a participating intellectual property office in which priority is claimed to the above-identified U.S. application to ensure that it is likely that the participating foreign intellectual property office will be successful in its attempt to retrieve a copy of the U.S. priority application from the Office.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/cvorachack/

Sandisk Technologies, Inc. - Ex. 1002, Page 000079

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3

CONFIRMATION NO. 6223

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

OC000000087009457

Date Mailed: 11/08/2016

Improper Submission of Authorization to Permit Access to Search Results under 37 CFR 1.14(h)(2)

The Authorization to Permit Access to the Search Results from the instant application under 37 CFR 1.14(h)(2) (authorization to permit access to search results) submitted on 10/26/2016 in the above-identified application is not accepted because:

- It was not signed. If applicant still wishes to provide authorization to permit access to the search results under 37 CFR 1.14(h)(2), applicant must submit a properly signed authorization (e.g., PTO/SB/69).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/cvorachack/

Sandisk Technologies, Inc. - Ex. 1002, Page 000080

To: patents@cypress.com,pbj@cypress.com,pbjtmp2@cypress.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 60909

Nov 08, 2016 03:37:57 AM

Dear PAIR Customer:

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 60909 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
15335180	NTC.MISS.PRT	11/08/2016	PM07027D1CIP1C3
	APP.FILE.REC	11/08/2016	PM07027D1CIP1C3
	PD.AUTH.NTC	11/08/2016	PM07027D1CIP1C3
	SREXR.NTC	11/08/2016	PM07027D1CIP1C3

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

Doc Code: PD.TO.AUTH
Document Description: Auth or Resc of Auth to Access Appl by DAS/PDX Office

PTO/SB/39 (11-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

AUTHORIZATION OR RESCISSION OF AUTHORIZATION TO PERMIT ACCESS TO APPLICATION-AS-FILED BY PARTICIPATING OFFICES

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Application Number (if known):	Filing Date:
15/335,180	10-26-2016
First Named Inventor:	Attorney Docket Number:
Igor Polishchuk	PM07027D1CIP1C3

Title (Required)
METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE

Check either box 1 or 2 below, but **not** both:

1. ☒ By checking this box, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization(WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

2. ☐ By checking this box, the undersigned hereby **rescinds the previous authority granted to the USPTO** to provide the EPO, JPO, KIPO, SIPO, WIPO or any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement access to the documents and information identified in paragraph 1 above.

This rescission of the previous authorization will not be effective unless and until an appropriate USPTO official recognizes and acts on the rescission.

However, once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

NOTE: This form must be signed by an authorized party in accordance with 37 CFR 1.14(c). Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below.*

Signature /Christopher Jordan/	Date 11/09/2016
Name (Print/Typed) Christopher Jordan	Practitioner Registration Number (If applicable) 65809
Name of Assignee (if applicable)	Title (if applicable)

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.14(h). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc Code: SREXR141
Document Description: Auth or Resc of Auth to Access Search Results

PTO/SB/69 (11-15)

AUTHORIZATION OR RESCISSION OF AUTHORIZATION TO PERMIT ACCESS TO SEARCH RESULTS BY THE EUROPEAN PATENT OFFICE (EPO)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Application Number (if known):	Filing Date:
15/335,180	10-26-2016
First Named Inventor:	Attorney Docket Number:
Igor Polishchuk	PM07027D1CIP1C3

Title (Required)
METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE

Check either box 1 or 2 below, but **not** both:

1. ☒ By checking this box, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. ☐ By checking this box, the undersigned hereby **rescinds the previous authority granted to the USPTO** to transmit to the EPO any search results from the instant patent application.

This rescission of the previous authorization will not be effective unless and until an appropriate USPTO official recognizes and acts on the rescission.

However, once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

NOTE: This form must be signed by an authorized party in accordance with 37 CFR 1.14(c). Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below.*

Signature /Christopher Jordan/	Date 11/09/2016
Name (Print/Typed) Christopher Jordan	Practitioner Registration Number (If applicable) 65809
Name of Assignee (if applicable)	Title (if applicable)

☐ *Total of _____ forms are submitted.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	27467242
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	09-NOV-2016
Filing Date:	26-OCT-2016
Time Stamp:	20:02:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	PM07027D1CIP1C3_SupplementalADS_AIA14_11092016.pdf	61514 7ace48ca37a55e24ea20c3fc8fff7709bc7d854c	no	9

Warnings:

Information:					
This is not an USPTO supplied ADS fillable form					
2	Auth or Resc of Auth to Access Appl by DAS/PDX Office	PM07027D1CIP1C3_sb0039_11092016_signed.pdf	101623 771baa327ecdcf6b9e5617718fdf3a1b24ceb1a3	no	2
Warnings:					
Information:					
3	Auth or Resc of Auth to Access Search Results	PM07027D1CIP1C3_sb0069_11092016_signed.pdf	103900 6c6555d0b377effb51febb5407f327481edc8290	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	267037	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	15/335,180
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Igor		Polishchuk	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Fremont	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	43355 Paseo Padre Pkwy		
Address 2			
City	Fremont	State/Province	CA
Postal Code	94539	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sagy	Charel	Levy	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Zichron Yaakov	Country of Residence	IL

Mailing Address of Inventor:

Address 1	44 Yigal Alon Street		
Address 2			
City	Zichron Yaakov	State/Province	
Postal Code	03900	Country	IL

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Krishnaswamy		Ramkumar	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Jose	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	1193 Lynbrook Way		
Address 2			
City	San Jose	State/Province	CA
Postal Code	95129	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	60909		
Email Address	patents@cypress.com	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
Attorney Docket Number	PM07027D1CIP1C3	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	60909		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15335180	Continuation of	14811346	2015-07-28

Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14811346	Continuation of	14159315	2014-01-20	9093318	2015-07-28

Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14159315	Continuation of	13539466	2012-07-01	8633537	2014-01-21

Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13539466	Continuation in part of	13288919	2011-11-03	8859374	2014-10-14

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13288919	Division of	12152518	2008-05-13	8063434	2011-11-22

Prior Application Status	Expired		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12152518	Claims benefit of provisional	60940160	2007-05-25

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◯ Assignee	◯ Legal Representative under 35 U.S.C. 117	◯ Joint Inventor
◯ Person to whom the inventor is obligated to assign.	◯ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Cypress Semiconductor Corporation		
Mailing Address Information For Applicant:			
Address 1	198 Champion Court		
Address 2			
City	San Jose	**State/Province**	CA
Country	US	Postal Code	95134
Phone Number	408-943-2600	Fax Number	408-545-6911
Email Address	patents@cypress.com		

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Christopher Jordan/			Date (YYYY-MM-DD)	2016-11-09
First Name	Christopher	Last Name	Jordan	Registration Number	65809

Additional Signature may be generated within this form by selecting the Add button.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/335,180

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3

CONFIRMATION NO. 6223

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

FORMALITIES LETTER

OC000000087199161

Date Mailed: 11/16/2016

NOTICE OF INCOMPLETE REPLY (NONPROVISIONAL)

Filing Date Granted

The U.S. Patent and Trademark Office has received your reply on 11/09/2016 to the Notice to File Missing Parts (Notice) mailed 11/08/2016 and it has been entered into the nonprovisional application. The reply, however, does not include the following items required in the Notice. A complete reply must be timely filed to prevent ABANDONMENT of the above-identified application. Replies should be mailed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

Applicant is given **TWO MONTHS** from the date of the Notice to File Missing Parts (Notice) mailed 11/08/2016 within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee was not received.
- The application examination fee was not received.
- Surcharge as set forth in 37 CFR 1.16(f) was not received.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of the Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **280** basic filing fee.
- $ **140** surcharge.
- $ **600** search fee.
- $ **720** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1740** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Sandisk Technologies, Inc. - Ex. 1002, Page 000098

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Igor Polishchuk
  Sagy Charel Levy
  Krishnaswamy Ramkumar

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ebekele/

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3

CONFIRMATION NO. 6223

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

OC000000087199167

Date Mailed: 11/16/2016

NOTICE OF ACCEPTANCE OF AUTHORIZATION TO PERMIT ACCESS TO SEARCH RESULTS

This is in response to the applicant's authorization to permit access to the search results from the instant application under 37 CFR 1.14(h)(2) submitted on 11/09/2016.

The authorization to permit access to the search results under 37 CFR 1.14(h)(2) is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ebekele/

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3

CONFIRMATION NO. 6223

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

OC000000087199164

Date Mailed: 11/16/2016

NOTICE OF ACCEPTANCE OF AUTHORIZATION TO PERMIT ACCESS TO APPLICATION VIA PRIORITY DOCUMENT EXCHANGE

This is in response to the applicant's authorization to permit access to the application-as-filed by participating offices under 37 CFR 1.14(h)(1) submitted on 11/09/2016.

The authorization to permit access to the application under 37 CFR 1.14(h)(1) is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ebekele/

Sandisk Technologies, Inc. - Ex. 1002, Page 000101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3

CONFIRMATION NO. 6223

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

IMPROPER CFR REQUEST

OC000000087199202

Date Mailed: 11/16/2016

RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

Power of Attorney, Claims, Fees, System Limitations, and Miscellaneous

In response to your request for a corrected Filing Receipt, the Office is unable to comply with your request because:

- The ADS submitted on 11/09/2016 attempts to change the applicant but cannot be entered. Any request to change the applicant once the applicant has been specified must include (1) an application data sheet specifying the new applicant in the Applicant Information section, and (2) a statement under 37 CFR 3.73(c) (USPTO Form PTO/AIA/96 or an equivalent) to show chain of title to the new applicant. The application data sheet must contain markings to show the information that is being changed, with underlining for additions and strike-through or brackets for deletions. See 37 CFR 1.76(c)(2).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ebekele/

Sandisk Technologies, Inc. - Ex. 1002, Page 000102

To: patents@cypress.com,pbj@cypress.com,pbjtmp2@cypress.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 60909

Nov 16, 2016 03:46:43 AM

Dear PAIR Customer:

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 60909 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
15335180	NT.INC.REPLY	11/16/2016	PM07027D1CIP1C3
	SREXR.G	11/16/2016	PM07027D1CIP1C3
	PD.AUTH.G	11/16/2016	PM07027D1CIP1C3
	M327	11/16/2016	PM07027D1CIP1C3

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Examiner: Unknown
Polishchuk et al.	Art Group: 2827
Application No.: 15/335,180	Confirmation No.: 6223
Filed: October 26, 2016	
For: METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Please enter these amendments before prosecution on the merits.

Amendments begin on page 2 of this paper.

Remarks begin on page 7 of this paper.

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AMENDMENTS TO THE CLAIMS:

Please amend the claims of the patent application as set forth below wherein new text is indicated with underlining and deleted text is indicated with strikethrough or with [[double-brackets]]:

What is claimed is:

1-20. (Canceled)

21. (New) A memory device, comprising:

a gate structure;

a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and

a tunnel dielectric layer, a multi-layer blocking layer, and a blocking dielectric layer disposed between the gate structure and the channel,

wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.

22. (New) The memory device of claim 21, wherein the channel, first and second diffusion regions are formed at least partially within a semiconductor material structure.

23. (New) The memory device of claim 21, wherein the channel, first and second diffusion regions are disposed above a semiconductor material structure.

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24. (New) The memory device of claim 21, wherein the channel, first and second diffusion regions are suspended above a semiconductor material structure.

25. (New) The memory device of claim 21, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure.

26. (New) The memory device of claim 21, wherein the first dielectric layer is disposed abutting the tunnel dielectric layer and substantially trap free, and wherein the second dielectric layer is disposed abutting the blocking dielectric layer.

27. (New) The memory device of claim 26, wherein the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first and second dielectric layers, and wherein the anti-tunneling layer includes an oxide layer.

28. (New) The memory device of claim 21, wherein the channel includes a silicon nanowire channel.

29. (New) The memory device of claim 21, wherein the gate structure includes a high work function gate electrode.

30. (New) The memory device of claim 28, further comprising:

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a gate-all-around (GAA) structure wherein the silicon nanowire channel is enclosed on all four sides by the gate structure.

31. (New) The memory device of claim 29, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.

32. (New) The memory device of claim 21, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO).

33. (New) A semiconductor device, comprising:

a memory device including,

a gate structure including a first high work function gate electrode,

a channel positioned between and electrically connecting a first diffusion region and a second diffusion region, and

a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel, wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride; and

a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.

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34. (New) The semiconductor device of claim 33, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure.

35. (New) The semiconductor device of claim 33, wherein the MOS logic device is formed at least partially within a semiconductor material structure.

36. (New) The semiconductor device of claim 35, wherein the channel is vertical and oriented substantially orthogonal to the semiconductor material structure.

37. (New) The semiconductor device of claim 34, wherein the first dielectric layer of the multi-layer charge trapping layer is disposed abutting the tunnel dielectric layer and substantially trap free, and wherein the second dielectric layer is disposed abutting the blocking dielectric layer.

38. (New) A semiconductor device, comprising:

a memory device including,

a gate structure including a first high work function gate electrode,

a blocking dielectric layer disposed abutting the gate structure,

a multi-layer charge trapping layer disposed abutting the blocking dielectric layer, wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride,

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a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer, and

a channel disposed abutting the tunnel dielectric layer, wherein the channel is positioned between and electrically connecting a first diffusion region and a second diffusion region; and

a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.

39. (New) The semiconductor device of claim 38, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and wherein the MOS logic device is formed at least partially on the semiconductor material structure.

40. (New) The semiconductor device of claim 38, wherein the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first and second dielectric layers, and wherein the anti-tunneling layer includes an oxide layer.

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REMARKS

Claims 1-20 are cancelled and claims 21-40 are new, fully supported in the specification and drawings, and are respectfully presented for examination. Accordingly, no new matter is added in this amendment.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.P.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the undersigned by telephone at (408) 545-6950. All correspondence should continue to be directed to the address given below.

Respectfully Submitted,

Date: 12/02/2016

/Kin Hung Lai/
Kin Hung LAI
Registration No. 69,251

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Sandisk Technologies, Inc. - Ex. 1002, Page 000110

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Attorney Docket Number	PM07027D1CIP1C1

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 14/159,315

  filed on January 20, 2014

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above identified application.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

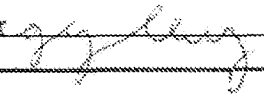
I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Sagy Charel Levy Date: 4/22/2015

Signature: 

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Attorney Docket Number	PM07627D1CIP1C1

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 14/159,315 filed on January 20, 2014

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above identified application.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Igor Polishchuk Date: May 6 2015

Signature: [signature]

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Attorney Docket Number	PM07027D1CIP1C1

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 14/159,315

filed on January 20, 2014

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby state that I have reviewed and understand the contents of the above identified application.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

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WARNING:

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LEGAL NAME OF INVENTOR

Inventor: Krishnaswamy Ramkumar Date: 4/13/2015

Signature: Krramkumar

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	15/335,180
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Igor		Polishchuk	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Fremont	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	43355 Paseo Padre Pkwy		
Address 2			
City	Fremont	State/Province	CA
Postal Code	94539	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sagy	Charel	Levy	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Zichron Yaakov	Country of Residence	IL

Mailing Address of Inventor:

Address 1	44 Yigal Alon Street		
Address 2			
City	Zichron Yaakov	State/Province	
Postal Code	03900	Country	IL

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Krishnaswamy		Ramkumar	

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	San Jose	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	1193 Lynbrook Way		
Address 2			
City	San Jose	State/Province	CA
Postal Code	95129	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	60909		
Email Address	patents@cypress.com	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
Attorney Docket Number	PM07027D1CIP1C3	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	60909		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15335180	Continuation of	14811346	2015-07-28

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14811346	Continuation of	14159315	2014-01-20	9093318	2015-07-28

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14159315	Continuation of	13539466	2012-07-01	8633537	2014-01-21

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13539466	Continuation in part of	13288919	2011-11-03	8859374	2014-10-14

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13288919	Division of	12152518	2008-05-13	8063434	2011-11-22

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12152518	Claims benefit of provisional	60940160	2007-05-25

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◯ Assignee	◯ Legal Representative under 35 U.S.C. 117	◯ Joint Inventor
◯ Person to whom the inventor is obligated to assign.	◯ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Cypress Semiconductor Corporation		
Mailing Address Information For Applicant:			
Address 1	198 Champion Court		
Address 2			
City	San Jose	**State/Province**	CA
Country	US	Postal Code	95134
Phone Number	408-943-2600	Fax Number	408-545-6911
Email Address	patents@cypress.com		

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Christopher Jordan/			Date (YYYY-MM-DD)	2016-12-19
First Name	Christopher	Last Name	Jordan	Registration Number	65809

Additional Signature may be generated within this form by selecting the Add button.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1C3
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Cypress Semiconductor Corporation

Application No./Patent No.: 15/335,180 Filed/Issue Date: 10-26-2016

Titled: METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Cypress Semiconductor Corporation, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: POLISHCHUK, IGOR, et al. To: Cypress Semiconductor Corporation

   The document was recorded in the United States Patent and Trademark Office at

   Reel 040394, Frame 0504, or for which a copy thereof is attached.

2. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Christopher Jordan/	12/19/2016
Signature	Date
Christopher Jordan	65809
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15335180
Filing Date:	26-Oct-2016
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Attorney Docket Number:	PM07027D1CIP1C3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	140	140
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1740**

Electronic Acknowledgement Receipt	
EFS ID:	27836717
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	19-DEC-2016
Filing Date:	26-OCT-2016
Time Stamp:	17:03:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1740
RAM confirmation Number	122016INTEFSW00004786503781
Deposit Account	503781
Authorized User	Timothy Croll
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	PM07027D1CIP1C3_ReplyToNoticeOfMissingParts_11082016.pdf	60211 3bf4b637b8bef29a7022450ca54df9d8f3902b4a	no	2
Warnings:					
Information:					
2	Preliminary Amendment	PM07027D1CIP1C3_PreliminaryAmendment_12012016.pdf	92890 2c7c01d958b7b4ab36f10834a051e590c8f47211	no	7
Warnings:					
Information:					
3	Oath or Declaration filed	PM07027D1CIP1C1_Oath_Levy.pdf	117729 f7678873ffc9fa04d0aa90f5f82652bd55d726f8	no	1
Warnings:					
Information:					
4	Oath or Declaration filed	PM07027D1CIP1C1_Oath_Polishchuk.pdf	122546 8cb3f342dae263e8070d062437ababa4e762950d	no	1
Warnings:					
Information:					
5	Oath or Declaration filed	PM07027D1CIP1C1_Oath_Ramkumar.pdf	111762 906b9dbc4d03af859e4b8d820b29086abc10e5d5	no	1
Warnings:					
Information:					
6	Application Data Sheet	PM07027D1CIP1C3_SupplementalADS_AIA14_12192016.pdf	58592 240d814abfef6682d5f08b6952f7b3dda38a7d5b	no	9
Warnings:					
Information:					

This is not an USPTO supplied ADS fillable form					
7	Assignee showing of ownership per 37 CFR 3.73	PM07027D1CIP1C3_373C_12192016.pdf	119873 470c4b6369161e7770961a3f4fb4ebd75cca8e94	no	3
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	37000 69dc253472a7630acbbcbceb2b5093f06351a763	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	720603		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	Examiner: Unknown
Igor Polishchuk, et al.	)	
	)	Group Art Unit: 2827
Application No.: 15/335,180	)	
	)	Confirmation No.: 6223
Filed: October 26, 2016	)	
	)	
For: METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	)	

RESPONSE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION AND NOTICE OF INCOMPLETE REPLY (NONPROVISIONAL)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madame:

Applicant hereby responds to the NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION, mailed November 08, 2016, and NOTICE OF INOCOMPLETE REPLY, mailed November 16, 2016. Enclosed is the basic filing fee, surcharge, search fee, examination fee, and oaths. Also enclosed please find a Supplemental Application Data Sheet underlining additions for the Applicant Information and a statement under 37 CFR 3.73(c) showing chain of title in response to the RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT mailed on November 16, 2016.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present

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application, and to credit any overpayments, to Deposit Account No. 50-3781.

Should the Patent Office have any questions regarding this response or the application in general, the Patent Office is urged to contact the Applicant's undersigned attorney by telephone at (408) 545-7399. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

Date: 12/19/2016 By: /Christopher Jordan/
Christopher Jordan
Registration No. 65,809

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Sandisk Technologies, Inc. - Ex. 1002, Page 000132

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/335,180	10/26/2016	2827	1740	PM07027D1CIP1C3	20	3

CONFIRMATION NO. 6223

UPDATED FILING RECEIPT

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

OC000000088083486

Date Mailed: 12/23/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Igor Polishchuk, Fremont, CA;
Sagy Charel Levy, Zichron Yaakov, ISRAEL;
Krishnaswamy Ramkumar, San Jose, CA;

Applicant(s)

Cypress Semiconductor Corporation, San Jose, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 14/811,346 07/28/2015 PAT 9502543
which is a CON of 14/159,315 01/20/2014 PAT 9093318
which is a CON of 13/539,466 07/01/2012 PAT 8633537
which is a CIP of 13/288,919 11/03/2011 PAT 8859374
which is a DIV of 12/152,518 05/13/2008 PAT 8063434
which claims benefit of 60/940,160 05/25/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

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Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 11/03/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/335,180**

Projected Publication Date: 03/30/2017

Non-Publication Request: No

Early Publication Request: No

Title

METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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Sandisk Technologies, Inc. - Ex. 1002, Page 000136

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/335,180

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

To: patents@cypress.com,pbj@cypress.com,pbjtmp2@cypress.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 60909

Dec 23, 2016 03:47:59 AM

Dear PAIR Customer:

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 60909 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
15335180	APP.FILE.REC	12/23/2016	PM07027D1CIP1C3

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

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Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	15/335,180
Filing Date	10-26-2016
First Named Inventor	Igor Polishchuk
Title	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jose Augusto de Oliveira/	Date (Optional)	03/27/2017
Name	Jose Augusto de Oliveira	Registration Number	
Title (if Applicant is a juristic entity)	Chief Technical Officer		
Applicant Name (if Applicant is a juristic entity)	Cypress Semiconductor Corporation		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
15/335,180	10-26-2016

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 60909

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Cypress Semiconductor Corporation

☐ Inventor or Joint Inventor (title not required below)
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	/Jose Augusto de Oliveira/	Date (Optional)	03/27/2017
Name	Jose Augusto de Oliveira		
Title	Chief Technical Officer, Cypress Semiconductor Corporation		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/82C (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
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POWER OF ATTORNEY BY APPLICANT

No more than ten (10) patent practitioners total may be appointed as set forth below by name and registration number. This page need not be submitted if appointing the Patent Practitioner(s) associated with a Customer Number (see form PTO/AIA/82B):

Name	Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	28744325
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Christine Morales
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	27-MAR-2017
Filing Date:	26-OCT-2016
Time Stamp:	14:09:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

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File Listing:

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1	Power of Attorney	PM07027D1CIP1C3_AIA82_POA_03272017.pdf	154808 e333bc80c740048a02c04a4819d8dc6ea6e50d57	no	4

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3

CONFIRMATION NO. 6223

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

POA ACCEPTANCE LETTER

OC000000090302388

Date Mailed: 03/31/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/27/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

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198 CHAMPION COURT
SAN JOSE, CA 95134-1709

PUBLICATION NOTICE

OC000000090295473

Title:METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Publication No.US-2017-0092729-A1
Publication Date:03/30/2017

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

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	50	Yang et al., "Reliability considerations in scaled SONOS nonvolatile memory devices, solid state Electronics", 43(1999) 2025-2032.	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Andrea Wheeler/	Date (YYYY-MM-DD)	2017-04-21
Name/Print	Andrea Wheeler	Registration Number	73780

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MAX 9000

Programmable Logic Device Family

July 1999, ver. 6.01 Data Sheet

A-DS-M9000-06.01

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...and More Features

- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable security bit for protection of proprietary designs
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), BitBlaster™ serial download cable, ByteBlaster™ parallel port download cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers
- Offered in a variety of package options with 84 to 356 pins (see Table 2)

Table 2. MAX 9000 Package Options & I/O Counts *Note (1)*

Device	84-Pin PLCC	208-Pin RQFP	240-Pin RQFP	280-Pin PGA	304-Pin RQFP	356-Pin BGA
EPM9320	60 *(2)*	132	–	168	–	168
EPM9320A	60 *(2)*	132	–	–	–	168
EPM9400	59 *(2)*	139	159	–	–	–
EPM9480	–	146	175	–	–	–
EPM9560	–	153	191	216	216	216
EPM9560A	–	153	191	–	–	216

Notes:

(1) MAX 9000 device package types include plastic J-lead chip carrier (PLCC), power quad flat pack (RQFP), ceramic pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.

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General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EPLDs is based on Altera's third-generation MAX architecture. Fabricated on an advanced CMOS technology, the EEPROM-based MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 144 MHz. The -10 speed grade of the MAX 9000 family is compliant with the *PCI Local Bus Specification, Revision 2.2*. Table 3 shows the speed grades available for MAX 9000 devices.

Table 3. MAX 9000 Speed Grade Availability

Device	Speed Grade		
	-10	-15	-20
EPM9320		✓	✓
EPM9320A	✓		
EPM9400		✓	✓
EPM9480		✓	✓
EPM9560		✓	✓
EPM9560A	✓		

Table 4 shows the performance of MAX 9000 devices for typical functions.

Table 4. MAX 9000 Performance *Note (1)*

Application	Macrocells Used	Speed Grade			Units
		-10	-15	-20	
16-bit loadable counter	16	144	118	100	MHz
16-bit up/down counter	16	144	118	100	MHz
16-bit prescaled counter	16	144	118	100	MHz
16-bit address decode	1	5.6 (10)	7.9 (15)	10 (20)	ns
16-to-1 multiplexer	1	7.7 (12.1)	10.9 (18)	16 (26)	ns

Note:

(1) Internal logic array block (LAB) performance is shown. Numbers in parentheses show external delays from row input pin to row I/O pin.

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field-programmable gate array (FPGA) devices and EPLDs.

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All MAX 9000 device packages provide four dedicated inputs for global control signals with large fan-outs. Each I/O pin has an associated I/O cell register with a clock enable control on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

MAX 9000 EPLDs provide 5.0-V in-system programmability (ISP). This feature allows the devices to be programmed and reprogrammed on the printed circuit board (PCB) for quick and efficient iterations during design development and debug cycles. MAX 9000 devices are guaranteed for 100 program and erase cycles.

MAX 9000 EPLDs contain 320 to 560 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. For increased flexibility, each macrocell offers a dual-output structure that allows the register and the product terms to be used independently. This feature allows register-rich and combinatorial-intensive designs to be implemented efficiently. The dual-output structure of the MAX 9000 macrocell also improves logic utilization, thus increasing the effective capacity of the devices. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 9000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay. MAX 9000 devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. MAX 9000 devices offer the MultiVolt feature, which allows output drivers to be set for either 3.3-V or 5.0-V operation in mixed-voltage systems.

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The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated software package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet.*

Functional Description

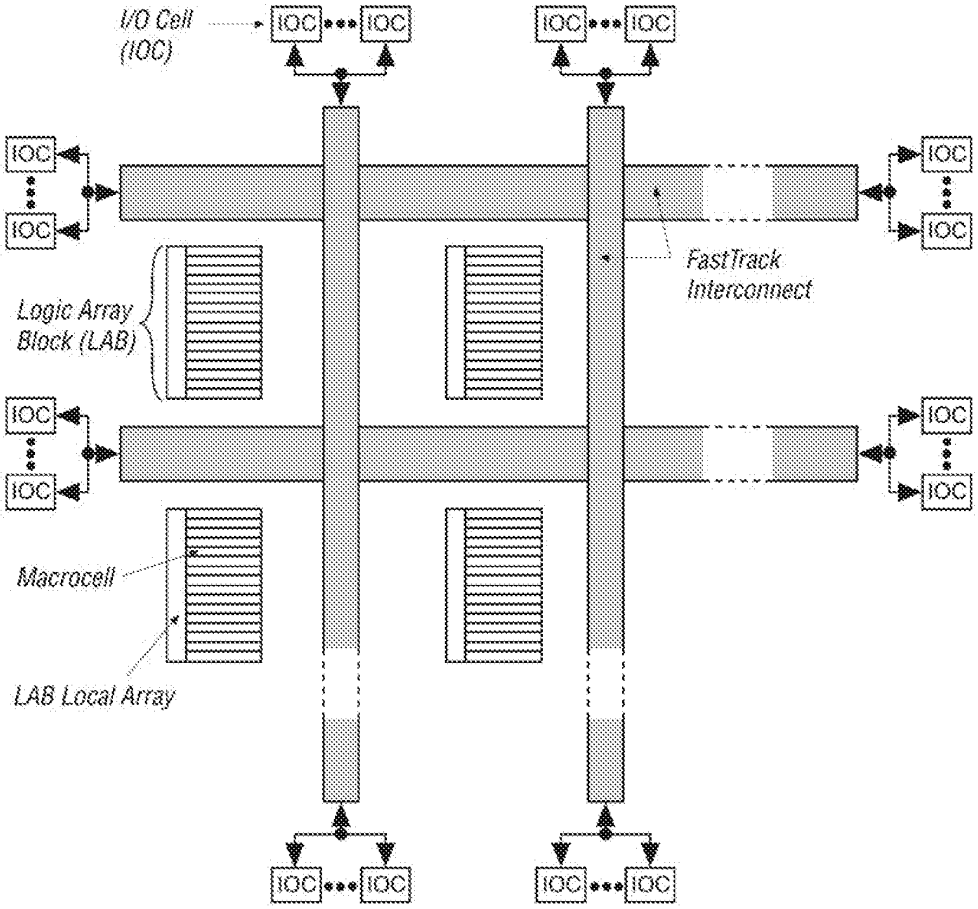
MAX 9000 devices use a third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. The MAX 9000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- Dedicated inputs
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

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Figure 1. MAX 9000 Device Block Diagram



Logic Array Blocks

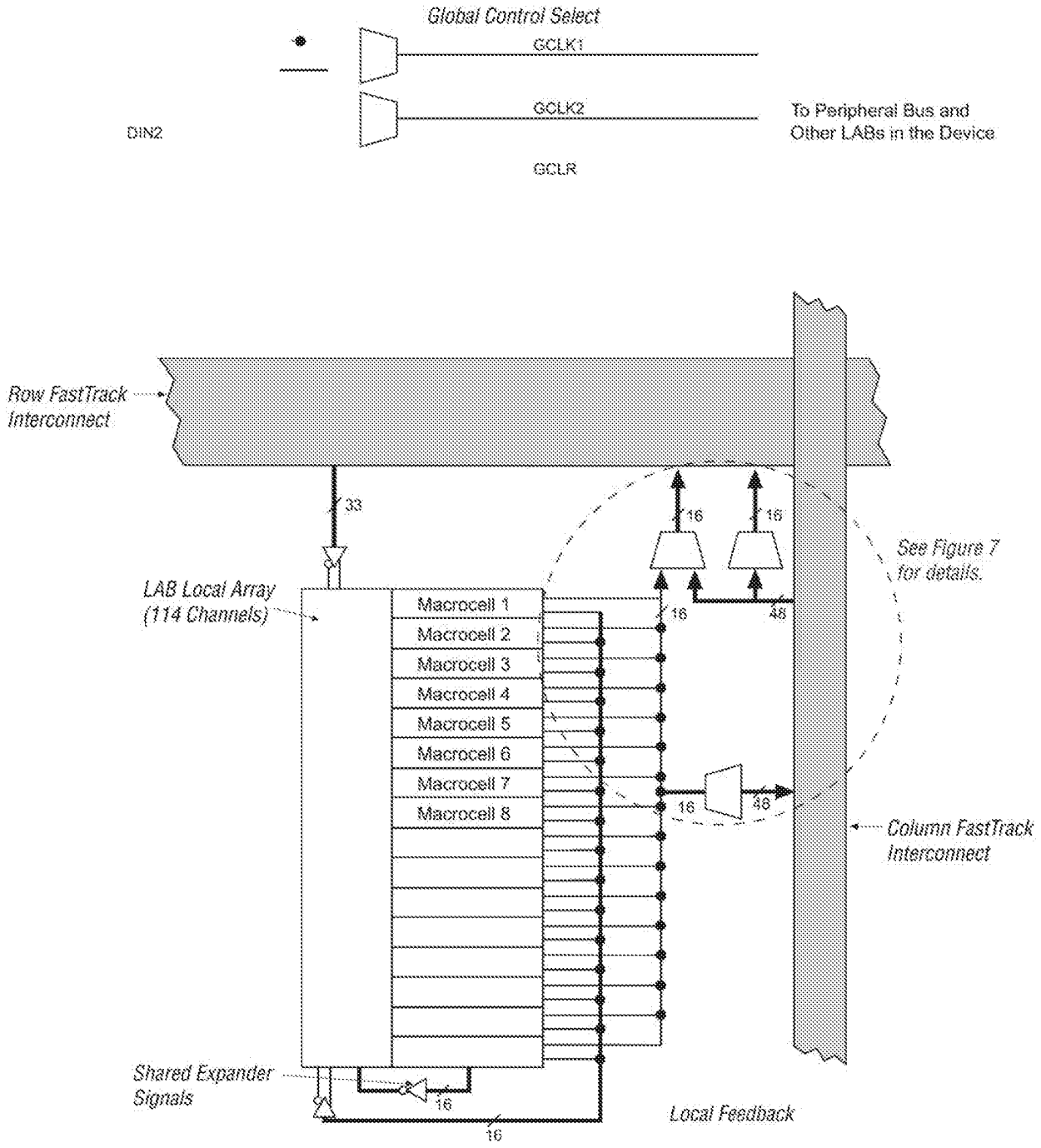
The MAX 9000 architecture is based on linking high-performance, flexible logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in Figure 2 on page 7. Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by I/O cells (IOCs) located at the end of each row (horizontal) and column (vertical) path of the FastTrack Interconnect.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms ("expanders") are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global clocks and one global clear that can be used for register control signals in all 16 macrocells.

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LABs drive the row and column interconnect directly. Each macrocell can drive out of the LAB onto one or both routing resources. Once on the row or column interconnect, signals can traverse to other LABs or to the IOCs.

Figure 2. MAX 9000 Logic Array Block

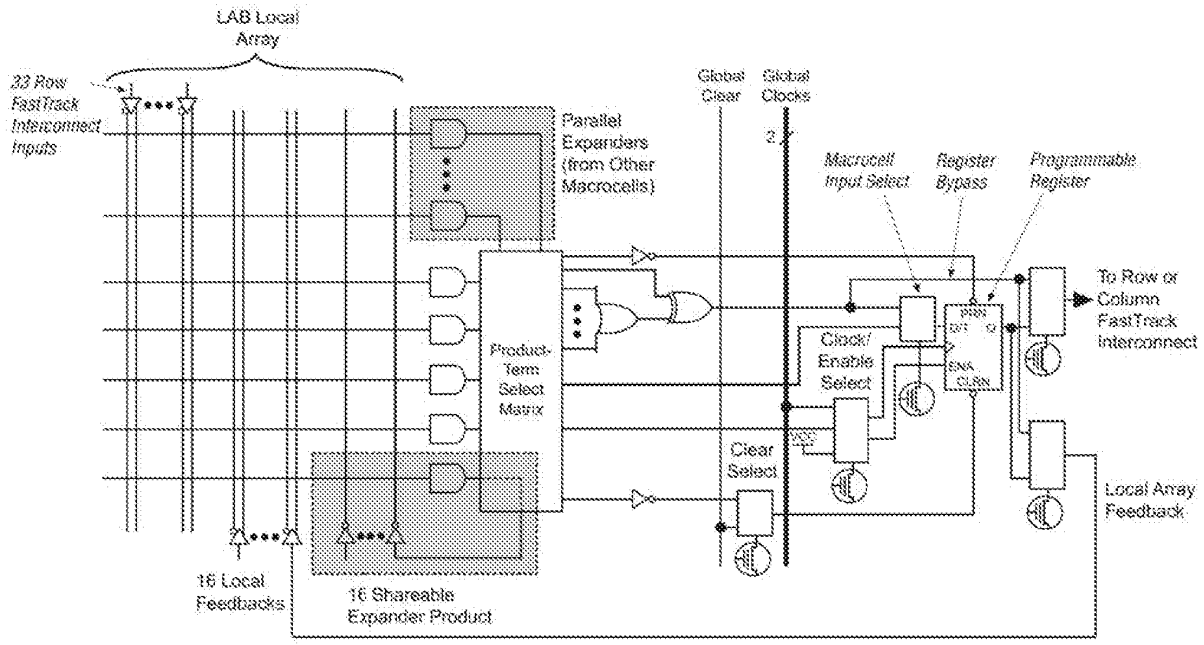


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Macrocells

The MAX 9000 macrocell consists of three functional blocks: the product terms, the product-term select matrix, and the programmable register. The macrocell can be individually configured for both sequential and combinatorial logic operation. See Figure 3.

Figure 3. MAX 9000 Macrocell & Local Array



Combinatorial logic is implemented in the local array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II software automatically optimizes product-term allocation according to the logic requirements of the design.

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For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; the MAX+PLUS II software then selects the most efficient register operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By either global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available. As shown in Figure 2, these global clock signals can be the true or the complement of either of the global clock pins (DIN1 and DIN2).

Each register also supports asynchronous preset and clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the dedicated global clear pin (DIN3). The global clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

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Expander Product Terms

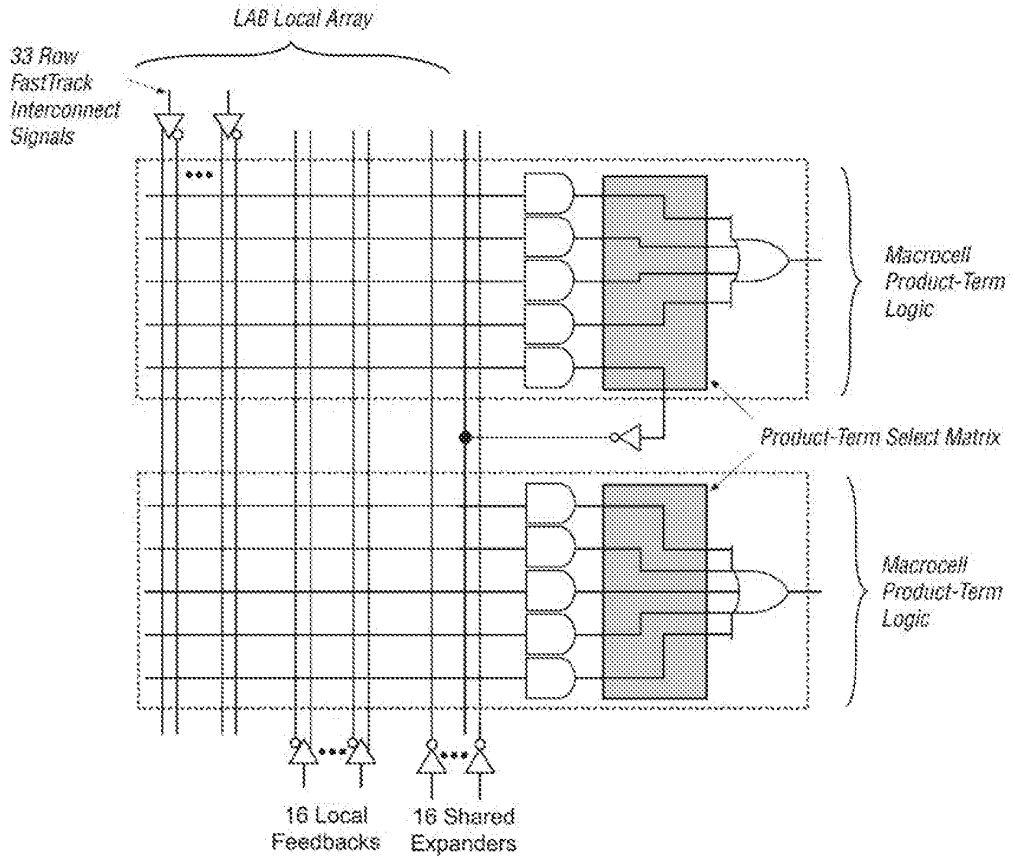
Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although another macrocell can supply the required logic resources, the MAX 9000 architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the LAB local array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{LOCAL} + t_{SEXP}) is incurred when shareable expanders are used. Figure 4 shows how shareable expanders can feed multiple macrocells.

Figure 4. MAX 9000 Shareable Expanders

Shareable expanders can be shared by any or all macrocells in the LAB.



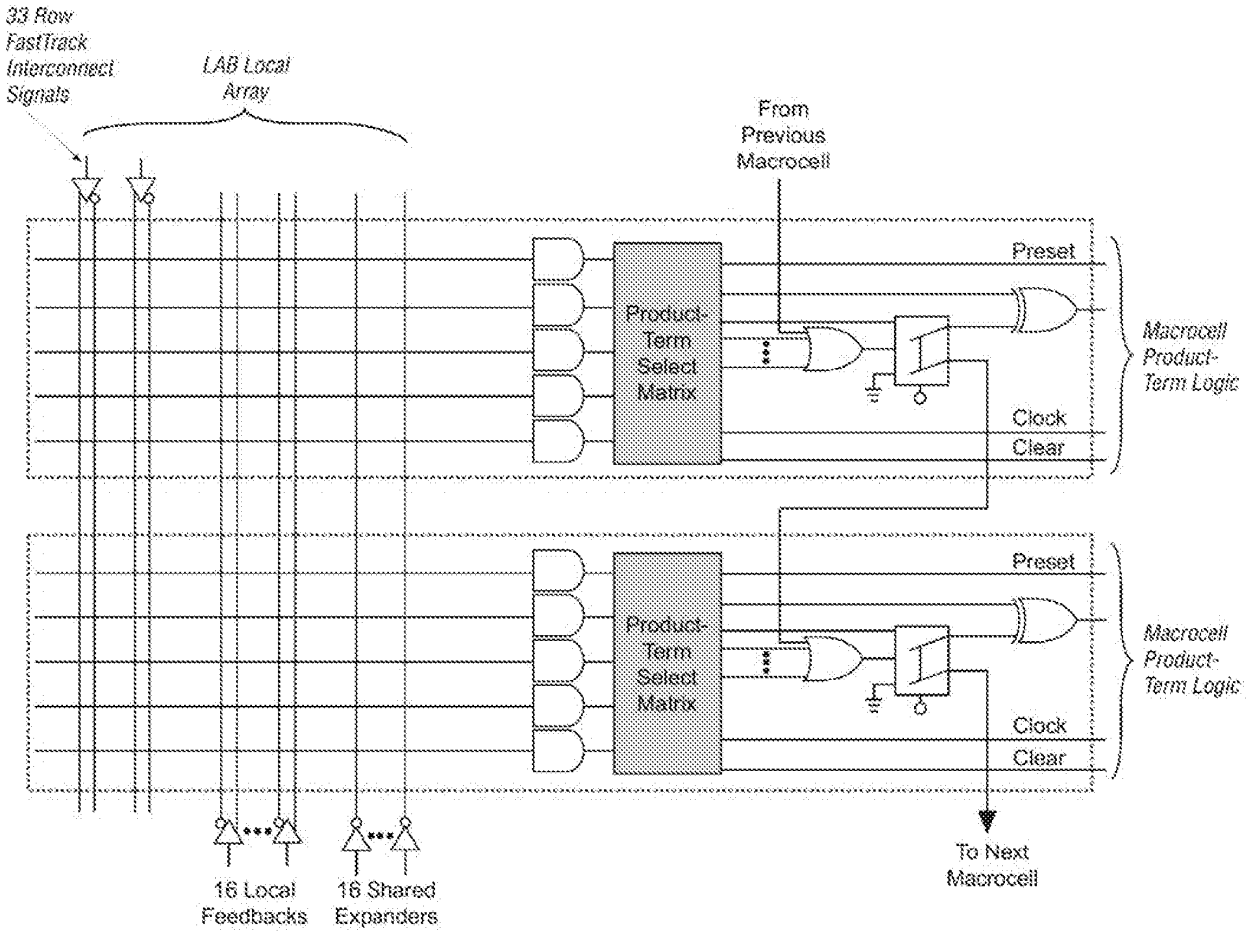
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Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. Figure 5 shows how parallel expanders can feed the neighboring macrocell.

Figure 5. MAX 9000 Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



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The MAX+PLUS II Compiler automatically allocates as many as three sets of up to five parallel expanders to macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

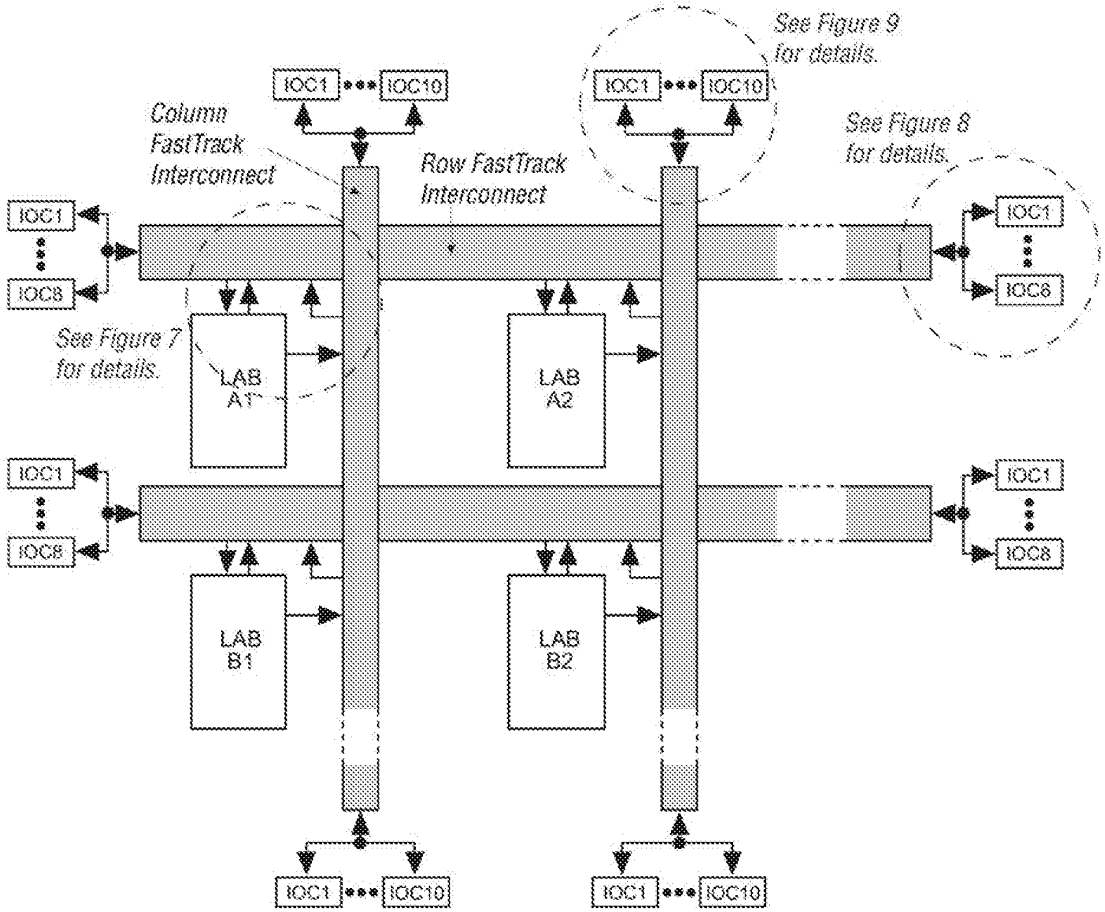
FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. Figure 6 shows the interconnection of four adjacent LABs with row and column interconnects.

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Figure 6. MAX 9000 Device Interconnect Resources

Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.



The LABs within MAX 9000 devices are arranged into a matrix of columns and rows. Table 5 shows the number of columns and rows in each MAX 9000 device.

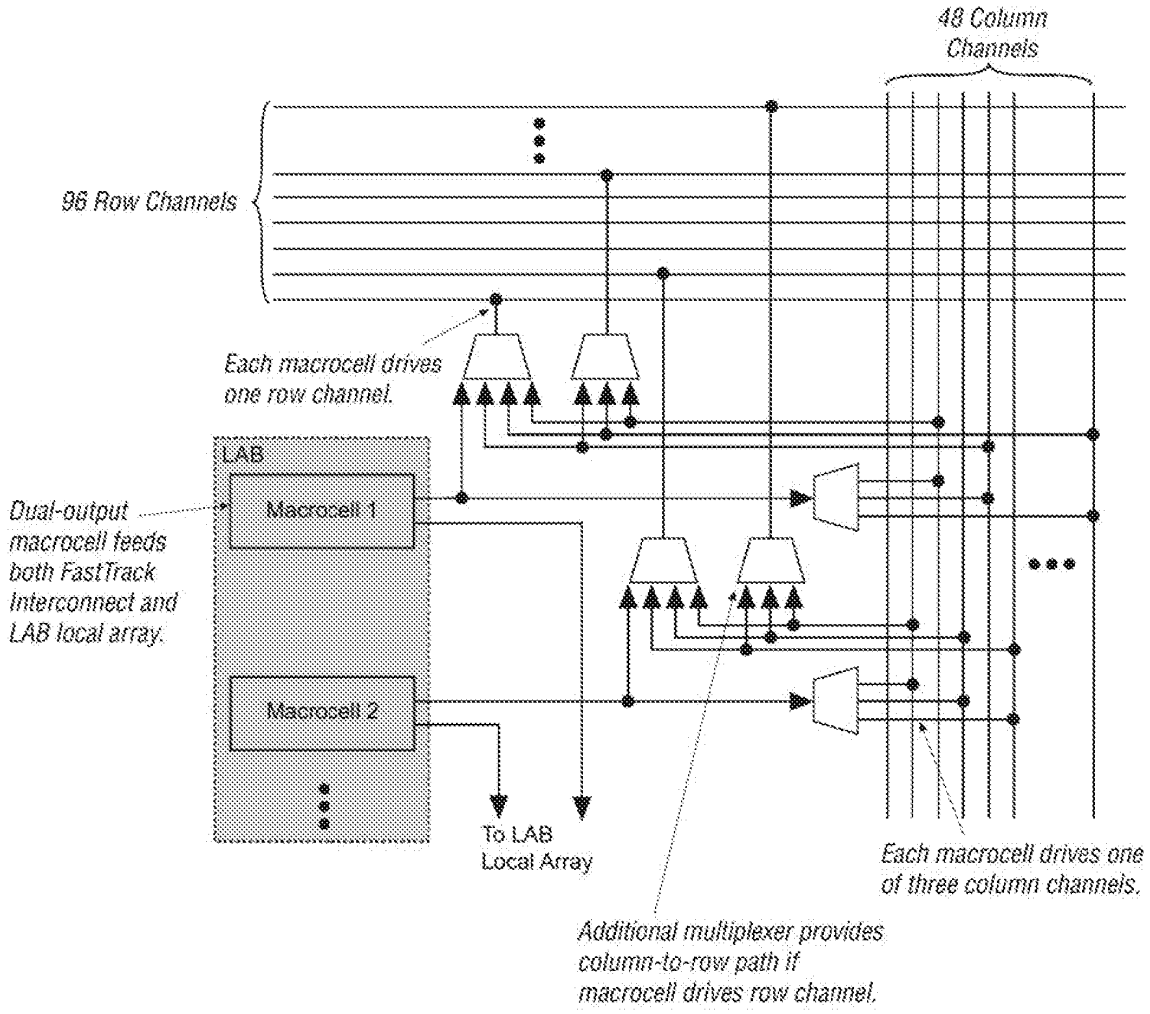
Table 5. MAX 9000 Rows & Columns

Devices	Rows	Columns
EPM9320, EPM9320A	4	5
EPM9400	5	5
EPM9480	6	5
EPM9560, EPM9560A	7	5

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Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Each row interconnect has a total of 96 channels. Figure 7 shows how a macrocell drives the row and column interconnect.

Figure 7. MAX 9000 LAB Connections to Row & Column Interconnect



Each macrocell in the LAB can drive one of three separate column interconnect channels. The column channels run vertically across the entire device, and are shared by the macrocells in the same column. The MAX+PLUS II Compiler optimizes connections to a column channel automatically.

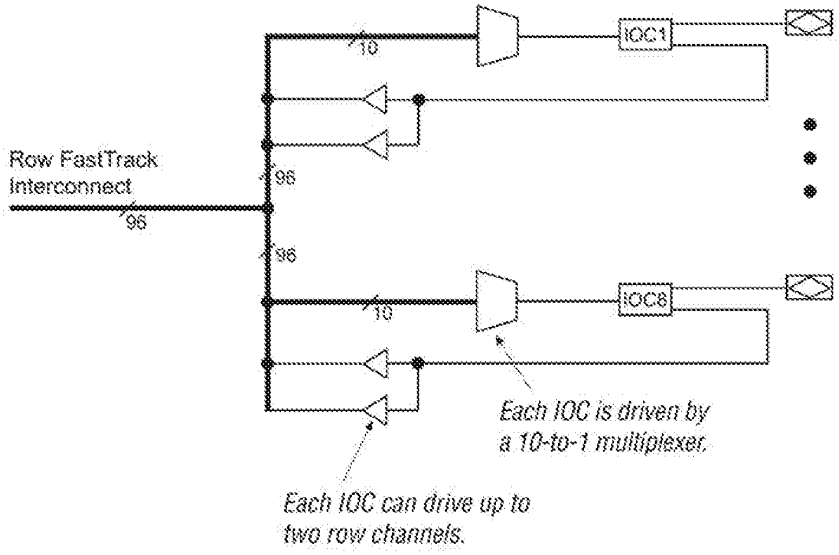
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A row interconnect channel can be fed by the output of the macrocell through a 4-to-1 multiplexer that the macrocell shares with three column channels. If the multiplexer is used for a macrocell-to-row connection, the three column signals can access another row channel via an additional 3-to-1 multiplexer. Within any LAB, the multiplexers provide all 48 column channels with access to 32 row channels.

Row-to-I/O Cell Connections

Figure 8 illustrates the connections between row interconnect channels and IOCs. An input signal from an IOC can drive two separate row channels. When an IOC is used as an output, the signal is driven by a 10-to-1 multiplexer that selects the row channels. Each end of the row channel feeds up to eight IOCs on the periphery of the device.

Figure 8. MAX 9000 Row-to-IOC Connections

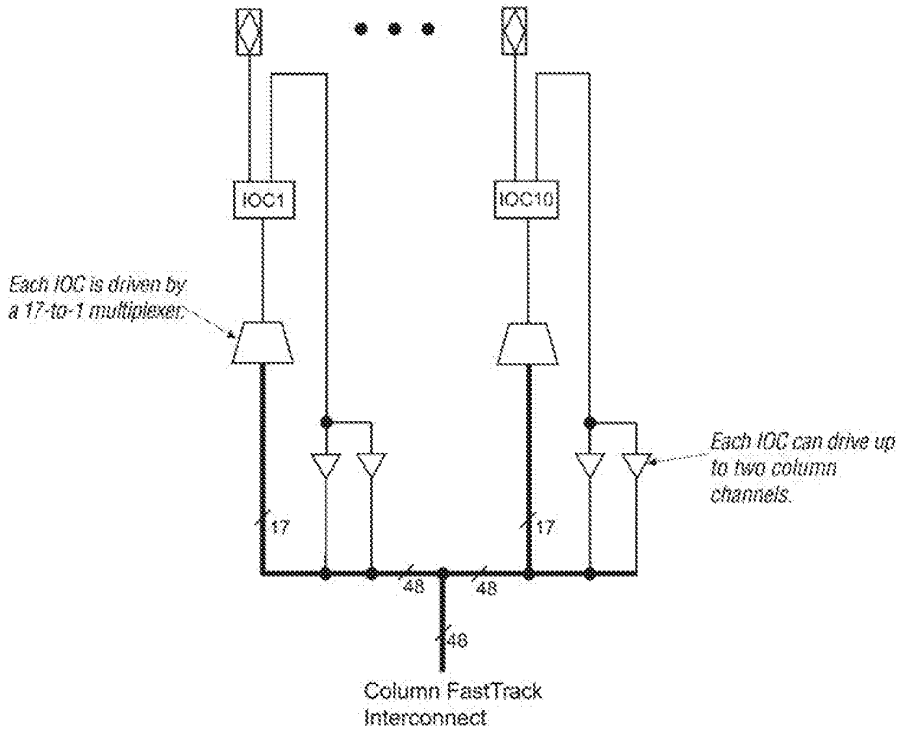


Column-to-I/O Cell Connections

Each end of a column channel has up to 10 IOCs (see Figure 9). An input signal from an IOC can drive two separate column channels. When an IOC is used as an output, the signal is driven by a 17-to-1 multiplexer that selects the column channels.

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Figure 9. MAX 9000 Column-to-IOC Connections



Dedicated Inputs

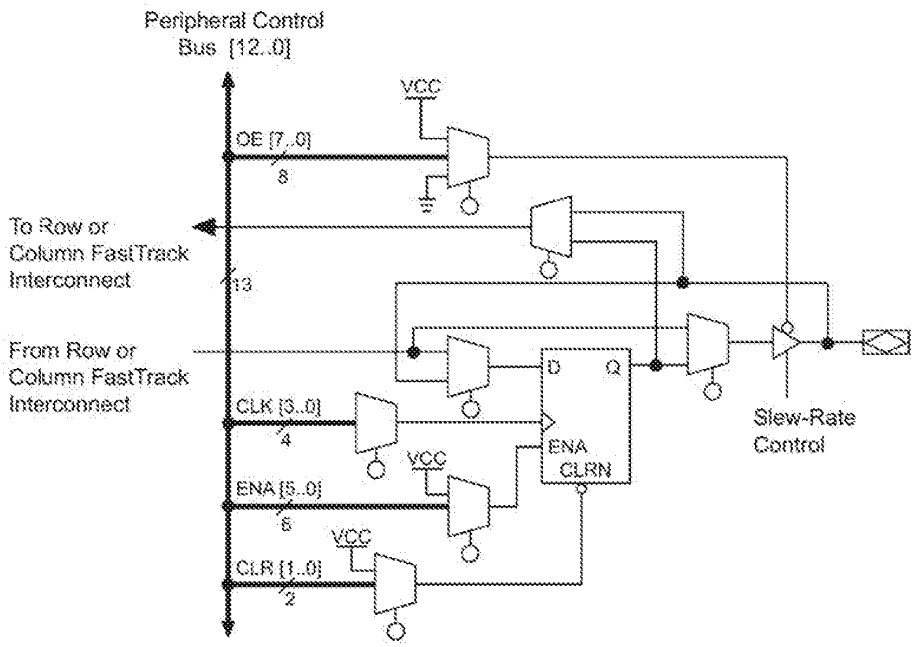
In addition to the general-purpose I/O pins, MAX 9000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution to the LABs and IOCs in the device, and are typically used for global clock, clear, and output enable control signals. The global control signals can feed the macrocell or IOC clock and clear inputs, as well as the IOC output enable. The dedicated inputs can also be used as general-purpose data inputs because they can feed the row FastTrack Interconnect (see Figure 2 on page 7).

I/O Cells

Figure 10 shows the IOC block diagram. Signals enter the MAX 9000 device from either the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOCs are located at the ends of the row and column interconnect channels.

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Figure 10. MAX 9000 IOC



I/O pins can be used as input, output, or bidirectional pins. Each IOC has an IOC register with a clock enable input. This register can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The IOC register clock enable allows the global clock to be used for fast clock-to-output performance, while maintaining the flexibility required for selective clocking.

The clock, clock enable, clear, and output enable controls for the IOCs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOC control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to eight output enable signals, up to four clock signals, up to six clock enable signals, and up to two clear signals. Table 6 on page 18 shows the sources that drive the peripheral bus and how the IOC control signals share the peripheral bus.

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The output buffer in each IOC has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces board-level noise and adds a nominal timing delay to the output buffer delay (t_{OD}) parameter. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis. The slew rate control affects both rising and falling edges of the output signals.

Table 6. Peripheral Bus Sources

Peripheral Control Signal	Source			
	EPM9320 EPM9320A	EPM9400	EPM9480	EPM9560 EPM9560A
OE0/ENA0	Row C	Row E	Row F	Row G
OE1/ENA1	Row B	Row E	Row F	Row F
OE2/ENA2	Row A	Row E	Row E	Row E
OE3/ENA3	Row B	Row B	Row B	Row B
OE4/ENA4	Row A	Row A	Row A	Row A
OE5	Row D	Row D	Row D	Row D
OE6	Row C	Row C	Row C	Row C
OE7/CLR1	Row B/GOE	Row B/GOE	Row B/GOE	Row B/GOE
CLR0/ENA5	Row A/GCLR	Row A/GCLR	Row A/GCLR	Row A/GCLR
CLK0	GCLK1	GCLK1	GCLK1	GCLK1
CLK1	GCLK2	GCLK2	GCLK2	GCLK2
CLK2	Row D	Row D	Row D	Row D
CLK3	Row C	Row C	Row C	Row C

Output Configuration

The MAX 9000 device architecture supports the MultiVolt I/O interface feature, which allows MAX 9000 devices to interface with systems of differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

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The VCCIO pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}.

In-System Programmability (ISP)

MAX 9000 devices can be programmed in-system through a 4-pin JTAG interface. ISP offers quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture internally generates the 12.0-V programming voltage required to program EEPROM cells, eliminating the need for an external 12.0-V power supply to program the devices on the board. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 9000 devices can be programmed by downloading the information via in-circuit testers, embedded processors, or the Altera BitBlaster, ByteBlaster, or ByteBlasterMV download cable. (The ByteBlaster cable is obsolete and has been replaced by the ByteBlasterMV cable, which can interface with 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high pin-count packages (e.g., QFP packages) due to device handling. MAX 9000 devices can also be reprogrammed in the field (i.e., product upgrades can be performed in the field via software or modem).

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers platforms have difficulties supporting an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm are marked with an "F" suffix in the ordering code.

Programming with External Hardware

MAX 9000 devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.



For more information, see the *Altera Programming Hardware Data Sheet*.

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The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 9000 device with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 9000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. Table 7 describes the JTAG instructions supported by the MAX 9000 family. The pin-out tables starting on page 35 show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 7. MAX 9000 JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be shifted out of TDO. Supported by the EPM9320A, EPM9400, EPM9480, and EPM9560A devices only.
UESCODE	Selects the user electronic signature (UESCODE) register and allows the UESCODE to be shifted out of TDO serially. This instruction is supported by MAX 9000A devices only.
ISP Instructions	These instructions are used when programming MAX 9000 devices via the JTAG ports with the BitBlaster or ByteBlasterMV download cable, or using a Jam File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format (**.svf**) File via an embedded processor or test equipment.

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The instruction register length for MAX 9000 devices is 10 bits. EPM9320A and EPM9560A devices support a 16-bit UESCODE register. Tables 8 and 9 show the boundary-scan register length and device IDCODE information for MAX 9000 devices.

Table 8. MAX 9000 Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM9320, EPM9320A	504
EPM9400	552
EPM9480	600
EPM9560, EPM9560A	648

Table 9. 32-Bit MAX 9000 Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits) *(2)*	Manufacturer's Identity (11 Bits)	1 (1 Bit)
EPM9320A *(3)*	0000	1001 0011 0010 0000	00001101110	1
EPM9400	0000	1001 0100 0000 0000	00001101110	1
EPM9480	0000	1001 0100 1000 0000	00001101110	1
EPM9560A *(3)*	0000	1001 0101 0110 0000	00001101110	1

Notes:
(1) The IDCODE's least significant bit (LSB) is always 1.
(2) The most significant bit (MSB) is on the left.
(3) Although the EPM9320A and EPM9560A devices support the IDCODE instruction, the EPM9320 and EPM9560 devices do not.

Figure 11 shows the timing requirements for the JTAG signals.

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Figure 11. MAX 9000 JTAG Waveforms

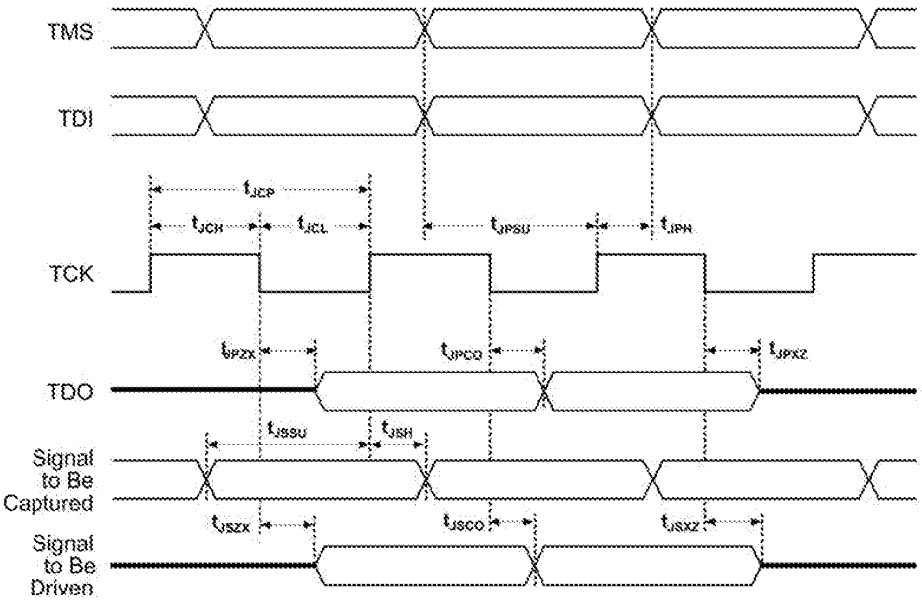


Table 10 shows the JTAG timing parameters and values for MAX 9000 devices.

Table 10. JTAG Timing Parameters & Values for MAX 9000 Devices

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices).*

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Programmable Speed/Power Control

MAX 9000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. Because most logic applications require only a small fraction of all gates to operate at maximum frequency, this feature allows total power dissipation to be reduced by 50% or more.

The designer can program each individual macrocell in a MAX 9000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the LAB local array delay (t_{LOCAL}).

Design Security

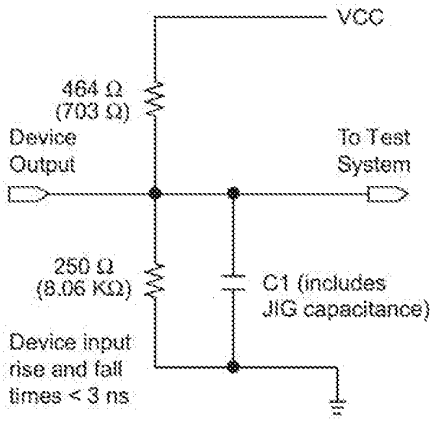
All MAX 9000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased.

Generic Testing

MAX 9000 EPLDs are fully functionally tested. Complete testing of each programmable EEPROM bit and all logic functionality ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 12. Test patterns can be used and then erased during the early stages of the production flow.

Figure 12. MAX 9000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V outputs. Numbers without parentheses are for 5.0-V devices or outputs.



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Operating Conditions

Tables 11 through 17 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 9000 devices.

Table 11. MAX 9000 Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
V_{CCISP}	Supply voltage during in-system programming		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP packages, under bias		135	° C

Table 12. MAX 9000 Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCISP}	Supply voltage during in-system programming		4.75	5.25	V
V_I	Input voltage		–0.5	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

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Table 13. MAX 9000 Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V *(7)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V *(7)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(7)*	V_{CCIO} – 0.2		V
V_{OL}	5.0-V low level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V *(7)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(7)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(7)*		0.2	V
I_I	I/O pin leakage current of dedicated input pins	V_I = V_{CC} or ground *(8)*	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or ground	–40	40	µA

Table 14. MAX 9000 Device Capacitance: EPM9320, EPM9400, EPM9480 & EPM9560 Devices *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{DIN1}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		18	pF
C_{DIN2}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		18	pF
C_{DIN3}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		17	pF
C_{DIN4}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
$C_{I/O}$	I/O pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF

Table 15. MAX 9000A Device Capacitance: EPM9320A & EPM9560A Devices *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{DIN1}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		16	pF
C_{DIN2}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{DIN3}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{DIN4}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
$C_{I/O}$	I/O pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF

Table 16. MAX 9000 Device Typical I_{CC} Supply Current Values

Symbol	Parameter	Conditions	EPM9320	EPM9400	EPM9480	EPM9560	Unit
I_{CC1}	I_{CC} supply current (low-power mode, standby, typical)	V_I = ground, no load *(10)*	106	132	140	146	mA

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Table 17. MAX 9000A Device Typical I_{CC} Supply Current Values

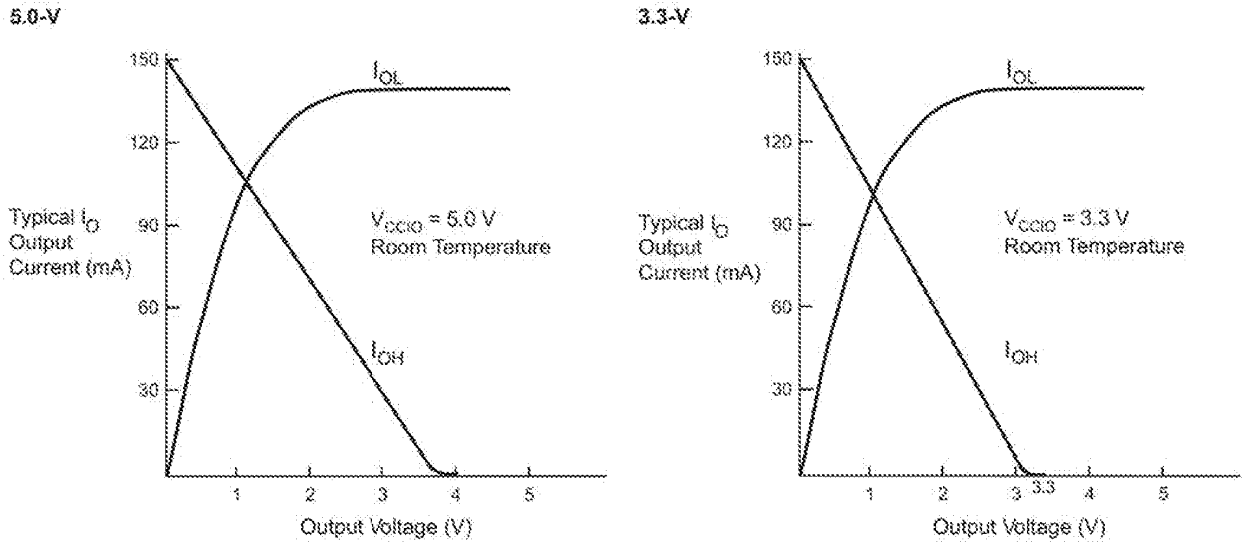
Symbol	Parameter	Conditions	EPM9320A	EPM9560A	Unit
I_{CC1}	I_{CC} supply current (low-power mode, standby, typical)	V_I = ground, no load *(10)*	99	174	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input on I/O pins is –0.5 V and on the four dedicated input pins is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) V_{CC} must rise monotonically.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under the MAX 9000 recommended operating conditions, shown in Table 12 on page 24.
(7) This parameter is measured with 50% of the outputs each sinking 12 mA. The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to the low-level TTL or CMOS output current.
(8) JTAG pin input leakage is typically –60 µA.
(9) Capacitance is sample-tested only and is measured at 25° C.
(10) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.

Figure 13 shows typical output drive characteristics for MAX 9000 devices with 5.0-V and 3.3-V V_{CCIO}.

Figure 13. Output Drive Characteristics of MAX 9000 Devices *Note (1)*



Note:

(1) Output drive characteristics include the JTAG TDO pin.

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Timing Model

The continuous, high-performance FastTrack Interconnect ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

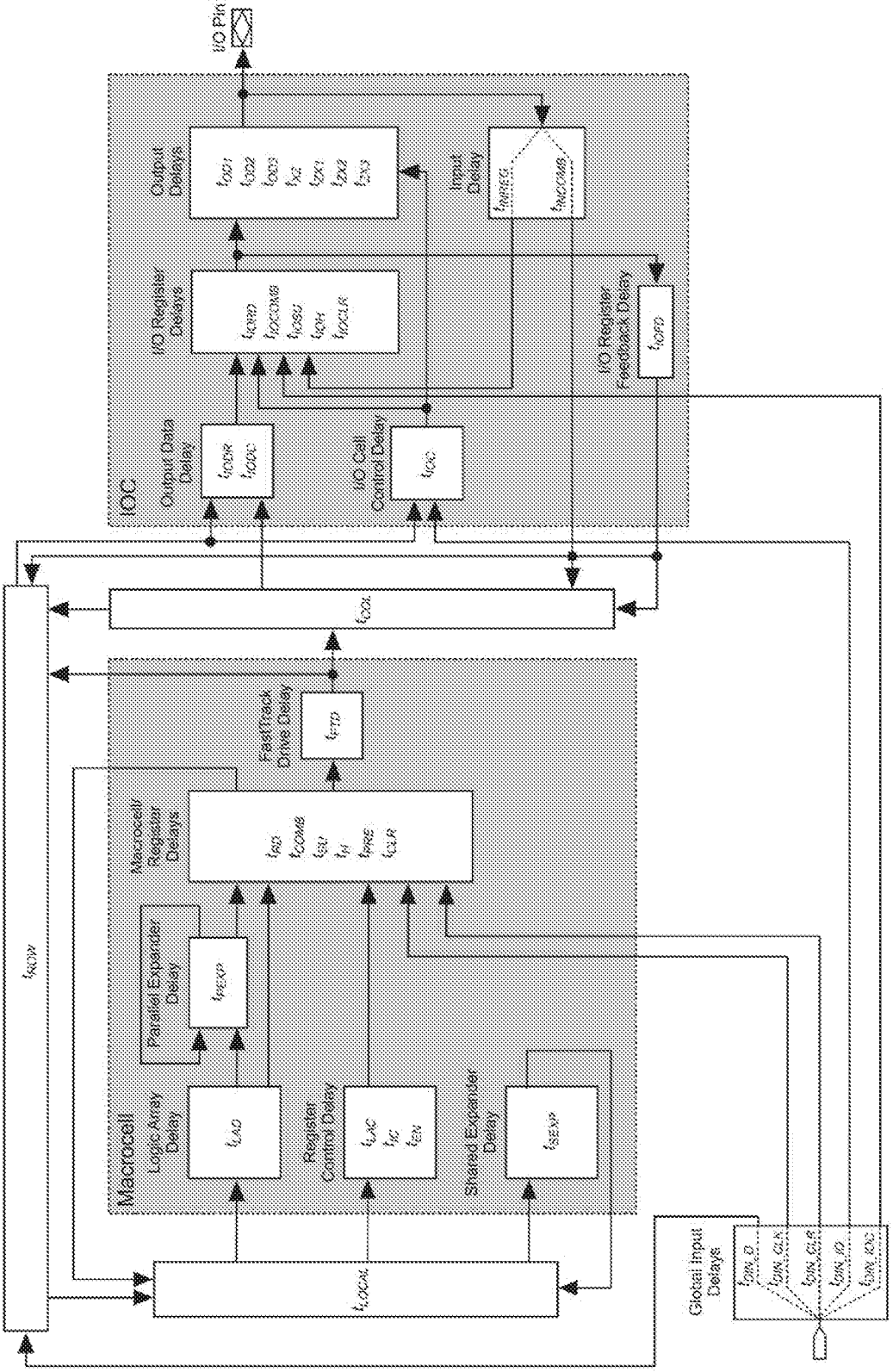
The MAX 9000 timing model in Figure 14 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the macrocell, IOC, and interconnect, including the row and column FastTrack Interconnect and LAB local array paths. Each parameter shown in Figure 14 is expressed as a worst-case value in the internal timing characteristics tables in this data sheet. Hand-calculations that use the MAX 9000 timing model and these timing parameters can be used to estimate MAX 9000 device performance.



For more information on calculating MAX 9000 timing delays, see *Application Note 77 (Understanding MAX 9000 Timing)* in this data book.

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Figure 14. MAX 9000 Timing Model



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Table 19. MAX 9000 Internal Timing Characteristics *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
t_{LAD}	Logic array delay			3.5		4.0		4.5	ns
t_{LAC}	Logic control array delay			3.5		4.0		4.5	ns
t_{IC}	Array clock delay			3.5		4.0		4.5	ns
t_{EN}	Register enable time			3.5		4.0		4.5	ns
t_{SEXP}	Shared expander delay			3.5		5.0		7.5	ns
t_{PEXP}	Parallel expander delay			0.5		1.0		2.0	ns
t_{RD}	Register delay			0.5		1.0		1.0	ns
t_{COMB}	Combinatorial delay			0.4		1.0		1.0	ns
t_{SU}	Register setup time		2.4		3.0		4.0		ns
t_{H}	Register hold time		2.0		3.5		4.5		ns
t_{PRE}	Register preset time			3.5		4.0		4.5	ns
t_{CLR}	Register clear time			3.7		4.0		4.5	ns
t_{FTD}	FastTrack drive delay			0.5		1.0		2.0	ns
t_{LPA}	Low-power adder	*(5)*		10.0		15.0		20.0	ns

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Table 20. IOC Delays

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
t_{IODR}	I/O row output data delay			0.2		0.2		1.5	ns
t_{IODC}	I/O column output data delay			0.4		0.2		1.5	ns
t_{IOC}	I/O control delay	(6)		0.5		1.0		2.0	ns
t_{IORD}	I/O register clock-to-output delay			0.6		1.0		1.5	ns
t_{IOCOMB}	I/O combinatorial delay			0.2		1.0		1.5	ns
t_{IOSU}	I/O register setup time before clock		2.0		4.0		5.0		ns
t_{IOH}	I/O register hold time after clock		1.0		1.0		1.0		ns
t_{IOCLR}	I/O register clear delay			1.5		3.0		3.0	ns
t_{IOFD}	I/O register feedback delay			0.0		0.0		0.5	ns
t_{INREG}	I/O input pad and buffer to I/O register delay			3.5		4.5		5.5	ns
t_{INCOMB}	I/O input pad and buffer to row and column delay			1.5		2.0		2.5	ns
t_{OD1}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF		1.8		2.5		2.5	ns
t_{OD2}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF		2.3		3.5		3.5	ns
t_{OD3}	Output buffer and pad delay, Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF		8.3		10.0		10.5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		2.5		2.5		2.5	ns
t_{ZX1}	Output buffer enable delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF		2.5		2.5		2.5	ns
t_{ZX2}	Output buffer enable delay, Slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF		3.0		3.5		3.5	ns
t_{ZX3}	Output buffer enable delay, Slow slew rate = on, V_{CCIO} = 3.3 V or 5.0 V	C1 = 35 pF		9.0		10.0		10.5	ns

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Table 21. Interconnect Delays

Symbol	Parameter	Conditions	Speed Grade						Unit
			-10		-15		-20		
			Min	Max	Min	Max	Min	Max	
t_{LOCAL}	LAB local array delay			0.5		0.5		0.5	ns
t_{ROW}	FastTrack row delay	*(6)*		0.9		1.4		2.0	ns
t_{COL}	FastTrack column delay	*(6)*		0.9		1.7		3.0	ns
t_{DIN_D}	Dedicated input data delay			4.0		4.5		5.0	ns
t_{DIN_CLK}	Dedicated input clock delay			2.7		3.5		4.0	ns
t_{DIN_CLR}	Dedicated input clear delay			4.5		5.0		5.5	ns
t_{DIN_IOC}	Dedicated input I/O register clock delay			2.5		3.5		4.5	ns
t_{DIN_IO}	Dedicated input I/O register control delay			5.5		6.0		6.5	ns

Notes to tables:

(1) These values are specified under the MAX 9000 device recommended operating conditions, shown in Table 12 on page 24.

(2) See *Application Note 77 (Understanding MAX 9000 Timing)* in this data book for more information on test conditions for t_{PD1} and t_{PD2} delays.

(3) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking as well as both macrocell and I/O cell registers.

(4) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.

(5) The t_{LPA} parameter must be added to the t_{LOCAL} parameter for macrocells running in low-power mode.

(6) The t_{ROW}, t_{COL}, and t_{IOC} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

Power Consumption

The supply power (P) versus frequency (f_{MAX}) for MAX 9000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book. The I_{CCINT} value depends on the switching frequency and the application logic.

The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times tog_{LC})$$

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The parameters in this equation are shown below:

MC_{TON} = Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Number of macrocells used in the design, as reported in the MAX+PLUS II Report File
f_{MAX} = Highest clock frequency to the device
tog_{LC} = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 22

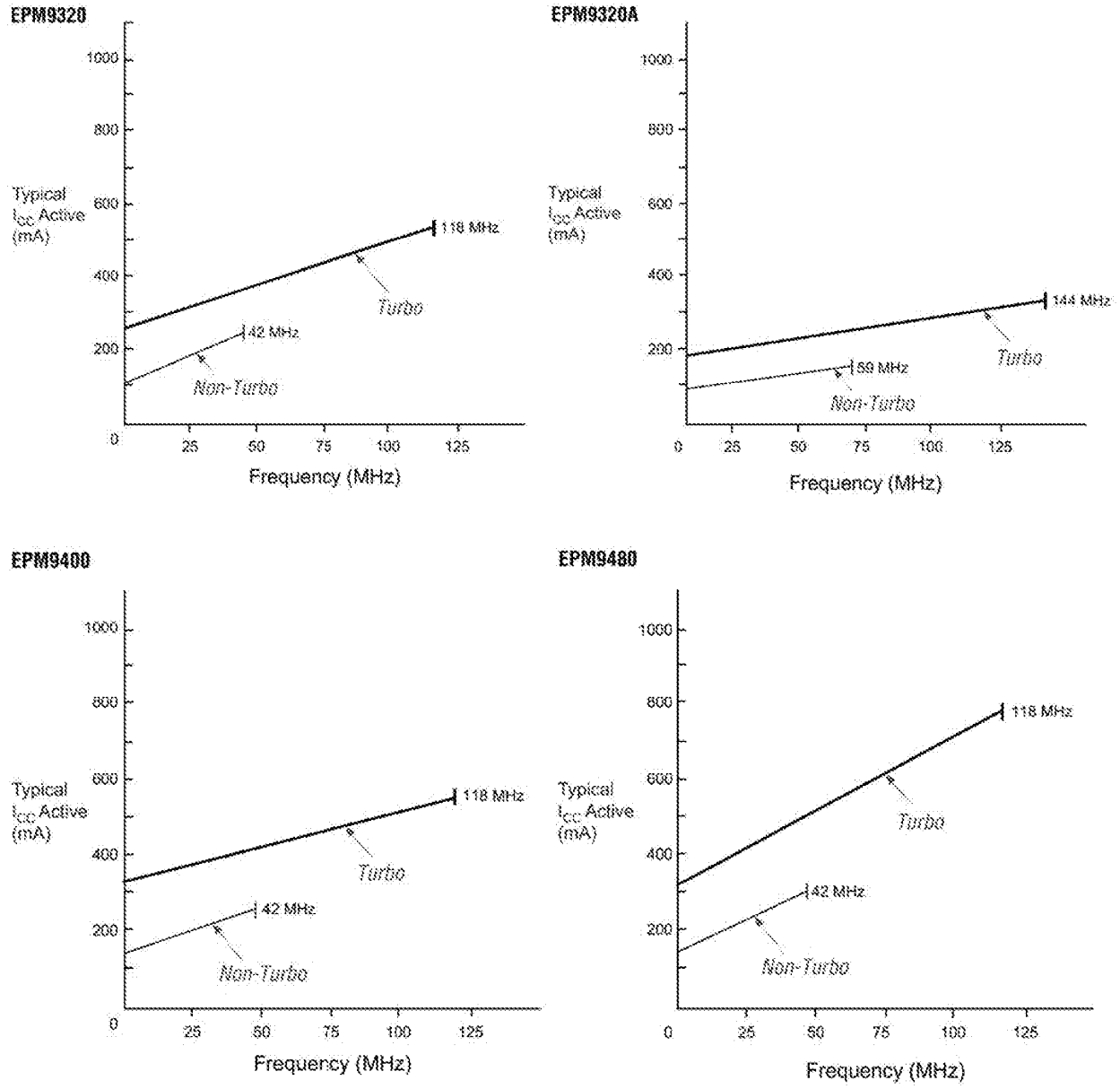
Table 22. MAX 9000 I_{CC} Equation Constants

Device	Constant A	Constant B	Constant C
EPM9320	0.81	0.33	0.056
EPM9320A	0.56	0.31	0.024
EPM9400	0.60	0.33	0.053
EPM9480	0.68	0.29	0.064
EPM9560	0.68	0.26	0.052
EPM9560A	0.56	0.31	0.024

This calculation provides an I_{CC} estimate based on typical conditions with no output load, using a typical pattern of a 16-bit, loadable, enabled up/down counter in each LAB. Actual I_{CC} values should be verified during operation, because the measurement is sensitive to the actual pattern in the device and the environmental operating conditions. Figure 15 shows typical supply current versus frequency for MAX 9000 devices.

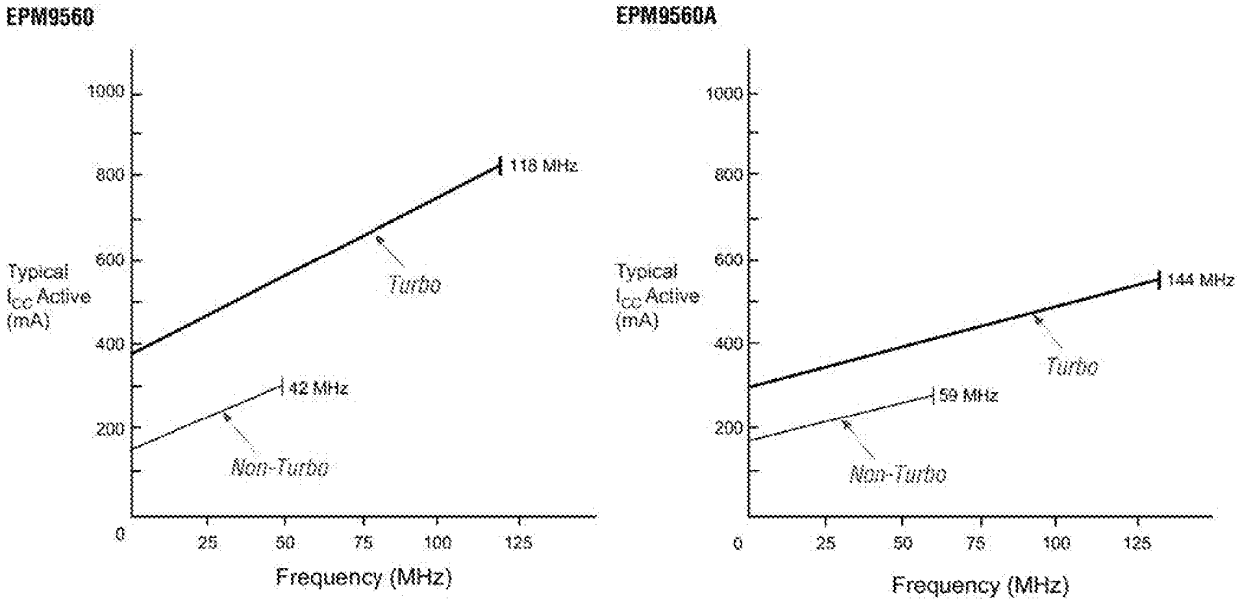
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Figure 15. I_{CC} vs. Frequency for MAX 9000 Devices (Part 1 of 2)



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Figure 15. I_{CC} vs. Frequency for MAX 9000 Devices (Part 2 of 2)



Device Pin-Outs

Tables 23 through 26 show the dedicated pin names and numbers for each EPM9320, EPM9320A, EPM9400, EPM9480, EPM9560, and EPM9560A device package.

Table 23. EPM9320 & EPM9320A Dedicated Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	84-Pin PLCC *(2)*	208-Pin RQFP	280-Pin PGA *(3)*	356-Pin BGA
DIN1 (GCLK1)	1	182	V10	AD13
DIN2 (GCLK2)	84	183	U10	AF14
DIN3 (GCLR)	13	153	V17	AD1
DIN4 (GOE)	72	4	W2	AC24
TCK	43	78	A9	A18
TMS	55	49	D6	E23
TDI	42	79	C11	A13
TDO	30	108	A18	D3

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Table 23. EPM9320 & EPM9320A Dedicated Pin-Outs (Part 2 of 2) *Note (1)*

Pin Name	84-Pin PLCC *(2)*	208-Pin RQFP	280-Pin PGA *(3)*	356-Pin BGA
GND	6, 18, 24, 25, 48, 61, 67, 70	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16	A9, A22, A25, A26, B25, B26, D2, E1, E26, F2, G1, G25, G26, H2, J1, J25, J26, K2, L26, M26, N1, N25, P26, R2, T1, U2, U26, V1, V25, W25, Y26, AA2, AB1, AB26, AC26, AE1, AF1, AF2, AF4, AF7, AF20
VCCINT (5.0 V only)	14, 21, 28, 57, 64, 71	10, 19, 30, 45, 112, 128, 139, 148	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	D26, F1, H1, K26, N26, P1, U1, W26, AE26, AF25, AF26
VCCIO (3.3 or 5.0 V)	15, 37, 60, 79	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	A1, A2, A21, B1, B10, B24, D1, H26, K1, M25, R1, V26, AA1, AC25, AF5, AF8, AF19
No Connect (N.C.)	29	6, 7, 8, 9, 11, 12, 13, 15, 16, 17, 18, 109, 140, 141, 142, 144, 145, 146, 147, 149, 150, 151	B6, K19, L2, L4, L18, L19, M1, M2, M3, M4, M16, M17, M18, M19, N1, N2, N3, N4, N16, N17, N18, N19, P1, P2, P3, P17, P18, P19, R1, R2, R3, R17, R18, R19, T1, T2, T3, T17, T18, T19, U1, U2, U3, U17, U18, U19, V1, V2, V19, W1	B4, B5, B6, B7, B8, B9, B11, B12, B13, B14, B15, B16, B18, B19, B20, B21, B22, B23, C4, C23, D4, D23, E4, E22, F4, F23, G4, H4, H23, J23, K4, L4, L23, N4, P4, P23, R3, R26, T2, T3, T4, T5, T22, T23, T24, T25, T26, U3, U4, U5, U22, U23, U24, U25, V2, V3, V4, V5, V22, V23, V24, W1, W2, W3, W4, W5, W22, W23, W24, Y1, Y2, Y3, Y4, Y5, Y22, Y23, Y24, Y25, AA3, AA4, AA5, AA22, AA23, AA24, AA25, AA26, AB2, AB3, AB4, AB5, AB23, AB24, AB25, AC1, AC2, AC23, AD4, AD23, AE4, AE5, AE6, AE7, AE9, AE11, AE12, AE14, AE15, AE16, AE18, AE19, AE20, AE21, AE22, AE23
VPP *(4)*	56	48	C4	E25
Total User I/O Pins *(5)*	60	132	168	168

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Notes:
(1) All pins not listed are user I/O pins.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.
(3) EPM9320A devices are not offered in this package.
(4) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(5) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 24. EPM9400 Dedicated Pin-Outs *Note (1)*

Pin Name	84-Pin PLCC *(2)*	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	2	182	210
DIN2 (GCLK2)	1	183	211
DIN3 (GCLR)	12	153	187
DIN4 (GOE)	74	4	234
TCK	43	78	91
TMS	54	49	68
TDI	42	79	92
TDO	31	108	114
GND	6, 13, 20, 26, 27, 47, 60, 66, 69, 73	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	16, 23, 30, 56, 63, 70	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	17, 37, 59, 80	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	–	6, 7, 8, 9, 11, 12, 13, 109, 144, 145, 146, 147, 149, 150, 151	1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 168, 169, 170, 171, 172, 173, 174, 175, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP *(3)*	55	48	67
Total User I/O Pins *(4)*	59	139	159

Notes:
(1) All pins not listed are user I/O pins.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* in this data book for more information.
(3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.

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Table 25. EPM9480 Dedicated Pin-Outs *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	182	210
DIN2 (GCLK2)	183	211
DIN3 (GCLR)	153	187
DIN4 (GOE)	4	234
TCK	78	91
TMS	49	68
TDI	79	92
TDO	108	114
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	6, 7, 8, 9, 109, 149, 150, 151	1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP *(2)*	48	67
Total User I/O Pins *(3)*	146	175

Notes:

(1) All pins not listed are user I/O pins.

(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

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Table 26. EPM9560 & EPM9560A Dedicated Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP	280-Pin PGA *(2)*	304-Pin RQFP *(2)*	356-Pin BGA
DIN1 (GCLK1)	182	210	V10	266	AD13
DIN2 (GCLK2)	183	211	U10	267	AF14
DIN3 (GCLR)	153	187	V17	237	AD1
DIN4 (GOE)	4	234	W2	296	AC24
TCK	78	91	A9	114	A18
TMS	49	68	D6	85	E23
TDI	79	92	C11	115	A13
TDO	108	114	A18	144	D3
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16	13, 22, 33, 42, 53, 62, 73, 74, 102, 121, 138, 155, 166, 167, 186, 187, 206, 207, 226, 254, 273, 290	A9, A22, A25, A26, B25, B26, D2, E1, E26, F2, G1, G25, G26, H2, J1, J25, J26, K2, L26, M26, N1, N25, P26, R2, T1, U2, U26, V1, V25, W25, Y26, AA2, AB1, AB26, AC26, AE1, AF1, AF2, AF4, AF7, AF20
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	12, 32, 52, 72, 157, 177, 197, 217	D26, F1, H1, K26, N26, P1, U1, W26, AE26, AF25, AF26
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	3, 23, 43, 63, 91, 108, 127, 156, 176, 196, 216, 243, 260, 279	A1, A2, A21, B1, B10, B24, D1, H26, K1, M25, R1, V26, AA1, AC25, AF5, AF8, AF19

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Table 26. EPM9560 & EPM9560A Dedicated Pin-Outs (Part 2 of 2) *Note (1)*

Pin Name	208-Pin RQFP	240-Pin RQFP	280-Pin PGA *(2)*	304-Pin RQFP *(2)*	356-Pin BGA
No Connect (N.C.)	109	–	B6, W1	1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304	B4, B5, B6, B7, B8, B9, B11, B12, B13, B14, B15, B16, B18, B19, B20, B21, B22, B23, C4, C23, D4, D23, E4, E22, F4, F23, G4, H4, H23, J23, K4, L4, L23, N4, P4, P23, T4, T23, U4, V4, V23, W4, Y4, AA4, AA23, AB4, AB23, AC23, AD4, AD23, AE4, AE5, AE6, AE7, AE9, AE11, AE12, AE14, AE15, AE16, AE18, AE19, AE20, AE21, AE22, AE23
VPP *(3)*	48	67	C4	75	E25
Total User I/O Pins *(4)*	153	191	216	216	216

Notes:
(1) All pins not listed are user I/O pins.
(2) EPM9560A devices are not offered in this package.
(3) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.
(4) The user I/O pin count includes dedicated input pins and all I/O pins.

Revision History

Information contained in the *MAX 9000 Programmable Logic Device Family Data Sheet* version 6.01 supersedes information published in previous versions. Version 6.01 contains corrected notes in Tables 12 and 13.

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Trimming Analog Circuits Using Floating-Gate Analog MOS Memory

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Abstract—A floating-gate MOS analog memory circuit that can be electrically programmed for positive and negative voltage changes, and that can be fabricated in a standard CMOS IC process is described. Unlike existing electrically erasable floating-gate memory circuits, this circuit does not require special fabrication techniques like ultrathin tunneling oxides or textured polysilicon. Instead, mask geometry is used to cause field-enhanced Fowler–Nordheim tunneling of electrons from a floating gate. Retention measurements at elevated temperatures indicate that the loss of floating-gate charge should be less than 0.1 percent over a ten year period at temperatures below 100°C. One limitation of this structure is that the rate of change of the floating-gate voltage can be quite small (e.g., 10 mV/s). A general trimming circuit, whose novel feature is that any number of trimming circuits can be independently and simultaneously adjusted across an entire IC, has been incorporated into a prototype CMOS op amp to decrease its input offset voltage from 10 mV to less than 0.5 mV.

I. Introduction

A MAJOR obstacle for the use of MOS transistors in precision analog circuits is the large mismatches typically found between adjacent devices, particularly differences in their threshold voltages. Often the size of large devices is dictated by matching requirements rather than by other circuit performance parameters. This paper presents an analog trim memory circuit that employs a floating-gate MOS structure similar to that used in digital electrically erasable programmable read-only memories (EEPROM's). Unlike existing floating-gate memory circuits, this circuit does not require special processing requirements like an ultrathin floating-gate oxide or textured-surface polysilicon. This is particularly important because the ultrathin oxide normally required for tunneling can be hard to fabricate reliably, and because these special processing features are simply not available in many design environments. The proposed analog memory circuit can be programmed electrically in both a positive and negative direction. This allows periodic recalibration of circuits to maintain trim accuracy in the face of temperature and age variations. In addition, the bipolar trim capability makes this circuit applicable to dynamic adjustment tasks, e.g., storing weights in adaptive filters and neural networks.

In this paper, a novel method for inducing electron tunneling through standard gate oxide at relatively low voltages is presented. This method differs from existing methods for field-enhanced tunneling of electrons though thick oxide [1], [2] because it does not require special texturing of the polysilicon surface. Instead, geometric factors induced by the layout are employed to enhance the electric field strength at the SiO_2 interface. In Section II, the structures used to inject electrons onto and remove electrons from the floating gate will be presented. In Section III, the characteristics of the analog memory circuit will be presented, and a design example utilizing the analog memory circuit for trimming the offset of an op amp will be presented in Section IV. Finally, other possible applications for the proposed analog memory circuit will be suggested in Section V.

II. Current Injector Structure

A floating-gate memory test circuit was fabricated in a 2-μm p-well CMOS process with a gate-oxide thickness of 40 nm. The test circuit consisted of the current injector, a PMOS sense transistor, a bootstrap capacitor to allow external control of the floating-gate voltage, and the input stage of a simple two-stage op amp.

Unlike many of the early EPROM technologies, which used avalanche injection of "hot" electrons to inject electrons onto the floating gate [3]–[5], the proposed analog memory circuit injects electrons onto and removes electrons from the floating gate using Fowler–Nordheim tunneling, which is the standard mechanism used for removing electrons or for both injecting and removing electrons in many EEPROM's [1], [5]–[13]. Circuits that use Fowler–Nordheim tunneling for both injecting and removing electrons have the advantage that although high voltages are needed, very little current is drawn and it is relatively easy to integrate the necessary power supplies onto the IC [1], [14]. Fowler–Nordheim tunneling of elec-

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trons in MOS structures has been the subject of much study (e.g., [6], [15]–[19]).

A simplified view of Fowler–Nordheim tunneling is the following. There is an energy barrier of approximately 3.2 eV that prevents electrons in the silicon or polysilicon from entering SiO_2. At room temperature, electrons have enough kinetic energy that they have a small but significant probability of tunneling approximately 5 nm into the SiO_2. If the potential within a 5-nm range of the Si/SiO_2 interface is below +3.2 V (defining the Si potential as 0 V), then electrons that tunnel into the SiO_2 will always return to the Si and no current will flow. However, if the electric field in the SiO_2 is strong enough (> 3.2 V/5 nm $= 6.4 \times 10^8$ V/m), then the few electrons that tunnel 5 nm into the SiO_2 will be carried away by the electric field and there will be a small current of electrons away from the Si surface. Increasing the electric field decreases the distance the electrons have to tunnel initially and increases the electron current. From this simple view of Fowler–Nordheim tunneling, one concludes that a gate to diffusion voltage of about 25 V would be required to remove electrons from the gate given an oxide thickness of 40 nm. Note, the gate-oxide breakdown voltage for the process employed was approximately 28 V.

It is not the field in the bulk of the SiO_2 that matters, but only the field within 5 nm of the SiO_2 interface. By structuring the geometry of the electron emitting surface to increase the local electric field strength, electron currents can be induced at much lower voltages. An increase in electron current at low voltages has been observed in oxide grown on polysilicon and has been attributed to its surface features [20], [21]. This concept has been employed in commercial EEPROM's by deliberately introducing spikes or other nonuniformities, referred to as texture, on the upper surface of the bottom plate of a poly–poly tunneling structure [1]. Approximate analytical studies of the electric fields at the textured polysilicon surface reported an increase in field strength by a factor of 4 to 5 [2], [22].

One goal of this research was to avoid any specialized processing (e.g., textured polysilicon, ultrathin oxides) so that analog trim circuits could be integrated into standard analog CMOS designs. Therefore, lithographic features have been used to enhance the electric field instead of special processing. In the case of the prototype current injector, a polysilicon rectangle ends in the middle of an n^+ diffusion region (see Fig. 1). The electric field is concentrated at the corners of the poly rectangle, but its exact distribution is very complex and depends on the precise shape of the interface [23]; therefore, it is difficult to analytically predict the $I-V$ curves for the current injector. Experimental measurements indicate a field enhancement factor of between 2 and 4, which is less than that predicted for the textured polysilicon current injector [2], [22].

Fig. 2 shows the measured current of electrons being injected onto the floating gate as a function of the voltage difference between the n^+ region and the floating gate, and Fig. 3 shows the measured current of electrons being removed from the floating gate as a function of the voltage

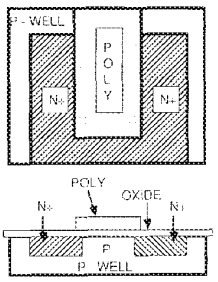


Fig. 1. Top and cross-sectional sketches of current injector structure.

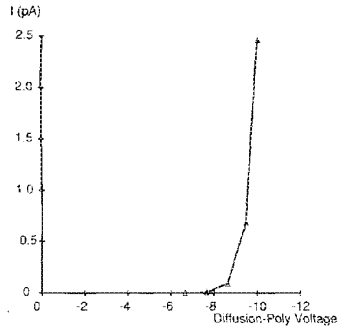


Fig. 2. Injecting electrons onto the floating gate. Plot shows electron current onto floating gate as a function of the voltage difference between the n^+ region and the gate.

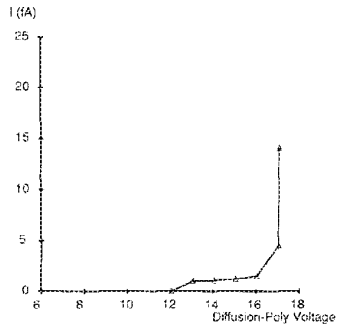


Fig. 3. Removing electrons from the floating gate. Plot shows electron current from the floating gate as a function of the voltage difference between the n^+ region and the gate.

difference between the n^+ region and the floating gate. Note that as long as neither the p-well–n^+ junction nor the p-well–substrate junction began avalanche breakdown, the p-well potential had no effect on the injected current. These $I-V$ characteristics were consistent to within 5 percent across four different dies from the same lot, eliminating the possibility that there was simply an oxide defect in the sample under test.

As expected, measurable tunneling currents occur at voltages considerably below the 28-V gate-oxide breakdown voltage. However, since the area of the gate that has

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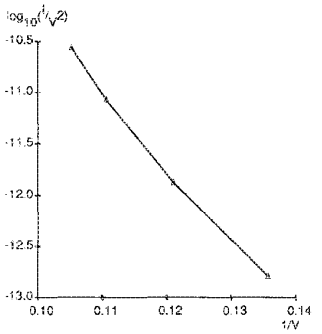


Fig. 4. Electron current onto the floating gate. A replot of $\log_{10}(I/V^2)$ versus $1/V$ for Fig. 2.

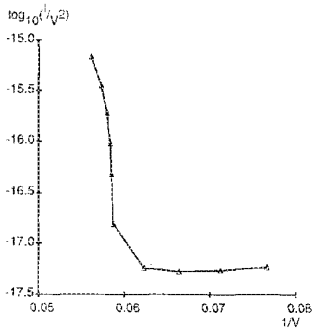


Fig. 5. Electron current from the floating gate. A replot of $\log_{10}(I/V^2)$ versus $1/V$ for Fig. 3.

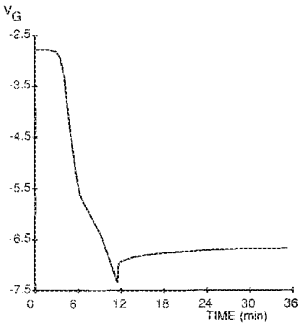


Fig. 6. Short-term stability of programmed voltage for the prototype. During the first 11 minutes the floating-gate voltage was driven 5-V negative and then the injector was turned off. The jump in voltage at 11 minutes was a result of the capacitive coupling between the injector and the gate. The short-term voltage shift was just the slow tail that starts after 12 minutes.

sufficient field strength to support tunneling currents is very small (just the corners), the currents associated with this form of tunneling are also extremely small. For example, a tunneling current of 1 fA with a capacitive load of 250 fF would result in a rate of change in floating-gate voltage of only 4 mV/s. A second, very important, characteristic is that there is a broad region (more than 3 V) over which the current injector acts approximately as a current source. This region is not due to a peculiarity in this particular lot, or even this particular fabrication process, because the shape of the $I-V$ curve for removing electrons from the floating gate of an earlier prototype fabricated by a different vendor in a 3-μm CMOS process [24] exhibited a very similar "current-source" region. The importance of this feature for the parallel trimming of analog circuits will be discussed further in Section IV.

A characteristic of Fowler–Nordheim tunneling is a very rapid increase in current with increasing applied voltage. Figs. 4 and 5 replot the data given in Figs. 2 and 3, respectively, as $\log_{10}(I/V^2)$ versus $1/V$. For classic Fowler–Nordheim tunneling, the measured points should fall along a straight line, which is approximately the case for Fig. 4. However, the measured characteristic for removing electrons from the floating gate, Figs. 3 and 5, shows only a slow increase in current with voltage between 13 and 16 V at which point the current increases dramatically. Above 16 V, the curve is approximately a straight line, but its slope is decreasing at higher voltages. This is consistent with field-enhanced Fowler–Nordheim tunneling currents [2]. It may be that another mechanism besides Fowler–Nordheim tunneling is responsible for the broad almost constant current region found in the $I-V$ characteristic for removing electrons from the floating gate (for other possibilities, see [17]).

III. Stability and Endurance of Analog Memory

There are several important physical properties of this type of memory device which must be considered during the design of an analog trim memory circuit. In this section, short-term stability characteristics, long-term stability characteristics, and the effects of repeated cycling will be considered

After inducing a voltage change at the floating gate, one observes that the gate tends to move back toward its original voltage over a period of several minutes (see Fig. 6). It has been speculated that this short-term drift is due to trap sites with long time constants near the SiO_2 interface settling to a new equilibrium. The size of the return appears to be proportional to the change in gate voltage induced [25]. The observed change was less than 1 percent of the change in gate voltage for the prototype, and was smaller for slower rates of change in the floating-gate voltage. If this error is unacceptable, it can be decreased at the system level by simply taking longer in the trimming process.

In terms of the stability of the charge placed on the floating gate, the prototype structure is comparable with existing thick polysilicon floating-gate EEPROM's [1], [26]. The rate of charge loss for the prototype was measured by performing 72-h retention tests at three different temperatures, with an initial floating-gate voltage of 1.5 V.

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Temperature	Exponential Charge Loss Rate
130°C	0.04 percent/day
160°C	1.2 percent/day
200°C	37 percent/day

Assuming that the retention characteristic at elevated temperatures is described by a thermionic emission model [9], [27]:

$$\frac{Q(t)}{Q(0)} = \exp\left(-t\nu\exp\left(-\frac{\Phi_B}{kT}\right)\right)$$

where Φ_B is the barrier height at the polysilicon–SiO_2 interface and ν is the dielectric relaxation frequency of electrons in the polysilicon. Fitting this model to the measured data gives Φ_B between 1.6 and 1.7 eV, and ν between 4.9×10^9 and 5.3×10^{10} s^{-1}, respectively. Although the value of Φ_B is substantially larger than the 1.0 to 1.3 eV typically found in EEPROM's using ultrathin tunneling oxides [9], [25], [27], it is consistent with the barrier height found in thick-oxide EEPROM's [26], [27]. Charge retention for the analog memory circuit is extremely good because it employs standard (thick) gate oxide rather than an ultrathin tunneling oxide. The expected charge loss would be less than 0.1 percent in ten years at operating and storage temperatures up to 100°C. Therefore precise analog trim voltages may be stored for the lifetime of many products.

The decrease in the charging and discharging current with repeated cycling which occurs in EEPROM's does not present a problem for the proposed analog memory circuit for two reasons. First, the trim voltage is typically set to one value and subsequent trimming operations only cause very small changes in that value. Second, by applying the charging or discharging current for a longer time, the same voltage change can be generated at the floating gate. In many trimming applications the duration of the trimming procedure is not a major stumbling block as there are usually only a few trims to be performed, relative to the size of an EEPROM, and in many cases they can all be performed in parallel.

IV. Design Example—Trimming Op Amp

Fig. 7 demonstrates one possible application of the analog memory circuit: in this case, to trim the input offset voltage of a simple two-stage Miller-compensated op amp whose input stage was integrated onto the same IC substrate as the trimming circuit. In order to guarantee that subtracting current from the drain of $M3$ can correct for input offset voltages of either sign, the equilibrium value of V_{GS7} is intentionally made smaller than the equilibrium value of V_{GS3}. This introduces an input offset, which is canceled out by current through $M5$, even when all devices match perfectly.

Trimming is performed by using the current injector to place charge on the gate of $M5$. The circuit operates in three modes: normal operation, erase mode, and trim mode. Trim mode is composed of two nonoverlapping

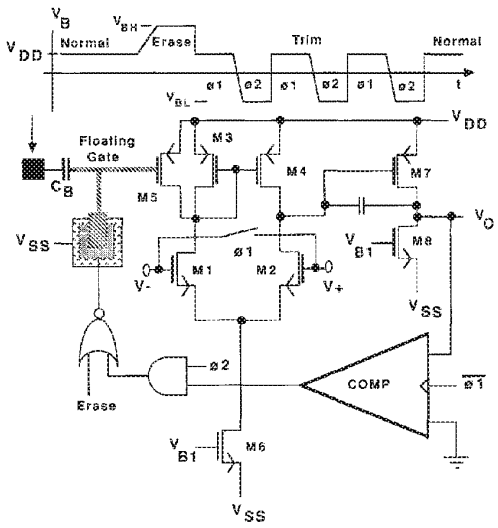


Fig. 7. Schematic diagram of a circuit to trim the offset of an operational amplifier.

clock phases. During normal operation, V_B and current injector are both tied to V_{DD} which prevents changes in the power supply voltage from capacitively coupling onto the gate of $M5$. This is important because the analog trim circuit is storing charge on the gate, not voltage. Therefore, a change in any signal with capacitance to the floating gate will result in a change in the voltage on the floating gate. Although the drain of $M5$ can move, its equilibrium voltage is held fixed during normal operation because the op amp is in a feedback loop.

To initiate a trimming cycle, the stored analog voltage must first be electrically erased. This is accomplished by connecting the current injector to V_{SS} and gradually raising V_B to V_{BH}, which is approximately 13–14 V. The slope of V_B versus t is chosen to limit the peak capacitive current through the injector to about 10 pA in order to prevent breakdown of the oxide. At the end of the erase cycle, with V_B returned to V_{DD}, the floating-gate voltage should be between 1 and 2 V. The bootstrap capacitor is necessary in order to control the voltage of the floating gate during both erase and trim modes. There is a trade-off between the amplitude of V_B required and the size of the bootstrap capacitor. In order to minimize the required programming voltages, the bootstrap capacitor should be significantly larger than the sum of the sense transistor's C_{GS} and the current injector's capacitance. In order to achieve a high capacitance per unit area and not impose significant limits on the programming voltage, the prototype used a poly-1/poly-2 capacitor, available in many analog CMOS processes, as the bootstrap capacitor. A diffusion-poly capacitor could be used instead, but would only be acceptable if the approximately ±14-V signals would not cause avalanche breakdown, either between the diffusion and the well, or between the well and the substrate. "Hot" electrons generated near the floating gate

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may be injected onto it resulting in an erroneous change in gate voltage. One potential generator of hot electrons is a large source-to-drain voltage on an NMOS sense transistor [25]. To prevent this, V_{DS} of the sense transistor should be kept small, or a PMOS sense transistor should be used. One final alternative, available in any CMOS process, is a poly, field oxide, metal capacitor. However, since the capacitance/unit area is quite low, this would be quite inefficient in terms of area. Note that the programming voltage may be above the field threshold, therefore care must be taken in routing the programming voltage to the bootstrap capacitors.

In the trim mode, a precise analog voltage is established on the floating gate. After the erase cycle, the magnitude of V_{GS5} is larger than that needed to make the op-amp input offset voltage zero. The magnitude of V_{GS5} is decreased by slowly removing electrons from the floating gate in a two-cycle process. During each ϕ_1 clock phase, the input of the op amp is shorted, and at the end of ϕ_1, the sign of the op-amp output is latched by the comparator. During ϕ_2, if the output of the op amp is above analog ground (nominally 2.5 V for the prototype), then electrons are removed from the floating gate using the current injector. V_{BL} is chosen so that with the current injector at V_{DD} (nominally 5V) the floating gate will be driven to between -8 and -11 V, which is the region in which the injector acts as a current source of about 1 fA. Note that the falling slope of ϕ_2 is chosen to limit the current through the injector if the difference between the floating-gate voltage and V_{DD} is above 16 V. The change in the voltage on the floating gate during each ϕ_2 clock period is given by $I/C \times \Delta t$. In the case of the prototype, the total capacitance at the floating gate was about 1 pF, and the duration of ϕ_2 was 0.01 s; hence the change in the floating-gate voltage was 10 μV. There is trade-off between the resolution for programming the floating-gate voltage and the total time required for trimming. If C_B is increased, the resolution will be finer, but a longer total time will be required for trimming. In the case of the prototype, the worst-case trimming would be if $M5$ must be turned almost completely off, which is a change in floating-gate voltage of at most 3 V. At 1 mV/s, the worst-case trimming time would be almost 50 min.

When the output of the op amp drops below analog ground, then the desired programming voltage has been reached, and no more electrons should be removed from the floating gate. Since many devices may be undergoing simultaneous trimming, rather than end the trim period, the current injector is tied to V_{SS} during all subsequent ϕ_2's. The voltage across the current injector is then safely below the point at which any current will flow.

The input offset voltage of a CMOS op amp was reduced from its initial value of 10 mV to below 0.5 mV by using the analog trim memory in this circuit to control a current source injected at the output of the op amp differential pair. The effect of temperature variations has been characterized by a series of simulations, in each of which a specific element mismatch has been introduced. For the prototype op amp, the worst-case trim variations with temperature were caused by mismatch in V_T of $M1$ and $M2$. Fig. 8 shows the variation of input offset voltage with temperature, after trimming at 25°C, for a V_T mismatch of +5 mV, −5 mV, and the actual variation for the prototype. The relatively poor temperature stability of this circuit is, in part, a result of initially imbalancing the input stage of the op amp in order to guarantee that the current through $M5$ could bring the input offset to zero.

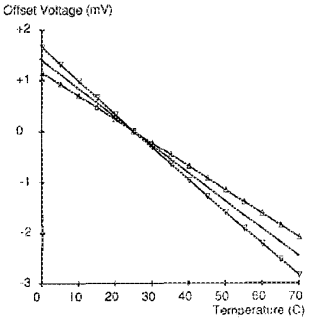


Fig. 8. Input offset voltage of op amp versus temperature. The Δ points are simulations with a +5-mV difference between V_{T1} and V_{T2}. The * points are measurements from the prototype trimming circuit. The ▽ points are simulations with a −5-mV difference between V_{T1} and V_{T2}.

The example circuit presented in this section is by no means the best way to employ the analog trim memory circuit. An analog trimming circuit that exhibits much better temperature stability has been reported by Säckinger and Guggenbühl [25]. Their trim circuit uses an analog trim voltage to divide a reference current through a differential pair and then to generate a differential trimming current. Although their circuit used ultrathin tunneling oxides, and hence required special fabrication techniques, the idea of generating a differential trim current could be used with the current injector proposed herein as well. Besides requiring special fabrication techniques, ultrathin tunneling oxides only allow control of the analog voltage via adjustment of the programming voltage (V_B in this case). Thus, it is not clear that multiple analog trim circuits using ultrathin tunneling oxides could be simultaneously adjusted.

V. Application Areas

There are several salient features that constrain the possible applications of the proposed analog memory circuit:

- trim circuits can be implemented in a standard CMOS process;
- trim rates are slow—typically 1–10 mV/s change in floating-gate voltage;
- many trims can be performed in parallel;
- drift rates are extremely low, less than 0.1 percent/decade below 100°C.

The most obvious trimming area is the adjustment of the input offset voltage of MOS differential pairs of the type

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used in most op amps and comparators. An example of this type of application was given in the previous section. Since both op amps and comparators are inherently amplifiers, it is easy to generate the decisions about which direction to drive the floating gate during the trimming process.

A second potentially important area for application of this analog memory circuit is element trimming for data converters. A novel dynamic method was recently presented to trim the difference between MOS current sources used to implement a low-power digital audio D/A converter [29]. One drawback of this scheme was that it generated a tone at the trimming rate which appeared in the audio band. By using analog trim memory cells, one per current source, and trimming the D/A converter either once at the factory or every time the power is applied, the tone in the audio band could be eliminated. Note, this trim cell is not a panacea for data converters as one cannot easily use a trim current to adjust the values of resistors in an R-2R ladder; i.e., this approach is only applicable to some converter topologies.

This analog trim memory circuit may or may not be appropriate for applications requiring a continuous adaptation of trim values. It would depend on whether the slow trimming rate of this analog memory is acceptable. One example where only small changes in the analog memory value is desirable is programmable neural networks where the learning algorithms often demand extremely small changes in tap weights per decision cycle. A circuit for applying analog storage to neural-network tap weight generation has been proposed in [25]. However, since the analog trim circuit proposed in this paper can only take small positive steps and negative steps are equivalent to full erasure, it may only be applicable for a limited class of learning algorithms.

Another possible application area for the analog memory circuit is adaptive filters, for example, the echo canceling filters used in modems, or the equalizing filters used in magnetic recording channels. However, the appropriateness of these applications will again depend on the rate at which the coefficients, which are stored as analog trim voltages, must be changed.

VI. Conclusions

A current injector structure has been presented which can be incorporated into a standard CMOS process and which acts as a long-term analog memory element. It does not require any special processing steps, nor special tunneling oxides. Instead, it relies on geometric factors to lower the necessary programming voltage at which field-enhanced Fowler–Nordheim tunneling occurs. The primary limitation of the analog memory circuit is that the achievable rates of change of floating-gate voltage are small, 1–10 mV/s. A general method for trimming any number of analog memories independently and simultaneously has also been presented. Two different geometries, fabricated by two different vendors, confirm the generality of the broad constant current-source region upon which this parallel operation relies. Parallel trimming is performed by applying a nonstandard voltage to only the bootstrap capacitors; all other parts of the analog trim circuit operate within the normal power supply range. This trimming strategy was used to reduce the offset voltage of a simple op amp from 10 mV to less than 0.5 mV.

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He has worked for M.I.T.'s Lincoln Laboratories and has acted as a consultant in the area of analog circuit design and design automation for Analog Devices and Hughes Aircraft among others. In 1984 he joined Carnegie Mellon University, Pittsburgh, PA, where he is currently an Associate Professor of Electrical and Computer Engineering. His research is in the area of analysis, design, automatic synthesis, and simulation of mixed analog/digital systems.

Dr. Carley received a National Science Foundation Presidential Young Investigator Award in 1985, and a Best Paper Award at the 1987 Design Automation Conference.

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Cypress Semiconductor
Product Qualification Report

QTP# 043004 VERSION 2.0
March 2007

DDR2-PLL Device Family C8Q-3R, Fab 4	
CY2SSTU877	**1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Mira Ben-Tzur
Quality Engineering Director
(408) 943-2675

Fredrick Whitwer
Principal Reliability Engineer
(408) 943-2722

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
042106	7C82877A DDR2 PLL New Device family on New C8Q-3R Technology, Fab4	Jan 05
050305	7C82877B DDR2 PLL All Layer Independent Mask Set on C8Q-3RQ Technology, Fab4	Mar 05
043004	Qualify Active Under Pad (AUP) for the CMI C8Q-3R Technology using DDR2 PLL Product	Nov 05

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualify Active Under Pad (AUP) for CMI C8Q-3R Technology using DDR2 PLL Product	
Marketing Part #:	CY2SSTU877
Device Description:	1.8V, Commercial/Industrial, available in 52-Ball VFBGA
Cypress Division:	Cypress Semiconductor Corporation – Consumer & Computation Division

TECHNOLOGY/FAB PROCESS DESCRIPTION C8Q-3R			
Number of Metal Layers:	4	Metal Composition:	Metal 1: 100A Ti/3,200A Al 0.5% Cu /300A TiW Metal 2: 150A Ti/4,230A Al 0.5% Cu/300A TiW Metal 3: 150A Ti/4,230A Al 0.5% Cu/300A TiW Metal 4: 150A Ti/8,000A Al 0.5% Cu/300A TiW
Passivation Type and Materials:			1,000A TEOs / 9,000A Si_3N_4
Generic Process Technology/Design Rule (μ-drawn):			CMOS, 0.13 μm
Gate Oxide Material/Thickness (MOS):			SiO_2 DGOX 32/55A
Name/Location of Die Fab (prime) Facility:			CMI/Bloomington MN
Die Fab Line ID/Wafer Process ID:			Fab4, C8Q-3R

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
52-Ball FBGA	**ASE-Taiwan (G)**

Note: Package Qualification details upon request.

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BV52
Package Outline, Type, or Name:	52-Ball Fine Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	KMC211AA
Mold Compound Flammability Rating:	UL94 V-O
Oxygen Rating Index:	34
Lead Frame Designation:	NA
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	SnPb
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Saw
Die Attach Supplier:	Ablebond
Die Attach Material:	8355F
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-05821
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0mil
Thermal Resistance Theta JA °C/W:	80°C/W
Package Cross Section Yes/No:	No
Assembly Process Flow:	49-41023
Name/Location of Assembly (prime) facility:	ASE-TAIWAN (TAIWN-G)
MSL Level	3
Reflow Profile	220C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R, CY WA

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max=3.8V, 125°C Dynamic Operating Condition, Vcc Max=2.35V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=3.8V, 125°C Dynamic Operating Condition, Vcc Max=2.35V, 125°C	P
Long Life Verification	Dynamic Operating Condition, Vcc Max=3.8V, 125°C	P
Low Temperature Operating Life	-30C, 4.3V	P
High Temperature Steady State life	125°C, 3.63V, Vcc Max	P
High Accelerated Saturation Test (HAST)	130°C, 1.8V/2.35V/3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C	P
Pressure Cooker	121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22, Method A114-B	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Age Bond Strength	200C, 4hrs MIL-STD-883, Method 883-2011	P
Ball Shear	Cypress Spec. 24-00018	P
Acoustic Microscopy	Cypress Spec. 25-00104	P
High Temperature Storage	150°C, no bias	P
Dynamic Latch up	125°C, 6.5V	P
Latch up Sensitivity	125C, ± 300mA Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	3,058 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	651,888 DHRs	0	0 .7	55	25 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2}-\frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 042106

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY68013A (7C681000A)	4416666	*610434406*	TAIWN-G	COMP	17	0	
CY2SSTU877 (7C87741A)	4416666B	*H20592*	TAIWN-G	COMP	16	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	COMP	17	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	COMP	16	0	
STRESS: AGE BOND STRENGTH							
CY68013A (7C681000A)	4416666	*610434406*	TAIWN-G	COMP	5	0	
CY68013A (7C682001A)	4416701	*610437657*	TAIWN-G	COMP	5	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	COMP	3	0	
STRESS: BALL SHEAR							
CY68013A (7C682001A)	4416701	*610437657*	TAIWN-G	COMP	5	0	
STRESS: DYNAMIC LATCH-UP TESTING (6.9V)							
CY68013A (7C682001A)	4416701	*610437657*	TAIWN-G	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY68013A (7C682001A)	4416666	*610437607*	TAIWN-G	COMP	9	0	
CY68013A (7C682000A)	4416666	*610437102*	TAIWN-G	COMP	9	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	COMP	9	0	
CY68013A (7C682000A)	4416701	*610437702*	TAIWN-G	COMP	9	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2200V							
CY68013A (7C682001A)	4416666	*610437607*	TAIWN-G	COMP	9	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	COMP	9	0	
CY2SSTU877 (7C82877A)	4413035	*H19747*	TAIWN-G	COMP	9	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2200V							
CY68013A (7C682001A)	4416666	*610437607*	TAIWN-G	COMP	3	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C82877A)	4413035	*H19747*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	COMP	3	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)							
CY68013A (7C682005A)	4416701	*610438121*	TAIWN-G	80	80	0	
CY68013A (7C682005A)	4416701	*610438121*	TAIWN-G	168	80	0	

Reliability Test Data

QTP #: 042106

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 3.8V, Vcc Max)							
CY68013A (7C682001A)	4416666	*610437607*	TAIWN-G	96	499	0	
CY68013A (7C682005A)	4417143	*610443845*	TAIWN-G	96	514	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (125C, 3.8V, Vcc Max)							
CY68013A (7C682001A)	4416666	*610437607*	TAIWN-G	168	200	0	
CY68013A (7C682001A)	4416666	*610437607*	TAIWN-G	1000	194	0	
CY68013A (7C682005A)	4417143	*610443845*	TAIWN-G	168	208	0	
CY68013A (7C682005A)	4417143	*610443845*	TAIWN-G	1000	208	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 2.35V, Vcc Max)							
CY2SSTU877 (7C87741A)	4416666B	*H20592*	TAIWN-G	96	276	0	
CY2SSTU877 (7C82877A)	4416701	*H20501*	TAIWN-G	96	126	0	
CY2SSTU877 (7C87741A)	4416701	*H20500*	TAIWN-G	96	89	0	
CY2SSTU877 (7C87740A)	4416791B	*H20536*	TAIWN-G	96	169	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	96	304	0	
CY2SSTU877 (7C87741A)	4419587	*H20650*	TAIWN-G	96	500	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (125C, 3.8V, Vcc Max)							
CY2SSTU877 (7C87741A)	4416666B	*H20592*	TAIWN-G	1000	253	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	168	150	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	1000	150	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 3.63V), PRE COND 192 HR, 30C/60%RH, MSL3							
CY68013A (7C682001A)	4416666	*610437607*	TAIWN-G	128	47	0	
CY68013A (7C682001A)	4416666	*610437607*	TAIWN-G	256	47	0	
CY68013A (7C682000A)	4416701	*610437702*	TAIWN-G	128	47	0	
CY68013A (7C682000A)	4416701	*610437702*	TAIWN-G	256	45	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 1.8V), PRE COND 192 HR, 30C/60%RH, MSL3							
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	128	43	0	
STRESS: LOW TEMPERATURE OPERATING LIFE (-30C, 4.3V)							
CY68013A (7C682005A)	4416701	*610438121*	TAIWN-G	500	80	0	
STRESS: STATIC LATCH-UP TESTING (125C, 5.5V, ±300mA)							
CY2SSTU877 (7C82877A)	4413035	*H19747*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	COMP	3	0	

Reliability Test Data

QTP #: 042106

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: STATIC LATCH-UP TESTING (125C, 6.5V, ±300mA)							
CY68013A (7C682001A)	4416666	*610437607*	TAIWN-G	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING (125C, 7.5V, ±300mA)							
CY68013A (7C682001A)	4416701	*610437657*	TAIWN-G	COMP	3	0	
STRESS: HIGH TEMPERATURE STORAGE, 150C, no bias							
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	500	50	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	1000	50	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	500	45	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	1000	45	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH), 15 Psig, PRE COND 192 HR, 30C/60%RH, MSL3							
CY68013A (7C681000A)	4416666	*610434406*	TAIWN-G	168	50	0	
CY68013A (7C681000A)	4416666	*610434406*	TAIWN-G	288	50	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	168	50	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	288	50	0	
CY2SSTU877 (7C82877A)	4413035	*H19747*	TAIWN-G	168	47	0	
CY2SSTU877 (7C82877A)	4413035	*H19747*	TAIWN-G	288	47	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	168	45	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	288	45	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS, 30C/60%RH, MSL3							
CY68013A (7C681000A)	4416666	*610434406*	TAIWN-G	300	50	0	
CY68013A (7C681000A)	4416666	*610434406*	TAIWN-G	500	50	0	
CY68013A (7C681000A)	4416666	*610434406*	TAIWN-G	1000	50	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	168	50	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	500	50	0	
CY68013A (7C681000A)	4416701	*610434407/8*	TAIWN-G	1000	50	0	
CY2SSTU877 (7C82877A)	4413035	*H19747*	TAIWN-G	300	46	0	
CY2SSTU877 (7C82877A)	4413035	*H19747*	TAIWN-G	500	45	0	
CY2SSTU877 (7C82877A)	4413035	*H19747*	TAIWN-G	1000	45	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	300	45	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	500	45	0	
CY2SSTU877 (7C87740A)	4417143	*H20549*	TAIWN-G	1000	45	0	

Reliability Test Data

QTP #: 050305

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY2SSTU877BVXC (7C828771B)	4448054	*610501198*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2200V							
CY2SSTU877BVXC (7C828771B)	4448054	*610501198*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2200V							
CY2SSTU877BVXC (7C828771B)	4448054	*610501198*	TAIWN-G	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 2.35V, Vcc Max)							
CY2SSTU877BVXC (7C828771B)	4448054	*610501198*	TAIWN-G	96	1018	0	
STRESS: STATIC LATCH-UP TESTING (125C, 6.5V, ±300mA)							
CY2SSTU877BVXC (7C828771B)	4448054	*610501198*	TAIWN-G	COMP	3	0	

Reliability Test Data

QTP #: 043004

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	COMP	16	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	COMP	16	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	COMP	15	0	
CY2SSTU877 (7C87741A)	4423798	*H20619*	TAIWN-G	COMP	15	0	
CY2SSTU877 (7C87741A)	4419587	*H20650*	TAIWN-G	COMP	16	0	
CY2SSTU877 (7C87741A)	4419587	*H20649*	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87741A)	4419587	*H20650*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87741A)	4419587	*H20649*	TAIWN-G	COMP	3	0	
STRESS: BOND PULL							
CY2SSTU877 (7C87741A)	4423798	*H20619*	TAIWN-G	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2200V							
CY2SSTU877 (7C87740A)	4416701	*H20499*	TAIWN-G	COMP	9	0	
CY2SSTU877 (7C87741A)	4416701	*H20500*	TAIWN-G	COMP	9	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	COMP	9	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2200V							
CY2SSTU877 (7C87740A)	4416701	*H20499*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87741A)	4416701	*H20500*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	COMP	3	0	

Reliability Test Data

QTP #: 043004

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 2.35V, Vcc Max)							
CY2SSTU877 (7C87741A)	4416701	*H20500*	TAIWN-G	96	89	0	
CY2SSTU877 (7C87742A)	4416666	*H20591*	TAIWN-G	96	134	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	96	276	0	
CY2SSTU877 (7C87740A)	4416791B	*H20536*	TAIWN-G	96	69	0	
CY2SSTU877 (7C87741A)	4417143	*H20548*	TAIWN-G	96	175	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	96	304	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	96	406	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	96	434	0	
CY2SSTU877 (7C87741A)	4423798	*H20619*	TAIWN-G	96	671	0	
CY2SSTU877 (7C87741A)	4419587	*H20650*	TAIWN-G	96	500	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (125C, 2.35V, Vcc Max)							
CY2SSTU877 (7C87740A)	4416791B	*H20536*	TAIWN-G	168	166	0	
CY2SSTU877 (7C87741A)	4417143	*H20548*	TAIWN-G	168	175	0	
CY2SSTU877 (7C87741A)	4417143	*H20548*	TAIWN-G	1000	175	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	1000	196	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	1000	253	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 1.8V), PRE COND 192 HR, 30C/60%RH, MSL3							
CY2SSTU877 (7C87742A)	4416666	*H20591*	TAIWN-G	128	46	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	128	43	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 2.35V), PRE COND 192 HR, 30C/60%RH, MSL3							
CY2SSTU877 (7C87741A)	4416666	*H19775*	TAIWN-G	128	46	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	128	45	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	128	46	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	128	46	0	

Reliability Test Data

QTP #: 043004

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMPERATURE STORAGE, 150C, no bias							
CY2SSTU877 (7C87740A)	4416701	*H20499*	TAIWN-G	500	47	0	
CY2SSTU877 (7C87740A)	4416701	*H20499*	TAIWN-G	1000	46	0	
CY2SSTU877 (7C87742A)	4413035	*H19746*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87742A)	4413035	*H19746*	TAIWN-G	1000	46	0	
CY2SSTU877 (7C87742A)	4416666	*H20591*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87742A)	4416666	*H20591*	TAIWN-G	1000	46	0	
CY2SSTU877 (7C87741A)	4416666	*H19775*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87741A)	4416666	*H19775*	TAIWN-G	1000	46	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	500	45	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	1000	45	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	1000	46	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	1000	46	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	1000	46	0	
STRESS: STATIC LATCH-UP TESTING (125C, 5.5V, ±300mA)							
CY2SSTU877 (7C87740A)	4416701	*H20499*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87741A)	4416701	*H20500*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	COMP	3	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	COMP	3	0	

Reliability Test Data

QTP #: 043004

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS, 30C/60%RH, MSL3							
CY2SSTU877 (7C87740A)	4416701	*H20499*	TAIWN-G	300	46	0	
CY2SSTU877 (7C87740A)	4416701	*H20499*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87742A)	4413035	*H19746*	TAIWN-G	300	47	0	
CY2SSTU877 (7C87742A)	4413035	*H19746*	TAIWN-G	500	47	0	
CY2SSTU877 (7C87742A)	4413035	*H19746*	TAIWN-G	1000	47	0	
CY2SSTU877 (7C87742A)	4416666	*H20591*	TAIWN-G	300	46	0	
CY2SSTU877 (7C87742A)	4416666	*H20591*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87741A)	4416666	*H19775*	TAIWN-G	300	47	0	
CY2SSTU877 (7C87741A)	4416666	*H19775*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87741A)	4416666	*H19775*	TAIWN-G	1000	46	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	300	46	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	300	46	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	500	45	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	300	46	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	1000	46	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	300	46	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	500	46	0	
CY2SSTU877 (7C87741A)	4423798	*H20619*	TAIWN-G	300	347	0	
CY2SSTU877 (7C87741A)	4423798	*H20619*	TAIWN-G	500	346	0	
CY2SSTU877 (7C87741A)	4423798	*H20619*	TAIWN-G	1000	346	0	
CY2SSTU877 (7C87741A)	4419587	*H20650*	TAIWN-G	300	348	0	
CY2SSTU877 (7C87741A)	4419587	*H20650*	TAIWN-G	500	348	0	
CY2SSTU877 (7C87741A)	4419587	*H20650*	TAIWN-G	1000	348	0	

Reliability Test Data

QTP #: 043004

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRESSURE COOKER TEST (121C, 100%RH), 15, Psig, PRE COND 192 HR, 30C/60%RH, MSL3							
CY2SSTU877 (7C87740A)	4416701	*H20499*	TAIWN-G	168	47	0	
CY2SSTU877 (7C87740A)	4416701	*H20499*	TAIWN-G	288	47	0	
CY2SSTU877 (7C87742A)	4413035	*H19746*	TAIWN-G	168	46	0	
CY2SSTU877 (7C87742A)	4413035	*H19746*	TAIWN-G	288	46	0	
CY2SSTU877 (7C87742A)	4416666	*H20591*	TAIWN-G	168	46	0	
CY2SSTU877 (7C87742A)	4416666	*H20591*	TAIWN-G	288	46	0	
CY2SSTU877 (7C87741A)	4416666	*H19775*	TAIWN-G	168	47	0	
CY2SSTU877 (7C87741A)	4416666	*H19775*	TAIWN-G	288	47	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	168	46	0	
CY2SSTU877 (7C87741A)	4416666B	*H20591*	TAIWN-G	288	46	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	168	46	0	
CY2SSTU877 (7C87741A)	4417975	*H20583*	TAIWN-G	288	46	0	
CY2SSTU877 (7C87742A)	4417975	*H20585*	TAIWN-G	240	45	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	168	46	0	
CY2SSTU877 (7C87742A)	4423798	*H20626*	TAIWN-G	288	46	0	



10 Gigabit Ethernet Technology Overview White Paper

May, 2001
Revision 1.0

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Executive Summary

From its origin more than 25 years ago, Ethernet has evolved to meet the increasing demands of packet-switched networks. Due to its proven low implementation cost, its known reliability, and relative simplicity of installation and maintenance, its popularity has grown to the point that today nearly all traffic on the Internet originates or ends with an Ethernet connection. Further, as the demand for ever-faster network speeds has grown, Ethernet has been adapted to handle these higher speeds and the concomitant surges in volume demand that accompany them.

The One Gigabit Ethernet standard is already being deployed in large numbers in both corporate and public data networks, and has begun to move Ethernet from the realm of the local area network out to encompass the metro area network. Meanwhile, an even faster 10 Gigabit Ethernet standard is nearing completion. This latest standard is being driven not only by the increase in normal data traffic but also by the proliferation of new, bandwidth-intensive applications, including motion video.

The draft standard for 10 Gigabit Ethernet is significantly different in some respects from earlier Ethernet standards, primarily in that it will only function over optical fiber, and only operate in full-duplex mode, meaning that collision detection protocols are unnecessary. Because of these characteristics, Ethernet can now step up to 10 gigabits per second, however, it remains Ethernet, including the packet format, and the current capabilities are easily transferable to the new draft standard.

In addition, 10 Gigabit Ethernet does not obsolete current investments in network infrastructure. The task force heading the standards effort has taken pains to see that 10 Gigabit Ethernet is interoperable with other networking technologies such as SONET and has carefully added technology to the standard to enable Ethernet packets to travel across SONET links with very little inefficiency.

Ethernet's expansion for use in metro area networks can now be expanded yet again onto wide area networks, both in concert with SONET and also end-to-end Ethernet. With the current balance of network traffic today heavily favoring packet-switched data over voice, it is expected that the new 10 Gigabit Ethernet standard will help to create a convergence between networks designed primarily for voice, and the new data centric networks.

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Introduction

This white paper is designed to provide a general discussion of the impending 10 Gigabit Ethernet standard to the technical reader. The draft 10 Gigabit standard is currently on track to be adopted in mid-2002.

This paper is sponsored by the 10 Gigabit Ethernet Alliance – a group of vendor companies interested in promoting the forthcoming standard. It begins with a brief history of the technology, and describes what the alliance is and its purposes. The paper then proceeds to present a description of the IEEE standards process, followed by the proposed standard itself, as it now stands, in a moderate level of technical detail. It concludes with a set of short discussions on how 10 Gigabit Ethernet may be used in various high-level applications scenarios.

A Brief History of Ethernet

In 1973, researchers at Xerox's Palo Alto Research Center, principally Robert Metcalfe and David Boggs, developed Ethernet as a technology for interconnecting the lab's Xerox Altos, early graphical personal computers also developed at PARC. Ethernet's clock was derived from the Alto's system clock, resulting in an initial data transmission rate of 2.94 Mbps. Metcalfe named the technology "Ethernet," choosing the word "ether" to describe the physical medium -- a cable -- that carries bits to all nodes in the network. Figure 1 shows a drawing by Metcalfe that illustrates the simplicity of the PARC researchers' design.

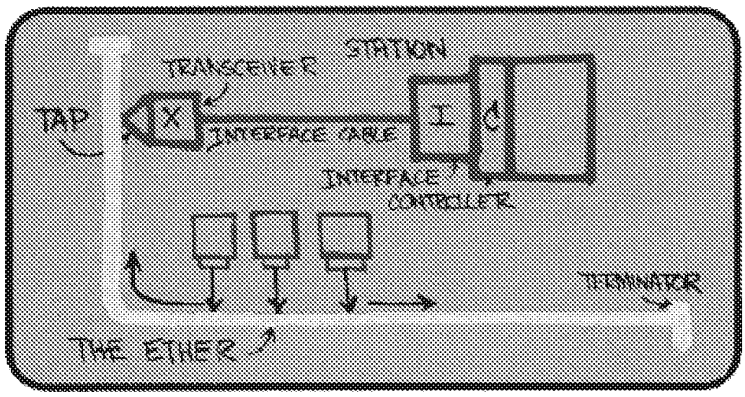


Figure 1. Robert Metcalfe's drawing of the first Ethernet design.

Metcalfe also posited a theorem about the growing importance of networks. Now known as "Metcalfe's Law," he predicted that the value of the network expands exponentially as the number of users increases. Not only was he correct about technological networks, his "law" has since also been successfully applied to the field of economics.

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In some respects, Metcalfe's Law is similar to "Moore's Law." Coined from statements made by Intel co-founder Gordon Moore sometime in the 1970s, Moore's Law predicts that every 18 months the power of microprocessors will double while the price falls by half. Since Ethernet's introduction, both "laws" have proven themselves, with dramatic growth in large part due to the successful combination of Ethernet with the microprocessor.

As the speed of Ethernet has increased, first to 10 million bits per second (Mbps), then to 100 Mbps, and recently to 1 billion bits per second or 1 gigabit (Gbps), the price of Ethernet technology has also plummeted thanks to Moore's Law and manufacturing economies of scale. Likewise, networks became exponentially more valuable as the number of users swelled to hundreds of millions – thanks to Metcalfe's Law. Ethernet has become the dominant network technology in local area networks (LAN). And with the advent of Gigabit Ethernet, it has started to make substantial inroads into metro area networks (MAN).

Additionally, the volume of data communications traffic has grown to where, today, it outweighs circuit-switched voice traffic four to one. Eighty-percent of all network traffic is now data rather than voice.

The technology exists to take Ethernet to the next level. The time is ripe for establishing a standard that moves the goal posts for 10 Gbps further into metro area networks (MAN) and, ultimately, into wide area networks (WAN) as well. This move, we believe, will ultimately bring about a convergence in voice and data networks, while still retaining compatibility with existing Ethernet technologies – thus assuring the safety of investments that customers and service providers have already made.

The 10 Gigabit Ethernet Project

The purpose of the 10 Gigabit Ethernet proposed standard is to extend the 802.3 protocols to an operating speed of 10 Gbps and to expand the Ethernet application space to include WAN links. This will provide for a significant increase in bandwidth while maintaining maximum compatibility with the installed base of 802.3 interfaces, previous investment in research and development, and principles of network operation and management.

In order to be adopted as a standard, the IEEE's 802.3ae Task Force has established five criteria that the new 10 Gigabit Ethernet P (proposed) standard must meet:

- It must have broad market potential, supporting a broad set of applications, with multiple vendors supporting it, and multiple classes of customers.
- It must be compatible with other existing 802.3 protocol standards, as well as with both Open Systems Interconnection (OSI) and Simple Network Management Protocol (SNMP) management specifications.
- It must be substantially different from other 802.3 standards, making it a unique solution for a problem rather than an alternative solution.
- It must have demonstrated technical feasibility prior to final ratification.

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- It must be economically feasible for customers to deploy, providing reasonable cost, including all installation and management costs, for the expected performance increase.

For a more complete discussion of the five criteria for 802.3ae, see: http://grouper.ieee.org/groups/802/3/ae/criteria.pdf.

The 10 Gigabit Ethernet Alliance

The 10 Gigabit Ethernet Alliance (10GEA) was established in order to promote standards-based 10 Gigabit Ethernet technology and to encourage the use and implementation of 10 Gigabit Ethernet as a key networking technology for connecting various computing, data and telecommunications devices.

The charter of the 10 Gigabit Ethernet Alliance includes:

- Supporting the 10 Gigabit Ethernet standards effort conducted in the IEEE 802.3 working group
- Contributing resources to facilitate convergence and consensus on technical specifications
- Promoting industry awareness, acceptance, and advancement of the 10 Gigabit Ethernet standard
- Accelerating the adoption and usage of 10 Gigabit Ethernet products and services
- Providing resources to establish and demonstrate multi-vendor interoperability and generally encourage and promote interoperability and interoperability events
- Fostering communications between suppliers and users of 10 Gigabit Ethernet technology and products

Further information about the 10GEA can be found at: www.10gea.org.

10GEA Membership

The 10 Gigabit Ethernet Alliance was organized to facilitate and accelerate the introduction of 10 Gigabit Ethernet into the networking market. It was founded by networking industry leaders 3Com, Cisco Systems, Extreme Networks, Intel, Nortel Networks, Sun Microsystems, and World Wide Packets. In addition, the 10GEA supports the activities of the IEEE 802.3ae (10 Gigabit) Task Force, fosters the development of the 802.3ae (10 Gigabit Ethernet) standard, and promotes interoperability among 10 Gigabit Ethernet products. Currently, the 10GEA has a membership of over 100 companies, and a listing of those companies can be found at: http://www.10gea.org/about_companies.htm.

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Standards Activities

The Institute of Electrical and Electronics Engineers (IEEE) was founded in order to foster the development of standards in all fields of science and technology within the organization's scope. A key principle throughout the standards process is consensus among the participants. The IEEE-SA (Standards Association) and its Standards Board oversee the process of standards formation through two committees. (See Figure 2.)

The New Standards Committee (NesCom) ensures that proposed standards fall within the IEEE's scope, that they are assigned to the correct technical committees, and that the makeup of working groups, etc,. fairly represents all interested parties. It also examines Project Authorization Requests (PAR) and recommends to the IEEE-SA Standards Board whether to approve them. The second committee, the Standards Review Committee (RevCom), examines proposed new and revised standards, ensures that such proposals represent a consensus of the members of the IEEE Sponsor balloting group, and makes recommendations to the Standards Board as to whether or not to approve a standard.

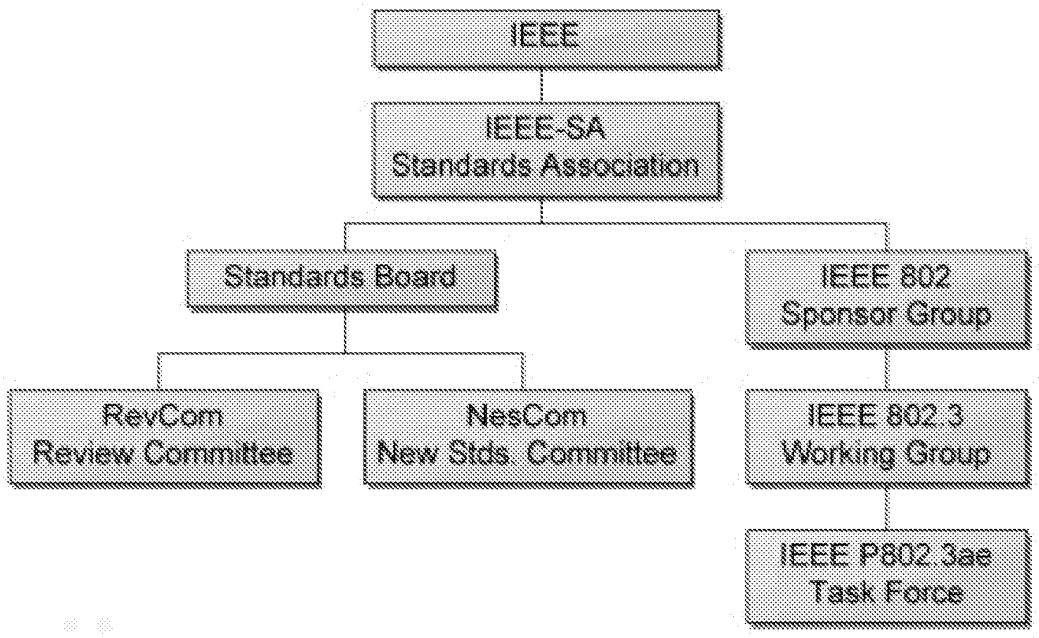


Figure 2. The IEEE groups involved in creating the 10 Gbps Ethernet standard.

Standards Process Flow

A new standard begins with a "sponsor" – a technical society or committee within the IEEE that agrees to provide oversight during the standards development process. This begins with a "call for interest" and formation of a sponsor's "study group." The next step is to submit a Project Authorization Request to NesCom. Upon approval of the PAR by the committee, a "working group" comprised of interested parties is formed. Approval of the

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PAR also starts the clock ticking. The proposed standard must be completed within four years.

The working group plans meetings and organizes the work that needs to be done to create the standard. When the task of defining a new standard is very large and/or complex, the working group will form a "task force" of people with more specialized skills to work on various aspects of the standard. Once a draft of the standard is complete, the working group will vote on it. (See Figure 3.) After the working group has passed the draft standard, the sponsoring group then circulates it for a vote – a process called "sponsor balloting."

The members of the sponsoring committee or group will then vote. In both ballots, 75% of the ballots sent out must be returned and, of those, 75% must be in favor of adopting the standard. Comments from voting members will also be incorporated into the final standards document. Finally, the IEEE-SA Standards Board must approve the final draft before its publication as a formal standard.

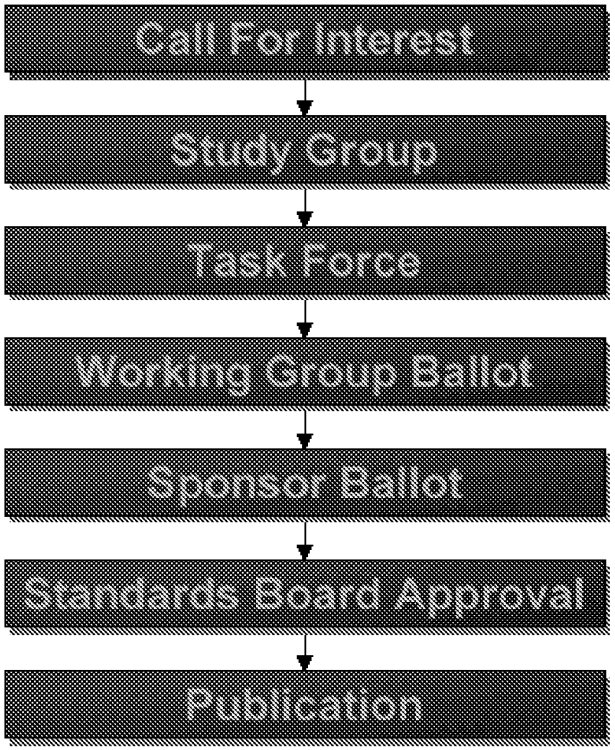


Figure 3. Flow chart showing the IEEE standards process.

For further information on the IEEE standards process, see:

IEEE
IEEE 802 LAN/MAN Standards Committee

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IEEE 802.3 CSMA/CD (ETHERNET)
IEEE P802.3ae 10Gb/s Ethernet Task Force
http://standards.ieee.org/resources/glance.html

Timetable

Figure 4 illustrates the current timetable for the 802.3ae standards process.

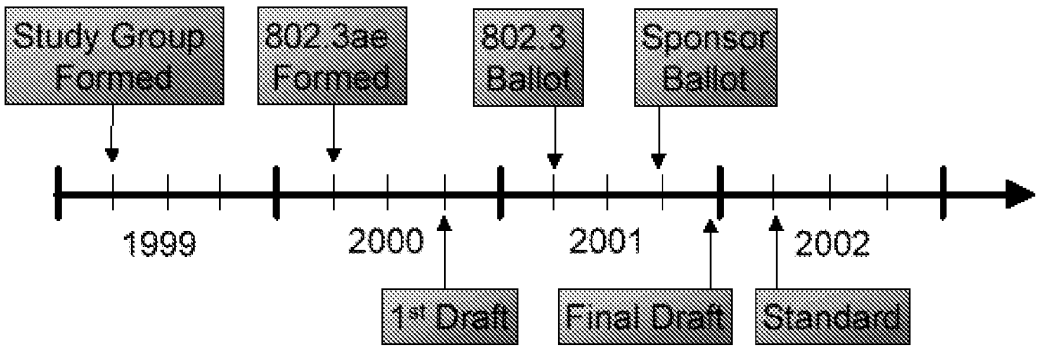


Figure 4. Key milestones in the development of the 10 Gigabit Ethernet standard.

The 10 Gigabit Ethernet Standard

Under the International Standards Organization's Open Systems Interconnection (OSI) model, Ethernet is fundamentally a Layer 2 protocol. 10 Gigabit Ethernet uses the IEEE 802.3 Ethernet Media Access Control (MAC) protocol, the IEEE 802.3 Ethernet frame format, and the minimum and maximum IEEE 802.3 frame size.

Just as 1000BASE-X and 1000BASE-T (Gigabit Ethernet) remained true to the Ethernet model, 10 Gigabit Ethernet continues the natural evolution of Ethernet in speed and distance. Since it is a full-duplex only and fiber-only technology, it does not need the carrier-sensing multiple-access with collision detection (CSMA/CD) protocol that defines slower, half-duplex Ethernet technologies. In every other respect, 10 Gigabit Ethernet remains true to the original Ethernet model.

An Ethernet PHYsical layer device (PHY), which corresponds to Layer 1 of the OSI model, connects the media (optical or copper) to the MAC layer, which corresponds to OSI Layer 2. Ethernet architecture further divides the PHY (Layer 1) into a Physical Media Dependent (PMD) and a Physical Coding Sublayer (PCS). Optical transceivers, for example, are PMDs. The PCS is made up of coding (e.g., 64/66b) and a serializer or multiplexing functions.

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The 802.3ae specification defines two PHY types: the LAN PHY and the WAN PHY (discussed below). The WAN PHY has an extended feature set added onto the functions of a LAN PHY. These PHYs are solely distinguished by the PCS. There will also be a number of PMD types. (See Figure 5.)

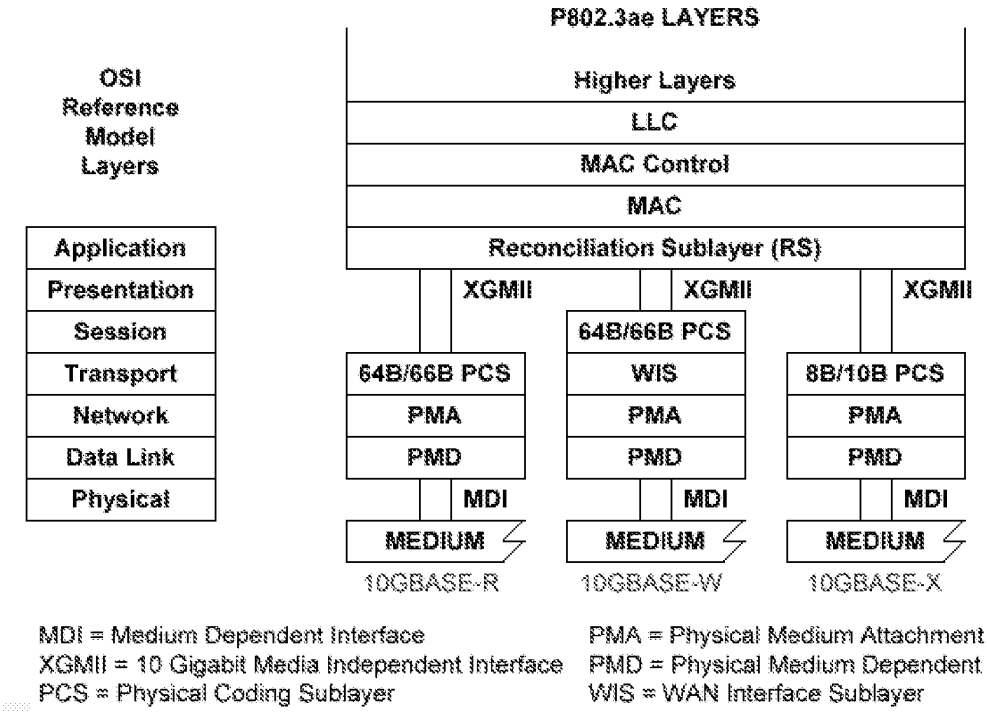


Figure 5. The architectural components of the LAN and WAN PHY.

Chip Interface (XAUI)

Among the many technical innovations of the 10 Gigabit Ethernet Task Force is an interface called the XAUI (pronounced "Zowie"). The "AUI" portion is borrowed from the Ethernet Attachment Unit Interface. The "X" represents the Roman numeral for ten and implies ten gigabits per second. The XAUI is designed as an interface extender, and the interface, which it extends, is the XGMII, the 10 Gigabit Media Independent Interface. The XGMII is a 74 signal wide interface (32-bit data paths for each of transmit and receive) that may be used to attach the Ethernet MAC to its PHY. The XAUI may be used in place of, or to extend, the XGMII in chip-to-chip applications typical of most Ethernet MAC to PHY interconnects. (See Figure 6.)

The XAUI is a low pin count, self-clocked serial bus that is directly evolved from the Gigabit Ethernet 1000BASE-X PHY. The XAUI interface speed is 2.5 times that of

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1000BASE-X. By arranging four serial lanes, the 4-bit XAUI interface supports the ten-times data throughput required by 10 Gigabit Ethernet.

The XAUI employs the same robust 8B/10B transmission code of 1000BASE-X to provide a high level of signal integrity through the copper media typical of chip-to-chip printed circuit board traces. Additional benefits of XAUI technology include its inherently low EMI (Electro-Magnetic Interference) due to it's self-clocked nature, compensation for multi-bit bus skew -- allowing significantly longer-distance chip-to-chip -- error detection and fault isolation capabilities, low power consumption, and the ability to integrate the XAUI input/output within commonly available CMOS processes.

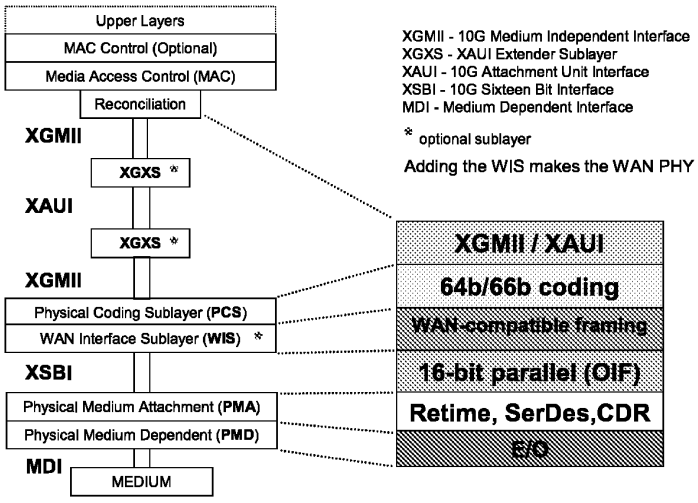


Figure 6. XAUI functions as an extender interface between the MAC and PCS.

A multitude of component vendors are delivering or have announced XAUI interface availability on standalone chips, custom ASICs (application-specific integrated circuits), and even FPGAs (field-programmable gate arrays). The 10Gigabit Ethernet XAUI technology is identical or equivalent to the technology employed in other key industry standards such as InfiniBand(TM), 10 Gigabit Fibre Channel, and general purpose copper and optical backplane interconnects. This assures the lowest possible cost for 10 Gbps interconnects through healthy free market competition.

Specifically targeted XAUI applications include MAC to Physical layer chip and direct MAC-to-optical transceiver module interconnects. The XAUI is the interface for the proposed Ten Gigabit Pluggable optical module definition called the XGP. Integrated XAUI solutions together with the XGP will enable efficient low-cost 10 Gigabit Ethernet direct multi-port MAC to optical module interconnects with only PC board traces in between.

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Physical Media Dependent (PMDs)

The IEEE 802.3ae Task Force has developed a draft standard that provides a physical layer that supports link distances for fiber optic media as shown in Table A.

To meet these distance objectives, four PMDs were selected. The task force selected a 1310 nanometer serial PMD to meet its 2km and 10km single-mode fiber (SMF) objectives. It also selected a 1550 nm serial solution to meet (or exceed) its 40km SMF objective. Support of the 40km PMD is an acknowledgement that Gigabit Ethernet is already being successfully deployed in metropolitan and private, long distance applications. An 850 nanometer PMD was specified to achieve a 65-meter objective over multimode fiber using serial 850 nm transceivers.

Additionally, the task force selected two versions of the wide wave division multiplexing (WWDM) PMD, a 1310 nanometer version over single-mode fiber to travel a distance of 10km and a 1310 nanometer PMD to meet its 300-meter-over-installed-multimode-fiber objective.

PMD (Optical Transceiver)	Type of Fiber Supported	Target Distance (Meters)
850 nm serial	Multi Mode	65
1310 nm WWDM	Multi Mode	300
1310 nm WWDM	Single Mode	10,000
1310 nm serial	Single Mode	10,000
1550 nm serial	Single Mode	40,000

Table A. Listing of the PMDs that have been selected to meet the task force's distance objectives.

Physical Layer (PHYs)

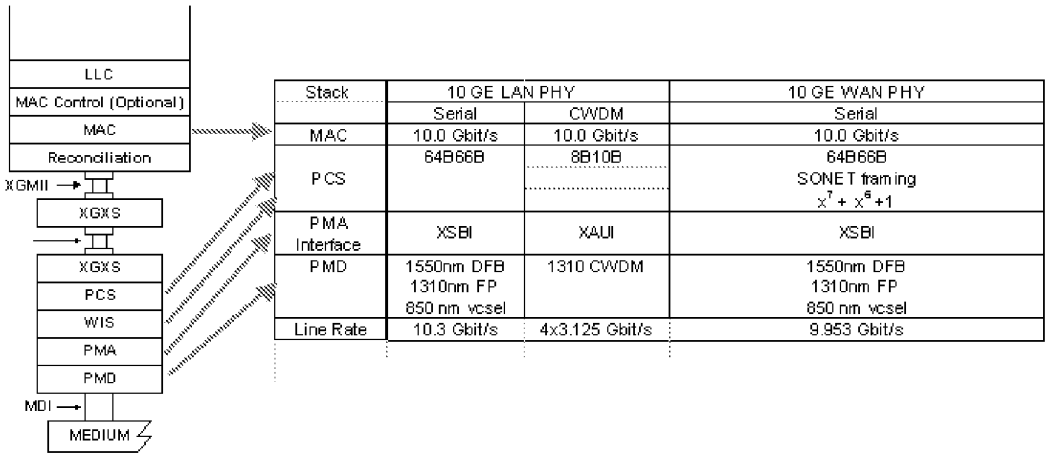
The LAN PHY and the WAN PHY will operate over common PMDs and, therefore, will support the same distances. These PHYs are distinguished solely by the Physical Encoding Sublayer (PCS). (See Figure 7.) The 10 Gigabit LAN PHY is intended to support existing Gigabit Ethernet applications at ten times the bandwidth with the most cost-effective solution. Over time, it is expected that the LAN PHY will be used in pure optical switching environments extending over all WAN distances. However, for compatibility with the existing WAN network, the 10 Gigabit Ethernet WAN PHY supports connections to existing and future installations of SONET/SDH (Synchronous Optical Network/Synchronous Digital Hierarchy) circuit-switched telephony access equipment.

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	Serial LAN	Serial WAN	4-Lane LAN
PHY (chipsets)	64/66	64/66	XAUI
		WIS	
	SerDes		
PMD (optics)	Serial 850nm (mmf 65m) 1310nm (smf 10km) 1550nm (smf 40km)		WWDM 1310nm (mmf 300m) 1310nm (smf 10km)

Figure 7. Conceptual Diagram of the PHYs and PMDs.

The WAN PHY differs from the LAN PHY by including a simplified SONET/SDH framer in the WAN Interface Sublayer (WIS). Because the line rate of SONET OC-192/SDH STM-64 is within a few percent of 10 Gbps, it is relatively simple to implement a MAC that can operate with a LAN PHY at 10 Gbps or with a WAN PHY payload rate of approximately 9.29 Gbps. (See Figure 8.)



Stack	10 GE LAN PHY		10 GE WAN PHY
	Serial	CWDM	Serial
MAC	10.0 Gbit/s	10.0 Gbit/s	10.0 Gbit/s
PCS	64B66B	8B10B	64B66B SONET framing $x^7 + x^6 + 1$
PMA Interface	XSBI	XAUI	XSBI
PMD	1550nm DFB 1310nm FP 850 nm vcsel	1310 CWDM	1550nm DFB 1310nm FP 850 nm vcsel
Line Rate	10.3 Gbit/s	4x3.125 Gbit/s	9.953 Gbit/s

Figure 8. Detailed Illustration of the LAN and WAN PHYs and associated PMDs.

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In order to enable low-cost WAN PHY implementations, the task force specifically rejected conformance to SONET/SDH jitter, stratum clock, and certain SONET/SDH optical specifications. The WAN PHY is basically a cost effective link that uses common Ethernet PMDs to provide access to the SONET infrastructure, thus enabling attachment of packet-based IP/Ethernet switches to the SONET/SDH and time division multiplexed (TDM) infrastructure. This feature enables Ethernet to use SONET/SDH for Layer 1 transport across the WAN transport backbone.

It is also important to note that Ethernet remains an asynchronous link protocol. As in every Ethernet network, 10 Gigabit Ethernet's timing and synchronization must be maintained within each character in the bit stream of data, but the receiving hub, switch, or router may re-time and re-synchronize the data. In contrast, synchronous protocols, including SONET/SDH, require that each device share the same system clock to avoid timing drift between transmission and reception equipment and subsequent increases in network errors where timed delivery is critical.

The WAN PHY attaches data equipment such as switches or routers to a SONET/SDH or optical network. This allows simple extension of Ethernet links over those networks. Therefore, two routers will behave as though they are directly attached to each other over a single Ethernet link. Since no bridges or store-and-forward buffer devices are required between them, all the IP traffic management systems for differentiated service operate over the extended 10 Gigabit Ethernet link connecting the two routers.

To simplify management of extended 10 Gigabit Ethernet links, the WAN PHY provides most of the SONET/SDH management information, allowing the network manager to view the Ethernet WAN PHY links as though they are SONET/SDH links. It is then possible to do performance monitoring and fault isolation on the entire network, including the 10 Gigabit Ethernet WAN link, from the SONET/SDH management station. The SONET/SDH management information is provided by the WAN Interface Sublayer (WIS), which also includes the SONET/SDH framer. The WIS operates between the 64B/66B PCS and serial PMD layers common to the LAN PHY.

10 Gigabit Ethernet in the Marketplace

The accelerating growth of worldwide network traffic is forcing service providers, enterprise network managers and architects to look to ever higher-speed network technologies in order to solve the bandwidth demand crunch. Today, these administrators typically use Ethernet as their backbone technology. Although networks face many different issues, 10 Gigabit Ethernet meets several key criteria for efficient and effective high-speed networks:

- Easy, straightforward migration to higher performance levels without disruption,

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- Lower cost of ownership vs. current alternative technologies – including both acquisition and support costs
- Familiar management tools and common skills base
- Ability to support new applications and data types
- Flexibility in network design
- Multiple vendor sourcing and proven interoperability

Managers of enterprise and service provider networks have to make many choices when they design networks. They have multiple media, technologies, and interfaces to choose from to build campus and metro connections: Ethernet (100, 1000, and 10,000 Mbps), OC-12 (622 Mbps) and OC-48 (2.488 Gbps), SONET or equivalent SDH network, packet over SONET/SDH (POS), and the newly authorized IEEE 802 Task Force (802.17) titled Resilient Packet Ring.

Network topological design and operation has been transformed by the advent of intelligent Gigabit Ethernet multi-layer switches. In LANs, core network technology is rapidly shifting to Gigabit Ethernet and there is a growing trend towards Gigabit Ethernet networks that can operate over metropolitan area distances.

The next step for enterprise and service provider networks is the combination of multi-gigabit bandwidth with intelligent services, leading to scaled, intelligent, multi-gigabit networks with backbone and server connections ranging up to 10 Gbps.

In response to market trends, Gigabit Ethernet is currently being deployed over tens of kilometers in private networks. With 10 Gigabit Ethernet, the industry has developed a way to not only increase the speed of Ethernet to 10 Gbps but also to extend its operating distance and interconnectivity. In the future, network managers will be able to use 10 Gigabit Ethernet as a cornerstone for network architectures that encompass LANs, MANs and WANs using Ethernet as the end-to-end, Layer 2 transport method.

Ethernet bandwidth can then be scaled from 10 Mbps to 10 Gbps – a ratio of 1 to 1000 -- without compromising intelligent network services such as Layer 3 routing and layer 4 to layer 7 intelligence, including quality of service (QoS), class of service (CoS), caching, server load balancing, security, and policy based networking capabilities. Because of the uniform nature of Ethernet across all environments when IEEE 802.3ae is deployed, these services can be delivered at line rates over the network and supported over all network physical infrastructures in the LAN, MAN, and WAN. At that point, convergence of voice and data networks, both running over Ethernet, becomes a very real option. And, as TCP/IP incorporates enhanced services and features, such as packetized voice and video, the underlying Ethernet can also carry these services without modification.

As we have seen with previous versions of Ethernet, the cost for 10 Gbps communications has the potential to drop significantly with the development of new technologies. In contrast to 10 Gbps telecommunications lasers, the 10 Gigabit Ethernet short links — less than 40km over single-mode (SM) fiber — will be capable of using lower cost, uncooled optics and, in some cases, vertical cavity surface emitting lasers (VCSEL), which have the potential to lower PMD costs. In addition, the industry is supported by an aggressive

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merchant chip market that provides highly integrated silicon solutions. Finally, the Ethernet market tends to spawn highly competitive start-ups with each new generation of technology to compete with established Ethernet vendors.

Applications for 10 Gigabit Ethernet

10 Gigabit Ethernet in Local Area Networks

Ethernet technology is already the most deployed technology for high performance LAN environments. With the extension of 10 Gigabit Ethernet into the family of Ethernet technologies, the LAN now can reach farther and support up coming bandwidth hungry applications.

Similar to Gigabit Ethernet technology, the 10 Gigabit proposed standard supports both single-mode and multi-mode fiber mediums. However in 10 Gigabit Ethernet, the distance for single-mode fiber has expanded from the 5km that Gigabit Ethernet supports to 40km in 10 Gigabit Ethernet.

The advantage for the support of longer distances is that it gives companies who manage their own LAN environments the option of extending their data centers to more cost-effective locations up to 40km away from their campuses. This also allows them to support multiple campus locations within that 40km range. Within data centers, switch-to-switch applications, as well as switch to server applications, can also be deployed over a more cost effective multi-mode fiber medium to create 10 Gigabit Ethernet backbones that support the continuous growth of bandwidth hungry applications. (See Figure 9.)

With 10 Gigabit backbones installed, companies will have the capability to begin providing Gigabit Ethernet service to workstations and, eventually, to the desktop in order to support applications such as streaming video, medical imaging, centralized applications, and high-end graphics. 10 Gigabit Ethernet will also provide lower network latency due to the speed of the link and over-provisioning bandwidth to compensate for the bursty nature of data in enterprise applications. Additionally, the LAN environment must continue to change to keep up with the growth of the Internet.

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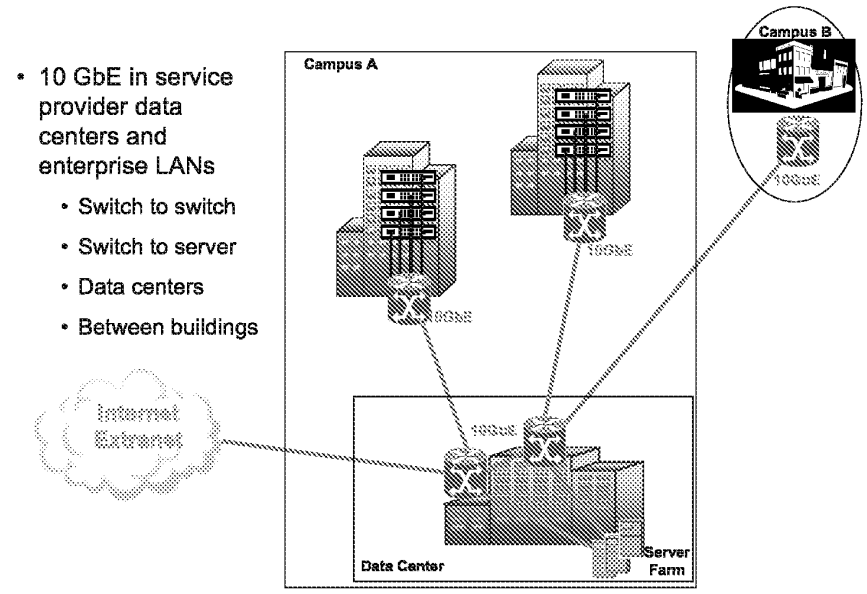


Figure 9. Illustration of 10 Gigabit Ethernet use in expanded LAN environments.

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10 Gigabit Ethernet in Metropolitan and Storage Area Networks

Vendors and users generally agree that Ethernet is inexpensive, well understood, widely deployed and backwards compatible from Gigabit switched down to 10 Megabit shared. Today a packet can leave a server on a short-haul optic Gigabit Ethernet port, move cross-country via a DWDM (dense wave division multiplexing) network, and find its way down to a PC attached to a "thin coax" BNC (Bayonet Neill Concelman) connector, all without any re-framing or protocol conversion. Ethernet is literally everywhere, and 10 Gigabit Ethernet maintains this seamless migration in functionality.

Gigabit Ethernet is already being deployed as a backbone technology for dark fiber metropolitan networks. With appropriate 10 Gigabit Ethernet interfaces, optical transceivers and single mode fiber, service providers will be able to build links reaching 40km or more. (See Figure 10.)

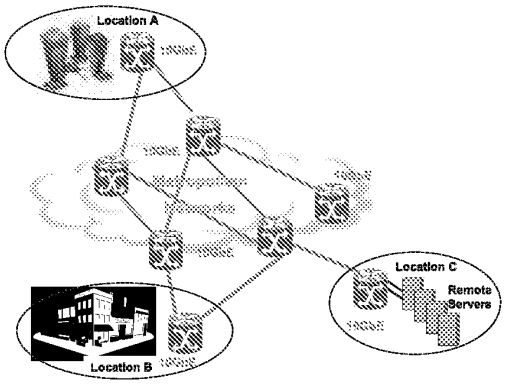


Figure 10. An Example of 10 Gigabit Ethernet use in a MAN.

Additionally, 10 Gigabit Ethernet will provide infrastructure for both network-attached storage (NAS) and storage area networks (SAN). Prior to the introduction of 10 Gigabit Ethernet, some industry observers maintained that Ethernet lacked sufficient horsepower to get the job done. Ethernet, they said, just doesn't have what it takes to move "dump truck loads worth of data." 10 Gigabit Ethernet, can now offer equivalent or superior data carrying capacity at similar latencies to many other storage networking technologies including 1 or 2 Gigabit Fiber Channel, Ultra160 or 320 SCSI, ATM OC-3, OC-12 & OC-192, and HIPPI (High Performance Parallel Interface). While Gigabit Ethernet storage servers, tape libraries and compute servers are already available, users should look for early availability of 10 Gigabit Ethernet end-point devices in the second half of 2001.

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There are numerous applications for Gigabit Ethernet in storage networks today, which will seamlessly extend to 10 Gigabit Ethernet as it becomes available. (See Figure 11.) These include:

- Business continuance/disaster recovery
- Remote backup
- Storage on demand
- Streaming media

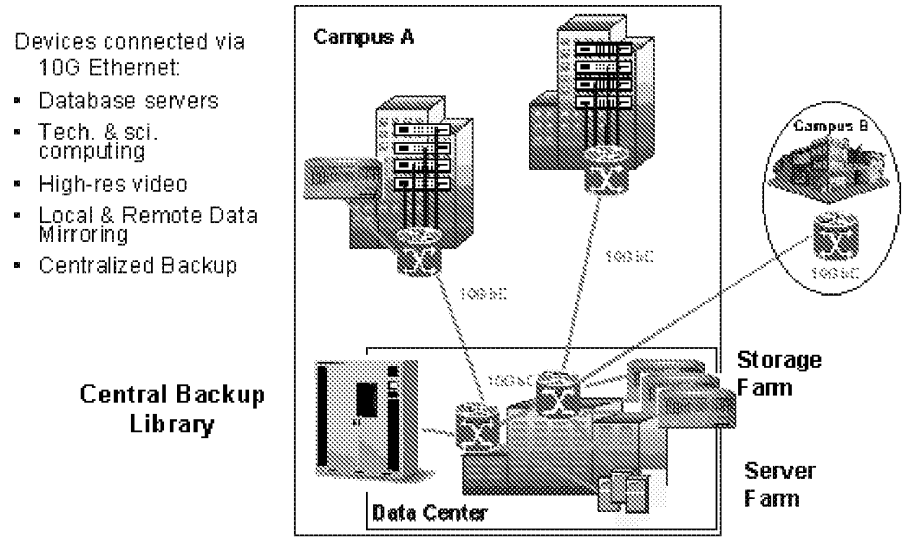


Figure 11. Use of 10 Gigabit Ethernet in Storage Area Networks.

10 Gigabit Ethernet in Wide Area Networks

10 Gigabit Ethernet will enable Internet service providers (ISP) and network service providers (NSPs) to create very high-speed links at a very low cost, between co-located, carrier-class switches and routers and optical equipment that is directly attached to the SONET/SDH cloud. 10 Gigabit Ethernet with the WAN PHY will also allow the construction of WANs that connect geographically dispersed LANs between campuses or POPs (points of presence) over existing SONET/SDH/TDM networks. 10 Gigabit Ethernet links between a service provider's switch and a DWDM (dense wave division multiplexing) device or LTE (line termination equipment) might in fact be very short -- less than 300 meters. (See Figure 12.)

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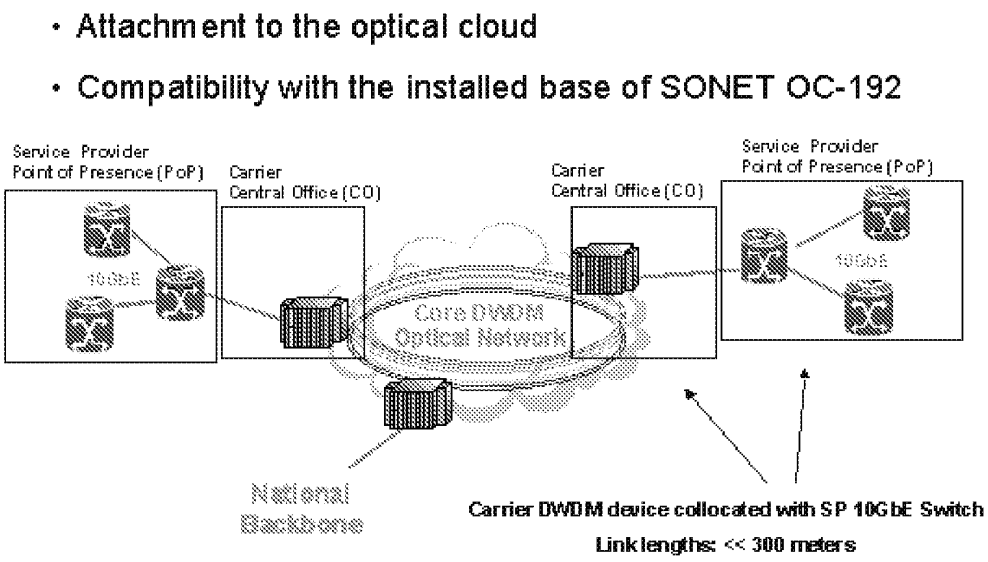


Figure 12. Example of 10 Gigabit Ethernet in WAN applications.

Conclusion

As the Internet transforms longstanding business models and global economies, Ethernet has withstood the test of time to become the most widely adopted networking technology in the world. Much of the world's data transfer begins and ends with an Ethernet connection. Today, we are in the midst of an Ethernet renaissance spurred on by surging E-Business and the demand for low cost IP services that have opened the door to questioning traditional networking dogma. Service providers are looking for higher capacity solutions that simplify and reduce the total cost of network connectivity, thus permitting profitable service differentiation, while maintaining very high levels of reliability.

Enter 10 Gigabit Ethernet. Ethernet is no longer designed only for the LAN. 10 Gigabit Ethernet is the natural evolution of the well-established IEEE 802.3 standard in speed and distance. It extends Ethernet's proven value set and economics to metropolitan and wide area networks by providing:

- Potentially lowest total cost of ownership (infrastructure/operational/human capital)
- Straightforward migration to higher performance levels
- Proven multi-vendor and installed base interoperability (Plug and Play)
- Familiar network management feature set

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An Ethernet-optimized infrastructure build out is taking place. The metro area is currently the focus of intense network development to deliver optical Ethernet services. 10 Gigabit Ethernet is on the roadmaps of most switch, router and metro optical system vendors to enable:

- Cost effective Gigabit-level connections between customer access gear and service provider POPs (points of presence) in native Ethernet format
- Simple, very high speed, low-cost access to the metro optical infrastructure
- Metro-based campus interconnection over dark fiber targeting distances of 10/40km and greater
- End to end optical networks with common management systems

Glossary

Acronyms

802.3ae – The proposed IEEE standard for 10 Gigabit Ethernet

802.3z – The IEEE standard for Gigabit Ethernet

CoS – Class of Service

CWDM – Coarse Wave Division Multiplexing

DWDM – Dense Wave Division Multiplexing

Gbps – Gigabits per second or billion bits per second

IEEE – Institute of Electrical and Electronics Engineers

IP – Internet Protocol

ISO – International Standards Organization

LAN – Local Area Network

MAC – Media Access Control layer

MAN – Metropolitan Area Network

Mbps – Megabits per second or million bits per second

MMF – Multi Mode Fiber

OC–X – Optical Carrier Level

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PCS – Physical Coding Sublayer

PHY – Physical layer device

PMD – Physical Media Dependent

POP – Points of Presence

RMON – Remote Monitoring

QoS – Quality of Service

SMF – Single Mode Fiber

SNMP – Simple Network Management Protocol

SDH – Synchronous Digital Hierarchy

SONET – Synchronous Optical Network

Tbps – Terabits per second or trillion bits per second

TCP/IP – Transmission Control Protocol/Internet Protocol

TDM – Time Division Multiplexing

WAN – Wide Area Network

WDM – Wave Division Multiplexing

WIS – WAN Interface Sublayer

WWDM – Wide Wave Division Multiplexing

Terms

Dense Wave Division Multiplexing -- Wavelengths are closely spaced, allowing more channels to be sent through one fiber. Currently, systems using 100Ghz spacing are deployed in the WAN environment. Overall wavelength range is typically between 1530nm to 1560nm. The minimum and maximum wavelengths are restricted by the wavelength dependent gain profile of optical amplifiers.

Media Access Control -- The media access control sublayer provides a logical connection between the MAC clients of itself and its peer station. It main responsibility is to initialize, control, and manage the connection with the peer station. The MAC layer of the 10 Gigabit protocol uses the same Ethernet address and frame formats as other speeds, and will

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operate in full-duplex mode. It will support a data rate of 10 Gbps using a pacing mechanism for rate adaptation when connected to a WAN-friendly PHY.

OC-192 -- A speed of SONET interconnect with a payload rate of 9.584640 Gbps, primarily used in WAN environments.

Physical Coding Sublayer -- Part of the PHY, the PCS sublayer is responsible for encoding the data stream from the MAC layer for transmission by the PHY layer and decoding the data stream received from the PHY layer for the MAC layer.

PHY – The physical layer device, a circuit block that includes a PMD (physical media dependent), a PMA (physical media attachment), and a PCS (physical coding sublayer).

PMD -- Part of the PHY, the physical media dependent sublayer is responsible for signal transmission. The typical PMD functionality includes amplifier, modulation, and wave shaping. Different PMD devices may support different media.

WWDM -- A technique used to effectively transmit several wavelengths (i.e. -- colors of light) from several laser sources through one fiber. Each laser source would be calibrated to send a unique optical wavelength (which are separated at the receiving end of the fiber).

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CY7C006
CY7C016

16K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **16K x 8 organization (CY7C006)**
- **16K x 9 organization (CY7C016)**
- **0.65-micron CMOS for optimum speed/power**
- **High-speed access: 15ns**
- **Low operating power: I_{CC} = 140 mA (typ.)**
- **Fully asynchronous operation**
- **Automatic power-down**
- **TTL compatible**
- **Expandable data bus to 16/18 bits or more using Master/Slave chip select when using more than one device**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin PLCC, 64-pin (7C006) and 80-pin (7C016)TQFP**
- **Pin compatible and functional equivalent to IDT7006/IDT7016**

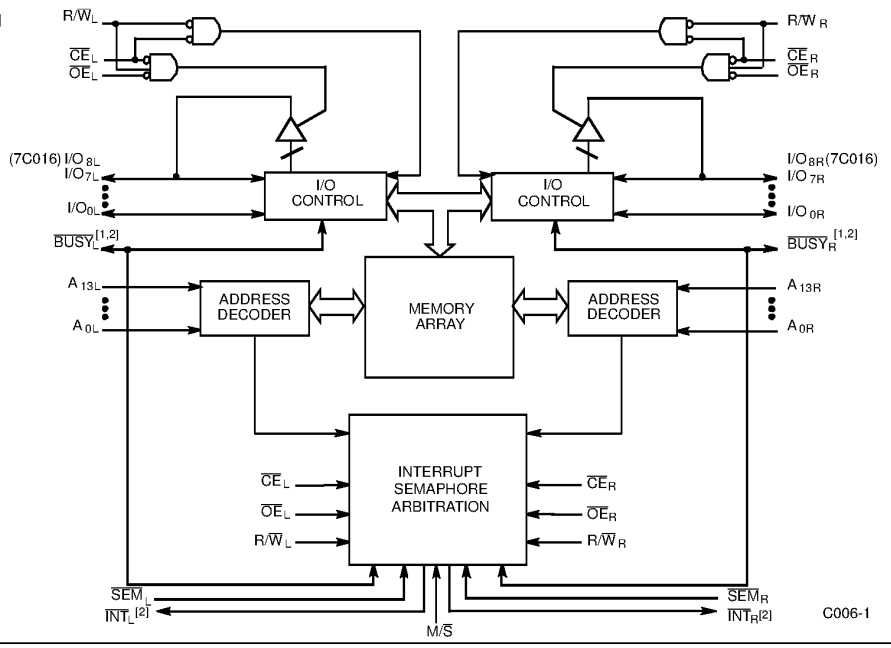
Functional Description

The CY7C006 and CY7C016 are high-speed CMOS 16K x 8 and 16K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7C006/016 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C006/016 can be utilized as a standalone 128-/144-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16-/18-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 16-/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags, $\overline{BUSY}$ and $\overline{INT}$, are provided on each port. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7C006 and CY7C016 are available in 68-pin PLCCs, and 64-pin (7C006) TQFP and 80-pin (7C016) TQFP.

Logic Block Diagram



Notes:

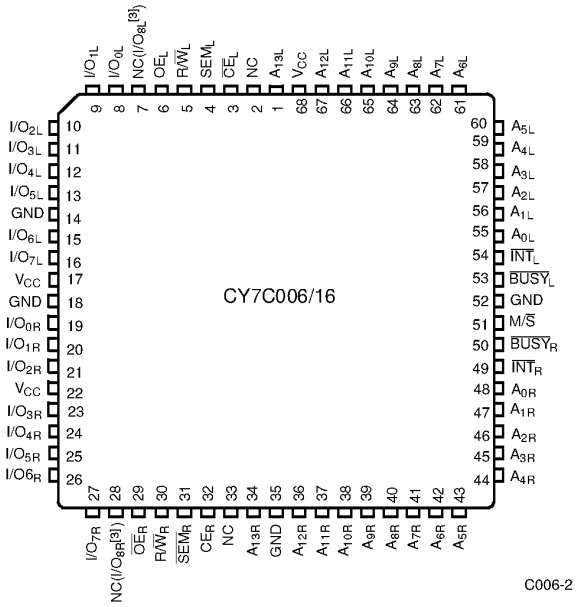
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Interrupt: push-pull output and requires no pull-up resistor.

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February 1995 – Revised November 1996

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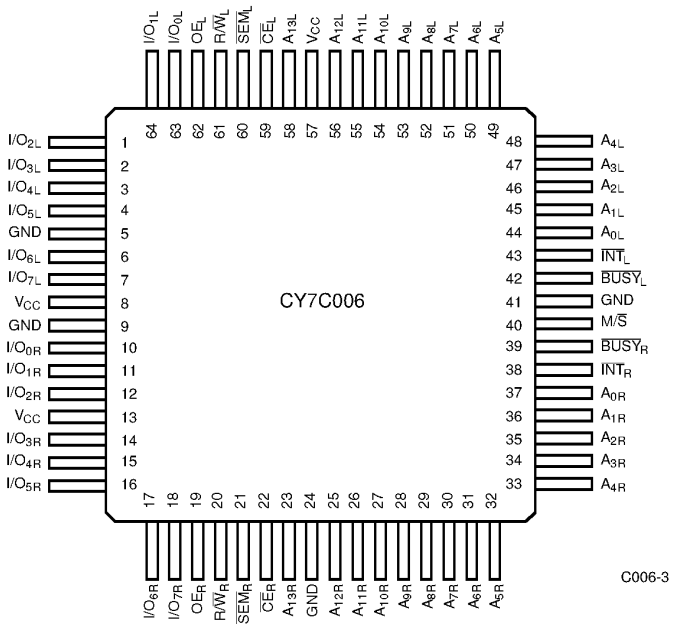
Pin Configurations

68-Pin PLCC
Top View



C006-2

64-Pin TQFP
Top View



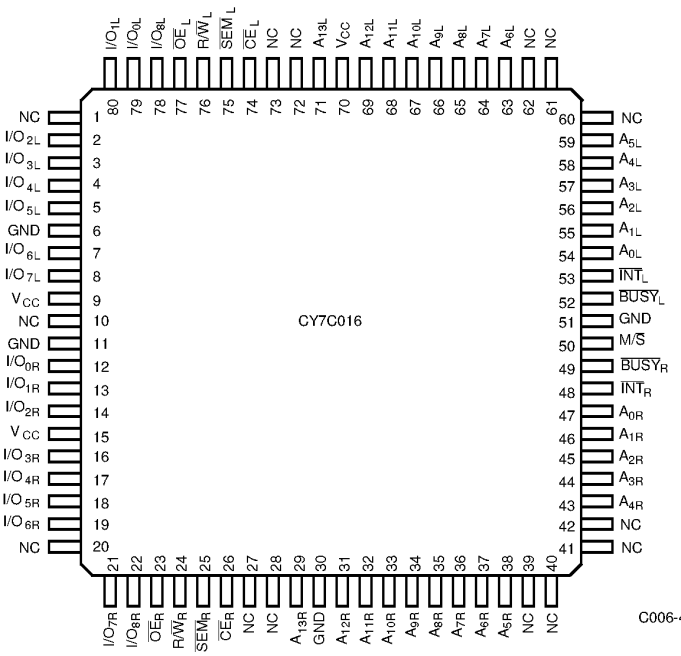
C006-3

Note:
3. I/O for 7C016 only.

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Pin Configurations (continued)

80-Pin TQFP
Top View



C006-4

Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data Bus Input/Output
A_{0L-13L}	A_{0R-13R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 3FFE and is cleared when left port reads location 3FFE. $\overline{INT}_R$ is set when left port writes location 3FFF and is cleared when right port reads location 3FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

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Selection Guide

	7C006–15 7C016–15	7C006–25 7C016–25	7C006–35 7C016–35	7C006–55 7C016–55
Maximum Access Time (ns)	15	25	35	55
Maximum Operating Current (mA)	260	220	210	200
Maximum Standby Current for I_{SB1} (mA)	70	60	50	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage[4]..... –0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Note:
4. Pulse width < 20 ns.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C006–15 7C016–15 Min.	Typ.	Max.	7C006–25 7C016–25 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}				2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10		+10	–10		+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10		+10	–10		+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		170	260		160	220	mA
			Ind					160	270	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l		50	70		40	60	mA
			Ind					40	75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l		110	170		90	130	mA
			Ind					90	150	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Com'l		3	15		3	15	mA
			Ind					3	15	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≥ 0.2V, Active Port Outputs, f = f_{MAX}[5]	Com'l		100	150		80	120	mA
			Ind					80	130	

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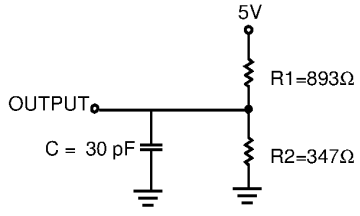
Electrical Characteristics (continued)

Parameter	Description	Test Conditions		7C006–35 7C016–35 Min.	Typ.	Max.	7C006–55 7C016–55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}				2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10		+10	–10		+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10		+10	–10		+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		150	210		140	200	mA
			Ind		150	250		140	240	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l		30	50		20	40	mA
			Ind		30	65		20	55	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l		80	120		70	100	mA
			Ind		80	130		70	115	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Com'l		3	15		3	15	mA
			Ind		3	15		3	15	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[5]	Com'l		70	100		60	90	mA
			Ind		70	110		60	95	

Capacitance[6]

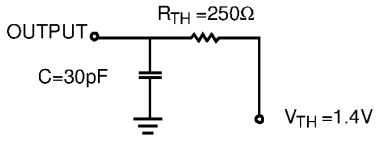
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



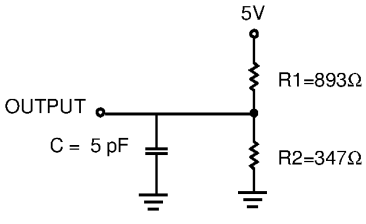
(a) Normal Load (Load 1)

C006-5



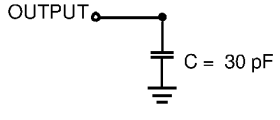
(b) Thévenin Equivalent (Load)

C006-6



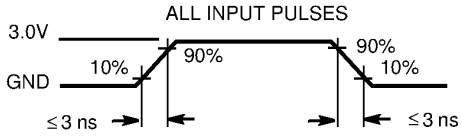
(c)Three-State Delay (Load 3)

C006-7



Load (Load 2)

C006-8



C006-9

Notes:

5. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
6. Tested initially and after any design or process changes that may affect these parameters.

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Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C006–15 7C016–15		7C006–25 7C016–25		7C006–35 7C016–35		7C006–55 7C016–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		20		25	ns
t_{LZOE}[8,9,10]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[8,9,10]	$\overline{OE}$ HIGH to High Z		10		15		15		25	ns
t_{LZCE}[8,9,10]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[8,9,10]	$\overline{CE}$ HIGH to High Z		10		15		15		25	ns
t_{PU}[10]	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}[10]	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		45		ns
t_{AW}	Address Set-Up to Write End	12		20		30		45		ns
t_{HA}	Address Hold From Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		40		ns
t_{SD}	Data Set-Up to Write End	10		15		15		25		ns
t_{HD}[11]	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[9,10]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[9,10]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[12]	Write Pulse to Data Delay		30		50		60		80	ns
t_{DDD}[12]	Write Data Valid to Read Data Valid		25		30		35		60	ns
BUSY TIMING[13]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		17		25		30	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		17		25		30		ns
t_{BDD}[14]	$\overline{BUSY}$ HIGH to Data Valid		Note 13		Note 13		Note 13		Note 13	ns

Notes:

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
9. Test conditions used are Load 3.
10. This parameter is guaranteed but not tested.
11. Must be met by the device writing to the RAM under all operating conditions.
12. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
13. Test conditions used are Load 2.
14. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

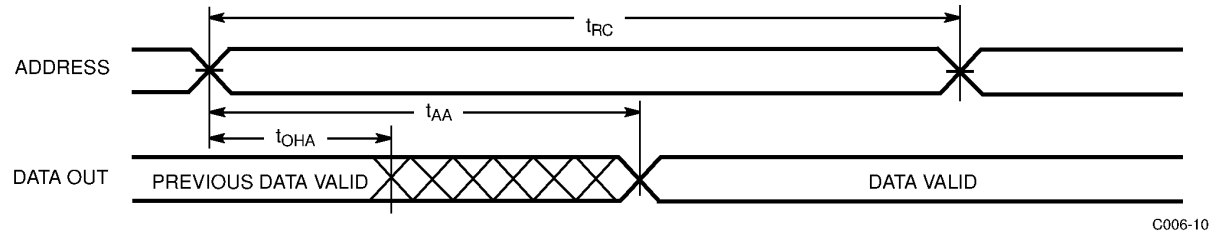
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Switching Characteristics Over the Operating Range[7] (continued)

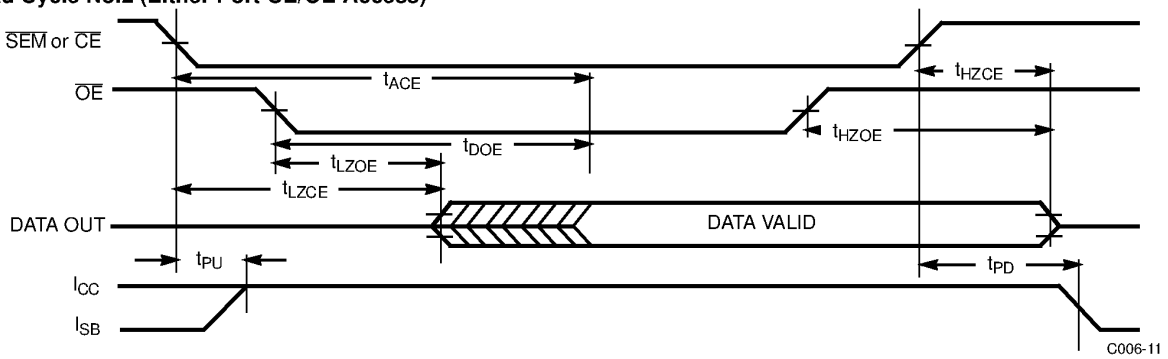
Parameter	Description	7C006–15 7C016–15		7C006–25 7C016–25		7C006–35 7C016–35		7C006–55 7C016–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING[13]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		30	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		30	ns
SEMAPHORE TIMING										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

Switching Waveforms

Read Cycle No.1 (Either Port Address Access)[15,16]



Read Cycle No.2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[15,17,18]

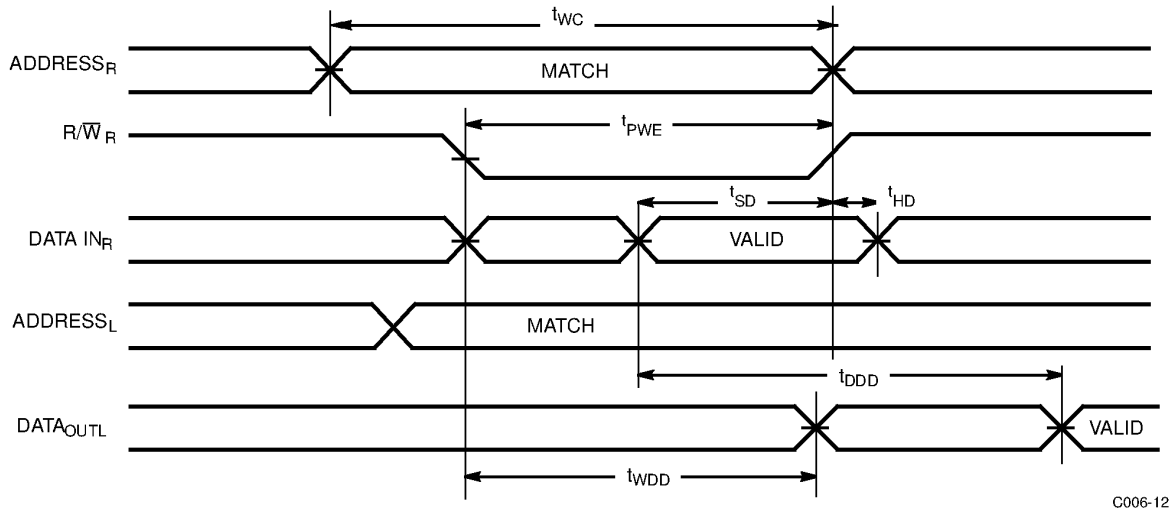


Notes:
15. R/$\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.

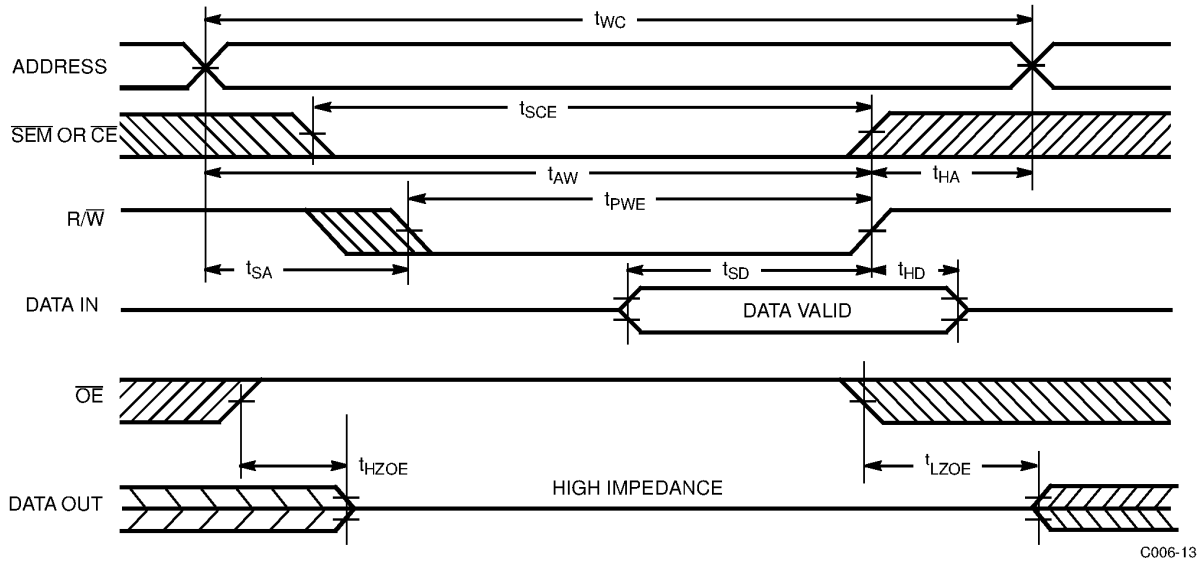
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Switching Waveforms (continued)

Read Timing with Port-to-Port Delay (M/$\overline{S}$=L)[19,20]



Write Cycle No.1: $\overline{OE}$ Three-State Data I/Os (Either Port)[21,22,23]



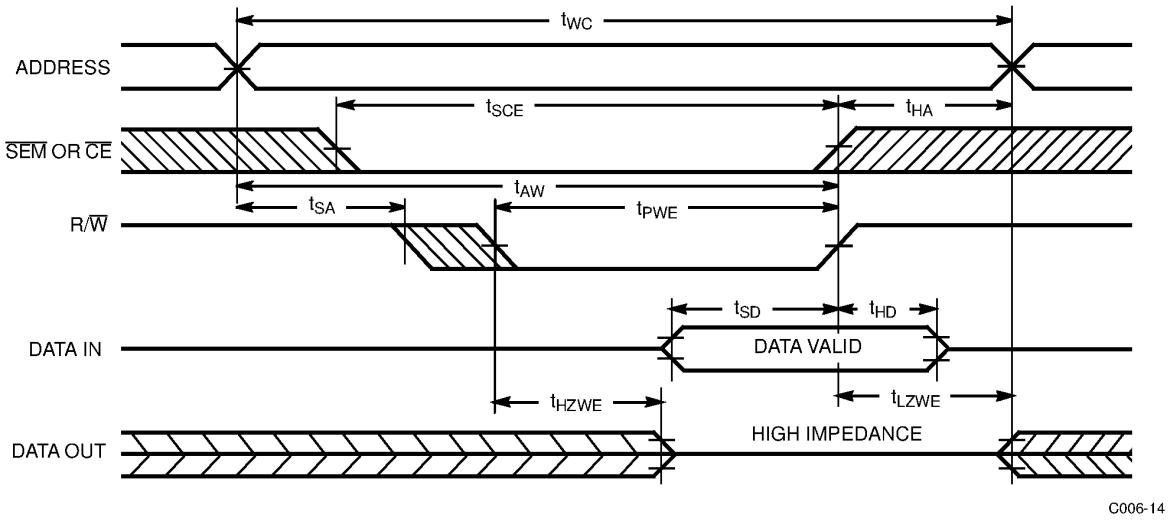
Notes:

19. $\overline{BUSY}$ = HIGH for the writing port.
20. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.
21. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or ($t_{HZWE} + t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
23. R/$\overline{W}$ must be HIGH during all address transitions.

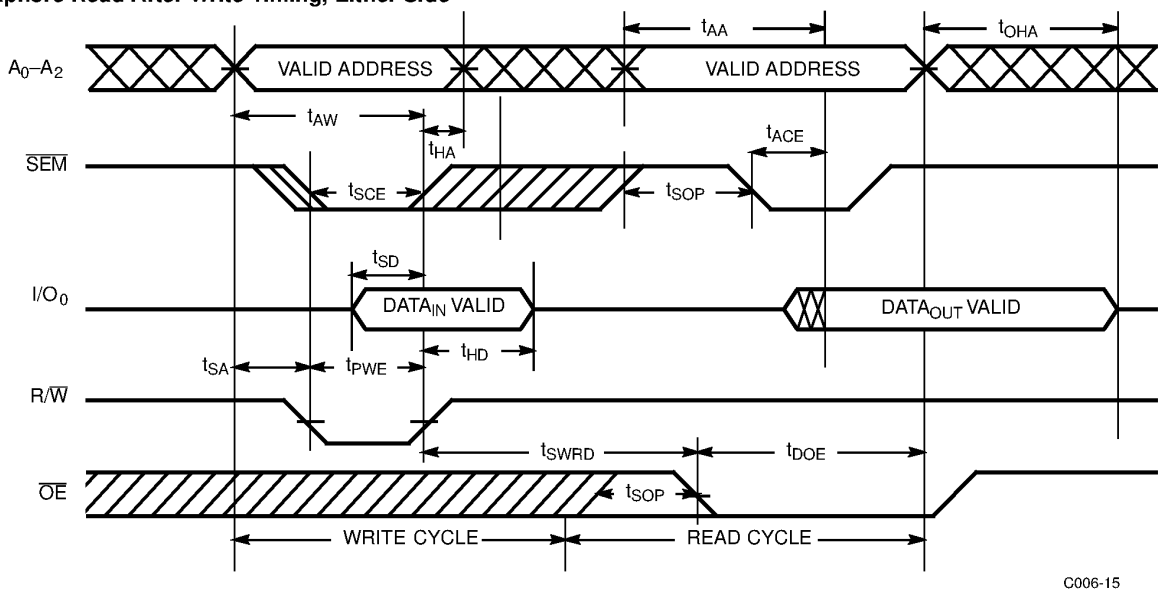
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Switching Waveforms (continued)

Write Cycle No.2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[20,22,24]



Semaphore Read After Write Timing, Either Side [25]

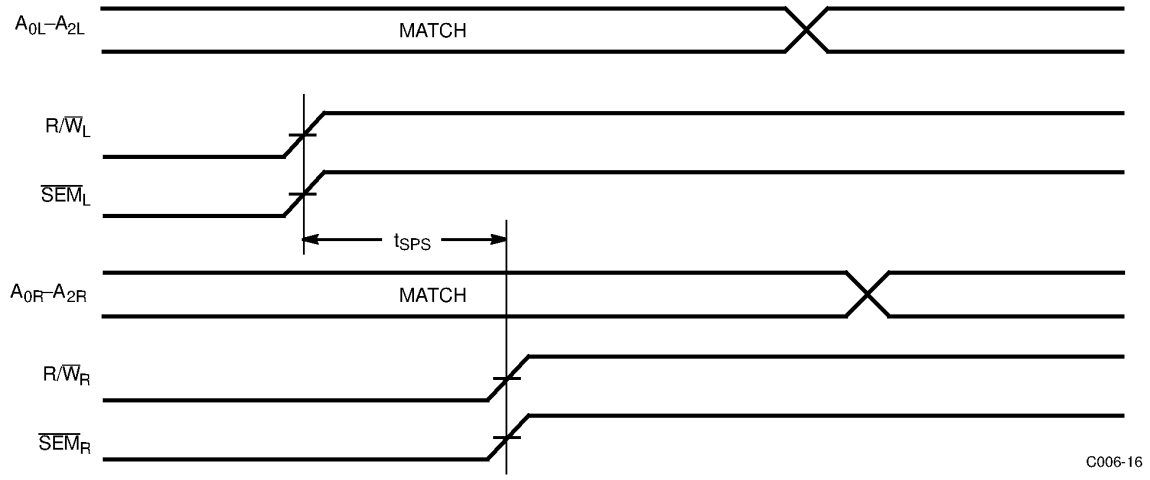


Notes:
24. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.
25. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).

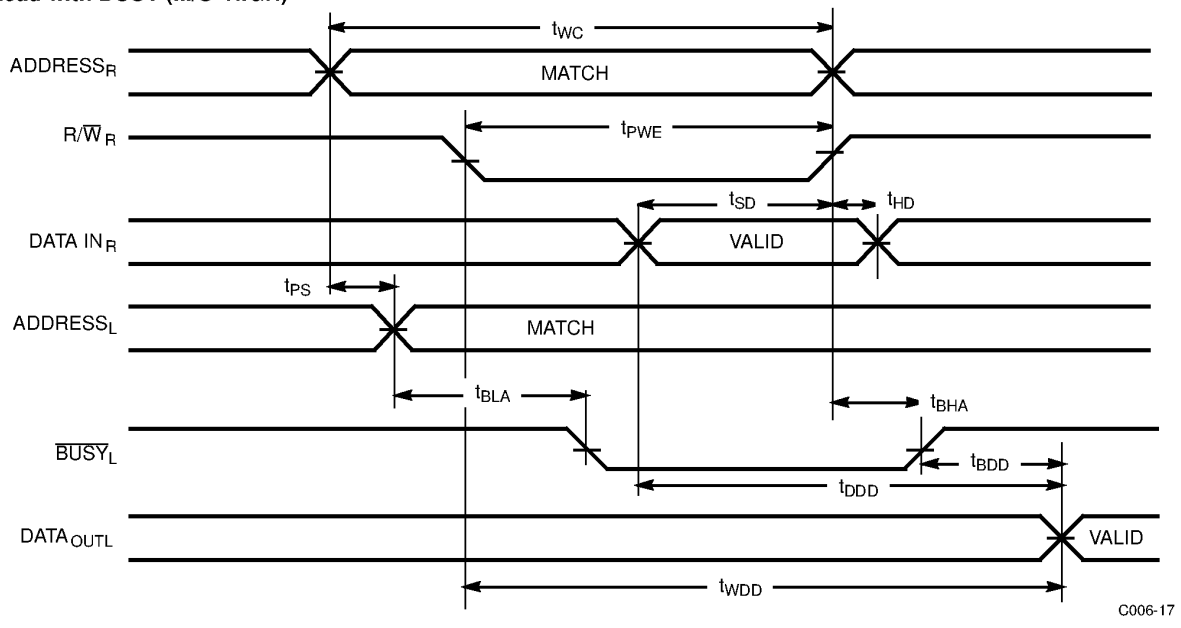
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Switching Waveforms (continued)

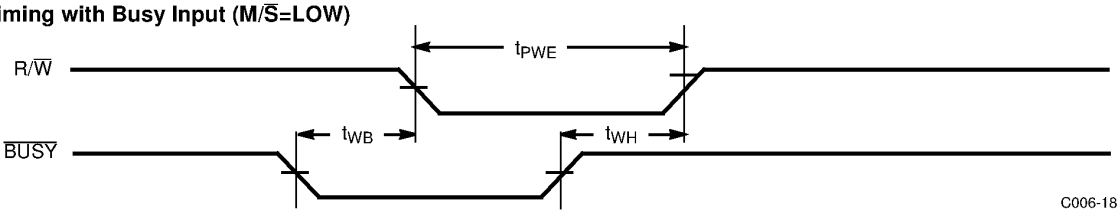
Semaphore Contention [26,27,28]



Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[19]



Write Timing with Busy Input (M/$\overline{S}$=LOW)



Notes:

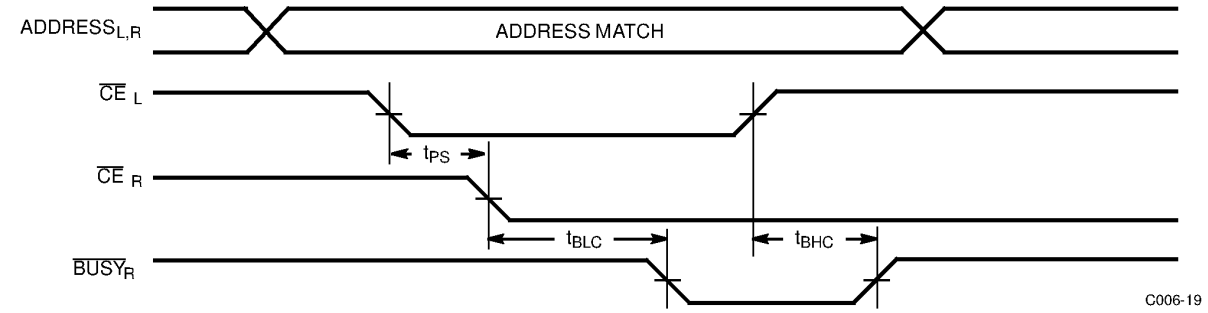
26. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
27. Semaphores are reset (available to both ports) at cycle start.
28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

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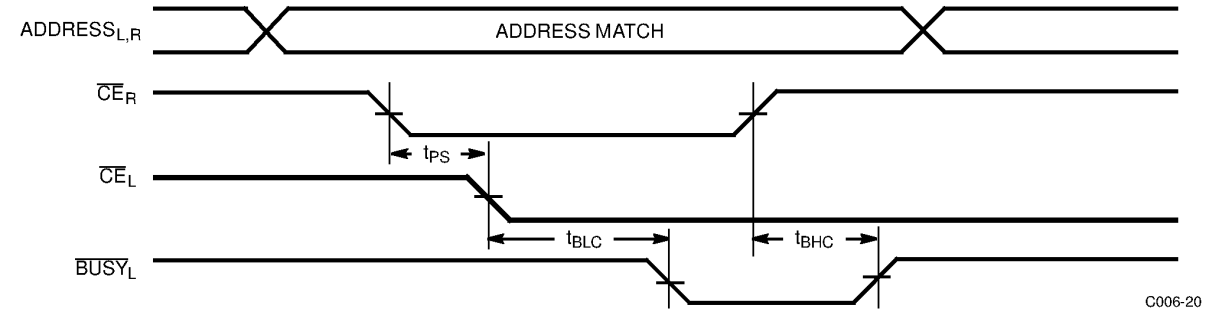
Switching Waveforms (continued)

Busy Timing Diagram No.1 ($\overline{CE}$ Arbitration)[29]

$\overline{CE}_L$ Valid First:

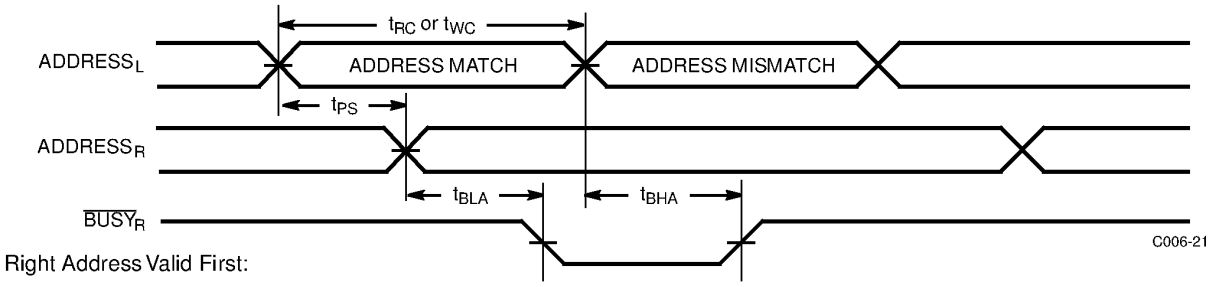


$\overline{CE}_R$ Valid First:

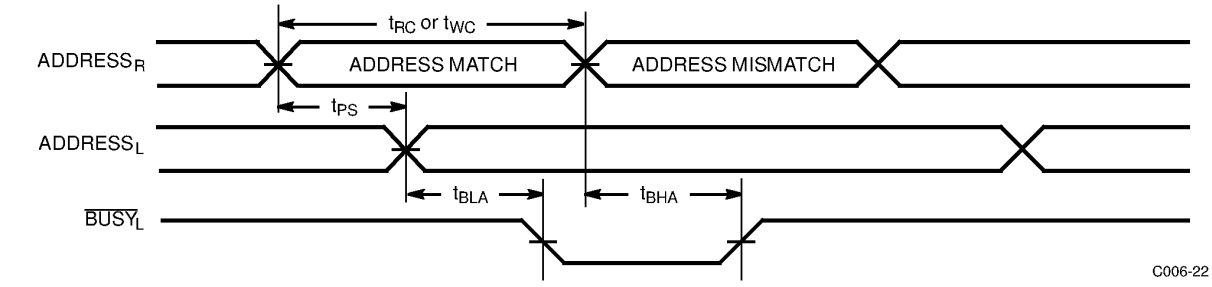


Busy Timing Diagram No.2 (Address Arbitration)[28]

Left Address Valid First:



Right Address Valid First:



Notes:

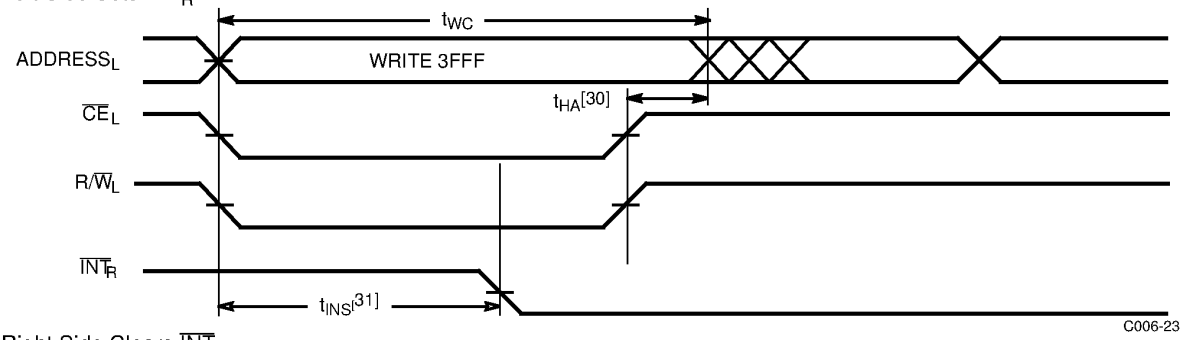
29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.
30. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
31. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

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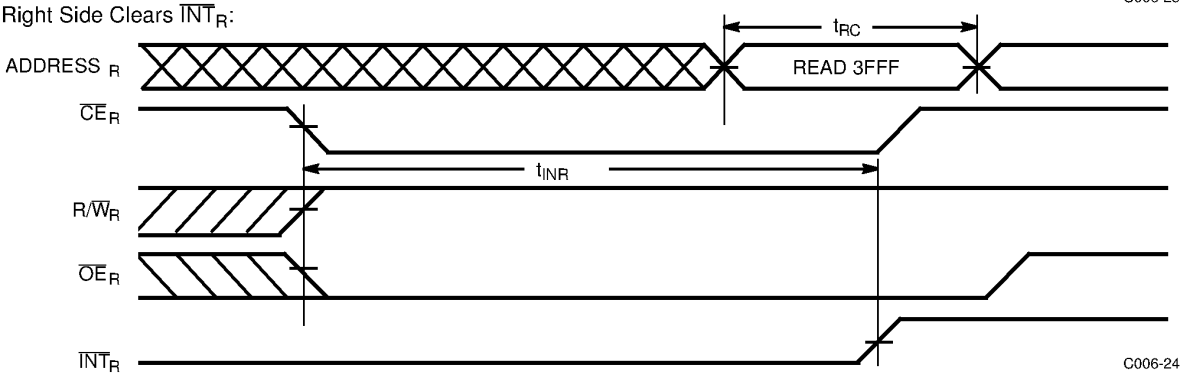
Switching Waveforms (continued)

Interrupt Timing Diagrams

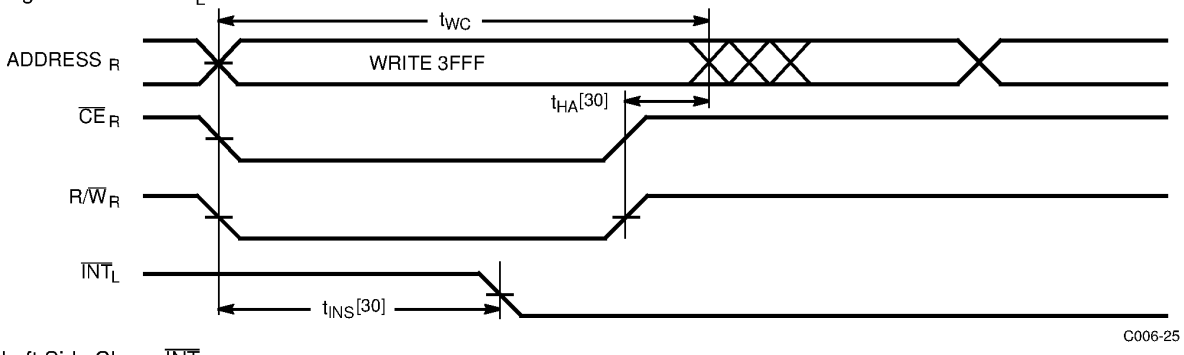
Left Side Sets $\overline{INT}_R$:



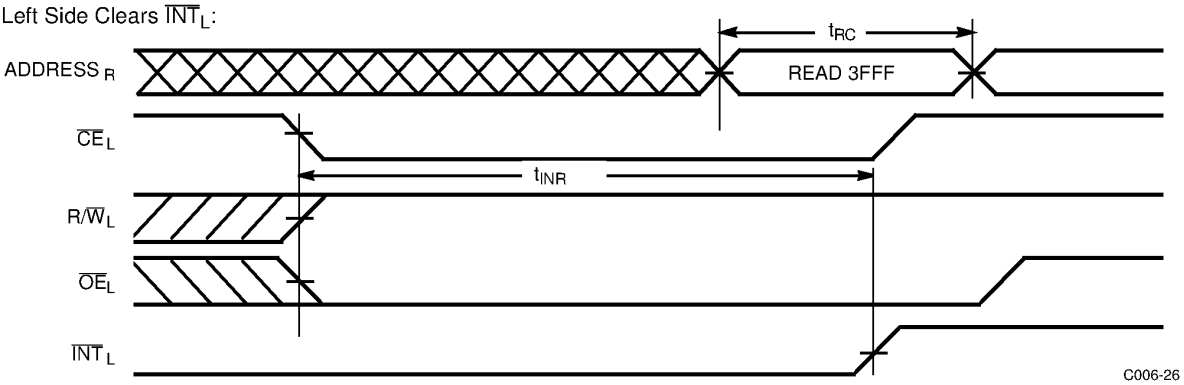
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



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Architecture

The CY7C006/016 consists of a an array of 16K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7C006/016 can function as a Master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7C006/016 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No.1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Table 1. Non-Contending Read/Write.

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_{0-7/8}$	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	_┌	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7C006/016 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports.When the left port writes to location 3FFF(HEX), the right port's interrupt flag ($\overline{INT}_R$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT}_L$) is accomplished when the right port writes to location 3FFE(HEX). This flag is cleared when the left port reads location 3FFE(HEX). The message at 3FFE(HEX) and 3FFF(HEX) is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT}_R$ and $\overline{INT}_L$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C006/016 provides on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components.Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLA}). Otherwise, the slave chip may begin a write cycle during a contention situation.When presented a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C006/016 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports.The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore.When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH).

	Left Port					Right Port				
Function	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0L-13L}	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0R-13R}	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	3FFE	X
Reset Left $\overline{INT}$	X	L	L	3FFE	H	X	L	L	X	X
Set Right $\overline{INT}$	L	L	X	3FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	3FFF	H

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Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access.When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All Semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 3. Semaphore Operation Example.

Function	$I/O_{0-7/8}$ Left	$I/O_{0-7/8}$ Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Ordering Information

16K x8 Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C006–15AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C006–25AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006–25AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C006–35AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006–35AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C006–55AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006–55AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

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Ordering Information (continued)

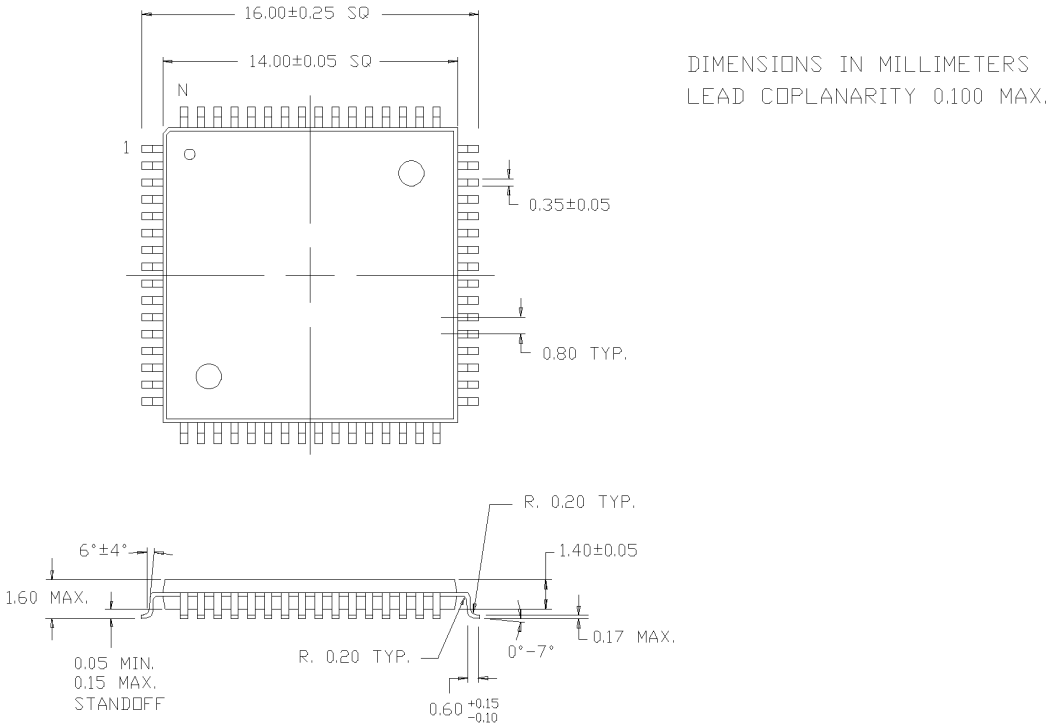
16K x9 Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C016–15AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C016–25AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016–25AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C016–35AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016–35AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C016–55AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016–55AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

Document #: 38-00416-A

Package Diagrams

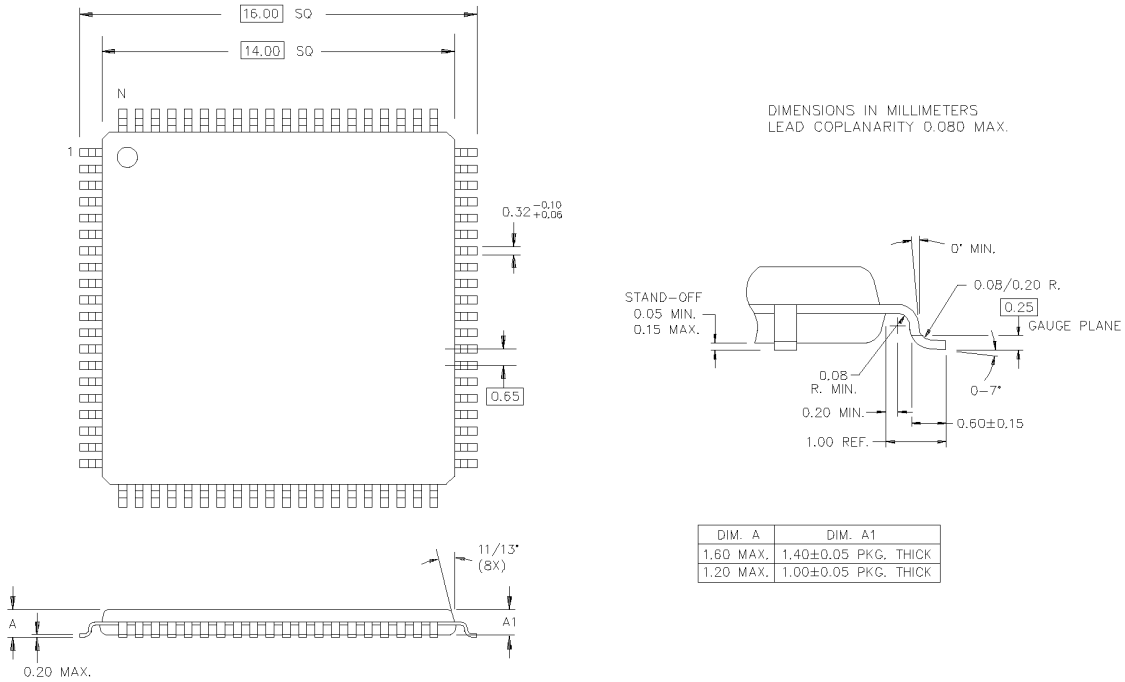
64-Lead Thin Plastic Quad Flat Pack A65



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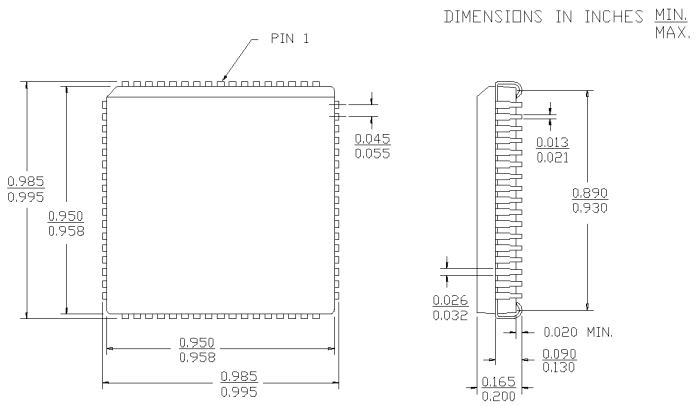
Package Diagrams (continued)

80-Pin Thin Plastic Quad Flat Pack A80



DIM. A	DIM. A1
1.60 MAX.	1.40±0.05 PKG. THICK
1.20 MAX.	1.00±0.05 PKG. THICK

68-Lead Plastic Leaded Chip Carrier J81



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CY7C130/CY7C131
CY7C140/CY7C141

1K x 8 Dual-Port Static Ram

Features

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **1K x 8 organization**
- **0.65-micron CMOS for optimum speed/power**
- **High-speed access: 15 ns**
- **Low operating power: I_{CC} = 90 mA (max.)**
- **Fully asynchronous operation**
- **Automatic power-down**
- **Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using slave CY7C140/CY7C141**
- **$\overline{BUSY}$ output flag on CY7C130/CY7C131; $\overline{BUSY}$ input on CY7C140/CY7C141**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 48-pin DIP (CY7C130/140), 52-pin PLCC and 52-pin TQFP**
- **Pin-compatible and functionally equivalent to IDT7130/IDT7140**

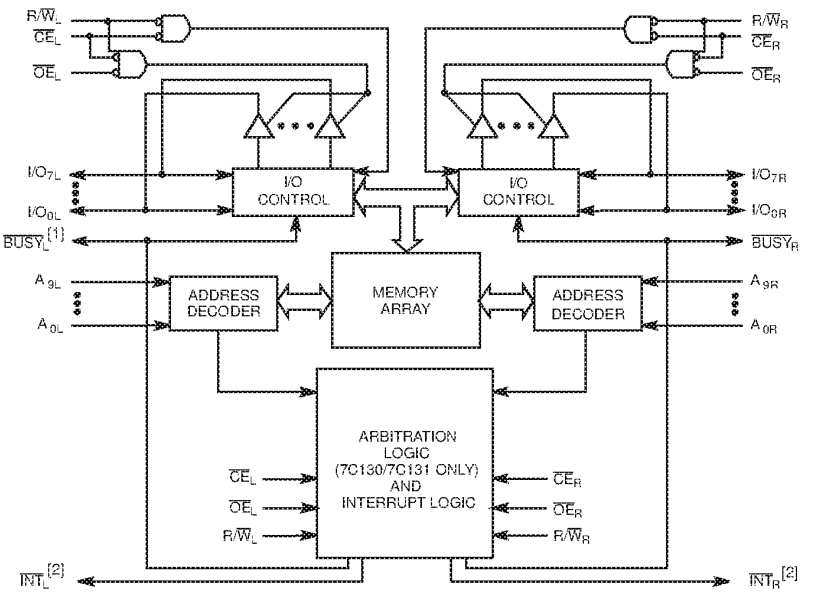
Functional Description

The CY7C130/CY7C131/CY7C140 and CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/ CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port, $\overline{BUSY}$ and $\overline{INT}$. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C130 and CY7C140 are available in 48-pin DIP. The CY7C131 and CY7C141 are available in 52-pin PLCC and PQFP.

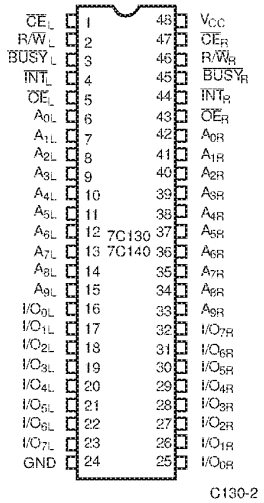
Logic Block Diagram



C130-1

Pin Configurations

DIP
Top View



C130-2

Notes:

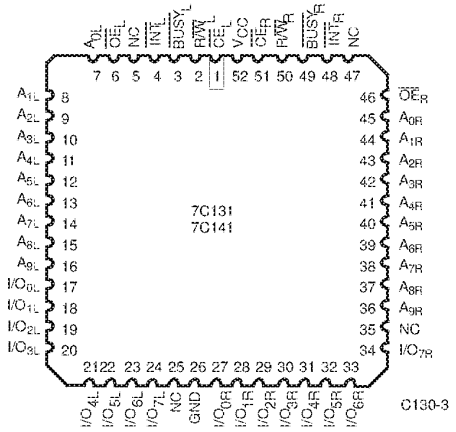
1. CY7C130/CY7C131 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor
   CY7C140/CY7C141 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs: pull-up resistor required

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May 1989 – Revised March 27, 1997

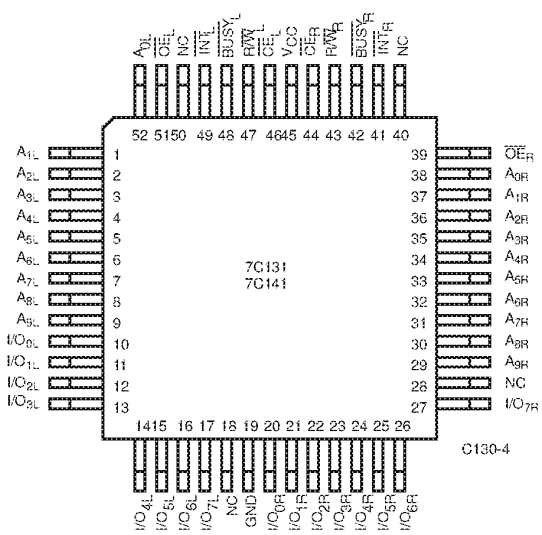
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Pin Configuration (continued)

PLCC
Top View



PQFP
Top View



Selection Guide

		7C131-15[3,4] 7C141-15	7C131-25[3] 7C141-25	7C130-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55
Maximum Access Time (ns)		15	25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	190	170	170	120	90	90
	Military				170	120	120
Maximum Standby Current (mA)	Com'l/Ind	75	65	65	45	35	35
	Military				65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage..... –3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%
Military[5]	–55°C to +125°C	5V ± 10%

Notes:

3. 15 and 25-ns version available only in PLCC/PQFP packages.
4. Shaded area contains preliminary information.
5. T_A is the "instant on" case temperature

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Electrical Characteristics Over the Operating Range[6]

Parameter	Description	Test Conditions		7C131-15[3,4] 7C141-15 Min.	7C131-15[3,4] 7C141-15 Max.	7C130-30[3] 7C131-25,30 7C140-30 7C141-25,30 Min.	7C130-30[3] 7C131-25,30 7C140-30 7C141-25,30 Max.	7C130-35 7C131-35 7C140-35 7C141-35 Min.	7C130-35 7C131-35 7C140-35 7C141-35 Max.	7C130-45,55 7C131-45,55 7C140-45,55 7C141-45,55 Min.	7C130-45,55 7C131-45,55 7C140-45,55 7C141-45,55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[7]			0.5		0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–5	+5	–5	+5	–5	+5	–5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[8, 9]	V_{CC} = Max., V_{OUT} = GND			–350		–350		–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[10]	Com'l		190		170		120		90	mA
			Mil						170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[10]	Com'l		75		65		45		35	mA
			Mil						65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[10]	Com'l		135		115		90		75	mA
			Mil						115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15		15	mA
			Mil						15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[10]	Com'l		125		105		85		70	mA
			Mil						105		85	

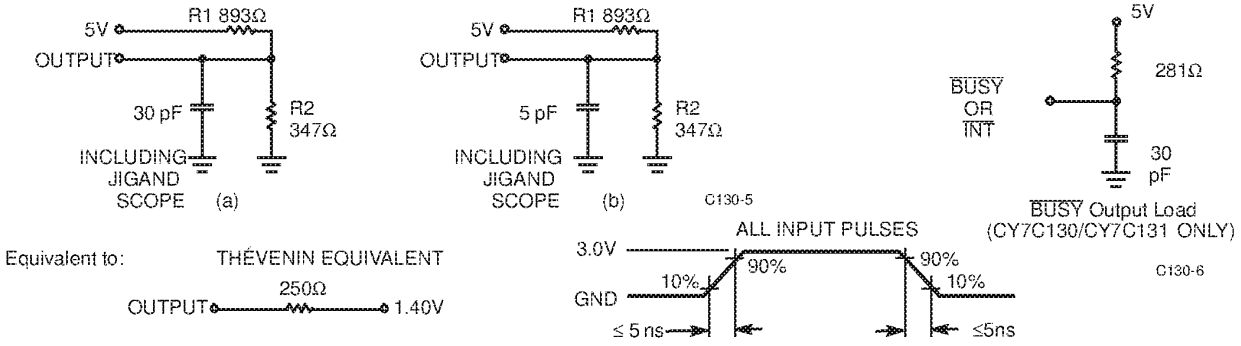
Notes:
6. See the last page of this specification for Group A subgroup testing information.
7. $\overline{BUSY}$ and $\overline{INT}$ pins only.
8. Duration of the short circuit should not exceed 30 seconds.
9. This parameter is guaranteed but not tested.
10. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.

Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

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AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[6,11]

Parameter	Description	7C131-15[3,4] 7C141-15		7C130-25[3] 7C131-25 7C140-25 7C141-25		7C130-30 7C131-30 7C140-30 7C141-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		25		30		ns
t_{AA}	Address to Data Valid[12]		15		25		30	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[12]		15		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[12]		10		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9,13, 14]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9,13, 14]		10		15		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9,13, 14]	3		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9,13, 14]		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up[9]	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down[9]		15		25		25	ns
WRITE CYCLE[15]								
t_{WC}	Write Cycle Time	15		25		30		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		25		ns
t_{AW}	Address Set-Up to Write End	12		20		25		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	12		15		25		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[14]		10		15		15	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[14]	0		0		0		ns

Notes:

11. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
12. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
13. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
14. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
15. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write

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Switching Characteristics Over the Operating Range[6,11] (continued)

Parameter	Description	7C131-15[3,4] 7C141-15		7C130-25[3] 7C131-25 7C140-25 7C141-25		7C130-30 7C131-30 7C140-30 7C141-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[16]		15		20		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[16]		15		20		20	ns
t_{PS}	Port Set Up for Priority	5		5		5		ns
t_{WB}[17]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		30		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		15		25		30	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 18		Note 18		Note 18	ns
t_{WDD}	Write Pulse to Data Delay		Note 18		Note 18		Note 18	ns
INTERRUPT TIMING								
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		15		25		25	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		15		25		25	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		15		25		25	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[16]		15		25		25	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[16]		15		25		25	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[16]		15		25		25	ns

Notes:
16. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
17. CY7C140/CY7C141 only.
18. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    $\overline{BUSY}$ on Port B goes HIGH.
    Port B's address is toggled.
    $\overline{CE}$ for Port B is toggled.
    R/$\overline{W}$ for Port B is toggled during valid read.

Switching Characteristics Over the Operating Range[6,11]

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid[12]		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[12]		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[12]		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9,13,14]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9,13,14]		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9,13,14]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9,13,14]		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up[9]	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down[9]		35		35		35	ns

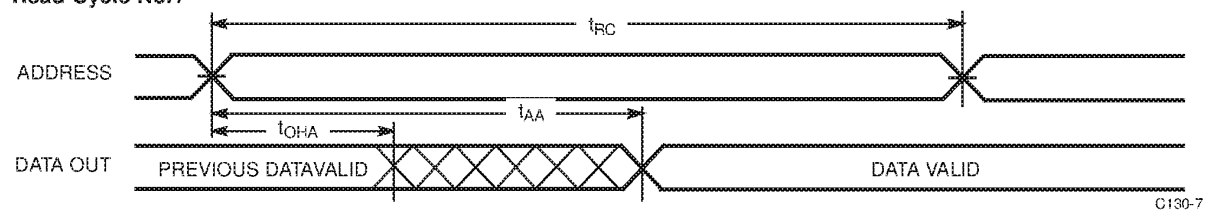
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Switching Characteristics Over the Operating Range[6,11] (continued)

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE[15]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	30		35		40		ns
t_{AW}	Address Set-Up to Write End	30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[14]		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[14]	0		0		0		ns
BUSY/INTERRUPT TIMING								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[16]		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[16]		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		ns
t_{WB}[17]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 18		Note 18		Note 18	ns
t_{WDD}	Write Pulse to Data Delay		Note 18		Note 18		Note 18	ns
INTERRUPT TIMING								
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[16]		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[16]		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[16]		25		35		45	ns

Switching Waveforms

Read Cycle No.1[19, 20]

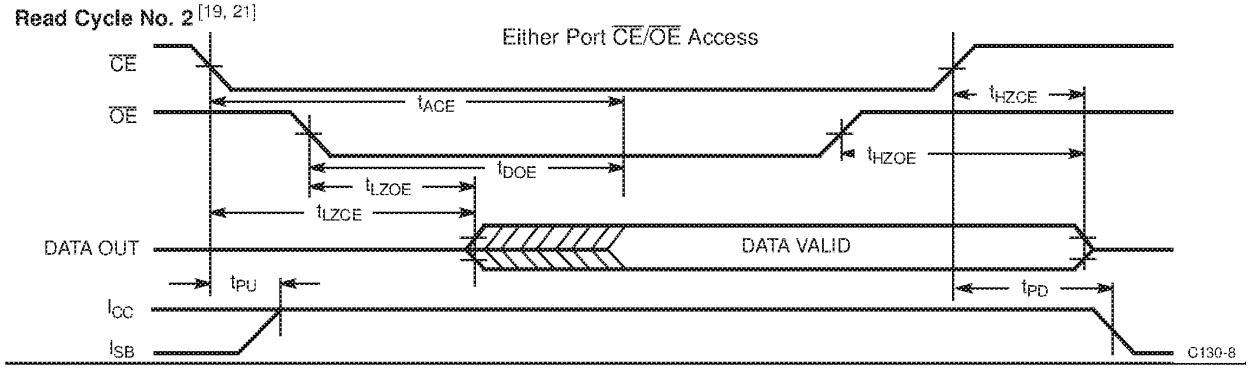


Notes:
19. R/$\overline{W}$ is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.

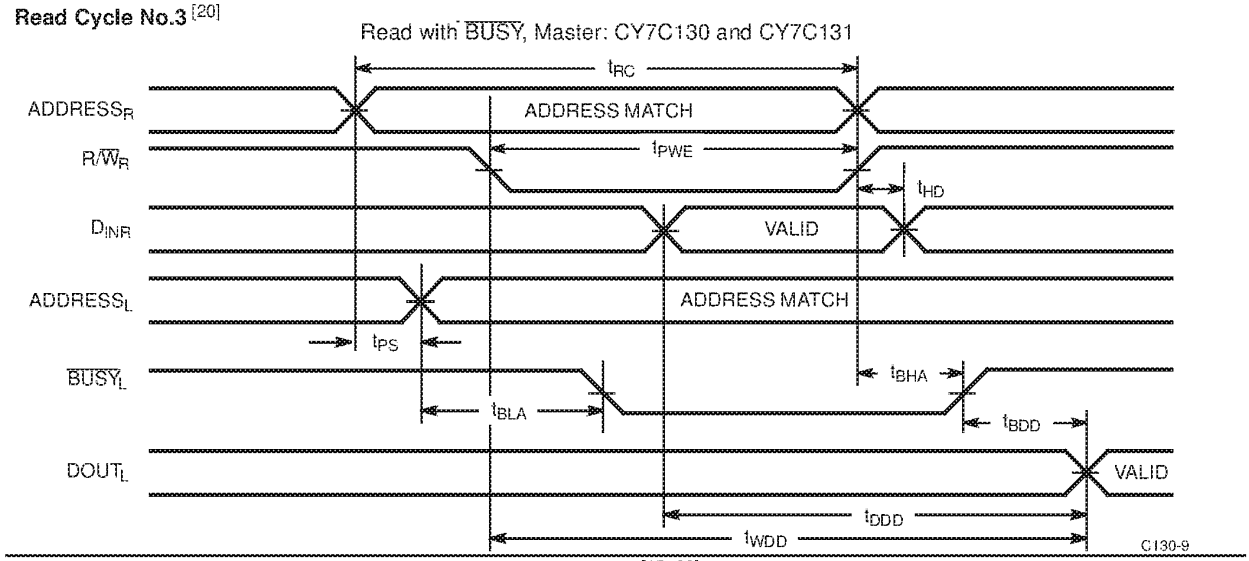
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Switching Waveforms (continued)

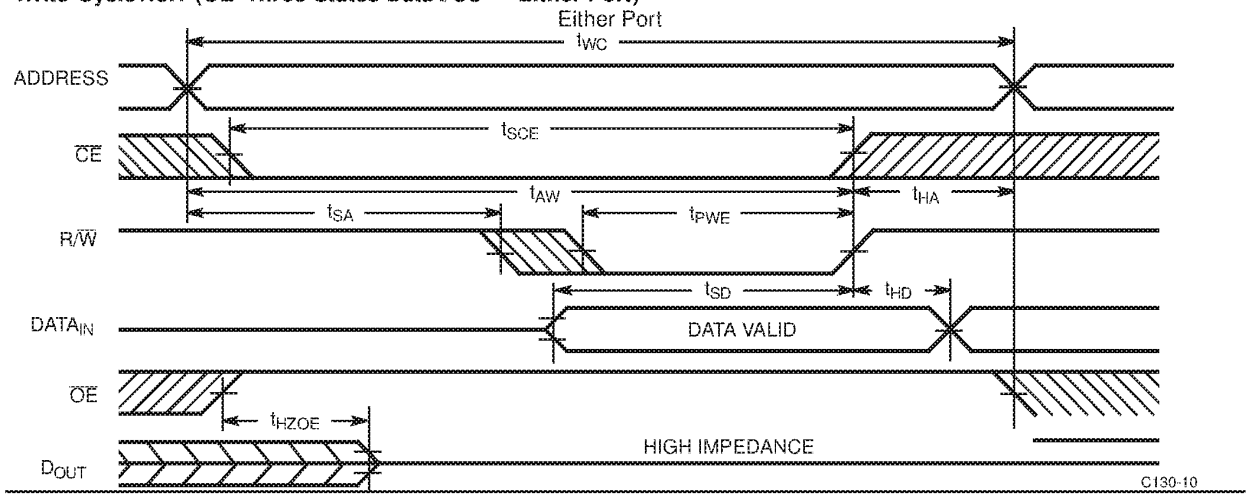
Read Cycle No. 2 [19, 21]



Read Cycle No.3 [20]



Write Cycle No.1 (OE Three-States Data I/Os - Either Port) [15, 22]



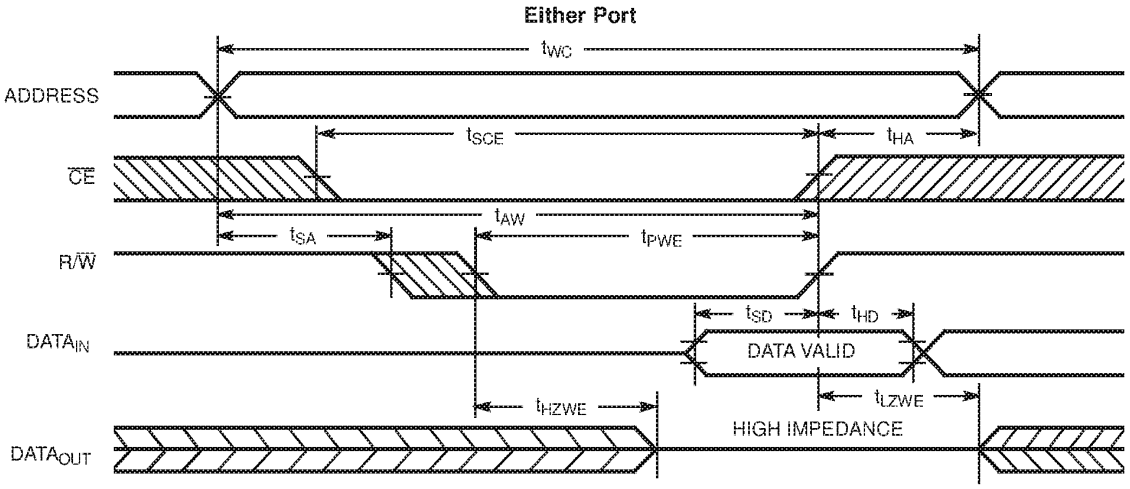
Notes:

21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

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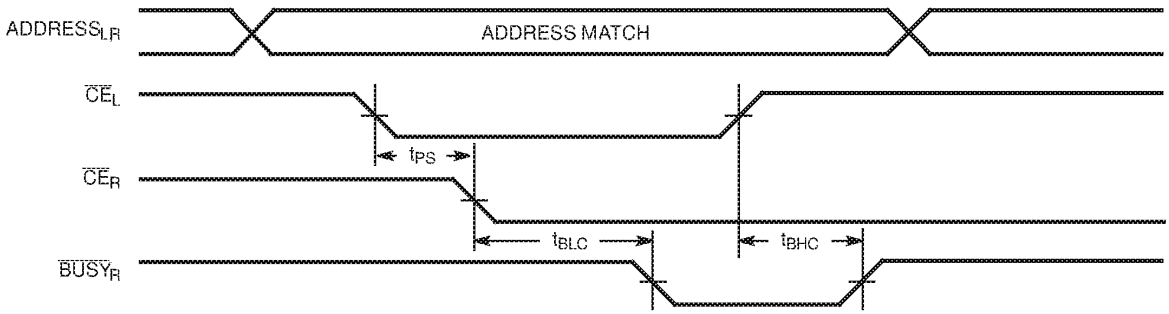
Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os - Either Port) [16, 23]

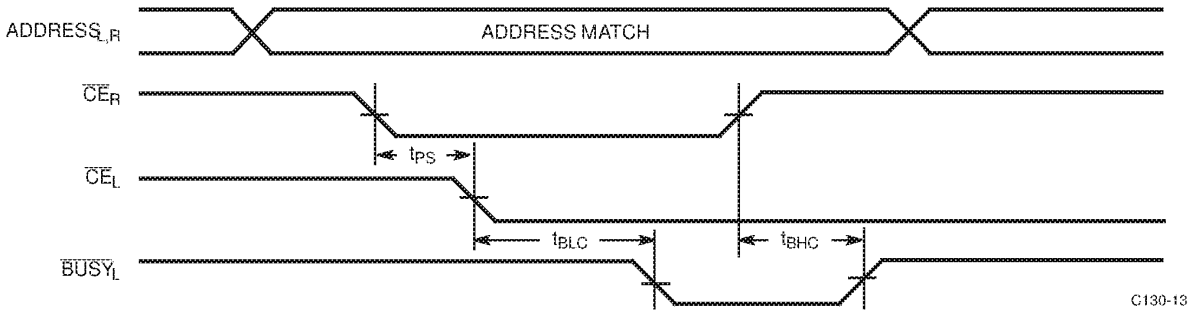


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



$\overline{CE}_R$ Valid First:



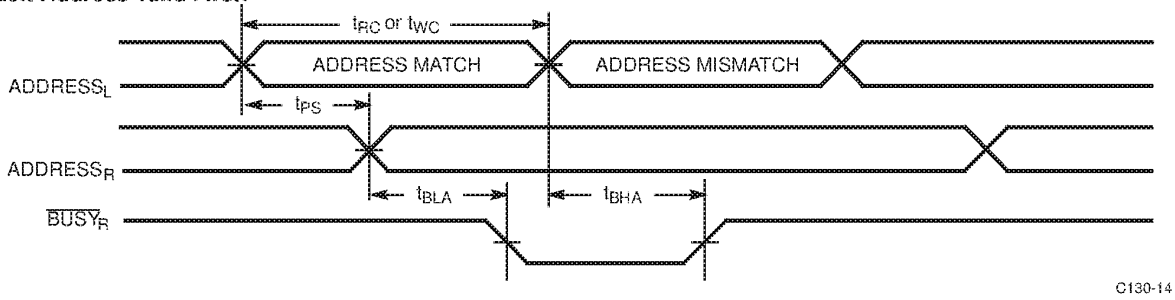
Note:
23. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state

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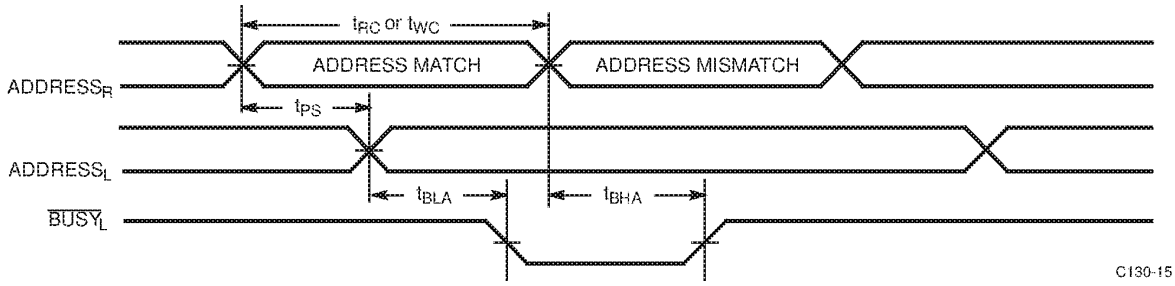
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:

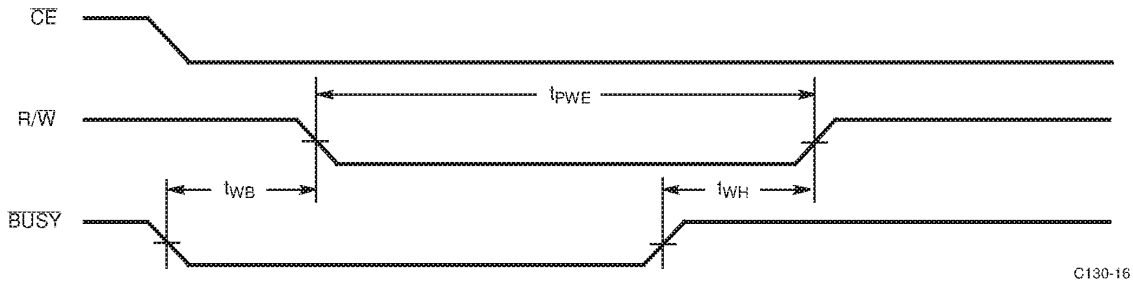


Right Address Valid First:



Busy Timing Diagram No. 3

Write with $\overline{BUSY}$ (Slave:CY7C140/CY7C141)

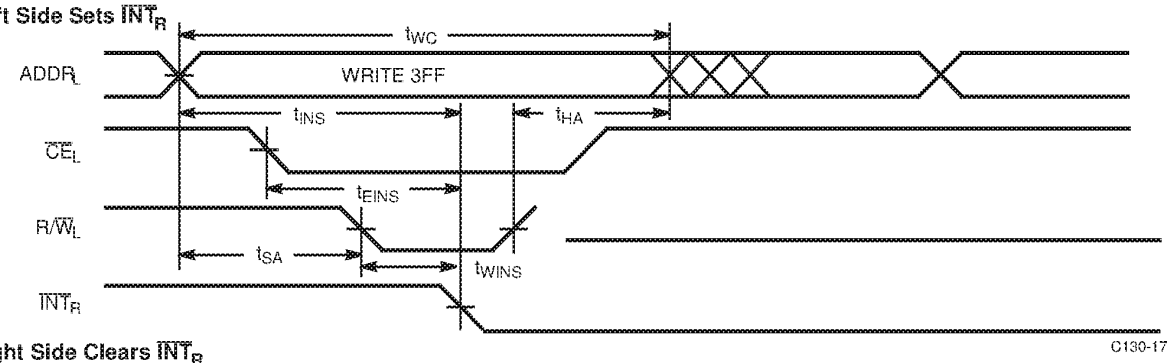


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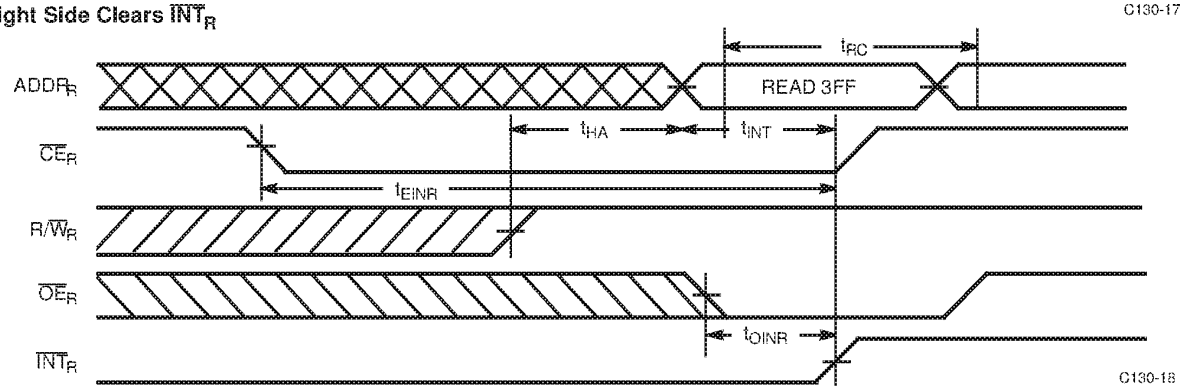
Switching Waveforms (continued)

Interrupt Timing Diagrams

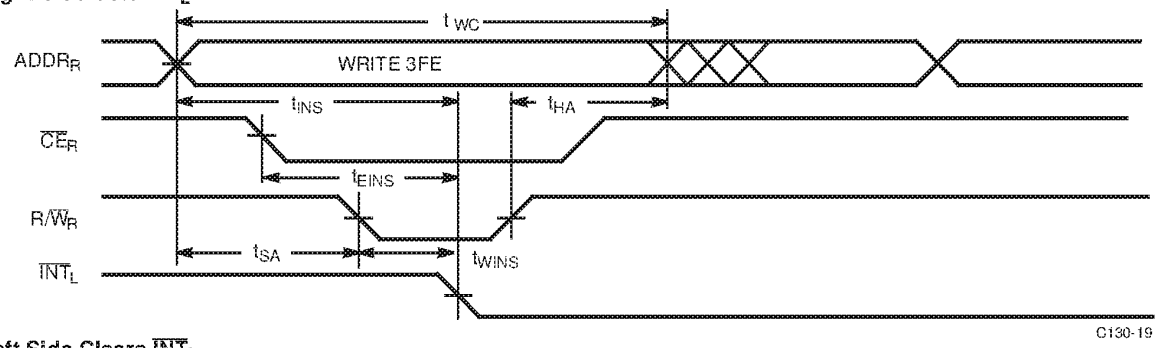
Left Side Sets $\overline{INT}_R$



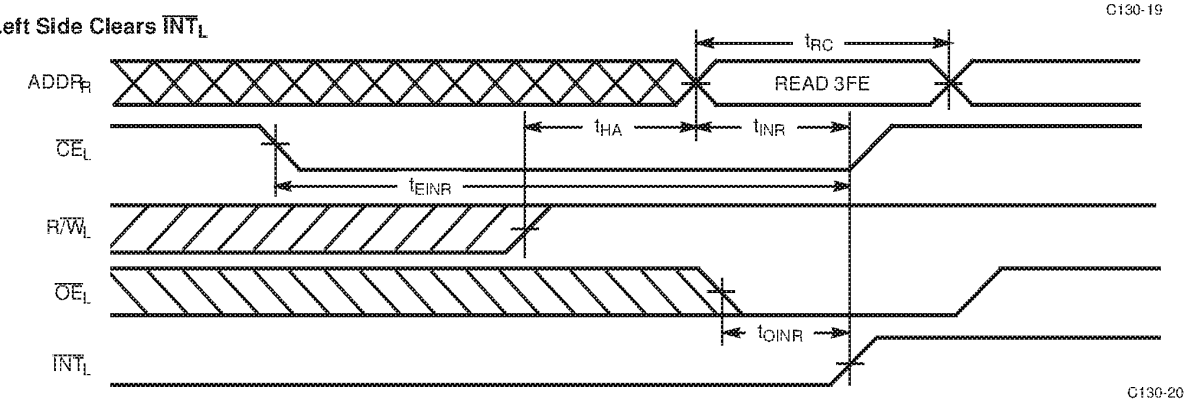
Right Side Clears $\overline{INT}_R$



Right Side Sets $\overline{INT}_L$

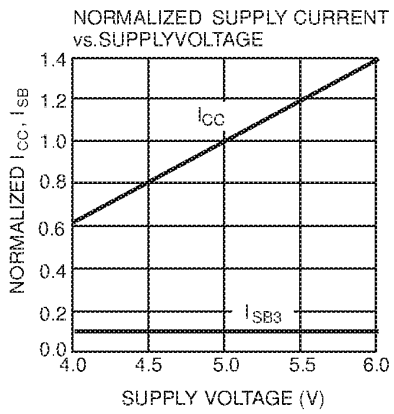


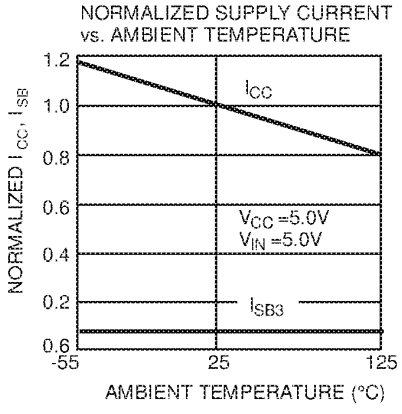
Left Side Clears $\overline{INT}_L$

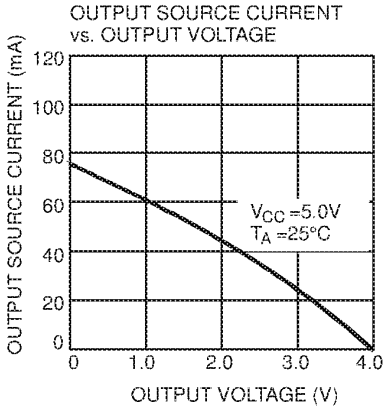


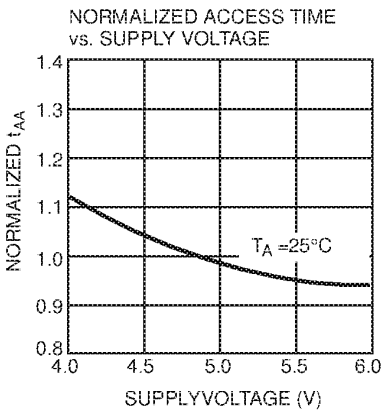
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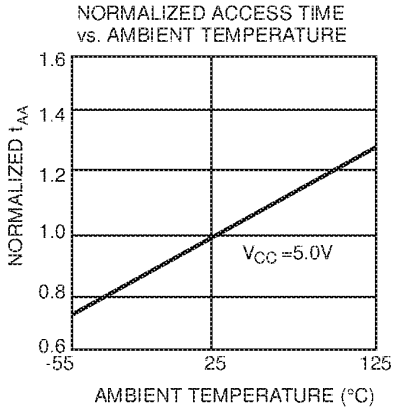
Typical DC and AC Characteristics

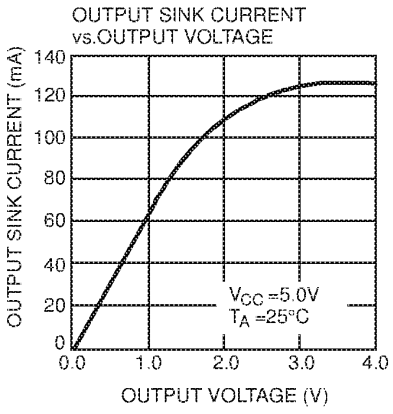


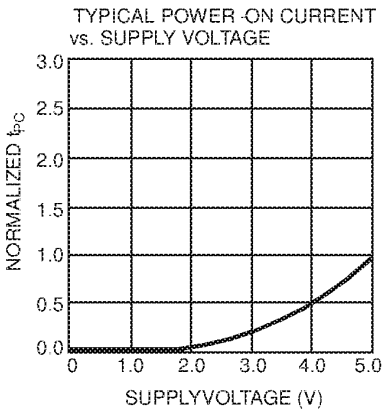


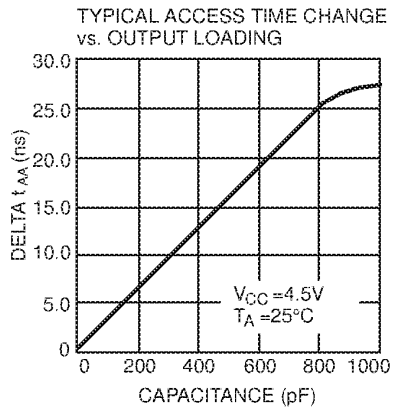


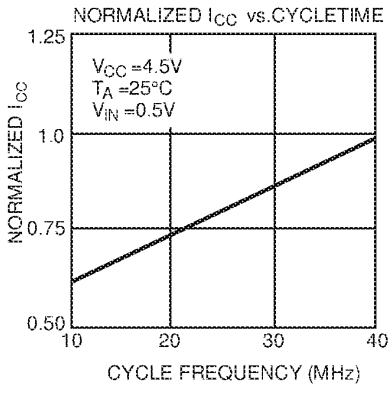












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Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C130-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C130-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C130-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C130-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C131-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C131-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C131-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C131-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-35NI	N52	52-Pin Plastic Quad Flatpack	
45	CY7C131-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-45NI	N52	52-Pin Plastic Quad Flatpack	
55	CY7C131-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-55NI	N52	52-Pin Plastic Quad Flatpack	

Shaded area contains preliminary information.

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Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C140-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C140-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C140-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C140-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C141-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C141-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C141-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C141-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-35NI	N52	52-Pin Plastic Quad Flatpack	
45	CY7C141-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-45NI	N52	52-Pin Plastic Quad Flatpack	
55	CY7C141-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-55NI	N52	52-Pin Plastic Quad Flatpack	

Shaded area contains preliminary information.

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MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[24]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

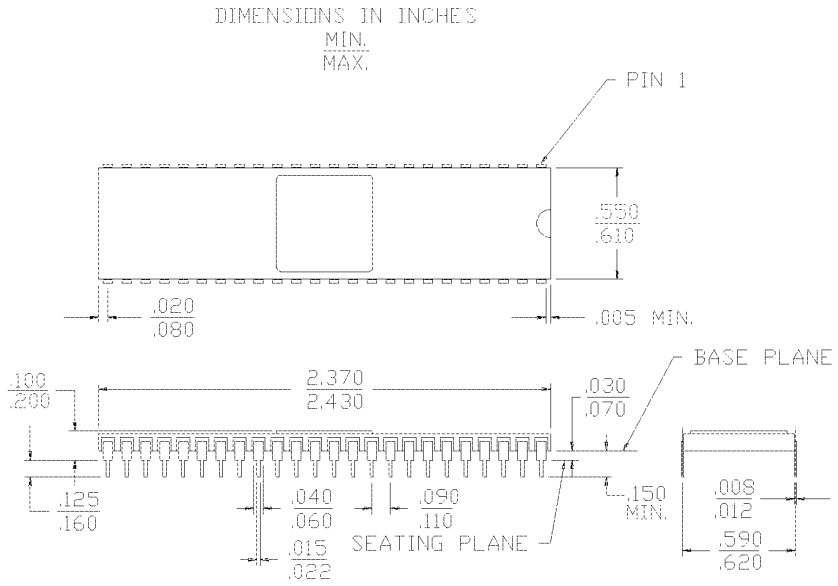
Note:
24. CY7C140/CY7C141 only.

Document #: 38-00027-L

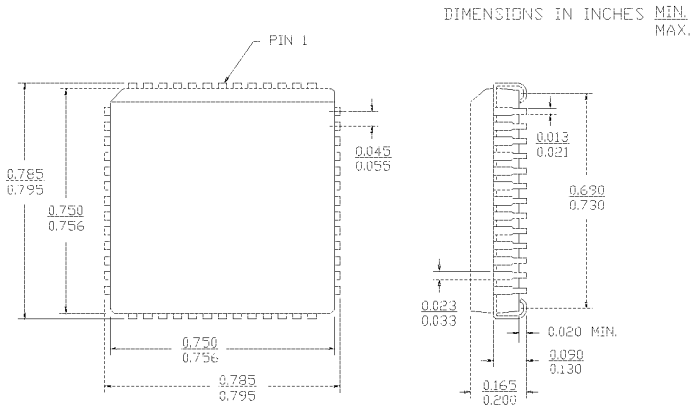
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Package Diagrams

48-Lead (600-Mil) Sidebraze DIP D26



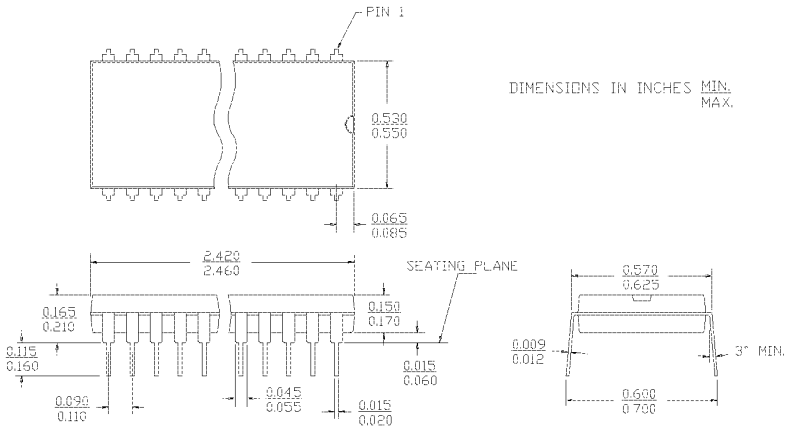
52-Lead Plastic Leaded Chip Carrier J69



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Package Diagrams (continued)

48-Lead (600-Mil) Molded DIP P25



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INITIAL RELEASE
Final Electrical Specifications

LTC1799

1kHz to 30MHz Resistor Set SOT-23 Oscillator

January 2001

FEATURES

- **One External Resistor Sets the Frequency**
- **1kHz to 30MHz Frequency Range**
- **SOT-23 Miniature Package**
- Frequency Error ≤1.5% 5kHz to 20MHz (T_A = 25°C)
- Frequency Error ≤2% 5kHz to 20MHz (T_A = 0°C to 70°C)
- ±40ppm/°C Temperature Stability
- 0.05%/V Supply Stability
- 50% ±1% Duty Cycle 1kHz to 2MHz
- 50% ±5% Duty Cycle 2MHz to 20MHz
- 1mA Typical Supply Current
- 100Ω CMOS Output Driver
- Operates from a Single 2.7V to 5.5V Supply

APPLICATIONS

- Low Cost Precision Oscillator
- Charge Pump Driver
- Switching Power Supply Clock Reference
- Clocking Switched Capacitor Filters
- Fixed Crystal Oscillator Replacement
- Ceramic Oscillator Replacement
- Small Footprint Replacement for Econ Oscillators

DESCRIPTION

The LTC®1799 is a precision oscillator that is easy to use and occupies very little PC board space. The oscillator frequency is programmed by a single external resistor (R_{SET}). The LTC1799 has been designed for high accuracy operation (≤1.5% frequency error) without the need for external trim components.

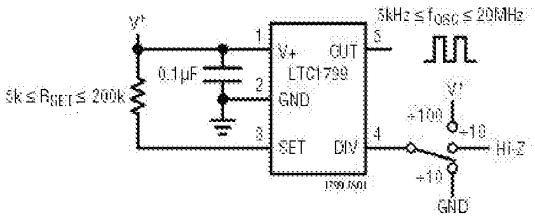
The LTC1799 operates with a single 2.7V to 5.5V power supply and provides a rail-to-rail, 50% duty cycle square wave output. The CMOS output driver ensures fast rise/fall times and rail-to-rail switching. The frequency-setting resistor can vary from 3.32k to 1M to select a master oscillator frequency between 100kHz and 30MHz (5V supply). The three-state DIV input determines whether the master clock is divided by 1, 10 or 100 before driving the output, providing three frequency ranges spanning 1kHz to 30MHz (5V supply). The LTC1799 features a proprietary feedback loop that linearizes the relationship between R_{SET} and frequency, eliminating the need for tables to calculate frequency. The oscillator can be easily programmed using the simple formula outlined below:

$$f_{OSC} = 10MHz \cdot \frac{10k}{N \cdot R_{SET}}, \quad N = \begin{cases} 100, & DIV\ PIN = V^+ \\ 10, & DIV\ PIN = Hi\text{-}Z \\ 1, & DIV\ PIN = GND \end{cases}$$

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

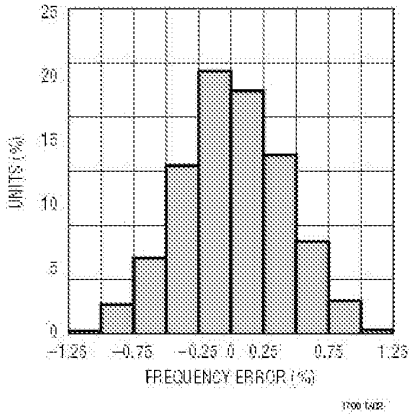
TYPICAL APPLICATION

Basic Connection



SOT-23 Actual Size

Typical Distribution of Frequency Error, T_A = 25°C



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

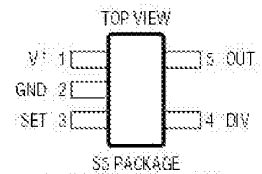
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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) to GND ..... –0.3V to 6V
DIV to GND ..... –0.3V to (V^+ + 0.3V)
SET to GND ..... –0.3V to (V^+ + 0.3V)
OUT to GND ..... –0.3V to (V^+ + 0.3V)
Operating Temperature Range
LTC1799C ..... 0°C to 70°C
LTC1799I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S5 PACKAGE
5-LEAD PLASTIC SOT-23

T_{JMAX} = 125°C, θ_{JA} = 256°C/W

ORDER PART NUMBER
LTC1799CS5 LTC1799IS5
S5 PART MARKING
LTND LTNE

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The λ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 2.7V to 5.5V, R_L=5k, C_L = 5pF, Pin 4 = V^+ unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Δf	Frequency Accuracy	V^+ = 5V	5kHz < f < 20MHz			±0.5	±1.5	%
			5kHz < f < 20MHz, LTC1799C	λ			±2	%
			5kHz < f < 20MHz, LTC1799I	λ			±2.5	%
	(Notes 2, 3)		1kHz < f < 5kHz			±2.5		%
			20MHz < f < 30MHz			±2.5		%
		V^+ = 3V	5kHz < f < 10MHz			±0.5	±1.5	%
			5kHz < f < 10MHz, LTC1799C	λ			±2	%
			5kHz < f < 10MHz, LTC1799I	λ			±2.5	%
			1kHz < f < 5kHz			±2.5		%
			10MHz < f < 20MHz			±2.5		%
R_{SET}	Frequency-Setting Resistor Range	Δf < 1.5%		V^+ = 5V	5		200	kΩ
				V^+ = 3V	10		200	kΩ
f_{MAX}	Maximum Frequency	Δf < 2.5%, Pin 4 = 0V		V^+ = 5V		30		MHz
				V^+ = 3V		20		MHz
f_{MIN}	Minimum Frequency	Δf < 2.5%, Pin 4 = V^+				1		kHz
ΔfΔT	Freq Drift Over Temp (Note 3)	R_{SET} = 31.6k		λ		±0.004		%/°C
ΔfΔV	Freq Drift Over Supply (Note 3)	V^+ = 2.7V to 5.5V, R_{SET} = 31.6k		λ		0.05	0.1	%/V
	Timing Jitter (Note 4)	Pin 4 = V^+				0.06		%
		Pin 4 = Floating				0.13		%
		Pin 4 = 0V				0.4		%
	Long-Term Stability of Output Frequency					300		ppm/√kHr
	Duty Cycle	Pin 4 = V^+ or Floating (DIV Either by 100 or 10)		λ	49	50	51	%
		Pin 4 = 0V (DIV by 1)		λ	45	50	55	%
V^+	Operating Supply Range			λ	2.7		5.5	V
I_S	Power Supply Current	R_{SET} = 200k, Pin 4 = V^+, R_L = 0	V^+ = 5V	λ		0.7	1.1	mA
		R_{SET} = 10k, Pin 4 = 0V, No Load	V^+ = 5V	λ			2.4	mA
			V^+ = 3V	λ			2	mA
V_{IH}	High Level DIV Input Voltage			λ	V^+ – 0.4			V
V_{IL}	Low Level DIV Input Voltage			λ			0.5	V
I_{DIV}	DIV Input Current	Pin 4 = V^+		λ		5	8	μA
		Pin 4 = 0V		λ		–5	8	μA

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ELECTRICAL CHARACTERISTICS

The λ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V⁺ = 2.7V to 5.5V, R_L=5k, C_L = 5pF, Pin 4 = V⁺ unless otherwise noted. All voltages are with respect to GND.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{OH}	High Level Output Voltage	V⁺ = 5V	I_{OH} = –1mA	λ	4.8	4.95		V
			I_{OH} = –4mA	λ	4.6	4.8		V
		V⁺ = 3V	I_{OH} = –1mA	λ	2.7	2.9		V
			I_{OH} = –4mA	λ	2.2	2.6		V
V_{OL}	Low Level Output Voltage	V⁺ = 5V	I_{OL} = 1mA	λ		0.05	0.15	V
			I_{OL} = 4mA	λ		0.2	0.4	V
		V⁺ = 3V	I_{OL} = 1mA	λ		0.1	0.3	V
			I_{OL} = 4mA	λ		0.4	0.7	V
t_r	OUT Rise Time (Note 5)	V⁺ = 5V	Pin 4 = V⁺ or Floating, R_L = 0			14		ns
			Pin 4 = 0V, R_L = 0			7		ns
		V⁺ = 3V	Pin 4 = V⁺ or Floating, R_L = 0			19		ns
			Pin 4 = 0V, R_L = 0			11		ns
t_f	OUT Fall Time (Note 5)	V⁺ = 5V	Pin 4 = V⁺ or Floating, R_L = 0			13		ns
			Pin 4 = 0V, R_L = 0			6		ns
		V⁺ = 3V	Pin 4 = V⁺ or Floating, R_L = 0			19		ns
			Pin 4 = 0V, R_L = 0			10		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Frequencies near 100kHz and 1MHz may be generated using two different values of R_{SET} (see the Table 1 in the Applications Information section). For these frequencies, the error is specified under the following assumption: 10k < R_{SET} ≤ 100k.

Note 3: Frequency error (defined as the deviation from the f_{OSC} equation) includes drift over temperature and over supply.

Note 4: Jitter is the ratio of the peak-to-peak distribution of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

Note 5: Output rise and fall times are measured between the 10% and 90% power supply levels. These specifications are based on characterization.

PIN FUNCTIONS

V⁺ (Pin 1): Voltage Supply (2.7V ≤ V⁺ ≤ 5.5V). This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane.

GND (Pin 2): Ground. Should be tied to a ground plane for best performance.

SET (Pin 3): Frequency-Setting Resistor Input. The value of the resistor connected between this pin and V⁺ determines the oscillator frequency. The voltage on this pin is held by the LTC1799 to approximately 1.1V below the V⁺ voltage. For best performance, use a precision metal film resistor with a value between 10k and 200k and limit the capacitance on this pin to less than 2pF.

DIV (Pin 4): Divider-Setting Input. This three-state input selects among three divider settings, determining the value of N in the frequency equation. Pin 4 should be tied to GND for the ÷1 setting, the highest frequency range. Floating Pin 4 divides the master oscillator by 10. Pin 4 should be tied to V⁺ for the ÷100 setting, the lowest frequency range. To detect a floating DIV pin, the LTC1799 attempts to pull the pin toward midsupply. Therefore, driving the DIV pin high requires sourcing approximately 5µA. Likewise, driving DIV low requires sinking 5µA. When floated, the DIV pin will be held near midsupply by these current sources. When it is floated, it is recommended that the DIV pin be bypassed by a 1nF capacitor or surrounded by a ground shield to prevent excessive coupling from other PCB traces.

OUT (Pin 5): Oscillator Output. This pin can easily drive 5kΩ or 10pF loads. Larger loads may cause inaccuracies due to supply bounce at high frequencies.

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APPLICATIONS INFORMATION

Selecting the Divider Setting and Resistor

The LTC1799's master oscillator has a frequency range spanning 0.1MHz to 30MHz. However, accuracy may suffer if the master oscillator is operated at greater than 10MHz with a supply voltage lower than 4V. A programmable divider extends the frequency range to greater than three decades. Table 1 describes the recommended frequencies for each divider setting. Note that the ranges overlap; at some frequencies there are two divider/resistor combinations that result in the desired frequency.

In general, any given oscillator frequency (f_{OSC}) should be obtained using the lowest master oscillator frequency. Lower master oscillator frequencies use less power and are more accuate. For instance, f_{OSC} = 100kHz can be obtained by either R_{SET} = 10k, N = 100, master oscillator = 10MHz or R_{SET} = 100k, N = 10, master oscillator = 1MHz. The R_{SET} = 100k is preferred for lower power and better accuracy.

Table 1. Frequency Range vs Divider Setting

DIVIDER SETTING			FREQUENCY RANGE
÷1	⇒	DIV (Pin 4) = GND	>500kHz*
÷10	⇒	DIV (Pin 4) = Floating	50kHz to 1MHz
÷100	⇒	DIV (Pin 4) = V+	<100kHz

*At master oscillator frequencies greater than 10MHz (R_{SET} < 10kΩ), the LTC1799 may suffer reduced accuracy with a supply voltage less than 4V.

After choosing the proper divider setting, determine the correct frequency-setting resistor. Because of the linear corresponderce between oscillation period and resistance, a simple equation relates resistance with frequency.

$R_{SET} = 10k \bullet [10MHz/(N \bullet f_{OSC})]$, N = 1, 10, 100
(R_{SETMIN} = 3.32k (5V Supply), 5k (3V Supply).
R_{SETMAX} = 1M)

Any resistor, R_{SET}, tolerance adds to the inaccuracy of the oscillator, f_{OSC}.

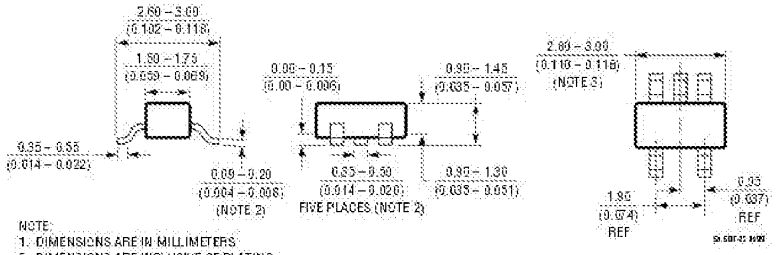
Settling Time

The settling time is proportional to R_{SET} and is approximately $t_{SETTLE} \approx R_{SET} \bullet (5\mu s/k\Omega)$. This parameter is guaranteed by design and not 100% tested.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S5 Package
5-Lead Plastic SOT-23
(LTC DWG # 05-08-1633)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
4. MOLD FLASH SHALL NOT EXCEED 0.254mm
5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)

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CY7C924ADX

200 MBaud HOTLink® Transceiver

Features

- Second generation HOTLink® technology
- Fibre channel and ESCON® compliant 8B/10B encoder/decoder
- 10 or 12-bit preencoded data path (raw mode)
- 8 or 10-bit encoded data transport (using 8B/10B coding)
- Synchronous or asynchronous TTL parallel interface
- UTOPIA compatible host bus interface
- Embedded/bypassable 256-character synchronous FIFOs
- Integrated support for daisy-chain and ring topologies
- Domain or individual destination device addressing
- 50 to 200 MBaud serial signaling rate
- Internal PLLs with no external PLL components
- Dual differential PECL compatible serial inputs
- Dual differential PECL compatible serial outputs
- Compatible with fiber optic modules and copper cables
- Built-in self-test (BIST) for link testing
- Link quality indicator
- Single +5.0 V ±10% supply
- 100-pin TQFP
- 0.35 µ CMOS technology
- Pb-free package available

Functional Description

The 200 MBaud CY7C924ADX HOTLink Transceiver is a point-to-point communications building block allowing the transfer of data over high speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at speeds ranging between 50 and 200 MBaud. The transmit section accepts parallel data of selectable width and converts it to serial data, while the receiver section accepts serial data and converts it to parallel data of selectable width. Figure 1 illustrates typical connections between two independent host systems and corresponding CY7C924ADX parts. As a second generation HOTLink device, the CY7C924ADX provides enhanced levels of technology, functionality, and integration over the field proven CY7B923/933 HOTLink.

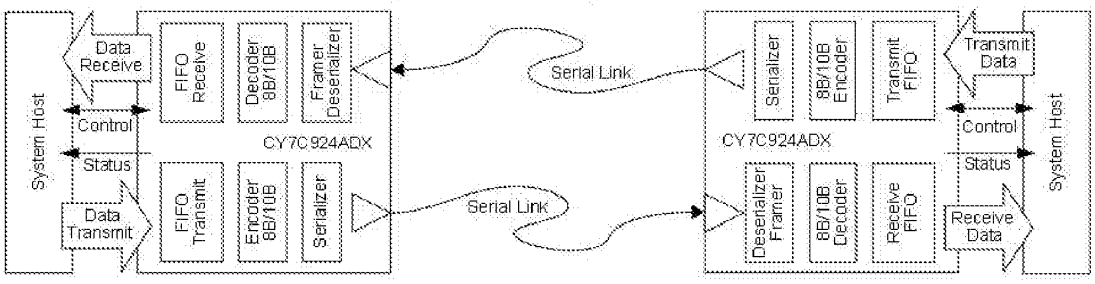
The transmit section of the CY7C924ADX HOTLink can be configured to accept either 8 or 10 bit data characters on each clock cycle, and stores the parallel data in an internal Transmit FIFO. Data is read from the Transmit FIFO and is encoded using an embedded 8B/10B encoder to improve its serial transmission characteristics. These encoded characters are then serialized and output from two Positive ECL (PECL) compatible differential transmission line drivers at a bit rate of 10 or 12 times the character rate.

The receive section of the CY7C924ADX HOTLink accepts a serial bit stream from one of two PECL compatible differential line receivers and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. The recovered bit stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are reconstructed into either 8 or 10 bit data characters, written to an internal Receive FIFO, and presented to the destination host system.

Systems that present externally encoded or scrambled data at the parallel interface may bypass the integrated 8B/10B encoder/decoder. The embedded FIFOs may also be bypassed to create a reference locked serial transmission link. For those systems requiring even greater FIFO storage capability, external FIFOs may directly couple to the CY7C924ADX device through the parallel interface without additional glue-logic.

You can configure the TTL parallel I/O interface as either a FIFO (configurable for UTOPIA emulation or for depth expansion through external FIFOs) or as a pipeline register extender. The FIFO configurations are optimized for transport of time-independent (asynchronous) 8 or 10 bit character oriented data across a link. A Built-In Self-Test (BIST) pattern generator and checker permits at-speed testing of the high speed serial data paths in both the transmit and receive sections, and across the interconnecting links. HOTLink devices are ideal for a variety of applications where parallel interfaces can be replaced with high speed, point-to-point serial links. Some applications include interconnecting workstations, backplanes, servers, mass storage, and video transmission equipment.

Figure 1. HOTLink System Connections



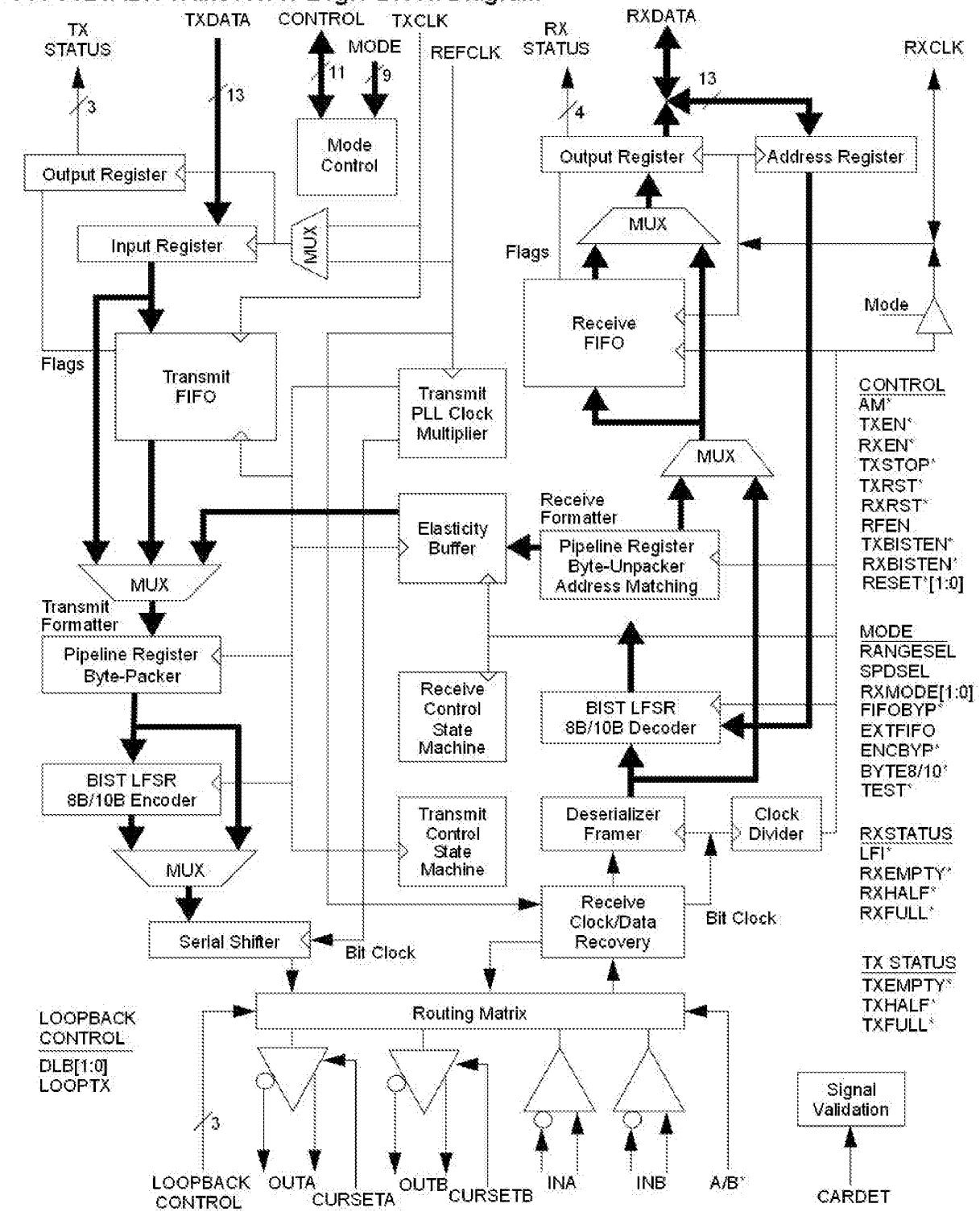
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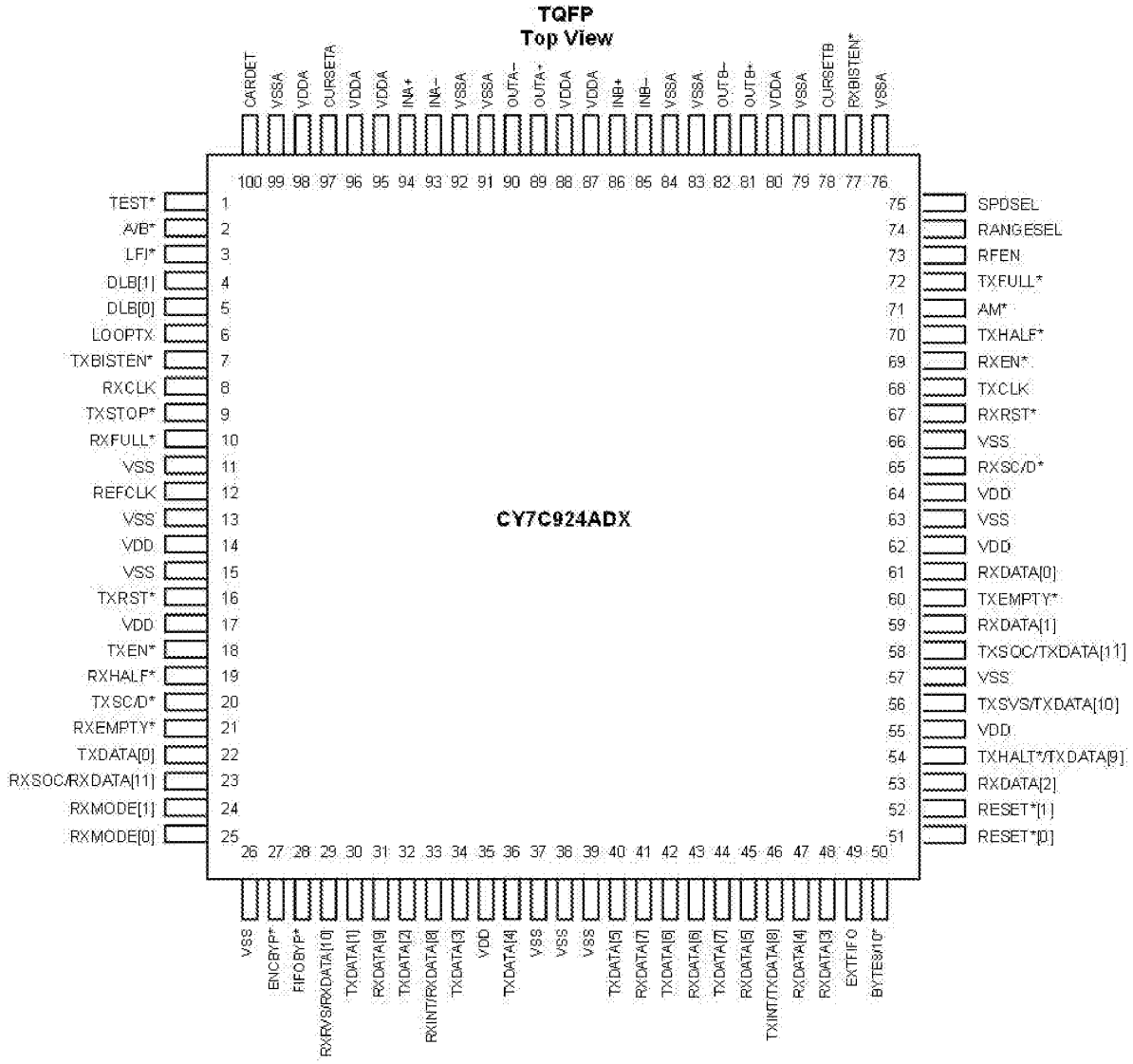
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CY7C924ADX Transceiver Logic Block Diagram



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Pin Configuration



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Pin Descriptions
CY7C924ADX HOTLink Transceiver

Pin Number	Name	I/O Characteristics	Signal Description
Transmit Path Signals			
44, 42, 40, 36, 34, 32, 30, 22	TXDATA[7:0]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull Up	**Parallel Transmit Data Input.** Bus width can be configured to accept either 8 or 10 bit characters. When the encoder is bypassed (ENCBYP* is LOW), TXDATA[7:0] functions as the least significant eight bits of the 10 or 12 bit preencoded transmit character.
46	TXINT/ TXDATA[8]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull Up	**Transmit Interrupt Input.** This input is only interpreted if both the Transmit FIFO and encoder are enabled (FIFOBYP* and ENCBYP* are HIGH). Any state change (0→1 or 1→0) in TXINT, forces a character into the transmit encoder and shifter before accessing the next Transmit FIFO contents. This signal passes around, not through, the Transmit FIFO. When TXINT transitions from 0→1, a C0.0 (K28.0) special code is sent. When TXINT transitions from 1→0, a C3.0 (K28.3) special code is sent. These special codes force a similar signal transition on the RXINT output of an attached CY7C924ADX HOTLink Transceiver. When the Transmit FIFO is bypassed and the encoder is enabled (FIFOBYP* is LOW and ENCBYP* is HIGH), this input is ignored. When the Transmit FIFO is bypassed and the encoder is bypassed (FIFOBYP* and ENCBYP* are LOW), TXDATA[8] functions as the 9th bit of the 10 or 12 bit preencoded transmit character.
54	TXHALT*/ TXDATA[9]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull Up	**Transmit FIFO Halt Immediate Input.** When the Transmit FIFO and the encoder are enabled (FIFOBYP* and ENCBYP* are HIGH) and TXHALT* asserts LOW, data transmission from the FIFO is suspended and the HOTLink transmits idle characters (K28.5). During this time, data can still be loaded into the FIFO. When TXHALT* is deasserted HIGH, normal data processing proceeds. When the encoder is bypassed (ENCBYP* is LOW), TXDATA[9] always functions as the tenth bit of the 10 or 12 bit preencoded transmit character. When the Transmit FIFO is bypassed and the encoder is enabled (FIFOBYP* is LOW and ENCBYP* is HIGH), this input is ignored
56	TXSVS/ TXDATA[10]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull Up	**Transmit Send Violation Symbol Input.** When the encoder is enabled and the Transmit FIFO is enabled (ENCBYP* and FIFOBYP* are HIGH), this input is interpreted along with TXSOC and TXSC/D* (see Table 2 on page 16 for details). When the Transmit FIFO is disabled (FIFOBYP* is LOW) and the TXSVS bit is set, the character on the TXDATA is ignored and a C0.7 exception is sent instead. When the encoder is bypassed and in 10 bit mode (ENCBYP* and BYTE8/10* are LOW), TXDATA[10] functions as the eleventh bit of the 12 bit preencoded transmit character. When the Encoder is bypassed and in 8 bit mode (ENCBYP* is LOW and BYTE8/10* is HIGH), this input is ignored.
58	TXSOC/ TXDATA[11]	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull Up	**Transmit Start of Cell Input.** When the Transmit FIFO and encoder are enabled (ENCBYP* and FIFOBYP* are HIGH), this input is a message frame delimiter that indicates the beginning of a data packet. It is interpreted along with TXSVS and TXSC/D* (see Table 2 for details). When the Transmit FIFO is bypassed (FIFOBYP* is LOW) and the encoder is enabled (ENCBYP* is HIGH) this input is ignored. When in 12 bit encoder bypass mode (ENCBYP* and BYTE8/10* are LOW), TXDATA[11] functions as the twelfth bit (MSB) of the 12 bit preencoded transmit character. When the encoder is bypassed and in 8 bit mode (ENCBYP* is LOW and BYTE8/10* is HIGH), this input is ignored.

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Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin Number	Name	I/O Characteristics	Signal Description
20	TXSC/D*	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull Up	**Transmit Special Character or Data Select Input.** When the Transmit FIFO is enabled and the encoder is enabled (FIFOBYP* and ENCBYP* are HIGH), this input is interpreted along with TXSVS and TXSOC (see Table 2 on page 16 for details). When the Transmit FIFO is bypassed and encoding is enabled (FIFOBYP* is LOW and ENCBYP* is HIGH), this signal controls whether the TXDATA[7:0] is sent as a data or control character. When the encoder is bypassed (ENCBYP* is LOW) TXSC/D* is ignored.
18	TXEN*	TTL input, sampled on TXCLK↑ or REFCLK↑, Internal Pull Up	**Transmit Enable Input.** Data enable for the TXDATA[11:0] data bus write operations. Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). When the Transmit FIFO is enabled (FIFOBYP* is HIGH) and TXEN* is asserted, data loads into the FIFO on every rising edge of TXCLK. When TXEN* is deasserted with TXHALT* and TXSTOP* deasserted, data continues to read out of the Transmit FIFO and is sent serially until the FIFO empties. At this time, C5.0 (K28.5) idle characters are transmitted. When the Transmit FIFO is bypassed (FIFOBYP* is LOW) and TXEN* is asserted, the parallel data on the TXDATA bus is clocked in and transmitted on every appropriate REFCLK rising edge. When TXEN* is deasserted, the parallel data bus is ignored and C5.0 sync characters are transmitted instead.
9	TXSTOP*	TTL input, sampled on TXCLK↑, Internal Pull Up	**Transmit Stop on Start_Of_Cell Input.** While the Transmit FIFO and encoder are enabled (FIFOBYP* and ENCBYP* are HIGH), this signal is used to prevent queued data characters from being serially transmitted. While TXSTOP* is deasserted, data flows through the Transmit FIFO without interruption. When TXSTOP* is asserted, data transfers continue until a TXSOC bit is detected in the character stream, at which point data transmission ceases. When transmission is stopped, C5.0 (K28.5) characters are sent instead. If data transmission is suspended due to a SOC character, pulsing TXSTOP* deasserted then asserted will allow only the next cell (delimited by SOC bits) to be transmitted. When the Transmit FIFO is bypassed (FIFOBYP* = LOW) TXSTOP* has no function. When the Transmit FIFO is enabled (FIFOBYP* is HIGH) and the encoder is bypassed (ENCBYP* is LOW), TXDATA[9]/TXHALT* is a data input and not TXHALT*. In this mode, the TXSOC bit is not interpreted and the TXSTOP* input assumes the same operation as TXHALT*. When TXSTOP* is asserted, data reads from the Transmit FIFO are suspended and alternating disparity 10 bit equivalents of C5.0 are transmitted instead.
68	TXCLK	TTL clock input, Internal Pull Up	**Transmit FIFO Clock.** The input clock for the parallel interface when the Transmit FIFO is enabled (FIFOBYP* is HIGH). Samples all Transmit FIFO related interface signals.
72	TXFULL*	3-state TTL output, changes following TXCLK↑ or REFCLK↑	**Transmit FIFO Full Status Flag.** Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). The TXFULL* output is enabled when AM* is asserted, otherwise it is High-Z. When the Transmit FIFO is enabled (FIFOBYP* is HIGH), TXFULL* indicates a Transmit FIFO full condition. When TXFULL* is first asserted, the Transmit FIFO accepts up to eight additional write cycles without data loss. When the Transmit FIFO is bypassed (FIFOBYP* is LOW), with RANGESEL HIGH or SPDSEL LOW, TXFULL* toggles at half the REFCLK rate to provide a character rate indication.

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Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin Number	Name	I/O Characteristics	Signal Description
70	TXHALF*	3-state TTL output, changes following TXCLK↑ or REFCLK↑	**Transmit FIFO Half-full Status Flag.** The TXHALF* flag is always active LOW, regardless of the EXTFIFO* setting. When the Transmit FIFO is enabled, TXHALF* is asserted LOW when the Transmit FIFO is half full or more (128 characters). TXHALF* is only set to High-Z state by the assertion of RESET*[1:0] LOW.
60	TXEMPTY*	3-state TTL output, changes following TXCLK↑ or REFCLK↑	**Transmit FIFO Empty Status Flag.** Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). The TXEMPTY* output is enabled when AM* is asserted, otherwise it is High-Z When the Transmit FIFO is enabled (FIFOBYP* is HIGH), TXEMPTY* is asserted either when no data has been loaded into the Transmit FIFO, or when the Transmit FIFO has been emptied by either a Transmit FIFO reset or by the normal transmission of the FIFO contents. When the Transmit FIFO is bypassed (FIFOBYP* is LOW), TXEMPTY* is asserted to indicate that the transmitter can accept data. When TXBISTEN* is asserted LOW, TXEMPTY* becomes the transmit BIST-progress indicator (regardless of the logic state of FIFOBYP*). In this mode TXEMPTY* is asserted for one TXCLK or REFCLK period at the end of each transmitted BIST sequence, depending on the FIFOBYP* setting.
16	TXRST*	TTL input, internal pull-up, sampled on TXCLK↑, Internal Pull Up	**Transmit FIFO Reset.** When TXRST* is asserted for eight or more TXCLK cycles, a reset operation begins on the Transmit FIFO. This input is ignored when the Transmit FIFO is bypassed.
7	TXBISTEN*	TTL input, asynchronous, Internal Pull Up	**Transmitter BIST Enable.** When TXBISTEN* is LOW, the transmitter generates a 511-character repeating built-in self test (BIST) sequence, that can validate link integrity. The transmitter returns to normal operation when TXBISTEN* is HIGH. All Transmit FIFO read operations suspend when BIST is active.
Receive Path Signals			
41, 43, 45, 47, 48, 53, 59, 61	RXDATA[7:0]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	**Parallel Data Output and Serial Address Register Access.** These outputs change following the rising edge of RXCLK, when enabled to output data (the device is addressed by AM* and selected by RXEN*). The contents of this bus are interpreted differently based on the levels present on ENCBYP*, BYTE8/10*, RXSC/D*, and when accessing the Serial Address Register. When the decoder is bypassed (ENCBYP* is LOW), RXDATA[7:0] functions as the least significant eight bits of the 10 or 12 bit preencoded receive character.
33	RXINT/ RXDATA[8]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	**Receive Interrupt Output.** When the Receive FIFO and decoder are enabled (FIFOBYP* and ENCBYP* are HIGH) and a C0.0 (K28.0) special code is received, RXINT is set HIGH. When a C3.0 (K28.3) special code is received RXINT is set LOW. These special codes are generated in response to equivalent transitions on the TXINT input of an attached CY7C924ADX HOTLink transceiver. This signal is extracted before the Receive FIFO and (except for Receive Discard Policy 0) the associated command codes are not considered "data" to be entered into the Receive FIFO and are discarded. When the Receive FIFO is bypassed (FIFOBYP* is LOW) and the decoder is enabled (ENCBYP* is HIGH), this output has no function. When the decoder is bypassed (ENCBYP* is LOW), RXDATA[8] functions as the ninth bit of the 10 or 12 bit undecoded receive character.

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Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin Number	Name	I/O Characteristics	Signal Description
31	RXDATA[9]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	**Receive Data Output.** When the decoder is enabled in 10 bit mode (ENCBYP* is HIGH and BYTE8/10* is LOW), this output is the tenth bit (MSB) of the 10 bit decoded and unpacked data character. When the Decoder is enabled and in 8 bit mode this output is ignored. When the Decoder is bypassed (ENCBYP* is LOW), RXDATA[9] functions as the tenth bit of the 10 or 12 bit undecoded receive character.
29	RXRVS/ RXDATA[10]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑, Internal Pull Up	**Received Violation Symbol Indicator.** For data accesses with the Receive FIFO and decoder are enabled (FIFOBYP* and ENCBYP* are HIGH) this signal is used as an output. It is decoded in conjunction with RXSC/D* and RXSOC, according to Table 6 on page 23, to indicate the presence of specific Special Character codes in the received data stream. For data accesses with the Receive FIFO disabled and the Decoder enabled, this output indicates a code word violation detection on the serial inputs. When the Decoder is bypassed (ENCBYP* is LOW) and in 10 -bit mode (BYTE8/10* is LOW), RXDATA[10] functions as the eleventh bit of the 12 bit undecoded receive character. In 8 bit mode this output is unused and is driven LOW. RXRVS reports BIST pattern mismatches when RXBISTEN* is LOW. When accessing the Serial Address Register, this signal is a "read/write" control input. RXRVS LOW allows the host system to write the Serial Address Register (RXDATA[9:0] and RXSC/D* are inputs). RXRVS HIGH allows the host system to read the Serial Address Register (RXDATA[9:0] and RXSC/D* are outputs).
23	RXSOC/ RXDATA[11]	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	**Receive Start Of Cell.** When the Receive FIFO and decoder are enabled (FIFOBYP* and ENCBYP* are HIGH), this output is decoded in conjunction with RXSC/D* and RXRVS, according to Table 6, to indicate the presence of specific Special Character codes in the received data stream. When the Decoder is bypassed (ENCBYP* is LOW) and in 10 bit mode (BYTE8/10* is LOW), RXDATA[11] is the twelfth bit (MSB) of the 12 bit undecoded receive character. In 8 bit mode (BYTE8/10* is HIGH) this output is unused and is driven LOW.
65	RXSC/D*	Bidirectional TTL, changes following RXCLK↑, or sampled by RXCLK↑	**Received Special Character or Data Indicator.** For data accesses with the Receive FIFO and decoder enabled (FIFOBYP* and ENCBYP* are HIGH) this signal is an output. It is decoded in conjunction with RXSOC and RXRVS, in accordance with Table 6, to indicate the presence of specific Special Character codes in the received data stream. For data accesses with the Receive FIFO disabled and the decoder enabled, this output indicates that the parallel output RXDATA[7:0] is a Special Character code. When accessing the Serial Address Register, this signal is an input that selects the addressing mode. RXSC/D* HIGH configures the Serial Address Register for Unicast address matching. RXSC/D* LOW configures the Serial Address Register for Multicast address matching. When operated with the decoder bypassed (ENCBYP* is LOW) this pin has no function.

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Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin Number	Name	I/O Characteristics	Signal Description
69	RXEN*	TTL input, sampled on RXCLK↑, Internal Pull Up	**Receive Enable.** Data enable for the RXDATA[11:0] data bus write and read operations. Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). When the Receive FIFO is enabled (FIFOBYP* is HIGH) and RXEN* is asserted, data is read out of the FIFO on every rising edge of RXCLK. When RXEN* is deasserted, reads are inhibited and the RXDATA bus is not driven. When the Receive FIFO is bypassed (FIFOBYP* is LOW) and RXEN* is asserted, parallel data is clocked out Receive Output Register to the RXData bus on every RXCLK edge. When RXEN* is deasserted, the RXDATA bus is not driven. RXEN* also controls the read and write access to the Serial Address Register.
8	RXCLK	Bidirectional TTL clock, Internal Pull-Up	**Receive Clock.** When the Receive FIFO is enabled (FIFOBYP* is HIGH), this clock is the Receive interface *input* clock and is used to control Receive FIFO read, reset, and serial register access operations. When the Receive FIFO is bypassed (FIFOBYP* is LOW), this clock is *output* continuously at the character rate of the data being received (1/10 or 1/12 of the serial bit rate).
10	RXFULL*	3-state TTL output, changes following RXCLK↑	**Receive FIFO Full Flag.** Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). The RXFULL* output is enabled when AM* is asserted, otherwise it is High-Z. When the Receive FIFO is addressed (FIFOBYP* is HIGH and the device is addressed by AM* and selected by RXEN*), RXFULL* is asserted when the Receive FIFO has room for eight or fewer writes. An RXFULL* condition may indicate loss of data. When the Receive FIFO is bypassed (FIFOBYP* is LOW), RXFULL* and RXHALF* are deasserted to indicate that valid data may be present. RXFULL* is also used as a BIST progress indicator, and pulses asserted once every pass through the 511-character BIST loop. The RXFULL* output is enabled when AM* is asserted, otherwise it is High-Z
19	RXHALF*	TTL output, changes following RXCLK↑	**Receive FIFO Half-full Flag.** The RXHALF* flag is always active LOW, regardless of the EXTFIFO* setting. When the Receive FIFO is enabled (FIFOBYP* is HIGH), this signal is asserted when the Receive FIFO is half full or more (128 characters). When the Receive FIFO is bypassed, RXHALF* is deasserted. RXHALF* is forced to the High-Z state only during a "full-chip" reset (that is, while RESET*[1:0] are LOW).

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Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin Number	Name	I/O Characteristics	Signal Description
21	RXEMPTY$^{[6]}$	3-state TTL output, changes following RXCLK↑	**Receive FIFO Empty Flag**. Active HIGH when configured for Cascade timing (EXTFIFO is HIGH), active LOW when configured for UTOPIA timing (EXTFIFO is LOW). The RXFULL$^{[6]}$ output is enabled when AM$^{[6]}$ is asserted, otherwise it is High-Z. When the Receive FIFO is enabled (FIFOBYP$^{[6]}$ is HIGH), RXEMPTY$^{[6]}$ is asserted when no data remains in the Receive FIFO. Any read operation occurring when RXEMPTY$^{[6]}$ is asserted results in no change in the FIFO status, and the data from the last valid read remains on the RXDATA bus. When the Receive FIFO is bypassed but the Decoder is enabled, RXEMPTY$^{[6]}$ is used as a valid data indicator. The RXMODE[1:0] settings allow the user to determine which data is valid and allows selective flagging of idle characters. When RXEMPTY$^{[6]}$ is deasserted it indicates that a valid character (as selected by RXMODE[1:0]) is present at the RXDATA outputs. When asserted it indicates that a C5.0 (K28.5) rejected by the current RXMODE[1:0] setting is present on the RXDATA output bus. If both the Receive FIFO and the Decoder are bypassed, RXEMPTY$^{[6]}$ is deasserted to indicate that all received characters are valid. The TXFULL$^{[6]}$ output is enabled when AM$^{[6]}$ is asserted, otherwise it is High-Z.
67	RXRST$^{[6]}$	TTL input, sampled on RXCLK↑, Internal Pull Up	**Receive FIFO Reset**. When the Receive FIFO is addressed (FIFOBYP$^{[6]}$ is HIGH and device is selected by AM$^{[6]}$) and RXRST$^{[6]}$ is sampled asserted for eight or more RXCLK cycles, a Receive FIFO reset is initiated. The RXRST$^{[6]}$ input is also asserted to access the Serial Address Register.
73	RFEN	TTL input, asynchronous, Internal Pull Up	**Reframe Enable**. Controls when the framer is enabled to adjust the character boundaries based on detection of one or more K28.5 characters in the data stream. When HIGH, the framer can adjust the character boundaries relative to the received serial data stream to match those of the remote transmitter. When LOW, the boundary is fixed.
77	RXBISTEN$^{[6]}$	TTL input, asynchronous, Internal Pull Up	**Receiver BIST Enable**. When asserted, built-in self test (BIST) is active and the receiver is configured to perform a character for character match of the incoming data stream with a 511-character BIST sequence. The result of character mismatches are indicated on RXRVS. Completion of each 511-character BIST loop is accompanied by an assertion pulse on the RXFULL$^{[6]}$ flag.
Control Signals			
71	AM$^{[6]}$	TTL input, sampled by TXCLK↑, RXCLK↑, and REFCLK↑	**Address Match**. This signal is a qualifier for TXEN$^{[6]}$, RXEN$^{[6]}$, TXRST$^{[6]}$, and RXRST$^{[6]}$. It also controls three-state enables for the TXFULL$^{[6]}$, TXEMPTY$^{[6]}$, RXFULL$^{[6]}$, and RXEMPTY$^{[6]}$ signals.
6	LOOPTX	TTL input, asynchronous, Internal Pull Down	**Serial-in to Serial-out LOOP Select**. This input controls the LOOP-through function in which the Clock/Data Recovery PLL recovers the serial data and then retransmits it using the Transmit PLL as the bit rate reference. It selects between the output of the Transmit FIFO and the output of the Elasticity Buffer as the input to the Transmit Encoder. When LOW, the Transmit FIFO is the source of data for transmission. When HIGH, the Elasticity Buffer is the source of data for transmission and serial input data is reclocked and routed to the serial outputs. The LOOPTX function can only be used if the FIFOs are enabled (FIFOBYP$^{[6]}$ = HIGH).
12	REFCLK	TTL input clock	**Reference Clock**. This clock input is the timing reference for the transmit and receive PLLs. When the Transmit FIFO is bypassed, REFCLK is also the clock for the external transmit data interface. See Table 5 on page 20 for the relationships among REFCLK, SPDSEL, RANGESEL, FIFOBYP$^{[6]}$, ENCBYP$^{[6]}$ and BYTE8/10$^{[6]}$.

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Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin Number	Name	I/O Characteristics	Signal Description
75	SPDSEL	Static control input TTL levels Normally wired HIGH or LOW	**Speed Select.** Selects one of two operating data rate ranges for the device. When the operating symbol rate is between 100 and 200 MBaud, SPDSEL must be HIGH. When the operating symbol rate is between 50 and 100 MBaud, SPDSEL must be LOW (see Table 5 on page 20).
74	RANGESEL	Static control input TTL levels Normally wired HIGH or LOW	**Range Select.** Selects the proper prescaler for the REFCLK input. See Table 6 for the various relationships among REFCLK, SPDSEL, RANGESEL, FIFOBYP*, ENCBYP* and BYTE8/10*. When the Transmit FIFO is bypassed (FIFOBYP* is LOW) and REFCLK is a nonunity multiple of the character rate (RANGESEL HIGH or SPDSEL LOW), TXFULL* toggles at half the REFCLK rate to provide a character rate indication, and to show when data can be accepted.
49	EXTFIFO	Static control input TTL levels Normally wired HIGH or LOW	**External FIFO Select.** EXTFIFO indicates whether the device is used with external FIFOs. It modifies the active level of the RXEN* and TXEN* inputs and the timing of the Transmitter data bus according to the interface selected. When in UTOPIA mode and not configured for external FIFOs (EXTFIFO is LOW), TXEN*, RXEN* and all FIFO flags are active LOW. In this mode the active data transition for the transmit data bus is within the same clock as the transmit interface is selected by TXEN*. When configured for Cascade mode where the CY7C924ADX device is cascaded with external FIFOs (EXTFIFO is HIGH), TXEN, RXEN, the Full and Empty FIFO flags are active HIGH (the Half-full flag is always active LOW). TXEN is driven by the empty flag of an attached CY7C42X5 FIFO, and RXEN is driven by the Almost Full flag of an attached CY7C42X5 FIFO. In this mode the active data transition for the transmit data bus is in the clock cycle following the clock edge where transmit interface is selected by TXEN*.
28	FIFOBYP*	Static control input TTL levels Normally wired HIGH or LOW	**FIFO Bypass Select.** When LOW, the Transmit and Receive FIFOs are bypassed. In this mode TXCLK is not used. Instead all transmit data must be synchronous to REFCLK. Transmit FIFO status flags are synchronized to REFCLK. RXCLK becomes an output at the Receive PLL recovered character clock rate. All received data and FIFO status flags are synchronized to RXCLK. When HIGH, the Transmit and Receive FIFOs are enabled. In this mode all Transmit FIFO writes are synchronized to TXCLK, and all Receive FIFO reads are synchronous to the RXCLK input.
27	ENCBYP*	Static control input TTL levels Normally wired HIGH or LOW	**Encoder Bypass Select.** When LOW, both the encoder and decoder are bypassed. Data transmits in NRZ format, without encoding, LSB first. Received data are presented to the interface as parallel characters without decoding. When HIGH, data passes through both the 8B/10B encoder in the Transmit path and the decoder in the Receive path.
24, 25	RXMODE[1:0]	Static control input TTL levels Normally wired HIGH or LOW	**Receive Discard Policy Select.** These inputs select among the four data handling and fill-character discard modes in the receiver. See Table 7 on page 24.

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Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin Number	Name	I/O Characteristics	Signal Description
50	BYTE8/10*	Static control input TTL levels Normally wired HIGH or LOW	**Parallel Data Character Size Select.** Selects the input data character width. When BYTE8/10* is HIGH and ENCBYP* is HIGH, the device is in 8 bit mode and the data is encoded using the 8B/10B code rules found in Table 11 on page 52 and Table 12 on page 56. When BYTE8/10* is HIGH and ENCBYP* is LOW, the 10 parallel data bits pass directly to or from the serial stream without encoding or decoding. When BYTE8/10* is LOW, the part is in 10 bit mode. If the encoder is enabled (ENCBYP* is HIGH), the part passes the 10 parallel bits to the byte stuffer and encoder. When the encoder is disabled (ENCBYP* is LOW), the 12 parallel data bits pass directly to or from the serial stream without encoding or decoding. For affected pin groupings and function see Table 1 on page 14 and Table 8 on page 26. If the FIFOs are BYPASSED and Encoding is enabled (FIFOBYP* = LOW and ENCBYP* = HIGH), BYTE8/10* MUST BE HIGH.
52, 51	RESET*[1:0]	TTL input,	**Global Logic Reset.** These inputs are pulsed LOW for one or more REFCLK periods to reset the internal logic. They must be tied together or driven concurrently to ensure a valid reset.
1	TEST*	TTL input, asynchronous. Normally wired HIGH	**Factory Test Mode Select.** Used to force the part into a diagnostic test mode for factory ATE test. This pin is tied HIGH during normal operation.
Analog I/O and Control			
89, 90, 81, 82	OUTA± OUTB±	PECL-compatible differential outputs	**Differential Serial Data Outputs.** These PECL-compatible outputs are capable of driving terminated transmission lines or commercial fiber optic transmitter modules. An unused output pair may be powered down by leaving the outputs unconnected and strapping the associated CURSETx pin to V_{DD}.
97	CURSETA	Analog input	**Current-set Resistor Input for OUTA±.** A precision resistor is connected between this input and a clean ground to set the output differential amplitude and currents for the OUTA± differential driver.
78	CURSETB	Analog input	**Current-set Resistor Input for OUTB±.** A precision resistor is connected between this input and a clean ground to set the output differential amplitude and currents for the OUTB± differential driver.
94, 93, 86, 85	INA± INB±	PECL-compatible differential inputs	**Differential Serial Data Inputs.** These inputs accept the serial data stream for deserialization and decoding. Only one serial stream at a time may be fed to the receiver PLL to extract the data content. This stream is selected using the A/B* input. These inputs may also be routed to the OUTB± serial outputs using the DLB[1:0] inputs.
2	A/B*	TTL input, asynchronous, Internal Pull Up	**Receive Data Input Selector.** Determines which external serial bit stream is passed to the receiver clock and data recovery circuit.
4,5	DLB[1:0]	TTL input, asynchronous, Internal Pull Down	**Loopback Select Inputs.** Selects connections between serial inputs and outputs. Controls diagnostic loopback and serial loopthrough functions. See Table 3 on page 18 for details.
100	CARDET	PECL-compatible input, asynchronous	**Carrier Detect Input.** Allows an external device to signify that a valid signal is being presented to the high speed PECL-compatible input buffers, as is typical on an Optical Module. When CARDET is deasserted LOW, the LFI* indicator asserts LOW signifying a Link Fault. This input can be tied to V_{DD} for copper media applications.

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Pin Descriptions (continued)
CY7C924ADX HOTLink Transceiver

Pin Number	Name	I/O Characteristics	Signal Description
3	LFI*	TTL output, changes following RXCLK↑	**Link Fault Indication Output**. Active LOW. LFI* changes synchronous with RXCLK. This output is driven LOW when the serial link currently selected by A/B* is not suitable for data recovery. This can be caused by ■ Serial Data Amplitude below acceptable levels. ■ Input transition density not sufficient for PLL clock recovery. ■ Serial Data stream outside an acceptable frequency range of operation. ■ CARDET LOW.
Power			
80, 87, 88, 95, 96, 98	V_{DDA}		**Power for PECL-compatible I/O signals and internal analog circuits.**
76, 79, 83, 84, 91, 92, 99	V_{SSA}		**Ground for PECL-compatible I/O signals and internal analog circuits.**
14, 17, 35, 55, 62, 64	V_{DD}		**Power for CMOS I/O signals and internal logic circuits.**
11, 13, 15, 26, 37, 38, 39, 57, 63, 66	V_{SS}		**Ground for CMOS I/O signals and internal logic circuits.**

CY7C924ADX HOTLink Operation

Overview

The CY7C924ADX is designed to move parallel data across both short and long distances with minimal overhead or host system intervention. To accomplish this it converts the parallel characters into a serial bit stream, transmits these serial bits at high speed, and converts the received serial bits back into the original parallel data format.

The CY7C924ADX offers a large feature set, so it can be used in a wide range of host systems. Some of the configuration options are:

- 8 bit, 10 bit or 12 bit character size
- User definable data packet or frame structure
- Two octave data rate range
- Asynchronous (FIFOed) or synchronous data interface
- 8B/10B encoded or nonencoded (raw data)
- Embedded or bypassable FIFO data storage
- Multi-PHY capability
- Point-to-point, point-to-multipoint, or ring data transport

This flexibility allows the CY7C924ADX to meet the data transport needs of almost any system.

Transmit Data Path

Transmit Data Interface/Transmit Data FIFO

The transmit data interface to the host system is configurable as either an asynchronous buffered (FIFOed) parallel interface or as a synchronous pipeline register. The bus itself can be configured for operation with 8 bit, 10 bit or 12 bit data.

When configured for asynchronous operation (where the host-bus interface clock operates asynchronous to the serial character and bit stream clocks), the host interface becomes that of a synchronous FIFO clocked by TXCLK. In these configurations an internal 256 character Transmit FIFO is enabled. It allows the host interface to be written at any rate from DC to 50 MHz.

When configured for synchronous operation, the transmit interface is clocked by REFCLK and operates synchronous to the internal character and bit stream clocks. The input register must be written at the character rate, but REFCLK can operate at one, two or four times the character rate.

Both asynchronous and synchronous interface operations support two interface timing models: UTOPIA and Cascade. The UTOPIA timing model is designed to match the active levels, bus timing, and signal sequencing called out in the ATM Forum UTOPIA specification. The Cascade timing model is designed to match a host bus that resembles a synchronous FIFO. These

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timing models allow the CY7C924ADX to directly couple to host systems, registers, state machines, FIFOs, and so on, with minimal and in many cases no external glue logic.

Encoder

Data from the host interface or Transmit FIFO is next passed to an encoder block. The CY7C924ADX contains an internal 8B/10B encoder that is used to improve the serial transport characteristics of the data. For systems that contain their own encoder or scrambler, this encoder may be bypassed.

Serializer/Line Driver

The data from the encoder is passed to a serializer. This serializer operates at either 2.5, 5, or 10 times the rate of the REFCLK input (or 3, 6, or 12 times when BYTE8/10˙ and ENCBYP˙ are LOW). The serialized data is output from two PECL-compatible differential line drivers configured to drive transmission lines or optical modules.

Receive Data Path

Line Receiver/Deserializer/Framer

Serial data is received at one of two PECL-compatible differential line receivers. The data is passed to both a Clock and Data Recovery PLL (Phase Locked Loop) and to a deserializer that converts serial data into parallel characters. The framer adjusts the boundaries of these characters to match those of the original transmitted characters.

Decoder

The parallel characters pass through a 10B/8B Decoder and return to their original form. For systems that use external decoding or descrambling, the decoder may be bypassed.

Receive Data Interface/Receive Data FIFO

Data from the decoder passes either to a Receive FIFO or directly to the output register. The output register can be configured for operation with 8 bit, 10 bit or 12 bit data

When configured for an asynchronous buffered (FIFOed) interface, the data passes through a 256-character Receive FIFO that allows data to be read at any rate from DC to 50 MHz. When configured for synchronous operation (Receive FIFO is bypassed) data is clocked out of the Receive Output register at the byte rate, up to 20 MHz. The receive interface is also configurable for both UTOPIA and Cascade timing models.

Table 1. Transmit Input Bus Signal Map

	Transmit Encoder Mode[1]			
	Encoded 8-bit Character Stream	Pre-encoded 10-bit Character Stream	Encoded 10-bit Character Stream	Pre-encoded 12-bit Character Stream
ENCBYP˙	HIGH	LOW	HIGH	LOW
BYTE8/10˙	HIGH	HIGH	LOW	LOW
TXDATA Bus Input Bit				
TXSC/D˙	TXSC/D˙		TXSC/D˙	
TXDATA[0]	TXD[0]	TXD[0][2]	TXD[0]	TXD[0][2]
TXDATA[1]	TXD[1]	TXD[1]	TXD[1]	TXD[1]
TXDATA[2]	TXD[2]	TXD[2]	TXD[2]	TXD[2]
TXDATA[3]	TXD[3]	TXD[3]	TXD[3]	TXD[3]
TXDATA[4]	TXD[4]	TXD[4]	TXD[4]	TXD[4]
TXDATA[5]	TXD[5]	TXD[5]	TXD[5]	TXD[5]
TXDATA[6]	TXD[6]	TXD[6]	TXD[6]	TXD[6]
TXDATA[7]	TXD[7]	TXD[7]	TXD[7]	TXD[7]
TXINT/TXDATA[8] (FIFOBYP˙ = HIGH)	TXINT	TXD[8]	TXD[8]	TXD[8]
TXINT/TXDATA[8] (FIFOBYP˙ = LOW)		TXD[8]	TXD[8]	TXD[8]
TXHALT˙/TXDATA[9] (FIFOBYP˙ = HIGH)	TXHALT˙	TXD[9]	TXD[9]	TXD[9]
TXHALT˙/TXDATA[9] (FIFOBYP˙ = LOW)		TXD[9]	TXD[9]	TXD[9]
TXSVS/TXDATA[10]	TXSVS		TXSVS	TXD[10]
TXSOC/TXDATA[11] (FIFOBYP˙ = HIGH)	TXSOC		TXSOC	TXD[11]
TXSOC/TXDATA[11] (FIFOBYP˙ = LOW)				TXD[11]

Notes
1. All open cells are ignored.
2. First bit shifted out. Others follow in numerical order creating an NRZ pattern.

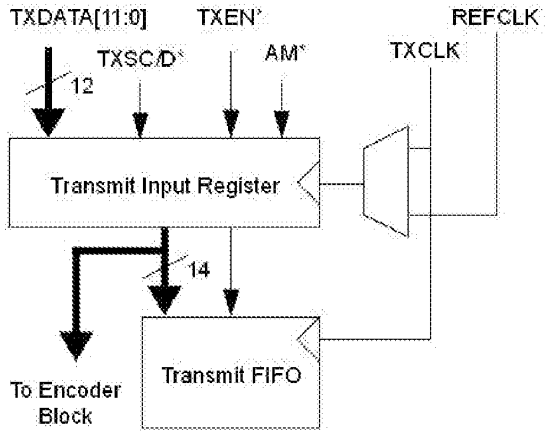
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CY7C924ADX HOTLink Transceiver Block Diagram Description

Transmit Input/Output Register

The Transmit Input Register, shown in Figure 2, captures the data to be processed by the HOTLink Transmitter, and allows the input timing to be compatible with asynchronous or synchronous host system buses. These buses can take the form of UTOPIA compliant interfaces, external FIFOs, state machines, or other control structures. Data present on the TXDATA[11:0] and TXSC/D' inputs are captured at the rising edge of the selected sample clock. The transmit data bus bit assignments vary depending on the data encoding, and bus width selected. These bus bit assignments are shown in Table 1 on page 14, and list the functional names of these different signals. Note that the function of several of these signals changes in different operating modes. The logical sense of the enable and FIFO flag signals depends on the intended interface convention and is set by the EXTFIFO pin.

Figure 2. Transmit Input Register



The transmit interface supports both synchronous and asynchronous clocking modes, each supporting both UTOPIA (EXTFIFO = LOW) and Cascade (EXTFIFO = HIGH) timing models. The selection of the specific clocking mode is determined by the RANGESEL and SPDSEL inputs and the FIFO Bypass (FIFOBYP') signal.

Synchronous Interface

Synchronous interface clocking operates the entire transmit data path synchronous to REFCLK. To enable it, connect FIFOBYP' LOW to disable the internal FIFOs.

Asynchronous Interface

Asynchronous interface clocking controls the writing of host bus data into the Transmit FIFO. To enable it, set FIFOBYP' HIGH to enable the internal FIFOs. In these configurations, TXCLK controls all writes to the Transmit Input Register and associated transfers to the Transmit FIFO. The data is clocked out of the Transmit FIFO and through the rest of the device on REFCLK or a synthesized derivative of REFCLK.

UTOPIA Timing Model

The UTOPIA timing model allows multiple CY7C924ADX transmitters to be addressed and accessed from a common host bus, using the protocols defined in the ATM Forum UTOPIA interface standards. To enable it, set EXTFIFO LOW.

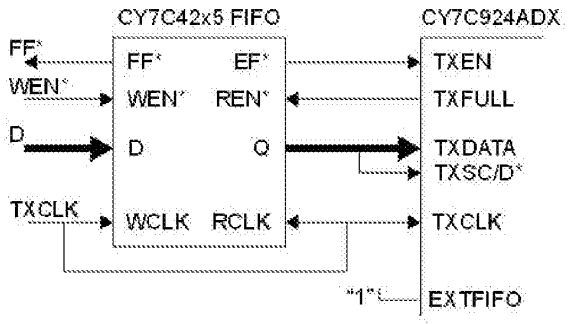
In UTOPIA timing, the TXEMPTY' and TXFULL' outputs and TXEN' input, are all active LOW signals. If the CY7C924ADX is addressed by AM', it is "selected" when TXEN' is asserted LOW. Following selection, data is written into the Transmit FIFO on every clock TXCLK cycle where TXEN' remains LOW.

Cascade Timing Model

The Cascade timing model is a variation of the UTOPIA timing model. Here the TXEMPTY' and TXFULL' outputs, and TXEN input, are all active HIGH signals. Cascade timing uses the same address and selection sequences as UTOPIA timing, but write data accesses use a delayed write. This delayed write is necessary to allow direct coupling to external FIFOs, or to state machines that initiate a write operation one clock cycle before the data is available on the bus. To enable Cascade timing, set EXTFIFO HIGH.

When used for FIFO depth expansion, Cascade timing allows the size of the internal Transmit FIFO to be expanded to an almost unlimited depth. It makes it possible to attach a CY7C42x5 series synchronous FIFO to the transmit interface without any extra logic, as shown in Figure 3.

Figure 3. External FIFO Depth Expansion of the CY7C924ADX Transmit Data Path



Transmit FIFO

The Transmit FIFO buffers data captured in the input register for later processing and transmission. This FIFO holds 256 14-bit characters. When the Transmit FIFO is active, and a Transmit FIFO write is enabled (the device is selected through AM' and TXEN' is sampled asserted), data and command are captured in the transmit input register and stored in the Transmit FIFO. TXCLK clocks all Transmit FIFO write operations.

The Transmit FIFO presents Full, Half-Full, and Empty FIFO flags. These flags are provided synchronous to TXCLK. When the Transmit FIFO is enabled, it allows operation with a Moore-type external controlling state machine. When configured for Cascade timing, the timing and active levels of these signals also support direct expansion to Cypress CY7C42x5 synchronous FIFOs.

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The read port of the Transmit FIFO is connected to a logic block that performs data formatting and validation. All data read operations from the Transmit FIFO are controlled by a Transmit Control State Machine that operates synchronous to REFCLK.

Transmit Formatter and Validation

The Transmit Formatter and validation logic perform two primary functions:

- Data format control
- Byte-packing

In addition to these logic functions, this block also controls the timing for the transfer of data from the Transmit Input Register, Transmit FIFO, or Elasticity Buffer.

Transmit Data Formatting

The CY7C924ADX supports a number of protocol enhancements over a raw physical layer device. These enhancements are possible in part through the use of the Transmit and Receive FIFOs. These FIFOs allow the CY7C924ADX to manage the data stream to a much greater extent than was possible before. In addition to the standard 8B/10B encoding used to improve serial data transmission, the CY7C924ADX also supports:

- Marking of packet or cell boundaries using TXSOC
- An expanded command set
- Ability to address and route packets or frames to specific receivers

All three of these capabilities are supported for both 8 and 10 bit encoded character sizes, and are made possible by using the TXSOC bit. This bit is interpreted, along with TXSC/D' and TXSVS, in modes where both the Transmit FIFO and the Encoder are enabled. All three bits determine how the data associated with them is processed for transmission. These operations are listed in Table 2.

The entries in Table 2 where TXSOC is LOW generate the same characters in the serial data stream as a standard CY7B923 HOTLink Transmitter. The data, command, and exception character encodings are listed in the Data and Special Character code tables (Table 11 on page 52 and Table 12 on page 56) found near the end of this data sheet.

Table 2. Transmit Data Formatting

TXSOC	TXSC/D'	TXSVS	Data Format Operation
0	0	0	Normal Data Encode
0	0	1	Replace Character with C0.7 Exception
0	1	0	Normal Command Encode
0	1	1	Replace Character with C0.7 Exception
1	0	0	Send Start of Cell Marker (C8.0) + Data Character
1	0	1	Replace Character with C0.7 Exception
1	1	0	Send Extended Command Marker (C9.0) + Data Character
1	1	1	Send Serial Address Marker (C10.0) + Data Character

The 001b, 011b, and 101b character formats instruct the encoder to discard the associated data character and to replace it with a C0.7 Exception character.

Excepting the previous 101b case, when the TXSOC bit read from the Transmit FIFO is HIGH, an extra character is inserted into the data stream. This extra character is always a Special Character code (see Table 12 on page 56) that informs the remote receiver that the immediately following character should be interpreted differently from its normal meaning. The associated character present on TXDATA[x:0] is always encoded as a data character.

The 100b combination (TXSOC = 1, TXSC/D' = 0, and TXSVS = 0) is used as a marker for the start of a cell, frame, or packet of data being sent across the interface. When a character is read from the Transmit FIFO with this combination of bits set, a C8.0 Special Character code is sent to the encoder before sending the associated data character.

The 110b character format expands the command space beyond that available with the default 8B/10B code. The 8B/10B code normally supports a *data* space of 256 data characters, and a *command* (non-data) space of twelve command characters (C0.0–C11.0 in Table 12). For data links where this is not sufficient, the 110b format can be used to mark the associated data as an extended command. This expands the command space to 256 commands (in addition to some of the present twelve). When a character is read from the Transmit FIFO with these bits set, a C9.0 Special Character code is sent to the encoder before sending the data character.

The 111b character format sends serial addresses to attached receivers. These serial addresses allow a host to direct (the following) data to a specific destination or destinations, when the CY7C924ADX devices are connected in a ring or bus topology.

The Serial Address marker may also be used to send packet identification fields, sequence numbers, or other high level routing information for those point-to-point connections that do not require physical address capabilities. However, the reporting of the address field contents may be affected by the present receiver discard policy. This marking or tagging can be performed with the 100b or 110b character formats without concern for receiver discard policy.

When a character is read from the Transmit FIFO with these bits set, a C10.0 Special Character is sent to the encoder before sending the associated data character.

Byte Packer

The byte packer is a logical construct that controls the efficient segmentation of 10 bit source data into 8 bit characters. This conversion allows these characters to be transported using 8B/10B encoding, with the same encoding overhead (20%) as when sending 8 bit characters. Because the serializer continues to operate using 10 bit transmission characters, this encoding mode only operates with the Transmit FIFO enabled.

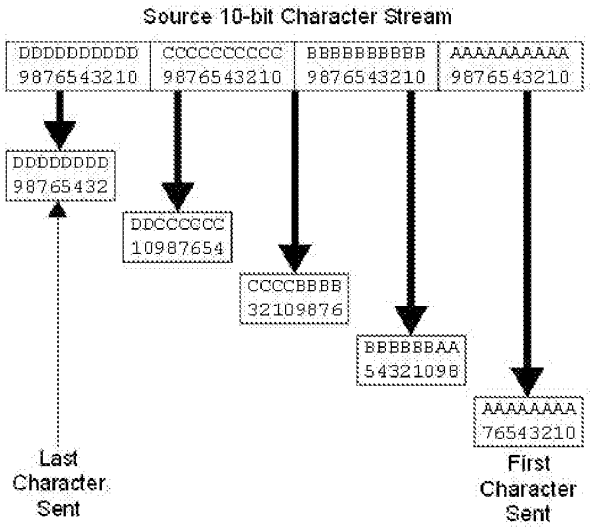
The byte packer takes pieces of one or more 10 bit characters, combines them into 8-bit groups, and passes these groups to the 8B/10B encoder. It takes exactly five 8 bit characters to transport four 10 bit characters. The allocation is performed, as shown in Figure 4 on page 17, where the low order eight bits of the first 10 bit character (A[7:0]) are passed to the encoder on the first clock cycle. During the second clock cycle the remaining two bits of the first character are combined with the lower six bits of the second

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10 bit character (B[5:0]+A[9:8]). In the third clock cycle the remaining four bits of the second 10 bit character are combined with the lower four bits of the third 10 bit character (C[3:0]+B[9:6]). In the fourth clock cycle the remaining six bits of the third 10 bit character are combined with the lower two bits of the fourth 10 bit character (D[1:0]+C[9:4]). In the fifth clock cycle the remaining eight bits of the fourth 10 bit character are passed to the encoder (D[9:2]).

This process repeats for additional data characters present in the FIFO. If at any time the Transmit FIFO is emptied, and a portion of a 10 bit character has not yet been transmitted, the remaining bits of the 8 bit character are filled with dummy bits before that character is passed to the encoder. The 8 bit character containing these dummy bits is immediately followed by a C5.0 (K28.5) fill character, which resets the sequencer boundaries to the first character position.

Figure 4. Byte-Packer 10-to-8 Character Mapping



Encoder Block

The Encoder logic block performs two primary functions: encoding the data for serial transmission and generating BIST (Built-In Self-Test) patterns to allow at speed link and device testing.

BIST LFSR

The Encoder logic block operates on data stored in a register. This register accepts information directly from the Transmit FIFO, the Transmit Input Register, the 10/8 Byte Packer, or from the Transmit Control State Machine when it inserts special characters into the data stream.

This same register is converted into a Linear Feedback Shift Register (LFSR) when the Built-In Self-Test (BIST) pattern generator is enabled (TXBISTEN˙ is LOW). When enabled, this LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Receiver.

The specific patterns generated are described in detail in the Cypress application note "HOTLink Built-In Self-Test." The sequence generated by the CY7C924ADX is identical to that in the HOTLink CY7B923 and HOTLink II family CYP(V)15G0x0x, allowing the user to build interoperable systems when the devices are used at compatible serial signaling rates.

Encoder

The data passed through the Transmit FIFO and formatter, or as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee:

- A minimum transition density (to allow the serial receiver PLL to extract a clock from the data stream)
- A DC balance in the signaling (to prevent baseline wander)
- Run length limits in the serial data (to limit the bandwidth of the link)
- A way to allow the remote receiver to determine the correct character boundaries (framing).

The CY7C924ADX contains an integrated 8B/10B encoder that accepts 8 bit data characters and converts these into 10 bit transmission characters that have been optimized for transport on serial communications links. The 8B/10B encoder can be bypassed for those system that operate with external 8B/10B encoders, or use alternate forms of encoding or scrambling to ensure good transmission characteristics. The operation of the 8B/10B encoding algorithm is described in detail later in this data sheet, and the complete encoding tables are listed in *Table 11* on page 52 and *Table 12* on page 56.

When the Encoder is enabled, the transmit data characters (as passed through the Transmit FIFO and formatter) are converted to either a 10 bit Data symbol or a 10 bit Special Character, depending upon the state of the TXSC/D˙ input. If TXSC/D˙ is HIGH, the data inputs represent a Special Character code and are encoded using the Special Character encoding rules in Table 12. If TXSC/D˙ is LOW, the data inputs are encoded using the Data Character encoding in Table 11.

If TXSVS is HIGH, the respective character is replaced with an SVS (C0.7) character. This can be used to check error handling system logic in the receiver controller or for proprietary applications.

The 8B/10B encoder is compliant with ANSI/NCITS ASC X3.230-1994 (Fibre Channel), IEEE 802.3z (Gigabit Ethernet), the IBM ESCON and FICON channels, and ATM Forum standards for data transport.

The 8B/10B coding function of the Encoder can be bypassed for systems that include an external coder or scrambler function as part of the controller or host system. Do this by setting ENCBYP˙ LOW. With the encoder bypassed, each 10 bit or 12 bit character (as captured in the Transmit Input Register) passes directly to the Transmit Shifter (or Transmit FIFO) without modification.

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Transmit Shifter

The Transmit Shifter accepts 10 bit or 12 bit parallel data from the Encoder block once each character time, and shifts it out the serial interface output buffers using a PLL-multiplied bit clock. This bit clock runs at 2.5, 5, or 10 times the REFCLK rate (3, 6, or 12 times when BYTE8/10* and ENCBYP* are LOW) as selected by RANGESEL and SPDSEL (see Table 4 on page 19). The counter and dividers in the Clock Multiplier PLL control timing for the parallel transfer, which is not affected by signal levels or timing at the input pins.

Bits in each character shift out LSB first, as required by ANSI and IEEE standards for 8B/10B coded serial data streams.

Routing Matrix

The Routing Matrix is a set of precision multiplexers that allow various combinations of Transmit Shifter, buffered INA± or INB± serial line receiver inputs, or a reclocked serial line receiver input to be transmitted from the OUTB± serial data outputs. The signal routing for the transmit serial outputs is controlled primarily by the DLB[1:0] inputs as listed in Table 3

The level restored (10b) and reclocked (11b) settings make use of one of the transmit data outputs. When configured for level restored or reclocked data, the selected input is retransmitted on OUTB±. The level restored connection simply buffers the input signal allowing a "bus like" connection to be constructed without concern for multidrop PECL compatible signal layout issues.

The reclocked connection buffers a PLL filtered copy of the selected input data stream. This removes most of the high frequency jitter that accumulates on a signal when sent over long transmission lines. Because the retransmitted data is clocked by the recovered clock, the data can suffer from jitter peaking when communicated through several PLLs.

For more details on these and LOOPTX reclocking options, see "Serial Line Receivers" on page 21.

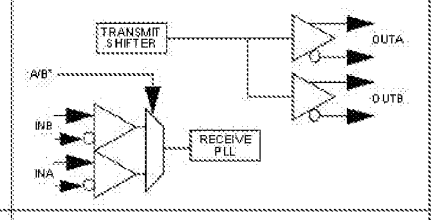
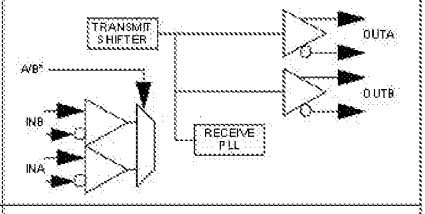
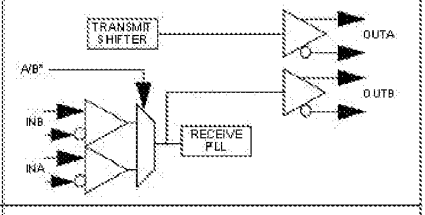
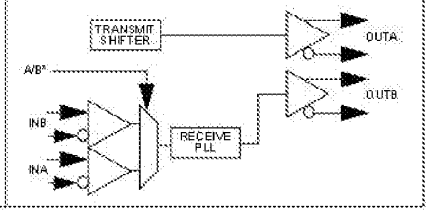
Serial Line Drivers

The serial interface PECL compatible Output Drivers (ECL referenced to +5 V) are the transmission line drivers for the serial media. OUTA± receives its data directly from the transmit shifter, while OUTB± receives its data from the Routing Matrix. These two outputs (OUTA± and OUTB±) can connect directly to +5 V optical modules, and can also directly drive DC or AC coupled transmission lines.

The PECL compatible Output Drivers can be viewed as programmable current sources. The output current and the load impedance Z_{LOAD} determine the output voltage. The desired output voltage swing is therefore controlled by the current set resistor R_{CURSET} associated with that driver. Different R_{CURSET} values are required for different line impedance/amplitude combinations. The output swing is designed to center around V_{DD} – 1.33 V. Each output must be externally biased to V_{DD} – 1.33 V.

When the interconnect and load are viewed as a differential transmission line, the absolute voltage V_{ODIF} and the differential load impedance are used to calculate the value of R_{CURSET}. This amplitude relationship is controlled by the load impedance on the driver, and by the resistance of the R_{CURSET} resistor for that driver, as listed in Equation 1.

Table 3. Transmit Data Routing Matrix

DLB[1]	DLB[0]	Data Connections
0	0	
0	1	
1	0	
1	1	

$$R_{CURSET} = \frac{90 \times Z_{LOAD}}{V_{ODIF}} \quad \text{Eq. 1}$$

In Equation 1, V_{ODIF} is the difference in voltage levels at one output of the differential driver when that output is driving HIGH and LOW. Z_{LOAD} is the differential load between the true and complement outputs of the driver. With a known load impedance and a desired signal swing, it is possible to calculate the value of the associated CURSETA or CURSETB resistor that sets this current.

Unused differential output drivers must be left open, and can reduce their power dissipation by connecting their respective CURSETx input to V_{DD}.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts an external clock at the REFCLK input, and multiples that clock by 2.5, 5, or 10 (3, 6, or 12 when BYTE8/10* is LOW and the encoder is disabled) to generate a bit rate clock for use by the transmit shifter. It also provides a character rate clock used by the Transmit Controller state machine.

The clock multiplier PLL can accept a REFCLK input between 8.33 MHz and 40 MHz, however, this clock range is limited by

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the operation mode of the CY7C924ADX as selected by the SPDSEL and RANGESEL inputs, and to a limited extent, by the BYTE8/10*, ENCBYP* and FIFOBYP* signals. *Table 4* shows the SPDSEL and RANGESEL for the case where the FIFOs and encoding are enabled. Table 5 provides the multiplier factors and clocking ranges for various combinations of signals.

Table 4. Speed Select and Range Select Settings, FIFOs and Encoding enabled

SPDSEL	RANGESEL	Serial Data Rate (MBaud)	REFCLK Frequency (MHz)
LOW	LOW	50–100	10–20
LOW	HIGH	50–100	20–40
HIGH	LOW	100–200	10–20
HIGH	HIGH	100–200	20–40

Transmit Control State Machine

The Transmit Control State Machine responds to multiple inputs to control the data stream passed to the encoder. It operates in response to:

- The state of the FIFOBYP* and LOOPTX inputs
- The state of the TXINT input
- The presence of data in the Transmit FIFO
- The contents of the Transmit FIFO
- The contents of the Elasticity Buffer
- The state of the transmitter BIST enable (TXBISTEN*)
- The state of external halt signals (TXHALT* and TXSTOP*)

These signals are used by the Transmit Control State Machine to control the data formatter, read access to the Transmit FIFO and Elasticity Buffer, the Byte-Packer, and BIST. They determine the content of the characters passed to the Encoder and Transmit Shifter.

When the Transmit FIFO is bypassed, the Transmit Control State Machine operates synchronous to REFCLK. In this mode, data from the TXDATA bus (or other source) passes directly from the Input Register to the Pipeline Register. If no data is enabled into the Input register (TXEN* is deasserted) then the Transmit Control State Machine presents a C5.0 Special Character code to the Encoder to maintain link synchronization. If both the Encoder and Transmit FIFO are bypassed and no data is enabled into the Input Register, the Transmit Control State Machine injects an alternating disparity sequence of preencoded (10 bit) forms of the C5.0 characters. This also occurs if the encoder is bypassed, the Transmit FIFO is enabled, and the Transmit FIFO is empty. However, since disparity tracking is part of the Encoder, the transmitted C5.0 characters may generate a running disparity error at the remote receiver. If the attached receiver has its decoder enabled, these characters may be reported as a normal C5.0, or as a C1.7 or C2.7 (K28.5 with incorrect running disparity).

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Table 5. Speed Select and Range Select Settings, all modes

FIFOBYP*	BYTE8/10*	ENCBYP*	SPDSEL	RANGESEL	REFCLK Frequency (MHz)	Serial Data Rate (MBd)	Multiplier Factor
HIGH	HIGH	X	LOW	LOW	10-20	50-100	x5
				HIGH	20-40	50-100	x2.5
			HIGH	LOW	10-20	100-200	x10
				HIGH	20-40	100-200	x5
	LOW	HIGH	LOW	LOW	10-20	50-100	x5
				HIGH	20-40	50-100	x2.5
			HIGH	LOW	10-20	100-200	x10
				HIGH	20-40	100-200	x5
		LOW	LOW	LOW	8.33-16.67	50-100	x6
				HIGH	16.67 -33.33	50-100	x3
			HIGH	LOW	8.33-16.67	100-200	x12
				HIGH	16.67 -33.33	100-200	x6
LOW	HIGH	X	LOW	LOW	10-20	50-100	x5
				HIGH	20-40	100-200	x5
			HIGH	LOW	10-20	100-200	x10
				HIGH	20-40	100-200	x5
	LOW	HIGH	LOW	LOW	10-20	50-100	x5
				HIGH	20-40	100-200	x5
			HIGH	LOW	10-20	100-200	x10
				HIGH	20-40	100-200	x5
		LOW	LOW	LOW	8.33-16.67	50-100	x6
				HIGH	16.67 -33.33	100-200	x6
			HIGH	LOW	8.33-16.67	100-200	x12
				HIGH	16.67 -33.33	100-200	x6

External Control of Data Flow

The Transmit Control State Machine supports three different types of external control:.

- TXSTOP*
- TXHALT*
- TXINT

These control signal inputs are only interpreted when the Transmit FIFO is enabled. They affect the transmission of data by bringing external signals to the state machine without sending the signals through the Transmit FIFO.

TXSTOP* stops transmission of the next packet or cell of data in the Transmit FIFO. When asserted (LOW) the Transmit Control State Machine continues to read and process characters in the Transmit FIFO until a location is read with the TXSOC bit set. Once a TXSOC is detected, the state machine sends out C5.0 fill characters until TXSTOP* is deasserted (HIGH) for one or more character times. When TXSTOP* is sampled deasserted it allows the next character with TXSOC set to be read from the Transmit FIFO and passed to the Encoder.

When TXSTOP* controls the flow of data, it is asserted (LOW) most of the time. To allow a cell or frame to pass, it only needs to be deasserted (HIGH) for one TXCLK cycle (assuming the transmit controller is at a cell boundary). Once the first character of the cell is transmitted the remainder of that cell is also processed. This allows the host system to control the transmission of data across the interface on a cell-by-cell or packet-by-packet basis.

TXHALT* (TXDATA[9]) is an immediate form of TXSTOP*. Instead of continuing to transmit data until a TXSOC is found, asserting TXHALT* stops character processing at the next FIFO character location. No additional data is read from the Transmit FIFO until TXHALT* is deasserted (HIGH).

Note. If the Encoder is bypassed, TXDATA[9] is a data input and not TXHALT*. Since in this mode the interface does not interpret the TXSOC bit, the TXSTOP* signal assumes the same functionality as TXHALT*.

TXINT is used to send one of two interrupt characters from the local transmitter to a remote receiver. While it also bypasses the Transmit FIFO, it does not directly stop data transmission.

The Transmit Control State Machine responds to transitions on the TXINT input. When TXINT transitions from 0→1, a C0.0

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(K28.0) Special Character code is inserted before the data character with which TXINT is associated is sent. When TXINT transitions from 1→0, a C3.0 (K28.3) Special Character code is sent. The reception of these characters generates an equivalent action on the attached receiver's RXINT status output.

The combination of RXHALF', TXINT, RXINT, and TXHALT' may be used to prevent a remote FIFO overflow, which would result in lost data. This back pressure mechanism can significantly improve data integrity in systems that cannot guarantee the full bandwidth of the host system at all times.

Elasticity Buffer

There is a short (8 character) FIFO between the receive and transmit paths. This FIFO separates the time domains of the received serial data stream and the outbound transmit data stream. This permits retransmission of received data without worry of jitter gain or jitter transfer. This allows error free transmission of the same data, when configured in daisy chain or ring configurations, to an unlimited number of destinations.

This Elasticity Buffer is enabled when the LOOPTX input is asserted HIGH. This directs the receiver to place all non-C5.0 (K28.5) characters into the Elasticity Buffer. LOOPTX also directs the Transmit Control State Machine to read data from the Elasticity Buffer instead of from the Transmit FIFO.

While retransmitting data from the Elasticity Buffer, the Transmit FIFO is available to preload data to be transmitted. Once LOOPTX is deasserted (LOW), normal data transmission from the Transmit FIFO resumes.

This LOOPTX capability is only possible when sending 8 bit encoded data streams. It cannot be used with byte-packed or nonencoded data streams, and requires that the Transmit and Receive FIFOs are enabled. The receiver must also be configured to process embedded commands (receiver Discard Policy cannot be 0). The reclocked connection may be required when sending non-8B/10B coded data streams, or data streams that cannot tolerate the data forwarding policies of the Elasticity Buffer.

Serial Line Receivers

Two differential line receivers, INA± and INB±, are available to accept serial data streams, with the active input selected using the A/B' input. The DLB[1:0] inputs allow the transmit Serializer output to be selected as a third input serial stream, but this path is generally used only for diagnostic purposes. The serial line receiver inputs are all differential, and will accommodate wire interconnect with filtering losses or transmission line attenuation greater than 9 dB ($V_{DIFF} \geq 200$ mV, or 400 mV peak-to-peak differential) or can be directly connected to +5 V fiber optic interface modules (any ECL logic family, not limited to ECL 100K). The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages.

As can be seen in Table 3 on page 18, these inputs are configured to allow single-pin control for most applications. For those systems requiring selection of only INA± or INB±, the DLB[1:0] signals can be tied LOW, and the A/B selection can be performed using only A/B'. For those systems requiring only a single input and a local loopback, the A/B' can be tied HIGH or LOW, DLB[1] signal can be tied LOW and DLB[0] can be used for loopback control.

Signal Detect

The selected Line Receiver (that routed to the clock and data recovery PLL) is simultaneously monitored for:

- Analog amplitude (>400 mV_{DIFF} pk-pk)
- Transition density
- Received data stream outside normal frequency range (±400 ppm)
- Detected carrier.

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFI' (Link Fault Indicator) output, which changes synchronous to RXCLK. While link status is monitored internally at all times, it is necessary to have transitions on RXCLK to allow this signal to change externally.

Clock/Data Recovery

The extraction of a bit rate clock and recovery of data bits from the received serial stream is performed within the Clock/Data Recovery (CDR) block. The clock extraction function is performed by a high performance embedded phase locked loop (PLL) that tracks the frequency of the incoming bit stream and aligns the phase of its internal bit rate clock to the transitions in the serial data stream.

The CDR makes use of the clock present at the REFCLK input. It ensures that the VCO (within the CDR) is operating at the correct frequency (rather than some harmonic of the bit rate), to improve PLL acquisition time, and to limit unlocked frequency excursions of the CDR VCO when no data is present at the serial inputs.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits for the range controls, the CDR PLL will track REFCLK instead of the data stream. When the frequency of the selected data stream returns to a valid frequency, the CDR PLL is allowed to track the received data stream. The frequency of REFCLK must be within ±400 ppm of the frequency of the clock that drives the REFCLK signal at the remote transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the LFI' output can select an alternate data stream. When an LFI' indication is detected, external logic can toggle selection of the INA± and INB± inputs through the A/B' input. When a port switch takes place, the PLL must reacquire the new serial stream and frame the incoming characters.

Clock Divider

This block contains the clock division logic, used to transfer the data from the Deserializer/Framer to the Decoder once every character (once every ten or twelve bits) clock. This counter is free running and generates outputs at the bit rate divided by 10 (12 when the BYTE8/10' and ENCBYP' are LOW). When the Receive FIFO is bypassed, one of these generated clocks is driven out the RXCLK pin.

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Deserializer/Framer

The CDR circuit extracts bits from the serial data stream and clocks these bits into the Shifter/Framer at the bit clock rate. When enabled, the Framer examines the data stream looking for C5.0 (K28.5) characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

The framer operates in one of three different modes, as selected by the RFEN input. When RFEN is first asserted (HIGH), the framer is allowed to reset the internal character boundaries on any detected C5.0 character.

Random errors that occur in the serial data can corrupt some data patterns into a bit pattern identical to a K28.5, and thus cause an erroneous data-framing error. To prevent this, the CY7C924ADX provides a multi-byte framer that is enabled once RFEN has been HIGH for greater than 2048 character. This requires two C5.0 characters within a span of five characters, with both C5.0 characters located on identical 10-bit character boundary locations, before the framer is allowed to reset the internal character boundary. This multi-byte framing option greatly reduces the possibility of erroneously reframing to an aliased K28.5 character.

If RFEN is LOW, the framer is disabled and no changes are made to character boundaries.

The framer in the CY7C924ADX operates by shifting the internal character position to align with the character clock. This ensures that the recovered clock does not contain any significant phase changes/hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other circuits using PLL-based logic elements.

Decoder Block

The decoder logic block performs two primary functions: decoding the received transmission characters back into Data and Special Character codes, and comparing generated BIST patterns with received characters to permit at-speed link and device testing.

10B/8B Decoder

The framed parallel output of the Deserializer is passed to the 10B/8B Decoder where, if the Decoder is enabled, it is transformed from a 10-bit transmission character back to the original Data and Special Character codes. This block uses the standard decoder patterns in *Tables 11* and *12* of this data sheet. Data patterns are indicated by a LOW on RXSC/D`, and Special Character codes are indicated by a HIGH. Invalid patterns or disparity errors are signaled as errors by a HIGH on RXRVS, and by specific Special Character codes.

If the Decoder is bypassed and BYTE8/10` is HIGH, the ten (10) data bits of each transmission character are passed unchanged from the framer to the Pipeline Register.

When the Decoder is bypassed and BYTE8/10` is LOW, the twelve (12) data bits of each transmission character are passed unchanged from the framer to the Pipeline Register.

BIST LFSR

The output register of the Decoder block is normally used to accumulate received characters for delivery to the Receive Formatter block. When configured for BIST mode (RXBISTEN` is LOW), this register becomes a signature pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). When enabled, this LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Transmitter. When synchronized with the received data stream, it checks each character in the Decoder with each character generated by the LFSR and indicates compare errors at the RXRVS output of the Receive Output Register.

The LFSR is initialized by the BIST hardware to the BIST loop start code of D0.0 (D0.0 is sent only once per BIST loop). Once the start of the BIST loop has been detected by the receiver, RXRVS is asserted for pattern mismatches between the received characters and the internally generated character sequence. Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXFULL` pulses asserted for one RXCLK cycle per BIST loop and can be used to check test pattern progress.

The specific patterns checked by the receiver are described in detail in the Cypress application note "HOTLink Built-In Self-Test." The sequence compared by the CY7C924ADX is identical to that in the HOTLink CY7B933 receiver and the HOTLink II family of devices CYP(V)15G0x0x, allowing interoperable systems to be built when used at compatible serial signaling rates.

If a large number of errors are detected, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

Receive Formatter

The Receive Formatter performs three primary functions:

- Data formatting
- Address matching
- Byte-unpacking

Receive Data Formatting

The protocol enhancements of the transmit path are mirrored in the receive path logic. The majority of these enhancements require that the Receive FIFO be enabled to allow the CY7C924ADX to manage the data stream. In addition to the standard 10B/8B decoding used for character reception and recovery, the CY7C924ADX also supports:

- Marking of packet or cell boundaries using RXSOC
- An expanded control/command character set
- Ability to accept or discard data based on an embedded address
- The ability to filter receive data of non-essential information

All of these capabilities are supported for both 8- and 10-bit character sizes, and are made possible through use of the RXSOC bit. RXSOC is generated upon reception of the C8.0, C9.0, or C10.0 Special Character codes, in those modes where both the Receive FIFO and the Decoder are enabled.

The entries in Table 6 show how the RXSOC, RXSC/D`, and RXRVS bits are formatted to indicate the reception of specific

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characters and character combinations. Normal Data and Special Character code characters are indicated by RXSOC being LOW (0). This allows the standard Special Characters codes to also be reported and output.

Table 6. Receive Data Formatting

RXSOC	RXSC/D*	RXRVS	Data Format Indication
0	0	0	Normal Data Character
0	0	1	Reserved
0	1	0	Normal Command Character
0	1	1	Received C0.7 Exception Character or Other Character Exception (as listed in Table 12)
1	0	0	Received Start of Cell Marker (C8.0) + Data Character
1	0	1	Received Illegal Sequence
1	1	0	Received Extended Command Marker (C9.0) + Data Character (interpreted as a command)
1	1	1	Received Serial Address Marker (C10.0) + Data Character (interpreted as an address)

Individual character errors that are not part of one of the supported sequences (Start of Cell, Extended Command, or Serial Address) are marked by the 011b (RXSOC = 0, RXSC/D* = 1, and RXRVS = 1) decode status.

Anytime RXSOC is reported HIGH (1) at least one of the C8.0, C9.0, or C10.0 characters was received as a valid character. If the immediately following character is a valid Data character, then the corresponding combination of RXSOC, RXSC/D*, and RXRVS indicate the type of information received. If the immediately following character is a Special Character code of any type (even a C5.0), then a 101b is posted to indicate an illegal sequence was received.

An illegal sequence can be caused by a remote transmitter sending incorrect information, or by receiving data corrupted during transmission. When such an error is detected, the 101b status bits are posted and the associated data field is set to the Special Character code that was received without error (C8.0, C9.0, or C10.0 reported as D8.0, D9.0, or D10.0 along with the 101b status). This information is provided to assist in debugging link or protocol faults.

The 100b indication is used to mark the associated Data character as the first character of a new frame, packet, cell, or other data construct used by the system. The Data characters and Special Character codes that follow this marker are written to the Receive FIFO (if the present address matching requirements are satisfied).

The 110b indication is used to mark the associated data character as the first character of an extended command. In reality there is no limit to the number of immediately following data characters that can be considered part of this command. The most common interpretation is based on the configured bus width, such that single-character configurations support the associated character as the extended command, providing up to 256 extended commands for 8-bit data and 1024 for 10-bit byte-packed data.

This marker is treated internally the same as the 100b Start Of Cell indication, which allows it to be used to mark the boundary of any user-specific information. As a boundary or cell marker, the immediately following data can be a data field, a header, a stream identifier, a transaction number, a packet length indicator, or any of a number of pieces of information connected to a data transfer.

Note. In reality, the 100b and 110b indicators can be used interchangeably; i.e., the 100b indication can be used to mark extended commands while the 110b indication can be used to mark the start of cells.

The 111b indication is used to mark the start of a Serial Address field. Unlike the Start Of Cell and Extended Command markers, which have no specific data-field length associated with them, the associated Serial Address is always comprised of the immediately following single data character, and supports a fixed 8-bit or 10-bit address field format in 8-bit or 10-bit byte-packed data formats.

When this serial address is received it may be passed to the Receive FIFO or discarded (see Table 7 on page 24).

Address Matching

For those modes where address matching is enabled, the CY7C924ADX's ability to accept or discard data can be controlled by the remote transmitter. This is often useful in configurations with one or more data sources and multiple data destinations.

Each CY7C924ADX contains an 8-bit or 10-bit Serial Address Register that is compared with the first data character received following a Serial Address marker (C10.0). This character constitutes an address, which can be configured for one of two modes for address matching. The first mode is used for multicast addresses, where a bit-wise AND is performed on each bit of the address character received, with the contents of each of the bits in the Serial Address Register. If any of the same bit locations in the register and the received data are both set to '1', a multicast address match is declared and the following data and Special Character codes are interpreted and passed to the Receive FIFO.

If the multicast address field is ever received as all 1s (FFh or 3FFh), the receiver always accepts the data. This all 1s setting is the broadcast address and is used to send data to all receivers.

This all 1s setting also has special meaning when written to the Serial Address Register. When the multicast address field is written to an all 1s (FFh or 3FFh) state, the receiver operates in promiscuous mode, and receives all data, regardless of the contents of any serial address commands received. This is also the default or power-up state of the Serial Address register.

The second mode of operation for address matching is when the Serial Address register contains a unique device address, and is compared with the character received following the C10.0 Serial Address marker. This unicast address requires an exact match between all 8 or 10 bits to declare a match found and allow the following data to pass.

When the Elasticity Buffer is enabled, all received characters (except C5.0) are written to the Elasticity Buffer, regardless of the state or configuration of any present address match. This allows

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one or more sources to send data to multiple receivers with the receivers connected in a ring or daisy-chain topology. By prefacing cells containing data with an address field, it is possible to have each receiver only process data specifically directed to it.

Byte-Unpacker

The Byte-Unpacker is used to reassemble 10-bit characters from a received stream of decoded 8-bit characters. This reassembly process is designed to allow transmission of the same embedded commands, serial addresses, and Start of Cell markers that are used with 8-bit data characters. Because of the change in time per received encoded character versus delivered 10-bit data character, this unpacking process is only possible with the Receive FIFO enabled.

The byte-unpacker reverses the character segmentation shown in Figure 4. It takes five data characters and combines them into four 10-bit characters. This five-state unpacking process is re-started by the detection of any Special Character code in the Decoder, including the C5.0 (K28.5) fill character. Since usage of the Elasticity Buffer inserts and deletes C5.0 characters (as necessary) to handle the speed differences between the receive and transmit character clocks, it is not possible to send byte-packed data through the Elasticity Buffer. To send 10-bit packed data from one source to multiple destinations it is necessary to either use a star topology of interconnect, or make use of the buffered and reclocked serial input-to-output connections controlled by the Routing Matrix.

Receive Control State Machine

The Receive Control State Machine responds to multiple input conditions to control the routing and handling of received characters. It controls the staging of characters across various registers and the Receive FIFO. It also interprets all embedded Special Character codes, and converts the appropriate ones to specific bit combinations in the Receive FIFO. It controls the various discard policies and error control within the receiver, and operates in response to:

- the received character stream
- the detection and validation of serial addresses
- the room for additional data in the Receive FIFO
- the state of the receiver BIST enable (RXBISTEN*)
- the state of LOOPTX
- the state of FIFOBYP*.

These signals and conditions are used by the Receive Control State Machine to control the Receive Formatter, write access to the Receive FIFO, write access to the Elasticity Buffer, the Byte-Unpacker, the Receive Output register, and BIST. They determine the content of the characters passed to each of these destinations.

The Receive Control State Machine always operates synchronous to the recovered character clock (bit-clock/10 or bit-clock/12). When the Receive FIFO is bypassed, RXCLK becomes an output that changes synchronous to the internal character clock. RXCLK operates at the same frequency as the internal character clock.

Discard Policies

When the Receive FIFO is enabled, the Receive Control State Machine has the ability to selectively discard specific characters from the data stream that are determined by the present configuration as being unnecessary. When discarding is enabled, it reduces the host system overhead necessary to keep the Receive FIFO from overflowing and losing data.

The discard policy is configured as part of the operating mode and is set using the RXMODE[1:0] inputs. The four discard policies are listed in Table 7.

Table 7. Receiver Discard Policies

Policy #	RXMODE[1:0]	Policy Description
0	00	Keep all received characters
1	01	Process Commands, discard all but the last C5.0 character
2	10	Process Commands, discard all C5.0 characters
3	11	Process Commands, discard all C5.0 characters, discard serial addresses

Policy 0 is the simplest and also applies for all conditions where the Receive FIFO is bypassed. In this mode, every character that is received is placed into the Receive FIFO (when enabled) or into the Receive Output Register.

In discard policy 1, all Start Of Cell, extended command, and serial address commands are processed as they are received. The C5.0 character, which is automatically transmitted when no data is present in the Transmit FIFO, is treated differently here. In this mode, whenever two or more adjacent C5.0 characters are received, all of them are discarded except the last one received before any other character type. This allows these fill characters to be removed from the data stream, but does not change the data flow for protocols (like Fibre Channel) that use a single C5.0 character as a delimiter.

Policy 2 is identical to policy 1 except that all C5.0 characters are removed from the data stream.

Policy 3 is a super-set of policy 2, where the serial address is also discarded.

When the FIFOs are bypassed (FIFOBYP* LOW), no characters are actually discarded, but the receiver discard policy can be used to control external filtering of the data. The RXEMPTY* FIFO flag is used to indicate if the character on the output bus is valid or not. In discard policy 0, the RXEMPTY* flag is always deasserted to indicate that valid data is always present. In discard policy 1 when a series of C5.0 characters are received, the RXEMPTY* flag indicates an empty condition for all but the last C5.0 character before any other character is presented. In discard policies 2 or 3, the RXEMPTY* flag indicates an empty condition for all C5.0 characters. When any other character is present, this flag indicates that valid or "interesting" Data or Special Characters are present.

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Receive FIFO

The Receive FIFO is used to buffer data captured from the selected serial stream for later processing by the host system. This FIFO is sized to hold 256, 14-bit characters. When the FIFO is enabled, it is written to by the Receive Control State Machine. When data is present in the Receive FIFO (as indicated by the RXFULL*, RXHALF*, and RXEMPTY* Receive FIFO status flags), it can be read from the Output Register by asserting AM* and RXEN*.).

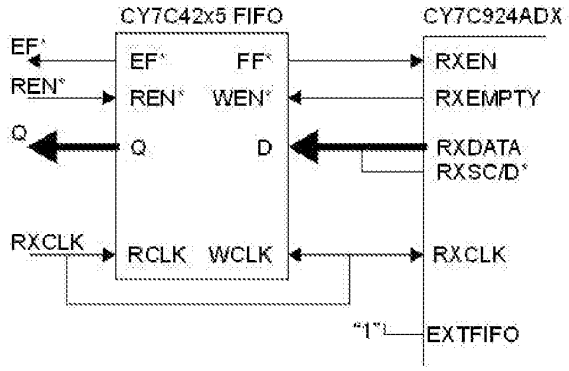
The read port on the Receive FIFO may be configured for the same two timing models as the transmit interface: UTOPIA and Cascade. Both are forms of a FIFO interface. The UTOPIA timing model (EXTFIFO = L) has active LOW RXEMPTY* and RXFULL* status flags, and an active LOW RXEN* enable. When configured for Cascade operation (EXTFIFO = H), these same signals are all active HIGH. The RXHALF* signal is always active LOW, regardless of EXTFIFO setting. Either timing model supports connection to various host bus interfaces, state machines, or external FIFOs for depth expansion (see *Figure 5*

The Receive FIFO presents Full, Half-Full, and Empty FIFO status flags. These flags are provided synchronous to RXCLK to allow operation with a Moore-type external controlling state machine. When configured with the Receive FIFO enabled, RXCLK is an input. When the Receive FIFO is bypassed (FIFOBYP* is LOW), RXCLK is an output operating at the received character rate.

Receive Input Register

The input register is clocked by the rising edge of RXCLK. It samples numerous signals that control the reading of the Receive FIFO and operation of the Receive Control State Machine.

Figure 5. External FIFO Depth Expansion of the CY7C924ADX Receive Data Path



Receive Output Register

The Receive Output Register changes in response to the rising edge of RXCLK. When the Receive FIFO is enabled (FIFOBYP* = H), the FIFO status flag outputs of this register are placed in a High-Z state when the CY7C924ADX is not addressed (AM* is sampled HIGH). The RXDATA bus output drivers are enabled when the device is selected by RXEN* being asserted in the RXCLK cycle immediately following that in which the device was addressed (AM* is sampled LOW), and RXEN* being sampled by RXCLK. This initiates a Receive FIFO read cycle.

Just as with the TXDATA bus on the Transmit Input Register, the receive outputs are also mapped by the specific decoding and bus-width selected by the ENCBYP*, BYTE8/10* and FIFOBYP* inputs. These assignments are shown in Table 8 on page 26.

When the Decoder and Receive FIFO are both enabled, the Receive Control State Machine interprets and discards (except in discard policy 0) received C0.0 and C3.0 command codes as set and clear directives for the RXINT output. This allows the RXINT output to duplicate the state transitions presented to the TXINT input at the source end of the link. This RXINT output can be used, along with TXHALT*, TXINT, and RXHALF*, to implement a back-pressure mechanism for the Receive FIFO, or for other time dependent signalling.

If the Receive FIFO and Decoder are bypassed, all received characters are passed directly to the Receive Output Register. If framing is enabled, and K28.5 characters have been detected meeting the present framing requirements, the output characters will appear on proper character boundaries. If framing is disabled (RFEN is LOW) or K28.5 characters have not been detected in the data stream, the received characters may not be output on their proper 10-bit boundaries. In this mode, some form of external framing and decoding/descrambling must be used to recover the original source data.

Serial Address Register

When the device is in UTOPIA mode (EXTFIFO = LOW), the receiver is capable of selectively accepting or discarding received data based on an address received in the data stream. The address matching capability allows for the choice of matching of either domains (multicast) or exact addresses (unicast). The 8- or 10-bit Serial Address Register represents a single character address field as shown in Figure 6 on page 26.

The multicast mode is bit-specific and allows allocation of up to 8 or 10 separate domains. In the unicast address mode the match is character specific and identifies up to 256 or 1024 destination addresses. A device can either belong to one or more domains, or it can have a single unique address.

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Table 8. Receive Output Bus Signal Map

	Receive Decoder Mode[3]			
	Decoded 10-bit Character Stream (8-bit characters)	Undecoded 10-bit Character Stream	Decoded 10-bit Byte-Packed Character Stream (10-bit characters)	Undecoded 12-bit Character Stream
ENCBYP*	HIGH	LOW	HIGH	LOW
BYTE8/10*	HIGH	HIGH	LOW	LOW
RXDATA Bus I/O Bit				
RXSC/D*	RXSC/D*		RXSC/D*	
RXDATA[0]	RXD[0]	RXD[0][3]	RXD[0]	RXD[0][3]
RXDATA[1]	RXD[1]	RXD[1]	RXD[1]	RXD[1]
RXDATA[2]	RXD[2]	RXD[2]	RXD[2]	RXD[2]
RXDATA[3]	RXD[3]	RXD[3]	RXD[3]	RXD[3]
RXDATA[4]	RXD[4]	RXD[4]	RXD[4]	RXD[4]
RXDATA[5]	RXD[5]	RXD[5]	RXD[5]	RXD[5]
RXDATA[6]	RXD[6]	RXD[6]	RXD[6]	RXD[6]
RXDATA[7]	RXD[7]	RXD[7]	RXD[7]	RXD[7]
RXINT/RXDATA[8] (FIFOBYP*=HIGH)	RXINT	RXD[8]	RXD[8]	RXD[8]
RXINT/RXDATA[8] (FIFOBYP*=LOW)		RXD[8]	RXD[8]	RXD[8]
RXDATA[9]	(LOW)	RXD[9]	RXD[9]	RXD[9]
RXRVS/RXDATA[10]	RXRVS		RXRVS	RXD[10]
RXSOC/RXDATA[11]	RXSOC		RXSOC	RXD[11]

When a serial address is received and a match is detected, the address, and all data following that address, is passed to the Receive FIFO (except in discard policy 3 where the address is discarded). This continues until a serial address is received that does not match the contents of the Address Register, whereupon writes to the Receive FIFO are inhibited. The Serial Address Register has a power-up default state where the multicast field set to an all ones condition (FFh or 3FFh). When set to this value the receiver accepts all data, regardless of the presence or content of any received serial address. This "promiscuous" address can also be forced by the momentary assertion of the RESET*[1:0] pair.

The Serial Address Register is only used when the receiver is operated with the Receive FIFO enabled (FIFOBYP* is HIGH) and in operating modes where the discard policy is not 0 (see Table 7 on page 24 for a list of discard policies).

Serial Address Register Access

The Serial Address Register is accessed through the RXDATA bus. Both reads and writes to the register require the device to be addressed (AM* is LOW) and for RXRST* to be asserted (LOW).

When accessed for write or read operations, the RXRVS signal is used as a read/write selector, and RXSC/D* is used to select the operating mode (multicast or unicast) of the Serial Address Register.

Figure 6. Serial Address Register Format and Access

Address Register Content

RXDATA[9] or [7] RXDATA[0]

MSB Serial Address Register LSB

RXEN*	RXRST*	RXRVS	RXSC/D*	
0	0	0	0	Multicast Address write
0	0	0	1	Unicast Address write
0	0	1	0	Multicast Address read
0	0	1	1	Unicast Address read

Note
3. First bit shifted in. Others follow in numerical order interpreted from an NRZ pattern.

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Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential ..... –0.5 V to +6.5 V

DC voltage applied to outputs in high-Z State ..... –0.5 V to V_{DD} + 0.5 V

Output current into TTL outputs (LOW) ..... 30 mA

DC input voltage ..... –0.5 V to V_{DD} + 0.5 V

Static discharge voltage ..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0 °C to +70 °C	5.0 V ± 10%
Industrial	–40 °C to +85 °C	5.0 V ± 10%

CY7C924ADX DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min	Max	Unit
TTL Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = –2 mA, V_{DD} = Min.	2.4		V
V_{OLT}	Output LOW Voltage	I_{OL} = 8 mA, V_{DD} = Min.		0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0 V[4]	–30	–80	mA
I_{OZL}	High-Z Output Leakage Current		–20	20	µA
TTL Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{DD}	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	V_{IN} = V_{DD}		+40	µA
I_{ILT}	Input LOW Current	V_{IN} = 0.0 V		–40	µA
I_{IHPD}	Input HIGH Current	V_{IN} = V_{DD}, Pins with internal pull-down		+300	µA
I_{ILPU}	Input LOW Current	V_{IN} = 0.0 V, Pins with internal pull-up	–300		µA
Transmitter PECL-Compatible Output Pins: OUTA+, OUTA–, OUTB+, OUTB–[5]					
V_{OHE}	Output HIGH Voltage (V_{DD} referenced)	Load = 50Ω to V_{DD} – 1.33 V R_{CURSET} = 10k	V_{DD} – 1.03	V_{DD} – 0.83	V
V_{OLE}	Output LOW Voltage (V_{DD} referenced)	Load = 50Ω to V_{DD} – 1.33 V R_{CURSET} = 10k	V_{DD} – 2	V_{DD} – 1.62	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	Load = 50Ω to V_{DD} – 1.33 V R_{CURSET} = 10k	600	1100	mV
Receiver Single-ended PECL-compatible Input Pin: CARDET					
V_{IHE}	Input HIGH Voltage (V_{DD} referenced)		V_{DD} – 1.165	V_{DD}	V
V_{ILE}	Input LOW Voltage (V_{DD} referenced)		2.5	V_{DD} – 1.475	V
I_{IHE}	Input HIGH Current	V_{IN} = V_{IHE}(min.)		+40	µA
I_{ILE}	Input LOW Current	V_{IN} = V_{ILE}(max.)	–40		µA
Differential Line Receiver Input Pins: INA+, INA–, INB+, INB–					
V_{DIFF}	Input Differential Voltage |(IN+) – (IN–)|		200	2500	mV
V_{IHH}	Highest Input HIGH Voltage			V_{DD}	V
V_{ILL}	Lowest Input LOW Voltage		2.5		V
I_{IHH}	Input HIGH Current	V_{IN} = V_{IHH} Max.		750	µA
I_{ILL}[6]	Input LOW Current	V_{IN} = V_{ILL} Min.	–200		µA
Miscellaneous			**Typ.**	**Max.**	
I_{DD}[7]	Power Supply Current	Freq. = Max.	170	250	mA

Notes

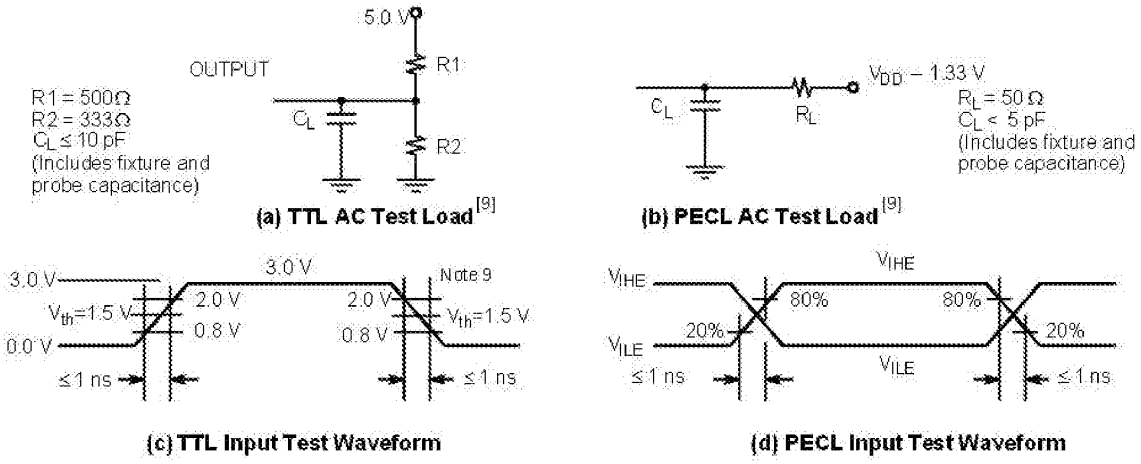
4. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
5. The output current and (resulting voltage swing) is set using a single resistor between CURSETx and V_{SS}. This CURSET resistor value is calculated as R_{CURSET} = (90*Z_{LOAD})/V_{ODIF}, where Z_{LOAD} is the differential load between the true and compliment outputs of the differential driver.
6. To guarantee positive currents for all PECL voltages, an external pull-down resistor must be present.
7. Maximum I_{DD} is measured with V_{DD} = MAX, RFEN = LOW, and outputs unloaded. Typical I_{DD} is measured with V_{DD} = 5.0 V, T_A = 25°C, RFEN = LOW, and outputs unloaded.

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Capacitance[8]

Parameter	Description	Test Conditions	Max	Unit
C_{INTTL}	TTL Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{DD} = 5.0 V	7	pF
C_{INPECL}	PECL-compatible input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{DD} = 5.0 V	4	pF

Figure 7. AC Test Loads and Waveforms



(a) TTL AC Test Load[9] (b) PECL AC Test Load[9]

(c) TTL Input Test Waveform (d) PECL Input Test Waveform

CY7C924ADX Transmitter TTL Switching Characteristics, FIFO Enabled Over the Operating Range

Parameter	Description	Min	Max	Unit
f_{TS}	TXCLK Clock Cycle Frequency With Transmit FIFO Enabled		50	MHz
t_{TXCLK}	TXCLK Period	20		ns
t_{TXCPWH}	TXCLK HIGH Time	6.5		ns
t_{TXCPWL}	TXCLK LOW Time	6.5		ns
t_{TXCLKR}[8]	TXCLK Rise Time[10]	0.7	5	ns
t_{TXCLKF}[8]	TXCLK Fall Time[10]	0.7	5	ns
t_{TXA}	Flag Access Time From TXCLK↑ to Output	2	15	ns
t_{TXDS}	Transmit Data Setup Time to TXCLK↑	4		ns
t_{TXDH}	Transmit Data Hold Time from TXCLK↑	1		ns
t_{TXENS}	Transmit Enable Set-Up Time to TXCLK↑	4		ns
t_{TXENH}	Transmit Enable Hold Time from TXCLK↑	1		ns
t_{TXRSS}	Transmit FIFO Reset (TXRST*) Setup Time to TXCLK↑	4		ns
t_{TXRSH}	Transmit FIFO Reset (TXRST*) Hold Time from TXCLK↑	1		ns
t_{TXAMS}	Transmit Address Match (AM*) Setup Time to TXCLK↑	4		ns
t_{TXAMH}	Transmit Address Match (AM*) Hold Time from TXCLK↑	1		ns
t_{TXZA}	Sample of AM* LOW by TXCLK↑, Output High-Z to Active HIGH or LOW	0		ns
t_{TXOE}	Sample of AM* LOW by TXCLK↑ to Output Valid	1.5	20	ns
t_{TXAZ}	Sample of AM* HIGH by TXCLK↑ to Output in High-Z	1.5	20	ns

Notes
8. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
9. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
10. Input/output rise and fall time is measured between 0.8 V and 2.0 V.

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CY7C924ADX Receiver TTL Switching Characteristics, FIFO Enabled Over the Operating Range

Parameter	Description	Min	Max	Unit
f_{RIS}	RXCLK Clock Cycle Frequency With Receive FIFO Enabled		50	MHz
$t_{RXCLKIP}$	RXCLK Input Period	20		ns
t_{RXCPWH}	RXCLK Input HIGH Time	6.5		ns
t_{RXCPWL}	RXCLK Input LOW Time	6.5		ns
$t_{RXCLKIR}$[8]	RXCLK Input Rise Time[10]	0.7	5	ns
$t_{RXCLKIF}$[8]	RXCLK Input Fall Time[10]	0.7	5	ns
t_{RXENS}	Receive Enable Setup Time to RXCLK↑	4		ns
t_{RXENH}	Receive Enable Hold Time from RXCLK↑	1		ns
t_{RXRSS}	Receive FIFO Reset (RXRXT*) Setup Time to RXCLK↑	4		ns
t_{RXRSH}	Receive FIFO Reset (RXRXT*) Hold Time from RXCLK↑	1		ns
t_{RXAMS}	Receive Address Match (AM*) Setup Time to RXCLK↑	4		ns
t_{RXAMH}	Receive Address Match (AM*) Hold Time from RXCLK↑	1		ns
t_{RXA}[11]	Flag and Data Access Time from RXCLK↑ to Output	1.5	15	ns
t_{RXZA}[11]	Sample of AM* LOW by RXCLK↑, Output High-Z to Active HIGH or LOW, or Sample of RXEN* Asserted by RXCLK↑, Output High-Z to Active HIGH or LOW	0		ns
t_{RXOE}[11]	Sample of AM* LOW by RXCLK↑ to Output Valid,[11] or Sample of RXEN* Asserted by RXCLK↑ to RXDATA Outputs Valid	1.5	20	ns
t_{RXAZ}[11]	Sample of AM* HIGH by RXCLK↑ to Output in High-Z,[11] or Sample of RXEN* Deasserted by RXCLK↑ to RXDATA Outputs in High-Z	1.5	20	ns

CY7C924ADX Transmitter TTL Switching Characteristics, FIFO Bypassed Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{TRA}	Flag Access Time From REFCLK↑ to Output	2	15	ns
t_{REFDS}	Write Data Set-Up Time to REFCLK↑	4		ns
t_{REFDH}	Write Data Hold Time from REFCLK↑	2		ns
t_{REFENS}	Transmit Enable Setup Time to REFCLK↑	4		ns
t_{REFENH}	Transmit Enable Hold Time from REFCLK↑	2		ns
t_{REFAMS}	Transmit Address Match (AM*) Setup Time to REFCLK↑	4		ns
t_{REFAMH}	Transmit Address Match (AM*) Hold Time from REFCLK↑	2		ns
t_{REFZA}	Sample of AM* LOW by REFCLK↑, Output High-Z to Active HIGH or LOW	0		ns
t_{REFOE}	Sample of AM* LOW by REFCLK↑ to Flag Output Valid	1.5	20	ns
t_{REFAZ}	Sample of AM* HIGH by REFCLK↑ to Flag Output High-Z	1.5	20	ns

Note
11. Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.

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CY7C924ADX Receiver TTL Switching Characteristics, FIFO Bypassed Over the Operating Range

Parameter	Description	Min	Max	Unit
f_{ROS}[12]	RXCLK Clock Output Frequency—100 to 200 MBaud (RANGESEL is HIGH, ENCBYP* is HIGH or BYTE8/10* is HIGH)	10	20	MHz
	RXCLK Clock Output Frequency—50 to 100 MBaud (RANGESEL is LOW, ENCBYP* is HIGH or BYTE8/10* is HIGH)	5	10	MHz
	RXCLK Clock Output Frequency—100 to 200 MBaud 12-bit Encoder Bypass Operation (RANGESEL is HIGH, ENCBYP* is LOW and BYTE8/10* is LOW)	8.33	16.67	MHz
	RXCLK Clock Output Frequency—50 to 100 MBaud 10-bit Operation (RANGESEL is LOW, ENCBYP* is LOW and BYTE8/10* is LOW)	4.16	8.33	MHz
$t_{RXCLKOP}$	RXCLK Output Period	25	250	ns
$t_{RXCLKOD}$	RXCLK Output Duty Cycle	40	60	%
$t_{RXCLKOR}$[8]	RXCLK Output Rise Time[10]	0.25	2	ns
$t_{RXCLKOF}$[8]	RXCLK Output Fall Time[10]	0.25	2	ns
t_{RXENS}	Receive Enable Setup Time to RXCLK↑	4		ns
t_{RXENH}	Receive Enable Hold Time from RXCLK↑	1		ns
t_{RXZA}[11]	Sample of AM* LOW by RXCLK↑, Outputs High-Z to Active Sample of RXEN* Asserted by RXCLK↑ to RXDATA Outputs High-Z to Active	0		ns
t_{RXOE}[11]	Sample of AM* LOW by RXCLK↑ to Flag Output Valid Sample of RXEN* Asserted by RXCLK↑ to RXDATA Output Low-Z	1.5	20	ns
t_{RXAZ}[11]	Sample of AM* HIGH by RXCLK↑ to Flag Output High-Z Sample of RXEN* Deasserted by RXCLK↑ to RXDATA Output High-Z	1.5	20	ns

CY7C924ADX Receiver Switching Characteristics Over the Operating Range

Parameter	Description	Min	Max	Unit
t_B[15]	Bit Time	5.0	20.0	ns
t_{IN_J}	IN± Peak-to-Peak Input Jitter Tolerance[13, 14]		0.5	UI
t_{SA}	Static Alignment[8, 16]		600	ps
t_{EFW}	Error Free Window[8, 13, 17]	0.65		UI

CY7C924ADX Transmitter Switching Characteristics Over the Operating Range

Parameter	Description	Min	Max	Unit
t_B[15]	Bit Time	5.0	20.0	ns
t_{RISE}	PECL-compatible Output Rise Time 20–80% (PECL Test Load)[8]	200	1700	ps
t_{FALL}	PECL-compatible Output Fall Time 80–20% (PECL Test Load)[8]	200	1700	ps
t_{DJ}	Deterministic Jitter (peak-peak)[8, 18]		0.02	UI
t_{RJ}	Random Jitter (σ)[8, 19]		0.008	UI
t_{JT}	Transmitter Total Output Jitter (pk-pk)[8]		0.08	UI

Notes

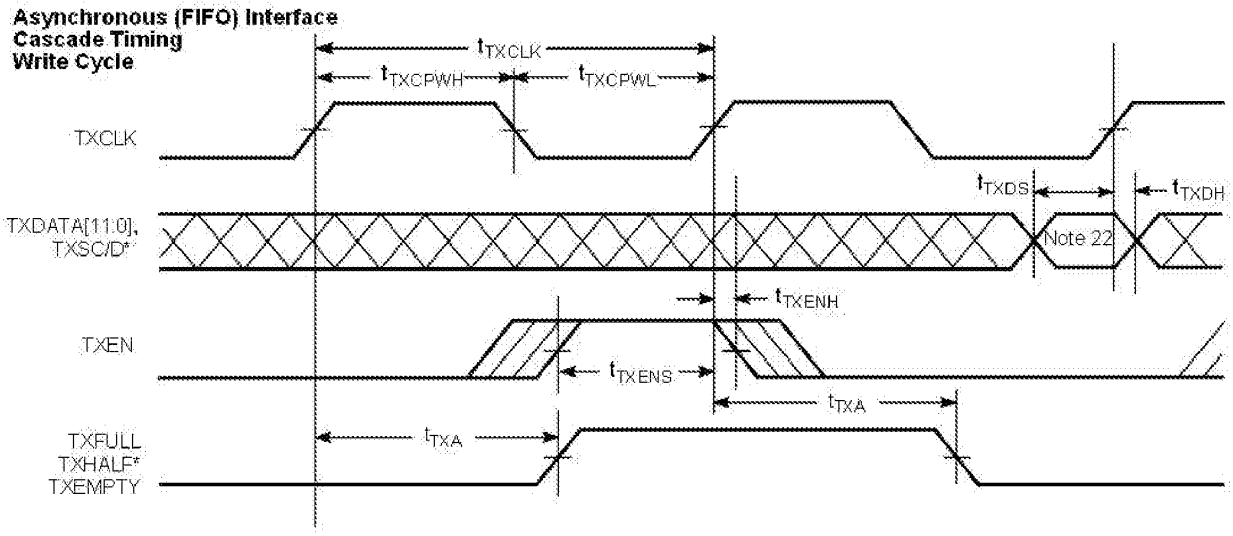
12. The period of f_{ROS} will match the period of the transmitter PLL reference (REFCLK) when receiving serial data. When data is interrupted, RXCLK may drift to REFCLK ±2500 ppm.
13. Receiver UI (Unit Interval) is calculated as 1/(Serial Baud Rate), where Baud Rate is the rate of change of signaling.
14. The specification is sum of 25% Duty Cycle Distortion (DCD), 10% Data Dependant Jitter (DDJ), 15% Random Jitter (RJ).
15. The PECL switching threshold is the midpoint between the V_{OHE} and V_{OLE} specifications (approximately V_{DD} – 1.33 V).
16. Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by the absolute difference of the left and right edge shifts ($|t_{SH\_L} - t_{SH\_R}|$) of one bit until a character error occurs.
17. Error Free Window is a measure of the time window between bit centers where a transition may occur without causing a bit sampling error. EFW is measured over the operating range, input jitter < 50% Dj.
18. While sending continuous K28.5s, outputs loaded to 50Ω to V_{DD} – 1.33 V, over the operating range.
19. While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.

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CY7C924ADX REFCLK Input Switching Characteristics Over the Operating Range

Parameter	Description	Conditions			Min	Max	Unit
		SPDSEL	RANGESEL	BYTE8/10*			
f_{REF}	REFCLK Clock Frequency—50 to 100 MBaud, 10-bit mode, encoder bypass, REFCLK = 2x character rate	0	0	0	8.33	16.67	MHz
	REFCLK Clock Frequency—50 to 100 MBaud, 8-bit mode, REFCLK = 2x character rate	0	0	1	10	20	MHz
f_{REF}	REFCLK Clock Frequency—50 to 100 MBaud, 10-bit mode, encoder bypass, REFCLK = 4x character rate	0	1[20]	0	16.67	33.33	MHz
	REFCLK Clock Frequency—50 to 100 MBaud, 8-bit mode, REFCLK = 4x character rate	0	1[20]	1	20	40	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 10-bit mode, encoder bypass, REFCLK = character rate	1	0	0	8.33	16.67	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 8-bit mode, REFCLK = character rate	1	0	1	10	20	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 10-bit mode, encoder bypass, REFCLK = 2x character rate	1	1	0	16.67	33.3	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 8-bit mode, REFCLK = 2x character rate	1	1	1	20	40	MHz
t_{REFCLK}	REFCLK Period				25	120	ns
t_{REFH}	REFCLK HIGH Time				6.5		ns
t_{REFL}	REFCLK LOW Time				6.5		ns
t_{REFRX}	REFCLK Frequency Referenced to Received Clock Period[21]				–0.04	+0.04	%

CY7C924ADX HOTLink Transmitter Switching Waveforms



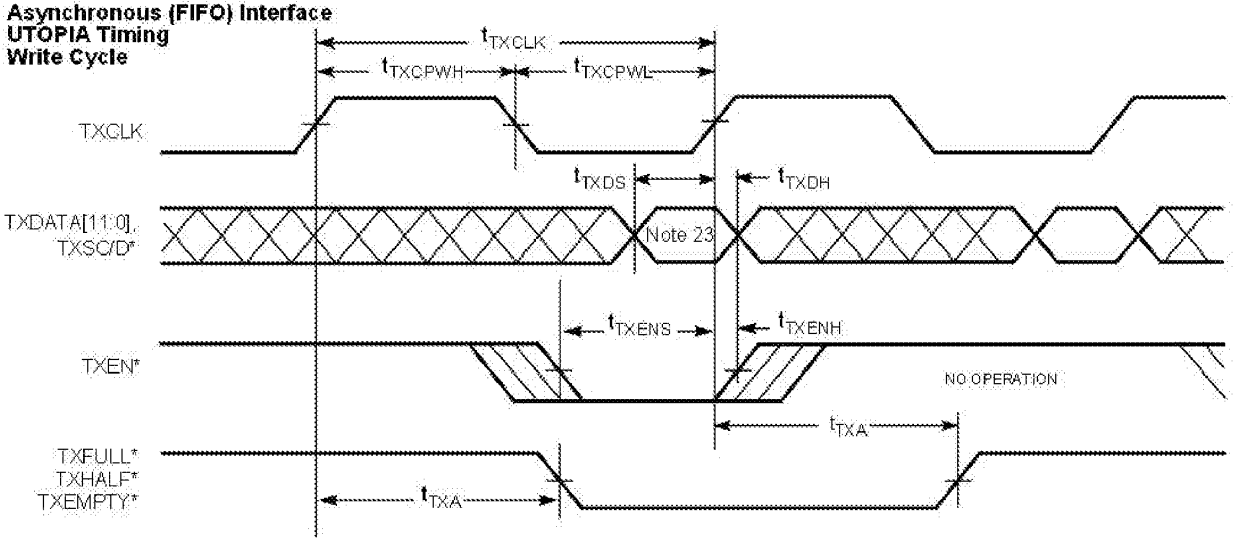
Notes

20. When configured for synchronous operation with the FIFOs bypassed (FIFOBYP* is LOW), if RANGESEL is HIGH the SPDSEL input is ignored and operation is forced to the 100–200 MBaud range.
21. REFCLK has no phase or frequency relationship with RXCLK and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±0.04% of the transmitter PLL reference (REFCLK) frequency.
22. When transferring data to the Transmit FIFO from a depth expanded external FIFO (EXTFIFO = H), the data is captured from the external FIFO one clock cycle following the actual enable.

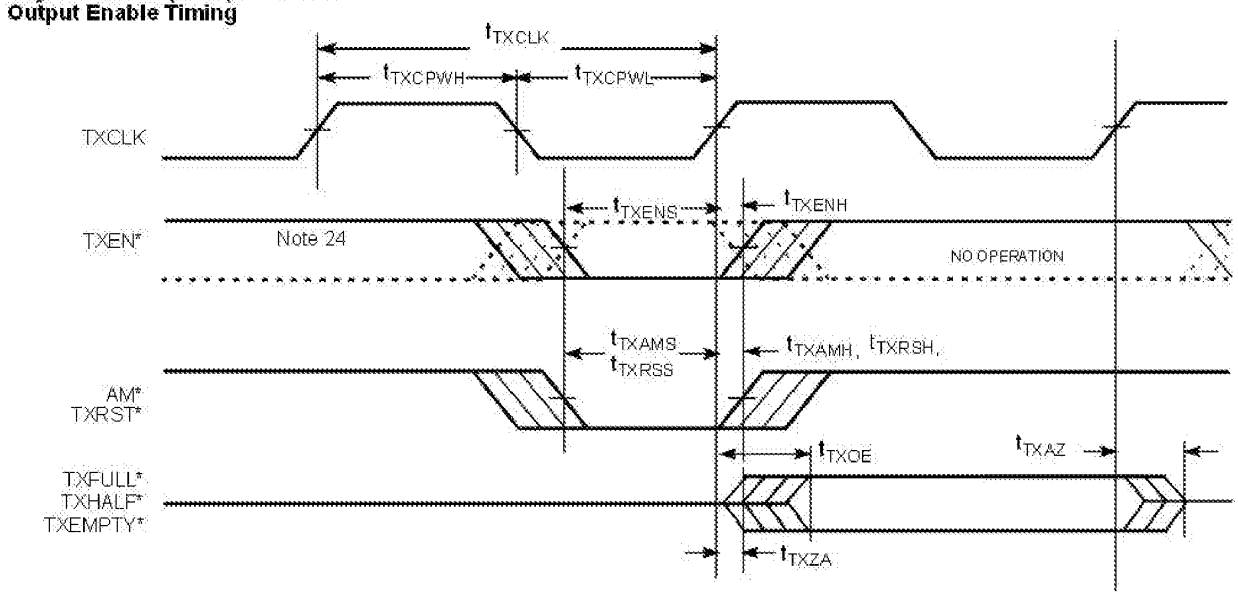
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CY7C924ADX HOTLink Transmitter Switching Waveforms (continued)

Asynchronous (FIFO) Interface
UTOPIA Timing
Write Cycle



Asynchronous (FIFO) Interface
Output Enable Timing

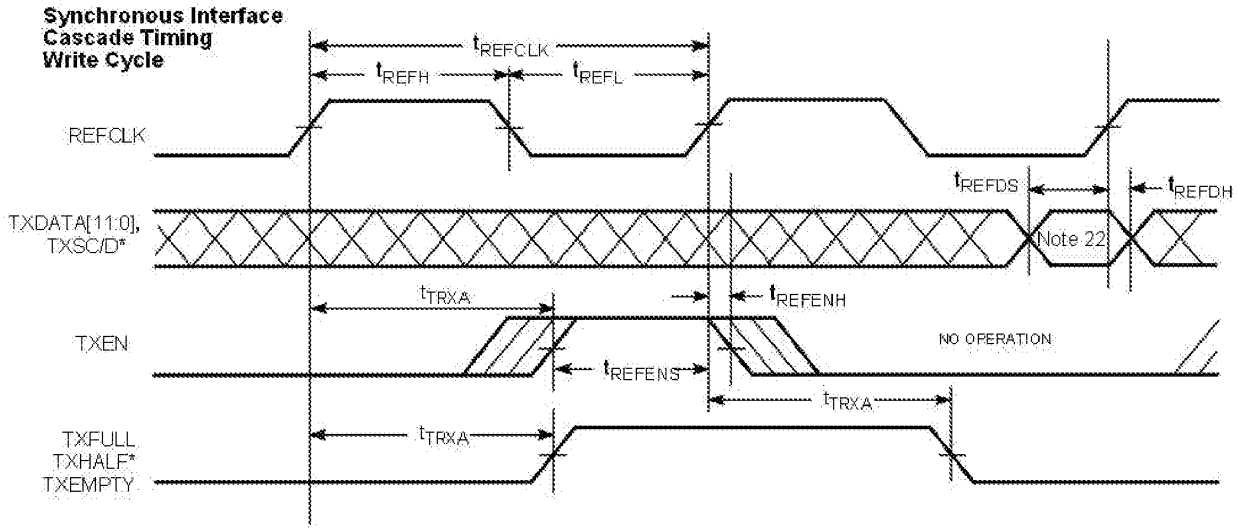


Notes
23. When writing data from a UTOPIA compliant interface (EXTFIFO = L), the write data is captured on the same clock cycle as the data.
24. Signals shown as dotted lines represent the differences in timing and active state of signals when operated in Cascade Timing.

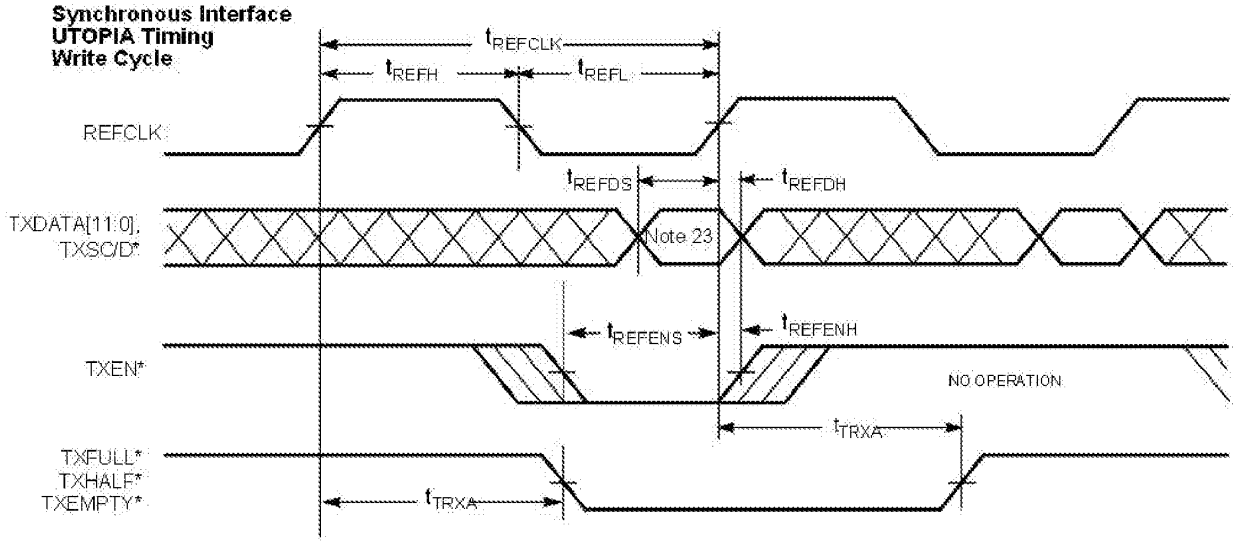
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CY7C924ADX HOTLink Transmitter Switching Waveforms (continued)

Synchronous Interface Cascade Timing Write Cycle



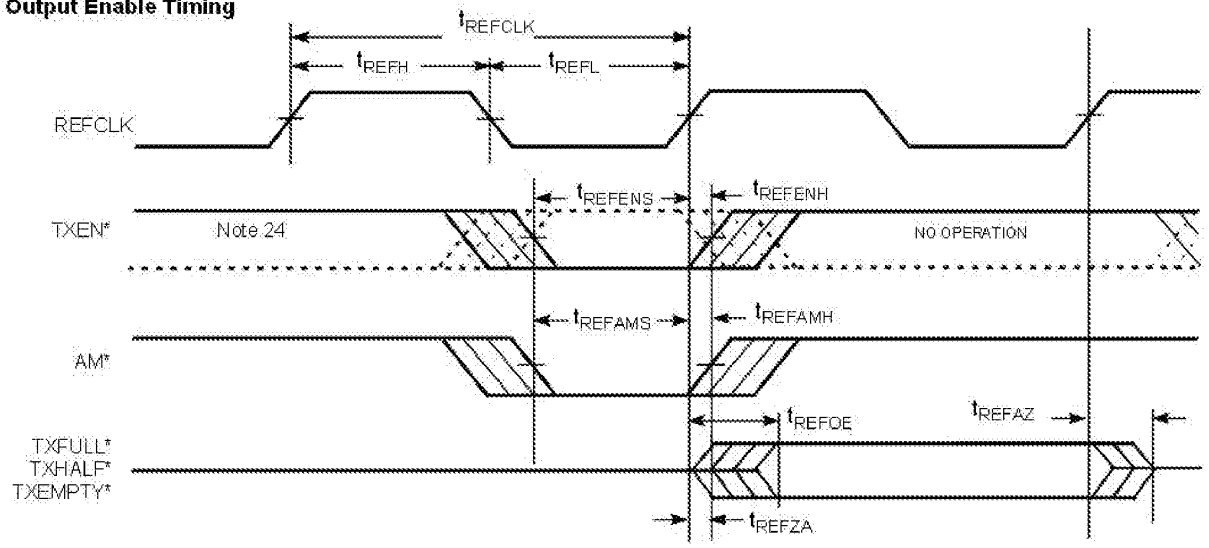
Synchronous Interface UTOPIA Timing Write Cycle



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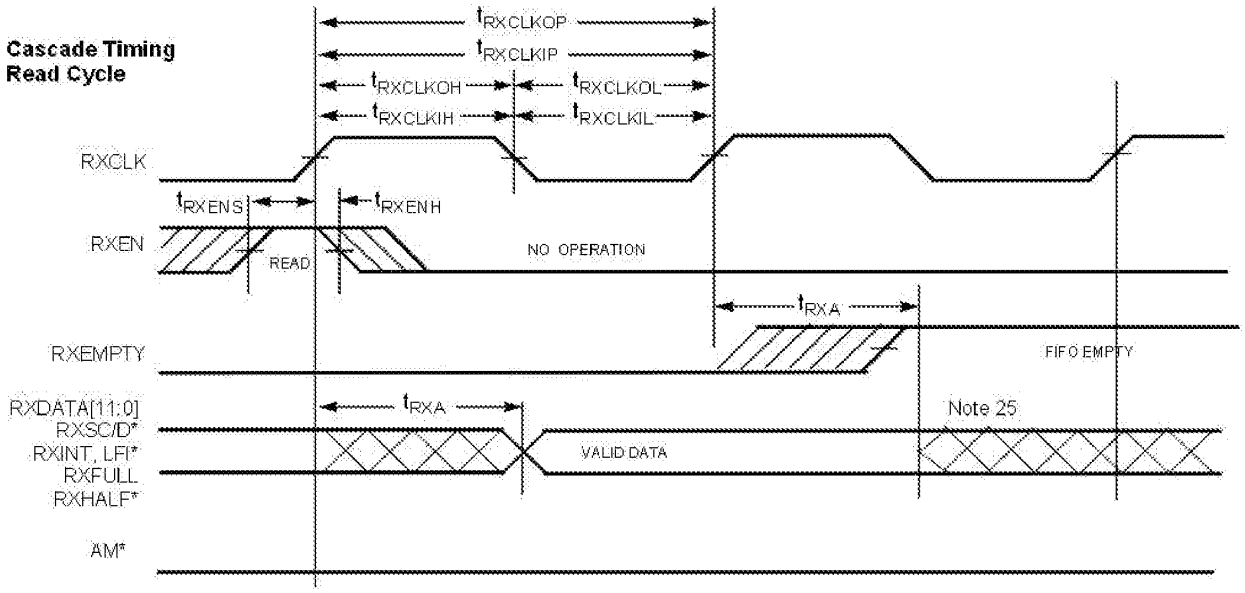
CY7C924ADX HOTLink Transmitter Switching Waveforms (continued)

Synchronous Interface
Output Enable Timing



CY7C924ADX HOTLink Receiver Switching Waveforms

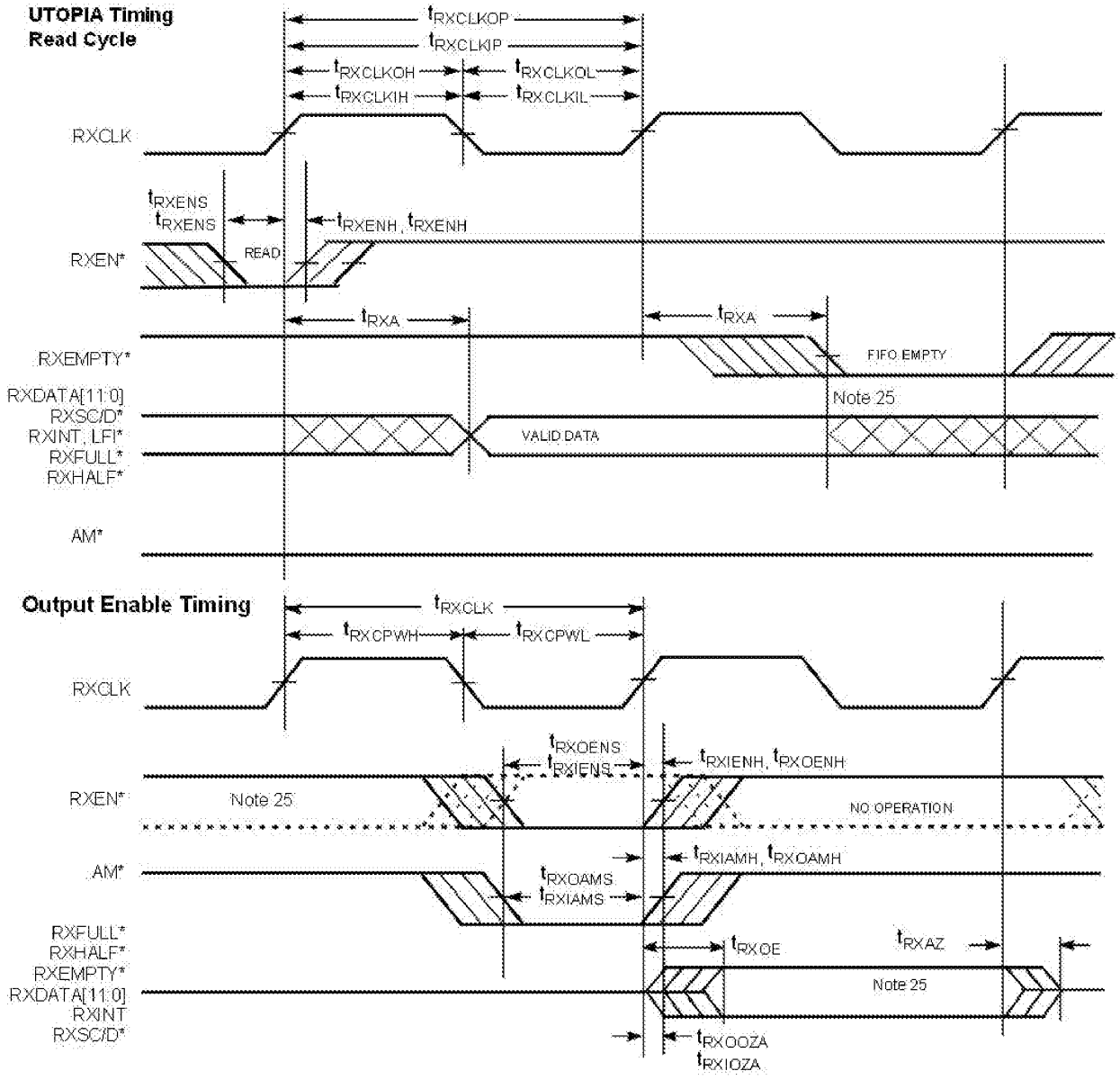
Cascade Timing
Read Cycle



Note
25. On inhibited reads when RXEN* is deasserted or BISTEN* is asserted, or if the Receive FIFO goes empty, the data outputs do not change.

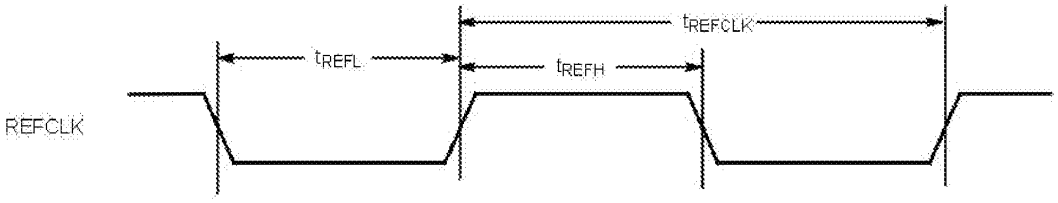
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CY7C924ADX HOTLink Receiver Switching Waveforms (continued)

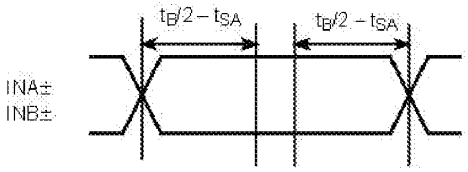


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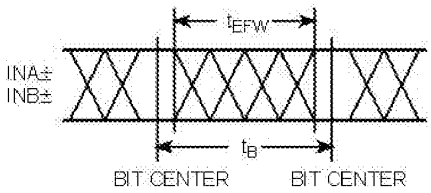
CY7C924ADX HOTLink Receiver Switching Waveforms (continued)



Static Alignment



Error-Free Window



CY7C924ADX HOTLink Transceiver Operation

The interconnection of two or more CY7C924ADX Transceivers form a general-purpose communications subsystem capable of transporting user data at up to 20 MBytes per second over several types of serial interface media. The CY7C924ADX is highly configurable with multiple modes of operation.

In the transmit section of the CY7C924ADX, data moves from the input register, through the Transmit FIFO, to the 8B/10B Encoder. The encoded data is then shifted serially out the OUTx± differential PECL-compatible drivers. The bit-rate clock is generated internally from a 2.5x, 5x, or 10x PLL clock multiplier (3x, 6x, or 12x if BYTE8/10˙ and ENCBYP˙ are LOW). A more complete description is found in the section CY7C924ADX HOTLink Transmit-Path Operating Mode Description.

In the receive section of the CY7C924ADX, serial data is sampled by the receiver on one of the INx± differential line receiver inputs. The receiver clock and data recovery PLL locks onto the selected serial bit stream and generates an internal bit-rate sample clock. The bit stream is deserialized, decoded, and presented to the Receive FIFO, along with a character clock. The data in the FIFO can then be read either slower or faster than the incoming character rate. A more complete description is found in the section *CY7C924ADX HOTLink Receive-Path Operating Mode Description*.

The Transmitter and Receiver parallel interface timing and functionality can be configured to Cascade directly to external FIFOs for depth expansion, to emulate a UTOPIA interface, couple directly to registers, or couple directly to state machines. These interfaces can accept or output either:

- 8-bit characters
- 10-bit characters (for byte-packed encoded transport)
- 10-bit pre-encoded characters (pre-scrambled or pre-encoded)
- 12-bit pre-encoded characters (pre-scrambled or pre-encoded)

The bit numbering and content of the parallel transmit interface is shown in Table 1 on page 14. When operated with the 8B/10B Encoder bypassed, the TXSC/D˙ and RXSC/D˙ bits are ignored.

The HOTLink Transceiver serial interface provides a seamless interface to various types of media. A minimal number of external passive components are required to properly terminate transmission lines and provide LVPECL loads. For power supply decoupling, a single capacitor (in the range of 0.02 µF to 0.1 µF) is required per power/ground pair. Additional information on interfacing these components to various media can be found in the *HOTLink Design Considerations* application note.

CY7C924ADX HOTLink Transmit-Path Operating Mode Description

The HOTLink Transmitter can be configured into several operating modes, each providing different capabilities and fitting different transmission needs. These modes are selected using the FIFOBYP˙, ENCBYP˙ and BYTE8/10˙ inputs on the CY7C924ADX Transceiver. These modes can be reduced to five primary classes:

- Synchronous Encoded
- Synchronous Pre-encoded
- Asynchronous Encoded
- Asynchronous Byte-packed
- Asynchronous Pre-encoded

Synchronous Encoded

In this mode, the Transmit FIFO is bypassed, while the 8B/10B encoder is enabled. One character is accepted at the Transmit Input Register at the rising edge of REFCLK, and passed to the Encoder where it is encoded for serial transmission. The Serializer operates synchronous to REFCLK, which is multiplied by 10 or 5 to generate the serial data bit-clock. In this mode the TXSOC, TXRST˙, TXINT, TXHALT˙, and TXSTOP˙ inputs (when they are not used for data bits) are not interpreted and may be

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tied either HIGH or LOW. To place the CY7C924ADX into synchronous modes, FIFOBYP* must be LOW.

This mode is usually used for products that must meet specific predefined protocol requirements, and cannot tolerate the uncontrolled insertion of C5.0 fill characters. The host system is required to asset TXEN* and to provide new data at every appropriate rising edge of REFCLK to maintain the data stream. If TXEN* is not asserted, the Encoder is loaded with C5.0 (K28.5) sync characters. Because the Encoder is enabled, the transmitted C5.0 characters follow all 8B/10B encoding rules.

Input Register Mapping

In Encoded modes, the bits of the TXDATA input bus are mapped into characters (as shown in Table 1 on page 14), including a TXSVS bit, eight or ten bits of data, and a TXSC/D* bit to select either Special Character codes or Data characters.

If the TXSVS bit is HIGH, an SVS (C0.7) character is passed to the encoder, regardless of the contents of the other TXDATA inputs. If the TXSVS bit is LOW, the associated TXDATA character is encoded per the remaining bits in that character.

The TXSC/D* bit controls the encoding of the TXDATA[7:0] or TXDATA[9:0] bits of each character. It is used to identify if the input character represents a Data Character or a Special Character code. If TXSC/D* is LOW, the character is encoded using the Data Character codes listed in Table 11 on page 52. If TXSC/D* is HIGH, the character is encoded using the Special Character codes listed in Table 12 on page 56.

Synchronous Pre-encoded

In synchronous pre-encoded mode (FIFOBYP* and ENCBYP* are LOW), both the Transmit FIFO and the 8B/10B encoder are bypassed, and data passes directly from the Transmit Input Register to the Serializer. The Serializer operates synchronous to REFCLK to generate the serial data bit-clock. As selected by SPDSEL and RANGESEL, the REFCLK input is multiplied by 5 or 10 when BYTE8/10* is HIGH or by 6 or 12 when BYTE8/10* is LOW. In this mode the TXINT, TXHALT*, TXSVS and TXSOC inputs are used as part of the data input bus.

This mode is usually used for products containing external encoders or scramblers, that must meet specific protocol requirements. The host system is required to assert TXEN* and to provide new data at every appropriate rising edge of the REFCLK to maintain the data stream. If TXEN* is not asserted, the Serializer is loaded with C5.0 (K28.5) sync characters. However, because the bypassed encoder is not able to track the running disparity of the previously transmitted character, the transmitted C5.0 characters may be received with a running disparity code-rule violation.

In this mode the LSB of each input character (TXDATA[0]) is shifted out first, followed sequentially by TXDATA[1] through TXDATA[9].

Asynchronous Encoded

Asynchronous Encoded mode is the most powerful operating mode of the CY7C924ADX. Both the Transmit FIFO and the Encoder are enabled (FIFOBYP* and ENCBYP* are HIGH). This allows transmission of normal data streams, while offering the added benefits of embedded cell or packet markers, an expanded command set, serial addressing, and in-band bypass-signaling (for flow control or other purposes). All characters added to the data stream to support these additional capabilities may be automatically extracted by the Receive Control State Machine in the CY7C924ADX Receiver.

The Serializer operates synchronous to REFCLK, which is multiplied by 2.5, 5, or 10 to generate the serial data bit-clock (as selected by SPDSEL and RANGESEL). In this mode the TXSOC, TXSC_D*, TXRST*, TXSVS, TXINT/TXDATA[8], TXHALT*/TXDATA[9], and TXSTOP* inputs are interpreted.

Embedded Cell Marker

An embedded cell marker is used to mark the start of cells or frames of information passed from one end of the link to the other. This marker is set by asserting TXSOC HIGH, with TXSC/D* and TXSVS both LOW, along with the remaining data on the TXDATA bus. When the data character accompanying this marker is read from the output end of the Transmit FIFO, a C8.0 (K23.7) character is inserted into the data stream prior to the associated data character being read from the Transmit FIFO.

Expanded Commands

The standard 8B/10B Character set contains all 256 possible data characters, but only twelve special or *command* characters. To allow use of a larger selection of command codes, a Special Character code was selected to expand the command set.

An expanded command marker is used to mark the associated data as any one of 256 (2^8) possible commands codes. This marker is generated by asserting both TXSOC and TXSC/D* HIGH, with TXSVS being LOW, along with the associated data on the TXDATA bus. When the character accompanying this marker is read from the output end of the Transmit FIFO, a C9.0 (K27.7) character is inserted into the data stream prior to the data character being read from the Transmit FIFO.

Serial Addressing

The CY7C924ADX receiver has the ability to accept or reject data based on an internal address-controlled switch. This switch is turned on when a serial address matching the receiver address settings is received. When the serial address received does not match the address programmed into the receiver, the receiver's input is ignored.

A serial address is transmitted by asserting TXSOC, TXSC/D*, and TXSVS all HIGH. When the character accompanying this marker is read from the output end of the Transmit FIFO, a C10.0 (K29.7) character is inserted into the data stream prior to the data characters being read from the Transmit FIFO. The serial address is either 8 or 10 bits depending on the level on BYTE8/10*.

In-Band Bypass-Signaling

In-band bypass-signaling allows a signal to be sent to the remote receiver without that signal having to pass through the Transmit (or Receive) FIFO. When TXINT transitions, a character is immediately inserted in the data stream at the Encoder block, delaying other data encoding for a cycle.

When TXINT transitions from 0→1, a C0.0 (K28.0) special character is sent. When TXINT transitions from 1→0, a C3.0 (K28.3) special code is sent. These special codes may be used to force a similar signal transition on the RXINT output of an attached CY7C924ADX HOTLink Receiver.

This input may be used to transport a low data rate signal (like a serial RS-232/UART signal) across the interface, without any

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significant impact on the actual data being transported across the link. It may also be used to transparently propagate FIFO flow control information across the link by directly connecting the RXHALF# flag of the local receiver to the TXINT of the local transmitter. The RXINT at the remote end of the link can then be connected to the TXHALT# input to halt data transfers at the remote end of the link until the local Receive FIFO has sufficient room to continue.

Asynchronous Byte-Packed

Asynchronous byte-packed mode contains the same features as asynchronous encoded, but with support for 10-bit source data. This data is byte-packed through the 8B/10B encoder to deliver the data across the interface. This mode is enabled when FIFOBYP# and ENCBYP# are HIGH and BYTE8/10# is LOW.

When sending extended commands, the larger 10-bit character size enlarges the extended command space to 1024 (2^{10}) possible commands codes.

Asynchronous Pre-encoded

In Asynchronous pre-encoded modes, the Transmit FIFO is enabled and the Encoder is disabled (FIFOBYP# is HIGH and ENCBYP# is LOW). This means that all words clocked into the input register are written to the Transmit FIFO before being sent to the Serializer. The Serializer operates synchronous to REFCLK to generate the serial data bit-clock. SPDSEL and RANGESEL determine whether REFCLK is multiplied by 10, 5 or 2.5 (if BYTE8/10# is HIGH) or 3, 6 or 12 (if BYTE8/10# is LOW). In this mode the TXINT and TXHALT# inputs are used as part of the 10-bit input character. TXSVS, TXSOC and TXSTOP# are still available.

These modes are usually used for products containing external encoders or scramblers, that must meet specific protocol requirements. The host system must assert TXEN# and provide new data at every rising edge of TXCLK to maintain the data stream (without overfilling the Transmit FIFO). If the Transmit FIFO ever goes empty, the Serializer is loaded with an alternating disparity string of C5.0 (K28.5) sync characters (when BYTE8/10# is HIGH) or the bit pattern 0110000100011 (when BYTE8/10# is LOW).

This insertion can be an issue for some system implementations. If the remote receiver is configured to decode 8B/10B coded characters, it will probably detect running disparity errors because the bypassed Encoder is not able to track the running disparity of the previously transmitted character. However, since these pre-encoded modes are generally used with alternate forms of scrambling or encoding, for these applications this disparity is not generally an issue.

To maintain a data stream without adding these C5.0 SYNC codes, it is necessary that the Transmit FIFO be loaded at the same speed or faster than the rate that data is read from that FIFO.

CY7C924ADX HOTLink Receive-Path Operating Mode Descriptions

The HOTLink Receiver can be configured into several operating modes, each providing different capabilities and fitting different reception needs. These modes are selected using the FIFOBYP#, ENBYP# and BYTE8/10# inputs on the CY7C924ADX Transceiver. These modes can be reduced to five primary classes:

- Synchronous Decoded
- Synchronous Undecoded
- Asynchronous Decoded
- Asynchronous Byte-packed
- Asynchronous Undecoded.

In all these modes, serial data is received at one of the differential line receiver inputs and routed to the Deserializer and Framer. The PLL in the clock and data recovery block is used to extract a bit-rate clock from the transitions in the data stream, and uses that clock to capture bits from the serial stream. These bits are passed to the Deserializer where they are formed into 10- or 12-bit characters.

To align the incoming bit stream to the proper character boundaries, the Framer must be enabled by asserting RFEN HIGH. The Framer logic-block checks the incoming bit stream for the unique pattern that defines the character boundaries. This logic filter looks for the ANSI X3.230 symbol defined as a "Special Character Comma" (K28.5 or C5.0). Once a K28.5 is found, the Framer captures the offset of the data stream from the present character boundaries, and resets the boundary to reflect this new offset, thus framing the data to the correct character boundaries.

Since noise induced errors can cause the incoming data to be corrupted, and since many combinations of corrupt and legal data can create and aliased K28.5, the framer may also be disabled by setting RFEN LOW.

An option exists in the framer to require multiple K28.5 characters, meeting specific criteria, before the character boundaries are reset. This multi-byte mode of the Framer is enabled by keeping RFEN asserted HIGH for greater than 2048 character clock cycles. For multi-byte framing, the receiver must find a pair of K28.5 characters, both on identical 10-bit boundaries, within a 5-character span (50 bits) before it shifts its framing boundaries. This option greatly reduces the probability of framing to aliased K28.5 characters while still allowing many links to maintain synchronization.

Synchronous Decoded

In these modes, the Receive FIFO is bypassed, while the 10B/8B Decoder is enabled (FIFOBYP# is LOW and ENCBYP# is HIGH). Framed characters output from the Deserializer are decoded, and passed direct to the Receive Output Register. The Deserializer operates synchronous to the recovered bit-clock, which is divided by 10 generate the output RXCLK clock. In this mode the RXRST# input is not interpreted and may be biased either HIGH or LOW.

These modes are usually used for products that must meet specific protocol requirements. New decoded characters are provided at the RXDATA outputs once every rising edge of RXCLK. When RXEMPTY# is deasserted along with the data, it indicates that a valid character (as selected by RXMODE[1:0]) is present at the RXDATA outputs. When asserted it indicates that a C5.0 (K28.5) not kept by the current RXMODE[1:0] setting is present on the RXDATA output bus. Because the decoder is enabled, all received characters are checked for compliance to the 8B/10B decoding rules.

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Output Register Mapping

The RXDATA[11:0] output bus is mapped into a character consisting of eight bits of data, one bit that carries violation information, and an RXSC/D* bit that identifies the character as either control or data.

These bits have combinations that identify the meaning of the remaining bits of the character. If RXRVS is HIGH and RXSC/D* is HIGH the decoder outputs a C0.7, C1.7, C2.7 or C4.7 in response to reception of either an SVS (C0.7) character or other invalid character.

Synchronous Undecoded

In this mode, both the Receive FIFO and the 10B/8B Decoder are bypassed (FIFOBYP* and ENCBYP* are LOW), and data passes directly from the Deserializer to the output register. The Deserializer operates synchronous to the recovered bit-clock, which is divided by 10 or 12 to generate the output RXCLK clock. In this mode the RXRST* input is not interpreted and may be biased either HIGH or LOW.

This mode is usually used for products containing external decoders or descramblers that must meet specific protocol requirements. New data is provided at the RXDATA outputs once every rising edge of RXCLK. Received characters are not checked for any specific coding requirements and no decoding errors are reported.

Asynchronous Decoded

Asynchronous Decoded mode is the most powerful operating mode of the CY7C924ADX HOTLink Receiver. Both the Receive FIFO and the Decoder are enabled (FIFOBYP* and ENCBYP* are HIGH). This allows reception of normal data streams, while offering the added benefits of embedded cell markers, an expanded command set, serial address support, and in-band bypass-signaling (for flow control or other purposes). All characters added to the data stream by the transmitter to support these additional capabilities may be automatically extracted by the Receive Control State Machine in the CY7C924ADX Transceiver.

The deserializer operates synchronous to the recovered bit-clock, which is divided by 10 to generate the Receive FIFO write clock. When the Receive FIFO is addressed by AM* and selected by RXEN*, characters are read from the FIFO using the external RXCLK input.

Asynchronous Decoded mode support the same Output Register mapping as the Synchronous Decoded mode. Because both the Receive FIFO and Decoder are enabled, the output FIFO may be read at any rate supported by the FIFO (0 to 50MHz), however, if the Receive FIFO ever indicates a full condition (RXFULL* is asserted), data may be lost.

Embedded Cell Marker

An embedded cell marker is used to mark the start of cells or frames of information passed from one end of the link to the other. When a C8.0 (K23.7) character is detected in the data stream, the next character is written to the Receive FIFO along with RXSOC set HIGH, and RXSC/D* and RXRVS set LOW. When the character accompanying this marker is read from the Receive FIFO with these same bits set, it indicates the start of a cell or frame.

Expanded Command

The standard 8B/10B Character set contains all 256 possible data characters, but only twelve Special Character codes. To allow use of a larger selection of command codes, one Special Character code was selected to expand the command set.

An Expanded Command marker is used to mark the associated data as any one of 256 (2^8) possible commands codes. When a C9.0 (K27.7) character is detected in the data stream, the following character is written to the Receive FIFO along with both RXSOC and RXSC/D* set HIGH, and RXRVS set LOW. When the character accompanying this marker is read from the Receive FIFO with these same bits set, it may be used to indicate that the data on the RXDATA bus is an Expanded Command.

Serial Addressing

The CY7C924ADX receive path can be directed to accept all characters, or to only accept that data specifically addressed to it. This address control is managed through an embedded Address Compare Register in the receiver logic. This register supports either domain (multicast) or exact-match (unicast) based compares on an address field received across the serial link. When a C10.0 (K29.7) special code is received, the immediately following data character contains the address field that is compared with the receiver Serial Address Register contents.

When the CY7C924ADX is configured for multicast address matching, the received address field is compared as an OR of a bit-wise AND with the Serial Address Register. A valid match between any of the bits sets the switch to allow the following data to be written into the Receive FIFO. If no matches are found, the data is not written to the Receive FIFO and is discarded.

When the CY7C924ADX is configured for unicast address matching, the received address field is compared for an exact match with the Serial Address Register. If an exact match is found, a switch is set in the receiver to accept all following data until the next serial address marker is found. If they do not match, the data is not written to the Receive FIFO and is discarded.

In-Band Bypass-Signaling

In-band bypass-signaling allows a signal to be received at the local receiver without that signal having to pass through the Receive FIFO.

When a C0.0 (K28.0) character is received, the RXINT output is set HIGH. When a C3.0 (K28.3) character is received, the RXINT output is set LOW. These special codes are generated by forcing similar transitions into the TXINT input of the CY7C924ADX HOTLink Transmitter sourcing the data stream.

This output may be used to transport a low data-rate signal (like a serial RS-232/UART signal) across the interface, without any significant impact on the actual data being transported across the link. It may also be used to transparently propagate FIFO flow-control information across the link by directly connecting the RXHALF* flag of the local receiver to the TXINT of the local transmitter. The RXINT at the remote end of the link can then be connected to the TXHALT* input to halt data transfers at the remote end of the link until the local Receive FIFO has sufficient room to continue.

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Asynchronous Byte-Packed

Asynchronous byte-packed mode contains the same features as asynchronous decoded, but with support for 10-bit source data (BYTE8/10* is LOW). The received characters are decoded first back into 8-bit data characters, which are then reassembled into 10-bit source data.

Because of the time difference involved with the packing and unpacking operations, this mode can only be used with the internal FIFOs enabled.

When receiving extended commands, the larger 10-bit character size enlarges the extended command space to 1024 (2^{10}) possible commands codes.

When receiving a serial address, the larger 10-bit character size also increases the Serial Address Register to 10 bits. This allows up to 10 separate domains for multicast addressing or 1024 unique addresses for unicast addressing.

Asynchronous Undecoded

In Asynchronous Undecoded modes, the Receive FIFO is enabled (FIFOBYP* is HIGH and ENCBYP* is LOW). This means that all characters received from the serial interface are written to the Receive FIFO before being passed to the output register. The Deserializer operates synchronous to the recovered bit-clock, which is divided by 10 or 12 to generate the Receive FIFO write clock. Data is read from the Receive FIFO, using the RXCLK input clock, when addressed by AM* and selected by RXEN*.

These modes are usually used for products containing external decoders or descramblers, that must meet specific protocol requirements. New data may be read from the Receive FIFO any time that the FIFO status flags indicate a non-empty condition (RXEMPTY* is deasserted). To ensure that data is not lost through a FIFO overflow, the Receive FIFO must be read faster than data is loaded into the Receive FIFO.

If the receiver is to provide framed characters, it is necessary for the transmit end to include C5.0 (K28.5) characters in the data stream. This can be done by:

- Operating the transmitter in encoded mode and writing C5.0 characters into the data stream
- Operating the transmitter in pre-encoded mode and writing the 10-bit value for an encoded C5.0 character to the data stream (1100000101 or 0011111010)
- Deasserting TXEN* when the transmitter is operated in synchronous mode
- Asserting TXHALT*, or by allowing the transmit FIFO to go empty when it is operated in asynchronous mode.

BIST Operation and Reporting

The CY7C924ADX HOTLink Transceiver incorporates the same Built-In Self-Test (BIST) capability used with the HOTLink CY7B923/ CY7B933 and HOTLink II CYP(V)15G0x0x families. This link diagnostic uses a Linear Feedback Shift Register (LFSR) to generate a 511-character repeating sequence that is compared, character-for-character, at the receiver.

BIST mode is intended to check the entire high-speed serial link at full link-speed, without the use of specialized and expensive test equipment. The complete sequence of characters used in BIST are documented in the *HOTLink Built-In Self-Test* application note.

BIST Enable Inputs

There are separate BIST enable inputs for the transmit and receive paths of the CY7C924ADX. These inputs are both active LOW; i.e., BIST is enabled in its respective section of the device when the BIST enable input is determined to be at a logic-0 level. Both BIST enable inputs are asynchronous; i.e., they are synchronized inside the CY7C924ADX to the internal state machines.

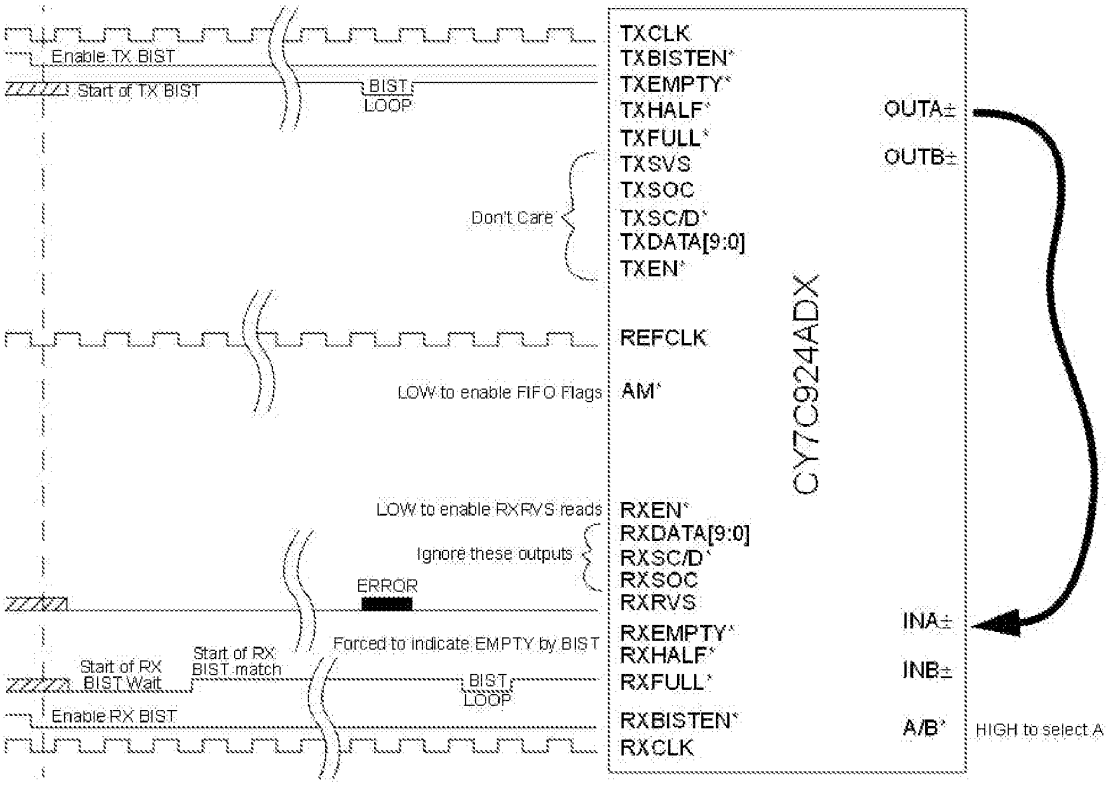
BIST Transmit Path

The transmit path operation with BIST is controlled by the TXBISTEN* input and overrides most other inputs (see Figure 8). When the Transmit FIFO is enabled (not bypassed) and TXBISTEN* is recognized internally, all reads from the Transmit FIFO are suspended and the BIST generator is enabled to sequence out the 511 character repeating BIST sequence. If the Transmit Control State Machine was in the middle of an atomic operation (e.g., sending an extended command) the Data Character associated with the Special Character code is transmitted prior to recognition of the TXBISTEN* signal and suspension of FIFO data processing. If the recognition occurs in the middle of a data field, the following data is not transmitted at that time, but remains in the Transmit FIFO. Once the TXBISTEN* signal is removed, the data in the Transmit FIFO is again available for transmission. To ensure proper data handling at the destination, the transmit host controller should either use TXHALT* or TXSTOP* to segment transmission of data at specific boundaries, or allow the Transmit FIFO to completely empty before enabling BIST.

With transmit BIST enabled, the Transmit FIFO remains available for loading of data. It may be written up to its normal maximum limit while the BIST operation takes place. To allow removal of stale data from the Transmit FIFO, it may also be reset during a BIST operation. The reset operation proceeds as documented, with the exception of the information presented on the TXEMPTY* FIFO status flag. Since this flag is used to present BIST loop status, it continues to reflect the state of the transmit BIST loop status until TXBISTEN* is no longer recognized internally. The completion of the reset operation may still be monitored through the TXFULL* FIFO status flag.

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Figure 8. Built-In Self-Test Illustration, UTOPIA Mode



The TXEMPTY* flag, when used for transmit BIST progress indication, continues to reflect the active HIGH or active LOW settings determined by the UTOPIA or Cascade timing model selected by EXTFIFO; i.e., when configured for the Cascade timing model, the TXEMPTY* and TXFULL* FIFO flags are active HIGH, when configured for the UTOPIA timing model the TXEMPTY* and TXFULL* FIFO flags are active LOW. The illustration in Figure 8 uses the UTOPIA conventions.

When TXBISTEN* is first recognized, the TXEMPTY* flag is clocked to a reset state, regardless of the addressed state of the Transmit FIFO (if AM* is LOW or not), but is not driven out of the part unless AM* has been sampled asserted (LOW). Following this, on each completed pass through the BIST loop, the TXEMPTY* flag is set for one interface clock period (TXCLK or REFCLK).

When the Transmit FIFO is enabled, the TXEMPTY* flag remains set until the interface is addressed and the state of TXEMPTY* has been observed. If the device is not addressed (AM* is not sampled LOW), the flag remains set internally regardless of the number of TXCLK clock cycles that are processed. If the device status is not polled on a sufficiently regular basis, it is possible for the host system to miss one or more of these BIST loop indications.

A pass through the loop is defined as that condition where the Encoder generates the D0.0 state that initiates the BIST loop. Depending on the initial state of the BIST LFSR, the first pass through the loop may occur at substantially less than 511 character periods. Following the first pass, as long as TXBISTEN* remains LOW, all remaining passes are exactly 511 characters in length.

When the Transmit FIFO is bypassed, the interface is clocked by the REFCLK signal instead of TXCLK. While the active or asserted state of the TXEMPTY* signal is still controlled by the EXTFIFO, the state of any completed BIST loops is no longer preserved. Instead, the TXEMPTY* flag reflects the dynamic state of the BIST loop progress, and is asserted only once every 511 character periods. If the interface is not addressed at the time that this occurs, then the FIFO status flags remain in a High-Z state and the loop event is lost.

BIST Receive Path

The receive path operation in BIST is similar to that of the transmit path. While the Receive FIFO is enabled and RXBISTEN* is recognized internally, all writes to the Receive FIFO are suspended. If the receiver had a previous serial address match and was accepting data, no additional characters are written to the Receive FIFO. If the receive data state machine was in the middle of processing a multi-character sequence or other atomic operation (e.g., a start of cell marker and its

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associated data), the characters associated with the atomic operation are discarded and not written to the Receive FIFO.

Upon internal recognition of RXBISTEN^, the serial address match flag is cleared such that once BIST has been disabled and data is again being received, all received data is rejected until a new serial address is again received that matches the address match criteria.

Note. If the CY7C924ADX is set to match all data (all 1s in the multicast match field), then it is not necessary to get an address match before receiving data following the termination of BIST. On reset or when programmed to this state, the device ignores all serial address commands and matches all data.

Any data present in the Receive FIFO when RXBISTEN^ is recognized remains in the FIFO and cannot be read until the BIST operation is complete. The data in the Receive FIFO remains valid, but is NOT available for reading through the host parallel interface. This is because the error output indicator for receive BIST operations is the RXRVS signal, which is normally part of the RXDATA bus. To prevent read operations while BIST is in operation, the RXEMPTY^ and RXHALF^ flags are forced to indicate an Empty condition. Once RXBISTEN^ has been removed and recognized internally, the Receive FIFO status flags are updated to reflect the current content status of the Receive FIFO.

To allow removal of stale data from the Receive FIFO, it may be reset during a BIST operation. The reset operation proceeds as documented, with the exception that the RXEMPTY^ and RXHALF^ status flags already indicate an empty condition. The RXFULL^ flag is used to present BIST progress. The active state on RXFULL^ and RXEMPTY^ flags remain controlled by the present operating mode and interface timing model (UTOPIA or Cascade) as selected by EXTFIFO^.

When RXBISTEN^ has been recognized, RXFULL^ becomes the receive BIST loop indicator, regardless of the logic state of FIFOBYP^. When RXBISTEN^ is first recognized with the Receive FIFO enabled, the RXFULL^ flag is clocked to a set state, regardless of the addressed state of the Receive FIFO (if AM^ is sampled LOW or not). Following this, RXFULL^ remains set until the receiver detects the start of the BIST pattern. Then RXFULL^ is deasserted for the duration of the BIST pattern, pulsing asserted for one RXCLK period on the last symbol of each BIST loop. If 14 of 28 consecutive characters are received in error, RXFULL^ returns to the set state until the start of a BIST sequence is again detected.

Just like the BIST status flag on the transmit data path, when the Receive FIFO is enabled the RXFULL^ flag captures the asserted states, and keeps them until they are read. This means that if the status flag is not read on a regular basis, events may be lost.

The detection of errors is presented on the RXRVS output. Unlike the RXFULL^ FIFO status flag, the active state of this output is not controlled by the EXTFIFO input. With the Receive FIFO enabled, these outputs should operate the same as the RXFULL^ flag, with respect to preserving the detection state of an error until it is read.

Unlike the RXFULL^ flag, which only needs the CY7C924ADX to be addressed (AM^ sampled LOW by RXCLK) to enable the RXFULL^ three-state driver, and an RXCLK to "read" the flag, the RXRVS output requires a selection (assertion of RXEN^ while addressed) to enable the RXDATA bus three-state drivers. The selection process is necessary to ensure that a multi-PHY implementation does not enable multiple RXRVS drivers at the same time.

When the Receive FIFO is bypassed, the interface is clocked by the RXCLK output signal. While the active or asserted state of the RXFULL^ signal is still controlled by the EXTFIFO input, the state of any completed BIST loops or detected errors are no longer preserved. Instead, the RXFULL^ flag reflects the dynamic state of the BIST loop progress, and is asserted only once every 511 character periods. If the interface is not addressed at the time that this occurs, then the FIFO status flags remain in a High-Z state and the loop event is lost. This is also true of the RXRVS output, such that if the CY7C924ADX receive path is not selected to enable the RXDATA bus three-state drivers, the detection of a BIST miscompare is lost.

BIST Three-state Control

When BIST is enabled on either the transmitter or the receiver, the three-state enable signals for the BIST status flags and error indicators work the same as for normal data processing. The output drivers for the BIST status that is presented on FIFO status flags are only enabled when AM^ has been sampled asserted (LOW) by the respective clock (TXCLK, RXCLK, or REFCLK).

To access the BIST error information, it is necessary to perform a read cycle of the addressed receiver. This means that AM^ must be LOW to allow a receiver address match (Rx_Match) to exist, and RXEN^ must then be asserted to select the device. Because the part is in BIST, no data is read from the FIFO, but the data bus is driven. This allows the RXRVS indicator to be driven onto the RXDATA bus. So long as RXEN^ remains asserted, the receiver stays selected, the data bus remains driven, and RXRVS has meaning.

Bus Interfacing

The parallel transmit and receive host interfaces to the CY7C924ADX are configurable for either synchronous or asynchronous operation. Each of these configurations supports two selectable timing and control models of UTOPIA or Cascade.

All asynchronous bus configurations have the internal Transmit and Receive FIFOs enabled. This allows data to be written or read from these FIFOs at any rate up to the maximum 50-MHz clock rate of the FIFOs. All internal operations of the CY7C924ADX do not use the external TXCLK or RXCLK, but instead make use of synthesized derivatives of REFCLK for transmit path operations and a recovered character clock for receive path operations.

All synchronous bus configurations require the bus interface operations to be synchronous to REFCLK on the transmit path and the recovered clock (output as RXCLK) on the receive path. The internal FIFOs are bypassed in all synchronous modes.

The two supported timing and control models are UTOPIA and Cascade. These timing models take their name from their default configuration. The UTOPIA timing model is based on the ATM Forum UTOPIA interface standards. This timing model is that of a FIFO with active LOW FIFO status flags and read/write enables.

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The Cascade timing model is a modification of the UTOPIA configuration that changes the flags and FIFO read/write enables to active HIGH. This model is present primarily to allow depth expansion of the internal FIFO by direct coupling to external CY7C42x5 synchronous FIFOs. To allow this direct coupling, the FIFO flag active levels and cycle-to-cycle timing between the transmit enable (TXEN*) and data latching are modified to ensure correct data transfer.

These four configurations of bus operation and timing/control can all be used with or without external FIFOs. Depending on the specific mode selected, the amount of external hardware necessary to properly couple the CY7C924ADX to state machines or external FIFOs is minimal in all cases, and may be zero if the proper configuration is selected.

UTOPIA Interface Background

The UTOPIA interface is defined by the ATM Forum as the bus interface between the ATM and PHY layer devices of an ATM system. This interface is defined as 8 or 16 bits wide, with the latter reserved mainly for high-speed physical interfaces (PHYs) such as 622 Mbps OC-12. Due to the limited speed range of the CY7C924, only the 8-bit interface is implemented.

UTOPIA-1 was the original UTOPIA specification (created in 1993) which covers transport of:

- 155.52 Mbps (scrambled SONET/OC-3)
- 155.52 Mbps (8B/10B block coded at 194.4 MBaud)
- 100 Mbps (4B/5B encoded TAXI)
- 44.736 Mbps (DS-3/T3)
- 51.84 Mbps (OC-1)

The UTOPIA-1 interface has a maximum clock rate of 25 MHz. All AC-timing and pin descriptions are covered in the UTOPIA-1 Specification, Version 2.01.

UTOPIA-2 was created as an addendum to the UTOPIA-1 specification. In this revision, the parallel interface was extended to both 33 MHz and 50 MHz to accommodate PCI bus architectures in ATM designs. A method of addressing was added to allow multiple devices (PHYs) to share a common host bus. Also, a description of a management interface was added (not supported by this device).

The CY7C924ADX contains all pins necessary to support the UTOPIA-1 and, through use of an external address decoder, can emulate the multi-PHY capability of a UTOPIA-2 interface. The maximum bus speed supports the full 50 MHz I/O rate for emerging high-performance systems.

UTOPIA Address Match and Selection

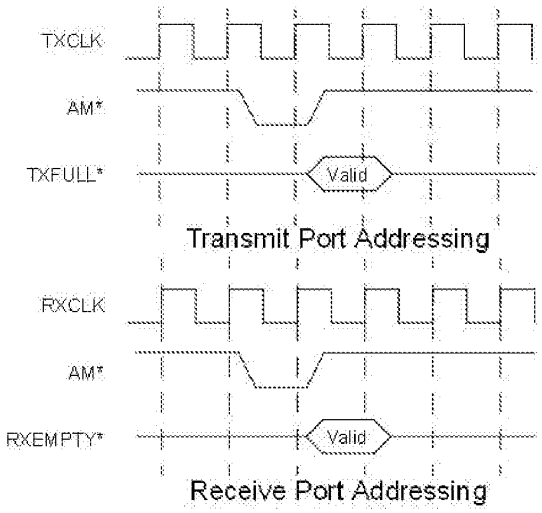
All actions on a UTOPIA-2 interface are controlled by the Address Match and selection states of the interface. These states control the read and write access to the Receive and Transmit FIFOs, access to the FIFO status flags, reset of the Transmit and Receive FIFOs, and read and write access to the Serial Address Register. The CY7C924ADX supports the concept of an "address match" through a single Address Match (AM*) input.

Address Match and FIFO Flag Access

The CY7C924ADX makes use of a single active-LOW Address Match (AM*) to generate address-match conditions. When this input is LOW it is equivalent to an ATM address compare on both the TXADDR and RXADDR buses. This allows multiple CY7C924ADX devices to share a common bus, with device output three-state controls being managed by either an address match condition (AM* sampled LOW), or by a selection state.

The Transmit and Receive FIFO flag empty and FIFO full output drivers are enabled in any TXCLK, REFCLK, or RXCLK cycle following AM* being sampled asserted (LOW) by the rising edge of the respective clock. The AM* input is sampled separately by the clocks for the transmit and receive interfaces, which allows these clocks to operate at different clock rates. An example of both Transmit and Receive FIFO flag access is shown in Figure 9.

Figure 9. FIFO Flag Driver Enables



When the Transmit FIFO is enabled (FIFOBYP* is HIGH) and AM* is sampled LOW by the rising edge of TXCLK, the output drivers for the TXFULL* and TXEMPTY* FIFO flags are enabled. When AM* is sampled HIGH by the rising edge of TXCLK, these same output drivers are disabled.

When the Transmit FIFO is bypassed (FIFOBYP* is LOW and not in byte-packed mode) and AM* is sampled LOW by the rising edge of REFCLK, the output drivers for the TXFULL* and TXEMPTY* FIFO flags are enabled. When AM* is sampled HIGH by the rising edge of REFCLK, the FIFO flag output drivers are disabled.

When AM* is sampled LOW by the rising edge of RXCLK (input or output), the output drivers for the RXFULL* and RXEMPTY* FIFO flags are enabled. When AM* is sampled HIGH by the rising edge of RXCLK, the FIFO flag output drivers are disabled.

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Device Selection

The concept of selection is used to control the access to the transmit and receive parallel-data ports of the device. There are three primary types of selection:

- Transmit data selection (with and without internal Transmit FIFO)
- Receive data selection (with and without internal Receive FIFO)
- Continuous selection (for either or both transmit and receive interfaces)

In addition to these normal selection types, there are two additional sequences that are used to control the internal Transmit and Receive FIFOs reset operations, and to control read/write access to the Serial Address Register:

- Transmit reset sequence
- Receive reset sequence (includes access to the Serial Address Register)

Of these operations, the transmit data selection and transmit reset sequence are mutually exclusive and cannot exist at the same time. The receive data selection and receive reset sequence are also mutually exclusive and cannot exist at the same time. Either transmit operation can exist at the same time as either receive operation.

All normal forms of selection require that an Address Match condition must exist (AM* sampled LOW) either at the same time as the selection control signal being sampled asserted, or one or more clock cycles prior to the selection control signal being sampled asserted.

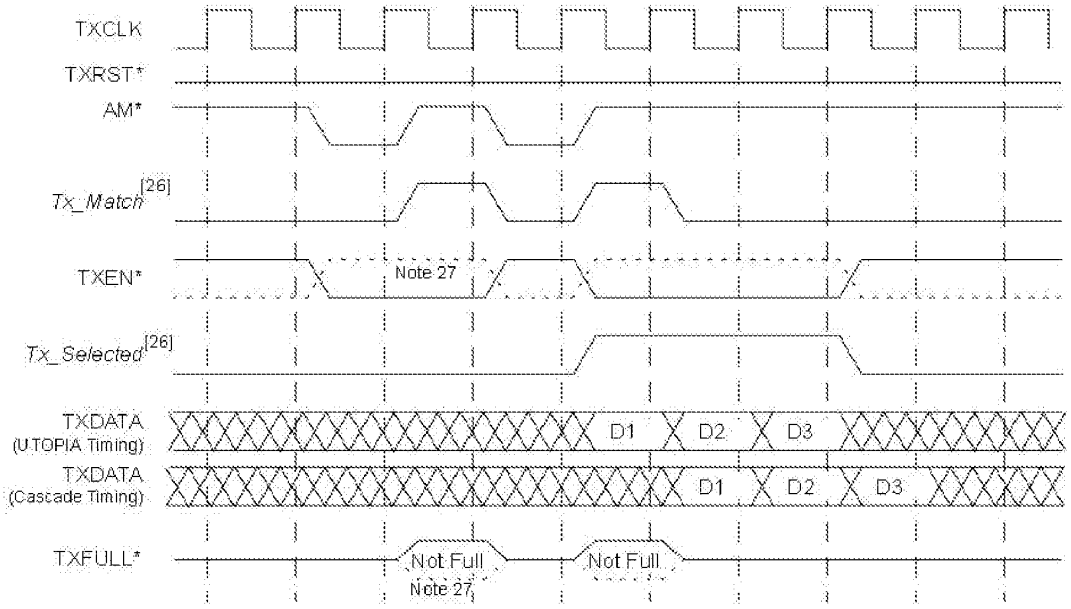
Transmit Data Selection

Asynchronous With UTOPIA Timing and Control (Transmit FIFO Enabled)

When AM* is sampled LOW and TXRST* is sampled HIGH by the rising edge of TXCLK, a Tx_Match condition is generated. This Tx_Match condition continues until AM* is sampled HIGH or TXRST* is sampled LOW at the rising edge of TXCLK. When a Tx_Match (or Tx_RstMatch) condition is present, the TXEMPTY* and TXFULL* output drivers are enabled. When a Tx_Match (or Tx_RstMatch) condition is not present, these same drivers are disabled (High-Z).

The selection state of the Transmit FIFO is entered when a Tx_Match condition is present, and TXEN* transitions from HIGH to LOW. Once selected, the Transmit FIFO remains selected until TXEN* is sampled HIGH by the rising edge of TXCLK. In the selected state, data present on the TXDATA inputs is captured and stored in the Transmit FIFO. This transmit interface selection process is shown in Figure 10. For the first TXEN* assertion, the TX_Match condition is not yet present so the Transmitter is not selected. However, the second TXEN* assertion meets this requirement and the Transmitter selection is successful.

Figure 10. Transmit Selection with Transmit FIFO Enabled



Notes
26. Signals labeled in italics are internal to the CY7C924ADX.
27. Signals shown as dotted lines represent the differences in timing and active state of signals when operated in Cascade Timing.

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Synchronous With UTOPIA Timing and Control (Transmit FIFO Bypassed)

When the Transmit FIFO is bypassed (FIFOBYP* is LOW and not in byte-packed mode), the CY7C924ADX must still be selected to write data into the Transmit Input Register.

Parallel TXDATA is clocked in and transmitted serially when TXEN* is asserted. When TXEN* is deasserted, the TXDATA bus contents are ignored and C5.0 idle characters are sent instead.

AM* must be asserted to enable the TXFIFO flags. When AM* is deasserted, the flags are High-Z.

When AM* is deasserted while TXEN* is enabled, the Transmit TXDATA is still read in and transmitted, but the FIFO flags are no longer enabled.

When data is not written to the Transmit Input Register, the data stream is automatically padded with C5.0 (K28.5) SYNC characters. If the 8B/10B Encoder is enabled, disparity tracking allows the added C5.0 fill characters to follow all 8B/10B encoding rules. If the 8B/10B encoder is bypassed, disparity tracking is disabled, and the transition between externally encoded data and internally generated C5.0 characters may generate a running disparity error at the attached receiver. The same error may occur at the transition between the internal C5.0 characters and the resumption of externally encoded data. When strings of contiguous C5.0 characters are generated, each C5.0 has alternating running disparity with the previous C5.0 character.

Receive Data Selection

Asynchronous With UTOPIA Timing and Control (Receive FIFO Enabled)

When AM* is sampled LOW and RXRST* is sampled HIGH by the rising edge of RXCLK input, an Rx_Match condition is generated. This Rx_Match condition continues until AM* is sampled HIGH or RXRST* is sampled LOW at the rising edge of RXCLK input. When an Rx_Match (or Rx_RstMatch) condition is present, the RXEMPTY* and RXFULL* output drivers are enabled. When an Rx_Match (or Rx_RstMatch) condition is not present, these same drivers are disabled (High-Z).

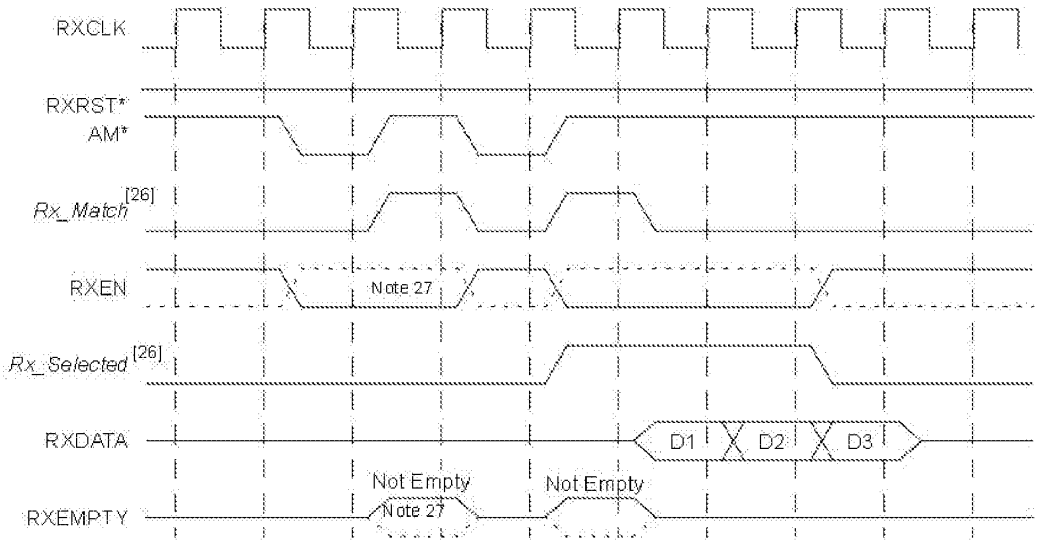
The selection state of the Receive FIFO is entered when an Rx_Match condition is present, and RXEN* transitions from HIGH to LOW. Once selected, the Receive FIFO remains selected until RXEN* is sampled HIGH by the rising edge of RXCLK input. The selected state initiates a read cycle from the Receive FIFO and enables the Receive FIFO data onto the RXDATA bus. This receive interface selection process is shown in Figure 11. For the first RXEN* assertion, the RX_Match condition is not present when RXEN* is asserted so the Receiver is not selected. However, the second RXEN* assertion occurs with an RX_Match condition present and the Receiver selection is successful.

Synchronous With UTOPIA Timing and Control (Receive FIFO Bypassed)

When the Receive FIFO is bypassed (FIFOBYP* is LOW and not in a byte-packed mode), the CY7C924ADX must still be selected to enable the output drivers for the RXDATA bus. With the Receive FIFO bypassed, RXCLK becomes a synchronous output clock operating at the character rate.

The Receive interface is selected when AM* is sampled asserted and RXEN* is asserted at least one cycle later. Once selected, it remains asserted until RXEN* is deasserted, regardless of the state of AM*.

Figure 11. Receive Selection with Receive FIFO Enabled



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If RXEN* is deasserted when AM* is deasserted, AM* must again be sampled LOW followed by RXEN* sampled low at least one cycle later for the Receive interface to again be selected. When the Receive interface is not selected, the RXDATA[11:0] bus is High-Z.

The Receive FIFO flags depend only on the state of AM*. When AM* is asserted, the flags are enabled. When AM* is deasserted, the flags are High-Z.)

Continuous Selection

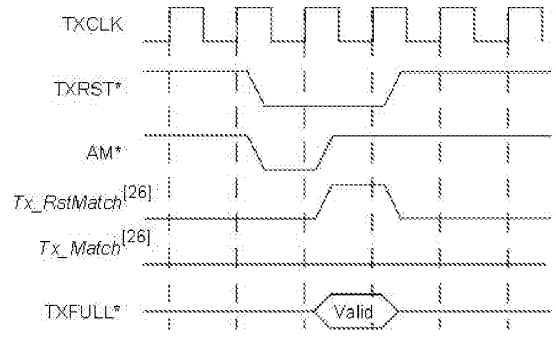
Continuous Selection is a specialized form of selection which does not require sequenced assertion of AM* and TXEN* or RXEN* to select the device for data transfers. In this Continuous Selection mode, the AM* and associated TXEN* or RXEN* enable signal must be asserted when the device is powered up or during assertion of RESET*[1:0]. So long as these signals remain asserted, the device remains selected and data is accepted and presented on every clock cycle.

Note. The use of continuous selection makes it impossible to reset the internal FIFOs, or to access the Serial Address Register.

FIFO Reset Address Match

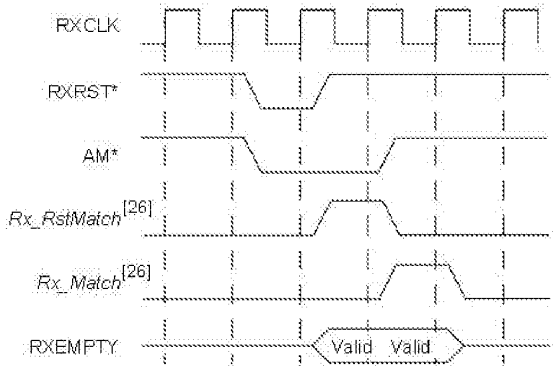
When AM* and TXRST* are both LOW, and this condition is sampled by the rising edge of TXCLK, a Tx_RstMatch condition is generated. This Tx_RstMatch condition continues until AM* or TXRST* is sampled HIGH by the rising edge of TXCLK. When a Tx_RstMatch (or Tx_Match) condition is present, the TXEMPTY* and TXFULL* output drivers are enabled (just as in a normal Tx_Match condition). When AM* is not asserted, these same drivers are disabled (High-Z). The Transmit FIFO reset Address Match is shown in Figure 12. Note that although TXRST* remains LOW for more than one clock cycle, the Tx_RstMatch does not because the AM* signal is no longer asserted (LOW).

Figure 12. Transmit FIFO Reset Address Match



When AM* and RXRST* are both LOW, and this condition is sampled by the rising edge of RXCLK, an Rx_RstMatch condition is generated. This Rx_RstMatch condition continues until AM* or RXRST* is sampled HIGH, at the rising edge of RXCLK. When an Rx_RstMatch (or Rx_Match) condition is present, the RXEMPTY* and RXFULL* output drivers are enabled. When AM* is not asserted these same drivers are disabled (High-Z). The Receive FIFO reset Address Match is shown in Figure 13.

Figure 13. Receive FIFO Reset Address Match



Note that while the FIFO flags remain asserted for more than one clock cycle, this is due to an Rx_Match condition, not a continuation of the Rx_RstMatch.

FIFO Reset Sequence

On power-up, the Transmitter and Receiver FIFOs are cleared automatically. If the usage of the FIFOs in specific operating modes results in stale or unwanted data, this data can be cleared by resetting the respective FIFO. Data in the Transmit FIFO will empty automatically if it is enabled to read the FIFO (assuming TXHALT* is not LOW). Stale received data can be "flushed" by reading it, or the Receive FIFO can be reset to remove the unwanted data.

The Transmit and Receive FIFOs are reset when the Tx_RstMatch or Rx_RstMatch condition remains present for eight consecutive clock cycles. Any disruption of the reset sequence prior to reaching the eight cycle count, either by removal of AM* or the respective TXRST* or RXRST* terminates the sequence and does not reset the FIFO. If the associated TXEN* or RXEN* signals are asserted during the reset, the relevant interface's reset operation is inhibited until the enable signal is deasserted. Because AM* must remain asserted during the reset sequence, the addressed FIFO flags remain driven during the entire sequence.

Transmit FIFO Reset Sequence

The Transmit FIFO reset sequence is started when TXRST* and AM* are first sampled LOW by the rising edge of TXCLK. If TXEN* is asserted (sampled HIGH for UTOPIA timing or LOW for Cascade timing), the reset sequence is inhibited until it is removed.

When a Transmit FIFO reset sequence is enabled and has been active for at least eight TXCLK cycles, a Transmit FIFO reset operation is started. To show this progress, the Transmit FIFO flags are forced to indicate a FULL* condition (TXEMPTY* is deasserted, and both TXHALF* and TXFULL* are asserted).

Note. The FIFO Full state forced by the reset operation is different from a Full state caused by normal FIFO data writes. For normal FIFO write operations, when Full is first asserted, the Transmit FIFO can still accept up to eight additional writes of data. When a Full state is asserted due to a Transmit FIFO reset operation, the FIFO will not accept any additional data.

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This FIFO reset operation is not allowed to progress within the device until the external reset condition is removed. This can occur by deasserting TXRST* or AM*. If AM* is deasserted (HIGH) to remove the reset condition, the Transmit FIFO flag's drivers are disabled, and the Transmit FIFO must be addressed at a later time to validate completion of the Transmit FIFO reset. If TXRST* is deasserted (HIGH) to remove the reset condition, the Tx_RstMatch is changed to a Tx_Match, and the Transmit FIFO status flags remain driven.

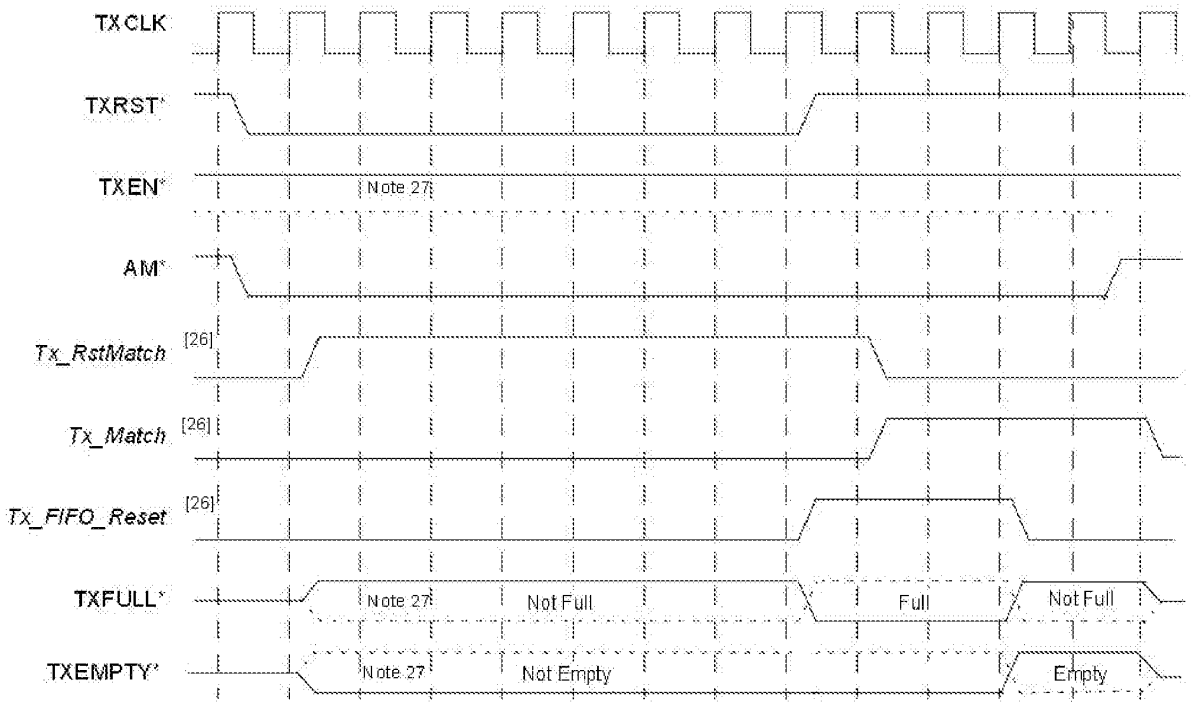
The Transmit FIFO reset operation is complete when the Transmit FIFO flags indicate an Empty state (TXEMPTY* is asserted and both TXHALF* and TXFULL* are deasserted). A valid Transmit FIFO reset sequence is shown in Figure 14. Figure 15 on page 48 shows a sequence of input signals which does not produce a FIFO reset. In this case TXEN* was asserted to select the a Transmit FIFO for data transfers. Because TXEN* remains active, the assertion of AM* and TXRST* does not initiate a reset operation. This is shown by the TXFULL* flag remaining HIGH (deasserted) following what would be the normal expiration of the eight-state reset counter.

Receive FIFO Reset Sequence

The Receive FIFO reset sequence operates similarly to the Transmit FIFO reset sequence. The same requirements exist for the assertion state of RXRST* and selection of the interface through AM*. A sample Receive FIFO reset sequence is shown in Figure 16 on page 48. Upon recognition of a Receive FIFO reset, the Receive FIFO flags are forced to indicate an Empty state to prohibit additional reads from the FIFO. Unlike the Transmit FIFO, where the internal completion of the reset operation is shown by first going Full and later going Empty when the internal reset is complete, there is no secondary indication of the completion of the internal reset of the Receive FIFO. The Receive FIFO is usable as soon as new data is placed into it by the Receive Control State Machine.

When a Receive FIFO reset sequence is enabled and has been active for at least eight RXCLK cycles, a Receive FIFO reset operation is started. This FIFO reset operation is not allowed to progress within the device until the associated RXRST* or AM* signal is sampled deasserted. Following deassertion of RXRST* (which starts the FIFO reset operation), selection of the device for normal data transfers is inhibited during the immediately following RXCLK clock cycle. If a selection of the receive interface is attempted during this immediately following cycle (by asserting RXEN*), the selection is ignored, and the device remains unselected until RXEN* is deasserted, and reasserted in a following RXCLK cycle.

Figure 14. Transmit FIFO Reset Sequence



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Figure 15. Invalid Transmit FIFO Reset Sequence with TXEN* Asserted

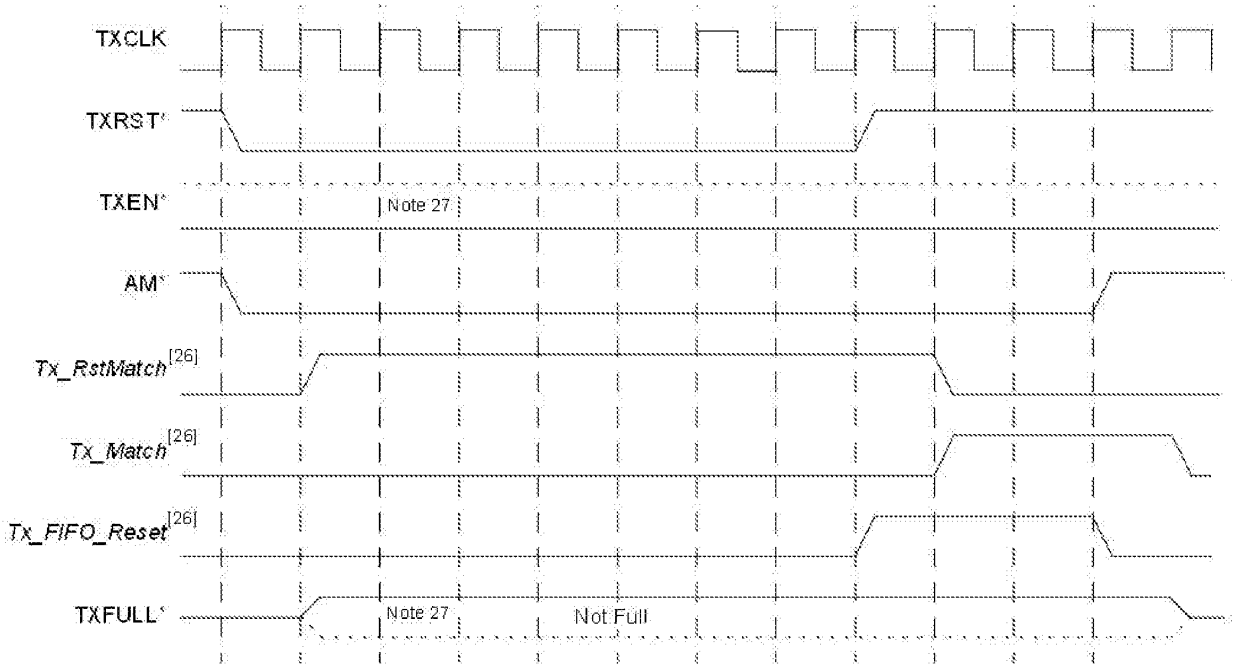
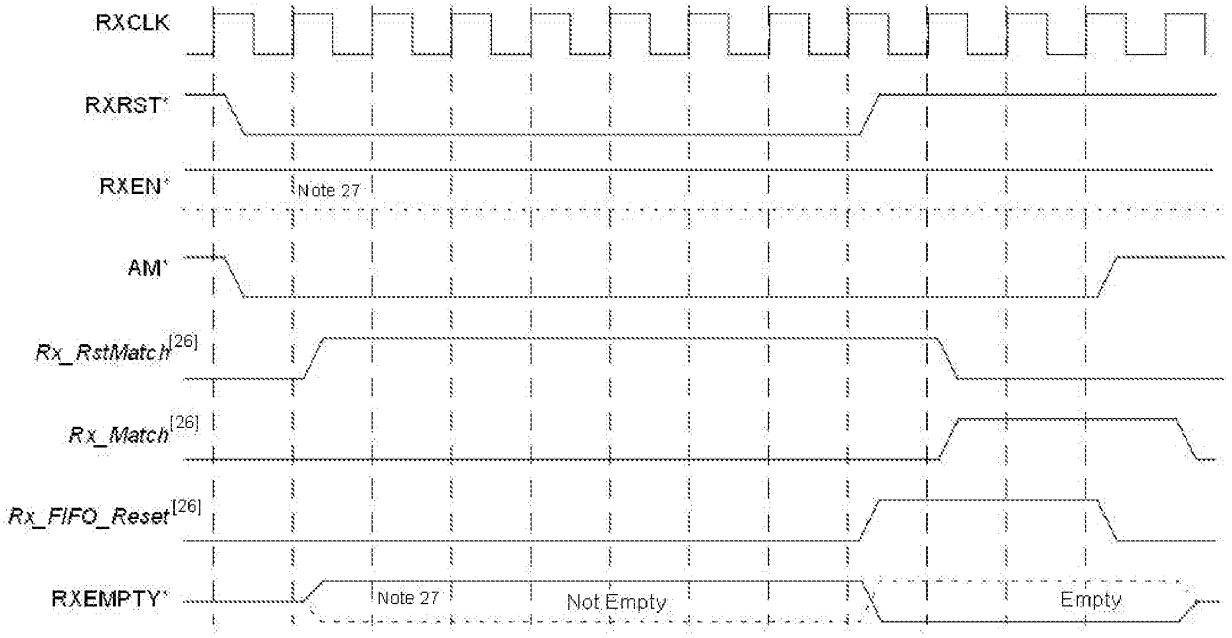


Figure 16. Receive FIFO Reset Sequence



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Serial Address Register Access

The Serial Address Register in the CY7B924ADX is accessed through the RXDATA bus. This Serial Address Register can only be accessed in UTOPIA mode (EXTFIFO = L). This register can be both written and read, and is accessed by asserting RXRST* to address the register in the device instead of the normal Receive FIFO data. Within this alternate address space, the RXRVS signal is an input at all times, and is used to select between read (RXRVS is HIGH) and write (RXRVS is LOW) operations on the Serial Address Register.

The Serial Address Register is the same size as the 8- or 10-bit data width selected by BYTE8/10*. It can be set to match domain or multicast addresses by the level on RXSC/D*. If RXS/D* is LOW when the Serial Address Register is written, it becomes the Multicast address register and declares a match if at least one bit matches the equivalent bit in the incoming Address character. If RXSC/D* is HIGH when the Serial Address Register is written, it becomes the Unicast address register and defines a match only if all of the bits match the incoming Address character.

This register mapping is shown in Figure 6 on page 26.

Accessing Serial Address Register

To access the Serial Address Register in the CY7B924ADX, an Rx_RstMatch condition must first be generated by the combined assertion of AM* and RXRST* and the device must be in UTOPIA timing mode (EXTFIFO = L). RXEN* is then used as the data strobe signal to initiate either a read or write cycle to the RXDATA bus. If RXRVS is HIGH at the time of the RXEN* data strobe, a register read operation takes place. If RXRVS is LOW at the time of the RXEN* data strobe, a register write operation takes place.

The RXSC/D* input is used in conjunction with RXDATA[9:0] or RXDATA[7:0] to select the operational mode of the Serial Address Register (Unicast or Multicast)

Register write and read operations are shown in Figure 17. If the serial address register write and read operations are both performed without deasserting RXRST* for at more than seven cycles, then RXRST* will still not extend to the requirement for a reset and the Receive FIFO will not be reset.

FIFO Reset, Serial Address Register Access and Continuous Selection

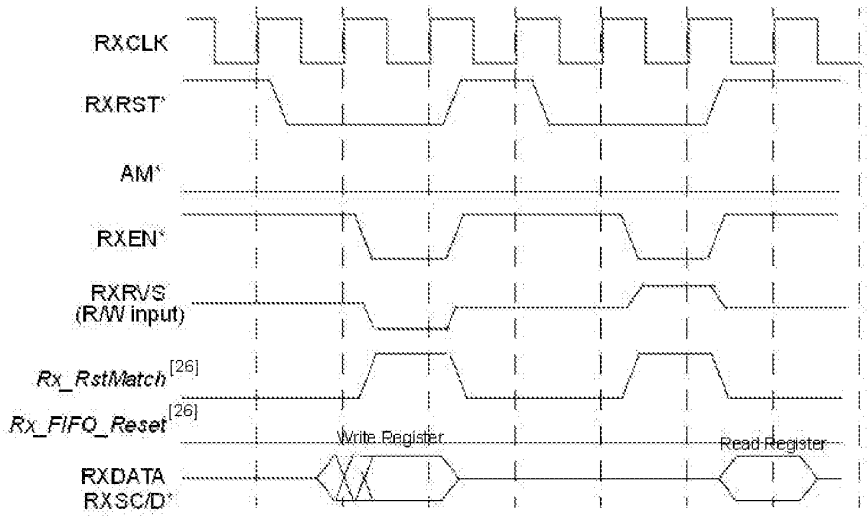
When configured for continuous selection (AM* asserted with TXEN* always enabled, or AM* asserted with RXEN* always enabled), it is not possible to reset the Transmit and Receive FIFOs. It is also not possible to write to the Serial Address Register without deselecting the Receive FIFO interface.

X3.230 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data (Data Characters) are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 8-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary rationale for use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard consist of a distinct and easily recognizable bit pattern (the Special Character Comma) that assists a Receiver in achieving word alignment on the incoming bit stream.

Figure 17. Serial Address Register Access



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Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an 8-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the 8-bit byte for the raw 8-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown here:

```
FC-2 bit designation—76543210
HOTLink TX/RX designation—76543210
8B/10B bit designation—HGFEDCBA
```

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character (using 8B/10B Transmission Code notation):

```
FC-2  45
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation (note carefully that the order of bits is reversed):

```
Data Byte Name    D5.2
                  Bits: ABCDE FGH
                        10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
Bits: abcdeifghj
      1010010101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D, and the SC/D` pin is LOW) or a Special Character (c is set to K, and the SC/D` pin is HIGH). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7).

Note. This definition of the 10-bit Transmission Code is based on (and is in basic agreement with) the following references, which describe the same 10-bit transmission code.

A.X. Widmer and P.A. Franaszek. "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code" *IBM Journal of Research and Development*, 27, No. 5: 440-451 (September, 1983).

U.S. Patent 4,486,739. Peter A. Franaszek and Albert X. Widmer. "Byte-Oriented DC Balanced (0,4) 8B/10B Partitioned Block Transmission Code" (December 4, 1984).

Fibre Channel Physical and Signaling Interface (ANSI X3.230–1994 ANSI FC–PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22–7202).

8B/10B Transmission Code

The following information describes how the tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within the higher-level constructs specified by the standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit "a" is transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order. (Note that bit i is transmitted between bit e and bit f, rather than in alphabetical order.)

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two (not necessarily different) Transmission Characters. The two columns correspond to the current value of the running disparity ("Current RD–" or "Current RD+"). Running disparity is a binary parameter with either the value negative (–) or the value positive (+).

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Transmitter calculates a new value for its running disparity based on the contents of the transmitted character. Special Character codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3.230.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver decides whether the Transmission Character is valid or invalid according to the following rules and tables and calculates a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity are used to calculate the new running-disparity value for Transmission Characters that have been transmitted (Transmitter's running disparity) and that have been received (Receiver's running disparity).

Running disparity for a Transmission Character is calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other

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sub-block. Running disparity at the beginning of the 6-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the 6-bit sub-block if the 6-bit sub-block is 000111, and it is positive at the end of the 4-bit sub-block if the 4-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the 6-bit sub-block if the 6-bit sub-block is 111000, and it is negative at the end of the 4-bit sub-block if the 4-bit sub-block is 1100.
3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate encoding for the Valid Data byte or the Special Character byte into a Transmission Character is listed in the character encoding *Table 11* and *Table 12*. The current value of the Transmitter's running disparity is used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity is calculated. This new value is used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. Table 9 shows naming notations and examples of valid transmission characters.

Table 9. Valid Transmission Characters

Data			
Byte Name	TX_{IN} or RX_{OUT}		Hex Value
	765	43210	
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
. .	. .	. .	. .
D5.2	010	000101	45
. .	. .	. .	. .
D30.7	111	11110	FE
D31.7	111	11111	FF

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity is searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the associated Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's validity, the received Transmission Character is used to calculate a new value of running disparity. The new value is used as the Receiver's current running disparity for the next received Transmission Character.Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. Table 10 shows an example of this behavior.

Table 10. Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

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Table 11. Valid Data Characters (TXSC/D* = LOW, RXSC/D* = LOW)

Data Byte Name	Bits	Current RD-	Current RD+	Data Byte Name	Bits	Current RD-	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011

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Table 11. Valid Data Characters (TXSC/D* = LOW, RXSC/D* = LOW) (continued)

Data Byte Name	Bits HGF EDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010

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Table 11. Valid Data Characters (TXSC/D* = LOW, RXSC/D* = LOW) (continued)

Data Byte Name	Bits HGF EDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000

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Table 11. Valid Data Characters (TXSC/D* = LOW, RXSC/D* = LOW) (continued)

Data Byte Name	Bits HGF EDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD– abcdei fghj	Current RD+ abcdei fghj
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

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Table 12. Valid Special Character Codes and Sequences (TXSC/D[x] = HIGH or RXSC/D[x] = HIGH)[28, 29]

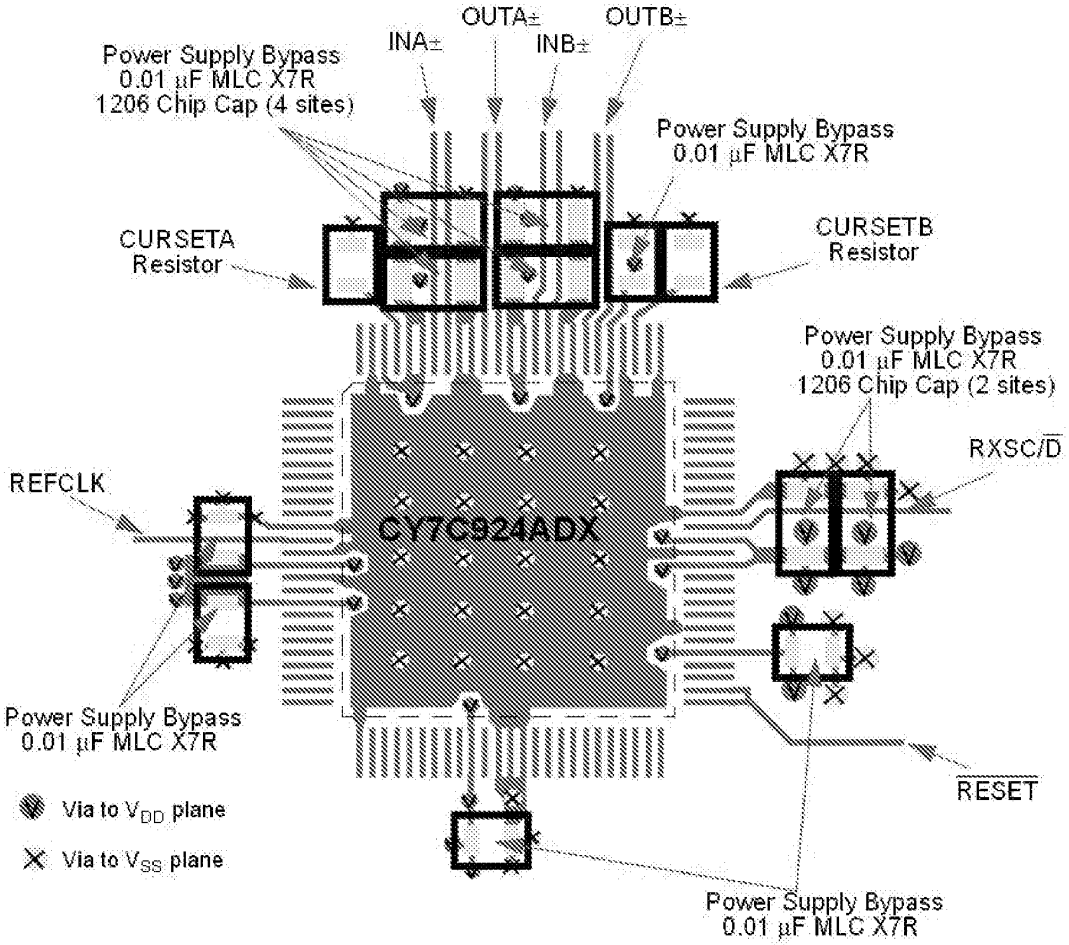
S.C. Byte Name	S.C. Code Name		Bits		Current RD–		Current RD+	
			HGF	EDCBA	abcdei	fghj	abcdei	fghj
K28.0	C0.0[30]	(C00)	000	00000	001111	0100	110000	1011
K28.1	C1.0[31]	(C01)	000	00001	001111	1001	110000	0110
K28.2	C2.0[31]	(C02)	000	00010	001111	0101	110000	1010
K28.3	C3.0[30]	(C03)	000	00011	001111	0011	110000	1100
K28.4	C4.0[31]	(C04)	000	00100	001111	0010	110000	1101
K28.5	C5.0[31, 32]	(C05)	000	00101	001111	1010	110000	0101
K28.6	C6.0[31]	(C06)	000	00110	001111	0110	110000	1001
K28.7	C7.0[31, 33]	(C07)	000	00111	001111	1000	110000	0111
K23.7	C8.0[30]	(C08)	000	01000	111010	1000	000101	0111
K27.7	C9.0[30]	(C09)	000	01001	110110	1000	001001	0111
K29.7	C10.0[30]	(C0A)	000	01010	101110	1000	010001	0111
K30.7	C11.0	(C0B)	000	01011	011110	1000	100001	0111
					End of Frame Sequence			
EOFxx	C2.1[34]	(C22)	001	00010	–K28.5.Dn.xxx0		+K28.5.Dn.xxx1	
					Code Rule Violation and SVS Tx Pattern			
Exception	C0.7[33, 35]	(CE0)	111	00000	100111	1000	011000	0111
–K28.5	C1.7[36]	(CE1)	111	00001	001111	1010	001111	1010
+K28.5	C2.7[37]	(CE2)	111	00010	110000	0101	110000	0101
					Running Disparity Violation Pattern			
Exception	C4.7[38]	(CE4)	111	00100	110111	0101	001000	1010

Notes

28. All codes not shown are reserved.
29. Notation for Special Character Code Name is consistent with Fibre Channel and ESCON naming conventions. Special Character Code Name is intended to describe binary information present on I/O pins. Common usage for the name can either be in the form used for describing Data patterns (i.e., C0.0 through C31.7), or in hex notation (i.e., Cnn where nn = the specified value between 00h and FFh).
30. These characters have reserved meanings when command processing is enabled. This includes all operating modes where the FIFOs are enabled and the discard policy is not 0.
31. These characters are used for control of ESCON interfaces. They can be sent as embedded commands or other markers when not operating using ESCON protocols.
32. The K28.5 character is used for framing operations by the receiver. It is also the pad or fill character transmitted to maintain the serial link when no user data is available.
33. Care must be taken when using this Special Character code. When a C7.0 or C0.7 is followed by a D11.x or D20.x, an alias K28.5 sync character is created. These sequences can cause erroneous framing and should be avoided while RFEN is HIGH.
34. C2.1 = Transmit either –K28.5+ or +K28.5– as determined by Current RD and modify the following Transmission Character by setting its least significant bit to 1 or 0. If Current RD at the start of the following character is plus (+) the LSB is set to 0, and if Current RD is minus (–) the LSB becomes 1. This modification allows construction of X3.230:1994 "EOF" frame delimiters wherein the second data byte is determined by the Current RD.
For example, to send "EOFdt" the controller could issue the sequence C2.1–D21.4– D21.4–D21.4, and the HOTLink Transmitter will send either K28.5–D21.4–D21.4–D21.4 or K28.5–D21.5– D21.4–D21.4 based on Current RD. Likewise to send "EOFdti" the controller could issue the sequence C2.1–D10.4–D21.4–D21.4, and the HOTLink Transmitter will send either K28.5–D10.4–D21.4– D21.4 or K28.5–D10.5–D21.4– D21.4 based on Current RD. The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.
35. C0.7 = Transmit a deliberate code rule violation. The code chosen for this function follows the normal Running Disparity rules. Transmission of this Special Character has the same effect as asserting TXSVS = HIGH. The receiver outputs this Special Character only if the Transmission Character being decoded is not found in the tables.
36. C1.7 = Transmit Negative K28.5 (–K28.5+) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C1.7 if –K28.5 is received with RD+, otherwise K28.5 is decoded as C5.0 or C2.7.
37. C2.7 = Transmit Positive K28.5 (+K28.5–) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C2.7 if +K28.5 is received with RD–, otherwise K28.5 is decoded as C5.0 or C1.7.
38. C4.7 = Transmit a deliberate code rule violation to indicate a Running Disparity violation. The receiver will only output this Special Character if the Transmission Character being decoded is found in the tables, but Running Disparity does not match. This may indicate that an error occurred in a prior byte.

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Printed Circuit Board Layout Suggestions



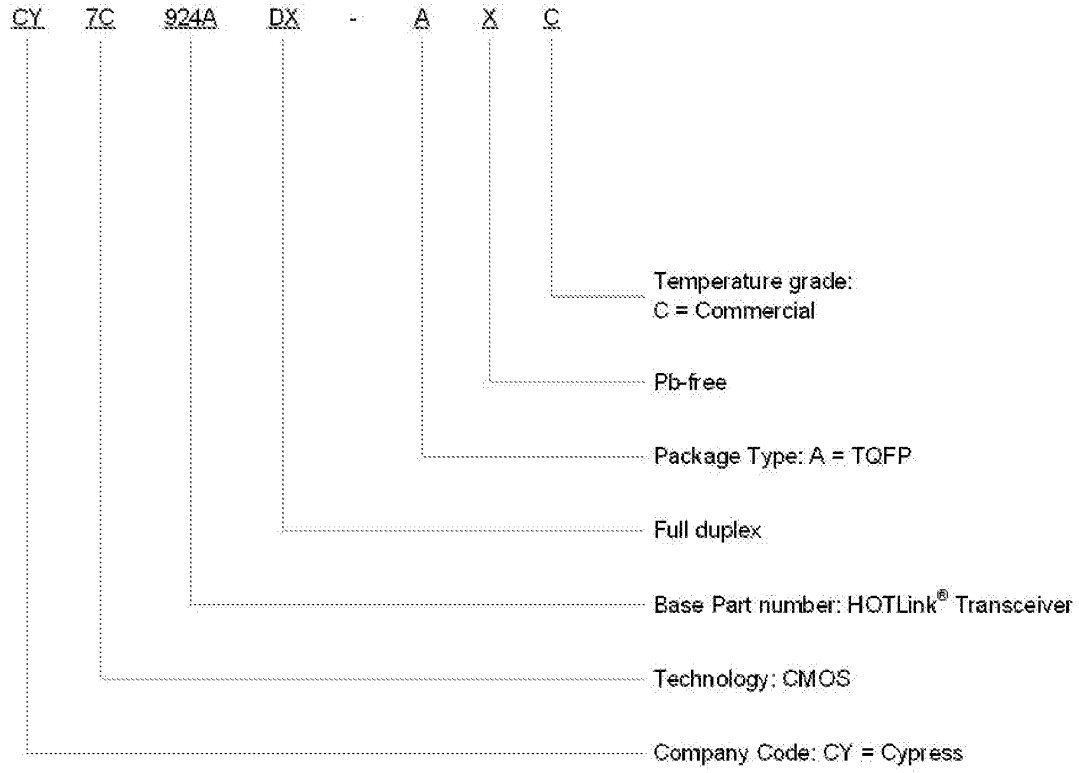
This is a typical printed circuit board layout showing example placement of power supply bypass components and other components mounted on the same side as the CY7C924ADX. Other layouts, including cases with components mounted on the reverse side would work as well.

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Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7C924ADX-AXC	A100	100-pin thin quad flat pack - Pb-free	Commercial

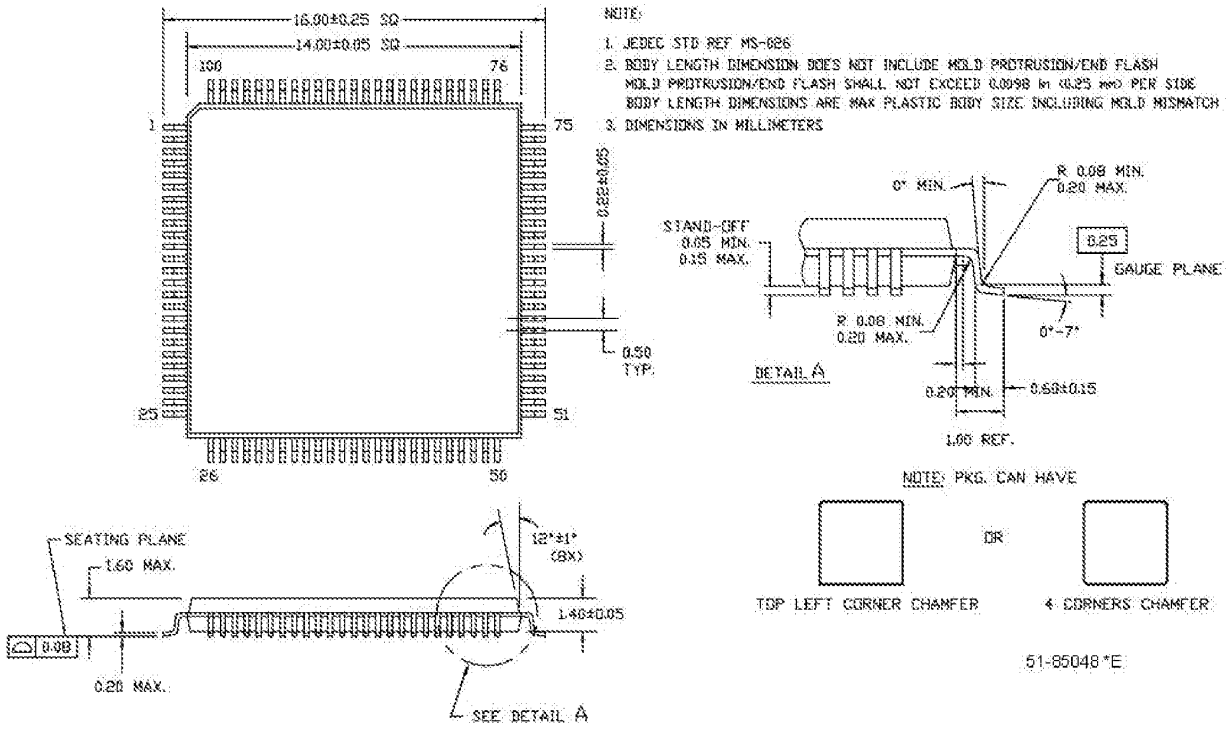
Ordering Code Definitions



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Package Diagram

Figure 18. 100-Pin Thin Plastic Quad Flat Pack (TQFP) A100SA



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Acronyms

The following table lists the acronyms that are used in this document.

Table 13. Acronyms Used in this Datasheet

Acronym	Description
BGA	ball grid array
BIST	built-in self test
I/O	input/output
JTAG	joint test action group
PLL	phase-locked loop
TMS	test mode select
TDO	test data out
TDI	test data in

Document Conventions

Table 14. Units of Measure

Acronym	Description
°C	degree Celsius
kΩ	Kilo ohm
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
Ω	ohm
pF	picofarad
V	volt
W	watt

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Document History Page

Document Title: CY7C924ADX 200 MBaud HOTLink® Transceiver Document Number: 38-02008				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	105846	SZV	03/26/01	Change from Spec number: 38-00770 to 38-02008
*A	107878	KET	07/09/01	Changed part number: CY7C924DX to CY7C924ADX
*B	118320	REV	11/13/02	Changed the mentioning of PECL inputs and outputs to PECL-compatible inputs and outputs, which is more correct. Changed the font and centered the part number in the device footprint Fixed the line wrap issue with DLB[1] and DLB[0] Changed labels on waveforms to make them more consistent with those in the tables Changed the I/O labels on the D-type flip flop Changed mentioning of PAREN to TXPAREN to make data sheet more consistent
*C	123796	KKV	01/29/03	Replaced incorrect source copy with correct source copy
*D	201401	TNT	01/19/04	Removed parity Changed device selection requirements when in FIFO Bypass mode Added comprehensive table showing SPDSEL/RANGESEL and data rate mapping Cascade mode read timing description changed, receive timing diagram updated to reflect operation Serial Address Register access listed as an option for UTOPIA mode only Changed FIFO reset condition to show that the count in suspended, not reset, when TXEN* is asserted
*E	988901	UKK	See ECN	Added Lead-free option package and removed Leaded package in ordering information
*F	2894000	CGX	03/17/10	Updated template. Added Table of Contents Removed pruned part CY7C924ADX-AI and added part CY7C924ADX-AXI Updated package diagram
*G	3334849	SAAC	08/02/11	Updated template according to current Cypress standards. Added ordering code definitions, acronyms, and units of measure.

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Cypress Semiconductor
3901 North First Street

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2K x 8 Dual-Port Static RAM

Features

- 0.8-micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C132/CY7C136 easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146
- BUSY output flag on CY7C132/CY7C136; BUSY input on CY7C142/CY7C146
- INT flag for port-to-port communication (52-pin LCC/PLCC/PQFP versions)

Functional Description

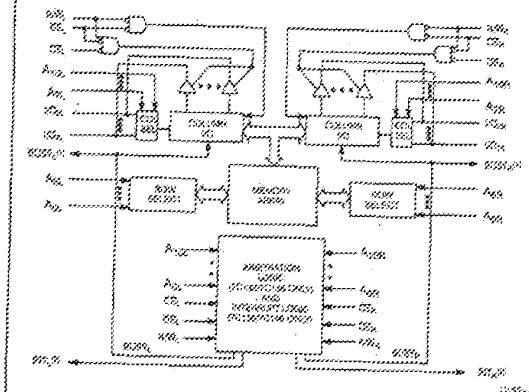
The CY7C132/CY7C136/CY7C142 and CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMS. Two ports are provided to permit independent access to any location in memory. The CY7C132/CY7C136 can be utilized as either a stand-alone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins: chip enable ($\overline{CE}$), write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). BUSY flags are provided on each port. In addition, an interrupt flag ($\overline{INT}$) is provided on each port of the 52-pin LCC and PLCC versions. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. On the LCC/PLCC versions, $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

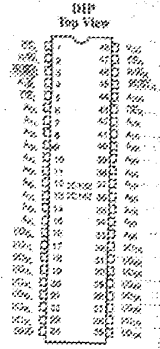
An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C132/CY7C142 are available in both 48-pin DIP and 52-pin LCC. The CY7C136/CY7C146 are available in 52-pin LCC, PLCC, and PQFP.

Logic Block Diagram

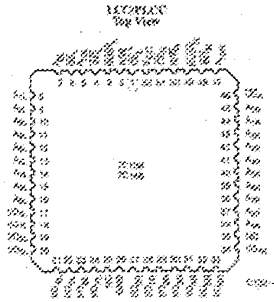


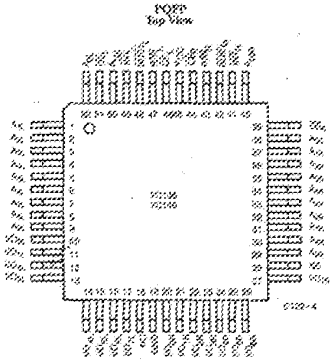
Pin Configuration



Notes:
1. CY7C132/CY7C136 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor.
   CY7C142/CY7C146 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs; pull-up resistor required.

Pin Configurations (continued)





Selection Guide

		7C132–25[1] 7C136–25 7C142–25 7C146–25	7C132–30 7C136–30 7C142–30 7C146–30	7C132–35 7C136–35 7C142–35 7C146–35	7C132–45 7C136–45 7C142–45 7C146–45	7C132–55 7C136–55 7C142–55 7C146–55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Commercial	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Commercial	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[3]	−55°C to +125°C	5V ± 10%

Notes:
3. "Z" version available in PQFP and PLCC packages only.
4. T_A is the "instant on" case temperature.

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Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C132–25, 30[3] 7C136–25, 30 7C142–25, 30 7C146–25, 30		7C132–35 7C136–35 7C142–35 7C146–35		7C132–45, 55 7C136–45, 55 7C142–45, 55 7C146–45, 55		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[6]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[8]	Com'l		170		120		90	mA
			Mil				170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		65		45		35	mA
			Mil				65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		115		90		75	mA
			Mil				115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		105		85		70	mA
			Mil				105		85	

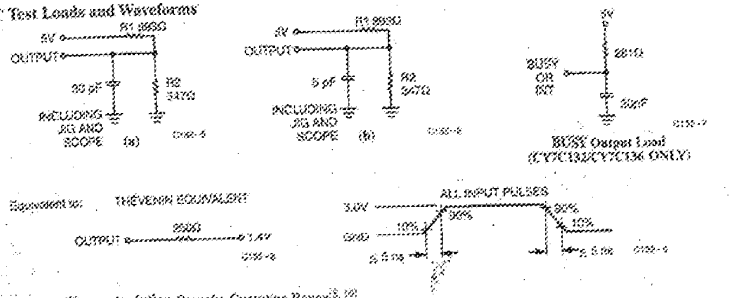
Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

5. See the last page of this specification for Group A subgroup testing information.
6. BUSY and INT pins only.
7. Duration of the short circuit should not exceed 30 seconds.
8. At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC test waveforms input levels of GND to 3V.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
11. AC test conditions use V_{TH} = 1.5V and V_{TL} = 1.4V.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
13. t_{HZCE}, t_{HZWE}, t_{HZOE}, t_{LZCE}, t_{LZWE}, and t_{LZOE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
14. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[5, 10]

Parameter	Description	7C132–25[3] 7C136–25 7C142–25 7C146–25		7C132–30 7C136–30 7C142–30 7C146–30		7C132–35 7C136–35 7C142–35 7C146–35		7C132–45 7C136–45 7C142–45 7C146–45		7C132–55 7C136–55 7C142–55 7C146–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid[11]		25		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[11]		25		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[11]		15		20		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[12]	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[12]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE[14]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	15		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		15		15		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	0		0		0		0		0		ns

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Switching Characteristics (Over the Operating Range[5, 16] (continued))

Parameter	Description	CY7C132–35 CY7C134–35 CY7C142–35 CY7C146–35 Min.	Max.	CY7C132–30 CY7C134–30 CY7C142–30 CY7C146–30 Min.	Max.	CY7C132–55 CY7C134–55 CY7C142–55 CY7C146–55 Min.	Max.	CY7C132–55 CY7C134–55 CY7C142–55 CY7C146–55 Min.	Max.	Unit
BUSY/INTERRUPT TIMING										
t_{BLA}	BUSY LOW from Address Match		20		25		25		30	ns
t_{BHA}	BUSY HIGH from Address Mismatch		20		25		25		30	ns
t_{BLC}	BUSY LOW from CE LOW		20		25		25		30	ns
t_{BHC}	BUSY HIGH from CE HIGH		20		25		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		ns
t_{WB}	R/W LOW after BUSY LOW	0		0		0		5		ns
t_{WH}	R/W HIGH after BUSY HIGH	20		20		25		35		ns
t_{BDD}	BUSY HIGH to Valid Data		35		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17	ns
t_{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING[18]										
t_{WINS}	R/W to INTERRUPT Set Time	25		25		35		35		ns
t_{EINS}	CE to INTERRUPT Set Time	25		25		35		35		ns
t_{INS}	Address to INTERRUPT Set Time	25		25		35		45		ns
t_{OINR}	OE to INTERRUPT Reset Time[19]		25		25		35		45	ns
t_{EINR}	CE to INTERRUPT Reset Time[19]		25		25		35		45	ns
t_{INR}	Address to INTERRUPT Reset Time[19]		25		25		35		45	ns

Notes:
15. These parameters are measured from the input signal changing until the output pin goes to a high-impedance state.
16. CY7C142/CY7C146 only.
17. Address propagation to Port A (Slave Port A accessing semaphore location on Port B) requires unobstructed path; see worst-case allowance in the following:
    A. BUSY on Port B goes HIGH.
    B. Port B address toggled.
    C. CE to Port B toggled.
    D. R/W to Port B toggled during valid read.
18. Guaranteed by t_{BLA} minimum.
19. R/W is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. If $\overline{OE}$ is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WDD} + t_{DH}). If $\overline{OE}$ is HIGH during a R/W controlled write cycle, the output will remain in a high-impedance state. For the shortest possible write pulse width, the user must minimize the sum of t_{WDD} + t_{DH}.
23. If $\overline{CE}$ is LOW during a R/W controlled write cycle, the output will remain in a high-impedance state.

Switching Waveforms

Read Cycle No. 1 (Either Port—Address Access)[16, 20]

Switching Waveforms (continued)

Read Cycle No. 2 (Either Port—$\overline{CE}$/$\overline{OE}$ Access)[16, 21]

Read Cycle No. 3 (Either Port—$\overline{CE}$/$\overline{OE}$ Access)[16, 21]

Read Cycle No. 3 Read with BUSY Master: CY7C132 and CY7C146)

Write Cycle No. 1 ($\overline{OE}$ Three-States Data I/Os — Either Port)[16, 22]

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CY7C132/CY7C136
CY7C142/CY7C146

CYPRESS

Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:

Right Address Valid First:

Busy Timing Diagram No. 3 (Write with BUSY, Slave: CY7C142/CY7C146)

Busy Timing Diagram No. 4 (CE Arbitration)

CE, Valid First:

CE, Valid First:

Write Cycle No. 2 (R/W Three-States Data I/Os — Either Port)[14, 15]

ADDRESS

CE

R/W

DATA

DOUT

DATA VALID

HIGH IMPEDANCE

ADDRESS MATCH

ADDRESS MISMATCH

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Interrupt Timing Diagrams[15]

Left Side Sets $\overline{INT}_R$

Right Side Clears $\overline{INT}_R$

Right Side Sets $\overline{INT}_L$

Left Side Clears $\overline{INT}_L$

Typical DC and AC Characteristics

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Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C132–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C132–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C132–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C132–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C136–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–25RC	R52	52-Pin Plastic Quad Flatpack	
30	CY7C136–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–30RC	R52	52-Pin Plastic Quad Flatpack	
	CY7C136–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C136–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–35RC	R52	52-Pin Plastic Quad Flatpack	
	CY7C136–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C136–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–45RC	R52	52-Pin Plastic Quad Flatpack	
	CY7C136–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C136–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–55RC	R52	52-Pin Plastic Quad Flatpack	
	CY7C136–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–55LMB	L69	52-Square Leadless Chip Carrier	Military

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C142–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C142–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C142–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C142–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C146–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–25RC	R52	52-Pin Plastic Quad Flatpack	
30	CY7C146–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–30RC	R52	52-Pin Plastic Quad Flatpack	
	CY7C146–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C146–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–35RC	R52	52-Pin Plastic Quad Flatpack	
	CY7C146–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C146–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–45RC	R52	52-Pin Plastic Quad Flatpack	
	CY7C146–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–45LMB	L69	52-Square Leadless Chip Carrier	Military

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MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{RCOM}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11
BUSY TIMING	
t_{BAA}	7, 8, 9, 10, 11
t_{BDA}	7, 8, 9, 10, 11
t_{BAC}	7, 8, 9, 10, 11

Note:
1. CY7C142/CY7C146 only.

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CYPRESS

PRELIMINARY

CY7C143

2K x 16 Dual-Port Static RAM

Features

- 0.65-micron CMOS for optimum speed/power
- High speed access: 35 ns
- Low operating power
  - I_{CC} = 170 mA (typ.)
- Automatic power-down
- TTL compatible
- Fully asynchronous operation
- Master CY7C133 easily expands data bus width to 32 or more bits using slave CY7C143
- BUSY output flag on CY7C133; BUSY input on CY7C143
- Available in 68-pin PLCC
- Pin compatible and functionally equivalent to IDT7133 and IDT7143

Functional Description

The CY7C133 and CY7C143 are high-speed CMOS 2K by 16 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C133 can be utilized as either a standalone 16-bit dual-port static RAM or as a master dual-port RAM in connection with the CY7C143 slave dual-port device in systems requiring 32-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins: chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). BUSY signals that the port is trying to access the same location currently being accessed by the other port. An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C133 and CY7C143 are available in 68-pin PLCC.

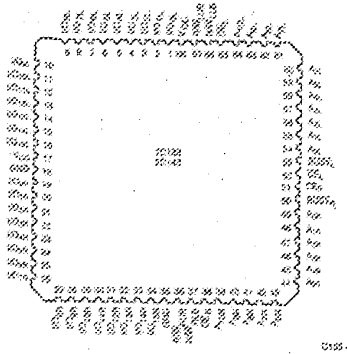
Logic Block Diagram

Note:
1. CY7C133 (Master): BUSY is open drain output and requires pull-up resistor. CY7C143 (Slave): BUSY is input.

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Pin Configuration

68-Pin LCC/PLCC
Top View



0105-2

Selection Guide

	7C133–25 7C143–25	7C133–35 7C143–35	7C133–55 7C143–55
Maximum Access Time (ns)	25	35[2]	55
Typical Operating Current I_{CC} (mA)	170	160	150
Typical Standby Current for I_{SB1} (mA)	40	30	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C133–25 7C143–25 Min.	Typ.	Max.	7C133–35 7C143–35 Min.	Typ.	Max.	7C133–55 7C143–55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA				0.4			0.4			0.4	V
		I_{OL} = 16.0 mA[4]				0.5			0.5			0.5	
V_{IH}	Input HIGH Voltage			2.2			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−5		+5	−5		+5	−5		+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5		+5	−5		+5	−5		+5	μA
I_{OS}	Output Short Circuit Current[5, 6]	V_{CC} = Max., V_{OUT} = GND				−200			−200			−200	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, $f = f_{MAX}$[6]	Com'l		170	250		160	230		150	220	mA
			Ind		170	300		160	260		150	250	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, $f = f_{MAX}$[6]	Com'l		40	60		30	50		20	30	mA
			Ind		40	75		30	65		20	55	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, $f = f_{MAX}$[6]	Com'l		100	140		85	125		75	110	mA
			Ind		100	160		85	140		75	125	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		3	15		3	15		3	15	mA
			Ind		3	15		3	15		3	15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≤ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, $f = f_{MAX}$[6]	Com'l		90	120		80	105		70	90	mA
			Ind		90	140		80	120		70	105	

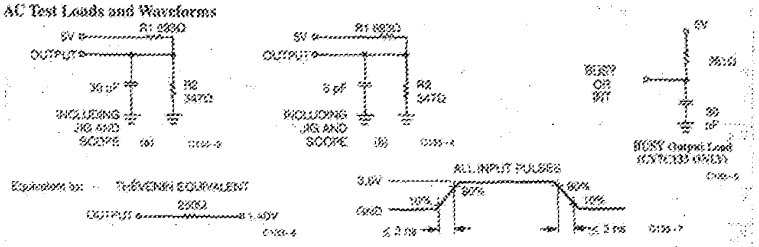
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. 8/88 pin only.
4. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{RC} and using AC Test Waveforms input levels of GND to 3V.

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AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[11]

Parameter	Description	7C133–25 7C143–25 Min.	Max.	7C133–35 7C143–35 Min.	Max.	7C133–55 7C143–55 Min.	Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		55		ns
t_{AA}	Address to Data Valid[12]		25		35		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	CE LOW to Data Valid[13]		25		35		55	ns
t_{DOE}	OE LOW to Data Valid[14]		20		25		30	ns
t_{LZOE}	OE LOW to Low Z[15, 16]	3		3		3		ns
t_{HZOE}	OE HIGH to High Z[15, 16]		15		20		25	ns
t_{LZCE}	CE LOW to Low Z[15, 16]	3		5		5		ns
t_{HZCE}	CE HIGH to High Z[15, 16]		15		20		20	ns
t_{PU}	CE LOW to Power-Up	0		0		0		ns
t_{PD}	CE HIGH to Power-Down		25		25		25	ns
WRITE CYCLE[17]								
t_{WC}	Write Cycle Time	25		35		55		ns
t_{SCE}	CE LOW to Write End	20		25		40		ns
t_{AW}	Address Set-Up to Write End	20		25		40		ns[17]
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	R/W Pulse Width	20		25		35		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/W LOW to High Z[15, 16]		15		20		20	ns
t_{LZWE}	R/W HIGH to Low Z[15, 16]	0		0		0		ns

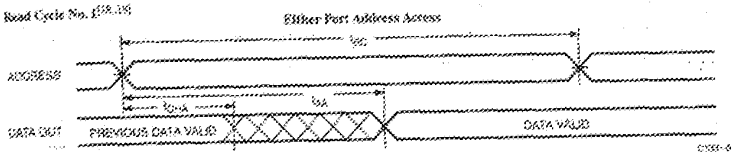
Notes:
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. t_{LZCE}, t_{LZWE}, t_{LZOE}, t_{PU}, t_{HZCE}, t_{HZWE}, and t_{HZOE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
11. The internal write time of the memory is defined by the overlap of CE LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[11] (continued)

Parameter	Description	7C133–25 7C143–25 Min.	Max.	7C133–35 7C143–35 Min.	Max.	7C133–55 7C143–55 Min.	Max.	Unit
BUSY/INTERRUPT TIMING (For Master CY7C133)								
t_{BLA}	BUSY Low from Address Match		25		35		50	ns
t_{BHA}	BUSY High from Address Mismatch		20		30		40	ns
t_{BLC}	BUSY Low from CE Low		20		25		35	ns
t_{BHC}	BUSY High from CE High		20		20		30	ns
t_{PWD}	Write Pulse to Data Delay[18]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[19]		35		45		55	ns
t_{WDD}	BUSY High to Valid Data[20]		Note 13		Note 13		Note 13	ns
t_{APS}	Arbitration Priority Set Up Time[21]	5		5		5		ns
t_{BDD}	BUSY TIMING (For Slave CY7C143)		45		45			ns
t_{WB}	Write to BUSY[22]	0		0		0		ns
t_{WH}	Write Hold After BUSY[22]	20		25		30		ns
t_{PWD}	Write Pulse to Data Delay[18]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[19]		35		45		55	ns

Switching Waveforms

Read Cycle No. 1[18, 19]



Notes:
12. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with BUSY, Master: CY7C133."
13. t_{ACE} is a calculated parameter and is greater of t_{RC} or t_{AA} (worst case) or t_{PU} + t_{PD} (worst case).
14. To ensure that the earlier of the two port writes.
15. To ensure that write cycle is inhibited during contention.
16. To ensure that a write cycle is completed after contention.
17. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveforms of "Read with Port-to-port Delay."
18. R/W is HIGH for read cycle.
19. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.

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CYPRESS

CY7C143

Switching Waveforms (continued)

Read Cycle No. 3 (Either Port CE/OE Access)

Read Cycle No. 4 (BUSY Read with BUSY, Master: CY7C130)

Notes

20. Address valid prior to or coincident with CE transition LOW.

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CYPRESS

CY7C143

Switching Waveforms (continued)

Timing Waveform of Read with Port-to-port Delay No. 4 (For Slave CY7C143)[19, 21, 22]

Write Cycle No.1 (OE Three-States Data I/Os — Either Port)[23, 24]

Notes

21. Setup and hold timing referenced to rising edge of R/W.

22. To access RAM, CE = L and SEM = H. To access semaphore, CE = H and SEM = L. Either condition must be valid for entire tEW time.

23. R/W must be HIGH during all address transitions.

24. A write occurs during the overlap (tEW or tWP) of a LOW CE and a LOW R/W for memory, and a LOW SEM and a LOW R/W for semaphores. Requirements for tWP and tDW must be met for either condition. Both signals must be HIGH to initiate a write cycle.

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6

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Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:

ADDRESS MISMATCH

ADDRESS MATCH

Right Address Valid First:

ADDRESS MISMATCH

ADDRESS MATCH

Busy Timing Diagram No. 3

Write with BUSY (Slave CY7C143)

Switching Waveforms (continued)

Write Cycle No. 2 (R/W Three-States Data I/Os — Either Port)[20, 21]

Either Port

DATA VALID

HIGH IMPEDANCE

Busy Timing Diagram No. 1 (CE Arbitration)

CE_R Valid First:

ADDRESS MATCH

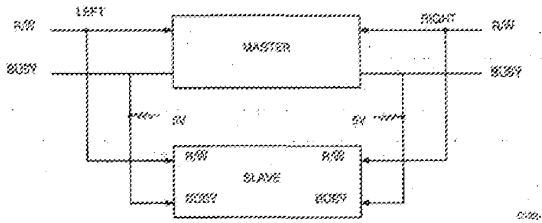
CE_L Valid First:

ADDRESS MATCH

Note

21. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.

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Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C132–25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C132–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C132–35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C132–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C132–55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C132–55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C143–25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C143–35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C143–55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143–55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{ADE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WBUS}	7, 8, 9, 10, 11
t_{WDDS}	7, 8, 9, 10, 11
t_{WPS}	7, 8, 9, 10, 11
t_{OBDS}	7, 8, 9, 10, 11
t_{BDDS}	7, 8, 9, 10, 11
t_{WDS}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[28]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
28. CY7C146 only.

Document #: 38-00414

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A Novel Integration Technology of EEPROM Embedded CMOS LOGIC VLSI Suitable for ASIC Applications

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Abstract

A novel process technology has been developed to fabricate an EEPROM embedded CMOS VLSI. The new technique utilizing a single poly-Si EEPROM cell reduces process steps by 25% as compared with the conventional double poly-Si EEPROM cell. The EEPROM-embedded CMOS LOGIC LSI can be shrunk over future technology generations by introducing three kinds of gate oxide thickness. A widely operating voltage ranging from 1.5 V to 6.0 V and a stand-by current below 100 nA have been achieved.

Introduction

Recently, in an era of SYSTEM ON CHIP, the demand for embedding EEPROM in a large scale CMOS LOGIC has been increasing for a data memories on one chip, especially for installing a security system on a chip, even when the bit size is small. It has been reported that EEPROM and CMOS LOGIC can be put on one chip[1].

Figure 1 shows the comparison of characteristics for important key factors in an ASIC between pure CMOS and conventional EEPROM. A conventional EEPROM has an advantage of high functionality(ZERO turn-around-time and 10^6 program cycles), compared with a pure CMOS. However, it has a disadvantage in its process sequence, operating voltage, and power consumption, compared with a CMOS. Target characteristics are required. The conventional EEPROM cell has a double poly-Si structure and requires a long process sequence. Therefore, a simple structure and a simple process sequence are required. Technologies for low voltage operation and low power consumption are indispensable for future ASIC applications. A low voltage operation is required for the trend of reducing the supply voltage. A low power is required for systems with battery back-up. A new cell technique with a single poly-Si EEPROM[2] embedded CMOS process and circuit technology has been developed. It is easy to apply it to future generation logic.

In this paper, the process, device technologies, and LSI characteristics are described.

Fabrication process

Figure 2 shows a cross-sectional view of the new single poly-Si EEPROM cell and CMOS. The cell has three types of MOSFETs with different gate oxide thicknesses. The tunnel oxide thickness, coupling capacitor thickness, and high voltage gate oxide thickness are 9 nm, 15 nm, and 40 nm, respectively. The CMOS has a twin-well and the logic gate oxide thickness is 15 nm. The new cell requires a large control gate area in order to gain a high coupling ratio. Therefore, this cell size is approximately 2.5 times larger than the double poly-Si cell size. In general, the chip cost of a memory LSI is proportional to the cell size. However, an EEPROM embedded CMOS LSI does not have a proportional relationship when considering both the process complexity and the area ratio of EEPROM to CMOS. From the view-points of chip cost and bit capacity, a single poly-Si EEPROM cell with a bit capacity of less than a certain value, has an advantage to a double poly-Si EEPROM cell. Both single poly-Si EEPROM and double poly-Si EEPROM line up on the 1.0 um rule.

Figure 3 shows the process flow up to gate formation. The EEPROM channel and N- implantations are carried out after field oxidation. First, gate oxide is grown, CMOS channel implantation is carried out, and then, the oxide at the logic region and the coupling capacitor region are removed using a masking step, and the second gate oxide is grown. Next, the tunnel window region is opened using a masking step, and the tunnel oxide is grown. Finally, poly-silicon is deposited. The logic gate oxide thickness can be easily shrunk through this process, taking the capability for coming generations into account, because this oxide can be controlled flexibly, using this 2-step oxidation technique (second gate oxidation and tunnel oxidation). These insulators consist of only oxides. They don't require complex insulating film formation like an ONO (oxide-nitride-oxide). Therefore, this process can be used in a CMOS logic fabrication line.

Figure 4 shows the reliability data for the 2-step gate oxide and conventional CMOS gate oxide. It has been verified by TDDB measurement that both have the same reliability.

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Device characteristics

A new cell layout and cross-sectional view are shown in Fig.5. The cell consists of 2 transistors. The cell is fundamentally the same as that for FLOTOX. The control gate is formed with an N+ diffused layer under the floating gate. The N+ diffused layer(control gate, source, and drain of the select-transistor) is formed with only one implantation by using a one masking step. Therefore, select-transistor is not a self-aligned structure. This is the most effective in a long process sequence to reduce the process step. Figure 6 shows the erase, write, and read mode bias set ups for the new cell, compared with those for the conventional cell. The erase and write operating biases are the same conditions. The read line in the new cell is precharged by the Vcc level. An inverter sense amplifier is used to achieve low voltage and low power consumption[3].

Figure 7 shows the cell characteristics of erase, write, and read operations, compared with Toshiba's double poly-Si EEPROM cell. After being erased, the threshold voltage, Vth, of a single poly-Si cell is lower than that of a double poly-Si cell, because the surface of the control gate is in an inverse state and the depletion layer voltage drops when the control gate of the single poly-Si cell is positively biased. The Icell has compatible characteristics between a single poly-Si cell and a double poly-Si cell even when different reading methods(source read mode and drain read mode) are used. It has been certified that a single poly-Si cell has the same coupling ratio as a double poly-Si cell.

The device characteristics on a 1.0 um EEPROM embedded CMOS and the pure CMOS process show in Table 1. Both processes have achieved the same performance. Therefore, EEPROM and CMOS logic VLSIs designed on Toshiba's CUR [4] can be on one chip.

LSI performances

Table 2 lists the chip features. A test chip can operate over a wide range of supply voltage, 1.5 V~ 6.0 V and consume only 300 uA at 4 MHz. This low operating voltage down to 1.5 V has not been achieved before (even for an external Vpp). Furthermore, its stand-by current is extremely low, below 100 nA.

A wide operating voltage for the test chip has been verified with a schmoo plot, as shown in Fig.8.

Figure 9 shows a test chip photograph. A 64 byte EEPROM core has been designed, using 1.0 um single poly-Si EEPROM embedded CMOS technology. The 64 byte EEPROM core size is 1.54 x 0.67 mm with a memory cell area of 175 um2.

Conclusions

A new cell technique utilizing a single poly-Si EEPROM cell reduces the process sequences by 25% as compared with a double poly-Si EEPROM. A wide operating voltage ranging from 1.5 V to 6.0 V and a stand-by current below 100 nA have been achieved for consumer oriented ASIC applications. It has been verified that EEPROM embedded CMOS LSIs are promising for future generations by utilizing novel process technology.

Acknowledgments

The authors would like to thank F.Tanaka for their continuous encouragement. T.Maruyama, H.Aoyagi, K.Noguchi, and H.Tanaka for their fruitful discussions.

References

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VLSI symp,Tech.Dig.,pp.41,1989.

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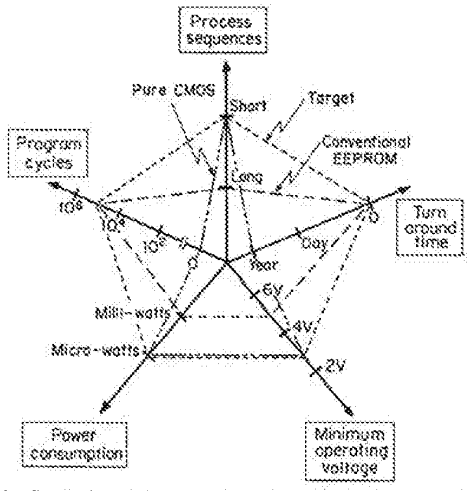


Fig.1 Comparison of characteristics between pure CMOS and conventional EEPROM

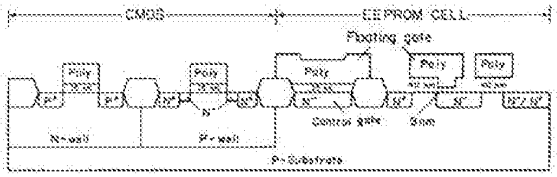


Fig.2 Cross-sectional view of single poly-Si EEPROM cell and CMOS

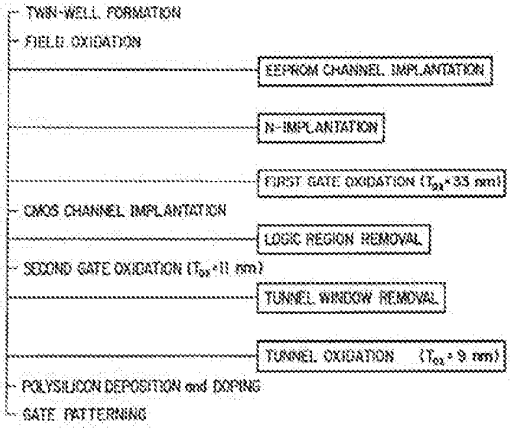


Fig.3 Single poly-Si EEPROM embedded CMOS process sequence

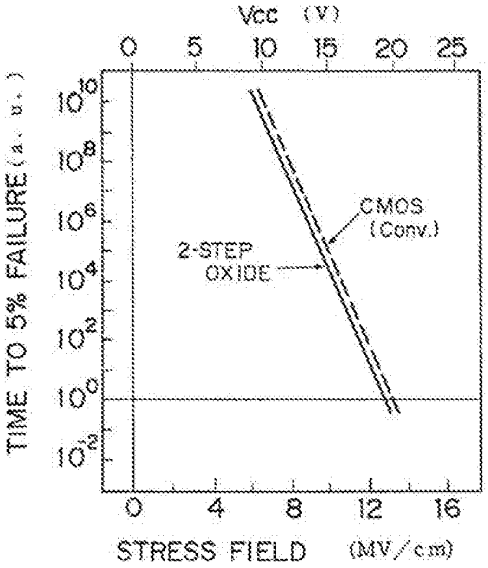


Fig.4 Dependence of times to 5% failure for 2-step oxide and conventional CMOS on stress field

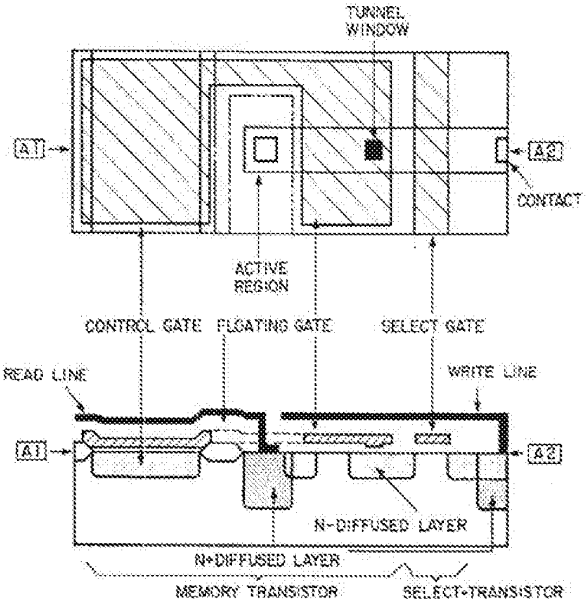


Fig.5 Layout and cross-sectional view of single poly-Si EEPROM cell

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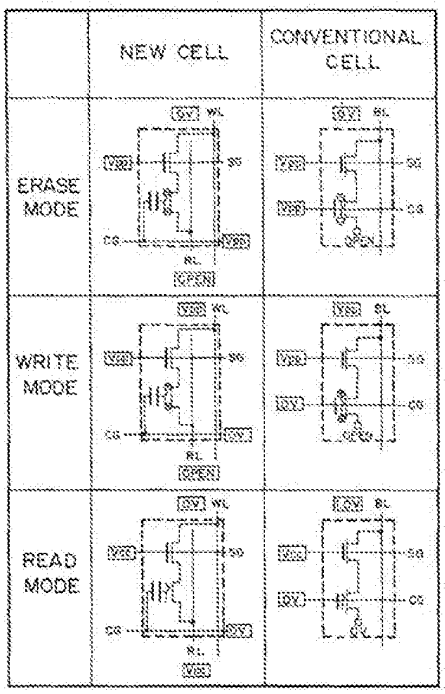


Fig.6 Schematics of new cell and conventional cell

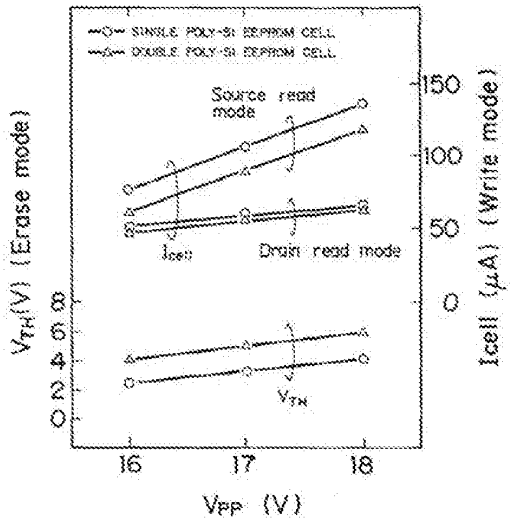


Fig.7 Erase/write characteristics:
Source read mode: WL or BL=0V, SG=5V, CG=0V, RL or source=5V
Drain read mode: WL or BL=1V, SG=5V, CG=0V, RL or source=0V

Table 1 Device characteristics of CMOS and EEPROM-CMOS processes

	PURE CMOS	EEPROM - CMOS
NMOS	1.0μm LDD	—
V_{th} (V)	0.89	—
I_{dp} (μA/μm)	240	320
PMOS	1.0μm Conv.	—
V_{th} (V)	-0.85	—
I_{dp} (μA/μm)	-160	-160

Table 2 Test chip features

Device technology	1.0μm EEPROM EMBEDDED CMOS
Total Transistors of number	2000
Core size	1.54 x 0.67 mm
Standby current (clock stop mode)	100 nA (Vcc=5.5V)
Operation current (1×4MHz)	300 μA (Vcc=5.5V)
Operating voltage	4.5~6.0 V
Program voltage	16 V
Erase time	2ms TYP.
Write time	2ms TYP.
EEPROM	64 bytes

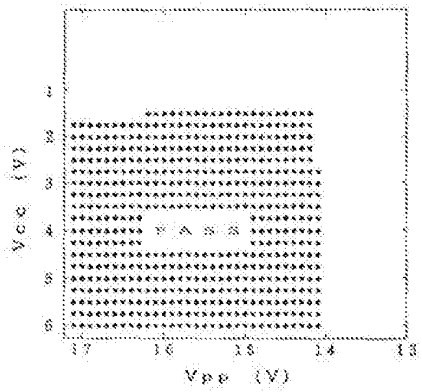


Fig.8 Schmoo-plot of operating voltage as a function of Vpp

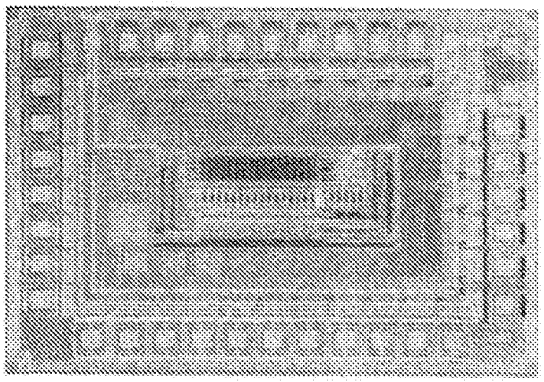


Fig.9 Test chip photograph (64 byte EEPROM core)

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A Novel Robust and Low Cost Stack Chips Package and Its Thermal Performance

Soon-Jin Cho, Sang-Wook Park, Myung-Guen Park, and Deok-Hoon Kim

Abstract—**In an attempt to provide a high density memory solution, especially for workstation and PC server, a stack chips package(referred to as "SCP" hereafter) has been developed. The major characteristics of SCP are as follows: 1) SCP contains a plurality of both memory chips and lead frames within a molded plastic package; 2) chip selection is made through the wire bonding option, resulting in the package with a memory capacity twice or four times that of monolithic chip; 3) plural lead frames are electrically interconnected all at once, using metal solders electroplated on the lead frame surface; and 4) SCP is found reliable and cost competitive when compared to other stack packages because it basically adopts the molded plastic packaging technology as well as the metal solder interconnection method. As electrical interconnection methods, both fluxless soldering joint of Ag/Sn and high-pressure mechanical joint of Ag were evaluated extensively and they successfully provided a reliable electrical conduction path without any signal degradation. Temperature cycle test and pressure cooker test were proved not to produce any micro cracks across the joint. The thermal performance of SCP was simulated by a thermal model based on finite element method (FEM) [1] and also experimentally verified, showing good agreement within 10% deviation from simulated value. 128M SCP showed better thermal performance than stacked two TSOP's because one chip could serve as a heat sink while the other chip is activated and thermal conduction path through the lead frame is short.**

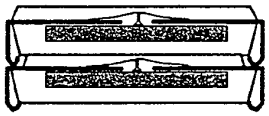
Index Terms—**Fluxless solder joint, memory device, reliability, stack package, thermal performance.**

I. Introduction

As THE DEMAND for miniaturization or portability of electronic systems continuously increases, the packaging technologies which can realize a high density product have received greater attention from system makers. Accordingly, modern electronic systems require much higher density memory for both their maximized electrical performance and miniaturization. Two approaches have been tried in order to increase the memory density. Memory density means the total memory capacity available divided by the board area taken by the package after second-level packaging in this study. The first approach is to produce more highly integrated memory chips than the previous one by adopting finer photolithographic technology in circuit fabrication. The effort to enhance the memory density has been focused on the first approach so far. Semiconductor industry has seen a four-time increase of memory density every three years. However, recently the increasing speed of memory integration density has been greatly challenged by the enormous development cost as well as plenty of technical barriers. The second approach is based on packaging technology, not on circuit integration technology, to provide a high density memory. Without cost and time to market issues, it goes without saying that the monolithic chip with high integration density is the best solution to realize a high density memory. For these reasons, the packaging technologies which can provide a high density memory have been developed by many IC makers and assembly subcontractors.



(a) 2-high TSOP stack



(b) 2-high SOJ stack

Fig. 1. Schematic diagrams of representative 2-high package stack: (a) 2-high TSOP stack and (b) 2-high SOJ stack.

Three-dimensional (3-D) packaging technologies have been investigated as one of the most promising solutions for a high density packaging, where either bare chips or MCM's are stacked along the z-axis [2]. Stacking bare chips or discrete packages along the z-axis can increase the memory density without sacrificing board area. Stacking technology based on the conventional resin-molded plastic package can be further divided into package stack technology and chip stack technology. In package stack technology, several packages of the same kind such as TSOP or SOJ are stacked in the vertical direction, while a plurality of bare chips of the same kind are stacked within a molded plastic package in chip stack technology. Samsung Electronics [3], [4], LG Semicon [5], [6], and Staktek [7]–[10] are well known for their package stack technology. Fig. 1 shows two examples of package stack technology. Chip stack technology was also developed using interposer materials such as lead frame or tape automated bonding (TAB) tape by Hitachi [11], [12] and LG Semicon [13].

Table I compares a couple of the main characteristics of Hyundai's 2-high chip stack with general 2-high package stack in terms of assembly cost, package thickness, and reliability. Assembly cost of SCP was estimated from the following two assumptions. First, lead frame cost represents half the total

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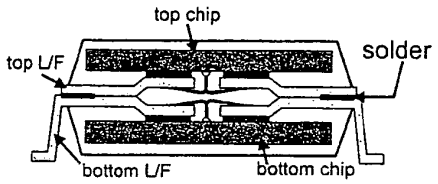
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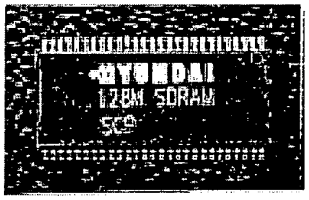
TABLE I
COMPARISONS OF HYUNDAI'S 2-HIGH CHIP STACK TECHNOLOGY AND GENERAL 2-HIGH PACKAGE STACK TECHNOLOGY

Items	2-high chip stack	2-high package stack
Feature	One SOP	Two TSOPs
Assembly Cost	1.78X* + α	2X* + β
Package Thickness	About 1.8mm	About 2.2mm
Reliability	Comparable to TSOP	NA

*X : assembly cost of a TSOP containing a chip and a lead frame in the package.

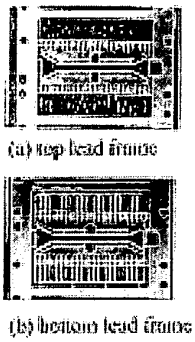


(a)



(b)

Fig. 2. (a) Cross-sectional drawing and (b) assembled package photograph of Hyundai's 2-high SCP.



(a) top lead frame

(b) bottom lead frame

Fig. 3. (a) Top view of as-received top lead frame and (b) bottom lead frame. The white region near dam bar line denotes the electroplated solder materials.

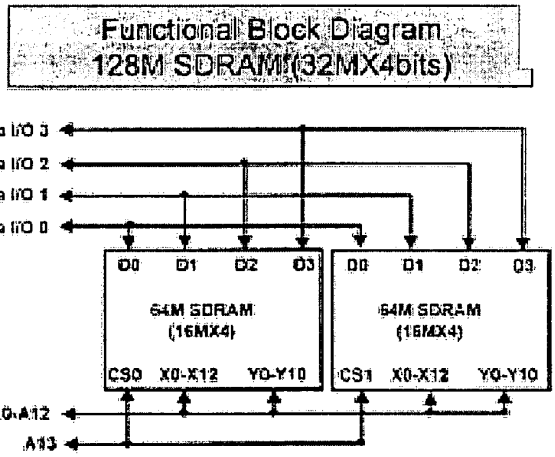


Fig. 4. Functional block diagram of 128M SDRAM SCP composed of two 64M SDRAM chips with the same bit configuration of 16M × 4 b.

assembly cost and increases by 15% due to selective electroplating of solder materials on the lead frame surface. Second, SCP claims the twice materials cost and processes cost as TSOP until it reaches transfer molding process. In assembly cost estimation of SCP, α represents the cost resulting from the lead frame joining process. So it is negligible. On the other hand, β, the additional cost needed to stack two TSOP's, exceeds $10 as of 1998. According to cost analysis result, chip stack is definitely much chipper than package stack. When it comes to reliability, chip stack is expected to show comparable reliability to the conventional plastic package, for example, TSOP. However, the reliability of package stack must be inferior to TSOP because of an additional solder joints made between two packages.

II. PACKAGE CONCEPT AND ASSEMBLY

Fig. 2(a) shows the cross-sectional drawing of a 2-high SCP. Two memory chips are mounted opposite to each other on the corresponding lead frame which serves as an interposer. Basically the SCP contains two types of lead frame with 6 mil (0.1524 mm) down-set. Down-set depth is determined such that the gold wires of top chip and bottom chips do not touch each other. Electrical interconnection between top lead frame and bottom lead frame is made by lead-to-lead solder joint. That is why SCP is low cost technology. Fig. 2(b) shows the assembled SCP. The SCP is a so called SOP (small outline package)-type package, having outer dimension of 380 mils (9.652 mm) in short side and 875 mils (22.225 mm) in long side. However, SCP has no specific limitations to the package format, package external size, and the kind of DRAM chips stacked.

Fig. 3(a) is the top view of top lead frame and Fig. 3(b) bottom lead frame. Solder materials electroplated are shown in white color near the dam bar line in the figure. The top lead frame has no outer leads. LOC die attaching and wire bonding are carried out separately. In the next step, the top and bottom lead frame are brought into contact with static pressure and heated in an inert gas atmosphere. Tens of the leads of top lead frame are bonded to the corresponding leads of bottom lead frame at the same time. In Section III, the lead-to-lead joining process and its related solder materials will be discussed in more detail. The joined lead frames are encapsulated by transfer molding. In the trimming process, the dam bars of top lead frame and bottom lead frame are cut simultaneously. The outer leads of bottom lead frame are finally deformed in gull-wing shape.

Fig. 4 is a functional block diagram illustrating an example of a 128 M synchronous dynamic random access memory (SDRAM) SCP. M is assumed equal to the twenties power of 2 hereafter. 128M SDRAM SCP comprises two 64M SDRAM

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TABLE II
VOLUME RESISTIVITY OF SOLDER MATERIALS AND Ag-FILLED CONDUCTIVE ADHESIVE AT ROOM TEMPERATURE

Materials	Sn	Ag	Sn-37Pb	Sn-0.7Cu	Sn-3.5Ag	Ag-filled epoxy (filler content=82wt%)
Resistivity ($\times 10^{-6}\Omega$cm)	10.9	1.6	15.0	12.9	7.5	80

chips with the same bit configuration plus two corresponding lead frames. 64M SDRAM chips can take different bit configurations, for instance, 8M × 8 b, 16M × 4 b, 64M × 1 b, and so on. One of them is 16M × 4 b as shown in Fig. 4. With reference to Fig. 4, an outline of SCP as well as chip selection method will be described. The 128M SDRAM SCP of 32M 4 b can be constituted by combining two 64M SDRAM chips with the bit configuration of 16M × 4 b and then accessing two 64M SDRAM chips alternatively. Data input/output pads $D0$–$D3$ of the two 64M SDRAM chips are connected in common to corresponding data input/output terminals $D0$–$D3$ of the SCP. In this bit configuration, 13-b X address signals $X0$–$X12$ and 11-b Y address signals $Y0$–$Y10$ are fed to address input pads $A0$–$A12$ of the 64M SDRAM chips in common. Furthermore, an X address signal, $X13$ which acts as a chip selection signal, is fed to an address input pad $A13$. The level of the X address signal, $X13$, determines which of the two 64M SDRAM chips will be brought into a selected state. As a result of alternative chip selection, the SCP has a bit configuration of 32M × 4 b and inputs or outputs data in the unit of 4 b at the same time. Since the two 64M SDRAM chips are activated in an alternative manner, the power consumption of 128M SDRAM SCP is almost equal to that of one 64M SDRAM chips.

III. LEAD-TO-LEAD JOINT

A strong mechanical joint is required to guarantee stable electrical interconnection between the top and bottom lead frames during the assembly as well as in the period of field operation. Except the case where a YAG laser is used for both cutting and interconnecting leads [11], a bonding medium is usually needed to electrically and mechanically join the two components together. Most common bonding media in electronic applications are solder materials and electrically conductive polymer adhesive. Table II summarizes the volume resistivity at room temperature of several solder materials and Ag-filled conductive polymer adhesives. Solder materials are generally preferred where high electrical and thermal conduction is required. In addition, Ag-filled epoxy is relatively expensive material and it needs post cure after joining process. Therefore, as-joined body should be handled with great care until it goes through post cure process. Because of the shortcomings of Ag-filled epoxy mentioned above, we excluded it among the candidates of bonding media.

The solder materials and joining methods are recommended to have the following characteristics; fluxless joining process, low electrical resistivity, environment friendly, strong mechanical joint strength, low α-particle emission, and low cost. After thoroughly evaluating the merits and demerits of technically feasible joining systems, finally two candidates were selected and extensively investigated. One is a fluxless soldering joint of Ag/Sn and the other is a high-pressure mechanical joint of Ag.

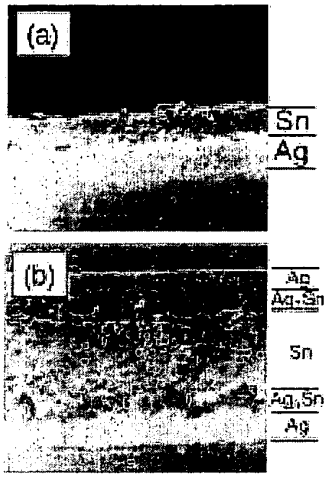


Fig. 5. (a) Cross-sectional view of as-received lead frame with Ag/Sn selective plating layer and (b) cross-sectional microstructure formed right after making fluxless soldering joint of Ag/Sn.

A. Fluxless Soldering Joint of Ag/Sn

For the fluxless soldering joint of Ag/Sn, the joint region of top and bottom lead frame were selectively electroplated with 5 μm-thick silver/5 μm-thick tin sequentially. In the joining process, the top and bottom lead frame are brought into contact with static pressure and heated beyond the melting temperature of Sn, i.e., 232 °C in nitrogen atmosphere. Nitrogen gas blow was indispensable to preventing the Sn layer from oxidizing, eventually to getting a high quality joint. Fig. 5(a) exhibits the two-layer structure of Ag/Sn electroplated on lead frame prior to lead-to-lead joining. The silver layer acts as an adhesion promoter to the lead frame material, Fe-42 wt% Ni alloy. The cross-sectional microstructure after joining top and bottom lead frame is shown in Fig. 5(b). As can be seen in Fig. 5(b), globular second phase newly developed at two interfaces between silver and tin. SEM EDS measurement confirmed that the second phase is silver-tin intermetallic compound, Ag_3Sn. Therefore, fluxless soldering joint of Ag/Sn gave birth to the multilayer structure of lead frame/Ag/Ag_3Sn/Sn/Ag_3Sn/Ag/lead frame.

B. High-Pressure Mechanical Joint of Ag

Because the melting temperature of silver is too high to apply fluxless soldering as a joining method, high-pressure mechanical joint was tried at an elevated temperature. At room temperature it was not feasible to get a robust joint. However the process temperature at 200 °C was sufficient to make a strong joint. For the high-pressure mechanical joint, the joint region of the top and bottom lead frame was electroplated with 7 μm-thick silver. In the joining process, the top and bottom lead frame are

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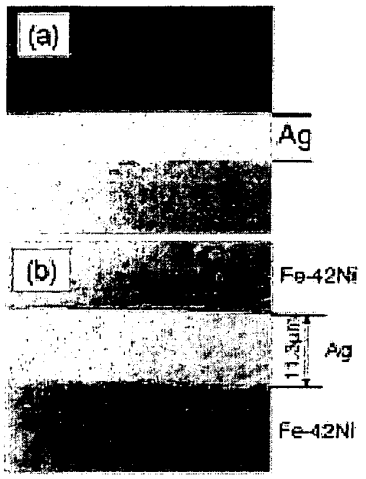


Fig. 6. (a) Cross-sectional view of as-received lead frame with Ag selective plating layer and (b) cross-sectional microstructure formed right after making high-pressure mechanical joint of Ag.

brought into contact with high static pressure ranging from 10–60 kNand heated to an elevated temperature. Unlike the fluxless soldering process, no atmosphere control was required.

Fig. 6(a) is the cross-sectional view of as-received lead frame with silver plating layer. Fig. 6(b), the silver-to-silver joint microstructure, proves that the perfect metallurgical bonding was formed between two silver plating layers, implying a high quality joint. The bondline thickness was about 11.3 μm, which means the severe plastic deformation of silver plating layer. The mechanical joining process produced nearly constant bondline thickness. On the contrary, fluxless soldering joint showed the variation of bondline thickness to some extent because the Sn completely melted during the joining process.

Ag/Sn plating was also found feasible to form a high-pressure mechanical joint, though it is not described here in detail. The high-pressure mechanical joint of Ag/Sn produced the very similar microstructure to that shown in Fig. 5(b).

Tens of kN clamping force acts on the top and bottom lead frame during the transfer molding. By extending the solder plating area of lead frame into the region on which clamping force acts, it was demonstrated that the high-pressure mechanical joint of Ag as well as Ag/Sn during the transfer molding could also provide a strong and reliable joint. The process temperature of transfer molding, 175 °C, was enough to obtain a strong joint. Thus when the high-pressure mechanical joint is considered the joining method, preliminary joining process before transfer molding could be skipped.

C. Mechanical Strength of Lead-to-Lead Joint

Mechanical robustness of the joint was measured at room temperature by single lap shear strength test. Exclusive test specimen shown in Fig. 7 was designed for the test. The joint area was 0.4536 cm^2. Four samples were tested for each joining systems. Test results on average are indicated in Fig. 8. The high-pressure mechanical joint of Ag produced the higher strength of 49.1 MPa, while the fluxless soldering joint of Ag/Sn resulted in somewhat lower strength of 32.7 MPa.

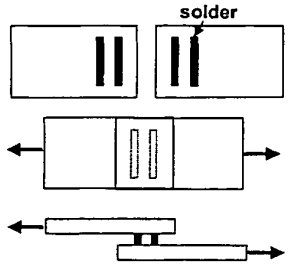


Fig. 7. Schematic illustrations of single lap shear test sample used for measuring joint strength.

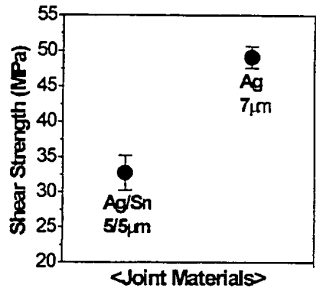


Fig. 8. Lap shear strength versus joint materials.

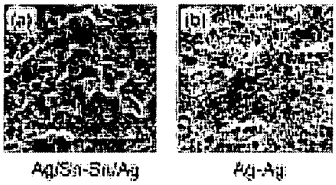


Fig. 9. (a) SEM microstructures taken from the mechanically separated surfaces of Ag/Sn and (b) Ag.

The mechanically separated surface of the top and bottom lead frame was observed by scanning electron microscope. According to Fig. 9(a), the adhesive failure along Ag_3Sn/Sn boundary took place predominantly in case of the fluxless soldering joint of Ag/Sn. SEM EDS profile verified again the presence of Ag_3Sn intermetallic compound on the separated surface. Fig. 9(b) shows the failure surface of mechanical joint of Ag, confirming ductile fracture of silver itself. SEM observation on the fracture surface indicated that the inferior joint strength of the fluxless soldering joint of Ag/Sn to the high-pressure mechanical joint of Ag was mainly attributed to the joint materials themselves rather than the joining method.

IV. Reliability

A. Pop-Corn Cracking Test

Studies have shown that moisture in the plastic package can cause cracking or delamination during the surface mount process [14]. Because the SCP is also made of molded plastic, it might be susceptible to moisture cracking and other plastic reliability concerns. Scanning acoustic tomograph (SAT) was taken on all packages prior to preconditioning to check out initial delamination or crack. The preconditioning flow used

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TABLE III
ELECTRICAL TEST RESULTS OBTAINED AFTER TEMPERATURE CYCLE TEST AND PRESSURE COOKER TEST

Test Items	Reliability Stress Conditions	Failures/sample size	
		Ag/Sn-Sn/Ag	Ag-Ag
Temp. Cycle Test	-65℃ to 150℃, 2 cycles/h 200 cycles	1/15	0/12
Pressure Cooker Test	121℃, 2atm, 100% RH 168 hours	0/15	0/12

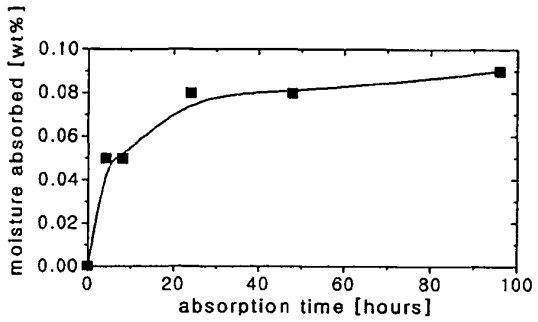


Fig. 10. Moisture absorption behavior of the SCP.

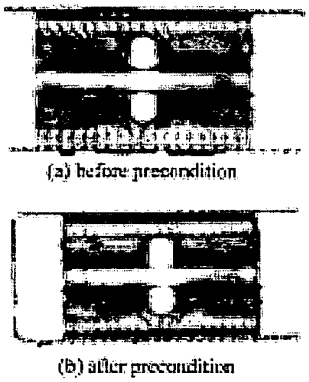


Fig. 11. (a) SAT T-scan image of the SCP before precondition and (b) after precondition.

for the moisture study is described here in detail. First, a 24-h prebake at 125 °C was carried out to drive out residual moisture. The packages were then exposed to moisture absorption under 85 °C/85% RH conditions. A sample size of 10 unit packages was used for each exposure time. After moisture exposure for a predetermined time, the packages were subjected to two passes of IR reflow stress. The temperature profile used in the solder reflow had a peak temperature of 235°C. The packages were then examined using a SAT and an optical microscope at 30 × to determine cracking and delamination.

Fig. 10 shows the moisture absorption behavior of SCP in weight percent. It has almost reached the saturation value of 0.09 wt% after 24-h storage at 85 °C/85% RH condition. Fig. 11(a) exhibits the SAT T-scan images of the SCP before preconditioning and (b) after 96 h of moisture absorption at 85 °C/85% RH followed by two cycles of IR reflow. When the lower image was compared with the upper one, observed was only a slight propagation of delamination around LOC tape area. There was

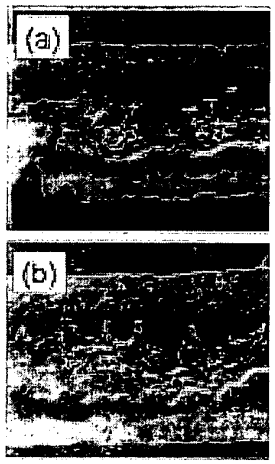


Fig. 12. Cross-sectional microstructures formed after going through reliability stress: (a) Two-hundred temperature cycles and (b) 168-h exposure to 85 °C/85% RH condition. Arrow marks indicate the formation of Ag_3Sn intermetallic compound after reliability test.

no new delamination interface created due to the moisture induced stress. From the SAT and optical microscope inspection after IR reflow, neither package crack nor interface delamination was observed, even in the package that absorbed moisture for 96 h. This result demonstrates the excellent resistance of SCP to moisture induced cracking.

B. Temperature Cycle Test and Pressure Cooker Test

In addition to the moisture induced sensitivity, SCP's were subjected to both temperature cycle test and pressure cooker test. As-assembled packages which had passed an electrical test underwent the same preconditioning as the one mentioned above, except that the packages were exposed to 85 °C/85% RH for 24 h at this time. After applying two types of reliability stress, the packages again received the electrical test to determine whether they are electrically good or not.

Table III shows the reliability test results. All packages tested survived the 200 temperature cycles as well as the 168 h under pressure cooker condition. From the moisture sensitivity test, temperature cycle test, and pressure cooker test, it can be concluded that the SCP has an excellent reliability comparable to a standard plastic package, TSOP.

Fig. 12(a) shows the typical joint microstructures of the fluxless soldering joint of Ag/Sn, which was taken after 200 temperature cycles and Fig. 12(b) after 168-h storage under pressure cooker condition, respectively. When both Fig. 12(a) and (b) was compared with the as-joined microstructure shown in Fig. 5(b), the growth of Ag_3Sn intermetallic compound is the

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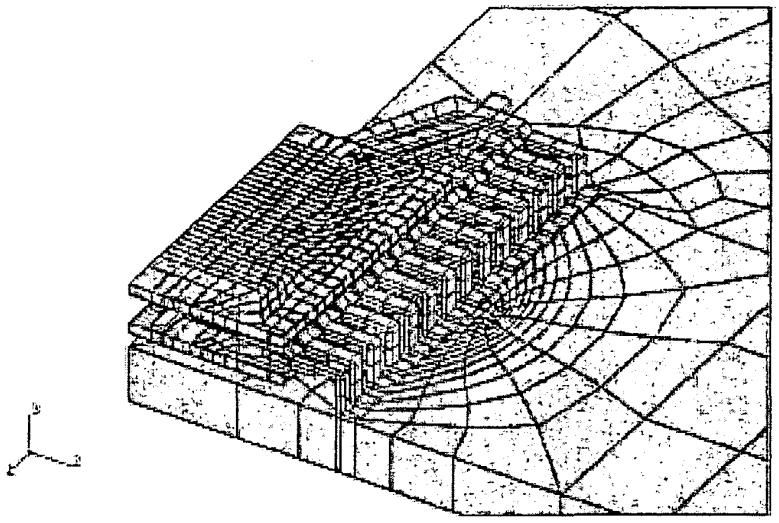


Fig. 13. Three-dimensional finite element model of 128M SDRAM SCP, showing only internal components, i.e., PCB, lead frame leads, chips.

most notable thing due to the reliability stress. Besides, also observed was the additional precipitation of silver atoms, which were supersaturated in Sn matrix during the joining process, as a form of Ag_3Sn intermetallic compound (arrow marked in the figure). As can be confirmed from Fig. 12, however, both temperature cycle test and pressure cooker test were proved not to produce any micro cracks across the joint, which are likely to degrade the long term reliability of lead-to-lead joint.

As expected from the material properties of silver, for instance, high melting temperature and high resistance to chemical corrosion, no measurable changes after reliability test were observed in the microstructure made by high-pressure mechanical joint of Ag.

V. Thermal Performance

A. Description of the Finite Element Model

Fig. 13 shows the FEM model used in this study. The package and test board were meshed in full 3-D solid elements. Due to the symmetry of test structure, only a quarter section was modeled for the analysis. The model was calculated using ABAQUS FEM software. The thermal performance of IC packages is represented as thermal resistance value, Θ_{JA}. This value is defined by following equation:

$$\Theta_{JA} = (T_j - T_a)/P$$

where

- T_j junction temperature;
- T_a ambient temperature;
- P dissipation power.

The parameter, Θ_{JA} has the advantage that the junction temperature of IC can be easily calculated from the dissipation power of IC and ambient temperature. However, since this parameter highly depends on the construction of test board, conductivity of material constructing package and test board, and environmental conditions, the application of this parameter should be carefully considered for each package and test board.

The boundary conditions consisted of heat transfer coefficients applied to the top surface and bottom surface of both package and test board. The heat transfer coefficient is a nonlinear function of external surface temperature in this model that applied to natural, mixed, and forced convection regime and includes the contribution of radiation. The total heat transfer coefficient, h_T, is calculated from following equations [15]:

$$h_t = \left(h_{NC}^3(L, \Delta T) + h_{FC}^3(L, V_{AIR})\right)^{1/3} + h_{RAD}(\Delta T)$$

$$h_{NC} = 0.944\left(\frac{\Delta T}{W}\right)^{0.35}$$

$$h_{FC} = 3.79\left(\frac{V_{AIR}}{W}\right)^{0.05}$$

$$h_{RAD} = \epsilon\sigma\left(\frac{T^4 - T_{Ambient}^4}{\Delta T}\right)$$

where

- ΔT temperature difference between the external surface of package and ambient;
- W characteristic length (here set equal to the package length);
- V_{AIR} free-stream air velocity;
- ϵ emissivity;
- σ Stefan–Boltzman constant.

B. Test Conditions

Table IV summarizes the dimension and material properties of all components used in this study. The test board is a FR4 PCB which has solder finished lead lands on both sides. Considering the PCB with 5% coverage of solder, the effective thermal conductivity of test board was calculated. The value are $k_{\text{cross plane}} = 0.25$ W/m.°C and $k_{\text{in plane}} = 2.63$ W/m.°C in this study.

Table V shows the test conditions used for thermal performance test of 128M SDRAM SCP. Ten packages was tested both under natural convection conditions in 1 ft^3 sealed chamber

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TABLE IV
MATERIAL PROPERTIES, MODEL DIMENSION, AND PARAMETERS USED IN THIS STUDY

Package	Size (mm x mm)	9.65×22.22
	Height (mm)	1.8
	I/O configuration	54 LD
	Chip thickness (mm)	0.29
Thermal test board	Size (mm x mm)	114×150
	Thickness (mm)	1.5
	Solder Metal Layer	2
	Solder Metal Thickness (oz)	1-2
	Solder Metal Coverage (%)	5
Thermal Conductivity (W/m.℃)	Chip	150
	Lead frame	14.7
	FR4	0.25
	Solder	51
	PCB (k_{xx},k_{yy}/k_{zz})	2.63 / 0.25

TABLE V
TEST CONDITION FOR 128M SDRAM SCP

V_H Heating Voltage (volt)	**3.0 – 3.6**	**@Room Temp**
t_{RRC} (nsec)	**100 – 200**	
Power (W)	**0.2 – 0.5**	
Heating Time (sec)	**3000**	
Air Velocity (ft/min)	**0 – 600**	

TABLE VI
DUT INTERCONNECTION FOR THERMAL TEST

Item	SDRAM
V_{CC} condition	1) +V_H forcing & sensing 2) Common to data I/O pins
V_{SS} condition	1) -V_H forcing & sensing 2) Common to all add./input pins
Heating pin	Clock(CLK)
L/F condition	Open to V_{CC} & short to V_{SS}

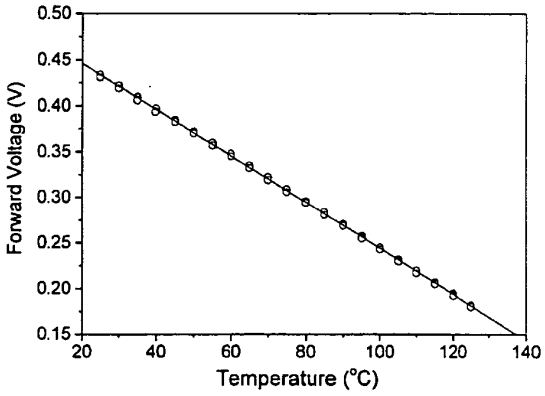


Fig. 14. Temperature calibration curve for thermal performance test.

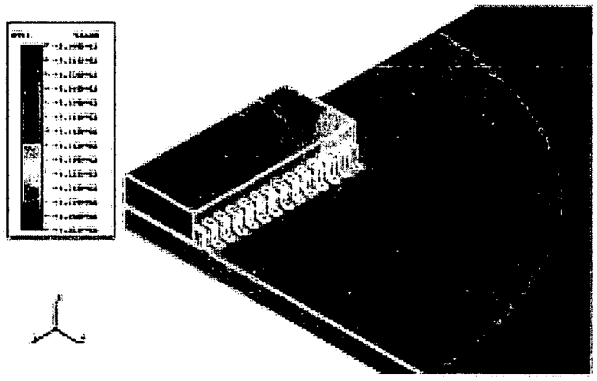


Fig. 15. Temperature contour plot of 128M SCP in case of natural convection mode.

and forced convection conditions in wind tunnel with a 12″ square test section. In case of forced convection, tests were performed at seven air velocities; 0, 100, 200, 300, 400, 500, and 600 ft/min with the air blow direction along the long dimension of package. Three voltage levels and cycle rates (t_{RRC}) were applied to the packages at natural convection mode.

Since the 128M SDRAM SCP consisted of two 64M SDRAM chips, DUT was electrically interconnected to the test board as described in Table VI in order to use the real SDRAM chip for heating source. The several dissipation power levels were applied by controlling cycle rate (t_{RRC}) or current. The chips was normally operated with /RAS pin in refresh mode, and the junction temperature was calculated from detected forward bias voltage (V_f) of substrate diode.

To use the V_f as the temperature sensitive parameter (TSP), diode was calibrated at several temperatures from 25–125 °C after equilibrium as indicated in Fig. 14. The slope of calibration curve is so called k-factor.

C. FEM Analysis Results and Experimental Verification

The FEM analysis was performed at the range of dissipation power from 0.2–0.5 W in SDRAM refresh mode. Fig. 15 shows the typical temperature distribution of SCP for natural convection mode. Since the temperature gradient of SCP is maximum through the lead frame, it is clear that the major heat flow path is chip-to-lead-to-thermal board.

Fig. 16 shows the converged h value for each model. The converged h value was 15–20 (W/°C m^2) for natural convection mode and 20–45 (W/°C m^2) for forced convection mode which is almost linear function of air velocity. The radiation effect can be ignored when air velocity exceeds a 300 ft/min at forced convection mode. However, as it can not be ignored at natural convection mode and mixed convection mode, critical is the adequate application of surface emissivity and radiative view factor [16]. In this study, the value of surface emissivity was 0.9.

The thermal performance predicted from FEM analysis is compared with experimentally measured one for natural convection mode in Fig. 17 and for forced convection mode in Fig. 18. The average deviation of FEM model from experimental results is 5% for forced convection mode, while the discrepancy is greater but it is still less than 10% for natural convection mode.

Table VII compares the thermal performance of several packages in terms of Θ_{JA}. 128M SCP has better thermal performance by about 10% than stacked two packages (2 × 64M

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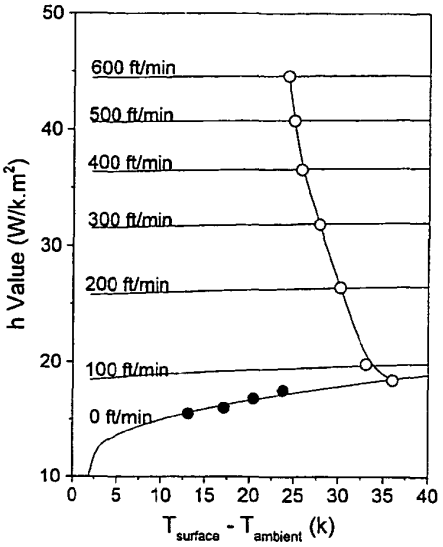


Fig. 16. Converged heat transfer coefficient of external surface of 128M SCP.

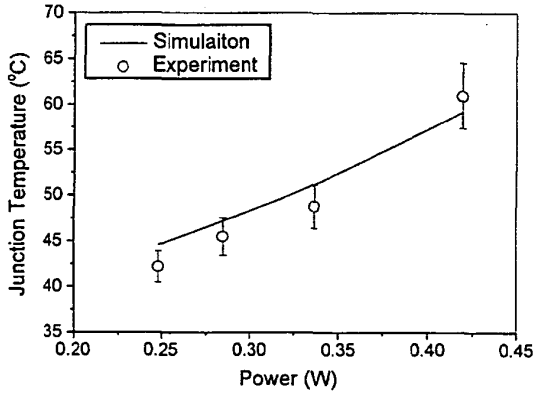


Fig. 17. Junction temperature of 128M SCP for natural convection mode at 25°C.

TSOP) because one chip could serve as a heat sink while the other chip is activated and thermal resistance through the lead frame is low. However, the Θ_{JA} of 128M SCP is 15% higher than 64M TSOP because of the thicker epoxy molding compound layer existing between junction and package surface as well as the relatively longer out-lead length. Even though the Θ_{JA} of 128M SCP is slightly higher than 64M TSOP, it is sufficiently acceptable to DRAM application considering the industrial specification for the maximum junction temperature, 80 °C at the ambient temperature of 25 °C and below 115 °C at the ambient temperature of 75 °C for natural convection mode.

VI. Conclusion

Based on lead-to-lead joint method using metal solders, a low cost and reliable SCP has been developed. The SCP contains plural memory chips and lead frames serving as an interposer within a molded plastic package. Thus, SCP allows system

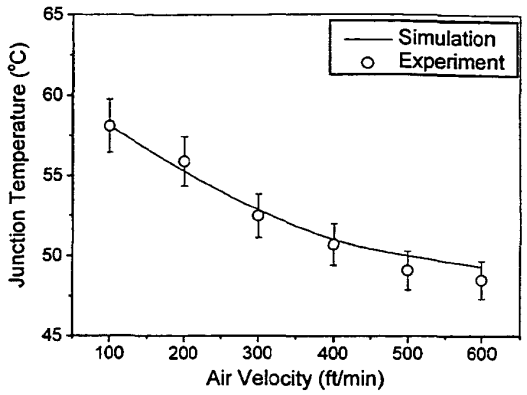


Fig. 18. Junction temperature of 128M SCP for forced convection mode at $P_{dissipation} = 0.42$ W.

TABLE VII
Thermal Performance of Various Packages for Natural Convection Mode

Package	Θ_{JA}		Remark
	Simulation	Experiment	
128M SCP	81.5	85.8	@ 25℃ V_{DD}=3.6V
64M TSOP	72.0	71.3	
2×64M TSOP	91.5	-	

makers to easily realize a memory capacity twice or four times that of monolithic chip without increasing board area.

As lead-to-lead joint methods, fluxless soldering joint of Ag/Sn and high-pressure mechanical joint of Ag were evaluated extensively and they successfully provided a strong and reliable electrical conduction path without any signal degradation. In addition to preliminary joint prior to transfer molding, high-pressure mechanical joint of Ag or Ag/Sn during the transfer molding was also found to provide a strong and reliable joint. Neither package crack nor interface delamination was found even in the packages which had absorbed moisture for 96 h at 85°C/85% RH, followed by two passes of IR reflow. SCP also survived two types of reliability stress, i.e., 200 temperature cycles ranging from −65 to 150 °C and 168-h exposure to pressure cooker condition, revealing a comparable reliability to standard TSOP.

The thermal performance of 128M SCP has been investigated by FEM simulation and experiment using real 64M SDRAM chips. The thermal resistance of SCP was improved by 10% compared to stacked two TSOP's and degraded by 15% compared to a TSOP. The junction temperature of SCP was 60 ± 3 °C for natural convection mode at ambient temperature of 25 °C under real SDRAM operating condition.

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He had worked at Anam/Amkor, from March 1993 to April 1995, as a Staff Engineer in the Electronics Packaging Research Group. He also had worked at Hyundai Electronics in their Advanced Package Development Group especially for DRAM application as a Principal Search Engineer as well as the Manager of the Group from May 1995 to January 1999. He now works for Flip Chip Technologies. His interest is in CSP's, especially wafer level CSP and characterization of their performance and reliability.

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A PLANAR TYPE EEPROM CELL STRUCTURE BY STANDARD CMOS PROCESS FOR INTEGRATION WITH GATE ARRAY, STANDARD CELL, MICROPROCESSOR AND FOR NEURAL CHIPS

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800 Ichimiyake Yasu-cho Yasu-gun Shiga-ken 520-23 Japan

ABSTRACT

A Planar type EEPROM cell structure which consists of adjacently placed a NMOS and a PMOS transistors with an electrically isolated common polysilicon gate by standard CMOS process (no ultra thin oxide,no stacking of floating and control gates) is developed. 5 to 10 volts shifts of threshold and more than thousands cycles of endurance is obtained.This EEPROM cell can be easily integrated with Gate Array, Standard Cell,Microprocessor LSIs. This can store Analog data and be applied to Neural chips.

1. INTRODUCTION

BIOS and micro-codes for system controls are stored in EPROM or EEPROM chips and used with system control logic LSIs. Integration of EEPROM with logic LSIs, Gate Array, Standard Cell and Microprocessor bring many merits.But such integration requires EEPROM unique processings, ultra thin oxide, stacking of floating and control gates and others.

We developed a Planar type EEPROM cell structure by Standard CMOS process without any conventional EEPROM process. By this EEPROM cell structure, we can easily make EEPROM integratedGate Array,Standard Cell and Microprocessor LSIs with many merits of lower cost, more space saving and easier micro-code storing/updating, etc.

2. PRINCIPLE OF EEPROM OPERATION

Our developed Planar type EEPROM consists of adjacently placed NMOS and PMOS transistors with a common poly Si gate.The common gate is electrically isolated from another component. It works as "Floating Gate". The P+ diffusions and N well are wired together, and work as "Control Node". See Fig-1-A,1-B,1-C. Fig-1-A is the concept of this EEPROM cell, and Fig-1-B the physical structure. This EEPROM cell is symbolically expressed as shown in Fig-1-C.

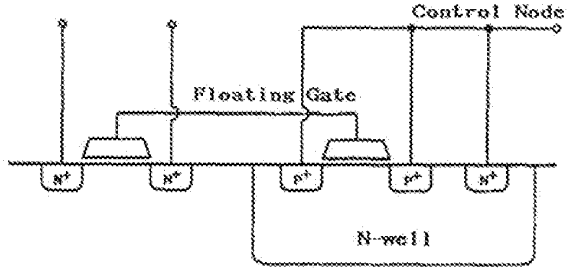


Fig-1-A : Concept

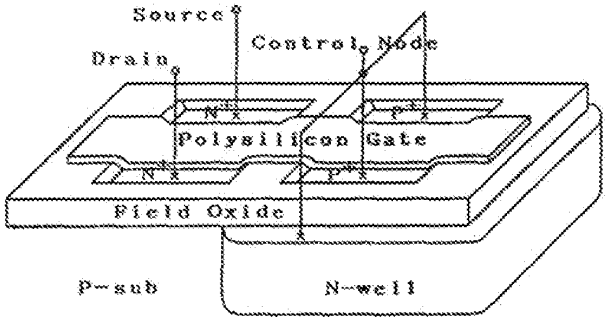


Fig-1-B : Physical Structure

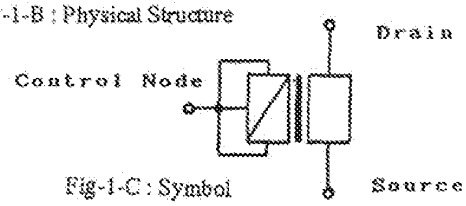


Fig-1-C : Symbol

2.1. WRITE OPERATION

There are two modes of Write operation as shown in Fig-2-A-1 and 2-A-2. One is by NMOS channel hot electron injection (NCHE Write) and the other by NMOS FN tunneling injection (NFN Write).

(A) NMOS Channel Hot Electron Injection (NCHE Write)

As shown in Fig-2-A-1, the source of NMOS is grounded, a medium voltage is applied to the drain and a high voltage Vp to the Control Node.Vp is divided by the series capacitances of PMOS and NMOS gates.A proper combination of the drain and Vp voltages is selected for channel hot electron injection into the FloatingGate, and the FloatingGate is negatively charged.

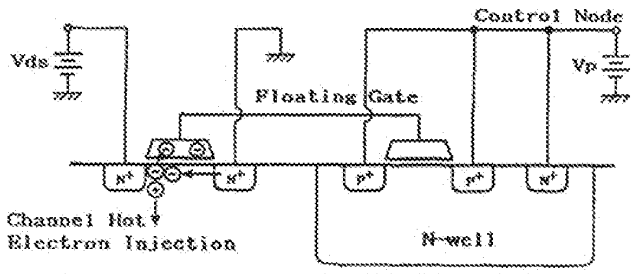


Fig-2-A-1 : Write Operation by NMOS Channel Hot Electron Injection (NCHE Write)

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(B) NMOS Gate FN Tunneling Injection(NFN Write)

The N+ diffusions of NMOS transistors are grounded, and a high voltage Vp is applied to the Control Node as shown in Fig-2-A-2. This mode is used when the gate capacitance ratio of CGP/CGN is larger than 2 or 3. Under this condition FN tunneling occurs in NMOS gate oxide. Many electrons are injected into the gate from N+ diffusions. The amount of injected electrons is determined by Vp and CGP/CGN.It is a linear function of Vp. This means that this mode can be used for Analog data storing. This EEPROM cell is applicable to Neural chips.

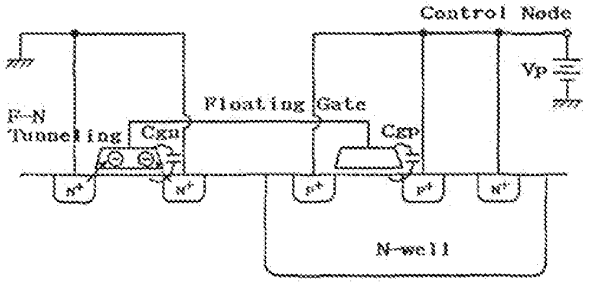


Fig-2-A-2 : Write Operation by NMOS F/N Tunneling (NFN Write)

2.1. READ OPERATION.

Read operation is done as shown in Fig-2-B.A medium voltage Vr is applied to the Control Node. When there is no charge on the Floating Gate, the NMOS transistor is in ON state. On the other hand, if the floating gate is negatively charged by the Write operation, the NMOS transistor is in OFF state. Sensing the ON/OFF state, the Read operation is done.

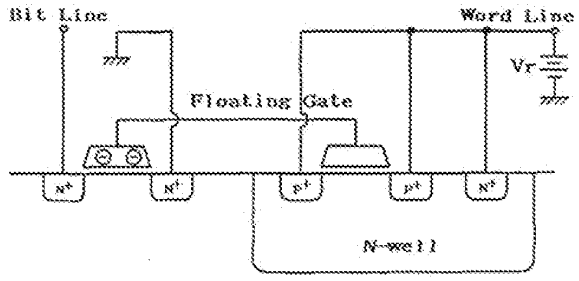


Fig-2-B : Read Operation

2.2. ERASE OPERATION

There are two modes of Erase Operation as shown in Fig-2-C-1 and 2-C-2. One is by FN tunneling in the oxide of PMOS, and the other by FN tunneling in the oxide of NMOS.

(A) PMOS Gate FN Tunneling (PFN Erase)

N+ diffusions of NMOS transistor are grounded, and a high voltage Ve is applied to the Control Node. When the gate capacitance ratio CGP/CGN is less than 1, the electric field across the PMOS oxide is larger and FN tunneling between the Floating Gate and P+ diffusions/channel occurs. And the charges on the Floating Gate are removed and the gate is recovered.

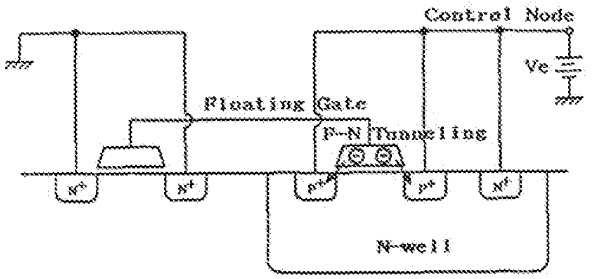


Fig-2-C-1 : Erase Operation by PMOS F/N Tunneling (PFN Erase)

(B) NMOS Gate FN Tunneling (NFN Erase)

As shown in Fig-2-C-2, the Control Node is grounded, and N+ diffusion of NMOS transistor are kept at a high potential Ve.The high electric field across the N+ diffusion and the Floating Gate causes FN tunneling. And the charges on the Floating Gate are removed.

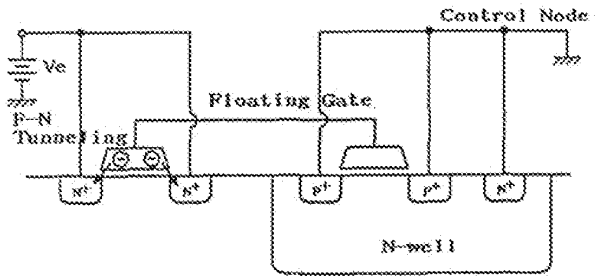


Fig-2-C-2 : Erase Operation by NMOS F/N Tunneling (NFN Erase)

3. EXPERIMENTS

Fig-3 shows the test chip.This is by standard 0.8um CMOS process, tox=150A, Ln=Lp=0.8um, EEPROM cells with various combination of NMOS and PMOS channel widths.

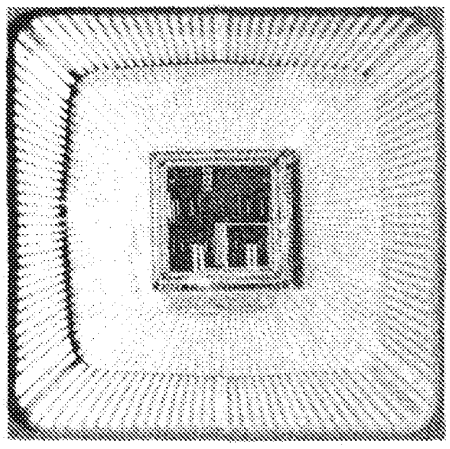


Fig-3 : Test Chip

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3.1. THRESHOLD VOLTAGE SHIFTS

The threshold voltage shifts of Write operation by NMOS Channel Hot Electron Injection (NCHE Write) is shown in the Fig-4-A. The gate capacitance ratio CGP/CGN=1.0. More than 9 volts shifts are observed at Vp=15V and Vds=9V. 5V shift is achieved at Vp=12V and Vds=8V. The write pulse duration is 100mS. When 10 mS, the shifts are 0.3 volts smaller.

Write operation by NMOS FN Tunneling Injection (NFN Write) gives the results in Fig-4-B. We see linear relations between the programming voltage Vp and threshold shifts. Larger ratio of CGP/CGN brings more shifts.

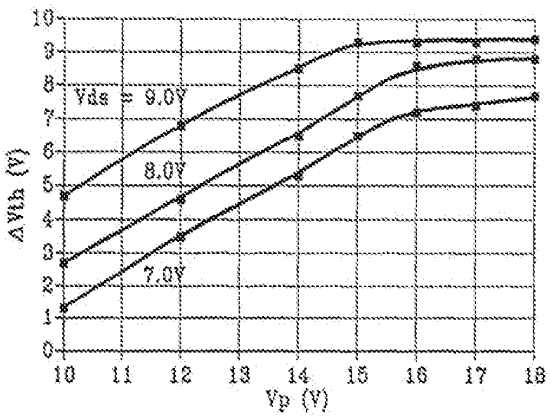


Fig-4-A : Vth Shift Characteristic (NCHE Write)

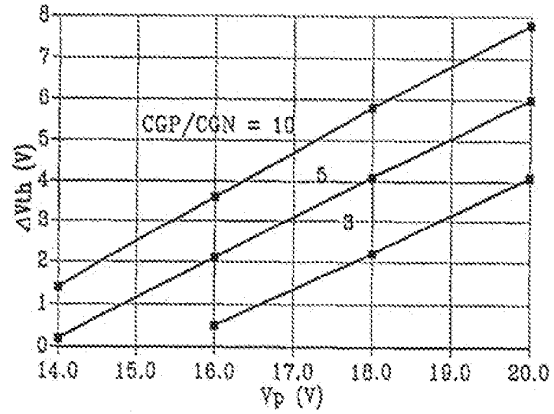


Fig-4-B : Vth Shift Characteristic (NFN Write)

3.2. ENDURANCE CHARACTERISTICS

In Fig-5-A, endurance characteristics of (NCHE Write + PFN Erase) is shown. The capacitance ratio CGP/CGN=2/3. The write is done at Vp=15V, Vds=9V with 10mS duration. Erase operation is done at Ve=18V with 100mS duration.

In Fig-5-B ,the endurance data of (NFN Write+ NFN Erase) is shown. The capacitance ratio CGP/CGN=5.0. Write is done at Vp=19V,Erase at Ve=14V with the same duration of 100mS.

After thousands cycles enough threshold voltage differences are obtained. This is the result of standard CMOS process. It is very enough for BIOS or micro-code storage.

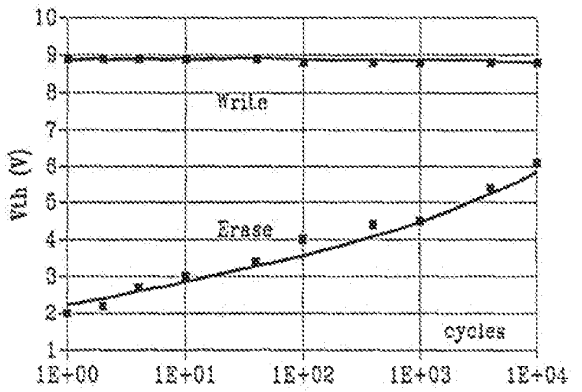


Fig-5-A : Endurance Characteristic (NCHE Write+PFN Erase)

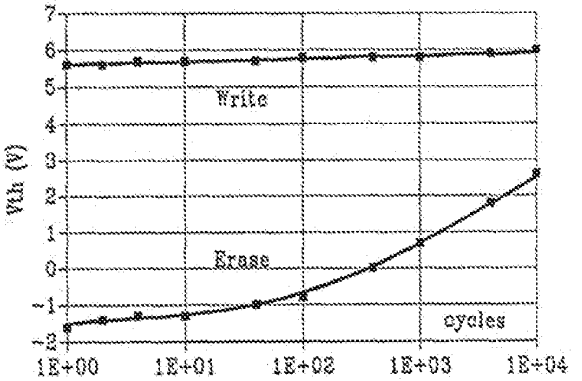


Fig-5-B : Endurance Characteristic (NFN Write+NFN Erase)

3.3. ENHANCEMENT OF ENDURANCE

The change of ERASE characteristic after thousands cycles is due to electron trapping in the oxide layer which reduces the electric field strength. This can be enhanced to some extent by optimizing erase potential Ve.Fig-6-A shows an endurance data by Ve optimization. Write was done at Vp=19V and 100mS by NFN write, erase at 100mS by NFN erase. The optimized Ve potential is shown in the Fig-6-B. A few more volts bring good erase characteristics (like in early erase cycles) after 10 thousands cycles. This kind of Ve control is easily done by on-chip circuits.

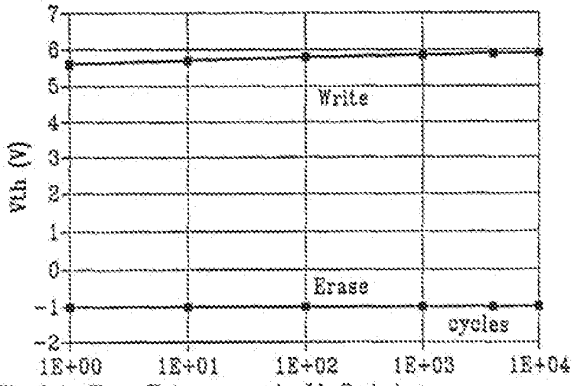


Fig-6-A : Erase Enhancement by Ve Optimization

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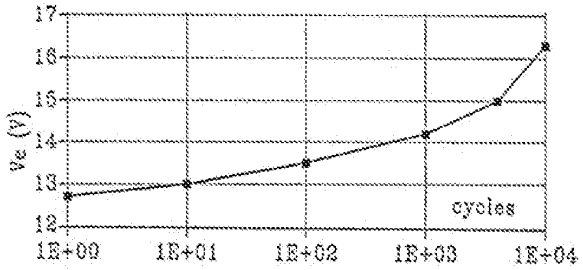


Fig-6-B : Ve Optimization

3.4. HIGH TEMPERATURE DATA RETENTION

In Fig-7 the high temperature data retention characteristic is shown. Assuming failure at 30% charge loss and the activation energy of 1.4eV, the life under 85 degree C is more than thousands years.

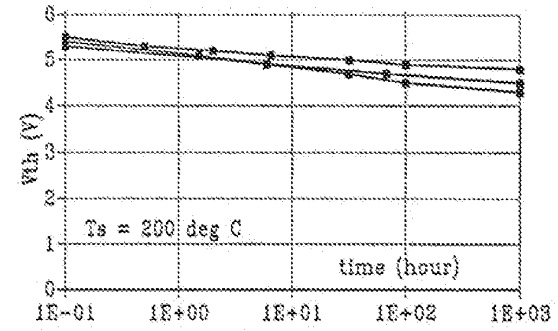


Fig-7 : High Temperature Data retention

4. APPLICATIONS

Almost all systems and sub-systems are software controlled and the software codes are stored in separate chips of EPROM or EEPROM. The size of such codes are small, a few KBytes. And a number of Write/Erase cycles is very small, less than 10. By integrating this EEPROM cells into Gate Array, Standard Cell and Microprocessor,we can enjoy many merits. Utilization of standard CMOS process line brings no cost increase in chip manufacturing. And lower cost in system/sub-system manufacturing, space saving (compact), easy micro-code storing and updating through LSI data bus, etc. are achieved.

The endurance can be greatly enhanced by oxide process optimization. And applications to NVRAM are possible too.

4.1. EEPROM ARRAY CIRCUIT

An example of EEPROM array circuit is shown in Fig-8-A. A control node is wired to a specific "Word Line", a drain to a "Bit Line", a source to a "Virtual Gnd Line" respectively. The Bit Line BL(i) is shared by Cell(i,j)-upper and Cell(i,j)-lower, the Virtual GND Line VGND(i,i+1) by Cell(i,j)-lower and Cell (i+1,j)-upper.

The principles of the circuit operation are described in Fig-8 -B. Selection of Cell(i,j)-upper or Cell(i,j)-lower is done by controls of VGND(i-1,i) and VGND(i,i+1). In Write / Read phases, VGND(i-1,i) and BL(i) are shorted and drived by same signals when Cell(i,j)-lower is selected. BL(i) and VGND(i,i +1) when Cell(i,j)-upper.The controls (Cell(i,j)-lower selected) in Fig-8-B is by NCHE write mode and PFN erase mode. Other combinations of Write and Erase modes are possible. Erase is done from WL to WL.

An example of this array is shown in Fig-9.

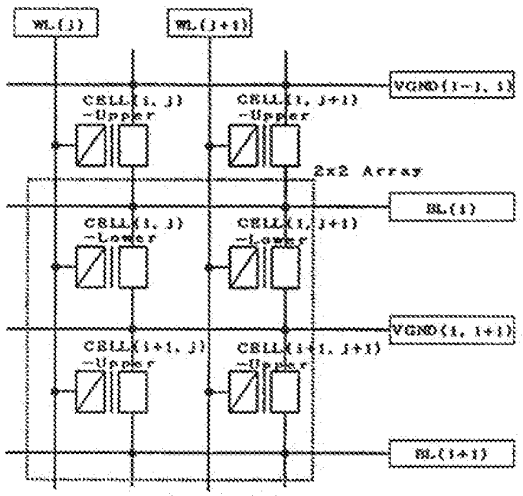


Fig-8-A : Example of EEPROM Array Circuit

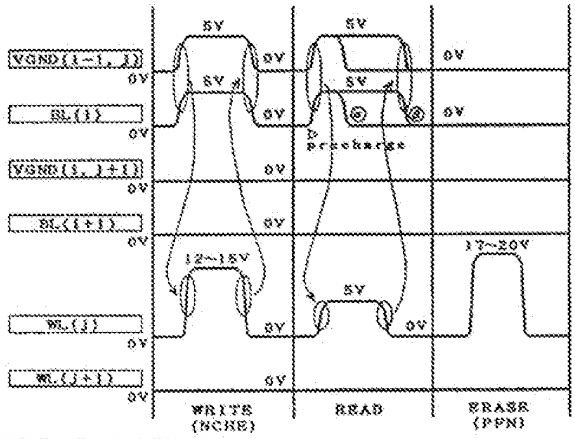
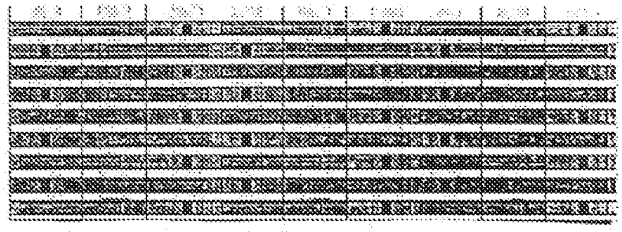


Fig-8-B : Control Signals


Fig-9 : Example of EEPROM Array

4.2. ANALOG DATA MEMORY

As shown in Fig-5-A, this EEPROM cell can store analog data by NFNwrite mode.The threshold shift is a linear function of the programming potential Vp. Precise Neural circuits are realized by this EEPROM cell structure.

ACKNOWLEDGEMENT

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A SINGLE CHIP SENSOR & IMAGE PROCESSOR FOR FINGERPRINT VERIFICATION

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ABSTRACT

This paper describes a real-time image processing system, including an image sensing array, which is implemented as a single VLSI device. The architectural overview and system performance figures demonstrate that, through efficient integration of the sensing, processing and memory elements of the image-processing system, increased performance and greatly reduced manufacturing costs can be achieved for a specific application (in this case fingerprint verification). The device, designed and fabricated using a standard 1.2µm ASIC CMOS process and 18MHz operation, includes a 258 x 258 image sensor array, real-time image normalisation and image matching circuitry, 8K bits of fast access memory and 16K bits of ROM.

INTRODUCTION

Integrated sensor-processor technology provides a new method for implementing image processing systems IPS as single chips. Typical IPS for the analysis and recognition of images conventionally consist of five main elements :- sensor, data preprocessor, image analysis hardware, memory and CPU. The input medium to this class of system is visible electromagnetic radiation which is sensed and converted into an electrical representation of the image. The sensor can be based on vidicon or solid-state CCD or MOS technology. The electrical signal usually corresponds to some standard such as PAL format video in order to simplify the interfacing to various systems, or it may simply be a raster scan read-out. A preprocessor stage then performs global functions such as spatial noise filtering, A/D conversion and image normalisation before the main image processing task is carried out. The core of the system can be either a high-performance single-chip DSP (e.g. TMS320) or, for real-time operation, an array of general purpose processors (e.g. Transputers) or dedicated image array-processors (e.g. IMS A110). Memory is required to buffer images, store reference data and results for post-analysis. The final component of a generic IPS is a low-bandwidth (when compared with the image processor) microprocessor which is needed to perform system control functions and analysis of results.

A prototype system for personal verification based on fingerprint matching which contains all the elements of such a typical image processing system, *(Figure 1)*,

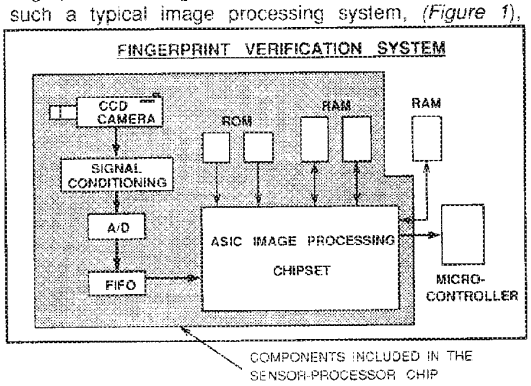


Figure 1: Block diagram of fingerprint matching system

has been developed at Edinburgh University[1]. The sensing unit used was a CCD based camera module. The preprocessing functions and the main comparison algorithm were implemented as a two device ASIC chip-set with a microcontroller performing all other system functions. The system has also been integrated as a single sensor-processor chip *(Figure 1)* as described below.

ALGORITHM

A simple optical system produces a high-contrast image of a fingerprint by utilising the total internal reflection effect of a prism. The image is focused onto the sensor which produces an analogue representation of the data. An image preprocessing stage filters and adaptively thresholds the grey scale image to produce

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a binary image ready for the matching stage. Basically the comparison is then performed as follows; to accommodate the translational and rotational movement the comparison algorithm correlates a number of reference signatures against the fingerprint over a range of angles and offsets. Matching decisions are then taken on the basis of results in this multi-dimensional correlation space. This is a reliable but computationally intensive process. To verify a fingerprint against a known reference in a time-scale of 1 second requires the equivalent of $2x10^9$ arithmetic operations per second. The results of these correlations are tabulated and compared against a specified threshold and a decision is made whether or not the fingerprint presented is a good match. The architecture used to implement the system as a single device is presented in this paper and its performance compared with that of the prototype, highlighting the advantages of integrating image sensing and processing on the same silicon substrate.

ARCHITECTURE : SENSOR

Integration of the image sensor has been made possible by the recent development of a high quality, customisable sensor array designed to be fabricated using the same standard low-cost ASIC CMOS process as is used for the surrounding digital image-processing circuitry. The sensing technology [2],[3] is based on a photodiode array and includes all necessary amplification and control circuitry on-chip. Middelhoek and Audet [4] state that one of the important disadvantages of integrated smart sensors is that the process required for the production of the sensing elements is generally not compatible with the process required for the digital circuitry. In the case of image processing we have now demonstrated that a more than adequate sensor performance is achieved without compromising the requirements for the rest of the system.

The nature of the sensor technology has allowed the sensor array to be customised to the requirements of the application. In this case a 256 x 258 array with a pixel aspect ratio of 4:3 has been chosen. Raster read out from this performs a simple spatial transform of the image to correct for optical distortion of the print image from the angled prism face. The clocking requirement is a simple single phase clock and power is provided by the same 5v supply that is used by the surrounding digital logic. The addressing and read out circuits have been modified to allow local 2-D smoothing to take place as the image data is scanned out. This is performed in the analogue domain and implements the required low-pass filtering without any hardware overhead, an example of the benefits of being able to tailor the sensor technology to the application.

ARCHITECTURE : PROCESSOR

The output signal from the sensor array is an analogue representation of the image at each pixel site. This signal is processed to give a normalised binary (i.e. black and white) representation of the fingerprint image which can then be interpreted by the digital processing logic. An adaptive threshold technique is employed to eliminate gross intensity variation across the image caused by uneven illumination of the fingerprint and variable skin characteristics. *Figure 2* shows two examples of grey-level fingerprints before and after the adaptive thresholding function has been applied. The image is divided into 256 16 x 16 pixel patches and local thresholds are calculated for each patch using a successive approximation method. The thresholds are then applied to the image to give the desired ratio of black to white pixels (usually 50%). The architecture implemented to achieve this function is described in greater detail in the next section. An off-chip 64K bit static RAM is used to store the resulting binary image. The data is then ready for correlation with the reference fingerprint data which has been pre-loaded into local memory.

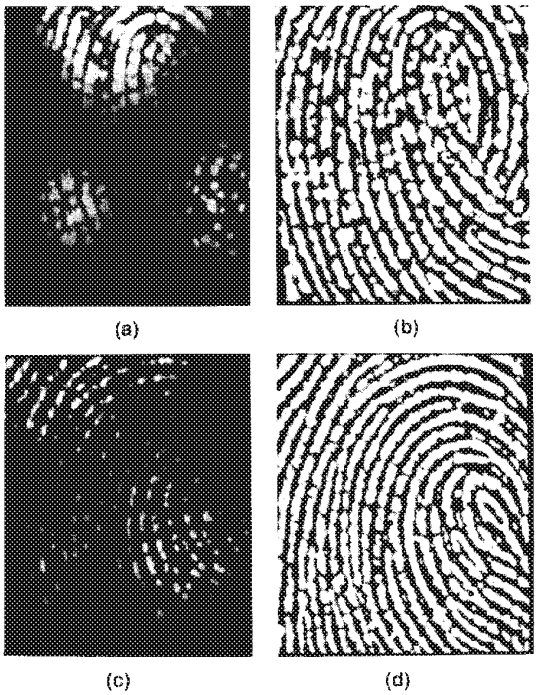


Figure 2: Grey-level fingerprint images (a),(c) Normalised binary fingerprint images (b),(d)

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The matching process is performed by an 8 x 8 matrix of correlation cells and a complex controller/address generator. The controller ensures the flow of data into the parallel correlation array is maximised to achieve the necessary high throughput. Fast on-chip memory close to the array together with pre-calculated address modifiers (to accommodate rotation of the image) allows 64 single-bit comparisons to be made on every cycle of the 18MHz system clocks. Each cell counts pixel matches and performs comparisons with locally held reference scores. At appropriate moments during the correlation sequence the current values of the 64 score registers are read and ranked in result tables for analysis after all the correlations have been completed. The final stage of the process is to analyse the ranked scores to determine whether or not the images match. Circuitry is provided on-chip to perform this function. *Table 1* provides a summary of the main features provided by the single-chip sensor processor.

PERFORMANCE

To illustrate the advantages offered by integrated sensor-processor systems, this section looks in detail at the digitisation and normalisation function of the fingerprint matching system. Assume the image size is 258 x 258 pixels and 9-bit grey-level data is required which is then to be processed to give a 256 x 256 normalised binary image.

In a typical image processing system this function would be achieved in the following manner. First the analogue signal from the sensor is digitised by a 9-bit A/D convertor to give a grey-level representation of the image. This data is then buffered in a 256 x 256 x 9-bit memory store. Assuming an adaptive threshold technique is to be employed with a patch size of 16 x 16 pixels, a local threshold is then calculated from the stored image for each patch. These are then applied to the image data and the resulting binary image is stored in memory for subsequent processing.

In principle the same function can be implemented without the need for an A/D converter or grey-level image buffer. *Figure 3* shows a simplified schematic of the image normalisation sub-system. This is achieved by reading sequence of 9 image frames during which the 9-bit local thresholds are calculated using a successive approximation technique. As the sensor array is scanned out the selected threshold is fed, via a custom DAC, to one input of a comparator while the analogue image signal is applied to the other. The output of the comparator is a binary representation of the image. The resulting digital pixel stream is analysed to determine the ratio of black and white pixels in each patch using a tally circuit. After each frame each threshold is updated according to the tally result ready for the next frame. This allows a 9-bit threshold to be calculated for each patch, 1-bit per frame, in 9 frames. A final frame is then read and the local thresholds are applied to it resulting in the required normalised binary image.

By suitable sensor addressing and sub-sampling (appropriate to this application) the calculation of the thresholds is achieved within in one frame time. This

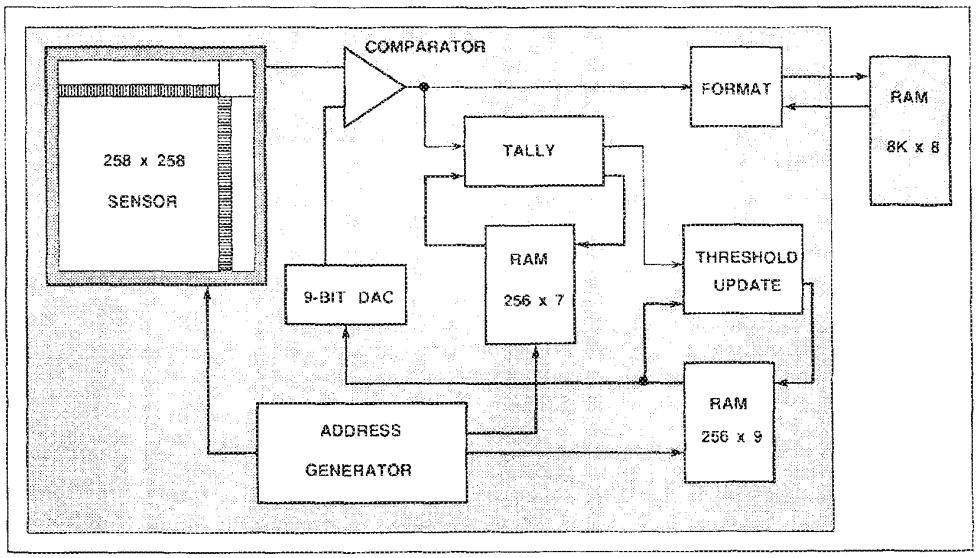


Figure 3: Block diagram of digitisation and normalisation function

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tailoring of the algorithm and hardware allows the following savings to be made :- the total RAM requirement reduces from (64K x 9 + 256 x 9 + 64K x 1) = 657,664 bits to (256 x 16 + 64K x 1) = 69,632 bits and the requirement for conversion from a 9-bit flash ADC to a simple DAC and single comparator.

IMPLEMENTATION

The development time for this device was one man year. The device is currently being prepared for fabrication at ES2 (European Silicon Structures) using a 1.2μm CMOS process. The sensor and digital image processing parts of the system have already been independently proven in silicon. The digital logic was implemented using silicon compilation software from ES2 while the full custom elements (sensor, DAC, comparator) were designed by available custom layout design tools. The chip-plot, *Figure 4*, shows clearly the standard cell format of the digital logic and the location of the sensor and memory blocks.

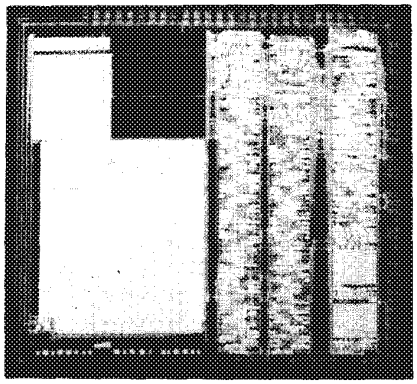


Figure 4: Integrated sensor-processor chip plot

CONCLUSIONS

The ability to integrate the sensor and processing logic as described in this paper facilitates reductions in size , from 525cm^2 to 48cm^2, and component count, from 453 to 23 for the fingerprint matching system. Other features are compared in *Table 2*. This is achieved not just through the usual leverage of integration but also by the additional factor of flexibility of choice of architecture for each component substructure in the system.

ACKNOWLEDGEMENTS

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CHIP FEATURES	
Sensor	256 x 256 CMOS Sensor
Functions	3 x 3 unary weighted smoothing filter 9-bit DAC & Comparator Module Adaptive threshold module 20 x 8-bit system registers 8 x 8 correlation cell array Rank-value filter Polling (result analysis module) Microcontroller Interface
Memory	2 x 512 x 16 SRAMs 1 x 16 x 16 SRAM 2 x 704 x 12 ROM
Physical	Package: 160-pin PGA No. Transistors: 272 000 Die size: 11.5mm x 11.5mm Power: 600mW @ 18MHz. Supply: 5v & 0V

Table 1: Integrated sensor-processor features

	ASIC BASED PROTOTYPE	INTEGRATED SYSTEM
No. VLSI / LSI devices	16	3
No. MSI devices	37	0
No. Discrete components	400 (approx.)	20
Power (Ave.)	6W@12MHz.	1W@18MHz.
Area (sub-system)	525 cm^2	48 cm^2
Response Time (typical)	1.5 secs.	0.5 secs

Table 2: Comparison of ASIC prototype and integrated sensor-processor

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A SINGLE POLY EPROM FOR CUSTOM CMOS LOGIC APPLICATIONS

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Abstract

A non volatile memory element which employs a single floating polysilicon gate is described. The cell comprises of a floating gate n-channel transistor and a control gate. The control gate is an n-well which is capacitively coupled to the floating gate. No additional process steps are required to implement this cell in an n-well CMOS technology. The single poly EPROM is programmed by channel hot carrier injection into the floating poly similar to a conventional EPROM. The cell is erased by exposure to UV light. A P^+ region is formed on a portion of the well to prevent the well-floating gate capacitor from going into deep depletion and, therefore, to enhance the gate coupling and AC response. The single poly cell is implemented in a 2Kx8 array employing standard EPROM array architecture.

Introduction

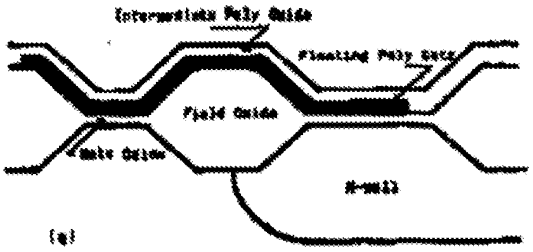
Application Specific Integrated Circuits (ASIC) have become a rapidly growing section of the semiconductor market in the past few years. The availability of EPROMs enhances the power of application specific chips to a large degree. The key point in implementing EPROM cells on custom chips is to maintain the process simplicity and, therefore, to keep the manufacturing costs low. Fabrication of conventional EPROMs usually requires two layers of polysilicon. As a result, implementation of double floating gate EPROM on custom chips complicates the process, degrades the yield, and increases the manufacturing costs.

The present paper describes a single poly EPROM as an alternative for custom CMOS logic applications. Fabrication of the single poly EPROM requires no additional processing steps in n-well CMOS process. As a simple extension of CMOS process this memory cell can be applied in a memory array, programmable logic array, or incorporated in a standard cell CMOS library.

The single poly EPROM can also be used as a redundancy element in DRAM, SRAM, and ROMs. Other applications of this cell are chip trace and trimming analog circuitry.

Cell Structure and Fabrication Technology

Cross section of the cell is shown in Figures 1(a) and 1(b). The floating polysilicon gate extends over an n-well and forms the gate coupling area. The n-well is used as the control gate during programming and read. The coupling between the control gate (n-well) and the floating gate is designed by selecting the ratio between the area of the floating gate over the n-well to the area of the floating gate over the channel.



(a)

(b)

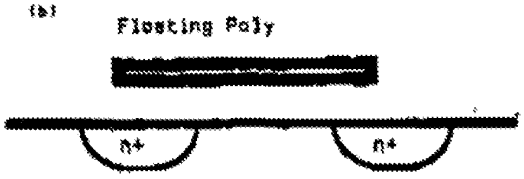


Fig. 1. The cross sections of the single poly EPROM.

A cross section of the gate coupling area is shown in Figure 2(a). In this structure, when the control gate (n-well) is pulsed high the floating poly to n-well capacitance goes into deep depletion and the gate coupling is strongly reduced. To overcome the "deep depletion" problem, a P^+ region is formed on part of the gate coupling area, as shown in Figure 2(b). The P^+ region in this structure provides a source of minority carriers (holes) which prevents the floating poly to n-well capacitance from going into deep depletion when the n-well is raised high. The layout of the cell with the addition

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of the P^+ layer is shown in Figure 3. The word line is formed by the n-well which is the control gate of the single poly EPROM. The cell area in the array is 150μ.²

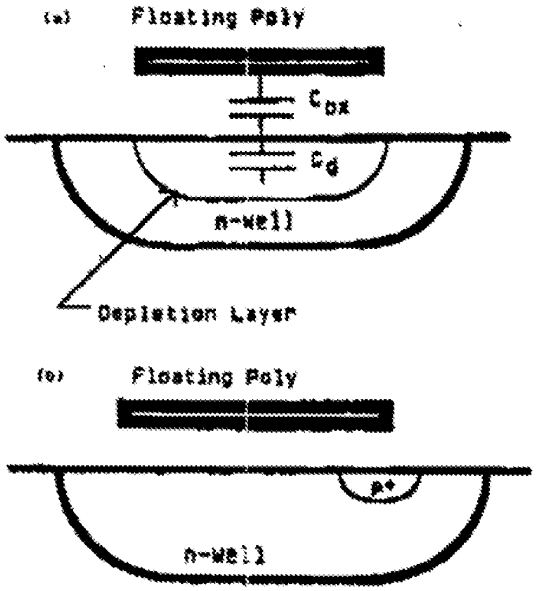


Fig. 2. Cross section of the gate area. (a) deep depletion capacitor, (b) added P^+ layer.

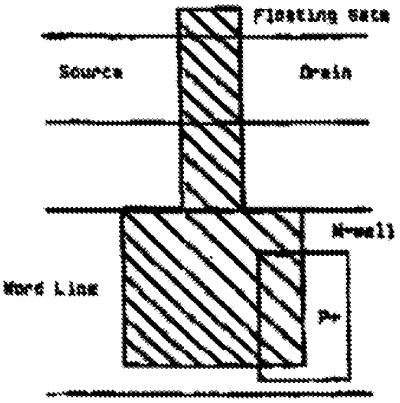


Fig. 3. Cell layout

Single poly EPROM cells are fabricated in a n-well CMOS process on P^-epi wafers. The key process features are presented in Table I. Conventional locos isolation and self aligned source/drain process are used. The single poly EPROM has the same gate oxide and source/drain junctions as NMOS devices. The gate coupling oxide is grown at the same time as the gate oxide. No additional process steps are implemented to fabricate the memory cells. The typical cell has a minimum effective channel length at 1.2μm.

TABLE I

L_{eff} (min)	NMOS	1.2μm
L_{eff} (min)	PMOS	1.2μm
L_{eff} (min)	EPROM	1.2μm
Gate Oxide	275Å	
Field Oxide	7000Å	
Intermediate Oxide	~300Å	
Junction depth	N^+	0.35μm
Junction depth	P^+	0.50μm
Junction depth	n-well	4.0μm
Typical cell size		150μm²

Performance

The I_D-V_D characteristics of the fabricated EPROM cells is shown in Figure 4. The initial threshold voltage of the cell is mainly controlled by the gate coupling. The cell read current becomes larger with increasing the effective gate coupling. The typical cell with a 1.2μm effective channel length and 36μm² gate coupling area has an initial threshold of 1.9 volts and a read current of 220μA.

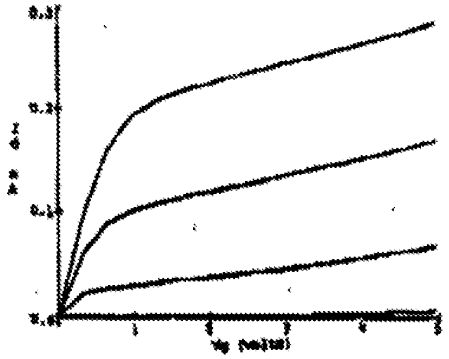


Fig. 4. Cell I_DV_D characteristics

The effect of coupling area on both I_R and V_{T1} is shown in Figure 5(a), 5(b). Initially, the I_R increases with gate coupling area as the V_{T1} decreases. Both I_R and V_{T1} become less sensitive to gate coupling as the gate area becomes large and gate coupling approaches unity. The cell read current, however, can be increased to desired level by adjusting the device width.

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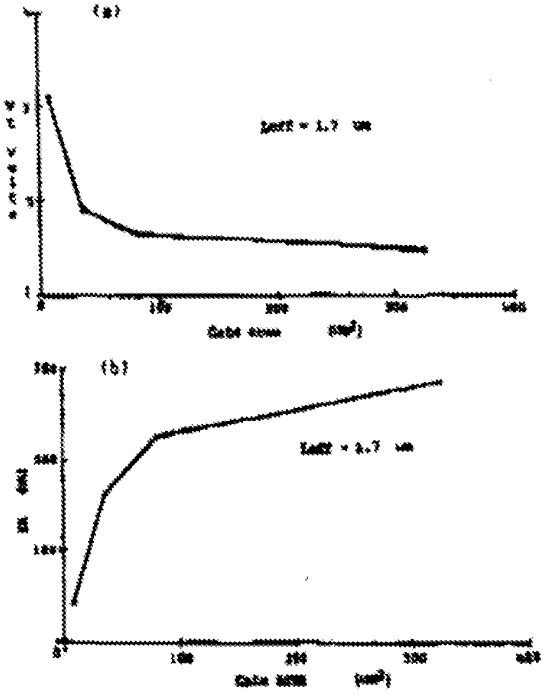


Fig. 5. Effect of gate coupling area on, (a) initial threshold voltage, (b) read current.

The single poly EPROM is programmed by channel hot carrier injection as the control gate and drain are simultaneously raised high. The programming rate is primarily controlled by the effective channel length and gate coupling. Programming characteristics of the cell is shown in Figure 6, for different channel lengths. The single poly EPROM exhibits programming speed which is comparable to conventional double poly EPROMs. For a cell programmed threshold voltage of greater than 5.5 volts, a programming pulse time of less than .10 msec is needed. The effect of gate coupling on cell programming is shown in Figure 7. The programmed threshold as a function of time is shown for different gate coupling areas. The programming rate initially increases with the gate coupling. Beyond a point, the programming rate is degraded with increasing gate coupling.

The single poly EPROM is implemented in a standard EPROM array architecture as shown in Figure 8. Array sizes of up to 2KXB are readily implemented on less than 2800 mil^2 area. To reduce word line, RC delay which is caused by large n-well resistance, a (256X32) array organization is selected.

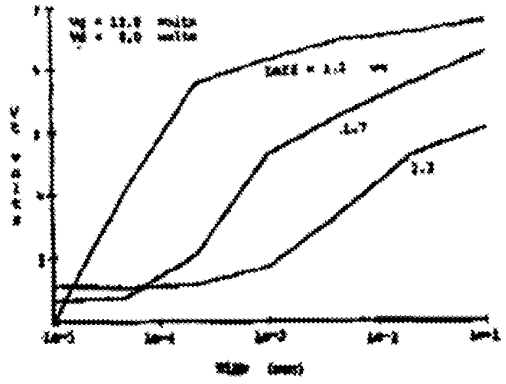


Fig. 6. The cell programming characteristics

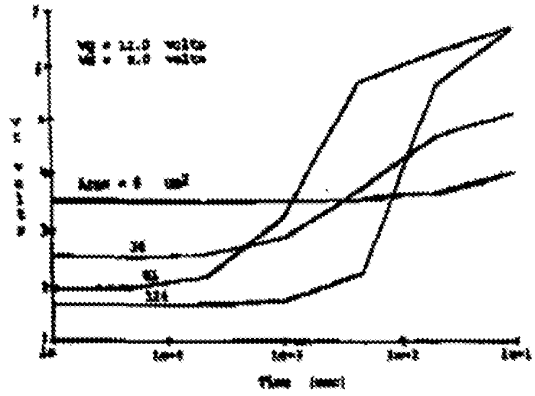
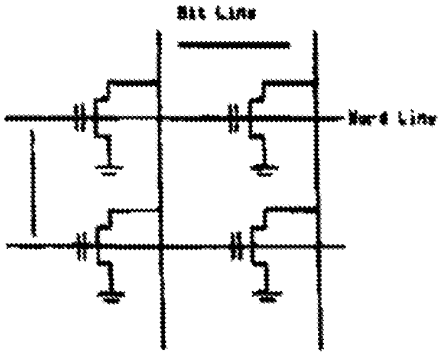


Fig. 7. The effect of gate coupling on cell programming



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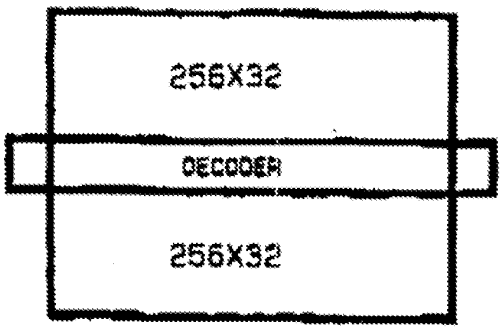


Fig. 8. Array implementation for single poly EPROM.

Reliability

Data retention characteristics of single poly EPROM cells is evaluated on single cells at three temperatures of 200, 250, and 300°C. A threshold voltage shift of less than 500 mV over a 10 year operation at 125°C (150°C for afterage) is ensured.

The single poly EPROM is erased by exposure to UV light. The erase characteristics of the cell is shown in Figure 9. The single poly EPROM is erased in less than 10 minutes which compares to conventional double poly EPROM. The UV erase rate is lower for the larger gate area. Photon injection of electrons from the edges of the polysilicon is suggested to be the dominant erase mechanism, which explains the decrease in UV erase rate as the gate area increases. (The increase in gate area results in a decrease in the ratio of gate perimeter to gate area.)

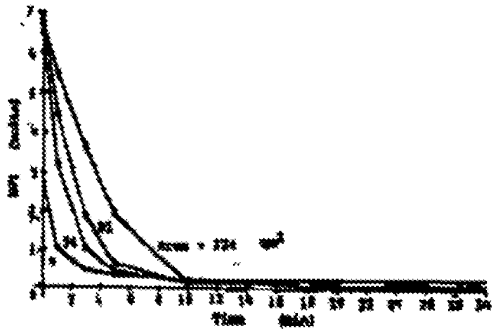


Fig. 9. UV erase characteristics of the single poly EPROM

Summary

The single poly EPROM is very attractive for custom CMOS logic applications where the cell size is traded off for process simplicity.

The memory element is successfully implemented in several CMOS technology without any additional processing steps. The cell has a high read current and a fast programming speed which is comparable to conventional double poly EPROMs. The single poly EPROM is easily implemented in standard EPROM array architecture. The charge retention and UV erase characteristics of the cell are similar to double poly EPROM. No experimental problem or reliability hazards are found to prevent use of the single poly EPROM in production.

Acknowledgement

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4.2

A Wide-Bandwidth Low-Voltage PLL for PowerPC™ Microprocessors

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Austin, Texas

Abstract

A 3.3V Phase-Locked-Loop (PLL) clock synthesizer implemented in 0.5um CMOS technology is described. The PLL supports internal to external clock frequency ratios of 1, 1.5, 2, 3, and 4 as well as numerous power down modes for PowerPC microprocessors. The processor clock lock range spans from 6-175MHz. Lock times below 15uS, PLL power dissipation below 10mW as well as phase error and jitter below +/-100pS have been measured. The total area of the PLL is 0.52 mm².

Introduction

This paper describes a fully integrated clock synthesizer analog PLL for PowerPC RISC microprocessors. A die photo of the PLL is shown in Figure 1. The PLL generates an internal processor clock with 50% duty cycle and low jitter from an external system clock (SYSCLK). The PLL supports processor to SYSCLK ratios of 1, 1.5, 2, 3, and 4 while maintaining proper edge alignment. The non-integer 1.5X mode allows the BUS and the processor to run at their maximum frequencies, 66MHz and 100 MHz respectively.

The PLL supports SYSCLK frequencies between 16.6-100MHz and does not require an accurately controlled duty cycle. The required bandwidth of the Voltage-Controlled-Oscillator (VCO) was reduced from 167MHz to 100MHz by using a novel dual-divider circuit in the feedback. The reduced bandwidth allows for a VCO with lower gain and therefore lower sensitivity to noise.

A programmable charge-pump is used in conjunction with two dividers in the feedback path to reduce the variation of damping coefficient and natural frequency. Good control of both stability parameters is critical for systems which use a board-level PLL to generate SYSCLK, as well as accurate control of lock time. This was implemented in the charge pump by decoding the divider settings and adjusting the reference current accordingly.

The PLL is shut down when the processor is in one of the power saving modes and can be restarted in less than 15uS. The on-chip RC filter allows for a fast lock-time as well as for improved reliability, lower system cost and lower clock jitter.

Functional Overview

The major functional blocks for the PLL are shown in Figure 2. A digital phase and frequency detector (PFD) designed to have minimum dead-band monitors phase as well as frequency differences between SYSCLK and the feedback clock. The PFD generates pump-down or pump-up signals when the feedback clock leads or lags SYSCLK respectively. These signals control the switched current sources in the charge pump. The output current charges or discharges the NMOS gate capacitor of the on-chip RC filter during frequency lock and produces phase correction voltage pulses during phase lock. This signal, which is the control voltage of the VCO, has a DC as well as an AC component. It is converted to an analog current and used to control the phase and frequency of the VCO. The output of the VCO is divided down by a high-speed dynamic divider (M divider) which in conjunction with a second divider (N divider) in the feedback loop sets the frequency of the processor clock. The output of the M divider circuit is buffered and distributed to the entire processor using a balanced distribution network, or HTREE, which minimizes clock skew among its several branches, one of them being the feedback path to the PLL.

The output current of the charge pump (Ip) is automatically adjusted to its proper value for different divider settings (Figure 3). Both the damping coefficient and the natural frequency of the PLL are proportional to the ratio Ip/(N*M). Therefore, to maintain the same system stability parameters for a given temperature and supply voltage, Ip is adjusted so that Ip/(N*M) is constant for varying N and M. The current reference circuit is based on diode ratios rather than fixed resistors which results in better control and a temperature coefficient that partially cancels out the one of the VCO.

The programmable delay-matching circuit is topologically equivalent to the N divider circuit. However, the signal is not divided, only delayed which guarantees that the SYSCLK and feedback clock signals have the same propagation delay to the PFD. Characterization data shows delay matching accuracy below 50pS between the two circuits.

The dual-divider topology minimizes the required VCO bandwidth, which results in lower gain and improved noise rejection. Furthermore, a narrow bandwidth requirement results in higher manufacturing yields since a larger amount of process variation can be tolerated. The required VCO bandwidth for the dual-divider PLL and for the traditional N divider and fixed prescaler PLL is presented in Table 1. For the same input frequency range the dual-divider topology requires a VCO with 99MHz less bandwidth. Table 1 also shows that the PLL can switch between 1, 2 and 4X modes without losing frequency lock since the VCO frequency is kept constant. Figure 5 shows that the dual-divider topology requires only 480ns to relock after the processor frequency is changed from 66 to 33MHz while the traditional synthesizer requires 3.7uS to relock.

The VCO consists of two synchronized, current-controlled, ring oscillators with an NMOS current source (Figure 4). A parallel current path is provided to ensure oscillation for low control voltages. A differential stage converts the output of the cross coupled rings to single ended. This circuit topology has excellent noise rejection and bandwidth, even for supply voltages less than 3V. A dedicated analog supply pin (AVDD) is provided for the VCO and charge pump to further reduce power-supply-induced clock jitter. The VCO is designed so that it's gain curve falls within the range of interest for all process corners and conditions resulting in a gain of 130MHz/V. Histograms from measured data show jitter and phase error below +/-100pS peak (Figure 6) for the 603 microprocessor (4).

* IBM

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Table 1. VCO Frequencies for Prescaler vs. Double Divider Circuits

			Prescaler			Double Divider		
mode	sysclk	f_{CPU}	N	M	f_{VCO}	N	M	f_{VCO}
1X	16.5	16.5	1	2	33	1	8	132
2X	16.5	33	2	2	66	2	4	132
4X	16.5	66	4	2	132	4	2	132
1X	33	33	1	2	66	1	4	132
1X	66	66	1	2	132	1	2	132
1X	100	100	1	2	200	1	2	200

This table shows that the dual divider PLL requires 99 MHz less VCO bandwidth than the traditional prescaler while allowing changes to the CPU/SYSCLK ratio without losing frequency lock.

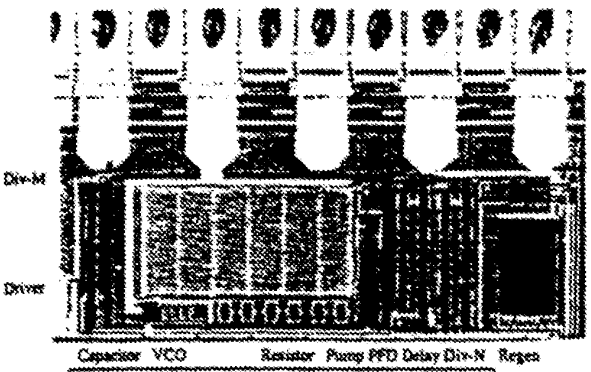


Fig. 1. Die Photo of PowerPC PLL

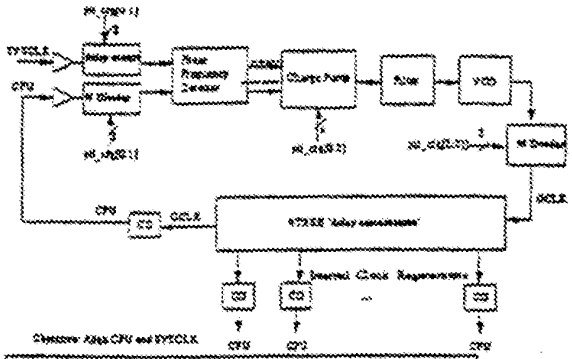


Fig. 2. Block Diagram for PowerPC PLL

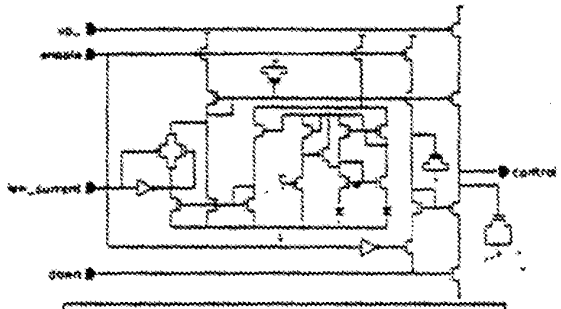


Fig. 3. Programmable Charge Pump Circuit

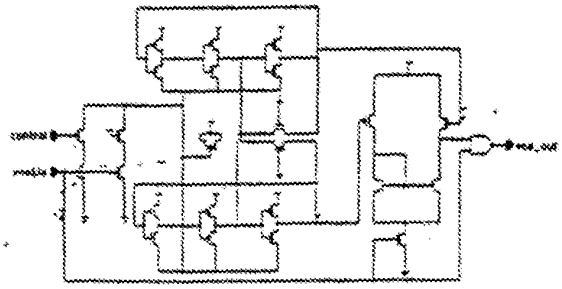


Fig. 4. Voltage-Controlled Oscillator Circuit

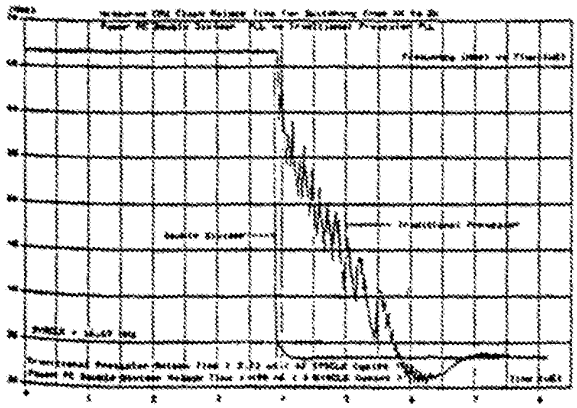


Fig. 5. Relock Time for Dual-Divider Topology vs. Prescaler

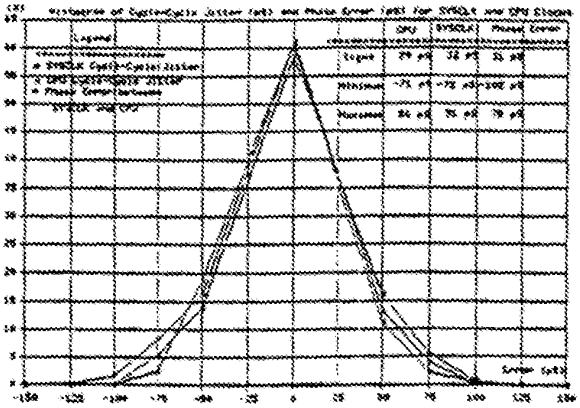


Fig. 6. Histogram for Clock Jitter, Skew, and Phase Error

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- Lithium-polymer battery charger via USB
- Battery monitor and protection circuitry

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- Battery charges automatically via USB during picture download
- Eliminates the frequent hassle and expense of battery changes

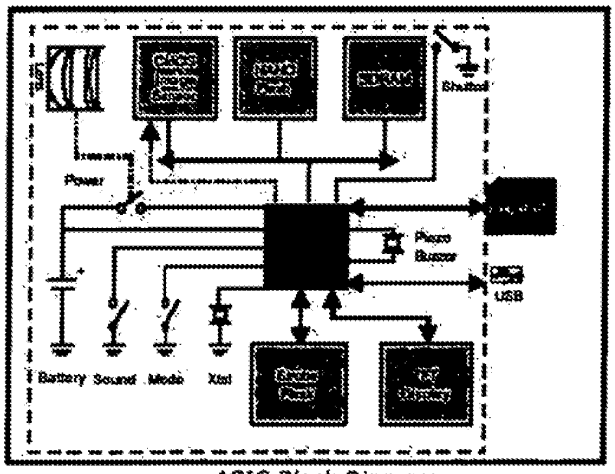
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Cameras enabled by SMaL's Ultra-Pocket 5 Kit use 1/2 to 1/3 the number of components compared to other digital cameras. In addition, the kit includes an all glass lens that has been optimized to the sensor. The combined benefits are:

- Smaller form factors, higher manufacturing yields and higher product reliability
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- Capacity: 190 mA -hr.
- Shots per charge: Ten times longer battery life than standard digital cameras with LCD and strobe on (approx. 170 images)

Taking Lens: Glass/plastic, F/3.0

Supported Operating Systems

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- TWAIN (Windows 98SE, ME, 200 XP)
- WIA (Windows XP)
- ICA (Mac OSX)

Imager

Model Number	IMG0042 3MP color CMOS image sensor with Autobrite
Active Array Format	2000 x 1500 pixels
Image Resolution Settings	High (2304 x 1768) (4MP)* Medium (2000 x 1500) (3MP) Low (800 x 600) (1MP)*
Pixel Size	3.35 µm x 3.35 µm
Pixel Type	Adaptive dynamic range photo diode
Sensor Area	6.75 mm x 5.08 mm
Intra-Scene Dynamic	

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Range	up to 120 dB with Autobrite
Optical Format	1/2-inch
Maximum Frame Rate	13 frames per second
Maximum Date Rate	70 megabytes per second at 8 bits
Supply Voltage	3.0 to 3.6V
Operating Temperature	0° to 40° C
Digital Gain	1x to 16x
Output	8 or 12-bit digital (selectable)
Shutter	Electronic rolling shutter
Correlated Double Sampling (CDS)	On-chip
Analog-to-Digital Converter (ADC)	On-chip 12-bit column parallel
Package	48-pin LCC plastic
Timing and Control	On-chip
Programmable Controls	Adaptive compression characteristics, power control, signal gain, exposure parameter

Optics

Lens	4-element glass/plastic, focal length = 8.2 mm, F/3.0 (equivalent to 44 mm lens on a 35 mm camera), FOV 54 degrees
Lens Focus	Fixed, 1.5 m (4.9 ft) to infinity

System

Exposure Control	Automatic with Autobrite and low-light-level strobe activation
Exposure Time	1/30 second to 1/10,000 second

** Higher resolution (interpolated) available based on customer request.*

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Achieving Uniform nMOS Device Power Distribution for Sub-micron ESD Reliability

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Abstract

The ESD reliability of the advanced sub-micron technologies is a major concern because of the shallow LDD junctions. This paper will show that by achieving uniform power distribution during the entire ESD event in a large multi-finger nMOS device of 0.6 μm technology, protection levels in excess of 10 kV can be realized. The evidence of this uniform power distribution resulting from the multi-finger parasitic *npn* turn-on is shown through an emission microscopy analysis.

Introduction

During the past few years, advances in integrated circuit technologies towards the sub-micron feature lengths have shown considerable impact on the electrostatic discharge (ESD) protection capability. In particular, the LDD structures introduced shallow junctions leading to higher current densities during the ESD event and hence lower failure thresholds [1][2][3]. Compounding this, the use of silicided diffusions reduced the desired ballast resistance at the drain junction. This can lead to current localization and much degraded ESD levels [4][5]. Solutions such as silicide-block through mask option [6] or LDD implant dose variations can be somewhat effective but they result in either increased cost in manufacturing or a trade-off with other reliability concerns such as hot carrier effects [7][8]. However, in this paper we will show that even for an advanced 0.6 μm CMOS technology, very effective protection levels can be achieved if uniform power dissipation is implemented into the NMOS protection design.

The design of output buffer ESD protection has been the most challenging issue with the LDD/silicide technologies. Conventionally, the nMOS output transistor itself can be used as the protection device where it operates as a parasitic bipolar *npn* transistor with the drain as the collector, the substrate as the base, and the source as the emitter. Even if a large nMOS multi-finger transistor is used as the protection device, uniform conduction of all parallel parasitic bipolar devices is difficult to achieve and hence the full protection level is never efficiently realized [9]. For improved uniform conduction, a dynamic gate-coupled device, as first reported in [10], can be used. This work will illustrate the use of this technique to achieve uniform power dissipation in a 0.6 μm technology as well as report the critical design issues for the gate coupling effect.

ESD Experiments and Results

The structures studied in this work were 0.6 μm poly gate transistors of 110 Å gate oxide. The process, similar to the one described in [11], involved a boron punch-through implant followed by a phosphorous LDD implant and arsenic source-drain implants. An nMOS device cross-section and simulated doping profiles are shown in Figures 1a and 1b. As seen, the effective junction depth is nearly 0.37 μm for this technology.

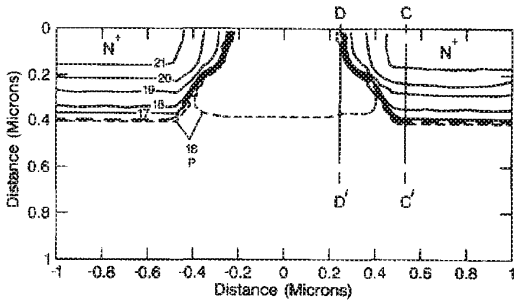
The ESD protection investigations were done on a novel gate-coupled multi-finger nMOS (GCnMOS) structure [10] schematically shown in Figure 2. The purpose of the field oxide device (FOD) is to turn off the MOSFET gate under high ESD current conditions after the nMOS gate is coupled above V_t due to the drain-gate overlap capacitance. The gate transient above V_t lowers the individual *npn* breakdown and facilitates the uniform turn-on of all fingers in a multi-finger device. This will result in a much improved ESD performance as shown below.

To demonstrate the gate-coupling effect, a monitor device, as shown in Figure 3, was built into the silicon test structure. A constant current source and a 510 Ω resistor were connected to the terminals of the monitor device. When a large pulse is applied at V_{PAD}, the gate coupling should change the conduction state of the monitor device. This is illustrated in Figure 4 where the oscilloscope traces for V_{PAD} and the drain-source voltage of the monitor device are shown for a single 1.0 μs pulse applied to the V_{PAD}. As the pad voltage increases, the coupled gate causes the effective resistance seen by the constant current source to drop, thus decreasing the measured V_{dsm}. It should be noted here that the protection nMOS is expected to go through MOS and parasitic bipolar current conduction, while the monitor device will only carry MOS current.

The gate coupling under ESD Human Body Model (HBM) was estimated by circuit simulation [12] of the structure depicted in Figure 3. The simulation results corresponding to a 5 kV ESD-HBM event are shown in Figure 5. The pad voltage reaches a maximum of about 25 V at 10 ns and then, with the decay of the stress

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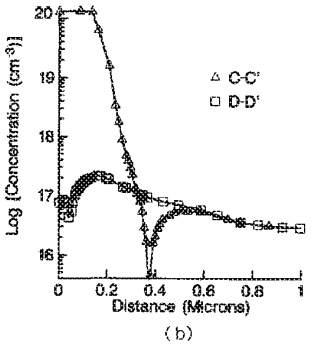


Fig. 1. (a) Cross section of an nMOS device with concentration contours given in $\log_{10}$ (atoms/cm^3); (b) doping profiles along the views indicated in (a).

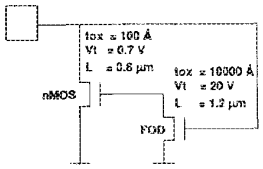


Fig. 2. Circuit Schematic of a typical GCnMOS structure.

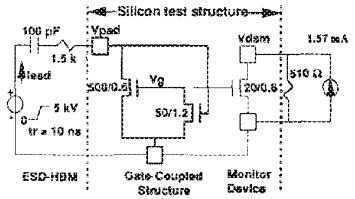


Fig. 3. Equivalent circuit used for circuit simulation of a GCnMOS structure with a built-in monitor device.

current (I_{ESD}), it approaches approximately 10 V corresponding to the bipolar snapback voltage. At the same time, the drain potential of the monitor device goes through a minimum corresponding to peak gate coupling, and slowly increases as the gate discharges. It should be noted here that with the pad voltage going beyond 20 V, the FOD in Figure 2 turns on to control

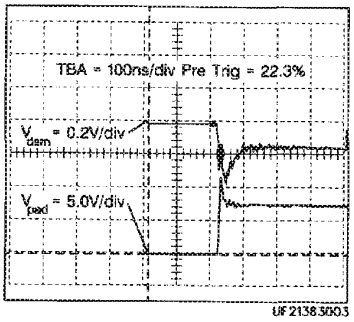


Fig. 4. Measured voltage responses to a square pulse applied to V_{PAD} for a GCnMOS structure with monitor device connected as in Fig. 3.

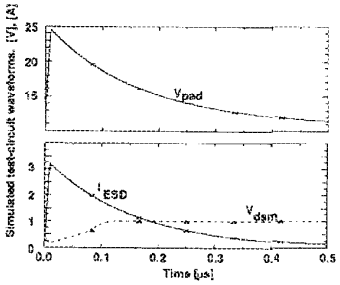


Fig. 5. Simulated waveforms for the equivalent circuit shown above in Figure 3 under a 5 kV ESD-HBM event.

the nMOS gate time constant. By matching the simulated waveforms with the measurements, we confirmed that the nMOS gate indeed goes above V_t for ESD events. This should result in optimum ESD performance as mentioned above.

Several GCnMOS structures with varying layout parameters were subjected to ESD-HBM and Machine Model (MM) stress. It was found that the drain-contact to gate space (DGS) is an important parameter that increases the ballast resistance for each finger which, in turn, allows the quick trigger of all *npn* fingers in only a few nanoseconds. The measured minimum and maximum ESD-HBM failure thresholds as a function of DGS are shown in Figure 6 for 500 µm wide devices. The data corresponds to a subset of 40 GCnMOS structures. Circuit simulation results of the gate transient for the various values of DGS considered are shown in Figure 7. Note that although the gate on-time in Figure 7 is about 4 ns for all four cases, Figure 6 indicates that a tight ESD-HBM failure level distribution is attained as DGS increases. It is likely that not all the fingers participate in the ESD event for low DGS values. To understand this, the measured breakdown I-V characteristics with square-wave current pulses are shown in Figure 8. It can be seen that the gate-coupling lowers the drain avalanche

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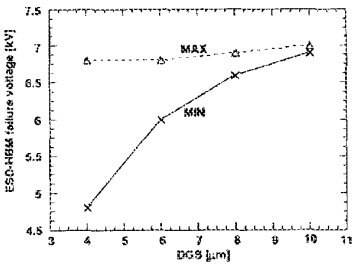


Fig. 6. Measured minimum and maximum ESD-HBM failure thresholds for 500 μm wide GCnMOS devices.

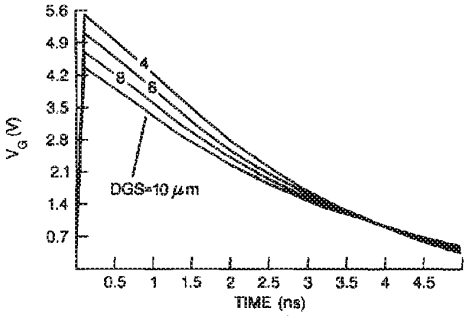


Fig. 7. Simulated gate transient of a GCnMOS device with 500 μm/0.6 μm nMOS and 50 μm/1.2 μm FOD.

close to the snapback voltage. After the first *npn* snapback, a larger DGS with higher resistance allows more of the fingers to rapidly turn on within the rise time of a typical ESD event (5–10 ns). On the other hand, this analysis also indicates that for smaller DGS values, a longer on-time is required which in turn can be controlled by the field oxide device size. Thus DGS is an important layout parameter that involves the proper gate transient design. In contrast to the GCnMOS, a grounded gate nMOS (GGnMOS), also shown in Figure 8, has to go through large voltage excursions to turn each subsequent finger. In most cases the GGnMOS reaches a failure point before even two or three fingers turn on.

The uniform power distribution in these devices was studied using emission microscopy (EMMI) [13]. First, the EMMI photograph for a 1.8 μm LDD technology GGnMOS is shown in Figure 9a. The device was being stressed with 250 ns current pulses of 500 mA. In the 0.6 μm technology, Figure 9b shows the emission photograph obtained from a GGnMOS device being stressed with 450 mA current pulses. In both cases, only one finger "locks-on" which can lead to failure corresponding to a single finger device. In some cases of the 0.6 μm technology, however, 2 or 3 fingers were seen to turn on but this was always a random event. The GCnMOS device emission results are shown in Figure 10. As the current level was increased from Figure 10a (100 mA) to

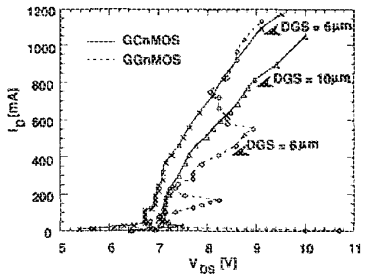


Fig. 8. Measured I-V breakdown characteristics.

Figure 10c (500 mA), more and more fingers turn on until all eight fingers participate in the event. It is important to note that, unlike the GGnMOS case, lock-on with a single finger dominating does not occur. Even in a sixteen finger device all of the fingers can participate as shown in Figure 10d. This sixteen finger device has shown an ESD failure level of 13 kV or 13 V/μm for this 0.6 μm technology. Thus, the emission results clearly illustrate that uniform power distribution can be achieved with optimum gate coupling. A floating gate device without the field oxide device was also studied under EMMI at the same current levels. No emission was observed indicating that the nMOS device conduction dominates in this case.

Conclusions

This paper demonstrated the effect of dynamic gate coupling for sub-micron ESD protection structures and the impact it has in obtaining more than 10kV of ESD-HBM performance. It was shown that the optimum gate transient is a critical function of the nMOS protection device layout parameters. Using emission microscopy, this work also has demonstrated that for sub-micron technologies excellent ESD levels can be obtained when uniform power distribution is achieved through gate-coupling in a multi-finger nMOS device. For future technologies thus harnessing the maximum available *npn* protection can become a key ESD reliability advantage.

Acknowledgements

We are grateful to Drs. Tom Holloway, Ping Yang, and Bill Hunter for valuable discussions and comments.

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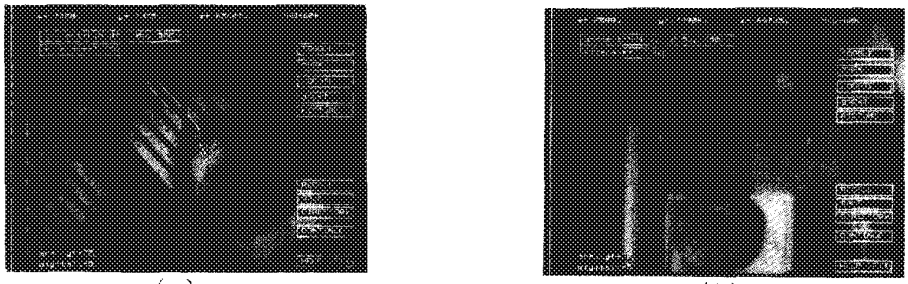


Fig. 9. EMMI photographs of GGnMOS devices in the (a) 1.2 μm technology at 500 mA stress current level and (b) 0.6 μm technology at 450 mA stress current level.

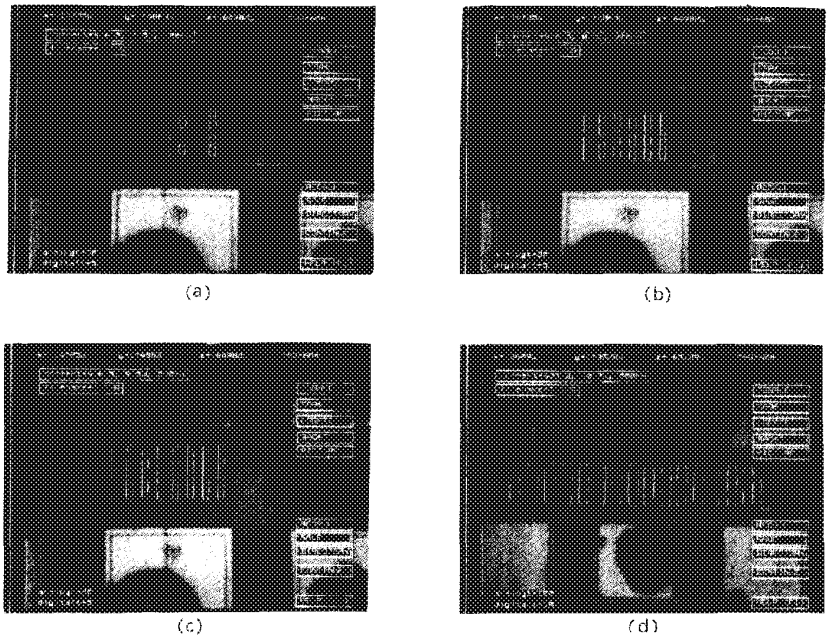


Fig. 10. EMMI photographs of GCnMOS devices in the 0.6 μm technology: (a), (b), and (c) are for a 500 μm device being stressed with 100 mA, 300 mA, and 500 mA current pulses, respectively; (d) shows a 1000 μm device subjected to 300 mA current pulse.

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11. R. Chapman, et al., "0.5 micron CMOS for high performance at 3.3V," IEEE IEDM Tech. Digest, 1988.
12. C. Diaz and S. Kang, "New algorithms for circuit simulation of device breakdown," to be published in IEEE trans. on CAD.
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ADNS-2030 · High-performance, Low Power Optical Mouse Sensor (Optimized for Cordless Mouse Applications)

For purchase and selection assistance:
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The ADNS-2030 is a low power reflective optical sensor that provides a non-mechanical tracking engine for implementing a computer-pointing device. It is based on optical navigation technology which measures changes in position by optically acquiring sequential surface images up to 2300 times per second and mathematically determining the direction and magnitude of movement at the maximum of 800 counts per inch (cpi) and at speeds up to 14 inches per second (ips). Agilent provides samples of the complete optical mouse tracking engine kit (Part #ADNK-2030). The CMOS based sensor is mounted in a 16-pin staggered dual inline package (DIP)and designed for use with the HDNS-2200 LED Assembly Clip)and HLMP-ED80 (639 nm LED illumination source)and HDNS-2100(lens).

With its low power feature, this optical mouse sensor enables longer battery life and more efficient power consumption. This eliminates the need for a recharger and making it an ideal choice for cordless optical mouse application.

More Details
- Technical Support
- Library
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Other Links
- Parametric Search
- Cross Reference
- Samples
- Order Information

Features

- Optical navigation technology
- No mechanical moving parts
- High reliability
- Complete 2-D motion sensor
- High speed motion detector
- No precision optical alignment
- Wave solderable
- Single 3.3 volt power supply
- Shutdown pin for USB suspend mode operation
- Power conservation mode during times of no movement
- On chip LED drive with regulated current
- Serial port registers

Application

- Cordless optical mice
- Mice for desktop PCs, workstations, and portable PCs
- Trackballs
- Integrated input devices

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Data Sheet: ADNK-2030: Solid State Optical 2003-03-10 115 KB

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Mouse Sensor Sample Kit One page Sample Kit for ADNK-2030 Solid State Optical Mouse Sensor			
Data Sheet: **ADNS-2030: Optical Mouse Sensor Product Overview** ADNS 2030 Optical Mouse Product Overview	2003-03-10	126 KB	
Data Sheet: **ADNS-2030: Low Power Optical Mouse Sensor** Data Sheet	2005-05-11	450 KB	
Selection Guide: **Optical Navigation Sensors** Agilent Optical Navigation Sensors Selection Guide	2004-11-03	42 KB	
White Paper: **Optical Mice and how they Work**	2001-11-05	205 KB	

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ADNS-2051 · High-performance Optical Mouse Sensor

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The ADNS-2051 is a low cost optical sensor used to implement a non-mechanical tracking engine for computer mice. It is based on optical navigation technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. The sensor is in a 16 pin staggered dual inline package (DIP) that is designed to be used with the HDNS-2100 Lens and HDNS-2200 Clip. These parts provide a complete and compact mouse sensor. There are no moving parts, and compact mouse sensor. There are no moving parts, and precision optical alignment is not required, facilitating high volume assembly. The output format is two channel quadrature (X and Y direction) which emulated encoder phototransistors. The current X and Y information are also available in registers accessed via a serial port. Default resoultion is specified as 400 counts per inch, with rates of motion up to 14 inches per second. Resolution can also be programmed to 800 cpi. The part is programmed via a two wire serial port, via registers.

More Details
- Technical Support
- Library
- Alliances & Channel Partners

Other Links
- Parametric Search
- Cross Reference
- Samples
- Order Information

Features

- Optical navigation technology
- No mechanical moving parts
- High reliability
- Complete 2-D motion sensor
- High speed motion detector
- No precision optical alignment
- Wave solderable
- Single 5.0 volt power supply
- Shutdown pin for USB suspend mode operation
- Power conservation mode during times of no movement
- On chip LED drive with regulated current
- Serial port registers

Application

- Mice for desktop PCs, workstations, and portable PCs
- Trackballs
- Integrated input devices

Key Library Information

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Data Sheet: **ADNK-2052: Solid State Optical Mouse Sensor Sample Kit**	2003-04-08	115 KB
Data Sheet: **ADNS-2051: Optical Mouse Sensor Datasheet**	2004-10-08	296 KB

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Data Sheet: **ADNS 2051: Optical Mouse Sensor Product Overview** Product overview for ADNS-2051 Optical Mouse Sensor	2003-03-31	127 KB
Selection Guide: **Optical Navigation Sensors** Agilent Optical Navigation Sensors Selection Guide	2004-11-03	42 KB
White Paper: **Optical Mice and how they Work**	2001-11-05	205 KB

Related Information

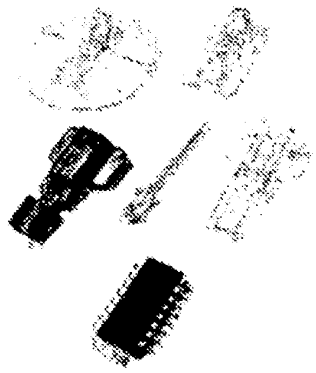
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Agilent ADNK-2030
Solid-State Optical Mouse Sensor
Sample Kit



Part Number	Description	Name	Quantity
ADNS-2030	Solid-State Optical Mouse Sensor	Sensor	5
HDNS-2100	Lens Plate (Round Lens)	Lens	5
HDNS-2100#001	Lens Plate (Trimmed Lens)	Lens	5
HDNS-2200	LED Assembly Clip (Black Clip)	LED Clip	5
HDNS-2200#001	LED Assembly Clip (Clear Clip)	LED Clip	5
HLMP-ED80-XXXXX	639 nm T 1 3/4 (5 mm) Diameter LED	LED	5
Documentation	ADNS-2030 Data Sheet	—	1
Documentation	HDNS-2100/HDNS-2100#001 Data Sheet	—	1
Documentation	HDNS-2200/HDNS-2200#001	—	1
Documentation	HLMP-ED80-XXXXX LED Data Sheet	—	1
Floppy Diskette	Base Plate Feature IGES File	—	1

Kit Components
See table below.

Sensor
The sensor technical information is contained in the ADNS-2030 Data Sheet.

Lens
The lens information is contained in the HDNS-2100/HDNS-2100#001 Data Sheet.

LED Assembly Clip
The assembly information is contained in the HDNS-2200/HDNS-2200#001 Technical Data Sheet.

LED
Information on the LED is contained in the HLMP-ED80-XXXXX Data Sheet.

Base Plate Feature IGES File
The IGES file provides recommended base plate molding features to ensure optical alignment.

www.agilent.com/semiconductors
For product information and a complete list of distributors, please go to our web site.

For technical assistance call:

Americas/Canada: +1 (800) 235-0312 or (408) 654-8675

Europe: +49 (0) 6441 92460

China: 10800 650 0017

Hong Kong: (+65) 6271 2451

India, Australia, New Zealand: (+65) 6271 2394

Japan: (+81 3) 3335-8152(Domestic/International), or 0120-61-1280(Domestic Only)

Korea: (+65) 6271 2194

Malaysia, Singapore: (+65) 6271 2054

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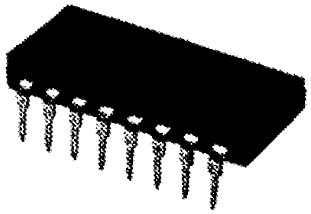
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Agilent ADNS-2030 Low Power Optical Mouse Sensor

Data Sheet



Description

The ADNS-2030 is a low-power optical mouse sensor used to implement a non-mechanical tracking engine for computer mice. With a 3.3V power supply and power-saving sleep functions, this sensor is particularly suited to cordless mouse applications.

It is based on optical navigation technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The sensor is housed in a 16-pin staggered dual inline package (DIP) that is designed for use with the HDNS-2100 Lens and HDNS-2200 Clip and HLMP-ED80-xx000 (639 nm LED illuminator source). There are no moving parts, and precision optical alignment is not required, facilitating high volume assembly.

The output format is two channel quadrature (X and Y direction) which emulates encoder photo-transistors. The current X and Y information are also available in registers accessed via a serial port.

Default resolution is specified as 400 counts per inch, with rates of motion up to 14 inches per second. Resolution can also be programmed to 800 cpi.

The part is programmed via a two wire serial port, through registers.

Theory of Operation

The ADNS-2030 is based on Optical Navigation Technology. It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP) and a two channel quadrature output, and a two wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system provided by the HDNS-2100, 2200, and HLMP-ED80-xx000. These images are processed by the DSP to determine the direction and distance of motion. The DSP generates the Δx and Δy relative displacement values that are converted to two channel quadrature signals.

Features

- Precise optical navigation technology
- No mechanical moving parts
- Complete 2D motion sensor
- Serial interface and/or quadrature interface
- Smooth surface navigation
- Programmable frame speed up to 2300 frames per sec (fps)
- Accurate motion up to 14 ips
- 800 cpi resolution
- High reliability
- High speed motion detector
- Wave solderable
- Single 3.3 volt power supply
- Shutdown pin for USB suspend mode operation
- Power conservation mode during times of no movement
- On chip LED drive with regulated current
- Serial port registers
  - Programming
  - Data transfer
- 16-pin staggered dual inline package (DIP)

Applications

- Cordless optical mice
- Mice for desktop PCs, workstations, and portable PCs
- Trackballs
- Integrated input devices

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Pinout of ADNS-2030 Optical Mouse Sensor

Pin Number	Pin	Description
1	SCLK	Serial port clock (input)
2	XA	XA quadrature output
3	XB	XB quadrature output
4	YB	YB quadrature output
5	YA	YA quadrature output
6	XY_LED	LED control
7	REFA	Internal reference
8	REFB	Internal reference
9	OSC_IN	Oscillator input
10	GND	System ground
11	OSC_OUT	Oscillator output
12	GND	System Ground
13	V_{DD}	3.3 volt power supply
14	R_BIN	LED current bin resistor
15	PD	Power Down Pin, active high
16	SDIO	Serial data (input and output)

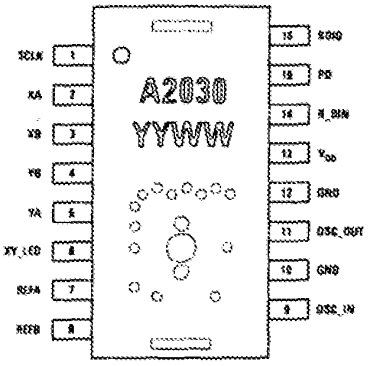


Figure 1. Top view.

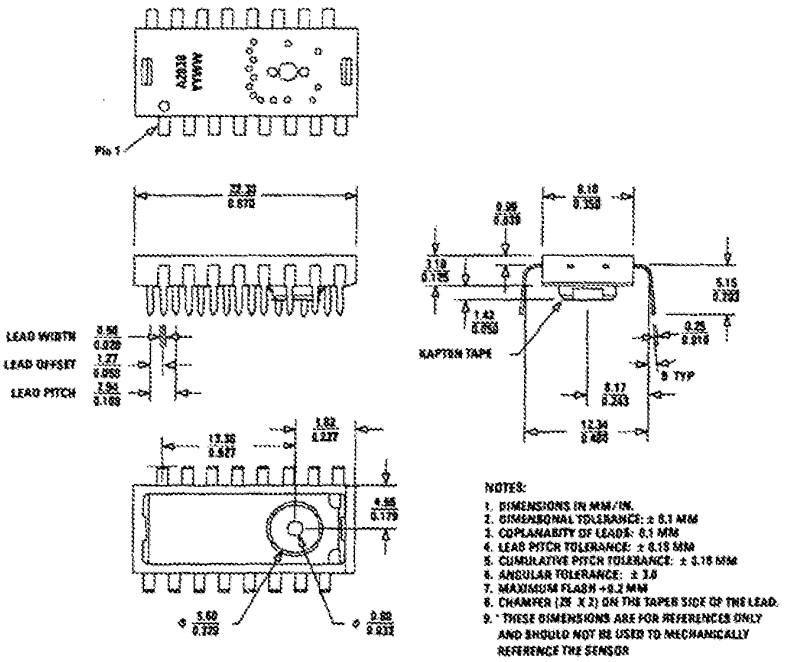


Figure 2. Package outline drawing of ADNS-2030 optical mouse sensor.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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Overview of Optical Mouse Sensor Assembly

2D Assembly Drawing of ADNS-2030

Figures 3 and 4, shown with HDNS-2100, HDNS-2200 and HLMP-ED80-xx000.

Agilent Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment

These components interlock as they are mounted onto defined features on the base plate.

The ADNS-2030 sensor is designed for mounting on a through hole PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The HDNS-2100 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor, base plate, and clip with the LED. The lens also has a large round flange to provide a long creepage path for any ESD events that occur at the opening of the base plate.

The HDNS-2200 clip holds the LED in relation to the lens. The LED must be inserted into the clip and the LED's leads formed prior to loading on the PCB. The clip interlocks the sensor to the lens, and through the lens to the alignment features on the base plate.

The HLMP-ED80-xx000 LED is recommended for illumination. If used with the bin table, sufficient illumination can be guaranteed.

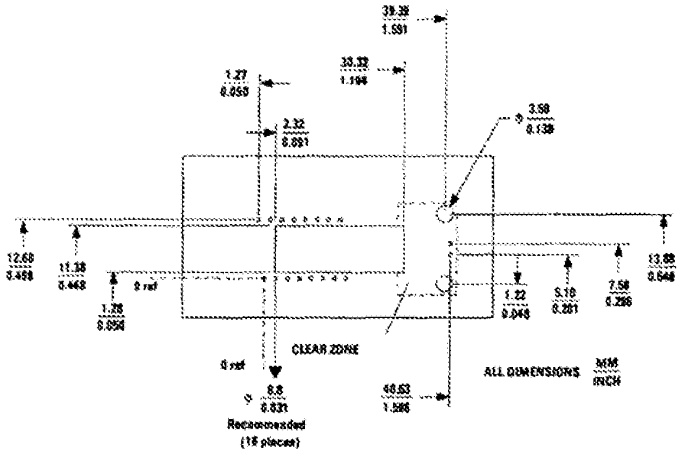


Figure 3. Recommended PCB mechanical cutouts and spacing (top view).

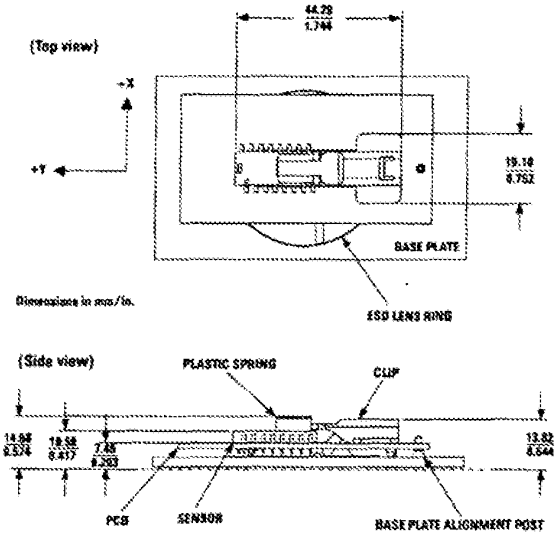


Figure 4. 2D assembly drawing of ADNS-2030 (top and side view).

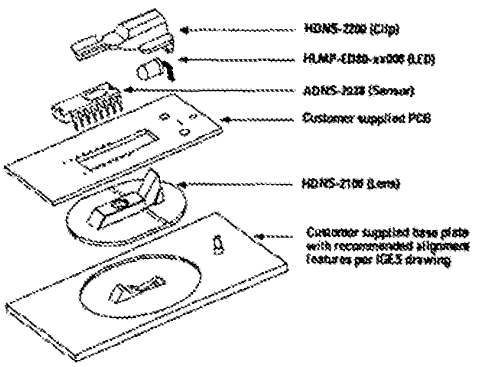


Figure 5. Exploded view drawing.

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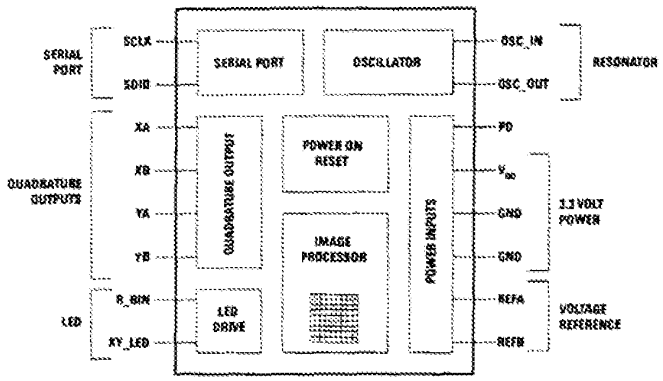


Figure 6. Block diagram of ADNS-2030 optical mouse sensor.

PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB.
2. Bend the LED leads 90° and then insert the LED into the assembly clip until the snap feature locks the LED base.
3. Insert the LED/clip assembly into PCB.
4. Wave Solder the entire assembly in a no-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact. The solder fixture is also used to set the reference height of the sensor to the PCB top during wave soldering (Note: DO NOT remove the kapton tape during wave soldering).
5. Place the lens onto the base plate.
6. Remove the protective kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. It is recommended not to place the PCB facing up during the entire mouse assembly process. The PCB should be held vertically during the kapton removal process.
7. Insert PCB assembly over the lens onto the base plate aligning post. The sensor aperture ring should self-align to the lens.
8. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
9. Install mouse top case. There must be a feature in the top case to press down onto the clip to ensure all components are interlocked to the correct vertical height.

Design Considerations for Improving ESD Performance

The flange on the lens has been designed to increase the creepage and clearance distance for electrostatic discharge. The table below shows typical values assuming base plate construction per the Agilent supplied IGES file and HDNS-2100 lens flange.

Typical Distance	Millimeters
Creepage	16.0
Clearance	2.1

For improved ESD performance, the lens flange can be sealed (i.e. glued) to the base plate. Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should **NOT** be used.

Note: It is recommended to submit all application designs including changes to form, fit or function for ESD spec compliance.

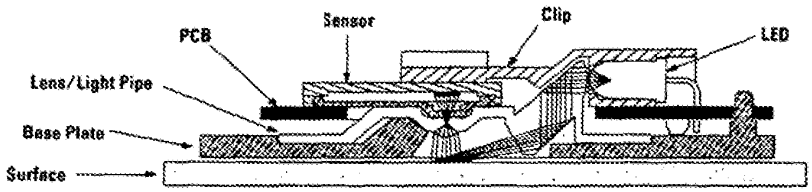


Figure 7. PCB assembly.

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Recommended Typical Application (Receiver side)

Recommended Typical Application (Transmitter side)

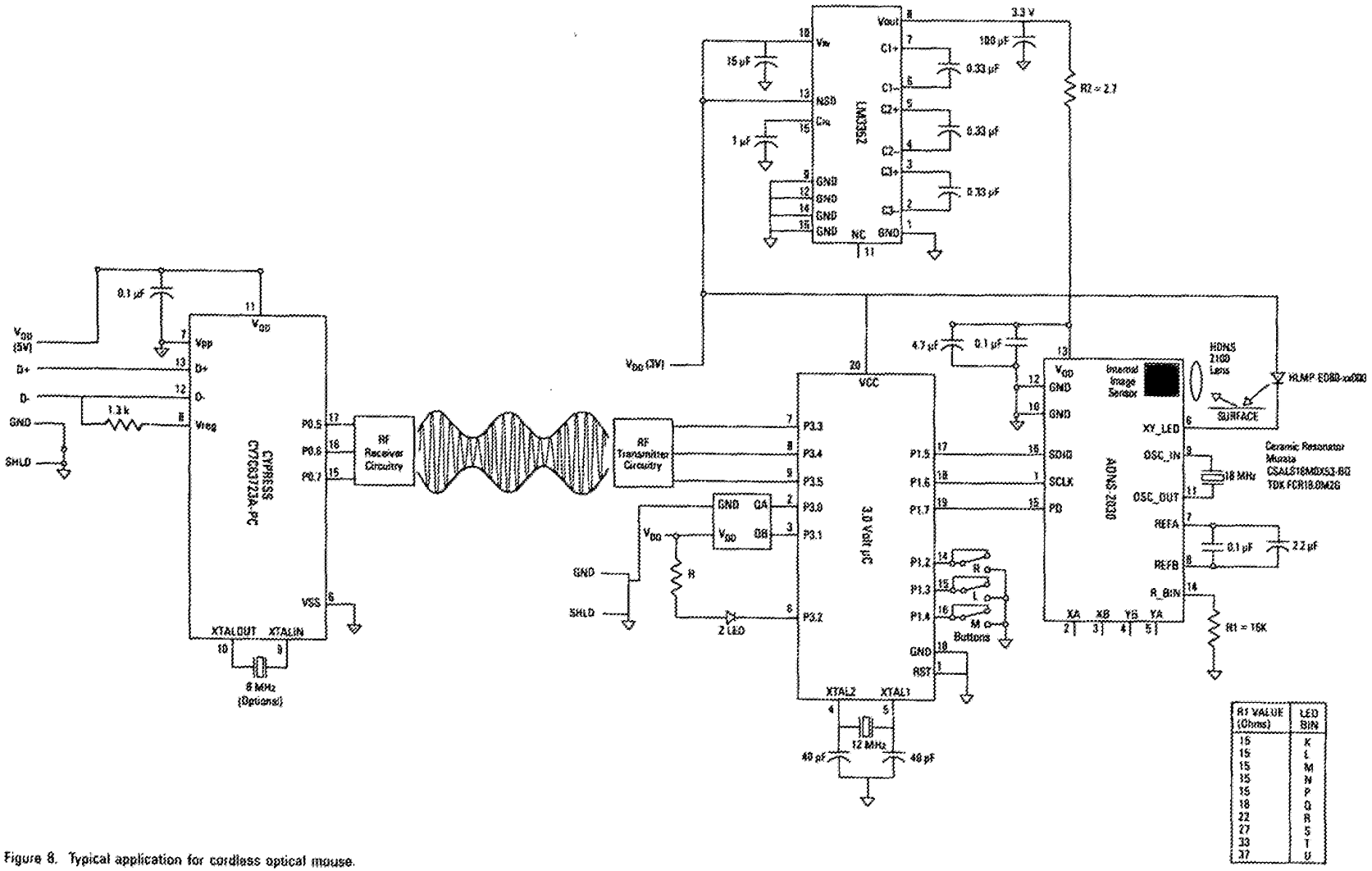


Figure 8. Typical application for cordless optical mouse.

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Notes on Bypass Capacitors

- Caps for pins 7, 8 and 12, 13 *MUST* have trace lengths *LESS* than 5 mm.
- The 0.1 µF caps must be ceramic.
- Caps should have less than 5 nH of self inductance.
- Caps should have less than 0.2Ω of ESR.
- Surface mount parts are recommended.

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with unshielded cable and following Agilent recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with unshielded cable and following Agilent recommendations.
- UL flammability level UL94 V-0.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15kV when assembled into a mouse according to usage instructions above.
- For eye safety consideration, please refer to the document, Eye Safety Calculation AN1228 available on the web site, http://www.agilent.com/view/opticalnavigation.
- The 15.0 kΩ resistor is determined by the absolute maximum rating of 50 mA for the HLMP-ED80-xx000. The other resistor values for brighter bins will guarantee sufficient intensity with reduced power.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_A	-15	55	°C	
Lead Solder Temp			260	°C	For 10 seconds, 1.6 mm below seating plane
Supply Voltage	V_{DD}	-0.5	3.6	V	
ESD			2	KV	All pins, human body model MIL 883 Method 3015
Input Voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	All I/O pins

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Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	Volts	
Power Supply Rise Time	V_{RT}			100	ms	
Supply Noise	V_N			30	mV	Peak to peak @27 MHz bandwidth
Clock Frequency	f_{CLK}	17.4	18.0	18.7	MHz	Set by ceramic resonator
Serial Port Clock Frequency	SCLK			$f_{CLK}/4$	MHz	
Resonator Impedance	X_{RES}			55	Ω	
Distance from Lens Reference Plane to Surface	Z	2.3	2.4	2.5	mm	Results in ±0.2 mm DOF (See Figure 9.)
Speed	S	0		14	in/sec	@ frame rate = 1500 fps
Acceleration	A			0.15	g	@ frame rate = 1500 fps
Light Level onto IC	IRR_{INC}	80 100		25,000 30,000	mW/m^2	λ = 639 nm λ = 875 nm
SDIO Read Hold Time	t_{HOLD}	100			µs	Hold time for valid data (Refer to Figure 27.)
SDIO Serial Write-write Time	t_{SWW}	100			µs	Time between two write commands (Refer to Figure 30.)
SDIO Serial Write-read Time	t_{SWR}	100			µs	Time between write and read operation (Refer to Figure 31.)
SDIO Serial Read-write Time	t_{SRW}	120			ns	Time between read and write operation (Refer to Figure 32.)
SDIO Serial Read-read Time	t_{SRR}	120			ns	Time between two read commands (Refer to Figure 32.)
Data Delay after PD ↓	$t_{COMPUTE}$	3.2			ms	After $t_{COMPUTE}$, all registers contain data from first image after PD↓. Note that an additional 75 frames for AGC stabilization may be required if mouse movement occurred while PD was high. (Refer to Figure 11.)
SDIO Write Setup Time	t_{SETUP}	60			ns	Data valid time before the rising of SCLK (Refer to Figure 25.)
PD Pulse Width (to power down the chip)	t_{PDW}	700			µs	Pulse width to initiate the power down cycle @1500 fps (Refer to Figure 13.)
PD Pulse Width (to reset the serial port)	t_{PD}	100			µs	Pulse width to reset the serial port @1500 fps (but may also initiate a power down cycle) (Refer to Figure 11.)
Frame Rate	FR		1500		frames/s	See Frame_Period register section
Bin Resistor	R1	15K	15K	37K	Ω	Refer to Figure 8

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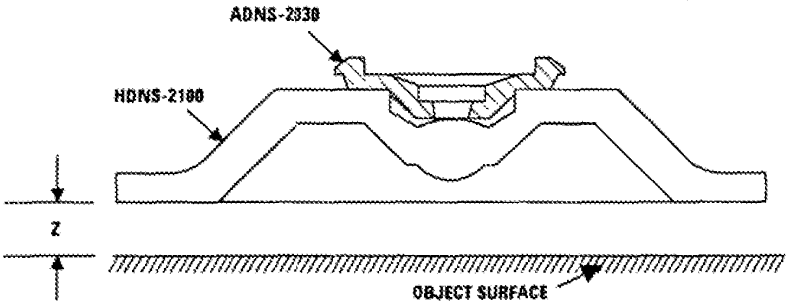


Figure 9. Distance from lens reference plane to surface.

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 3.3 V, 18 MHz, 1500 fps.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Power Down	t_{PD}		700		µs	From PD↑ Time uncertainty due to firmware delay (Refer to Figure 11).
Power Up from PD↓	t_{PUPD}			50	ms	From PD↓ to valid quad signals 785 µsec + 75 frames (Refer to Figure 11).
PowerUp from V_{DD} ↑	t_{PU}			30	ms	From V_{DD}↑ to valid quad signals 785 µsec + 40 frames
Rise and Fall Times						
SDIO	t_r		15		ns	C_L = 30 pF (the rise time is between 10% to 90%)
	t_f		12		ns	C_L = 30 pF (the fall time is between 10% to 90%)
XA, XB, YA, YB	t_r		30		ns	C_L = 30 pF (the rise time is between 10% to 90%)
	t_f		22		ns	C_L = 30 pF (the fall time is between 10% to 90%)
ILED between	t_r		35		ns	With HLMP-ED80-xx000 LED (the rise time is 10% to 90%).
between	t_f		170		ns	With HLMP-ED80-xx000 LED (the fall time is 10% to 90%).
Serial Port Transaction Timer	t_{SPTT}	0.7	0.9	1.0	s	Serial port will reset if current transaction is not complete within t_{SPTT} (Refer to Figure 35).
Transient Supply Current	I_{DDT}		18	37	mA	Max supply current during a V_{DD} ramp from 0 to 3.3V with > 500 ms rise time. Does not include charging current for bypass capacitors.

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DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 3.3 V, 18 MHz.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
DC Supply Current (mouse moving)	$I_{DD\ AVG}$		13	23	mA	No load on XA, XB, YA, YB, SCLK, SDIO. Excluding LED current.
Peak Supply Current (mouse moving)	$I_{DD\ PEAK}$		18		mA	No load on XA, XB, YA, YB, SCLK, SDIO. Excluding LED current.
DC Supply Current (mouse not moving)	I_{DD}		18	23	mA	No load on XA, XB, YA, YB, SCLK, SDIO. Excluding LED current.
DC Supply Current (Power Down)	I_{DDPD}		4	30	µA	PD = V_{DD}, SCLK, SDIO = GND or V_{DD}
SCLK, SDIO, PD						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	0.65 * V_{DD}			V	
Output Low Voltage	V_{OL}			0.45	V	@ I_{OL} = 2 mA (SDIO only)
Output High Voltage	V_{OH}	0.6 * V_{DD}			V	@ I_{OH} = 2 mA (SDIO only)
Output Low Voltage (XA, XB, YA, YB)	V_{OL}			0.6	V	@I_{OL} = 0.5 mA
Output High Voltage (XA, XB, YA, YB)	V_{OH}	0.6 * V_{DD}			V	@I_{OH} = 0.5 mA
Output Low Voltage (XY_LED)	V_{OL}			0.5	V	Refer to Figure 18.
XY LED Current	I_{LED}	Typ –20% Typ –15%	614/R1 614/R1	Typ +20% Typ +15%	A A	Recommended operating conditions @25°C, V_{DD} = 3.3V (Refer to Figure 18 and table below).
XY LED Current (Fault Mode)	I_{LED}			1000	µA	R1 < 200Ω
Powerup XY LED Current	I_{LED}			500	µA	V_{DD} < 2.5 V

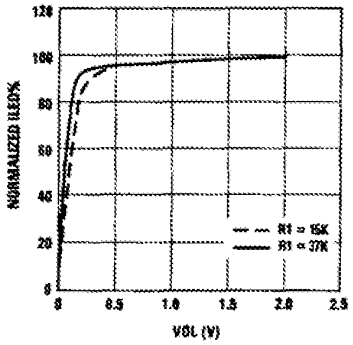


Figure 18. Typical I-V characteristic of ADNS-2030 XY_LED pin.

Typical LED Current Table

R1 value	kΩ	15	18	22	27	33	37
LED current (Typical)	mA	41	34	28	23	19	17

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PD Pin Timing

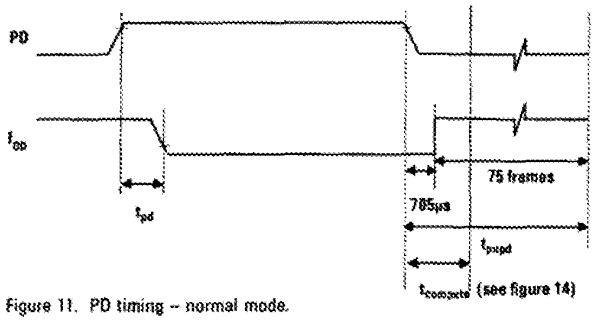


Figure 11. PD timing – normal mode.

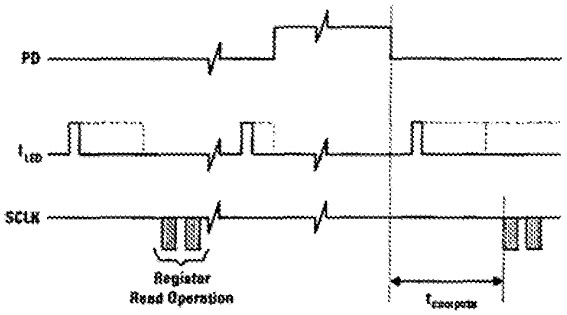


Figure 12. PD timing – sleep mode.

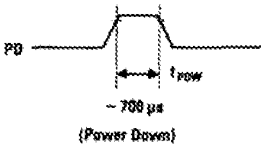


Figure 13. PD minimum pulse width.

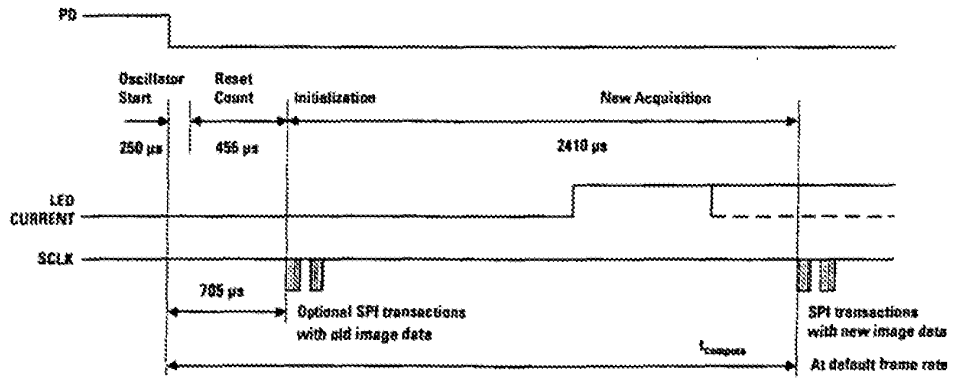


Figure 14. Detail of PD falling edge timing.

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Quadrature Mode Timing

The output waveforms emulate the output from encoders. With the resolution set to 400 cpi, from one to five quadrature states can exist within one frame time. The minimum state time is 133 µs. If the resolution is 800 cpi, then up to ten quadrature states can exist within a frame time. If the motion within a frame is greater than these values, the extra motion will be reported in the next frame. The following diagrams (see Figures 15, 16 and 17) show the timing for positive X motion, to the right, or positive Y motion, up. If a power down via the PD pin occurs during a transfer, the transfer will resume after PD is de-asserted. The timing for that quadrature state will be increased by the length of the PD time.

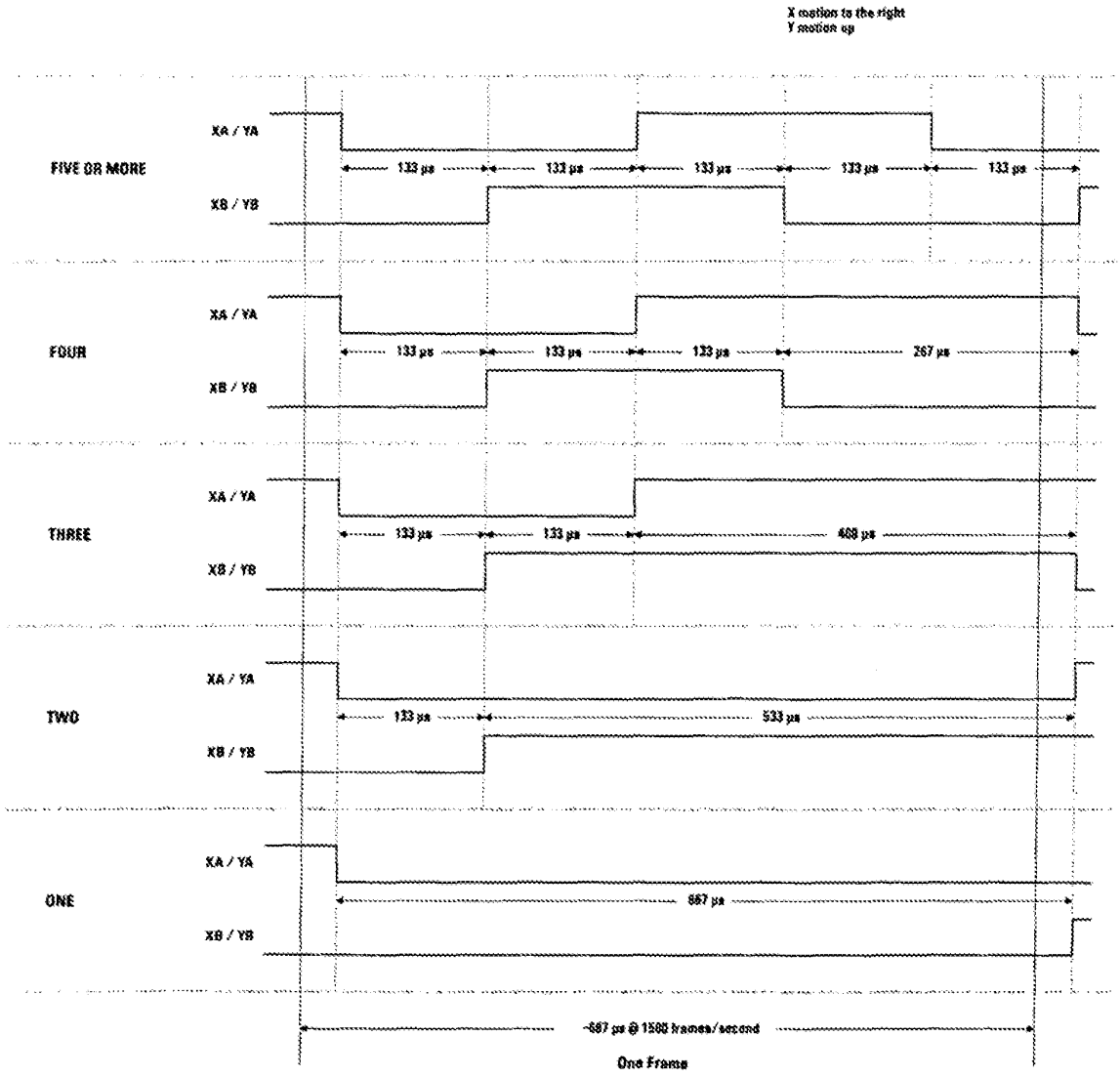


Figure 15. Quadrature states per frame (400 cpi mode).

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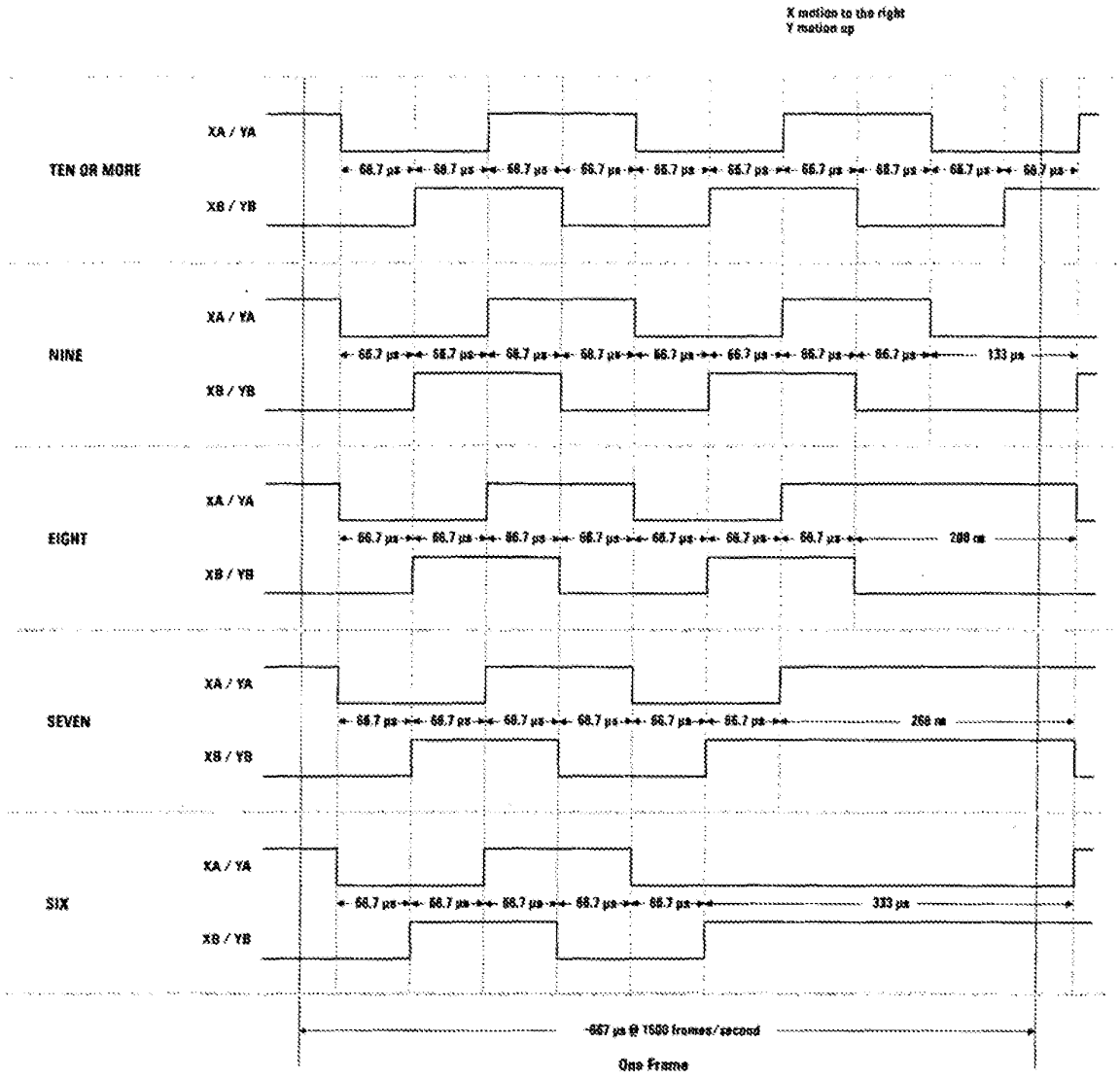


Figure 16. Quadrature states per frame (800 cpi mode).

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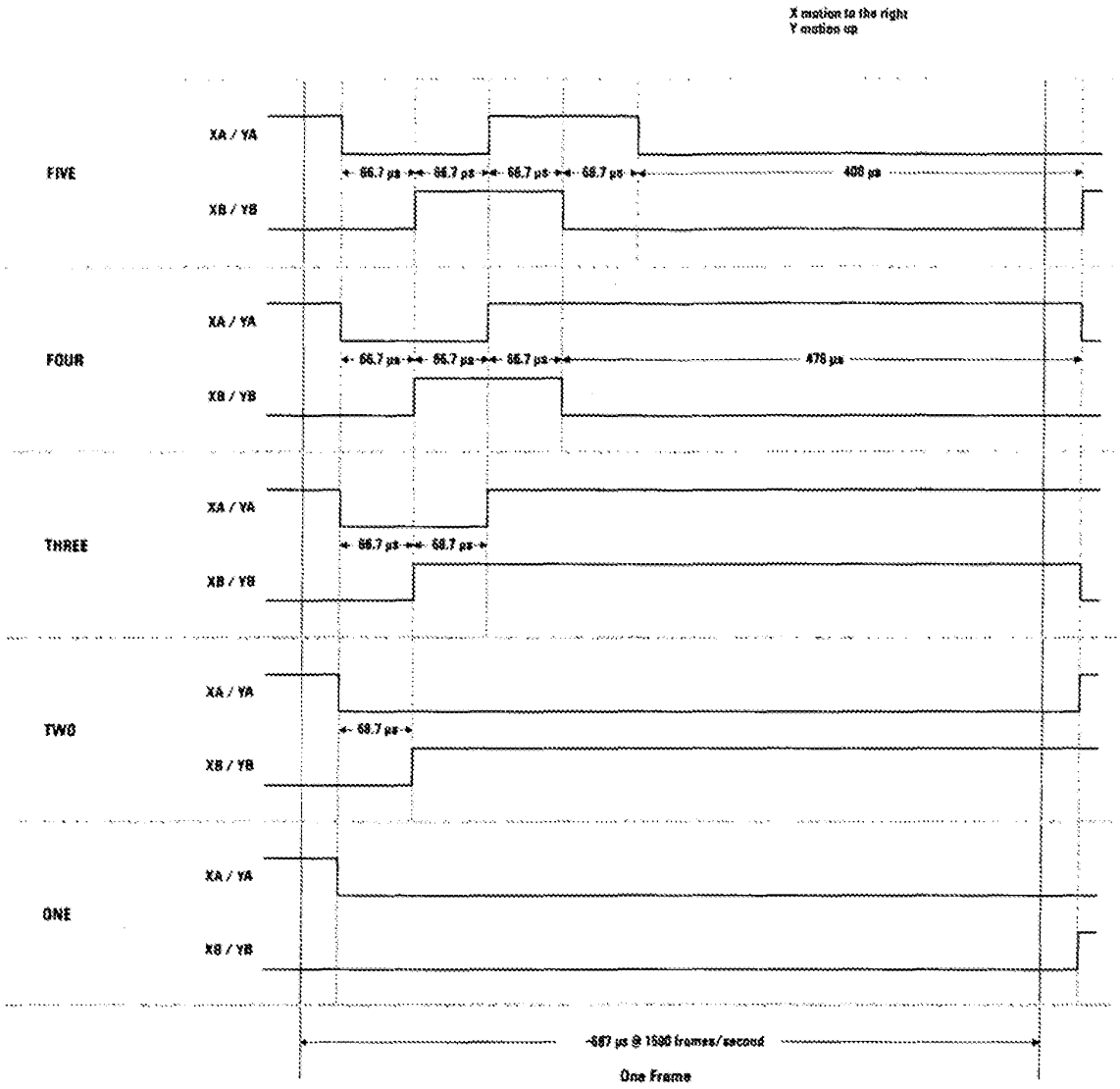
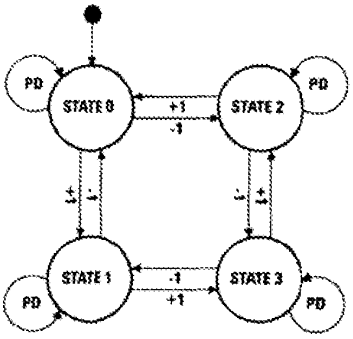


Figure 17. Quadrature states per frame (800 cpi mode).

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Quadrature State Machine

The following state machine shows the states of the quadrature pins. The two things to note are that while the PD pin is asserted, the state machine is halted. Once PD is de-asserted, the state machine picks up from where it left off. State 0 is entered after a power up reset.



STATE	X and Y OUTPUT	
	A	B
0	0	0
1	0	1
2	1	0
3	1	1

Figure 18. Quadrature state machine.

Quadrature Output Waveform

The two channel quadrature outputs are 3.3 volt CMOS outputs. The Δx count is used to generate the XA and XB signals, and Δy count is used for the YA and YB signals.

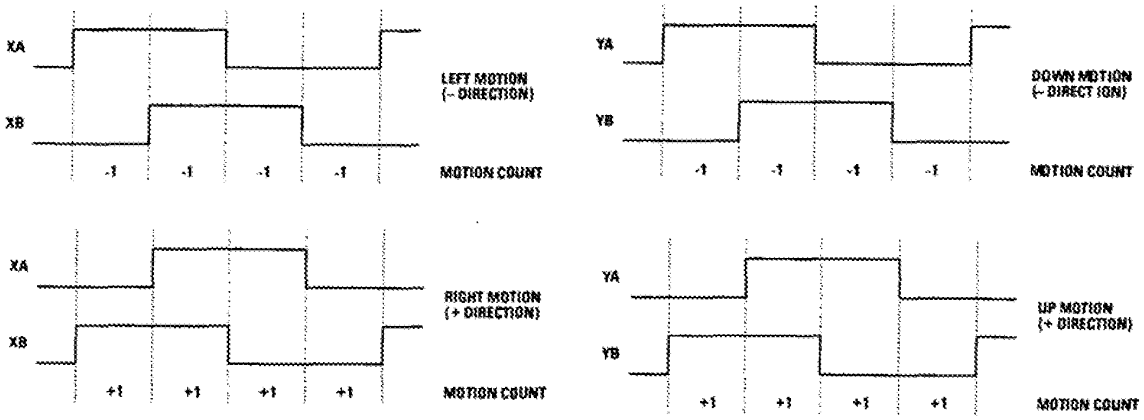


Figure 19. Quadrature output waveform.

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Typical Performance Characteristics

Performance characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 3.3V, 18 MHz.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Path Error (Deviation) expressed	P_{Error}		0.5		%	Path Error (Deviation) is the error from the ideal cursor path. It is as a percentage of total travel and is measured over standard surfaces.

The following graphs (Figs 20–23) are the typical performance of the ADNS-2030 sensor, assembled as shown in the 2D assembly drawing with the HDNS-2100 Lens/Prism, the HDNS-2200 clip, and the HLMP-ED80-xx000 LED (See Figure 5).

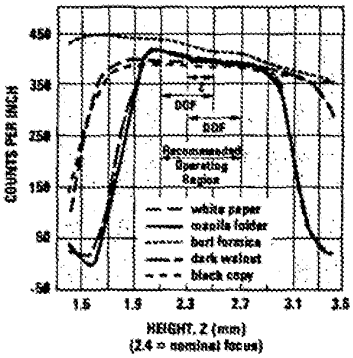


Figure 20. Typical Resolution vs. Height, Z. (Comparative Surfaces)

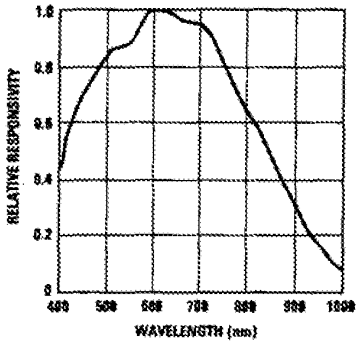


Figure 21. Wavelength Responsivity[1].

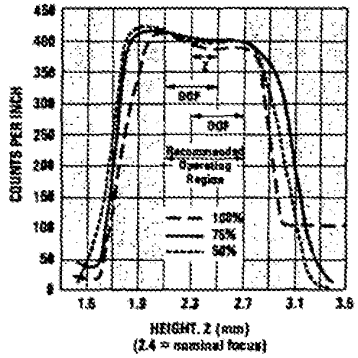


Figure 22. Typical Resolution vs. Height, Z. (Manila folder and LED variation)[2,3]

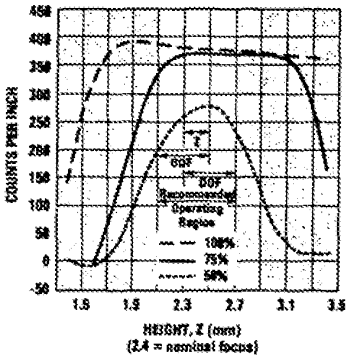


Figure 23. Typical Resolution vs. Height, Z. (Black copy and LED variation)[2,3]

Notes:

1. The ADNS-2030 is designed for optimal performance when used with the HLMP-ED80-xx000 (Red LED 639nm). For use with other LED colors (ie. blue, green), please consult factory. When using alternate LED's there may also be performance degradation and additional eye safety consideration.
2. Z = Distance from Lens Reference Plane to Surface.
3. DOF = Depth of Field

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Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-2030, and can be used to read out the motion information instead of the quadrature data pins.

The port is a two wire, half duplex port. The host microcontroller always initiates communication; the ADNS-2030 never initiates data transfers.

SCLK: The serial port clock. It is always generated by the master (the microcontroller).

SDIO: The data line.

PD: A third line is sometimes involved. PD (Power Down) is usually used to place the ADNS-2030 in a low power mode. PD can also be used to force re-synchronization between the microcontroller and the ADNS-2030 in case of an error.

Write Operation

A write operation, which means that data is going from the microcontroller to the ADNS-2030, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The transfer is synchronized by **SCLK**. The microcontroller changes **SDIO** on falling edges of **SCLK**. The ADNS-2030 reads **SDIO** on rising edges of **SCLK**.

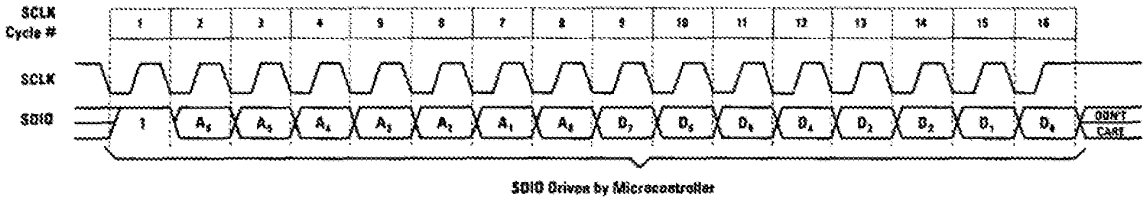


Figure 24 . Write operation.

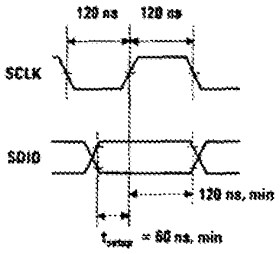


Figure 25. SDIO setup and hold times SCLK pulse width.

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Read Operation

A read operation, which means that data is going from the ADNS-2030 to the microcontroller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is written by the micro-controller, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-2030. The transfer is synchronized by **SCLK**. **SDIO** is changed on falling edges of **SCLK** and read on every rising edge of **SCLK**. The micro-controller must go to a high Z state after the last address data bit. The ADNS-2030 will go to the high Z state after the last data bit. (see detail "B" in Figure 28). One other thing to note during a read operation is that SCLK will need to be delayed after the last address data bit to ensure that the ADNS-2030 has at least 100 µs to prepare the requested data. This is shown in the timing diagrams below.

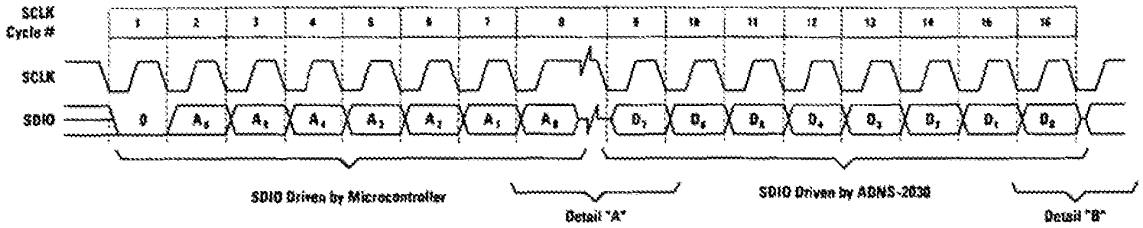


Figure 26. Read operation.

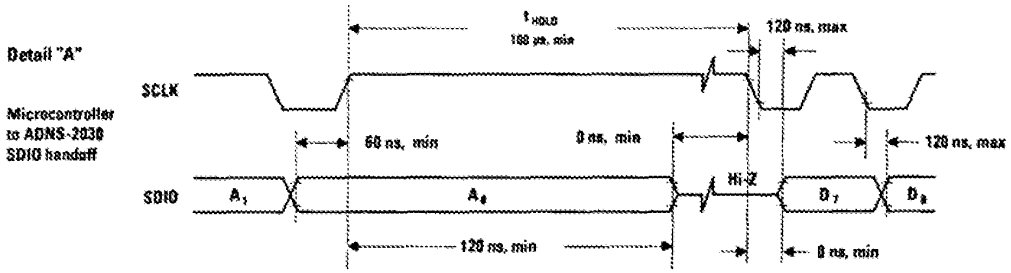


Figure 27. Microcontroller to ADNS-2030 SDIO handoff.

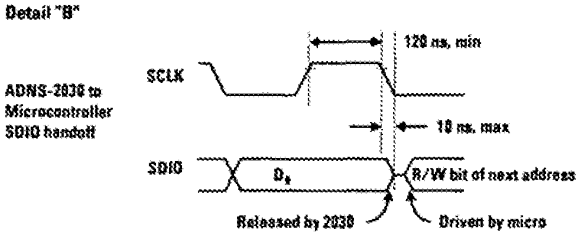


Figure 28. ADNS-2030 to microcontroller SDIO handoff.

NOTE: The 120 ns high state of SCLK is the minimum data hold time of the ADNS-2030. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-2030 will hold the state of D_0 on the SDIO line until the falling edge of SCLK. In both write and read operations, SCLK is driven by the microcontroller.

Serial port communications is not allowed while PD (Power Down) is high. See "Error Detection and Recovery" regarding re-synchronizing via PD.

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Forcing the SDIO Line to the Hi-Z State

There are times when the SDIO line from the ADNS-2030 should be in the Hi-Z state. If the microprocessor has completed a write to the ADNS-2030, the SDIO line is Hi-Z, since the SDIO pin is still configured as an input. However, if the last operation from the microprocessor was a read, the ADNS-2030 will hold the D0 state on SDIO until a falling edge of SCLK.

To place the SDIO pin into the Hi-Z state, first raise the PD pin for 100 µs (min). The PD pin can stay high, with the ADNS-2030 in the shutdown state, or the PD pin can be lowered, returning the ADNS-2030 to normal operation. In either case, the SDIO line will now be in the Hi-Z state.

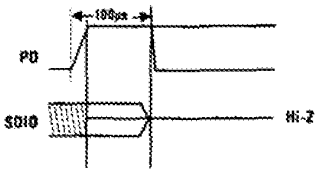


Figure 29. SDIO Hi-Z state and timing.

Required Timing Between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port. See Figure 30.

If the rising edge of SCLK for the last data bit of the second write command occurs before the 100 microsecond required delay, then the first write command may not complete correctly. See Figure 31.

If the rising edge of SCLK for the last address bit of the read command occurs before the 100 microsecond required delay, then the write command may not complete correctly. See Figure 32.

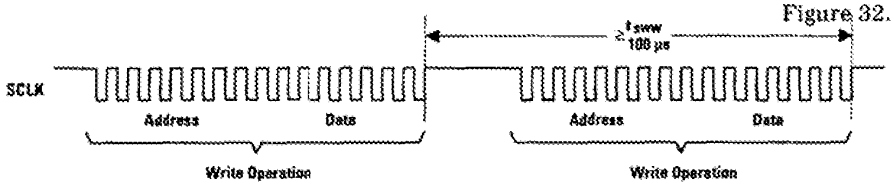


Figure 30. Timing between two write commands.

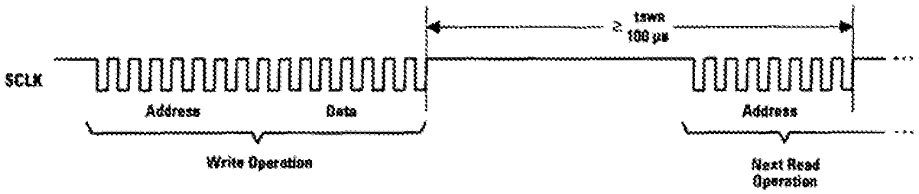


Figure 31. Timing between write and read commands.

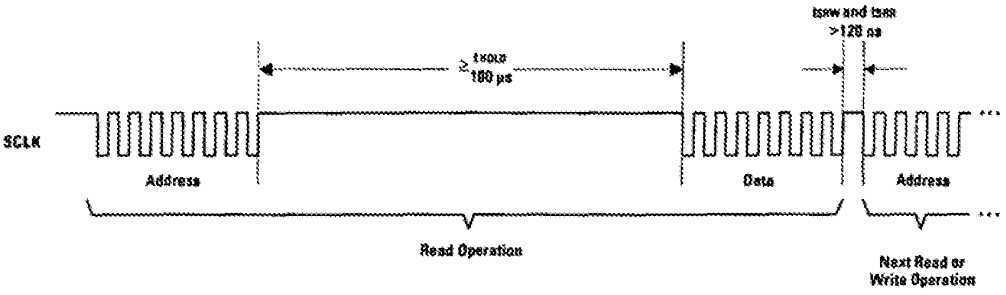


Figure 32. Timing between read and either write or subsequent read commands.

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The falling edge of SCLK for the first address bit of either the read or write command must be at least 120 ns after the last SCLK rising edge of the last data bit of the previous read operation.

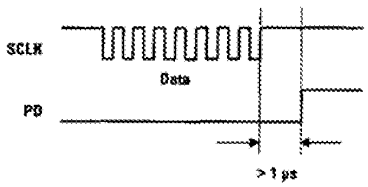


Figure 33. Timing between SCLK and PD rising edge.

Error Detection and Recovery

1. The ADNS-2030 and the microcontroller might get out of synchronization due to ESD events, power supply droops or microcontroller firmware flaws. In such a case the microcontroller should raise PD for 100 µs. The ADNS-2030 will reset the serial port but will not reset the registers, and be prepared for the beginning of a new transmission.
2. The ADNS-2030 has a transaction timer for the serial port. If the 16th SCLK rising edge is spaced more than approximately 0.9 seconds from the first SCLK edge of the current transaction, the serial port will reset.
3. Invalid addresses:

   Writing to an invalid address will have no effect. Reading from an invalid address will return all zeros.
4. Collision detection on SDIO:

   The only time that the ADNS-2030 drives the SDIO line is during a READ operation. To avoid data collisions, the microcontroller should relinquish SDIO before the falling edge of SCLK after the last address bit. The ADNS-2030 begins to drive SDIO after the next rising edge of SCLK. The ADNS-2030 relinquishes SDIO within 120 ns of the falling SCLK edge after the last data bit. The microcontroller can begin driving SDIO any time after that. In order to maintain low power consumption in normal operation or when the PD pin is pulled high, the micro-controller should not leave SDIO floating until the next transmission (although that will not cause any communication difficulties).
5. In case of synchronization failure, both the ADNS-2030 and the microcontroller may drive SDIO. The ADNS-2030 can withstand 30 mA of short circuit current and will withstand infinite duration short circuit conditions.
6. Termination of a transmission by the microcontroller may sometimes be required (for example, due to a USB suspend interrupt during a read operation). To accomplish this the microcontroller should raise PD. The ADNS-2030 will not write to any register and will reset the serial port (but nothing else) and be prepared for the beginning of future transmissions after PD goes low.
7. The microcontroller can verify success of write operations by issuing a read command to the same address and comparing written data to read data.
8. The microcontroller can verify the synchronization of the serial port by periodically reading the product ID register.

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Notes on Power up and the Serial Port

The sequence in which V_{DD}, PD, SCLK and SDIO are set during powerup can affect the operation of the serial port. The diagram below shows what can happen shortly after powerup when the microprocessor tries to read data from the serial port.

This diagram shows the V_{DD} rising to valid levels, at some point the microcontroller starts its program, sets the SCLK and SDIO lines to be outputs, and sets them high. It then waits to ensure that the ADNS-2030 has powered up and is ready to communicate. The microprocessor then tries to read from location 0x00, Product_ID, and is expecting a value of 0x03. If it receives this value, it then knows that the communication to the ADNS-2030 is operational.

The problem occurs if the ADNS-2030 powers up before the microprocessor sets the SCLK and SDIO lines to be outputs and high. The ADNS-2030 sees the raising of the SCLK as a valid rising edge, and clocks in the state of the SDIO as the first bit of the address (sets either a read or a write depending upon the state).

In the case of SDIO low, then a read operation has started. When the microprocessor begins to actually send the address, the ADNS-2030 already has the first bit of an address. When the 7th bit is sent by the micro, the ADNS-2030 has a valid address, and drives the SDIO line high within 120 ns (see detail "A" in Figure 26 and Figure 27). This results in a bus fight for SDIO. Since the address is wrong, the data sent back will be incorrect.

In the case of SDIO high, a write operation is started. The address and data are out of synchronization, and the wrong data will be written to the wrong address.

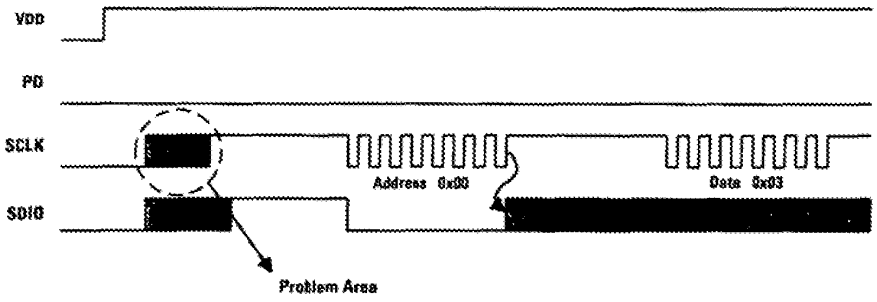


Figure 34. Power up serial port sequence.

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Two Solutions

There are two different ways to solve the problem: (1) waiting for the serial port watchdog timer to time out, or (2) using the PD line to reset the serial port.

1. Serial port watchdog timer timeout (Refer to Figure 35.)

If the microprocessor waits at least t_{SPTT} from V_{DD} valid, it will ensure that the ADNS-2030 has powered up and the watchdog timer has timed out. This assumes that the microprocessor and the ADNS-2030 share the same power supply. If not, then the microprocessor must wait t_{SPTT} from ADNS-2030 V_{DD} valid. Then when the SCLK toggles for the address, the ADNS-2030 will be in sync with the microprocessor.

2. PD Sync (Refer to Figure 36.)

The PD line can be used to resync the serial port. If the microprocessor waits for 4 ms from V_{DD} valid, and then outputs a valid PD pulse (Refer to Figure 14), then the serial port will be ready for data.

Resync Note

If the microprocessor and the ADNS-2030 get out of sync, then the data either written or read from the registers will be incorrect. An easy way to solve this is to output a PD pulse to resync the parts after an incorrect read.

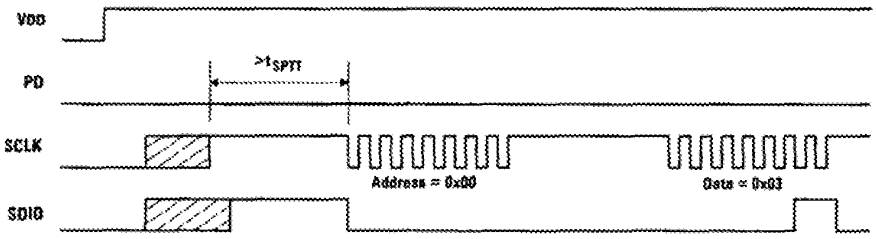


Figure 35. Power up serial port watchdog timer sequence.

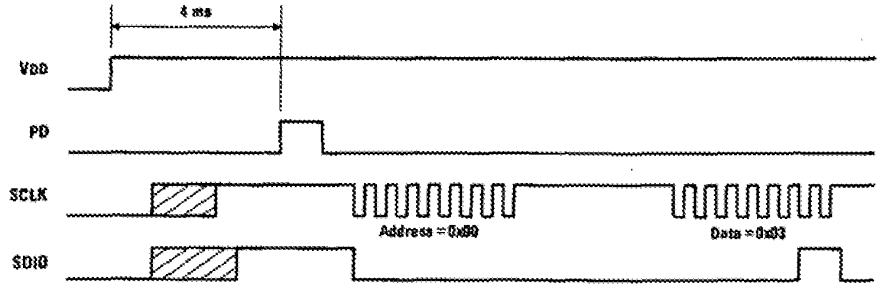


Figure 36. Power up serial port PD sync sequence.

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Registers

The ADNS-2030 can be programmed through registers, via the serial port, and configuration and motion data can be read from these registers.

Address	Register
0x00	Product_ID
0x01	Revision_ID
0x02	Motion
0x03	Delta_X
0x04	Delta_Y
0x05	SQUAL
0x06	Average_Pixel
0x07	Maximum_Pixel
0x08	Reserved
0x09	Reseved
0x0a	Configuration_bits
0x0b	Reserved

Address	Register
0x0c	Data_Out_Lower
0x0d	Data_Out_Upper
0x0e	Shutter_Lower
0x0f	Shutter_Upper
0x10	Frame_Period_Lower
0x11	Frame_Period_Upper

Product_ID **Address: 0x00**
Access: Read **Reset Value: 0x03**

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: Eight bit number with the product identifier.

USAGE: The value in this register does not change; it can be used to verify that the serial communications link is OK.

Revision_ID **Address: 0x01**
Access: Read **Reset Value: 0xNN**

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: Eight bit number with current revision of the IC.

USAGE : NN is a value between 00 and FF which represent the current design revision of the device.

IC Revision	NN
Rev. 1.0	0x10
Rev. 2.0	0 x 20

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Motion **Address: 0x02**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	FAULT	OVFY	OVFX	Reserved	Reserved	RES

Data Type: Bit field

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If so, then the user should read registers 0x03 and 0x04 to get the accumulated motion. It also tells if the motion buffers have overflowed and whether or not an LED fault occurred since the last reading. The current resolution is also shown.

Field Name	Description
MOT	Motion since last report or PD **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers
Reserved	Reserved for future
FAULT	LED Fault detected -- set when RBIN is too low or too high, shorts to V_{DD} or Ground **0 = No fault** 1 = Fault detected
OVFY	Motion overflow Y, ΔY buffer has overflowed since last report **0 = No overflow** 1 = Overflow has occurred
OVFX	Motion overflow X, ΔX buffer has overflowed since last report **0 = No overflow** **1 = Overflow has occurred**
Reserved	
Reserved	Reserved for future
RES	Resolution in counts per inch **0 = 400** 1 = 800

Notes for Motion:

1. Reading this register freezes the Delta_X and Delta_Y register values. Read this register before reading the Delta_X and Delta_Y registers. If Delta_X and Delta_Y are not read before the motion register is read a second time, the data in Delta_X and Delta_Y will be lost.
2. Agilent RECOMMENDS that registers 0x02, 0x03 and 0x04 be read sequentially.
3. Internal buffers can accumulate more than eight bits of motion for X or Y. If either one of the internal buffers overflows, then absolute path data is lost, and the OVFX or OVFY bit is set. To clear these bits (OVFX and OVFY), read the Motion, Delta_X and Delta_Y registers consecutively. Repeat until the motion bit (MOT) is cleared. Until MOT is cleared, the Delta_X or Delta_Y registers will read either positive or negative full scale, except possibly the last read. If the motion register has not been read for long time, at 400 cpi it may take up to 16 read cycles to clear the buffers, at 800 cpi, up to 32 cycles.
4. The FAULT bit signifies that an LED fault has occurred since the last time the motion register was read. An LED fault occurs if RBIN has a low resistance connection to ground. When this is detected the LED is turned off. The FAULT bit remains set until the fault condition is cleared and the motion register is read. This bit is updated only when the motion register is read. Once an LED fault has cleared, the hardware will drive the LED normally.

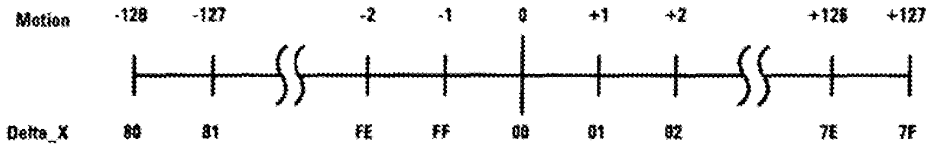
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Delta_X **Address: 0x03**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number.

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.

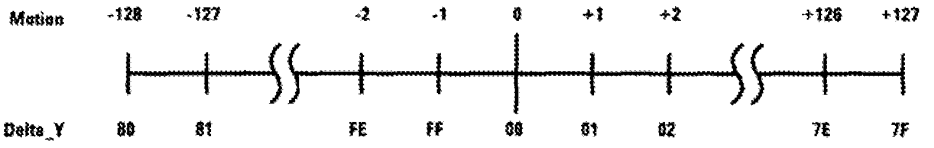


Delta_Y **Address: 0x04**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number.

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register



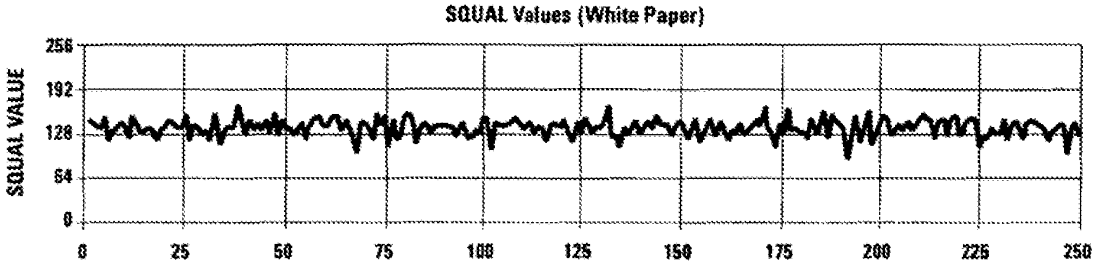
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SQUAL **Address: 0x05**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Eight bit number.

USAGE: SQUAL (Surface QUALity) is a measure of the number of features visible by the sensor in the current frame. The maximum value is 255. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 250 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor.



The focus point is important and could affect the SQUAL value. Figure 37 shows another setup with various Z-height. This graph clearly shows that the SQUAL count is dependent on focus distance. The data is obtained by getting multiple readings over different heights.

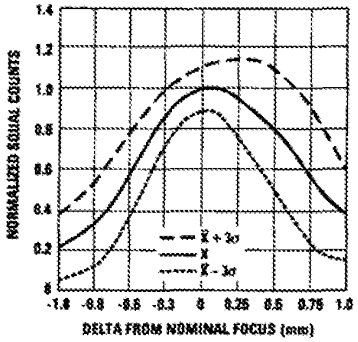


Figure 37. Typical SQUAL vs. Height, Z. (white paper)

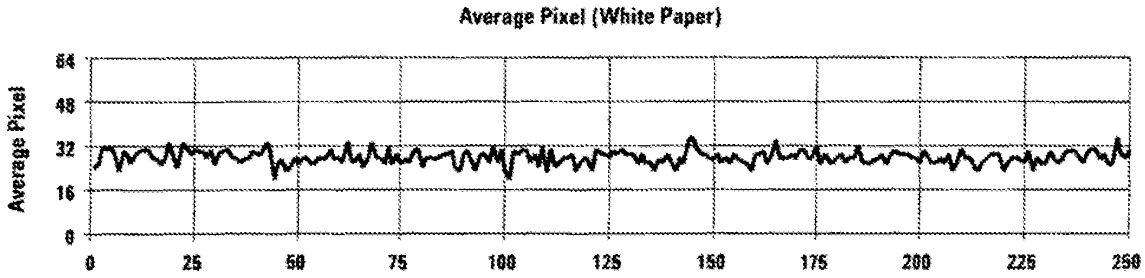
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Average_Pixel **Address: 0x06**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	0	0	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type: Six bit number.

USAGE: Average Pixel value in current frame. Minimum value = 0, maximum = 63. The average pixel value may vary from frame to frame. Shown below is a graph of 250 sequentially acquired average pixel values, while the sensor was moved slowly over white paper.

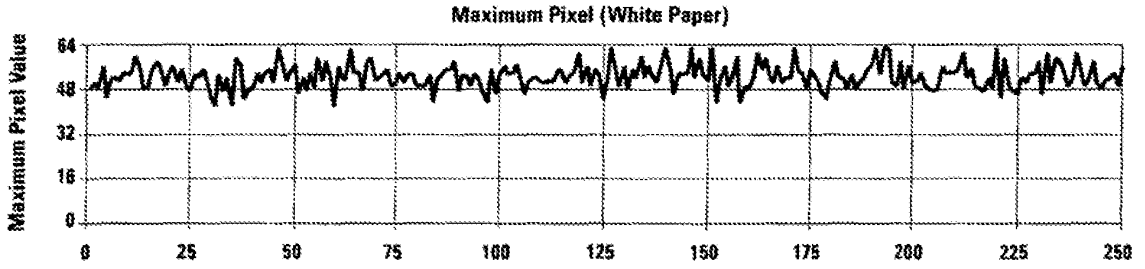


Maximum_Pixel **Address: 0x07**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	0	0	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Six bit number.

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 63. The maximum pixel value may vary from frame to frame. Shown below is a graph of 250 sequentially acquired maximum pixel values, while the sensor was moved slowly over white paper.



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Reserved **Address: 0x08**

Reserved **Address: 0x09**

Configuration_bits **Address: 0x0a**
Access: Read/Write **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	RESET	LED_MODE	Self Test	RES	PixDump	Reserved	Reserved	Sleep

Data Type: Bit field

USAGE: Register 0x0a allows the user to change the configuration of the sensor. Shown below are the bits, their default values, and optional values.

Field Name	Description
RESET	Power up defaults (bit always reads 0) **0 = No effect** 1 = Reset registers and bits to power up default settings (bold entries)
LED_MODE	LED Shutter Mode **0 = Shutter mode off (LED always on, even if no motion up to 1 sec)** 1 = Shutter mode on (LED only on when electronic shutter is open)
Self Test[1]	Self Tests (bit always reads 0) **0 = No tests** 1 = Perform all self tests, output 16 bit CRC via Data_Out_Upper and Data_Out_Lower registers.
RES	Resolution in counts per inch **0 = 400** 1 = 800
Pix Dump	Dump the pixel array through Data_Out_Upper and Data_Out_Lower, 256 bytes each **0 = Disabled** 1 = Dump pixel array
Reserved	
Reserved	
Sleep	Sleep Mode **0 = Normal, falls asleep after one second of no movement (1,500 frames/s)** **1 = Always awake**

Note:

1. Since part of the self test is a RAM test, the RAM will be overwritten with the default values when the test is done. If any configuration changes from the default are needed for operation, make the changes AFTER the self test is run. This operation requires substantially more time to complete than other register transactions.

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Reserved **Address: 0x0b**

Data_Out_Lower **Address: 0x0c**
Access: Read **Reset Value: undefined**

Bit	7	6	5	4	3	2	1	0
Field	DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0

Data_Out_Upper Address: 0x0d
Access: Read **Reset Value: undefined**

Bit	7	6	5	4	3	2	1	0
Field	DO_{15}	DO_{14}	DO_{13}	DO_{12}	DO_{11}	DO_{10}	DO_9	DO_8

Data Type: Sixteen bit word.

USAGE: Data from the system self test or the pixel dump command can be read out with these registers. The data can be read from 0x0d only, or from 0x0d followed by 0x0c.

	Data_Out_Upper	Data_Out_Lower	Notes
Self Test result 1:	DB	FD	One of two results returned.
Self Test result 2:	29	D6	These values are subject to change with each device design revision.
Pixel Dump command:	Pixel Address	Pixel Data (bits 0-5) and Pixel Data Status (bit 7)	

Once the pixel dump command is given, the sensor writes the address and the value for the first pixel into the Data_Out_Upper and Data_Out_Lower registers. The MSB of Data_Out_Lower is the status bit for the data. If the bit is high, the data are NOT valid. Once the MSB is low, the data for that particular read are valid and should be saved. The pixel address and data will then be incremented on the next frame. Once the pixel dump is complete, the PixDump bit in register 0x0a should be set to zero. To obtain an accurate image to get the Pixel Dump image, the LED needs to be turned on by changing the sleep mode of the configuration register 0x0e to always awake.

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Pixel Address Map (looking through the HDNS-2100 lens)

Last Pixel

FF	FE	FD	FC	FB	FA	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
EF	EE	ED	EC	EB	EA	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CF	CE	CD	CC	CB	CA	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
BF	BE	BD	BC	BB	BA	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
AF	AE	AD	AC	AB	AA	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
9F	9E	9D	9C	9B	9A	99	98	97	96	95	94	93	92	91	90
8F	8E	8D	8C	8B	8A	89	88	87	86	85	84	83	82	81	80
7F	7E	7D	7C	7B	7A	79	78	77	76	75	74	73	72	71	70
6F	6E	6D	6C	6B	6A	69	68	67	66	65	64	63	62	61	60
5F	5E	5D	5C	5B	5A	59	58	57	56	55	54	53	52	51	50
4F	4E	4D	4C	4B	4A	49	48	47	46	45	44	43	42	41	40
3F	3E	3D	3C	3B	3A	39	38	37	36	35	34	33	32	31	30
2F	2E	2D	2C	2B	2A	29	28	27	26	25	24	23	22	21	20
1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00

First Pixel

Top X-ray View of Mouse

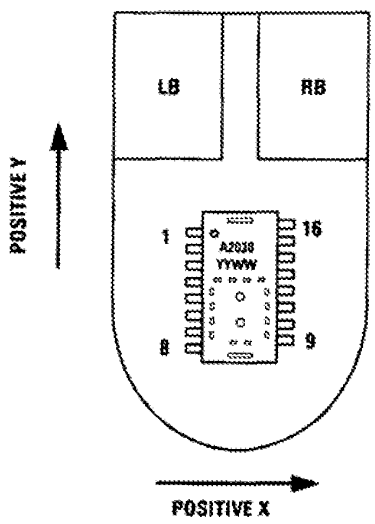
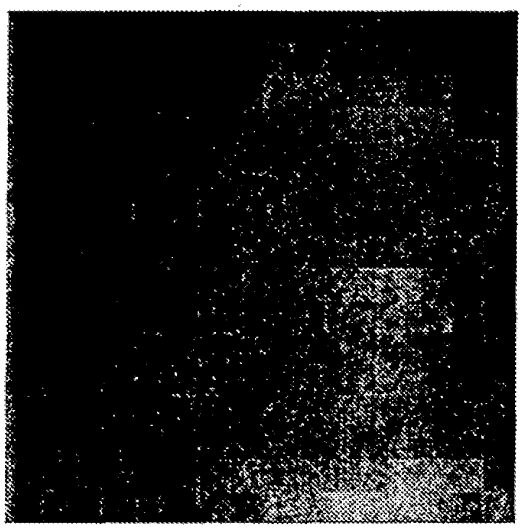


Figure 38. Directions are for a complete mouse, with the HDNS-2100 lens.

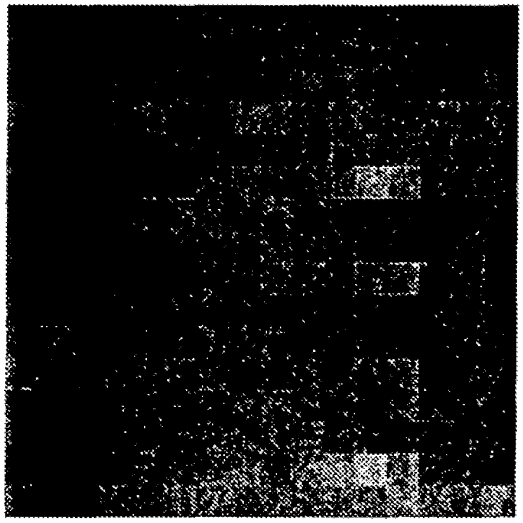
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Pixel Dump Pictures

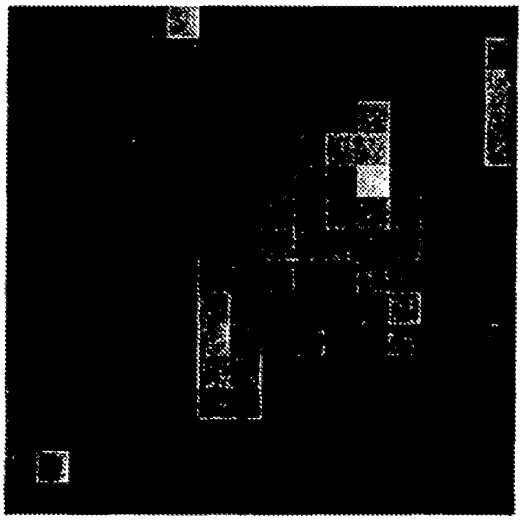
The following images are the output of the pixel dump command. The data ranges from zero for complete black, to 63 for complete white. An internal AGC circuit adjusts the shutter value to keep the brightest feature (max pixel) in the mid 50's.



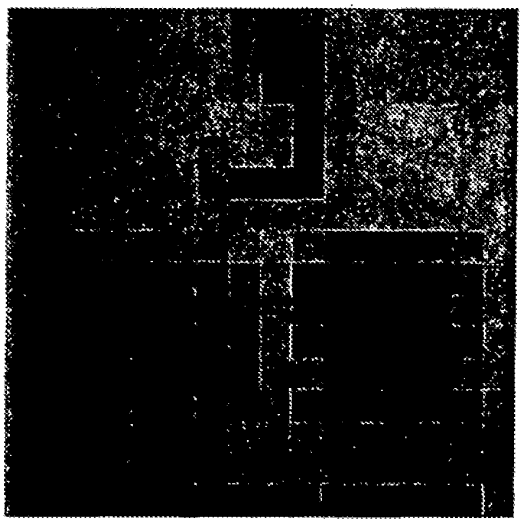
(a) White Paper



(b) Manila Folder



(c) Neoprene Mouse Pad (Gray)



(d) USAF Test Chart Group 3, Element 1, 8 line pairs per mm

Figure 39. Pixel dump pictures.

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Shutter_Lower **Address: 0x0e**
Access: Read **Reset Value: 0x64**

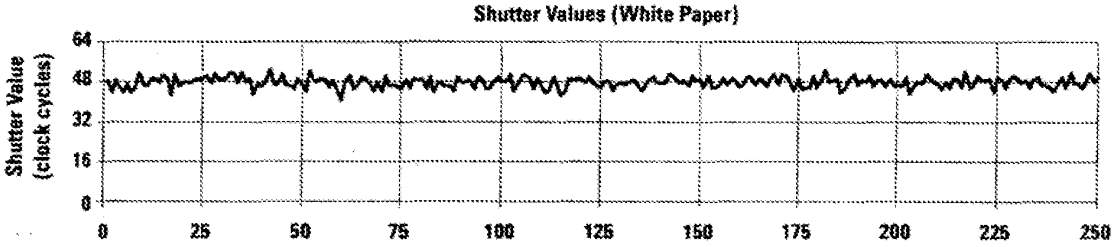
Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Shutter_Upper **Address: 0x0f**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Data Type: Sixteen bit word.

USAGE: Units are clock cycles; default value is 64. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value may be different on every frame. For each frame, the shutter can only change by ± 1/16 of the current value. Shown below is a graph of 250 sequentially acquired shutter values, while the sensor was moved slowly over white paper.



The focus point is important and could affect the shutter value. Figure 40 shows another setup with various Z-heights. This graph clearly shows that the shutter value is dependent on focus distance. It shows average readings over different heights.

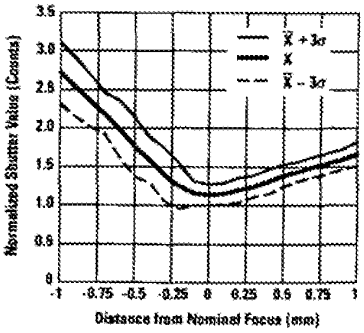


Figure 40. Typical shutter vs. Z (white paper).

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The maximum value of the shutter is dependent upon the frame rate and clock frequency. The formula for the maximum shutter value is:

$$\text{Max shutter value} = \frac{\text{clock freq}}{\text{frame rate}} - 2816$$

For a clock frequency of 18 MHz, the following table shows the maximum shutter value. 1 clock cycle is 55.56 usec.

Frames/second	Max Shutter		Shutter		
	Decimal	Hex	Upper	Lower	
2300*	5016	0x1392	13	92	
2000*	6184	0x1828	18	28	
1500	9184	0x23E0	23	E0	Default Max Shutter
1000	15184	0x3B50	3B	50	
500	33184	0x81A0	81	A0	

* Note: To optimize tracking performance on dark surfaces, it is recommended that an adaptive frame rate based on shutter value be implemented for frame rates greater than 1500.

Frame_Period_Lower **Address: 0x10**
Access: Read/Write **Reset Value: 0x20**

Bit	7	6	5	4	3	2	1	0
Field	FP_7	FP_6	FP_5	FP_4	FP_3	FP_2	FP_1	FP_0

Frame_Period_Upper **Address: 0x11**
Access: Read/Write **Reset Value: 0xd1**

Bit	7	6	5	4	3	2	1	0
Field	FP_{15}	FP_{14}	FP_{13}	FP_{12}	FP_{11}	FP_{10}	FP_9	FP_8

Data Type: Sixteen bit 2's complement word.

USAGE: Sets the frame rate. The frame period counter counts up until it overflows. Units are clock cycles.

The formula is: $\frac{\text{clock rate}}{\text{frame rate}}$ = counts (2's complements hex)

For an 18 MHz clock, below are the Frame_period values for popular frame rates.

Frames/second	Counts			Frame_Period		
	Decimal	Hex	2's comp	Upper	Lower	
2300*	7826	0x1E92	0xE16E	E1	6E	
2000*	9000	0x2328	0xDCD8	DC	D8	
1500	12000	0x2EE0	0xD120	D1	20	←Default Frame Period
1000	18000	0x4650	0xB9B0	B9	B0	
500	36000	0x8CA0	0x7360	73	60	←Minimum Frame Period

*Note: To optimize tracking performance on dark surfaces, it is recommended that an adaptive frame rate based on shutter value be implemented for frame rates greater than 1500.

Changing the frame rate results in changes in the maximum speed, acceleration limits, and dark surface performance.

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IC Register State after Reset (power up or setting bit 7, register 0x0a)

Address	Register	Default Value	Meaning
0x00	Product_ID	0x03	Product ID = 3 (Fixed value)
0x01	Revision_ID	0xNN	Revision of IC (Fixed value) (For each device design revision)
0x02	Motion	0x00	No Motion LED = No fault No X data overflow No Y data overflow Resolution is 400 counts per inch
0x03	Delta_X	0x00	No X motion
0x04	Delta_Y	0x00	No Y motion
0x05	SQUAL	0x00	No image yet to measure
0x06	Average_Pixel	0x00	No image yet to measure
0x07	Maximum_Pixel	0x00	No image yet to measure
0x08	Reserved		
0x09	Reserved		
0x0a	Configuration_bits	0x00	Part is not Reset LED Shutter Mode is off No Self Tests Resolution = 400 counts per inch Pixel Dump is disabled Sleep mode is enabled
0x0b	Reserved	—	
0x0c	Data_Out_Lower	undefined	No data to read
0x0d	Data_Out_Upper	undefined	No data to read
0x0e	Shutter_Lower	0x64	Initial shutter value
0x0f	Shutter_Upper	0x00	Initial shutter value
0x10	Frame_Period_Lower	0x20	Initial frame period value (corresponds to 1500 fps)
0x11	Frame_Period_Upper	0xd1	Initial frame period value (corresponds to 1500 fps)

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Optical Mouse Design References

Application Note AN1179

Eye Safety Calculation AN1228

Ordering Information

Specify part number as follows:

ADNS-2030 = Sensor IC in a 16-pin staggered DIP, 20 per tube.

HDNS-2100 = Round Optical Mouse Lens

HDNS-2100#001 = Trimmed Optical Mouse Lens

HDNS-2200 = LED Assembly Clip (Black)

HDNS-2200#001 = LED Assembly Clip (Clear)

HLMP-ED80-xx000 = LED

www.agilent.com/ semiconductors

For product information and a complete list of distributors, please go to our web site.

For technical assistance call:

Americas/Canada: +1 (800) 235-0312 or (916) 788-6763

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China: 10800 650 0017

Hong Kong: (65) 6756 2394

India, Australia, New Zealand: (65) 6755 1939

Japan: (+81 3) 3335-8152(Domestic/International), or 0120-61-1280(Domestic Only)

Korea: (65) 6755 1989

Singapore, Malaysia, Vietnam, Thailand, Philippines, Indonesia: (65) 6755 2044

Taiwan: (65) 6755 1843

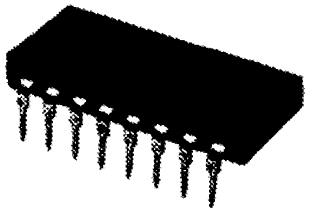
Data subject to change.
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Obsoletes 5988-5686EN
May 11, 2005
5988-8421EN

Agilent Technologies

Agilent ADNS-2051 Optical Mouse Sensor

Product Overview



Features

- Precise optical navigation technology
- No mechanical moving parts
- Complete 2D motion sensor
- Serial interface and/or quadrature interface
- Smooth surface navigation
- Programmable frame speed up to 2300 frames per sec (fps)
- Accurate motion up to 14 ips
- 800 cpi resolution
- High reliability
- High speed motion detector
- No precision optical alignment
- Wave solderable
- Single 5.0 volt power supply
- Shutdown pin for USB suspend mode operation
- Power conservation mode during times of no movement
- On chip LED drive with regulated current
- Serial port registers
  - Programming
  - Data transfer
- 16-pin staggered dual inline package (DIP)

Applications

- Mice for desktop PCs, workstations, and portable PCs
- Trackballs
- Integrated input devices

Description

High Performance Optical Mouse Sensor for More Precise Navigation

The ADNS-2051 is a low cost reflective optical sensor that provides a non-mechanical tracking engine for implementing a computer pointing device. It is based on optical navigation technology which measures changes in position by optically acquiring sequential surface images up to 2300 times per second and mathematically determining the direction and magnitude of movement at the maximum of 800 counts per inch (cpi) and at speeds up to 14 inches per second (ips). Agilent provides the complete optical mouse sample kit (Part # ADNK-2052). The CMOS based sensor is mounted in a 16 pin staggered dual inline package (DIP) and designed for use with the HDNS-2200 (LED Assembly Clip) and HLMP-ED80-XXXXX (639 nm LED illumination source) and HDNS-2100 (lens).

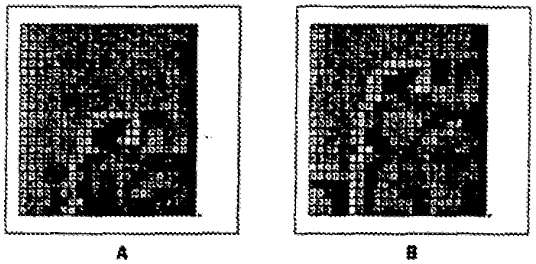
Theory of Operation

The ADNS-2051 is based on Optical Navigation Technology. It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), a two-channel quadrature output, and a two-wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system provided by the HDNS-2100, 2200, and HLMP-ED80-XXXXX. These images are processed by the DSP to determine the direction and distance of motion. The DSP generates the Δx and Δy relative displacement values that are converted into two channel quadrature signals.

Other optical mouse sensors available from Agilent Technologies

- ADNS-2610
- ADNS-2620
- HDNS-2000
- ADNS-2030



A B

Figure 1. The Navigation Engine identifies common features in sequential images to determine the direction and amount of mouse movement. Image B was taken while the mouse was moving, a short time after image A.

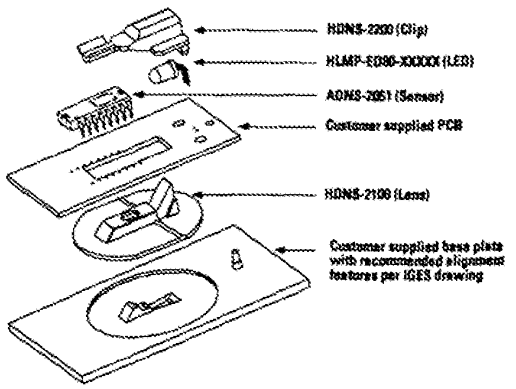


Figure 2. Exploded view drawing of optical mouse components.

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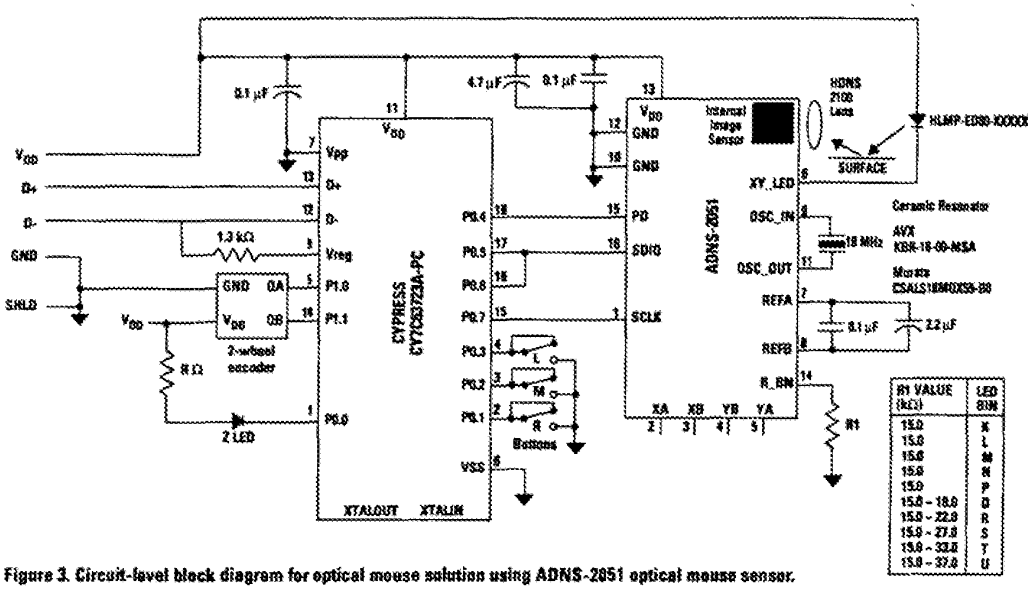


Figure 3. Circuit-level block diagram for optical mouse solution using ADNS-2051 optical mouse sensor.

ADNS-2051 Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	4.25	5.0	5.5	V	Register values retained for voltage transients below 4.25V but greater than 4V
DC Supply Current (mouse moving)	$I_{DD\,AVG}$		15	25	mA	No load on XA, XB, YA, YB, SCLK, SDIO. Excluding LED current
Peak Supply Current (mouse moving)	$I_{DD\,PEAK}$		20		mA	No load on XA, XB, YA, YB, SCLK, SDIO. Excluding LED current
DC Supply Current (mouse not moving)	I_{DD}		12	25	mA	No load on XA, XB, YA, YB, SCLK, SDIO. Excluding LED current
DC Supply Current (power down)	I_{DDPD}		170	248	µA	PD = high; SCLK, SDIO = GND or V_{DD}; V_{DD} = 4.25V to 5.25V
Clock Frequency	f_{CLK}	17.4	18.0	18.7	MHz	Set by ceramic resonator
Resonator Impedance	X_{RES}			55	Ω	
Distance from lens reference plane to surface	Z	2.3	2.4	2.5	mm	Results in ± 0.2 mm DOF
Speed	S	0		14	in/sec	@ frame rate = 1500 frames/second
Acceleration	A			0.15	g	@ frame rate = 1500 frames/second
Light level onto IC	IRR_{INC}	80 100		25,000 30,000	mW/m²	λ = 639 nm λ = 875 nm
Resolution	RES		400	800	counts/in	
Frame Rate	FR		1500		frames/s	

For product information and a complete list of Agilent contacts and distributors, please go to our web site.

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Agilent Optical Mouse Sensors
Selection Guide

Introduction

When Agilent Technologies introduces an optical mouse sensor, the part is normally made available in different offerings; sensor only, bundle set, sample kit, or designer's kit. Except for the sensor standalone part, the others are configured with either one or more optical mouse accessories. These accessories are the lenses, clips and LEDs.

This document is intended to highlight these part numbers and to list down the accessories or other components they consist of.

Part Numbering System

When an optical mouse sensor is introduced, these are the part numbers that are made available with the sensor:

Part Numbers	Description	Products With Base Part Number Mentioned
ADNS-XXXX	Stand alone components	**1. Optical Mouse Sensor**
		2. Lens (Round/Trim)
		3. Assembly Clip (Clear/Black)
ADNB-XXXX	Optical Mouse Bundle	**1. Optical Mouse Sensor and Round Lens** (ADNB-XXX1) *
		2. Optical Mouse Sensor and Trim Lens (ADNB-XXX2) *
		* Except for ADNB-2050 and ADNB-2051
ADNK-XXXX	Optical Mouse Kits	**1. Optical Mouse Sample Kit**
		a. Optical Mouse Sensor (5 units)
		b. Round lens (5 units)
		c. Trim lens (5 units)
		d. Black Clip (5 units)
		e. Clear Clip (5 units)
		f. LED (5 units)
		g. Diskette containing relevant technical literature (1 unit)
		2. Optical Mouse Designer's Kit
		a. Optical Mouse Sensor (5 units)
		b. Round lens (5 units)
		c. Trim lens (5 units)
		d. Black Clip (5 units)
		e. Clear Clip (5 units)
		f. LED (5 units)
		g. Microcontroller (5 units) - optional
		h. CD containing Agilent's technical literature and support files (1 unit)
		i. CD containing microcontroller's technical literature and support files (1 unit) - optional
		j. Complete working reference design mouse (1 unit)

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Currently, there are four different optical mouse sensors available from Agilent Technologies. These are:

No.	Part Number	Description
1.	Agilent ADNS-2030	Low power optical mouse sensor optimized for cordless mouse applications
2.	Agilent ADNS-2051	High-performance optical mouse sensor for corded and cordless mouse applications
3.	Agilent ADNS-2620	Entry-level, small form-factor, optical mouse sensor with performance features for general mouse applications
4.	Agilent ADNS-2610	Entry-level, small form-factor, optical mouse sensor for general mouse applications

Based on this guideline, the list below contains the current products and their respective list of bundles, kits and designer's kit.

Sensor Part Number	Bundle Part Number (with Round Lens)	Bundle Part Number (with Trim Lens)	Sample Kit Part Number	Ref DesignKit Part Number
ADNS-2610	ADNB-2611	ADNB-2612	ADNK-2610	
ADNS-2620	ADNB-2621	ADNB-2622	ADNK-2620	ADNK-2623
ADNS-2051	ADNB-2050	ADNB-2051	ADNK-2052	ADNK-2051
ADNS-2030	ADNB-2031	ADNB-2032	ADNK-2030	ADNK-2133

ACCESSORIES - LENSES

Lens Type	Part Number	Associated Bundles
Round	HDNS-2100	ADNB-2611
		ADNB-2621
		ADNB-2050
		ADNB-2031
Trim	HDNS-2100-001	ADNB-2612
		ADNB-2622
		ADNB-2051
		ADNB-2032

ACCESSORIES - LED ASSEMBLY CLIP

Type of clip	Part Number	Associated Products
Black	HDNS-2200	ADNS-2610
		ADNS-2620
		ADNS-2051
		ADNS-2030
Clear	HDNS-2200-001	ADNS-2610
		ADNS-2620
		ADNS-2051
		ADNS-2030

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ACCESSORIES - LED

Part Number	Associated Products
HLMP-ED80-XX000	ADNS-2610
	ADNS-2620
	ADNS-2051
	ADNS-2030

If you have any questions please contact your local Agilent representative.

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Japan: (+81 3) 3335-8152(Domestic/International), or 0120-81-1280(Domestic Only)

Korea: (+65) 6755 1989

Singapore, Malaysia, Vietnam, Thailand, Philippines, Indonesia: (+65) 6755 2044

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5989-1719EN

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TDB-ACC-NO: NB8908488

DISCLOSURE TITLE: Algorithm for Managing Multiple First-In, First-Out Queues From a Single Shared Random-Access Memory

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, August 1989, US

VOLUME NUMBER: 32

ISSUE NUMBER: 3B

PAGE NUMBER: 488 - 492

PUBLICATION-DATE: August 1, 1989 (19890801)

CROSS REFERENCE: 0018-8689-32-3B-488

DISCLOSURE TEXT:

- In the following, a technique is described for efficiently managing a plurality of first-in, first-out (FIFO) queues in a single shared random-access memory (RAM). This technique obviates the necessity for garbage collection procedures, i.e., operations to reorganize memory containing scattered records and to gather unused memory cells.
- FIFO queues can be implemented in a RAM, with associated control to maintain the head and tail pointers of each queue. When the requirement arises to implement multiple FIFO queues, the classical approach is to accomplish some physical or logical separation of the RAM and have each queue implemented in such a partition. The total required memory is then the sum of these partitions. The size of a partition is determined by the estimated maximum (or average) queue size for a particular queue. A disadvantage of this method is that the collection of queues can not effectively share the whole RAM. It is, for example, not possible that a queue which temporarily exceeds its allocated space 'steals' some RAM space from a queue which is not using its allocation. In general, this leads to a waste of RAM space, because every partition is sized for its maximum expected length. This implementation is denoted as the fixed partitioned case.
- From some operating systems, examples of queues implemented in shared RAM are known. However, the algorithms usually require a 'garbage-collection' operation to reorganize fragmented memory after some period of operation. These garbage collection operations are not suited for implementation in hardware.
- An algorithm is proposed which allows a full sharing of the total available RAM space among a set of queues. An extension to this algorithm is given which guarantees for every queue a certain amount of 'private' space. The proposed algorithm does not require garbage collection, and, therefore, lends itself easily for hardware implementation. Key to the algorithm is that the collection of not

occupied cells in the shared RAM is treated as an extra queue: for every element which leaves one of the data queues, this 'empty-queue' grows by one element, and for every element which enters one of the data queues, the empty-queue shrinks by one element.

- In the figure, a hardware implementation of the algorithm is shown. The shared data RAM 19 contains the queue elements. The n_part RAM 20 together with the data RAM 19 forms a linked list for every queue. In the n_part RAM 20 the address of the next element in a queue is found on the same address where the current element in that queue is stored. Thus, whenever an element is taken from a queue, the corresponding n_part entry points to the next element in that queue. A reading of zero indicates that the queue is empty. This holds also for the 'empty-queue', and therefore the n_part RAM 20 is initialized such that the contents of every address i point to the next address in the n_part RAM: i+1. Only the last position in the n_part RAM contains the value zero, and when this is read, there is no free data RAM 19 location left.
- Whenever data is put into the data RAM 19, the corresponding value of the n_part RAM 20 points to the next free location in the data RAM 19. This reading is saved in the n_nf register 17.
- For an initial description of the operation, disregard the Config. Mem. 9 and the nf RAM 25. Input data to queue:

Assume that input counter (inp.cnt.) 1 selects to add an element to queue 'q'. Selector 7 will select the value of the counter to select the proper queue index in the qi RAM 3 and qo RAM 6. The qi RAM 3 contains a pointer to where the last element was added to this queue. If the value is zero, this queue has currently no elements. If the value is non-zero, then comparator 14 will be used to select the value of u_nf by selector 21, and address qi(q) by selector 16, to write the pointer to this added element to the chained list for this queue. The nf_c register 27 holds the address where the data element is to be stored. This value is latched through selector 24 in u_nf register 23.

If the value of nf_c register 27 is zero, then the data RAM is full, and a FULL is signalled by comparator 28.

- At the selected address 'q' in the qi RAM 3 the value of u_nf will be written, selected by selector 2. Because there is no next element in this queue, at the corresponding address (u_nf) in the n_part RAM 20 the value zero is written. The address is selected by selector 18, the data by selector 21. Before this write occurs, the value of the addressed location in the n_part RAM 20 is saved in n_nf register 17. This value points to the next free location in the data RAM 19, and is used as the next value nf_c. At the end of the input cycle, this value is selected by selector 26 and written to nf_c register 27.
- At the same time, the output-chain for this queue is to be started, and qo RAM 6 points to the next element to be output for this queue. Only if qo(q) is zero, this qo(q) is set to u_nf. Address to qo RAM 6 is 'q', and data is selected by selector 5.
- This completes the input cycle. The following has taken place: qi(q) has been set to the address in the data RAM where this element was written. The old value of qi(q), when not zero, was used to write the pointer in the n_part RAM to the added element, thereby forming

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the chained pointer list. The value of n_part where the new element was written is used as the address for writing the next element (for any queue) in the data RAM. This entry in n_part is set to zero, to indicate the end of this queue. When qo(q) was zero, it is set to the address where this data element was stored. qo(q) is a pointer to the next element output from this queue.

- Output data from queue: Assume the output counter (out cnt.) 8 determines a queue number 'q' from which an element is to be read. Selector 7 selects the proper counter to provide the address 'q' for the qi RAM 3 and qo RAM 6. When the addressed value qo(q) is equal to zero, comparator 11 will flag EMPTY and the cycle is done.
- When this is not the case, selector 18 will select qo(q) as the address to be read, and the data is fetched from the data RAM 19. The next element in this queue is obtained from the corresponding value n_part(qo(q)) in n_part RAM 20. Selector 5 selects this value to be set into qo RAM 6. This value can be zero when there are no more elements in this queue. If this value is zero, then comperator 4 instructs to set qi(q) to zero. The original value of qo(q) is temporarily stored in qo_temp register 10. This value is now used to set the corresponding address in the n_part RAM 20 to the current value of u_nf. (For this case equal to nf_c). The cycle is finished by setting nf_c to the value stored in qo_temp register 10.
- This completes the output cycle. The following has taken place: The data item pointed to by qo(q) has been fetched from data RAM 19. If there was no next item in this queue, qi(q) has been set to zero to indicate that there are no elements in this queue for a subsequent input operation. The value of qo(q) has been set to point to the next item in the list (or zero). This pointer was obtained from the corresponding qo(q) address in the n_part RAM 20. The corresponding n_part RAM entry was set to point to the next empty location in the data RAM 19 which was obtained from u_nf. The value of nf_c has been set to the address of the just read location. Note that the 'next-free' queue is thus a sort of last-in, first-out (LIFO) queue. This ensures that if the value of u_nf is zero, there are really no empty locations in the data RAM 19.

Additional Features:

In the proposed algorithm it is possible that one of the queues in the system monopolizes the whole data RAM 19 space at the cost of the other queues: There is no effective mechanism to guarantee a minimum queue length for each queue. The additional elements in the figure, namely: nf RAM 25, Config.Mem. 9, comparators 12 and 13, and selectors 22 and 24 are used to guarantee each queue a minimum queue length at all times.

- The basic mechanism is to put some zero entries in the n_part RAM 20 and to implement a next-free pointer for every queue plus one, the last one being the next-free pointer in the 'common queue area'.
- The following example is used to clarify this operation:

Assume there are two queues, with a minimum queue length of 5 and 3 elements, respectively. The rest of the data area is common queue memory from which each queue can claim space, as required.

- The following shows the initialization of n_part RAM 20, Config. Mem. 9, nf RAM 25, and nf_c register 27:

n_part(0) = 1 Config.Mem.(0) = 8

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n_part(1) = 2 Config.Mem.(1) = 10
n_part(2) = 3
n_part(3) = 4 nf(0) = 0
n_part(4) = 5 nf(1) = 7
n_part(5) = 6
n_part(6) = 0 nf_c = 11
n_part(7) = 8
n_part(8) = 9
n_part(9) = 10
n_part(10) = 0
n_part(11) = 12
n_part(12) = 13
etc.

- Instead of selecting the nf_c pointer for every input to a queue, the 'private nf pointer' for a queue is selected from nf RAM 25 first. If this renders a value of zero, comparator 12 will detect so, and on input to a queue then the common queue memory nf_c pointer 27 is selected to set u_nf (23). If both 25 and 27 are zero, then there is no possibility to add an entry to this queue. This means that the private queue space and the common queue space are full. The difference is, however, that for another queue there can be space left in its private queue space, and it is possible to add an entry there.
- When, on an output cycle, the value returned by qo RAM 6 is greater then the fixed value in the Config.Mem. 9 for this queue, then comparator 13 will detect so, and the nf_c pointer 27 is selected to partition in the output cycle. Overhead

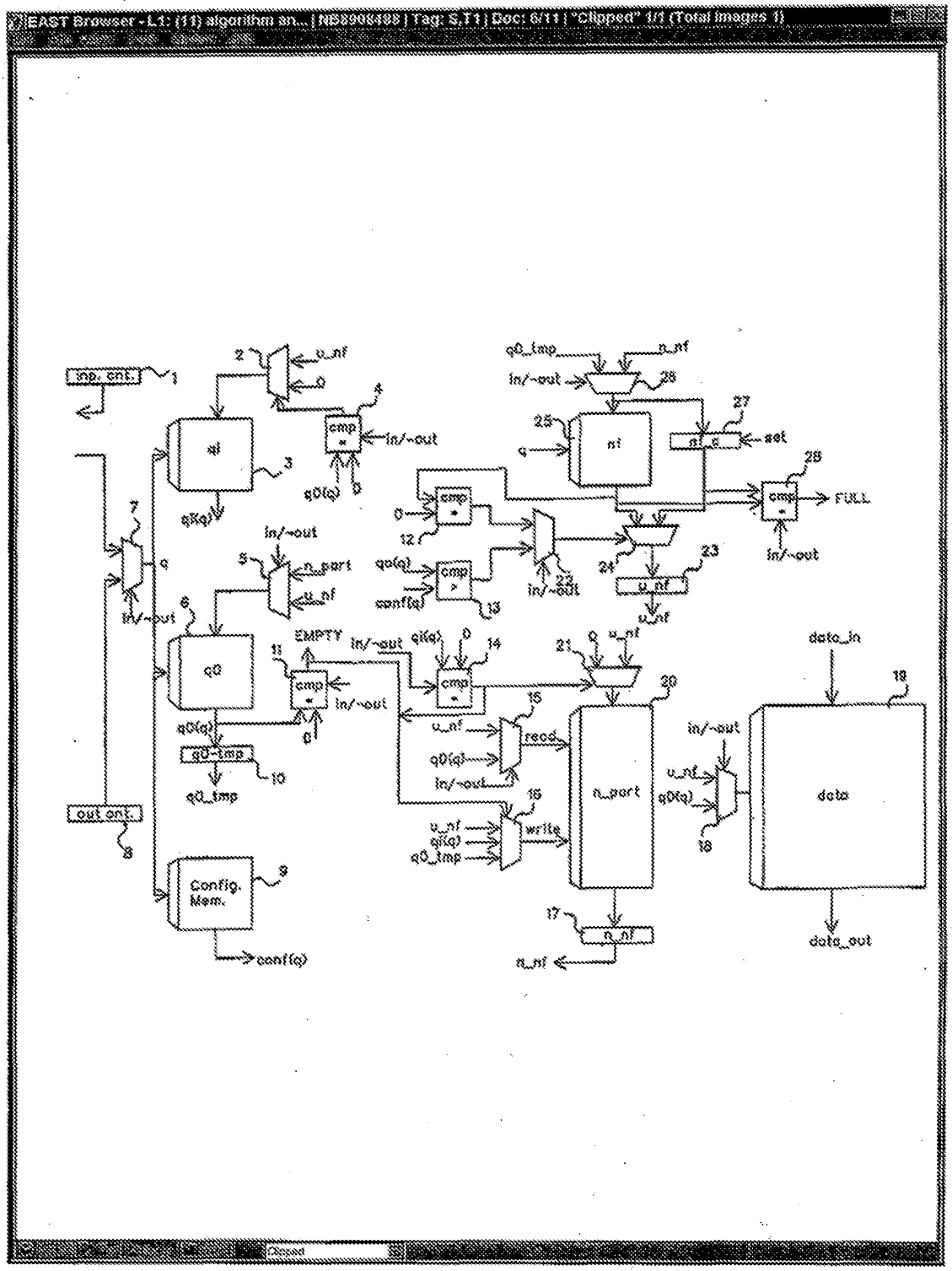
Compared to the simple case of fixed partitioning of the data RAM 19, the n_part RAM 20 is the only additional resource required. The qi RAM 3, qo RAM 6, and Config.Mem. 9 are also required to handle the pointer management in the fixed (or semi-fixed) partitioned case. The size of n_part RAM 20 is determined by the following parameters: 1) It needs the same amount of addresses as there are entries in the data RAM 19. 2) Its width must be enough to accommodate the addressing of all the entries of the data memory.

- Example: If the data RAM 19 has 1024 entries (of any given size), then the n_part RAM 20 is 10 bits wide and has 1024 entries.
- It is estimated that the additional selectors and comparators shown in the figure are comparable to those of the fixed partitioned case.

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inp. ent.
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EMPTY
FULL
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n_nf
n_port
data
data_in
data_out
conf(q)
q0_tmp
write
read
set

Am99C10A

256 x 48 Content Addressable Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **256 word x 48-bit Content Addressable Memory (CAM)**
  - Optimized for Address Decoding in Local Area Networks (LAN) and bridging applications
- **Each CAM word has a 48-bit register and 48-bit maskable comparator**
  - Maskable-bits and maskable-words
- **48-bit input word compared against all 256 words in the CAM in a single cycle**
- **Single and multiple match detection with fast on-chip priority address encoder**
- **Single cycle reset on all 256 words of the CAM Array**
- **100 nsec and 70 nsec cycle time devices available**
- **Flexible operation and diagnostics capability through user programmable control logic**
- **TTL-compatible inputs and outputs**
- **Available in a 28-pin 400 mil CERDIP, 300 mil plastic DIP and 32-pin PLCC**
- **Low power CMOS technology**
  - 880 mW max. operating power
  - 55 mW max. standby

GENERAL DESCRIPTION

The Am99C10A is a high performance Content Addressable Memory (CAM) with a capacity of 256 words and a user-programmable word width of 16 bits or 48 bits. The Am99C10A is ideal for use in high speed Ethernet and FDDI local area network applications where it can function as an address filter and perform the network address look-up function. It can also find use in Database Machines, File Servers, Image Processing, Neural Networks and many other applications.

The Am99C10A CAM is composed of 256 words, each consisting of a 48-bit comparator and a 48-bit register. A block diagram of the Am99C10A is shown below. When data (the comparand) is presented to the CAM array, a simultaneous compare operation is performed between the comparand and all data (256 words) in the CAM in a single cycle. When the comparand and a word in the CAM are matched, the on-chip priority encoder generates a match word address identifying the location of the data in the CAM. If multiple matches occur, the encoder generates the lowest matched address. Any or all bits of the comparand value can be selectively masked. The masked bits do not participate in the compare decisions, allowing comparison on a portion of the data word.

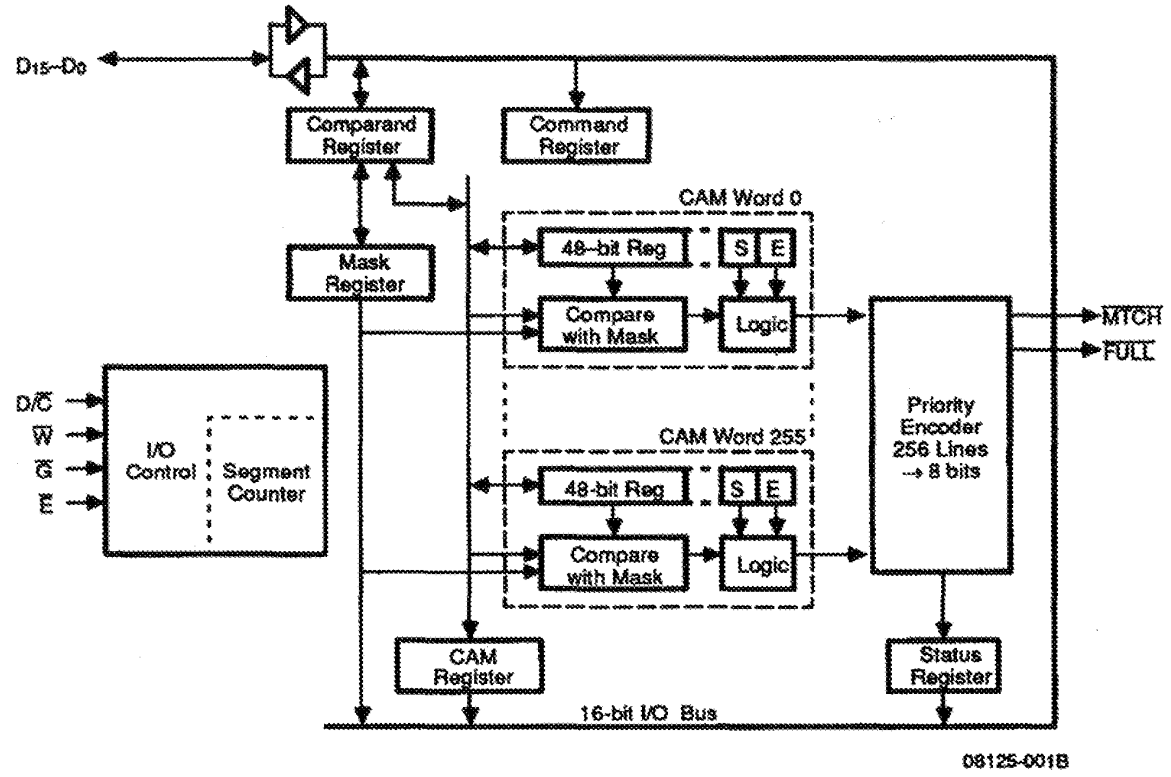
The Am99C10A is user programmable. The user can read and write to any location in the CAM Array and to all of the Am99C10A internal registers. Each word in the CAM array can be loaded with data or set to the empty state so that it does not participate in match operations. All words in the CAM Array can be set to empty in a single cycle.

The Am99C10A is manufactured with state-of-the-art CMOS processing technology. It is assembled in a 28-pin, 400 mil CERDIP, a 300 mil plastic DIP, a 32-pin PLCC package, and requires a single 5-V power supply.

Publication# 08125 Rev. F Amendment/0
Issue Date: March 1991

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BLOCK DIAGRAM

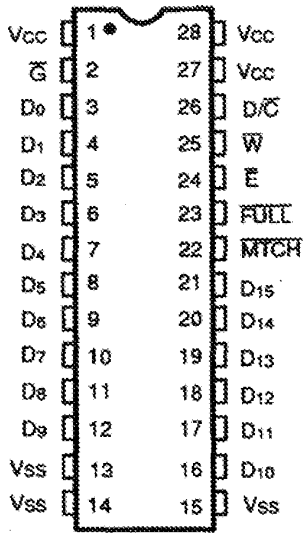


Am99C10A Block Diagram

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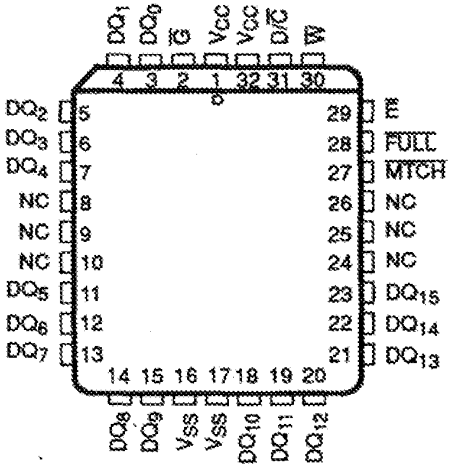
CONNECTION DIAGRAMS

DIP



08125-004A

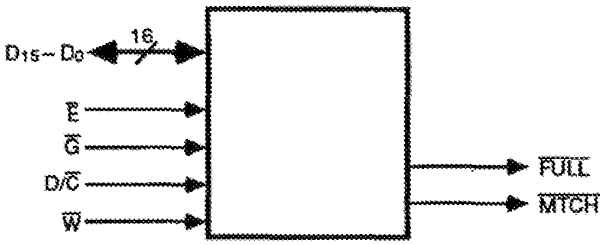
PLCC



08125-040A

Vcc = Power Supply
Vss = Ground

LOGIC SYMBOL



08125-002A

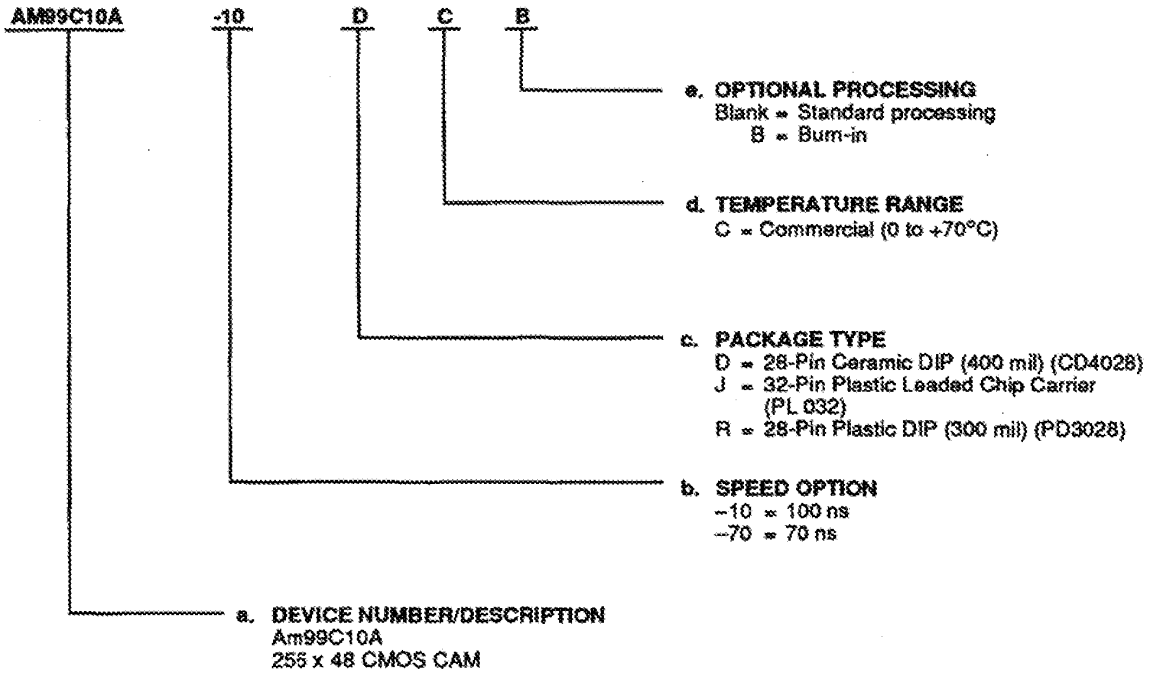
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM99C10A	RC, RCB, DC, DCB, JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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PIN DESCRIPTION

D/$\overline{C}$
Data/Command mode selection, Input, TTL

A LOW on this input selects the command mode. A HIGH on this input selects the data mode.

$\overline{W}$
Write enable, Input, TTL

This pin controls the writing of the internal registers and the CAM Array. New data may be written into a register or memory by forcing the appropriate state of D/$\overline{C}$ and $\overline{E}$, and by switching $\overline{W}$ LOW and back HIGH.

$\overline{G}$
Output Enable, Input, TTL

This pin controls reading of the internal registers. A LOW on both the $\overline{E}$ and $\overline{G}$ inputs gates the selected register onto the data bus and turns on the output drivers.

$\overline{E}$
Chip Enable, Input, TTL

A LOW on this input enables the chip operations as specified by the state of D/$\overline{C}$, $\overline{W}$, $\overline{G}$ inputs and the Command Register. A HIGH on this pin powers down the chip. This signal must be low during all operations including match.

D_{15-0}
Data Bus, 16-bit, Bidirectional, Three-state

D0 is the least significant bit position and D_{15} is the most significant bit position. A HIGH on the Data Bus specifies logic 1 and a LOW specifies logic 0. The Data Bus is not driven by the device when $\overline{W}$ is LOW, when $\overline{G}$ is HIGH or when chip enable $\overline{E}$ is HIGH.

$\overline{FULL}$
Address Full, Output, TTL

A LOW on this output indicates that all the words in the 256 address locations in CAM Array are full. A HIGH on this output indicates that one or more words in the CAM Array are still available or that the $\overline{FULL}$ output is disabled. The $\overline{FULL}$ output is in the HIGH state when $\overline{E}$ is HIGH and is valid otherwise.

$\overline{MTCH}$
Match, Output, TTL

A LOW on this output indicates that the masked data of the Comparand Register and one or more words in the CAM Array are matched. A HIGH on this output indicates that a mismatch has taken place or that the match output is disabled. The match output is in the HIGH state when $\overline{E}$ is HIGH and is valid otherwise.

V_{CC}
Power Supply Pin, Input, +5 Volts

V_{SS}
Ground Supply Pin, Input, 0 Volts

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FUNCTIONAL DESCRIPTION

The CAM ARRAY is a bank of 256 CAM words, each a combination of a 48 bit wide logic comparator and a 48 bit register, as shown in Figure 1. The CAM Array compares a 48 bit input data word against all of its 256 words simultaneously for logic equality in one cycle. If any of the CAM Array 256 words find an exact match with the incoming bit pattern, the CAM Array raises a Match flag and outputs the 8 bit address of the matching word.

When a Match cycle is initiated, every CAM word compares each bit in its register against the appropriate bit of the incoming 48 bit pattern. Additionally, a logic "1" (HIGH level) set in any Mask Register bit will disable that bit position in the CAM Array. A match is declared if all enabled CAM cells find an exact comparison with the input data. The CAM Array word that finds a match activates an internal signal called the Match Line (ML). There are 256 match lines: ML0 to ML255.

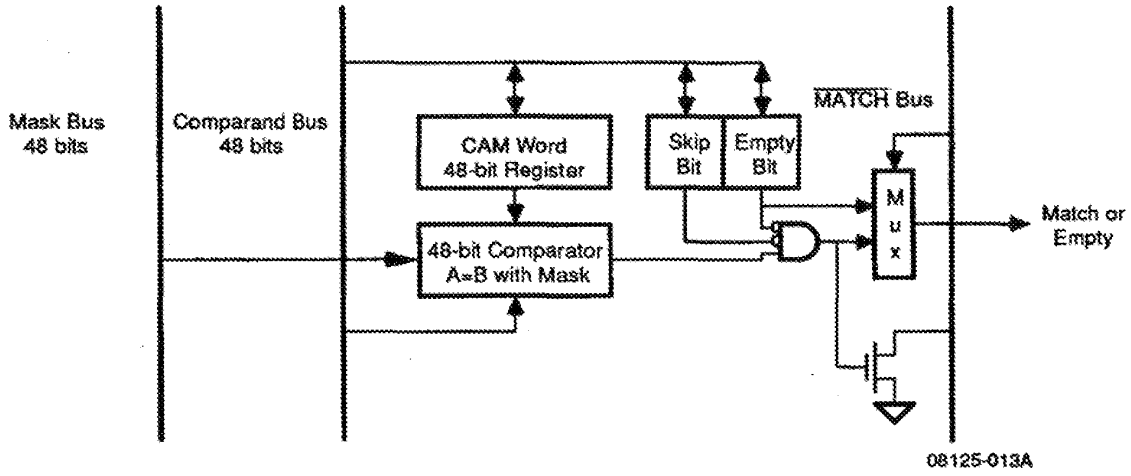


Figure 1. CAM Word Block Diagram

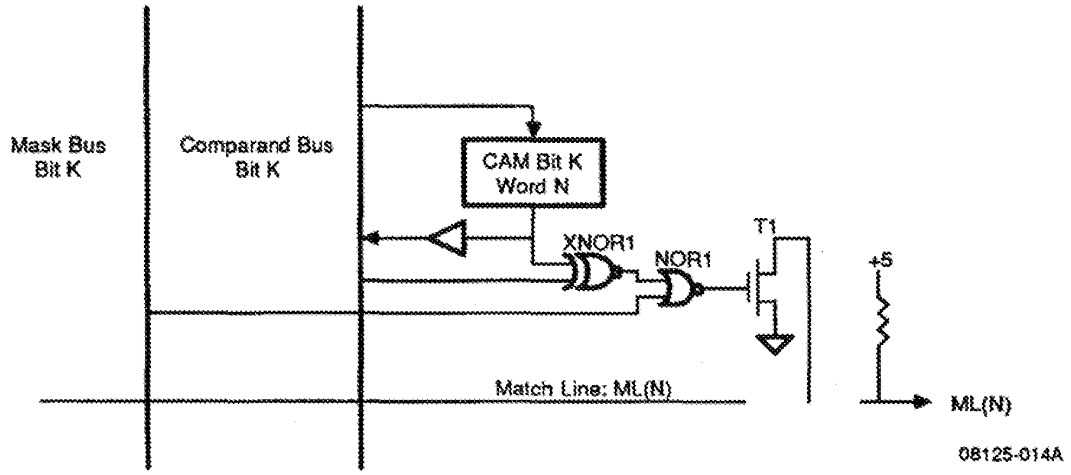


Figure 2. CAM Bit Block Diagram

Each CAM word consists of 48 CAM data bits. Each CAM data bit consists of a register bit latch, an exclusive-NOR comparator, an OR gate for masking, and a transistor for performing a 48-bit wire-AND across the 48 data bits, as shown in Figure 2. The logic comparator exclusive-Nors the contents of the register bit with the corresponding bit of the Comparand Register. A match between the two bits result in a HIGH level at the output of the exclusive-Nor gate (XNOR1). The output of XNOR1 is further gated (Nor function) with a bit of the Mask Register. A HIGH level on either one of the inputs to NOR1 forces its output LOW, indicating a match. The

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ML signal will stay HIGH (indicating a match for that CAM word) if all 48 CAM cells of this word have their T1 transistors shut off by their NOR1 gates. If any one of the 48 NOR1outputs is HIGH, the ML line will be forced LOW, indicating a mismatch.

The Priority Encoder identifies the address of the CAM word that found a match. All 256 comparators of the CAM Array receive the same bit pattern for matching at the same time, and more than one of them can find a match with the masked data. All 256 ML lines are presented to the Priority Encoder block that decides which comparator of the ones that activate their MLs has the lowest address. If at least one ML is active the Priority Encoder will activate the $\overline{\text{MTCH}}$ line and at the same time will set the $\overline{\text{MTC}}$ bit in the Status Register. The Priority Encoder will transfer the 8 bit address of the lowest matching CAM Array word to the Status Register.

Each of the 256 words of the CAM Array has two additional bits of memory associated with it – A Skip bit and an Empty bit. These are shown in the CAM Word Block Diagram. The actual size of the CAM is therefore 256 X 50 (48+2). Both the Skip and the Empty bits can disable a match for their word. The Skip bit can be used in situations where there are multiple matches – it gives the user the ability to detect additional words that were matched other than the one with the lowest address. The Empty bit indicates available or empty addresses in the CAM into which data can be written.

The Empty bit is also used by the Priority Encoder. The Priority Encoder identifies the lowest address of an Empty CAM Array word if no match occurred in any of the 256 words. If a match operation did not result in a positive match (the $\overline{\text{MTCH}}$ signal is HIGH) and if the CAM Array is not full (the $\overline{\text{FULL}}$ signal is HIGH) the Priority Encoder will generate the lowest empty address. The 8 bit empty address is accessed by reading the Status Register.

Initializing the CAM

When powering up the CAM, the data and status bits may come up at any state. Opcode 0 is used to globally set the Empty bits of the CAM to "1" and reset the Skip bits to "0". Opcode 0 may be used to empty the CAM during system operation. When command write of Opcode 0 follows a second data write of the 48-bit data write sequence, Opcode 0 must be preceded by Opcode F command write (Set Segment Counter) to ensure proper initialization.

CAM Registers - Reading and Writing

The Am99C10A has 5 programmable registers involved in data transfers. The Command and Status registers are 16 bits wide, and the Comparand, Mask and CAM registers are 48 bits wide. Figure 3. is a model of the Am99C10A registers and their interaction with each other and the CAM Array. Table 1 lists the registers and their respective data sources and destinations.

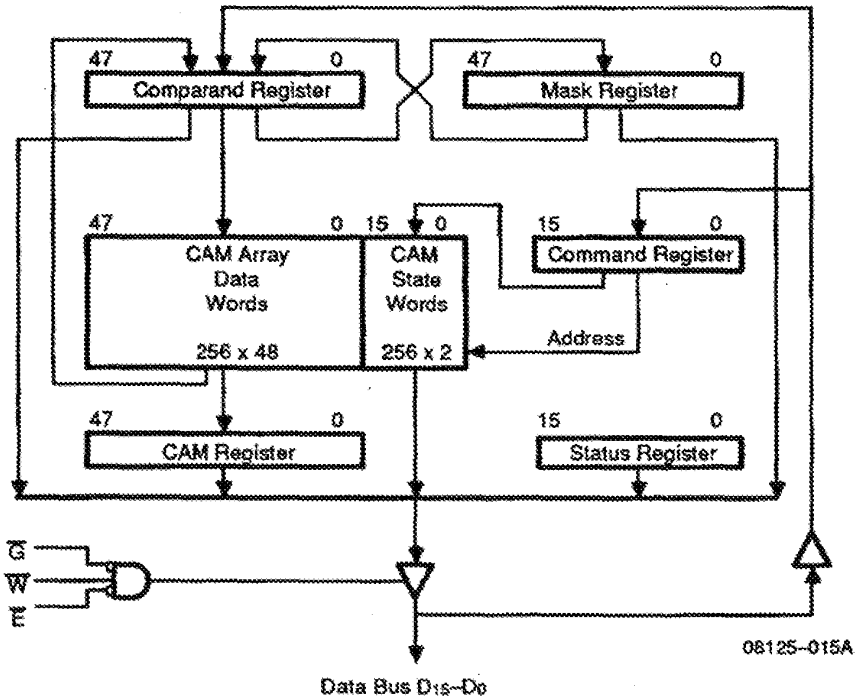


Figure 3. CAM Register Transfer Model

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Table 1. Am99C10A Registers

Register	Type	Size	Direction	Data Source	Destination
Command	Cmd	16	Input	D-Bus	—
Status	Cmd	16	Output	—	D-Bus
Comparand	Data	48	In/Out	D-Bus, CAM Array Mask Register	D-Bus, CAM Array Mask Register
Mask	Data	48	Output	Comparand Register	D-Bus, Comparand Register
CAM	Data	48	Output	CAM Array	D-Bus, Comparand Register

Data Bus Transfers

All data is transferred to and from the CAM over the 16-bit bidirectional Data Bus. Data transfer is controlled by a combination of 4 control signals ($\overline{E}$, D/$\overline{C}$, $\overline{W}$, and $\overline{G}$), as described in the Pin Description section.

Data is written into the Am99C10A by placing the data on the Data Bus and activating $\overline{W}$ and $\overline{E}$. When D/$\overline{C}$ is low (Command Write cycle), the input data is loaded into the Command Register. When D/$\overline{C}$ is high (Data Write cycle), the input data is loaded into the Comparand Register.

Data is read from the Am99C10A (output drivers enabled) when $\overline{G}$ and $\overline{E}$ are low and W is high. When D/$\overline{C}$ is low (Status Read cycle) the Status register is gated onto the Data Bus. When D/$\overline{C}$ is high (Data Read cycle) one of the data registers is gated onto the Data Bus. This register is selected by the contents of the Command register. Prior to reading, a command is loaded into the Command Register to select which of the internal registers is to be read.

Data can be read from any register by loading the appropriate command into the Command register; however, data can be written only to the Comparand register. Data to be written to the Mask register or to the CAM array must first be written into the Comparand register and transferred to the Mask register or CAM array word by writing the appropriate transfer command to the Command register.

48-bit Data Transfers

Data is transferred to and from the Am99C10A in 16-bit words. Data for the 16-bit Command and Status registers are transferred in one read or write cycle. Data for the 48-bit Comparand, Mask and CAM registers are transferred to and from the chip in three cycles. Data transfer to and from each 48-bit register is done by dividing each register into three 16-bit segments. A two-bit counter, the Segment Counter is used to select which segment of a 48-bit register is to be loaded or read.

The Segment Counter is a two-bit binary counter that counts from 0 to 2 (modulo-three). It can be preset by writing a command code of "B", "C", "D", or "F" to the Command register. In all four commands bits 10 and 11 (S0, S1) define the binary value (0,1 or 2) to be preset into the counter. Note that a value of 3 (S1,S0 = 11) in these bits will result in a value of 0 in the counter. The counter is also reset to 0 by the Initialize command, Opcode "0".

The Segment Counter is incremented after each data read or write cycle if the CAM is in the 48-bit mode. This allows a 48-bit register to be loaded or read in three successive cycles. The counter is clocked by the LOW-to-HIGH transition of $\overline{W}$ in case of a Data Write cycle and by the LOW-to-HIGH transition of $\overline{G}$ in case of a Data Read cycle.

When the Am99C10A is set to 48-bit mode, the user will normally execute 3 Data Write cycles or 3 Data Read cycles in sequence to transfer a 48 bit data word. At the end of such sequence the state of the Segment Counter is equal to its initial state before the data transfer began. This allows continuous 48-bit transfers without having to preset the Segment Counter between words. This is useful in the CAM's normal operating mode of checking a stream of 48-bit words for a match.

Note that reading a 16-bit State word requires only one cycle. If the CAM is in the 48-bit mode, this data read operation will increment the Segment Counter. Any subsequent cycles that use the Segment Counter have to take this into account.

16-bit Mode Data Transfers

In 16 bit mode the Segment Counter is not incremented and it points to one of the three segments of the Comparand, Mask and CAM Registers. Writing and reading the selected segment of those registers is achieved in one cycle. However, internal transfers between the registers and the CAM Array as well as the Match operation are done on all 48 bits.

CAM Array-Reading and Writing

To write a word into the CAM Array, the data is first loaded into the Comparand register and then transferred from the Comparand register to the register in the selected CAM word by executing a transfer command.

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The transfer command is executed by writing a command word (command code = 6 or E) into the Command register. The transfer command contains the address of the CAM word to be written.

To read a word from the CAM Array, data is transferred from the CAM array to either the Comparand or CAM registers by writing the appropriate command (command code = 7 or D, respectively) into the Command register. The transfer command contains the address of the CAM word to be read. The CAM Array word is then read from the register selected by the command.

Writing into the Skip or Empty bit in a CAM word is done directly by writing the appropriate command code (command code = 9 or A, respectively) into the Command register. The command word contains the value of the Skip or Empty bit to be written and the address of the CAM word containing the bit.

The same command codes (9 or A) which are used to set a specific Skip or Empty bit can also be used to set all Skip or Empty bits in the CAM array. If bit 11of these command words is a one, the address portion of the command is ignored and the value of the Skip or Empty bit is written into all words of the CAM array. This is useful in clearing all Skip and Empty bits.

The Skip and Empty bits of a CAM word are also cleared to zero when data is written into the CAM using command code E. This allows writing a new word of data into an empty CAM word without requiring an extra cycle to clear the Skip and Empty bits.

The Skip and Empty bits of all CAM words can be preset to the empty state by writing an Initialize command (command code = 0) to the Command register. Initialize clears all Skip bits to zero and sets all Empty bits to one, corresponding to an empty CAM condition.

To read the Skip and Empty bits of a word from the CAM Array, the State Memory is selected as the source of data driving the Data Bus by writing the appropriate command (command code = 5) into the Command register. That command contains the address of the CAM word whose state is to be read. The State word (i.e., the Skip and Empty bits of the CAM Array word) are then read directly. Reading the State word requires only one Data Read cycle.

Match Operations

Comparison of data in the Comparand against the 256 words of data in the CAM array is called a match operation. The result of a match operation is a match address which appears in the Status register and the activation of the $\overline{\text{MTCH}}$ and $\overline{\text{FULL}}$ flags.

A match operation can be initiated by writing a command into the Command register or by writing data into the Comparand register. A match operation begins after a single data write to the Comparand Register in 16-bit mode or after three data write cycles to the Comparand Register in 48-bit mode. Note that the $\overline{\text{E}}$ line must be kept low for the match time, t_{WMPE} or t_{WMPE48} after write start to allow the match to occur.

If a match occurs, the $\overline{\text{MTC}}$ bit is set in the Status register and the $\overline{\text{MTCH}}$ pin is activated if it has been enabled. The address of the word that matched appears in the lower 8 bits of the Status register. If more than one match occurs, the $\overline{\text{MUL}}$ bit is set in the status register, indicating a multiple match. In this case, the match address is that of the match word with the lowest numerical address. If no match occurs, the $\overline{\text{MTC}}$ bit and $\overline{\text{MTCH}}$ flag are not set, and the address is that of the first empty word, i.e. the empty word with the lowest address.

Both $\overline{\text{MTCH}}$ flag and $\overline{\text{MTC}}$ bit change their state upon 16-bit and 48-bit data write cycles, and upon command write cycle for commands 9 and A. Commands 3, 4, 6, 7 and E change the state of the $\overline{\text{MTC}}$ bit only but do not affect the physical $\overline{\text{MTCH}}$ flag.

The match flag access time is measured from a high-to-low transition of $\overline{\text{W}}$ to the transition of $\overline{\text{MTCH}}$ flag. The state of the $\overline{\text{MTCH}}$ flag changes after the high-to-low transition of the $\overline{\text{W}}$ line on the third data write in the 48-bit mode, on each high-to-low transition of $\overline{\text{W}}$ in 16-bit mode, and after each high-to-low transition of $\overline{\text{W}}$ for command writes which initiate a match. (See Table 2.)

Match and Full Flags

The Am99C10A has two output signals that indicate its status - Full, $\overline{\text{FULL}}$ and Match, $\overline{\text{MTCH}}$.

The Full signal, $\overline{\text{FULL}}$, indicates whether the CAM Array is full or not. A low level on $\overline{\text{FULL}}$ indicates that all 256 words of the CAM Array are full. A HIGH on this output indicates that one or more words in the CAM Array are still available or that the $\overline{\text{FULL}}$ output is disabled. The $\overline{\text{FULL}}$ output can be disabled (= HIGH) under program control or when the chip is disabled (Chip Enable $\overline{\text{E}}$ is high).

The Match signal, $\overline{\text{MTCH}}$, indicates whether a match has been detected, i.e. that the masked data of the Comparand Register and one or more words in the CAM Array are matched. A HIGH on this output indicates that a mismatch has taken place or that the match output is disabled. The $\overline{\text{MTCH}}$ output can be disabled (= HIGH) under program control or when the chip is disabled (Chip Enable $\overline{\text{E}}$ is high).

Status Register Format

The Status register shows the results of match operations and the contents of the Segment Counter. The State Register is read onto the Data Bus by executing a Status Read cycle. Since it takes time to encode a match address (t_{WMPE}), the Status Read cannot immedi-

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