ately follow a Command Write cycle or a Data Write cycle if a valid match address is sought. A time delay of (t_{WMPE}) after the last command or data write before reading the Status register will guarantee proper address encoding. A Status Read operation does not affect the state of the flags or other register contents.

The Status Register has 3 fields - the Address field (A_0 - A_7), the Segment Counter State (S0 - S1) and the Flags field ($\overline{MTC}$, $\overline{MUL}$ and $\overline{FUL}$), as shown in Figure 4.

$\overline{MTC}$

A LOW on $\overline{MTC}$ (D_{15}) indicates that at least one word in the CAM Array and the masked data of the Comparand Register are matched. A HIGH indicates that no word in the CAM Array found a match. The $\overline{MTC}$ bit is the same as the match output signal $\overline{MTCH}$ during data writes and commands 9 and A.

$\overline{MUL}$

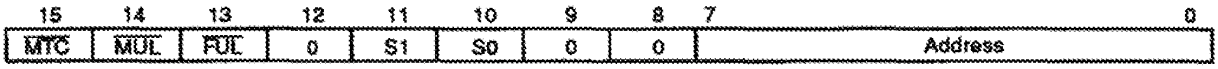
A LOW on $\overline{MUL}$ (D_{14}) indicates that two or more words in the CAM Array match the masked data of the Comparand Register. It is activated during a Match operation and latched by an internal clock at the end of the Match cycle.

$\overline{FUL}$

A LOW on $\overline{FUL}$ (D_{13}) indicates that the CAM Array is full. The $\overline{FUL}$ flag is the same as the full output signal $\overline{FULL}$ except the $\overline{FUL}$ flag cannot be disabled. It is activated during a Match operation and latched by an internal clock at the end of the Match cycle.

S1, S0

The Segment Counter bits (S0 - S1) are driven by the two flip-flops that comprise the Segment Counter. These two bits (D_{10} and D_{11}) reflect the current state of the Segment Counter.



08125-017A

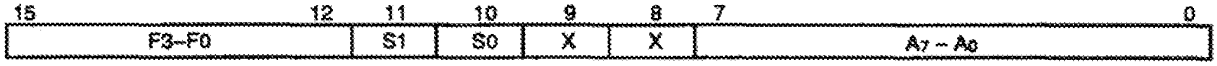
Figure 4. Status Word Bit Assignment

A_7-A_0

Lowest address of the matched word in the CAM when data in the Comparand Register and the data in the CAM are matched ($\overline{MTCH}$ = L, $\overline{MTC}$ = L and $\overline{FULL}$ = don't care). Lowest address of empty 48-bit word in the CAM when data is mismatched and the CAM is not full ($\overline{FULL}$ = H). Address is undefined when data is mismatched and CAM is full. After initialize, A_7 – A_0 holds the value FF (Hex). Once a data read or write or a command write is executed, A_7 – A_0 holds the address of the first match or the first empty location.

Command Register Format

The Am99C10A can execute a variety of commands. Each command is executed by writing the appropriate command word to the Command register. All commands are executed during the write pulse applied to the the write clock, $\overline{W}$. The format of the Command Register is shown in Figure 5, and a summary of the commands is shown in Table 2.



08125-018A

F3-F0: A 4 bit Instruction Code which defines one of sixteen commands.

S0 - S1: Modifier bits for the various commands.

A_0 - A_7: An Address field which selects one of the 256 CAM Array data or State words.

Bits 8, 9: Not used.

Figure 5. Command Register Bit Assignment

Sandisk Technologies, Inc. - Ex. 1002, Page 000475

Table 2. 99C10A Command Summary

Op Code	Operation		S1	S0	A_0-A_7	Start Match
0	Initialize		X	X	X	X
1	Flag Output control enable/disable		MTCH	FULL	X	X
2	16/48 bit Mode Select		48-bit	X	X	X
3	Comparand Reg. --> Mask Reg		X	X	X	Start
4	Mask Reg. --> Comparand Reg.		X	X	X	Start
5	SIM --> Data Bus		X	X	CAM State	X
6	Comparand Reg. --> CAM Array		X	X	CAM Data	Start
7	CAM Array --> Comparand Reg.		X	X	CAM Data	Start
8	Reserved		X	X	X	X
9	Skip Control	Per Word All Words	0 1	Skip Skip	CAM State X	Start
A	Empty control	Per Word All Words	0 1	Empty Empty	CAM State X	Start
B	Comparand Reg. --> Data Bus		Segment Counter		X	X
C	Mask Reg. --> Data Bus		Segment Counter		X	X
D	CAM Array --> CAM Reg. --> Data Bus		Segment Counter		CAM Data	X
E	Comparand Reg. -->CAM Array, clear S +E		X	X	CAM Data	Start
F	Set Segment Counter		Segment Counter		X	X

Sandisk Technologies, Inc. - Ex. 1002, Page 000476

Am99C10A COMMAND DESCRIPTIONS

Op Code 0
Initialization

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	Not Used											

08125-019A

All Skip-bits are set to "0" (LOW level) meaning–don't skip, and all Empty-bits are set to "1" (HIGH level) meaning-empty. This is equivalent to resetting the CAM Array. The $\overline{MTCH}$ and $\overline{FULL}$ outputs are enabled. The mode is set to 48-bit mode. The Mask Register and Segment Counter are reset to zero. Subsequent data writes and reads are to and from the Comparand Register.

Op Code 1
Flag Output Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	S1	S0	Not Used									

08125-020A

This command controls the enable and disable of the $\overline{FULL}$ and $\overline{MTCH}$ status output pins. The S0 and S1 fields of this command are latched into the control logic. Once loaded, they control the status output pins $\overline{FULL}$ and $\overline{MTCH}$ as follows: When S0 is 0, the $\overline{FULL}$ output is disabled and remains unconditionally HIGH. When S0 is 1, the $\overline{FULL}$ output is enabled and may be asserted when $\overline{E}$ is low. When S1 is 0, the $\overline{MTCH}$ output is disabled and remains unconditionally high. When S1 is 1, the $\overline{MTCH}$ output is enabled and may be asserted if $\overline{E}$ is low.

Op Code 2
Mode Select

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	S1	Not Used										

08125-021A

This command sets the 99C10 into the 16-bit or 48-bit mode. The S1 bit in the command is loaded into the 16/48-bit mode control register. The 16-bit mode is enabled when S1 is 0, and the 48-bit mode is enabled when S1 is 1. The Am99C10A will remain in the mode selected until another Command Write is executed with Op Code "0" or "2".

Op Code 3
Move Comparand Register to Mask Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	Not Used											

08125-022A

The 48-bit contents of the Comparand Register is loaded into the Mask Register. The Segment Counter is not affected. A Match cycle will begin automatically following this command.

Op Code 4
Move Mask Register to Comparand Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	Not Used											

08125-023A

The 48-bit contents of the Mask Register is loaded into the Comparand Register. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Sandisk Technologies, Inc. - Ex. 1002, Page 000477

Op Code 5

Enable Output from State Memory to Data Bus

15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
0	1	0	1	Not Used	$A_7 - A_0$

08125-024A

This command selects a State word in the CAM Array as the source of data to be read. The Skip-bit and Empty-bit appear on bits D_{14} and D_{15} of the Data Bus, all other bits of the bus are driven LOW. The Segment Counter is not changed.

Op Code 6

Move Comparand Register to CAM Array

15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
0	1	1	0	Not Used	$A_7 - A_0$

08125-025B

The 48-bit contents of the Comparand Register are written into the CAM Array data word. The 16/48 bit mode select setting does not affect this instruction. The Empty-bit and Skip-bit in the State Memory are not changed. The CAM Array address is specified by the Command Register address field. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Op Code 7

Move CAM Array to Comparand Register

15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
0	1	1	1	Not Used	$A_7 - A_0$

08125-026A

The 48-bit contents of the CAM Array data word specified by the address field are loaded into the Comparand Register. The Segment Counter is not changed. The State Memory is not changed. The 16/48 bit mode select setting does not affect this instruction. A Match cycle will begin automatically following this command.

Op Code 8

Reserved

15	14	13	12	11 10 9 8 7 6 5 4 3 2 1 0
1	0	0	0	Not Used

08125-027A

Op Code 9

Skip-bit Control

15	14	13	12	11	10	9 8	7 6 5 4 3 2 1 0
1	0	0	1	0	S0	Not Used	$A_7 - A_0$

08125-028A

When bit 11 in the Command Register is LOW, S0 is loaded into the Skip-bit within the State word location specified by the Command Register address field. A Match cycle will begin automatically following this command.

15	14	13	12	11	10	9 8 7 6 5 4 3 2 1 0
1	0	0	1	1	S0	Not Used

08125-029A

When bit 11 in the Command Register is HIGH, S0 is loaded into all skip-bit memory locations. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Sandisk Technologies, Inc. - Ex. 1002, Page 000478

Op Code A

Empty-bit Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	S0	Not Used		$A_7 - A_0$							

08125-030A

When bit 11 in the Command Register is LOW, S0 is loaded into the Empty-bit within the State word location specified by the Command Register address field. A Match cycle will begin automatically following this command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	1	S0	Not Used									

08125-031A

When bit 11 in the Command Register is HIGH, S0 is loaded into all Empty-bit memory locations. The Segment Counter is not changed. A Match cycle will begin automatically following this command

Op Code B

Enable Output from Comparand Register to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	S1	S0	Not Used									

08125-032A

This command selects the Comparand Register as the source of data to be read. The S0 and S1 data in the Command Register are clocked into the Segment Counter at the end of this Command Write cycle. When S0 and S1 are both 0 or both 1, the Segment Counter is reset to zero. Subsequent Data Read operations result in data flowing from the Comparand Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle will automatically increment the modulo-three Segment Counter.

Op Code C

Enable Output from Mask Register to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	S1	S0	Not Used									

08125-033A

This command selects the Mask Register as the source of data to be read. The S0 and S1 data in the Command Register are clocked into the Segment Counter at the end of this Command Write cycle. When S0 and S1 are both 0 or both 1, the Segment Counter is reset to zero. Subsequent Data Read operations result in data flowing from the Mask Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle will automatically increment the modulo-three Segment Counter.

Op Code D

Move CAM to CAM Register, Enable Output from CAM Register to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	S1	S0	Not Used		$A_7 - A_0$							

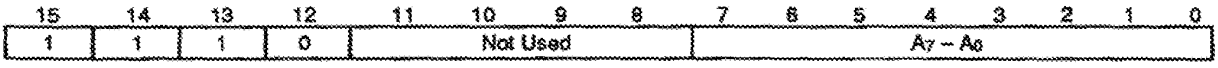
08125-034A

This command selects the CAM Register as the source of data to be read. The S0 and S1 data in the Command Register are moved to the Segment Counter. When S0 and S1 are both 0 or both 1, the Segment Counter is reset to zero. The CAM Array word specified by the address field is transferred to the CAM Register. Subsequent Data Read operations result in data flowing from the CAM Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle automatically increments the modulo-three Segment Counter.

Sandisk Technologies, Inc. - Ex. 1002, Page 000479

Op Code E

Move Comparand Register to CAM (Set Empty-bit and Skip-bit LOW)

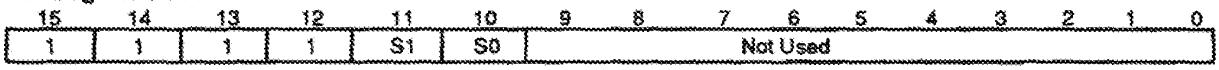


08125-035A

The 48-bit contents of the Comparand Register is written into the CAM Array data word specified by the address field. The 16/48 bit mode select setting does not affect this instruction. Both the Empty-bit and the Skip-bit in the State Memory address specified by the Command Register address field are set cleared to zero (Not Empty and Don't Skip). The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Op Code F

Set Segment Counter



08125-036B

This command clocks the data in S1, S0 into the Segment Counter. When S1, S0 are both 0 or both 1, the Segment Counter is reset to 0.

Typical Command Sequences

The following are examples of some common sequences of commands. Most command sequences assume segment counter set to zero.

Power-up Initialization

After power-up, the CAM must be initialized. This is done by executing the Initialize command. All the CAM words are reset to the empty state, and the device is set up in the 48-bit mode. Another command is needed if the16-bit mode is desired.

For 48-bit mode:

Command Write 0000 = Initialize (16/48 mode is set automatically to 48 bit mode)

For 16-bit mode:

Command Write 0000 = Initialize (16/48 mode is set automatically to 48 bit mode)
Command Write 2000 = Mode Select (S1=0, Set mode to 16 bit)

Loading CAM Array with Data

After initialization, the CAM must be loaded with data in order to be used. Since all locations are initialized to the empty state, the CAM can be loaded starting from address zero. This is done by loading the Comparand register and writing a command with an op code of E, which will transfer the data to a specified CAM word and clear the Skip and Empty bits of that word.

Filling the CAM in the 48-bit mode is normally done using the following command sequence:

Set Segment Counter to zero
Data Write (D_{15} -- D_0 --> Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Command Write E0XX = Comparand Register -->CAM Array + Clear S+E
(Repeat for every CAM Array word to be loaded.)

Sandisk Technologies, Inc. - Ex. 1002, Page 000480

Filling the CAM in the 16-bit mode is done using the following command sequence:

Set Segment Counter to zero
Command Write BX00 = Comparand Register -->Data Bus (Load Segment Counter)
Data Write (D_{15} -- D_0 -->Comparand Register) (segment selected by counter)
Command Write E0XX = Comparand Register -->CAM Array + Clear S+E (all 48 bits are written).

Repeat the last two steps for every CAM Array word to be loaded.
Repeat all three steps when a different 16 bit segment is to be loaded.

Load Mask Register

The mask register is loaded by writing the data into the Comparand Register and then writing a command to transfer the data from the Comparand register to the Mask register.

Set Segment Counter to zero
Data Write (D_{15} -- D_0 -->Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Command Write 3000 = Comparand Register -->Mask Register

48-Bit Compare for Match (48-bit Mode)

To perform a match operation on new data, the data to be tested is written into the Comparand register, time is allowed for the match operation to be performed, and then the match flag and match address are read from the Status register. Note that no special command is required to start the match: it begins after the last word is loaded into the Comparand register.

Set Segment Counter to zero
Data Write (D_{15} -- D_0 -->Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Allow time for Match operation
Check $\overline{MTCH}$ output pin after t_{WMAF48} or t_{WMA}; Status Read,
check bits 13, 14 and 15 ($\overline{MTC}$, $\overline{MUL}$, $\overline{FUL}$) after t_{WMAF48} or t_{WMPE}.

Check for Multiple Matches

Typical match operations yield a single match. Some applications, however may yield multiple matches. In this case, the addresses of each match may be read by successively reading the current lowest address, setting its Skip bit, and reading the next lowest address, etc., until no matches are left.

Status Read, bit 15 ($\overline{MTC}$) = 0, bit 14 ($\overline{MUL}$) = 0
Status bits 7-0 contain the address of the lowest word in the CAM that found a match.
Read and save the match address, use it to form the next command

Command Write 94XX = Skip Control - F(9), set bit 11(S1) = 0, set bit 10 (S0) = 1(Skip),
Set the Skip bit: Command bits 7-0 to the lowest matching word address.

Wait for the next Match operation to complete and the Status register to settle
Status Read
Check $\overline{MTC}$ for match, save the address if $\overline{MTC}$ =0
Status bits 7-0 contain the address of the lowest word in the CAM that found a match.
Read and save the match address, use it to form the next command

Repeat the last three steps until there are no more matches

Sandisk Technologies, Inc. - Ex. 1002, Page 000481

Finding and Loading an Empty Location

A CAM word may be empty since initialization or it can be declared empty by setting its Empty bit. Data is added to the CAM by finding an empty location and writing into it. This is done by loading the data to be written into the Comparand register and checking for a match. If the data is not already stored in the CAM, the match operation will respond with the address of the lowest empty word. The address of the empty location may be used to write the new data into the CAM. If a match is found, a copy of the data already exists in the CAM.

Set Segment Counter to zero
Data Write (D_{15} -- D_0 -->Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Allow time for Match operation and priority encode.
Status Read, check bits 15 ($\overline{MTC}$) should be 1, and 13 ($\overline{FUL}$) should be 1,
  Bits 0-7 contain the address of the lowest empty word in the CAM.
Command Write E0XX = Comparand Register -->CAM Array + Flags,
  Bits 0-7 should have the address of the empty word from the Status Read.

Reading Data

To read the contents of a word in the CAM Array

Command Write D0XX = CAM Array -->CAM Register -->Data Bus,
Bits 0-7 indicate the address of the word to be read.
Data Read - (CAM Register (15-0) -->D_{15} - D_0)
Data Read - (CAM Register (31-16) -->D_{15} - D_0)
Data Read - (CAM Register (47-32) -->D_{15} - D_0)

Example of a Command Sequence

Table 3 shows the control signals, data bus contents and Segment Counter contents for a typical command sequence. The sequence consists of initialization, filling the CAM Array, and loading the Mask Register. A data pattern is then loaded into the Comparand Register, a match is executed and the sequence terminates with the reading of the Status Register.

Sandisk Technologies, Inc. - Ex. 1002, Page 000482

Table 3. Command Sequence Example

Cycle Type	Instruction	$\overline{E}$	D/$\overline{C}$	W	$\overline{G}$	Data Bus (Hex)	Segment Counter Before	Segment Counter After	Operation
Command Write	Initialize	L	L	C	H	0XXX	XX	00	Set default conditions (repeat)
Data Write	——	L	H	C	H	3210	00	01	D_{15}–D_0 ⟶ Comparand Reg (15–0)
Data Write	——	L	H	C	H	7654	01	10	D_{15}–D_0 ⟶ Comparand Reg (31–16)
Data Write	——	L	H	C	H	BA98	10	00	D_{15}–D_0 ⟶ Comparand Reg (47–32)
Command Write	Comparand Reg. ⟶ CAM	L	L	C	H	E000	00	00	"BA9876543210" into CAM word 0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Data Write	——	L	H	C	H	1111	00	01	D_{15}–D_0 ⟶ Comparand Reg (15–0)
Data Write	——	L	H	C	H	2222	01	10	D_{15}–D_0 ⟶ Comparand Reg (31–16)
Data Write	——	L	H	C	H	4444	10	00	D_{15}–D_0 ⟶ Comparand Reg (47–32)
Command Write	Comparand Reg. ⟶ CAM	L	L	C	H	EOFF	00	00	"444422221111" into CAM word 255
Data Write	——	L	H	C	H	00FF	00	01	D_{15}–D_0 ⟶ Comparand Reg (15–0)
Data Write	——	L	H	C	H	0000	01	10	D_{15}–D_0 ⟶ Comparand Reg (31–16)
Data Write	——	L	H	C	H	FF00	10	00	D_{15}–D_0 ⟶ Comparand Reg (47–32)
Command Write	Comparand Reg. ⟶ Mask Reg.	L	L	C	H	3000	00	00	"FF00000000FF" into Mask Register
Data Write	——	L	H	C	H	7654	00	01	D_{15}–D_0 ⟶ Comparand Reg (15–0)
Data Write	——	L	H	C	H	BA98	01	10	D_{15}–D_0 ⟶ Comparand Reg (31–16)
Data Write	——	L	H	C	H	FEDC	10	00	D_{15}–D_0 ⟶ Comparand Reg (47–32)
Wait (Match)	——	L	X	H	H	XXXX	00	00	Compare "XXDCBA9876XX" against CAM
Wait (Encode)	——	L	X	H	H	XXXX	00	00	Encode match address ⟶ Status reg
Status Read	——	L	L	H	C	Status	00	00	Check Flags

L = LOW
H = HIGH
C = LOW going pulse

CAM Applications

Content Addressable Memory (CAM) devices have many potential applications. The availability of high density CAM devices such as the Am99C10A will allow many applications to be developed which were not practical in the past because of lack of CAM devices. Some of these application areas are:

Local Area Network (LAN) bridge address filtering
Local Area Network (LAN) ring message insertion and removal

Data base machine support - Search and sort accelerators
Pattern recognition - String search engines, etc.
Image processing and machine vision - Pattern recognition, Image registration, etc.
Neural net simulation
AI language support - (LISP, etc.) garbage collection support, PROLOG accelerators, etc.

Sandisk Technologies, Inc. - Ex. 1002, Page 000483

Local Area Network Bridge Address Filtering

Bridges between high speed Local Area Networks (LAN) provide a good example of CAM use. A LAN bridge provides transparent communication between two networks. An example is a bridge between a 100MBit/second FDDI network and an Ethernet network. A block diagram of such a network system is shown in Figure 6, and a block diagram of the bridge is shown in Figure 7.

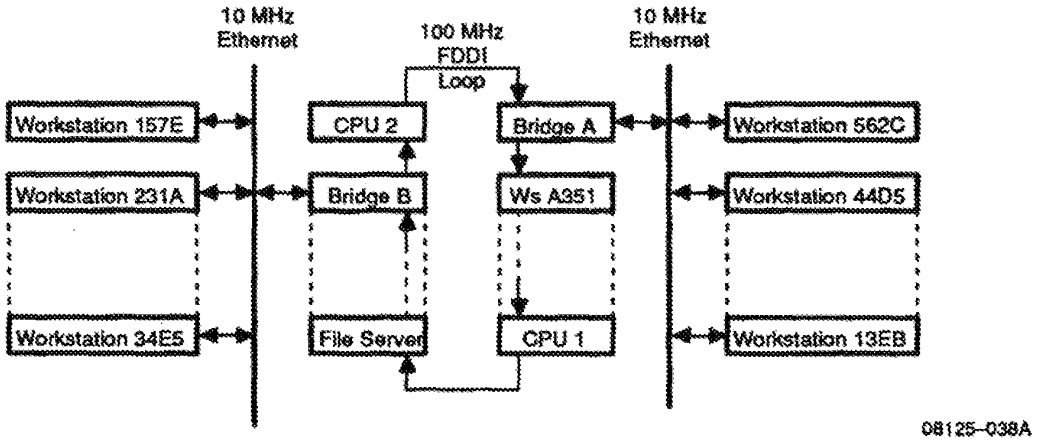


Figure 6. FDDI-Ethernet Network System

The function of the FDDI-Ethernet bridge is to pass messages between the two networks in order to allow the various workstations to communicate. Messages are sent according to unique 48-bit addresses assigned to each workstation. Each message contains the source address and the destination address. The notations shown in the workstation boxes in Figure 6 are assumed to be examples of these addresses: e.g. 157E, 231A, etc.. F

Let us assume that workstation 562C sends a message to workstation 231A. In order for this to occur, the first FDDI-Ethernet bridge must pass along the address to the FDDI loop. The second bridge must recognize that the message is for one of the workstations on its Ethernet LAN and pass it along to workstation 231A.

The problem for the FDDI-Ethernet bridge is to recognize-in time-that the message is for a station on its Ethernet LAN and no other. There could be 4000 workstations on the Ethernet LAN. This means that the bridge must check the message destination address against 4000 addresses in order to determine whether to accept the message and pass it on to the Ethernet.

Sandisk Technologies, Inc. - Ex. 1002, Page 000484

Address identification must be done quickly. The message acceptance decision must be made before the arrival of the next message, i.e. within the minimum message time. If the minimum message length is 9 bytes on a 100 mbit/sec FDDI network, the decision must be made in 720 ns, including 480 ns to acquire the address. The Am99C10A can do the job in 480+100=580 ns. At these speeds, the Am99C10A is not only effective, it is the only practical, cost effective approach.

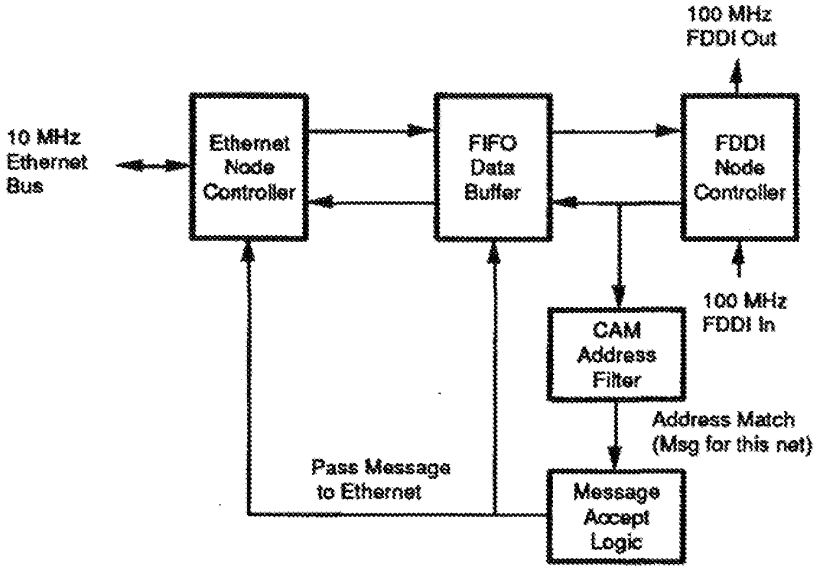


Figure 7. FDDI-Ethernet Bridge Block Diagram

Sandisk Technologies, Inc. - Ex. 1002, Page 000485

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Voltage on Any Pin with Respect to GND	–0.5 to + 7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to + 70°C
Supply Voltage (V_{CC})	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS are valid over the operating range unless otherwise specified. All values are guaranteed maximum type limits.

Parameter Symbol	Parameter Description	Test Conditions	70 ns		100 ns		Unit
			Min.	Max.	Min.	Max.	
I_{OH}	Output High Current	V_{OH} = 2.4 V, V_{CC} = 4.5 V	–1.6		–1.6		mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V	+2.4		+2.4		mA
V_{IH}	Input High Voltage		2.2	V_{CC} + .5	2.2	V_{CC} + .5	V
V_{IL}	Input Low Voltage	(Note 3)	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		2.0		2.0	µA
I_{OZ}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{E} \ge V_{IH}$ or $\overline{G} \ge V_{IH}$		2.0		2.0	µA
I_{CC1}	Static Operating Supply Current	$\overline{E} \ge V_{IL}$		70		70	mA
I_{CC2}	Dynamic Operating Supply Current, 48-bit mode	Cycle = 48-bit Data Write		140		110	mA
I_{CC3}	Dynamic Operating Current, 16-bit mode	Cycle = 16-bit Data Write $\overline{E} \ge V_{IL}$, f = 1/t_{WC}		160		130	mA
I_{SB1}	Standby Current TTL Input Levels	$\overline{E} \ge V_{IH}$ V_{CC} Max.		10		10	mA
I_{SB2}	Standby Current CMOS Input Levels	$\overline{E} \ge (V_{CC} - 0.2\ V)$; $V_{IN} \le 0.2$ V or $V_{IN} \ge (V_{CC} - 0.2)$		10		10	mA

Sandisk Technologies, Inc. - Ex. 1002, Page 000486

AC CHARACTERISTICS

Parameter Symbol	Parameter Description (Note 2)	70 ns		100 ns		Unit	Notes
		Min.	Max.	Min.	Max.		
Common Parameters							
t_{DCS}	D/$\overline{C}$, $\overline{E}$ setup before read or write	0		0		ns	
t_{DCH}	D/$\overline{C}$, $\overline{E}$ hold time after read or write	0		5		ns	
Read Cycle Parameters							
t_{RC}	Read cycle time	70		100		ns	
t_{RP}	Read cycle pulse width	45		75		ns	4
t_{RR}	Read recovery time	20		25		ns	
t_{OLZ}	Output enable time to low Z	10		10		ns	1,3,4
t_{OHZ}	Output disable time to high Z	5	30	5	30	ns	1,3
t_{RA}	Read access time		45		65	ns	
t_{FA}	Flag enable time		25		30	ns	1,6
t_{FH}	Flag disable time		25		30	ns	1,6
Write Cycle Parameters							
t_{WC}	Write cycle time	70		100		ns	
t_{WP}	Write pulse time	40		75		ns	4
t_{WR}	Write recovery time	25		25		ns	
t_{WDS}	Data setup time before write	3		3		ns	
t_{WDH}	Data hold time after write start	15		80		ns	5
t_{WMA}	Match flag access after write start		125		175	ns	5,6,7
t_{WFA}	Full flag access after write end		70		100	ns	6,7
t_{WMPE}	Priority encode after write start		140		200	ns	5
Write Cycle Parameters – 48-Bit Data Write Mode Only							
t_{WC48}	Write cycle time	60		100		ns	
t_{WP48}	Write pulse width	25		75		ns	4
t_{WMAF48}	Match flag access after write start		90		175	ns	5,6,7
t_{WMPE48}	Priority encode after write start		100		200	ns	5

Notes:

1. Parameter guaranteed by design and characterization data but not 100% tested.
2. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified IOL/IOH and load capacitance (see test load A in switching test circuits) unless otherwise noted. Output timing reference is 1.5 V.
3. Test load B. Disable time is measured as the time to a ±500 mV change from prior output level.
4. $\overline{W}$ and $\overline{G}$ may not overlap: i.e., may not both be low at the same time (while $\overline{E}$ is low).
5. Data hold and match timings with respect to leading edge of $\overline{W}$.
6. Test Load C applies.
7. A $\overline{G}$ HIGH to LOW transition will cause the $\overline{MTCH}$ and $\overline{FULL}$ flags to be in an undefined state for a period = t_{RA}.

CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Max.	Unit
C_I	Input Capacitance	f = 1 MHz, V_{IN} = 0 V	5	pF
C_{IO}	Input/Output Capacitance	f = 1 MHz, V_{IO} = 0 V	7	pF

Notes:

1. These parameters are guaranteed by characterization but not tested. Measurements performed at T_A = +25°C.

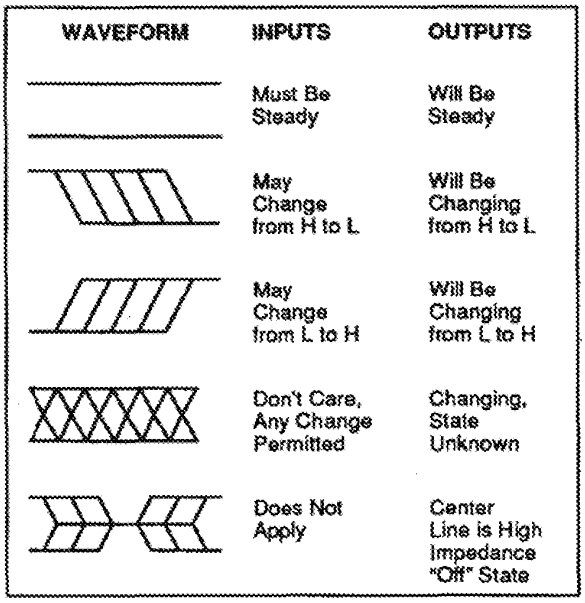
Sandisk Technologies, Inc. - Ex. 1002, Page 000487

Data Transfer Control Signals

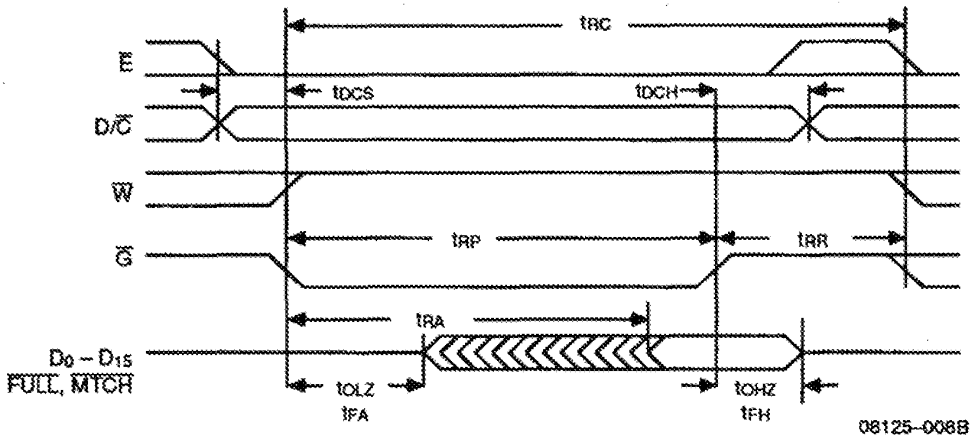
OPERATION MODE	CONTROL SIGNALS				DATA BUS	SUPPLY CURRENT
	$\overline{E}$	D/$\overline{C}$	$\overline{W}$	$\overline{G}$		
Command Write	L	L	L	H	Data In	I_{CC1}, I_{CC2}
Data Write	L	H	L	H	Data In	I_{CC1}, I_{CC2}, I_{CC3}
Status Read	L	L	H	L	Data Out	I_{CC1}, I_{CC2}
Data Read	L	H	H	L	Data Out	I_{CC1}, I_{CC2}
Output Disabled	L	X	H	H	Hi – Z	I_{CC1}
Standby	H	X	X	X	Hi – Z	I_{SB1}, I_{SB2}
Invalid	L	X	L	L	Hi – Z	—

Sandisk Technologies, Inc. - Ex. 1002, Page 000488

KEY TO SWITCHING WAVEFORMS



SWITCHING WAVEFORMS



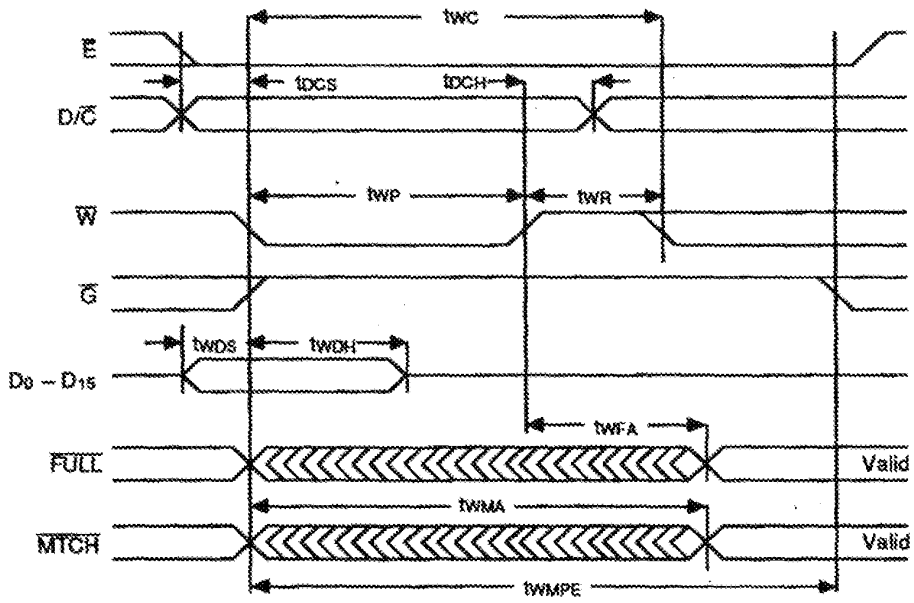
Note:

t_{OLZ} and t_{OHZ} may be measured from $\overline{E}$ transitions provided $\overline{G}$ is Low.

Read Timing Diagram

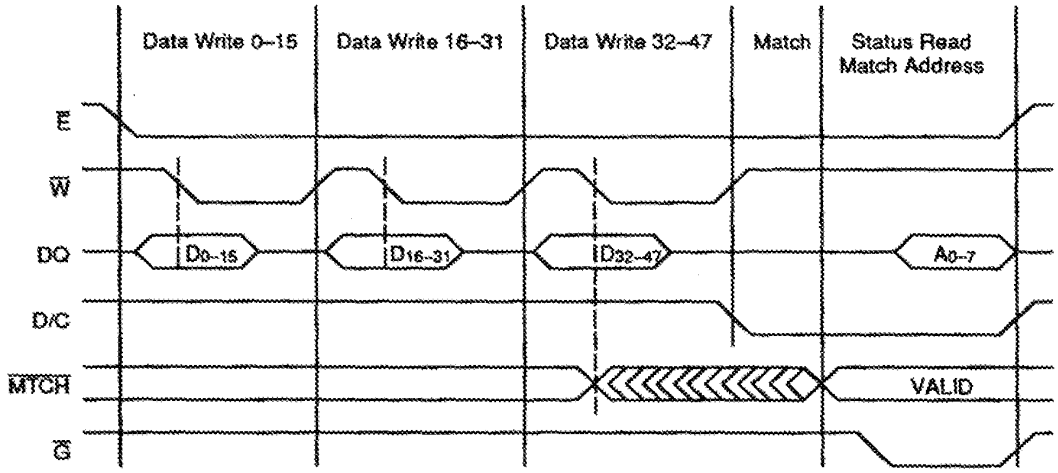
Sandisk Technologies, Inc. - Ex. 1002, Page 000489

SWITCHING WAVEFORMS



08125-009B

Write Timing Diagram

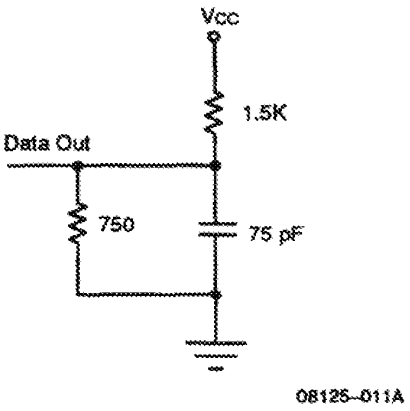


08125-010B

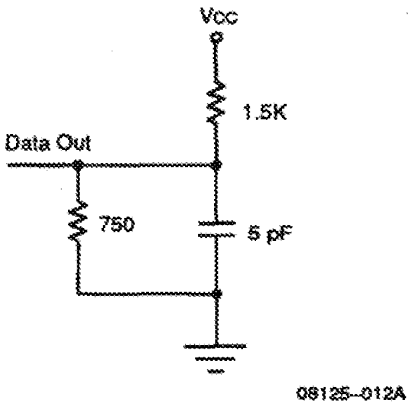
Match Timing Diagram (Reference)

Sandisk Technologies, Inc. - Ex. 1002, Page 000490

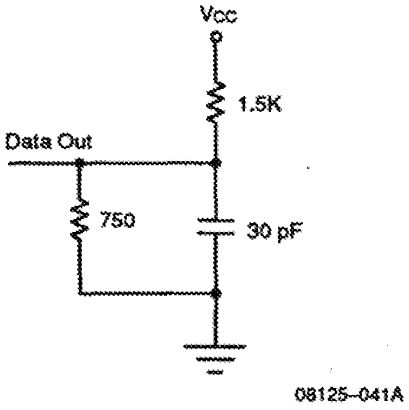
SWITCHING TEST CIRCUITS



Test Load A



Test Load B



Test Load C

Sandisk Technologies, Inc. - Ex. 1002, Page 000491

An Analog PLL-Based Clock and Data Recovery Circuit with High Input Jitter Tolerance

SAM YINSHANG SUN, MEMBER, IEEE

Abstract—A clock and data recovery circuit for a T1 network is described. A fully integrated PLL extracts the carrier signal embedded in the data. Two trimming DAC's simultaneously bring the VCO center frequency and the PLL closed-loop bandwidth to their specified values. A triple sampler captures the jittering data and aligns them with the recovered clock. The input jitter tolerance of this circuit is three times more than previously reported PLL-based circuits.

I. Introduction

RECENT advances in the Integrated Service Digital Network (ISDN) have made its realization for the general public a likely prospect in the near future. For its primary rate interface, 1.544 Mbit/s in the U.S. and 2.048 Mbit/s in Europe, a higher input jitter tolerance requirement has been newly imposed demanding better performance of its line interface unit (LIU). This requirement challenges the performance of the key circuit block in the LIU, namely the clock and data recovery circuit, to a greater level.

Clock and data recovery circuits can be categorized into three types: *LC* tuned tank, digital PLL-based, and analog PLL-based circuits. The *LC* tank requires tuning of the external components and is sensitive to the data pattern. The digital PLL suffers high-speed phase "hit" on its output which is inherent to the scheme. The analog PLL can be fully integrated and provides a smooth clock output. Nevertheless, the performance of the analog PLL-based circuit needs to be optimized. Designed to be highly tolerant of input jitter, this paper describes a fully integrated analog PLL-based clock and data recovery circuit in a monolithic LIU using novel techniques to meet the performance challenge.

II. Circuit Description

The circuit shown in Fig. 1 is constructed with a signal slicer to convert the alternate mark inversion (AMI) signal into a return-to-zero (RZ) signal, a charge-pump PLL to extract the carrier clock embedded in the input data stream, and a triple sampler to capture the jittering data and align them with the recovered clock (RCLK). A frequency comparator is also included to monitor the PLL lock-in status.

A. Charge-Pump Phase-Locked Loop

As illustrated in Fig. 2 the PLL consists of a data-activating frequency/phase detector (FPD), a charge-pump loop filter (LF), and a current-controlled relaxation oscillator (ICO) [1]. Two current DAC's are used to trim the VCO center frequency and the PLL closed-loop bandwidth respectively. The FPD compares the phase difference between the RZ data and VCO output RCLK and steers the LF current sources to charge or discharge the large capacitor C. The voltage change on C will then drive the VCO output frequency to a direction to reduce the phase difference. The small capacitor C_2 is used to suppress the ripple in the charge-pump LF.

The capture range of this PLL is approximately the same as the VCO frequency range because the frequency/phase detector shown in Fig. 3 compares not only the phase difference, but also the frequency difference. When a pulse is present on RZ data this FPD will be activated as follows: if the phase of RZ data leads the RCLK phase, the UP output will be ON for a duration proportional to the phase difference; if RZ data lags RCLK, the DOWN output will be ON in the same fashion. The output logic prevents the UP/DOWN outputs from being ON simultaneously. This FPD has 1 bit of memory to keep the last comparison result that will eliminate an output phase jump at the beat frequency when the two input signals have different frequencies. When no pulse appears on RZ data, these two outputs will be deactivated and the VCO is free running until the next pulse comes.

The VCO consists of two parts. One is a relaxation ICO; its output frequency is controlled by its input current I_p as shown in Fig. 4. Two identical holding capacitors and auto-reset comparators provide near 50-percent duty cycle on clock output without a dividing counter. The VCO center frequency is switchable from 1.544 to 2.048 MHz by changing the trigger level of the comparators. The other part of the VCO is a 4-bit current DAC with VCO input

Manuscript received September 2, 1988; revised December 13, 1988.
The author is with the Semiconductor Product Division, Rockwell International, Newport Beach, CA 92660.
IEEE Log Number 8826245.

0018-9200/89/0400-0325$01.00 ©1989 IEEE

Sandisk Technologies, Inc. - Ex. 1002, Page 000492

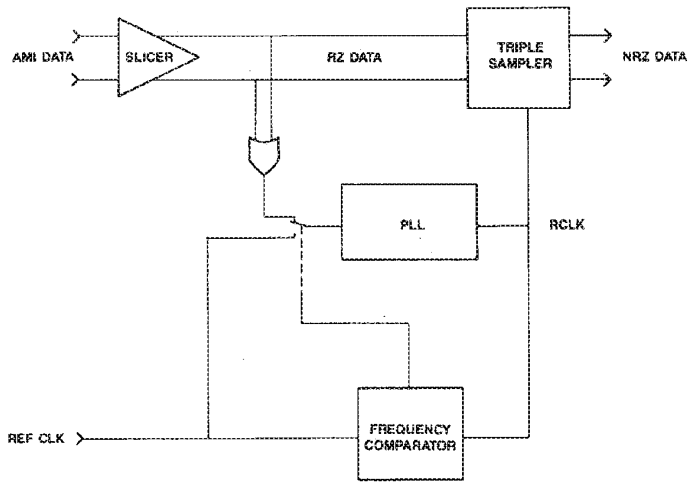


Fig. 1. Functional block diagram.

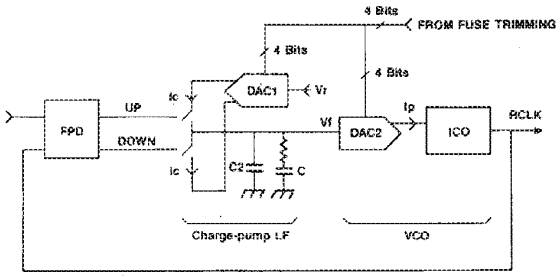


Fig. 2. Charge-pump PLL block diagram.

voltage V_f as its reference voltage. This DAC functions as a programmable voltage-to-current converter to adjust the transfer curve between the input voltage V_f and output current I_p to the ICO under different digital input codes. The VCO center frequency f_o and VCO gain K_o are delineated in the expressions below:

$$f_o = \frac{1}{2V_T} \cdot \frac{I_p}{C_h} \tag{1}$$

$$K_o = 0.8\pi \cdot f_o. \tag{2}$$

The other DAC is used in the charge-pump loop filter with a preset reference voltage V_r to provide a suitable injecting current I_c to determine the PLL closed-loop bandwidth which can be expressed by (3) [1]:

$$f_n^2 = \frac{K_o}{8\pi^3} \cdot \frac{I_c}{C} \tag{3}$$

$$\xi = \pi R C f_n. \tag{4}$$

The PLL is a second-order loop of which the damping factor ξ is determined in (3) by the resistor R, capacitor C, and PLL closed-loop bandwidth f_n. The two DAC's are made identically in the circuit and layout with the intention to adjust these key circuit parameters.

Two inherently conflicting aspects were considered when deciding the PLL closed-loop bandwidth. Stable locking to a random data stream needs a narrow bandwidth while a reliable data recovery demands a wide bandwidth to enable RCLK to quickly track the jittering data phase instance. The key performance characteristic of a clock/data recovery circuit is its input jitter tolerance. The input jitter tolerance is the maximum amount of phase jittering on an input data stream tolerable by the circuit that still recovers the clock and data from input. Fig. 5 shows the input jitter tolerance of a conventional PLL-based circuit with different closed-loop bandwidths. It is apparent that the wide loop bandwidth yields better performance in low jitter frequencies below 10 kHz while the narrow loop bandwidth produces a better result in higher frequencies.

B. Triple Sampling Data Recovery

To alleviate the dilemma of choosing the PLL closed-loop bandwidth, a triple sampler for data recovery was developed in an attempt to relax the phase tracking requirement. Instead of sampling the RZ signal only at 90° as the conventional approach, the triple sampler samples at 0°, 90°, and 180° as shown in Fig. 6. Whichever sampler detects a ONE, the output will be ONE due the characteristic of the RZ signal. This scheme makes the acceptable instantaneous phase error between the RZ signal and RCLK as high as 180° in contrast to the 90° from the conventional approach. The closed-loop bandwidth was then chosen to be 8 kHz for optimal jitter performance. Fig. 7 shows the measured PLL phase jitter frequency response (i.e., PLL phase-transfer function).

III. Circuit Adjustment

The circuit integration on silicon demands adjustments for the VCO center frequency and the PLL closed-loop bandwidth to compensate for the large component varia-

Sandisk Technologies, Inc. - Ex. 1002, Page 000493

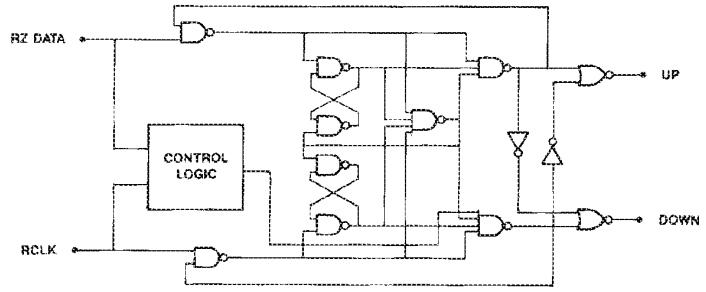


Fig. 3. Schematic of data activating frequency/phase detector.

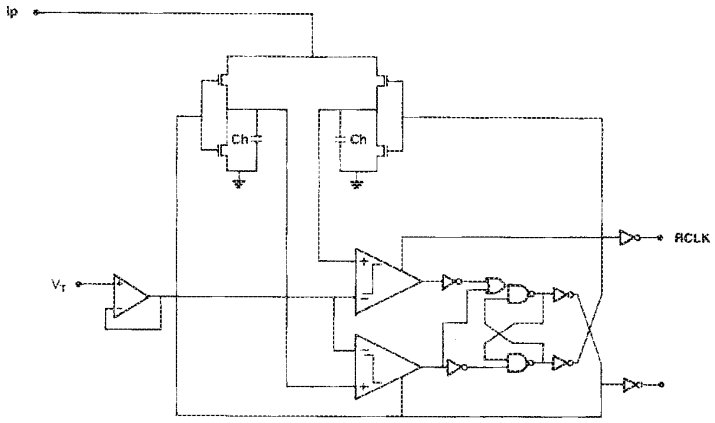


Fig. 4. Schematic of current-controlled oscillator (ICO).

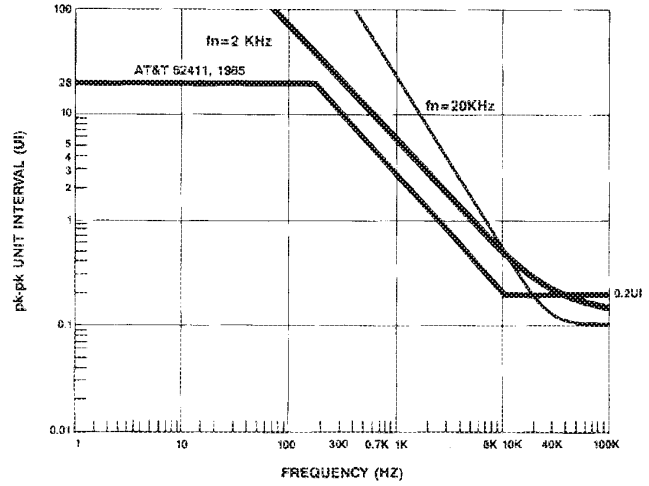


Fig. 5. Input jitter tolerance of the prototype with different PLL closed-loop bandwidth.

tions in MOS fabrication process. In mass production measuring the VCO center frequency is fast but measuring the PLL closed-loop bandwidth takes a relatively long time. Instead of calibrating them separately, a new technique was developed to complete the two tasks with one trimming. Two identical current DAC's were used to trim these two key parameters. At the wafer test stage, the on-chip polysilicon fuses were blown according to the VCO frequency measurement. The resulting digital code controlled the VCO current DAC to adjust the transfer

Sandisk Technologies, Inc. - Ex. 1002, Page 000494

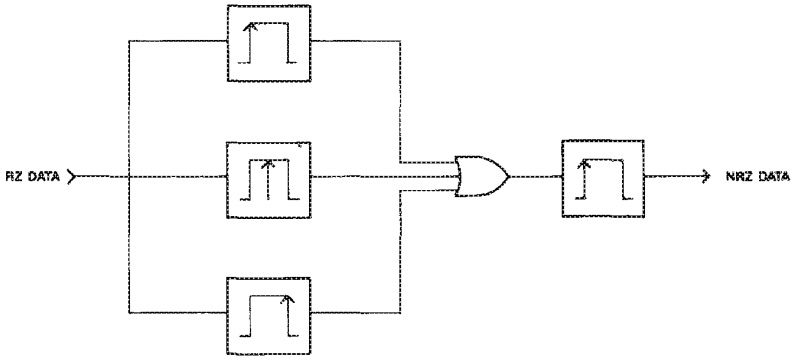


Fig. 6. Triple sampler data recovery.

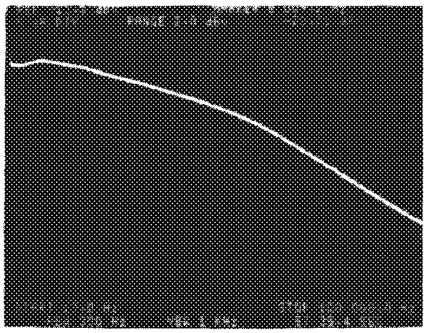


Fig. 7. Measured PLL phase jitter frequency response to a random data input.

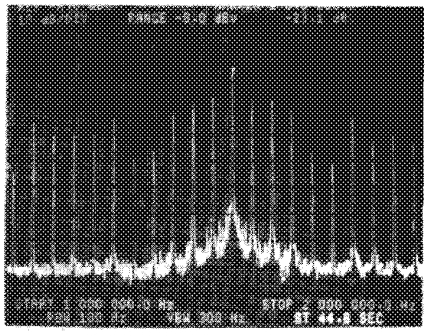


Fig. 8. Frequency spectrum of a repetitive data pattern.

curve between the VCO input voltage and the charging current I_p which allows the VCO to oscillate at the desired frequency. The same digital code was also used to change the current DAC of the charge-pump LF to adjust the charging current I_c which, in turn, centered the PLL closed-loop bandwidth to a predetermined frequency.

The correlation between these two adjustments is apparent when examining the mechanisms of the VCO frequency and the formation of the PLL closed-loop bandwidth. As expressed in (1) the VCO center frequency f_o is proportional to its charging current I_p divided by capacitance C_h. The PLL closed-loop bandwidth f_n^2 (see (2)) is also proportional to its charging current I_c divided by holding capacitance C. The input voltages of the two identical DAC's in the VCO and LF are equal by design and by definition. With the same digital input code the ratio of the DAC's output current I_p to I_c is approximately constant within the precision of component matching in the process. That is,

$$I_p/I_c = A \tag{5}$$

where A is a constant. Therefore, the PLL closed-loop bandwidth is derived as

$$f_n^2 = \frac{0.2V_T}{A\pi^2} \cdot \frac{C_h}{C} \cdot f_o^2. \tag{6}$$

Thus, trimming I_p by a certain percentage to let f_o reach a desired value will also change I_c by the same percentage, consequently making f_n come near the predetermined bandwidth. This is accomplished by the simultaneous control of the two identical DAC's used in the VCO and the charge-pump LF circuits.

IV. Anti-Harmonic Lock Technique

One inherent danger in the analog PLL-based clock and data recovery circuit is the PLL being locked onto the subharmonic of the data carrier frequency, especially when the data pattern is repetitive. The spectrum of a repetitive data pattern shown in Fig. 8 has local peaks at a subharmonic frequency near the peak of the carrier frequency. A commonly used scheme is to limit the VCO frequency range to within 6 or 7 percent of the center frequency to avoid locking onto the frequency outside the VCO range [2]. This scheme provides only limited protection to subharmonic locking and is useless to subharmonic locking within the VCO range. The nearest local peak on Fig. 8 is about 3 percent away from the carrier frequency, where the PLL was observed to be locked onto it in the prototype experiment. Further reduction of the VCO range creates problems under different operating conditions and temperatures.

Sandisk Technologies, Inc. - Ex. 1002, Page 000495

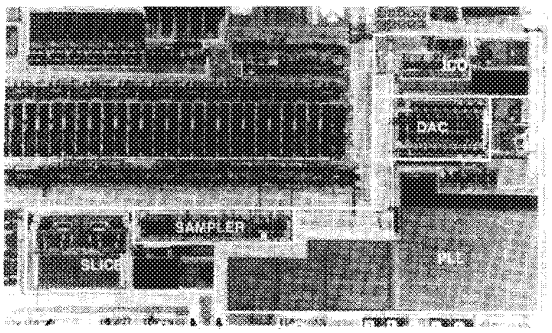


Fig. 9. Die photo of the clock and data recovery circuit.

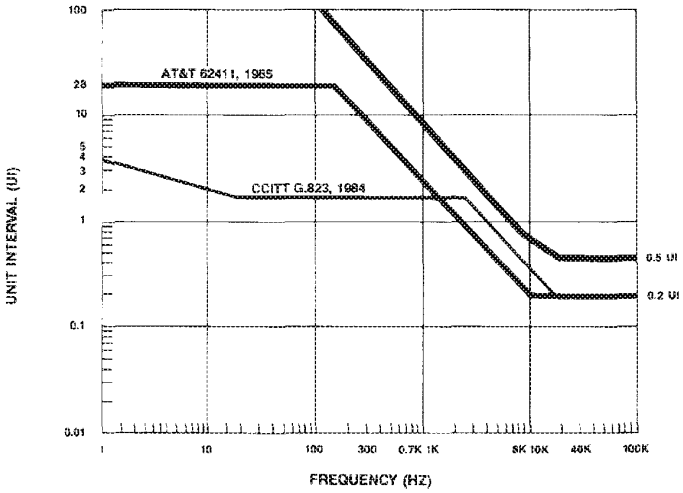


Fig. 10. Input jitter tolerance to a random data input.

A unique technique was developed to detect and correct potential subharmonic locking. As shown in Fig. 1 a frequency comparator was added to monitor the recovered clock RCLK against a precision reference clock also derived from the data stream. If the RCLK frequency deviates from the reference frequency, it will be declared abnormal and the PLL input will be switched to the reference clock for training and then switched back to the RZ data stream. Since the trained VCO clock is very close to the carrier frequency of the data it will easily lock onto it. Thus, instead of resisting the subharmonic locking, this circuit detects the subharmonic locking and corrects it.

V. Experimental Result

This circuit was realized with a 3-μm bulk CMOS process and occupied 5500 mil^2. A die photo of this circuit is shown in Fig. 9. The input jitter tolerance given in Fig. 10 exceeds the requirement of the newly revised AT&T pub. 62411 "High Capacity Digital Service Interface Specification" [3]. The high jitter frequency tolerance is at least three times better than previously reported PLL clock and data recovery circuits [2]. The performance is summarized in Table I.

TABLE I
Device Characteristics

Technology	CMOS 3 micro double poly
Power Supply	5 V ± 10%
Power Consumption	25 mW (typical)
Silicon Area	5500 mil^2
Allowable Instant Phase Error	± 0.47 UI
PLL loop Bandwidth	8 KHz ± 1 KHz
Pull-in Time	< 300 us
Tolerance to "0" stream	300 "0"s (typical)
Intrinsic Jitter Output	0.01 UI (All "1" input) 0.015 UI (Random data)
Max. Static Phase Error	15°

VI. Conclusion

A high input jitter tolerance was achieved in this analog PLL-based clock and data recovery circuit. The task of making the circuit system stable and fast data phase cap-

Sandisk Technologies, Inc. - Ex. 1002, Page 000496

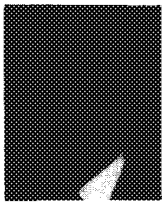
turing was accomplished by adjusting the key PLL parameters and using a novel data recovery circuit. Full integration in CMOS technology makes this circuit a useful functional block which can be incorporated easily into VLSI systems.

Acknowledgment

The author would like to express his gratitude to S. Hao and Dr. K.-L. Lee for their suggestions and encouragement. The author would also like to thank R. R. Co for the initial work on the PLL architecture.

References

[1] F. M. Gardner, "Charge-pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, pp. 1849–1858, Nov. 1980.
[2] K. J. Stern, N. S. Sooch, D. J. Knapp, and M. A. Nix, "A monolithic line interface circuit for T1 terminals," in *ISSCC Dig. Tech. Papers*, 1987, pp. 292–293.
[3] AT&T PUB 62411, "High capacity digital service interface specification," 1985.
[4] S. Y. Sun, "A PLL based clock and data recovery circuit with high input jitter tolerance," in *Proc. IEEE CICC*, 1988, pp. 9.7.1–9.7.3.



Sam Yinshang Sun (S'85–M'86) was born in Beijing, China, in 1957. He studied electrical engineering at the Beijing Normal University, Beijing, for two and a half years before he transferred to the University of California, Irvine, where he received the B.S. degree (Cum Laude, Dean's honor) and the M.S. degree in electrical engineering in 1984 and 1986, respectively.

Since 1984 he has worked as a Design Engineer for Precision Monolithics Inc. on data acquisition IC and for Rockwell International on CMOS process development and on analog IC for ISDN systems. He is currently a member of the technical staff in the Semiconductor Product Division of Rockwell International, Newport Beach, CA. His interests include the design of analog and digital integrated circuits with particular interest in circuits for telecommunication systems.

Sandisk Technologies, Inc. - Ex. 1002, Page 000497

An EEPROM for Microprocessors and Custom Logic

ROGER CUPPENS, CORNELIS D. HARTGRING, MEMBER, IEEE, JAN F. VERWEY, HERMAN L. PEEK, FRANS A. H. VOLLEBREGT, ELISABETH G. M. DEVENS, AND INGRID A. SENS

—An EEPROM extension to a 2.5-μm n-well CMOS technology developed. In this technology an EEPROM has been designed suitable for integration with (existing) microprocessors in a 5-V technology. A 2K EEPROM memory module, usable as a block in a cell library for custom logic measures 3.2 mm² with a cell area of 440 μm².

I. INTRODUCTION

RECENT YEARS there has been an increase in for microprocessor chips with (electrically) programmable nonvolatile memories [1], for use program store or data store. These devices are made by redesigning an existing microprocessor it suitable for a high-voltage (E)EPROM technol- procedure is not only time consuming but also the speed of the device.

paper presents a different approach: a 5-V-only has been designed into a low-voltage CMOS so that only a few extra processing steps have ed to the baseline process. These steps do not device characteristics nor the minimum design s of the process. So to add nonvolatile memory ting design (e.g., a microprocessor) no redesign d processing and increased design rules is needed ced of the original design is retained.

low-voltage EEPROM cell will be discussed, as el circuit techniques that enable the EEPROM at internal voltages up to the junction break- Also some measured data on a 2K EEPROM odule, suitable for addition to a cell library for c, will be presented.

II. EEPROM MEMORY CELL

ventional floating gate EEPROM memory cell consists of an access transistor and a floating y transistor. The gate of this transistor is capac- pled to a control gate (CG) which is etched in a lysilicon layer. The memory transistor is programmed by Fowler–Nordheim tunneling of electrons through a thin oxide layer (< 200 Å) [2] between the gate and the drain of this transistor (Fig. 1(a): injector). In the WRITE mode the CG is grounded and the drain (D) is connected via the access transistor to a high voltage. Electrons tunnel from the floating gate to the drain, shifting the threshold voltage of the memory transistor in the negative direction. In the READ mode this transistor will be "on."

In the ERASE mode the control gate is at high voltage while the drain is grounded. Now electrons tunnel to the floating gate and the threshold voltage of the memory transistor becomes positive; so in the READ mode this transistor will be "off."

Until now all cell concepts require a program voltage of about 20 V. This high WRITE/ERASE voltage is incompatible with a modern VLSI process. In our new cell concept the program voltage is reduced to 13 V by decreasing the injector oxide thickness to 80 Å and by increasing the capacitive coupling between control and floating gate at the expense of somewhat larger cell area. This makes the EEPROM cell more suitable for integration in a baseline-technology created for single 5-V operation. Instead of a capacitor between two polysilicon layers, in the EEPROM memory cell discussed in this paper (Fig. 1(b)) a tunnel-oxide MOS capacitor is used for the capacitive coupling between floating gate and control gate. This coupling capacitor has a large capacitance per unit area. Fig. 2 shows a top view and cross section of this single-poly EEPROM cell. In this figure the CG is a n^+-diffusion that is shared by two adjacent memory cells (only one cell is shown) and that is accessed via a pass transistor. The coupling capacitor between floating gate and control gate is made much larger than that between floating gate and drain (D). As a consequence only a small fraction of the program voltage applied between control gate and drain will be over this coupling capacitor. So the tunneling through this capacitor can be neglected and hence the operation of this single-poly cell (Fig. 1(b)) does not differ from that of the double-poly cell (Fig. 1(a)). To incorporate this new cell in a VLSI process only one extra mask for the definition of the thin oxide regions and a few extra processing steps have to be added.

Since the single-poly cell uses the same oxide in the injector as in the coupling capacitor, the total thin oxide

received March 28, 1984; revised September 27, 1984.
are with Philips Research Laboratories, 5600 JA Eindhoven, Netherlands.

0018-9200/85/0400-0603$01.00 ©1985 IEEE

Sandisk Technologies, Inc. - Ex. 1002, Page 000498

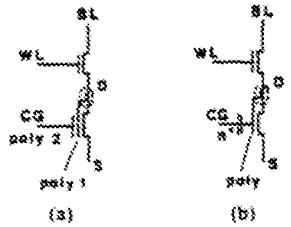


Fig. 1. Schematic representation of (a) a double-poly EEPROM cell (b) a single-poly EEPROM cell with a thin oxide capacitor as the coupling capacitor. ◇ injector.

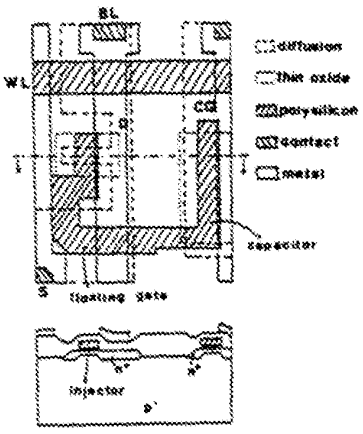


Fig. 2. Top view and cross section of the single-poly memory cell: cell area 440 μm^2.

area per memory cell is relatively large. This will influence some of the characteristics of this memory cell as will be shown in the following comparison, where the characteristics of the single-poly EEPROM cell are compared with those of a double-poly EEPROM cell designed in a similar technology. Both cells have equal injectors and can be programmed with the same voltage (13 V).

A. Memory Cell Area

Since growing of thin oxides of high quality on polysilicon is much more difficult than on silicon, the interpoly oxide-thickness for the double-poly cell has to be chosen to exceed 500 Å. This six-times-thicker dielectric for the coupling capacitor together with the large coupling factor needed to allow the EEPROM cell to be programmed at 13 V consumes the area advantage that the double-poly cell might have over the single-poly cell. So in this low-voltage process the area for both cell types is about the same. However the total amount of thin oxide area in the single-poly cell is larger than in the double-poly cell (about six times).

B. Endurance

Due to the strong coupling between floating gate and control gate, the voltage drop across the thin oxide in the coupling capacitor of the single-poly cell always remains small. So there is no high-field stress of, or tunneling through this oxide. Therefore the endurance is only determined by the injector area which is the same for both devices; so the endurance of the single-poly cell equals the endurance of the double-poly device [5].

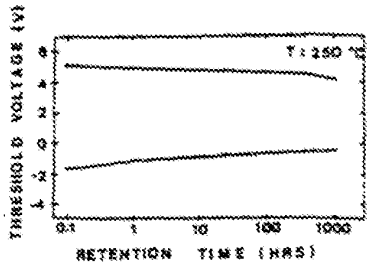


Fig. 3. Threshold voltages of the single-poly cell in written state as a function of data retention time at 250°C.

C. Data Retention

Since the data retention time is proportional to the oxide area, the retention time of the single-poly cell is about six-times smaller than that of the double-poly cell. Since floating gate EEPROM's demonstrate very good retention characteristics even for the single-poly cell, a specification of 10 years can be achieved. Fig. 3 shows the threshold voltages of the single-poly cell in the written and erased states versus the storage time at 250°C.

D. Yield Consideration

Adding a single-poly EEPROM instead of a double-poly EEPROM to an integrated system, e.g., a microprocessor, can result in a yield improvement, since two additional double-poly processing steps are not required. However, for large EEPROM's the single-poly cell can have a yield disadvantage due to the six times larger thin-oxide area. The turnover point for selecting a single-poly memory cell or a double-poly cell depends on the thin-oxide defect density for which the latter effect becomes dominant.

III. Circuit Techniques

5-V-only operation requires generation of the programming voltage on-chip, which means that only low programming currents can be supplied. Therefore, all circuits that are exposed to high voltage have to be designed to sink no dc current. Also switching of signals at high voltage has to be avoided. Since a floating gate EEPROM cell consumes only a small tunnel current during programming the charge pump has to supply only a current to compensate for diode leakage and to ramp up the program voltage supply line.

A consequence of using a programming supply with small current drive capability is that small parasitic leakage paths will clamp the program voltage to a level significantly lower than the maximum possible pump level. Since a standard VLSI process is optimized for circuits working from a single nominal 5-V supply, some of these parasitic leakage paths will already occur at voltages below the 13 V required for programming. To insure minimal modification

Sandisk Technologies, Inc. - Ex. 1002, Page 000499

technology these leakage paths have to be sup- by special circuit design techniques. For our pro- program voltage limiting effects are: punchthrough, ck in short-channel MOST's, and the turn-on of sitic field MOS transistor. The circuit techniques re used to suppress leakage paths due to these are discussed separately below, together with a on of other circuits used in the memory.

chthrough

diffusion to diffusion punchthrough is a strong of the spacing in between, this effect can easily be ed by increasing the minimal spacings. In this he minimum effective channel length of MOS rs in parts of the circuit that operate at high is increased by 0.5 μm (from about 2 to 2.5 μm). , the minimum spacing between diffusions is in- by 1 μm. In other parts of the circuit the minimum ules are retained.

-Back

nap-back effect or avalanche-induced breakdown n-channel MOSFET's, not only reduces the n-voltage of these transistors, but it also gener- rate currents [3] that may cause latchup in CMOS The voltage at which this effect occurs can be to a value above 16 V by increasing the channel the NMOS transistors to about 20 μm. However, re transistors that operate at high voltage (in the ming mode) in the critical path of the circuit, this strongly degrades the speed of the memory.

r technique is based on the understanding that occurs only in transistors that conduct a current. ct can therefore be eliminated by biasing the ansistors during programming in a way that no low in the device at high voltages, i.e., in general re switched when a high voltage is applied. To , all decoding is done at low voltages when the es at the interface between the low-voltage and oltage parts of the circuit are connected to the y (V_{cc}). Fig. 4 shows a block diagram of this Only two memory cells connected to different bit and B_1) have been drawn and R, E, W are, y, the READ, ERASE, and WRITE signals. The led "driver," "detector" represent the interface d the read amplifier/clamp voltage generator, y. The drivers have been designed to sink no dc n when they are driven by normal CMOS levels) and when the supply (V_{cc}/V_p) is charged to a ge. The supply V_{cc}/V_p to these drivers is con- the external supply (V_{cc}) in the READ mode and rge pump in the programming mode (ERASE or

hows the switch which makes these connections. ure V_{cc}/V_p is the supply to the drivers which in mode is connected via PMOST P_1 to the external

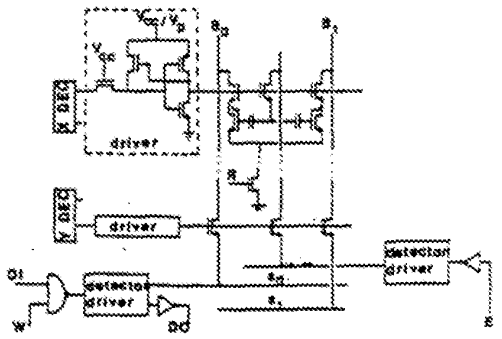


Fig. 4. Schematic block diagram of the high-voltage part of the EEPROM memory.

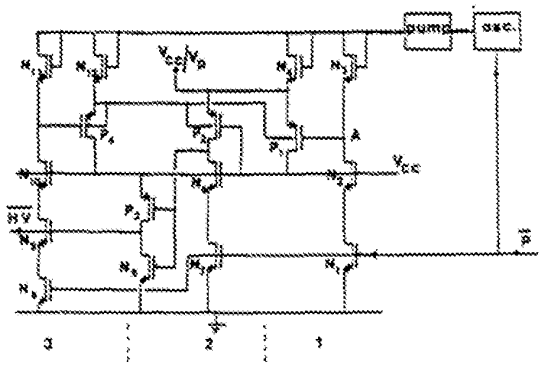


Fig. 5. The high-voltage switch.

supply (V_{cc}) ($\overline{P}$ is at V_{cc}). In this mode the charge pump is off. In the programming mode ($\overline{P}$ is at 0 V), the transistor P_1 is off and the V_{cc}/V_p supply is charged by the pump via NMOST $N4$ to the program voltage. The high voltage at node A is divided over the cascoded NMOS transistors N_2 and N_3. Also the channel length of these transistors has been increased to 10 μm. This has been done to avoid snap-back at the end of the programming cycle when $\overline{P}$ switches to V_{cc} and node A starts to be discharged. The same holds for transistors N_6, N_7, and N_8, N_9, N_{10}.

Part 2 of the circuit in Fig. 5 is a detector which supplies a signal $\overline{HV}$ equal to 0 V if V_{cc}/V_p is at voltages higher than $V_{cc} + |V_{TP}|$, where V_{TP} is the threshold voltage of PMOST P_2. The $\overline{HV}$ signal is used to latch all the data (addresses and input data) in order to prevent switching of signals at high voltage levels. This technique prevents snap-back in the drivers and enables the use of MOST's with small channel lengths in the high-voltage part of the circuit.

Part 3 of this circuit (Fig. 5) is a similar switch to that of part 1 which connects the well of the PMOST transistors P_1 and P_2 either to V_{cc} or to the charge pump. This has been done to prevent latchup, since transient currents in the drivers during reading (V_{cc}/V_p is connected via P_1 to V_{cc}) cause a dip in the V_{cc}/V_p voltage. If the well of the transistors P_1 and P_2 has been connected to the V_{cc}/V_p, this dip can initiate latchup.

C. Parasitic Field MOS Transistors

The occurrence of a leakage paths due to the turn-on of parasitic field MOS transistors can be suppressed at the

Sandisk Technologies, Inc. - Ex. 1002, Page 000500

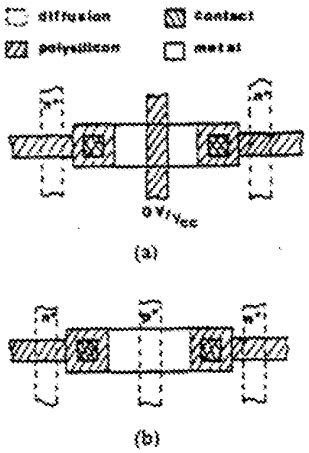


Fig. 6. Elimination of the leakage path due to the turn-on of the parasitic field MOST (NMOST) (a) with a poly plane and (b) with the source/drain diffusion as channel stopper.

expense of an increase in chip area. Two possibilities are shown in Fig. 6, one uses a poly plane connected to a low voltage (V_{cc} or 0 V), while the other uses the source/drain diffusion of the PMOS transistors as channel stopper. These techniques consume a lot of area and are therefore only suitable in the periphery.

In the memory matrix the turn-on of the parasitic NMOST between diffusions is prevented by a circuit design technique: a small voltage is applied to the source of these parasitic transistors during the programming cycle. This voltage effectively acts as an artificial substrate-bias for the parasitic MOST, which due to the high substrate doping and due to the thick gate oxide strongly increases its threshold voltage. The voltage is generated by the same circuit which clamps during the read cycle the drain of the floating gate transistor at a low voltage (needed to avoid read disturb). Fig. 7 shows the read amplifier (detector) that also generates the clamp voltage together with the driver stage of the data input path.

The detector circuit is a current–voltage converter which at the same time clamps the sense line s and also the selected bit line and the drain of the selected memory transistor at about 1 V. This circuit is based on the NMOS read amplifier described in [4]. Some modifications were made to cut off dc currents in the standby mode (transistors N_4, P_6) and a clamp function for voltages larger than the input reference voltage was added (transistors P_5, N_5).

This amplifier has been designed to keep the clamp voltage nearly constant for a wide range of memory cell currents. In the READ mode (R, $\overline{DI}$, V_{cc}/V_p are at V_{cc} level, $\overline{CE}$ is at 0 V) if the selected memory cell is off, the sense line "s" and also the bit line and the drain of the E^{2}PROM are charged via transistors P_6, N_3, and N_2 until the voltage at node B has decreased such that N_2 goes off. The voltage at line "s" is determined by the dimensions of transistors P_1 and N_1 and equals the voltage at node B minus the threshold voltage of N_2. The voltage at node $\overline{DO}$ equals V_{cc}. If the selected memory transistor is on, the small drop

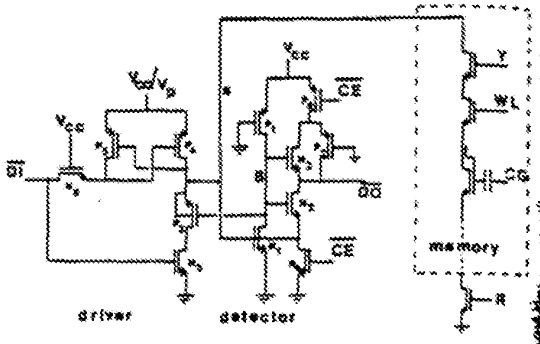


Fig. 7. Data input high-voltage driver and current detector that generates the clamp voltage.

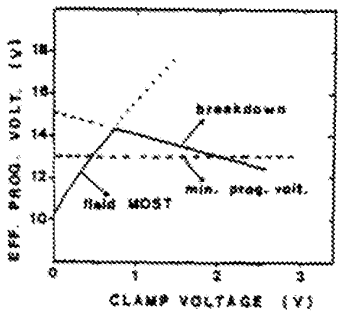


Fig. 8. Effective program voltage for worst case processing, worst case operation conditions as a function of the clamp volt

at "s" (a few millivolts) is inverted and amplified by inverter N_1, P_1. Transistor N_2 turns on and the cell current will cause a voltage drop across P_2. The voltage at node B decreases. For larger cell currents transistor P_2 no longer source sufficient current to maintain the B voltage. A further slight drop in the voltage at line "s" will increase the voltage at node B to a higher level turning on transistor N_3 which allows for additional current from the memory cell. The voltage at $\overline{DO}$ is now somewhat below the clamp voltage level. This sense amplifier is followed by a strongly asymmetric inverter that restores the full logic levels. During programming (R equals 0 V) the voltage on the line "s" depends on the voltage at node $\overline{DI}$. If $\overline{DI}$ is at V_{cc} level the PMOST P_3 prevents discharging this line below 1 V and hence clamps it at the voltage set by the clamp circuit. If $\overline{DI}$ equals 0 V the driver allows the line "s" to be discharged by the charge pump to the program voltage.

The blocks labeled "detector/driver" in Fig. 4 represent the circuit of Fig. 7. The clamping procedure previously discussed guarantees that during programming there are no diffusions in the memory matrix at 0 V. They are either at program voltage or at the clamp voltage level. The diffusions in nonselected cells are floating. Due to this technique the parasitic field MOST in the memory matrix has a back bias that equals the clamp voltage which will significantly increase its threshold voltage.

In Fig. 8 the effective program voltage (the voltage difference between the drain and the control gate of the memory transistor) is plotted as a function of the applied clamp voltage. These curves have been calculated by

Sandisk Technologies, Inc. - Ex. 1002, Page 000501

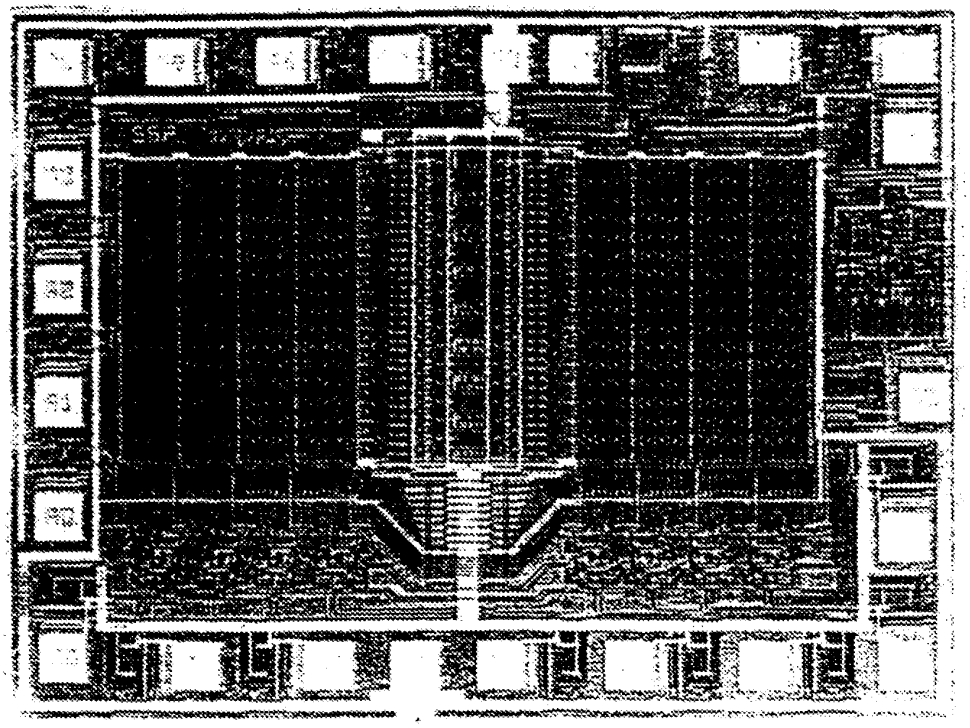
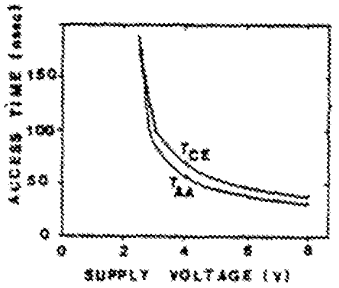


Fig. 9. Microphotograph of the 2K EEPROM; chip area: 2.66 × 1.98 mm², module area 3.2 mm².



$\overline{CE}$ and address access time as a function of the supply voltage.

e process parameters and worst case operation ns. For small clamp voltages the programming s limited by the turn-on of the parasitic field n the memory. For higher clamp voltages the sted breakdown of the NMOS transistors in the ill clamp the charge pump. This figure indicates memory cell can be programmed if the clamp chosen between 0.5 and 2 V.

IV. 2K EEPROM Library Module

e techniques have been applied to realize a 2K M memory module in a 2.5-μm n-well CMOS gy. Fig. 9 shows a microphotograph of this module ed by buffer circuits. The memory has been as a 256 by 8-bit memory. The die measures 5.3 h a cell area of 440 μm^2 and the module itself only 3.2 mm^2 of area.

The device operates from a single supply which may range from 3 to 7 V in the READ mode. Fig. 10 shows the $\overline{CE}$ and the address access time as a function of the supply voltage. In the active mode the 2K module dissipates 10 mW (V_{cc} = 5 V, cycled at 10 MHz). This power consumption is reduced in the standby mode to a value less than 5 μW. For programming a supply voltage larger than 4 V is needed. Typical programming time is about 1 ms.

V. Conclusion

The realization of a 2K EEPROM library module in a 2.5-μm n-well CMOS VLSI process has been described. Only few extra processing steps (one extra mask) have to be added to the baseline process to fabricate this device. These steps have no effect on the transistor characteristics, and do not affect the minimum design dimensions of the process. So to add the EEPROM memory module to an existing design, no redesign for changed processing is needed and the speed of the existing circuit blocks is retained. Design techniques that are needed to allow programming of the EEPROM memory with voltages up to junction breakdown have been discussed.

Acknowledgment

The authors wish to thank W. C. H. Gubbels for developing test programs for the EEPROM memory.

Sandisk Technologies, Inc. - Ex. 1002, Page 000502

REFERENCES

[1] J. R. Lineback, "EE-PROM adds on-chip flexibility," *Electron.*, vol. 56, no. 23, pp. 99–100, Nov. 17, 1983.

[2] D. H. Oto, V. K. Dham, K. H. Gudger, M. J. Rietsma, G. S. Gongwer, Y. W. Hu, J. F. Olund, H. S. Jones, and S. T. K. Nieh, "High-voltage regulation and process considerations for high-density 5 V—Only E²PROM's," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 532–538, Oct. 1983.

[3] W. Müller, L. Risch, and A. Schütz, "Short-channel MOS transistors in the avalanche-multiplication regime," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1778–1784, Nov. 1982.

[4] B. Giebel, "An 8K EEPROM using the SIMOS storage cell," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 311–315, June 1980.

[5] R. Cuppens, C. D. Hartgring, J. F. Verwey, and H. L. Peek, "An EEPROM for microprocessors and custom logic," in *ISSCC Dig. Tech. Papers*, Feb. 1984, pp. 268–269.



Roger Cuppens was born in Zonhoven, Belgium, on March 10, 1948. He received the electrical engineering degree and the Ph.D. degree in applied science from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1972 and 1980, respectively.

In 1972 he was employed as a Research Assistant at the E.S.A.T. Laboratory of the Katholieke Universiteit Leuven. In 1979 he joined Philips Research Laboratories, Eindhoven, The Netherlands, where he is involved in the development and design of nonvolatile memories.



Cornelis D. Hartgring (S'80–M'81) was born in Haarlem, The Netherlands, on November 18, 1953. He received the degree of Ingenieur in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1977, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1978 and 1981, respectively. His thesis research in The Netherlands dealt with junction charge-coupled devices and that in the U.S. with silicon MESFET's.

In 1979–1980, he spent a year at Tektronix, Inc., OR, to conduct a joint investigation related to his Ph.D. topic. In 1981 he joined Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on the development and design of programmable nonvolatile memories. He is currently involved in the design of high-density static R.A.M's.



Jan F. Verwey was born in Benschop, The Netherlands. He received the Ph.D. degree in 1967 in solid state chemistry at the University of Utrecht. The title of his thesis was "Photochemical processes in lead halides."

In 1967 he joined the Philips Research Laboratories in Eindhoven, The Netherlands, where he has been subsequently involved in research on the hot carrier injection into SiO_2, reliability problems related to oxide quality, high-voltage integrated circuits, and nonvolatile memory devices. He became Extraordinary Professor in applied physics at the University of Groningen in 1976. He is heading a small research gr working on the subject "Insulating layers on semiconductors."

Dr. Verwey, from 1974 until 1982 was a Member of the Progr Committee of the Symposium on Solid State Device Technology. T international conference is held annually together with the Europ Solid State Device Research Conference (ESSDERC). He has organi the International Conference "Insulating Films on Semiconduct (INFOS 83) which was held in Eindhoven on April 11–13, 1983. S 1982 he is an Editor of the journal "Microelectronics and Reliability," is also involved in the National research organizations of the Netherla For instance, he is chairman of the semiconductor branch of Founda Fundamental Research on Matter (FOM) and a Member of the com tee for Solid State Physics of the same foundation.



Herman L. Peek was born in Haalderen, Netherlands, on June 25, 1942. He received Ingenieur Diploma in physics from Eindh Technological College, Eindhoven, The Ne lands, in 1969.

He joined the Semiconductor Research G of Philips Research Laboratories, Eindhov 1964, where he worked on MOS technology con epitaxy, and silicon vidicon devices. 1973 he has been working in the CCD re group, where he has been involved in the opment of solid-state image sensor technology. From 1979 to 1983 h worked on the development of EEPROM technology.



Frans H. A. Vollebregt was born in Na The Netherlands, on August 7, 1957. He r the M.S. degree in solid state chemistry University of Leiden, in 1982.

In 1983 he joined the Philips Research L tories in Eindhoven and from that time h interest has been in the field of no memories.



Elisabeth G. M. Devens was born in N Netherlands, on June 28, 1957. She re Ing. degree from H.T.S. Heerlen, the lands, in 1979.

In 1979 she joined Philips Research L ries, Eindhoven, the Netherlands, whe working on EEPROM's.



Ingrid A. Sens was born in Schie Netherlands, on February 28, 1953. S the Ing. degree from H.T.S. Heerlen, T lands in 1977.

In the same year she joined the search Laboratories in Eindhoven, T lands.

Sandisk Technologies, Inc. - Ex. 1002, Page 000503

An EPROM Cell Structure for EPLD's Compatible with Single Poly-Si Gate Process

KUNIYOSHI YOSHIKAWA, MEMBER, IEEE, SEIICHI MORI, AND NORIHISA ARAI

Abstract—A single poly-Si gate EPROM cell structure, which can eliminate the process complexity involved in conventional double poly-Si EPROM technologies, is proposed to realize EPLD's with a faster turnaround time. Since the proposed cell uses an n^+ diffused layer on a bulk Si substrate as a control gate instead of a second poly-Si, markedly improved reliability is obtained, especially for bias stress data retention. This is due to the higher quality of bulk Si oxide, compared with an interpoly insulator of double poly EPROM's. Basic cell characteristics (write, erase, *I–V*, high temperature data retention, etc.) are almost the same as those for a double poly cell. It was found that the single poly cell is easily combined with logic's single poly and double metal process, therefore it should greatly contribute to developing CMOS EPLD's in spite of the cell area increase.

I. Introduction

With the rapid development in application specific integrated circuits (ASIC's), CMOS erasable programmable logic devices (EPLD's) are now receiving much attention. CMOS EPLD's can realize user programmable and reconfigurable logic devices with a faster production turnaround time. Moreover, new devices with more sophisticated AND, OR, NAND or NOR array configurations can be easily developed by EPLD's. Therefore, it should be necessary to combine current double poly CMOS EPROM technologies [1]–[3] with advanced architecture and circuit techniques. Since most popular logic devices use a single poly-Si gate and double metal technologies, the introduction of conventional double poly-Si EPROM technology to a logic process naturally leads to fabrication process complexity and degrades production yields, resulting in die cost increase. Moreover, novel process technologies should be used to form a reliable interpoly-Si insulator, such as high temperature oxidation [4] and stacked CVD film technology [5], as well as double poly cell formation with plasma etching. Recently, several attempts have been made to introduce a single poly technology into EPROM memories [6]–[8].

This paper describes newly developed single poly-Si gate EPROM cell technology in detail. The structure uses an n^+ diffused layer on a Si substrate as a control gate (CG) to meet the previously mentioned requirements. As the n^+ layer is additionally formed for CG and used instead of an n-well layer [6], relatively smaller cell sizes are realized. Obtained cell performance and reliability have been found sufficient for fabricating EPLD's. Thus, the possibility of applications to logic and microprocessors are also increased.

Manuscript received February 27, 1989. Revised August 13, 1989. The review of this paper was arranged by Associate Editor P. K. Ko.

K. Yoshikawa and S. Mori are with the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki, 210 Japan.

N. Arai is with Toshiba Microelectronics Corporation, Kawasaki, 210 Japan.

IEEE Log Number 8932811.

II. Cell Structure and Fabrication Process

A typical cross section of proposed single poly-Si gate cell structure is shown in Fig. 1(a), compared with a conventional double poly cell (Fig. 1(b)). In the single poly cell, the n^+ diffused layer in the bulk Si substrate is used for a control gate (CG), instead of a second poly layer, which is capacitively coupled to an extended poly-Si floating gate (FG). A top view photograph is shown in Fig. 2. Both the cell transistor channel region and the CG n^+ layer are fabricated on the Si substrate and are electrically isolated from each other by an isolation field oxide. Fig. 3 shows one example of the cell layout in the memory array. Control gate and source regions are shared by two adjacent cells. The unit cell area is about two and a half times larger than for conventional cells. For example, about 50-μm^2 cell size with 1.2-μm design rule has been realized, compared with the 19.8-μm^2 double poly cell. It should be noted that this cell size can be applicable not only for the logic and microprocessor field, but also for medium scale memory devices and logic devices with medium density memories. In the new cell, since the CG is embedded in the Si substance, the CG's total capacitance increases to around five times that of a conventional double poly cell. Considering that n^+ CG sheet resistance ($\sim 40\ \Omega$) is comparable to that for a poly CG, RC delay will increase. Since n^+ word line resistance can be reduced by a second Al snapping technique, a word line delay increase can be prevented. If the second Al can not be available, an n^+ CG should be divided appropriately.

Table I shows device process parameters for fabricated cells. The process sequence is shown in Fig. 4, which is based on a 1.2-μm NMOS technology with 200-Å gate oxide. After the field isolation oxide formation, a photo mask step was carried out to define CG n^+ layers. Then, the first gate oxide and control gate oxide were simultaneously formed. The first gate oxide was 200-Å thick. Oxide thickness on the n^+ control gate layer usually becomes more than 200 Å, due to the oxidation rate enhancement for highly doped n^+ layers. After that, the

0018-9383/90/0300-0675$01.00 © 1990 IEEE

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 05,2010 at 18:07:17 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000504

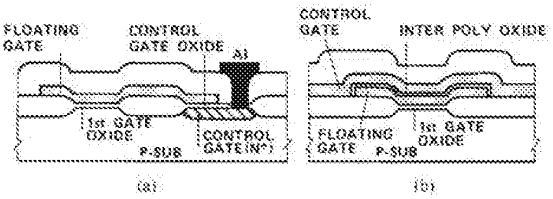


Fig. 1. Cross-sectional views of (a) single poly gate EPROM cells, and (b) conventional double poly gate cells.

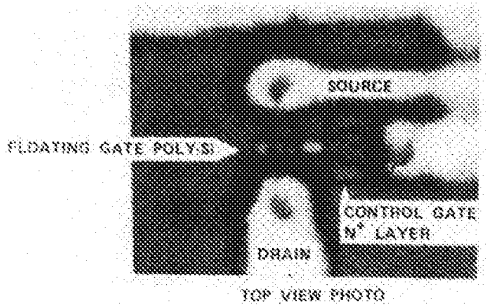


Fig. 2. Top view photograph of the single poly cell test structure.

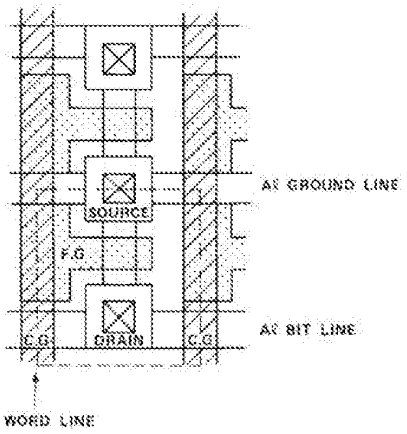


Fig. 3. Typical memory cell layout.

poly-Si layer was deposited, followed by phosphorus doping. Finally, the poly-Si gates were defined.

Essentially, for the new EPROM cell, only one extra photomask step to define the CG n^+ layer and the n^+ ion implant process, has to be added to conventional logic process. However, if logic parts require LDD or DDD NMOS, one more extra mask step with additional n^+ implants will be necessary [8].

One of the key fabrication technologies for the cell is the gate oxide formation. For an EPROM cell, capacitance coupling between FG and CG strongly affects the electrical characteristics. Gate oxide thickness, between FG and CG, namely CG oxide thickness, determines coupling ratio. The oxide thickness ratio between CG oxide and cell gate oxide greatly affects the coupling ratio. This

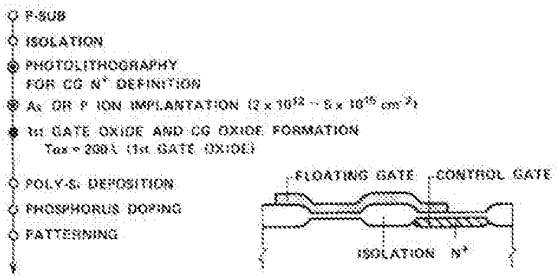


Fig. 4. Process sequence for the single poly cell.

TABLE I
DEVICE PROCESS PARAMETERS FOR SINGLE POLY CELLS

Leff	0.7 μm
W	1.2 μm
GATE OXIDE	200 Å
CG OXIDE	200 ~ 600 Å
CG N+	As 1/1 $2\times10^{12}cm^{-2}$, 100 keV
STRUCTURE	As 1/1 $5\times10^{15}cm^{-2}$, 35 keV
	P 1/1 $5\times10^{15}cm^{-2}$, 35 keV

oxide thickness ratio depends upon oxidation temperature, because CG oxide is formed on an n^+ diffused layer. Fig. 5 shows the relationship between the first gate oxide thickness and CG oxide thickness as a function of oxidation temperature. The first gate oxide thickness was controlled to 200 Å. Higher oxidation temperature can realize a relatively thinner control gate oxide. Thus, using the diluted high-temperature oxidation method, a thin gate oxide can be formed on the channel and the CG n^+ region, simultaneously. An increase in capacitance coupling, due to thin oxide formation, leads to fast READ/WRITE speed or reduction in the unit cell size. Note that since the breakdown field strength for CG oxide on n^+ is generally lower than that for cell gate oxide, i.e., around 70 percent of oxide on lightly doped substrate even with diluted oxidation method, thicker CG oxide will be preferable for production.

To investigate the effect of deep depletion layer formation in CG on WRITE characteristics, various CG n^+ diffused structures were examined. The CG n^+ layers, formed by P ion implantation and As ion implantation with higher and lower dosages, were examined.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Electrical Cell Characteristics

Basic WRITE characteristics for the new cell with W/L_{eff} = 1.2 μm/0.7 μm are shown in Fig. 6. The new cell shows better WRITE speed than the conventional cell, but this comes from a smaller CG to FG capacitance coupling capacitance ratio and a shorter effective channel length. Since the cell WRITE properties fundamentally are governed by the coupling capacitance ratio and gate length, the new cell and conventional cell will show almost the

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 05,2010 at 18:07:17 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000505

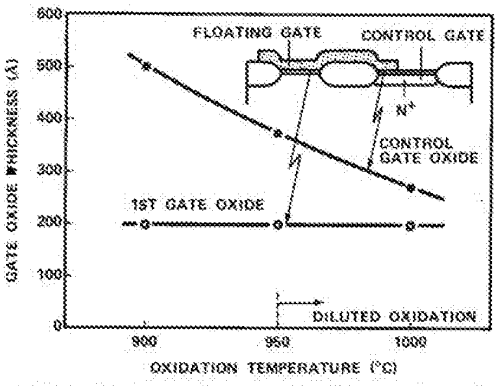


Fig. 5. Relationship between first gate oxide thickness and control gate oxide thickness as a function of oxidation temperature. N^+ CG region is formed by As ion implants, with 5×10^{15} cm^{-2} dose. Oxidation conditions are 900°C, dry O_2, 950°C, 20-percent N_2 diluted—and 1000°C, 20-percent N_2 diluted oxygen oxidation, respectively.

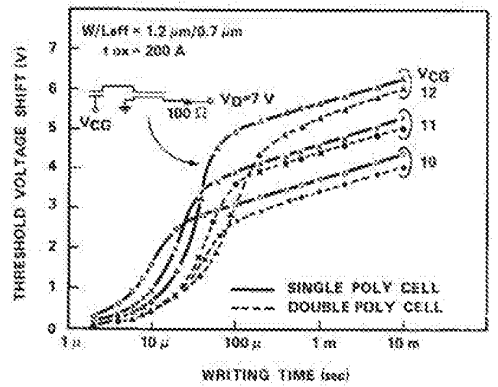


Fig. 6. Write characteristics for single poly cells as a function of control gate voltage, compared with those for double poly cells. Cell parameters are as follows: 1) for single poly cell, t_{ox} = 200 Å, CG_{ox} = 500 Å, CG–FG coupling area = 5.52 μm^2, L_{eff} = 0.7 μm, and 2) for double poly cell, t_{ox} = 300 Å, interpoly = 280 Å, CG–FG coupling area = 4.32 μm^2, L_{eff} = 0.72 μm.

same characteristics, if these parameters are the same. It is clear that around a 5-V threshold voltage shift can be obtained after writing within 100-μs of writing time. This value is substantial for practical application.

In the new cell, since the CG is formed by an n^+ diffused layer and isolated from the channel region by the field oxide, maximum write voltage exists. This is determined by the lowest voltage for the CG n^+ junction breakdown voltage, the turn-on voltage for the parasitic poly-gate field transistor, and the punchthrough voltage between the CG and the channel region for the cell. Fig. 7 shows the limiting CG voltage as a function of isolation oxide width. Above 1.2-μm isolation width, the punchthrough voltage and the threshold voltage for the field transistor are higher than 14 V, which is the junction breakdown voltage. Therefore, a standard 1.2-μm EPROM WRITE voltage, 12.5 V, can be used with sufficient margin.

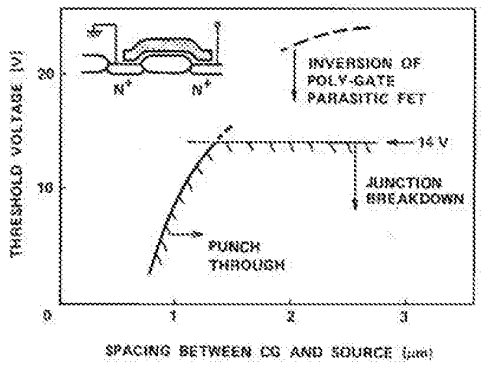


Fig. 7. Limiting control gate voltages as a function of field isolation width.

In order to evaluate the CG n^+ doping concentration effect on the WRITE characteristics, three junction structures were examined. Phosphorus ion implant ($5 \times 10^{15}$$cm^{-2}$), arsenic ion implants at higher (5×10^{15} cm^{-2}) and lower (2×10^{12} cm^{-2}) dosages were compared. As the doping concentration in n^+ layer decreases, the depletion layer in the CG becomes easily formed, leading to effective writing voltage decrease. To estimate this effect, threshold voltage shifts after writing, as shown in Fig. 8, were examined. Around 1 V degradation for 2×10^{12} cm^{-2} As dosage is observed. As this value is not so large, it becomes possible to utilize this CG formation dose by optimizing WRITE CG voltage and writing time. Since EPROM's sometimes use depletion (D) type NMOS (As dose is around 2×10^{12} cm^{-2}) in the circuits, the D-type NMOS channel implants can replace CG n^+ doping ion implants, if D-type NMOS is implemented in EPLD's. In this case, the extra n^+ defined mask and n^+ ion implant process can be completely reduced.

Fig. 9 shows typical *I–V* characteristics for the cell. Cell READ current I_d of 140 μA at V_d = 1.5 V with a 5.5-μm^2 gate coupling area is obtained. This is about 1.5 times larger than that for the conventional cell. Essentially, since the channel width and the FG potential determines the cell READ current, it is possible to gain more READ current by increasing the channel width, along with increasing the CG area, to meet the requirement for higher speed operation.

Ultraviolet (UV) light ERASE characteristics are shown in Fig. 10. Erasing speed is almost 2.8 times faster than that for the double poly cell. This enchancement is well explained by the model [9], in which the UV irradiated FG perimeter length, facing the n^+ layer, dominates the erasing speed [6], [9]. To maintain this desirable fast erasing feature, precautions on actual cell layout are necessary to maximize the FG perimeter length as much as possible.

B. Reliability

One of the most important items regarding EPROM reliability is the bias stress data deprogramming immunity [1], [5] and high-temperature data retention.

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 05,2010 at 18:07:17 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000506

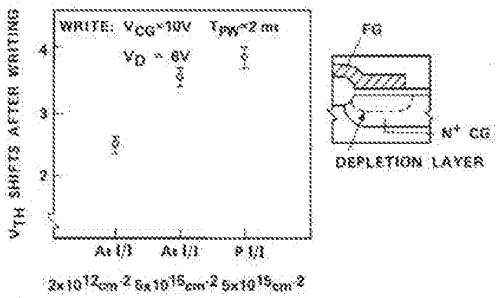


Fig. 8. Control gate doping concentration effect on the threshold shift after writing.

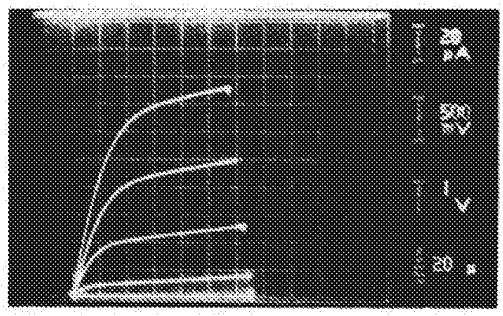


Fig. 9. Typical I-V curve for single poly EPROM cells with 3.5-μm^2 gate coupling area. L_{ov} = 0.7 μm, and W = 1.2 μm. $V_{G\,MAX}$ = 5 V.

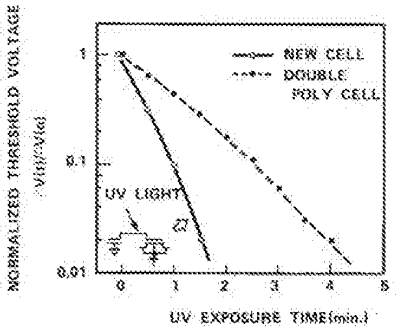


Fig. 10. Erase characteristics for single poly cells, compared with those for double poly cells.

Data deprogramming characteristics for the new cell, by applying a positive voltage on CG, are shown in Fig. 11. More than 5-MV/cm electric field strength for the single poly cell was obtained, which is about 2 MV/cm higher than that for a conventional double poly cell with poly oxides as an interpoly insulator. Below the CG n^+ layer junction breakdown voltage, current leakage from FG is completely suppressed. This feature results from the use of the bulk Si oxide instead of a poly oxide for a double poly cell. The poly-oxide leakage electric field strength is generally lower than that for bulk Si oxide, due to the grown poly-Si surface asperity [10] and the degradation in oxide quality related defect density increase [11].

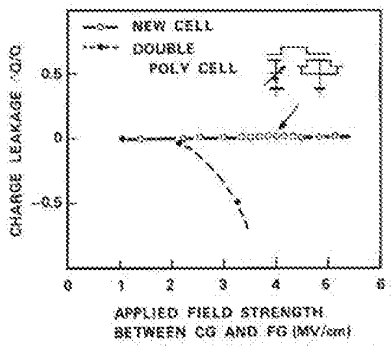


Fig. 11. Data deprogramming characteristics as a function of applied positive bias electric field on control gate.

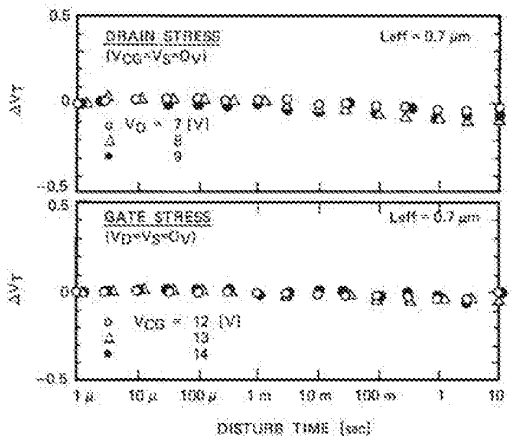


Fig. 12. Write-disturb characteristics for drain and gate stress conditions as a function of stress time.

Moreover, the single poly-Si gate structure itself improves the leakage resistance. Generally, the electric field enhancement at the FG poly-Si edge, which is conformally surrounded by the CG poly-Si, dramatically reduces the electric field strength for a double poly cell. On the other hand, since the single poly cell structure has no edge effect, no electric field enhancement problems occur. As a result, without a special interpoly insulator (high quality poly oxide [4], stacked CVD layer, such as ONO structure [5], etc.) technology, a reliable cell can be obtained. Fig. 12 shows WRITE-DISTURB characteristics as a function of stress time. Both for gate and drain stress conditions, no significant degradation is observed.

Fig. 13 shows the worst cell data retention characteristics for the single poly-gate structure as a function of temperature. High temperature retention is found to be essentially the same as for conventional double-poly gate EPROM cells, because the quality of the poly oxide covering the FG determines the thermionic electron emission from the floating gate [12]. Since about 0.8-eV activation energy was obtained for the worst case samples, more than 10 years' data retention at 150°C has been ensured.

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 05,2010 at 16:07:17 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000507

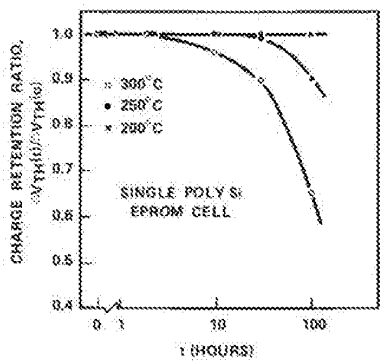


Fig. 13. High temperature bake retention characteristics.

IV. Summary and Conclusion

A single poly-Si gate EPROM cell technology has been described and discussed. In spite of a slight increase in unit cell area with a single poly-Si gate cell, the proposed cell shows marked reliability and realizes substantial cell electrical performance. Thus, by adding a few extra process steps, the introduction of this cell to the logic and microprocessor field will greatly contribute to the development of ASIC's.

Acknowledgment

The authors would like to thank J. Matsunaga and Dr. O. Ozawa for their support and encouragement.

References

[1] K. Yoshikawa *et al.*, "Technology requirements for megabit EPROM's," in *IEDM Tech. Dig.*, 1984, p. 456.
[2] J. Lien *et al.*, "A high performance CMOS process for the next generation EPROM," in *IEDM Tech. Dig.*, 1984, p. 460.
[3] S. Mori *et al.*, "Novel process and device technologies for submicron 4-Mbit EPROM's," in *IEDM Tech. Dig.*, 1987, p. 556.
[4] Y. Mikata, S. Mori, K. Shimada, and T. Usami, "Low leakage current polysilicon oxide grown by two-step oxidation," in *Proc. IRPS*, 1985, p. 32.
[5] S. Mori, M. Sato, Y. Mikata, T. Yanase, and K. Yoshikawa, "Polyoxide/nitride/oxide structures for highly reliable EPROM cells," in *Proc. VLSI Symp.*, 1984, p. 40.
[6] R. Kazerounian and B. Eitan, "A single poly EPROM for custom CMOS logic applications," in *CICC Tech. Dig.*, 1986, p. 59.
[7] K. Yoshikawa, S. Mori, and N. Arai, "An EPROM cell structure for EPLD's compatible with single poly gate process," in *Ext. Abst. SSDM*, 1986, p. 323.
[8] P. J. Cacharelis, M. J. Han, M. H. Manley, S. O. Franke, and M. W. Knecht, "A modular 1-μm CMOS single polysilicon EPROM PLD technology," in *IEDM Tech. Dig.*, 1988, p. 60.
[9] R. D. Katznelson and D. Frohman-Bentchkowsky, "An erase model for FAMOS EPROM devices," *IEEE Trans. Electron Devices*, vol. ED-27, no. 9, p. 1744, 1980.
[10] D. J. Dimaria and D. R. Kerr, "Interface effects and high conductivity in oxide grown from polycrystalline silicon," *Appl. Phys. Lett.*, vol. 27, no. 9, p. 505, 1975.
[11] S. Mori *et al.*, "Reliable CVD inter-poly dielectrics for advanced E & EEPROM," in *Proc. VLSI Symp.*, 1985, p. 16.
[12] H. Nozawa and S. Kohyama, "A thermionic electron emission model for charge retention in SAMOS structure," *Japan. J. Appl. Phys.*, vol. 21, p. L111, 1983.

*



Kuniyoshi Yoshikawa (M'85) was born in Tokyo, Japan, on August 24, 1950. He received the B.S. and M.S. degrees in applied physics from Waseda University, Tokyo, Japan, in 1974 and 1976, respectively.

In 1976 he joined Toshiba Semiconductor Division, Toshiba Corporation, Kawasaki, Japan, where he was engaged in the development of 8K, 16K, and 32K NMOS EPROM's. In 1982 he joined the Toshiba Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki, where he developed CMOS EPROM's technology. He has developed 256K, 1-Mbit and 4-Mbit CMOS EPROM's. He has been engaged in the research of high density and high speed CMOS EPROM's. He is interested in device design and fabrication process in submicron VLSI's, nonvolatile memory devices, thin-gate dielectrics, and Si oxidation. He is currently developing ultrahigh density EPROM's as Senior Researcher.

Mr. Yoshikawa is a member of the Japan Society of Applied Physics and of the IEEE Electron Devices Society.

*



Seiichi Mori was born in Tokyo, Japan, on January 17, 1959. He received the B.S. and M.S. degrees in electrical engineering from Keio University, Tokyo, Japan, in 1981 and 1983, respectively.

In 1983 he joined the Toshiba Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki, Japan. He has been engaged in the research and development of CMOS EPROM technology. He has developed 1-Mbit and 4-Mbit EPROM's. He is interested in thin-gate dielectric integrity, silicide and hot carrier effect in small geometry MOSFET's.

Mr. Mori is a member of the Japan Society of Applied Physics.

*



Norihisa Arai was born in Saitama, Japan, on March 19, 1962. He received the B.S. degree in electrical engineering from Tokyo Denki University, Tokyo, Japan, in 1985.

In 1985 he joined the Toshiba Microcomputer Engineering Corporation (now Toshiba Microelectronics Corporation), Kawasaki, Japan. He was engaged in the research and development of the EPROM process. He is currently engaged in MOSFET physics, designs, and analysis for CMOS EPROM's.

Mr. Arai is a member of the Japan Society of Applied Physics.

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 05,2010 at 16:07:17 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000508

An Experimental 5-V-Only 256-kbit CMOS EEPROM with a High-Performance Single-Polysilicon Cell

JUN-ICHI MIYAMOTO, JUN-ICHI TSUJIMOTO, NAOHIRO MATSUKAWA, SHIGERU MORITA, KAZUYOSI SHINADA, HIROSHI NOZAWA, AND TETSUYA IIZUKA, MEMBER, IEEE

Abstract — A 256-kbit (32K-words × 8-bit) 5-V-only electrically erasable and programmable read-only memory (EEPROM) with a high-performance cell has been developed. A unique single-polysilicon EEPROM cell, called DIFLOX (DIFfused Layer controlled floating-gate-type cell with thin Oxide), was applied to this memory. The floating-gate voltage is controlled by two thin oxide capacitors coupled with two N^+ diffused layers: the drain and the control gate. Its size is reduced to 86.25 μm^2 by exploiting 1.2-μm photolithograph and scaled transistors with 1.4-μm gate length. For programming time reduction, a PAGE-MODE programming scheme was applied. Successive data of up to 16 bytes are loaded into internal storage and are programmed simultaneously. All high voltages needed to perform the ERASE/PROGRAM (E/P) function are generated internally, and two kinds of timers were designed using an improved switched-capacitor technique. Owing to the open-bit-line scheme, cell data were detected with high sensitivity in spite of the large bit- and word-line parasitic capacitance. The EEPROM offers typically 150-ns address access time, 80-mW active and 1-μW standby power dissipation. It was successfully fabricated in a single-polysilicon and single-metal CMOS process. The chip is 7.33 × 6.23 mm^2 and is packed into the DIP 28 pin, which is pin-to-pin compatible to 256-kbit SRAM.

I. INTRODUCTION

RECENTLY, electrically erasable and programmable read-only memory (EEPROM) has been developed by the electronic industry due to its in-system reprogramming capability. So far, several kinds of devices up to 64 kbits [1]–[8] have been intensively demonstrated. They have one standardization of 5-V-only operation, which is achieved by the internal generated high voltage taking advantage of extremely low current consumption for their ERASE/PROGRAM function. On the other hand, they revealed many diversities, too. One was demonstrated to have high-reliability characteristics, such as over 10^6 endurance with on-chip ECC, or extended temperature operations. Another aimed at high-speed access time competitive with the bipolar PROM. And there is a synchronous EEPROM like microprocessors operated by some commands. However, in order to apply the nonvolatile mass storage for microcomputer peripherals, it is necessary to achieve high-density EEPROM with lower cost, in addition to ease of use and high reliability. For this purpose, a small-sized cell with a simple structure is required. Utilizing the electron tunneling through thin oxide from the bulk to the floating gate, several types of cells aiming to be used for a large bit capacity EEPROM were reported [9], [10]. One of the most popular structures is composed of two transistors, that is the select transistor and the floating-gate transistor, fabricated in a double-polysilicon process. In order to gain larger capacitance coupling between the control gate and the floating gate within the limited stacked area, it is necessary to decrease the interpolysilicon oxide thickness. However, this is accompanied by several fabrication difficulties such as the asperity growth, affected by the impurity concentration of polysilicon and the annealing condition [11]. Of course, there are some attempts for obtaining thin dielectric films by use of an oxide–nitride–oxide structure. However, one of the simplest approaches for size reduction is to use the single-polysilicon structure, since the larger capacitance coupling with the control gate can be obtained through a reliable thin oxide on bulk without sacrificing large cell area. In addition, no special technique is required. Previously, a single-polysilicon cell for 2-kbit EEPROM was reported [12]. However, it occupied 440 μm^2, rather larger than the double-polysilicon ones, because it was designed for compatibility with the logic circuits.

In the high-density EEPROM, there are several hedges to achieve the design goal besides the cell area reduction. One is the data detection technique, as a large parasitic capacitance affects the small signal generated by the scaled cell, which has a comparatively low drive capability. The second is the ERASE/PROGRAM time reduction, because it increases proportional to the bit density. Utilizing a differential amplifier constructed by a CMOS current mirror circuit or a bipolar one is a way to detect small bit-line signals [13]–[15]. However, as is used for high-speed or high-density SRAMs [16], the internally synchronous approach is one of the promising methods for single-ended bit-line cells such as EPROM's and EEPROM's. In particular, the scheme has a good compatibility with the

Manuscript received July 24, 1985; revised January 21, 1986.

J.-I. Miyamoto is with the Computer Systems Laboratory, Stanford University, Stanford, CA 94305 on leave from the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki 210, Japan.

J.-I. Tsujimoto, N. Matsukawa, S. Morita, K. Shinada, H. Nozawa, and T. Iizuka are with the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki 210, Japan.

IEEE Log Number 8609689.

0018-9200/86/1000-0852$01.00 ©1986 IEEE

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 02,2010 at 22:49:44 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000509

PAGE-MODE programming function, which is effective in reducing the ERASE/PROGRAM time.

This paper describes a 256-kbit 5-V-only EEPROM fabricated by a single-polysilicon and single-metal CMOS process. The cell structure will be revealed in Section II. The READ and ERASE/PROGRAM scheme of this memory will be explained in Sections III and IV, respectively. The measurement results of the device will be given in Section V.

II. CELL STRUCTURE

In this paper, the ERASE state is defined as the positive threshold shift of the floating-gate transistor, and the PROGRAM state is the negative. The electric field between the floating gate and the drain, which dominates the Fower–Nordheim current flow, is approximately given by

$$E = \frac{C_2 V_{CG} - (C_2 + C_3) V_D - Q_F}{d_1 C_T} \qquad (C_T = C_1 + C_2 + C_3)$$

where

- Q_F stored negative charge on the FG,
- C_1 thin oxide capacitance,
- C_2 control-gate capacitance,
- C_3 gate oxide capacitance,
- V_{CG} control-gate voltage,
- V_D drain voltage, and
- d_1 thin oxide thickness.

Now, we define an appropriate high voltage as V_{pp}. The ERASE conditions are $V_D = 0$, $V_{CG} = V_{pp}$, and the PROGRAM's are $V_D = V_{pp}$, $V_{CG} = 0$. A larger threshold shift ΔV_{th} is caused by a larger tunneling current, or a larger electric field. Although the most efficient way for increasing E is to increase V_{pp}, this approach is opposed to the reduction of the maximum applied voltage, which is required to achieve VLSI with higher packing density. So, it is natural to increase the ratio C_2/C_T or $(C_2 + C_3)/C_T$ to get sufficient ΔV_{th} with the limited applicable voltage and the thin oxide thickness.

Fig. 1 shows an optimized single-polysilicon cell layout for a high-density EEPROM, which is named DIFLOX (DIFfused Layer controlled floating-gate-type cell with thin OXide). It is composed of a select- and a floating-gate transistor. The floating-gate voltage is controlled by the capacitance coupling of the N^+ diffused layer and the drain through thin oxide. A large capacitance coupling value between the N^+ control gate and the floating gate can be obtained with this structure. The capacitance ratio C_2/C_T is mainly determined by the thin oxide area ratio, as the thin films are formed simultaneously. The ratio of DIFLOX is designed as 0.83. The equivalent circuit of the DIFLOX cell array configurations is shown in Fig. 2. The program line *PL* is connected to the diffused control gate via a transfer gate, which is controlled by the word line. It is to be noted that the N^+ region of the control gate is common to only one byte (eight cells). The N^+ implantation dose for this region must be chosen carefully. A lower concentration suppresses the effective applied voltage to the thin oxide in the negative gate bias condition, while a higher concentration lowers the barrier height of the thin oxide [17]. Under the optimized concentration applied to DIFLOX, the resistance and junction capacitance of the N^+ control-gate region were measured to be 20 kΩ and 14 fF, respectively. So the *RC* time constant is calculated to be lower than 1 ns, and the delay caused by this diffused layer is not a dominant factor on the access time.

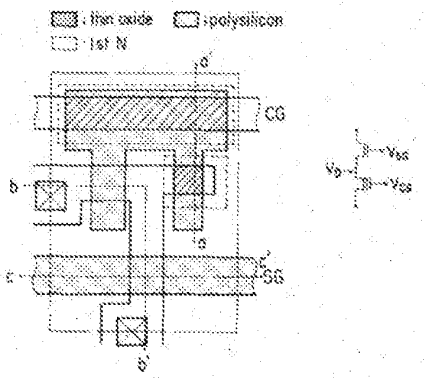


Fig. 1. Layout pattern of a new single-polysilicon EEPROM cell, named DIFLOX. The cell is composed of a select-gate and a floating-gate transistor.

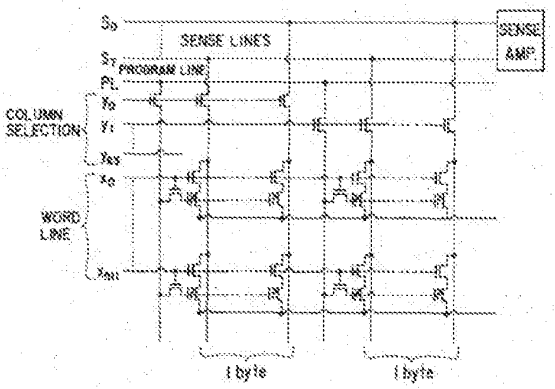


Fig. 2. Cell arrays of DIFLOX. The select gate is equivalent to the word line, and the control gate is connected to the program line (*PL*) via a transfer gate transistor.

To reduce the cell area of DIFLOX, the isolation between active regions is one of the most important technologies. A new isolation technology, SEPOX [18], was applied to the cell, which can realize a field distance between the active regions as narrow as the minimum dimension determined by the photoetching. In addition to this technology, a high-voltage structure was contrived to perform the ERASE/PROGRAM function. Fig. 3 shows the cross-sectional views of DIFLOX, along the lines $a-a'$, $b-b'$, and $c-c'$ in Fig. 1. As shown in Fig. 3(a), the high concentration N^+ below the thin oxide was covered with a lower doped zone of 0.2 μm thick. This structure improves the breakdown voltage of the p-n junction. In order to optimize the distance between the N^+ control gate and the drain, the field inversion effect under the floating gate

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 02,2010 at 22:49:44 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000510

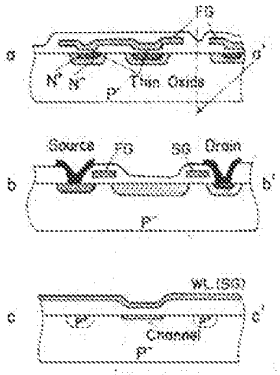


Fig. 3. Cross-sectional views of DIFLOX, along the lines a–a', b–b', and c–c' in Fig. 1.

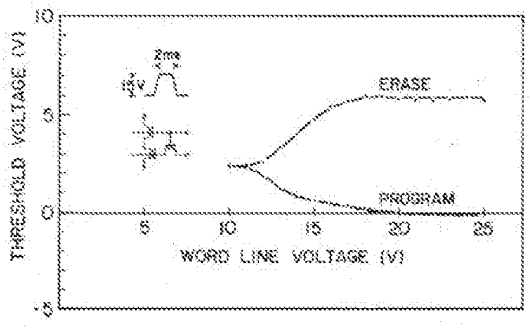


Fig. 5. Threshold shifts of DIFLOX in the ERASE/PROGRAM state as a function of a word-line voltage. $V_{pp} = 15$ V, $d_1 = 85$ A.

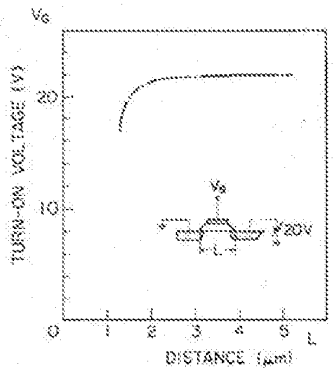


Fig. 4. Turn-on voltage of the field transistors as a function of the distance. It is defined as the leakage current exceeding 10^{-10} A/μm. The drain is biased to 20 V.

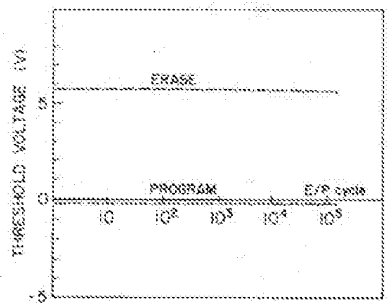


Fig. 6. Endurance characteristics of DIFLOX. $V_{pp} = 15$ V, $d_1 = 85$ A, $V_{WL} = 20$ V.

must be counted. By defining the turn-on voltage as the gate voltage at which the leakage current exceeds 10^{-10} A/μm under a drain bias of 20 V, the field turn-on voltages as a function of the length are measured as shown in Fig. 4. It is indicated that a 2-μm field length can guarantee the 15-V ERASE/PROGRAM operation. To eliminate the leakage current from the drain regions of the select- and floating-gate transistors to the substrate due to the avalanche breakdown, the source and drain of the select-gate transistors were doped with a low impurity concentration of 10^{17}/cm^3, as shown in Fig. 3(b). The value is about one order of magnitude lower than the usual lightly doped drain (LDD), used for 1.2-μm NMOS FET for 5-V circuits [21]. In order to reduce the contact resistance between the aluminum and the N^+ region, a high dose implantation of arsenic was carried out through the contact holes. This self-aligned formation of the diffusion area contributes to the cell area reduction. Only the source of the floating-gate transistor was formed by N^+, as is used for 5-V circuits.

In order to be able to design the peripheral circuits, the characteristics of the cell in the array of Fig. 2 must be analyzed. The V_{th} shift of DIFLOX cell in the erased and programmed state as a function of the select-gate voltage is shown in Fig. 5. The thin oxide thickness d_1 is 85 A, and a pulse of 15 V height, 2 ms width is provided to the program line or bit line. To obtain the wider threshold window, or eliminate the degradation by the select gate, the word-line voltage should be elevated above 20 V. This voltage might be achieved as it was. However, in order to take some margin, as is taken in the case of the drain control-gate voltage design, heavy channel-stop ion implantation was carried out between the select gates as shown in Fig. 3(c).

The read current measured with $V_{FL} = V_{BIT} = 2.5$ V and the word-line voltage $V_{WL} = 5$ V exceed 100 μA in the conductive state by employing 1.4-μm gate length, in spite of the series connection of two high-voltage transistors. The endurance characteristics of DIFLOX are shown in Fig. 6. Although it uses larger thin oxide area than the conventional double-polysilicon cells, no characteristics' degradation could be observed up to 10^5 ERASE/PROGRAM cycles.

The charge retention characteristics would be drastically degraded, if a thin oxide thickness of below 60 A were used, because of the direct tunneling effect of oxide. However, up to the thickness, the retention characteristics are mainly dominated by the barrier height of polysilicon oxide, surrounding the floating gate, rather than that of thin oxide [17]. So, the cell can guarantee the same retentivity as the conventional UV EPROM cell.

The microphotograph of the DIFLOX cell array is shown in Fig. 7.

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 02,2010 at 22:49:44 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000511

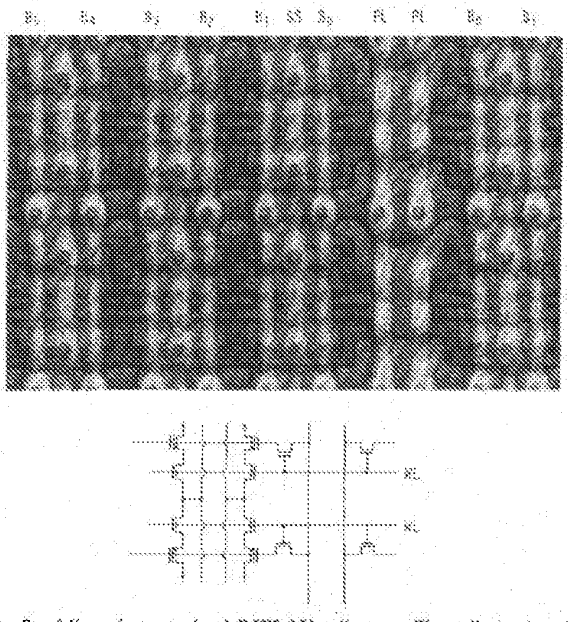


Fig. 7. Microphotograph of DIPLOX cell array. The cell size is 7.5 × 11.5 μm.

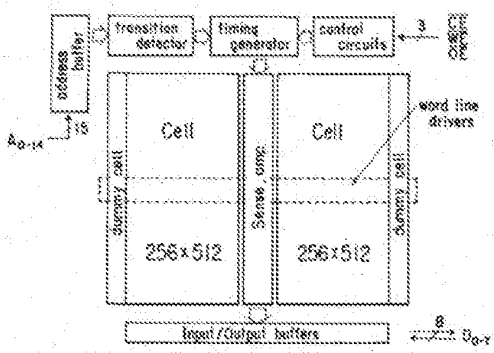


Fig. 8. Block diagram of 256-kbit EEPROM in the READ operation.

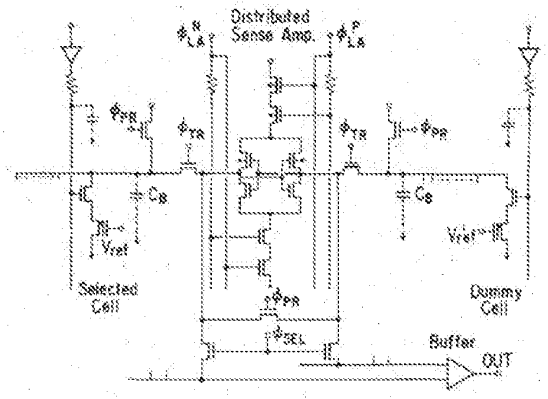


Fig. 9. Cell peripheral circuitry. Improved open-bit-line scheme and distributed sense amplifiers are shown.

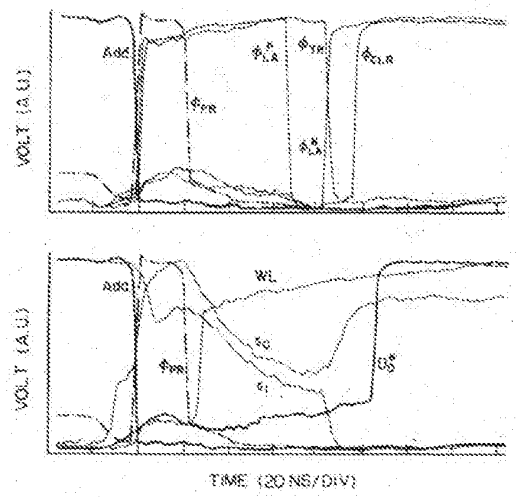


Fig. 10. Monitored waveforms of internal nodes, observed by the electron beam tester. x_0 and x_1 are two nodes of a sense amplifier, and D_0^* corresponds to the output signal before one buffer. The voltage levels are incorrect, not only absolutely, but also relatively, because they are disturbed by the electron scattering of neighbor patterns.

III. Open Bit-Line Structure

In order to compensate the large bit-line parasitic capacitance, an open bit-line scheme was improved and applied to the EEPROM. The block diagram of the memory in READ operation is shown in Fig. 8. The cell arrays are divided into left and right hemispheres, and the sense amplifiers are located between them. Every bit line has 256 cells and one dummy cell. When the memory cell on a hemisphere is selected, the dummy cell on the other side is selected as a reference. The cell peripheral circuitry in the READ operation is shown in Fig. 9. At the transition edge of the address input signals, the precharge pulse Φ_{PR} is generated internally. It precharges bit-line pairs and their corresponding sense-amplifier nodes, and equalizes them, simultaneously. The successive clocks triggered by Φ_{PR} control all of the reading procedure as follows. In the period of the precharge, the bit lines are raised to $V_{DD} - V_{th}$. The level is estimated to be 2.5 V by the body effect of NMOS FET. All word lines including the dummy cell's are biased to zero. When Φ_{PR} goes low, the selected- and the dummy-cell word lines are raised simultaneously. So, both bit-line levels begin to fall gradually, according to the conductance of the selected and dummy cells. As no pull-up devices are activated, the level variation in this free-running state is expected to be fast. In addition, the effect of the equivalent parasitic capacitances connected to the bit-line pairs compensate each other. After an appropriate period, Φ_{LA}^{n} goes low and then Φ_{LA}^{p} goes high. In other words, the sense amplifiers are activated, and the bit-line data are boosted by them. Finally, Φ_{TR} goes low and the bit lines are isolated from the sense amplifiers. In the quiescent state, as Φ_{CLR} goes high, the bit lines are biased to zero in order to eliminate the idle current and to avoid cell data destruction by noise. The program line *PL* is kept about 2.5 V during the READ operation. These internal timings of READ mode were verified by the tester with electron beams, as shown in Fig. 10. It is important for these open-bit-line schemes to synchronize the bit-line

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 02,2010 at 22:49:44 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000512

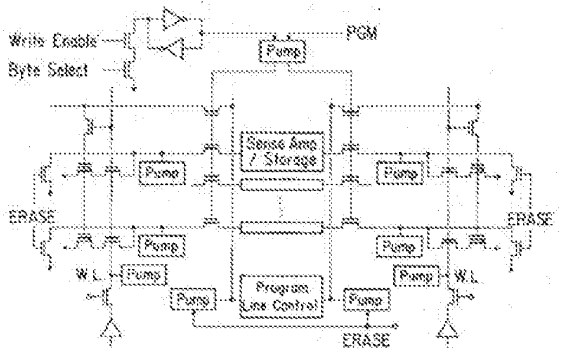


Fig. 11. Cell peripheral circuitry in ERASE/PROGRAM operation.

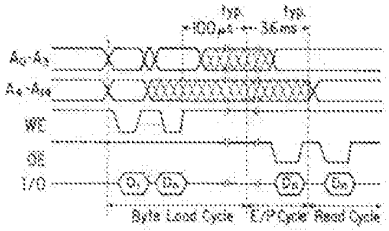


Fig. 12. Timing chart of the PAGE-MODE programming and the data polling.

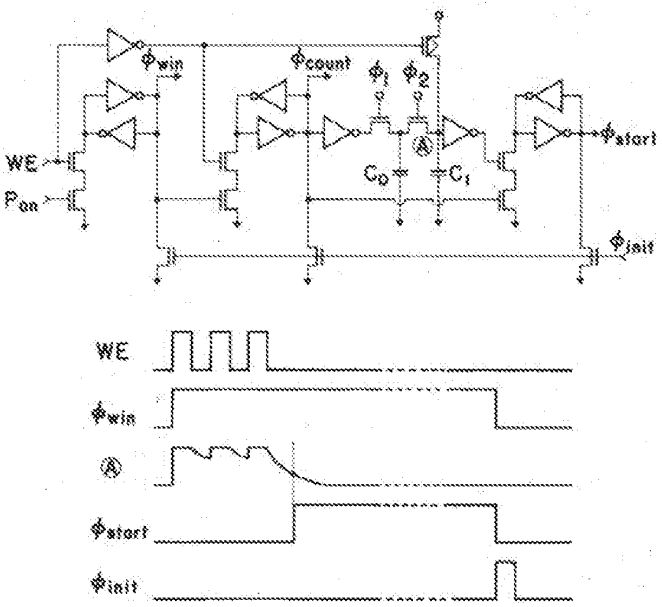


Fig. 13. Successive data loading control circuits (Φ_{start} generator). A period of 100 μs is counted by the switched capacitor.

signal variation associated with the word-line delay to the activation of sense amplifiers. So, a scheme of distributed sense amplifiers was applied. The activation of sense amplifiers is designed to depend on the distance from the word-line drivers, by adjusting the gate capacitance and the line resistance. This enables the bit-line data to be latched just at the time when the voltage difference reaches an appropriate level, wherever it may be located. It also reduces the large current peak caused by the sense-amplifier activation.

It is necessary for the nonvolatile memories that the logical data coincide with the physical data, which is different from the case of the RAM. Therefore the final output data are inverted on the buffer if they come from the left hemisphere. So the data in the chip clear state, which is defined as all cells in positive threshold, correspond to all one.

IV. ERASE/PROGRAM CONTROL CIRCUITS

The PAGE-MODE programming gives one solution to reduce the ERASE/PROGRAM (E/P) time. This feature applied to the 256-kbit EEPROM allows programming up to 16 byte (128 bits) simultaneously. The scheme fits into the open-bit-line structure, since the flip-flop which acts as a bit-line sense amplifier in the READ mode plays the role of a temporary storage for programming data, shown in Fig. 11. Therefore the data can be written in almost the same timing as a SRAM. The timing chart of E/P procedure is shown in Fig. 12. Once the WRITE ENABLE *WE* is detected by the chip, all the sense amplifiers are activated and isolated from the bit lines. The programming data are loaded to the latches successively. If the time, 100 μs, lapses without any *WE* input, the chip goes into the ERASE state automatically. In this state, the bit lines are biased to zero and the program lines of the selected columns are elevated to V_{pp}. Therefore the data of the selected cells are erased. Next, the chip turns in the PROGRAM state. Φ_{TR} goes high and the stored data are transferred to the bit lines. The charge pumps only elevate bit-lines of logical high to V_{pp}. As the *PL* is biased to zero, the programming is performed on the corresponding cells. As each byte storage has one additional flag latch, the E/P procedure is performed only on bytes that are actually being programmed.

The data polling function, shown in Fig. 12, is accomplished by reading the stored data on the sense amplifiers during the E/P state, which are inverted from the data to be read.

The timing circuits constructed by the switched-capacitor technique take care of the complicated E/P procedure. This technique is widely applied to recent MOS analog circuits such as digital filters [19], [20]. The lapse of the 100-μs waiting time for successive *WE* pulses is controlled by the Φ_{start} generator circuit as shown in Fig. 13. The rising and falling edges of the first *WE* pulse under an appropriate applied voltage V_{DD} above 4 V (P_{on} is high) cause two control signals, Φ_{win} and Φ_{count}, respectively. Φ_{win} initiates the flip-flops including flag latches, and Φ_{count} activates internal oscillator of 10 MHz and raises V_{pp}. This basic clock goes to some high-voltage pumps, and generates nonoverlap pulses Φ_1 and Φ_2. The voltage of node *A* falls gradually with the discharge of the capacitor. The *RC* time constant is calculated from the switched-capacitor theory as C_1/fC_0, where *f* is the frequency of Φ_1 and Φ_2. Every time the *WE* pulse becomes

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 02,2010 at 22:49:44 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000513

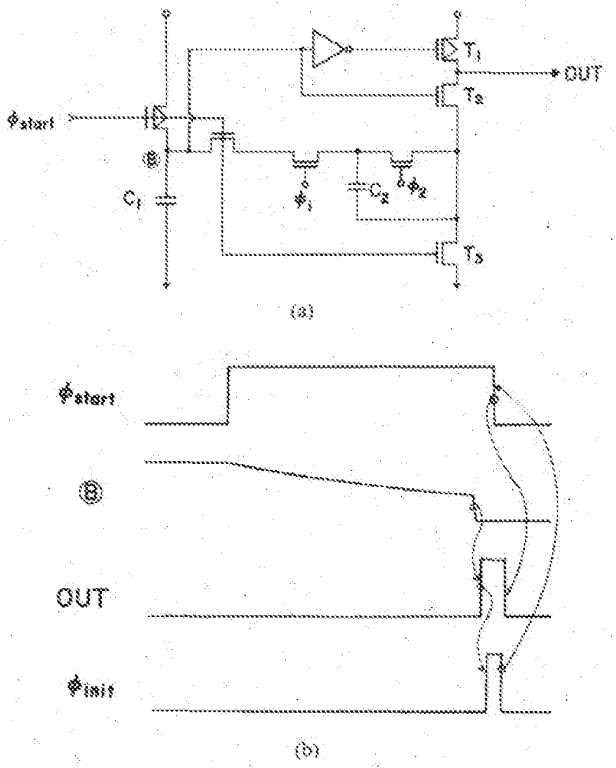


Fig. 14. (a) Timer circuit for ERASE/PROGRAM. Improved switched-capacitor technique is applied. It counts 1.8-ms lapse time. (b) Continued.

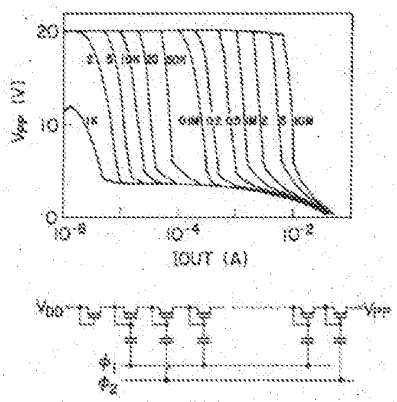


Fig. 15. Output characteristics of high-voltage generator. In the memory, the basic frequency of the internal oscillator is set to 10 MHz.

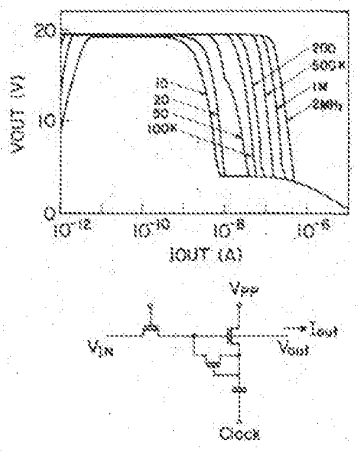


Fig. 16. Output characteristics of high-voltage pump. It is attached every bit and word line.

high, the capacitor C_1 is charged, or the state is initialized. At the crosspoint of the falling edge of node A and the threshold voltage of the next inverter, the clock Φ_{start} is generated. This Φ_{start} makes all E/P circuits active and initiates the second timer which controls longer time for E/P, as is shown in Fig. 14(a) and (b). This second timer designed by using a modified switched-capacitor technique counts the millisecond-order ERASE and PROGRAM time within the reasonable capacitance occupied area. In contrast with the conventional one, the voltage drop through the discharge capacitor C_2 is determined by the conductance ratio of two transistors, T_2 and T_3. In other words, the combination of higher conductance of T_2 and lower conductance of T_3 keeps the drain of T_3 high and makes the amount charge pumped out of C_1 small. Consequently, by adjusting the conductance ratio of T_2 and T_3, the capacitance area was reduced to about one-tenth in comparison with the conventional technique.

Figs. 15 and 16 show the drivability characteristics of the internal high-voltage generator and the pumping circuits. To supply sufficient current, this high-voltage generator (Fig. 15) has a comparatively low output impedance. The output terminal is clamped by the series connection of diodes for regulation. The rise time of this high voltage does not affect the thin oxide stress. On the other hand, the pumps (Fig. 16), which are attached to every bit and word line, have relatively small drive capability, which results in the decrease of the rising speed of the voltage for the lines connected to the tunnel oxides. The rise time was measured as 50 μs, and it reduces thin oxide stress.

V. Performance and Results

The microphotograph of the 5-V-only 256-kbit CMOS EEPROM is shown in Fig. 17. The die size is 6.23×7.33 mm and is packed into the DIP 28-pin standard package. It is pin-to-pin compatible with 256-kbit SRAM [21].

The chip contains several circuits which enable the chip clear and the READ margin check functions. They are activated by providing 12 V to appropriate pins.

The monitored waveforms of the internally generated V_{pp} and the E/P time control signal ϕ_{EP} and the WRITE ENABLE input clock $\overline{WE}$ are given in Fig. 18. It is indicated that V_{pp} is elevated to 20 V and that all the timings are well controlled corresponding to the PAGE-MODE programming. The total amount of the ERASE and PROGRAM time is 3.6 ms/16 byte at 5-V power supply.

The microphotograph of the address and data out waveforms with external 100-pF load is shown in Fig. 19. The address access time of 150 ns was successfully ob-

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 02,2010 at 22:49:44 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000514

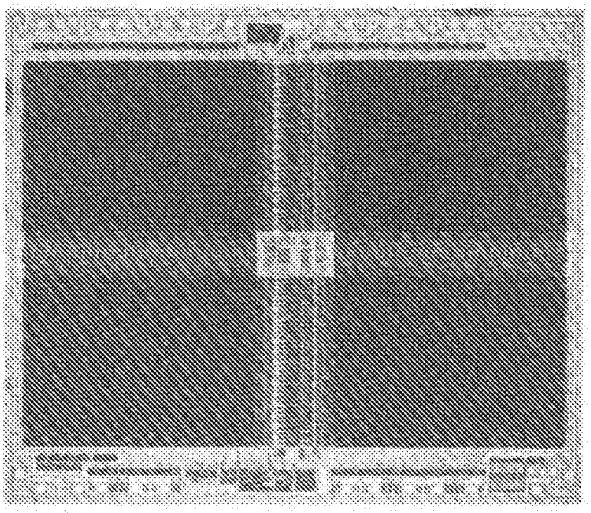


Fig. 17. Microphotograph of the whole chip of 256-kbit EEPROM. The size is 7.33×6.23 mm^2.

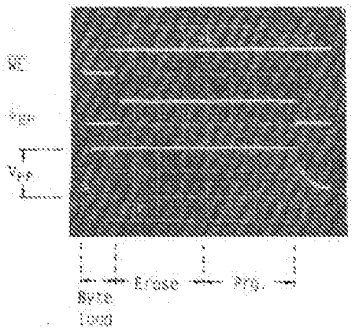


Fig. 18. The monitored waveforms of Φ_{EP} and V_{pp}. V_{pp} is elevated to 20 V.

tained with a nominal 5-V voltage supply. The active power dissipation is 80 mW. Similar to the other CMOS devices, the active power dissipation depends on the READ cycle time. It reduces to 35 mW at a 1-MHz READ cycle, and drops below 1 μW at the STANDBY mode.

The characteristics of this EEPROM are summarized in Table I.

VI. Conclusion

A 5-V-only 256-kbit CMOS EEPROM employing a new single-polysilicon cell, DIFLOX, has been successfully designed and fabricated. Exploiting 1.2-μm design rules and 1.4-μm gate length, the cell size was reduced to 86.25 μm^2. The cell was designed to eliminate any leakage current caused by the junction breakdown and the field inversion. The cell, which offers a 5-V threshold window between the ERASE and PROGRAM state, allows 100-μA reading current in the conductive state. It guarantees over 10^5 ERASE/PROGRAM cycles. By employing the PAGE-MODE programming, the EEPROM allows successive data load up to 16 bytes with the same timings as an SRAM. The ERASE/PROGRAM is carried out at once within 3.6 ms. All timings are controlled by several kinds of clocks, all of which are generated internally by timers constructed by the switched-capacitor technique. The improved open bit-line scheme was applied for the READ operation. This internally synchronous architecture fits with the PAGE-MODE programming, because the sense amplifiers are also used to share the internal storage of the programming data. Due to the CMOS circuit configuration, the chip offers extremely small standby power dissipation.

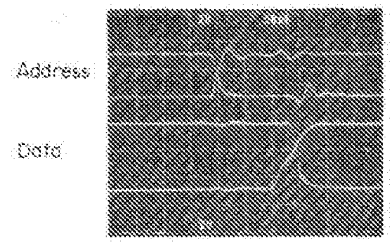


Fig. 19. The oscillograph of the address and data out waveforms with external loads.

TABLE I
Characteristics of 5-V-only 256-kbit EEPROM

Organization	32K words $\times$ 8 bit
Operation	Fully asynchronous (with internal clocks)
Technology	N-well CMOS (single poly & single Al)
Minimum gate length	1.4 μm
Gate oxide thickness	250 A
Thin oxide thickness	85 A
Cell size	86.25 μm^2
Die size	7.33×6.23 mm^2
I/O interface	TTL
Address access time	150 ns (typical)
Chip select-access time	150 ns (typical)
ERASE/PROGRAM time	3.6 ms (typical) (16-byte page)
Active power	80 mW 35 mW (1 MHz)
Standby power	1 μW
Package	28-pin DIP (256-kbit CMOS SRAM compatible)

Acknowledgment

The authors would like to thank T. Sako for his design support, and S. Tanaka and Dr. Y. Nishi for their encouragement throughout the work and useful suggestions.

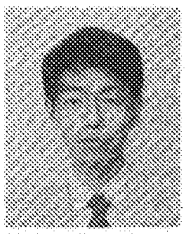
References

[1] P. I. Suciu, M. Briner, C. S. Bill, and D. Rinerson, "A 64K EEPROM with extended temperature and page mode operation," in *1985 ISSCC Dig. Tech. Papers*, Feb. 1985, p. 170.
[2] R. Jolly, R. Tesch, K. Campbell, D. Tennant, J. Oliuad, B. Cremen, R. Lefferts, and P. Andrews, "Two 35ns 64K CMOS EEPROMs," in *1985 ISSCC Dig. Tech. Papers*, Feb. 1985, p. 172.
[3] S. Mihrotra, T. C. Wu, T. L. Chiu, and G. Perlegos, "A 64Kb

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 02,2010 at 22:49:44 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000515

CMOS EEPROM with on-chip ECC," in *1984 ISSCC Dig. Tech. Papers*, Feb. 1984, p. 149.
[4] F. Jones and A. Lancaster, "EEPROM adapts easily to in-system changes," *Electron. Des.*, p. 189, Aug. 1983.
[5] C. Kuo, J. Yeargain, W. Downey, K. Ilgenstein, J. Jorvig, S. Smith, and A. Bormann, "An 80-ns 32K EEPROM using the FETMOS cell," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 5, p. 821, Oct. 1982.
[6] G. Landers, "5-volt-only EEPROM mimics static-RAM timing," *Electronics*, vol. 55, p. 127, 1982.
[7] S. Logie, E. Hanari, S. Li, W. Lin, and R. Das, "A new floating gate cell and technology for a 5V only CMOS 16K EEPROM," in *IEDM Dig. Tech. Papers*, Dec. 1983.
[8] M. Wada, M. Asano, H. Iwahashi, S. Inoue, R. Kirisawa, K. Hieda, and T. Shibata, "A 50msec 64Kbit CMOS EEPROM with 200msec programming," in *1985 Symp. VLSI Tech.* May 1985, p. 96.
[9] S. K. Lai, Y. W. Hu, S. Tam, G. K. Lum, and V. K. Dham, "Design of an EEPROM memory cell less than 100 square microns using 1 micron technology," in *IEDM Dig. Tech. Papers*, Dec. 1984, p. 468.
[10] C. Kuo, K. Fu, P. Kim, M. Chonko, J. Jorvig, J. R. Yeargain, and J. J. Barnes, "High density FETMOS EEPROM cell using ONO inter-polysilicon dielectrics," in *1985 Symp. VLSI Tech.*, May 1985, p. 76.
[11] K. Shinada, Y. Nagakubo, K. Yoshikawa, and K. Kanzaki, "Current leakage through thermal oxide films grown on patterned polysilicon layers," in *ECS Extended Abstr.*, vol. 83-2, 1984, p. 354.
[12] R. Cuppens, C. Hartgring, J. Verway, and H. Peek, "An EEPROM for microprocessors and custom logic," in *1984 IEEE ISSCC Dig. Tech. Papers*, Feb. 1984, p. 268.
[13] J. Miyamoto, S. Saito, H. Momose, H. Shibata, K. Kanzaki, and T. Iizuka, "A high speed 64K CMOS SRAM with bipolar sense amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 5, p. 578, Oct. 1984.
[14] S. Atsumi, S. Tanaka, K. Shinada, K. Yoshikawa, K. Makita, Y. Nagakubo, and K. Kanzaki, "Fast programmable 256K read only memory with on-chip test circuits," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 1, p. 422, Feb. 1985.
[15] O. Minato, T. Masuhara, T. Sasaki, Y. Sakai, and T. Hayashida, "HI-CMOSII 8K×8bit static RAM," in *1982 IEEE ISSCC Dig. Tech. Papers*, Feb. 1982, p. 256.
[16] K. H. Hardee and R. Sud, "Fault tolerant 30 ns/375 mW 16K×1 NMOS static RAM," *IEEE J. Solid-State Circuits*, vol. SC-16, p. 435, Oct. 1981.
[17] N. Matsukawa, S. Morita, K. Shinada, J. Miyamoto, J. Tsujimoto, T. Iizuka, and H. Nozawa, "A high density single-polysilicon structure EEPROM with LB (lowered barrier height) oxide for VLSI's," in *1985 Symp. VLSI Tech.*, May 1985, p. 100.
[18] N. Matsukawa, H. Nozawa, J. Matsunaga, and S. Kohyama, "Selective polysilicon oxidation technology for VLSI isolation," *IEEE Trans. Electron Devices*, vol. ED-29, no. 4, p. 561, Apr. 1982.
[19] B. J. Hosticka, R. W. Brodersen, and P. R. Gray, "MOS sampled data recursive filters using switched capacitor integrators," *IEEE J. Solid-State Circuits*, vol. SC-12, p. 600, Dec. 1977.
[20] R. Gregorian, Y. A. Haque, R. Mao, R. Blasco, and W. E. Nicholson Jr., "CMOS switched-capacitor filter for a two-chip PCM voice coder," in *1979 ISSCC Dig. Tech. Papers*, Feb. 1979, p. 28.
[21] T. Sakurai, M. Isobe, T. Ohtani, K. Sawada, A. Aono, H. Nozawa, T. Iizuka, and S. Kohyama, "A low power 46-ns 256-kbit CMOS static RAM with dynamic double word line," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 5, p. 578, Oct. 1984



Jun-ichi Miyamoto was born in Kamakura, Japan, on July 6, 1949. He received the B.S. and M.S. degrees in electronic engineering from Kyoto University, Kyoto, Japan, in 1973, and 1975, respectively.

In 1975, he joined Toshiba R&D Center and worked on the development of bipolar integrated circuits such as IIL, ECL RAM, and PROM. Since 1982 he has been engaged in the circuit and device designs of CMOS static RAM and EEPROM at Toshiba Semiconductor Device Engineering Laboratory, Kawasaki, Japan. He is currently a Visiting Research Scholar at the Computer Systems Laboratory at Stanford University, Stanford, CA, on one-year assignment.

Mr. Miyamoto is a member of the Institute of Electronics and Communication Engineers of Japan.



Jun-ichi Tsujimoto was born in Osaka, Japan, on May 26, 1953. He received the B.S. and M.S. degrees in mathematics from Osaka University, Osaka, Japan, in 1977 and 1979, respectively. He researched partial differential equations from 1979 to 1983 at Osaka University.

In 1983 he joined Toshiba Semiconductor Device Engineering Laboratory, Kawasaki, Japan. Since 1983 he has been engaged in the circuit design of EEPROM's and in the development of CAD.

Mr. Tsujimoto is a member of the Mathematical Society of Japan.



Naohiro Matsukawa was born in Tokyo, Japan, on October 4, 1952. He received the B.S. degree in high energy physics from Tokyo University of Agriculture and Technology, Tokyo, Japan, in 1975 and the M.S. and Ph.D. degrees in solid state physics from the University of Tokyo, Tokyo, Japan, in 1977 and 1982, respectively.

In 1980 he joined Toshiba Semiconductor Device Engineering Laboratory, Kawasaki, Japan, where he has been engaged in the process of CMOS static and nonvolatile memory. He is interested in isolation technology and thin oxide.

Mr. Matsukawa is a member of the Physical Society of Japan and the Japan Society of Applied Physics.



Shigeru Morita was born in Tokyo, Japan, on September 21, 1955. He graduated from Koganei Industrial Senior High School, Tokyo, Japan, in 1974.

In 1974 he joined the IC Laboratory of the Toshiba Research and Development Center, Kanagawa, Japan, where he mainly studied chemical vapor deposition technology. Since December of 1978, he has been with the Toshiba Semiconductor Device Engineering Laboratory, Kawasaki, Japan, where he has studied the development of fabrication processes for nonvolatile ROM's and CMOS RAM's.

Mr. Morita is a member of the Japan Society of Applied Physics and the Institute of Electronics and Communication Engineers of Japan.



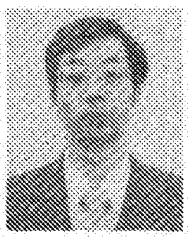
Kazuyoshi Shinada was born in Saitama, Japan, on May 21, 1945. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from Waseda University, Tokyo, Japan.

In 1975 he joined Toshiba Research and Development Center, Tokyo Shibaura Electric Co. Ltd., Kawasaki, Japan. He performed research on process technologies of bipolar digital integrated circuits, such as IIL, ECL memory, and PROM. Since 1982 he has been developing the device process and reliability of nonvolatile memories at Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki, Japan.

Dr. Shinada is a member of Japan Society of Applied Physics.

Authorized licensed use limited to: Andrew Bateman. Downloaded on April 02,2010 at 22:49:44 EDT from IEEE Xplore. Restrictions apply.

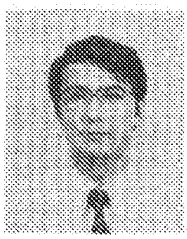
Sandisk Technologies, Inc. - Ex. 1002, Page 000516



Hiroshi Nozawa was born in Kanagawa Prefecture, Japan, on December 10, 1947. He received the B.S. and M.S. degrees in metal science and technology from Kyoto University, Kyoto, Japan, in 1970 and 1972, respectively.

In 1972 he joined the Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he was engaged in the development of EPROM processes. Since 1979, he has been engaged in the development of high-density CMOS memory processes, isolation technology, and high-density nonvolatile memory processes. He is currently Manager of the Advanced CMOS Technology Group in the Semiconductor Device Engineering Laboratory.

Mr. Nozawa is a member of the Japan Society of Applied Physics and the Institute of Electronics and Communication Engineers of Japan.



Tetsuya Iizuka (M'79) was born in Ibaraki, Japan, on April 17, 1947. He received the B.S. degree in applied physics, and the M.S. and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1970, 1972, and 1975, respectively.

In 1975, he joined the Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he was engaged in research on IIL and CMOS/SOS devices and in development of dynamic RAM testing method. In 1979, he transferred to a newly organized laboratory, the Semiconductor Device Engineering Laboratory (SDEL), Toshiba Corporation, Kawasaki, Japan, where he developed first generations of 16K, 64K, and 256K CMOS SRAM's. In 1981, he stayed for one year at the Integrated Circuit Laboratory, Hewlett-Packard Co., Palo Alto, CA, as a Visiting Engineer. He worked on CMOS latch-up modeling and bird's-beak free isolated MOST analysis. He is presently Manager of the Advanced SRAM, EPROM, and EEPROM Design Group of the SDEL.

Dr. Iizuka is a member of the Institute of Electrical and Communication Engineers of Japan.

Authorized licensed use limited to: Andrew Sateman. Downloaded on April 02,2010 at 22:49:44 EDT from IEEE Xplore. Restrictions apply.

Sandisk Technologies, Inc. - Ex. 1002, Page 000517

Performance Improvement of SONOS Memory by Bandgap Engineering of Charge-Trapping Layer

Tung-Sheng Chen, Kuo-Hong Wu, Hsien Chung, and Chin-Hsing Kao

Abstract—**A significant improvement in device performance and reliability characteristics of silicon–oxide–nitride–oxide–silicon (SONOS) Flash memory has been achieved. Superior endurance characteristic shows no sign of degradation even after 10^6 program/erase cycles and an extrapolated ten-year detection window of 1.4 V has been attained from retention measurement. The dramatic improvement results from a bandgap engineering of the SiN charge-trapping layer. With a gradual variation of the Si/N ratio from bottom to top of nitride film rather than uniform standard composition, a large number of highly accessible trapping levels are created in addition to the deepened barrier height between nitride and tunnel oxide that reduces back-tunneling probability. The proposed technique shall be valuable in pushing Flash memory technology into the next generation.**

Index Terms—**Endurance, reliability, retention, silicon–oxide–nitride–oxide–silicon (SONOS).**

I. Introduction

SONOS Flash memory devices have been considered a potential replacement of floating-gate structures for next-generation nonvolatile semiconductor memory applications due to their numerous advantages such as excellent scalability, high density, and radiation hardness [1]–[3]. However, the reliability issues such as endurance and retention characteristics in addition to the small detection-window nature have hindered the progression of SONOS Flash memory toward mainstream portable solid-state memory products [4], [5]. The crucial problem of many efforts that have been made to improve the performance of SONOS devices is the insufficient charge-trapping efficiency of the silicon nitride layer. In this letter, a bandgap engineering technique by varying relative Si/N ratio from high to low during the deposition process has been proposed, and the composition profile of silicon nitride from silicon-rich at the bottom toward nitrogen-rich on top has been formed. The purpose of nitride-composition variation is to alter nitride bandgap so that sufficient available trapping levels are accessible to incoming charges during program operation. In addition, the back-tunneling probability of substrate-injected charges can be reduced significantly with silicon-rich-at-bottom composition due to the increased barrier height between nitride and tunnel oxide.

Manuscript received November 5, 2003; revised December 27, 2003. This work has been supported in part by eMemory Company and the National Nano Device Laboratory (NDL). The review of this letter was arranged by Editor S. S. Chung.

T.-S. Chen and H. Chung are with the Department of Electric Engineering, Chung-Cheng Institute of Technology, National Defense University, Taoyuan 33501, Taiwan, R.O.C. (e-mail: tschen@ccit.edu.tw).

K. H. Wu is with School of Defense Science,Chung-Cheng Institute of Technolgy, National Defense University, Taoyuan 33501, Taiwan, R.O.C.

C.-H. Kao is with the Department of Applied Physics, Chung-Cheng Institute of Technology, National Defense University, Taoyuan 33501, Taiwan, R.O.C.

Digital Object Identifier 10.1109/LED.2004.825163

II. Sample Preparation

The SONOS test devices were fabricated by a standard CMOS process on (100) p-type substrate (2 to 3 Ωcm), except the oxide–nitride–oxide (ONO) structure formation and the key process steps of the dielectrics are described as follows. A 3-nm-thick tunnel oxide was formed by diluted N_2O dry oxidation with a gas flow ratio of $N_2O : N_2 = 1 : 1$ (slm) at 800 °C. Next, a 5-nm-thick silicon nitride was deposited in a low-pressure chemical vapor deposition (LPCVD) reactor under various process conditions at 780 °C, and the gas flow-rate control of SiH_2Cl_2 and NH_3 was utilized to manipulate relative Si/N profile during film deposition [6]. The relative gas flow-rate ratio of SiH_2Cl_2/NH_3 for standard nitride, uniform silicon-rich nitride, and modified nitride (from silicon-rich-at-bottom to nitrogen-rich-on-top) are 0.23, 2.07, and 2.07 → 0.1, respectively. Then, a 4.5-nm-thick blocking oxide formed by LPCVD tetraethylorthosilicate (TEOS) was deposited on top of nitride at 700 °C. The final equivalent oxide thickness (EOT) of the ONO stack is 10.3 nm determined by high-frequency capacitance–voltage (C–V) characterization. After the ONO stack was formed, the $POCl_3$-doped polysilicon deposition, gate pattern, contact hole opening, source/drain (S/D) implant, and the rest of the process simply followed standard CMOS procedure.

III. Results and Discussion

The proposed bandgap engineering of the silicon nitride layer with modified Si/N ratio profile in the SONOS structure can be illustrated by the band diagram as shown in Fig. 1. The purpose of the tapered nitride bandgap from a nitrogen-rich side to a silicon-rich side is to create more accessible trapping levels for the electrons injected from the substrate. As shown in Fig. 1, the electrons that fell in shallow trapping levels can be transferred to adjacent deeper levels easily by lateral hopping. In addition, the increased barrier height between nitride and oxide that reduces the back-tunneling probability also helps in promoting the charge-trapping efficiency of the nitride layer. For standard nitride, most deep trapping levels are buried underneath and may not be able to capture electrons as simple as shallow levels. On the other hand, the trapping levels of uniform silicon-rich nitride are simply too shallow to grasp electrons firmly and, hence, lead to high detrapping rate and lower trapping efficiency. The availability and accessibility of trapping levels have exhibited signif-

0741-3106/04$20.00 © 2004 IEEE

Sandisk Technologies, Inc. - Ex. 1002, Page 000518

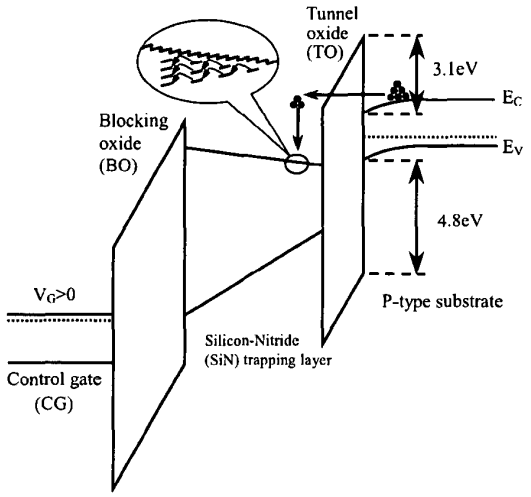


Fig. 1. Band diagram of SONOS structure with modified nitride composition illustrates that the trapping levels become more accessible through lateral hopping.

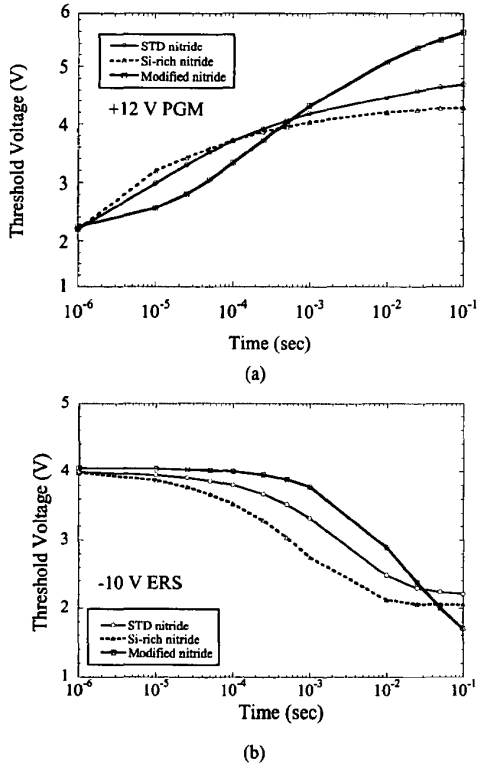


Fig. 2. (a) Threshold voltage shift after +12 V program and (b) −10 V erase operation for SONOS device indicates that modified nitride provides wide operation window and reasonable speed.

icant impact on program speed and endurance characteristics, as shown in Figs. 2 and 3.

In Fig. 2(a), standard nitride and uniform nitride appear to be charged faster than modified nitride at first (< 0.5 ms) due to their abundant shallow trapping levels, but they also saturate quickly since most shallow trapping levels are filled up in a short time. Since the deep trapping levels of standard nitride

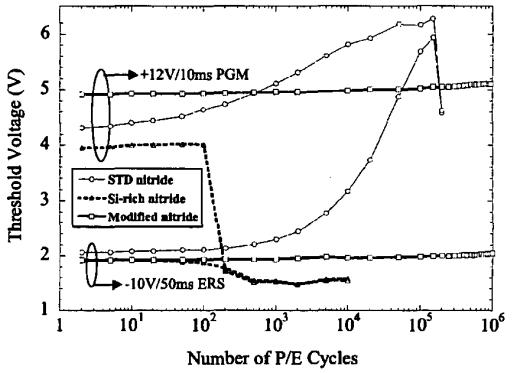


Fig. 3. Superior endurance characteristic of SONOS device with modified nitride layer shows no sign of degradation even after 10^6 program/erase cycles while those with standard nitride and uniform silicon-rich nitride degrade very fast.

are not competitive in capturing electrons, they contribute very little to the threshold voltage shift during program operation. The continuous growth of threshold voltage for the case of modified nitride as program time exceeds 0.5 ms indicates that many more trapping levels are accessible to the injected electrons. Although modified nitride seems to exhibit slower erasing speed, as shown in Fig. 2(b), due to higher charge-storage capacity, a reasonable erase time of approximately 50 ms should be adequate since block erase is a common Flash operation mode. As a result, an expanded operation window of SONOS memory device is realized with a modified nitride. In Fig. 3, the endurance characteristics clearly demonstrate the ability of the modified nitride to capture and release electrons easily without degradation, even after 10^6 program/erase cycles. The ascending trend of threshold voltage after program/erase cycles in the case of standard nitride indicates that electrons are gradually accumulated in the nitride layer and are difficult to be driven out, even under erasing operation. It is believed that the slower and irreversible electron transition from shallow levels down to deep levels after many operation cycles may be responsible for the accumulation. Eventually, the nitride saturates after certain cycles of operation when remnant charges finally fill up all of the available trapping levels. The endurance degradation of standard nitride samples is rather fast since higher operation voltage and longer stress time are adopted in this work [7]. For uniform silicon-rich nitride, the extremely shallow trapping levels lose their tapping ability very soon after few operation cycles.

The other critical challenge for SONOS devices is to maintain a long retention time. The retention property is mostly dominated by the insulating property of tunnel oxide for SONOS structure [8]. In our design, N_2O grown oxide has proven to be quite efficient in blocking back-tunneling electrons, and the wider detection window of the SONOS device with modified nitride can be attributed to the larger threshold voltage shift at the beginning, as shown in Fig. 4. The fact that all devices exhibit comparable slopes implies that the nitride layer does not have significant influence on retention characteristics in our experiment.

IV. Conclusion

SONOS Flash memory devices with excellent performance have been developed by nitride bandgap engineering. A nitride

Sandisk Technologies, Inc. - Ex. 1002, Page 000519

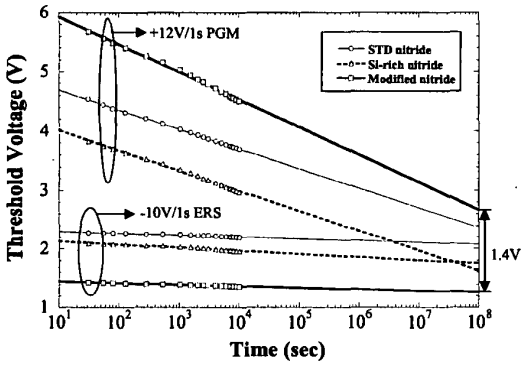


Fig. 4. Much wider detection window after ten years can be expected in retention test for SONOS device with modified nitride compared to those with standard nitride and uniform silicon-rich nitride.

with varied relative Si/N ratio throughout the film has increased the charge-trapping efficiency significantly. The experimental results from this work indicate that SONOS devices with superior endurance and retention characteristics for Flash memory application can be achieved if an optimized process of fabricating nitride charge-trapping layer is adopted.

ACKNOWLEDGMENT

The authors would like to thank the National Nano Device Laboratory for technical assistance.

REFERENCES

[1] M. L. French, C.-Y. Chen, H. Sathianathan, and M. H. White, "Design and scaling of a SONOS multidielectric device for nonvolatile memory applications," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 17, pp. 390–397, Mar. 1994.

[2] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A novel localized trapping, 2-bit nonvolatile memory cell," *IEEE Electron Device Lett.*, vol. 21, pp. 543–545, Aug. 2000.

[3] D. Williams, J. Marthinuss, R. Bishop, D. Adams, M. Knoll, R. McClintock, and J. Murray, "A qualified radiation hardened EEPROM for space and tactical weapons applications," in *Proc. IEEE National Aerospace and Electronics Conf.*, vol. 2, 1994, pp. 761–764.

[4] P. Pavan, R. Bez, P. Olovo, and E. Zanoni, "Flash memory cells-an overview," *Proc. IEEE*, vol. 85, pp. 1248–1271, Aug. 1997.

[5] J. Bu and M. White, "Effects of two-step high temperature deuterium anneals on SONOS nonvolatile memory devices," *IEEE Electron Device Lett.*, vol. 22, pp. 17–19, Jan. 2001.

[6] H. J. Stein and W. A. R. Wegener, "Chemically bound hydrogen in CVD Si_3N_4: Dependence on NH_3/SiH_4 ratio and on annealing," *J. Electrochem. Soc.*, vol. 124, p. 908, 1997.

[7] M. She, H. Takeuchi, and T.-J. King, "Silicon-nitride as a tunnel dielectric for improved SONOS-type Flash memory," *IEEE Electron Device Lett.*, vol. 24, pp. 309–311, May 2003.

[8] W. J. Tsai, S. H. Gu, N. K. Zous, C. C. Yeh, C. C. Liu, C. H. Chen, T. Wang, S. Pan, and C. Y. Lu, "Cause of data retention loss in a nitride-based localized trapping storage Flash memory cell," in *Proc. IEEE Int. Reliability Physics Symp.*, 2002, pp. 34–38.

Sandisk Technologies, Inc. - Ex. 1002, Page 000520

Europäisches Patentamt
European Patent Office
Office européen des brevets

European Patent Office
80298 MUNICH
GERMANY
Tel: +49 89 2399 0
Fax: +49 89 2399 4465

Cooper, John
Murgitroyd & Company
Scotland House
165-169 Scotland Street
Glasgow G5 8PL
ROYAUME-UNI

Formalities Officer
Name: Condron, Millie
Tel: +49 89 2399 - 2296
or call
+31 (0)70 340 45 00

Substantive Examiner
Name: Ley, Marc
Tel: +49 89 2399 - 5253

Application No.	Ref.	Date
13 767 422.2 - 1552	P168307.EP.01/J	30.03.2017
Applicant: Cypress Semiconductor Corporation		

Communication pursuant to Article 94(3) EPC

The examination of the above-identified application has revealed that it does not meet the requirements of the European Patent Convention for the reasons enclosed herewith. If the deficiencies indicated are not rectified the application may be refused pursuant to Article 97(2) EPC.

You are invited to file your observations and insofar as the deficiencies are such as to be rectifiable, to correct the indicated deficiencies within a period

of 4 months

from the notification of this communication, this period being computed in accordance with Rules 126(2) and 131(2) and (4) EPC. One set of amendments to the description, claims and drawings is to be filed within the said period on separate sheets (R. 50(1) EPC).

If filing amendments, you must identify them and indicate the basis for them in the application as filed. Failure to meet either requirement may lead to a communication from the Examining Division requesting that you correct this deficiency (R. 137(4) EPC).

Failure to comply with this invitation in due time will result in the application being deemed to be withdrawn (Art. 94(4) EPC).

Registered letter

Ley, Marc
Primary Examiner
For the Examining Division

Enclosure(s): 4 page/s reasons (Form 2906)

The examination is being carried out on the **following application documents**

Description, Pages

1-34	as published	

Claims, Numbers

1-5	filed in electronic form on	03-02-2017

Drawings, Sheets

1/12-12/12	as published

Reference is made to the following documents; the numbering will be adhered to in the rest of the procedure.

D1	US 8 222 688 B1
D2	US 2011/248332 A1
D3	US 2008/054346 A1
D4	WO 2013/148112 A1

1 The amendments filed with the letter dated 3-02-2017 introduce subject-matter which extends beyond the content of the application as filed, contrary to Article 123(2) EPC. The amendments concerned are the following:

Claim 1 is directed to a memory device comprising (i) a first oxynitride layer that comprises a concentration of carbon selected to increase the number of traps therein and comprising (ii) an anti-tunnelling layer comprising an oxide.

The combination of the features of claims 2 - 5 and features (i) and (ii) is not disclosed in the application as originally filed. A concentration of carbon selected to increase the number of traps in the first first oxynitride layer is disclosed in paragraph [0036] for the planar device of figure 2, which clearly has no anti-tunnelling layer according to claim 1 on file and which clearly does not contain a silicon nanowire or a finFET.

In addition, PCT claims 9 - 14 do not disclose the subject matter of claims 2 - 5 on file.

Sandisk Technologies, Inc. - Ex. 1002, Page 000523

The subject matter of claims 2 - 5 is therefore novel over the application as originally filed so that the requirements of Article 123(2) EPC are not met. Claims 2 - 5 have to be deleted.

2 The application does not meet the requirements of Article 84 EPC, because claims 1 - 5 are not clear.

2.1 The terms "substantially trap free" and "trap dense" used in claim 1 are vague and unclear and leave the reader in doubt as to the meaning of the technical features to which they refer, thereby rendering the definition of the subject-matter of claim 1 and all dependent claims unclear (Article 84 EPC). From the wording of claim 1, it remains unclear for the skilled reader which are the ranges of trap concentrations to be defined by the above terms. It should be noted that a layer, and in particular a charge storing layer, is never 100 % free of traps. As the description itself does not provide any clarifications, it is understood that, according to claim 1, the trap concentration in the first oxynitride layer is lower than the trap concentration in the second oxynitride layer.

The applicant argued that the terms are clear for the skilled reader, because they are related to, and a consequence of, the difference in oxygen concentration in the first and second oxynitride layers. This argument is not accepted, because claim 1 is not limited to trap concentrations implied by the presence of oxygen. The examining division is of the opinion that the concentrations of traps in the first and second oxynitride layers are not necessarily a consequence of the concentration of oxygen.

2.2 According to claim 1, the first oxynitride layer is separated from the second oxynitride layer by an anti-tunnelling layer comprising an oxide, which indicates that the device comprises three distinctive layers: 1) the first oxynitride layer, 2) the anti-tunnelling layer and 3) the second oxynitride layer.

According to claim 5, however, the anti-tunnelling layer is a part of the first first oxynitride layer, so that the device comprises only two layers. This contradiction renders claim 5 unclear (Article 84 EPC).

In addition, device claim 5 defines the device by means of its manufacturing method "that has been oxidised by radical oxidation". A skilled person cannot compare a given device with the subject matter of claim 5, because for a finished device, it is not possible to determine if the anti-tunnelling layer is made by radical oxidation of a part of the first oxynitride layer or not.

Sandisk Technologies, Inc. - Ex. 1002, Page 000524

2.3 The term "anti-tunneling layer" used in claim 1 is vague and unclear and leaves the reader in doubt as to the meaning of the technical feature to which it refers, thereby rendering the definition of the subject-matter of said claim unclear (Article 84 EPC). The term anti-tunneling has no recognized meaning for the skilled person. It is understood that a layer comprising oxide is to be considered as an anti-tunnelling layer.

3 The subject-matter of claim 1 is not new within the meaning of Article 54(1) and (2) EPC for the reasons given in section 4 of the previous communication.

D2 discloses that the first oxynitride layer is separated from the second oxynitride layer by an anti-tunnelling layer comprising an oxide ([0049]), that the second oxynitride layer further comprises a concentration of carbon selected to increase the number of traps therein ([0031]).

4 Should the applicant intend to overcome the above objections by deleting feature (i) from claim 1, then the subject-matter of claim 1 is not new within the meaning of Article 54(1) and (2) EPC for the reasons given in section 3 of the previous communication.

D1 discloses (figure 11) a memory device comprising: a channel (112) formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; and a gate (1502) having multiple surfaces abutting the channel, the gate comprising: a tunnel oxide layer (116) overlaying the channel (112); and a multi-layer charge storing layer including a first oxynitride layer (1519) closer to the tunnel oxide layer and a second oxynitride layer (1518), wherein the first oxynitride layer is separated from the second oxynitride layer by an anti-tunnelling layer (1521) comprising an oxide, and wherein the first oxynitride layer is a substantially trap-free, oxygen-rich, oxynitride layer and the second oxynitride layer is a trap dense, oxygen-lean, oxynitride layer ~~which further comprises a concentration of carbon selected to increase the number of traps therein.~~

5 Should the applicant intend to overcome the above objections by deleting feature (i) from claim 1, then the subject-matter of claim 1 is not new within the meaning of Article 54(3) EPC for the following reasons:

D4 discloses (figure 11) a memory device comprising: a channel (112) formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; and a gate (1502) having multiple surfaces abutting the channel, the gate comprising: a tunnel oxide layer (116) overlaying the channel (112); and a multi-layer charge storing layer including

Sandisk Technologies, Inc. - Ex. 1002, Page 000525

a first oxynitride layer (1519) closer to the tunnel oxide layer and a second oxynitride layer (1518), wherein the first oxynitride layer is separated from the second oxynitride layer by an anti-tunnelling layer (1521) comprising an oxide, and wherein the first oxynitride layer is a substantially trap-free, oxygen-rich, oxynitride layer and the second oxynitride layer is a trap dense, oxygen-lean, oxynitride layer ~~which further comprises a concentration of carbon selected to increase the number of traps therein.~~

6 At least some of the objections raised above are such that there appears to be no possibility of overcoming them by amendment. Refusal of the application under Article 97(2) EPC is therefore to be expected.

Sandisk Technologies, Inc. - Ex. 1002, Page 000526

Europäisches Patentamt
European Patent Office
Office européen des brevets

European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?
Contact Customer Services at www.epo.org/contact

Cooper, John
Murgitroyd & Company
Scotland House
165-169 Scotland Street
Glasgow G5 8PL
ROYAUME UNI

Date
20.10.15

Reference	Application No./Patent No.
P168307.EP.01/J	13767422.2 - 1552 / 2831917 PCT/US2013032339
Applicant/Proprietor	
Cypress Semiconductor Corporation	

Communication pursuant to Rules 70(2) and 70a(2) EPC

A supplementary European search report has been drawn up concerning the above-identified European patent application (publication number: 2831917).

Since the request for examination has been filed (R. 70(1), 159(1)(f), Art. 94(1) EPC) prior to the transmission of the supplementary European search report, you are hereby invited to indicate within

six months

of notification of this communication whether you wish to proceed further with the European patent application.

If you do not indicate in due time that you wish to proceed further with the European patent application, it **will be deemed to be withdrawn** (R. 70(3) EPC).

You are invited, within the above-mentioned six-month period, to comment on the objections raised in the opinion accompanying the European search report and/or to file any amendments to the description, claims and drawings correcting any deficiencies noted in the opinion (R. 70a(2), R. 137(2) EPC; Guidelines for Examination in the EPO, B-XI, 8).

If filing amendments, you must identify them and indicate the basis for them in the application as filed. Failure to meet either requirement may lead to a communication from the Examining Division requesting that you correct this deficiency (R. 137(4) EPC).

Should the reply to the invitation pursuant to Rule 70a(2) EPC be filed in an admissible non-EPO language, a translation is to be submitted within one month of its filing (R. 6(2) EPC).

Should you not comply with this invitation within the time limit, the application **will be deemed to be withdrawn** in accordance with Rule 70a(3) EPC.

Receiving Section

Europäisches Patentamt • European Patent Office • Office européen des brevets

Registered letter
EPO Form 1224 11.12 (RTB/ESOP01+N) DMEX

Europäisches Patentamt
European Patent Office
Office européen des brevets

SUPPLEMENTARY EUROPEAN SEARCH REPORT

Application Number
EP 13 76 7422

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X,P	US 8 222 688 B1 (JENNE FREDRICK [US] ET AL) 17 July 2012 (2012-07-17) * column 3, line 38 - column 7, line 37; figures 6-10 * -----	1-3	INV. H01L29/792 H01L29/423 H01L29/51 H01L27/115
X Y	US 2011/248332 A1 (LEVY SAGY [IL] ET AL) 13 October 2011 (2011-10-13) * paragraphs [0025] - [0048]; figures 2,3,5 * -----	1-3,7,8 4-6	H01L21/28 H01L29/66 B82Y10/00
Y	US 2008/054346 A1 (SAITOH MASUMI [JP] ET AL) 6 March 2008 (2008-03-06) * paragraphs [0048] - [0054]; figures 1-3 * -----	4-6	
E	WO 2013/148112 A1 (CYPRESS SEMICONDUCTOR CORP [US]; JENNE FREDRICK [US]; RAMKUMAR KRISHNA) 3 October 2013 (2013-10-03) * the whole document * -----	1,4-7	

TECHNICAL FIELDS SEARCHED (IPC)

H01L

The supplementary search report has been based on the last set of claims valid and available at the start of the search.

Place of search	Date of completion of the search	Examiner
Munich	28 September 2015	Ley, Marc

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C04)

Sandisk Technologies, Inc. - Ex. 1002, Page 000528

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 13 76 7422

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

28-09-2015

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 8222688 B1	17-07-2012	US 8222688 B1	17-07-2012
		US 8710579 B1	29-04-2014
		US 2014374813 A1	25-12-2014
US 2011248332 A1	13-10-2011	US 2011248332 A1	13-10-2011
		US 2014284696 A1	25-09-2014
US 2008054346 A1	06-03-2008	CN 101136439 A	05-03-2008
		JP 4282699 B2	24-06-2009
		JP 2008060440 A	13-03-2008
		KR 20080020962 A	06-03-2008
		US 2008054346 A1	06-03-2008
WO 2013148112 A1	03-10-2013	CN 104254921 A	31-12-2014
		EP 2831916 A1	04-02-2015
		JP 2015517211 A	18-06-2015
		KR 20140147083 A	29-12-2014
		TW 201349505 A	01-12-2013
		WO 2013148112 A1	03-10-2013

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

The examination is being carried out on the **following application documents**

Description, Pages

1-34 as published

Claims, Numbers

1-8 filed with entry into the regional phase before the EPO

Drawings, Sheets

1/12-12/12 as published

Reference is made to the following documents; the numbering will be adhered to in the rest of the procedure.

D1 US 8 222 688 B1 (JENNE FREDRICK [US] ET AL) 17 July 2012 (2012-07-17)

D2 US 2011/248332 A1 (LEVY SAGY [IL] ET AL) 13 October 2011 (2011-10-13)

D3 US 2008/054346 A1 (SAITOH MASUMI [JP] ET AL) 6 March 2008 (2008-03-06)

1 The application does not meet the requirements of Article 84 EPC, because claims 1 - 8 are not clear.

1.1 The terms "substantially trap free" and "trap dense" used in claim 1 are vague and unclear and leave the reader in doubt as to the meaning of the technical features to which they refer, thereby rendering the definition of the subject-matter of claim 1 and all dependent claims unclear (Article 84 EPC). From the wording of claim 1, it remains unclear for the skilled reader which are the ranges of trap concentrations to be defined by the above terms. It should be noted that a layer, and in particular a charge storing layer, is never 100 % free of traps.

As the description itself does not provide any clarifications, it is understood that, according to claim 1, the trap concentration in the first oxynitride layer is lower than the trap concentration in the second oxynitride layer.

Sandisk Technologies, Inc. - Ex. 1002, Page 000530

1.2 The term "recrystallized polysilicon" used in claim 3 is vague and unclear and leaves the reader in doubt as to the meaning of the technical feature to which it refers, thereby rendering the definition of the subject-matter of said claim unclear (Article 84 EPC). A skilled man is not able to the decide if the crystalline channel of of finished device according to claim 3 results or not from recrystallisation of polysilicon. Claim 3 is therefore read as requiring that the channel comprises crystalline silicon.

2 The present application claims the priority date of 31-03-2012 from US patent application US 13/436872 (published on 11-07-2013 as US 2013/0175504 A1). US 13/436872 is is a continuation-in-part of US application 11/811958 filed on 13-06-2007 and published as US 2009/0179253 A1 on 16-07-2009.

The present application does not meet the requirements of Article 52(1) EPC because the subject-matter of claims 1- 3 is not new within the meaning of Article 54(1) and (2) EPC for the following reasons:

D1 discloses a memory device (figure 6) comprising:
a channel (112) formed from a semiconducting material overlying a surface on a substrate (108) connecting a source and a drain (110) of the memory device;
a tunnel oxide layer (116) overlying the channel; and
a multi-layer charge storing layer including an oxygen-rich, first oxynitride layer (819) on the tunnel oxide layer (116) in which a stoichiometric composition of the first oxynitride layer (819) results in it being substantially trap free, and an oxygen-lean, second oxynitride layer (818) on the first oxynitride layer (819) in which a stoichiometric composition of the second oxynitride layer (819) results in it being trap dense, figure 7.

In D1, the channel comprises polysilicon, see col. 4, line 64 or the channel comprises recrystallized polysilicon, i.e. crystalline silicon, see col. 5, lines 47 - 55.

D1 discloses the subject matter of present claims 1 - 3 and has the same applicant than the present application. Therefore, document US 13/436872 cannot be considered as "first application" in the sense of Article 87 EPC for said subject matter.

It follows that for the subject matter of claims 1 - 3, the priority date of 31-03-2012 is not validly claimed and the effective filing date for this subject matter is 15-03-2013.

A consequence is that for the subject matter of claims 1 - 3 document D1 (published on 17-07-2012) is prior art in the sense of Art. 54(2) EPC.

Sandisk Technologies, Inc. - Ex. 1002, Page 000531

In other words, the present application does not meet the requirements of Article 52(1) EPC, because the subject-matter of claims 1 - 3 is not new within the meaning of Article 54(1) and (2) EPC.

3 The present application does not meet the requirements of Article 52(1) EPC because the subject-matter of claims 1 and 8 is not new within the meaning of Article 54(1) and (2) EPC for the following reasons:

3.1 Document D2 discloses a memory device (figure 2) comprising:
a channel (212) formed from a semiconducting material overlying a surface on a substrate (208) connecting a source and a drain (210) of the memory device;
a tunnel oxide layer (216) overlying the channel (212); and
a multi-layer charge storing layer including an oxygen-rich, first oxynitride layer (220B) on the tunnel oxide layer (216) in which a stoichiometric composition of the first oxynitride layer (220B) results in it being substantially trap free ([0044], figure 5), and an oxygen-lean, second oxynitride layer (220A) on the first oxynitride layer (220B) in which a stoichiometric composition of the second oxynitride layer (220A) results in it being trap dense ([0045], figure 5).

In D2, the second oxynitride layer (220A) further comprises a concentration of carbon selected to increase a number of traps therein, see [0031], claims 5, 10 and 22. A carbon concentration of from 5% to 15% is disclosed in [0031].

Hence, the subject-matter of claims 1 and 8 is not new within the meaning of Article 54(1) and (2) EPC

4 The present application does not meet the requirements of Article 52(1) EPC because the subject-matter of claims 2 - 7 does not involve an inventive step within the meaning of Article 56 EPC for the following reasons:

claims 2 and 3: polysilicon or recrystallized polysilicon is a well-known suitable channel material the skilled person would consider for the device of D2.

claims 4 - 6: The device of D2 comprises a blocking layer 218 and a metal gate 214. Claims 4 - 6 differ from D2 in that the memory device comprises a nonplanar transistor including a gate having multiple surfaces abutting the channel, i.e. in that the channel comprises a nano-wire. The so called FinFET configuration is however well known in the field of non-volatile memories, see document D3 (figure 1, channel 105, tunnel insulator 120, charge storing layer 122, blocking layer 124, control gate 130). The skilled person would select this type of transistor depending on the circumstances.

claim 7: The use of high-k materials is obvious.

5 At least some of the objections raised above are such that there appears to be no possibility of overcoming them by amendment. Refusal of the application under Article 97(2) EPC is therefore to be expected.

Sandisk Technologies, Inc. - Ex. 1002, Page 000532

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 16820P568PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 08/06627	International filing date *(day/month/year)* 23 May 2008 (23.05.2008)	(Earliest) Priority Date *(day/month/year)* 25 May 2007 (25.05.2007)
Applicant CYPRESS SEMICONDUCTOR CORPORATION		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 2

☐ as suggested by the applicant.

☒ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (April 2007)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 08/06627

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/336 (2008.04)
USPC - 438/261
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
438/261; 19 August 2008 (19.08.2008)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
438/475, 474, 257, 258, 680, 905, 910, 954, 261; 19 August 2008 (19.08.2008)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST(USPT,PGPB,EPAB,JPAB); DialogPRO(Engineering); Google Scholar
Search Terms: SONOS, radical oxidation, 1:1 ratio, oxygen and hydrogen ratio and 1:1, CVD, angstroms, nanometers, thickness, charge trapping, blocking layer, OH, O, chamber. 19 August 2008 (19.08.2008)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2005/0266637 A1 (Wang) 01 December 2005 (01.12.2005), entire document especially para. [0007], [0018], [0019], [[0020], [0021], [0027], [0029].	1-4, 6, 8-11, 13, 15-20 --- 5, 7, 12, 14
Y	US 7,033,957 B1 (Shiraiwa et al.) 25 April 2006 (26.04.2006), entire document especially col. 9, ln 1-5; col. 16, ln 55-60.	5, 12
Y	US 6,835,621 B2 (Yoo et al.) 28 December 2004 (28.12.2004), entire document especially col. 4, ln 40-45	7, 14
A	US 7,112,486 B2 (Cho et al.) 26 September 2006 (26.09.2006), entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 August 2008 (19.08.2008)	26 AUG 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PM07002CIP1WO	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 12/21583	International filing date *(day/month/year)* 17 January 2012 (17.01.2012)	(Earliest) Priority Date *(day/month/year)* 14 January 2011 (14.01.2011)
Applicant CYPRESS SEMICONDUCTOR CORPORATION		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 2
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 12/21583

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/792; H01L 21/336 (2012.01)
USPC - 257/324; 257/E21.209; 257/E29.309; 438/257
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC – 257/324; 257/E21.209; 257/E29.309; 438/257

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC -- 257/324; 257/E21.209; 257/E29.309; 438/257 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST (USPT, PGPB, JPAB,EPAB): Google
Search Terms Used: silicon oxide nitride oxide, oxynitride, source, drain, tunnel oxide, spaced apart, dichlorosilane, substrate, ammonia, oxygen, hydrogen

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2009/0179253 A1 (Levy et al.) 16 July 2009 (16.07.2009), entire document especially Abstract, para [0018], [0027], [0036], [0021], [0023], [0024]-[0026], [0034], [0025]-[0026]	1-20, 22 ---------- 21, 23
Y	US 6,153,543 A (Chesire et al.) 28 November 2000 (28.11.2000), entire document especially Abstract; col 5, ln 5-40	21, 23

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 April 2012 (24.04.2012)	08 MAY 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PM07002CIP2W	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2013/032339	International filing date *(day/month/year)* 15 March 2013	(Earliest) Priority Date *(day/month/year)* 31 March 2012
Applicant CYPRESS SEMICONDUCTOR CORPORATION		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 9 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 2

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/032339

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/792 (2013.01)
USPC - 257/411
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/336, 29/792 (2013.01)
USPC - 257/324, 406, 411, E21.423, E29.309; 438/287, 763

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
CPC - H01L 29/792; 29/7926 (2013.01)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Orbit, Google Patent, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 8,063,434 B1 (POLISHCHUK et al) 22 November 2011 (22.11.2011) entire document	1, 8 -- 2-7, 9-20
Y	US 2008/0048237 A1 (IWATA) 28 February 2008 (28.02.2008) entire document	2, 3
Y	US 2005/0275010 A1 (CHEN et al) 15 December 2005 (15.12.2005) entire document	4-7, 9-14
Y	US 6,709,928 B1 (JENNE et al) 23 March 2004 (23.03.2004) entire document	9-14, 17, 19
Y	US 2008/0293255 A1 (RAMKUMAR) 27 November 2008 (27.11.2008) entire document	13
Y	WO 2011/162725 A1 (SINGH et al) 29 December 2011 (29.12.2011) entire document	15-20
A	US 8,067,284 B1 (LEVY) 29 November 2011 (29.11.2011) entire document	1-20
A	US 2009/0179253 A1 (LEVY et al) 16 July 2009 (16.07.2009) entire document	1-20
P,A	US 8,222,688 B1 (JENNE et al) 17 July 2012 (17.07.2012) entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 May 2013	30 MAY 2013
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PM07024CIPWO	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US13/48876	International filing date (*day/month/year*) 01 July 2013 (01.07.2013)	(Earliest) Priority Date (*day/month/year*) 01 July 2012 (01.07.2012)
Applicant CYRPRESS SIMICONDUCTOR CORPORATION		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 5 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the Report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 Rule 43.6 *bis(a)*
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 5
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT	International application No. PCT/US13/48876

Box No. I Nucleotide and/or amino acid sequence(s) (Continuation of item 1.c of the first sheet)

1. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international search was carried out on the basis of:

a. type of material

☐ a sequence listing

☐ table(s) related to the sequence listing

b. format of material

☐ on paper

☐ in electronic form

c. time of filing/furnishing

☐ contained in the international application as filed

☐ filed together with the international application in electronic form

☐ furnished subsequently to this Authority for the purposes of search

2. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

3. Additional comments:

INTERNATIONAL SEARCH REPORT	International application No. PCT/US13/48876

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT	International application No. PCT/US13/48876

Box IV TEXT OF THE ABSTRACT (Continuation of Item 5 of the first sheet)

NEW ABSTRACT

Sandisk Technologies, Inc. - Ex. 1002, Page 000542

INTERNATIONAL SEARCH REPORT	International application No. PCT/US13/48876

A. CLASSIFICATION OF SUBJECT MATTER

IPC: **H01L 21/316**(2006.01),**21/336**(2006.01),**21/318**(2006.01)

USPC: 438/269,762;257/E21.285,E21.292,E21.410,E321.423

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/269, 762; 257/E21.285, E21.292, E21.410, E321.423

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 8,283,261 B2 (RAMKUMAR) 09 October 2012 (09.10.2012).	1-20
A	US 8,318,608 B2 (RAMKUMAR et al.) 27 November 2012 (27.11.2012).	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 July 2013 (19.07.2013)	26 JUL 2013
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Brian Sircus Telephone No. 571-272-2058

Form PCT/ISA/210 (second sheet) (April 2007)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PM727D1CIPWO	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US13/48885	International filing date *(day/month/year)* 01 July 2013 (01.07.2013)	(Earliest) Priority Date *(day/month/year)* 01 July 2012 (01.07.2012)
Applicant Cypress Semiconductor Corporation		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 9 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☐ the text is approved as submitted by the applicant.

☒ the text has been established by this Authority to read as follows:

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 3

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US13/48885

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/792 (2013.01)
USPC - 438/591; 257/324, E29.308
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 29/792 (2013.01)
USPC - 438/920, 591; 257/321, 324, 325, E29.308, E29.309

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); Google Patents; Google Scholar; IP.COM, IEEE Xplore; Search Terms Used: non volatile memory, memory, NVM, charge trapping layers, SONOS, silicon oxynitride, tunneling layer, anti-tunneling layer, high K dielectric, thin film, nanowire*, FinFET, metal gate, nitrated oxide, capping, blocking, trench, channel, opening, vertical, ONO logic, MOS, HV MOS.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/0248332 A1 (LEVY S et al.) October 13, 2011, Figure 2, paragraphs [0022], [0025], [0045].	1 - 20
Y	US 7,999,295 B2 (LAI E et al.) August 16, 2011, column 3, lines 29 – 39, column 3, line 60 to column 4, line 4.	1-17, 20
Y	US 7,723,789 B2 (LIN H et al.) May 25, 2010, Figures 1A – 1H, column 2, line 63 to column 3, line 45.	2-5, 12-15, 18-20
Y	US 2008/0293207 A1 (KOUTNY JR W et al.) November 27, 2008, Abstract, Figures 3A, 3B, paragraphs [0050] – [0053].	6-9, 17, 19
Y	US 2009/0039414 A1 (LUE H et al.) February 12, 2009, Abstract.	4, 5, 13, 14, 16

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 October 2013 (21.10.2013)	14 NOV 2013
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability

Hang-Ting Lue, Szu-Yu Wang*, Erh-Kun Lai, Yen-Hao Shih, Sheng-Chih Lai, Ling-Wu Yang*, Kuang-Chao Chen*, Joseph Ku*, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu

Emerging Central Lab, *Technology Development Center, Macronix International Co. Ltd.
16, Li-Hsin Road, Hsinchu Science Park, Hsinchu 300, Taiwan
E-mail: htlue@mxic.com.tw

Abstract

A bandgap engineered SONOS with greatly improved reliability properties is proposed. This concept is demonstrated by a multi-layer structure of O1/N1/O2/N2/O3, where the ultra-thin "O1/N1/O2" serves as a non-trapping tunneling dielectric, N2 the high-trapping-rate charge storage layer, and O3 the blocking oxide. The ultra-thin "O1/N1/O2" provides a "modulated tunneling barrier" -- it suppresses direct tunneling at low electric field during retention, while it allows efficient hole tunneling erase at high electric field due to the band offset. Therefore, this BE-SONOS offers fast hole tunneling erase, while it is immune to the retention problem of the conventional SONOS. With a N^+-poly gate, we achieve self-convergent erased Vt ~3 V, suitable for NOR Flash application. On the other hand, by using a P^+-poly gate, a depletion mode device (Vt < 0) is obtained, and a very large memory window (> 6 V) is achieved, ideal for MLC- NAND application. Excellent performance and reliability for both applications are demonstrated. Furthermore, with this simple structure and no new materials BE-SONOS is readily manufacturable.

I. Introduction

Floating gate devices are rapidly approaching serious scaling challenges due to inter-floating gate coupling, while nitride-trapping device is free from such limitations. Nitride-trapping device consists of two main types: SONOS [1] which uses channel program/erase, and NROM [2] which store charges locally. SONOS suffers from retention problems due to direct tunneling leakage through the thin tunnel oxide, and NROM is sensitive to hot-hole induced damages [3, 4]. There has been several proposals that promise the further scaling of NROM [5, 6], however, new solutions that do not invoke hot holes are still desirable.

A multi-layer SONOS with stacked thin nitride films (<4 nm) has been previously reported [7]. The purpose was to introduce a double trapping layer in order to increase the trapping efficiency. However, this device suffers from slow programming speed (>100 msec) and small memory window (< 2 V).

Contrary to the previous work [7], we found that ultra-thin nitride (<2 nm) has negligible charge trapping. Therefore, we propose a bandgap engineered ONO tunneling dielectric to replace the traditional tunnel oxide in SONOS.

An analogy is the concept of "crested barrier" [8], which was previously proposed to modulate the electron tunneling current for floating gate devices. However, such concept often requires high-*k* gate dielectric [9] and so far no practical application is successful. On the other hand, our proposed ONO tunneling dielectric serves as an efficient hole tunneling barrier for SONOS, and it is much more reliable and practical.

In this work, we have designed BE-SONOS devices using N^+ and P^+ poly gates that are suitable for NOR and NAND Flash applications (illustrated in Table 1), respectively.

II. Principle of the BE-SONOS – ONO tunneling dielectric

The structure and parameters of n-channel BE-SONOS are illustrated in Fig. 1 and Table 2, respectively. The "O1/N1/O2" tunneling dielectric consists of ultra-thin (<2 nm) oxide and nitride that modulates the hole tunneling current. The thicker (7 nm) N2 serves as the charge-trapping layer and O3 (9 nm) serves as the blocking oxide. O3 is grown by thermal conversion of N2 so that efficient interfacial traps between N2/O3 are provided [10].

The properties of ultra-thin O1/N1/O2 tunneling dielectric are characterized by both MOSFET and capacitors. The MOSFET with ultra-thin O1/N1/O2 gate dielectric shows negligible charge trapping regardless of the injection mode: CHE, +FN and –FN (Fig. 2). Constant current stressing (CCS) of the capacitor (Fig. 3) indicates excellent stress tolerance. The poor trapping efficiency may be due to that the capture mean free path is much longer than the ultra-thin nitride thickness. In addition, no interfacial traps between O1/N1 and N1/O2 are introduced during processing.

Since the ultra-thin ONO layer has negligible charge trapping, it is suitable for tunneling dielectric. The principal merit comes from the low hole-tunneling barrier (~1.9 eV) of SiN compared to that of oxide (~4.5 eV). The band diagrams of the ONO tunneling dielectric (O1/N1/O2=15/20/18 Å) are shown in Figs. 4 and 5. Under low electrical field during retention (Fig. 4), hole direct tunneling cannot happen because the total thickness of O1/N1/O2 is large. On the other hand, band offset happens under high electric field (Fig. 5) and the hole barriers of N1 and O2 are below the valence band. Thus a large hole tunneling current through O1 occurs under –FN bias. This is clearly shown by WKB simulation of the hole tunneling current in Fig. 6, where a high ON-OFF ratio of tunneling currents is achieved.

0-7803-9269-8/05/$20.00 (c) 2005 IEEE

Sandisk Technologies, Inc. - Ex. 1002, Page 000546

The experimental hole tunneling current can be extracted by differentiation of the erase characteristic in Fig. 7 using the transient analysis method [10]. The experimental hole currents are well matched with the simulation.

III. NOR Application Using N^+-Poly Gate

For NOR applications, the device is programmed by CHE method. Since electrons are locally trapped near the junction, the reverse read method [2] can be employed for 2-bit/cell memory operation. Contrary to NROM for which hot-hole is used for erase, the erase operation is performed by uniform hole tunneling to compensate the electrons. During $-V_G$ erase, both electron injection from N^+-poly gate and hole injection from substrate happen simultaneously, leading to a dynamic balancing condition [5, 6], (Fig. 7). Figure 8 shows that the self-convergent V_T is controlled by the erase voltage. As expected, a higher gate voltage results in a higher saturation V_T because gate injection is stronger. This self-convergent erase is very desirable for NOR Flash because the over-erase problem is avoided.

Figure 9 illustrates the excellent P/E cycling endurance. Contrary to NROM, there is no hard-to-erase [5, 6] even after dumb-mode 10K cycles (without any P/E verify and stepping algorithm), since channel hole-tunneling erase is a uniform erase thus electrons cannot pile up at the channel center region. Figure 10 shows that the *I-V* curves have very slight degradation after 10K P/E cycles. Subthreshold swing stays mostly the same, indicating small interface trap generation. In addition, charge pumping measurement (Fig. 11) also shows no excess hole traps after P/E cycles because excess hole traps are compensated by the gate injected electrons. High-temperature (150 ^{0}C) baking (Fig. 12) shows excellent electron retention for this BE-SONOS device.

Apart from the FN annealing effect [5, 6], the superb reliability performance is also due to that hole tunneling erase causes much less damage than hot-hole erase used in NROM.

IV. NAND Application Using P^+-Poly Gate

For NAND application, depletion mode device ($V_T < 0$) for the erased state is desired. By using a P^+-poly gate, the gate injection is reduced [6] and the device can be erased into depletion mode ($V_T < 0$), as shown in Fig. 13.

Figure 13 shows that the erase speed is increased when applying a higher gate voltage. However, erase saturation may happen because gate injection is stronger at higher gate voltage. Figure 14 shows the +FN programming speed, where more than 7 V memory window can be achieved within 10 msec.

Excellent cycling endurance is shown in Fig. 15; only very small degradation is observed. V_G accelerated retention test (Fig. 16) shows that the direct tunneling at low electric field (<4 MV/cm) is completely suppressed. As a result, more than 6 V memory window is preserved even after 500 hours of 150 ^{0}C baking (Fig. 17). The large memory window (>6 V) and the excellent retention are the best reported results so far for NROM and SONOS-type devices.

The erase characteristics of BE-SONOS can be controlled by the thickness of ONO tunneling dielectric (Fig. 18) and gate material engineering (Fig. 19). Figure 18 shows that the erase speed is mainly dominant by O1 because the band offset as shown in Fig. 5 effectively screens out the barrier of N1 and O2. Figure 19 shows that the gate injection of a high work function Platinum (Pt) gate can almost be completely suppressed so that erase saturation does not happen. Figure 20 shows the retention of various P/E cycled conditions. The cycling induced charge loss is very small, indicating a small P/E induced damage. Furthermore, the retention of the short-loop capacitors (up to metal 1) are consistent with the full-run MOSFET (up to metal 3). The device dimension and back-end metal processes have little impact on the retention of BE-SONOS.

V. Summary

BE-SONOS with bandgap engineered tunneling dielectric is proposed. This new device is free from the direct tunneling leakage of conventional SONOS, and hot-hole induced damages of NROM devices. Excellent reliability and performance are demonstrated. BE-SONOS may be used for both NOR and NAND applications and is readily manufacturable. Without the floating gate coupling interference problem, BE-SONOS is a promising candidate for the next-generation Flash memories.

References

[1] M. White, "On the go with SONOS", *IEEE Circuits and Designs*, pp.22-31, 2000.

[2] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A novel localized Trapping, 2-Bit Nonvolatile Memory Cell", *IEEE Electron Device Letters*, pp. 543-545, 2000.

[3] W. J. Tsai, N. K. Zous, C. J. Liu, C. C. Liu, C. H. Chen, T. Wang, S. Pang and C. Y. Lu, "Data retention of SONOS-type two-bit storage flash memory cell", *Tech. Digest of International Electron Devices Meeting (IEDM)*, pp. 719-722, 2001.

[4] M. Janai, "Data retention, endurance and acceleration factors for NROM devices", *Proceeding of the International Reliability Physics Symposium (IRPS)*, pp. 502-505, 2003.

[5] Y. H. Shih, H. T. Lue, K. Y. Hsieh, R. Liu, and C. Y. Lu, "A novel 2-bit/cell nitride storage flash memory with greater than 1M P/E-cycle endurance", *Technical Digest 2004 IEDM*, session 36-3, pp. 881-884, 2004.

[6] H. T. Lue, Y. H. Shih, K. Y. Hsieh, R. Liu, and C. Y. Lu, "Novel soft erase and re-fill methods for a P+-poly gate nitride-trapping non-volatile memory device with excellent endurance and retention properties", *Proceedings 2005 International Reliability Physics Symposium (IRPS)*, session 2D-3, pp. 168-174, 2005.

[7] S. K. Sung, Y. K. Lee, J. S. Sim, J. D. Lee, S. K. Kim, S. T. Kang, J. U. Han, and B. G. Park, "Multi-layer SONOS with direct tunnel oxide for high-speed and long retention time ", *IEEE Silicon Nanoelectronics Workshop*, pp. 83-84, 2002.

[8] K. K. Likharev, "Layered tunnel barriers for non-volatile memory", *Applied Physic Letters*, pp. 2137-2139, 1998.

[9] B. Govoreanu, P.Blomme, M. Rosmeulen, J. V. Houdt, and K. D. Meyer, "VARIOT: a novel multilayer tunnel barrier concept for low-voltage non-volatile memory devices", *IEEE Electron Device Letters*, pp. 99-101, 2003.

[10] H. T. Lue, Y. H. Shih, K. Y. Hsieh, R. Liu, and C. Y. Lu, "A Transient Analysis Method to characterize the trap vertical location in nitride trapping devices", *IEEE Electron Device Letters*, pp. 816-818, 2004.

	N^+-Poly Gate	P^+-Poly Gate
Applications	NOR-type Flash	NAND-type Flash
Self-convergent V_T	>0 V	<0 V
Programming Method	CHE	+FN
Reading Method	Reverse Read Method (2-bit/cell)	Normal Read (1-bit/cell or MLC)
Erasing Method	Hole Tunneling Erase V_G= -15 V	Hole Tunneling Erase V_G= -18 V

Table 1 Summary of the applications of BE-SONOS with N^+ and P^+-poly gate.

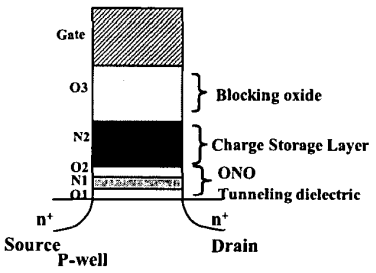


Fig. 1 Structure of the n-channel BE-SONOS using ultra-thin ONO tunneling dielectric.

Bottom Oxide (O1)	15 Å
Inter Nitride (N1)	20 Å
Inter Oxide (O2)	18 Å
Trapping Nitride (N2)	70 Å
Blocking Oxide (O3)	90 Å
Gate Material	N^+-Poly (NOR-type) P^+-Poly (NAND-type)
Channel Length	0.22 μm
Channel Width	0.16 μm

Table. 2 Typical parameters of the n-channel BE-SONOS.

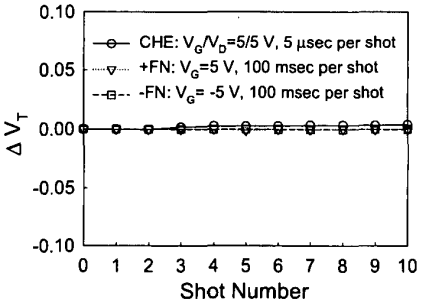


Fig. 2 The characteristics of nMOSFET with ONO tunneling dielectric O1/N1/O2=15/20/18 Å. Various injection methods including +FN, -FN and CHE all show negligible charge trapping.

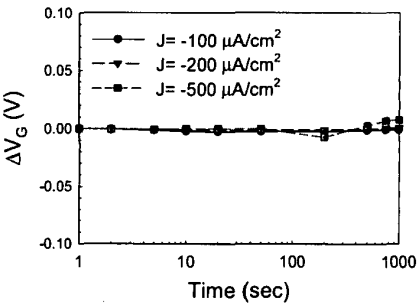


Fig. 3 Constant current stress (CCS) of the ONO tunneling dielectric (15/20/18) capacitor. Small charge trapping is observed under negative gate current stress.

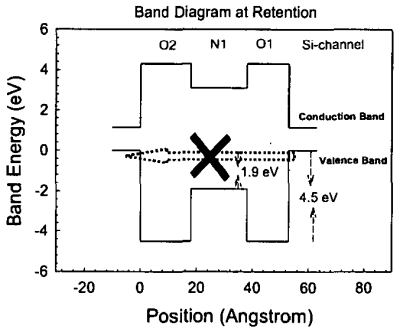


Fig. 4 Band diagram of the of O1/N1/O2 tunneling dielectric at zero electrical field. Hole direct tunneling can not happen due to the thick ONO layer. The charge loss during retention can be suppressed.

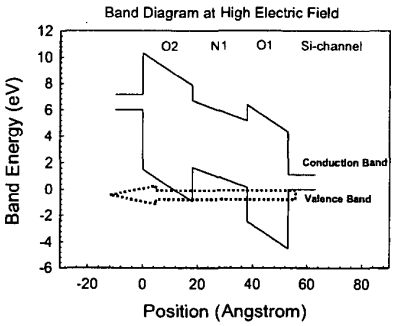


Fig. 5 Band diagram of the of O1/N1/O2 tunneling dielectric under negative gate bias. The tunnel barriers of N1 and O2 are almost screened due to the band offset such that hole direct tunneling through O1 can happen.

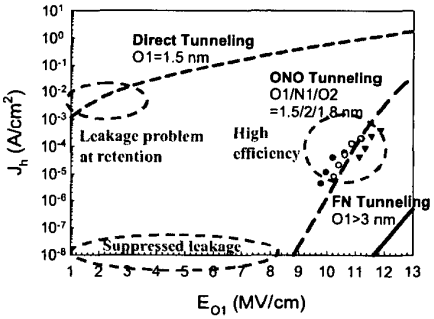


Fig. 6 The measured and simulated hole tunneling current for this device. The measured hole tunneling current (dotted symbols) are extracted by the transient analysis method [10] in Fig 7. WKB method is used to calculate the tunneling barrier in Fig. 5.

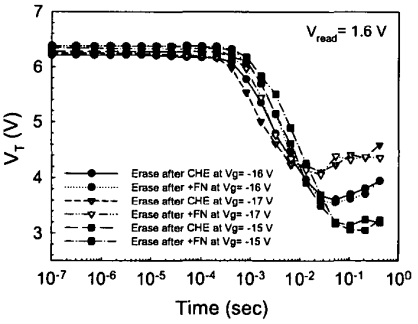


Fig. 7 Erase characteristics of the N^+-poly gate BE-SONOS at various gate voltages. The erase saturates at a positive V_T. The erase speeds for CHE and +FN programmed devices are similar.

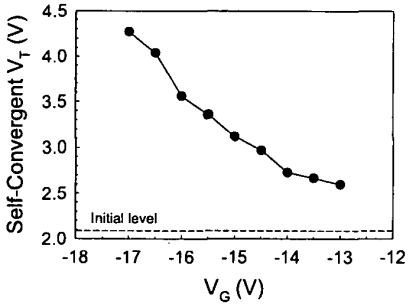


Fig. 8 Self-convergent V_T as a function of erase V_G of the N^+-poly gate BE-SONOS. A larger V_G corresponds to a larger convergent V_T because gate injection is higher.

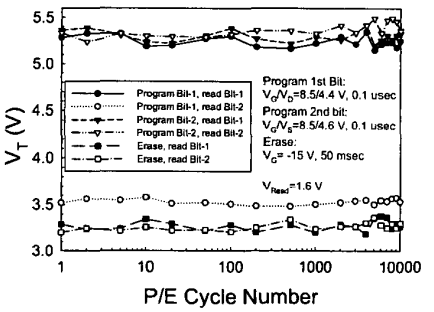


Fig. 9 P/E cycle endurance of N^+-poly gate BE-SONOS (NOR-type). Only one-shot program and one-shot erase were used without P/E verify, and the device possesses excellent endurance property.

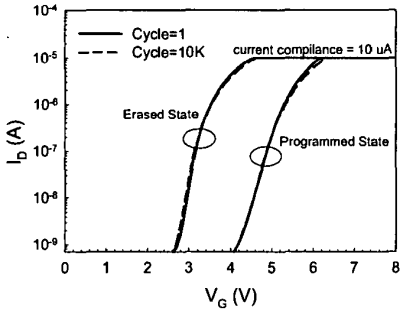


Fig. 10 *IV* curves during 10K P/E cycles in Fig. 9. It shows small degradation of sub-threshold slope and trans-conductance.

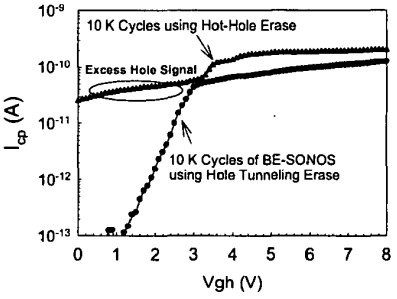


Fig. 11 Charge pumping measurement of the NOR-type operations after 10K P/E cycles. A comparison with the condition using hot-hole erase is also provided.

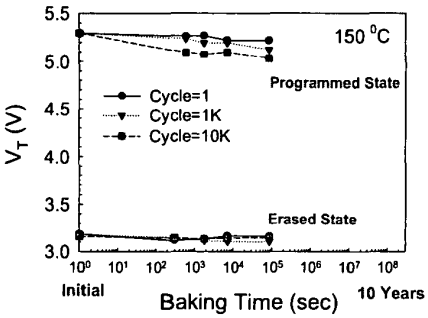


Fig. 12 High-temperature baking of the NOR-type operations at various P/E cycle condition.

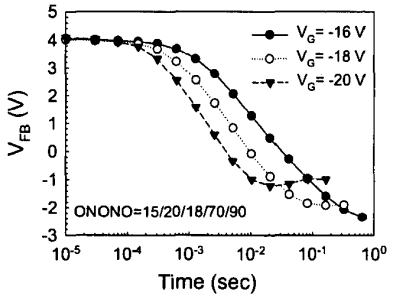


Fig. 13 Erase characteristics of the P+-poly BE-SONOS capacitors. Gate injection is suppressed and negative V_{FB} can be achieved. At larger V_G, gate injection becomes significant, resulting in erase saturation.

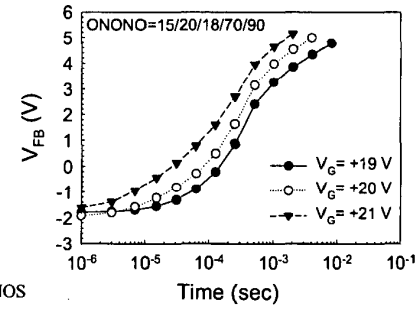


Fig. 14 +FN programming characteristics of the P+-poly gate capacitor. A large memory window (>7 V) can be obtained within 10 msec.

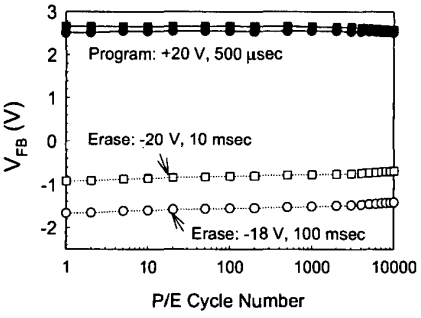


Fig. 15 P/E cycle endurance of the P+-poly gate capacitor. Only one-shot program and one-shot erase was used during P/E cycles.

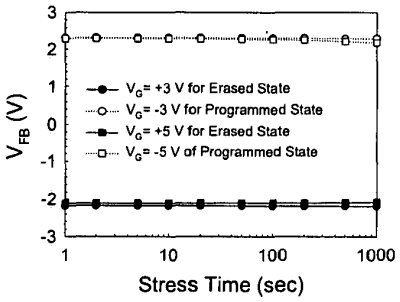


Fig. 16 V_G accelerated retention test. $-V_G$ is applied for programmed state and $+V_G$ for erased state. The small charge loss and charge gain indicate that direct tunneling are suppressed below medium field (< 4 MV/cm).

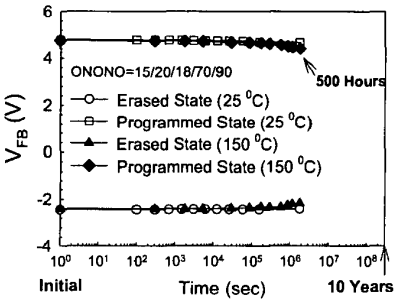


Fig. 17 Charge retention of the P+-poly gate capacitor (P/E cycle=1). The charge loss and charge gain are negligible at room temperature. More than 6.5 V memory window can be preserved even after 500 hour of 150 °C baking.

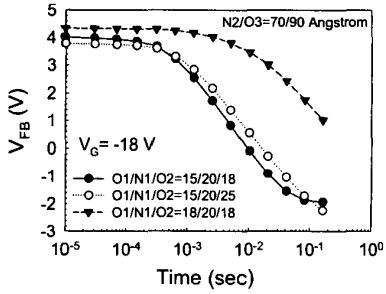


Fig. 18 Erase characteristics of various O1/N1/O2 tunneling dielectric with P+-poly gate. The erase speed is very sensitive to O1, while O2 has much smaller effect. This is because ONO tunneling is dominated by O1, while O2 is almost screened by the band offset (shown in Fig. 5).

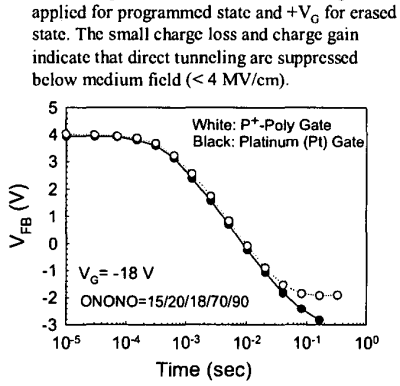


Fig. 19 Comparison of the erase characteristic of P+-poly gate and Platinum (Pt) gate capacitors. Pt has a high work function that can suppress gate injection, leading to a non-saturated erase. Pt gate was patterned by the lift-off process.

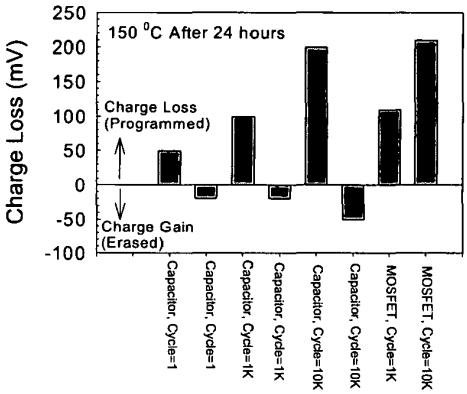


Fig. 20 Comparison of the charge loss/charge gain after 24-hour baking for various P/E cycle conditions. The programmed and erased delta V_T are +3 V and -2 V referenced to the initial state, respectively. The P/E cycle induced charge loss is small. Furthermore, the retention results of a full-run MOSFET device (Lg=0.16 μ m) with up to metal 3 processes are close to that of the short-loop capacitors with only metal 1 processes. It indicates that the retention properties of BE-SONOS is insensitive to back-end processes. It is only related to the intrinsic properties of ONONO.

Reliability Model of Bandgap Engineered SONOS (BE-SONOS)

Hang-Ting Lue, Szu-Yu Wang*, Yi-Hsuan Hsiao, Erh-Kun Lai, Ling-Wu Yang*, Tahone Yang*, Kuang-Chao Chen*, Kuang-Yeu Hsieh, Rich Liu, and Chih Yuan Lu

Emerging Central Lab, *Technology Development Center, Macronix International Co. Ltd,
16, Li-Hsin Road, Hsinchu Science Park, Hsinchu, Taiwan.
E-mail: htlue@mxic.com.tw

Abstract -

Reliability properties of bandgap engineered SONOS (BE-SONOS) [1] are extensively studied. First, the erase mechanism of BE-SONOS is confirmed as substrate hole tunneling through the ultra-thin ONO tunneling dielectric. Next, very long-term (>3,000 hours) high-temperature baking data (from 150 to 250°C) for various programmed/erased states and cycling history are collected and analyzed for a thorough understanding of the retention property. By transforming retention data (V_{FB}-time) into de-trapping current (J) and modeling its dependence on electric field and temperature, the long-term retention of various programmed states are consistently and accurately predicted. This modeling technique avoids the ambiguity of the common Arrhenius plot, and is useful for developing other predictive models too. We have shown that BE-SONOS surpasses the 10-year 85°C storage criterion for Flash memory applications.

I. Introduction

Recently, floating gate flash memories are rapidly approaching scaling limits such as the coupling ratio issues, and charge-trapping memory devices are forecasted as the solution below 45 nm node [1,2]. Although there are many varieties proposed, the major challenge is whether these new devices can pass the 10-year 85^0C storage criterion. In fact, charge-trapping devices tend to suffer memory window closure after long-term high-temperature baking and so far there is no general consensus on a predictive model. Therefore, a reliable device as well as an accurate life-time prediction model is in urgent need.

Last year, we proposed BE-SONOS [1] device for both NOR and NAND Flash applications. The structure and typical process condition of the BE-SONOS device are shown in Fig. 1 and Table 1, respectively. This new device exploits a bandgap engineered tunnel dielectric to replace the traditional thin tunnel oxide in SONOS. As shown in Fig. 2, under high electric field during erase, the hole tunneling distance is effectively reduced to the thin O1 due to the band offset. Therefore, efficient hole tunneling current is achieved. On the other hand, at low electric field during retention, charge leakage is completely blocked by the thick ONO barrier. Hence, good data retention is granted by the entire ONO barrier that prevents direct tunneling. With its simple structure and using only known materials, BE-SONOS is a very promising solution for below 45nm node. In this work, the reliability of BE-SONOS is extensively studied and an accurate retention model is developed.

II. Erase Characteristics of BE-SONOS

The *IV* characteristics of the thin ONO barrier are shown in Fig. 3. The results show that the measured hole current at high electric field is consistent with the theoretical calculation from WKB approximation. Moreover, the *IV* characteristics of ONO tunneling dielectric show no degradation after continuous current stress. This excellent stress tolerance makes the ultra-thin ONO an ideal variable-thickness tunneling barrier.

Note that the ultra-thin ONO does not need to be perfect. Even if the SiN in the thin ONO is slightly trappy, the band diagram in Fig. 2 is still valid so that the program/erase operations are not affected. On the other hand, the retention of SONOS-type devices can be excellent for a non-perfect tunnel barrier because charges are deeply trapped in nitride. Therefore, the tunnel barrier engineering in SONOS-type devices is much more feasible than that in the floating-gate devices.

In order to further clarify the erase mechanism, a refill [3] technique is applied. The refill method is a repeating sequence of partial erasing followed by reprogramming in order to alter the trap energy spectrum. The detailed procedure is illustrated in Fig. 4. For comparison, a SONOS device with a thick tunnel oxide (4.5nm) is also measured. Since the thick tunnel oxide does not allow hole tunneling and the erase speed is much slower than BE-SONOS, this SONOS device is erased through a de-trap tunneling mechanism. Figure 4 shows that the erase speed of SONOS is significantly reduced after the refill method, while BE-SONOS shows a constant erase speed. This indicates that the two devices have different erase mechanisms.

For the de-trapping tunneling mechanism, the refill method reduces the shallowly-trapped electrons [3], thus reduces the erase speed. On the other hand, BE-SONOS device uses hole tunneling for the erase, which does not depend on the electron trap energy. Hence, its erase speed is not affected by the refill method.

Therefore, the refill behavior serves as a tool to distinguish hole tunneling from electron de-trapping. Since hole-tunneling erase is independent of the electron trap energy, the erase speed of BE-SONOS is insensitive to the programming method, as shown in Fig. 5.

Figure 6 shows that the erase speed is not degraded after 10K P/E cycling, indicating very excellent endurance, consistent with Fig. 3. Figure 7 illustrates the erase speed characteristics with respect to various ONO barrier. The results clearly indicate that the erase speed for BE-SONOS is

1-4244-0439-8/06/$20.00 ©2006 IEEE

Sandisk Technologies, Inc. - Ex. 1002, Page 000550

dominated by the thin O1, while O2 and N1 thickness have very small effect. This is consistent with the bandgap engineering concept (Fig. 2), where the barriers of N1 and O2 are almost screened due to the band offset [1].

III. Long-Term High-Temperature Baking

Figure 8 shows the long-term retention of various PV and EV states at three temperatures (150, 200 and 250°C). The characteristics can be briefly summarized:

(1) The programmed states (excess electron) do not show any significant charge loss until a particular life time, and the life time decreases as temperature increases.
(2) The erased states (excess hole) do not show significant charge gain even after 250°C/1,000 hour baking. Moreover, the retention is insensitive to the temperature.
(3) The P/E cycled devices show only a slightly larger initial charge loss (for PV) or charge gain (for EV), but the long-term retention behavior is the same as un-cycled devices. The long-term charge loss rate is very similar.

IV. Retention Model

Arrhenius plots are often used [4] to extrapolate the device life time. In this method, life time is plotted versus 1/kT. By assuming that the slope is equal to the activation energy (E_A), life time can be extrapolated. However, this method has ambiguities in the definition of life time. Besides, Arrhenius fitting is always inconsistent for various programmed state, as shown in Fig. 9. The reason is that Arrhenius analysis does not include the effect of built-in electric field.

In this work, we model the de-trapping current (J) instead of Vt (or V_{FB}). J is obtained by differentiation of Vt with respect to time, and it is physical and has direct dependence on temperature and electric field. The detailed procedures and related equations are listed in Tables 2-4. Since excess-hole states show very small charge gain even under 250°C baking, only electron retention is considered here. For simplicity, the fresh state is considered first.

Following Table 2, the retention data (Vt-time) can be transformed into J-E at various temperatures, where E is the built-in electric field. This method is similar to the transient analysis method [5]. The extracted J-E for various programmed state and baking temperatures are shown in Fig. 10. Interestingly, the experimental curves show very similar behaviors with the Frenkel-Poole (F-P) equation. Therefore, we adopted a F-P equation to fit these data, as illustrated in Table 3. There are three parameters. E_A is the activation energy that accounts for the temperature acceleration factor. b is the factor that accounts for the electric field factor. $b=1$ for the ideal F-P equation. a is a global coefficient for F-P equation.

The major parameter of this fitting is E_A, which is extracted by fitting the distance between J-E curves of various temperatures. E_A is found to be close to 1.1 eV, as shown in Table 5. The extracted E_A indicates the major trapping energy level. Interestingly, it is consistent with the previous result using thermionic emission model [6].

In Fig. 10, J-E curves have a well-fitted $E^{1/2}$ dependence, which is consistent with the F-P equation. Finally, the extracted F-P parameters can be used to simulate the retention at various temperatures. Following Table 4, Vt can be obtained by integrating J with respect to time using iteration methods. The simulation results in Figs. 11-13 show very accurate fitting for various PV states and temperatures, using only three parameters (E_A, a and b). Based on this model, the charge loss after 10-year 85°C storage is less than 300 mV for PV= + 4 V (Fig. 14). The excellent long-term retention and the well-predicting model of BE-SONOS are the best-reported results so far for nitride storage devices.

Table 5 compares BE-SONOS devices with various ONO tunneling dielectrics; the extracted F-P parameters are very similar. This indicates that the F-P mechanism is governed by the nitride-trapping layer. We also compare the P/E stressed devices (Fig. 15), and find that the long-term charge loss rate is similar with the fresh device. This may indicate that the effect of P/E stressing can be regarded as an effective increase in shallow traps. The shallow trap generation is calculated as ~5 % (200 mV for PV=+4V), which contributes to the faster initial charge loss (Fig. 15). However, the long-term charge loss is dominated by the deeper traps, which is an intrinsic (fresh) behavior.

The retention behaviors of various electron injection techniques are shown in Fig. 16. Hot-electron (CHE for n-channel device [1] and BBHE for p-channel device [7]) programming shows larger initial charge losses, but the long-term retention behavior converges with FN programming.

V. Summary

The reliability model for BE-SONOS is developed. We have shown that BE-SONOS surpasses the 10-year 85°C storage criterion for Flash memory applications. Moreover, the present work also provides useful characterization methods for other charge-trapping non-volatile memory devices.

References:

[1] H.T. Lue, S.Y. Wang, E.K. Lai, Y.H. Shih, S.C. Lai, L.W. Yang, K.C. Chen, J. Ku, K.Y. Hsieh, R. Liu, and C.Y. Lu, "BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability", *Tech. Digest 2005 International Electron Devices Meeting*, pp. 547-550, 2005.

[2] K. Kim, "Technology for sub 50 nm node DRAM and NAND Flash Manufacturing", *Tech. Digest 2005 International Electron Devices Meeting*, pp. 539-543, 2005.

[3] H. T. Lue, Y. H. Shih, K. Y. Hsieh, R. Liu, and C. Y. Lu, "Novel soft erase and re-fill methods for a P^+-poly gate nitride-trapping non-volatile memory device with excellent endurance and retention properties", *Proceedings of the International Reliability Physics Symposium (IRPS)*, session 2D-3, pp. 168-174, 2005.

[4] S. Kumar, and E.L. Russell, "Model to predict ONO non-volatile memory", *Integrated Reliability Workshop (IRW)*, pp. 34-40, 2001.

[5] H.T. Lue, Y.H. Shih, K.Y. Hsieh, R. Liu, and C.Y. Lu, "A transient analysis method to characterize the trap vertical location in nitride-trapping devices", *IEEE Electron Device Letters*, vol. 25, pp.816-818, 2004.

[6] Y. Yang and M. White, "Charge retention of scaled SONOS non-volatile memory devices at elevated temperatures", *Solid-State Electronic*, vol. 44, pp. 949-958, 2000.

[7] H. T. Lue, S. Y. Wang, E. K. Lai, M. T. Wu, L. W. Yang, K. C. Chen, J. Ku, K. Y. Hsieh, R. Liu, and C. Y. Lu, "A Novel P-Channel NAND-Type Flash Memory with 2-Bit/Cell Operation and High Programming Throughput (>20 MB/sec)," in *IEDM Tech. Dig.*, 2005, session 13-7, pp. 331-334.

Bottom Oxide (O1)	ISSG, 15 Å
Inter Nitride (N1)	LPCVD, 20 Å
Inter Oxide (O2)	HTO, 25 Å
Trapping Nitride (N2)	LPCVD, 70 Å
Blocking Oxide (O3)	Furnace, 90 Å
Gate Material	P+-Poly

Table 1 Typical process condition of BE-SONOS.

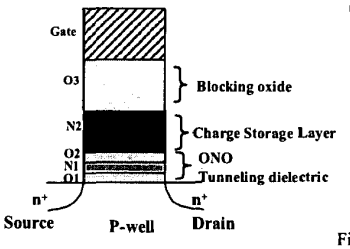


Fig. 1 Structure of the n-channel BE-SONOS using ultra-thin ONO tunneling dielectric.

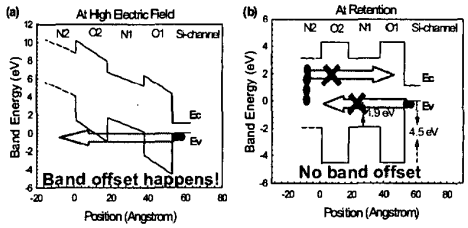


Fig. 2 Bandgap engineering concept for the BE-SONOS device. (a) At high field during erase, band offset reduces the hole tunneling barrier to merely O1. (b) At low field during retention, both electron de-trapping and hole back tunneling are prohibited by the full O1/N1/O2 barrier stack.

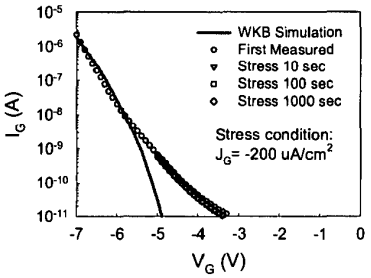


Fig. 3 I_G-V_G of ONO tunneling dielectric (O1/N1/O2=15/20/25) with P+-poly gate after constant current stressing. The solid line is the hole current simulated by WKB method.

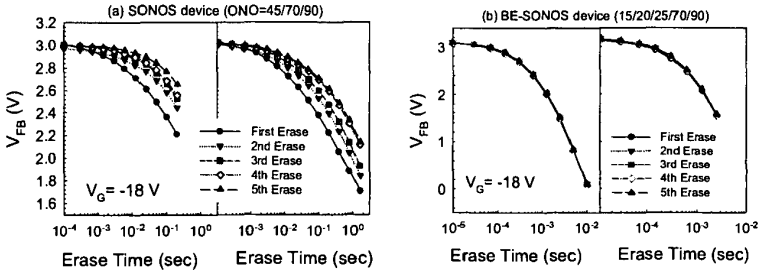


Fig. 4 Refill [3] comparison of (a) SONOS (45/70/90) (b) BE-SONOS (15/20/25/70/90) capacitors. A heavily-doped P+-poly gate is used to suppress gate injection. The device is first programmed to V_{FB}=+3V, and then erased (to a non-saturated state) with various erase times, and then re-programmed (refill) to the programmed state. This process is repeated several times to eliminate the shallowly trapped electrons. BE-SONOS device shows constant erase speed after the refill process, while the SONOS device with a thick tunnel oxide (45 Å) shows lower erase speed after the refill process.

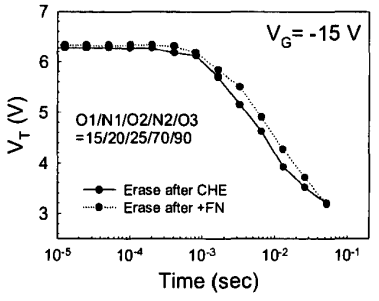


Fig. 5 The erase behavior for BE-SONOS using +FN injection and CHE injection. The device is an n-channel MOSFET with L/W=0.18/0.16 um. The erase speed is independent of the programming method.

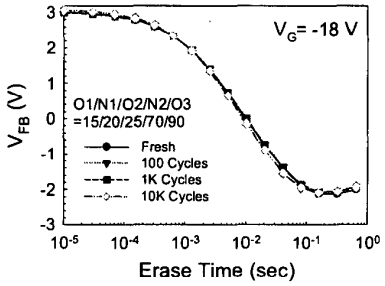


Fig. 6 The erase speed comparison after P/E cycling stress. BE-SONOS device shows very small erase speed degradation after 10K P/E cycles.

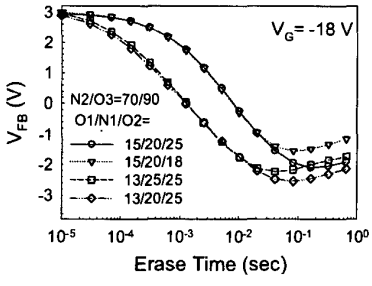


Fig. 7 Erase speed comparison for BE-SONOS with various ONO tunneling dielectrics. The erase speed is dominated by O1.

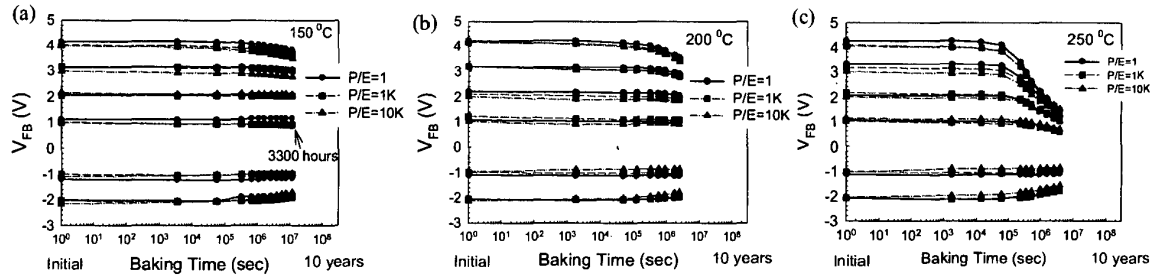


Fig. 8 Long-term retention data for BE-SONOS at (a) 150 (b) 200 (c) 250 °C. Various programmed states (up to PV= +4V) and erased states (up to EV= -2 V) with P/E cycle = 1 (fresh), 1K and 10K are tested. The testing devices are identical BE-SONOS capacitors with O1/N1/O2/N2/O3=15/20/25/70/90A.

Step 1: Plot J-E

$$J = \frac{\varepsilon_0 \cdot \varepsilon_{ox}}{T_{Tox}} \frac{dV_{FB}}{dt}$$

$$E = \frac{(V_{FB} - V_{FB,i}) \cdot \varepsilon_n}{T_{Box} \cdot \varepsilon_n + T_{Tox} \cdot \varepsilon_n + T_{SiN} \cdot \varepsilon_{ox}}$$

Table 2 The equations for obtaining the de-trapping current (J) and built-in electric field (E) from the baking retention data (V_{FB}-t). J is obtained by differentiating V_{FB} with respect to time (t). T_{BOX}, T_{TOX}, T_{SiN} are the equivalent oxide thickness of O1/N1/O2, O3, and N2, respectively. $V_{FB,i}$ is the initial uncharged V_{FB} of BE-SONOS, which is close to 0 V for P+-poly gate.

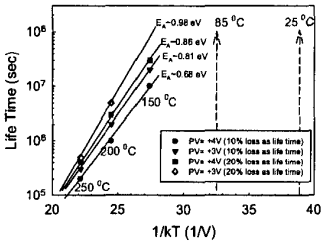


Fig. 9 Arrhenius plots for life time extrapolation. Life time is defined at 10 % or 20 % charge loss. Various definitions and PV states produce inconsistent results.

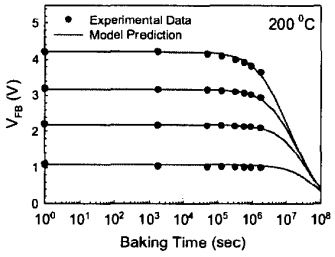


Fig. 12 Comparison of experimental and simulated retention data at 200 °C using the procedure in Table 4. The F-P parameters are identical to those in Fig. 10.

O1/N1/O2 (Å)	E_A (eV)	a (A/cm²)	b
15/20/25	1.17	5E-4	0.90
13/20/25	1.18	6E-4	0.90
15/20/18	1.15	4E-4	0.88
13/25/25	1.17	8E-4	0.87

Table 5 The extracted F-P parameter for various ONO tunneling dielectrics. The parameters are very similar, indicating that BE-SONOS retention is insensitive to ONO tunneling dielectric. The long-term retention is determined by the intrinsic nitride trap property.

Step 2: Fit J-E

$$J = a \cdot Exp\left(-\frac{E_A - b\sqrt{qE_N/\pi\varepsilon_N\varepsilon_0}}{kT/q}\right)$$

Table 3 The Fenkel-Poole equation used to fit the extracted J-E plots at various temperatures. E_A is the activation energy that accounts for the temperature (T) dependency. b is the parameter that accounts for dependency on nitride electric field (E_N), where $E_N = E \cdot \varepsilon_{ox}/\varepsilon_n$
a is the parameter of proportional constant.

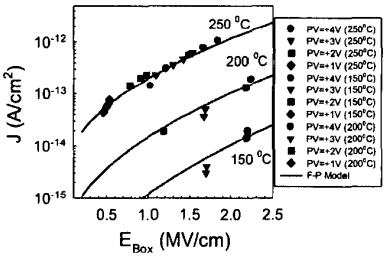


Fig. 10 The extracted de-trapping current (J) as a function of built-in electric field (E) in the bottom oxide at various temperatures and PV states. The line is the fitting results (Table 3) using Frenkel-Poole equation with E_A=1.17 eV, a= 5.1E-4 (A/cm²), b=0.9.

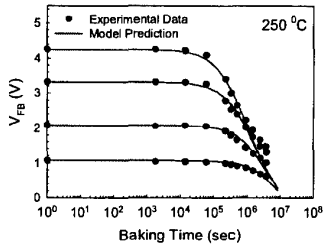


Fig. 13 Comparison of experimental and simulated retention data at 250 °C using the procedure in Table 4. The F-P parameters are identical to those in Fig. 10.

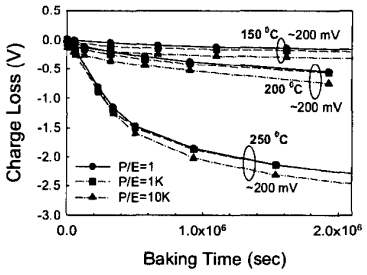


Fig. 15 Comparisons of charge loss for PV=+4V state at various temperatures. The P/E cycled devices show larger initial charge losses, but the charge loss rate converges with the fresh state, leading to a constant difference (~200 mV).

Step 3: Simulate V_{FB}-t

$$E = \frac{(V_{FB}(t) - V_{FB,i}) \cdot \varepsilon_n}{T_{Box} \cdot \varepsilon_n + T_{Tox} \cdot \varepsilon_n + T_{SiN} \cdot \varepsilon_{ox}} \quad , E_N = E \cdot \varepsilon_{ox}/\varepsilon_n$$

$$J = a \cdot Exp\left(-\frac{E_A - b\sqrt{qE_N/\pi\varepsilon_N\varepsilon_0}}{kT/q}\right)$$

$$V_{FB}(t + \Delta t) = V_{FB}(t) - J \cdot \Delta t \cdot \frac{T_{OX}}{\varepsilon_0 \cdot \varepsilon_{ox}}$$

Table 4 The retention (V_{FB}-t) simulation methods. For any given V_{FB} (t), the built-in electric field and de-trapping current (J) are calculated. V_{FB}-t at any temperature and time can be obtained by iteration.

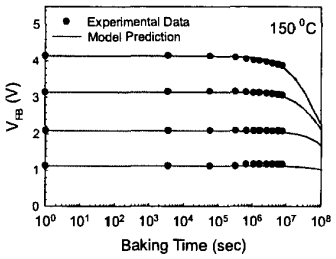


Fig. 11 Comparison of experimental and simulated retention data at 150 °C using the procedure in Table 4. The F-P parameters are identical to those in Fig. 10.

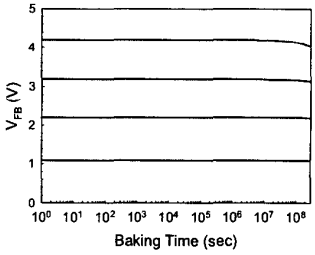


Fig. 14 Simulated retention data at 85 °C after 10 years. It shows only 300 mV charge loss for PV=+4V, and negligible charge loss for PV<=+3V.

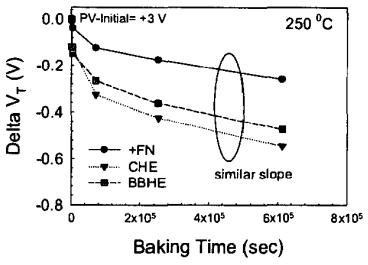


Fig. 16 The retention comparisons of +FN, CHE and BBHE (p-channel device in Ref. [7]). PV is +2V referenced to the initial state. Hot-carrier injection shows a faster initial charge loss, but the long-term charge loss slope (J) is similar to +FN programming..

Materials Science of Thin Films

Deposition and Structure

Second Edition

Milton Ohring
Department of Materials Science and Engineering
Stevens Institute of Technology
Hoboken, New Jersey



ACADEMIC PRESS
San Diego San Francisco New York Boston London Sydney Tokyo

Sandisk Technologies, Inc. - Ex. 1002, Page 000554

This book is printed on acid-free paper. ♾

Copyright © 2002 by Academic Press

All rights reserved.

No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopy, recording, or any information storage and retrieval system, without permission in writing from the publisher. Requests for permission to make copies of any part of the work should be mailed to the following address: Permissions Department, Harcourt, Inc., 6277 Sea Harbor Drive, Orlando, Florida 32887-6777.

Academic Press
A division of Harcourt, Inc.
525 B Street, Suite 1900, San Diego, CA 92101-4495, USA
http://www.academicpress.com

Academic Press
Harcourt Place, 32 Jamestown Road, London, NW1 7BY, UK
http://www.academicpress.com

Library of Congress Catalog Card Number: 2001089414
International Standard Book Number: 0-12-524975-6

Printed in the United States of America
01 02 03 04 05 06 ML 9 8 7 6 5 4 3 2 1

Sandisk Technologies, Inc. - Ex. 1002, Page 000555

6.8.3 Deposition and Structure of Amorphous Silicon Films

Amorphous silicon (a-Si) and hydrogenated versions of it, e.g., a-Si:H, are the basic materials discussed in this section. They have been deposited by both PVD and CVD techniques. Of the elements, silicon and others in column IV of the periodic table are among the easiest to prepare in amorphous form. Further, they do not require particularly low substrate temperatures (T_S) for their preparation. When normalized to the melting point (T_M), the ratio of T_S/T_M for amorphous CVD materials is higher by at least a factor of ~ 5 relative to what is required to amorphize typical PVD metal alloys. What accounts for the particular ease in amorphizing Si by CVD is the steric hindrance provided by molecular groups. Such structural obstruction leads to the high viscosity conducive to glass formation in bulk hydrocarbon polymers and oxide melts. In the case of a-Si:H films derived from SiH_4–H_2 mixtures, for example, the assorted radical and molecular fragments, e.g., SiH_3, SiH_2, Si_2H_6, are the source of the steric hindrance. A continuum of Si–H structures links the gas phase of $SiH_4 + H_2$ to the deposit surface. Contained within this transition region are assorted fragmented molecular species, which in turn connect to the film growth zone and eventually to the stable a-Si:H network beneath the film surface. Atom incorporation reactions are complex and not known with certainty (Refs. 53, 54); they resemble network polymerization of assorted Si_nH_{2n} molecular fragments and include dissociation and hydrogen desorption as well. The net result is the incorporation of as much as 35 at.% hydrogen (Ref. 55) into a silicon deposit disordered by bond stretching and distortion.

6.8.4 Amorphous Silicon Nitride

Silicon nitride is normally prepared by reacting silane with ammonia in an argon plasma, but a N_2/SiH_4 discharge can also be used. During plasma deposition, as much as 30 at.% hydrogen can be incorporated which apparently forms bonds to both Si and N. It is in this sense that silicon nitride is often described as a ternary solid-solution alloy, SiNH. Amorphous silicon nitride should be distinguished from the stoichiometric compound, Si_3N_4, formed by reacting silane and ammonia at 900°C in an atmospheric CVD reactor. It is instructive to further compare the physical and chemical property differences in three types of silicon nitride (Ref. 57), and this is done in Table 6-5. While Si_3N_4 is denser and more resistant to chemical attack and has higher resistivity and dielectric breakdown strength, SiNH tends to provide better step coverage. An upper tempera-

Sandisk Technologies, Inc. - Ex. 1002, Page 000556

Table 6-5
Physical and Chemical Properties of Silicon Nitride Films from $SiH_4 + NH_3$

Property	Si_3N_4 1 atm CVD (900°C)	Si_3N_4(H) LPCVD (750°C)	SiNH PECVD (300°C)
Density (g/cm^3)	2.8–3.1	2.9–3.1	2.5–2.8
Refractive index	2.0–2.1	2.01	2.0–2.1
Dielectric constant	6–7	6–7	6–9
Dielectric breakdown field (V/cm)	10^7	10^7	6×10^6
Bulk resistivity (Ω-cm)	10^{15}–10^{17}	10^{16}	10^{15}
Stress at 23°C (GPa)	0.7–1.2(T)	0.6(T)	0.3–1.1(C)
Color transmitted	None		Yellow
H_2O permeability	Zero		Low–none
Thermal stability	Excellent		Variable >400°C
Si/N ratio	0.75	0.75	0.8–1.0
Etch rate, 49% HF (23°C)	80 Å/min		1500–3000 Å/min
Na^+ penetration	<100 Å		<100 Å
Step coverage	Fair		Conformal

Note: T = tensile; C = compressive.
Adapted from Refs. 56 and 57.
Stress data from S. M. Hu, *J. Appl. Phys.* **70**, R60 (1991).

limit that can be tolerated in some completed integrated circuits is ~300°C because interconnection metallizations begin to react with the surrounding insulation beyond this point. Since SiHN can be deposited at such temperatures and is an effective barrier against moisture penetration, it has been used to encapsulate IC chips.

Further aspects of the structure of amorphous elemental and alloy films, including silicon nitride, will be deferred to Section 9.6.

6.8.5 Ultrahard Thin Films

In this section we discuss films based on the three hardest substances known, diamond, boron nitride, and carbon nitride, and consider their deposition, properties, and uses. In common, they are all primarily produced by CVD methods. Diamond is by far the most important of these materials and is therefore given the greatest attention.

Sandisk Technologies, Inc. - Ex. 1002, Page 000557

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

[redacted]

January 6, 2017

[redacted]

Attn.: [redacted]

[redacted]

Via Email Only

[redacted]

Re: National Phase in China of PCT/US2013/048885
In the name of Cypress Semiconductor Corporation
Title: Memory Transistor with Multiple Charge Storing Layers
CN Application No.: 2013800318408
Your Ref.: P169385.CN.01
Our Ref.: [redacted]

Deadline for Responding to this Office Action: **April 17, 2017 (Beijing Time)**
Issue Date: December 2, 2016; 4 Months Rejection

Dear Ms. Hachemi:

The State Intellectual Property Office of China recently has issued the First Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below with our recommendation and proposed amendments.

Examiner's Opinions in this OA

1. Inventiveness – Claim 1

The Examiner points out that claim 1 does not possess inventiveness over Reference 1 (US8071453B1, December 6, 2011) in view of known common knowledge, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 1 (see column 3, line 24 to column 8, line 44 of its Description and Figs. 1-10), the Examiner admits that the distinguishing technical feature of the technical scheme in claim 1 is that *the channel comprises polysilicon.*

The Examiner holds that the polycrystal is conventional channel material in the art, it cannot produce any unexpected technical effects. And thus on the basis of Reference 1 in combination of known common knowledge, the technical scheme of claim 1 is obvious to a

[redacted]

person skilled in the art.

2. Inventiveness – Claims 2-3

The Examiner points out that claims 2-3 do not possess inventiveness either. The Examiner holds that the additional technical features of claims 2-3 are conventional channel materials in the art, which cannot produce any unexpected technical effect. And thus the technical schemes of claims 2-3 do not possess inventiveness on the condition that claim 1 they refer to does not possess inventiveness.

3. Inventiveness – Claim 4

The Examiner points out that claim 4 does not possess inventiveness either. The Examiner holds that Reference 1 (see column 8, lines 11-17 of its Description) discloses that gate electrode comprises polysilicon, and the rest additional technical feature can be reasonably configured by a person skilled in the art according to needs. And thus the technical scheme of claim 4 does not possess inventiveness on the condition that claim 3 it refers to does not possess inventiveness.

4. Inventiveness – Claim 5

The Examiner points out that claim 5 does not possess inventiveness either. The Examiner holds that Reference 1 (see column 7, lines 25-35 of its Description) discloses the relevant technical features, and high K high temperature oxide is conventional the blocking dielectric layer material, which cannot produce any unexpected technical effects. And thus the technical scheme of claim 5 does not possess inventiveness on the condition that claim 4 it refers to does not possess inventiveness.

5. Inventiveness – Claim 6

The Examiner points out that claim 6 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 6 is disclosed by Reference 1 (see Figs 1A-1D). And thus the technical scheme of claim 6 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

6. Inventiveness – Claims 7-8

The Examiner points out that claims 7-8 do not possess inventiveness either. The Examiner holds that the additional technical features of claims 7-8 can be reasonably configured by a person skilled in the art according to needs. And thus the technical schemes of claims 7-8 do not possess inventiveness on the condition that claim 6 they refer to does not possess inventiveness.

7. Inventiveness – Claim 9

The Examiner points out that claim 9 does not possess inventiveness either. The

Sandisk Technologies, Inc. - Ex. 1002, Page 000559

Examiner holds that the additional technical feature of claim 9 is disclosed by Reference 1 (see Figs 9-10). And thus the technical scheme of claim 9 does not possess inventiveness on the condition that claim 6 it refers to does not possess inventiveness.

8. Inventiveness – Claim 10

The Examiner points out that claim 10 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 10 is disclosed by Reference 1 (see column 5, lines 58-67 of its Description and Fig. 3C). And thus the technical scheme of claim 10 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

9. Inventiveness – Claim 11

The Examiner points out that claim 11 does not possess inventiveness over Reference 1 in view of known common knowledge, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 1 (see column 3, line 24 to column 8, line 44 of its Description and Figs. 1-10), wherein the middle oxide layer 124' is equivalent to the anti-tunneling layer, and the Examiner admits that the distinguishing technical feature of the technical scheme in claim 11 is that: *the channel comprises polysilicon.*

The Examiner holds that the polycrystal is conventional channel material in the art, it cannot produce any unexpected technical effects. And thus on the basis of Reference 1 in combination of known common knowledge, the technical scheme of claim 11 is obvious to a person skilled in the art.

10. Inventiveness – Claim 12

The Examiner points out that claim 12 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 12 is conventional channel material in the art, which cannot produce any unexpected technical effects. And thus the technical scheme of claim 12 does not possess inventiveness on the condition that claim 1 *[sic, claim 11]* it refers to does not possess inventiveness.

11. Inventiveness – Claim 13

The Examiner points out that claim 13 does not possess inventiveness either. The Examiner holds that Reference 1 (see column 8, lines 11-17 of its Description) discloses that gate electrode comprises polysilicon, and the rest additional technical feature can be reasonably configured by a person skilled in the art according to needs. And thus the technical scheme of claim 13 does not possess inventiveness on the condition that claim 12 it refers to does not possess inventiveness.

12. Inventiveness – Claim 14

[redacted]

The Examiner points out that claim 14 does not possess inventiveness either. The Examiner holds that the high K high temperature oxide is conventional blocking dielectric layer material in the art, which cannot produce any unexpected technical effects. And thus the technical scheme of claim 14 does not possess inventiveness on the condition that claim 13 it refers to does not possess inventiveness.

13. Inventiveness – Claim 15

The Examiner points out that claim 15 does not possess inventiveness either. The Examiner holds that the silicon nanowire is conventional channel material in the art, which cannot produce any unexpected technical effects. And thus the technical scheme of claim 15 does not possess inventiveness on the condition that claim 1 *[sic, claim 11]* it refers to does not possess inventiveness.

14. Inventiveness – Claim 16

The Examiner points out that claim 16 does not possess inventiveness either. The Examiner holds that Reference 1 (see column 8, lines 11-17 of its Description) discloses that gate electrode comprises polysilicon, and the rest additional technical feature can be reasonably configured by a person skilled in the art according to needs. And thus the technical scheme of claim 16 does not possess inventiveness on the condition that claim 11 it refers to does not possess inventiveness.

15. Inventiveness – Claim 17

The Examiner points out that claim 17 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 17 is disclosed by Reference 1 (see Figs.1A-1D). And thus the technical scheme of claim 17 does not possess inventiveness on the condition that claim 11 it refers to does not possess inventiveness.

16. Inventiveness – Claim 18

The Examiner points out that claim 18 does not possess inventiveness over Reference 1 in view of Reference 2 (US2002/0109138A1, August 15, 2002), and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 1 (see column 3, line 24 to column 8, line 44 of its Description and Figs. 1-10), the Examiner admits that the distinguishing technical feature of the technical scheme in claim 18 is the following:

the channel is a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region.

The Examiner holds that Reference 2 (see paragraphs 26-51 of its Description and

Sandisk Technologies, Inc. - Ex. 1002, Page 000561

Figs.2-6F) discloses the relevant technical features. And thus on the basis of Reference 1 in combination of Reference 2, the technical scheme of claim 18 is obvious to a person skilled in the art.

17. Inventiveness – Claim 19

The Examiner points out that claim 19 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 19 is disclosed by Reference 1 (see Figs.1A-1D). And thus the technical scheme of claim 19 does not possess inventiveness on the condition that claim 18 it refers to does not possess inventiveness.

18. Inventiveness – Claim 20

The Examiner points out that claim 20 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 20 is disclosed by Reference 1 (see column 5, line 58-67 of its Description and Fig. 3C). And thus the technical scheme of claim 20 does not possess inventiveness on the condition that claim 18 it refers to does not possess inventiveness.

Conclusive opinion

Based on the above opinions, the Examiner also holds, as marked in the form of this Office Action, that the application does not possess any patentable substantial contents, and if the applicant fails to expound reasons or the reasons expounded are not sufficient, this application will be rejected.

This generally is a conclusive opinion of the Examiner and in next the Examiner is likely to issue a final rejection if the response to this Action is not persuasive or no substantial amendments are made.

Our Comments and Recommendation

With regard to the Examiner's rejections above, after reviewing the application documents and the OA text, we would like to provide the following information and our recommendation for your reference.

With regard to the inventiveness issue of claims 1-20

Regarding inventiveness, please be advised that for determining the inventiveness, two factors are required:

(i) non-obviousness, which means that its technical scheme, as compared with the prior art, should be non-obvious to a person skilled in the art, and

(ii) notable progress, which means its technical scheme, as compared with the prior art, could produce advantageous technical effect.

Therefore, it is suggested to prove that the technical scheme of a claim is non-obvious to a person skilled in the art and could produce advantageous technical effect as compared with the prior art.

[redacted]

In addition, if the followings exist for this invention, it is helpful to include them into the response:

- it is hard for a person skilled in the art to create the technical scheme of this invention due to some technical difficulties, technical prejudice or misleading from common thoughts;
- this invention brings unanticipated technical effects;
- this invention brings unanticipated success in the market; and
- other similar situations, such as long-felt but unsolved needs, failure of others.

Independent Claim 1

As for this issue, in order to add the weight of arguments, we recommend amending claim 1 by further defining the meaning of the high work function gate electrode and arguing that amended claim 1 does possess inventiveness as follows:

Claim 1 (as amended, wherein the added technical feature is underlined) defines a semiconductor device comprising: a memory transistor including: a channel region electrically connecting a source region and a drain region formed in a substrate, the channel region comprising polysilicon; an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer; and a high work function gate electrode formed over a surface of the ONNO stack, which means that minimum energy needed to remove an electron from a gate electrode is increased.

Supports for such amendments may be found from the contents "*By high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased*" in paragraph [0028] of the initial description.

Reference 1 (US8071453B1) discloses a method of integrating a non-volatile memory device and a MOS device comprising: forming a pad dielectric layer above a first region of a substrate; forming a patterned dielectric stack above a second region of said substrate, said patterned dielectric stack comprising a tunnel layer, a charge-trapping layer, and a sacrificial top layer; removing said sacrificial top layer from said second region of said substrate; removing said pad dielectric layer from said first region of said substrate; simultaneously forming a gate dielectric layer above said first region of said substrate and a blocking dielectric layer above said charge-trapping layer;……(see claim 1 of Reference 1).

From the above contents, besides the distinguishing feature "the channel region comprising polysilicon" admitted by the Examiner in this office action, it can be seen that amended claim 1 of the present application also possesses at least the following distinguishing technical feature when comparing with Reference 1:

a high work function gate electrode formed over a surface of the ONNO stack, which means that minimum energy needed to remove an electron from a gate electrode is increased.

Reference 1 does **not** disclose that its gate dielectric layer is high work function gate electrode, which means that minimum energy needed to remove an electrode from a gate electrode is increased.

[redacted]

In addition, in Reference 1, the gate dielectric layer is formed above the first region of the substrate, but not over the surface of the dielectric stack, as defined in amended claim 1 of the present invention.

And the above distinguishing technical features are not common knowledge in the art.

With these distinguishing technical features, the semiconductor device defined in claim 1 of the present invention can **increase data retention and/or to improve programming time and efficiency** (see paragraph [0025] of the initial description).

Therefore amended claim 1 does possess inventiveness over Reference 1 in view of common knowledge.

Dependent Claims 2-10

Claims 2-10 are dependent claims of claim 1. On the basis that claim 1 is proved to possess inventiveness, claims 2-10 also possess inventiveness.

Independent Claims 11 and 18

As for this issue, we recommend amending claims 11 and 18, and arguing that amended claims 11 and 18 do possess inventiveness over Reference 1, in a similar way as for claim 1.

Dependent Claims 12-17 and 19-20

Claims 12-17 are dependent claims of claim 11, claims 19-20 are dependent claims of claim 18. On the basis that claims 11 and 18 are proved to possess inventiveness, claims 12-17 and 19-20 also possess inventiveness.

We have prepared an English version of our proposed claim amendments for your reference, in which terms about "ONONO stack" in claims 11 and 18 are recommended to be amended to "ONNO stack" to correct obvious typing errors. Please see the attachment for details.

The above amendments and comments are for your reference only. Considering that the Office currently takes strict examination rules, if, unfortunately, the Examiner does not accept them, further amendments and/or arguments might be necessary.

Please be advised that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. The Office currently examines go-beyond issue very strictly, more strictly than that in many other countries. The "scope recorded in the initial description and claims", pursuant to the Patent Examination Guidelines, includes (1) literal contents of the initial description and claims, and (2) contents determined directly and undoubtedly from the drawings and the literal contents of the initial description and claims.

According to the Supreme Court's ruling in one recent case, such "scope" should include (i) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims of the application, and (ii) contents directly or definitely derived by a person skilled in the art from the initial description, drawings and claims as a whole, which should correct the strict rules of the Office. However, in practice, examiners are still likely to

Sandisk Technologies, Inc. - Ex. 1002, Page 000564

examine the go-beyond issue strictly. The applicant had better take this in mind if deciding to make any amendments.

A response and possible amendments must be submitted to the Office by **April 17, 2017 (Beijing Time)**. Please give us your further instructions as soon as possible.

[redacted]

We also list the related regulations below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your prompt reply is highly appreciated.

Please kindly confirm receipt of this letter by return e-mail.

Sincerely yours,
AFD China Intellectual Property



[redacted]

/Ljp/Lyl
/Lhm/Ldz

Enclosures: (All by E-mail only)
1. A copy of the Chinese Notification of the First Office Action;
2. A copy of Reference documents;
3. A set of pending claims; and
4. Our invoice.

Patent Law:

Article 22(3): Inventiveness means that, as compared with the prior art, the invention has prominent substantive features and represents a notable progress, and that the utility model has substantive features and represents progress.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

[redacted]

RELIABILITY AND PROCESSING EFFECTS OF BANDGAP ENGINEERED SONOS (BE-SONOS) FLASH MEMORY

Szu-Yu Wang[1,2], Hang-Ting Lue[1], Erh-Kun Lai[1], Ling-Wu Yang[1], Tahone Yang[1], Kuang-Chao Chen[1], Jeng Gong[2], Kuang-Yeu Hsieh[1], Rich Liu[1], and Chih Yuan Lu[1]

[1]Macronix International Co. Ltd, No. 16, Li-Hsin Road, Hsinchu Science Park, Hsinchu 300, Taiwan
[2] Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 300, Taiwan
E-mail: kirinwang@mxic.com.tw

ABSTRACT

The reliability properties of BE-SONOS [1] are extensively studied. BE-SONOS employs a multi-layer O1/N1/O2/N2/O3 stack, where O1/N1/O2 serves as a bandgap engineered tunneling barrier that provides an efficient hole tunneling erase but eliminates the direct tunneling leakage. BE-SONOS can overcome the fundamental limitation of the conventional SONOS, for which fast erase speed and good data retention cannot be simultaneously achieved. In this work, we provide a comprehensive understanding of the reliability of BE-SONOS. Various processes to form the critical O1/N1/O2 barrier, the trapping layer (N2), and the top blocking oxide (O3) are investigated. The results of this work provide design and processing guidelines for optimizing the performance and reliability of BE-SONOS Flash memory devices.

I. Introduction

Recently, SONOS-type devices are forecasted to be the solution for NAND Flash beyond 45 nm node [1,2]. Unlike floating-gate device, SONOS device has no floating gate coupling ratio issue hence it greatly saves the process complexities in the floating poly geometry. Since charges are independently trapped, it is naturally immune to the capacitance coupling interference due to the adjacent memory cells [2]. Moreover, SONOS-type device requires very few electrons (<500) and is without erratic behaviors. Therefore, SONOS device is ideal in terms of scaling and reliability.

However, the conventional SONOS has a fundamental limitation. Since electrons are deeply trapped in nitride, de-trapping speed is very slow if tunnel oxide is thick (>3nm). A higher electric field does not help since it introduces a large gate injection [3] negating the erase operation. Therefore, SONOS devices are often designed with a thin tunnel oxide (~2 nm), where hole direct tunneling from the substrate can compensate the trapped electrons during erase operation. However, such thin oxide leads to very poor data retention because hole direct tunneling occurs even at very low field.

Recently, we proposed BE-SONOS [1] to overcome this limitation. The structure of BE-SONOS is shown in Fig. 1. Unlike SONOS, a bandgap engineered ONO barrier is used to replace the tunnel oxide. The band diagram concept is illustrated in Fig. 2. Under high electric field, the band offset can reduce the hole tunneling distance to effectively the thin O1, thus a large hole current is allowed. On the other hand, at low electric field during retention, both electron-de-trapping and hole direct tunneling are completely prohibited by the total barrier thickness (O1+N1+O2).

The simulated hole tunneling current is shown in Fig. 3. For a thin oxide used in the conventional SONOS, the direct tunneling current cannot be turned-off even at 1 MV/cm, which is typically the built-in electric field for a device in the programmed state. Therefore, severe charge leakage is observed even at room temperature for SONOS. For a thick oxide (>3nm), the hole tunneling current is negligible ($<10^{-6}$A/cm^2) because of the large hole barrier height of oxide (4.5 eV). Therefore, conventional SONOS with a thick tunnel oxide has a very slow erase speed. On the other hand, the engineered ONO barrier behaves entirely differently. At high field (~10 MV/cm), the hole current is high, ~10^{-3}A/cm^2 and provides high erase speed, yet it is completely suppressed at low field (<2 MV/cm). Therefore, BE-SONOS provides both fast erase speed and good data retention.

The basic characteristics of BE-SONOS devices were described in previous works [4-7]. Recently we have carried out very long-term (>1000 hours) retention tests at various temperatures, and developed a model to predict the lifetime of BE-SONOS [4]. In this work, the reliability properties and their correlation with processing methods of BE-SONOS are examined in detail. The present work provides a comprehensive understanding of BE-SONOS reliability.

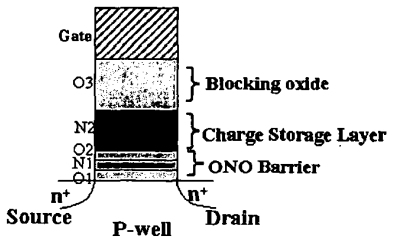


Fig. 1 Structure of the n-channel BE-SONOS using ultra-thin ONO tunneling barrier.

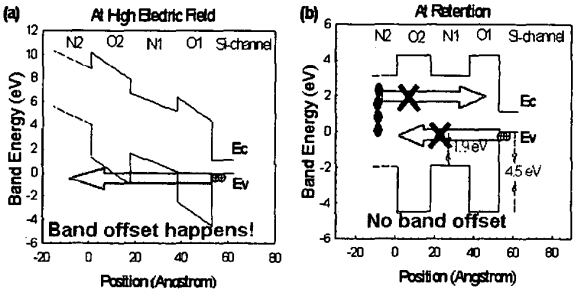


Fig. 2 Bandgap engineering concept for the BE-SONOS device. (a) At high field during erase, band offset reduces the hole tunneling barrier to merely O1. (b) At low field during retention, both electron de-trapping and hole back tunneling are prohibited by the full O1/N1/O2 barrier stack.

Sandisk Technologies, Inc. - Ex. 1002, Page 000566

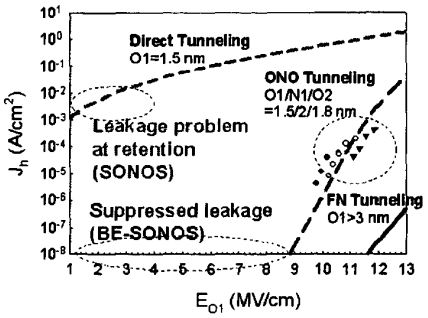


Fig. 3 J-E characteristics of various tunneling barrier. Thin oxide (1.5 nm), thick oxide (>3 nm) and ONO barrier are compared.

II. Processing Description

The ultra-thin oxide (<2 nm) is fabricated by in-situ steam generation (ISSG). ISSG is a rapid-thermal radical reaction method. Since ultra-thin oxide is critical for BE-SONOS, a test run on control wafer is carried out before O1 formation in order to guarantee the thickness control. The thickness is measured by optical ellipsometer. The thickness accuracy can be controlled within 1 Å.

LPCVD is used for nitride deposition (for both N1 and N2). The typical thickness for N1 and N2 are 2 and 7 nm, respectively. Deposition is carried out at 680^{0}C with DCS and NH_3 precursors. For the SiON thin films (N2), additional N_2O gas is applied in the gas flow.

For the inter oxide (O2), LPCVD oxide (HTO) with thickness thinner than 3 nm is deposited. For the top oxide (O3), the standard method is the thermal conversion of nitride in furnace at high temperature (950-1000^{0}C) with O_2 and H_2O gas (wet conversion process). In this process, a 13 nm nitride is converted into a 9 nm top oxide, with 7 nm nitride remaining. The wet conversion process produces a strong top oxide that can withstand a large P/E cycling stress. However, it requires a large thermal budget. In some samples, HTO and ISSG top oxides are fabricated for comparison. The typical thickness for O3 is 9 nm.

A heavily doped P^+-poly gate is used for all the samples in this work. P^+-poly gate can greatly reduce the gate injection during –FN erase, thus resulting in lower erase saturation V_{FB}.

III. Properties of Ultra-Thin ONO Barrier

BE-SONOS employs an ultra-thin ONO as the tunneling barrier. The first nitride N1 serves as a non-trapping dielectric that alters the hole tunneling current. The non-trapping behavior of the ONO barrier is shown in Fig. 4, where constant current stress (CCS) shows no significant trapping even after1000 sec continuous stress. Figure 5 shows that the measured I_G-V_G curve is consistent with the theoretical calculation at high field. Besides, the I_G-V_G curves show no degradation after current stress.

Figure 6 shows the I_G-V_G curves of the ONO barrier at various temperatures. The measured current is insensitive to temperature. This further supports that the measured current is indeed tunneling current rather than Frenkel-Poole (F-P) current, since F-P current strongly depends on the temperature.

Recently, many high-*k* dielectrics are found to have a fast transient injection effects [8]. In order to clarify this possible effect, we have carried out the pulsed *IV* measurement [6] for BE-SONOS device. The result is shown in Fig. 7, where the pulsed *IV* shows identical drain current as the DC results. This indicates that the ultra-thin ONO does not have any instant charge trapping/de-trapping within a short (~20 μsec) transient time.

We have found that the capture efficiency of nitride significantly decreases for thickness below 3 nm [9]. The physical reason is not completely understood even now. A possible reason is that the capture mean free path is larger than the nitride thickness such that very low trapping can occur. Moreover, both oxide and nitride are very thin thus the electrons gain very small energy during the tunneling process.

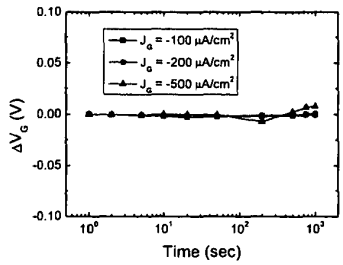


Fig. 4 Constant current stress (CCS) of the ONO capacitor (15/20/25 Å). The selected current density is chose to be close to that during typical –FN erase (<10^{-3}A/cm^2).

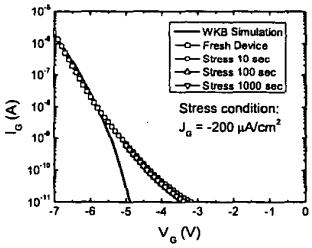


Fig. 5 Constant current stress (CCS) of the ONO (15/20/25 Å) capacitor. The selected current density is chose to be that used in the erase (<10^{-3}A/cm^2). P^+-poly gate is used to suppress the gate injection during –Vg stress.

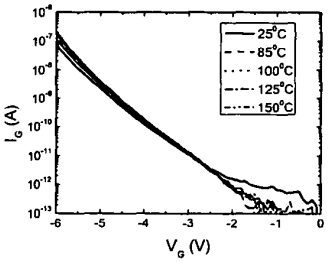


Fig. 6 I_G-V_G curve of ONO barrier at various temperatures.

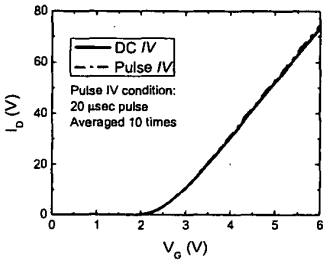


Fig. 7 Comparison of the pulse IV and DC IV results of a BE-SONOS transistor. The pulse IV measurement is carried out in a Keithley 4200 system.

It should be noted that SONOS-type devices tolerate a much less perfect tunneling barrier than the floating-gate device. In the floating-gate device, a single defect in the tunneling barrier can drain the entire charge in the floating-gate, leading to severe charge loss and erratic behaviors. Therefore, tunneling barrier engineering, such as the "crested barrier" [10] concept, for floating-gate devices is difficult to realize due to reliability concerns.

On the other hand, the charges are discretely trapped in SONOS-type devices, hence it is much less sensitive to defects in the tunneling barrier. Therefore, even as the bandgap engineered ONO barrier is not perfect (it contains a SiN layer), BE-SONOS has already shown excellent reliability performance.

IV. Comparisons of BE-SONOS and the Conventional SONOS

Figure 8 compares the –FN erase speed of various SONOS and BE-SONOS devices. The erase speed of BE-SONOS with a 15/20/25Å ONO barrier is comparable with SONOS using a 20Å tunnel oxide. However, SONOS with a 25Å tunnel oxide has a dramatically slower erase speed. For the device erased from fresh state (Fig. 8(a)), the gate injection current is even larger than hole tunneling. This is because oxide has a large hole barrier height (~4.5 eV) so that FN tunneling of hole is negligible for a thicker oxide. Hole direct tunneling occurs only for very thin oxide (<2.5 nm).

Figure 9 indicates that the retention of SONOS with tunnel oxide equal to 20Å is very poor. Although the retention of SONOS with a 25Å tunnel oxide is improved (but still much worse than BE-SONOS), the erase speed becomes too slow for practical applications. Therefore, there is no single tunnel oxide thickness that can satisfy both erase speed and retention requirements for the conventional SONOS.

BE-SONOS can overcome this limitation. BE-SONOS provides far superior data retention than conventional SONOS for the same erase speed. This is achieved by employing the bandgap engineered ONO barrier. In the following sections, the processing methods and reliability performance of BE-SONOS are investigated.

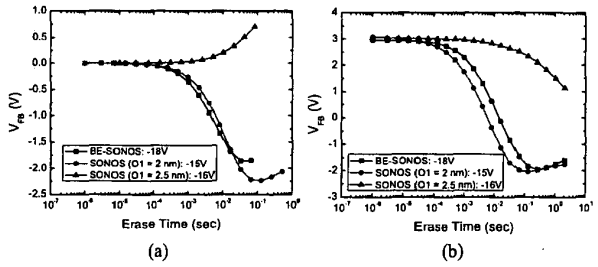


Fig. 8 Comparison of the –FN erase speed of BE-SONOS (15/20/25/70/90Å), SONOS (20/70/90 Å) and SONOS (25/70/90 Å). (a) Erased from fresh state. (b) erased from V_{FB}=+3V. The bias voltages are selected to make these samples to have approximately the same electric field.

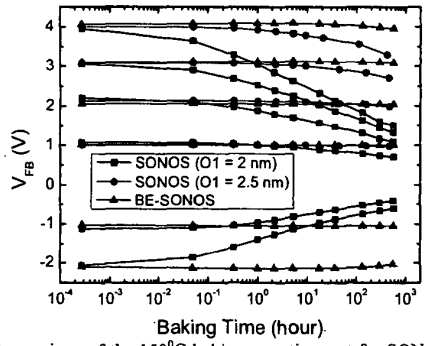


Fig. 9 Comparison of the 150°C baking retention test for SONOS and BE-SONOS (15/20/25/70/90Å). A wide range of PV state (up to +4 V) and EV states (down to EV= -2V) are tested.

V. BE-SONOS Characteristics with Various O1/N1/O2 Tunneling Dielectric

The erase characteristics of BE-SONOS with various ONO barrier thickness are shown in Fig. 10. The results indicate that the erase speed is mainly dominant by O1 only, while O2 and N1 have a small effect. This is consistent with the bandgap engineering concept, where the band offset effectively screens out N1 and O2 so that the thickness dependency is insignificant.

In Fig. 11, the erase speed of various nitridation of O1 is examined. The ONO barrier with thickness of 15/20/25 Å is adopted for all the samples. Two nitridation treatment processes in NO ambient are conducted. One is to apply NO annealing on O1, and the other is to grow O1 directly in NO ambient. Both processes have the same final optical thickness of 15Å.

Significantly enhanced erase speed is achieved with O1 nitridation treatment. This indicates that the speed of hole direct tunneling is raised. One possible reason is the lowering of oxide barrier height by nitridation. Interestingly, the retention shows insignificant dependence on various ONO barrier processes, as shown in Figs. 12 and 13. This implies that we can improve the erase speed by O1 processing tuning without scarifying the retention of BE-SONOS devices.

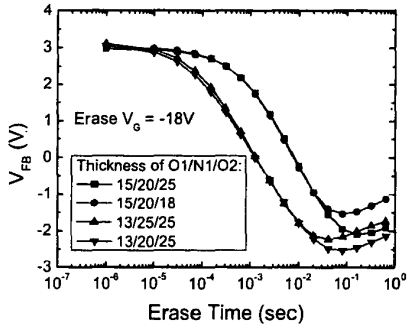


Fig. 10 Comparisons of the –FN erase speed of BE-SONOS devices with various thickness O1/N1/O2 (Å) tunneling barrier. The thickness scheme of N2/O3 is 70/90 (Å) for all samples.

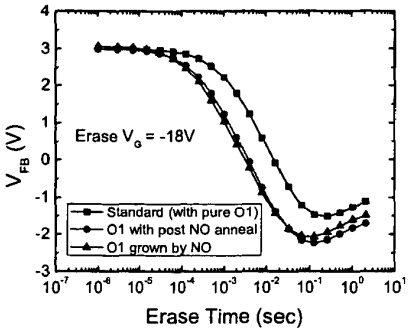


Fig. 11 Comparisons of the –FN erase speed of BE-SONOS devices with various nitridation treatments on O1. The same erase Vg of –18V is applied on all devices.

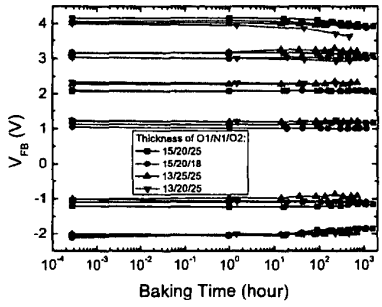


Fig. 12 Comparisons of the150^{0}C retention of BE-SONOS with various ONO barrier thickness (the same devices in Fig. 10).

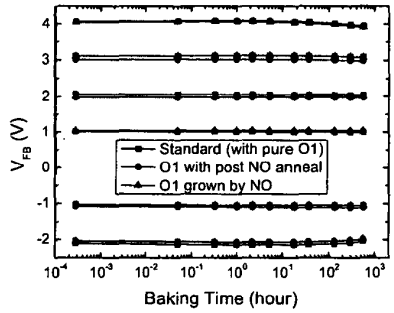


Fig. 13 Comparisons of the150^{0}C retention of BE-SONOS with various nitridation treatments on O1 (the same devices in Fig. 11). All devices perform comparable and this indicates that O1 engineering is not sensitive to data retention characteristic in BE-SONOS device.

VI. BE-SONOS Characteristics with Various O3 Top Dielectric

The top oxide process is also critical for both BE-SONOS and SONOS devices. The role of top oxide is often not seriously taken into account for floating gate devices because most research focuses on the tunnel oxide. However, SONOS-type devices do not have coupling ratio design as the floating gate device and the top oxide must endure similar electric field as that in the bottom oxide during program/erase. This large electric field stress causes a significant impact on the device reliability.

Figure 14 illustrates the -FN erase for various top oxide processes. For the standard wet conversion process, the erase saturated V_{FB} is the lowest one, while HTO top oxide shows a larger saturated V_{FB}. Previous study [11] shows that HTO top oxide has a lower electron barrier height (<3.0 eV) than wet converted top oxide (~3.2 eV). The smaller electron barrier height can results in a larger gate injection of electrons during –FN erase, leading to larger erase saturation V_{FB}.

Fig. 15 shows the endurance performance for both programmed and erased states. All the samples are subjected to the same voltage stress during cycling. For a clear comparison, the threshold voltage shift with respect to the first-cycle result is shown to illustrate the program/erase degradation. The programmed state all shows small degradation. On the other hand, significant erase degradation of HTO top oxide is observed after 1K cycles. Correspondingly, the retention for HTO top oxide is worse than the wet conversion process, especially for the P/E cycled device. These results imply that HTO top oxide is weaker than the furnace wet converted top oxide.

The HTO top oxide can be greatly improved by high temperature annealing. The annealing is carried out in a furnace using a similar thermal budget used in wet conversion. The improvement in the HTO quality in turn improves the endurance and retention performance, as shown in Figs. 15-16. In Fig. 15(b), the erase degradation due to weaker HTO top oxide is greatly improved by the post thermal annealing. The data retention is also improved as shown in Fig. 16, especially for 1K-cycled devices. Recently, we have shown [9] that HTO top oxide easily traps charges under high FN stress. The charge trapping in the HTO top oxide may be the cause of endurance and retention degradation.

We have also applied ISSG to convert nitride into top oxide. ISSG is a low-thermal budget process. In Fig. 14, the erase saturation is in between the HTO and wet conversion. The reliability performance shown in Figs. 15-16 is only slightly worse than that from the wet conversion. These results are encouraging since ISSG has significantly lower thermal budget thus can be applied to TFT memory devices [6,7].

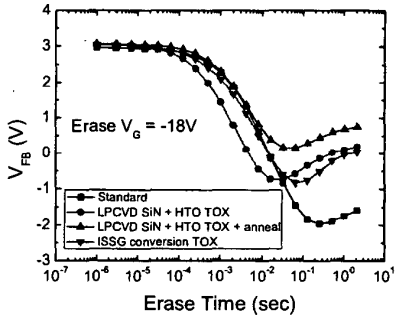


Fig. 14 Comparisons of the –FN erase speed of BE-SONOS devices with various top oxide (O3). The same erase Vg of –18V is applied on all devices.

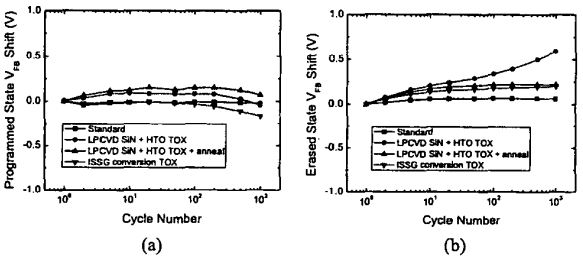
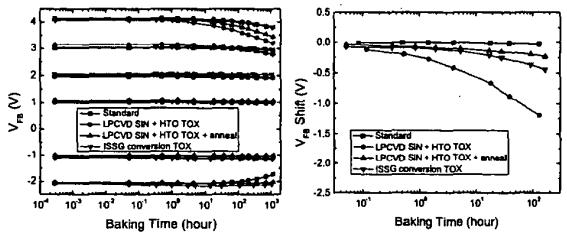


Fig. 15 Comparisons of the endurance for (a) programmed state and (b) erased state. All the device are programmed by +20 V, 200 μsec to V_{FB}~+3V, and erased by –18V 50msec to V_{FB}~ -1 V. The threshold voltage shifts

compared with the first-cycle result are shown to illustrate the program/erase degradation.



(a) (b)

Fig. 16 Comparisons of the 150°C retention for BE-SONOS with various top oxide (O3). (a) fresh device without P/E cycles, (b) charge loss of V_{FB}=+3 V sate for the 1K cycled device. The cycling condition is as the same as that in Fig. 15. The processes with converted top oxide perform consistent even after 1K-cycling stress. The severe degradation in data retention that caused by weak HTO top oxide is revealed in (b). While applied with post thermal anneal, the degradation is significantly reduced.

VII. BE-SONOS Characteristics with Various N2 Trapping Dielectric

The trapping material plays an important role in data storage characteristics. An understand of the trapping layer behavior may lead us to understand why BE-SONOS has such superior reliability performance.

The trapping SiN of BE-SONOS is fabricated by a LPCVD SiN film that is then partially converted to top oxide by high temperature furnace wet oxidation. During this wet oxidation, a transition SiON layer between top oxide and SiN is formed [11].

Our previous works have revealed that there exists some correlation of trapping characteristics between the transition SiON layer and the LPCVD SiON thin film [12]. However, the correlation to reliability characteristics such as data retention has not been evaluated yet. Since the thermal conversion of SiON into top oxide is much more complicated, a HTO top oxide is adopted. From section VI, the HTO top oxide can be strengthened by a furnace thermal anneal in order to minimize the reliability degradation. Here three different trapping materials of standard process, LPCVD SiN, and LPCVD SiON are conducted on BE-SONOS devices to examine the role of the transition SiON layer in the standard process.

The SiN (without wet conversion) trapping material is deposited in a vertical LPCVD furnace using dichlorosilane (DCS) and NH_3, while the SiON is deposited in the same tool using DCS, NH_3 and N_2O. Fig. 17 shows the data retention performance of fresh devices under different baking temperatures. In Fig. 17(a), the standard process continues to show superior data retention even when the initial V_{FB} is programmed to 4V (<200 mV charge loss at 150°C 1000 hours baking). The LPCVD SiON trapping material shows comparable retention performance to that of the standard process but the LPCVD SiN trapping material is significantly worse. When the samples are baked to 250°C (Fig. 17(b)), the programmed state vertical charge loss increases but the SiON group (the standard process and the LPCVD SiON trapping layer) still performs much better than that with only the SiN trapping material. Therefore, it is clearly shown that SiON indeed provides better trapping stability than SiN. Additionally, this suggests that the transition SiON layer very possibly plays a key role in the superior data retention of the standard BE-SONOS process.

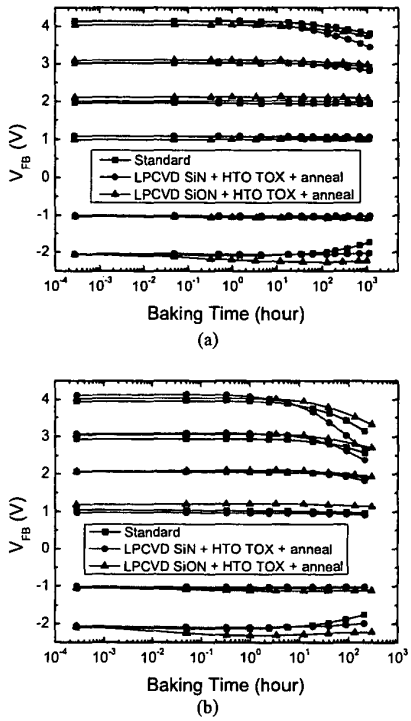


Fig. 17 (a) 150°C and (b) 250°C retention comparisons of BE-SONOS device with standard wet conversion, SiN with HTO and SiON with HTO processes. The tests are executed on fresh devices that directly programmed or erased to the respective six different V_{FB} levels from –2V to 4V.

IIX. Discussions and Summary

The present work provides a comprehensive understanding of BE-SONOS reliability and processing methods. The processing guideline is briefly summarized below:

(1) The erase speed is mainly determined by the thin O1. Therefore, the process control in O1 (≤ 15Å) is critical. On the other hand, N1 and O2 have little impact on the erase speed. Therefore, they are not critical and just have to maintain enough thickness to prevent leakage.

(2) The top oxide must be strengthened so that lower erase saturation Vt and better endurance and retention performances can be obtained. However, this layer often uses the largest thermal budget. Therefore, new low thermal-budget processes such as ISSG or plasma oxidation are the best.

(3) The trapping layer can be replaced by other trapping materials. SiON is found to have better retention than standard SiN. However, it requires more process integration with the top oxide.

(4) For the gate material, a heavily doped P^+-poly gate is used to reduce gate injection during –FN erase.

BE-SONOS uses only well known materials including nitride, oxide, and poly gate. Therefore, it is readily manufactured by CMOS process.

Finally, it should be noted that BE-SONOS is also readily integrated with high-*k*/metal gate materials to further enhance the performances.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
LESTER J. VINCENT
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Applicant's or agent's file reference 16820P568PCT	Date of mailing *(day/month/year)* 26 AUG 2008 **FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 08/06627	23 May 2008 (23.05.2008)	25 May 2007 (25.05.2007)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H01L 21/336 (2008.04)
USPC - 438/261

Applicant CYPRESS SEMICONDUCTOR CORPORATION

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	19 August 2008 (19.08.2008)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 08/06627

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. type of material

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing

      ☐ contained in the international application as filed

      ☐ filed together with the international application in electronic form

      ☐ furnished subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 08/06627

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	5, 7, 12, 14	YES
	Claims	1-4, 6, 8-11, 13, 15-20	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1-4, 6, 8-11, 13, 15-20 lack novelty under PCT Article 33(2) as being anticipated by US 2005/0266637 A1 to Wang.

As per claim 1, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising: providing a substrate having a charge-trapping layer disposed thereon (para [0029]); and oxidizing, by exposing the charge-trapping layer to a radical oxidation process, a portion of the charge-trapping layer to form a blocking dielectric layer above the charge-trapping layer (para. [0007]).

As per claim 2, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the radical oxidation process including oxidizing with a radical selected from the group consisting of an OH radical, an HO2 radical and an O diradical (para. [0007], [0027]).

As per claim 3, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the radical oxidation process being carried out at a temperature approximately in the range of 700 - 800 degrees Celsius at a pressure approximately in the range of 0.5 - 5 Torr (para. [0027]).

As per claim 4, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the blocking dielectric layer comprises silicon dioxide (para. [0029]).

As per claim 6, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising annealing the blocking dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N2), nitrous oxide (N20), nitrogen dioxide (N02), nitric oxide (NO) and ammonia (NH3) at a temperature approximately in the range of 700 - 800 degrees Celsius (para. [0021]).

As per claim 8, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising providing a substrate in a process chamber (para. [0018]); subjecting, in the process chamber, the substrate to a first radical oxidation process to form a first dielectric layer (para. [0018]-[0019]); subjecting, in the process chamber, the substrate to a deposition process to form a charge-trapping layer above the first dielectric layer (para. [0029]); and subjecting, in the process chamber, the substrate to a second radical oxidation process to form a second dielectric layer above the charge-trapping layer by oxidizing a portion of the charge-trapping layer (para. [0020]).

As per claim 9, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising both the first and the second radical oxidation processes include oxidizing with a radical selected from the group consisting of an OH radical, an HO2 radical and an O diradical (para. [0027]).

As per claim 10, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising both the first and the second radical oxidation processes being carried out at a temperature approximately in the range of 700 . 800 degrees Celsius at a pressure approximately in the range of 0.5 - 5 Torr (para. [0027]).

As per claim 11, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the charge-trapping layer comprising a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (para. [0029]).

As per claim 13, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising annealing, in the process chamber, the second dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N2), nitrous oxide (N2O), nitrogen dioxide (NO2), nitric oxide (NO) and ammonia (NH3) at a temperature approximately in the range of 700 - 800 degrees Celsius (para. [0021]); and, subsequently, depositing a gate layer above the second dielectric layer (para. [0029]).

---Please See Continuation Page---

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 08/06627

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V. 2. Citations and explanations:

As per claim 15, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising subjecting the substrate to the deposition process to form the charge-trapping layer includes using a gas selected from the group consisting of dichlorosilane (H2SiCh), bis-(tert-butylamino)silane (BTBAS), ammonia (NH3) and nitrous oxide (N20) (para. [0007]).

As per claim 16, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the process chamber being a low-pressure chemical vapor deposition chamber (para. [0007]).

As per claim 17, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising providing a substrate in a process chamber (para. [0018]); mixing, in the process chamber, hydrogen gas and oxygen gas without subjecting the hydrogen gas and oxygen gas to a combustion process (para. [0027]); and oxidizing, in the process chamber, a portion of the substrate with radicals generated from the mixing of the hydrogen gas and oxygen gas (para. [0027]).

As per claim 18, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the mixing of the hydrogen gas and oxygen gas and the oxidizing of the portion of the substrate are carried out at a temperature approximately in the range of 700 - 800 degrees Celsius at a pressure approximately in the range of 0.5 - 5 Torr (para. [0027]).

As per claim 19, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the hydrogen gas and oxygen gas being mixed in an approximate ratio of 1:1 (para. [0027]).

As per claim 20, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the process chamber being a low-pressure chemical vapor deposition chamber (para. [0027]).

Claims 5, 12 lack and inventive step under PCT Article 33(3) as being obvious over Wang in view of US 7,033,957 B1 to Shiraiwa et al. (hereinafter 'Shiraiwa').

As per claim 5, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the charge-trapping layer comprising a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5 - 3.5 nanometers (Wang, para. [0027]). However Wang does not disclose a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9 - 10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer having a thickness approximately in the range of 3.5 - 4.5 nanometers. Shiraiwa discloses ONO fabrication process comprising a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9 - 10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer having a thickness approximately in the range of 3.5 - 4.5 nanometers (Shiraiwa, col. 9, ln 1-5; col. 16, ln 55-60). One of ordinary skill in the art would have been motivated to modify the method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory) of Wang and the ONO fabrication process as taught by Shiraiwa in order to form a memory device comprising layers of desired thicknesses.

As per claim 12, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory), comprising the charge-trapping layer comprising a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5 - 3.5 nanometers (Wang, para. [0027]). However Wang does not disclose a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9 - 10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer having a thickness approximately in the range of 3.5 - 4.5 nanometers. Shiraiwa discloses ONO fabrication process comprising a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9 - 10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer having a thickness approximately in the range of 3.5 - 4.5 nanometers (Shiraiwa, col. 9, ln 1-5; col. 16, ln 55-60). One of ordinary skill in the art would have been motivated to modify the method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory) of Wang and the ONO fabrication process as taught by Shiraiwa in order to form a memory device comprising layers of desired thicknesses.

Claims 7, 14 lack and inventive step under PCT Article 33(3) as being obvious over Wang in view of US 6,835,621 B2 to Yoo et al. (hereinafter 'Yoo').

As per claim 7, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory). However Wang does not disclose the nonvolatile charge trap memory device being a SONOS-type device, and wherein a tunnel dielectric layer is disposed between the substrate and the charge-trapping layer. Yoo discloses method of fabricating non-volatile memory device having a structure of SONOS comprising nonvolatile charge trap memory device being a SONOS-type device, and wherein a tunnel dielectric layer is disposed between the substrate and the charge-trapping layer (col. 4, ln 40-45). One of ordinary skill in the art would have been motivated to modify the method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory) of Wang and the method of fabricating non-volatile memory device having a structure of SONOS as taught by Yoo in order to form a SONOS type memory device structure.

---Please See Continuation Page---

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 08/06627

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:
Box V. 2. Citations and explanations:

As per claim 14, Wang discloses a method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory). However Wang does not disclose SONOS-type device, wherein the first dielectric layer is a tunnel dielectric layer, and wherein the second dielectric layer is a blocking dielectric layer. Yoo discloses method of fabricating non-volatile memory device having a structure of SONOS comprising SONOS-type device, wherein the first dielectric layer is a tunnel dielectric layer, and wherein the second dielectric layer is a blocking dielectric layer (col. 4, ln 40-45). One of ordinary skill in the art would have been motivated to modify the method of fabricating a nonvolatile charge trap memory device (tunnel oxynitride in flash memory) of Wang and the method of fabricating non-volatile memory device having a structure of SONOS as taught by Yoo in order to form a SONOS type memory device structure.

Claims 1-20 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: LARRY JOHNSON
CYPRESS SEMICONDUCTOR
CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	30 MAY 2013
Applicant's or agent's file reference PM07002CIP2W	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2013/032339	15 March 2013	31 March 2012

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H01L 29/792 (2013.01)
USPC - 257/411

Applicant CYPRESS SEMICONDUCTOR CORPORATION

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	17 May 2013	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/032339

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/032339

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	2-7, 9-20	YES
	Claims	1, 8	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1 and 8 lack novelty under PCT Article 33(2) as being anticipated by Polishchuk et al. (hereafter Polishchuk).

Regarding claim 1, Polishchuk discloses a memory device (Fig. 3, 304 "non-volatile memory transistor") comprising:
a channel (Fig. 3, 312 "channel region") formed from a semiconducting material (substrate 306 is made of silicon; Col. 8, line 47) overlying a surface on a substrate (306) connecting a source and a drain (314 "source and drain (S/D) regions") of the memory device;
a tunnel oxide layer (316 "tunnel oxide"; Col. 8, line 53) overlying the channel; and
a multi-layer charge storing layer (318A and 318B; Col. 8, lines 53-54) including an oxygen-rich, first oxynitride layer (318B; Col. 2, lines 38-46 "bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer") on the tunnel oxide layer (316) in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free (Col. 2, lines 38-46 "substantially trap free bottom oxynitride layer"; also see Col. 8, lines 55-58), and an oxygen-lean, second oxynitride layer (318A; Col. 2, lines 38-46 "top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer") on the first oxynitride layer (318B) in which a stoichiometric composition of the second oxynitride layer results in it being trap dense (Col. 2, lines 38-46 "charge trapping top oxynitride layer"; also see Col. 8, lines 55-58).

Regarding claim 8, Polishchuk discloses the memory device of claim 1. Polishchuk further discloses wherein the second oxynitride layer further comprises a concentration of carbon selected to increase a number of traps therein (Col. 3, lines 42-47 "increase a concentration of carbon and thereby the number of traps therein").

Claims 2 and 3 lack an inventive step under PCT Article 33(3) as being obvious over Polishchuk in view of Iwata.

Regarding claim 2, Polishchuk discloses the memory device of claim 1.
Polishchuk fails to explicitly disclose wherein the channel comprises polysilicon.
However, Iwata, in the related field of forming MOS transistors including an ONO structure (Para. [0005]; Fig. 7B), teaches a channel comprising polysilicon (Para. [0132] "channel regions 25...can be formed by re-crystallizing deposited amorphous silicon or polysilicon").
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the channel material of Polishchuk and form the channel from polysilicon as taught by Iwata. The motivation would have been to use a material that is compatible with high temperature processing.

Regarding claim 3, Polishchuk discloses the memory device of claim 1.
Polishchuk fails to explicitly disclose wherein the channel comprises recrystallized polysilicon.
However, Iwata, in the related field of forming MOS transistors including an ONO structure (Para. [0005]; Fig. 7B), teaches a channel comprising recrystallized polysilicon (Para. [0132] "channel regions 25...can be formed by re-crystallizing deposited amorphous silicon or polysilicon")).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the channel formed method of Polishchuk and form the channel from recrystallized polysilicon as taught by Iwata. The motivation would have been decrease the defects in the channel that hamper carrier mobility.

Claims 4-7 lack an inventive step under PCT Article 33(3) as being obvious over Polishchuk in view of Chen et al. (hereafter Chen).

Regarding claim 4, Polishchuk discloses the memory device of claim 1.
Polishchuk fails to explicitly disclose wherein the channel comprises a silicon nanowire.
However, Chen, in the related filed of forming field effect transistors (Para. [0025] "FinFET"; Fig. 2c), teaches using a silicon nanowire (Para. [0025] "nano-wire FinFET" and Para. [0036] "a rounded semiconductor nano-wire may be formed from the semiconductor layer" and "such as silicon") as the channel (see Fig. 2c; note that the channel is under the gate electrode and between the source and drain regions).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the channel of Polishchuk and use a silicon nanowire as the channel as taught by Chen. The motivation would have been form a rounded channel so that the gate electrode can gain significant influence on the channel potential, therefore improving suppression of short-channel effects as taught by Chen (Paras. [0005]-[0007]).

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/032339

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Regarding claim 5, Polishchuk discloses the memory device of claim 1. Polishchuk further discloses wherein the gate comprises the tunnel oxide layer (Fig. 3, 316) and the multi-layer charge storing layer (Fig. 3, 318A and 318B).
Polishchuk fails to explicitly disclose wherein the memory device comprises a non-planar transistor including a gate having multiple surfaces abutting the channel.
However, Chen, in the related filed of forming field effect transistors (Para. [0025] "FinFET"; Fig. 2c), teaches a memory device comprising a non-planar transistor (Fig. 2c) including a gate (G) having multiple surfaces (the gate is contacting the top and side surfaces of the channel) abutting a channel (note that the channel is under the gate electrode (G) and between the source (S) and drain (D) regions).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the transistor structure of Polishchuk and incorporate a non-planar transistor including a gate having multiple surfaces abutting the channel as taught by Chen. The motivation would have been form a rounded channel so that the gate electrode can gain significant influence on the channel potential, therefore improving suppression of short-channel effects as taught by Chen (Paras. [0005]-[0007]).

Regarding claim 6, Polishchuk in view of Chen discloses the memory device of claim 5. Polishchuk further discloses wherein the gate further comprises a blocking dielectric (Fig. 3, 320 "top of blocking oxide layer"; Col. 8, line 54) overlying the multi-layer charge storing layer (318A and 318B), and a gate layer (308 "gate electrode"; Col. 8, line 48) overlying the blocking dielectric layer.
Polishchuck fails to explicitly disclose wherein the gate electrode is metal (Polishchuk discloses a polysilicon gate electrode).
However, Chen, in the related filed of forming field effect transistors (Para. [0025] "FinFET"; Fig. 2c), teaches a gate electrode formed of metal (Para. [0047] "gate electrode material may be...metal material").
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the gate electrode material of Polishchuk and use metal material for the gate electrode as taught by Chen. The motivation would have been to use a highly conductive material to decrease resistance.

Regarding claim 7, Polishchuk in view of Chen discloses the memory device of claim 6.
Polishchuk fails to explicitly disclose wherein the blocking dielectric comprises a high K dielectric.
However, Chen, in the related filed of forming field effect transistors (Para. [0025] "FinFET"; Fig. 2c), teaches a gate electrode formed over a high K dielectric (Para. [0046]).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the blocking dielectric of Polishchuk and use a high K dielectric material as taught by Chen. The motivation would have been to use a highly insulative material to increase gate capacitance without current leakage as the transistor decreases in size.

Claims 9-12 and 14 lack an inventive step under PCT Article 33(3) as being obvious over Polishchuk in view of Chen and Jenne et al. (hereafter Jenne).

Regarding claim 9, Polishchuk discloses a memory device (Fig. 3, 304 "non-volatile memory transistor") comprising:
an electrically conducting channel (Fig. 3, 312 "channel region") formed from a semiconducting material (substrate 306 is made of silicon; Col. 8, line 47) overlying a surface on a substrate (306) connecting a source and a drain (314 "source and drain (S/D) regions") of the memory device; and
a gate (Fig. 3) abutting the channel, the gate comprising:
a tunnel oxide layer (316 "tunnel oxide"; Col. 8, line 53) overlying the channel; and
a multi-layer charge storing layer (318A and 318B; Col. 8, lines 53-54) including a first oxynitride layer (318B; Col. 2, lines 38-46 "bottom oxynitride layer ") closer to the tunnel oxide layer, and a second oxynitride layer (318A; Col. 2, lines 38-46 "top oxynitride layer").
Polishchuk fails to explicitly disclose a gate having multiple surfaces abutting the channel.
However, Chen, in the related filed of forming field effect transistors (Para. [0025] "FinFET"; Fig. 2c), teaches a memory device comprising a non-planar transistor (Fig. 2c) including a gate (G) having multiple surfaces (the gate is contacting the top and side surfaces of the channel) abutting a channel (note that the channel is under the gate electrode (G) and between the source (S) and drain (D) regions).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the transistor structure of Polishchuk and incorporate a non-planar transistor including a gate having multiple surfaces abutting the channel as taught by Chen. The motivation would have been form a rounded channel so that the gate electrode can gain significant influence on the channel potential, therefore improving suppression of short-channel effects as taught by Chen (Paras. [0005]-[0007]).
Polishchuk fails to explicitly disclose wherein the first oxynitride layer is separated from the second oxynitride layer by an anti-tunneling layer comprising an oxide.
However, Jenne, in the related field of forming a SONOS-type dielectric (Abstract), teaches a first oxynitride layer (Fig. 2B, 206e; Col. 5, lines 37-47; note that layers 206a-e are the nitride in the SONOS stack and that Col. 4, lines 28-35 discloses that the nitride can be "silicon oxynitride") separated from a second oxynitride layer (212b) by an anti-tunneling layer comprising an oxide (212a; note that silicon oxynitride is an oxide; also note that a charge trapping layer is an anti-tunneling layer).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the charge storing layers of Polishchuk and separate the first oxynitride layer from the second oxynitride layer by an anti-tunneling layer comprising oxide as taught by Jenne. The motivation for forming a multilayered charge storing layer containing multiple charge trapping layers would have been to trap charge that may tunnel through the lower charge trapping layer, thereby retaining charge with a multilayered charge storing layer as taught by Jenne (Col. 5, lines 1-12).

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/032339

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Regarding claim 10, Polishchuk in view of Chen and Jenne discloses the memory device of claim 9.
Polishchuk fails to explicitly disclose wherein the channel comprises a silicon nanowire.
However, Chen, in the related filed of forming field effect transistors (Para. [0025] "FinFET"; Fig. 2c), teaches using a silicon nanowire (Para. [0025] "nano-wire FinFET" and Para. [0036] "a rounded semiconductor nano-wire may be formed from the semiconductor layer" and "such as silicon") as the channel (see Fig. 2c; note that the channel is under the gate electrode and between the source and drain regions).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the channel of Polishchuk and use a silicon nanowire as the channel as taught by Chen. The motivation would have been form a rounded channel so that the gate electrode can gain significant influence on the channel potential, therefore improving suppression of short-channel effects as taught by Chen (Paras. [0005]-[0007]).

Regarding claim 11, Polishchuk in view of Chen and Jenne discloses the memory device of claim 9. Polishchuk further discloses wherein the gate further comprises a blocking dielectric (Fig. 3, 320 "top of blocking oxide layer"; Col. 8, line 54) overlying the multi-layer charge storing layer (318A and 318B), and a gate layer (308 "gate electrode"; Col. 8, line 48) overlying the blocking dielectric layer.
Polishchuk fails to explicitly disclose wherein the device comprises a finFET.
However, Chen, in the related filed of forming field effect transistors (Para. [0025] "FinFET"; Fig. 2c), teaches a memory device comprising a finFET (Fig. 2c).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the transistor structure of Polishchuk and incorporate a finFET structure as taught by Chen. The motivation for forming a finFET would have been to wrap a gate electrode around a rounded channel so that the gate electrode can gain significant influence on the channel potential, therefore improving suppression of short-channel effects as taught by Chen (Paras. [0005]-[0007]).
Polishchuck fails to explicitly disclose wherein the gate electrode is metal (Polishchuk discloses a polysilicon gate electrode).
However, Chen, in the related filed of forming field effect transistors (Para. [0025] "FinFET"; Fig. 2c), teaches a gate electrode formed of metal (Para. [0047] "gate electrode material may be...metal material").
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the gate electrode material of Polishchuk and use metal material for the gate electrode as taught by Chen. The motivation would have been to use a highly conductive material to decrease resistance.

Regarding claim 12, Polishchuk in view of Chen and Jenne discloses the memory device of claim 11.
Polishchuk fails to explicitly disclose wherein the blocking dielectric comprises a high K dielectric.
However, Chen, in the related filed of forming field effect transistors (Para. [0025] "FinFET"; Fig. 2c), teaches a gate electrode formed over a high K dielectric (Para. [0046]).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the blocking dielectric of Polishchuk and use a high K dielectric material as taught by Chen. The motivation would have been to use a highly insulative material to increase gate capacitance without current leakage as the transistor decreases in size.

Regarding claim 14, Polishchuk in view of in view of Chen and Jenne discloses the memory device of claim 9. Polishchuk further discloses wherein the first oxynitride layer (Fig. 3, 318B) is a substantially trap free, oxygen-rich, oxynitride layer (Col. 2, lines 38-46 "bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer" and "substantially trap free bottom oxynitride layer"; also see Col. 8, lines 55-58), and the second oxynitride layer (318A) is a trap dense, oxygen-lean, oxynitride layer (Col. 2, lines 38-46 "top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer" and "charge trapping top oxynitride layer"; also see Col. 8, lines 55-58) further comprising a concentration of carbon selected to increase a number of traps therein (Col. 3, lines 42-47 "increase a concentration of carbon and thereby the number of traps therein").

Claim 13 lacks an inventive step under PCT Article 33(3) as being obvious over Polishchuk in view of Chen and Jenne and further in view of Ramkumar.

Regarding claim 13, Polishchuk in view of Chen and Jenne discloses the memory device of claim 9.
Polishchuk fails to explicitly disclose wherein the anti-tunneling layer comprises a portion of the first oxynitride layer that has been oxidized by radical oxidation.
However, Ramkumar, in the related field of forming a charge trap memory device (Abstract), teaches forming a dielectric by exposing a portion of a charge trapping layer to a radical oxidation process (Para. [0041]).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of forming the anti-tunneling layer of Polishchuk and form the anti-tunneling layer from a portion of the first oxynitride layer by radical oxidation as taught by Ramkumar. The motivation to use radical oxidation would have been to provide higher quality films than films formed from wet growth processes as taught by Ramkumar (Para. [0037]).

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/032339

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Claims 15, 16, 18 and 20 lack an inventive step under PCT Article 33(3) as being obvious over Polishchuk in view of Singh et al. (hereafter Singh).

Regarding claim 15, Polishchuk discloses a memory device (Fig. 3, 304 "non-volatile memory transistor") comprising:
a channel (Fig. 3, 312 "channel region") formed from semiconducting material (substrate 306 is made of silicon; Col. 8, line 47) extending from a first diffusion region to a second diffusion region (314 "source and drain (S/D) regions"), the channel electrically connecting the first diffusion region to the second diffusion region;
a tunnel oxide layer (316 "tunnel oxide"; Col. 8, line 53) abutting the channel; and
a multi-layer charge storing layer (318A and 318B; Col. 8, lines 53-54) abutting the tunnel oxide layer, the multi-layer charge storing layer including a first oxynitride layer (318B) comprising an oxygen-rich nitride (Col. 2, lines 38-46 "bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer") closer to the tunnel oxide layer, and a second oxynitride layer (318A) comprising a silicon-rich, oxygen-lean nitride (Col. 2, lines 38-46 "top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer") overlying the first oxynitride layer, wherein the second charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region (Col. 2, lines 38-46 "charge trapping top oxynitride layer"; also see Col. 8, lines 55-58).
Polishchuk fails to explicitly disclose wherein the channel is a vertical channel formed from a thin projection of semiconducting material extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate.
However, Singh, in the related field of forming a transistor (Abstract; Fig. 6), teaches a vertical channel (608 "channel region"; Para. [0129]) formed from a thin projection of semiconducting material (606 "nanowire structure"; Para. [0129] "vertical nanowire structure 606 being made of the same material as the carrier 602", which may be silicon) extending from a first diffusion region (614a; Para. [0131]) formed on a surface on a substrate (602) to a second diffusion region (614b) formed over the surface of the substrate.
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the channel structure of Polishchuk and form a vertical channel from a thin projection of semiconducting material extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate as taught by Singh. The motivation would have been first to provide a gate-all-around structure to resist short channel effects and second to use a vertical wire device since they are more suitable than lateral devices for providing gate uniformity and wire shape control as taught by Singh (Paras. [0006]-[0007]).

Regarding claim 16, Polishchuk in view of Singh discloses the memory device of claim 15.
Polishchuk fails to explicitly disclose wherein the channel comprises a silicon nanowire.
However, Singh, in the related field of forming a transistor (Abstract; Fig. 6), teaches a vertical channel (608 "channel region"; Para. [0129]) formed from a silicon nanowire (606 "nanowire structure"; Para. [0129] "vertical nanowire structure 606 being made of the same material as the carrier 602", which may be silicon).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the channel structure of Polishchuk and form a vertical channel from a silicon nanowire as taught by Singh. The motivation would have been first to provide a gate-all-around structure to resist short channel effects and second to use a vertical nanowire device since they are more suitable than lateral devices for providing gate uniformity and wire shape control as taught by Singh (Paras. [0006]-[0007]).

Regarding claim 18, Polishchuk in view of Singh discloses the memory device of claim 16. Polishchuk further discloses a blocking dielectric (Fig. 3, 320 "top of blocking oxide layer"; Col. 8, line 54) overlying the multi-layer charge storing layer (318A and 318B).
Polishchuk fails to explicitly disclose wherein the blocking dielectric comprises a high K dielectric.
However, Singh, in the related filed of forming a transistor (Abstract), teaches a gate electrode formed over a high K dielectric (Paras. [0060] and [0085]).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the blocking dielectric of Polishchuk and use a high K dielectric material as taught by Singh. The motivation would have been to use a highly insulative material to increase gate capacitance without current leakage as the transistor decreases in size.

Regarding claim 20, Polishchuk in view of Singh discloses the structure of claim 15. Polishchuk further discloses wherein the second oxynitride layer further comprises a concentration of carbon selected to increase a number of traps therein (Col. 3, lines 42-47 "increase a concentration of carbon and thereby the number of traps therein").

Claims 17 and 19 lack an inventive step under PCT Article 33(3) as being obvious over Polishchuk in view of Singh and further in view of Jenne.

Regarding claim 17, Polishchuk in view of Singh discloses the memory device of claim 16.
Polishchuk fails to explicitly disclose wherein the wherein the multi-layer charge storing layer further comprises an oxide anti-tunneling layer separating the first oxynitride layer from the second oxynitride layer.
However, Jenne, in the related field of forming a SONOS-type dielectric (Abstract), teaches a multi-layer charge storing layer (Fig. 2B, note that layers 206a-e are the nitride in the SONOS stack, Col. 5, lines 37-47, and that Col. 4, lines 28-35 discloses that the nitride can be "silicon oxynitride") comprising a first oxynitride layer (206e) separated from a second oxynitride layer (212b) by an anti-tunneling layer comprising an oxide (212a; note that silicon oxynitride is an oxide; also note that a charge trapping layer is an anti-tunneling layer).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the charge storing layers of Polishchuk and separate the first oxynitride layer from the second oxynitride layer by an anti-tunneling layer comprising oxide in the multi-layer charge storing layer as taught by Jenne. The motivation for forming a multilayered charge storing layer containing multiple charge trapping layers would have been to trap charge that may tunnel through the lower charge trapping layer, thereby retaining charge with a multilayered charge storing layer as taught by Jenne (Col. 5, lines 1-12).

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/032339

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Regarding claim 19, Polishchuk in view of Singh discloses the memory device of claim 18.
Polishchuk fails to explicitly disclose wherein the wherein the multi-layer charge storing layer further comprises an oxide anti-tunneling layer separating the first oxynitride layer from the second oxynitride layer.
However, Jenne, in the related field of forming a SONOS-type dielectric (Abstract), teaches a multi-layer charge storing layer (Fig. 2B, note that layers 206a-e are the nitride in the SONOS stack, Col. 5, lines 37-47, and that Col. 4, lines 28-35 discloses that the nitride can be "silicon oxynitride") comprising a first oxynitride layer (206e) separated from a second oxynitride layer (212b) by an anti-tunneling layer comprising an oxide (212a; note that silicon oxynitride is an oxide; also note that a charge trapping layer is an anti-tunneling layer).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the charge storing layers of Polishchuk and separate the first oxynitride layer from the second oxynitride layer by an oxide anti-tunneling layer in the multi-layer charge storing layer as taught by Jenne. The motivation for forming a multilayered charge storing layer containing multiple charge trapping layers would have been to trap charge that may tunnel through the lower charge trapping layer, thereby retaining charge with a multilayered charge storing layer as taught by Jenne (Col. 5, lines 1-12).

Claims 1-20 meet the criteria set out in PCT Article 33(4) and thus have industrial applicability because the subject matter claimed can be made or used in industry.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709
USA

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Applicant's or agent's file reference PM07024CIPWO	Date of mailing (*day/month/year*) 26 JUL 2013 **FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/US13/48876	01 July 2013 (01.07.2013)	01 July 2012 (01.07.2012)

International Patent Classification (IPC) or both national classification and IPC

IPC: **H01L 21/316**(2006.01),**21/336**(2006.01),**21/318**(2006.01)
USPC: 438/269,762;257/E21.285,E21.292,E21.401,E21.423

Applicant

CYRPRESS SIMICONDUCTOR CORPORATION

1. This opinion contains indications relating to the following items:

- ☒ Box No. I — Basis of the opinion
- ☐ Box No. II — Priority
- ☐ Box No. III — Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV — Lack of unity of invention
- ☒ Box No. V — Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI — Certain documents cited
- ☐ Box No. VII — Certain defects in the international application
- ☐ Box No. VIII — Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(*b*) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/ US	Date of completion of this opinion	Authorized officer
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	19 July 2013 (19.07.2013)	Brian Sircus Telephone No. 571-272-2058

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY	International application No. PCT/US13/48876

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

☒ the international application in the language in which it was filed

☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

a. type of material

☐ a sequence listing

☐ table(s) related to the sequence listing

b. format of material

☐ on paper

☐ in electronic form

c. time of filing/furnishing

☐ contained in the international application as filed.

☐ filed together with the international application in electronic form.

☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY	International application No. PCT/US13/48876

Box No. V Reasoned statement under Rule 43 *bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims 1-20	YES
	Claims NONE	NO
Inventive step (IS)	Claims 1-20	YES
	Claims NONE	NO
Industrial applicability (IA)	Claims 1-20	YES
	Claims NONE	NO

2. Citations and explanations:

Claims 1-20 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the claimed invention.

Claims 1-20 meet the criteria set out in PCT Article 33(4), and thus meet the criteria for industrial applicability because the subject matter claimed can be made or used in industry.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	08 MAY 2012
Applicant's or agent's file reference PM07002CIP1WO	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 12/21583	17 January 2012 (17.01.2012)	14 January 2011 (14.01.2011)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H01L 29/792; H01L 21/336 (2012.01)
USPC - 257/324; 257/E21.209; 257/E29.309; 438/257

Applicant CYPRESS SEMICONDUCTOR CORPORATION

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1 *bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	24 April 2012 (24.04.2012)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 12/21583

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

   ☐ on paper

   ☐ in electronic form

   b. (time)

   ☐ in the international application as filed

   ☐ together with the international application in electronic form

   ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 12/21583

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	2-5, 7-10, 13-15, 17, 20-23	YES
	Claims	1, 6, 11, 12, 16, 18, 19	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-23	NO
Industrial applicability (IA)	Claims	1-23	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1, 6, 11, 12, 16, 18, and 19 lack novelty under PCT Article 33(2) as being anticipated by US 2009/0179253 A1 to Levy et al. (hereinafter Levy).

Regarding claims 1, 6, and 11, Levy discloses a method of forming a semiconductor device including a silicon-oxide-oxynitride-oxide-silicon structure (Fig. 2) comprising:
-substrate comprising silicon (208) and having a surface (206) with laterally spaced-apart source and drain regions (210) (para [0021]);
-a tunnel oxide layer (216) on the surface of the substrate overlying the source and drain regions (para [0023]);
-a multi-layer charge storing layer on the tunnel oxide layer and disposed laterally between the spaced-apart source and drain regions, the multi-layer charge storing layer including an oxygen-rich first oxynitride layer (220B) in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean second oxynitride layer (220A) in which a stoichiometric composition of the second oxynitride layer results in it being trap dense (para [0021], [0024]-[0026]);
-a blocking oxide layer (218) on the second oxynitride layer (para [0021]); and
-a silicon containing gate layer on the blocking oxide layer. (para [0034]).

Regarding claim 12, Levy further discloses the method of claim 11, wherein the stoichiometric composition of the first oxynitride layer comprises a concentration of oxygen selected to increase a retention performance of the multi-layer charge storing layer by acting as a barrier between charge trapped in the second oxynitride layer and the substrate. (para [0018] and [0025]).

Regarding claim 16, Levy further discloses the method of claim 12, wherein the retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years. (para [0036]).

Regarding claim 18, Levy further discloses the method of claim 11, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2Cl2)/ammonia (NH3) mixture at a ratio in a range of about 5:1 to 15:1 and a nitrous oxide (N2O)/NH3 mixture at a ratio in a range of about 2:1 to 4:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N2O/NH3 mixture at a ratio in a range of about 1:6 to 1:8 and a SiH2Cl2/NH3 mixture at a ratio in a range of about 1.5: 1 to 3: 1. (para [0025]-[0026]).

Regarding claim 19, Levy further discloses the method of claim 18, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N2O/NH3 and SiH2Cl2/NH3 mixtures. (para [0027]).

Claims 2-5, 7-10, 13-15, 17, 20, and 22 lack an inventive step under PCT Article 33(3) as being obvious over Levy.

Regarding claims 2, 3, 7, 8, and 13-15, Levy does not expressly teach wherein a concentration of oxygen in the first oxynitride layer is from about 15% to about 40% and wherein a concentration of oxygen in the second oxynitride layer is less than about 5%. However, Levy does teach optimizing the oxygen levels in both oxynitride layers (see para [0018]), thereby rendering the recited levels obvious to a skilled artisan through routine experimentation.

Regarding claims 4, 5, 9, 10, 17, and 22, Levy does not expressly each wherein the second oxynitride layer comprises a carbon concentration that increases the number of traps so that the charge trap density is at least 1000 times greater than the first oxynitride layer. However, Levy does teach optimizing the concentration of constituents within the oxynitride layers in order to reduce stored charge loss (see para [0018]). Thus, a skilled artisan would have found these limitations obvious based upon routine experimentation.

Regarding claim 20, Levy further discloses the method of claim 11, wherein the tunnel oxide layer is grown in an ISSG (InSituSteam Generation) chamber with a radical oxidation using a reaction between oxygen (O2) and hydrogen (H2) on the substrate. (para [0023] and [0028]). Levy does not expressly teach temperatures of at least 1000.C, but a skilled artisan would have found the recited temperature obvious based upon routine experimentation.

---------- See Supplemental Box ----------

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 12/21583

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
V.2 Citations and Explanations;

Claims 21 and 23 lack an inventive step under PCT Article 33(3) as being obvious over Levy in view of US 6,153,543 A to Chesire et al. (hereinafter Chesire).

Regarding claim 21, Levy teaches the method of claim 11 including a blocking oxide layer, but does not expressly teach the further claim limitation taught by Chesire of wherein said layer is formed by high density plasma (HDP) oxidation of a portion of the second oxynitride layer (see col 5, ln 5-40). It would have been obvious to a skilled artisan to utilize HDP oxidation to form the blocking oxide layer in order to provide a smooth layer with an optimal aspect ratio.

Regarding claim 23, Levy further teaches wherein the second oxynitride layer is formed in a CVD process using a process gas comprising Bis-TertiaryButylAminoSilane (BTBAS) and ammonia (NH3) mixed at a ratio of from about 7: 1 to about 1:7. (para [0024] and [0026]).

Claims 1-23 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
United States of America

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	14 NOV 2013
Applicant's or agent's file reference PM727D1CIPWO	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US13/48885	01 July 2013 (01.07.2013)	01 July 2012 (01.07.2012)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H01L 29/792 (2013.01)
USPC - 438/591; 257/324, E29.308

Applicant Cypress Semiconductor Corporation

1. This opinion contains indications relating to the following items:

- [X] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [X] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1 *bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	21 October 2013 (21.10.2013)	Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US13/48885

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US13/48885

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	NONE	NO

2. Citations and explanations:

Claims 1, 10, and 11 lack an inventive step under PCT Article 33(3) as being obvious over US 2011/0248332 A1 to Levy et al. (hereinafter Levy) in view of US 7,999,295 B2 to Lai et al. (Hereinafter "Lai").

As to claim 1, Levy discloses a semiconductor device (semiconductor device, Abstract) comprising: a memory transistor (memory transistor, paragraph [0019]) including a channel region electrically connecting a source region and a drain region formed in a substrate (The channel (212) connects the source and drain electrodes (210), Figure 2, paragraph [0025]); an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer (tunneling oxide layer (216), oxygen rich silicon oxynitride bottom charge-trapping layer (220B), oxygen lean nitride rich silicon oxynitride top charge-trapping layer (220A) and top oxide layer (218) together form the oxide-nitride-nitride-oxide stack on the channel (212), Figure 2, paragraphs [0022], [0025]); and a high work function gate electrode formed over a surface of the ONNO stack (polysilicon gate layer (214) (high work function gate) is formed on top of the multi-layered charge storage stack (204), Figure 2, paragraph [0025]). But, Levy does not disclose the channel region comprising polysilicon. However, Lai discloses a memory device (Abstract), wherein the channel region comprising polysilicon (The channel (204) is polysilicon, column 3 line 60 to column 4, line 7). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Levy in view of the polysilicon channel disclosed by Lai as it had advantageously enabled the formation of a memory device with less process complexity like recrystallization.

As to claim 10, Levy in view of Lai disclose the semiconductor device of claim 1, but Levy does not disclose wherein the multi-layer charge trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer. However, Lai discloses a memory device (Abstract), wherein the multi-layer chargetrapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer (The first and second nitride layers (286, 290) are the bottom and top charge trapping layers that are separated by an oxide layer (288), Figure 18C, column 6, lines 48 – 65, column 7, lines 20 - 34). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Levy with the anti-tunneling layer disclosed by Lai as it had advantageously enabled the formation of raised channel non-volatile memory for charge storage leading to decreased substrate effects on the memory performance.

As to claim 11, Levy discloses a semiconductor device (semiconductor device, Abstract) comprising: a memory transistor (memory transistor, paragraph [0019]) including: a channel region electrically connecting a source region and a drain region formed in a substrate (The channel (212) connects the source and drain electrodes (210), Figure 2, paragraph [0025]); an oxide-nitride-nitride-oxide (ONONO) stack disposed above the channel region, the ONONO stack comprising: a tunnel dielectric layer disposed above the channel region; a multi-layer charge-trapping region including an oxygen-rich first nitride layer disposed above the tunnel dielectric layer, an oxygen-lean second nitride layer disposed above the first nitride layer (tunneling oxide layer (216), oxygen rich silicon oxynitride bottom charge-trapping layer (220B), oxygen lean nitride rich silicon oxynitride top charge-trapping layer (220A) and top oxide layer (218) together form the oxide-nitride-nitride-oxide stack on the channel (212), Figure 2, paragraphs [0022], [0025]); and a blocking dielectric layer disposed above the multi-layer charge trapping region (top blocking oxide layer (218) is formed over multi-layer charge trapping stack (204), Figure 2, paragraph [0025]); and a high work function gate electrode disposed above a surface of the ONONO stack (polysilicon gate layer (214) (high work function gate) is formed on top of the multi-layered charge storage stack (204), Figure 2, paragraph [0025]). But, Levy does not disclose the channel region comprising polysilicon; and an antitunneling layer comprising an oxide separating the first nitride layer from the second nitride layer. However, Lai discloses a memory device (Abstract), wherein the channel region comprising polysilicon (The channel (204) is polysilicon, column 3 line 60 to column 4, line 7); and an antitunneling layer comprising an oxide separating the first nitride layer from the second nitride layer (The first and second nitride layers (286, 290) are the bottom and top charge trapping layers that are separated by an oxide layer (288), Figure 18C, column 6, lines 48 – 65, column 7, lines 20 - 34). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Levy with the polysilicon channel and anti-tunneling layer disclosed by Lai as it had advantageously enabled the formation of raised channel non-volatile memory for charge storage leading to decreased substrate effects on the memory performance.

-***-Continued Within the Next Supplemental Box-***-

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US13/48885

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

-***-Continued from Previous Supplemental Box-***-

Claim 18 lacks an inventive step under PCT Article 33(3) as being obvious over Lin in view of Levy.

As to claim 18, Lin discloses a semiconductor device (A non-volatile memory device, Abstract) comprising: a memory transistor (non-volatile memory FET, Abstract, column 3, lines 63 - 67) including: a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region (The silicon channel (190) projects above the surface of the substrate (100& 110) in the vertical direction and electrically interconnects the source and drain regions (170, 180) that are ion implanted in the first region, Figures 1A – 1H, column 2, line 63 to column 3, line 45); a charge trapping dielectric stack disposed about the vertical channel (fin comprising the tunnel oxide (150) and the split charge trapping region (200) above the tunnel oxide (150) overlap the channel (190), Figures 1A – 1H, column 2, line 63 to column 3, line 45). But, Lin does not disclose the charge trapping dielectric stack comprising an oxide-nitride-nitride-oxide (ONNO) stack, the ONNO stack comprising: a tunnel dielectric layer abutting the vertical channel; a multi-layer charge-trapping region including a first nitride layer comprising an oxygen-rich nitride abutting the tunnel dielectric layer, and a second nitride layer comprising a silicon-rich, oxygen-lean nitride overlying the first nitride layer; and a blocking dielectric layer overlying the multi-layer charge-trapping region; and a high work function gate electrode disposed about the ONONO stack, abutting the blocking dielectric layer. However, Levy discloses a semiconductor device (semiconductor device, Abstract), wherein the charge trapping dielectric stack comprising an oxide-nitride-nitride-oxide (ONNO) stack, the ONNO stack comprising: a tunnel dielectric layer abutting the channel; a multi-layer charge-trapping region including a first nitride layer comprising an oxygen-rich nitride abutting the tunnel dielectric layer, and a second nitride layer comprising a silicon-rich, oxygen-lean nitride overlying the first nitride layer (tunneling oxide layer (216), oxygen rich silicon oxynitride bottom charge-trapping layer (220B), oxygen lean nitride rich silicon oxynitride top charge-trapping layer (220A) and top oxide layer (218) together form the oxide-nitride-nitride-oxide stack on the channel (212), Figure 2, paragraphs [0022], [0025]); and a blocking dielectric layer overlying the multi-layer charge-trapping region (top blocking oxide layer (218) is formed over multi-layer charge trapping stack (204), Figure 2, paragraph [0025]); and a high work function gate electrode disposed about the ONONO stack, abutting the blocking dielectric layer (polysilicon gate layer (214) (high work function gate) is formed on top of the multi-layered charge storage stack (204) adjacent the blocking oxide layer (218), Figure 2, paragraph [0025]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the semiconductor device disclosed by Lin in view of the multilayered charge trapping stack layer disclosed by Levy as it had advantageously enabled the formation of raised channel non-volatile memory for charge storage leading to decreased substrate effects on the memory performance.

Claims 2, 3, 12, and 15 lack an inventive step under PCT Article 33(3) as being obvious over Levy in view of Lai further in view of US 7,723,789 B2 to Lin et al. (Hereinafter "Lin").

As to claim 2, Levy in view of Lai disclose the semiconductor device of claim 1, but, Levy does not disclose wherein the channel comprises a silicon nanowire. However, Lin discloses a memory (Abstract), wherein the channel comprises a silicon nanowire (The channel is recrystallized polysilicon based nanowire, column 3, lines 33-35, column 4, lines 1-5). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Levy in view of the silicon nanowire channel disclosed by Lin as it had advantageously enabled the formation of a transistor with reduced dimensions.

As to claim 3, Levy in view of Lai disclose the semiconductor device of claim 1, but, Levy does not disclose wherein the channel comprises recrystallized polysilicon. However, Lin discloses a memory (Abstract), wherein the channel comprises recrystallized polysilicon (The channel is recrystallized polysilicon based nanowire, column 3, lines 33-35, column 4, lines 1-5). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Levy in view of the recrystallized polysilicon disclosed by Lin as it had advantageously enabled the formation a crystalline silicon channel at reduced temperatures.

As to claim 12, Levy in view of Lai disclose the semiconductor device of claim 11, but, Levy does not disclose wherein the channel region comprises recrystallized polysilicon. However, Lin discloses a memory (Abstract), wherein the channel comprises a silicon nanowire (The channel is recrystallized polysilicon based nanowire, column 3, lines 33-35, column 4, lines 1-5). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Levy in view of the silicon nanowire channel disclosed by Lin as it had advantageously enabled the formation of a transistor with reduced dimensions.

As to claim 15, Levy in view of Lai disclose the semiconductor device of claim 11, but, Levy does not disclose wherein the channel comprises a silicon nanowire. However, Lin discloses a memory (Abstract), wherein the channel comprises a silicon nanowire (The channel is recrystallized polysilicon based nanowire, column 3, lines 33-35, column 4, lines 1-5). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Levy in view of the silicon nanowire channel disclosed by Lin as it had advantageously enabled the formation of a transistor with reduced dimensions.

-***-Continued Within the Next Supplemental Box-***-

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US13/48885

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

-***-Continued from Previous Supplemental Box-***-

Claims 6-9 and 17 lack an inventive step under PCT Article 33(3) as being obvious over Levy in view of Lai further in view of US 2008/0293207 A1 to Koutny, Jr.et al. (Hereinafter "Koutny Jr").

As to claim 6, Levy in view Lai disclose the semiconductor device of claim 1, but, Levy does not disclose further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode. However, Koutny Jr discloses a method of forming a semiconductor device (Abstract), further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate (MOS logic transistor (370) is fabricated on the second region of the substrate, Figure 5, Abstract), wherein the MOS logic transistor comprises a gate oxide (gate insulator (320) of the MOS logic transistor (370), Figure 3E, paragraph [0074]) and a high work function gate electrode (A P-polysilicon gate layer (330) (high work function gate) is deposited over the gate insulator (320) and patterned to form the gate electrode (378) over the MOS transistor (370), Figure 3G, 3H, paragraphs [0082] - [0084]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the semiconductor device disclosed by Levy in view of the MOS logic transistor disclosed by Koutney Jr as it had advantageously enabled the integration of devices with diverse functionality, thereby enhancing, low power operations.

As to claim 7, Levy in view of Lai further in view of Koutny Jr disclose the semiconductor device of claim 6, but, Levy does not disclose wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a N+ doped polysilicon layer to form an P-type (PMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a N-type (NMOS) logic transistor. However, Koutny Jr discloses a method of forming a semiconductor device (Abstract), wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a N+ doped polysilicon layer to form an P-type (PMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor (the gate layer (330) can be N+doped polysilicon for forming a PMOS SONOS memory transistor (300), Figures 3G, 3H, paragraphs [0046], [0083]) and a N-type (NMOS) logic transistor (the gate layer (330) is dual doped to form N+doped polysilicon over the gate insulator (320) to form NMOS transistor (370) (MOS logic transistor), Figures 3G, 3H, paragraph [0083]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the semiconductor device disclosed by Levy in view of the high work function electrode disclosed by Koutny Jr as it had advantageously enabled the formation of a memory transistor with enhanced charge retention properties.

As to claim 8, Levy in view of Lai further in view of Koutny Jr disclose the semiconductor device of claim 6, but, Levy does not disclose wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a P+ doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (NMOS) logic transistor. However, Koutny Jr discloses a method of forming a semiconductor device (Abstract), wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a P+ doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor (the gate layer (330) can be P+doped polysilicon for forming a NMOS SONOS memory transistor (300), Figures 3G, 3H, paragraph [0083]) and a P-type (NMOS) logic transistor (the gate layer (330) is dual doped to form P+doped polysilicon over the gate insulator (320) to form PMOS transistor (370) (MOS logic transistor), Figures 3G, 3H, paragraph [0083]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the semiconductor device disclosed by Levy in view of the high work function electrode disclosed by Koutny Jr as it had advantageously enabled the formation of a memory transistor with enhanced charge retention properties.

As to claim 9, Levy in view of Lai further in view of Koutny Jr disclose the semiconductor device of claim 6, but, Levy does not disclose wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor are formed from a single, patterned doped polysilicon layer. However, Koutny Jr discloses a method of forming a semiconductor device (Abstract), wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor are formed from a single, patterned doped polysilicon layer (A P-polysilicon gate layer (330) (high work function gate) is deposited over the dielectric stack (306) of the SONOS memory transistor (300) and MOS logic gate insulator (320) and patterned to form the gate electrode (308) for the SONOS memory transistor (300) and gate electrode (378) over the MOS transistor (370), Figure 3G, 3H, paragraphs [0082] - [0084]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the semiconductor device disclosed by Levy in view of the single doped polysilicon gate layer as disclosed by Koutny Jr as it had advantageously enabled the formation of gate electrodes by reducing processing steps.

As to claim 17, Levy in view of Lai disclose the semiconductor device of claim 11, but, Levy does not disclose further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode. However, Koutny Jr discloses a method of forming a semiconductor device (Abstract), further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate (MOS logic transistor (370) is fabricated on the second region of the substrate, Figure 5, Abstract), wherein the MOS logic transistor comprises a gate oxide (gate insulator (320) of the MOS logic transistor (370), Figure 3E, paragraph [0074]) and a high work function gate electrode (A P-polysilicon gate layer (330) (high work function gate) is deposited over the gate insulator (320) and patterned to form the gate electrode (378) over the MOS transistor (370), Figure 3G, 3H, paragraphs [0082] - [0084]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the semiconductor device disclosed by Levy in view of the MOS logic transistor disclosed by Koutney Jr as it had advantageously enabled the integration of devices with diverse functionality, thereby enhancing, low power operations.

-***-Continued Within the Next Supplemental Box-***-

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US13/48885

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
-***-Continued from Previous Supplemental Box-***-

Claim 16 lack an inventive step under PCT Article 33(3) as being obvious over Levy in view of Lai further in view of Lue.

As to claim 16, Levy in view of Lai disclose the semiconductor device of claim 11, Levy further discloses wherein the high work function gate electrode comprises a polysilicon layer (polysilicon gate layer (214) (high work function gate) is formed on top of the multi-layered charge storage stack (204), Figure 2, paragraph [0025]). But, Levy does not disclose P+ doped polysilicon layer. However, Lue discloses a charge trapping memory cell (Abstract), further comprising a P+ doped polysilicon layer (P+ polysilicon gate, paragraph [0064]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the high work function gate electrode disclosed by Levy in view of the P+ polysilicon disclosed by Lue as it had advantageously enabled the formation of a high conductivity gate electrode.

Claim 19 lacks an inventive step under PCT Article 33(3) as being obvious over Lin in view of Levy further in view of Koutny Jr.

As to claim 19, Lin in view of Levy disclose the semiconductor device of claim 18, but, Lin does not disclose further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode. However, Koutny Jr discloses a method of forming a semiconductor device (Abstract), further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate (MOS logic transistor (370) is fabricated on the second region of the substrate, Figure 5, Abstract), wherein the MOS logic transistor comprises a gate oxide (gate insulator (320) of the MOS logic transistor (370), Figure 3E, paragraph [0074]) and a high work function gate electrode (A P-polysilicon gate layer (330) (high work function gate) is deposited over the gate insulator (320) and patterned to form the gate electrode (378) over the MOS transistor (370), Figure 3G, 3H, paragraphs [0082] - [0084]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the semiconductor device disclosed by Lin in view of the MOS logic transistor disclosed by Koutney Jr as it had advantageously enabled the integration of devices with diverse functionality, thereby enhancing, low power operations.

Claim 20 lacks an inventive step under PCT Article 33(3) as being obvious over Lin in view of Levy further in view of Lai.

As to claim 20, Lin in view of Levy disclose the semiconductor device of claim 18, but, Lin does not disclose wherein the multi-layer chargetrapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer. However, Lai discloses a memory device (Abstract), wherein the multi-layer chargetrapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer (The first and second nitride layers (286, 290) are the bottom and top charge trapping layers that are separated by an oxide layer (288), Figure 18C, column 6, lines 48 – 65, column 7, lines 20 - 34). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Lin with the anti-tunneling layer disclosed by Lai as it had advantageously enabled the formation of raised channel non-volatile memory for charge storage leading to decreased substrate effects on the memory performance.

Claims 4, 5, 13, and 14 lack an inventive step under PCT Article 33(3) as being obvious over Levy in view of Lai further in view of Lin further in view of US 2009/0039414 A1 to Lue et al. (Hereinafter "Lue").

As to claim 4, Levy in view of Lai further in view of Lin disclose the semiconductor device of claim 3, Levy further discloses the high work function gate electrode comprises a polysilicon layer (polysilicon gate layer (214) (high work function gate) is formed on top of the multi-layered charge storage stack (204), Figure 2, paragraph [0025]). But, Levy does not disclose P+ doped polysilicon layer. However, Lue discloses a charge trapping memory cell (Abstract), further comprising a P+ doped polysilicon layer (P+ polysilicon gate, paragraph [0064]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the high work function gate electrode disclosed by Levy in view of the P+ polysilicon disclosed by Lue as it had advantageously enabled the formation of a high conductivity gate electrode.

As to claim 5, Levy in view of Lai further in view of Lin and Lue disclose the semiconductor device of claim 4, Levy further discloses wherein the ONNO stack further includes a blocking dielectric layer disposed above the multi-layer charge-trapping region (The blocking oxide layer (218) is disposed on top of the multi-layer charge storing layer (204), Figure 2, paragraphs [0025], [0035]), and wherein the blocking dielectric layer comprises a dielectric comprises a high K High Temperature Oxide (HTO) (The blocking oxide layer (218) is a high temperature oxide and is disposed on top of the multi-layer charge storing layer (204), Figure 2, paragraphs [0025], [0035] Figure 2, paragraphs [0025], [0035]). But, Levy does not disclose the dielectric being high K oxide. However, Lue discloses a charge trapping memory cell (Abstract), wherein the blocking layer comprises a high K dielectric oxide (A high K dielectric constant blocking layer like aluminum oxide, Abstract). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Levy in view of the high K blocking layer disclosed by Lue as it had advantageously enabled the prevention of charge carrier tunneling leading to leading to improved memory retention.

-***-Continued Within the Next Supplemental Box-***-

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US13/48885

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
-***-Continued from Previous Supplemental Box-***-

As to claim 13, Levy in view of Lai further in view of Lin disclose the semiconductor device of claim 12, Levy further discloses wherein the high work function gate electrode comprises a polysilicon layer (polysilicon gate layer (214) (high work function gate) is formed on top of the multi-layered charge storage stack (204), Figure 2, paragraph [0025]). But, Levy does not disclose P+ doped polysilicon layer. However, Lue discloses a charge trapping memory cell (Abstract), further comprising a P+ doped polysilicon layer (P+ polysilicon gate, paragraph [0064]). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the high work function gate electrode disclosed by Levy in view of the P+ polysilicon disclosed by Lue as it had advantageously enabled the formation of a high conductivity gate electrode.

As to claim 14, Levy in view of Lai further in view of Lin and Lue disclose the semiconductor device of claim 13, Levy further discloses wherein the blocking dielectric layer comprises a dielectric comprises a high K High Temperature Oxide (HTO) (The blocking oxide layer (218) is a high temperature oxide and is disposed on top of the multi-layer charge storing layer (204), Figure 2, paragraphs [0025], [0035] Figure 2, paragraphs [0025], [0035]). But, Levy does not disclose the dielectric being high K oxide. However, Lue discloses a charge trapping memory cell (Abstract), wherein the blocking layer comprises a high K dielectric oxide (A high K dielectric constant blocking layer like aluminum oxide, Abstract). It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the memory device disclosed by Levy in view of the high K blocking layer disclosed by Lue as it had advantageously enabled the prevention of charge carrier tunneling leading to leading to improved memory retention.

Claims 1-20 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

SONOS Device With Tapered Bandgap Nitride Layer

Kuo-Hong Wu, Hua-Ching Chien, Chih-Chiang Chan, Tung-Sheng Chen, and Chin-Hsing Kao

Abstract—**A unique, band-engineered, configuration of the charge-trapping layer in silicon–oxide–nitride–oxide–silicon (SONOS) devices is proposed for high-density Flash memory applications. In this paper, a varying Si–N ratio in modified silicon nitride is obtained by controlling reaction gas flow-rate during deposition. This generates a graded composition profile from Si-rich at the bottom to N-rich at the top in a nitride film. The nonuniform composition profile of the silicon nitride layer corresponds to a tapered bandgap and results in significant improvement in device performance and reliability characteristics including operation window, cycling endurance and data retention. The dramatic improvement can be attributed to increased charge-trapping efficiency of the nitride layer since a significant number of highly accessible trapping levels are created in the tapered bandgap. In addition, the increased barrier height between the nitride and tunnel oxide layers also reduces back-tunneling probability and assists charge trapping. The SONOS device designed in this paper is suitable for next-generation Flash memory applications.**

Index Terms—**Endurance and retention, SONOS, tapered bandgap, trapping efficiency.**

I. Introduction

THE RAPIDLY increasing market for portable electronic products such as digital cameras, MP3 players, personal digital assistants (PDA), mobile phones, and external data storage devices for personal computers, has stimulated the development of nonvolatile memory profoundly. Among various nonvolatile memory architectures, Flash memory has out run other competitors due to its full process compatibility with CMOS technology and superior performance. However, conventional floating-gate structure will soon face a limit due to the aggressive scaling trend in the vertical dimension. As a result, the SONOS structure has become an appealing alternative for next-generation Flash memory applications due to its numerous advantages such as film scalability, process simplicity, power economy, operation versatility and radiation hardness [1]–[6]. Nevertheless, some performance and reliability issues such as insufficient charge-trapping efficiency, poor endurance, and short retention must be overcome before SONOS can be utilized in commercial production [7], [8]. In this paper, a promising bandgap-engineering technique using gradual variation of the Si–N ratio during nitride deposition is proposed and a tapered bandgap nitride in a SONOS device is formed [9]. The purpose of the graded composition profile is to adjust the nitride bandgap into a tapered shape so that the substrate-injected charges fall into shallow trapping levels and are transferred to adjacent deeper levels by lateral hopping. This increases the charge-trapping efficiency of the nitride layer. Furthermore, the increased barrier height between the nitride and the bottom tunnel oxide may help constrain the tunneled charges in the nitride and increase its charge-trapping probability. Significantly improved performance and reliability of SONOS devices is achieved.

Manuscript received July 1, 2004; revised February 7, 2005. This work was supported in part by the eMemory Company and in part by the National Nano Device Laboratory (NDL). The review of this paper was arranged by Editor R. Shrivastava.

K.-H. Wu is with the Army Communication Electronics Information School, Taoyuan 324, Taiwan, R.O.C.

H.-C. Chien is with the School of Defense Science, Chung-Cheng Institute of Technology, National Defense University, Taoyuan 335, Taiwan, R.O.C.

C.-C. Chan and T.-S. Chen are with the Department of Electric Engineering, Chung-Cheng Institute of Technology, National Defense University, Taoyuan 335, Taiwan, R.O.C.

C.-H. Kao is with the Department of Applied Physics, Chung-Cheng Institute of Technology, National Defense University, Taoyuan 335, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TED.2005.846347

II. Experimental

The preparation of test devices basically follows a standard nMOSFET process except that the gate oxide is replaced by an ONO structure and the key process steps for the dielectric layers are as follows. First, a bottom dielectric tunnel oxide (3 nm) was grown by diluted N_2O dry oxidation at 1 standard liter per minute (slm) gas flow rate at 800 °C. Then, the charge-trapping silicon nitride layer (5 nm) was formed in a low-pressure chemical vapor deposition (LPCVD) reactor under various process conditions at 780 °C. In order to manipulate the composition of the nitride layer, the SiH_2Cl_2–NH_3 gas flow-rate ratio was set differently for various film deposition conditions [10], [11]. The SiH_2Cl_2–NH_3 gas flow-rate ratio for standard nitride and uniform Si-rich nitride was maintained constant at 0.23 and 2.07 respectively. In the case of modified nitride, the deposition process was divided into five steps and the gas flow-rate ratio of SiH_2Cl_2–NH_3 was varied from 2.07 at the first step to 0.1 at the last step. The final composition profile of the tapered bandgap nitride film was thus silicon-rich at the bottom and nitrogen-rich at the top. Subsequent to nitride film deposition, a 4.5-nm-thick LPCVD tetraethylorthosilicate (TEOS) blocking oxide was deposited as a capping dielectric. Once the ONO structure was formed, $POCl_3$-doped polysilicon deposition, gate patterning, TEOS coverage, contact hole etching, S/D implant, and the rest of the process simply followed standard CMOS procedure. The final equivalent oxide thickness (EOT) of the ONO stack was 10.3-nm as determined by capacitance–voltage (C–V) characterization and confirmed by scanning electron microscopy (SEM) and high-resolution transmission electron microscopy (HRTEM).

For the sake of evaluating performance and reliability characteristics of all fabricated SONOS devices, an HP4156 high-precision semiconductor parameter analyzer was utilized as the main characterization tool. Essential Flash memory device parameters, such as program/erase (P/E) speed, operation window, cycling endurance and data retention, were examined and compared for different nitrides.

0018-9383/$20.00 © 2005 IEEE

Sandisk Technologies, Inc. - Ex. 1002, Page 000597

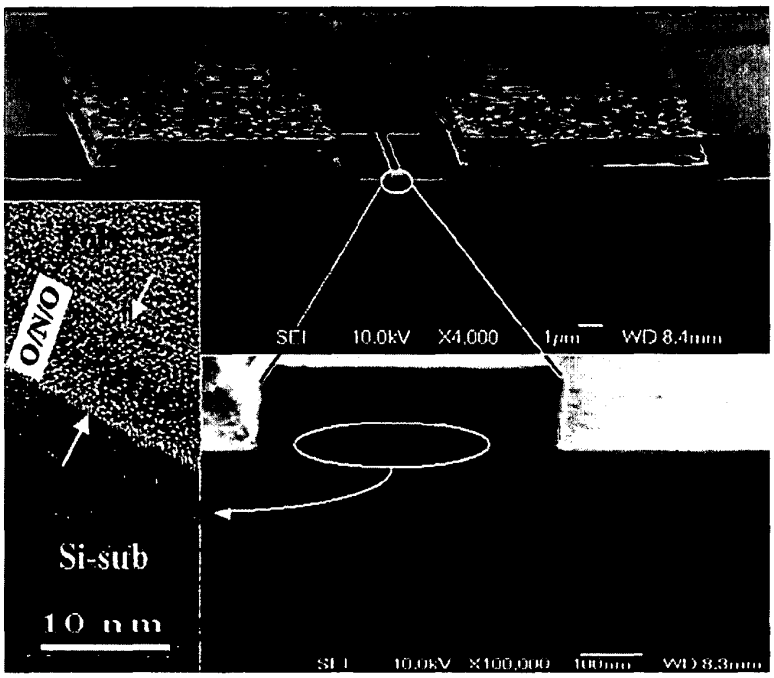


Fig. 1. Cross-sectional SEM and TEM micrographs of a SONOS device confirm the physical thickness of the ONO film.

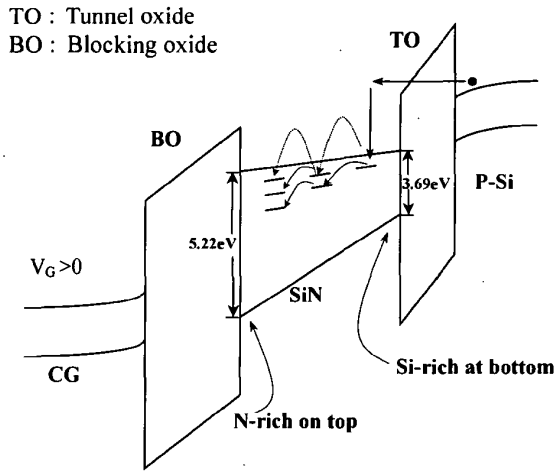


Fig. 2. Tapered bandgap of modified nitride in an ONO structure and the corresponding charge trapping mechanism.

III. Results and Discussion

Fig. 1 shows a cross-sectional SEM micrograph of a test device with tapered bandgap nitride and the physical thickness of each layer of the ONO film is confirmed with TEM analysis. The result of micrographic analysis is consistent with electrical *C–V* characterization. Fig. 2 illustrates the band diagram of a test device incorporating the proposed tapered bandgap nitride. As reported previously [12], [13], the Si–N content ratio determines the bandgap of nitride. A SONOS structure with a varying Si–N composition ratio corresponds to a tapered nitride bandgap and its function may be explained as follows. A gradually increasing bandgap from the bottom to the top of the nitride increases the accessibility of deep trapping levels and an increased nitride/oxide barrier height reduces back tunneling of injected charges. In standard nitride, shallow trapping levels catch incoming charges easily while deep trapping levels are buried underneath and may not be able to capture electrons easily. For uniform Si-rich nitride, the trapping levels are too shallow to trap electrons tightly and they are insufficient in number as well. Consequently, the modified nitride serves as a better solution that provides sufficient and accessible charge-trapping levels for efficient memory storage. As shown in Fig. 2, the substrate-injected charges are first caught by shallow trapping levels and then migrate to deeper trapping levels through lateral hopping. Thus, more trapping levels are available for charge storage. In addition, the increased barrier height between the nitride and the bottom tunnel oxide reduces the probability that injected charges leave trap states in the nitride and therefore increases the charge-trapping probability. Overall, the charge-trapping efficiency of tapered bandgap nitride is improved by its tapered bandgap.

The tapered bandgap is predicted in its design, but it would be highly desirable if the actual bandgap of the nitride could be measured. However, the very thin film thickness (5 nm) and nonuniform bandgap makes any direct measurement almost impossible. As an alternative, two uniform nitride films were grown separately. One is Si-rich ($SiH_2Cl_2/NH_3 = 2.07$) and the other is N-rich (SiH_2Cl_2–$NH_3 = 0.1$) using exactly the same gas flow-rate conditions as the first and the last steps in the tapered bandgap nitride. The optical bandgaps (E_g) of the two different nitride films were characterized by an N&K 1200 thin-film analyzer [14], [15]. The results indicate an Eg of 3.7

Sandisk Technologies, Inc. - Ex. 1002, Page 000598

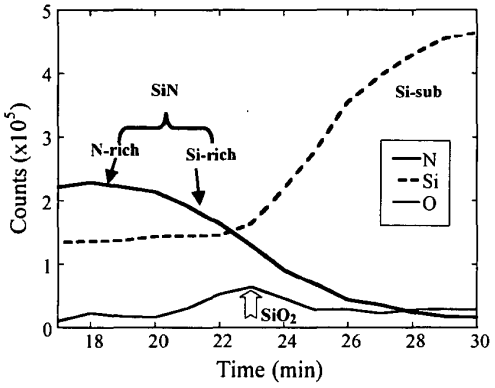


Fig. 3. Auger analysis of a thickened modified nitride in an ONO structure.

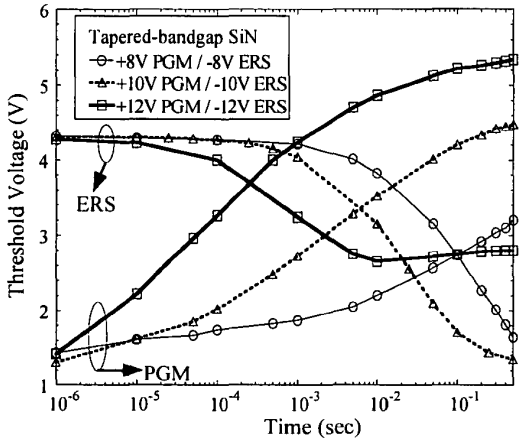


Fig. 4. P/E characteristics of test devices with tapered bandgap nitride under various bias conditions.

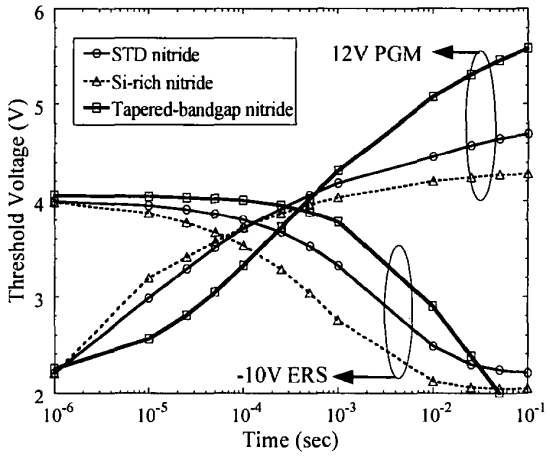


Fig. 5. Comparison of P/E speeds and operation windows for devices with three different nitride films.

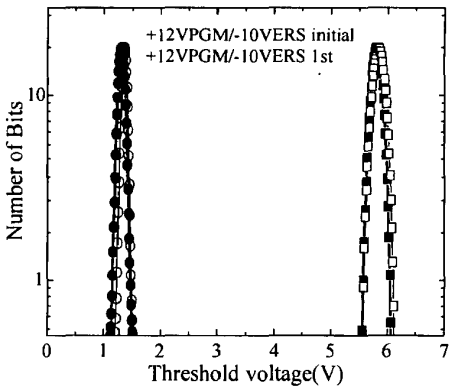


Fig. 6. V_T distribution of test devices initially and after the first P/E operation.

eV for Si-rich nitride and 5.2 eV for N-rich nitride respectively. Another way to probe the actual composition profile of tapered bandgap nitride is to perform an Auger analysis on a thicker sample of tapered bandgap nitride (50 nm thick) prepared by the same five-step gas flow-rate conditions as in the 5-nm-thick modified nitride but with extended deposition times. Since the extended modified nitride film is resolvable by Auger analysis, it can be thought of as a magnification of the original 5-nm-thick modified nitride. A graded composition profile from Si-rich near bottom portion to N-rich near top segment of film is confirmed as shown in Fig. 3.

After detailed material analysis of the ONO dielectrics, a series of electrical characterizations were then carried out. Fig. 4 surveys the P/E response of test devices with modified nitride under different biasing conditions. Although higher voltages result in faster program speed and larger V_T shift, an undesirable early saturation phenomenon occurs after 300 ms during -12 V erasing operations. Therefore, an optimal asymmetric P/E operating voltage of $+12/-10$ V was determined. Once P/E bias conditions were established, the operation speed and window of SONOS devices with three different nitride films were compared in Fig. 5. As shown clearly, test devices with tapered bandgap nitride films exhibit the largest threshold voltage shifts and hence wider P/E operation windows. For test devices with standard and uniform Si-rich nitride, faster initial P/E speed (<0.5 ms) is observed compared to those with modified nitride. The early-stage behavior may be attributed to the fast filling of widespread shallow trapping levels. However, quick saturation also occurs because most accessible trapping levels are filled up instantaneously. For test devices with tapered bandgap nitride, the threshold voltage surpasses that of standard or uniform Si-rich nitride at 0.5 ms due to the greater number of accessible trapping levels and less back-tunneling probability. Although the erase speed of test devices with tapered bandgap nitride seems to be slower, an erase time of 50 ms is sufficient for most operation specifications since block erase is a common operation in Flash circuits. In addition, the self-convergence property of test devices is quite beneficial for multibit operation design. To test reproducibility, a survey of threshold voltage dispersion after P/E operation was conducted and a very tight distribution is observed in Fig. 6. The concentrated threshold voltage distribution suggests that the tested SONOS devices will not suffer tail-bits-sensitivity problems [6] and a shorter block erase time can be expected.

In order to evaluate operational reliability, endurance characteristics of all test devices were compared in Fig. 7. The results imply that residual charges are gradually accumulated

Sandisk Technologies, Inc. - Ex. 1002, Page 000599

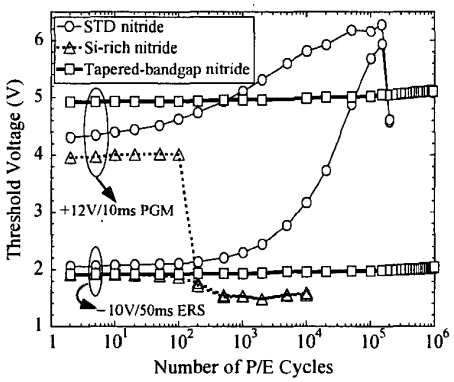


Fig. 7. Endurance characteristics of test devices with three different nitride films.

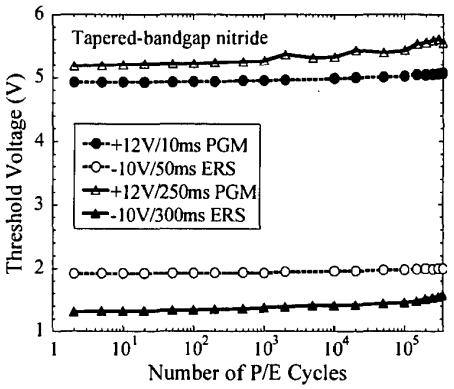


Fig. 9. Highly stressed cycling test of devices with tapered bandgap nitride.

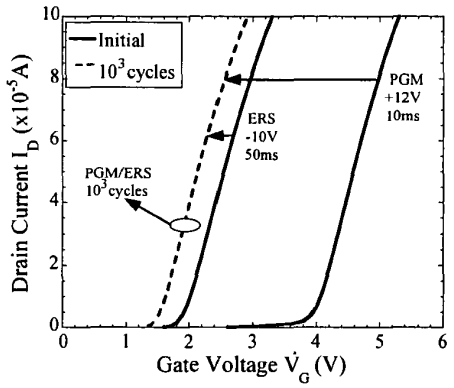


Fig. 8. *I–V* characteristics of test devices with Si-rich nitride before and after 10^3 P/E cycles.

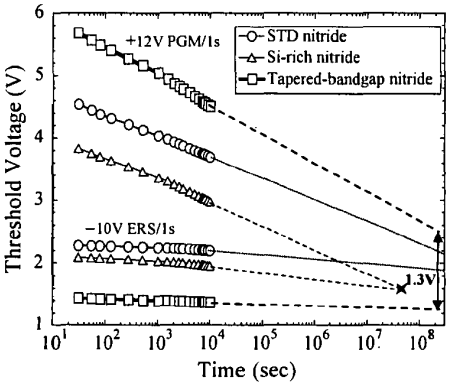


Fig. 10. Data retention characteristics of test devices with different nitride films.

in standard nitride during P/E operation as previously reported by Min She *et al.* [16]. This leads to increasing V_T and eventual loss of charge-trapping ability after 2×10^5 cycles. The charge accumulation takes place by gradual charge transition from shallow trapping levels down to deep trapping levels during repeated program operations. Since the deep trapping levels are buried underneath, the transition is very difficult to reverse by erase operations. Si-rich nitride cannot withstand P/E operations for more than 200 cycles. This result indicates that the extremely shallow trapping levels lose their trapping ability quickly. For the device with tapered bandgap nitride, no observable endurance degradation is observed even after 10^6 cycles. The long endurance of tapered bandgap nitride can be attributed to the highly accessible trapping levels that allow charges to be trapped and de-trapped during P/E operation without much trouble. Although the samples with standard nitride and uniform Si-rich nitride fail after a certain number of cycles, none of the devices actually broke down. Fig. 8 shows the *I–V* characteristics of test devices with uniform Si-rich nitride before and after 10_3 P/E cycles. These electrical stressing results suggest that the tunnel oxide does not breakdown and it is only nitride that loses its ability to trap charges since the off-leakage of the failed device is actually not degraded. The test device with modified nitride survives well even under severe stress condition (+12 V/250 ms and −10 V/300 ms) as shown in Fig. 9.

Another reliability requirement for Flash memory devices is to retain data longer than 10 years. In the retention characterization at room temperature shown in Fig. 10, tapered bandgap nitride exhibits a window of 1.3 V after ten years while the other two do not preserve sufficient charges under same test conditions. Based on extrapolation of these retention characteristics, it is believed that the large operation window of modified nitride is inherited from its superior performance at the beginning. The fact that all samples reveal similar slopes indicates that the nitride layer does not dominate the retention characteristics in our experiment. Therefore, retention characteristics seem to be dictated by the insulating quality of the tunnel oxide in SONOS devices [17]. Similar trends in read disturbance are shown in Fig. 11. However, the self-recovery or soft-programming mechanism during read operation actually improves retention characteristics of device with modified nitride. For devices with standard and uniform Si-rich nitride, serious read-disturb problems lead to shortened data retention as reported previously [18]. One possible theory of the peculiar V_T upsurge of erased bits within the first minute is that the holes pulled in during erase operations tend to accumulate near the bottom oxide due to their poor propagation ability and hence they lower E_c momentarily until incoming electrons recombine with them during a read operation. For devices with tapered bandgap nitride, the substrate-injected holes can migrate easily toward the increased bandgap near the top oxide by lateral hopping and hence do not contribute

Sandisk Technologies, Inc. - Ex. 1002, Page 000600

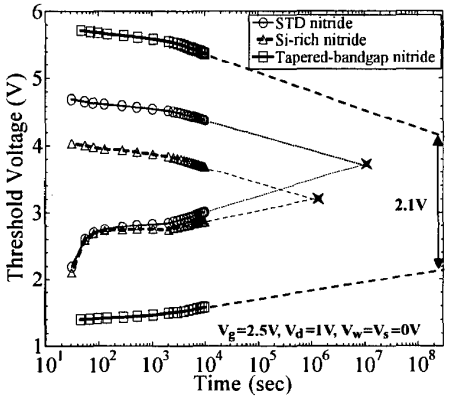


Fig. 11. Read-disturb characteristic of test devices with three different nitride films.

much to electron tunneling during read operations. Overall, the tapered bandgap nitride stands out among the three different nitride structures as demonstrating superior device performance and reliability.

IV. Conclusion

A highly efficient and reliable SONOS device has been developed by optimization of the nitride layer. Based on bandgap engineering, a new SONOS device structure with nonuniform composition nitride has been created. It is found that nitride modified by careful manipulation of the Si–N gas flow-rate ratio during nitride film deposition resultes in a tapered bandgap and significant improvement of device performance as well as reliability. The SONOS device with modified nitride exhibits improved charge-trapping efficiency, cycling endurance, data retention and read disturbance characteristics. The unique modified nitride structure provides a very promising solution for future high-density Flash memory design.

Acknowledgment

The authors would like to thank NDL for technical assistance.

References

[1] J. W. Hill-Lindsay and J. T. Yuen, "Ultra-high impact resistant digital data recorder for missile flight testing," *IEEE Trans. Compon., Packag., Manuf. Technol. A*, vol. 17, no. 3, pp. 398–403, Sep. 1994.

[2] A. K. Sharma, *Semicond. Memories Technol., Testing Reliabil.* Piscataway, NJ: IEEE Press, 1997, ch. 3, pp. 109–110.

[3] C. Y. Chang and S. M. Sze, *ULSI Devices*, New York: Wiley, 2000, ch. 8, pp. 430–448.

[4] W. D. Brown and J. E. Brewer, *Nonvolatile Semiconductor Memory Technol.* Piscataway, NJ: IEEE Press, 1998, ch. 1, pp. 49–50.

[5] M. H. White, Y. Yang, A. Purwar, and M. L. French, "A low voltage SONOS nonvolatile semiconductor memory technology," *IEEE Trans. Compon., Packag., Manufact. Technol. A*, vol. 20, no. 2, pp. 190–195, Jun. 1997.

[6] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: a novel localized trapping, 2-Bit nonvolatile memory cell," *IEEE Electron Device Lett.*, vol. 21, no. 11, pp. 543–545, Nov. 2000.

[7] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *IEEE Circuits Devices Mag.*, vol. 16, no. 4, pp. 22–31, Jul. 2000.

[8] P. Pavan, R. Bez, P. Olovo, and E. Zanoni, "Flash memory cells—an overview," *Proc. IEEE*, vol. 85, no. 8, pp. 1248–1271, Aug. 1997.

[9] T.-S. Chen, K.-H. Wu, and C.-H. Kao, "Performance improvement of SONOS memory by bandgap engineering of charge-trapping layer," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 205–207, Apr. 2004.

[10] M. Modreanu, N. Tomozeiu, P. Cosmin, and M. Gartner, "Physical-optical properties of LPCVD amorphous silicon rich nitride and oxynitride," in *Proc. Int. Semiconductor Conf.*, 1998, pp. 201–204.

[11] J. Masin, R. Mena, M. Brugler, and B. Raiagopalan, "Impact of Si–N ratios in a pre-metal Si_XN_Y : H_Z dielectric film on nMOS channel hot carrier reliability," in *Proc. IEEE Integrat. Reliabil. Workshop Final Rep.*, 1999, pp. 154–155.

[12] T. S. Chao, C. L. Lee, and T. F. Lei, "Ellipsometry study on refractive index profiles of the Si02\hbox {--}Si3N4\hbox {--}Si02\hbox {--}Si structure," *J. Appl. Phys.*, vol. 73, no. 4, 15, pp. 1732–1736, Feb. 1993.

[13] V. A. Gritsenko, Y. N. Morokov, Y. N. Novikov, I. P. Petrenko, S. N. Svitasheva, H. Wong, R. Kwok, and R. Chan, "Characterization of the silicon nitride-thermal oxide interface in ONO structures by ELS, XPS, ellipsometry, and numerical simulation," in *Proc. Int. Conf. Microelectronics*, vol. 1, Sep. 1997, pp. 111–114.

[14] A. Callegari, E. Cartier, M. Gribelyuk, H. F. Okorn-Schmidt, and T. Zabel, "Physical and electrical characterization of hafnium oxide and hafnium silicate sputtered films," *J. Appl. Phys.*, vol. 90, no. 12, pp. 6466–6475, 2001.

[15] D. Davazoglou, "Optical absorption threshold of low pressure chemically vapor deposited silicon oxynitride films from $SiCl_2H_2 - NH_3 - N_20$ mixtures," *Thin Solid Films*, vol. 437, pp. 266–271, 2003.

[16] D. MinShe, H. Takeuchi, and T.-J. King, "Silicon-nitride as a tunnel dielectric for improved SONOS-type Flash memory," *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 309–311, May 2003.

[17] W. J. Tsai, S. H. Gu, N. K. Zous, C. C. Yeh, C. C. Liu, C. H. Chen, T. Wang, S. Pan, and C. Y. Lu, "Cause of data retention loss in a nitride-based localized trapping storage Flash memory cell," in *Proc. IEEE Int. Reliabil. Phys. Symp.*, 2002, pp. 34–38.

[18] W.-J. Tsai, C.-C. Yeh, N.-K. Zous, C.-C. Liu, S.-K. Cho, T. Wang, S. C. Pan, and C.-Y. Lu, "Positive oxide charge-enhanced read disturb in a localized trapping storage Flash memory cell," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 434–439, Mar. 2004.



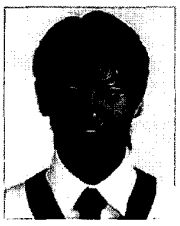
Kuo-Hong Wu was born in Taiwan, R.O.C., on July 20, 1966. He received the M.S. degree in electronics engineering from Chung-Cheng Institute of Technology (CCIT), Taiwan, in 1999 and the Ph.D. degree from the Defense Science School, CCIT, National Defense University (NDU), Taiwan, in 2005.

He is currently with the Army Communication Electronics Information School, Taoyuan, Taiwan. His research activities have been focused in the area of SONOS Flash memory and stacked-gate memory related issues.



Hua-Ching Chien received the B.S. degree in physics from Republic of China Military Academy (ROCMA), Taiwan, R.O.C., in 1988, the M.S. degree in electrical engineering from Chung-Cheng Institute of Technology (CCIT), Taiwan, in 1996. He is currently pursuing the Ph.D. degree at the Defense Science School, CCIT, National Defense University (NDU).

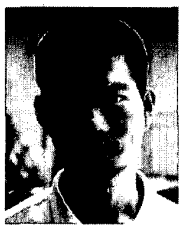
His research activities have been focused in the area of SONOS Flash memory and bandgap voltage reference circuit design.



Chih-Chiang Chan received the M.S. degree in electronics engineering from Chung-Cheng Institute of Technology (CCIT), Taiwan, R.O.C., in 2003.

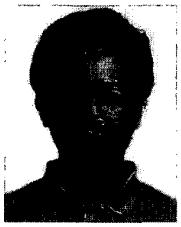
He is currently with the Department of Electric Engineering, Chung-Cheng Institute of Technology, National Defense University, Taoyuan, Taiwan. His research activities have been focused in stacked-gate Flash memory related issues.

Sandisk Technologies, Inc. - Ex. 1002, Page 000601



Tung-Sheng Chen received the B.S. degree in physics from Chung-Cheng Institute of Technology (CCIT), Taiwan, R.O.C., in 1986, the M.S. degree in electrical engineering from Naval Postgraduate School, Monterey, CA, in 1990, and the Ph.D. degree in electrical engineering from the University of Texas, Austin, in 1998.

While pursuing the Ph.D. degree, he also worked as a Teaching Assistant at the University of Texas. In the summer of 1997, he worked at Motorola Semiconductor Technology Laboratory as an intern. He was an Associate Professor in the Department of Electrical Engineering, CCIT, National Defense University (NDU). His research topics include GB DRAMs, piezoresistive sensors, packaging-induced stressing effect on microelectronic devices, crosstalk related issues in RFIC, high-Q spiral inductors, and SONOS Flash memory. Currently, he is with the Department of Electric Engineering, Chung-Cheng Institute of Technology, National Defense University, Taoyuan, Taiwan.



Chin-Hsing Kao received the B.S. degree in physics from Chung-Cheng Institute of Technology (CCIT), Taiwan, R.O.C., in 1980, and the Ph.D. degree in electrical engineering from National Tsing-Hua University, Hsinchu, Taiwan, in 1990.

He joined the Department of Applied Physics at CCIT in 1990. He is currently the Dean of the Science School and his research interests are mainly in MOS device analysis and quantum dot computations. He is also involved in the RFIC-related crosstalk analysis and Flash memory development.

Sandisk Technologies, Inc. - Ex. 1002, Page 000602

PERGAMON

Solid-State Electronics 43 (1999) 2025–2032

SOLID-STATE ELECTRONICS

Reliability considerations in scaled SONOS nonvolatile memory devices

Yang (Larry) Yang[a,*], Ansha Purwar[b], Marvin H. White[a]

[a]*Electrical Engineering and Computer Science Department, Sherman Fairchild Center, Lehigh University, Bethlehem, PA 18015, USA*
[b]*Lucent Technologies, Allentown, PA 18013, USA*

Received 7 March 1999; accepted 19 May 1999

Abstract

The memory characteristics and reliability of a SONOS nonvolatile memory device are determined, to a large extent, by the charge transport and trapping properties of its storage nitride film. In this paper we investigate carrier trapping phenomenon in a scaled SONOS transistor with an effective gate oxide thickness of 94 and a nitride storage layer deposited with LPCVD at 680°C. Atomic Force Microscopy (AFM) has been employed to examine the surface quality of deposited nitride films. We have found that nitride film deposited at 680°C shows the lowest surface roughness, as compared to the films formed at 725C and 650°C. With a charge separation technique, we have demonstrated that the charge centroid is deep into the nitride layer at low injection levels and moves towards the center of the film as the injection level is increased. From our measurement, a trap density of 1.7×10^{19} cm^{-3} in the nitride has been determined. Devices with nitride (2.1 Å RMS roughness) deposited at 680°C show less degradation in data retention with respect to erase/write cycling when compared to devices with nitride (2.9 Å RMS roughness) deposited at 725°C. © 1999 Elsevier Science Ltd. All rights reserved.

Keywords: Nonvolatile semiconductor memory; SONOS; EEPROM

1. Introduction

Since the 1960's, there have been two major technologies in the field of nonvolatile semiconductor memories (NVSM): the floating-gate structure [1] and the SONOS (polysilicon-blocking oxide-silicon nitride-tunnel oxide-silicon) structure [2]. The principal structural differences between these two types of devices are the nature of the storage medium and the thickness of the tunnel oxide. The relatively thick (70–120 Å) tunnel oxide in floating-gate type memories provides good long-term data retention. A thick tunnel oxide also eases the process control in oxide growth, thus making floating-gate technology a popular choice in the semiconductor industry. However, floating-gate type memories are subject to single pin-hole defects in the tunnel oxide which permit stored charge to escape from the conducting polysilicon layer. On the other hand, the SONOS memory device stores charges in a high density of traps located within an insulating nitride layer. These traps are isolated with each other and, thereby, provide immunity to the deleterious effects of single pinhole defects. The tunnel oxide thickness is in the range of 10–30 Å for SONOS structures. The control of this ultra-thin tunnel oxide was considered to be difficult in the 70's and manufacturers had relatively little experience with the use of thin layers of silicon oxide

* Corresponding author. Tel.: +1-610-758-4518; fax: +1-610-758-6705.
E-mail address: yy02@lehigh.edu (Y. (Larry). Yang)

0038-1101/99/$ - see front matter © 1999 Elsevier Science Ltd. All rights reserved.
PII: S0038-1101(99)00161-6

Sandisk Technologies, Inc. - Ex. 1002, Page 000603

and nitride. As a result, SONOS devices found applications primarily in space and strategic applications due to their radiation hardness. However, as the industry gained familiarity with nitride films in localized oxidation of silicon (LOCOS), SiN cap passivation, multiple dielectrics in DRAM's and interpoly-dielectrics in polysilicon FLASH EEPROM's and ultra-thin CMOS gate oxides of 30–40 Å for 1000–2000 Å channel lengths, the reproducibility of ONO triple dielectrics has been improved greatly and the SONOS structure has become a viable candidate for scaled NVSM technology.

Recently, interest in SONOS technology has been stimulated by the advance of portable computers and personal telecommunication devices. For floating-gate type memories, the on-chip programming voltage is generally higher than 12 V and the scaling of these structures has become difficult. On the contrary, the scalability of SONOS device allows operation at low programming voltage of 5–8 V [3,4]. In addition, channel current is necessary to program floating-gate devices while the programming of SONOS memories does not require channel current, which makes SONOS attractive for battery operated applications.

SONOS nonvolatile memory devices employ Modified-Fowler-Nordheim (MFN) tunneling in both erase and write operations. A high density of traps in the silicon nitride is responsible for charge storage and memory action. To date, the microscopic structure of these traps is not well understood. From their low-temperature electron spin resonance measurement data, Kamigaki et al. [5] proposed a two-trap model in which electrons and holes are captured at different trap centers. They have suggested electron/hole traps are at the interface between silicon cluster and silicon nitride bulk, while hole traps are at nitrogen vacancies in silicon nitride bulk. According to theoretical calculations, Robertson and Powell [6] have suggested that the trivalent silicon center with a dangling bond is the origin of both electron and hole trapping in silicon nitride. The electron spin resonance and injection experiments by Fujita and Sasake [7] and Krick et al. [8] have supported this amphoteric model.

This paper concentrates on reliability considerations of scaled SONOS memory devices with particular emphasis on data retention degradation due to excess erase/write cycling. We investigate the correlation between retention degradation and surface roughness of the nitride film in the ONO dielectric stack. In SONOS devices, a rough silicon nitride surface causes local thinning in the ONO dielectric stack. This local thinning results in a local electric field enhancement which, combined with an increase in nitride conductivity during erase/write cycling, leads to acceleration in charge decay. In the next section, an AFM is used to measure the surface roughness of nitride films deposited at various temperatures. An optimum deposition temperature is found for a given gas flow ratio to achieve minimum surface roughness. Then, the charge trapping properties of this nitride film, including the trap density and the charge centroid movement, is studied. Finally, data retention behavior of devices with a minimum nitride surface roughness and devices with a higher nitride surface roughness are compared.

2. Effect of deposition temperature on nitride surface roughness

Silicon nitride films serve as the storage medium in SONOS devices and optimization of its trapping properties is an important issue. In early studies, the nitride film deposition was performed by atmospheric pressure chemical vapor deposition (APCVD) with a dilute mixture of silane and ammonia at temperatures in the range of 800–900°C [9]. These films suffered nonuniformity due to the high deposition rate. In today's state-of-the-art technology, low pressure chemical vapor deposition (LPCVD) is used to deposit the silicon nitride. The LPCVD nitride is obtained in a reactor at a temperature of 650–750°C when dichlorosilane and ammonia react at the wafer surface. The chemical composition and deposition temperature greatly influence the trapping properties of the silicon nitride. According to Fujita et al. [10], silicon dangling bonds create deep trapping states in the nitride while oxygen and hydrogen atoms act as terminators to decrease the amount of traps. Therefore, silicon nitride films deposited with high $SiCl_2H_2/NH_3$ gas flow ratios show high trap densities, which leads to an improvement in the programming speed of the SONOS memories. A $SiCl_2H_2/NH_3$ gas flow ratio of 75:25 (sccm) has been employed in SONOS transistors designed for fast programming [11]. On the other hand, films deposited with low $SiCl_2H_2/NH_3$ ratios exhibit low trap density. These films have weaker Coulombic repulsion between the trapped charges and reduced charge interaction, which translates into improved data retention. To further improve the data retention of SONOS devices, oxynitride deposited with a mixture of $SiCl_2H_2$, NH_3 and N_2O has been used in place of silicon nitride as the storage medium [12]. The incorporation of oxygen in these films further reduces the trap density and results in longer data retention [13]. As a result, chemical composition in silicon nitride deposition process can be used as a means to control the trap density in SONOS devices. In our work, we have selected a $SiCl_2H_2/NH_3$ gas flow ratio of 10:100 (sccm) to obtain SONOS devices with simultaneous good overall performance in programming speed and data retention.

Deposition temperature is another important parameter to achieve high-quality silicon nitride films.

Sandisk Technologies, Inc. - Ex. 1002, Page 000604

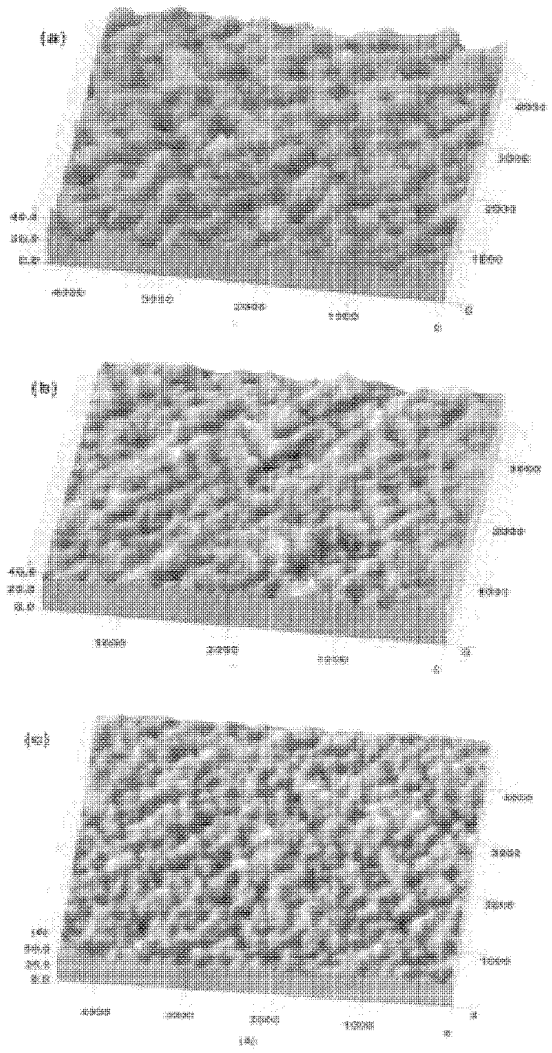


Fig. 1. AFM images of the nitride films in a square region about 4000 Å × 4000 Å. LPCVD nitride deposition temperature are (a) 650°C, (b) 680°C, and (c) 725°C, respectively.

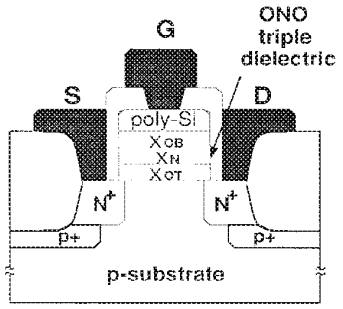


Fig. 2. The device structure of a n-channel SONOS transistor. X_{OT} is the tunnel oxide thickness, X_N is the nitride film thickness and X_{OB} is the blocking oxide thickness.

Tanaka et al. [14] have found nitride films deposited at lower temperatures provide improved breakdown characteristics for the ONO composite films in DRAM storage capacitors. In SONOS devices, surface roughness can cause reliability problems. At a place where local thinning occurs, the local electrical field is enhanced. This film thinning combined with local field enhancement accelerates the charge decay and causes a faster deterioration of the device to erase/write cycling. We have conducted AFM studies on silicon nitride films deposited at different temperatures and discovered an optimum temperature for LPCVD nitride deposition, which achieves minimum surface roughness and improves memory retention.

To investigate the impact of deposition temperatures on silicon nitride surface roughness, three groups of samples, each with 50 Å silicon nitride film deposited at a different temperature on a p-type (100) silicon wafer, have been used in our study. An in situ tunnel oxide of 10–12 Å has been formed in the LPCVD reactor prior to the nitride deposition The silicon nitride deposition has been performed with $SiCl_2H_2$:NH_3 = 10:100 sccm at 650, 680 and 725°C, respectively. The surface roughness of silicon nitride films has been evaluated with an AFM. Fig. 1 shows the AFM images of the nitride films in a square region about 4000 Å × 4000 Å. The surface roughness data from the image analysis is shown in Table 1. The surface roughness is reduced as the deposition tempera-

Table 1
Surface roughness data from the image analysis

Deposition temperature (°C)	Peak to valley (Å)	Mean height (Å)	RMS roughness (Å)
650	37	19	3.4
680	18	8.8	2.1
725	28	14	2.9

Sandisk Technologies, Inc. - Ex. 1002, Page 000605

ture is lowered from 725 to 680°C. As the deposition temperature is further lowered to 650°C, an increase in surface roughness is observed.

3. SONOS transistor fabrication

SONOS transistors have been fabricated with N-well CMOS technology and LOCOS isolation processes. The starting material is 2–3 Ω cm (100) p-type substrates. The structure of an n-channel SONOS transistor is shown in Fig. 2. The processing sequence is identical to conventional CMOS technology except for the formation of the ONO dielectric stack. The quality of the tunnel oxide, silicon nitride and blocking oxide determines the electrical properties of these films, which in turn, determines the device characteristics.

Prior to the tunnel oxide growth, the wafers are cleaned with a standard RCA clean procedure, followed by a 100:1 dilute HF etch to remove the thermally and chemically grown oxide. A tunnel oxide of 15 Å is grown at 700°C for 30 minutes by using an argon-diluted oxygen ambient (1.5% O_2 in Ar) in a custom-designed triple wall oxidation furnace [15]. Next, a thin layer of silicon nitride is immediately deposited in a LPCVD reactor for 20 min at 680°C with gas flow rate of $SiCl_2H_2$:NH_3 = 10:100 (sccm). To obtain high quality films, the wafer transfer time from the oxidation furnace to the LPCVD reactor is minimized (i.e. less than 1 min). A thin layer of LPCVD oxide is then deposited with $SiCl_2H_2$:N_2O = 10:100 (sccm) at 725°C, followed by a steam densification at 900°C for 30 minutes. During this steam densification, about 5 to 10 Å of silicon nitride is converted to oxide [16]. The final nitride thickness is 62 Å and the blocking oxide thickness is 42 Å. After the ONO triple dielectric film is formed, a layer of polysilicon is deposited and doped with a $POCl_3$ process. Next, the gate is patterned and the contact windows are opened. A forming gas anneal at 500°C is performed to improve the quality of the Si-SiO_2 interface [17]. The electrodes are then formed with Al(1% Si) sputtering and a 30 min post metal anneal (PMA) is performed at 400°C in a forming gas ambient.

4. Charge injection analysis

In order to understand and model the behavior of SONOS devices, we have examined the charge transport and trapping properties of the nitride films. In this section, we use a charge separation technique to investigate the charge injection, back-tunneling and charge centroid in scaled SONOS transistors. The charge separation, a split C-V technique, is a generalization of the linear voltage ramp (LVR) technique. This technique was first introduced by Koomen [18] and later pursued by Sodini et al. [19] to investigate the mobility of channel carriers. The difference between this technique and the LVR method is the separate measurement of the bulk and channel charge current as a function of the gate voltage. Agarwal et al. [20] applied this technique to study the charge injection and back tunneling across the tunnel oxide in SONOS transistor. Electron injection and hole back tunneling may be studied with a n-channel SONOS transistor, while hole injection and electron back tunneling can be investigated with a p-channel device. The back tunneling minority carriers cannot be collected by the source/drain junctions due to their recombination with majority carriers at the accumulated semiconductor surface. In a dual-channel SONOS structure, Roy et al.

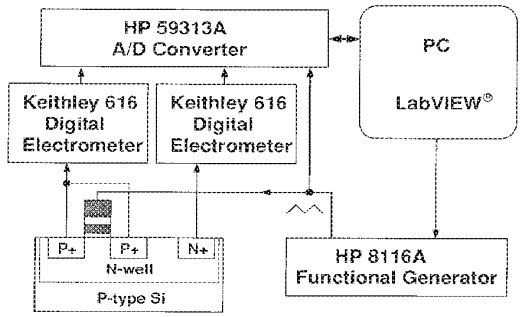


Fig. 3. Block diagram of a computer-aided split C-V data acquisition system. The experimental setup is controlled by a PC using Lab-VIEW® software.

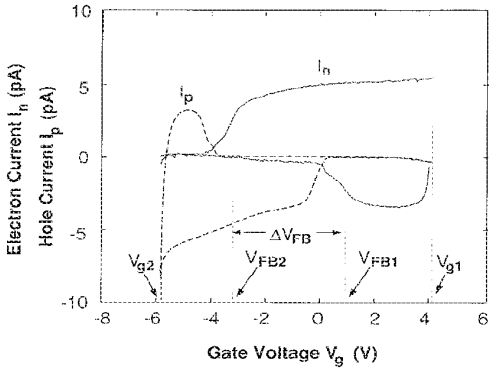


Fig. 4. Experimental curve of a split C-V measurement on a p-channel SONOS transistor with 15 Å tunnel oxide, 62 Å storage nitride and 42 Å blocking oxide. Parasitics have been subtracted from the data. The gate voltage is linearly ramped between a positive voltage V_{g1} and a negative voltage V_{g2} with a ramp rate α of 100 mV/s.

Sandisk Technologies, Inc. - Ex. 1002, Page 000606

[21] demonstrated electron and hole charge separation for both gate polarities within one device structure. In our work, we study hole injection and the movement of the hole charge centroid within the nitride film for different injection levels with a p-channel SONOS transistor. The memory or data retention behavior of the excess hole state is presented in the next section.

Figure 3 illustrates the block diagram of a computer-aided split C-V data acquisition system. The experimental setup is controlled by a PC using Lab-VIEW® software. The linear voltage is supplied by a programmable function generator with a triangular waveform. The source and drain electrodes are shorted together. The source and bulk currents are measured with Keithley 616 digital electrometers. In the measurement, the parasitic components are determined and subtracted from the data [20]. Fig. 4 shows an experimental curve of a split C-V measurement on a p-channel SONOS transistor with the parasitics subtracted from the data.

The gate voltage is linearly ramped between a positive voltage V_{g1} and a negative voltage V_{g2} with a ramp rate α of 100 mV/s. The ramp starts at V_{g1} with the p-channel SONOS device in accumulation. Electrons tunnel from the silicon into the nitride conduction band and are captured by the traps in the nitride film. The negatively charged nitride layer corresponds to a positive flatband voltage V_{FB1}. As the gate voltage ramps towards V_{g2}, the semiconductor surface moves successively from accumulation to flatband, depletion, and finally to inversion. During this process, two charge transfer processes may occur: (1) holes may tunnel from the inversion layer to the nitride and trap in the nitride film, and (2) a portion of the previously trapped electrons may back-tunnel from the nitride film to the semiconductor substrate. The net result is a positively charged nitride film and the flatband voltage of the device shifts negatively from V_{FB1} to V_{FB2}.

The injected positive charges, ΔQ_p^{inj}, and the back-tunnel negative charges, ΔQ_n^{bt}, can be written as [21,22]:

$$\Delta Q_p^{inj} = \frac{1}{\alpha A_g}\left(\int_{V_{FB1}}^{V_{g2}} I_p dV_g - \int_{V_{g2}}^{V_{FB2}} I_p dV_g\right) \quad (1)$$

$$\Delta Q_n^{bt} = \frac{1}{\alpha A_g}\left(\int_{V_{FB1}}^{V_{g2}} I_n dV_g - \int_{V_{g2}}^{V_{FB2}} I_n dV_g\right), \quad (2)$$

where α is the gate voltage ramp rate, and A_g is the device gate area. V_{FB1} and V_{FB2} are the device flatband voltages corresponding to electron trapped and hole trapped states, respectively. In the development of these equations we assume a quasi-equilibrium condition during the voltage ramp with all injected charge

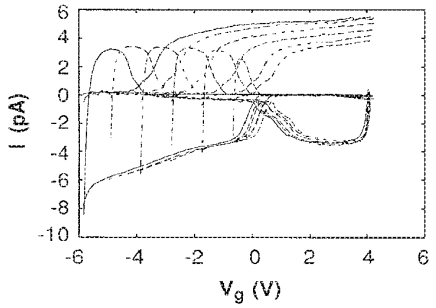


Fig. 5. Experimental results of the split-CV measurement. Parasitics have been subtracted from the data.

remaining in the nitride film. The shift in flatband voltage, ΔV_{FB}, is related to the charge transfer by the following expression [21]:

$$\Delta V_{FB} = \Delta Q_p^{inj}\left(\frac{x_N - \bar{x}_p^{inj}}{\epsilon_n} + \frac{x_{OB}}{\epsilon_{ox}}\right) + \Delta Q_n^{bt}\left(\frac{x_N - \bar{x}_n^{bt}}{\epsilon_n} + \frac{x_{OB}}{\epsilon_{ox}}\right), \quad (3)$$

where $\bar{x}_p^{inj}$ is the injected hole charge centroid, $\bar{x}_n^{bt}$ is the back-tunnel electron charge centroid, x_N is the nitride layer thickness, with ϵ_{ox} and ϵ_n the permittivity of the silicon oxide and nitride, respectively. The charge centroids are measured from the tunnel oxide-nitride interface.

In order to obtain a good signal to noise ratio, we have employed transistors with a length of 100 μm and a width of 100 μm. In our experiments, the gate voltage ramps from a fixed $V_{g1} = 4$ V to a varying V_{g2} ranging from −1 to −6 V. Fig. 5 shows the experimental results of the measurement. As the amplitude of V_{g2} increases, the amount of positive charge in the nitride film and the magnitude of flatband voltage,

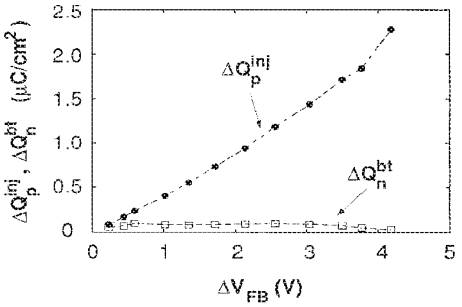


Fig. 6. Relationship between flatband voltage shifts, ΔV_{FB}, and injected holes, ΔQ_p^{inj}, and back-tunneled electrons, ΔQ_n^{bt}.

Sandisk Technologies, Inc. - Ex. 1002, Page 000607

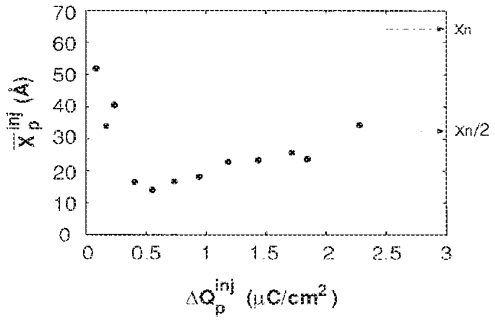


Fig. 7. Extracted values of charge centroid as a function of ΔQ_p^{inj} for $\bar{x}_n^{bt} = 20$Å.

V_{FB2}, increases. The injected hole charge and back-tunneled electron charge are evaluated numerically using Eqs. (1) and (2). Fig. 6 shows the relationship between flatband voltage shift, ΔV_{FB}, and injected hole charge, ΔQ_p^{inj}, and back-tunneled electron charge, ΔQ_n^{bt}. At low injection levels, ΔV_{FB} increases linearly with injected charge ΔQ_p^{inj} while the back-tunnel charge ΔQ_n^{bt} appears constant. Libsch [23] pointed out that even though ΔQ_n^{bt} is a small quantity compared to ΔQ_p^{inj}, it should not be neglected in the calculation of the charge centroid using Eq. (3), especially at low injection levels. In Eq. (3), the value of $\bar{x}_p^{inj}$ can not be exactly determined because $\bar{x}_n^{bt}$ is unknown, even though ΔV_{FB}, ΔQ_p^{inj} and ΔQ_n^{bt} can be obtained experimentally. From the observation of time duration for the back-tunnel process, Roy estimated $\bar{x}_n^{bt}$ to be about 20 Å [21]. Assuming a $\bar{x}_n^{bt}$ value of 20 Å, we can extract the charge centroid as a function of ΔQ_p^{inj}, as shown in Fig. 7. At low injection levels, the electric fields are low and the charge injection occurs at a position close to the nitride-blocking oxide interface (i.e. $\bar{x}_p^{inj} \approx x_N$) which results in a large charge centroid. As the charge injection level increases, the fields are higher, the band bending is more severe and the charge centroid moves closer to the tunnel oxide-nitride interface. Assuming a uniform trap distribution in the nitride, the charge centroid should approach half the nitride film thickness at high injection levels. Using Chao's approach [24], the trap density of the nitride film, N_{T0} can be obtained from the slope of Fig. 7 at increased injection levels:

$$N_{T0} = \frac{1}{4q} \times \left| \frac{\Delta(\Delta Q_p^{inj})}{\Delta \bar{x}_p^{inj}} \right| = 1.7 \times 10^{19} cm^{-3} \quad (4)$$

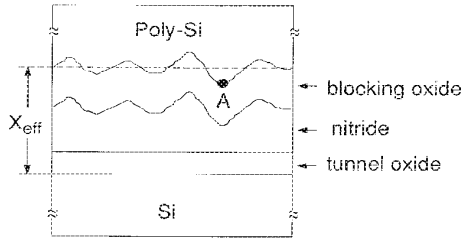


Fig. 8. Schematic cross section of a portion of the channel in a SONOS transistors. Due to surface roughness of the nitride film, electric field at point A is enhanced.

5. Data retention reliability

The nitride films deposited at 680°C have 'smoother' surfaces than films deposited at a higher temperature (725°C) or lower temperature (650°C). In this section, we address the correlation between surface roughness of the nitride film and the data retention characteristics, in particular the resistance of data retention to erase/write cycling for a SONOS transistor. Hu et al. [16] have pointed out charge loss mechanisms in scaled SONOS devices are (1) tunneling of trapped charges to silicon conduction band, (2) tunneling of trapped charges to Si-SiO_2 interface traps, and (3) tunneling of charges from silicon substrate to nitride traps and subsequent recombination of electrons and holes. These tunneling processes are strong functions of electric fields. In nitride films with rough surfaces, local thinning causes an increase in local electric fields for a given voltage. These increased local fields enhance the tunneling processes and accelerate the local charge decay. Fortunately, the nonconducting nature of the nitride prevents the complete discharging from these discrete, localized sites.

The consequences of nitride films with rough surface may not be noticeable. If, however, the device experiences a considerable amount of erase/write cycles, then the nitride film can deteriorate. During erase/write cycling, electrons and holes are injected into the nitride. These injected charges, along with the high field stress, can change the microscopic bond structure and increase the conduction between traps within the nitride [25]. In addition, local thinning can accelerate the nitride deterioration. Fig. 8 illustrates the cross section of a portion of the channel region in a SONOS transistor, assuming the oxide surface roughness is small. At point A in Fig. 8, local field is enhanced by the surface roughness [22]:

$$E = \left(1 + \frac{X_{eff}}{r_c}\right) E_0, \quad (5)$$

where r_c is the local radius parameter characterizing

Sandisk Technologies, Inc. - Ex. 1002, Page 000608

Table 2
Fabrication parameters of devices

	Tunnel oxide thickness (Å)	Nitride film thickness (Å) and deposition temperature °C	Blocking oxide thickness (Å)
lot A	15	62, 680	42
lot B	18	50, 725	40

the surface roughness, X_{eff} is the average value of the effective dielectric thickness, and E_0 is the average electric field, respectively. For a programming voltage of 7 V, the maximum value of E_0 is about 8 to 9 MV/cm depending on the amount of stored charges in the nitride. Because of the local thinning, the local fields can be much higher than E_0. These enhanced electric fields facilitate the injected charges with higher energies, thereby accelerating the degradation of nitride films. As a result of a local field enhancement and an increased nitride conductivity, an increase in charge decay rate becomes observable after extensive erase/write cycling.To examine the effect of nitride surface roughness on data retention reliability, SONOS nonvolatile memory transistors have been employed from two lots, A and B. Devices in lots A and B are fabricated with basically the same technology outlined in the device fabrication section, except for the formation of the ONO triple dielectrics. Except for a slight difference in dielectric film thickness, the storage nitride in lot A is deposited at 680°C while the nitride in lot B is deposited at 725°C under the same gas ratio and reactor pressure. The differences in ONO layer parameters between lot A and lot B are summarized in Table. 2. We have examined the data retention characteristics for the excess electron state in devices from both lots. The retention characteristics do not show degradation to erase/write cycling. On the other hand, erase/write cycling influences the data retention of the excess hole state. Similar observations have been made by White et al. [26]. Fig. 9 shows a typical data retention characteristic for the excess hole state of an n-channel SONOS devices from lot A, before and after 1 million erase/write cycles. Retention characteristics for the n-channel SONOS devices from lot B are shown in Fig. 10. These measurements are performed at 85°C, which is the highest temperature specified for commercial EEPROMs. First, we notice in both Figs. 9 and 10 the device threshold voltage is shifted positively after 1 million erase/write cycles which indicates a net increase in negative charge trapping within the dielectric [27]. Secondly, the threshold voltage decay rate is a measure of the discharging rate because the threshold voltage shift is proportional to the amount of charge trapped in the nitride. The threshold voltage decay rate is 0.16 V/dec for devices in lot A and remains unchanged after the device experiences 1 million erase/write cycles. For devices in lot B, the threshold voltage decay rate is 0.14 V/dec before the erase/write cycling, which is slightly smaller than that of lot A due to the slightly thicker tunnel oxide. However, the threshold voltage decay rate is increased to 0.17 V/dec after 1 million erase/write cycles. In order to make meaningful comparison, erase/write cycling conditions must be carefully arranged. In our experiments, the devices from both lots experience the same electric field strength (about 8.5 MV/cm) with approximately the same

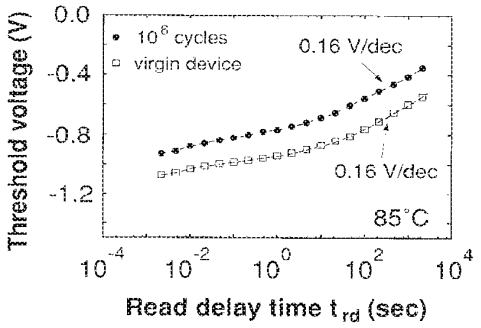


Fig. 9. Typical data retention of n-channel SONOS transistors of lot A. Open squares are data taken before erase/write cycling, while solid circles are data taken after 1 million erase/write cycles. All data is taken at 85°C.

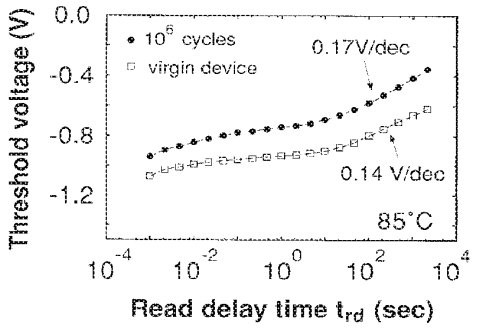


Fig. 10. Typical data retention of n-channel SONOS transistors of lot B. Open squares are data taken before erase/write cycling, while solid circles are data taken after 1 million erase/write cycles. All data is taken at 85°C.

Sandisk Technologies, Inc. - Ex. 1002, Page 000609

amount of charge passing through the tunnel oxide during erase/write cycling.

6. Conclusion

Silicon nitride film surface roughness can be reduced when LPCVD is performed at 680°C, as compared with 650 and 725°C, which indicates there exists an optimized temperature range for nitride deposition to achieve a silicon nitride film with a smoother surface. With a charge separation technique, we have investigated the trapping properties of nitride films deposited at 680°C. The effects of nitride surface roughness on SONOS device data retention reliability are discussed. We postulate local thinning due to silicon nitride films with rough surfaces can (1) accelerate the nitride degradation with erase/write cycling, and (2) enhance the discharge of trapped charges in the nitride. Furthermore, we demonstrate the data retention of scaled SONOS nonvolatile memory devices can be improved by employing a smoother nitride.

Acknowledgements

This work was supported by the National Science Foundation under contract #ECS-9810923, the Sherman Fairchild Foundation and Northrop-Grumman Corp.

References

[1] Kahng D, Sze SM. A floating gate and its application to memory devices. Bell Syst Tech J 1967;46:1288.
[2] Wegner HAR, Lincoln AJ, Pao HC, O'Connel MR, Oleksiok RE. Metal-insulator-semiconductor transistor as a nonvolatile storage element. IEEE IEDM Abstract 1967, p. 58.
[3] French ML, White MH. Scaling of multidielectric nonvolatile SONOS memory structures. Solid-State Electron 1995;37(12):1913.
[4] White MH, Yang YL, Purwar A, French ML. A low voltage SONOS nonvolatile semiconductor memory technology. IEEE Trans Comp Pack and Manu Tech part A 1997;20(2):190.
[5] Kamigaki Y, Minami S, Kato H. A new portrayal of electron and hole traps in amorphous silicon nitride. J Appl Phys 1990;68(5):2211.
[6] Robertson J, Powell M. The electronic properties of silicon nitride. Philos Mag B 1981;44(2):215.
[7] Fujita S, Sasaki A. Dangling bonds in memory-quality silicon nitride films. J Electrochem Soc 1985;132(2):398.
[8] Krick DT, Lenahan PM, Kanicki J. Nature of the dominant deep trap in amorphous silicon nitride. Phys Rev B 1988;38(12):8226.
[9] Schauer H, Arnold E, Murau P. Interface states and memory decay in MNOS capacitors. IEEE Trans Elec Dev 1978;25(8):1037.
[10] Fujita S, Toyoshima H, Nishihara M, Sasaki A. Variation of trap states and dangling bonds in CVD Si_3N_4 Layer on Si substrate by NH_3/SiH_4 ratio. J Electron Mater 1982;11(4):795.
[11] Wann HC, Hu C. High-endurance ultra-thin tunnel oxide in MONOS device structure for dynamic memory application. IEEE Elec Dev Lett 1995;16:491.
[12] William D, Adams D, Bishop R. Radiation Hardened 64K/256K EEPROM Technology. In: Sixth IEEE Int. NVM Tech. Conf. Proc., 1996. p. 67.
[13] Kapoor VJ, Xu D, Bailey RS, Turi RA. The combined effect of hydrogen and oxygen impurities in the silicon nitride film of MNOS devices. J Electrochem Soc 1992;139(3):915.
[14] Tanaka H, Uchida H, Ajioka T, Hirashita N. The degradation of TDDB characteristics of $SiO_2/Si_3N_4/SiO_2$ stacked films caused by surface roughness of Si_3N_4 films. IEEE Trans Elec Dev 1993;40(12):2231.
[15] Yoon S, White MH. Study of thin gate oxides grown in an ultra-dry/clean-triple-wall oxidation furnace system. J Electron Mater 1990;19(5):487.
[16] Hu Y, White MH. Charge retention in scaled SONOS nonvolatile semiconductor memory devices-modeling and characterization. Solid-State Electron 1993;36(10):1401.
[17] Lyding JW, Hess K. Reduction of hot electron degradation in metal oxide semiconductor transistors by deuterium processing. Appl Phys Lett 1996;68(18):2526.
[18] Koomen J. Investigation of the MOST channel conductance in weak inversion. Solid-State Electron 1973;16(7):801.
[19] Sodini CG, Ekstedt TW, Moll JL. Charge accumulation and mobility in thin dielectric MOS transistors. Solid-State Electron 1982;25(9):833.
[20] Agarwal AK, White MH. New results on electron injection, hole injection and trapping in MONOS nonvolatile memory devices. IEEE Trans Elect Dev 1985;32(5):941.
[21] Roy A, White MH. A new approach to study electron and hole charge separation at the semiconductor-insulator interface. IEEE Trans Elect Dev 1990;37(6):1504.
[22] Roy A. Characterization and modeling of charge trapping and retention in noval multi-dielectric nonvolatile semiconductor memory devices. Ph.D. dissertation, Lehigh University, 1989.
[23] Libsch FR, White MH. Charge transport and storage of low programming voltage SONOS/MONOS memory devices. Solid-State Electron 1990;33(1):105.
[24] Chao CC, White MH. Characterization of charge injection and trapping in scaled SONOS/MONOS memory devices. Solid-State Electron 1987;30(3):307.
[25] Pryor RW. mechanism for endurance failure in metal-nitride-oxide-semiconductor device structures. J Appl Phys 1981;52(5):3702.
[26] White MH, Cricchi JR. Characterization of thin-oxide MNOS memory transistors. IEEE Trans Elect Dev 1972;19(12):1280.
[27] Minami S, Kamigaki Y. A novel MONOS nonvolatile memory device ensuring 10 year data retention after 10^7 erase/write cycles. IEEE Trans Elect Dev 1993;40(11):2011.

Sandisk Technologies, Inc. - Ex. 1002, Page 000610

Electronic Acknowledgement Receipt

EFS ID:	29011181
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	24-APR-2017
Filing Date:	26-OCT-2016
Time Stamp:	16:59:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C3_IDS_04182017.pdf	1063542 45a116655b90e8c02fb86953fa35150eced3bc7d	no	35

Warnings:

Information:					
2	Non Patent Literature	Altera_MAX9000ProgrammableLogicDeviceFamily.pdf	8913303 7c5133eeeb72d44045a7f4232080e5d0f35d0215	no	41
Warnings:					
Information:					
3	Non Patent Literature	TrimmingAnalogCircuits.pdf	1598760 e6b1908a3c91b7efb1226da08e0a3516cf6cbf60	no	7
Warnings:					
Information:					
4	Non Patent Literature	18V_500MHz_10Output.pdf	205422 a2172f75a107fb0f2fcd1c59162791d54d060eaf	no	15
Warnings:					
Information:					
5	Non Patent Literature	10Gigabit_EthernetTechnology.pdf	4802570 30eccb47013933f982c7cd67de3438f0dbb1c4ae	no	22
Warnings:					
Information:					
6	Non Patent Literature	16K_DualPortStaticRAMwithSemIntBusy.pdf	409447 ba03668bb18d1d9397ac440b82a9e7d22615855d	no	16
Warnings:					
Information:					
7	Non Patent Literature	1Kx8_DualPortStaticRAM.pdf	312556 5a988114d0503d3ea80b0b4064e0529b2541e4ff	no	16
Warnings:					
Information:					
8	Non Patent Literature	1khzTo30mhz_ResistorSetSOT23Oscillator.pdf	971585 f7d41d0de53eebdba243778636f27a0ec7375288	no	5
Warnings:					
Information:					

9	Non Patent Literature	200MBaudHOTlinkTransceiver.pdf	17316096 35c7125950131de0f31f39e1e8e106106ead7ba8	no	62
Warnings:					
Information:					
10	Non Patent Literature	2Kx8_DualPort_StaticRM.pdf	2023436 c94e9251e214e3e89ff7f32296e32957abb64bda	no	8
Warnings:					
Information:					
11	Non Patent Literature	2Kx16_DualPort_St.pdf	1658622 67eb462043d0b438eb2822f8b3563189b7c337b5	no	7
Warnings:					
Information:					
12	Non Patent Literature	Takebuchi_NovelIntegrationTechPDF.pdf	745818 cb4c00e5327cb452598b75229a1acc1841022c2e	no	4
Warnings:					
Information:					
13	Non Patent Literature	Cho_NovelRobustLowCostStack.pdf	782770 a4832fdf15721cb0be2c06d232458ee105d28b46	no	10
Warnings:					
Information:					
14	Non Patent Literature	APlanarTypeEEPROM.pdf	599518 e171484b2f108ffd3d39b49fef7b657020421a40	no	4
Warnings:					
Information:					
15	Non Patent Literature	ASingleChipSensor.pdf	928992 4e77b95af87524a9c8061c9f7c4197357f20b1e5	no	4
Warnings:					
Information:					

16	Non Patent Literature	ASinglePolyEEPROMforCustom.pdf	351567 994ddd786a02d873de63de3f333ac9423b0801ef	no	4
Warnings:					
Information:					
17	Non Patent Literature	Alvarez_WideBandwidth.pdf	1170512 624bdf00c4b4e8fae585417ccca5e597cc91d337	no	2
Warnings:					
Information:					
18	Non Patent Literature	AboutSMaLCameraTechnologies.pdf	734160 355c8cf4fc6465e1b17b350ca5d756bd18691e3e	no	3
Warnings:					
Information:					
19	Non Patent Literature	AchievingUniformnMOSDevicePower.pdf	834390 06bbf5b7d8fd02cc83a547af308bc7d7ebf59fdb	no	4
Warnings:					
Information:					
20	Non Patent Literature	ADNS2030HighPerformanceOpticalMouseSensor.pdf	440822 d28eed31c140d9aaeb411bfe78152f3328e88fdf	no	2
Warnings:					
Information:					
21	Non Patent Literature	CD05144_adns_2051HighPerformance.pdf	89809 0daac443f57d870a6dfc7f64ca943574720cf449	no	2
Warnings:					
Information:					
22	Non Patent Literature	Agilent_ADNK_Solid_State_Optical_Mouse.pdf	98617 b84787855a666bd84f0e204024470e04c63eedb3	no	1
Warnings:					
Information:					

23	Non Patent Literature	Agilent_ADNK_2030_LowPower.pdf	2071249 fd36d867ad910a6cacbb413d38e943697240a62b	no	34
Warnings:					
Information:					
24	Non Patent Literature	Agilent_2051_Optical_Mouse.pdf	202566 024090b3258189bc488908bc43dbcee98c4dc838	no	2
Warnings:					
Information:					
25	Non Patent Literature	AgilentOpticalMouseSelectionGuide.pdf	506893 2e3560708341c44d31b464847997009063a0e40b	no	3
Warnings:					
Information:					
26	Non Patent Literature	AlgorithmForManagingMultipleFirstIn.pdf	1307372 b02d776b842781a16ba4f306917f5805a011c3fb	no	5
Warnings:					
Information:					
27	Non Patent Literature	Am99C10AContentAddressableMemory.pdf	8277596 27c1d1d84f8d848b2b7a86b791c139eede8c3e94	no	26
Warnings:					
Information:					
28	Non Patent Literature	AnAnalogPLL_basedClockAndDataRecoveryCircuitWithHighInputJitterTolerance.pdf	944137 1556c084579b66113fa0b7dfbf2573f242ac8357	no	6
Warnings:					
Information:					
29	Non Patent Literature	Cuppens_AnEEPROMforMicroprocessorsAndCustomLogic.pdf	3436269 72b12203e2f29592276ddca9749a7cadb4728b42	no	6
Warnings:					
Information:					

30	Non Patent Literature	Yoshikawa_AnEPROMcellStructure.pdf	1237223 17f9c0d992191de39d2e83e928e02074b390a011	no	5
Warnings:					
Information:					
31	Non Patent Literature	Miyamoto_AnExperimental5Vonly2565kbitCMOS.pdf	3264829 78876b7be1336949e2df86292b57fdfb04658e62	no	9
Warnings:					
Information:					
32	Non Patent Literature	PerformanceImprovementofSONOS.pdf	221031 a48a0747f9036b7024467d2ac4ed8a84ab3e62a1	no	3
Warnings:					
Information:					
33	Non Patent Literature	PM07002CIP2EP_EPExaminationReport_03302017.pdf	206037 734c0d7e0e68033eec453c843a4ec487b83b2f83	no	6
Warnings:					
Information:					
34	Non Patent Literature	PM07002CIP2EP_EPOOASearchReport_10202015.pdf	517858 be4762bfb5b27f5cda68cee6c3a93afd8c120d51	no	6
Warnings:					
Information:					
35	Other Reference-Patent/App/Search documents	PM07024WO_SearchReport_08262008.pdf	101902 f115d891db78267d5df70fcd5015c559c23e600c	no	2
Warnings:					
Information:					
36	Other Reference-Patent/App/Search documents	PM07002CIP1WO_SearchReport_05082012.pdf	97182 6a0af84d6d122c561389c4c063218fc7b71e3a88	no	2
Warnings:					
Information:					

37	Other Reference-Patent/App/Search documents	PM07002CIP2WO_SearchReport_05302013.pdf	97598 5b22b47d7aff411c319077c8764433ef6a490b02	no	2
Warnings:					
Information:					
38	Other Reference-Patent/App/Search documents	PM07024CIP1WO_SearchReport_07262013.pdf	165852 b1ceec7612ca1538578a533e8b8dd7406bf1b9dd	no	5
Warnings:					
Information:					
39	Other Reference-Patent/App/Search documents	PM07027D1CIP1WO_SearchReport_11142013.pdf	100980 033f94b04d20013304a99361ca6ad29fd1d75de2	no	2
Warnings:					
Information:					
40	Non Patent Literature	BESONOSABandgapEngineeredSONOS.pdf	347370 b0c342fb9e94ae97e2787c70c9693b8bd5889a1e	no	4
Warnings:					
Information:					
41	Non Patent Literature	ReliabilityModelofBandgap.pdf	344869 b3c6336c4f1c2a6fa3ea9c81c9c30a3177ce3a1a	no	4
Warnings:					
Information:					
42	Non Patent Literature	Milton_TheMaterialsScienceofThin.pdf	529640 9565b5d2e88cdab0e212164c9e9e04d2a2781d07	no	4
Warnings:					
Information:					
43	Non Patent Literature	PM07027D1CIP1CN_SIPOOA_01062017.pdf	256984 c05c26efa6dc55edb801c86f79607a0e72dfa440	no	8
Warnings:					
Information:					

44	Non Patent Literature	ReliabilityAndProcessingEffectsofBandgap.pdf	409962 ddcd494c28c55f6fde6d289bb1cdf43c780fc4b2	no	5
Warnings:					
Information:					
45	Other Reference-Patent/App/Search documents	PM07024WO_WrittenOpinion_08262008.pdf	278276 f7057c746786b6f2a0a16ad5c5c3b78cefb9def0	no	5
Warnings:					
Information:					
46	Other Reference-Patent/App/Search documents	PM07002CIP2WO_WrittenOpinion_05302013.pdf	468473 3bce20ee42e16de2dadf832c4ca0975962d1b713	no	7
Warnings:					
Information:					
47	Other Reference-Patent/App/Search documents	PM07024CIP1WO_WrittenOpinion_07262013.pdf	103429 55f053ad649cb33dae6701015fd27a9ee870243c	no	3
Warnings:					
Information:					
48	Other Reference-Patent/App/Search documents	PM07002CIP1WO_WrittenOpinion_05082012.pdf	172664 2e7ed43eb518c40507ac4f5cd345ed4fa29d134e	no	4
Warnings:					
Information:					
49	Other Reference-Patent/App/Search documents	PM07027D1CIP1WO_WrittenOpinion_11142013.pdf	500045 d79d916d47f9f184dbdcbdb471e125c310b0db14	no	7
Warnings:					
Information:					
50	Non Patent Literature	SONOSDeviceWithTaperedBandgap.pdf	489136 756ec4870ffeef25fb89c3d63261e4d14626d7b4	no	6
Warnings:					
Information:					

51	Non Patent Literature	Yang_ReliabilityConsiderations.pdf	1393330 27cf2dba4e64725ee701012d3d516c439a34a87d	no	8
Warnings:					
Information:					
			Total Files Size (in bytes):	74103066	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4667217	A	1987-05-19	Janning	Entire Document
	2	5773343	A	1998-06-30	Lee Sung et al.	Entire Document
	3	6001713	A	1999-12-14	Ramsbey et al.	Entire Document
	4	6518113	B1	2003-02-11	Buynoski	Entire Document
	5	6596590	B1	2003-07-22	Miura et al.	Entire Document
	6	6717860	B1	2004-04-06	Fujiwara	Entire Document
	7	7060594	B2	2006-06-13	Wang	Entire Document
	8	7279740	B2	2007-10-09	Bhattacharyya et al.	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	9	7646041	B2	2010-01-12	Chae et al.	Entire Document
	10	7692246	B2	2010-04-06	Dreeskornfeld et al.	Entire Document
	11	7927951	B2	2011-04-19	Kim et al.	Entire Document
	12	8008713	B2	2011-08-30	Dobuzinsky et al.	Entire Document
	13	8163660	B2	2012-04-24	Puchner et al.	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	2005093054		2005-05-05	Jung	Entire Document
	2	2005245034		2005-11-03	Fukuda et al.	Entire Document
	3	20060017092	A1	2006-01-26	Dong et al.	Entire Document
	4	20060051880	A	2006-03-09	Doczy et al.	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	5	20060081331	A1	2006-04-20	Campian	Entire Document
	6	20060228907	A1	2006-10-12	Cheng et al.	Entire Document
	7	2006113627		2006-06-01	Chen et al.	Entire Document
	8	2006220106	A	2006-10-05	Choi et al.	Entire Document
	9	20070012988	A	2007-01-18	Bhattacharyya	Entire Document
	10	20070272971	A	2007-11-29	Lee et al.	Entire Document
	11	20080087942	A1	2008-04-17	Hsu et al.	Entire Document
	12	20080237684	A1	2008-10-02	Specht et al.	Entire Document
	13	20080290398	A	2008-11-27	Polishchuk et al.	Entire Document
	14	2008150003		2008-06-26	Chen et al.	Entire Document
	15	2008237694		2008-10-02	Specht et al.	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	16	20090206385	A	2009-08-20	Kim et al.	Entire Document
	17	20090227116	A	2009-09-10	Joo Moon et al.	Entire Document
	18	20100252877	A1	2010-10-07	Nakanishi et al.	Entire Document

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	101517714	CN	A	2009-08-26	CYPRESS SEMICONDUCTOR CORP	Entire Document	
	2	101558481	CN	B	2012-05-30	Cypress Semiconductor Corporation	Entire Document	
	3	101859702	CN	A	2010-10-13	FREDERICK et al.	Entire Document	
	4	104254921	CN	A	2014-12-31	CYPRESS SEMICONDUCTOR CORP	Entire Document	
	5	1801478	CN	A	2006-07-12	TAIWAN SEMICONDUCTOR MFG	Entire Document	
	6	1832201	CN	A	2006-09-13	SAMSUNG ELECTRONICS CO LTD	Entire Document	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	7	2005347679	JP		2005-12-15	RENESAS TECH CORP	Entire Document	
	8	2007318112	JP		2007-12-06	SEMICONDUCTOR ENERGY LAB	Entire Document	
	9	2007515060	JP	A	2007-06-07	Unknown	Entire Document	
	10	2009260070	JP		2009-11-05	TOSHIBA CORP	Entire Document	
	11	20040070669	KR	A	2004-08-11	ANAM SEMICONDUCTOR LTD	Entire Document	
	12	20060100092	KR		2006-09-20	LEE CHANG WON	Entire Document	
	13	200703671	TW	A	2007-01-16	MICRON TECHNOLOGY INC	Entire Document	
	14	200847343	TW	A	2008-12-01	Jenne et al.	Entire Document	
	15	2007064048	WO	A1	2007-06-07	Masuzaki et al.	Entire Document	
	16	2008129478	WO	A	2008-10-30	Huerta et al.	Entire Document	
	17	2011162725	WO	A1	2011-12-29	Singh et al.	Entire Document	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	18	2013148112	WO	A1	2013-10-03	Jenne et al.	Entire Document	
	19	2013148343	WO	A1	2013-10-03	Levy et al.	Entire Document	

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	Chinese Office Action for Application Number 200880000820.3 (PM07024CN) dated 01/26/2011; 6 pages	
	2	SIPO Office Action for CN Application Number 201380031969.9 (PM07024CIP1CN) dated 08/19/2016; 8 pages	
	3	USPTO Advisory Action for Application Number 12/197,466 (PM07024C1) dated 01/31/2012; 3 pages	
	4	USPTO Advisory Action for Application Number 14/605,231 (PM07024CIP1C1) dated 03/09/2016; 3 pages	
	5	USPTO Advisory Action for Application Number 14/605,231 (PM07024CIP1C1) dated 07/05/2016; 3 pages	
	6	USPTO Final Rejection for Application Number 12/124,855 (PM07024) dated 01/31/2012; 7 pages	
	7	USPTO Final Rejection for Application Number 12/124,855 (PM07024) dated 05/10/2010; 11 pages	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	8	USPTO Final Rejection for Application Number 12/197,466 (PM07024C1) dated 11/17/2011; 13 pages	
	9	USPTO Final Rejection for Application Number 14/307,858 (PM07027D1C1) dated 10/08/2015; 6 pages	
	10	USPTO Final Rejection for Application Number 14/605,231 (PM07024CIP1C1) dated 12/17/2015; 15 pages	
	11	USPTO Non Final Rejection for Application Number 13/539,458 (PM07024CIP1) dated 03/13/2013; 5 pages	
	12	USPTO Non Final Rejection for Application Number 13/539,458 (PM07024CIP1) dated 10/2/2014; 5 pages	
	13	USPTO Non Final Rejection for Application Number 13/620,071 (PM07024C2) dated 04/03/2014; 12 pages	
	14	USPTO Non Final Rejection for Application Number 13/620,071 (PM07024C2) dated 07/18/2014; 5 pages	
	15	USPTO Non-Final Rejection for Application Number 12/124,855 (PM07024) dated 01/18/2011; 5 pages	
	16	USPTO Non-Final Rejection for Application Number 12/124,855 (PM07024) dated 08/16/2011; 9 pages	
	17	USPTO Non-Final Rejection for Application Number 12/124,855 (PM07024) dated 10/29/2009; 9 pages	
	18	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 03/09/2011; 4 pages	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	19	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 09/29/2010; 5 pages	
	20	USPTO Non-Final Rejection for Application Number 12/197,466 (PM07024C1) dated 06/01/2011; 11 pages	
	21	USPTO Non-Final Rejection for Application Number 13/288,919 (PM07027D1) dated 06/19/2014; 5 pages	
	22	USPTO Non-Final Rejection for Application Number 13/288,919 (PM07027D1) dated 12/05/2013; 4 pages	
	23	USPTO Non-Final Rejection for Application Number 13/539,466 (PM07027D1CIP1) dated 09/28/2012; 9 pages	
	24	USPTO Non-Final Rejection for Application Number 14/159,315 (PM07027D1CIP1C1) dated 10/21/2014; 12 pages	
	25	USPTO Non-Final Rejection for Application Number 14/307/858 (PM07027D1C1) dated 06/29/2015; 5 pages	
	26	USPTO Non-Final Rejection for Application Number 14/605,231 (PM07024CIP1C1) dated 07/07/2015; 13 pages	
	27	USPTO Notice of Allowance for Application Number 12/124,855 (PM07024) dated 05/01/2012; 7 pages	
	28	USPTO Notice of Allowance for Application Number 12/124,855 (PM07024) dated 05/03/2011; 7 pages	
	29	USPTO Notice of Allowance for Application Number 12/124,855 (PM07024) dated 07/28/2010; 6 pages	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	30	USPTO Notice of Allowance for Application Number 12/124,855 (PM07024) dated 08/01/2012; 7 pages	
	31	USPTO Notice of Allowance for Application Number 12/152,518 (PM07027) dated 07/14/2011; 6 pages	
	32	USPTO Notice of Allowance for Application Number 12/197,466 (PM07024C1) dated 06/15/2012; 4 pages	
	33	USPTO Notice of Allowance for Application Number 12/197,466 (PM07024C1) dated 09/24/2012; 8 pages	
	34	USPTO Notice of Allowance for Application Number 13/288,919 (PM07027D1) dated 04/28/2014; 5 pages	
	35	USPTO Notice of Allowance for Application Number 13/288,919 (PM07027D1) dated 07/08/2014; 5 pages	
	36	USPTO Notice of Allowance for Application Number 13/288,919 (PM07027D1) dated 08/26/2014; 7 pages	
	37	USPTO Notice Of Allowance for Application Number 13/539,458 (PM07024CIP1) dated 05/24/2013; 8 pages	
	38	USPTO Notice of Allowance for Application Number 13/539,458 (PM07024CIP1) dated 08/04/2014; 7 pages	
	39	USPTO Notice of Allowance for Application Number 13/539,458 (PM07024CIP1) dated 11/03/2014; 7 pages	
	40	USPTO Notice Of Allowance for Application Number 13/539,466 (PM07027D1CIP1) dated 09/04/2013; 9 pages	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

If you wish to add additional non-patent literature document citation information please click the Add button	Add		
EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kin Hung Lai/	Date (YYYY-MM-DD)	2017-04-24
Name/Print	Kin Hung Lai	Registration Number	69251

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Espacenet

Bibliographic data: CN101517714 (A) — 2009-08-26

Sonos ono stack scaling

Inventor(s): SAGY LEVY [US] ± (LEVY SAGY, ; JENNE FREDRICK B)

Applicant(s): CYPRESS SEMICONDUCTOR CORP [US] ± (CYPRESS SEMICONDUCTOR CORP)

Classification: **- international:*H01L21/31***
- cooperative: **H01L21/28282**; **H01L21/3143**; **H01L29/4234**; **H01L29/4916**; **H01L29/512**; **H01L29/513**; **H01L29/518**; **H01L29/792**

Application number: CN2007835963 20070928

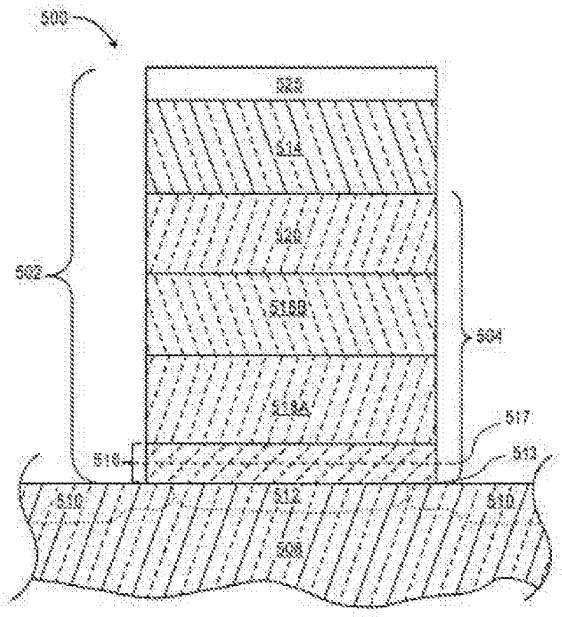
Priority number (s): WO2007US20966 20070928 ; US20070940384P 20070525 ; US20070904506 20070926

Also published as: CN101517714 (B) US2008290400 (A1) US8614124 (B2) US9349877 (B1) WO2008147386 (A1) more

Abstract of CN101517714 (A)

The invention relates to scaling a nonvolatile trapped-charge memory device. In an embodiment, scaling includes multiple oxidation and nitridation operations to provide a tunneling layer with a dielectric constant higher than that of a pure silicon dioxide tunneling layer but with a fewer hydrogen and nitrogen traps than a tunneling layer having nitrogen at the substrate interface. In an embodiment, scaling includes forming a charge trapping layer with a non-homogenous oxynitride stoichiometry. In one embodiment the charge trapping layer includes a silicon-rich, oxygen-rich layer and a silicon-rich, oxygen-lean oxynitride layer on the silicon-rich, oxygen-rich layer. In an embodiment, the method for scaling includes a dilute wet oxidation to density a deposited blocking oxide and to oxidize a portion of the silicon-rich, oxygen-lean oxynitride layer.

Sandisk Technologies, Inc. - Ex. 1002, Page 000632



Sandisk Technologies, Inc. - Ex. 1002, Page 000633

Espacenet

Bibliographic data: CN101558481 (A) — 2009-10-14

Radical oxidation process for fabricating a nonvolatile charge trap memory device

Inventor(s): KRISHNASWAMY RAMKUMAR [US] ± (RAMKUMAR KRISHNASWAMY)

Applicant(s): CYPRESS SEMICONDUCTOR CORP [US] ± (CYPRESS SEMICONDUCTOR CORP)

Classification: - international:*H01L21/336*
- cooperative: **H01L21/28282**; **H01L21/3144**; **H01L21/3145**; **H01L29/4234**; H01L29/66833

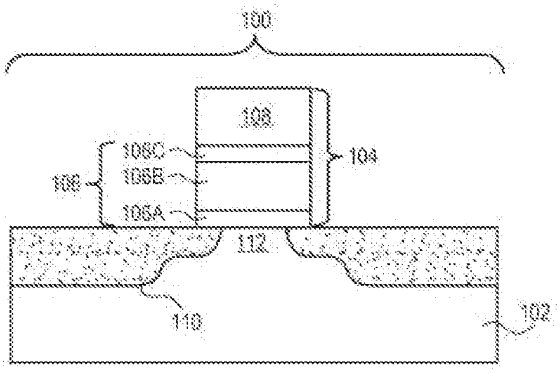
Application number: CN2008800820 20080523

Priority number (s): US20070986637P 20071109 ; US20070940139P 20070525 ; WO2008US06627 20080523 ; US20080124855 20080521

Also published as: CN101558481 (B) US2008293255 (A1) US8283261 (B2) US8993453 (B1) WO2008147541 (A1) more

Abstract of CN101558481 (A)

A method for fabricating a nonvolatile charge trap memory device is described. The method includes providing a substrate having a charge-trapping layer disposed Thereon. A portion of the charge-trapping layer is then oxidized to form a blocking Dielectric layer above the charge-trapping layer by exposing the charge-trapping layer to a radical oxidation process.



Sandisk Technologies, Inc. - Ex. 1002, Page 000634

Espacenet

Bibliographic data: CN101859702 (A) — 2010-10-13

Oxide-nitride-oxide stack containing a plurality of oxynitrides layers

Inventor(s): JANA FREDERICK; KUMAR KRISHNASWAMY; JIHA SAM; LIVER SEGE ± (FREDERICK JANA, ; KRISHNASWAMY KUMAR, ; SAM JIHA, ; SEGE LIVER)

Applicant(s): CYPRESS SEMICONDUCTOR CORP ± (CYPRESS SEMICONDUCTOR CORPORATION)

Classification: **- international:** ***C23C16/44; H01L21/283; H01L21/316; H01L29/423; H01L29/792***

- cooperative:

Application number: CN20091134374 20090410

Priority number (s): CN20091134374 20090410

Also published as: CN101859702 (B)

Abstract of CN101859702 (A)

The invention discloses a semiconductor device of an oxide-nitride-oxide (ONO) stack containing a plurality of charge storage layers and a forming method thereof. Generally, the method comprises the following steps of: firstly, forming a first oxide layer on an ONO structure; secondly, forming the plurality of charge storage layers containing nitride on the first oxide layer; and thirdly, forming a second oxide layer in the ONO structure on the plurality of charge storage layers. Preferably, each charge storage layer comprises at least two silicon oxynitride layers with two chemical constitutional ratios of oxygen, nitrogen and/or silicon. More preferably, the ONO structure is a part of a silicon-oxide-nitride-oxide-silicon (SONOS) structure, and the semiconductor device is an SONOS memory transistor.

Sandisk Technologies, Inc. - Ex. 1002, Page 000635

Espacenet

Bibliographic data: CN104254921 (A) — 2014-12-31

SONOS STACK WITH SPLIT NITRIDE MEMORY LAYER

Inventor(s): JENNE FREDRICK; RAMKUMAR KRISHNASWAMY ± (JENNE FREDRICK, ; RAMKUMAR KRISHNASWAMY)

Applicant(s): CYPRESS SEMICONDUCTOR CORP ± (CYPRESS SEMICONDUCTOR CORPORATION)

Classification: **- international:*H01L29/792***
- cooperative: **B82Y10/00**; **H01L21/28282**; **H01L27/11582**; **H01L29/0673**; **H01L29/0676**; **H01L29/42348**; **H01L29/513**; **H01L29/518**; **H01L29/66439**; **H01L29/66833**; **H01L29/775**; **H01L29/792**; **H01L29/7926**; H01L29/785 more

Application number: CN2013816882 20130308 Global Dossier

Priority number(s): WO2013US29784 20130308 ; US201213431069 20120327

Also published as: WO2013148112 (A1) TW201349505 (A) KR20140147083 (A) JP2015517211 (A) EP2831916 (A1) more

Abstract of CN104254921 (A)

Embodiments of a non-planar memory device including a split charge-trapping region and methods of forming the same are described. Generally, the device comprises: a channel formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide overlying the channel; a split charge-trapping region overlying the tunnel oxide, the split charge-trapping region including a bottom charge-trapping layer comprising a nitride closer to the tunnel oxide, and a top charge-trapping layer, wherein the bottom charge-trapping layer is separated from the top charge-trapping layer by a thin anti-tunneling layer comprising an oxide. Other embodiments are also disclosed.

Sandisk Technologies, Inc. - Ex. 1002, Page 000636

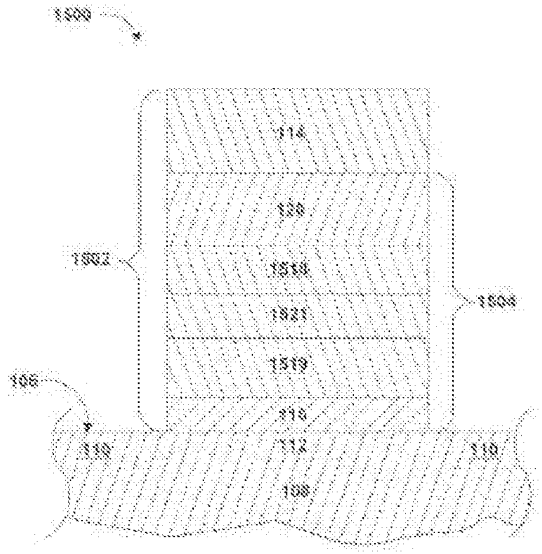


FIG. 11

Sandisk Technologies, Inc. - Ex. 1002, Page 000637

Espacenet

Bibliographic data: CN1801478 (A) — 2006-07-12

Semiconductor devices, semiconductor nano-wire devices and methods of fabrication the same

Inventor(s): CHEN HUNG-WEI YEO [CN] ± (HUNG-WEI,YEO CHEN, ; HU CHENMING)

Applicant(s): TAIWAN SEMICONDUCTOR MFG [CN] ± (TAIWAN SEMICONDUCTOR MFG)

Classification: - international: ***B82B3/00; H01L21/00; H01L21/324; H01L21/336; H01L21/84; H01L29/423; H01L29/786; H01L29/788***
- cooperative: **B82B3/00; B82Y10/00; H01L21/324; H01L29/0673; H01L29/42384; H01L29/42392; H01L29/66795; H01L29/7854; H01L29/78645; H01L29/78696**

Application number: CN2005175664 20050610

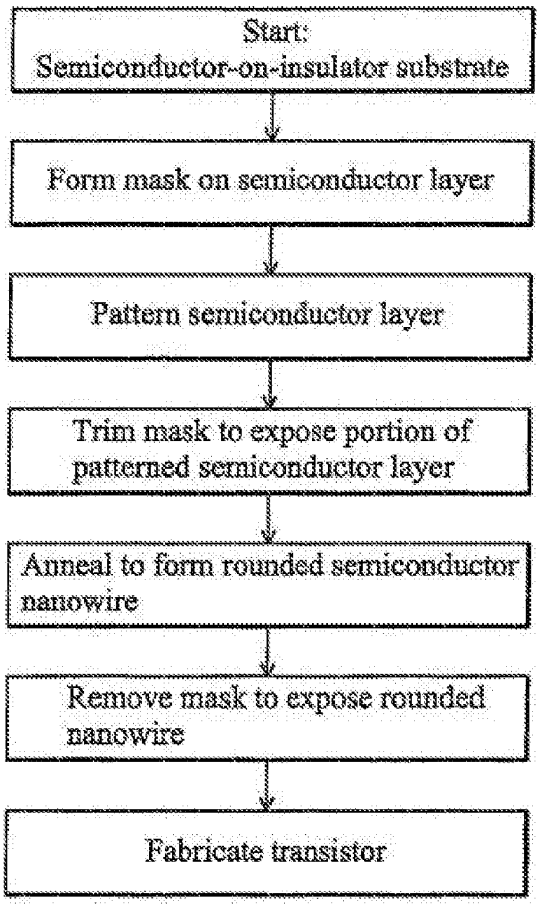
Priority number (s): US20040578673P 20040610

Also published as: CN100428446 (C) US2005275010 (A1) US7452778 (B2) TW200610004 (A) TWI282582 (B)

Abstract not available for CN1801478 (A)
Abstract of corresponding document: US2005275010 (A1)

Nano-wires, preferably of less than 20 nm diameter, can be formed with minimized risk of narrowing and breaking that results from silicon atom migration during an annealing process step. This is accomplished by masking portion of the active layer where silicon atomer would otherwise agglomerate with a material such as silicon dioxide, silicon nitride, or other dielectric that eliminates or substantially reduces the silicon atom migration. Nano-wires, nanotubes, nano-rods, and other features can be formed and can optionally be incorporated into devices, such as by use as a channel region in a transistor device.

Sandisk Technologies, Inc. - Ex. 1002, Page 000638



Sandisk Technologies, Inc. - Ex. 1002, Page 000639

Espacenet

Bibliographic data: CN1832201 (A) — 2006-09-13

Non-volatile memory possessing a plurality of capture film

Inventor(s): NYON-SEOG GEUM CHOO-HAENG HAHN [KR] ± (GEUM CHOO-HAENG,HAHN CHONG-HEE,GEUM CHONG-WOO,MINYUE-SAI,GEUM MOON-GYONG,CHEONG NYON-SEOG)

Applicant(s): SAMSUNG ELECTRONICS CO LTD [KR] ± (SAMSUNG ELECTRONICS CO., LTD)

Classification: **- international:** ***H01L27/115; H01L29/792***
- cooperative: **H01L29/4232**; **H01L29/42324**; **H01L29/513**; **H01L29/7881**; **H01L29/792**

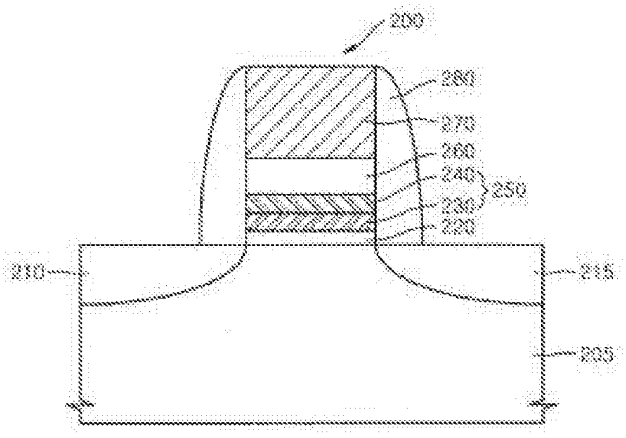
Application number: CN2006104393 20060216

Priority number(s): KR20050012914 20050216

Also published as: US2006255399 (A1) JP2006229233 (A) KR20060091649 (A) KR100652401 (B1)

Abstract not available for CN1832201 (A)
Abstract of corresponding document: US2006255399 (A1)

Provided is a nonvolatile memory device which includes a tunneling insulating film formed on a semiconductor substrate, a storage node formed on the tunneling insulating film, a blocking insulating film formed on the storage node, and a control gate electrode formed on the blocking insulating film. The storage node includes at least two trapping films having different trap densities, and the blocking insulating film has a dielectric constant greater than that of the silicon oxide film.



Espacenet

Bibliographic data: JP2005347679 (A) — 2005-12-15

METHOD OF MANUFACTURING NONVOLATILE SEMICONDUCTOR MEMORY

Inventor(s): HAMAMURA HIROTAKA; MINE TOSHIYUKI; YOKOYAMA NATSUKI ± (HAMAMURA HIROTAKA, ; MINE TOSHIYUKI, ; YOKOYAMA NATSUKI)

Applicant(s): RENESAS TECH CORP ± (RENESAS TECHNOLOGY CORP)

Classification: **- international:** ***H01L21/28; H01L21/336; H01L21/8238; H01L21/8247; H01L27/10; H01L27/115; H01L29/423; H01L29/51; H01L29/788; H01L29/792;*** (IPC1-7): H01L21/8247; H01L27/10; H01L27/115; H01L29/788; H01L29/792

- cooperative: **H01L21/28282**; **H01L29/42344**; **H01L29/513**; **H01L29/792**

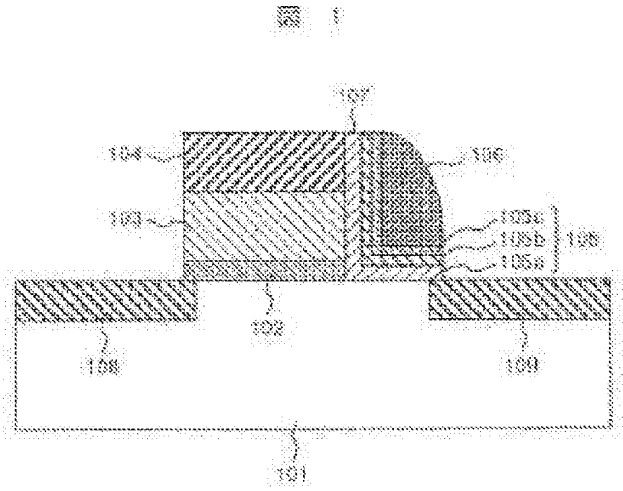
Application number: JP20040168325 20040607

Priority number(s): JP20040168325 20040607

Also published as: JP4477422 (B2) US2005272198 (A1) US7682990 (B2)

Abstract of JP2005347679 (A)

PROBLEM TO BE SOLVED: To solve such a problem that former in a MONOS type nonvolatile memory, a top silicon oxide film having an ONO structure was formed by an ISSG oxidation of a silicon nitride film, however, when an ISSG oxidation condition becomes strong, an interface state density (Dit) and an electron trap density increase with rewriting, and an ON current of sufficient values cannot be obtained, and consequently a deterioration of a charge retention property cannot be suppressed. SOLUTION: A method of manufacturing a nonvolatile semiconductor memory comprises the steps of: oxidizing the silicon nitride film by using a high concentration ozone gas; and forming the top silicon oxide film. ;COPYRIGHT: (C)2006,JPO&NCIPI


107
104
106
103
105a
105b
105c
105
102
108
109
101

Espacenet

Bibliographic data: JP2007318112 (A) — 2007-12-06

SEMICONDUCTOR DEVICE, AND METHOD OF FABRICATING SEMICONDUCTOR DEVICE

Inventor(s): ISOBE ATSUO; TAKANO TAMAE; ARAI YASUYUKI; TERASAWA IKUKO ± (ISOBE ATSUO, ; TAKANO TAMAE, ; ARAI YASUYUKI, ; TERASAWA IKUKO)

Applicant(s): SEMICONDUCTOR ENERGY LAB ± (SEMICONDUCTOR ENERGY LAB CO LTD)

Classification: **- international:** ***H01L21/336; H01L21/76; H01L21/762; H01L21/8247; H01L27/115; H01L29/786; H01L29/788; H01L29/792***

- cooperative:

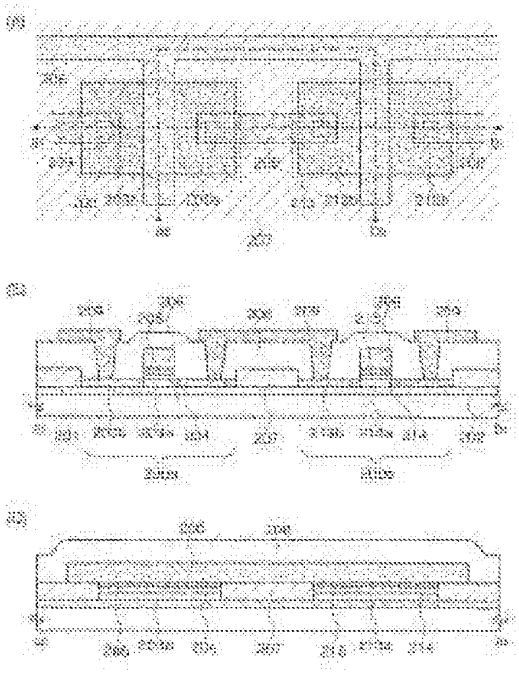
Application number: JP20070116797 20070426

Priority number(s): JP20060126636 20060428 ; JP20070116797 20070426

Also published as: JP5285235 (B2)

Abstract of JP2007318112 (A)

PROBLEM TO BE SOLVED: To reduce an influence that the characteristic of an end portion of a channel forming region of a semiconductor film affects on the characteristic of a transistor. ;SOLUTION: A semiconductor film, a gate insulating film, and a first conductive film are sequentially laminated on a substrate to form a laminate, and by removing the laminate, a plurality of laminates are provided in an island shape, then an insulating film is formed so as to cover the laminate provided in an island shape. Then, a part of the insulating film is removed so that its height is approximately equal to the height of the surface of the first conductive film to expose the surface of the first conductive film, and a second conductive film is formed on the first insulating film and on a remaining first insulating film. Then a resist is formed on the second conductive film, and the first conductive film and the second conductive film are selectively removed, with the resist as a mask. ;COPYRIGHT: (C)2008,JPO&INPIT



Espacenet

Bibliographic data: JP2007515060 (A) — 2007-06-07

Thermal chemical vapor deposition of silicon nitride using BTBAS bis(tertiary-butylamino silane) in a single wafer chamber

Inventor(s):

Applicant(s):

Classification:	**- international:**	***C23C16/00; C23C16/34; C23C16/42; C23C16/44; C23C16/455; H01L21/31; H01L21/318***
	- cooperative:	**C23C16/345; C23C16/4412; C23C16/45565; C23C16/4557**
Application number:	JP20060541132 20040825	
Priority number(s):	WO2004US27584 20040825 ; US20030525241P 20031125 ; US20040911208 20040804	
Also published as:	JP4801591 (B2) US2005109276 (A1) WO2005059200 (A1) US2006102076 (A1) KR20110139323 (A) more	

Abstract not available for JP2007515060 (A)
Abstract of corresponding document: US2005109276 (A1)

A method and apparatus for a CVD chamber that provides uniform heat distribution, efficient precursor delivery, uniform distribution of process and inert chemicals, and thermal management of residues in the chamber and exhaust surfaces by changing the mechanical design of a single wafer thermal CVD chamber. The improvements include a processing chamber comprising a chamber body and a chamber lid defining a processing region, a substrate support disposed in the processing region, a gas delivery system mounted on the chamber lid, the gas delivery system comprising a lid, an adapter ring and two blocker plates that define a gas mixing region, and a face plate fastened to the adapter ring, a heating element positioned to heat the adapter ring to a desired temperature, and a temperature controlled exhaust system. The improvements also include a method for depositing a silicon nitride layer on a substrate, comprising vaporizing bis(tertiary-butylamino) silane, flowing the bis(tertiary-butylamino) silane into a processing chamber, flowing ammonia into a processing chamber, combining the two reactants in a mixer in the chamber lid, having an additional mixing region defined by an adapter ring and at least two blocker plates, heating the adapter ring, flowing the bis(tertiary-butylamino) silane through a gas distribution plate into a processing region above a substrate. The improvements reduce defects across the surface of the

substrate and improve product yield.

Espacenet

Bibliographic data: JP2009260070 (A) — 2009-11-05

SEMICONDUCTOR DEVICE, AND METHOD OF MANUFACTURING THE SAME

Inventor(s): OZAWA YOSHIO; FUJITSUKA RYOTA ± (OZAWA YOSHIO, ; FUJITSUKA RYOTA)

Applicant(s): TOSHIBA CORP ± (TOSHIBA CORP)

Classification: **- International:** ***H01L21/8247; H01L27/115; H01L29/788; H01L29/792***
- cooperative: **H01L27/11568**; **H01L29/513**; H01L29/78

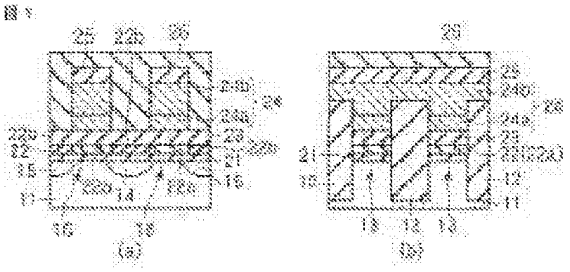
Application number: JP20080108048 20080417

Priority number(s): JP20080108048 20080417

Also published as: JP5238332 (B2) US2009261400 (A1) US8278696 (B2)

Abstract of JP2009260070 (A)

PROBLEM TO BE SOLVED: To provide a semiconductor device that can effectively prevent migration of charges between adjacent memory cells. ;SOLUTION: A semiconductor device includes a tunnel insulating film 21 formed on a semiconductor substrate 11, a charge storage insulating film 22 formed on the tunnel insulating film and including at least two separated low oxygen concentration portions 22a and a high oxygen concentration portion 22b positioned between the adjacent low oxygen concentration portions and having a higher oxygen concentration than the low oxygen concentration portions, a charge block insulating film 23 formed on the charge storage insulating film, and control gate electrodes 24 formed on the charge block insulating film and above the low oxygen concentration portions. ;COPYRIGHT: (C)2010,JPO&INPIT



Espacenet

Bibliographic data: KR20040070669 (A) — 2004-08-11

METHOD FOR IMPROVING RETENTION CHARACTERISTIC OF SONONOS ELEMENT OF QUANTUM TRAP DEVICE

Inventor(s): JUNG JIN HYO ± (JUNG, JIN HYO)

Applicant(s): ANAM SEMICONDUCTOR LTD ± (ANAM SEMICONDUCTOR., LTD)

Classification: **- international:** ***H01L27/115;*** (IPC1-7): H01L27/115
- cooperative:

Application number: KR20030006848 20030204 Global Dossier

Priority number(s): KR20030006848 20030204

Also published as: KR100501457 (B1)

Abstract of KR20040070669 (A)

PURPOSE: A method for improving a retention characteristic of a SONONOS element of a quantum trap device is provided to improve a program/erase characteristic by using a tunnel ring of a tunnel oxide layer. CONSTITUTION: A tunnel oxide layer(102) is formed on a lateral part of a silicon substrate. A buffer nitride layer(103) is inserted into a lateral part of the tunnel oxide layer. A buffer oxide layer(104) is inserted into a lateral part of the buffer nitride layer. A block oxide layer(106) is inserted into a lateral part of the buffer oxide layer. A program/erase characteristic is improved by a tunnel ring of the tunnel oxide layer. A retention characteristic is improved by using the tunnel ring of the tunnel oxide layer.

Sandisk Technologies, Inc. - Ex. 1002, Page 000649

DERWENT-ACC-NO: 2007-279666

DERWENT-WEEK: 200727

Copyright ©2014 Thomson Reuters

TITLE: Method for manufacturing semiconductor device capable of

improving leakage current characteristics

INVENTOR: LEE C W; SOHN W H ; YOUN S P

PATENT-ASSIGNEE: SAMSUNG

Sandisk Technologies, Inc. - Ex. 1002, Page 000650

ELECTRONICS CO LTD[SMSU]

PRIORITY-DATA: 2005KR-021739 (March 16, 2005)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
KR 2006100092 A	September 20, 2006	KO

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2006100092A	N/A	2005KR-021739	March 16, 2005

INT-CL-CURRENT:

TYPE	IPC	DATE
CIPP	H01L21/8247	20060101

ABSTRACTED-PUB-NO: KR 2006100092 A

BASIC-ABSTRACT:

NOVELTY - A method for manufacturing a semiconductor device is provided to improve operation characteristics and to enhance leakage current characteristics by using an improved gate structure.

DESCRIPTION - A gate structure (116) is formed on

a substrate (100). The gate structure is composed of an oxide pattern and a conductive pattern. A blocking oxide layer (126) is formed on the gate structure by performing a plasma oxidation on the gate structure under oxygen radical atmosphere. A blocking **oxynitride layer (128) is formed on the blocking oxide** layer by performing a nitrification process on the blocking oxide layer.

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: METHOD

Sandisk Technologies, Inc. - Ex. 1002, Page 000653

MANUFACTURE SEMICONDUCTOR DEVICE CAPABLE IMPROVE LEAK CURRENT CHARACTERISTIC

DERWENT-CLASS: L03 U11 U13

CPI-CODES: L04-C12A; L04-C12B;

EPI-CODES: U11-C05B5; U11-C05B7; U13-C04;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: 2007-102433

Sandisk Technologies, Inc. - Ex. 1002, Page 000654

Espacenet

Bibliographic data: TW200703671 (A) — 2007-01-16

High density NAND non-volatile memory device

Inventor(s): BHATTACHARYYA ARUP [US] + (BHATTACHARYYA, ARUP)

Applicant(s): MICRON TECHNOLOGY INC [US] + (MICRON TECHNOLOGY, INC)

Classification: - international: *H01L29/788*
- cooperative: G11C16/0483; H01L21/28273; H01L27/115; H01L27/11521; H01L27/11524; H01L27/11568; H01L29/4232; H01L29/42336; H01L29/513; H01L29/7881; H01L29/792; G11C16/0475

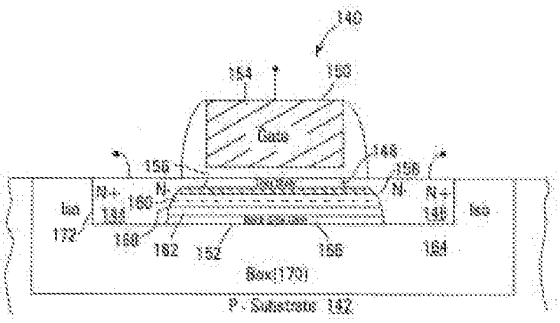
Application number: TW20060124840 20060707

Priority number (s): US20050181345 20050714

Also published as: TWI314361 (B) US2007012988 (A1) US7829938 (B2) WO2007011582 (A2) WO2007011582 (A3) more

Abstract of TW200703671 (A)

Non-volatile memory devices and arrays are described that utilize dual gate (or back-side gate) non-volatile memory cells with band engineered gate-stacks that are placed above or below the channel region in front-side or back-side charge trapping gate-stack configurations in NAND memory array architectures. The band-gap engineered gate-stacks with asymmetric or direct tunnel barriers of the floating node memory cells of embodiments of the present invention allow for low voltage tunneling programming and efficient erase with electrons and holes, while maintaining high charge blocking barriers and deep carrier trapping sites for good charge retention. The memory cell architecture also allows for improved high density memory devices or arrays with the utilization of reduced feature word lines and vertical select gates.



Sandisk Technologies, Inc. - Ex. 1002, Page 000655

Sandisk Technologies, Inc. - Ex. 1002, Page 000656

Espacenet

Bibliographic data: TW200847343 (A) — 2008-12-01

SONOS ONO stack scaling

Inventor(s): JENNE FREDRICK B [US]; LEVY SAGY [IL] ± (JENNE, FREDRICK B, ; LEVY, SAGY)

Applicant(s): CYPRESS SEMICONDUCTOR CORP [US] ± (CYPRESS SEMICONDUCTOR CORPORATION)

Classification: **- international:** ***H01L21/8247; H01L27/115***
- cooperative: **H01L21/28282**; **H01L21/3143**; **H01L29/513**; **H01L29/792**

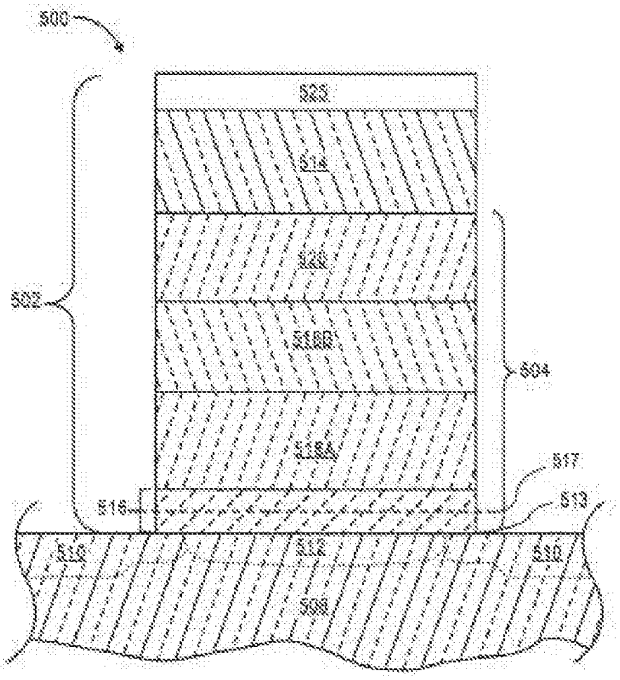
Application number: TW20070136630 20070929

Priority number(s): US20070940384P 20070525 ; US20070904506 20070926

Also published as: TWI436455 (B) US2008290400 (A1) US8614124 (B2) WO2008147386 (A1) US2009032863 (A1) more

Abstract of TW200847343 (A)

Scaling a nonvolatile trapped-charge memory device and the article made thereby. In an embodiment, scaling includes multiple oxidation and nitridation operations to provide a tunneling layer with a dielectric constant higher than that of a pure silicon dioxide tunneling layer but with a fewer hydrogen and nitrogen traps than a tunneling layer having nitrogen at the substrate interface. In an embodiment, scaling includes forming a charge trapping layer with a non-homogenous oxynitride stoichiometry. In one embodiment the charge trapping layer includes a silicon-rich, oxygen-rich layer and a silicon-rich, oxygen-lean oxynitride layer on the silicon-rich, oxygen-rich layer. In an embodiment, the method for scaling includes a dilute wet oxidation to densify a deposited blocking oxide and to oxidize a portion of the silicon-rich, oxygen-lean oxynitride layer.


500
523
514
520
518D
518A
502
504
517
513
516
512
510
508

Espacenet

Bibliographic data: WO2007064048 (A1) — 2007-06-07

SEMICONDUCTOR STORAGE DEVICE, METHOD FOR DRIVING SAME, AND METHOD FOR MANUFACTURING SAME

Inventor(s): SUNAMURA HIROSHI [JP]; MASUZAKI KOUJI [JP]; TERAI MASAYUKI [JP] ± (SUNAMURA, HIROSHI, ; MASUZAKI, KOUJI, ; TERAI, MASAYUKI)

Applicant(s): NEC CORP [JP]; SUNAMURA HIROSHI [JP]; MASUZAKI KOUJI [JP]; TERAI MASAYUKI [JP] ± (NEC CORPORATION, ; SUNAMURA, HIROSHI, ; MASUZAKI, KOUJI, ; TERAI, MASAYUKI)

Classification: **- international:** ***H01L21/8247; H01L27/115; H01L29/788; H01L29/792***
- cooperative: **G11C16/0466; H01L21/28282; H01L29/4234; H01L29/42344; H01L29/792**

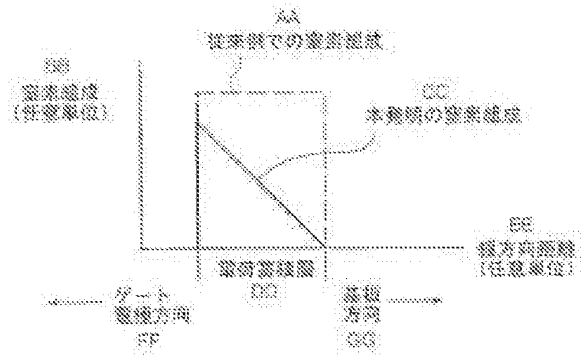
Application number: WO2006JP324506 20061201

Priority number(s): JP20050348677 20051202

Also published as: US2009316484 (A1) US7821823 (B2)

Abstract of WO2007064048 (A1)

Disclosed is a semiconductor storage device comprising a semiconductor substrate, a first and a second impurity diffusion layer formed in the semiconductor substrate, a gate insulating film formed on the semiconductor substrate, and a first gate electrode formed on the semiconductor substrate via the gate insulating film. The gate insulating film has a nitrogen-containing silicon oxide film inside, and a silicon oxide film is so arranged on both sides of the nitrogen-containing silicon oxide film as to sandwich the nitrogen-containing silicon oxide film. In addition, the nitrogen composition in the nitrogen-containing silicon oxide film is increased from the semiconductor substrate side to the first gate electrode side.



AA NITROGEN COMPOSITION OF CONVENTIONAL EXAMPLE
BB NITROGEN COMPOSITION (ARBITRARY UNIT)
CC NITROGEN COMPOSITION OF PRESENT INVENTION
DD CHARGE STORAGE LAYER
EE DISTANCE IN LENGTHWISE DIRECTION (ARBITRARY UNIT)
FF DIRECTION TO GATE ELECTRODE
GG DIRECTION TO SUBSTRATE

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 October 2008 (30.10.2008)

PCT

(10) International Publication Number
WO 2008/129478 A1

(51) International Patent Classification:
H01L 21/28 (2006.01) *H01L 29/792* (2006.01)
H01L 21/336 (2006.01) *G11C 16/04* (2006.01)
H01L 21/8246 (2006.01) *H01L 29/423* (2006.01)
H01L 21/8247 (2006.01) *H01L 29/06* (2006.01)
H01L 27/115 (2006.01) *H01L 29/78* (2006.01)
H01L 29/788 (2006.01)

(21) International Application Number:
PCT/IB2008/051478

(22) International Filing Date: 17 April 2008 (17.04.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
07106502.3 19 April 2007 (19.04.2007) EP

(71) Applicant *(for all designated States except US)*: **NXP B.V.** [NL/NL]; High Tech Campus 60, NL-NL - 5656 AG Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **BUERTA, Almudena** [ES/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **VAN DUUREN, Michiel Jos** [NL/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **AKIL, Nader** [FR/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **GOLUBOVIC, Dusan** [RS/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **BOUTCHICH, Mohamed** [FR/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT).

(74) Agents: **BÖGGLA, Harald** et al.; NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

[Continued on next page]

(54) Title: NONVOLATILE MEMORY CELL COMPRISING A NANOWIRE AND MANUFACTURING METHOD THEREOF

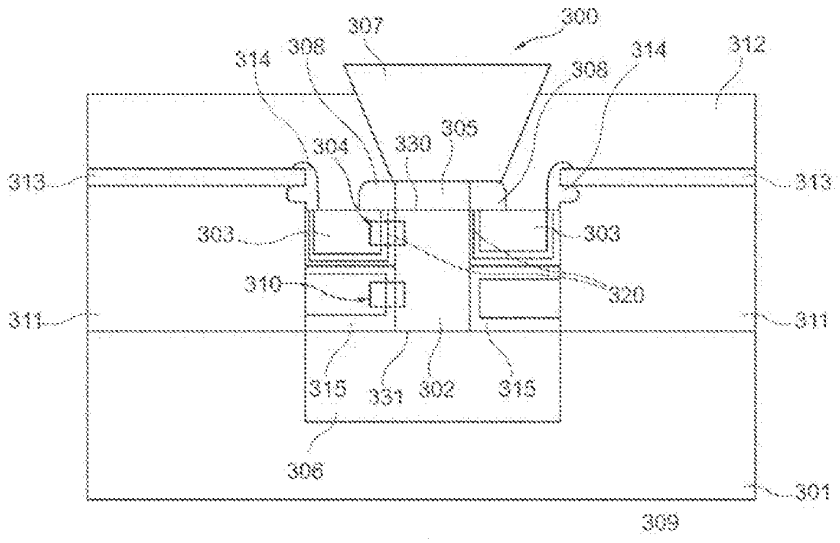


FIG. 3

(57) Abstract: A memory cell (300, 500), the memory cell (300, 500) comprising a substrate (301), a nanowire (302) extending along a vertical trench formed in the substrate (301), a control gate (303) surrounding the nanowire (302), and a charge storage structure (320, 501) formed between the control gate (303) and the nanowire (302).

WO 2008/129478 A1

Sandisk Technologies, Inc. - Ex. 1002, Page 000661

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

NONVOLATILE MEMORY CELL COMPRISING A NANOWIRE AND MANUFACTURING METHOD THEREOF

FIELD OF THE INVENTION

The invention relates to a memory cell.

Moreover, the invention relates to a memory array.

Beyond this, the invention relates to a method of manufacturing a memory cell or a memory array comprising a plurality of memory cells.

BACKGROUND OF THE INVENTION

The storage of huge amount of information on computer systems becomes more and more important. Particularly, flash memory arrays may be employed for this purpose.

Two-transistor configurations in a memory cell with an access transistor and a memory transistor allow fast random access and low power program and erase by tunnelling.

Fig. 1 shows a conventional two-transistor configuration with a conventional floating gate memory cell 100.

In a silicon substrate 101, a source region 102, a source and drain region 103 and a drain region 104 are provided as highly doped portions. An access transistor 110 comprises a gate oxide layer 111, an access gate 112, an interpolydielectric (IPD) layer 113, a contact structure 114 and a polysilicon structure 115. Furthermore, a memory transistor 120 is provided which comprises a tunnel oxide layer 111, a floating gate 121, an interpolydielectric layer 113 and a control gate 122.

Thus, Fig. 1 shows a transistor configuration in which the memory transistor 120 is implemented with a floating gate 121. Typically, the gate oxide 111 is approximately 8 nm thick. The memory transistor 120 stores the information (charge) in the floating gate 121. Both tunnel oxide 111 and interpolydielectric 113 layer are thicker than 8 nm due to retention issues.

According to another conventional two-transistor memory architecture which is shown as a memory cell 200 in Fig. 2, an access transistor 210 is provided as well as a memory transistor 220. As a charge carrier storage structure, the memory transistor 220 includes an ONO layer 221, that is a silicon oxide - silicon nitride - silicon oxide layer sequence.

Fig. 2 shows a so-called SONOS memory cell 200 (semiconductor - silicon oxide - silicon nitride - silicon oxide - semiconductor).

The access transistor 110, 210 (basically a MOSFET) which acts like a switch contributes to the selection/inhibition of a memory transistor 120, 220 in a memory array comprising a large number of memory cells 100, 200. The use of an access transistor 110, 210 allows the memory 100, 200 to be fully programmed and erased by Fowler-Nordheim tunnelling and allows to operate the individual memory cells 100, 200 without disturbing cross talk. The memory transistor 120, 220 stores the information that is encoded in stored electric charge. This charge can be injected in a polysilicon floating gate layer 121, a nitride layer of the ONO layer 221, nano-crystal dots, etc.

Fig. 2 therefore illustrates a transistor configuration in which the memory transistor 220 is implemented as a SONOS sequence. In this case, both the access transistor 210 and the memory transistor 220 have a single poly layer 112, 122. The gate oxide 111 of the access transistor 210 has a thickness of approximately 8 nm. The memory transistor 220 stores the information (charge) in a nitride layer 230 of approximately 6 nm thickness and is sandwiched between two insulator (SiO_2) layers, namely a bottom oxide 231 and a top oxide 232 of 2 nm and 8 nm thickness, respectively, whereas the three layers 230 to 232 form the ONO layer 221.

However, it is a problem that a standard planar flash memory cannot be scaled properly beyond 50 nm. Particularly, the scaling of tunnel and control dielectric thickness is limited by concerns for data-retention, yielding low coupling ratios and consequently high operating voltages. Moreover, one of the major limiting scaling parameters for two-transistor flash cells is the length of the access gate transistor 110, 210, which under worst case conditions (Fowler-Nordheim program inhibit) should have a leakage current not exceeding approximately 100 pA with as much as 5 V on its drain. These circumstances result in the fact that future scaled cells suffer of short channel effects and punch through phenomena, as well as of small on-current/off-current ratio, thus reducing the sensing margin.

A possible strategy is to increase the control of the gate over the channel with configurations such as double gate and FinFET transistors to increase the coupling efficiency between the control gate over the floating gate. Higher coupling is needed to scale down the programming voltages so as the memory cell dimensions. However, double gate and FinFET transistors are difficult in manufacture and operation.

US 2003/0015755 A1 discloses a vertical transistor, a memory arrangement

and a method for fabricating a vertical transistor. Particularly, US 2003/0015755 A1 discloses a vertical transistor which has a source region, a drain region, a gate region, and a channel region between the source region and the drain region, which are arranged in a vertical direction in a semiconductor substrate, the gate region having an electrical insulation from the source region, from the drain region and from the channel region and being arranged around the channel region in such a way that the gate region and the channel region form a coaxial structure.

However, with the procedure of forming a memory arrangement according to US 2003/0015755 A1, it may be difficult to obtain a sufficient integration density of memory cells. Furthermore, the manufacturing procedure according to US 2003/0015755 A1 is difficult and cost intensive.

OBJECT AND SUMMARY OF THE INVENTION

It is an object of the invention to provide a memory having a sufficient integration density.

In order to achieve the object defined above, a memory cell, a memory array, and a method of manufacturing a memory cell according to the independent claims are provided.

According to an exemplary embodiment of the invention, a memory cell is provided, the memory cell comprising a substrate, a nanowire (particularly an oblong nanowire) extending along a vertical trench formed in the substrate, a control gate surrounding the nanowire, and a charge storage structure formed between the control gate and the nanowire.

According to another exemplary embodiment of the invention, a memory array is provided, the memory array comprising a plurality of memory cells having the above-mentioned features and formed in the (common) substrate.

According to still another exemplary embodiment of the invention, a method of manufacturing a memory cell is provided, the method comprising forming a vertical trench in a substrate, forming a nanowire (particularly an oblong nanowire) extending along the vertical trench, forming a control gate surrounding the nanowire, and forming a charge storage structure between the control gate and the nanowire.

The term "memory cell" may particularly denote a physical structure (such as a layer sequence) which allows to store information in an electronic manner. An amount of

information stored in a memory cell may be 1 bit (which may be encoded, for instance, in the presence or absence of charge carriers in a dedicated structure) or may be more than 1 bit (which may be encoded, for instance, in the amount of stored charge and/or the type of the charge carriers, that is to say positively or negatively charged charge carriers).

The term "substrate" may denote any suitable material, such as a semiconductor, glass, plastic, etc. According to an exemplary embodiment, the term "substrate" may be used to define generally the elements for layers that underlie and/or overlie a layer or portions of interest. Also, the substrate may be any other base on which a layer is formed, for example a semiconductor wafer such as a silicon wafer or silicon chip.

The term "nanowire" may denote a wire-like structure of dimensions in the order of magnitude of several to several hundreds of nanometers (and may also cover larger or smaller dimensions). Many different types of nanowires may be used for embodiments of the invention, including semiconducting nanowires (for instance made of silicon, germanium, InP, GaN, etc.), metallic nanowires (for instance nickel, platinum, gold), and nanotubes, particularly carbon nanotubes (intrinsic or doped). According to an exemplary embodiment of the invention, such nanowires may form the channel of a transistor.

The term "oblong nanowire" may denote that the length of the nanowire is larger, particularly significantly larger, than a dimension perpendicular to the length extension. In other words, typical nanowires may exhibit aspect ratios (the ratio between length to width) of more than one, particularly of more than 2, more particularly of more than 5, or up to 1000 or more. For instance, a tubular nanowire may have a length of 50 nm to 70 nm and may have a diameter of 10 nm.

The term "charge storage structure" may particularly denote a structure that is specifically adapted to allow introducing electric charge in this structure by tunnelling or other programming procedures. The charge storage structure may be adapted in a manner that this charge is stored and remains stored within the structure for a sufficiently long time. Examples for appropriate charge storage structures are a floating gate, a nitride layer of an ONO layer sequence, etc.

The term "source/drain region" may particularly denote a source region or a drain region. Since the functionality of a source region and a drain region may depend on the operation mode of a transistor, for instance voltages applied thereto, the term source/drain region may denote a structure which can act as a source region or as a drain region.

The term "vertical trench" may denote an oblong blind hole formed in a surface

and extending inside of the substrate. In other words, a substrate usually has a main surface, and the trench is usually formed perpendicularly to this main surface. However, the term "vertical" may cover also embodiments in which a certain deviation from the 90° angle between trench and main surface of the substrate is present, but in which the trench still has a relatively steep orientation inside of the material of the substrate.

According to an exemplary embodiment of the invention, a method of producing memory cells is provided in which vertical nanowires are grown or are formed using an etching procedure as channels of transistors of the memory cells, wherein a gate stack may be partially or all-wrapped around the respective channel, for instance to form a coaxial structure. Furthermore, the nanowires may be grown within trenches surrounded by electrically insulating structures such as silicon oxide that provides electrical isolation between word lines in a memory array configuration. By taking this measure, it may be made possible to improve scaling issues. In other words, an area required for a memory array may be scaled down to a great extent with enhanced control over the channel. Beyond this, efficient process integration is possible to build memory arrays with vertical nanowire-based transistors.

A measure for advanced solid-state nanoelectronic devices is the surrounding gate geometry. Transistors having a surrounding gate structure have proper sub-threshold behaviour due to the high coupling efficiency and a significant reduction of short channel effects compared to double gate or FinFET devices. Silicon nanowire-based transistors exhibit advantageous properties. Moreover, vertically aligned nanowires are capable to reduce the processing complexity and result in ultra high transistor densities as the transistor geometry is pushed into the third dimension. 3D geometry also shows more relaxed conditions regarding transistor lengths that greatly helps as the access transistor should sustain 5V on its drain at low leakage current. By forming a nanowire within a trench, the growing or etching procedure may be very simple and may allow to mechanically protecting the relatively sensitive nanowire.

Such memory cells may be implemented in a SONOS (semiconductor - silicon oxide - silicon nitride - silicon oxide - semiconductor) or floating gate architecture with a single transistor or a two-transistor configuration in stand-alone flash memories. In other words, an array of 3D memory cells with one or two nanowire-based transistors may be provided for ultrahigh integration densities. Particularly, a vertical memory cell may be built around a nanowire with a gate stack of one or more transistors all wrapped around the nanowire.

More particularly, an easy process integration scheme is provided to build

arrays of three-dimensional memory cells comprising nanowire-based transistor configurations with one or two transistors. Such a cell design may enable the reduction of the whole memory array to a great extent. Moreover, as the gate stack may be all-wrapped around the nanowire, a high coupling coefficient may be obtained. By providing an all-wrapped around gate for a vertical nanowire, positioning the channel as a vertical nanowire may allow to obtain ultrahigh densities. As the gate may be all-wrapped around, there is full control of the gate over the channel that prevents short channel effects and increases the drive current density (improved access time). For an embodiment of a floating gate flash, the coupling characteristic between the control gate and the floating gate may be greatly improved, since the control gate may be all-wrapped around the floating gate. In an embodiment in which a nanowire is grown (for instance on a catalyst or precursor), there is no surface etching needed which results in a simple manufacturing architecture. In case of growing nanowire, the surface may be smooth so that it is possible to gain mobility (less traps).

By using a two-transistor configuration with an access transistor and a memory transistor, it may be possible to allow for a fast random access and a low power operation, since the program procedure and the erase procedure can be fully realized by tunnelling. The access transistor (basically a MOSFET transistor), which may act like a switch, may help in the selection/inhibition of the memory transistor within the array. The use of the access transistor may allow the memory to be fully programmed and erased by Fowler-Nordheim tunnelling.

It may be possible to select the dimensions of the nanowire width to be approximately ten (10) nm or several ten nanometers, which may be particularly advantageous in combination with the use of nitride spacers at the drain which reliably prevents any electrical contact between the drain and the gate, thus the nanowire can be much smaller than the contact. Therefore, an increased integration density may be obtained. It is also possible to manufacture the gate to be self-aligned to the trenches at the beginning of the process integration to isolate the word lines. When trenches are used, one mask may be saved which results in reduced costs. Thus, in order to define the source lines and the gates, this may be performed within one mask. The trench formation may require one additional mask, but then the source lines and the gate lines may be self-aligned to the trenches. Furthermore, the use of silicon nanowires may be cheap in manufacture.

According to an exemplary embodiment, a flash cell may be provided which is a non-volatile memory being able to store its information for a long period of time without

Sandisk Technologies, Inc. - Ex. 1002, Page 000668

refreshment.

Thus, it is possible to provide a memory array with an area that is scaled down to a great extent with enhanced control over the channel (reduced drain-induced barrier lowering, short channel effects, etc.) and drive current density (improved access time). A nanowire based memory cell according to an exemplary embodiment of the invention does not suffer from corner effects, in contrast to FinFET approaches.

The coupling efficiency between the control gate over the floating gate may be greatly improved as the control gate is all wrapped around the floating gate. The process integration is relatively easy and makes it feasible to build memory arrays with a large number of cells comprising vertical nanowire-based transistors. The process integration covers several memory cell implementations with a memory transistor implemented as a floating gate or as a SONOS, with or without an access transistor, etc.

The 3D geometry of a cell has the advantage that the channel current may flow vertically so that there is no need to scale down the length of the transistors. As the length of the transistor can be relatively long due to the vertical integration, it is possible to store multiple bits in the charge storage layer or structure, for instance with a SONOS memory transistor programmed by hot carrier injection (similar to an NROM).

Therefore, vertical nanowires may be grown as a channel of transistor of the memory cell, where the gate stack may be all-wrapped around a channel. The nanowire may be grown within trenches surrounded by silicon dioxide which may provide isolation between the bit lines in an array configuration.

Next, further exemplary embodiments of the memory cell will be explained. However, these embodiments also apply to the memory array and to the method.

The memory cell may comprise a first source/drain region (particularly a drain) coupled to a substrate external end portion of the nanowire and may comprise a second source/drain region (particularly a source) coupled to a substrate internal end portion of the nanowire. In other words, the end portion of the nanowire which is deepest buried within the trench connected to the substrate may form the second source/drain region, whereas the end portion of the nanowire which is closer to the main surface of the layer sequence (close to the bit lines) may form the first source/drain region. The first and second source/drain regions may be doped, for instance n^+-doped or p^+-doped. In contrast to this, the nanowire may be intrinsically or weakly doped, for instance may be n-doped or p-doped. Thus, the nanowire may form the channel portion of a nanowire-based field effect transistor.

Sandisk Technologies, Inc. - Ex. 1002, Page 000669

A contact structure may be coupled to the first source/drain region. Such a contact structure may be an electrically conductive portion which provides an electric coupling between the nanowire and an environment external to the memory cell which may be formed as a monolithically integrated circuit. Thus, such a contact structure may be a filled via and may be made of materials such as highly doped polysilicon, silicide, or may be made from a metallic material such as copper or nickel.

The memory cell may comprise an electrically insulating spacer structure surrounding the first source/drain region for securely electrically decoupling the first source/drain region from the control gate. Such an electrically insulating spacer structure may be formed on a laterally limited layer sequence, whereas the lateral walls of such a layer sequence may be covered with an electrically insulating material such as silicon dioxide (SiO_2) or silicon nitride (Si_3N_4). It may be highly advantageous to reliably decouple the source/drain region from the control gate to avoid undesired current paths or leakage currents.

The contact structure may be broader than the first source/drain region in a lateral direction. Such a lateral direction may be orthogonal to the vertical direction along which the nanowire extends. When the nanowire is smaller than the contact, an undesired electrically contact between the drain and the gate may be prevented.

The charge storage structure may comprise at least one of the group consisting of a floating gate, an ONO structure, a silicon nitride structure, and a nano-crystal dot structure. A floating gate may be an electrically conductive portion such as a polysilicon structure in which charge carriers may be stored by tunnelling or other programming procedures. An ONO structure is a silicon oxide - silicon nitride - silicon oxide layer sequence, wherein charge carriers may be permanently stored in the nitride layer by Fowler-Nordheim tunnelling or the like. A simple silicon nitride layer may also serve as a basis for a proper charge storage structure, for instance in an embodiment in which miniature dimension of the memory cell is desired. However, also nano-crystals may be used to store charge carriers such as electrons or holes.

The control gate may surround the nanowire along its entire circumference. In other words, the control gate may be provided with a blind hole through which the nanowire extends, thereby forming a coaxial nanowire gate structure. This may allow for an accurate control of the electrical conductivity of the nanowire by applying an electric voltage to the control gate.

A cross-section of the nanowire may have a diameter of less than 100 nm.

particularly of less than fifty (50) nm, more particularly of less than twenty (20) nm. According to a preferred embodiment, the nanowire has a diameter of 10 nm that allows to properly control conductivity by the surrounding gate.

Furthermore, an access gate may be provided surrounding the nanowire. The access can be part of an access transistor which may be considered as a switch which can be switched on or off by applying a voltage to the access gate. By such a two-transistor configuration, namely a configuration with an access gate and a control gate, a properly controllable memory system may be provided.

The access gate may be buried deeper within the trench than the control gate. In other words, a current flow may occur from the second source/drain region through the portion of the nanowire adjacent to the access gate, through the portion of the nanowire adjacent to the control gate, and to the first source/drain region, or vice versa.

The nanowire may be a semiconductor nanowire (such as made from silicon, germanium, etc.), a carbon nanotube (electrically conductive or semiconductive), a silicon nanowire or a group III-group V nanowire such as made of gallium arsenide.

Next, further exemplary embodiments of the memory array will be explained. However, these embodiments also apply to the memory cell and to the method.

The memory array may comprise a plurality of memory cells, particularly thousands or millions or billions or more of memory cells. These may be arranged in a matrix-like manner, wherein each of the individual memory cells can be addressed by bit lines and word lines, as known by the skilled person.

For programming, a memory cell may be selected by activating a specific access transistor, and by applying corresponding voltages to the control gate and to the source/drain connections so as to induce tunnelling or other programming effects which inject charge carriers in the charge carrier structure. After such a programming procedure, the charge carriers may remain permanently or for a long time in the charge carrier structure.

For reading out the stored information, a memory cell may again be selected by applying a readout voltage to the access gate. The current flow along the nanowire may then depend on the conductivity of the channel portion adjacent to the memory transistor, and therefore from the fact whether the charge carrier structure has been provided with charge carriers during a previous programming phase or not. Therefore, a current flowing between the source/drain regions depends on the stored information and is indicative of the stored information.

Sandisk Technologies, Inc. - Ex. 1002, Page 000671

In order to avoid or suppress artefacts (when programming or reading out the memory cell or in a passive mode of the memory cell) due to leakage or tunnelling effects, electrically insulating regions may be formed between adjacent trenches formed in the same substrate. This may allow to reliably decouple different word lines.

A common control gate may be provided for a sub-group of at least two of the plurality of memory cells. For instance, a single assigned control gate may control a column or row of memory cells. This may allow for a secure readout and an efficient architecture.

The memory array may be a two-dimensional arrangement of the memory cells, but may also be a three-dimensional stack of memory cells. Particularly, the latter measure further increases the storage volume and the integration density.

Next, further exemplary embodiments of the method will be explained. However, these embodiments also apply to the memory cell and to the memory array.

The nanowire may be formed by a growing procedure. For this purpose, a precursor may be provided in the trench so as to define a location at which the growth of the nanowire starts. This is a very simple procedure that allows to accurately define a portion at which a nanowire grows.

Alternatively, the nanowire may be formed by an etching procedure using a wafer (n-type or p-type). In such a scenario, the trench may be filled with material forming the nanowire, and a subsequent etching procedure may then define the lateral extension of the nanowire.

The method may be carried out in CMOS technology. Since the described procedures are compatible with CMOS technology, it may be possible to form a memory purely in semiconductor technology.

In an embodiment of the invention in which a floating gate configuration is implemented, programming a memory cell may be performed by applying a voltage of 12 V to 15 V to the control gate, and by simultaneously grounding the two source/drain regions (i.e. source and drain). Then, charge carriers may be injected into the floating gate by Fowler-Nordheim tunnelling. Since embodiments of the invention significantly improve the coupling efficiency, the programming voltage may be reduced compared to conventional approaches. Reading out a memory cell may be performed by applying a voltage of 1 V to the control gate, by applying a voltage of 0.5 V to the drain and by grounding the source. A voltage of 1 V may be applied to the access gate. Erasing a memory cell may be performed by applying a voltage of -12 V to -15 V to the control gate, and by simultaneously grounding the two source/drain

Sandisk Technologies, Inc. - Ex. 1002, Page 000672

regions (i.e. source and drain), so that charge carriers may be injected into or removed from the floating gate by Fowler-Nordheim tunnelling. The given voltage values are only examples and may vary over a broad interval. They may depend on dimensions, materials and electronic characteristics of the memory cell such as the threshold voltage of the transistor(s).

For any method step, any conventional procedure as known from semiconductor technology may be implemented. Forming layers or components may include deposition techniques like CVD (chemical vapour deposition), PECVD (plasma enhanced chemical vapour deposition), ALD (atomic layer deposition), or sputtering. Removing layers or components may include etching techniques like wet etching, vapour etching, etc., as well as patterning techniques like optical lithography, UV lithography, electron beam lithography, etc.

Embodiments of the invention are not bound to specific materials, so that many different materials may be used. For conductive structures, it may be possible to use metallization structures, silicide structures or polysilicon structures. For semiconductor regions or components, crystalline silicon may be used. For insulating portions, silicon oxide or silicon nitride may be used.

The structure may be formed on a purely crystalline silicon wafer or on an SOI wafer (Silicon On Insulator).

Any process technologies like CMOS, BIPOLAR, and BICMOS may be implemented.

The aspects defined above and further aspects of the invention are apparent from the examples of embodiment to be described hereinafter and are explained with reference to these examples of embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in more detail hereinafter with reference to examples of embodiment but to which the invention is not limited.

Fig. 1 shows a conventional two-transistor memory cell comprising an access transistor and a floating gate memory transistor.

Fig. 2 shows a conventional two-transistor memory cell comprising an access transistor and an ONO memory transistor.

Fig. 3 shows a cross-sectional view of a memory cell comprising an access

transistor and an ONO memory transistor according to an exemplary embodiment of the invention.

Fig. 4 shows a partial plan view of the memory cell of Fig. 3.

Fig. 5 shows a cross-sectional view of a memory cell comprising an access transistor and a floating gate memory transistor according to an exemplary embodiment of the invention.

Fig. 6 shows a partial plan view of the memory cell of Fig. 5.

Fig. 7 to Fig. 30 show layer sequences (cross-sectional views and partial plan views) obtained during carrying out a method of forming the memory cell of Fig. 3 according to an exemplary embodiment of the invention.

Fig. 7 to Fig. 17, Fig. 31 to Fig. 46 show layer sequences (cross-sectional views and partial plan views) obtained during carrying out a method of forming the memory cell of Fig. 5 according to an exemplary embodiment of the invention.

Fig. 47 to Fig. 58 show layer sequences (cross-sectional views and partial plan views) obtained during carrying out another method of forming a nanowire according to an exemplary embodiment of the invention.

DESCRIPTION OF EMBODIMENTS

The illustration in the drawing is schematical. In different drawings, similar or identical elements are provided with the same reference signs.

In the following, referring to Fig. 3, a memory cell 300 according to an exemplary embodiment of the invention will be explained.

The memory cell 300 comprises a substrate 301 that is an n-type silicon wafer. An oblong nanowire 302 extends along a vertical trench formed in the substrate 301. Furthermore, a control gate 303 is provided which surrounds the nanowire 302 in a coaxial manner along a portion of the vertical extension of the nanowire 302. A charge storage structure 304 is formed as an ONO layer sequence and is arranged between the control gate 303 and the nanowire 302. Actually, the charge will be stored in the nitride layer of the ONO layer sequence 304.

The memory cell 300 further comprises a first source/drain region 305 (which may particularly act as a drain) and is formed by an n^+-doped silicon material. The first source/drain region 305 is coupled to a substrate external end portion 330 of the nanowire

302. The first source/drain region 305 may be a doped portion of the nanowire 302 or may be configured as a separate component. A buried second source/drain region 306 (which may particularly act as a source) is provided in the substrate 301 and is another n^+-doped portion. The second source/drain region 306 is coupled to a substrate internal end portion 331 of the nanowire 302. The second source/drain region 306 may be a portion of the substrate 301 or may be configured as a separate component. A contact structure 307 of an electrically conductive material is provided and is electrically coupled to the first source/drain region 305. Beyond this, an electrically insulating spacer structure 308 surrounds the first source/drain region 305 and is adapted for electrically decoupling the first source/drain region 305 from the control gate 303.

As can be taken from Fig. 3, the contact structure 307 is broader (in a horizontal direction of Fig. 3) than the first source/drain region 305. The control gate 303 circumferentially surrounds the nanowire 302 entirely, i.e. along its entire diameter. A diameter of the nanowire along a horizontal direction of Fig. 3 is approximately 10 nm.

Furthermore, an access gate 309 is provided below the control gate and is therefore buried deeper within the trench than the control gate 303. The access gate 309 surrounds the nanowire along its entire circumference and along a part of its vertical extension. Depending on a voltage to be externally applied to the access gate 309, the value of the electrical conductivity of a controllable portion 310 of the nanowire 302 may be adjusted so that the access gate 309 serves as an access transistor with the nanowire 302 acting as a channel region.

The memory cell 300 further comprises a lateral silicon oxide (SiO_2) structure 311. On a surface of the structure 300, an electrically insulating layer 312 is provided, which may also be made from silicon oxide (SiO_2). A silicon nitride layer 313 separates the electrically insulating layers 311 and 312. Furthermore, an electrically insulating spacer structure 314 is provided. With regard to its environment, the access gate 309 is electrically insulated by an encapsulation structure 315.

In a similar manner, the control gate 303 is partially encapsulated by the ONO layer sequence 304, that is to say by a sequence comprising a first silicon oxide layer, a silicon nitride layer and a second silicon oxide layer.

Fig. 3 shows a cross-section of the memory cell 300 with a two-transistor configuration, namely the described access transistor and the memory transistor, wherein the memory transistor is implemented in a SONOS design. Possible misalignments of the contact

Sandisk Technologies, Inc. - Ex. 1002, Page 000675

307 with respect to the source/drain region 305 are indicated schematically in Fig. 3.

The intrinsically doped silicon nanowire 302 with an approximate width/diameter of 10 nm or tens of nanometers forms the channel (n-channel) of the access transistor and of the memory transistor and connects drain region 305 and source region 306 which are n-type doped as well but to a higher extent compared to the nanowire 302. The control gate 303/ONO stack 304 (part of the memory transistor) and the access gate 309/gate oxide stack 310 (part of the access transistor) are all wrapped around the channel 302. Since the gate stack 304 and the access gate/gate oxide 310 are all around the channel 302, the controllability of the conductivity of the channel 302 is greatly enhanced. This may lead to a large density drive current and low-density leakage. In the memory cell design, it is taken into account that the contact 307 to the drain 305 may be much larger than the nanowire 302 and that it can also have some misalignment (non-self-aligned contact), this is why nitride spacers 308 may be formed at the drain side 305.

Fig. 4 shows a top view of the cross-section of Fig. 3 where the contact 307 and the silicon oxide passivation layer 312 are not present to make easier the visualization of all the different layers being part of the gate stack around the channel 302.

More particularly, the plan view of Fig. 4 shows a first word line 400 and a second word line 401. However, any desired number of word lines is possible.

An enlarged view 410 is indicated in the overview of Fig. 4 as well. Furthermore, the top oxide, nitride, bottom oxide layer sequence 304, the nanowire 302, the control gate 303 and a nitride spacer 308 are shown as well. Thus, Fig. 4 shows the top view of Fig. 3 without the contact 307 to the drain 305 and the silicon oxide passivation layer 312. The insert 410 shows the different layers within the gate stack all around the channel (nanowire) 302.

In the following, referring to Fig. 5, a memory cell 500 according to another exemplary embodiment of the invention will be explained.

The embodiment of Fig. 5 differs from the embodiment of Fig. 3 particularly in that the ONO layer 304 as a charge storage structure is substituted by a floating gate 501, that is to say by an electrically conductive structure which is surrounded by an electrically insulating encapsulation 502. Therefore, charge carriers (such as electrons or holes) stored in the electrically conductive floating gate 501 which may be made of a polysilicon material, may be kept for a long duration in the floating gate 501 to store information. The conductivity of the channel region 302 adjacent to the storage region 304 depends on the type and amount of

Sandisk Technologies, Inc. - Ex. 1002, Page 000676

charge carriers located within the floating gate 501.

Therefore, Fig. 5 shows a two-transistor floating gate memory cell configuration 500. In this embodiment, the memory transistor is implemented using the floating gate 501. The principle is similar as for the SONOS memory cell 300. However, in the embodiment of Fig. 5, the control gate 303 - IPD - floating gate 501 - tunnel oxide 502 stack of the memory transistor and the access gate 309 - gate oxide 502 stack of the access transistor are all wrapped around the nanowire 302 serving as a cylindrical channel region with an essentially circular cross-section.

Fig. 6 shows a top view 600 of the memory cell 500 of Fig. 5 without the contact 307 and the silicon passivation layer 312. The insert 610 shows the different layers within the gate stack all around the channel 302 (nanowire). As indicated in the insert 610, the floating gate 501, the tunnel oxide 502 and the nanowire 302 are (partially) covered by the nitride spacer 308.

In the following, referring to Fig. 7 to Fig. 58, embodiments will be explained as to how to build memory cells according to the invention in detail with the whole process integration scheme and some possible variations (such as growing nanowires versus silicon etching of nanowires, one transistor versus two transistor configurations, and floating gate versus SONOS configurations). Silicon oxide has been considered as the dielectric material in these embodiments, although other materials different from silicon oxide (for instance high-k materials or silicon nitride) can also be used for dielectric components. In each of Fig. 7 to Fig. 58, a top view is shown on the left-hand side and a cross-sectional view is shown on the right-hand side.

Fig. 7 shows a layer sequence 700 that consists of an n-type silicon wafer 301. Such an n-type wafer 301 may be used to make a contact to the lower source of a nanowire transistor configuration to be manufactured. A p-well type as a substrate (planar) is not needed in this embodiment, but may be used in other embodiments of the invention.

Fig. 8 shows a layer sequence 800 obtained after having deposited a layer of silicon oxide (SiO_2) 311 which may later serve to isolate the word lines. Thus, an electrically insulating layer 311 is formed on the substrate 301.

Fig. 9 shows a layer sequence 900 obtained after deposition of a layer of silicon nitride 901 on the silicon oxide layer 311.

Fig. 10 shows a layer sequence 1000 that is obtained after depositing and etching an auxiliary layer 1001 (such as a photoresist) for patterning the word lines.

Fig. 11 shows a layer sequence 1100 that is obtained after removing an exposed portion of the layers 901, 311 using the patterned auxiliary layer 1001 as a mask. After having etched a trench 1101 in the layers 901, 311, an exposed portion of the substrate 301 is doped by an n^+-implantation to thereby generate an n^+-doped source region 306. Arrows 1102 indicate the implantation schematically.

Fig. 12 shows a layer sequence 1200 obtained after deposition of a precursor structure 1201 which will be later used to grow a nanowire. Gold may be used to form the precursor structure 1201. Less contaminate materials such as a titanium catalyst may be used as well. The precursor 1201 is deposited onto a specific position within the trench 1101.

Fig. 13 shows a layer sequence 1300 obtained after growing a nanowire 302 on the precursor 1201 which will later form the channel of the access and memory transistor of the memory cell to be manufactured. Optionally, the precursor 1201 is removed, and the auxiliary layer 1001 may be removed as well.

The layer sequence 1400 shown in Fig. 14 is obtained by forming (for instance by thermal oxidation) an electrically insulating layer 1401, for instance of silicon oxide, on the surface of the silicon nanowire 302 and of the source/drain region 306 within the trench 1101. As can be taken from Fig. 14, the grown silicon oxide material 1401 builds a gate oxide 1403 of the access transistor. In a surface region where a higher concentration of a dopant is present, namely on the surface of the source/drain region 306, the oxidation will result in a thicker silicon oxide layer 1402 as compared to a region at the surface of the nanowire 302 which is intrinsically doped. This effect is favourable for providing isolation between the polysilicon (deposited later on) and the source/drain region 306.

The layer sequence 1500 shown in Fig. 15 is obtained by depositing a polysilicon layer 1501 on the layer sequence 1400. The material of the polysilicon layer 1501 may later form the basis for an access gate.

In order to obtain the layer sequence 1600 shown in Fig. 16, the polysilicon structure 1501 is partially removed by CMP ("chemical mechanical polishing").

To obtain the layer sequence 1700 shown in Fig. 17, the polysilicon structure 1501 is then etched selectively to oxide and nitride. The remaining polysilicon will later form the basis for the gate region of the access transistor, denoted with reference numeral 309. The polysilicon material is in situ doped.

In order to obtain a layer sequence 1800 shown in Fig. 18, the exposed portion of the silicon oxide structure 1401 is etched, so that it is selectively removed from the

Sandisk Technologies, Inc. - Ex. 1002, Page 000678

nanowire 302, and indentations or recesses 1801 may be formed as well as a consequence of the etching procedure.

In order to obtain a layer sequence 1900 shown in Fig. 19, a bottom oxide 1901 of an ONO layer (in a configuration of a SONOS memory transistor) is grown, for instance by thermal oxidation. Again, in the polysilicon region 309, the formed oxide layer 1901 is thicker (see portion 1902) than in the nanowire 302 region providing an insulation (see portion 1903). Particularly, the portion 1902 serves as an electrically insulating portion, and the portion 1903 serves as a bottom oxide of the ONO stack (memory transistor in SONOS design).

In order to obtain a layer sequence 2000 as shown in Fig. 20, a nitride layer 2001 of the ONO stack to be formed is deposited. The deposition procedure may be performed in a manner that the thickness of the layer 2001 will be essentially uniform. Reference numeral 2002 indicates a portion of the nitride layer 2001 of the ONO stack (control gate in SONOS configuration), i.e. a portion in which charge may be stored for encoding information.

In order to obtain a layer sequence 2100 as shown in Fig. 21, a top silicon oxide layer 2101 is deposited, again essentially uniformly. Therefore, as indicated with reference numeral 2102, an ONO (oxide/nitride/oxide) stack is formed.

In order to obtain a layer sequence 2200 shown in Fig. 22, a polysilicon layer 2201 is deposited, forming a basis for a control gate polysilicon structure.

In order to obtain the layer sequence 2300 shown in Fig. 23, the further polysilicon layer 2201 is planarized by CMP ("chemical mechanical polishing").

The layer sequence 2400 shown in Fig. 24 is obtained by selectively etching the polysilicon structure 2201 relative to silicon oxide, thereby constituting the polysilicon control gate 303 of the memory transistor. The polysilicon gate 303 is in situ doped.

In order to obtain the layer sequence 2500 shown in Fig. 25, the exposed portions of the ONO layer 1901, 2001, 2101 are removed. It is not detrimental if the remained ONO layer 1901, 2001, 2101 is not aligned to the control gate 303 polysilicon material, whenever the ONO layer 1901, 2001, 2101 fully covers the region below the control gate 309. It should be prevented that the ONO layer 1901, 2001, 2101 is overetched below the control gate polysilicon material 303. As can be taken from Fig. 25, the described processing manufactures the memory transistor (SONOS) and the access transistor. The memory portion of the ONO layer 1901, 2001, 2101 which actually stores the charge is shown as a portion

Sandisk Technologies, Inc. - Ex. 1002, Page 000679

illustrated as a rectangular 304.

To obtain the layer sequence 2600 of Fig. 26, nitride spacers 308 are formed to make a contact to the drain (to be formed subsequently feasible). Nitride spacers 314 may be formed as well.

In order to obtain the layer sequence 2700 shown in Fig. 27, a shallow n^+-implantation procedure is performed in order to form the drain region (denoted with reference numeral 305, see Fig. 3 or Fig. 28). This is indicated by arrows 2701 in Fig. 27.

Consequently, an n^+-drain 305 is formed, as indicated in the layer sequence 2800 as shown in Fig. 28.

In order to obtain the layer sequence 2900 shown in Fig. 29, a silicon oxide layer 312 is deposited on the entire surface of the layer sequence 2800.

In order to obtain the layer sequence 3000 shown in Fig. 30, the electrically insulating layer 312 is patterned using a lithography procedure and an etching procedure, thereby forming a through hole in the layer 312 to thereby expose a surface of the drain region 305. Then, electrically conductive material is filled in the hole to form an electrically conductive contact 307.

In other words, manufacture of a contact to the drain 305 stopping at the nitride structure 308 is performed. The contact 307 may be wider than the nanowire 302, and possible misalignments (non-self-aligned contact) may be taken into account and are not harmful thanks to the nitride spacers 308.

The configuration shown in Fig. 30 essentially equals to the configuration shown in Fig. 3.

As an alternative to such an implementation of the memory transistor using a SONOS architecture, it is also possible to manufacture the memory transistor including a floating gate.

For this purpose, the manufacturing procedures described above referring to Fig. 7 to Fig. 17 can be performed and can be combined with the processing procedures that will be explained below referring to Fig. 31 to Fig. 46. As a result, a memory cell similar to that shown in Fig. 5 is obtainable.

Referring to Fig. 31, after forming the access gate 309 (common to SONOS), a tunnel oxide layer 3101 is grown, providing isolation at the polygate side 309.

The layer sequence 3200 shown in Fig. 32 is obtained by depositing polysilicon material for the floating gate, thereby forming a polysilicon layer 3201.

Sandisk Technologies, Inc. - Ex. 1002, Page 000680

The layer sequence 3300 shown in Fig. 33 is obtained by planarizing the polysilicon structure 3201 by CMP ("chemical mechanical polishing").

To obtain a layer sequence 3400 as shown in Fig. 34, the polysilicon structure 3201 is further etched and therefore selectively removed relative to silicon oxide to build the floating gate.

In order to obtain the layer sequence 3500 shown in Fig. 35, a top portion of the electrically insulating structure 3101 is removed by wet etching.

In order to obtain the layer sequence 3600 shown in Fig. 36, lateral silicon nitride spacers 308, 314 are formed to cover lateral walls of the first source/drain region to be able to contact without harming the device.

In order to obtain the layer sequence 3700 of Fig. 37, a polysilicon overetch procedure is performed, removing the non-exposed portions of the polysilicon material 3201 which is not covered by the nitride spacers 308, 314.

A layer sequence 3800 shown in Fig. 38 is obtained by depositing silicon oxide (SiO_2) as interpolydielectric material, thereby forming a layer 3801 covering the layer sequence 3700.

In order to obtain the layer sequence 3900 shown in Fig. 39, polysilicon material 3901 is deposited on the surface of the layer sequence 3800, thereby providing material for forming the control gate.

In order to obtain a layer sequence 4000 shown in Fig. 40, the polysilicon structure 3901 is planarized by performing a CMP procedure ("chemical mechanical polishing").

In order to obtain the layer sequence 4100 shown in Fig. 41, a control gate 303 are formed by selectively etching polysilicon material of the structure 3901 relative to silicon oxide.

By etching the silicon oxide material on the surface of the layer sequence 4100, the layer sequence 4200 shown in Fig. 42 is obtained.

Subsequently, as shown in a layer sequence 4300 in Fig. 43, an n^+-shallow implantation procedure is performed to form the drain 305 in an upper portion of the nanowire 302 (see Fig. 44). Arrows 4301 indicate this doping procedure schematically.

Consequently, the layer sequence 4400 shown in Fig. 44 shows the second source/drain region 305.

The layer sequence 4500 shown in Fig. 45 is obtained by depositing silicon

oxide material on the surface of the layer sequence 4400, thereby forming an electrically insulating layer 312.

Then, as can be taken from the layer sequence 4600 in Fig. 46, a contact to the drain 305 is provided by item 307. Again, possible misalignments of the contact 307, or the fact that the contact 307 for contacting the drain 305 is larger than the nanowire 302, is not harmful thanks to the nitride spacers 308.

The layer sequence 4600 essentially corresponds to the memory cell 500 shown in Fig. 5.

The above-described Fig. 7 to Fig. 13 explain a procedure of growing a nanowire 302.

Alternatively, the nanowire can also be manufactured by etching a silicon structure, which will be explained in the following.

Therefore, after having manufactured the layer sequence in a manner as shown in Fig. 47 to Fig. 58, the procedures of Fig. 14 to Fig. 46 can be performed in a similar manner.

Fig. 47 shows a view 4700 of a wafer 301.

In order to obtain the layer sequence 4800 shown in Fig. 48, a nitride layer 901 is deposited on the wafer 301 to create a stopping layer for a later CMP ("chemical mechanical polishing") procedure.

As indicated in Fig. 49 showing a layer sequence 4900, an active mask 4901 is applied as a template for forming trenches (such as STI trenches, "shallow trench isolation").

In order to obtain the layer sequence 5000 shown in Fig. 50, the entire wafer 301 is etched, thereby forming STI trenches 5001. The active mask 4901 may be removed.

As shown in Fig. 51 illustrating a layer sequence 5100, the trenches 5001 are filled with silicon oxide material, and an additional amount of silicon oxide material is deposited over this layer structure. Consequently, a silicon oxide layer 5101 is formed.

As shown in Fig. 52 illustrating a layer sequence 5200, silicon oxide material of layer 5101 is removed by CMP ("Chemical Mechanical Polishing"), wherein the silicon nitride material 901 is used as a stopping layer.

In order to obtain the layer sequence 5300 shown in Fig. 53, silicon nitride material 5301 is deposited on top of the layer sequence 5200.

Fig. 54 shows a layer sequence 5400 in which a patterned mask 5401 is shown. The inverse 5401 to the active mask 4901 (instead of light field dark field) is used to remove

the silicon nitride material of top of the silicon wafer 301.

Etching the layers 5301 and 901 results in the layer sequence 5500 shown in Fig. 55.

The nanowire 302 is then defined by etching silicon material of the substrate 301.

The result of such an etching procedure is shown as the layer sequence 5600 in Fig. 56.

Fig. 57 shows a layer sequence 5700 and arrows 5701 indicating an n^+-implantation to define the source and the drain. With a 0° tilt angle of the implantation, it is possible to avoid the doping of the nanowire 302.

A layer sequence 5800 illustrated in Fig. 58 shows the result with the two source/drain regions 305 and 306.

Starting with the layer sequence 5800, it is possible to continue with Fig. 14.

Finally, it should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be capable of designing many alternative embodiments without departing from the scope of the invention as defined by the appended claims. In the claims, any reference signs placed in parentheses shall not be construed as limiting the claims. The word "comprising" and "comprises", and the like, does not exclude the presence of elements or steps other than those listed in any claim or the specification as a whole. The singular reference of an element does not exclude the plural reference of such elements and vice-versa. In a device claim enumerating several means, several of these means may be embodied by one and the same item of software or hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

Sandisk Technologies, Inc. - Ex. 1002, Page 000683

CLAIMS:

1. A memory cell (300, 500), the memory cell (300, 500) comprising
a substrate (301);
a nanowire (302) extending along a vertical trench formed in the substrate (301);
a control gate (303) surrounding at least a part of the nanowire (302);
a charge storage structure (320, 301) arranged between the control gate (303) and the nanowire (302).

2. The memory cell (300, 500) according to claim 1, comprising a first source/drain region (305) coupled to a substrate external end portion (330) of the nanowire (302) and comprising a second source/drain region (306) coupled to a substrate internal end portion (331) of the nanowire (302).

3. The memory cell (300, 500) according to claim 2, comprising a contact structure (307) coupled to the first source/drain region (305).

4. The memory cell (300, 500) according to claim 2, comprising an electrically insulating spacer structure (308) surrounding the first source/drain region (305) for electrically decoupling the first source/drain region (305) from the control gate (303).

5. The memory cell (300, 500) according to claim 3, wherein the contact structure (307) has a larger dimension than the first source/drain region (305) in a direction being perpendicular to the vertical extension of the trench.

6. The memory cell (300, 500) according to claim 1, wherein the charge storage structure comprises one of the group consisting of a floating gate (501), a silicon oxide-silicon nitride-silicon oxide layer sequence (320), a silicon nitride structure, and a nano-crystal dot structure.

Sandisk Technologies, Inc. - Ex. 1002, Page 000684

7. The memory cell (300, 500) according to claim 1, wherein the control gate (303) surrounds the nanowire (302) along the entire circumference of the nanowire (302).

8. The memory cell (300, 500) according to claim 1, wherein the nanowire (302) has a diameter of less than 100 nm, particularly of less than 50 nm, more particularly of less than 20 nm, in a direction perpendicular to the vertical extension of the trench.

9. The memory cell (300, 500) according to claim 1, comprising an access gate (309) surrounding at least a part of the nanowire (302), particularly surrounding the nanowire (302) along the entire circumference of the nanowire (302).

10. The memory cell (300, 500) according to claim 9, wherein the access gate (309) is arranged deeper within the trench than the control gate (303).

11. The memory cell (300, 500) according to claim 1, wherein the nanowire (302) comprises one of the group consisting of a semiconductor nanowire, a carbon nanotube, a silicon nanowire, and a group III-group V nanowire.

12. The memory cell (300, 500) according to claim 1, adapted as a flash memory cell (300, 500).

13. The memory cell (300, 500) according to claim 1, adapted as a multi-bit memory cell (300, 500).

14. A memory array (400, 600), the memory array (400, 600) comprising a plurality of memory cells (300, 500) according to claim 1 formed in the substrate (301).

15. The memory array (400, 600) according to claim 14, comprising electrically insulating regions (311) between adjacent trenches.

16. The memory array (400, 600) according to claim 14, wherein a common control gate (303) is provided in common for a sub-group of at least two of the plurality of memory cells (300, 500).

17. A method of manufacturing a memory cell (300, 500), the method comprising
forming a vertical trench in a substrate (301);
forming a nanowire (302) extending along the vertical trench;
forming a control gate (303) surrounding at least a part of the nanowire (302);
arranging a charge storage structure (320, 501) between the control gate (303) and the nanowire (302).

18. The method according to claim 17, wherein the nanowire (302) is formed by one of the group consisting of a growing procedure and an etching procedure.

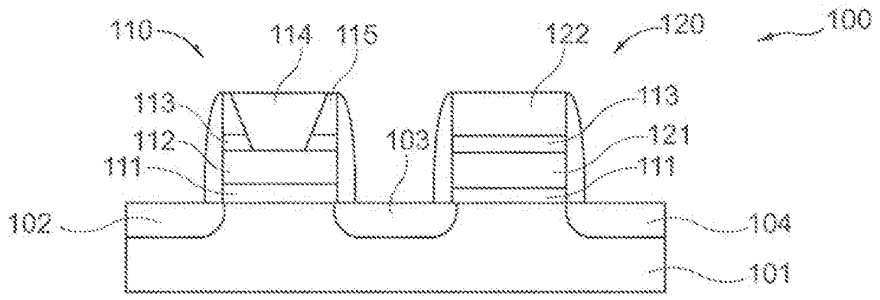


FIG. 1

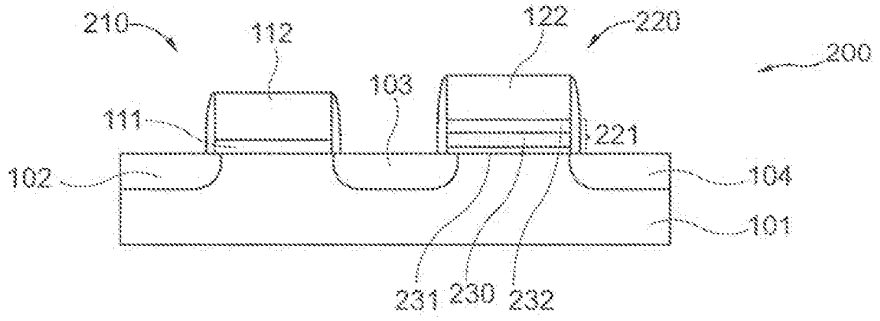


FIG. 2

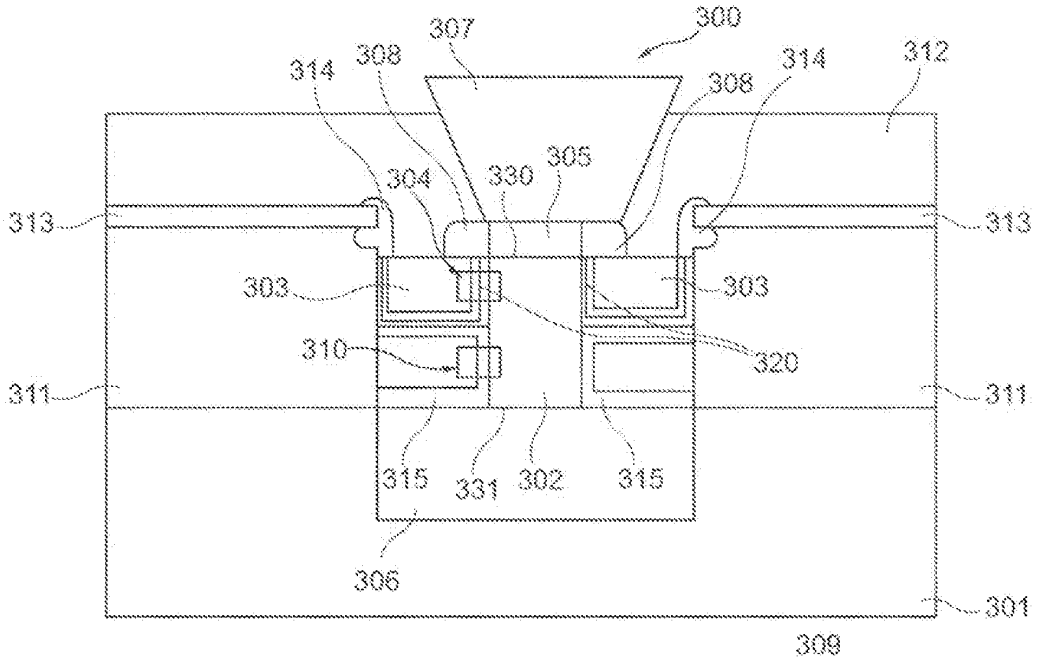


FIG. 3

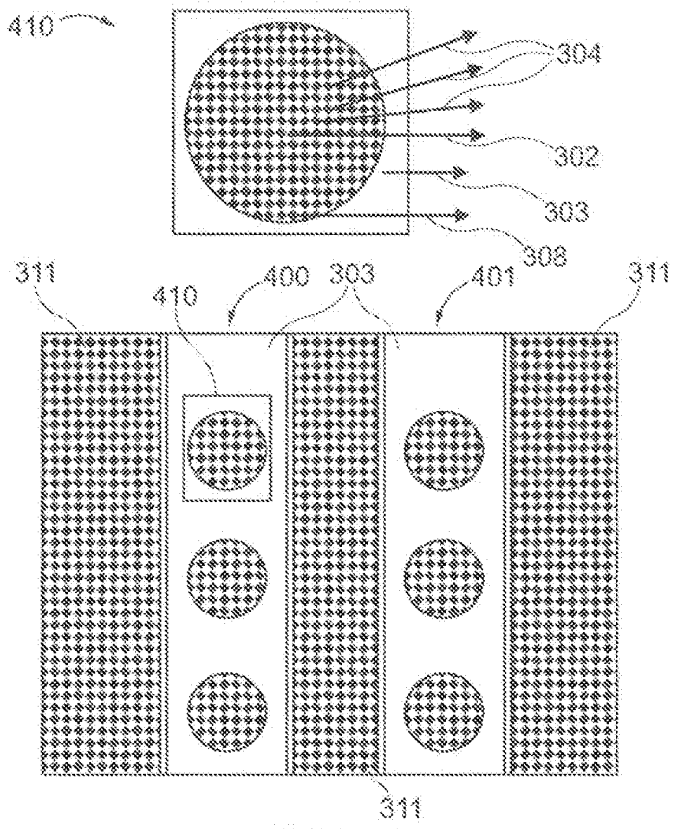

410
304
302
303
308
311
410
400
303
401
311
311

FIG. 4

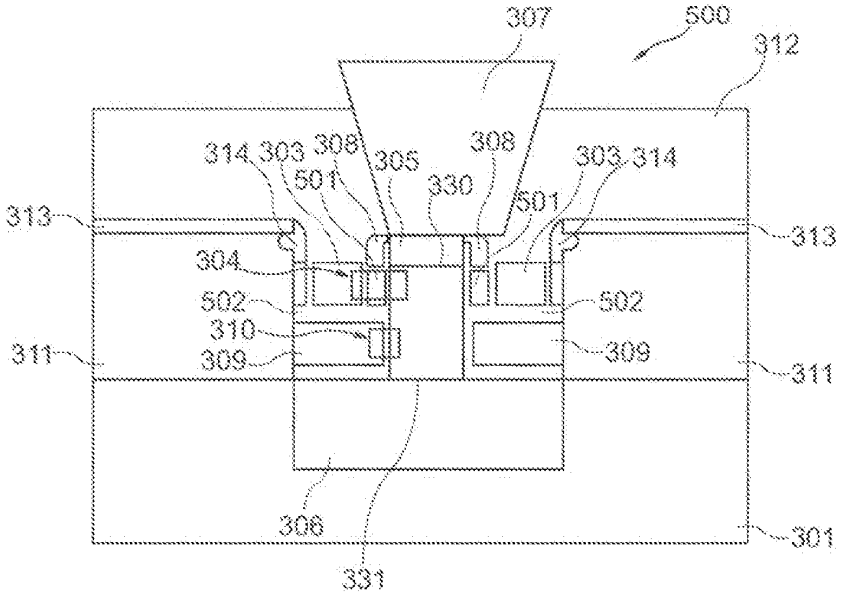

307
500
312
314
303
308
501
305
330
308
303
314
501
313
313
304
502
502
310
309
311
309
311
306
301
331

FIG. 5

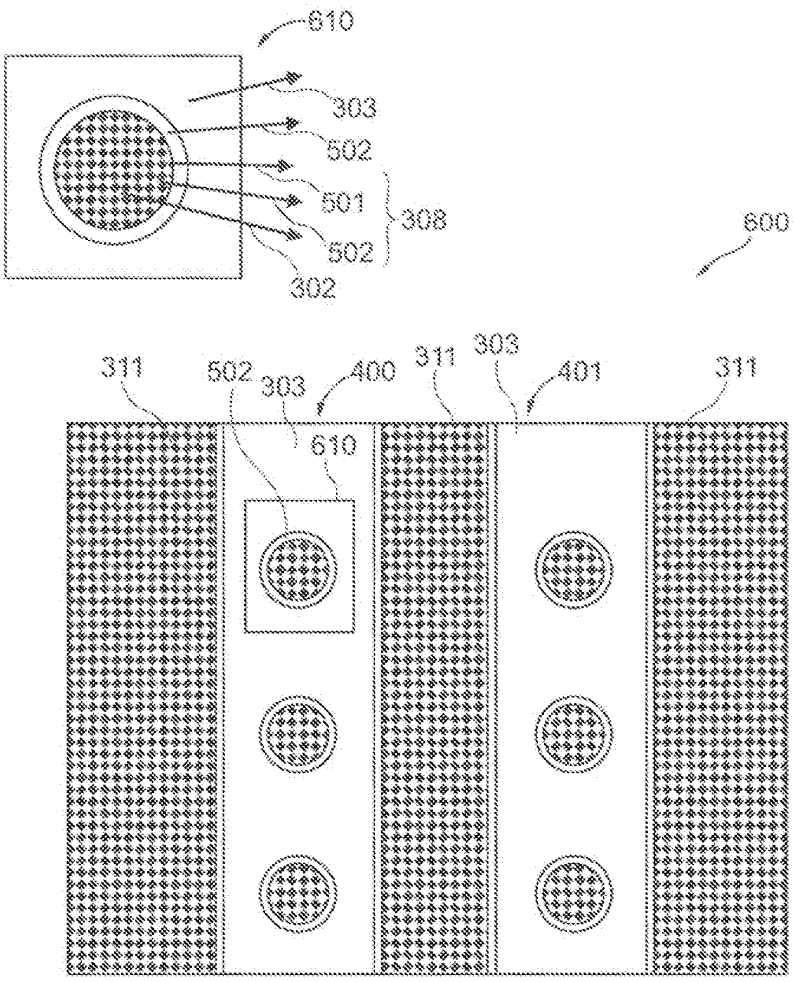

610
303
502
501
308
502
302
600
311
502
303
400
311
303
401
311
610

FIG. 6

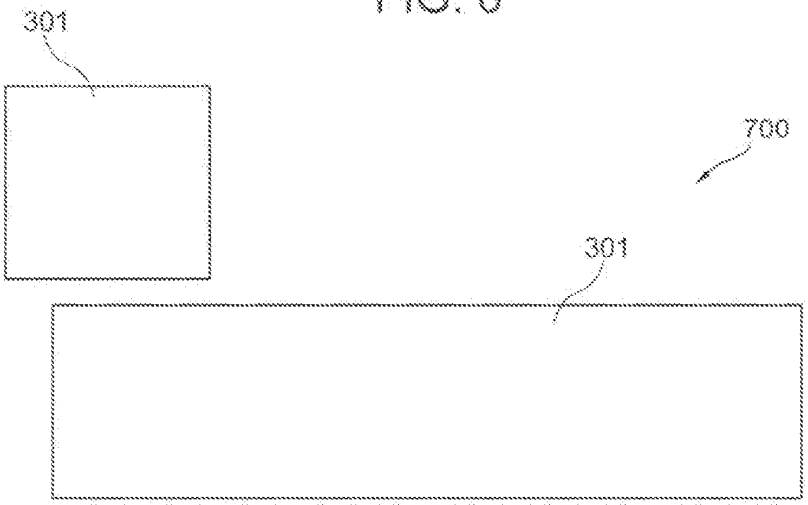

301
700
301

FIG. 7

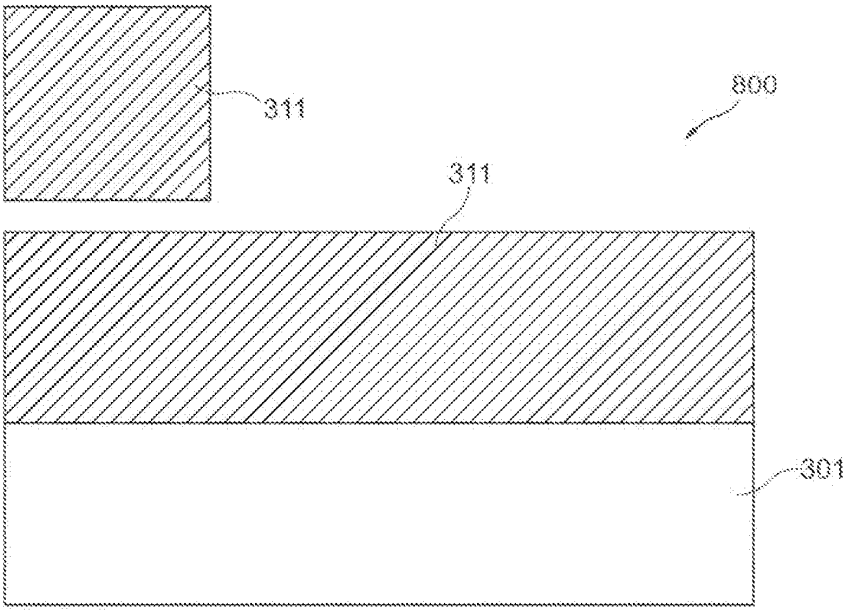


FIG. 8

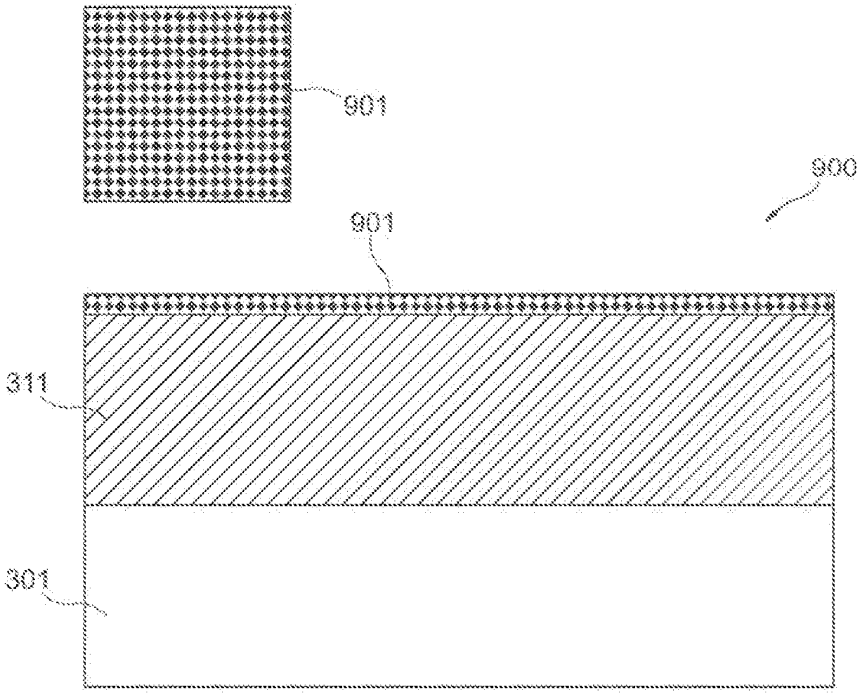


FIG. 9

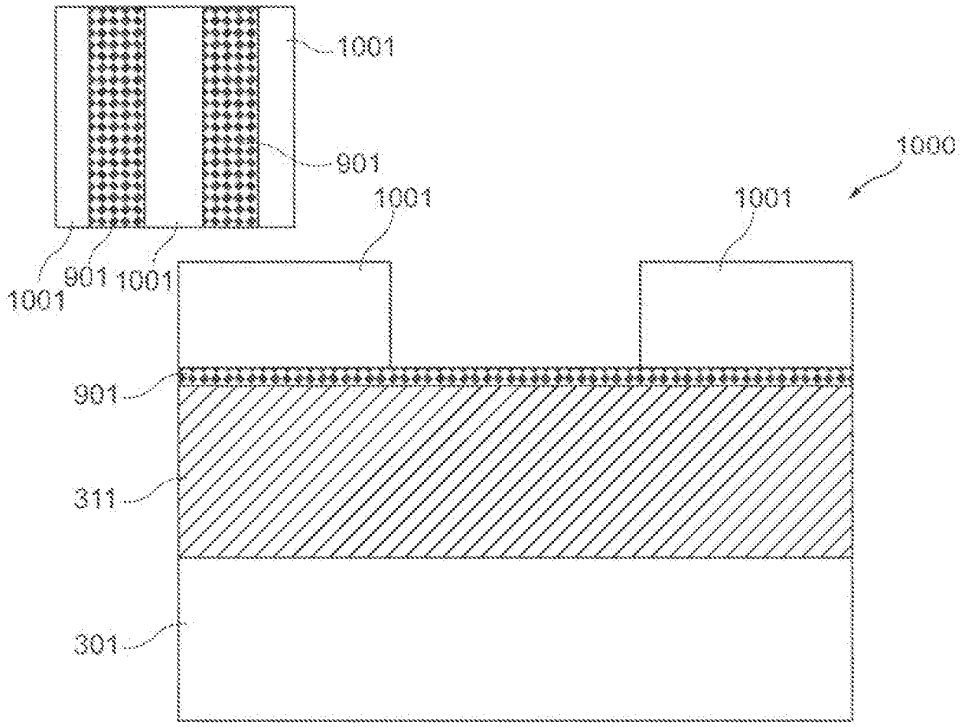

1001
901
1000
1001
1001
1001
901
1001
901
311
301

FIG. 10

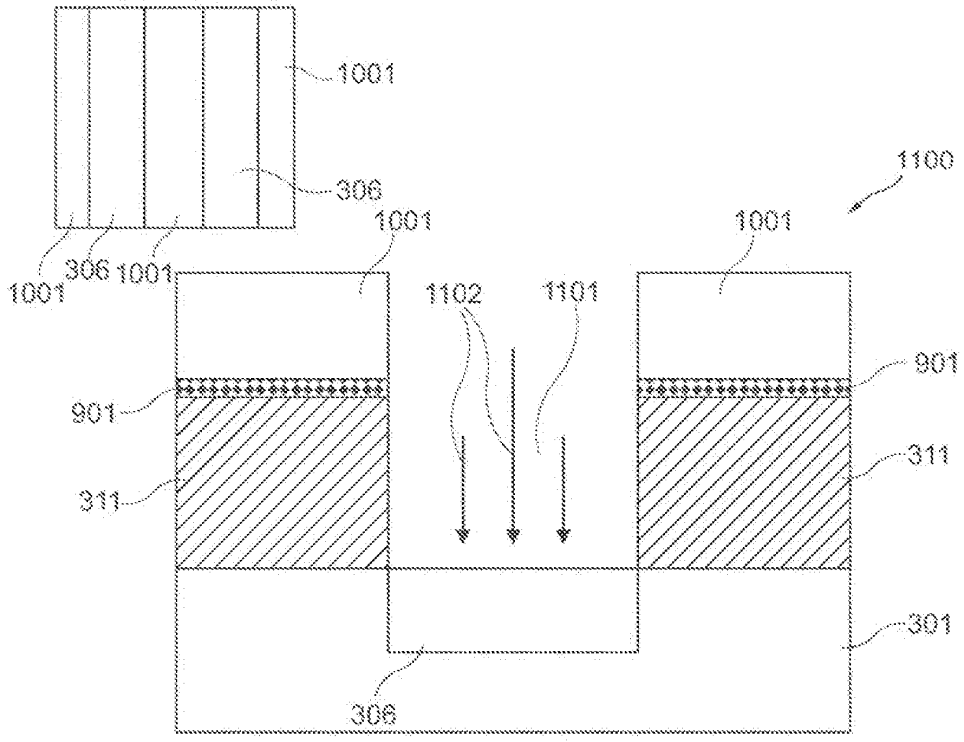

1001
306
1100
1001
1001
1001
306
1001
1102
1101
901
901
311
311
301
306

FIG. 11

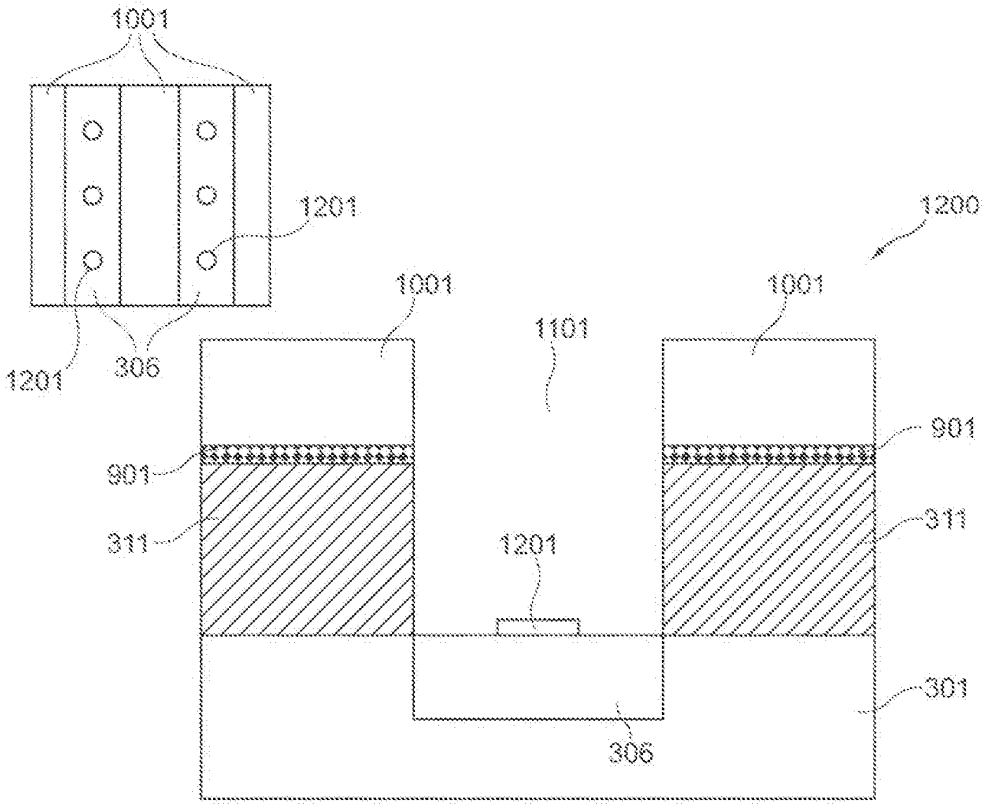

1001
1201
1200
1001
1001
1201
306
1101
901
901
311
311
1201
301
306

FIG. 12

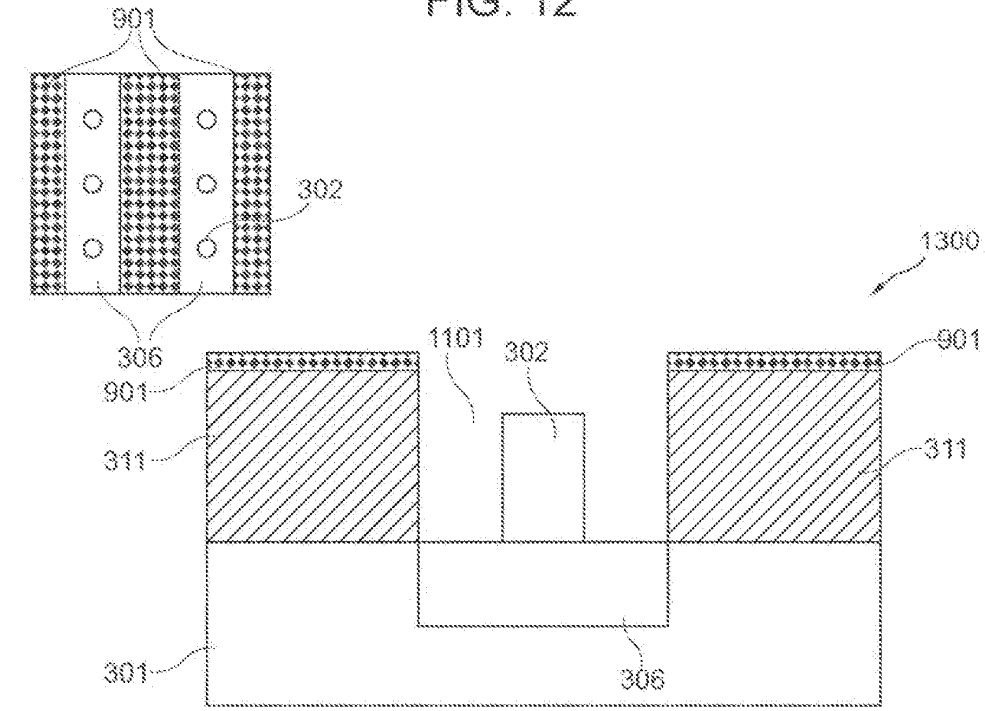

901
302
1300
306
1101
302
901
901
311
311
301
306

FIG. 13

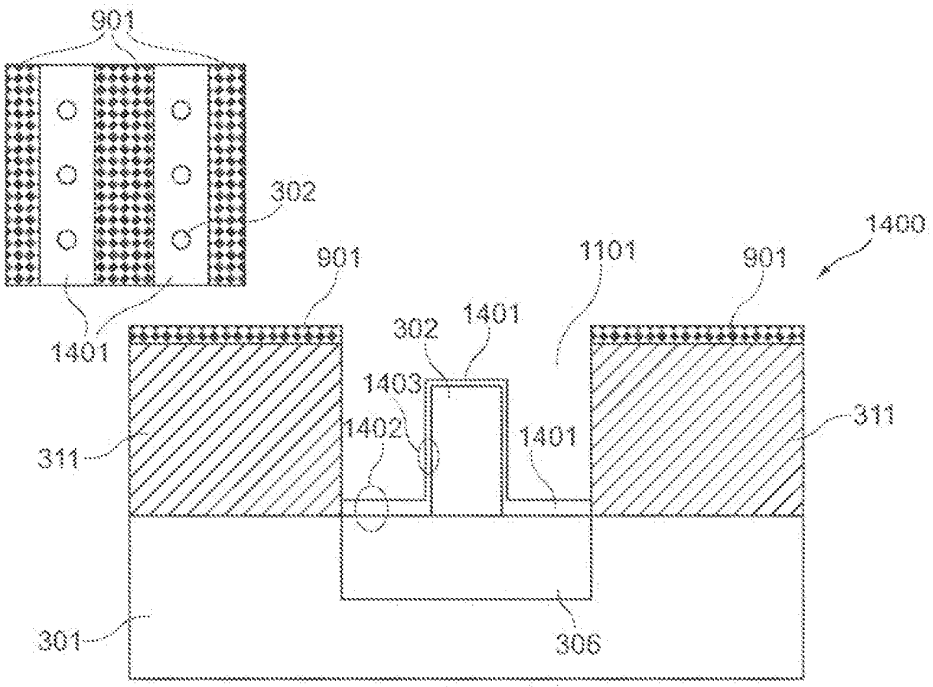

901
302
1400
901
1101
901
1401
302
1401
1403
1402
1401
311
311
301
306

FIG. 14

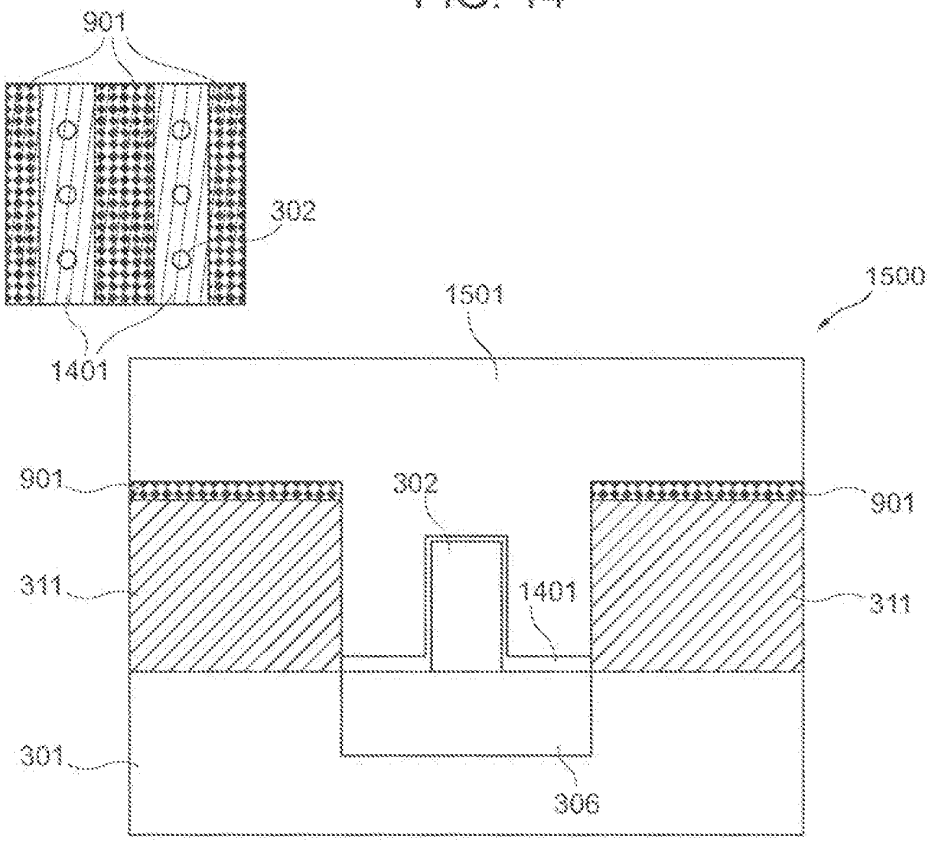

901
302
1500
1501
1401
901
302
901
311
1401
311
301
306

FIG. 15

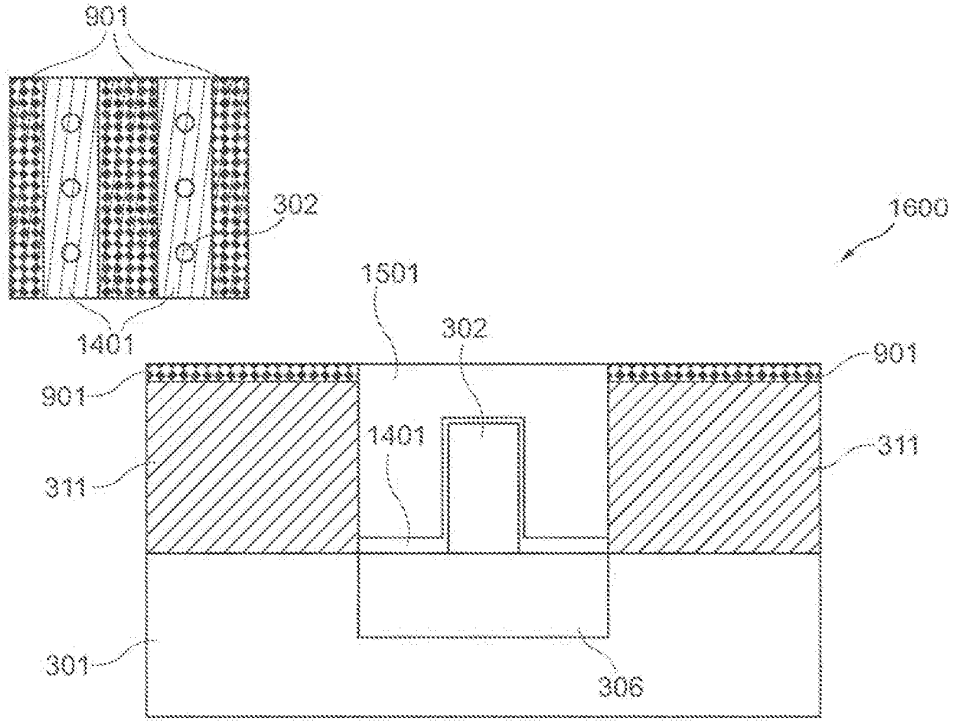

901
302
1600
1501
1401
302
901
901
1401
311
311
301
306

FIG. 16

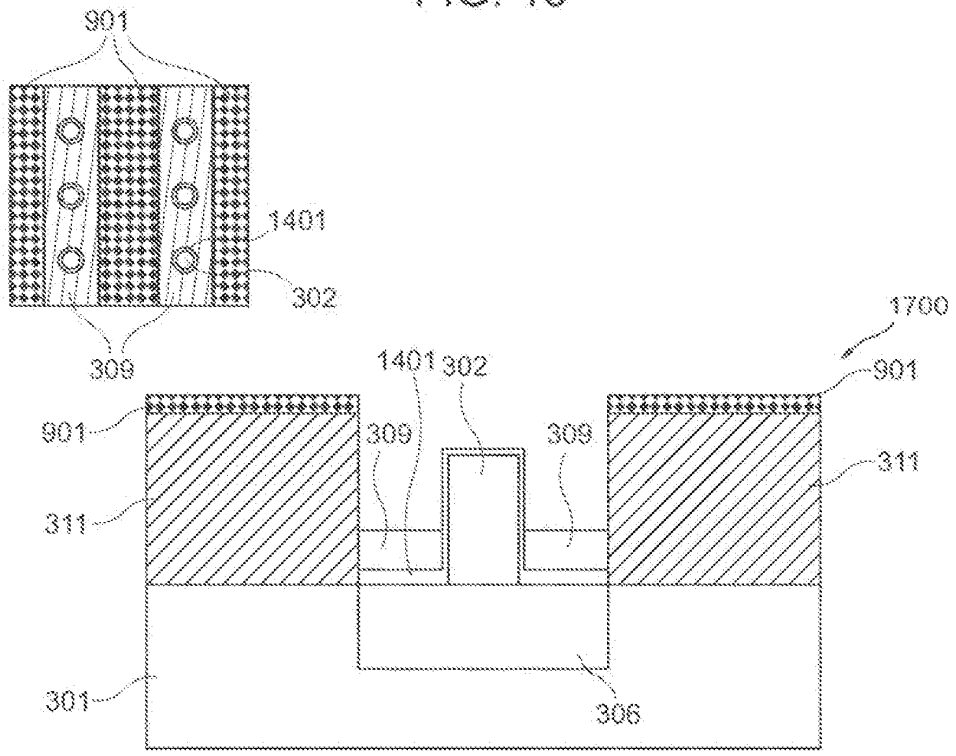

901
1401
302
1700
309
1401
302
901
901
309
309
311
311
301
306

FIG. 17

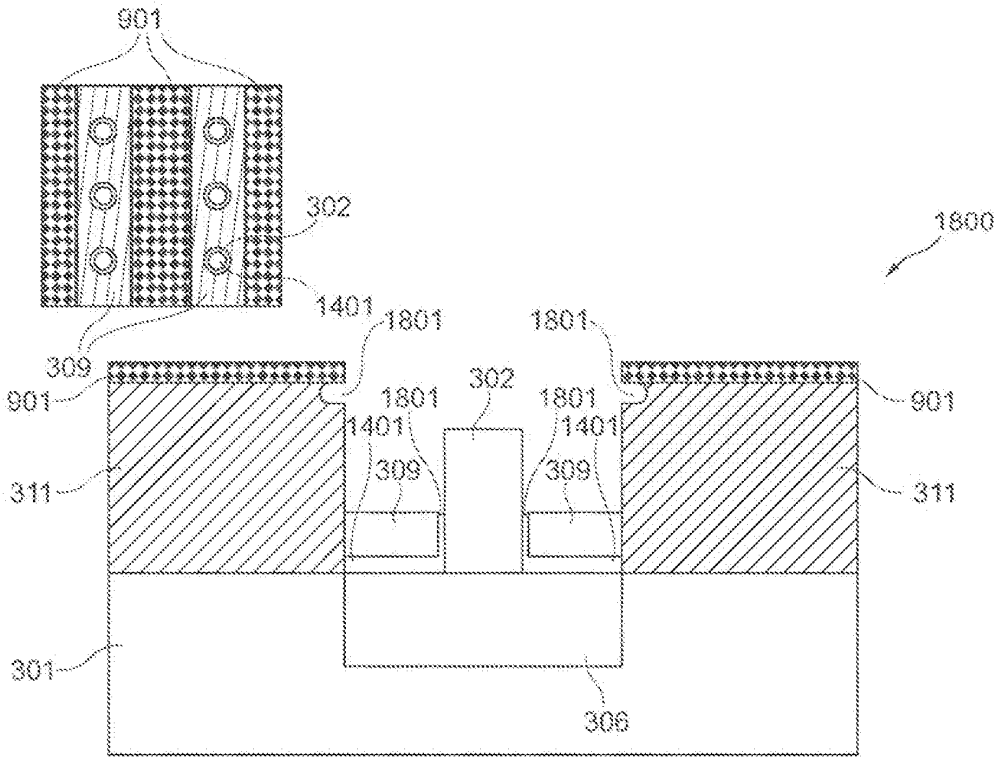

901
302
1800
1401
1801
1801
309
901
1801
302
1801
901
1401
1401
309
309
311
311
301
306

FIG. 18

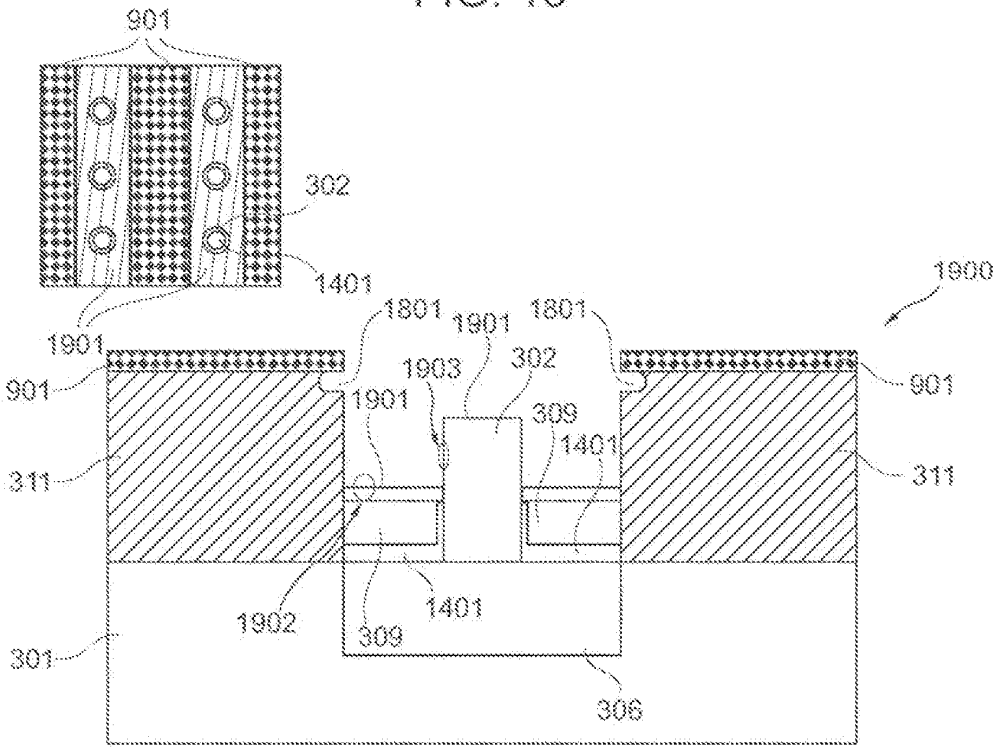

901
302
1900
1401
1801
1901
1801
1901
1903
302
901
901
1901
309
1401
311
311
1902
1401
309
301
306

FIG. 19

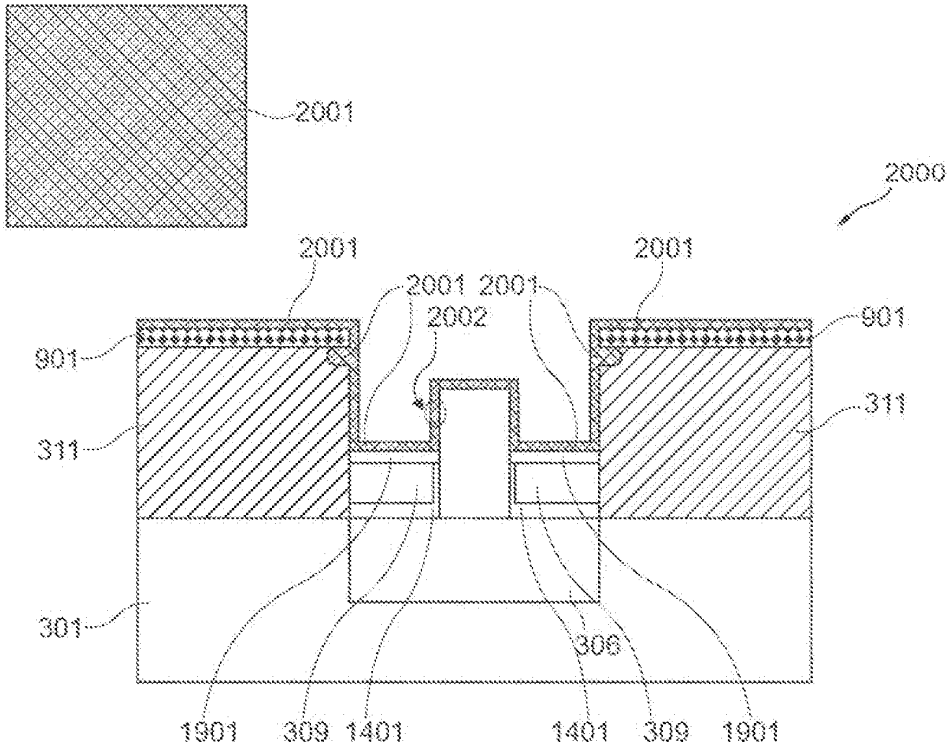

2001
2000
2001
2001
2001
2001
2002
901
901
311
311
301
306
1901
309
1401
1401
309
1901

FIG. 20

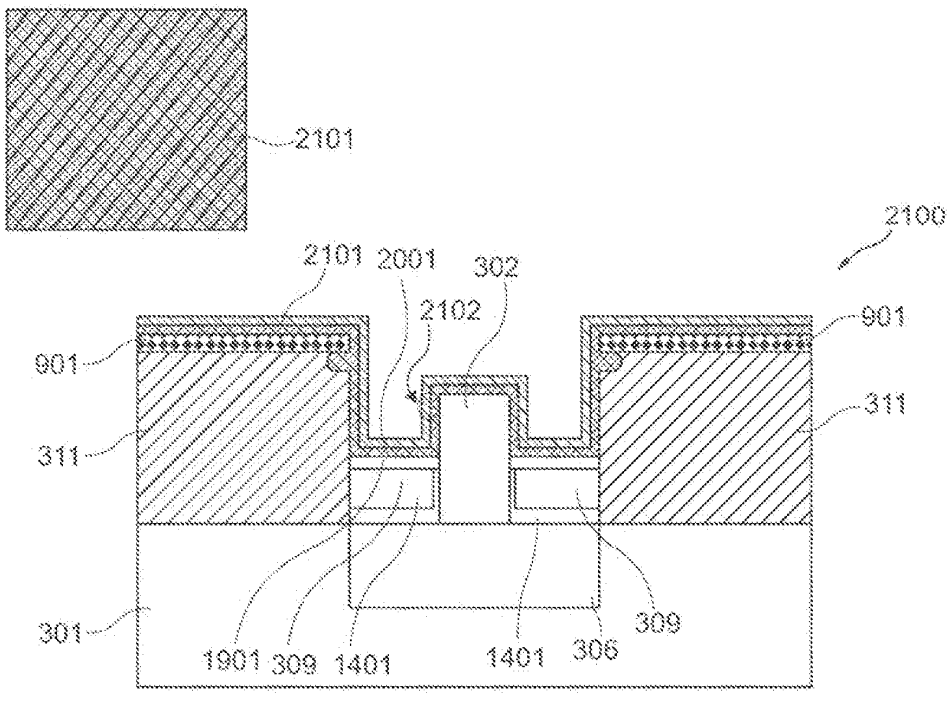

2101
2100
2101
2001
302
2102
901
901
311
311
301
309
1901
309
1401
1401
306

FIG. 21

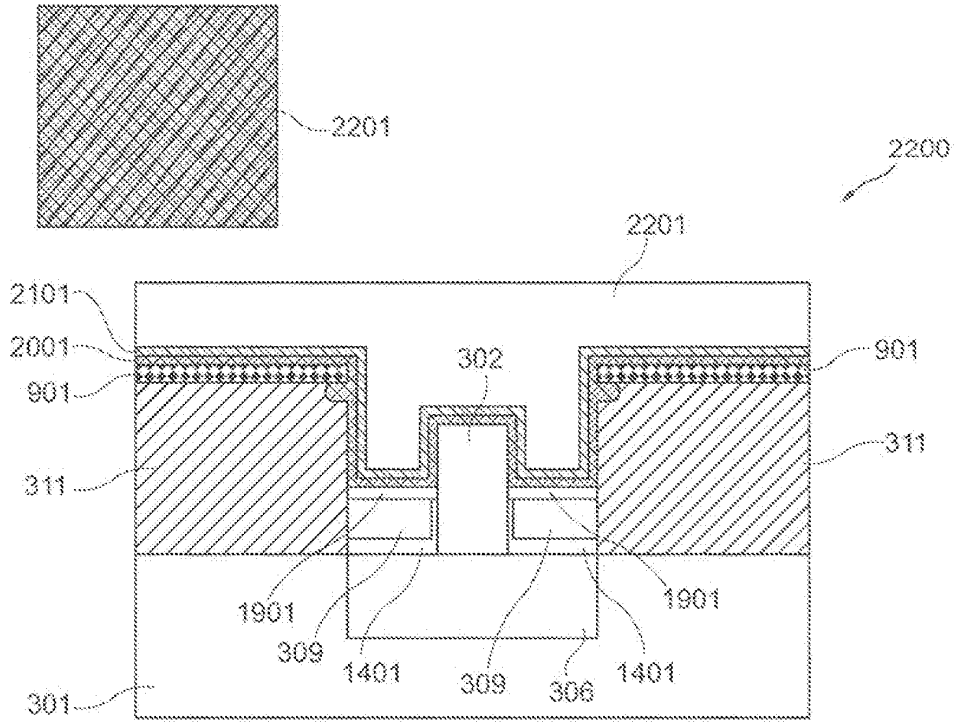

2201
2200
2201
2101
2001
901
302
901
311
311
1901
1901
309
1401
309
306
1401
301

FIG. 22

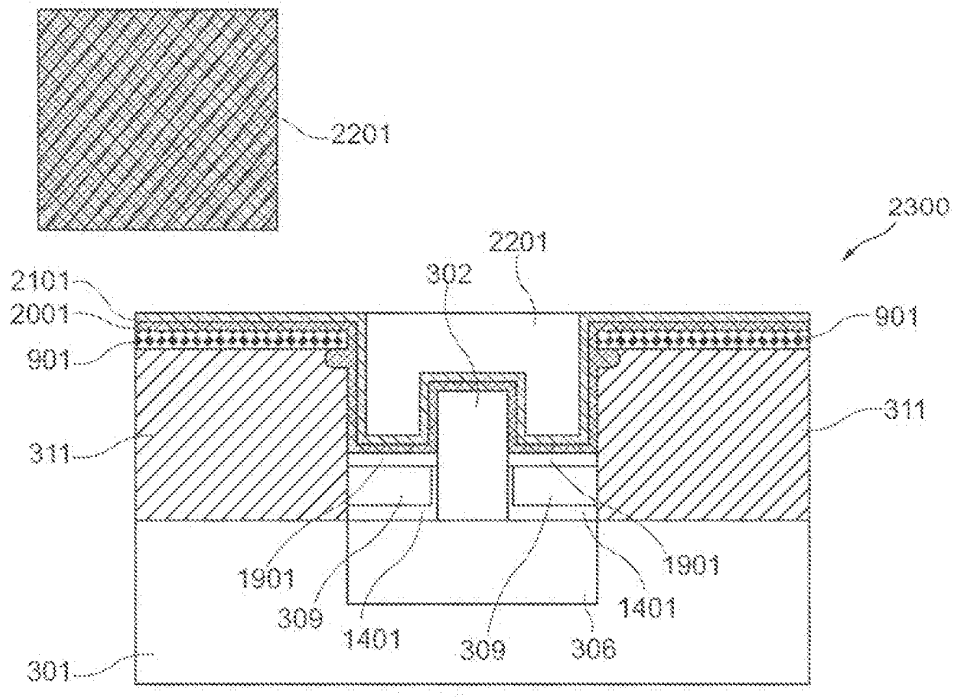

2201
2300
2201
302
2101
2001
901
901
311
311
1901
1901
309
1401
1401
309
306
301

FIG. 23

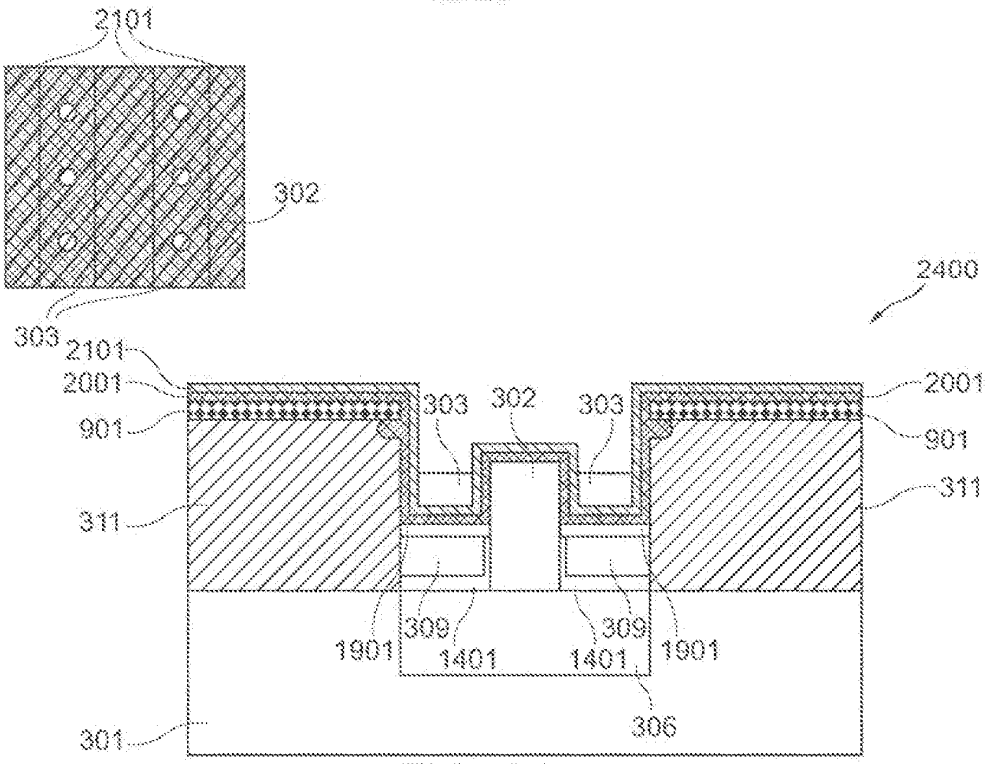

2101
302
303
2400
2101
2001
303
302
303
2001
901
901
311
311
309
309
1901
1401
1401
1901
306
301

FIG. 24

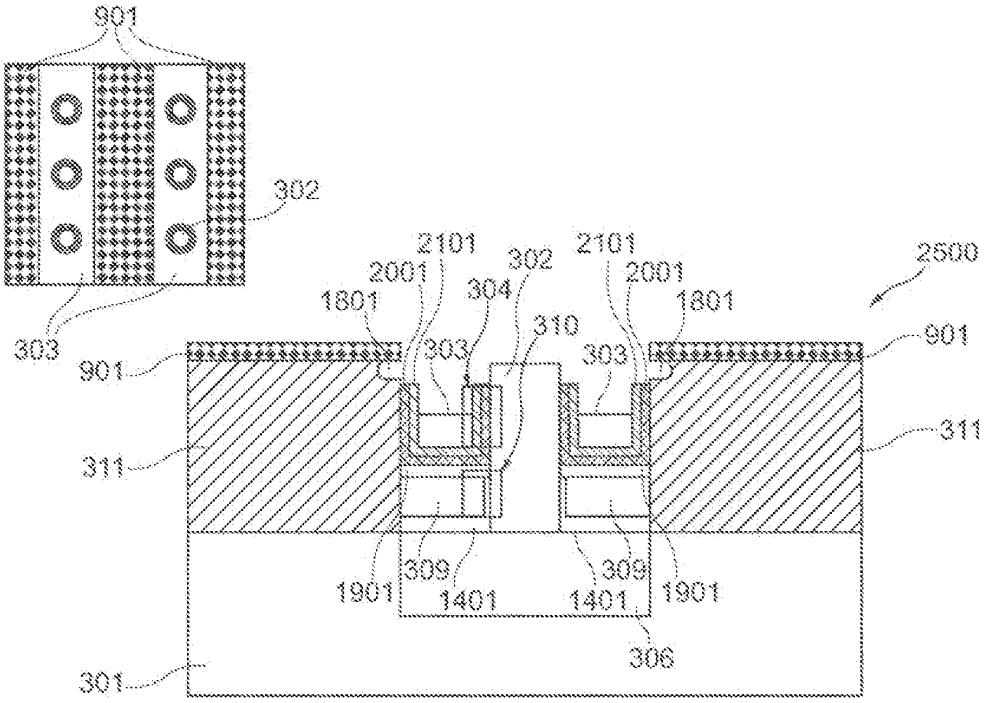

901
302
2101
2101
2500
2001
302
2001
1801
304
1801
310
303
303
901
901
311
311
309
309
1901
1401
1401
1901
306
301

FIG. 25

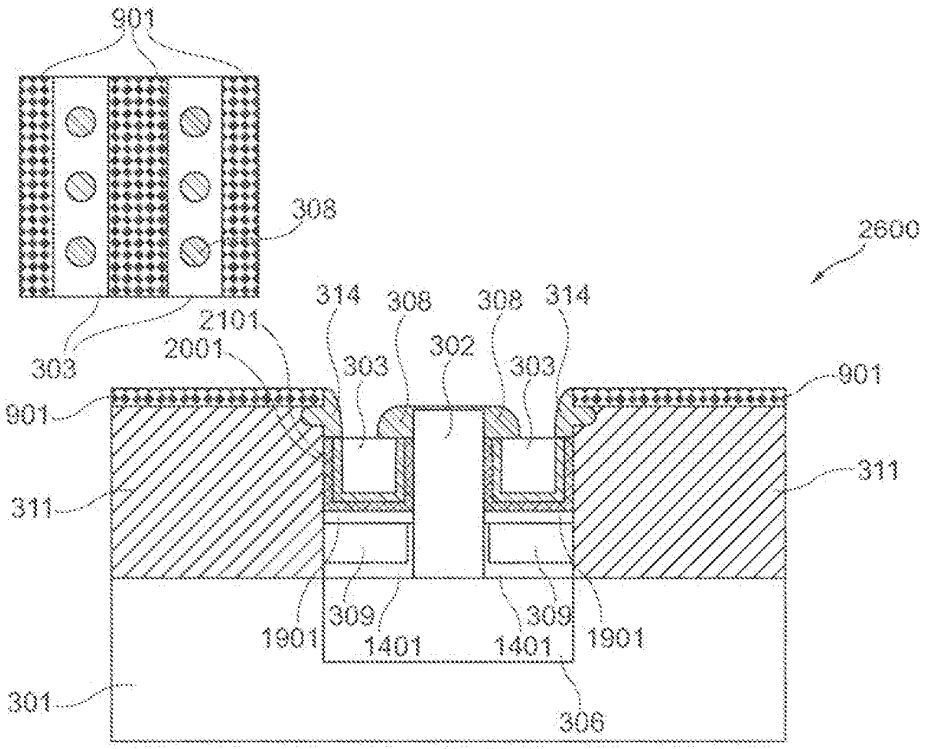

901
308
2600
314
308
308
314
2101
2001
303
303
302
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 26

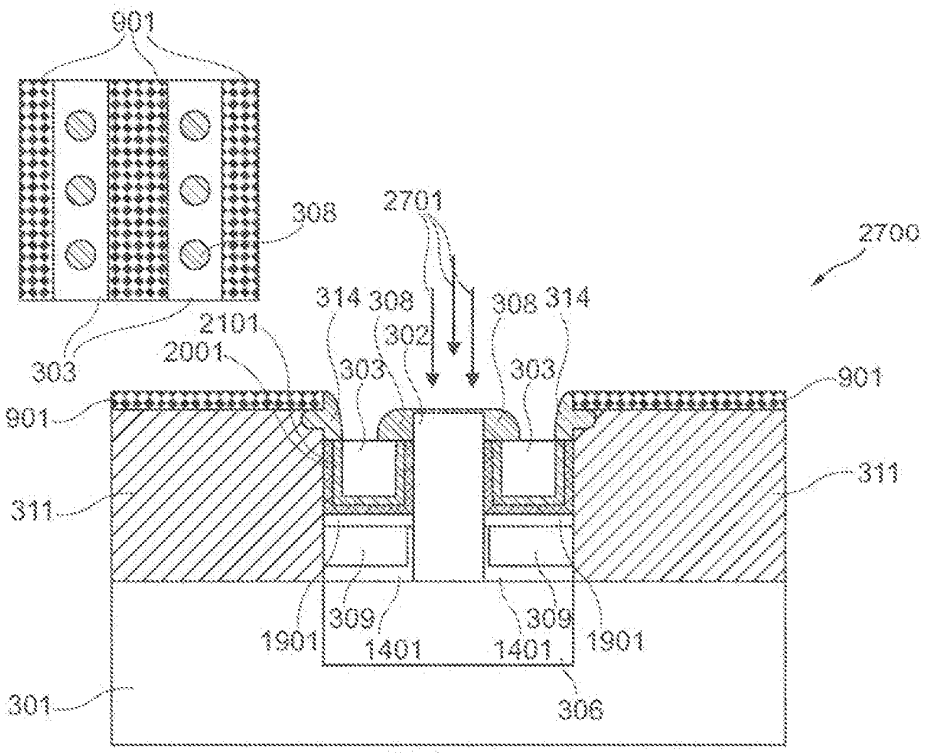

901
308
2701
2700
314
308
308
314
2101
2001
303
302
303
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 27

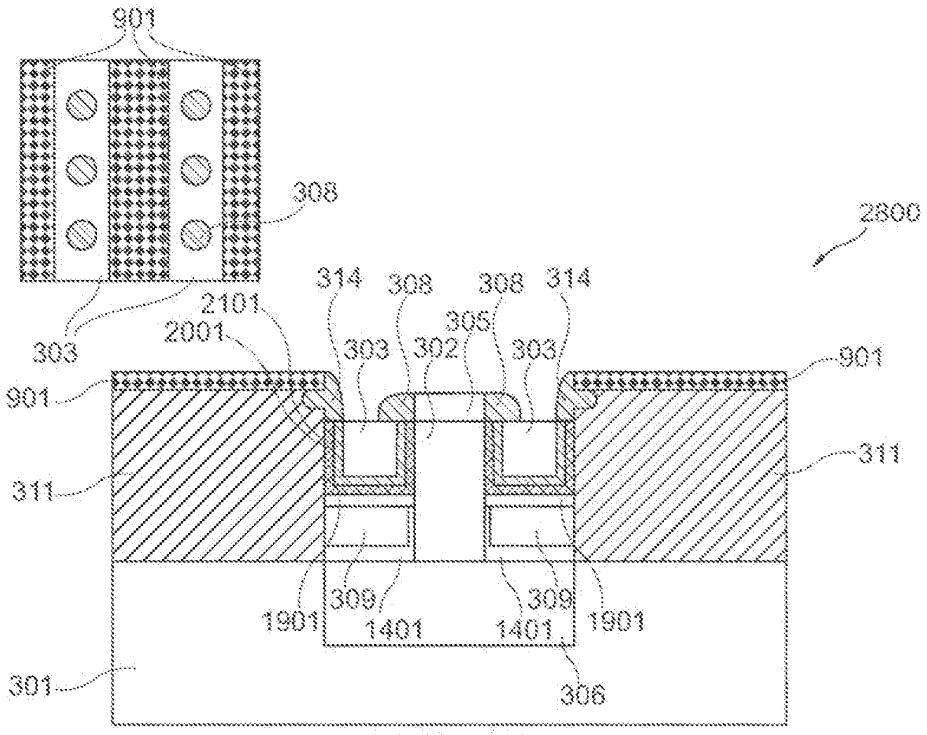

901
308
2800
314
308
308
314
2101
2001
305
303
303
302
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 28

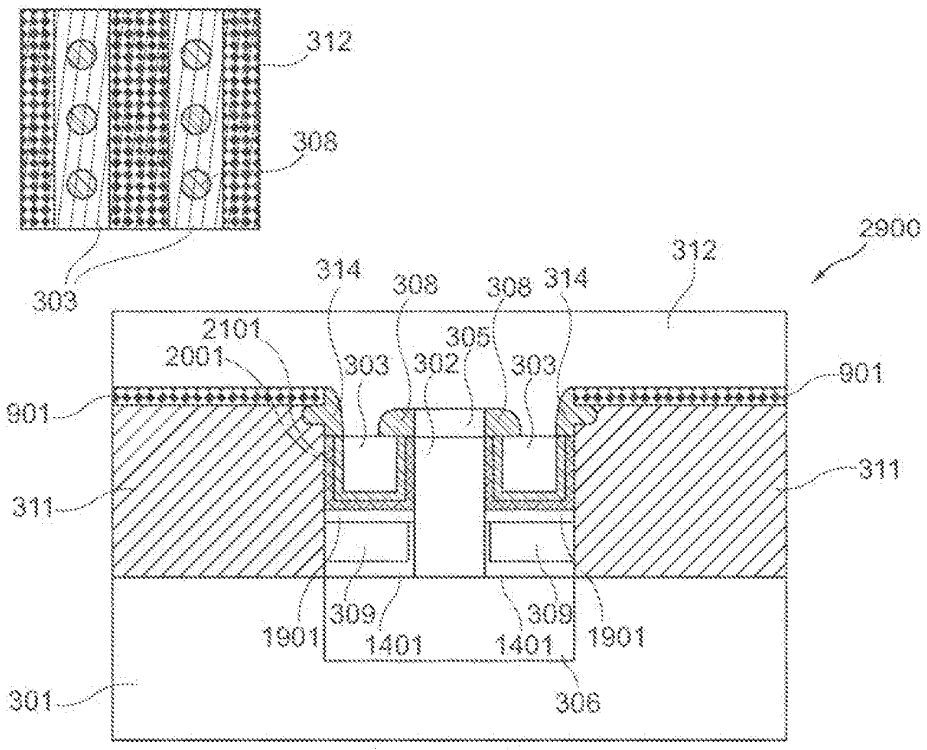

312
308
2900
303
314
308
308
314
312
2101
2001
305
303
302
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 29

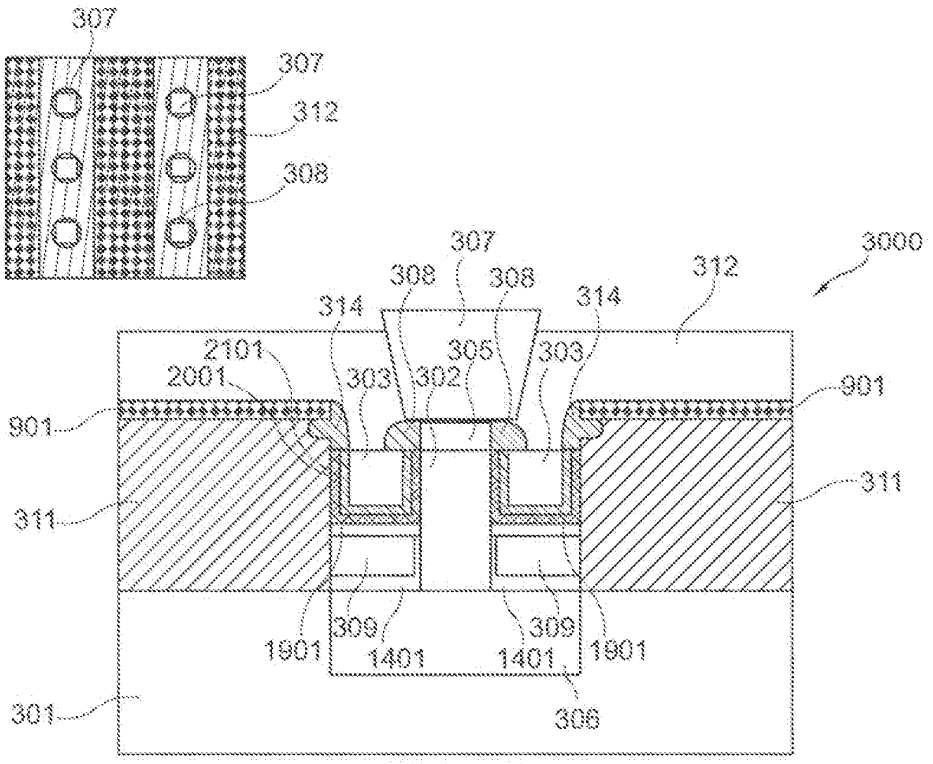

307
307
312
308
307
3000
308
308
312
314
314
2101
305
303
2001
303
302
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 30

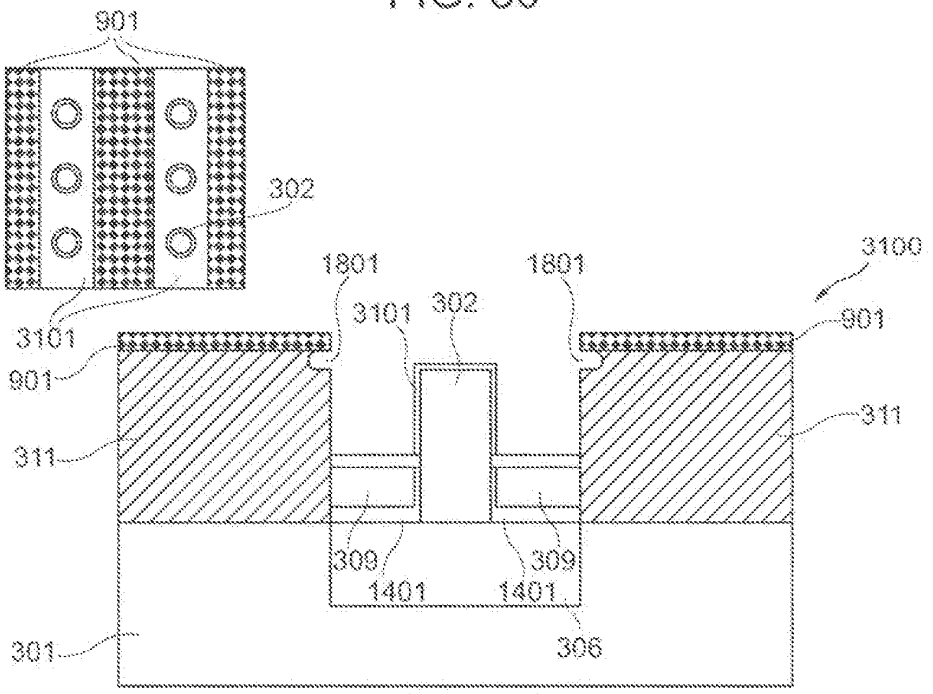

901
302
3100
1801
1801
3101
302
3101
901
901
311
311
309
309
1401
1401
301
306

FIG. 31

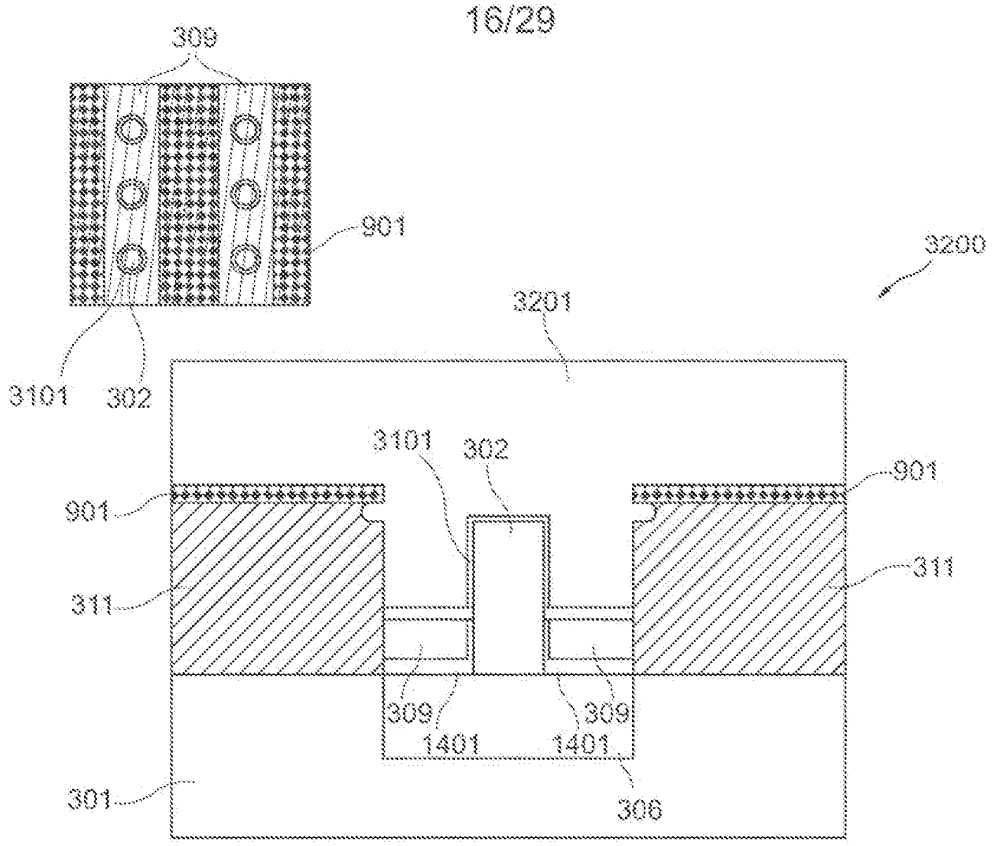

309
901
3200
3201
3101
302
3101
302
901
901
311
311
309
309
1401
1401
301
306

FIG. 32

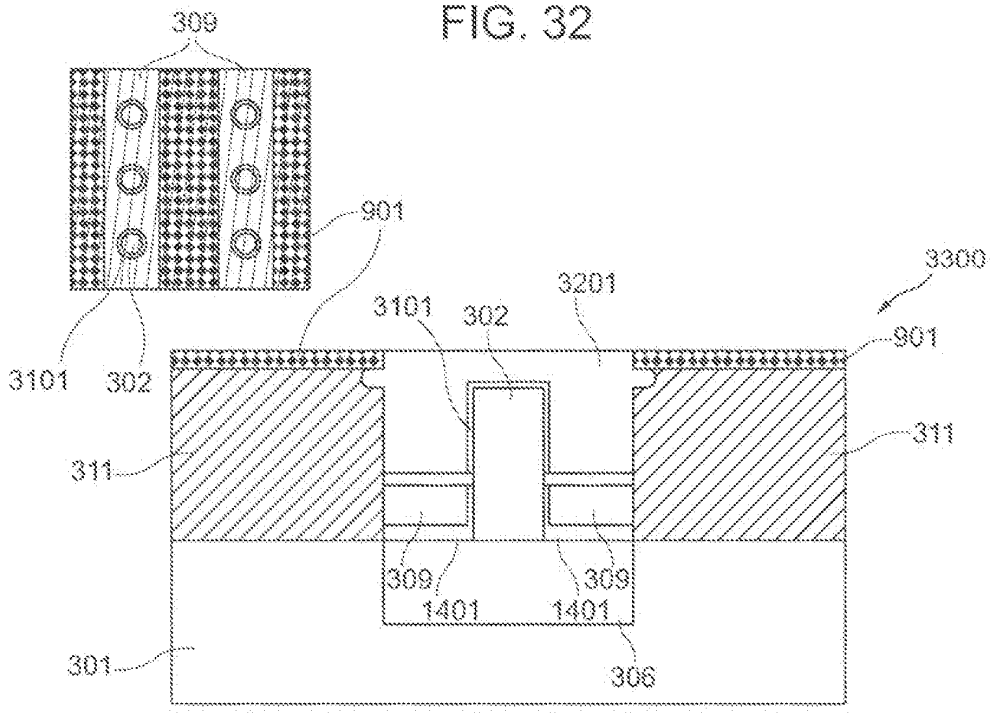

309
901
3300
3201
3101
302
3101
302
901
311
311
309
309
1401
1401
301
306

FIG. 33

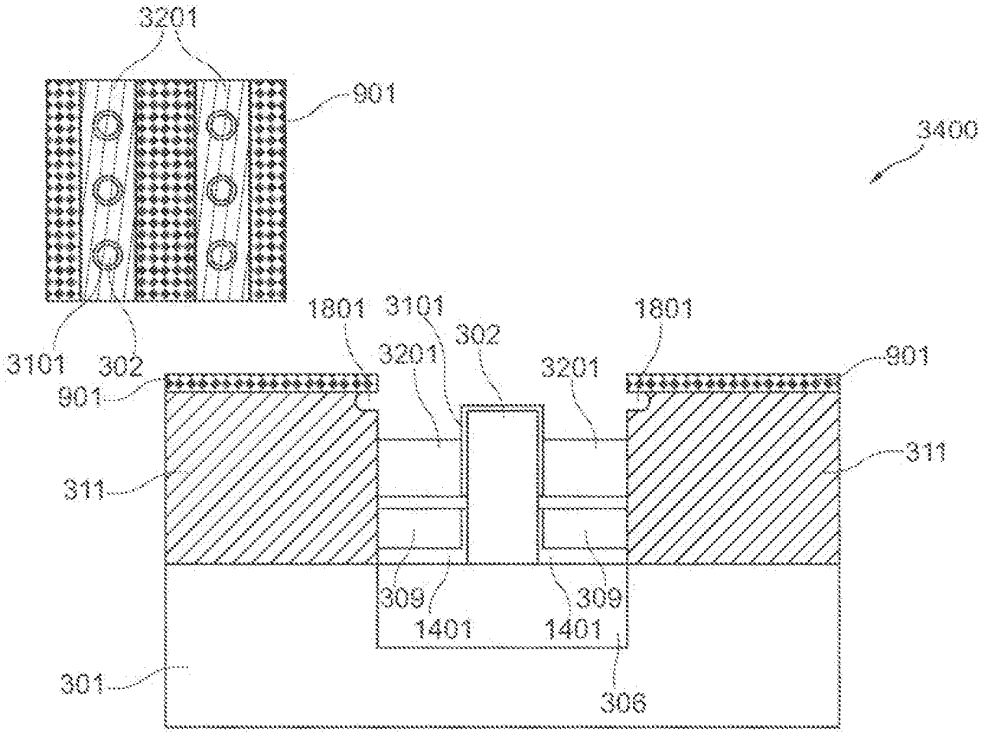

3201
901
3400
1801
3101
302
3101
302
901
3201
3201
901
311
311
309
309
1401
1401
301
306

FIG. 34

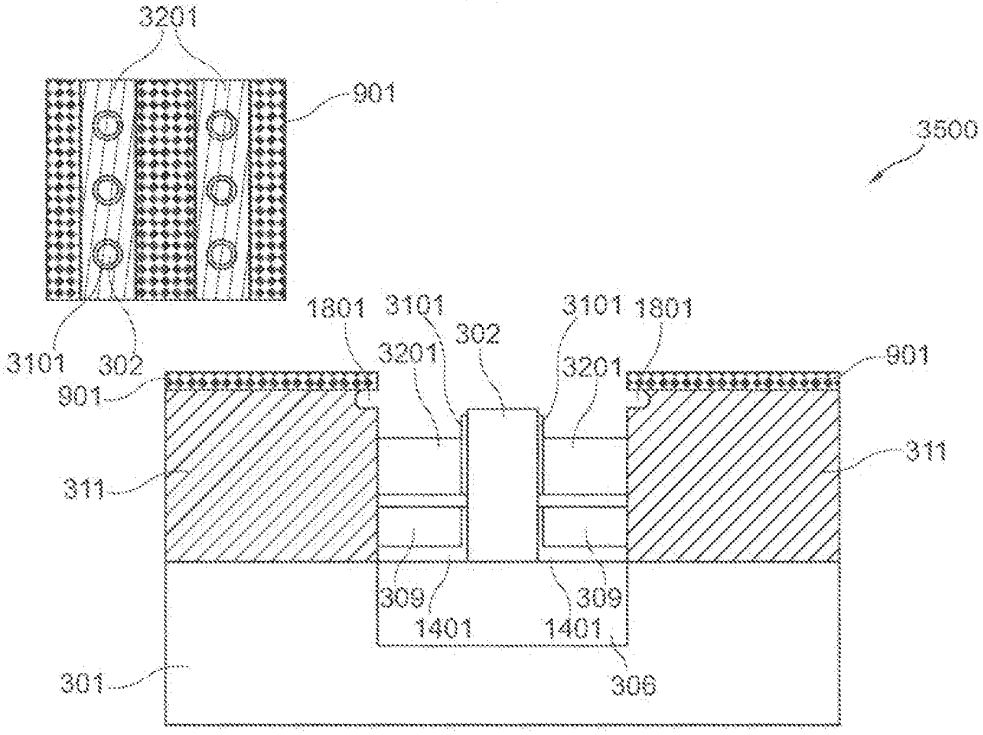

3201
901
3500
1801
3101
302
3101
3101
1801
3101
302
901
3201
3201
901
311
311
309
309
1401
1401
301
306

FIG. 35

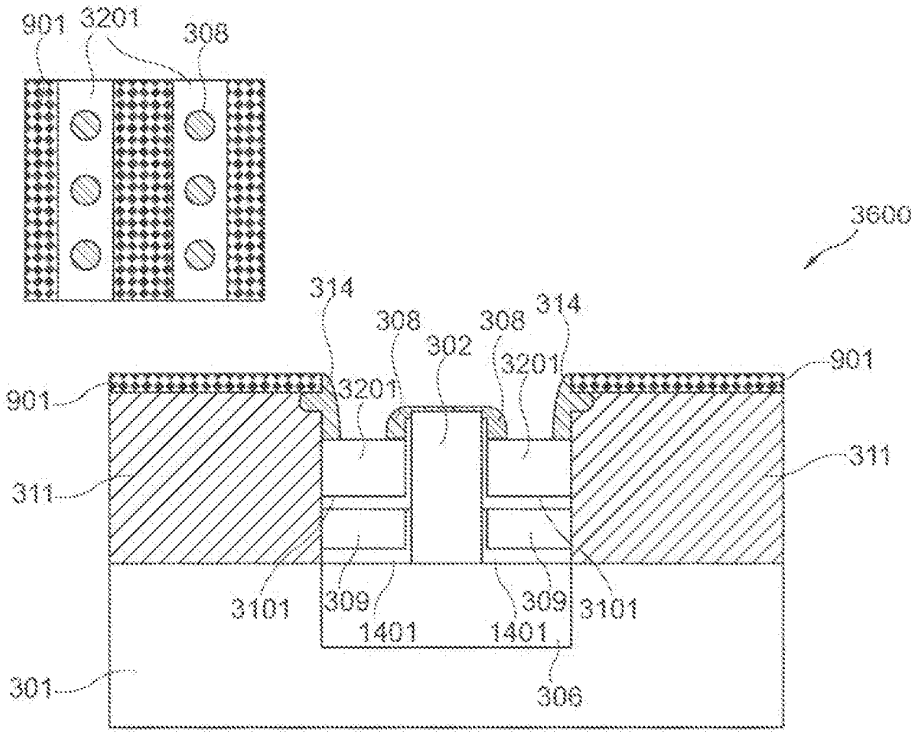

901
3201
308
3600
314
308
308
314
302
3201
3201
901
901
311
311
3101
309
309
3101
1401
1401
301
306

FIG. 36

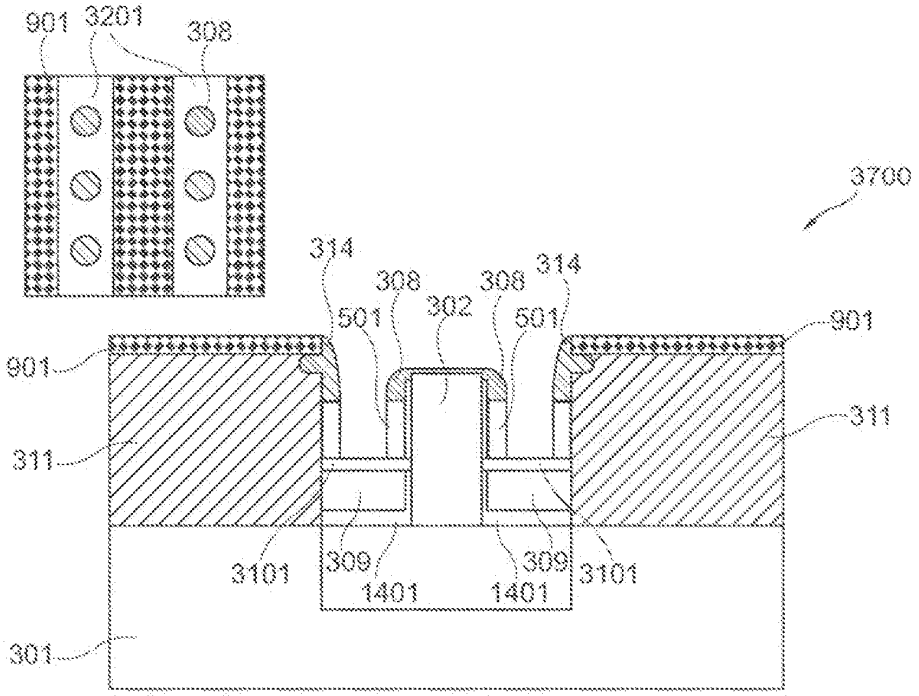

901
3201
308
3700
314
308
308
314
501
302
501
901
901
311
311
3101
309
309
3101
1401
1401
301

FIG. 37

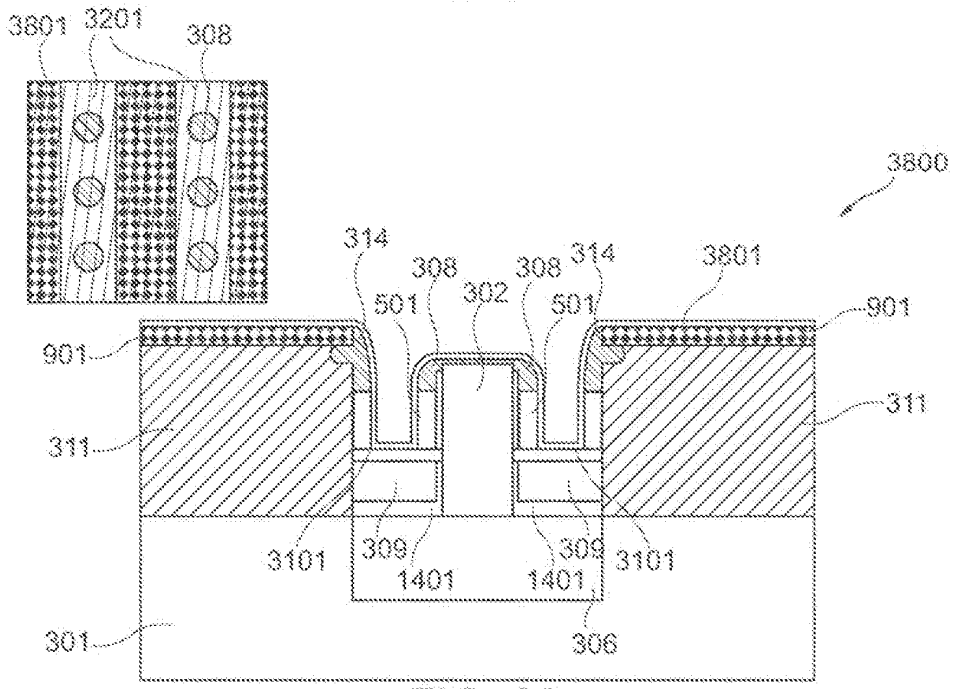

3801
3201
308
3800
314
308
308
314
3801
501
302
501
901
901
311
311
3101
309
309
3101
1401
1401
301
306

FIG. 38

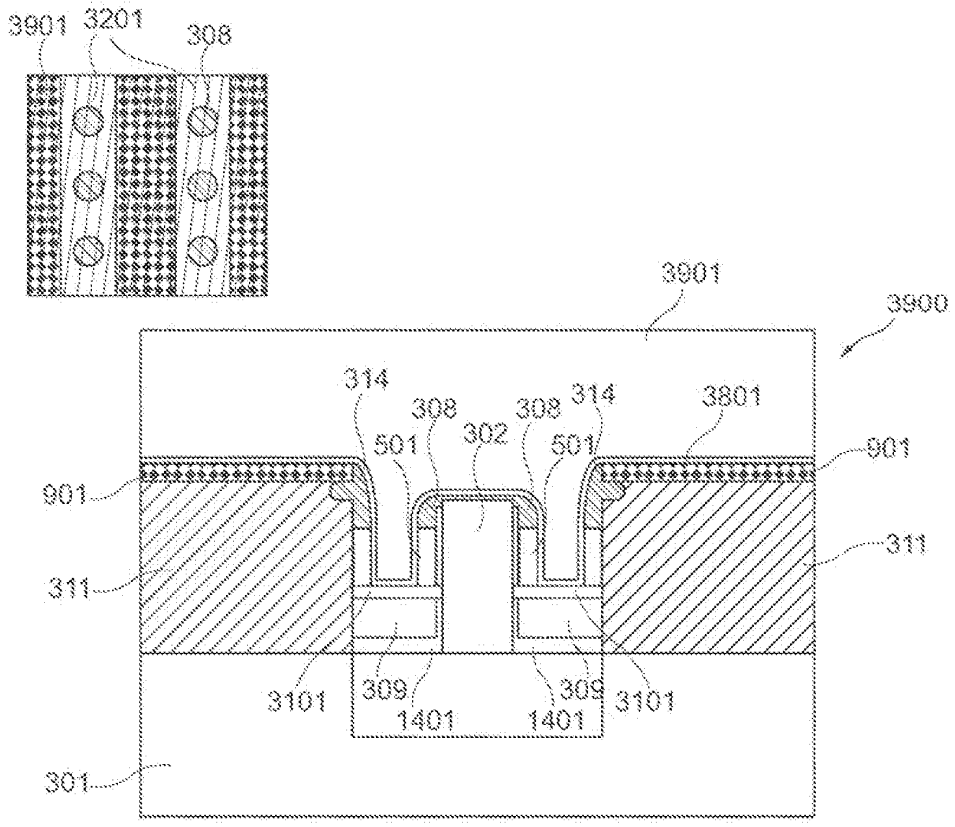

3901
3201
308
3901
3900
314
308
308
314
3801
501
302
501
901
901
311
311
3101
309
309
3101
1401
1401
301

FIG. 39

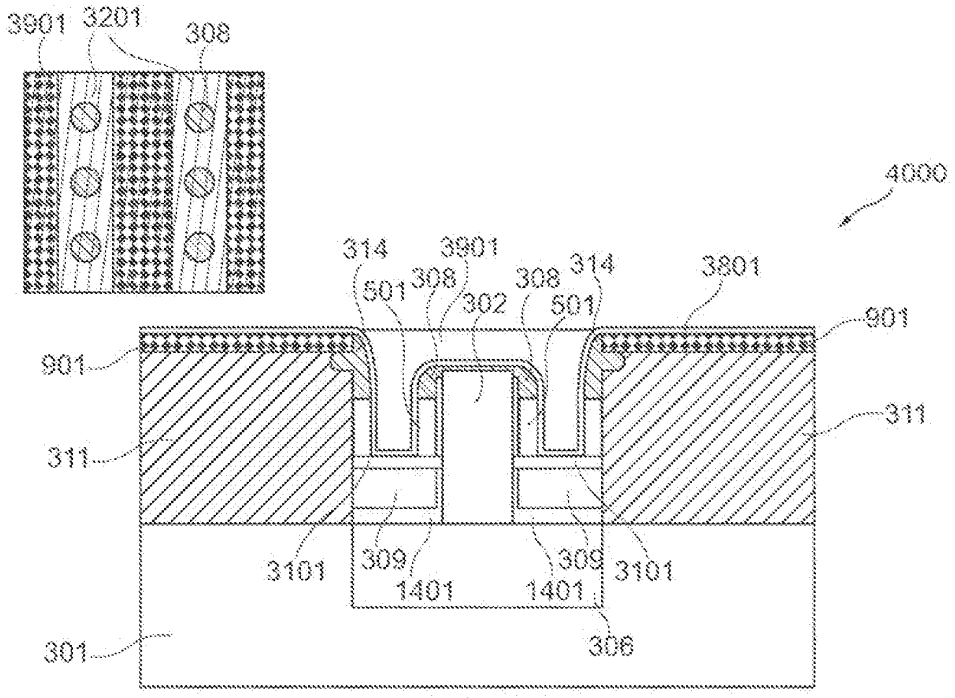

3901
3201
308
4000
314
3901
501
308
308
314
3801
302
501
901
901
311
311
3101
309
309
3101
1401
1401
301
306

FIG. 40

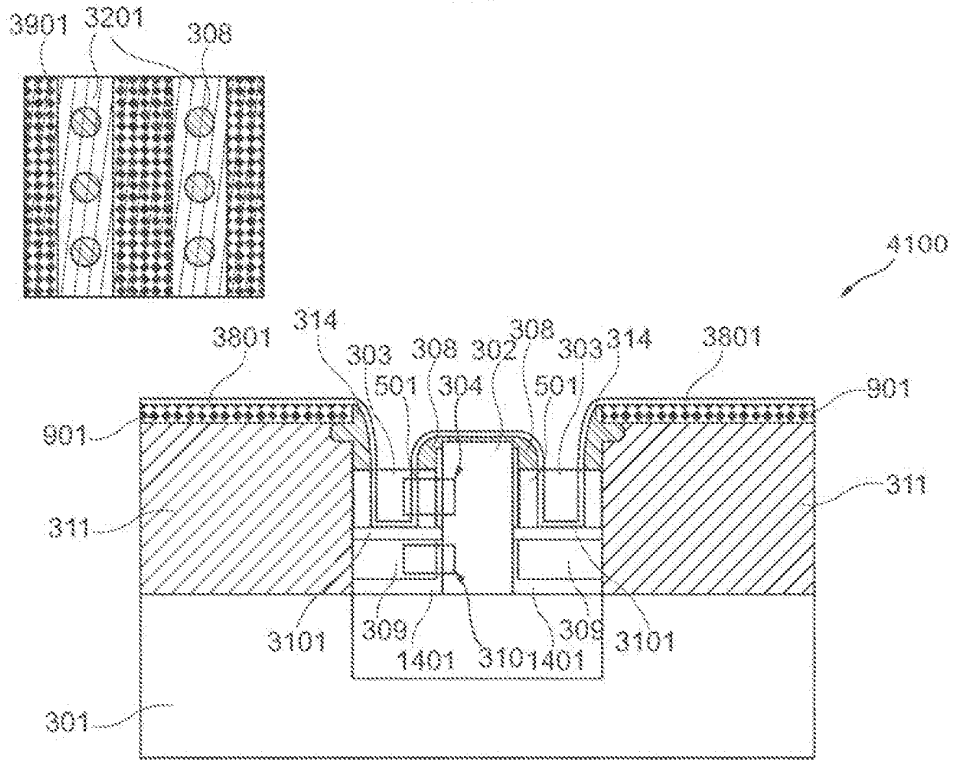

3901
3201
308
4100
3801
314
303
308
302
308
303
314
3801
501
304
501
901
901
311
311
3101
309
309
3101
1401
3101
1401
301

FIG. 41

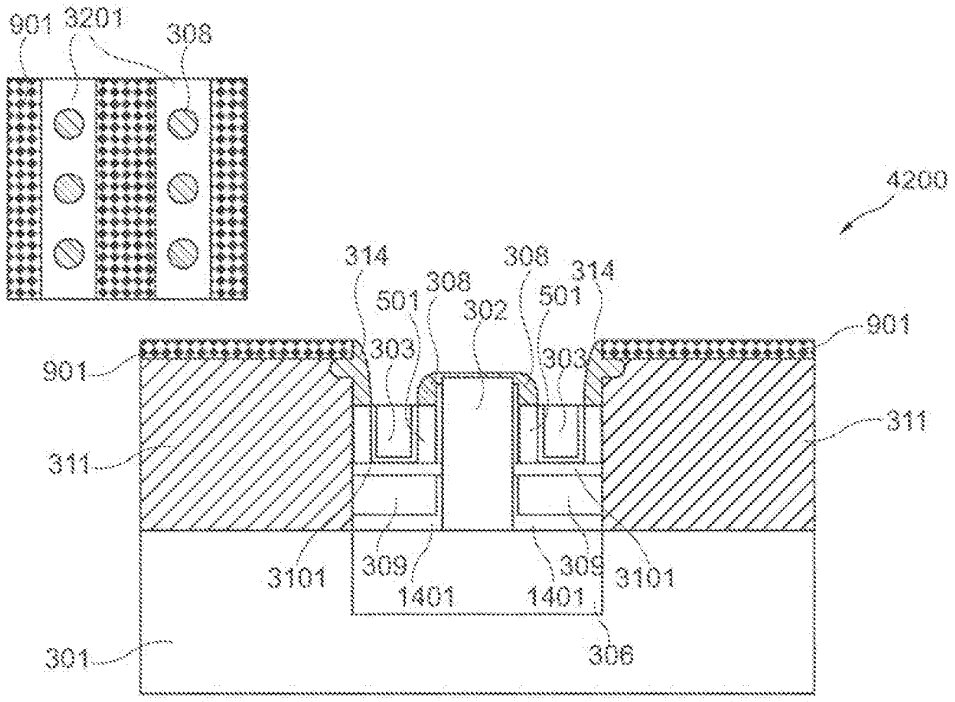

901
3201
308
4200
314
308
308
314
501
308
501
302
303
303
901
901
311
311
3101
309
309
3101
1401
1401
301
306

FIG. 42

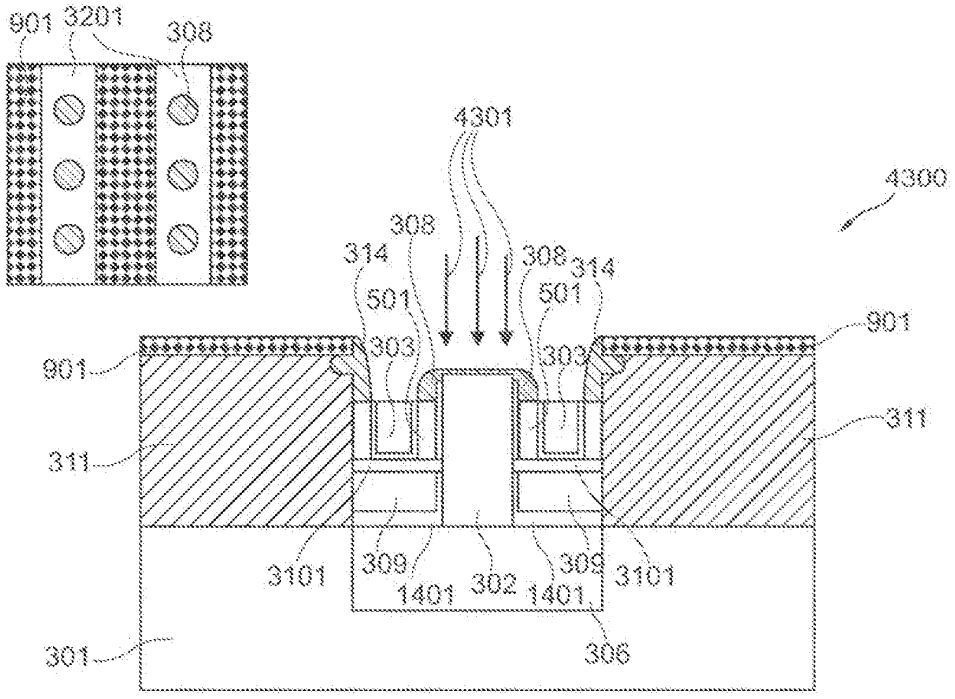

901
3201
308
4301
4300
308
314
308
314
501
501
303
303
901
901
311
311
3101
309
302
309
3101
1401
1401
301
306

FIG. 43

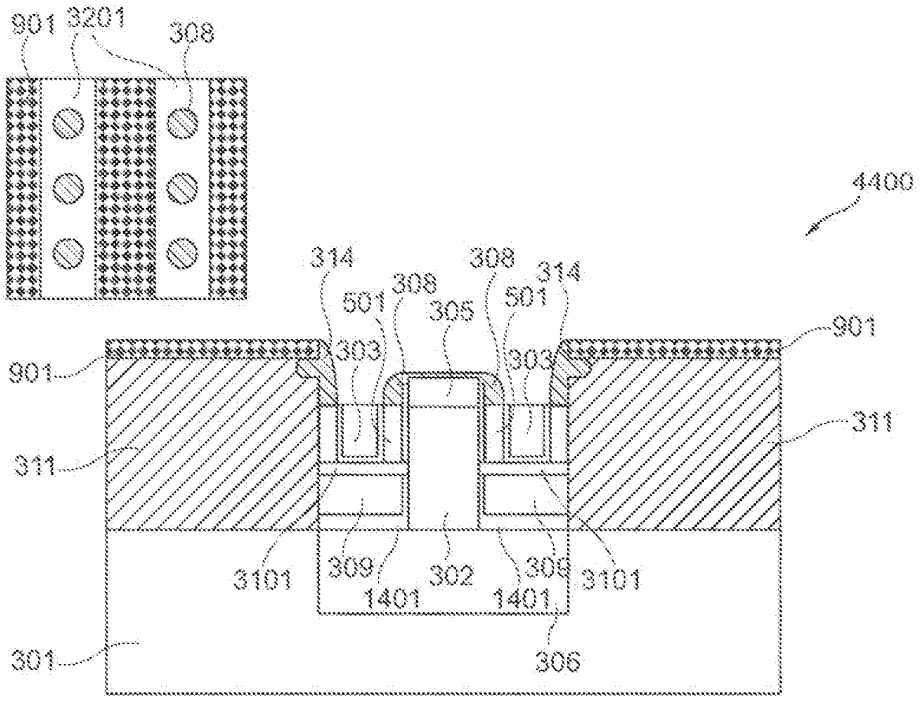

901
3201
308
4400
314
308
308
314
501
501
305
303
303
901
901
311
311
3101
309
302
309
3101
1401
1401
301
306

FIG. 44

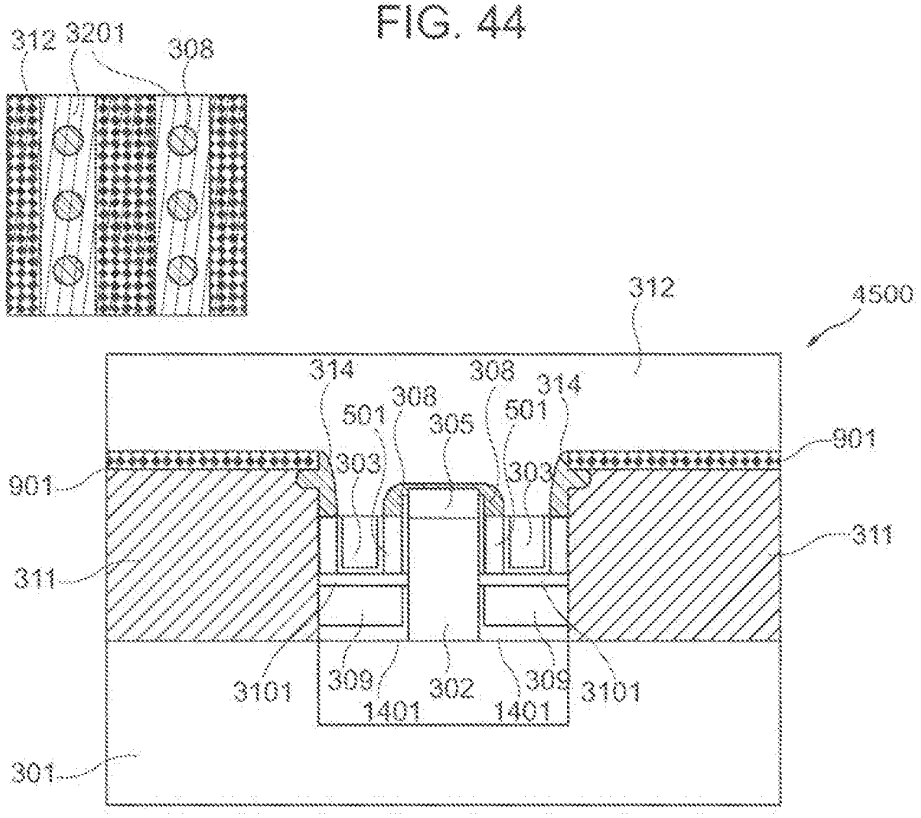

312
3201
308
312
4500
314
308
308
314
501
501
305
303
303
901
901
311
311
3101
309
302
309
3101
1401
1401
301

FIG. 45

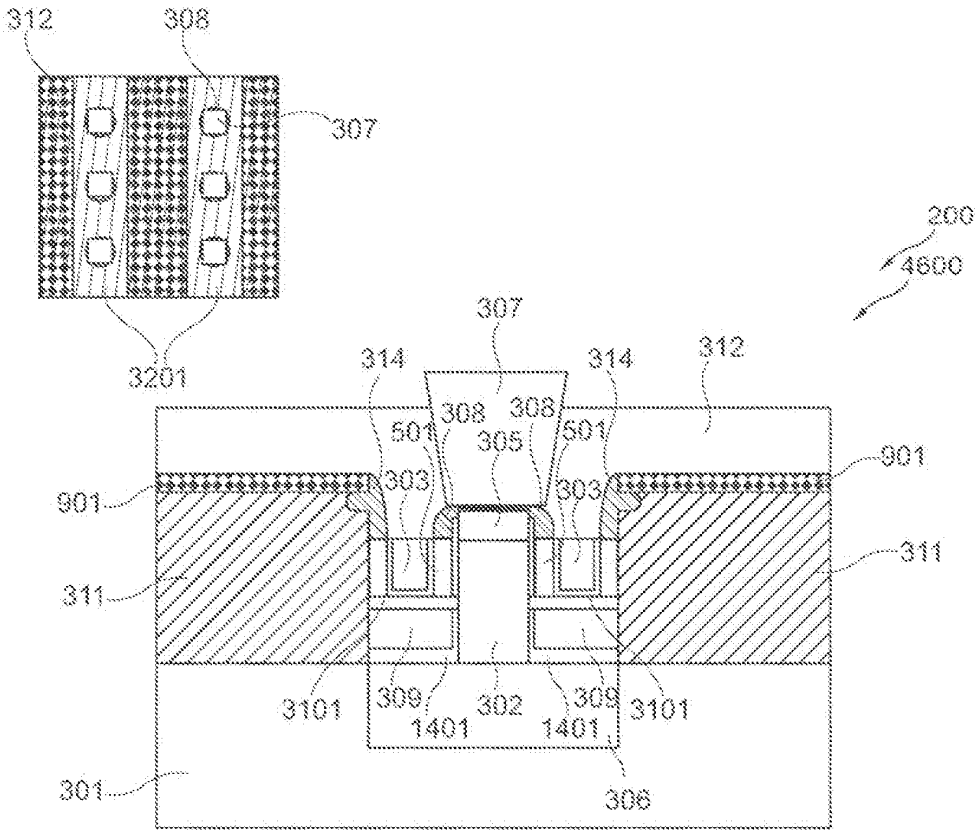

312
308
307
3201
200
4600
307
314
314
312
308
308
501
501
305
901
303
303
901
311
311
3101
309
302
309
3101
1401
1401
301
306

FIG. 46

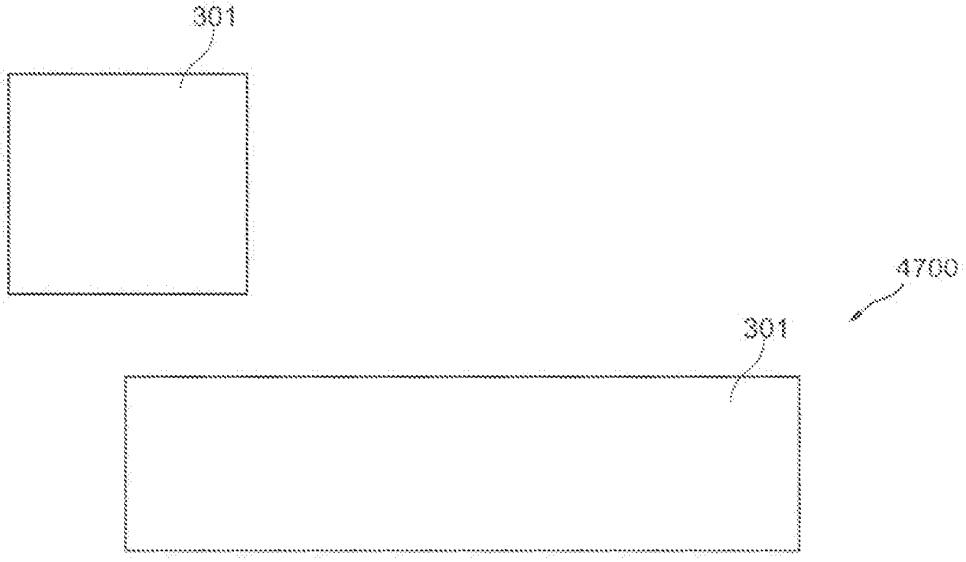

301
4700
301

FIG. 47

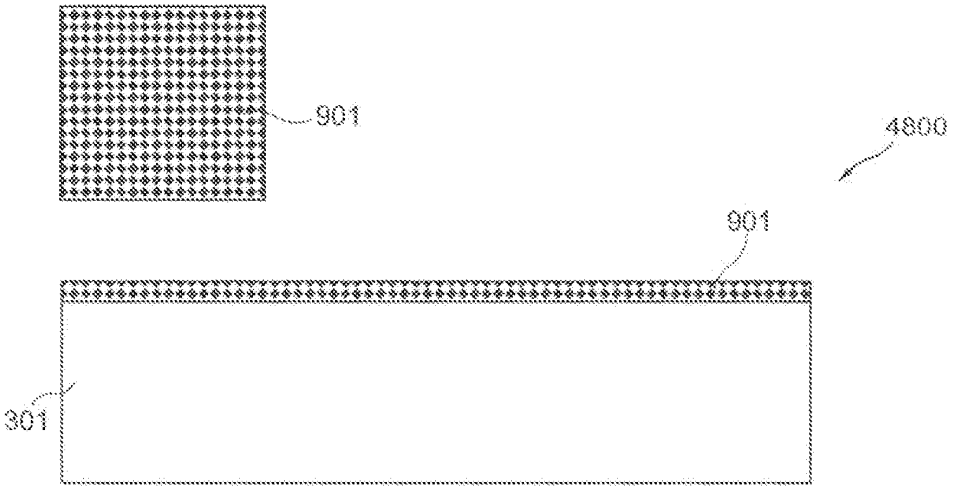


FIG. 48

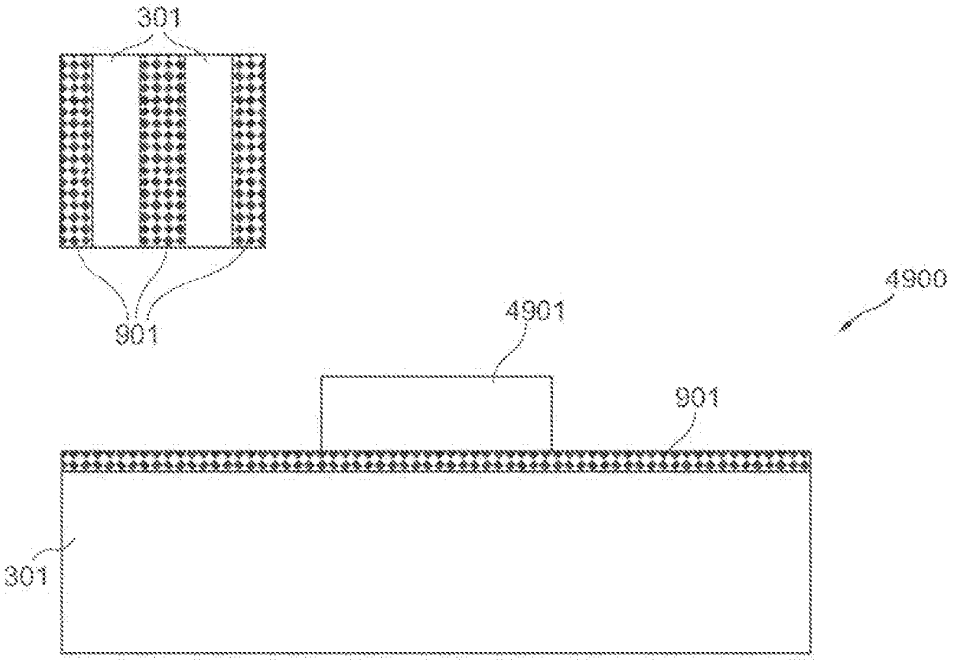


FIG. 49

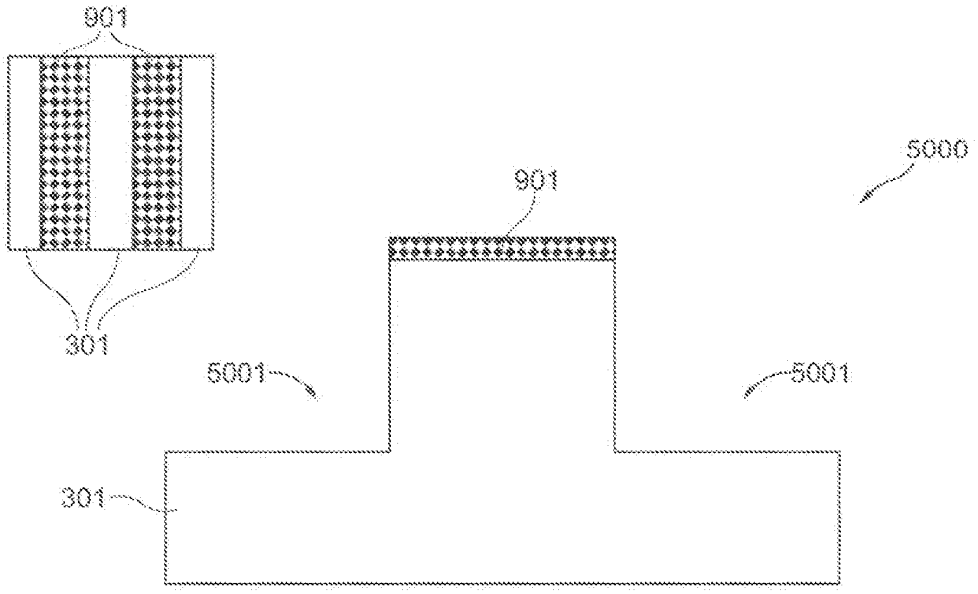


FIG. 50

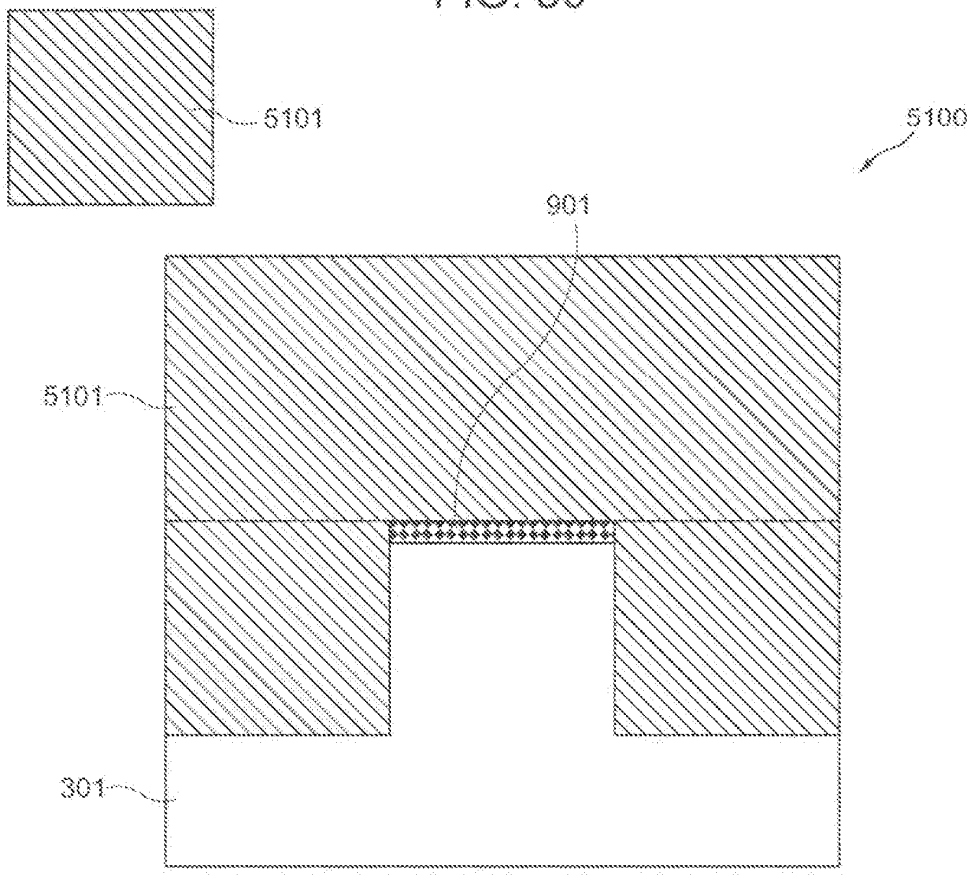


FIG. 51

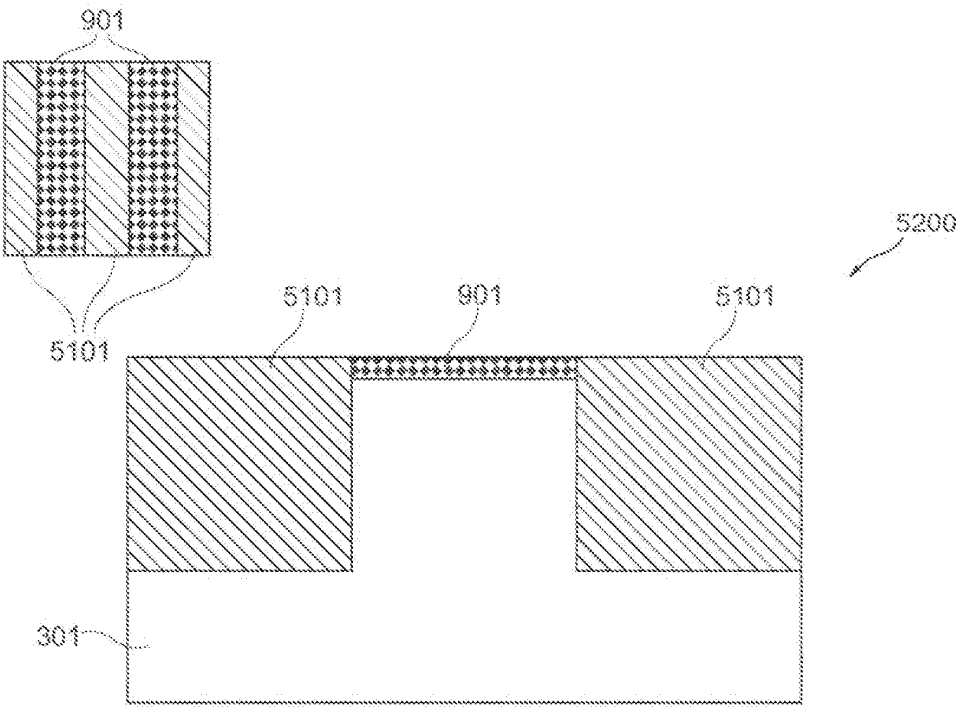

901
5200
5101
5101
901
5101
301

FIG. 52

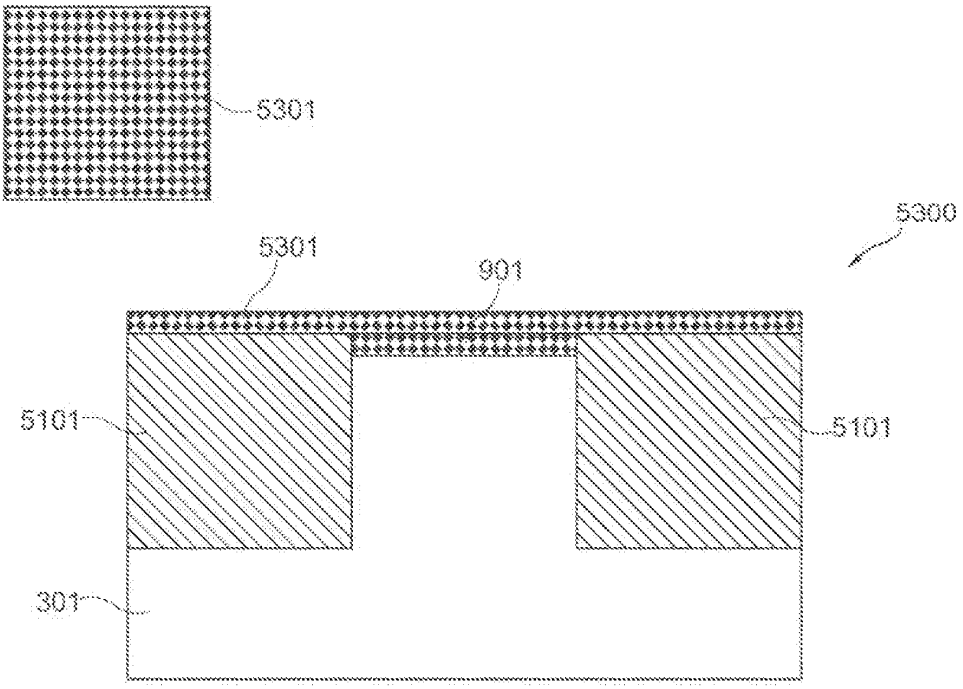

5301
5300
5301
901
5101
5101
301

FIG. 53

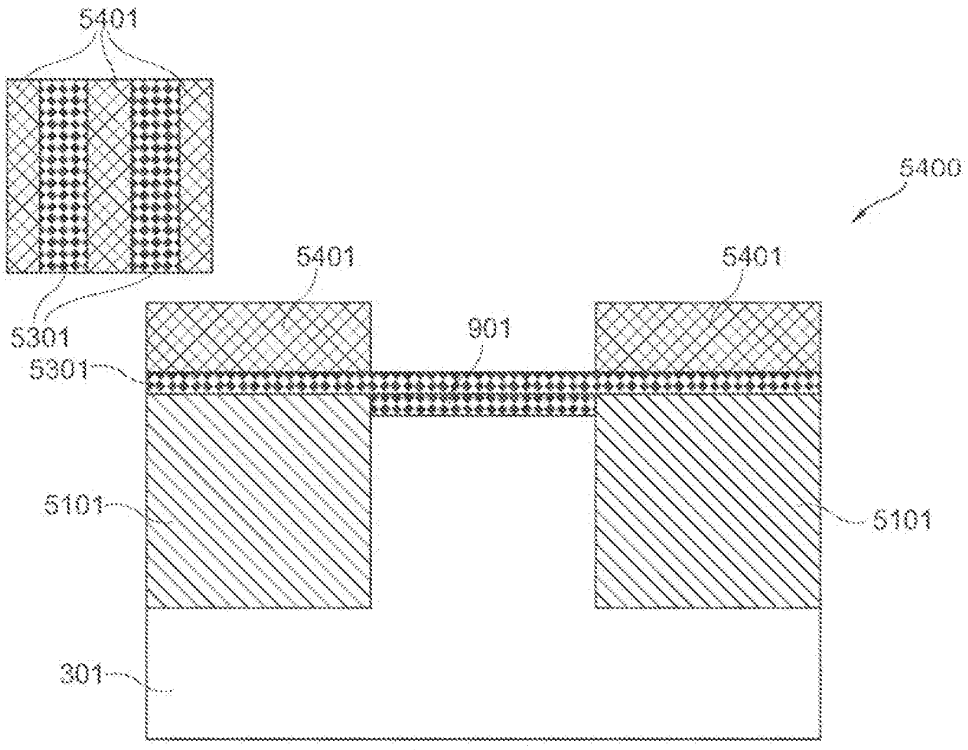

5401
5400
5401
5401
5301
901
5301
5101
5101
301

FIG. 54

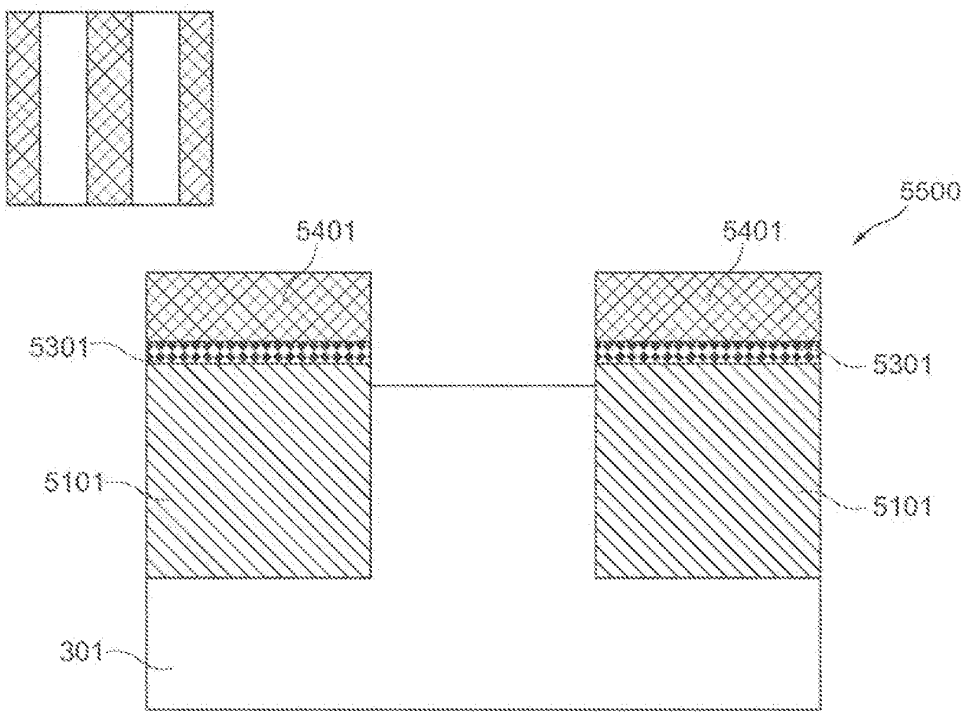

5500
5401
5401
5301
5301
5101
5101
301

FIG. 55

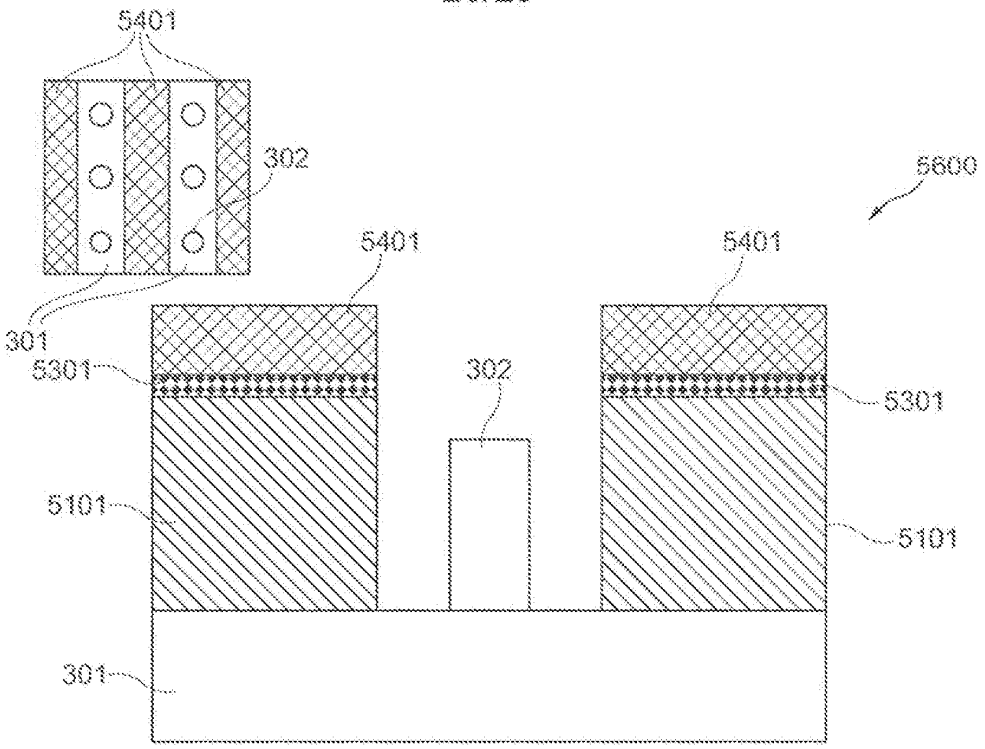

5401
302
5600
5401
5401
301
5301
302
5301
5101
5101
301

FIG. 56

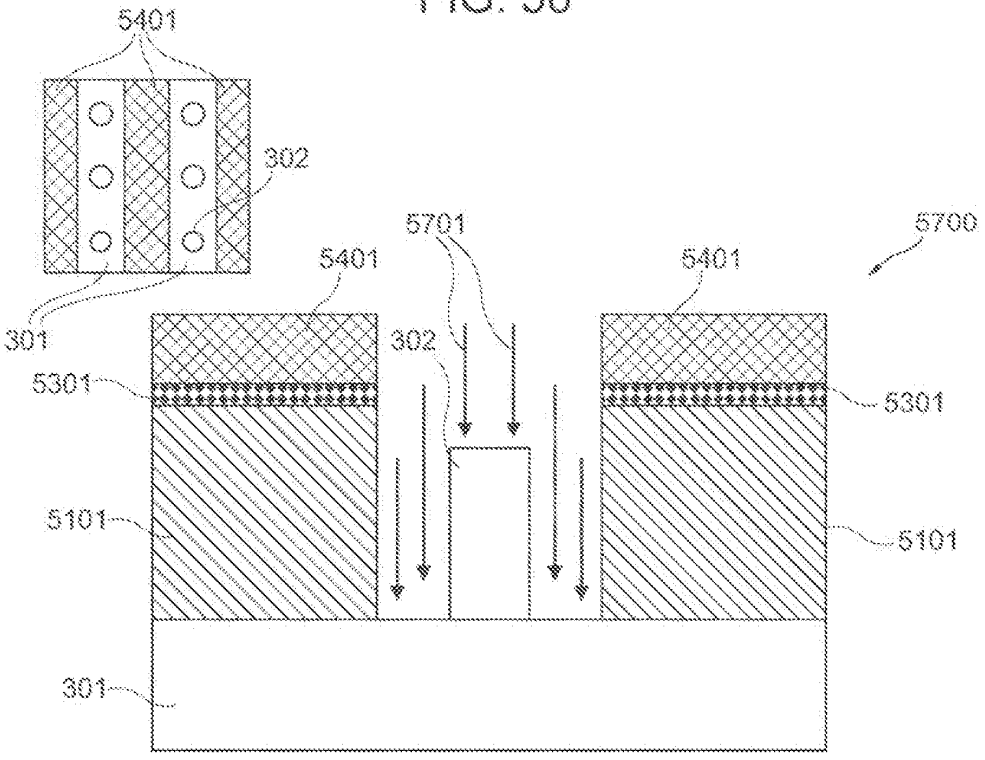

5401
302
5701
5700
5401
5401
301
302
5301
5301
5101
5101
301

FIG. 57

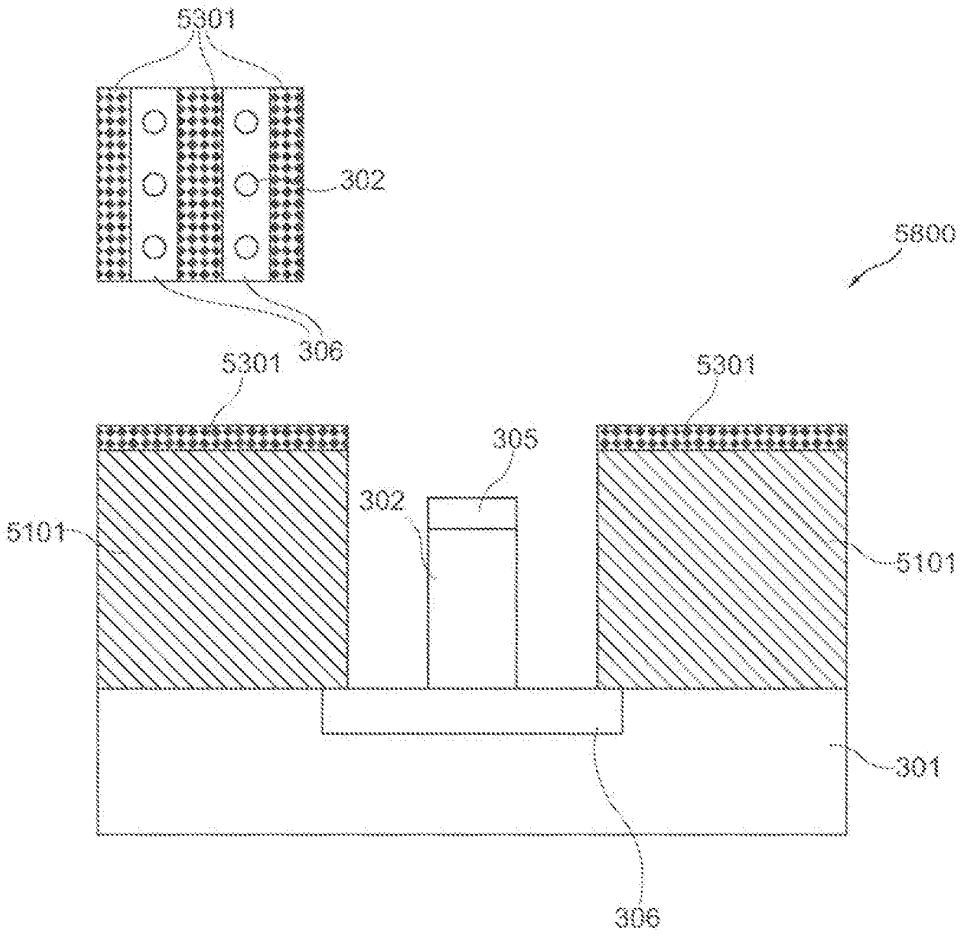


FIG. 58

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/051478

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/28 H01L21/336 H01L21/8246 H01L21/8247 H01L27/115
H01L29/788 H01L29/792 G11C16/04 H01L29/423 H01L29/06
H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PEIN H ET AL: "PERFORMANCE OF THE 3-D PENCIL FLASH EPROM CELL AND MEMORY ARRAY" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 42, no. 11, 1 November 1995 (1995-11-01), pages 1982-1991, XP000582412 ISSN: 0018-9383 the whole document	1-18
X	WO 2004/040667 A (INFINEON TECHNOLOGIES AG [DE]; GRAHAM ANDREW [DE]; HOFMANN FRANZ [DE];) 13 May 2004 (2004-05-13) the whole document	1-18
Y	EP 1 420 414 A (SAMSUNG ELECTRONICS CO LTD [KR]) 19 May 2004 (2004-05-19) the whole document	1-18
	-/--	

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 August 2008	18/08/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Neumann, Andreas

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/051478

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2005/124872 A (KONINKL PHILIPS ELECTRONICS NV [NL]; HIJZEN ERWIN A [BE]; BAKKERS ERIK) 29 December 2005 (2005-12-29) page 7, line 28 - page 8, line 19; figure 2	1-18
A	US 6 433 382 B1 (ORLOWSKI MARIUS [US] ET AL) 13 August 2002 (2002-08-13) column 3, line 57 - column 4, line 11; figure 1	9,10

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2008/051478

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2004040667 A	13-05-2004	DE 10250829 A1	19-05-2004
		EP 1568087 A1	31-08-2005
		JP 2006504278 T	02-02-2006
		US 2006011972 A1	19-01-2006
EP 1420414 A	19-05-2004	CN 1501503 A	02-06-2004
		DE 60300477 D1	12-05-2005
		DE 60300477 T2	23-02-2006
		JP 4047797 B2	13-02-2008
		JP 2004172616 A	17-06-2004
		JP 2007329500 A	20-12-2007
		KR 20040043043 A	22-05-2004
		US 2004095837 A1	20-05-2004
WO 2005124872 A	29-12-2005	CN 1977385 A	06-06-2007
		EP 1759417 A1	07-03-2007
		JP 2008503081 T	31-01-2008
		US 2008029909 A1	07-02-2008
US 6433382 B1	13-08-2002	NONE	

Sandisk Technologies, Inc. - Ex. 1002, Page 000718

Espacenet

Bibliographic data: WO2011162725 (A1) — 2011-12-29

NANOWIRE TRANSISTOR AND METHOD FOR MANUFACTURING A NANOWIRE TRANSISTOR

Inventor(s): SINGH NAVAB [SG]; SHEN NANSHENG [SG]; CHEN ZHIXIAN [SG]; LO GUO QIANG PATRICK [SG] ± (SINGH, NAVAB, ; SHEN, NANSHENG, ; CHEN, ZHIXIAN, ; LO, GUO QIANG PATRICK)

Applicant(s): AGENCY SCIENCE TECH & RES [SG]; SINGH NAVAB [SG]; SHEN NANSHENG [SG]; CHEN ZHIXIAN [SG]; LO GUO QIANG PATRICK [SG] ± (AGENCY FOR SCIENCE, TECHNOLOGY AND RESEARCH, ; SINGH, NAVAB, ; SHEN, NANSHENG, ; CHEN, ZHIXIAN, ; LO, GUO QIANG PATRICK)

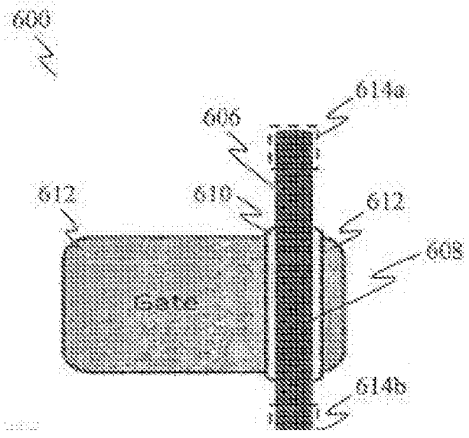
Classification: - international: ***B82Y10/00; H01L29/772***
- cooperative: **B82Y10/00**; **B82Y40/00**; **G11C16/0483**; **H01L29/0665**; **H01L29/0676**; **H01L29/4232**; **H01L29/66439**; **H01L29/66666**; **H01L29/66833**; **H01L29/775**; **H01L29/78642**; **H01L29/7926**; H01L27/11578; H01L27/11582

Application number: WO2011SG00222 20110622

Priority number(s): SG20100004576 20100625

Abstract of WO2011162725 (A1)

According to embodiments of the present invention, a nanowire transistor is provided. The nanowire transistor includes a carrier; a vertical nanowire structure extending from the carrier, the vertical nanowire structure comprising a channel region, and the vertical nanowire structure being made of the same material as the carrier; a gate insulator region covering at least a portion of the vertical nanowire structure; and at least one gate region covering at least a portion



Sandisk Technologies, Inc. - Ex. 1002, Page 000719

of the gate insulator region. In various embodiments, there is no doped junction between the channel region and the source/drain regions of the nanowire transistor.

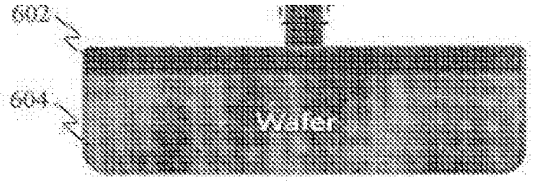


FIG. 6

Sandisk Technologies, Inc. - Ex. 1002, Page 000720

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 October 2013 (03.10.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/148112 A1

(51) International Patent Classification:
H01L 29/792 (2006.01)

(21) International Application Number:
PCT/US2013/029784

(22) International Filing Date:
8 March 2013 (08.03.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/431,069 27 March 2012 (27.03.2012) US

(71) Applicant: **CYPRESS SEMICONDUCTOR CORPORATION** [US/US]; 198 Champion Court, San Jose, California 95134 (US).

(72) Inventors; and
(71) Applicants : **JENNE, Fredrick** [US/US]; 790 Lynxwood Court, Sunnyvale, California 94086 (US). **RAMKUMAR, Krishnaswamy** [US/US]; 1193 Lynbrook Way, San Jose, California 95129 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: SONOS STACK WITH SPLIT NITRIDE MEMORY LAYER

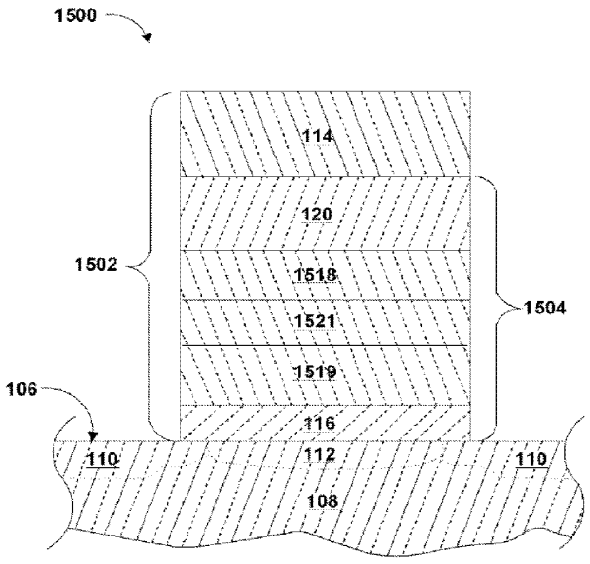


FIG. 11

(57) Abstract: Embodiments of a non-planar memory device including a split charge-trapping region and methods of forming the same are described. Generally, the device comprises: a channel formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide overlying the channel; a split charge-trapping region overlying the tunnel oxide, the split charge-trapping region including a bottom charge-trapping layer comprising a nitride closer to the tunnel oxide, and a top charge-trapping layer, wherein the bottom charge-trapping layer is separated from the top charge-trapping layer by a thin anti-tunneling layer comprising an oxide. Other embodiments are also disclosed.

WO 2013/148112 A1

Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

Published:

— *with international search report (Art. 21(3))*

SONOS STACK WITH SPLIT NITRIDE MEMORY LAYER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of co-pending U.S. application Ser. No. 12/767,105, filed April 26, 2010, which claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 61/172,320, filed on April 24, 2009, both of which are incorporated by reference herein.

TECHNICAL FIELD

[0002] Embodiments of the present invention relate to the field of semiconductor devices.

BACKGROUND

[0003] Non-volatile semiconductor memories, such as a split gate flash memory, sometimes use a stacked floating gate structure, in which electrons are induced into a floating gate of a memory cell to be programmed by biasing a control gate and grounding a body region of a substrate on which the memory cell is formed.

[0004] An oxide-nitride-oxide (ONO) stack may be used as either a charge storing layer, as in silicon-oxide-nitride-oxide-silicon (SONOS) transistor, or as an isolation layer between the floating gate and control gate, as in a split gate flash memory.

[0005] FIG. 1 is a partial cross-sectional view of a structure for a semiconductor device 100 having a SONOS gate stack or structure 102. The structure 100 includes a conventional ONO stack 104 formed over a surface 106 of a silicon substrate 108. The device 100 typically further includes one or more diffusion regions 110, such as source and drain regions, aligned to the gate stack and separated by a channel region 112. The SONOS structure 102 includes a polysilicon gate layer 114 formed upon and in contact with the ONO stack 104. The poly gate 114 is separated or electrically isolated from the

substrate 108 by the ONO stack 104. The ONO stack 104 generally includes a lower (tunnel) oxide layer 116, a nitride or oxynitride layer 118 which serves as a charge storing or memory layer for the device 100, and a top oxide layer 120 overlying the nitride or oxynitride layer 118.

[0006] One problem with this conventional SONOS structure 102 is the poor data retention of the nitride or oxynitride layer 118 that limits the device 100 lifetime and/or its use in several applications due to leakage current through the layer. Another problem with conventional SONOS structures 102 is that the stoichiometry of the layer 118 is non-uniform across the thickness of the layer. In particular, the layer 118 is conventionally formed or deposited in a single step using a single process gas mixture and fixed or constant processing conditions in an attempt to provide a homogeneous layer having a high nitrogen and high oxygen concentration across the thickness of the relatively thick layer. However, this may result in nitrogen, oxygen and silicon concentrations that vary throughout the conventional layer 118. Consequently, the charge storage characteristics, and in particular programming and erase speed and data retention of a memory device 100 made with the ONO stack 104, are adversely effected.

[0007] FIG. 2-5 illustrate charge retention and migration in a conventional SONOS structure such as the one illustrated in FIG. 1. Charge traps are distributed through the nitride layer 118. The distribution of traps is uniform under ideal stoichiometric conditions (FIG. 2), but typically the distribution would not be so ideally uniform. When an ERASE (FIG. 3) is performed, holes migrate toward the blocking oxide 120. Electron charge accumulates at the layer boundaries after programming (FIG. 4). This stored charge distribution can lead to significant leakage due to tunneling at the

Sandisk Technologies, Inc. - Ex. 1002, Page 000724

nitride boundaries, for example by the process illustrated in the energy diagram FIG. 5, in which stored charge transitions among trapped states (e.g. E_{TA}, E_{TD}) to cause leakage.

[0008] Thus there is an ongoing need for a memory device that exhibits improved data retention and improved stoichiometry.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] These and various other features and advantages of the present structure and method will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

[0010] FIG. 1 is a cross-sectional view of a conventional SONOS structure.

[0011] FIGs. 2-4 illustrate charge retention and migration in a conventional SONOS structure such as the one illustrated in FIG. 1.

[0012] FIG. 5 illustrates an energy band diagram for a conventional SONOS structure, in which stored charge transitions among trapped states (e.g. E_{TA}, E_{TD}) to cause leakage.

[0013] FIG. 6 is a cross-sectional view of a SONNOS structure.

[0014] FIG. 7-9 illustrate charge retention and migration in a SONNOS structure such as the one illustrated in FIG. 6.

[0015] FIG. 10 illustrates an energy band diagram for a SONNOS structure in which stored charge transitions among trapped states (e.g. E_{TA}, E_{TD}) to cause leakage.

[0016] FIG. 11 is a cross-sectional view of a SONONOS structure.

Sandisk Technologies, Inc. - Ex. 1002, Page 000725

[0017] FIG. 12-14 illustrate charge retention and migration in a SONONOS structure such as the one illustrated in FIG. 14.

[0018] FIG. 15 illustrates an energy band diagram for a SONONOS structure in which stored charge transitions among trapped states (e.g. E_{TA}, E_{TD}) to cause leakage.

[0019] FIG. 16A illustrates a non-planar multigate device including a split charge-trapping region;

[0020] FIG. 16B illustrates a cross-sectional view of the non-planar multigate device of FIG. 16A.

[0021] FIGs. 17A and 17B illustrate a non-planar multigate device including a split charge-trapping region and a horizontal nanowire channel.

[0022] FIGs. 18A and 18B illustrate a non-planar multigate device including a split charge-trapping region and a vertical nanowire channel.

[0023] FIG. 19A and 19B illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 18A.

[0024] FIG. 20A and 20B illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 18A.

DETAILED DESCRIPTION

[0025] References to "one embodiment" or "an embodiment" do not necessarily refer to the same embodiment, although they may.

[0026] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in the sense

Sandisk Technologies, Inc. - Ex. 1002, Page 000726

of "including, but not limited to." Words using the singular or plural number also include the plural or singular number respectively. Additionally, the words "herein," "above," "below" and words of similar import, when used in this application, refer to this application as a whole and not to any particular portions of this application. When the claims use the word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list and any combination of the items in the list.

Overview

[0027] A charge-storage circuit may be formed with multiple charge storing layers including multiple nitride layers having differing concentrations of oxygen, nitrogen and/or silicon. The nitride layers may include at least a top nitride layer and a bottom nitride layer. At least the bottom nitride layer may comprise silicon oxynitride (e.g. $Si_xO_yN_x$). The stoichiometric compositions of the layers may be tailored or selected such that the lower or bottom nitride has a high oxygen and silicon content, and the top nitride layer has high silicon and a high nitrogen concentration with a low oxygen concentration to produce a silicon-rich nitride or oxynitride. The silicon-rich and oxygen-rich bottom nitride layer reduces stored charge loss without compromising device speed or an initial (beginning of life) difference between program and erase voltages. The silicon-rich, oxygen-lean top nitride layer increases a difference between programming and erase voltages when the structure is employed in memory devices, thereby improving device speed, increasing data retention, and extending the operating life of the device.

Sandisk Technologies, Inc. - Ex. 1002, Page 000727

[0028] However, this structure also has drawbacks in terms of charge retention. Therefore, a middle oxide layer may be formed between the two nitride layers, forming a split charge trapping region comprising two nitride layers separated by a relatively thin oxide layer. In one embodiment, the two nitride layers are approximately equal thicknesses. Each nitride layer may be at least 30Å. The middle oxide layer may be at least 5A. Some tolerance for process variations is also envisioned, for example ±2Å. In general, the middle oxide layer will be thin relative to the two nitride layers, where 'thin relative to' means at least a ratio of about .75:1. One nitride layer (the bottom layer) may be closer to a substrate, and oxygen-rich relative to the other (upper) nitride layer.

[0029] One process for manufacturing such a semiconductor device includes forming a first oxide layer on a silicon substrate; forming a first nitride layer on the first oxide layer; applying radical oxidation to the first nitride layer to form a second oxide layer; and forming a second nitride layer on the second oxide layer. The first nitride layer is made oxygen-rich relative to the second nitride layer by varying the process parameters. For example, each nitride layer may be formed using a low pressure CVD process using a silicon source, a nitrogen source, and an oxygen-containing gas. With appropriate process parameters, a bottom oxynitride layer may be formed that is a silicon-rich and oxygen-rich, and a top nitride layer is may be formed that is silicon-rich, nitrogen-rich, and oxygen-lean. In one embodiment the first (lower) nitride layer is formed to a thickness of between 35Å and 50Å, oxidized to a depth of between 5Å and 20Å to form the middle oxide layer, and then the second nitride layer is formed over the middle oxide layer to a thickness of between 30Å and 60Å. The first (tunnel) oxide layer

Sandisk Technologies, Inc. - Ex. 1002, Page 000728

on the silicon substrate may be formed to a thickness of about 15-20Å. Again, some tolerance for process variations are envisioned, for example ±2Å.

[0030] A third oxide layer may be formed over the second nitride layer, to a thickness of about 40- 50Å, and a polysilicon or metal gate layer may be formed over the third oxide layer.

Multi-Layer Charge Storing Structure

[0031] FIG. 6 is a block diagram illustrating a cross-sectional side view of a portion of a semiconductor memory device 800. The memory device 800 includes a SONNOS gate stack 802 including an ONNO structure 804 formed over a surface 106 of silicon layer on a substrate 108. The device 800 further includes one or more diffusion regions 110, such as source and drain regions, aligned to the gate stack 802 and separated by a channel region 112. Generally, the SONNOS structure 802 includes a gate layer 114 formed upon and in contact with the ONNO structure 804. The gate 114 is isolated from the substrate 108 by the ONNO structure 804. The ONNO structure 804 includes a thin, lower oxide layer or tunneling oxide layer 116 that isolates the gate stack 802 from the channel region 112, a top or blocking oxide layer 120, and a multi-layer charge storing layer 804 including multiple nitride containing layers. Preferably, the multi-layer charge storing layer 804 includes at least two nitride layers, including a top nitride layer 818 and a bottom nitride layer 819.

[0032] FIG. 7-9 illustrate charge retention and migration in a SONNOS structure such as the one illustrated in FIG. 6. Charge traps are distributed through the nitride

Sandisk Technologies, Inc. - Ex. 1002, Page 000729

layers 818, 819, with a distribution that is uniform under ideal stoichiometric conditions (FIG. 7). As a result of an ERASE (FIG. 8), holes migrate toward the blocking oxide 120. Electron charge accumulates at the boundaries of the upper nitride layer 818 after programming (FIG. 9), and there is less accumulation of charge at the lower boundary of the lower nitride layer 819. This may result in lower leakage current. Nonetheless, this charge distribution may lead to charge leakage due to tunneling at the nitride boundaries, as shown for example in FIG. 10, which illustrates how charge may transition among different trapped states (e.g. E_{TA}, E_{TD}) to cause leakage after programming.

Oxide Split Multi-Layer Charge Storing Structure

[0033] FIG. 11 is a block diagram illustrating a cross-sectional side view of a semiconductor memory device 1500. The memory device 1500 includes a SONONOS stack 1502 including an ONONO structure 1504 formed over a surface 106 of a substrate 108. Substrate 108 includes one or more diffusion regions 110, such as source and drain regions, aligned to the gate stack 1502 and separated by a channel region 112. Generally, the SONONOS structure 1502 includes a polysilicon or metal gate layer 114 formed upon and in contact with the ONONO structure 1504. The gate 114 is separated or electrically isolated from the substrate 108 by the ONONO structure 1504. The ONONO structure 1504 includes a thin, lower oxide layer or tunneling oxide layer 116 that separates or electrically isolates the stack 1502 from the channel region 112, a top or blocking oxide layer 120, and a multi-layer charge storing layer 1504 including multiple nitride containing layers 1518, 1519. Preferably, the multi-layer charge storing layer 1504

Sandisk Technologies, Inc. - Ex. 1002, Page 000730

includes at least two nitride layers, including a top nitride layer 1518, a bottom oxynitride layer 1519, and an intermediate oxide layer 1521.

[0034] The various layers of the device 1500 may be fabricated to certain thicknesses. Different possibilities for the thicknesses are described herein, representing possible different embodiments. In general, the middle oxide layer will be relatively thin in comparison to the two nitride layers. For example, the middle oxide may be between approximately 5Å and 20Å. The nitride layers may be the same or different thicknesses as one another, but will typically be at least approximately 30Å. With advances in process technology and material science, nitride thicknesses as low as 20Å may be possible in the near future.

[0035] FIG. 12-14 illustrate charge retention and migration in a SONONOS structure such as the one illustrated in FIG. 11. Charge traps are distributed in the two nitride layers 1518, 1519, with a discontinuity where the intermediate oxide layer 1521 resides (few or no traps form in the oxide layer 1521). The majority of traps form in the top nitride layer 1518. Within each nitride layer, trap distribution is more or less uniform under ideal stoichiometric conditions (FIG. 12). As a result of an ERASE (FIG. 13), holes migrate toward the blocking oxide 120, but the majority of trapped hole charges form in the top nitride layer 1518. Electron charge accumulates at the boundaries of the upper nitride layer 1518 after programming (FIG. 14), and there is less accumulation of charge at the lower boundary of the lower nitride layer 1519. Furthermore, due to the intermediate oxide 1521, the probability of tunneling by trapped electron charges in the upper nitride layer 1518 is substantially reduced. This may result in lower leakage current than for the structures illustrated in FIG. 1 and FIG. 6. This charge distribution

Sandisk Technologies, Inc. - Ex. 1002, Page 000731

significantly lowers the probability of tunneling from the upper nitride layer, as shown for example in the energy band diagrams FIG. 15, which illustrate the obstacles to tunneling that charges encounter as they transition among different trapped states (e.g. E_{TA}, E_{TD}) after programming.

Fabrication Techniques

[0036] A process of forming a SONOS structure with superior charge retention begins with forming a first oxide layer, such as a tunneling oxide layer, of the ONO structure over a substrate. The substrate may be, for example, polysilicon, or a silicon surfaced germanium substrate. Next, the first nitride layer of a multi-layer charge storing structure is formed on the first oxide layer. This first or bottom nitride layer may be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The first nitride layer is then oxidized to a chosen depth using radical oxidation. This forms the middle oxide layer. Radical oxidation may be performed, for example, at a temperature of 1000-1100°C using a single wafer tool, or 800-900°C using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0037] The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The second nitride layer has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the first (lower)

Sandisk Technologies, Inc. - Ex. 1002, Page 000732

nitride layer. The second nitride layer may be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer. Finally, a second oxide layer of the ONO structure is formed on a surface of the second nitrided layer. This top or blocking oxide layer may be formed or deposited by any suitable means. In one embodiment the top oxide is a high temperature oxide deposited in a HTO CVD process. Alternatively, the top or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the top nitride thickness may be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer. A third option is to oxidize the top nitride layer to a chosen depth using radical oxidation.

[0038] In some embodiments, it may be possible perform fabrication by forming the tunnel oxide layer in one chamber of a CVD tool, then form the bottom oxynitride layer in a second chamber of the CVD tool, then radical oxidize the lower oxynitride layer in the first chamber, then deposit more nitride in the second chamber, then radical oxidize the second nitride layer in the first chamber again, thus forming the semiconductor device using a two-chamber process.

[0039] Fabrication may further involve forming or depositing a silicon containing layer on a surface of the second oxide layer to complete a SONOS stack. The silicon containing layer may, for example, be a polysilicon layer deposited by a CVD process to form a control gate of a SONOS transistor or device. In some embodiments metal may be deposited instead of polysilicon.

Sandisk Technologies, Inc. - Ex. 1002, Page 000733

[0040] Generally, the substrate 108 may include any known silicon-based semiconductor material including silicon, silicon-germanium, silicon-on-insulator, or silicon-on-sapphire substrate. Alternatively, the substrate 108 may include a silicon layer formed on a non-silicon-based semiconductor material, such as gallium-arsenide, germanium, gallium-nitride, or aluminum phosphide. Preferably, the substrate 108 is a doped or undoped silicon substrate.

[0041] The lower oxide layer or tunneling oxide layer 116 generally includes a relatively thin layer of silicon dioxide (SiO_2) of from about 15Å to about 22Å, and more preferably about 18-20Å, with some process variation (e.g. ±1Å). The tunneling oxide layer 116 may be formed or deposited by any suitable means including, for example, being thermally grown or deposited using chemical vapor deposition (CVD). In one embodiment, the tunnel oxide layer is formed or grown using a steam anneal. This involves a wet-oxidizing process in which the substrate 108 is placed in a in a deposition or processing chamber, heated to a temperature from about 700°C to about 850°C, and exposed to a wet vapor for a predetermined period of time selected based on a desired thickness of the finished tunneling oxide layer 116. Exemplary process times are from about 5 to about 20 minutes. The oxidation may be performed at atmospheric or at low pressure, or using a dry process under ambient conditions using either batch or single wafer tools.

[0042] The multi-layer charge storing structure generally includes at least two nitride layers having differing compositions of silicon, oxygen and nitrogen, and a middle oxide layer between the two nitride layers. In a preferred embodiment the nitride layers are formed or deposited in a low pressure CVD process using a silicon source, such as

Sandisk Technologies, Inc. - Ex. 1002, Page 000734

silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane (SiH_2Cl_2), tetrachlorosilane ($SiC1_4$) or Bis-TertiaryButylAmino Silane (BTBAS), a nitrogen source, such as nitrogen (N2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas, such as oxygen (0_2) or N_2O. Alternatively, gases in which hydrogen has been replaced by deuterium can be used, including, for example, the substitution of deuterated-ammonia (ND_3) for NH_3. The substitution of deuterium for hydrogen advantageously passivates Si dangling bonds at the silicon-oxide interface, thereby increasing the endurance of the devices.

[0043] For example, the lower or bottom oxynitride layer 819, 1519 may be deposited over the tunneling oxide layer 116 by placing the substrate 108 in a deposition chamber and introducing a process gas including N_2O, NH3 and DCS, while maintaining the chamber at a pressure of from about 5 millitorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700°C to about 850°C, and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes. The process gas may include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and may be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm). A layer produced or deposited under these condition yields a silicon-rich, oxygen-rich, bottom oxynitride layer 819, that decrease the charge loss rate after programming and after erase, which may be manifested in a small voltage shift in the retention mode.

[0044] The top nitride layer 818, 1518 may be deposited in a CVD process using a process gas including N_2O, NH3 and DCS, at a chamber pressure of from about 5 mT

Sandisk Technologies, Inc. - Ex. 1002, Page 000735

to about 500 mT, and at a substrate temperature of from about 700°C to about 850°C, and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes. The process gas may include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and may be introduced at a flow rate of from about 5 to about 20 sccm. A layer produced or deposited under these condition yields a silicon-rich, nitrogen-rich, and oxygen-lean top nitride layer 818, 1518.

[0045] Preferably, the top nitride layer 818, 1518 is deposited sequentially, after formation of the middle oxide layer, in the same process chamber used to form the bottom oxynitride layer 819, 1519, without altering the temperature to which the substrate 108 was heated during deposition of the bottom oxynitride layer 819, 1519. In one embodiment, the top nitride layer 818, 1518 is deposited sequentially following the deposition of the bottom oxynitride layer 819, 1519 by (1) moving to a different process chamber to form the middle oxide layer by radical oxidation of the bottom oxynitride layer, (2) returning to the process chamber used to form the bottom oxynitride layer and decreasing the flow rate of the N_2O/NH_3 gas mixture relative to the DCS/NH_3 gas mixture to provide the desired ratio of the gas mixtures to yield the silicon-rich, nitrogen-rich, and oxygen-lean top nitride layer 818, 1518.

[0046] A suitable thickness for the bottom oxynitride layer 819, 1519 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the middle oxide layer. A suitable thickness for the top nitride layer 818, 1518 may be at least 30Å. In certain embodiments, the upper nitride layer may be formed up to 130Å thick, of which

Sandisk Technologies, Inc. - Ex. 1002, Page 000736

30-70Å may be consumed by radical oxidation to form the top oxide layer. A ratio of thicknesses between the bottom oxynitride layer and the top nitride layer is approximately 1:1 in some embodiments, although other ratios are also possible.

[0047] The top oxide layer 120 includes a relatively thick layer of SiO_2 of from about 30Å to about 70Å, and more preferably about 40-50Å. The top oxide layer 120 may be formed or deposited by any suitable means including, for example, being thermally grown or deposited using CVD. In one embodiment, the top oxide layer 120 is a high-temperature-oxide (HTO) deposited using CVD process. This deposition process involves exposing the substrate 108 to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-containing gas, such as O_2 or N_2O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

[0048] The top oxide layer 120 may be formed by oxidizing the top nitride layer 818, 1518. This may be accomplished in the same chamber used to form the nitride layers 116, 818, 819. The nitride layers 818, 819, 1518, 1519 may be formed in a first chamber, and the oxide layers 116, 1521, 120 may formed in a second chamber, of a two-chamber tool. Suitable tools include, for example, an ONO AVP, commercially available from AVIZA technology of Scotts Valley, Calif.

[0049] Although shown and described above as having two nitride layers, i.e., a top and a bottom layer, the present invention is not so limited, and the multi-layer charge storing structure may include a number, n, of nitride layers, any or all of which may have differing stoichiometric compositions of oxygen, nitrogen and/or silicon. In particular,

Sandisk Technologies, Inc. - Ex. 1002, Page 000737

multi-layer charge storing structures having up to five, and possibly more, nitride layers each with differing stoichiometric compositions are contemplated. At least some of these layers will be separated from the others by one or more relatively thin oxide layers. However, as will be appreciated by those skilled in the art it is generally desirable to utilize as few layers as possible to accomplish a desired result, reducing the process steps necessary to produce the device, and thereby providing a simpler and more robust manufacturing process. Moreover, utilizing as few layers as possible also results in higher yields as it is simpler to control the stoichiometric composition and dimensions of the fewer layers.

[0050] It will further be appreciated that although applicable as part of a SONOS stack in a SONOS memory device, the structure and method of the present invention is not so limited, and the ONO structure can be used in or with any semiconductor technology or in any device requiring a charge storing or dielectric layer or stack including, for example, in a split gate flash memory, a TaNOS stack, in a 1 T (transistor) SONOS cell, a 2T SONOS cell, a 3T SONOS cell, a localized 2-bit cell, and in a multilevel programming or cell, without departing from the scope of the invention.

[0051] Advantages of ONO structures and methods of forming the same according to an embodiment of the present invention over previous or conventional approaches include: (i) the ability to enhance data retention in memory devices using the structure by dividing the nitride layer into a plurality of films or layers and tailoring the oxygen, nitrogen and silicon profile across each layer, with an intermediate oxide layer to reduce the probability of charge tunneling; (ii) the ability to enhance speed of a memory device without compromising data retention; (iii) the ability to meet or exceed data

Sandisk Technologies, Inc. - Ex. 1002, Page 000738

retention and speed specifications for memory devices using an ONO structure of an embodiment of the present invention at a temperature of at least about 125°C; and (iv) provide heavy duty program erase cycles of 100,000 cycles or more.

Implementations and Alternatives

[0052] In another aspect the present disclosure is directed to multigate or multigate-surface memory devices including charge-trapping regions overlying two or more sides of a channel formed on or above a surface of a substrate, and methods of fabricating the same. Multigate devices include both planar and non-planar devices. A planar multigate device (not shown) generally includes a double-gate planar device in which a number of first layers are deposited to form a first gate below a subsequently formed channel, and a number of second layers are deposited thereover to form a second gate. A non-planar multigate device generally includes a horizontal or vertical channel formed on or above a surface of a substrate and surrounded on three or more sides by a gate.

[0053] FIG. 16A illustrates one embodiment of a non-planar multigate memory device including a charge-trapping region. Referring to FIG. 16A, the memory device 1600, commonly referred to as a finFET, includes a channel 1602 formed from a thin film or layer of semiconducting material overlying a surface 1604 on a substrate 1606 connecting a source 1608 and a drain 1610 of the memory device. The channel 1602 is enclosed on three sides by a fin which forms a gate 1612 of the device. The thickness of the gate 1612 (measured in the direction from source to drain) determines the effective channel length of the device.

Sandisk Technologies, Inc. - Ex. 1002, Page 000739

[0054] In accordance with the present disclosure, the non-planar multigate memory device 1600 of FIG. 16A can include a split charge-trapping region. FIG. 16B is a cross-sectional view of a portion of the non-planar memory device of FIG. 16A including a portion of the substrate 1606, channel 1602 and the gate 1612 illustrating a split charge-trapping region 1614. The gate 1612 further includes a tunnel oxide 1616 overlying a raised channel 1602, a blocking dielectric 1618 and a metal gate layer 1620 overlying the blocking layer to form a control gate of the memory device 1600. In some embodiments a doped polysilicon may be deposited instead of metal to provide a polysilicon gate layer. The channel 1602 and gate 1612 can be formed directly on substrate 1606 or on an insulating or dielectric layer 1622, such as a buried oxide layer, formed on or over the substrate.

[0055] Referring to FIG. 16B, the split charge-trapping region 1614 includes at least one lower or bottom charge-trapping layer 1624 comprising nitride closer to the tunnel oxide 1616, and an upper or top charge-trapping layer 1626 overlying the bottom charge-trapping layer. Generally, the top charge-trapping layer 1626 comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in multiple charge-trapping layers, while the bottom charge-trapping layer 1624 comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the top charge-trapping layer to reduce the number of charge traps therein. By oxygen-rich it is meant wherein a concentration of oxygen in the bottom charge-trapping layer 1624 is from about 15 to about 40%, whereas a concentration of oxygen in top charge-trapping layer 1626 is less than about 5%.

Sandisk Technologies, Inc. - Ex. 1002, Page 000740

[0056] In one embodiment, the blocking dielectric 1618 also comprises an oxide, such as an HTO, to provide an ONNO structure. The channel 1602 and the overlying ONNO structure can be formed directly on a silicon substrate 1606 and overlaid with a doped polysilicon gate layer 1620 to provide a SONNOS structure.

[0057] In some embodiments, such as that shown in FIG. 16B, the split charge-trapping region 1614 further includes at least one thin, intermediate or anti-tunneling layer 1628 comprising a dielectric, such as an oxide, separating the top charge-trapping layer 1626 from the bottom charge-trapping layer 1624. The anti-tunneling layer 1628 substantially reduces the probability of electron charge that accumulates at the boundaries of the upper nitride layer 1626 during programming from tunneling into the bottom nitride layer 1624, resulting in lower leakage current than for the structures illustrated in FIG. 1 and FIG. 6.

[0058] As with the embodiments described above, either or both of the bottom charge-trapping layer 1624 and the top charge-trapping layer 1626 can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The top charge-trapping layer 1626 has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the bottom charge-trapping layer 1624, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

Sandisk Technologies, Inc. - Ex. 1002, Page 000741

[0059] In those embodiments including an intermediate or anti-tunneling layer 1628 comprising oxide, the anti-tunneling layer can be formed by oxidation of the bottom oxynitride layer, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100°C using a single wafer tool, or 800-900°C using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0060] Finally, in those embodiments including a blocking dielectric 1618 comprising oxide the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of the blocking dielectric 1618 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric 1618 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the top nitride thickness may be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer. A third option is to oxidize the top nitride layer to a chosen depth using radical oxidation.

[0061] A suitable thickness for the bottom charge-trapping layer 1624 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 1628. A suitable thickness for the top charge-trapping layer 1626 may be at least 30Å. In certain embodiments, the top charge-trapping layer 1626 may be formed up to 130Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric 1618. A ratio of thicknesses between the bottom charge-trapping layer 1624

Sandisk Technologies, Inc. - Ex. 1002, Page 000742

and top charge-trapping layer 1626 is approximately 1:1 in some embodiments, although other ratios are also possible.

[0062] In other embodiments, either or both of the top charge-trapping layer 1626 and the blocking dielectric 1618 may comprise a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0063] In another embodiment, shown in FIGs. 17A and 17B, the memory device can include a nanowire channel formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device. By nanowire channel it is meant a conducting channel formed in a thin strip of crystalline silicon material, having a maximum cross-sectional dimension of about 10 nanometers (nm) or less, and more preferably less than about 6 nm. Optionally, the channel can be formed to have <100> surface crystalline orientation relative to a long axis of the channel.

[0064] Referring to FIG. 17A, the memory device 1700 includes a horizontal nanowire channel 1702 formed from a thin film or layer of semiconducting material on or overlying a surface on a substrate 1706, and connecting a source 1708 and a drain 1710 of the memory device. In the embodiment shown, the device has a gate-all-around (GAA) structure in which the nanowire channel 1702 is enclosed on all sides by a gate 1712 of the device. The thickness of the gate 1712 (measured in the direction from source to drain) determines the effective channel length of the device.

[0065] In accordance with the present disclosure, the non-planar multigate memory device 1700 of FIG. 17A can include a split charge-trapping region. FIG. 17B is

Sandisk Technologies, Inc. - Ex. 1002, Page 000743

a cross-sectional view of a portion of the non-planar memory device of FIG. 17A including a portion of the substrate 1706, nanowire channel 1702 and the gate 1712 illustrating a split charge-trapping region. Referring to FIG. 17B, the gate 1712 includes a tunnel oxide 1714 overlying the nanowire channel 1702, a split charge-trapping region, a blocking dielectric 1716 and a gate layer 1718 overlying the blocking layer to form a control gate of the memory device 1700. The gate layer 1718 can comprise a metal or a doped polysilicon. The split charge-trapping region includes at least one inner charge-trapping layer 1720 comprising nitride closer to the tunnel oxide 1714, and an outer charge-trapping layer 1722 overlying the inner charge-trapping layer. Generally, the outer charge-trapping layer 1722 comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in multiple charge-trapping layers, while the inner charge-trapping layer 1720 comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the outer charge-trapping layer to reduce the number of charge traps therein.

[0066] In some embodiments, such as that shown, the split charge-trapping region further includes at least one thin, intermediate or anti-tunneling layer 1724 comprising a dielectric, such as an oxide, separating outer charge-trapping layer 1722 from the inner charge-trapping layer 1720. The anti-tunneling layer 1724 substantially reduces the probability of electron charge that accumulates at the boundaries of outer charge-trapping layer 1722 during programming from tunneling into the inner charge-trapping layer 1720, resulting in lower leakage current.

[0067] As with the embodiment described above, either or both of the inner charge-trapping layer 1720 and the outer charge-trapping layer 1722 can comprise silicon

Sandisk Technologies, Inc. - Ex. 1002, Page 000744

nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The outer charge-trapping layer 1722 has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the inner charge-trapping layer 1720, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

[0068] In those embodiments including an intermediate or anti-tunneling layer 1724 comprising oxide, the anti-tunneling layer can be formed by oxidation of the inner charge-trapping layer 1720, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100°C using a single wafer tool, or 800-900°C using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0069] Finally, in those embodiments in which the blocking dielectric 1716 comprises oxide, the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of blocking dielectric 1716 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric 1716 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the thickness of the outer charge-trapping layer 1722 may need to be adjusted or increased as

Sandisk Technologies, Inc. - Ex. 1002, Page 000745

some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer.

[0070] A suitable thickness for the inner charge-trapping layer 1720 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 1724. A suitable thickness for the outer charge-trapping layer 1722 may be at least 30Å. In certain embodiments, the outer charge-trapping layer 1722 may be formed up to 130Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric 1716. A ratio of thicknesses between the inner charge-trapping layer 1720 and the outer charge-trapping layer 1722 is approximately 1:1 in some embodiments, although other ratios are also possible.

[0071] In other embodiments, either or both of the outer charge-trapping layer 1722 and the blocking dielectric 1716 may comprise a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0072] In another embodiment, the memory device is or includes a non-planar device comprising a vertical nanowire channel formed in or from a semiconducting material projecting above or from a number of conducting, semiconducting layers on a substrate. In one version of this embodiment, shown in cut-away in FIG. 18A, the memory device 1800 comprises a vertical nanowire channel 1802 formed in a cylinder of semiconducting material connecting a source 1804 and drain 1806 of the device. The channel 1802 is surrounded by a tunnel oxide 1808, a charge-trapping region 1810, a blocking layer 1812 and a gate layer 1814 overlying the blocking layer to form a control

Sandisk Technologies, Inc. - Ex. 1002, Page 000746

gate of the memory device 1800. The channel 1802 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or can include an annular layer formed over a cylinder of dielectric filler material. As with the horizontal nanowires described above, the channel 1802 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel. Optionally, where the channel 1802 includes a crystalline silicon, the channel can be formed to have <100> surface crystalline orientation relative to a long axis of the channel.

[0073] In some embodiments, such as that shown in FIG. 18B, the charge-trapping region 1810 can be a split charge-trapping region including at least a first or inner charge trapping layer 1816 closest to the tunnel oxide 1808, and a second or outer charge trapping layer 1818. Optionally, the first and second charge trapping layers can be separated by an intermediate oxide or anti-tunneling layer 1820.

[0074] As with the embodiments described above, either or both of the first charge trapping layer 1816 and the second charge trapping layer 1818 can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer.

[0075] Finally, either or both of the second charge trapping layer 1818 and the blocking layer 1812 may comprise a high K dielectric, such as HfSiON, HfSiO, HfO, ZrSiON, ZrSiO, ZrO, or Y_2O_3.

[0076] A suitable thickness for the first charge trapping layer 1816 may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer

Sandisk Technologies, Inc. - Ex. 1002, Page 000747

1820. A suitable thickness for the second charge trapping layer 1818 may be at least 30Å, and a suitable thickness for the blocking dielectric 1812 may be from about 30-70Å.

[0077] The memory device 1800 of FIG. 18A can be made using either a gate first or a gate last scheme. FIG. 19A-F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 18A. FIG. 20A-F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 18A.

[0078] Referring to FIG. 19A, in a gate first scheme a first or lower dielectric layer 1902, such as a blocking oxide, is formed over a first, doped diffusion region 1904, such as a source or a drain, in a substrate 1906. A gate layer 1908 is deposited over the first dielectric layer 1902 to form a control gate of the device, and a second or upper dielectric layer 1910 formed thereover. As with embodiments described above, the first and second dielectric layers 1902, 1910, can be deposited by CVD, radical oxidation or be formed by oxidation of a portion of the underlying layer or substrate. The gate layer 1908 can comprise a metal deposited or a doped polysilicon deposited by CVD. Generally the thickness of the gate layer 1908 is from about 40- 50Å, and the first and second dielectric layers 1902, 1910, from about 20- 80Å.

[0079] Referring to FIG. 19B, a first opening 1912 is etched through the overlying gate layer 1908, and the first and second dielectric layers 1902, 1910, to the diffusion region 1904 in the substrate 1906. Next, layers of a tunneling oxide 1914, charge-trapping region 1916, and blocking dielectric 1918 are sequentially deposited in the opening and the surface of the upper dielectric layer 1910 planarize to yield the intermediate structure shown in FIG. 19C.

Sandisk Technologies, Inc. - Ex. 1002, Page 000748

[0080] Although not shown, it will be understood that as in the embodiments described above the charge-trapping region 1916 can include a split charge-trapping region comprising at least one lower or bottom charge-trapping layer closer to the tunnel oxide 1914, and an upper or top charge-trapping layer overlying the bottom charge-trapping layer. Generally, the top charge-trapping layer comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in multiple charge-trapping layers, while the bottom charge-trapping layer comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the top charge-trapping layer to reduce the number of charge traps therein. In some embodiments, the split charge-trapping region 1916 further includes at least one thin, intermediate or anti-tunneling layer comprising a dielectric, such as an oxide, separating the top charge-trapping layer from the bottom charge-trapping layer.

[0081] Next, a second or channel opening 1920 is anisotropically etched through tunneling oxide 1914, charge-trapping region 1916, and blocking dielectric 1918, FIG. 19D. Referring to FIG. 19E, a semiconducting material 1922 is deposited in the channel opening to form a vertical channel 1924 therein. The vertical channel 1924 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or, as shown in FIG. 19E, can include a separate, layer semiconducting material 1922 surrounding a cylinder of dielectric filler material 1926.

[0082] Referring to FIG. 19F, the surface of the upper dielectric layer 1910 is planarized and a layer of semiconducting material 1928 including a second, doped diffusion region 1930, such as a source or a drain, formed therein deposited over the upper dielectric layer to form the device shown.

Sandisk Technologies, Inc. - Ex. 1002, Page 000749

[0083] Referring to FIG. 20, in a gate last scheme a dielectric layer 2002, such as an oxide, is formed over a sacrificial layer 2004 on a surface on a substrate 2006, an opening etched through the dielectric and sacrificial layers and a vertical channel 2008 formed therein. As with embodiments described above, the vertical channel 2008 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material 2010, such as a polycrystalline or monocrystalline silicon, or can include a separate, layer semiconducting material surrounding a cylinder of dielectric filler material (not shown). The dielectric layer 2002 can comprise any suitable dielectric material, such as a silicon oxide, capable of electrically isolating the subsequently formed gate layer of the memory device 1800 from an overlying electrically active layer or another memory device. The sacrificial layer 2004 can comprise any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 2002, substrate 2006 and vertical channel 2008.

[0084] Referring to FIG. 20B, a second opening 2012 is etched through the etched through the dielectric and sacrificial layers 2002, 2004, to the substrate 1906, and the sacrificial layer 2004 etched or removed. The sacrificial layer 2004 can comprise any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 2002, substrate 2006 and vertical channel 2008. In one embodiment the sacrificial layer 2004 comprises silicon dioxide that can be removed by buffered oxide etch (BOE etch).

[0085] Referring to FIGs. 20C and 20D, layers of a tunneling oxide 2014, charge-trapping region 2016, and blocking dielectric 2018 are sequentially deposited in the opening and the surface of the dielectric layer 2002 planarize to yield the intermediate

Sandisk Technologies, Inc. - Ex. 1002, Page 000750

structure shown in FIGs. 20C and 20D. In some embodiments, such as that shown in FIG. 20D, the charge-trapping region 2016 can be a split charge-trapping region including at least a first or inner charge trapping layer 2016a closest to the tunnel oxide 2014, and a second or outer charge trapping layer 2016b. Optionally, the first and second charge trapping layers can be separated by an intermediate oxide or anti-tunneling layer 2020.

[0086] Next, a gate layer 2022 is deposited into the second opening 2012 and the surface of the upper dielectric layer 2002 planarized to yield the intermediate structure illustrated in FIG. 20E. As with embodiments described above, the gate layer 2022 can comprise a metal deposited or a doped polysilicon. Finally, an opening 2024 is etched through the gate layer 2022 to form control gate of separate memory devices 2026.

[0087] "Logic" refers to signals and/or information that may be applied to influence the operation of a device. Software, hardware, and firmware are examples of logic. Hardware logic may be embodied in circuits. In general, logic may comprise combinations of software, hardware, and/or firmware.

[0088] Embodiments of the charge retention devices described herein may be employed in logic circuits to function as machine-memory. Those having skill in the art will appreciate that there are various logic implementations that may embody the described structures, and that the preferred vehicle will vary with the context in which the processes are deployed. For example, if an implementer determines that speed and accuracy are paramount, the implementer may opt for a hardware and/or firmware vehicle; alternatively, if flexibility is paramount, the implementer may opt for a solely software implementation; or, yet again alternatively, the implementer may opt for some combination of hardware, software, and/or firmware. Hence, there are many vehicles that

Sandisk Technologies, Inc. - Ex. 1002, Page 000751

may employ the devices described herein, none of which is inherently superior to the other in that any vehicle to be utilized is a choice dependent upon the context in which the vehicle will be deployed and the specific concerns (e.g., speed, flexibility, or predictability) of the implementer, any of which may vary. Those skilled in the art will recognize that optical aspects of implementations may involve optically-oriented hardware, software, and or firmware.

[0089] The foregoing detailed description has set forth various embodiments of the devices and/or processes via the use of block diagrams, flowcharts, and/or examples. Insofar as such block diagrams, flowcharts, and/or examples contain one or more functions and/or operations, it will be understood as notorious by those within the art that each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof

[0090] Embodiments of the structures described herein may be employed in Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), central processing units (CPUs), digital signal processors (DSPs), or other integrated formats. However, those skilled in the art will recognize that some aspects of the embodiments disclosed herein, in whole or in part, can be equivalently implemented in dedicated memory circuits, for the purpose of storing digital information for data and/or programs running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more processors (e.g., as one or more programs running on one or more microprocessors), as firmware, or as virtually any combination thereof

Sandisk Technologies, Inc. - Ex. 1002, Page 000752

[0091] In a general sense, those skilled in the art will recognize that the various structures described herein may be embodied, individually and/or collectively, by a wide range of electrical circuitry. As used herein "electrical circuitry" includes, but is not limited to, electrical circuitry having at least one discrete electrical circuit, electrical circuitry having at least one integrated circuit, electrical circuitry having at least one application specific integrated circuit, electrical circuitry forming a general purpose computing device configured by a computer program (e.g., a general purpose computer configured by a computer program which at least partially carries out processes and/or devices described herein, or a microprocessor configured by a computer program which at least partially carries out processes and/or devices described herein), electrical circuitry forming a memory device (e.g., forms of random access memory), and/or electrical circuitry forming a communications device (e.g., a modem, communications switch, or optical-electrical equipment).

[0092] Those skilled in the art will recognize that it is common within the art to describe devices and/or processes in the fashion set forth herein, and thereafter use standard engineering practices to integrate such described devices and/or processes into larger systems. That is, at least a portion of the devices and/or processes described herein can be integrated into a network processing system without an undue amount of experimentation.

Sandisk Technologies, Inc. - Ex. 1002, Page 000753

IN THE CLAIMS

WHAT IS CLAIMED IS:

1. A memory device comprising:

a channel formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device;

a tunnel oxide overlying the channel;

a split charge-trapping region overlying the tunnel oxide, the split charge-trapping region including a bottom charge-trapping layer comprising a nitride closer to the tunnel oxide, and a top charge-trapping layer, wherein the bottom charge-trapping layer is separated from the top charge-trapping layer by a thin anti-tunneling layer comprising an oxide.

2. The memory device of claim 1, wherein the top charge-trapping layer comprises a silicon-rich, oxygen-lean nitride, the bottom charge-trapping layer comprises an oxygen-rich nitride, and further comprising a blocking dielectric layer overlying the split charge-trapping region.

3. The memory device of claim 2, wherein the top charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region.

4. The memory device of claim 2, wherein the blocking layer comprises a high K dielectric.

Sandisk Technologies, Inc. - Ex. 1002, Page 000754

5. The memory device of claim 2, wherein the channel is fabricated from silicon having <100> surface crystalline orientation relative to a long axis of the channel.

6. The memory device of claim 2, wherein the channel comprises polysilicon.

7. The memory device of claim 2, wherein the channel comprises recrystallized polysilicon.

8. The memory device of claim 2, wherein the channel comprises a silicon nanowire.

9. The memory device of claim 2, wherein the tunnel oxide comprises a nitrided oxide.

10. The memory device of claim 1, wherein the top charge-trapping layer comprises a high K dielectric.

11. The memory device of claim 1, wherein the channel projects above the surface on the substrate, and further comprising a fin intersecting and overlying at least a portion of the channel, the fin comprising the tunnel oxide and the split charge-trapping region overlying the tunnel oxide.

Sandisk Technologies, Inc. - Ex. 1002, Page 000755

12. The memory device of claim 11, wherein the top charge-trapping layer comprises a silicon-rich, oxygen-lean nitride, the bottom charge-trapping layer comprises an oxygen-rich nitride layer, and further comprising a blocking oxide layer overlying the split charge-trapping region.

13. The memory device of claim 12, further comprising a metal gate layer overlying the blocking oxide layer.

14. A memory device comprising:

a vertical channel formed from a thin projection of semiconducting material extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region;

a tunnel oxide abutting the vertical channel;

a split charge-trapping region abutting the tunnel oxide, the split charge-trapping region including a first charge-trapping layer comprising an oxygen-rich nitride closer to the tunnel oxide, and a second charge-trapping layer comprising a silicon-rich, oxygen-lean nitride overlying the first charge-trapping layer,

wherein the second charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region.

Sandisk Technologies, Inc. - Ex. 1002, Page 000756

15. The non-planar memory device of claim 14, wherein the first charge-trapping layer is separated from the second charge-trapping layer by a thin anti-tunneling layer comprising an oxide.

16. The non-planar memory device of claim 15, wherein the vertical channel comprises silicon.

17. The non-planar memory device of claim 15, further comprising a high K dielectric blocking layer abutting the split charge-trapping region

18. The non-planar memory device of claim 14, further comprising a high K dielectric blocking layer abutting the split charge-trapping region.

19. A process of manufacturing a semiconductor device, the process comprising:

forming a channel from a thin film of semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device;

forming a tunnel oxide overlying the channel;

forming a split charge-trapping region over the tunnel oxide including a bottom charge-trapping layer comprising an oxygen-rich nitride overlying the tunnel oxide, a thin anti-tunneling layer comprising an oxide overlying the tunnel oxide bottom charge-trapping layer, and a top charge-trapping layer comprising a silicon-rich, oxygen-lean nitride overlying the thin anti-tunneling layer,

Sandisk Technologies, Inc. - Ex. 1002, Page 000757

wherein the top charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region.

20. The process of claim 19, wherein forming the channel comprises forming from the thin film of semiconducting material overlying the surface on the substrate a channel connecting a source and a drain raised above the surface on the substrate.

Sandisk Technologies, Inc. - Ex. 1002, Page 000758

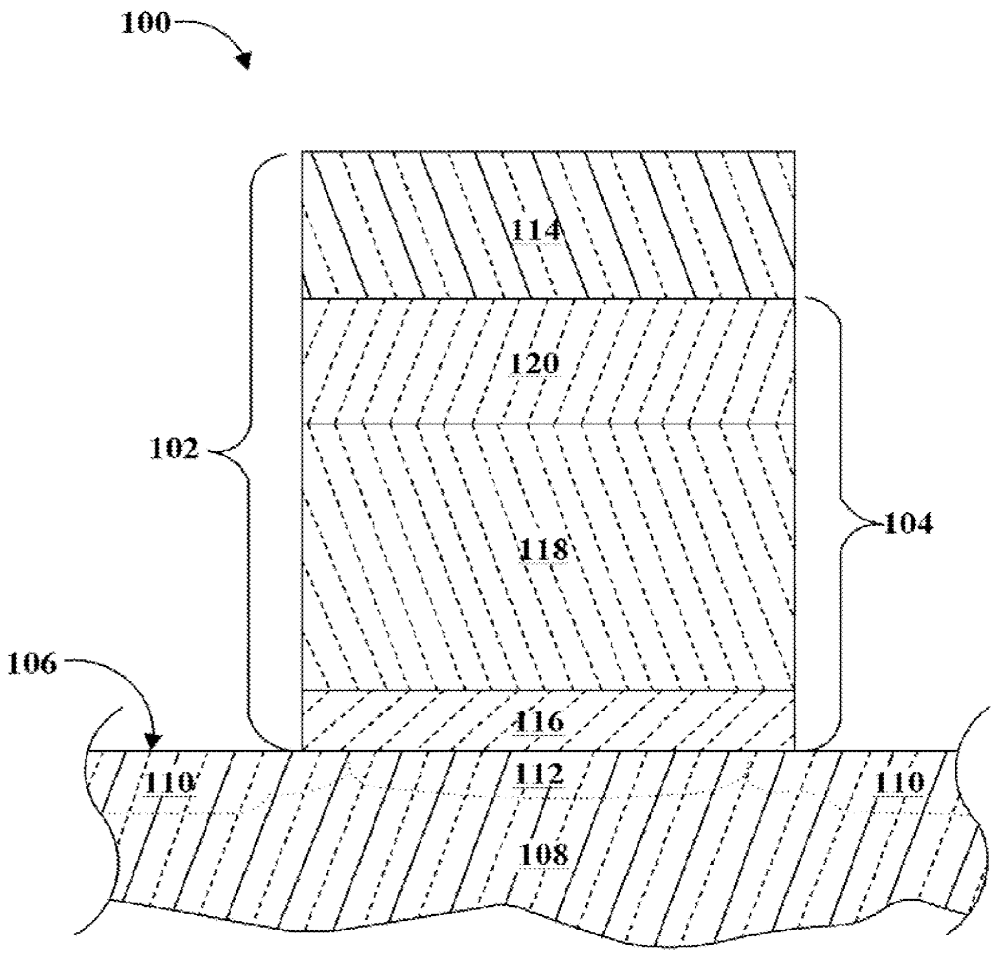


FIG. 1 (Prior Art)

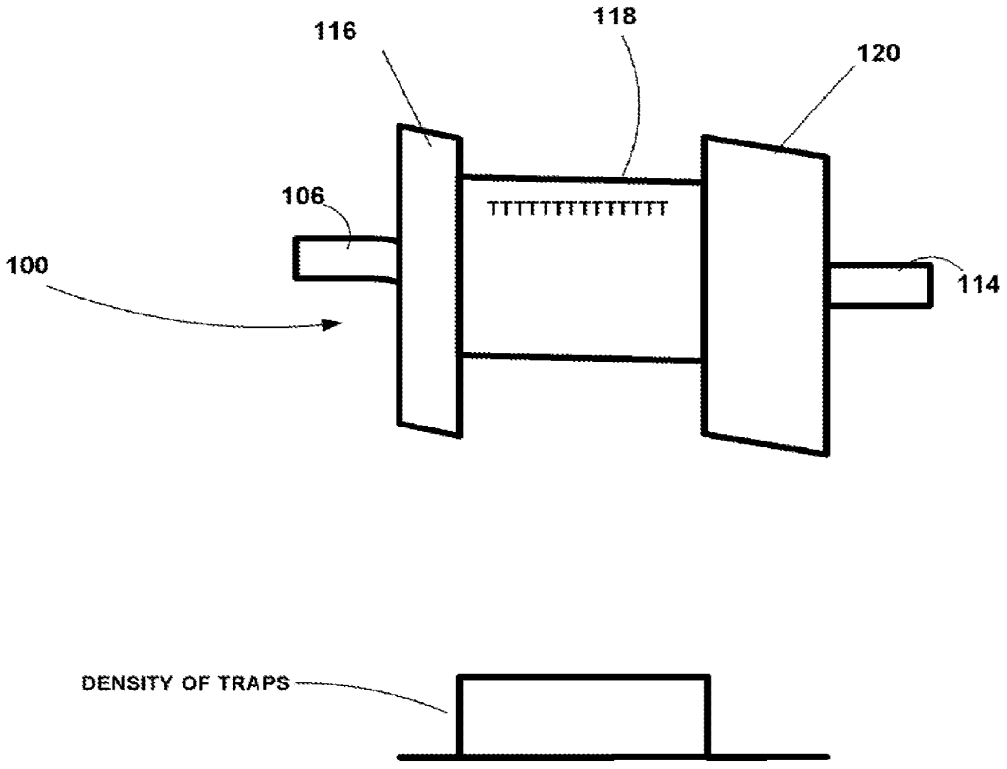


FIG. 2 (Prior Art)

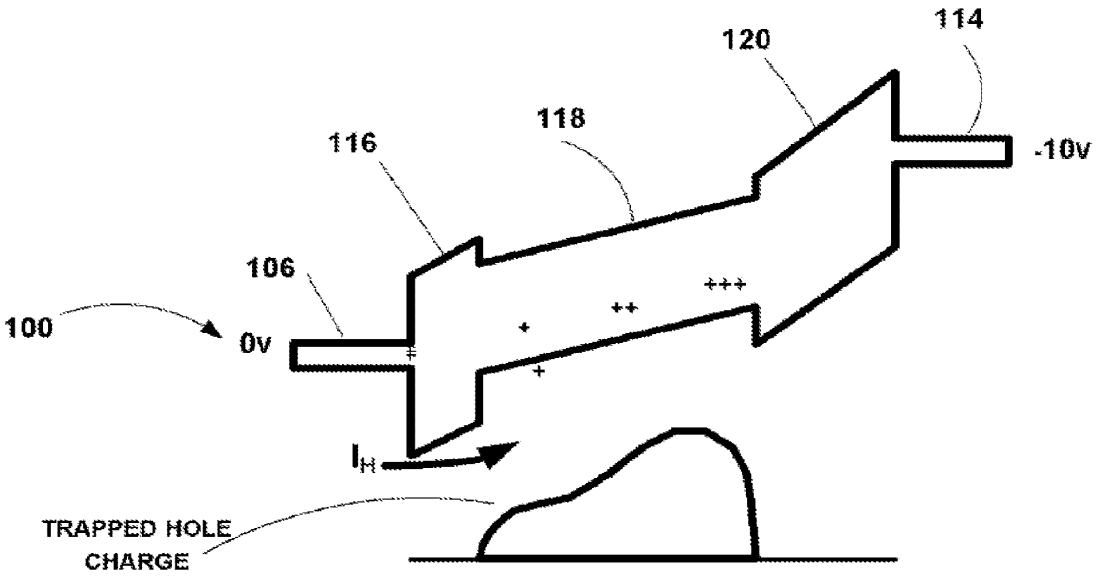


FIG. 3 (Prior Art)

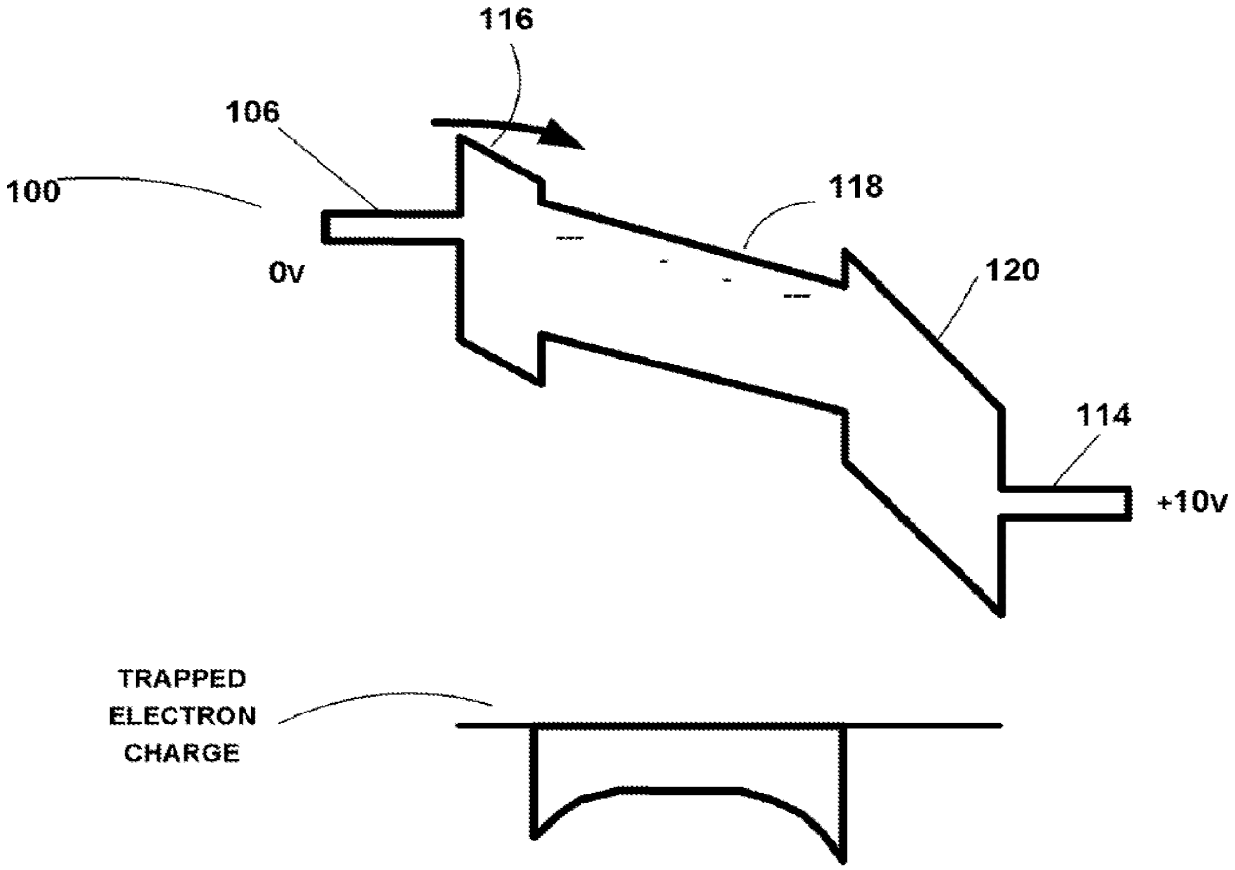


FIG. 4 (Prior Art)

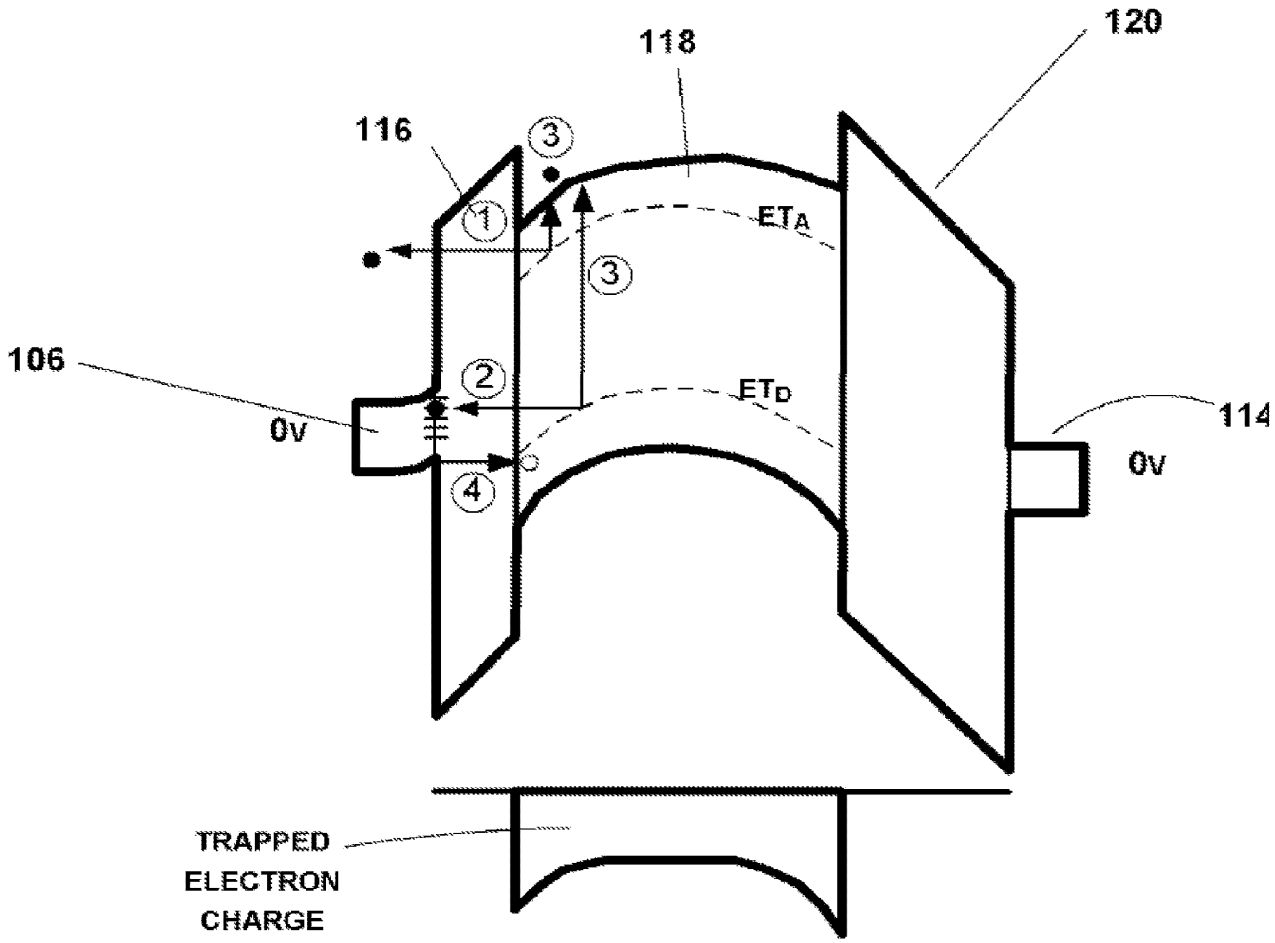


FIG. 5 (Prior Art)

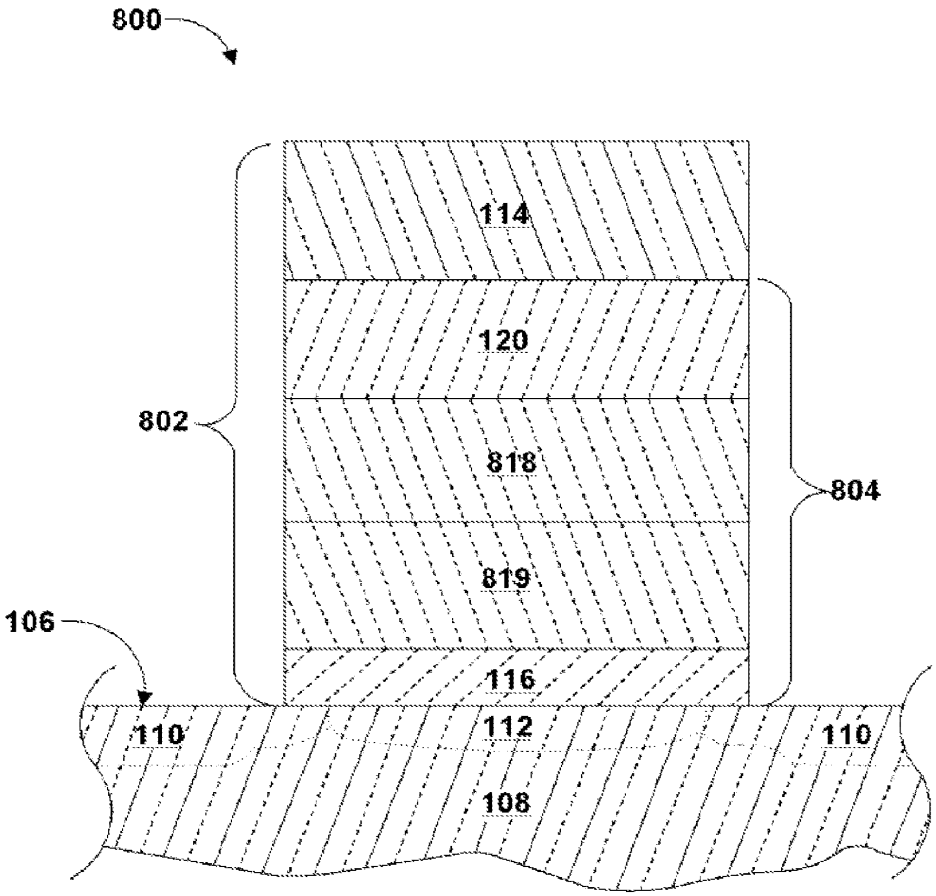


FIG. 6

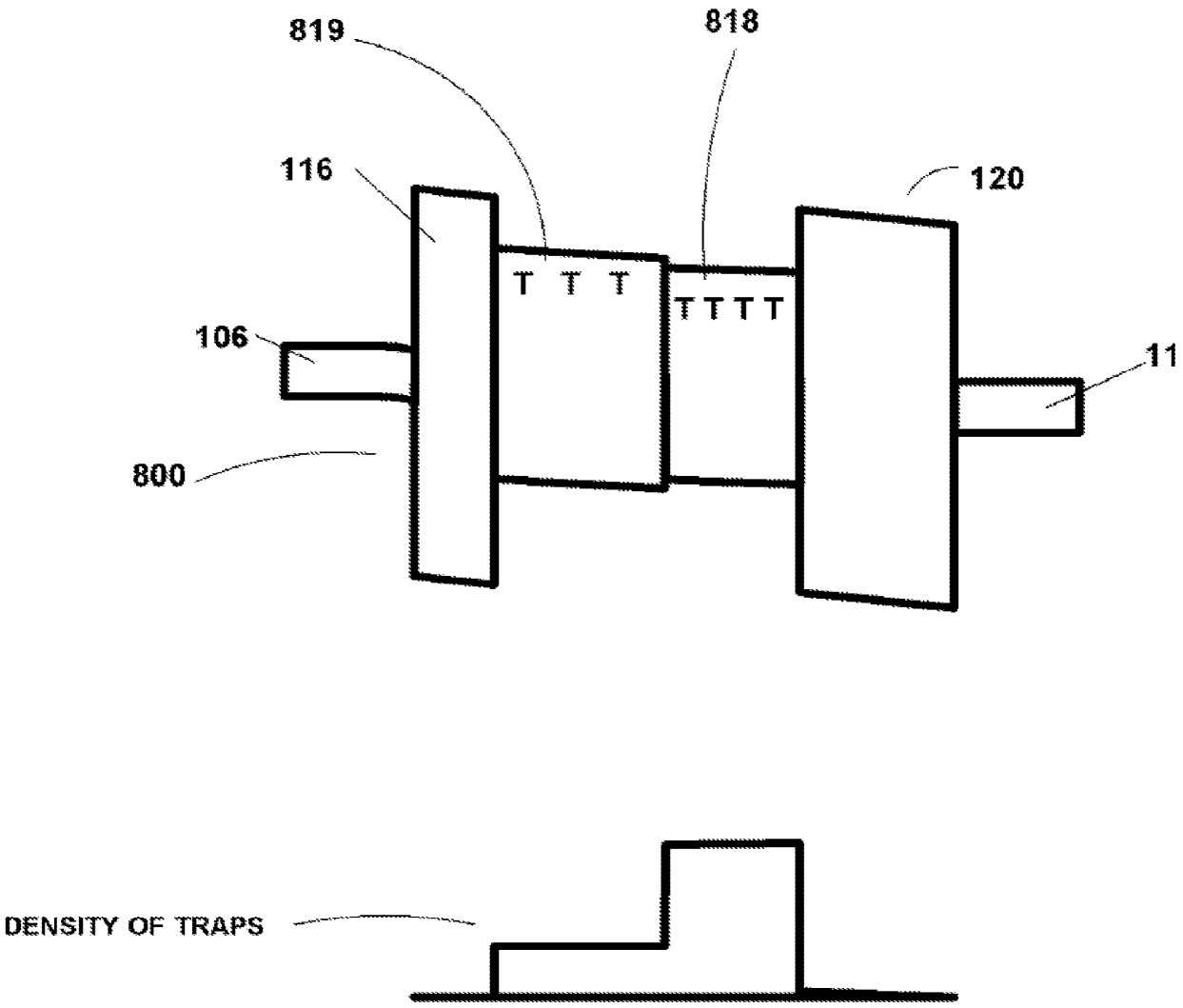


FIG. 7

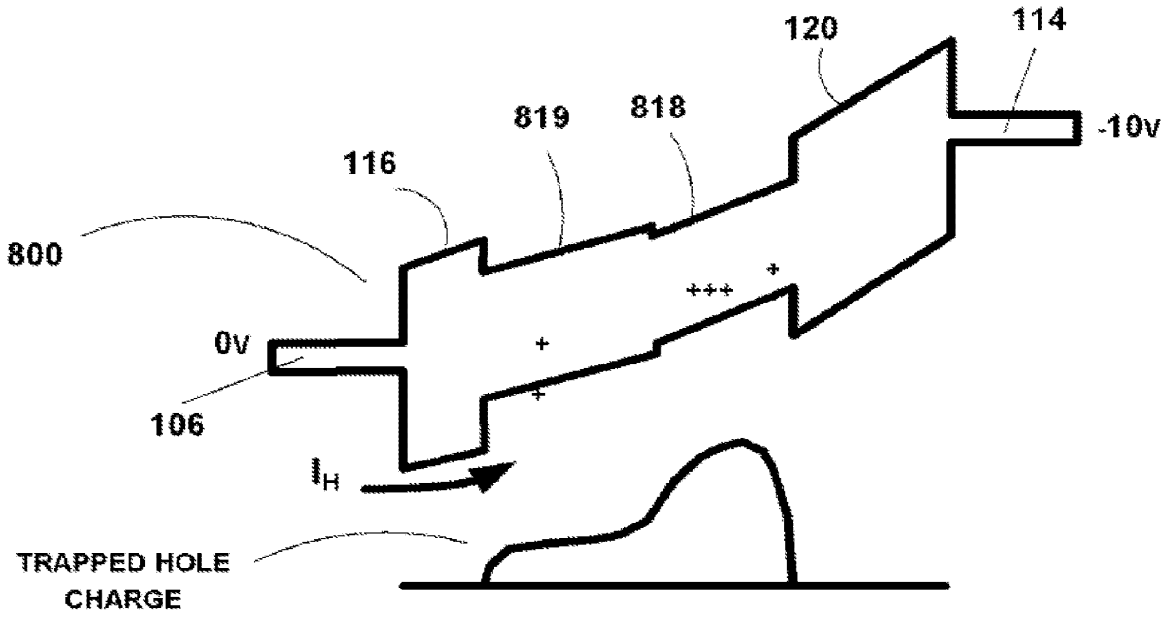


FIG. 8

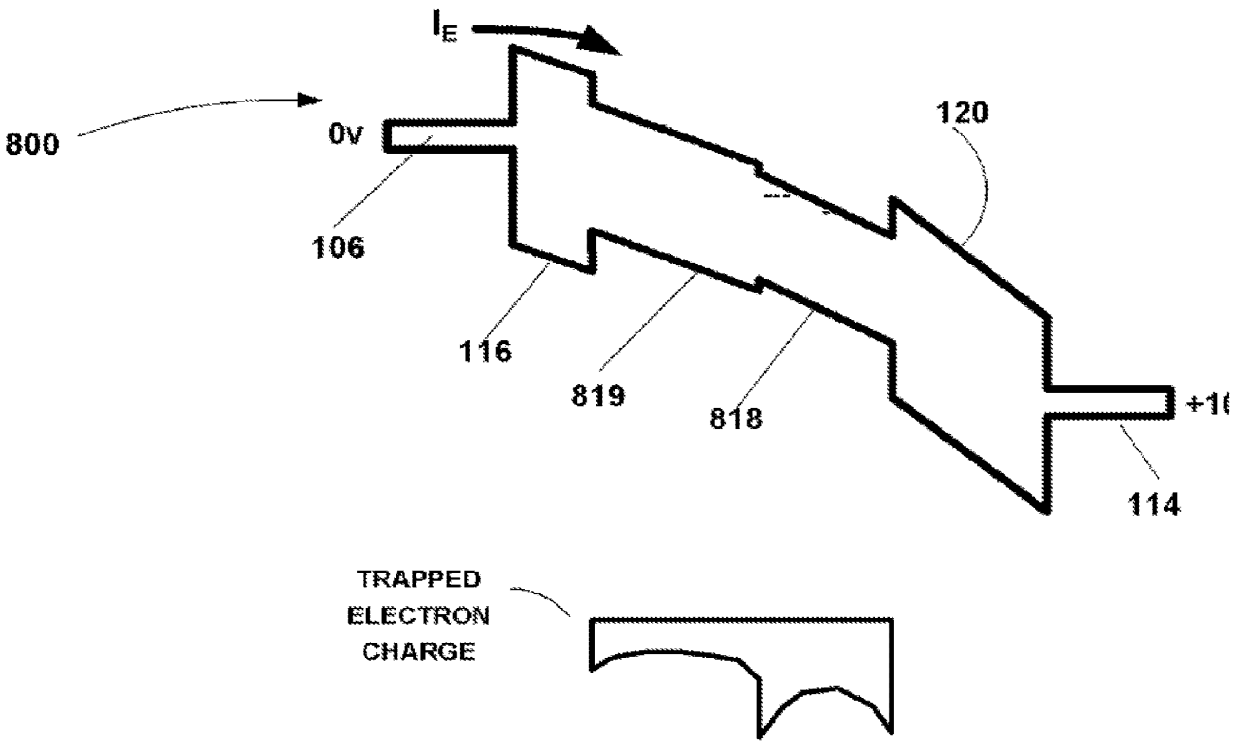


FIG. 9

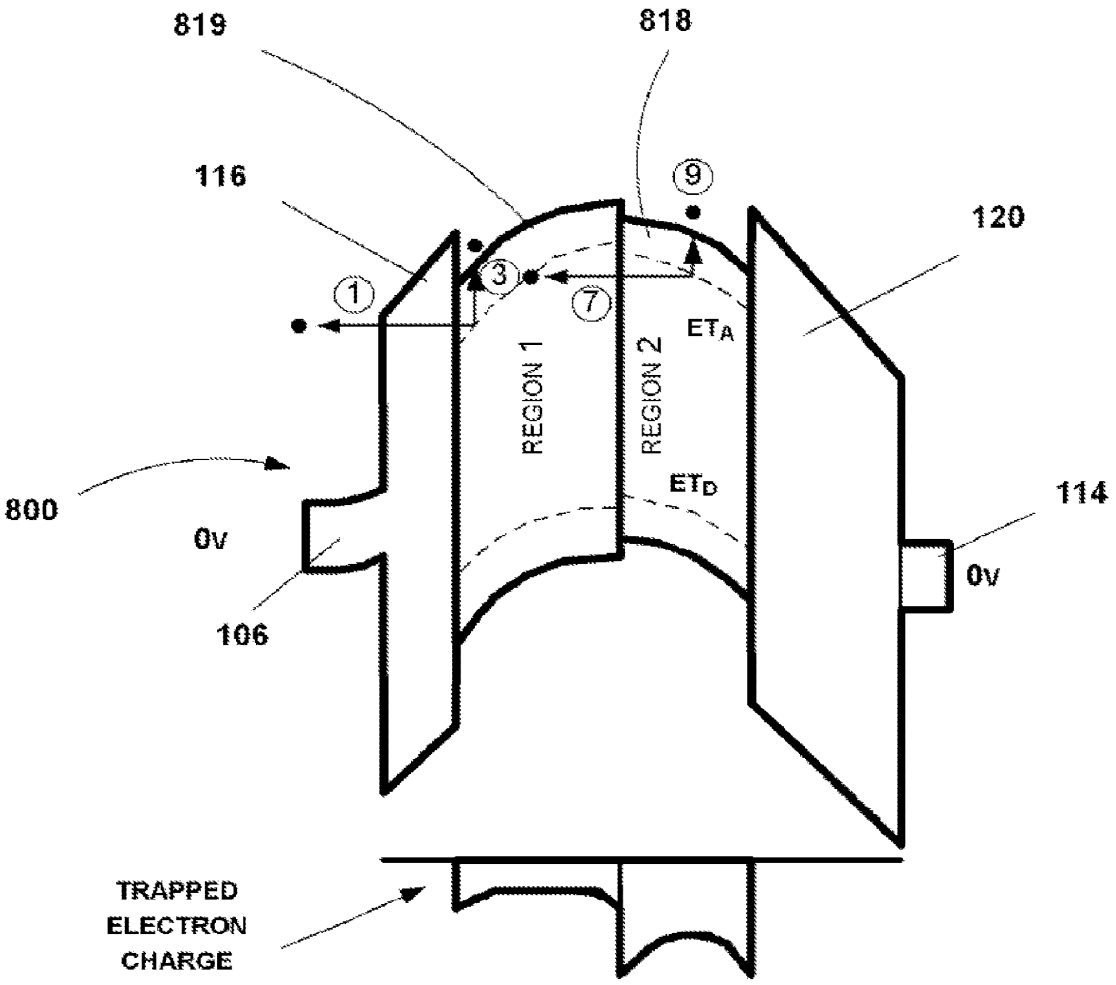

819
818
116
9
120
1
3
7
ET_A
REGION 1
REGION 2
800
ET_D
114
0V
0V
106
TRAPPED
ELECTRON
CHARGE

FIG. 10

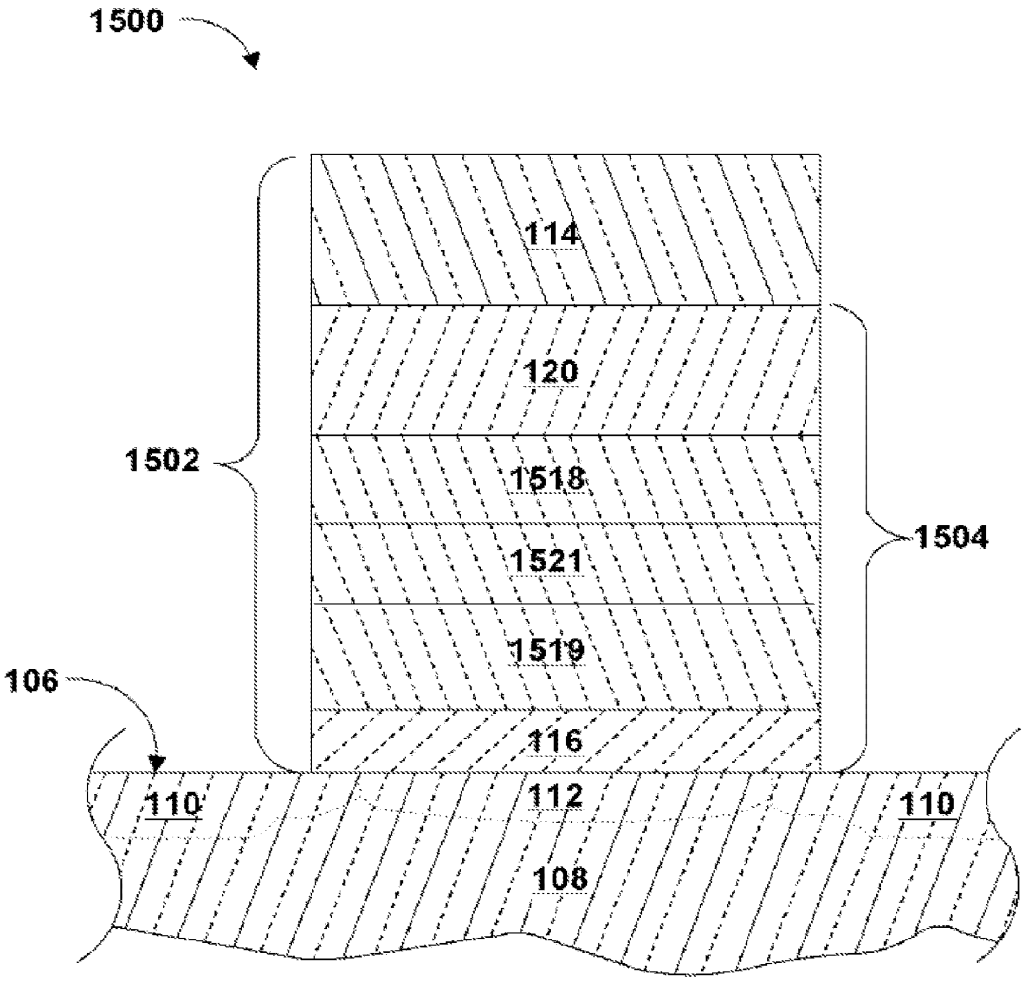


FIG. 11

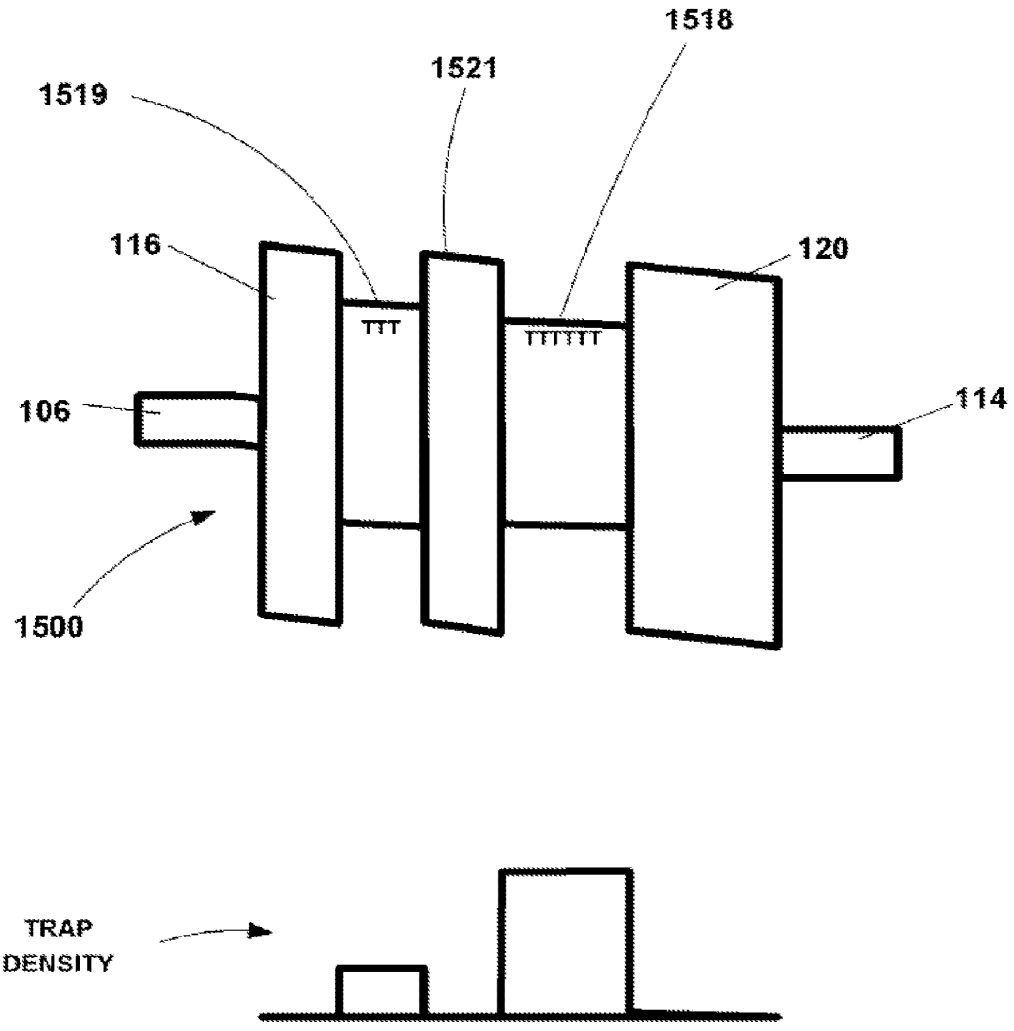


FIG. 12

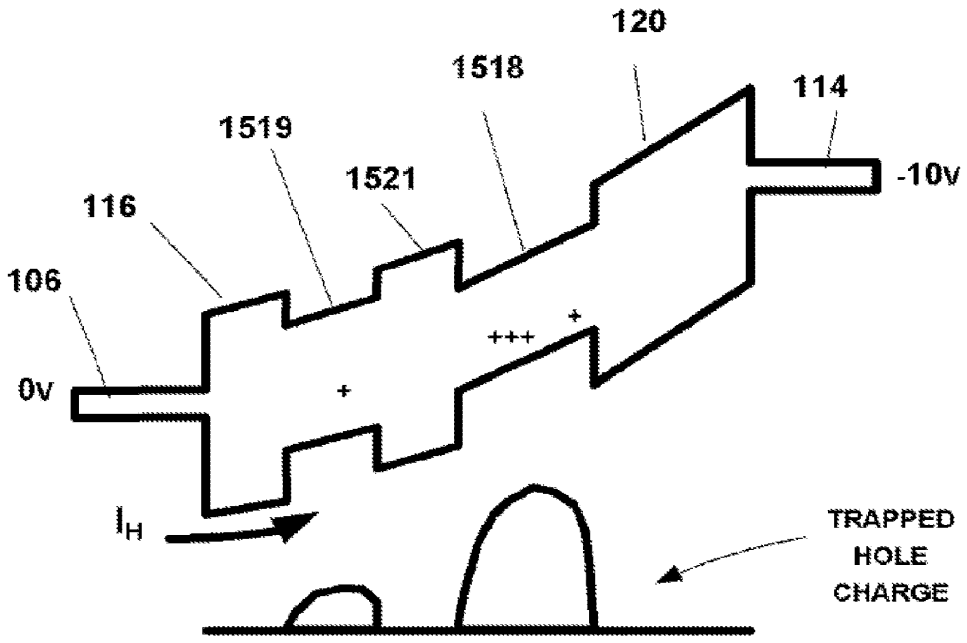


FIG. 13

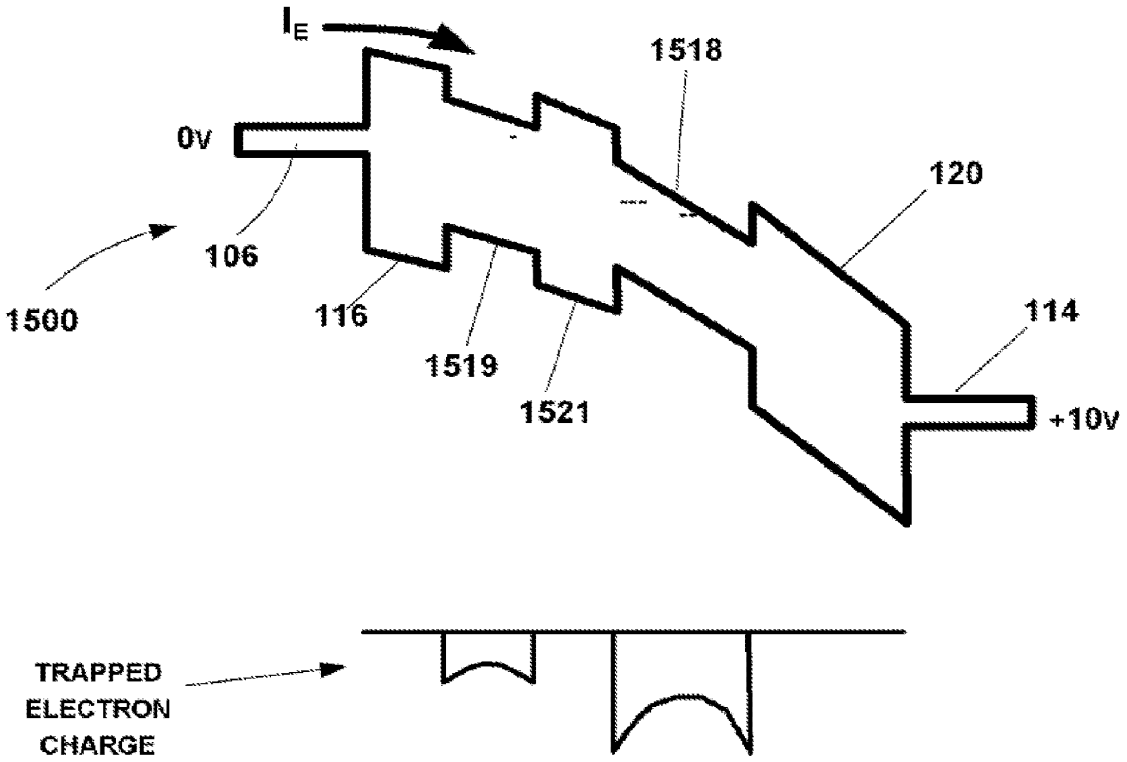

I_E
1518
0V
120
106
1500
116
114
1519
1521
+10V
TRAPPED
ELECTRON
CHARGE

FIG. 14

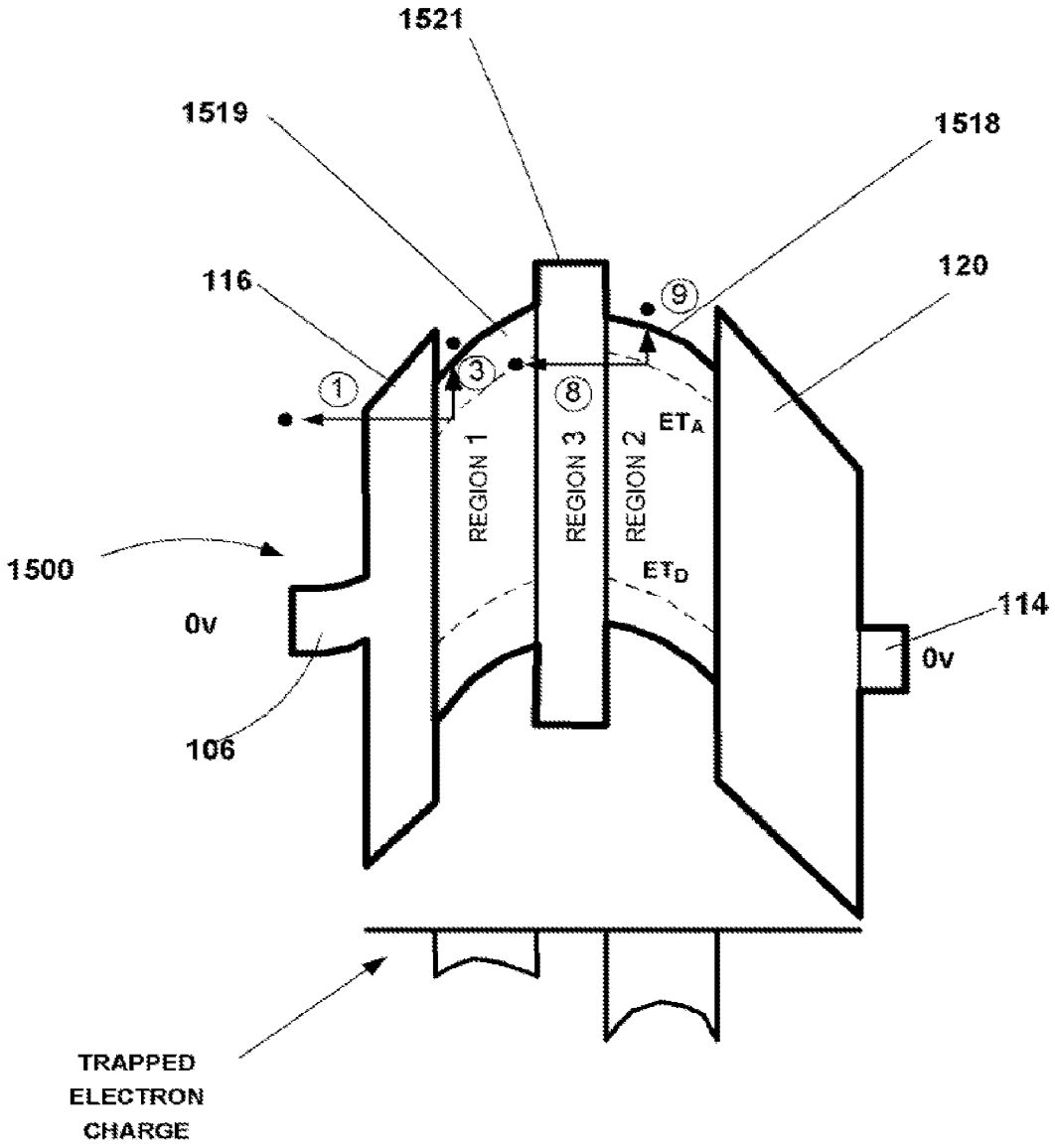

1521
1519
1518
116
120
9
1
3
8
REGION 1
REGION 3
REGION 2
ET_A
ET_D
1500
0V
114
0V
106
TRAPPED
ELECTRON
CHARGE

FIG. 15

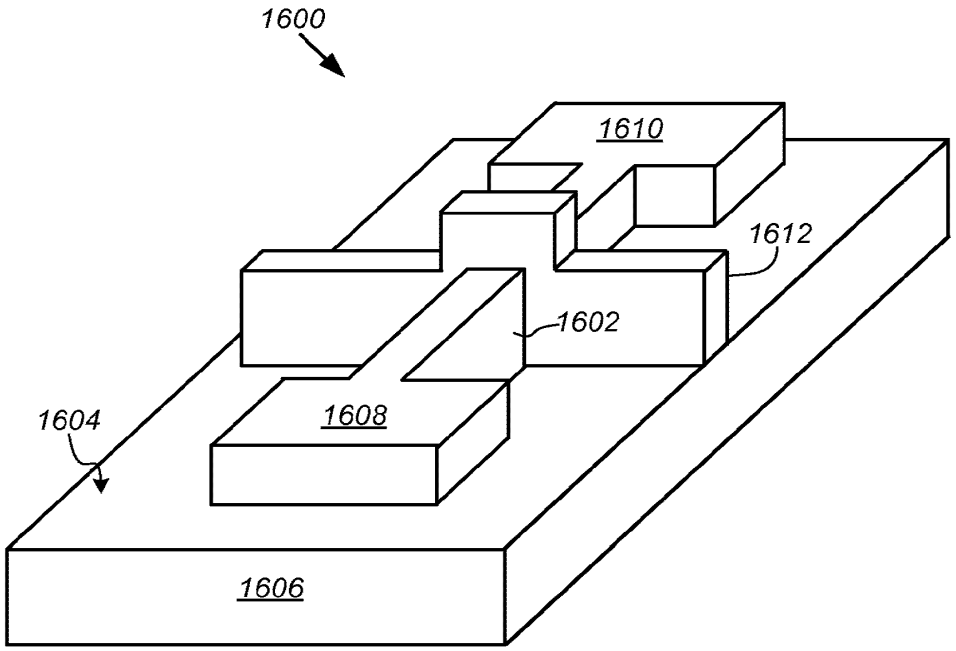


FIG. 16A

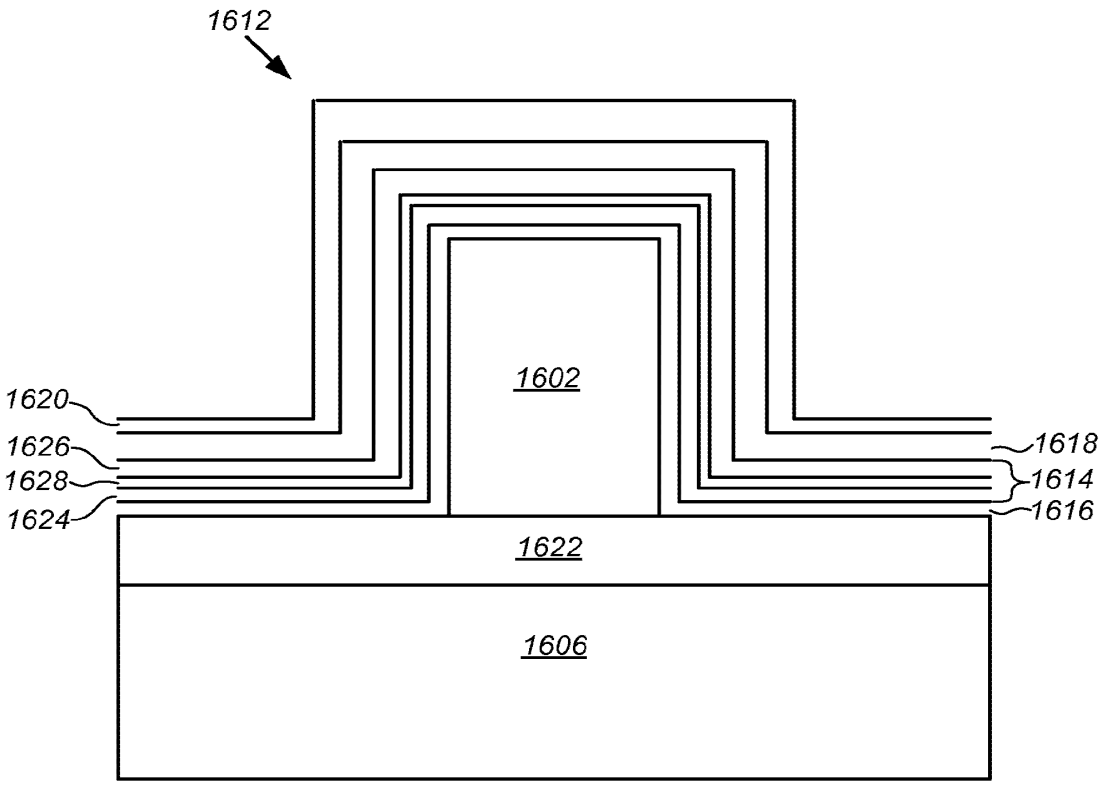


FIG. 16B

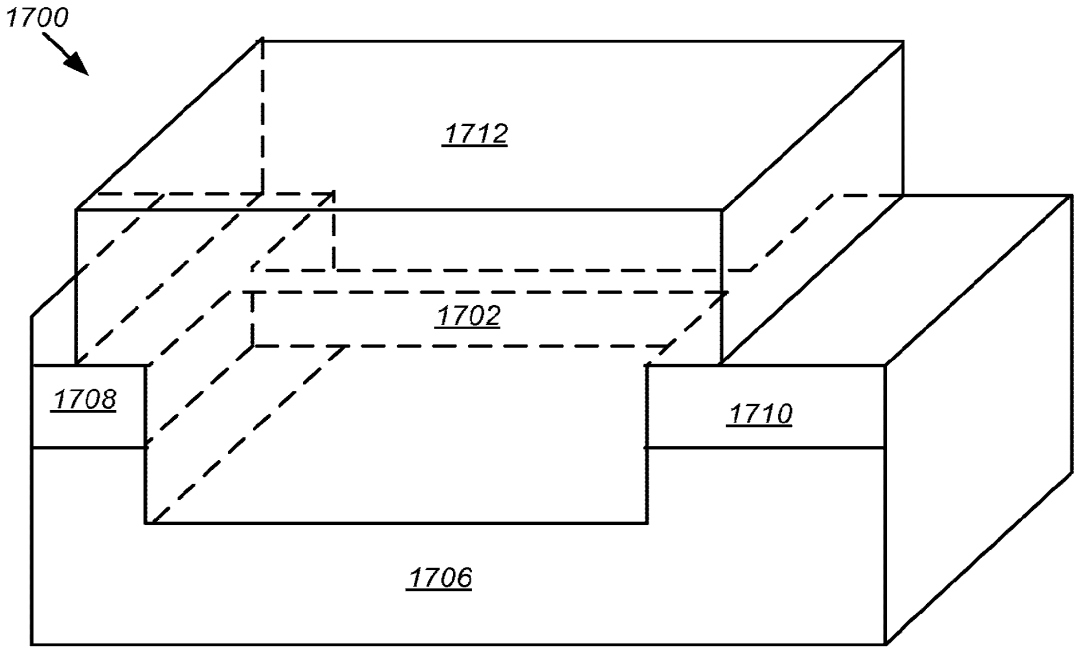


FIG. 17A

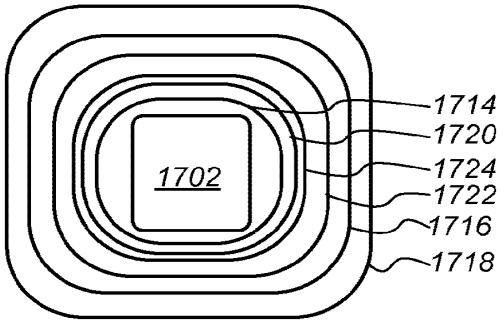


FIG. 17B

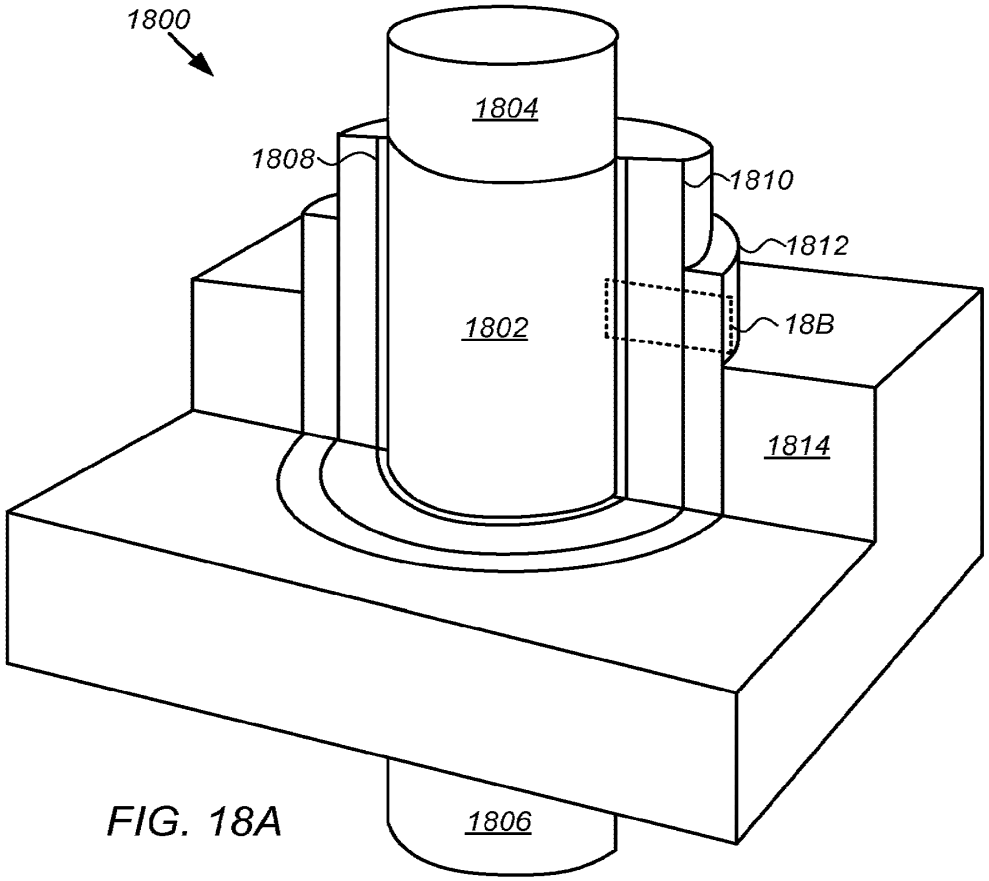


FIG. 18A

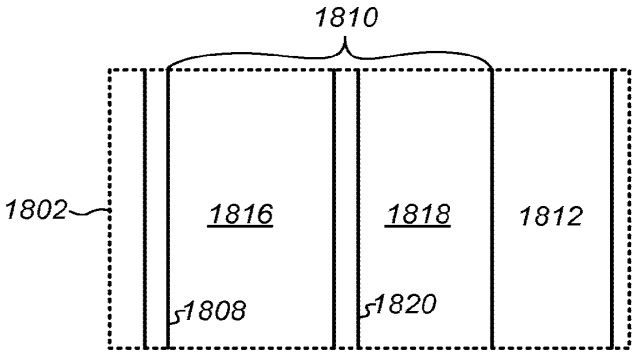


FIG. 18B

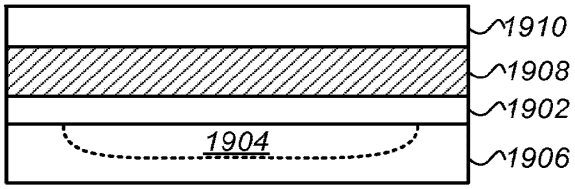


FIG. 19A

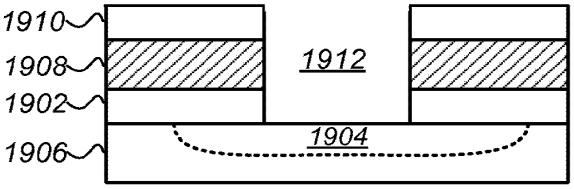


FIG. 19B

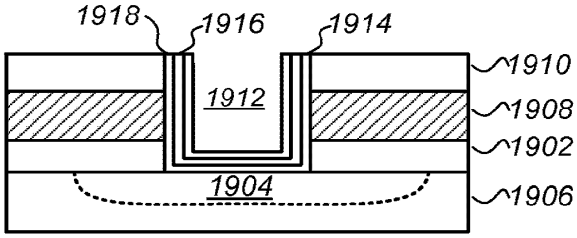


FIG. 19C

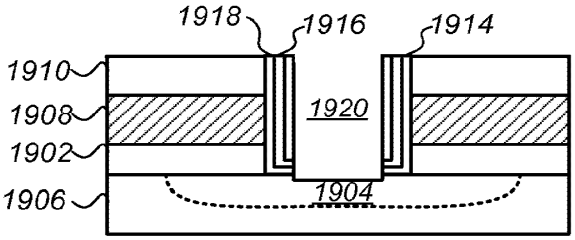


FIG. 19D

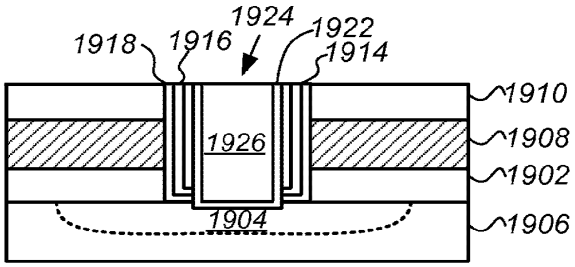


FIG. 19E

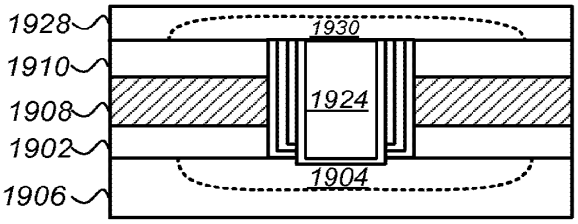


FIG. 19F

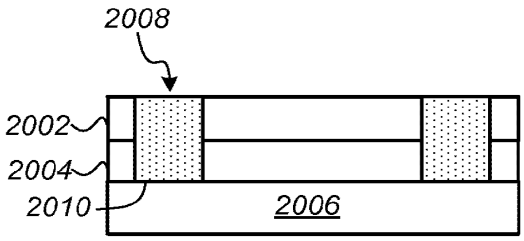


FIG. 20A

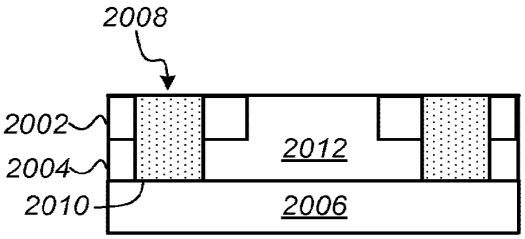


FIG. 20B

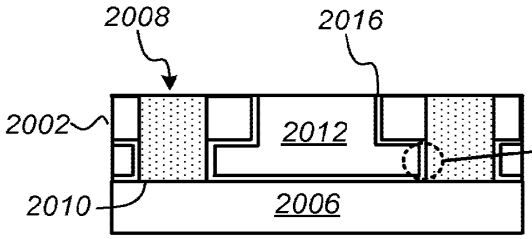


FIG. 20C

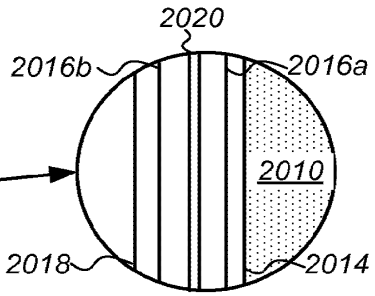


FIG. 20D

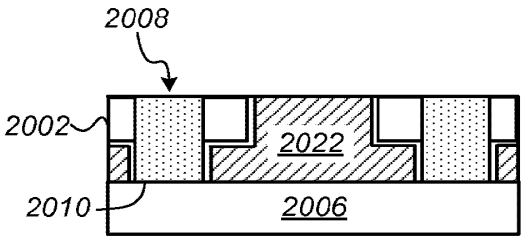


FIG. 20E

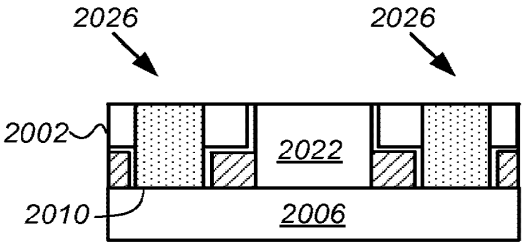


FIG. 20F

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US13/29784

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/792 (2013.01)
USPC - 438/591; 257/324, E29.308
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 29/792 (2013.01)
USPC - 438/920, 591; 257/321, 324, 325, E29.308, E29.309

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); Google Patents; Google Scholar; IP.COM, IEEE Xplore; Search Terms Used: Search Terms Used: non volatile memory, memory, NVM, charge trapping layers, SONOS, silicon oxynitride, tunneling layer, anti-tunneling layer, high K dielectric, thin film, nanowire*, FinFET, metal gate, nitrated oxide.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/0248332 A1 (LEVY S et al.) October 13, 2011, Figure 2, paragraphs [0022], [0025], [0045].	1-20
Y	US 7,999,295 B2 (LAI E et al.) August 16, 2011, column 3, lines 29 – 39, column 3, line 60 to column 4, line 4.	1-13, 15-17, 19, 20
Y	US 7,723,789 B2 (LIN H et al.) May 25, 2010, Figures 1A – 1H, column 2, line 63 to column 3, line 45.	7, 8, 11-18
Y	US 2009/0039414 A1 (LUE H et al.) February 12, 2009, Abstract.	4, 9, 13, 17, 18
Y	US 2009/0011609 A1 (RAMKUMAR K et al.) January 08, 2009, Figures 6E, 7A, paragraphs [0059] – [0065].	5

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 April 2013 (26.04.2013)	20 MAY 2013
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

Espacenet

Bibliographic data: WO2013148343 (A1) — 2013-10-03

OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

Inventor(s): LEVY SAGY [IL]; RAMKUMAR KRISHNASWAMY [US]; JENNE FREDRICK [US]; GEHA SAM [US] ± (LEVY, SAGY, ; RAMKUMAR, KRISHNASWAMY, ; JENNE, FREDRICK, ; GEHA, SAM)

Applicant(s): CYPRESS SEMICONDUCTOR CORP [US]; LEVY SAGY [IL]; RAMKUMAR KRISHNASWAMY [US]; JENNE FREDRICK [US]; GEHA SAM [US] ± (CYPRESS SEMICONDUCTOR CORPORATION, ; LEVY, SAGY, ; RAMKUMAR, KRISHNASWAMY, ; JENNE, FREDRICK, ; GEHA, SAM)

Classification: **- international:** ***H01L29/792***
- cooperative: **B82Y10/00**; **H01L21/28282**; **H01L27/11582**; **H01L29/0673**; **H01L29/0676**; **H01L29/42348**; **H01L29/513**; **H01L29/518**; **H01L29/66439**; **H01L29/66833**; **H01L29/775**; **H01L29/792**; **H01L29/7926**; H01L29/785

Application number: WO2013US32339 20130315 Global Dossier

Priority number(s): US201213436872 20120331

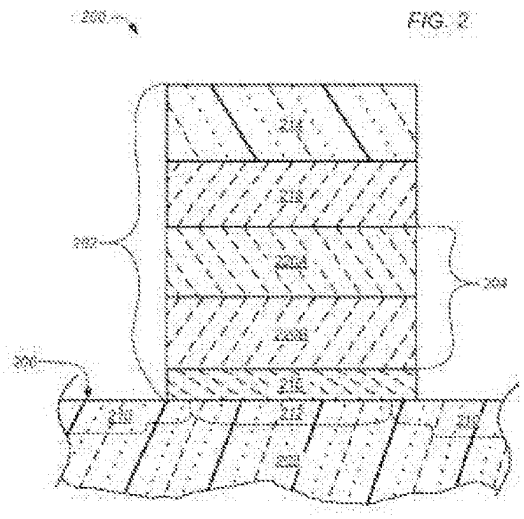
Also published as: TW201347151 (A) KR20140144181 (A) JP2015516678 (A) EP2831917 (A1) EP2831917 (A4) CN104321878 (A) less

Abstract of WO2013148343 (A1)

An embodiment of a semiconductor memory device including a multi-layer charge storing layer and methods of forming the same are described. Generally, the device includes a channel formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide layer overlying the channel; and a multi-layer charge storing layer including an oxygen-rich, first oxynitride layer on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean, second oxynitride layer on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense. In one embodiment, the device comprises a non-planar transistor including a gate having

Sandisk Technologies, Inc. - Ex. 1002, Page 000781

multiple surfaces abutting the channel, and the gate comprises the tunnel oxide layer and the multi-layer charge storing layer.



Sandisk Technologies, Inc. - Ex. 1002, Page 000782

台一國際專利法律事務所
Tai E International Patent & Law Office
9Fl., No. 112, Sec. 2, Chang-An E. Rd., Taipei 10491, Taiwan, R.O.C.
P.O. Box 46-478 Taipei 10499, Taiwan, R.O.C.
Tel: 886-2-25061023, 25081531
Fax: 886-2-25064319, 25076571, 25090804, 25068147
URL: http://www.taie.com.tw E-mail: ipdept@taie.com.tw

TRANSLATION OF THE OFFICIAL LETTER

1. SUMMARY

1.1 The present application was examined based on the Chinese version of the PCT application.

1.2 Citation:
1. US 2006/0228899A1 published on October 12, 2006.

1.3 Violation of the Claim Requirements
Claims 1-2, 4, 7-9, 11, 14-15 and 17 do not meet the novelty requirements of Article 22 §2 of the Patent Law.
Claims 3, 6, 10, 13, 16 and 18-20 do not meet the inventiveness requirements of Article 22 §3 of the Patent Law.
Claims 1 and 8 do not meet the requirements of Article 26 §4 of the Patent Law.

2. EXPLANATION
After the examination, the examiner deems that:

2.1 Claims 1-2, 4, 7-9, 11, 14-15 and 17 do not meet the novelty requirements of Article 22 §2 of the Patent Law and claims 3, 6, 10, 13, 16 and 18-20 do not meet the inventiveness requirements of Article 22 §3 of the Patent Law.

2.1.1 Claim 1 claims a method of fabricating a nonvolatile charge trap memory device. Citation 1 (US 2006/0228899A1) discloses a method of fabricating a nonvolatile charge trap memory device by referring to paragraphs [0071]-[0121] and figures 1-12 and specifically discloses the method, comprising: providing a substrate 101 having a charge-trapping layer disposed thereon; and oxidizing, by exposing the charge-trapping layer 202 to a radical oxidation process, a portion of the charge-trapping layer to form a blocking dielectric layer above the charge-trapping layer. Based on the foregoing descriptions, citation 1 discloses the technical features of claim 1 and the disclosed technical

Sandisk Technologies, Inc. - Ex. 1002, Page 000783

manner of citation 1 and the claimed scope of claim 1 belong to the same technical field, which can solve the same technical issues and generate the same technical effect. Hence, claim 1 does not meet the novelty requirements of Article 22 §2 of the Patent Law.

2.1.2 Claim 2 further limits the scope of claim 1. Citation 1 discloses that the radical oxidation process includes oxidizing with a radical selected from the group consisting of an OH radical, an HO_2 radical and an O diradical. Hence, claim 1 lacks novelty, so claim 2 does not meet the novelty requirements of Article 22 §2 of the Patent Law.

2.1.3 Claim 3 further limits the scope of claim 2. The attached technical feature is that the radical oxidation process is carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-5 Torr. However, a skilled person in the related field can confirm the suitable ranges of the above parameters by conventional manners and several tests. Hence, claim 2 lacks novelty, so claim 3 does not meet the inventiveness requirements of Article 22 §3 of the Patent Law.

2.1.4 Claim 4 further limits the scope of claim 1. Citation 1 discloses that the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the blocking dielectric layer comprises silicon dioxide. Hence, claim 1 lacks novelty, so claim 4 does not meet the novelty requirements of Article 22 §2 of the Patent Law.

2.1.5 Claim 6 further limits the scope of claim 1. The attached technical feature is annealing the blocking dielectric layer in an atmosphere comprising a gas is selected from the group consisting of nitrogen (N_2), nitrous oxide (N_2O), nitrogen dioxide (NO_2), nitric oxide (NO) and ammonia (NH_3) at a temperature approximately in the range of 700-800 degrees Celsius. However, a skilled person in the related field can confirm the suitable ranges of the above parameters by conventional manners and several tests. Hence, claim 1 lacks novelty, so claim 6 does not meet the inventiveness requirements of Article 22 §3 of the Patent Law.

2.1.6 Claim 7 further limits the scope of claim 1. Citation 1 discloses that a tunnel dielectric layer is disposed between the substrate and the charge-trapping layer. Hence, claim 1 lacks novelty, so claim 7 does not meet the novelty requirements of Article 22 §2 of the Patent Law.

Sandisk Technologies, Inc. - Ex. 1002, Page 000784

2.1.7 Claim 8 claims a method of fabricating a nonvolatile charge trap memory device. Citation 1 discloses a method of fabricating a nonvolatile charge trap memory device, comprising: providing a substrate 101 in a process chamber; subjecting, in the process chamber, the substrate to a first radical oxidation process to form a first dielectric layer 202; subjecting, in the process chamber, the substrate to a deposition process to form a charge-trapping layer above the first dielectric layer; and subjecting, in the process chamber, the substrate to a second radical oxidation process to form a second dielectric layer 64 above the charge-trapping layer by oxidizing a portion of the charge-trapping layer. Based on the foregoing descriptions, citation 1 discloses the technical features of claim 8 and the disclosed technical manner of citation 1 and the claimed scope of claim 8 belong to the same technical field, which can solve the same technical issues and generate the same technical effect. Hence, claim 8 does not meet the novelty requirements of Article 22 §2 of the Patent Law.

2.1.8 Claim 9 further limits the scope of claim 8. Citation 1 discloses that both the first and the second radical oxidation processes include oxidizing with a radical selected from the group consisting of an OH radical, an HO_2 radical and an O diradical. Hence, claim 8 lacks novelty, so claim 9 does not meet the novelty requirements of Article 22 §2 of the Patent Law.

2.1.9 Claim 10 further limits the scope of claim 9. The attached technical feature is that both the first and the second radical oxidation processes are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-5 Torr. However, a skilled person in the related field can confirm the suitable ranges of the above parameters by conventional manners and several tests. Hence, claim 9 lacks novelty, so claim 10 does not meet the inventiveness requirements of Article 22 §3 of the Patent Law.

2.1.10 Claim 11 further limits the scope of claim 8. Citation 1 discloses that the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide. Hence, claim 8 lacks novelty, so claim 11 does not meet the novelty requirements of Article 22 §2 of the Patent Law.

2.1.11 Claim 13 further limits the scope of claim 8. The attached technical

Sandisk Technologies, Inc. - Ex. 1002, Page 000785

feature is annealing, in the process chamber, the second dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N_2), nitrous oxide (N_2O), nitrogen dioxide (NO_2), nitric oxide (NO) and ammonia (NH3) at a temperature approximately in the range of 700 - 800 degrees Celsius; and, subsequently, depositing a gate layer above the second dielectric layer. However, a skilled person in the related field can confirm the suitable ranges of the above parameters by conventional manners and several tests. Hence, claim 8 lacks novelty, so claim 13 does not meet the inventiveness requirements of Article 22 §3 of the Patent Law.

2.1.12 Claim 14 further limits the scope of claim 8. Citation 1 discloses that the first dielectric layer is a tunnel dielectric layer, and wherein the second dielectric layer is a blocking dielectric layer. Hence, claim 8 lacks novelty, so claim 14 does not meet the novelty requirements of Article 22 §2 of the Patent Law.

2.1.13 Claim 15 further limits the scope of claim 8. Citation 1 discloses that subjecting the substrate to the deposition process to form the charge-trapping layer includes using a gas selected from the group consisting of dichlorosilane (H_2SiCh), bis-(tert-butylamino)silane (BTBAS), ammonia (NH^3) and nitrous oxide (N_2O). Hence, claim 8 lacks novelty, so claim 15 does not meet the novelty requirements of Article 22 §2 of the Patent Law.

2.1.14 Claim 16 further limits the scope of claim 8. The attached technical feature is that the process chamber is a low-pressure chemical vapor deposition chamber and belongs to a conventional technical manner in the field. Hence, claim 8 lacks novelty, so claim 16 does not meet the inventiveness requirements of Article 22 §3 of the Patent Law.

2.1.15 Claim 17 claims a radical oxidation method. Citation 1 discloses a radical oxidation method, comprising: providing a substrate 101 in a process chamber; mixing, in the process chamber, hydrogen gas and oxygen gas without subjecting the hydrogen gas and oxygen gas to a combustion process (by referring to paragraph [0066]); and oxidizing, in the process chamber, a portion of the substrate with radicals generated from the mixing of the hydrogen gas and oxygen gas. Based on the foregoing descriptions, citation 1 discloses the technical features of claim 17 and the disclosed technical manner of citation 1 and the claimed scope of claim 17 belong to the same technical field, which can solve the same technical issues and generate the same technical effect. Hence, claim 17 does not meet the novelty

Sandisk Technologies, Inc. - Ex. 1002, Page 000786

requirements of Article 22 §2 of the Patent Law.

2.1.16 Claim 18 further limits the scope of claim 17. The attached technical feature is that the mixing of the hydrogen gas and oxygen gas and the oxidizing of the portion of the substrate are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-5 Torr. However, a skilled person in the related field can confirm the suitable ranges of the above parameters by conventional manners and several tests. Hence, claim 17 lacks novelty, so claim 18 does not meet the inventiveness requirements of Article 22 §3 of the Patent Law.

2.1.17 Claim 19 further limits the scope of claim 18. The attached technical feature is that the hydrogen gas and oxygen gas are mixed in an approximate ratio of 1:1. However, a skilled person in the related field can confirm the suitable ranges of the above parameters by conventional manners and several tests. Hence, claim 18 lacks novelty, so claim 19 does not meet the inventiveness requirements of Article 22 §3 of the Patent Law.

2.1.18 Claim 20 further limits the scope of claim 17. The attached technical feature is that the process chamber is a low-pressure chemical vapor deposition chamber. However, a skilled person in the related field can confirm the suitable ranges of the above parameters by conventional manners and several tests. Hence, claim 17 lacks novelty, so claim 20 does not meet the inventiveness requirements of Article 22 §3 of the Patent Law.

2.2 Claims 1 and 8 do not meet the requirements of Article 26 §4 of the Patent Law.

The term "charge-trapping layer" described in claims 1 and 8 comprises a larger scope. Based on the description in the specification, the specification describes that the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5-3.5 nanometers and a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9-10 nanometers, wherein the charge-trapping layer comprises a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 2-3 nanometers and is oxidized to form blocking dielectric layer having a thickness approximately in the range of 3.5-4.5 nanometers. A skilled person in the relevant art would have difficulty in forecasting that other manner except for the manner based on the description in the specification can solve its technical issue and achieve the same technical effect. Therefore, claims 1 and 8 are not supported

Sandisk Technologies, Inc. - Ex. 1002, Page 000787

by the specification.

The applicant should file a response within a period assigned by the Official Letter and amend the application and explain the reasons for overcoming each problem listed in the Official Letter. Furthermore, amendments to the application must meet the requirements of Article 33 of the Patent Law and the requirements of Article 51 §3 of Implementing Regulations of the Patent Law. The examiner suggests that the applicant file an amended document in full text replacement (i.e. filing an amended specification in full text replacement when amending the specification or filing an amended set of claims in full text replacement when amending the claims).

Sandisk Technologies, Inc. - Ex. 1002, Page 000788

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

[redacted]

August 19, 2016

[redacted]

Attn.: [redacted]

[redacted]

Via Email Only

[redacted]

Re: National Phase in China of PCT/US2013/048876
In the name of Cypress Semiconductor Corporation
Title: Radical Oxidation Process for Fabricating a Nonvolatile Charge Trap Memory Device
CN Application No.: 2013800319699
Your Ref.: [redacted]
Our Ref.: 081409910-E

Deadline for Responding to this Office Action: **December 10, 2016 (Beijing Time)**
Issue date: July 26, 2016 ; 4 months rejection

Dear [redacted]:

The State Intellectual Property Office of China recently has issued the First Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below.

Examiner's Opinions in this OA

1. Novelty-Claims 1, 8-9 and 16

Claim 1

The Examiner points out that claim 1 does not possess novelty over Reference 1 (CN 104254921A, priority date: March 27, 2012, application date: March 8, 2013, publication date: December 31, 2014), Reference 1 constitutes a conflicting application over claim 1 of the present application and thus is not in conformity with the provisions of Article 22(2) of Patent Law, since Reference 1 (see paragraphs 0001-0101, 0044, 0081, 0092 of its Description, claim 6 and Figs. 1-20F) discloses all technical features of the technical scheme in claim 1, the technical scheme of claim 1 and the disclosure of Reference 1 are substantially the same and within the same technical field and can yield the same effect.

[redacted]

To overcome this issue, generally it is suggested to find the distinguishing technical features of the technical scheme of claim 1 from the technical scheme of Reference 1, or amend the technical scheme of claim 1 to include any distinguishing technical feature(s). If the present application and Reference 1 are in the different technical fields or the disclosure of Reference 1 cannot yield the same effect as the technical scheme of claim 1, please indicate so in the response.

Additionally, according to Chinese practice, on the basis that the novelty of a claim has been proved, it is also necessary to prove its inventiveness as the second step.

For the inventiveness, it is suggested to argue that the distinguishing technical features, found or included as in the above step, in claim 1 is non-obvious to a person skilled in the art and could produce advantageous technical effect as compared with the prior art.

In addition, if the followings exist for this invention, it is helpful to include them into the response:

- a person skilled in the art is hard to create the technical scheme of this invention due to some technical difficulties, technical prejudice or misleading from common thoughts;
- this invention brings unanticipated technical effects;
- this invention brings unanticipated success in the market; and
- other similar situations, such as long-felt but unsolved needs, failure of others.

Please consider the above information, analyze and give us your instruction. If you need any assistance, please let us know. We would be happy to assist.

2. Claim 8

The Examiner points out that claim 8 does not possess novelty on the condition that claim 1 it refers to does not possess novelty and the additional technical feature of claim 8 is disclosed by Reference 1 (see paragraphs 0029-0101 of its Description and Figs. 6-20F).

The solution for this issue depends on the solution for claim 8, to argue or let claim 1 have novelty and inventiveness. Once claim 1 has novelty and inventiveness, claim 8 has novelty and inventiveness too.

Claim 9

The Examiner points out that claim 9 does not possess novelty over Reference 1 (CN 104254921A, priority date: March 27, 2012, application date: March 8, 2013, publication date: December 31, 2014), Reference 1 constitutes a conflicting application over claim 9 of the present application and thus is not in conformity with the provisions of Article 22(2) of Patent Law, since Reference 1 (see paragraphs 0001-0101, 0044, 0081, 0092 of its Description, claim 6 and Figs. 1-20F) discloses all technical features of the technical scheme in claim 9, the technical scheme of claim 9 and the disclosure of Reference 1 are substantially the same and within the same technical field and can yield the same effect.

Sandisk Technologies, Inc. - Ex. 1002, Page 000790

To overcome this issue, you may follow the above similar suggestion as for claim 1.

Claim 16

The Examiner points out that claim 16 does not possess novelty over Reference 1 (CN 104254921A, priority date: March 27, 2012, application date: March 8, 2013, publication date: December 31, 2014), Reference 1 constitutes a conflicting application over claim 16 of the present application and thus is not in conformity with the provisions of Article 22(2) of Patent Law, since Reference 1 (see paragraphs 0001-0101, 0044, 0045, 0081, 0092 of its Description, claim 6 and Figs. 1-20F) discloses all technical features of the technical scheme in claim 16, the technical scheme of claim 16 and the disclosure of Reference 1 are substantially the same and within the same technical field and can yield the same effect.

To overcome this issue, you may follow the above similar suggestion as for claim 1.

2. Inventiveness –Claims 1-20

[AFD Remarks: Please be informed that in the form of this Office Action, claims 2-7, 10-15 and 17-20 are listed for not possessing inventiveness.]

Claim 1

The Examiner points out that claim 1 does not possess inventiveness over Reference 2 (US2008/0293255A1, November 27, 2008) in view of known common knowledge in the art, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 2 (see paragraphs 0001-0106 of its Description and Figs. 1-13B), the Examiner points out that a first dielectric layer 1002 is a tunnel oxide layer, an oxygen-rich silicon oxy-nitride layer 1004A is a first layer, a silicon-rich silicon oxy-nitride layer 1004B is equivalent to an oxygen-lean, second layer, a second dielectric layer 1006 is equivalent to a high-temperature-oxide (HTO) layer, and the Examiner admits that the distinguishing technical feature of the technical scheme in claim 1 is "*wherein the channel comprises polysilicon*".

The Examiner holds that the above distinguishing technical feature is conventional choice in the art. And thus on the basis of Reference 2 in combination of known common knowledge in the art, the technical scheme of claim 1 is obvious to a person skilled in the art.

Claim 9

The Examiner points out that claim 9 does not possess inventiveness over Reference 2 in view of Reference 3 and known common knowledge in the art, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 2 (see paragraphs 0001-0106 of its Description and Figs. 1-13B), the Examiner admits that the distinguishing technical features of the technical scheme in claim 9 are "*wherein the channel comprises polysilicon; wherein*

Sandisk Technologies, Inc. - Ex. 1002, Page 000791

the first layer is separated from the second layer by an anti-tunneling layer comprising an oxide".

The Examiner holds that Reference 3 (KR 10-2004-0070669A, August 11, 2004) (see line 1 on page 1 to the last line on page 5 of its Description and Figs. 1-3) discloses that a buffer nitride layer 103 (equivalent to a first layer) is separated from a trapping nitride layer (equivalent to a second layer) by a buffer oxide layer (equivalent to an anti-tunneling layer comprising an oxide); and provides technical teaching of providing a oxide layer between two nitride layers in the charge storage structure, finally forming S0N0N0S, thereby improving its maintaining feature so as to reduce charge leakage; under such teaching, a person skilled in the art has motivation to apply it to Reference 2, i.e. providing an anti-tunneling layer comprising an oxide between silicon oxy-nitride layer 1004A and silicon oxy-nitride layer 1004B. Moreover, it is conventional choice in the art to select polysilicon as the channel material according to the need of practical application. And thus on the basis of Reference 2 in combination of Reference 3 and known common knowledge in the art, the technical scheme of claim 9 is obvious to a person skilled in the art.

To overcome this issue, you may follow the above similar suggestion as for claim 1.

Claims 2, 4, 10 and 12

The Examiner points out that claims 2, 4, 10 and 12 do not possess inventiveness either. The Examiner holds that the additional technical features of claims 2, 4, 10 and 12 are conventional technical means in the art. And thus the technical schemes of claims 2, 4, 10 and 12 do not possess inventiveness on the condition that their respective claims they refer to do not possess inventiveness.

Claims 3, 5-6, 11 and 13-14

The Examiner points out that claims 3, 5-6, 11 and 13-14 do not possess inventiveness either. The Examiner holds that the additional technical features of claims 3, 5-6, 11 and 13-14 are conventional technical means in the art. And thus the technical schemes of claims 3, 5-6, 11 and 13-14 do not possess inventiveness on the condition that their respective claims they refer to do not possess inventiveness.

Claims 7 and 15

The Examiner points out that claims 7 and 15 do not possess inventiveness either. The Examiner holds that the additional technical features of claims 7 and 15 are disclosed by Reference 2 (see paragraphs 0035-0092 of its Description and Figs. 2-10E). And thus the technical schemes of claims 7 and 15 do not possess inventiveness on the condition that their respective claims they refer to do not possess inventiveness.

Claim 8

The Examiner points out that claim 8 does not possess inventiveness either. The

Sandisk Technologies, Inc. - Ex. 1002, Page 000792

Examiner holds that Reference 3 discloses relevant technical features, providing technical teaching. And thus on the basis of Reference 2 in combination of Reference 3 and known common knowledge in the art, the technical scheme of claim 8 is obvious to a person skilled in the art.

Claim 16

The Examiner points out that claim 16 does not possess inventiveness over Reference 4 (US 2009/0294844A1, December 3, 2009) in view of Reference 5 and known common knowledge in the art, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 4 (see paragraphs 0001-0130 of its Description and Figs. 1-26), the Examiner points out that a dielectric layer2303 is equivalent to a first dielectric layer, a dielectric layer 2305 is equivalent to a second dielectric layer, a source region 2303 is equivalent to a first doped diffusion region, a silicon oxide film 2401 is equivalent to a high-temperature-oxide (HTO) layer, a silicon nitride film 2402 is equivalent to a charge storing layer, a silicon oxide film 2404 is equivalent to a tunnel oxide layer, a silicon oxide film 2602 belongs to a layer of semiconducting material, a drain region 2603 is equivalent to a second doped diffusion region, and the Examiner admits that the distinguishing technical features of the technical scheme in claim 16 are the following:

the charge storing layer is a multi-layer charge storing layer, the multi-layer charge storing layer comprising an oxygen-lean, first oxynitride layer on the HTO layer in which a stoichiometric composition of the first oxynitride layer results in it being trap dense; and an oxygen-rich, second oxynitride layer on the first oxynitride layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free; channel comprising polysilicon.

The Examiner holds that Reference 5 (CN 101517714A, August 26, 2009) (see line 1 on page 1 to the last line on page 15 of its Description and Figs. 1-10) discloses that charge trapping layer is charge storing layer, a silicon oxynitride 518B is a first oxynitride layer, a silicon oxynitride 518A is a second oxynitride layer, a blocking layer 520 is equivalent to HTO layer. As can be seen, Reference 5 provides technical teaching of providing a multi-layer charge storing layer comprising comprising an oxygen-lean, first oxynitride layer and an oxygen-rich, second oxynitride layer, thereby, in case of maintaining good data maintaining, proportionately scaling the thickness of charge trapping layer. Under such teaching, a person skilled in the art has motivation to apply it to Reference 4, i.e. providing a multi-layer charge storing layer comprising an oxygen-lean, first oxynitride layer on the above silicon oxide film 2401 and an oxygen-rich, second oxynitride layer on the first oxynitride layer, without paying inventive work. Moreover, it is conventional choice in the art to select polysilicon as the channel material according to the need of practical application. And thus on the basis of Reference 4 in combination of Reference 5 and known common knowledge in the art, the technical scheme of claim 16 is obvious to a person skilled in the art.

To overcome this issue, you may follow the above similar suggestion as for claim 1.

Sandisk Technologies, Inc. - Ex. 1002, Page 000793

Claims 17-18

The Examiner points out that claims 17-18 do not possess inventiveness either. The Examiner holds that the additional technical features of claims 17-18 are conventional technical means in the art. And thus the technical schemes of claims 17-18 do not possess inventiveness on the condition that their respective claim they refer to does not possess inventiveness.

Claims 19-20

The Examiner points out that claims 19-20 do not possess inventiveness either. The Examiner holds that Reference 3 (see line 1 on page 1 to the last line on page 5 of its Description and Figs. 1-3) discloses relevant technical features, providing technical teaching of providing a oxide layer between two nitride layers in the charge storage structure, finally forming S0N0N0S, thereby improving its maintaining feature so as to reduce charge leakage; under such teaching, a person skilled in the art has motivation to apply it to Reference 4. Moreover, in practical application, a person skilled in the art has motivation to form a high-temperature-oxide (HTO) layer by any other suitable manner, which belongs to conventional technical means in the art. And thus on the basis of Reference 4 in combination of References 5 and 3 and known common knowledge in the art, the technical schemes of claims 19-20 are obvious to a person skilled in the art.

The solution for the inventiveness issue in the above groups of claims depends on the solution for their respective independent claims, to prove or amend the independent claims for inventiveness. Once the independent claims have inventiveness, all above dependent claims would have inventiveness too.

Conclusive opinion

Based on the above opinions, the Examiner also holds, as marked in the form of this Office Action, that the application does not possess any patentable substantial contents, and if the applicant fails to expound reasons or the reasons expounded are not sufficient, this application will be rejected.

This generally is a conclusive opinion of the Examiner and in next the Examiner is likely to issue a final rejection if the response to this Action is not persuasive or no substantial amendments are made.

Please be advised that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. The Office currently examines go-beyond issue very strictly, more strictly than that in many other countries. The "scope recorded in the initial description and claims", pursuant to the Patent Examination Guidelines, includes (1) literal contents of the initial description and claims, and (2) contents determined directly and undoubtedly from the drawings and the literal contents of the initial description and claims.

According to the Supreme Court's ruling in one recent case, such “scope” should include

Sandisk Technologies, Inc. - Ex. 1002, Page 000794

(i) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims of the application, and (ii) contents directly or definitely derived by a person skilled in the art from the initial description, drawings and claims as a whole, which should correct the strict rules of the Office. However, in practice, examiners are still likely to examine the go-beyond issue strictly. The applicant had better take this in mind if deciding to make any amendments.

A response and possible amendments must be submitted to the Office by **December 10, 2016 (Beijing Time)**. Please give us your further instructions as soon as possible.

[redacted]

Sincerely yours,
AFD China Intellectual Property

[redacted]

Patent Law:

Article 22(2): Novelty means that, the invention or utility model does not form part of the prior art; nor has any entity or individual filed previously before the date of filing with the Patent Administration Department Under the State Council an application relating to the identical invention or utility model disclosed in patent application documents published or patent documents announced after the said date of filing.

Article 22(3): Inventiveness means that, as compared with the prior art, the invention has prominent

Sandisk Technologies, Inc. - Ex. 1002, Page 000795

substantive features and represents a notable progress, and that the utility model has substantive features and represents progress.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/197,466	08/25/2008	Krishnaswamy Ramkumar	PM07024C1	2398

60909 7590 01/31/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2893	

MAIL DATE	DELIVERY MODE
01/31/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** *12/197,466*	**Applicant(s)** RAMKUMAR ET AL.
	Examiner THANH T. NGUYEN	**Art Unit** 2893

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 13 January 2012 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: *none*.
   Claim(s) objected to: *none*.
   Claim(s) rejected: *1-16 and 20*.
   Claim(s) withdrawn from consideration: *17-19*.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☒ Other: Claims 1-4, 6-10 are stand rejected as previously applied. Applicant contends that Nansei does not teach or suggest "radical oxidation using a source gas containg hydrogen". This is not found persuasive because Nansei et al. clearly teaches "radical oxidation using a source gas containing hydrogen" (see paragraph# 66, it is noted that Nansei et al. teaches numerous ways to form radical oxygen which clearly shown in paragraph# 66, wherein using oxygen with hydrogen gas is one alternative way).

Claims 5, 11-16, 20 are overcomed the prior art rejections.

Claims 1-16, 20 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting.

	/THANH T NGUYEN/ Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/605,231	01/26/2015	Krishnaswamy Ramkumar	PM07024CIP1C1	4843

60909 7590 03/09/2016

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
03/09/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@cypress.com
pbj@cypress.com
pbjtmp2@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000800

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 14/605,231	**Applicant(s)** RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	**Art Unit** 2893	**AIA (First Inventor to File) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 17 February 2016 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): (a) ☐ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☒ Other: Note the attached PTOL-2323.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed: n/a.
    Claim(s) objected to: n/a.
    Claim(s) rejected: 21-25, 29, 32-33, 35-38, 40-45.
    Claim(s) withdrawn from consideration: n/a.

/THANH T NGUYEN/
Primary Examiner, Art Unit 2893

Continuation of 12. does NOT place the application in condition for allowance because: all claims are overcomed the Prior Art rejection but they are still stand rejected on Double Patenting rejection. It is suggested to file the terminal disclaimer.

Sandisk Technologies, Inc. - Ex. 1002, Page 000802

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/605,231	01/26/2015	Krishnaswamy Ramkumar	PM07024CIP1C1	4843

60909 7590 07/05/2016

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
07/05/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@cypress.com
pbj@cypress.com
pbjtmp2@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000803

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 14/605,231	**Applicant(s)** RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	**Art Unit** 2893	**AIA (First Inventor to File) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 08 April 2016 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): (a) ☐ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed: n/a.
    Claim(s) objected to: n/a.
    Claim(s) rejected: 21-25,29-33,35-38 and 40-45.
    Claim(s) withdrawn from consideration: n/a.

/THANH T NGUYEN/
Primary Examiner, Art Unit 2893

Continuation of 12. does NOT place the application in condition for allowance because: Claims 21-25,29-33,35-38,40-45 are stand rejected on the ground of nonstatutory double patenting. The Terminal Disclaimer filed on 4/8/16 are disappoved because the person who signed the terminal disclaimer does not have Power of Attorney.

Sandisk Technologies, Inc. - Ex. 1002, Page 000805

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

60909 7590 01/31/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2893	

MAIL DATE	DELIVERY MODE
01/31/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/124,855	RAMKUMAR, KRISHNASWAMY	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/16/11*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *5,12 and 21-25* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *5,12 and 21-25* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 5, 12, 21-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) in view of Lee et al. (U.S. Patent No. 6,365,518).

Referring to figures 1-36, Nansei et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising:

Subjecting a substrate (1/101/201/301) to an oxidation process to form a first dielectric layer (21/62/203/302);

Depositing a charge-trapping layer (202/22/63/303) above the first dielectric layer (21/62/203/302), the charge-trapping layer (202/22/63/303) comprising a bottom portion and a top portion; and

Subjecting the charge-trapping layer (202/22/63/303) to a radical oxidation process to form a second dielectric layer (64/70/23/30/304/204/105) above the charge-trapping layer (202/22/63/303), forming radicals at a surface of the charge-trapping layer (see paragraph# 80), and consuming a portion of the top portion of the charge-trapping layer to form the second dielectric layer (oxidize the surface of the charge trapping by using the plasma oxidation process, see figures 3b, paragraph# 84).

Nansei et al teaches forming the layers in the cluster tool. However, the reference does not clearly teach using hydrogen and oxygen to oxidize the silicon nitride film.

Nansei et al. in paragraph# 66 teaches oxidizing process by mixing the hydrogen and oxygen radical oxidation, the radical oxidation process does not include an ignition event to pyrolyze the H_2 and O_2 gas to form steam (see paragraph# 66), the oxidation process to form the first dielectric layer is also a radical oxidation process comprising exposing the substrate to a H_2 and O_2 gas flow, and forming radicals at a surface of the substrate to form the second dielectric layer (see paragraphs# 66, 80).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would oxidize the silicon nitride film by using hydrogen and oxygen in process of Nansei et al. because oxidizing in hydrogen and oxygen would provide higher oxidation rate.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 5, 12, 21-25 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-16 of copending Application No. 12/197,466. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the instant invention and the copending application teaches oxidizing a portion of a charge-trapping layer disposed above a substrate to form a blocking dielectric layer above the charge-trapping layer, the oxidizing performed by exposing the charge-trapping layer to a hydrogen and oxygen radical oxidation process, wherein the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5-3.5 nanometers and a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9-10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer having a thickness approximately in the range of 3.5-4.5 nanometers.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM2007024	3433

60909 7590 05/10/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
05/10/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/124,855	RAMKUMAR, KRISHNASWAMY	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, 8, 11, 17 rejected under 35 U.S.C. 102(b/e) as being anticipated by Hisamoto et al. (U.S. Patent Publication No. 2007/0210371).

Referring to figures 3-30, Hisamoto et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising:

subjecting, in a process chamber, a substrate to a first hydrogenen and oxygen radical oxidation process to form a first dielectric layer (7, the lower portion, see figure 5, pargraph# 95);

subjecting, in the process chamber, the substrate to a deposition process to form a charge-trapping layer (7, silicon nitride, above the silicon oxide layer, see paragraph# 95, figure 5) above the first dielectric layer; and

subjecting, in the process chamber, the substrate to a second hydrogen and oxygen radical oxidation process to form a second dielectric layer (7, the upper part of layer 7) above the charge-trapping layer by oxidizing a portion of the charge-trapping layer (see figure 5, paragraph# 95).

Regarding to claim 4, 11, wherein the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (see paragraphs# 95).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4, 7-11, 14-15, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899).

Referring to figures 1-36, Nansei et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising:

Oxidizing a portion of a charge-trapping layer (202/22/63/303) to form a blocking dielectric layer (33/8) above the charge trapping layer, the oxidizing performed by exposing the charge-trapping layer (202/22/63/303) to a radical oxidation process (see paragraph# 66);

Depositing a gate layer above the second dielectric layer (8/33).

Regarding to claim 2, wherein both the first and the second radical oxidation processes include oxidizing with a radical selected from the group consisting of an OH radical, an HO.sub.2 radical and an O diradical (see paragraph# 66).

Regarding to claim 4, wherein the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (see paragraphs# 65, 68-69).

Regarding to claims 7, 14, wherein the nonvolatile charge trap memory device is a SONOS-type device, wherein the first dielectric layer is a tunnel dielectric layer, and wherein the second dielectric layer is a blocking dielectric layer (see paragraphs# 152, 164-166).

Regarding to claim 8, a method of fabricating a nonvolatile charge trap memory device, comprising:

Providing a substrate (1/101/201/301) in a process chamber (see figure 14);

subjecting, in a first process chamber (see figure 14), a substrate to a first radical oxidation process to form a first dielectric layer (21/62/203/302);

subjecting, in the process chamber, the substrate to a deposition process to form a charge-trapping layer above the first dielectric layer (202/22/63/303); and

subjecting, in the process chamber, the substrate to a second radical oxidation process to form a second dielectric layer above the charge-trapping layer by oxidizing a portion of the charge-trapping (64/70/23/30/304/204/105).

Regarding to claim 9, wherein both the first and the second radical oxidation processes include oxidizing with a radical selected from the group consisting of an OH radical, an HO.sub.2 radical and an O diradical (see paragraph# 66).

Regarding to claim 10, wherein the first dielectric layer, the charge-trapping layer and the second dielectric layer are formed without breaking vacuum in the cluster tool.

Regarding to claim 11, wherein the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (see paragraphs# 65, 68-69).

Regarding to claim 15, subjecting the substrate to the deposition process to form the charge-trapping layer (202/22/63/303) includes using a gas selected from the group consisting of dichlorosilane (H.sub.2SiCl.sub.2), bis-(tert-butylamino)silane (BTBAS), ammonia (NH.sub.3) and nitrous oxide (N.sub.2O) (see paragraph# 166).

Regarding to claim 17, a radical oxidation method, comprising:

Providing a substrate (1/101/201/301) in a process chamber (see figure 14);

Mixing, in the process chamber, hydrogen gas and oxygen gas without subjecting the hydrogen gas and oxygen gas to a combustion process (see paragraph# 66); and

Oxidizing, in the process chamber, a portion of the substrate with radicals generated from the mixing of the hydrogen gas and oxygen gas (see paragraph# 66).

However, the reference does not clearly teach using hydrogen and oxygen to oxidize the silicon nitride film.

Nansei et al. in paragraph# 66 teaches oxidizing process by mixing the hydrogen and oxygen radical oxidation.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would oxidize the silicon nitride film by using hydrogen and oxygen in process of Nansei et al. because oxidizing in hydrogen and oxygen would provide higher oxidation rate.

Claims 3, 6, 13, 16, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) as applied to claims 1-2, 4, 7-11, 14-15, 17 above in view of Wang (U.S. Patent No. 2005/0266637).

Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach radical oxidation processes are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-15 Torr (claims 3, 10, 18), annealing the blocking dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N.sub.2), nitrous oxide (N.sub.2O), nitrogen dioxide (NO.sub.2), nitric oxide (NO) and ammonia (NH.sub.3) at a

temperature approximately in the range of 700-800 degrees Celsius (claim 6, 13), the hydrogen gas and oxygen gas are mixed in an approximate ratio of 1:1 (claim 19), the process chamber is a low-pressure chemical vapor deposition chamber (claim 16, 20).

Wang teaches a method of forming a flash memories device forming radical oxidation processes are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-15 Torr (see paragraph# 27), annealing the blocking dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N.sub.2), nitrous oxide (N.sub.2O), nitrogen dioxide (NO.sub.2), nitric oxide (NO) and ammonia (NH.sub.3) at a temperature approximately in the range of 700-800 degrees Celsius (see paragraph# 21), the hydrogen gas and oxygen gas are mixed in an approximate ratio of 1:1 (see paragraph# 27), the process chamber is a low-pressure chemical vapor deposition chamber (see paragraph# 7).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to forming radical oxidation at the specific temperature/pressure, annealing at a specific temperature/gas, and using LPCVD chamber to form layers for memory device in Nansei et al. as taught by Wang because forming radical oxidation at the specific temperature/pressure, annealing at a specific temperature/gas, and using LPCVD chamber to form layers for memory device is known in the semiconductor art to form conformal/desired layers for memory device.

Claims 5, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) as applied to claims 1-2, 4, 7-11, 14-15, 17 above in view of Rathor et al. (U.S. Patent No. 6,818,558).

Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5-3.5 nanometers and a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9-10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the second dielectric layer having a thickness approximately in the range of 3.5-4.5 nanometers (claim 5, 12).

Rathor et al. teaches forming charge storing dielectric for SONOS-type device having multiple layers (see figures 7-8E) wherein the bottom portion (816, see col. 12, lines 26-33), the top layer (818/820, see col. 12, lines 49-67, col. 13, lines 1-15).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a charge-trapping oxy-nitride film with a desired thickness in process of Nansei et al. as taught by Rathor et al. because the process is known in the semiconductor art to form a SONOS type memory device structure comprising an oxy-nitride film with a desired thickness.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau, can be reached on (571) 272-1945. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/197,466	08/25/2008	Krishnaswamy Ramkumar	PM07024C1	2398

60909 7590 11/17/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2893	

MAIL DATE	DELIVERY MODE
11/17/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/197,466	RAMKUMAR ET AL.	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-21* is/are pending in the application.

5a) Of the above claim(s) *17-19* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-16,20 and 21* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-16, 20-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4, 7, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) in view of Lee et al. (U.S. Patent No. 6,365,518).

Referring to figures 1-36, Nansei et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising:

Providing a substrate (1/101/201/301) in a process chamber (see figure 14);

subjecting, in a first process chamber (see figure 14), a substrate to a first radical oxidation process to form a first dielectric layer (21/62/203/302);

subjecting, in the process chamber, the substrate to a deposition process to form a charge-trapping layer above the first dielectric layer (202/22/63/303); and

subjecting, in the process chamber, the substrate to a second radical oxidation process to form a second dielectric layer above the charge-trapping layer by oxidizing a portion of the charge-trapping (64/70/23/30/304/204/105).

Regarding to claims 2, wherein both the first and the second radical oxidation processes include oxidizing with a radical selected from the group consisting of an OH radical, an HO.sub.2 radical and an O diradical (see paragraph# 66).

Regarding to claim 4, wherein the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (see paragraphs# 65, 68-69).

Regarding to claims 7, wherein the nonvolatile charge trap memory device is a SONOS-type device, wherein the first dielectric layer is a tunnel dielectric layer, and wherein the second dielectric layer is a blocking dielectric layer (see paragraphs# 152, 164-166).

Regarding to claim 8, subjecting the substrate to the deposition process to form the charge-trapping layer (202/22/63/303) includes using a gas selected from the group consisting of dichlorosilane (H.sub.2SiCl.sub.2), bis-(tert-butylamino)silane (BTBAS), ammonia (NH.sub.3) and nitrous oxide (N.sub.2O) (see paragraph# 166).

Nansei et al teaches forming the layers in the cluster tool. However, the reference does not clearly teach the radical oxidation process comprises flowing hydrogen and oxygen gas into the chamber to oxidize the silicon nitride film and forming the layers in different chamber of cluster tool.

Nansei et al. in paragraph# 66 teaches oxidizing process by mixing the hydrogen and oxygen radical oxidation. It is noted that in paragraph# 66 shows many alternative processes to oxidize the silicon nitride film which include using mixed gas of oxygen and hydrogen while the example of Nansei et al. use one of the plurality process to oxidize the silicon nitride film which is oxygen gas.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would oxidize the silicon nitride film by using hydrogen and oxygen in process of Nansei et al. because oxidizing in hydrogen and oxygen would provide higher oxidation rate.

Lee et al. teaches cluster tool includes more than one processing chamber and transfer chamber (see col. 1, lines 54-67).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would recognize the cluster tool have more than one processing chamber as taught by Lee et al. in process of Nansei et al. because the process is known in the semiconductor art to reduce processing time with evacuating and re-pressurizing different processing chamber.

Claims 3, 6, 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) in view of Lee et al. (U.S. Patent No. 6,365,518) as applied to claims 1-2, 4, 7, 10 above in view of Wang (U.S. Patent No. 2005/0266637).

Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach radical oxidation processes are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-15 Torr (claims 3), annealing the blocking dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N.sub.2), nitrous oxide (N.sub.2O), nitrogen dioxide (NO.sub.2), nitric oxide (NO) and ammonia (NH.sub.3) at a temperature approximately in the range of 700-1100 degrees Celsius (claim 6, 13), the process chamber is a low-pressure chemical vapor deposition chamber (claim 9).

Wang teaches a method of forming a flash memories device forming radical oxidation processes are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-15 Torr (see paragraph# 27), annealing the blocking dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N.sub.2), nitrous oxide (N.sub.2O), nitrogen dioxide (NO.sub.2), nitric oxide (NO) and ammonia (NH.sub.3) at a temperature approximately in the range of 700-800 degrees Celsius (see paragraph# 21), the hydrogen gas and oxygen gas are mixed in an approximate ratio of 1:1 (see paragraph# 27), the process chamber is a low-pressure chemical vapor deposition chamber (see paragraph# 7).

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the temperature range, time range, thickness range and pressure of forming dielectric layers, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- the temperature range, time range, thickness range and

pressure of forming dielectric layers), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- the temperature range, time range, thickness range and pressure of forming dielectric layers) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to forming radical oxidation at the specific temperature/pressure, annealing at a specific temperature/gas, and using LPCVD chamber to form layers for memory device in Nansei et al. as taught by Wang because forming radical oxidation at the specific temperature/pressure, annealing at a specific temperature/gas, and using LPCVD chamber to form layers for memory device is known in the semiconductor art to form conformal/desired layers for memory device.

Claims 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) in view of Lee et al. (U.S. Patent No. 6,365,518) as applied to claims 1-2, 4, 7, 10 above in view of Rathor et al. (U.S. Patent No. 6,818,558).

Referring to figures 1-36, Nansei et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising:

Providing a substrate (1/101/201/301) in a process chamber (see figure 14);

subjecting, in a first process chamber (see figure 14), a substrate to a first radical oxidation process to form a first dielectric layer (21/62/203/302);

subjecting, in the process chamber, the substrate to a deposition process to form a charge-trapping layer above the first dielectric layer (202/22/63/303); and

subjecting, in the process chamber, the substrate to a second radical oxidation process to form a second dielectric layer above the charge-trapping layer by oxidizing a portion of the charge-trapping (64/70/23/30/304/204/105).

Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach forming the layers in different chamber of cluster tool, the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion, and wherein oxidizing the portion of the charge-trapping layer of the top silicon-rich silicon oxy-nitride portion to form the second dielectric layer.

Lee et al. teaches cluster tool includes more than one processing chamber and transfer chamber (see col. 1, lines 54-67).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would recognize the cluster tool have more than one processing chamber as taught by Lee et al. in process of Nansei et al. because the process is known in the semiconductor art to reduce processing time with evacuating and re-pressurizing different processing chamber.

Rathor et al. teaches forming charge storing dielectric for SONOS-type device having multiple layers (see figures 7-8E) wherein the bottom portion (816, see col. 12, lines 26-33), the top layer (818/820, see col. 12, lines 49-67, col. 13, lines 1-15).

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the thickness range of forming dielectric layers, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- the thickness range of forming dielectric layers), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- the thickness range of forming dielectric layers) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a charge-trapping oxy-nitride film with a desired thickness in process of Nansei et al. as taught by Rathor et al. because the process is known in the semiconductor art to form a SONOS type memory device structure comprising an oxy-nitride film with a desired thickness.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-21 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 5, 12 of copending Application No. 12/124,855. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the instant invention and the copending application teaches

oxidizing a portion of a charge-trapping layer disposed above a substrate to form a blocking dielectric layer above the charge-trapping layer, the oxidizing performed by exposing the charge-trapping layer to a hydrogen and oxygen radical oxidation process, wherein the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Arguments

Applicant's arguments with respect to claims 1-16, 20-21 have been considered but are moot in view of the new ground(s) of rejection.

Applicant contends that Nansei et al. does not clearly teach "wherein at least the second radical oxidation process comprises flowing hydrogen (H2) and oxygen (O2) gas into the first process chamber, forming radicals at a surface of the charge-trapping layer, and consuming a portion of the charge-trapping layer, to form a second dielectric layer." This is not found persuasive because Nansei et al. clearly teaches the second radical oxidation process comprises flowing hydrogen (H2) and oxygen (O2) gas into the first process chamber, forming radicals at a surface of the charge-trapping layer, and consuming a portion of the charge-trapping layer, to form a second dielectric layer (see paragraph# 66). Applicant further contends that Nansei et al. only teaches forming an oxygen radical by using oxygen gas without hydrogen. This is not

found persuasive because there are many ways to form radical oxygen which clearly shown in paragraph #66, wherein using only oxygen is one alternative way.

Applicant contends that Nansei does not teach/suggest forming the radicals at a surface of the charge-trapping layer. This is not found persuasive because oxygen radicals have to form at the surface of the charge-trapping layer in order to oxidize the charge trapping layer (see paragraph#44).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by

Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

TTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/307,858	06/18/2014	Igor Polishchuk	PM07027D1C1	7201

60909 7590 10/08/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	

ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
10/08/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000837

Office Action Summary	Application No. 14/307,858	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2819	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8-18-15*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-40* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21-40* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

The Terminal Disclaimer filed August 18, 2015 is not approved.

This application was filed on or after September 16, 2012. The person who signed the terminal disclaimer is not the applicant, the patentee or an attorney or agent of record. See 37 CFR 1.321(a) and (b).

This application was filed on or after September 16, 2012. The person who signed the terminal disclaimer has failed to state his/her capacity to sign for the juristic entity, and he/she has not been established as being authorized to act on behalf of the applicant.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 21-40 stand rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 2, and 7 of U.S. Patent No. 8,063,434 B1. Although the claims at issue are not identical, they are not patentably distinct from each other because the examined application claims 21-40 is either anticipated by, or would have been obvious over claims 1, 2, and 7 of U.S. Patent No. 8,063,434 B1. It is known that silicon nitride is a component of silicon oxynitride or it is known as equivalent materials to substitute one for the other.

Claims 21-40 stand alternatively rejected on the ground of nonstatutory double patenting as being unpatentable over claims 3, 4, 6, and 14-16 of U.S. Patent No.

8,859,374 B1. Although the claims at issue are not identical, they are not patentably distinct from each other because the examined application claims 21-40 is either anticipated by, or would have been obvious over claims 3, 4, 6, and 14-16 of U.S. Patent No. 8,859,374 B1. It is known that silicon nitride is a component of silicon oxynitride or it is known as equivalent materials to substitute one for the other.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

October 5, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/605,231	01/26/2015	Krishnaswamy Ramkumar	PM07024CIP1C1	4843

60909 7590 12/17/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
12/17/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@cypress.com
pbj@cypress.com
pbjtmp2@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000843

Office Action Summary	Application No. 14/605,231	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/3/15*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-25,29-33,35-38 and 40-45* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21-25, 29-33, 35-38, 40-45* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 21-25, 29-33, 35-38, 40-45 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Claim Objections

Claims 29 is objected to because of the following informalities: Claim 29 is the same as claim 21. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-25, 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (U.S. Patent No. 7,450423) in view of Yan (U.S. Patent Publication No. 2008/0135946) and further in view of Ranade (U.S. Patent Publication No. 2008/0121932).

Referring to figures 1-3, Lai et al. teaches a memory device, comprising:

a tunnel oxide layer (called gate oxide, see col. 4, lines 34-37) overlying a channel (115) connecting a source and a drain (110/112) of the memory device (100) formed in a substrate (101);

a multi-layer charge storing layer (120/130) overlying the tunnel oxide layer (called gate oxide, see col. 4, lines 34-37), the multi-layer charge storing layer (120/130) comprising an oxygen-rich (120), first layer comprising a nitride (130) on the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free (130, see figure 1), and second layer comprising a Zirconium or Yttrium based high K dielectric (142) on the first layer in which a composition of the second layer results in it being trap dense (142, see figure 1); and

a blocking layer (144) overlying the multi-layer charge storing layer (120/130), the blocking layer (144, see figure 1).

Regarding to claims 25, wherein at least one of the first layer or the second layer of the multi-layer charge storing layer comprises silicon nitride or silicon oxy-nitride (120/130, see col. 9, lines 2-8).

Regarding to claim 42, the first layer is separated from the second layer by an anti-tunneling layer comprising an oxide (see col. 9, lines 9-26).

Regarding to claim 43, the blocking layer comprises a high-temperature-oxide (HTO) (see col. 8, lines 4-18, col. 9, lines 47-52).

However, the reference does not clearly teach the channel comprises polysilicon, recrystallized polysilicon or silicon nanowire.

Yan teaches forming channel comprise polysilicon (see paragraph# 32, meeting claim 21-23). The limitation "the channel comprising ***recrystallized*** polysilicon" in claim 21 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form polysilicon channel in Ramsbey et al. as taught by Yan because determining the optimum material for the layer only involved routine skill in the art to form a desired memory device.

Ranade teaches forming channel comprise a silicon nanowire (see figures 2a-2n, paragraph# 25, meeting claims 24).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form silicon nanowire channel in Ramsbey et al. as taught by Ranade because determining the optimum material for the layer only involved routine skill in the art to form a desired memory device.

Claims 29-33, 35-38, 40-41, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramsbey et al. (U.S. Patent No. 6,433,383) in view of Yan (U.S. Patent Publication No. 2008/0135946) and further in view of Ranade (U.S. Patent Publication No. 2008/0121932).

Regarding to claim 29, a memory device, comprising:

a tunnel oxide layer (15) overlying a channel connecting a source and a drain (13a/13b) of the memory device formed in a substrate (12);

a multi-layer charge storing layer (32/34) overlying the tunnel oxide layer (15), the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the

tunnel oxide layer in which a composition of the first layer results in it being substantially trap free (32, see figure 4c-7, col. 6, lines 35-55), and an oxygen-lean, silicon nitride second layer on the first layer in which a composition of the second layer results in it being trap dense (34, see figures 4c-7, col. 6, lines 56-67, col. 7, lines 1-5); and

a high-temperature-oxide (HTO) layer (36) overlying the multi-layer charge storing layer (32/34), the HTO layer comprising an oxidized silicon nitride with a thickness approximately in the range of 2-3 nanometers, and an oxide overlaying the oxidized silicon nitride (see col. 7, lines 6-22). The limitation "the HTO layer comprising an oxidized silicon nitride" in claim 29 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding to claim 35, a device comprising:

a vertical channel (between source/drain (13a/13b) extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region (13a/13b); and

an oxide-nitride-nitride-oxide (ONNO) stack (15/32/34/36) disposed about the vertical channel (between source/drain (13a/13b), the ONNO stack comprising:

a tunnel oxide layer (15) abutting the vertical channel (between source/drain (13a/13b);

a multi-layer charge storing layer (32/34) overlying the tunnel oxide layer (15), the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride abutting the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free (32, see figure 4c-7, col. 6, lines 35-55), and an oxygen-lean, silicon nitride second layer overlying the first layer in which a composition of the second layer results in it being trap dense (34, see figures 4c-7, col. 6, lines 56-67, col. 7, lines 1-5); and

a high-temperature-oxide (HTO) layer (36) overlying the multi-layer charge storing layer (32/34), the HTO layer comprising an oxidized silicon nitride with a thickness approximately in the range of 2-3 nanometers and an oxide overlaying the oxidized nitride (see col. 7, lines 6-22). The limitation “the HTO layer comprises an oxidized silicon nitride layer” in claim 35 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed

in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding to claims 33, wherein at least one of the first layer or the second layer of the multi-layer charge storing layer comprises silicon nitride or silicon oxy-nitride (32/34, see col. 6, lines 35 to col. 7, lines 5).

Regarding to claim 40, the first layer is separated from the second layer by an anti-tunneling layer comprising an oxide (32, see figure 4c-7, col. 6, lines 35-55, it is noted that layer 32 comprises oxide and oxynitride layer). Absent a showing of unexpected result, a change in sequence involves routine optimization of process of prior art and would have been obvious to one skilled in the art at the time the invention was made. A change in sequence/reversal of process steps is obvious under 35 USC 103 (exparte Rubin, 128 USPQ 440 (Bd. App. 1959)). See also in re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA).

Regarding to claim 41, 45, the HTO layer further comprises a nitride HTO layer overlying the oxide of the HTO layer (see col. 7, lines 6-22, it is noted that layer 32 comprises

oxide and oxynitride layer). Absent a showing of unexpected result, a change in sequence involves routine optimization of process of prior art and would have been obvious to one skilled in the art at the time the invention was made. A change in sequence/reversal of process steps is obvious under 35 USC 103 (exparte Rubin, 128 USPQ 440 (Bd. App. 1959)). See also in re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA).

However, the reference does not clearly teach the channel comprises polysilicon, recrystallized polysilicon or silicon nanowire.

Yan teaches forming channel comprise polysilicon (see paragraph# 32, meeting claim 30-31, 36-37). The limitation "the channel comprising recrystallized polysilicon" in claim 31 is taken to be a product by process limitation; it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form polysilicon channel in Ramsbey et al. as taught by Yan because determining the optimum material for the layer only involved routine skill in the art to form a desired memory device.

Ranade teaches forming channel comprise a silicon nanowire (see figures 2a-2n, paragraph# 25, meeting claims 32, 38).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form silicon nanowire channel in Ramsbey et al. as taught by Ranade because determining the optimum material for the layer only involved routine skill in the art to form a desired memory device.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van*

Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 21-25, 29-33, 35-38, 40-45 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-19 of U.S. Patent No. 8,633,537; 9,093,318. Although the claims at issue are not identical, they are not patentably distinct from each other because both the present invention and the patent teach a memory device, comprising: a tunnel oxide layer overlying a channel connecting a source and a drain of the memory device formed in a substrate; a multi-layer charge storing layer overlying the tunnel oxide layer, the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free, and

an oxygen-lean, second layer comprising a nitride on the first layer in which a composition of the second layer results in it being trap dense; and a high-temperature-oxide (HTO) layer overlying the multi-layer charge storing layer, the HTO layer comprising an oxidized portion of the second layer.

Therefore, the instant claims are within the scope to the cited prior art claims.

Response to Arguments

Applicant's arguments with respect to claims 21-25, 29-33, 35-38, 40-45 have been considered but are moot of new ground rejection.

Applicant contends that none of the reference teaches the second layer comprises "a Zirconium or Yttrium based high K dielectric material on the first layer in which a composition of the second layer results in it being trap dense. This is not found persuasive because Lai et al. clearly teaches second layer comprising a Zirconium or Yttrium based high K dielectric (142) on the first layer in which a composition of the second layer results in it being trap dense (142, see figure 1).

Applicant contends that none of the reference teaches oxygen-lean, silicon nitride second layer on the first layer in which a composition of the second layer results in it being trap dense; and a high-temperature-oxide (HTO) layer overlying the multi-layer charge storing layer, the HTO layer comprising an oxidized silicon nitride with a thickness approximately in the range of 2 to 3 nanometers, and an oxide overlaying the oxidized silicon nitride. This is not found persuasive because Ramsbey et al. teaches an oxygen-lean, silicon nitride second layer overlying

the first layer in which a composition of the second layer results in it being trap dense (34, see figures 4c-7, col. 6, lines 56-67, col. 7, lines 1-5); and a high-temperature-oxide (HTO) layer (36) overlying the multi-layer charge storing layer (32/34), the HTO layer comprising an oxidized silicon nitride with a thickness approximately in the range of 2-3 nanometers and an oxide overlaying the oxidized nitride (see col. 7, lines 6-22). The limitation "the HTO layer comprises an ***oxidized*** silicon nitride layer" in claim 35 is taken to be a product by process limitation; it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

60909 7590 03/13/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2893	

MAIL DATE	DELIVERY MODE
03/13/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Sandisk Technologies, Inc. - Ex. 1002, Page 000858

Office Action Summary	Application No.	Applicant(s)	
	13/539,458	RAMKUMAR ET AL.	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2012*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

Oath/Declaration filed on 7/19/12 has been considered.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned

with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-20 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 8,318,608 and claims 1-6 of U.S. Patent No. 8,283,261. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant invention and the patents teach a method of fabricating a memory device, comprising: subjecting a substrate to a first oxidation process to form a tunnel oxide layer overlying a channel connecting a source and a drain of the memory device formed in the substrate, wherein the channel comprises polysilicon; forming a multi-layer charge storing layer overlying the tunnel oxide layer, the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a stoichiometric composition of the first layer results in it being substantially trap free, and an oxygen-lean, second layer comprising a nitride on the first layer in which a stoichiometric composition of the second layer results in it being trap dense; and subjecting the substrate to a second oxidation process to consume a portion of the second layer and form a high-temperature-oxide (HTO) layer overlying the multi-layer charge storing layer.

.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

TTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

60909 7590 10/02/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2893	

NOTIFICATION DATE	DELIVERY MODE
10/02/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000863

Office Action Summary	Application No. 13/539,458	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/17/14*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *9/17/14*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-20 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 17-21, 23-28, 30-31 of copending Application No. 13/620071 Although the claims at issue are not identical, they are not patentably distinct from each other because the instant invention and the patents teach a method of fabricating a memory device, comprising: subjecting a substrate to a first oxidation process to form a tunnel oxide layer overlying a channel connecting a source and a drain of the memory device formed in the substrate, wherein the channel comprises polysilicon; forming a multi-layer charge storing layer overlying the tunnel oxide layer, the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a stoichiometric composition of the first layer results in it being substantially trap free, and an oxygen-lean, second layer comprising a nitride on the first layer in which a stoichiometric composition of the second layer results in it being trap dense; and subjecting the substrate to a second oxidation process to consume a portion of the second layer and form a high-temperature-oxide (HTO) layer overlying the multi-layer charge storing layer.

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

TTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/620,071	09/14/2012	Krishnaswamy Ramkumar	PM07024C2	7190

60909 7590 04/03/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2893	

NOTIFICATION DATE	DELIVERY MODE
04/03/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000868

Office Action Summary	Application No. 13/620,071	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/6/14*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *17-36* is/are pending in the application.

5a) Of the above claim(s) *32-36* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *17-31* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *6/13/13*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

Applicant's election of Species I, claims 17-31 in the reply filed on 1/6/14 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Claims 32-36 are withdrawn from further consideration by the examiner, 37 C.F.R. 1.142(b) as being drawn to a non-elected invention.

Information Disclosure Statement

The information disclosure statements filed 6/13/13 have been considered.

Oath/Declaration

Oath/Declaration filed on 6/20/13 has been considered.

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-18, 21, 23-24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. (U.S. Patent Publication No. 2007/0200168) in view of Nansei et al. (U.S. Patent Publication No. 2006/0228899).

Referring to figures 1A-8F, Ozawa et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising:

providing a substrate (10) in an oxidation chamber, wherein the substrate comprises a first exposed crystal plane and a second exposed crystal plane, and wherein the crystal orientation of the first exposed crystal plane is different from the crystal orientation of the second exposed crystal plane (see figures 6d-8f, paragraphs# 78-79); and

subjecting the substrate (10) to a radical oxidation process to form a first portion of a dielectric layer on the first exposed crystal plane and a second portion of the dielectric layer on the second exposed crystal plane, wherein the thickness of the first portion of the dielectric layer is approximately equal to the thickness of the second portion of the dielectric layer (11, see paragraphs# 80-84).

Regarding to claim 18, the radical oxidation process includes oxidizing with a radical selected from the group consisting of an OH radical, an HO_2 radical and an O diradical (see paragraphs# 80).

Regarding to claims 21, 26, the first exposed crystal plane and second exposed crystal plane extends above a top surface of isolation regions (41) formed on the substrate (10, see figures 6E-7A).

Regarding to claim 23, a method comprising:

subjecting a substrate (10) comprising a first exposed crystal plane and a second exposed crystal plane to a first radical oxidation process to form first dielectric layer (11, see paragraphs# 80-84) comprising a first portion on the first exposed crystal plane and a second portion on the second exposed crystal plane (see figures 6d-8f, paragraphs# 78-79);

forming a charge-trapping layer (12) above the first dielectric layer (11); and

forming a second dielectric layer (13) above the charge-trapping layer (12).

Regarding to claim 24, the crystal orientation of the first exposed crystal plane is different from the crystal orientation of the second exposed crystal plane (see figures 6d-8f, paragraphs# 78-79).

However, the reference does not clearly teach subjecting the charge-trapping layer to a second radical oxidation process consuming a portion of the charge-trapping layer to form a

second dielectric layer above the charge-trapping layer by oxidizing a portion of the charge-trapping layer.

Referring to figures 1-36, Nansei et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising: having a substrate (1/101/201/301) in a process chamber (see figure 14); subjecting, in a first process chamber (see figure 14), a substrate to a first radical oxidation process to form a first dielectric layer (21/62/203/302); subjecting, in the process chamber, the substrate to a deposition process to form a charge-trapping layer above the first dielectric layer (202/22/63/303); and subjecting, in the process chamber, the substrate to a second radical oxidation process to form a second dielectric layer above the charge-trapping layer by oxidizing a portion of the charge-trapping (64/70/23/30/304/204/105, meeting claim 23).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to subjecting the charge-trapping layer to a second radical oxidation process consuming a portion of the charge-trapping layer to form a second dielectric layer above the charge-trapping layer by oxidizing a portion of the charge-trapping layer in process of Ozawa et al. as taught by Nansei et al. because the process is known in the semiconductor art to provide a desired dielectric layer to form a high reliability and low cost memory device structure.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. (U.S. Patent Publication No. 2007/0200168) in view of Nansei et al. (U.S. Patent Publication

No. 2006/0228899) as applied to claims 17-18, 21, 23-24, 26 above and further in Wang (U.S. Patent No. 2005/0266637).

Ozawa et al. in view of Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach the radical oxidation process is carried out at a temperature approximately in the range of 950-1100 degrees Celsius at a pressure approximately in the range of 5 - 15 Torr (claim 19).

Wang teaches a method of forming a flash memories device forming radical oxidation processes are carried out at a temperature approximately in the range of 950-1100 degrees Celsius at a pressure approximately in the range of 5-15 Torr (see paragraph# 27).

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the temperature range, time range, thickness range and pressure of forming dielectric layers, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- the temperature range, time range, thickness range and pressure of forming dielectric layers), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- the temperature range, time range, thickness range and pressure of forming dielectric layers) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to forming radical oxidation at the specific temperature/pressure, annealing at a specific temperature/gas, and using LPCVD chamber to form layers for memory device in Ozawa et al. as taught by Wang because forming radical oxidation at the specific temperature/pressure to form layers for memory device is known in the semiconductor art to form conformal/desired layers for memory device.

Claims 20, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. (U.S. Patent Publication No. 2007/0200168) in view of Nansei et al. (U.S. Patent Publication No. 2006/0228899) as applied to claims 17-18, 21, 23-24, 26 above and further in Zhu et al. (U.S. Patent Publication No. 2006/0237803).

Ozawa et al. in view of Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach substrate with crystallographical orientation of <100> and <110>.

Zhu et al. teaches a semiconductor device having a substrate with crystallographical orientation of <100> and <110> (see paragraph# 39, meeting claims 20, 25).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a substrate with crystallographical orientation of <100> and <110> in Ozawa et al. as taught by Zhu et al. because forming a substrate with specific crystal orientation would increase performance of the device.

Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. (U.S. Patent Publication No. 2007/0200168) in view of Nansei et al. (U.S. Patent Publication No. 2006/0228899) as applied to claims 17-18, 21, 23-24, 26 above and further in Rathor et al. (U.S. Patent No. 6,818,558).

Ozawa et al. in view of Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion, and wherein oxidizing the portion of the charge-trapping layer of the top silicon-rich silicon oxy-nitride portion to form the second dielectric layer.

Rathor et al. teaches forming charge storing dielectric for SONOS-type device having multiple layers (see figures 7-8E) wherein the bottom portion (816, see col. 12, lines 26-33), the top layer (818/820, see col. 12, lines 49-67, col. 13, lines 1-15, meeting claims 27-28).

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the thickness range of forming dielectric layers, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- the thickness range of forming dielectric layers), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- the thickness range of forming dielectric layers) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a charge-trapping oxy-nitride film with a desired thickness in process of Ozawa et al. as taught by Rathor et al. because the process is known in the semiconductor art to form a SONOS type memory device structure comprising an oxy-nitride film with a desired thickness.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with

this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 17-31 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-6 of Patent No. 8,283,261. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the instant invention and the Patent teaches oxidizing a portion of a charge-trapping layer disposed above a substrate to form a blocking dielectric layer above the charge-trapping layer, the oxidizing performed by exposing the charge-trapping layer to a hydrogen and oxygen radical oxidation process, wherein the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer. Or subjecting a substrate to an oxidation process to form a first dielectric layer; depositing a charge-trapping layer above the first dielectric layer, the charge-trapping layer comprising a bottom portion and a top portion; and subjecting the charge-trapping layer to a radical oxidation process to form a second dielectric layer above the charge-trapping layer by

exposing the charge-trapping layer to a hydrogen (H.sub.2) and oxygen (O.sub.2) gas flow, forming radicals at a surface of the charge-trapping layer, and

consuming a portion of the top portion of the charge-trapping layer to form the second dielectric layer, wherein the bottom portion of the charge-trapping layer comprises an oxygen-rich silicon oxy-nitride.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

TTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/620,071	09/14/2012	Krishnaswamy Ramkumar	PM07024C2	7190

60909 7590 07/18/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
07/18/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000880

Office Action Summary	Application No. 13/620,071	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/22/14*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *17-21,23-28 and 30-36* is/are pending in the application.

5a) Of the above claim(s) *32-36* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *17-21,23-28,30 and 31* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 17-21, 23-28, 30-31 have been considered but are moot of new ground rejection.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 17-21, 23-28, 30-31 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 8,318,608, claims 3-6 of U.S. Patent No. 8,283,261, and claims 1-15 of U.S. Application No. 13/539,458 (2013/0309826). Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant invention and the patents teach A method of fabricating a nonvolatile charge trap memory device, comprising: providing a substrate in an oxidation chamber, wherein the substrate comprises a first exposed crystal plane and a second exposed crystal plane, and wherein the crystal orientation of the first exposed crystal plane is different from the crystal orientation of the second exposed crystal plane; and subjecting the substrate to a radical oxidation process to form a first portion of a dielectric layer on the first exposed crystal plane and a second portion of the dielectric layer on the second exposed crystal plane, wherein the thickness of the first portion of the dielectric layer is approximately equal to the thickness of the second portion of the dielectric layer, wherein the radical oxidation process comprises flowing hydrogen (H_2) and oxygen (O_2) gas into the oxidation chamber, forming radicals at a surface of the first exposed crystal plane and second exposed crystal plane without

an ignition event to pyrolyze the H_2 and O_2 and consuming portions of the first exposed crystal plane and second exposed crystal plane, to form the dielectric layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

TTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

60909 7590 01/18/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2893	

MAIL DATE	DELIVERY MODE
01/18/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/124,855	RAMKUMAR, KRISHNASWAMY	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/22/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/12/10 has been entered.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re

Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 5, 12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-19 of copending Application No. 12/197466 (2008/0293255). Although the conflicting claims are not identical, they are not patentably distinct from each other because both the instant invention and the copending application teaches oxidizing a portion of a charge-trapping layer disposed above a substrate to form a blocking dielectric layer above the charge-trapping layer, the oxidizing performed by exposing the charge-trapping layer to a hydrogen and oxygen radical oxidation process, wherein the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau, can be reached on (571) 272-1945. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

TTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

60909 7590 08/16/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2893	

MAIL DATE	DELIVERY MODE
08/16/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/124,855	RAMKUMAR, KRISHNASWAMY	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/29/11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/29/11 has been entered.

Information Disclosure Statement

The information disclosure statement filed 7/29/11 has been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) in view of Lee et al. (U.S. Patent No. 6,365,518), and further in view of Rathor et al. (U.S. Patent No. 6,818,558).

Referring to figures 1-36, Nansei et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising:

Subjecting in a process chamber, a substrate to a first hydrogen and oxygen radical oxidation process to form a first dielectric layer (see paragraph# 66)

subjecting, in a first process chamber (see figure 14), a substrate to a first radical oxidation process to form a first dielectric layer (21/62/203/302);

subjecting, in the process chamber, the substrate to (see paragraph # 66); and

subjecting, in the process chamber, the substrate to a hydrogen and oxygen radical oxidation process to form a second dielectric layer above the charge trapping layer (see para.# 66) by oxidizing a portion of the charge-trapping (64/70/23/30/304/204/105), wherein the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (see paragraphs# 65, 68-69).

Nansei et al teaches forming the layers in the cluster tool. However, the reference does not clearly teach using hydrogen and oxygen to oxidize the silicon nitride film and forming the layers in different chamber of cluster tool.

Nansei et al. in paragraph# 66 teaches oxidizing process by mixing the hydrogen and oxygen radical oxidation.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would oxidize the silicon nitride film by using hydrogen and oxygen in process of Nansei et al. because oxidizing in hydrogen and oxygen would provide higher oxidation rate.

Lee et al. teaches cluster tool includes more than one processing chamber and transfer chamber (see col. 1, lines 54-67).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would recognize the cluster tool have more than one processing chamber as taught by Lee et al. in process of Nansei et al. because the process is known in the semiconductor art to reduce processing time with evacuating and re-pressurizing different processing chamber.

However, the reference does not teach the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5-3.5 nanometers and a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9-10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the second dielectric layer having a thickness approximately in the range of 3.5-4.5 nanometers (claim 5, 12).

Rathor et al. teaches forming charge storing dielectric for SONOS-type device having multiple layers (see figures 7-8E) wherein the bottom portion (816, see col. 12, lines 26-33), the top layer (818/820, see col. 12, lines 49-67, col. 13, lines 1-15).

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the thickness range of forming dielectric layers, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- the thickness range of forming dielectric layers), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- the thickness range of forming dielectric layers) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a charge-trapping oxy-nitride film with a desired thickness in process of Nansei et al. as taught by Rathor et al. because the process is known in the semiconductor art to form a SONOS type memory device structure comprising an oxy-nitride film with a desired thickness.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined

application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 5, 12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-16 of copending Application No. 12/197,466. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the instant invention and the copending application teaches oxidizing a portion of a charge-trapping layer disposed above a substrate to form a blocking dielectric layer above the charge-trapping layer, the oxidizing performed by exposing the charge-trapping layer to a hydrogen and oxygen radical oxidation process, wherein the

charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5 - 3.5 nanometers and a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9 - 10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer having a thickness approximately in the range of 3.5 - 4.5 nanometers.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

TTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM2007024	3433

60909 7590 10/29/2009

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
10/29/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/124,855	RAMKUMAR, KRISHNASWAMY	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/21/08*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/21/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed on 10/21/08 has been considered.

Oath/Declaration

Oath/Declaration filed on 5/21/08 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4, 7-11, 14-15, 17 are rejected under 35 U.S.C. 102(b/e) as being anticipated by Nansei et al. (U.S. Patent Publication No. 2006/0228899).

Referring to figures 1-36, Nansei et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising:

Providing a substrate (1/101/201/301) having a charge-trapping layer (202/22/63/303) disposed thereon; and

Oxidizing, by exposing the charge-trapping layer (202/22/63/303) to a radical oxidation process, a portion of the charge-trapping layer to form a blocking dielectric layer above the charge-trapping layer (64/70/23/30/304/204/105); and

Depositing a gate layer above the second dielectric layer (8/33).

Regarding to claim 2, wherein both the first and the second radical oxidation processes include oxidizing with a radical selected from the group consisting of an OH radical, an HO.sub.2 radical and an O diradical (see paragraph# 66).

Regarding to claim 4, wherein the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (see paragraphs# 65, 68-69).

Regarding to claims 7, 14, wherein the nonvolatile charge trap memory device is a SONOS-type device, wherein the first dielectric layer is a tunnel dielectric layer, and wherein the second dielectric layer is a blocking dielectric layer (see paragraphs# 152, 164-166).

Regarding to claim 8, a method of fabricating a nonvolatile charge trap memory device, comprising:

Providing a substrate (1/101/201/301) in a process chamber (see figure 14);

subjecting, in a first process chamber (see figure 14), a substrate to a first radical oxidation process to form a first dielectric layer (21/62/203/302);

subjecting, in the process chamber, the substrate to a deposition process to form a charge-trapping layer above the first dielectric layer (202/22/63/303); and

subjecting, in the process chamber, the substrate to a second radical oxidation process to form a second dielectric layer above the charge-trapping layer by oxidizing a portion of the charge-trapping (64/70/23/30/304/204/105).

Regarding to claim 9, wherein both the first and the second radical oxidation processes include oxidizing with a radical selected from the group consisting of an OH radical, an HO.sub.2 radical and an O diradical (see paragraph# 66).

Regarding to claim 10, wherein the first dielectric layer, the charge-trapping layer and the second dielectric layer are formed without breaking vacuum in the cluster tool.

Regarding to claim 11, wherein the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (see paragraphs# 65, 68-69).

Regarding to claim 15, subjecting the substrate to the deposition process to form the charge-trapping layer (202/22/63/303) includes using a gas selected from the group consisting of dichlorosilane (H.sub.2SiCl.sub.2), bis-(tert-butylamino)silane (BTBAS), ammonia (NH.sub.3) and nitrous oxide (N.sub.2O) (see paragraph# 166).

Regarding to claim 17, a radical oxidation method, comprising:

Providing a substrate (1/101/201/301) in a process chamber (see figure 14);

Mixing, in the process chamber, hydrogen gas and oxygen gas without subjecting the hydrogen gas and oxygen gas to a combustion process (see paragraph# 66); and

Oxidizing, in the process chamber, a portion of the substrate with radicals generated from the mixing of the hydrogen gas and oxygen gas (see paragraph# 66).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 6, 13, 16, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) as applied to claims 1-2, 4, 7-11, 14-15, 17 above in view of Wang (U.S. Patent No. 2005/0266637).

Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach radical oxidation processes are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-15 Torr (claims 3, 10, 18), annealing the blocking dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N.sub.2), nitrous oxide (N.sub.2O), nitrogen dioxide (NO.sub.2), nitric oxide (NO) and ammonia (NH.sub.3) at a temperature approximately in the range of 700-800 degrees Celsius (claim 6, 13), the hydrogen gas and oxygen gas are mixed in an approximate ratio of 1:1 (claim 19), the process chamber is a low-pressure chemical vapor deposition chamber (claim 16, 20).

Wang teaches a method of forming a flash memories device forming radical oxidation processes are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-15 Torr (see paragraph# 27), annealing the blocking dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N.sub.2), nitrous oxide (N.sub.2O), nitrogen dioxide (NO.sub.2), nitric oxide (NO) and ammonia (NH.sub.3) at a temperature approximately in the range of 700-800 degrees Celsius (see paragraph# 21), the hydrogen gas and oxygen gas are mixed in an approximate ratio of 1:1 (see paragraph# 27), the process chamber is a low-pressure chemical vapor deposition chamber (see paragraph# 7).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to forming radical oxidation at the specific temperature/pressure, annealing at a specific temperature/gas, and using LPCVD chamber to form layers for memory device in Nansei et al. as taught by Wang because forming radical oxidation at the specific temperature/pressure, annealing at a specific temperature/gas, and using LPCVD chamber to form layers for memory device is known in the semiconductor art to form conformal/desired layers for memory device.

Claims 5, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) as applied to claims 1-2, 4, 7-11, 14-15, 17 above in view of Rathor et al. (U.S. Patent No. 6,818,558).

Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5-3.5 nanometers and a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9-10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the second dielectric layer having a thickness approximately in the range of 3.5-4.5 nanometers (claim 5, 12).

Rathor et al. teaches forming charge storing dielectric for SONOS-type device having multiple layers (see figures 7-8E) wherein the bottom portion (816, see col. 12, lines 26-33), the top layer (818/820, see col. 12, lines 49-67, col. 13, lines 1-15).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a charge-trapping oxy-nitride film with a desired thickness in process of Nansei et al. as taught by Rathor et al. because the process is known in the semiconductor art to form a SONOS type memory device structure comprising an oxy-nitride film with a desired thickness.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau, can be reached on (571) 272-1945. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM07027	5484

60909 7590 03/09/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	
ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
03/09/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/152,518	POLISHCHUK ET AL.	
	Examiner	Art Unit	
	Ngan Ngo	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-15 and 21-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-27* is/are allowed.

6)☒ Claim(s) *1-5,8-15,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The amendment filed December 28, 2010 has been entered and made of record as paper no. 20101228.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8-15, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nomoto et al (US 6,906,390 B2) in view of Zheng et al (6,912,163 B2, of record).

Nomoto discloses in figures 2-3H a non-volatile memory transistor comprising: an oxide-nitride-oxide (BTM, CS, and TOP) dielectric stack on a surface of a semiconductor substrate, the 0N0 dielectric stack comprising a multi-layer charge storage layer including a substantially trap free bottom silicon oxynitride layer (CS1) and a charge trapping top silicon oxynitride layer (CS2); and a gate electrode (G) formed of doped polysilicon over a surface of the 0N0 dielectric stack. Note lines 9-13, column 7 of Nomoto. Zheng teaches that gate electrode formed of doped polysilicon is high work function gate electrode. Therefore it would have been obvious to one of ordinary skill in the art that the gate electrode in Nomoto is a high work function gate electrode.

Claims 23-27 are allowed.

Applicant's arguments with respect to claims 1-5, 8-15, 21, and 22 have been considered but are moot in view of the new ground(s) of rejection.

The other references are cited to show other structures pertinent to Applicants' disclosure.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

March 9, 2011

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM2007027	5484

60909 7590 09/29/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	
ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
09/29/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Sandisk Technologies, Inc. - Ex. 1002, Page 000912

Office Action Summary	Application No.	Applicant(s)	
	12/152,518	POLISHCHUK ET AL.	
	Examiner	Art Unit	
	Ngan Ngo	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20081121*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The election filed July 9, 2010 has been entered and made of record as paper no. 20100709.

Applicant's election without traverse of claims 1-15 in the reply filed on July 9, 2010 is acknowledged.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Zheng et al (US 6,912,163 B2).

Zheng discloses a non-volatile memory transistor comprising: an oxide-nitride-oxide (18) dielectric stack on a surface of a semiconductor substrate; and high work function gate electrode (34) formed over a surface of the ONO dielectric stack.

In re claim 2, the high work function gate electrode in Zheng comprises a doped polysilicon layer.

In re claim 3, the transistor in Zheng is a SONOS memory transistor.

In re claim 4, the doped polysilicon layer in Zheng comprises a P+ dopant to form an NMOS SONOS memory transistor. Note line 33, column 9 of Zheng.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zheng et al (US 6,912,163 B2) in view of Wang et al (US 2007/0272916 A1) and Lue et al (US 2007/0268753 A1).

Zheng discloses all of the subject matter discussed above. Wang further teaches that the charge storing layer can be formed of multi-layer of oxynitrides. Note paragraph [0024]. Lue further discloses in figure 31 memory transistors and logic transistors including gate oxide and high work function gate electrodes formed on the same substrate. Therefore it would have been obvious to one of ordinary skill in the art to use the teachings of Zheng, Wang, and Lue to form the claimed device.

The other references are cited to show other structures pertinent to Applicant's disclosure.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

September 27, 2010

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/197,466	08/25/2008	Krishnaswamy Ramkumar	PM07024C1	2398

60909 7590 06/01/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	
MAIL DATE	DELIVERY MODE
06/01/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/197,466	RAMKUMAR ET AL.	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *17-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/21/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species 1 claims 1-19, figures 5-6 in the reply filed on 4/19/11. This is not found persuasive because claims 1-16 belongs to species 1, figures 5-6, while claims 17-19 belongs to species 2, figures 7a-7b. Therefore, claims 17-19 are withdrawn from consideration.

Information Disclosure Statement

The information disclosure statement filed 10/21/08 has been considered.

Oath/Declaration

Oath/Declaration filed on 9/17/08 has been considered.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4, 7, 10-12, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) in view of Lee et al. (U.S. Patent No. 6,365,518).

Referring to figures 1-36, Nansei et al. teaches a method of fabricating a nonvolatile charge trap memory device, comprising:

Providing a substrate (1/101/201/301) in a process chamber (see figure 14);

subjecting, in a first process chamber (see figure 14), a substrate to a first radical oxidation process to form a first dielectric layer (21/62/203/302);

subjecting, in the process chamber, the substrate to a deposition process to form a charge-trapping layer above the first dielectric layer (202/22/63/303); and

subjecting, in the process chamber, the substrate to a second radical oxidation process to form a second dielectric layer above the charge-trapping layer by oxidizing a portion of the charge-trapping (64/70/23/30/304/204/105).

Regarding to claims 2, 12, wherein both the first and the second radical oxidation processes include oxidizing with a radical selected from the group consisting of an OH radical, an HO.sub.2 radical and an O diradical (see paragraph# 66).

Regarding to claim 4, wherein the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (see paragraphs# 65, 68-69).

Regarding to claims 7, 16, wherein the nonvolatile charge trap memory device is a SONOS-type device, wherein the first dielectric layer is a tunnel dielectric layer, and wherein the second dielectric layer is a blocking dielectric layer (see paragraphs# 152, 164-166).

Regarding to claim 8, subjecting the substrate to the deposition process to form the charge-trapping layer (202/22/63/303) includes using a gas selected from the group consisting of dichlorosilane (H.sub.2SiCl.sub.2), bis-(tert-butylamino)silane (BTBAS), ammonia (NH.sub.3) and nitrous oxide (N.sub.2O) (see paragraph# 166).

Regarding to claim 11, wherein the charge-trapping layer comprises a material selected from the group consisting of silicon nitride, silicon oxy-nitride, oxygen-rich silicon oxy-nitride and silicon-rich silicon oxy-nitride, and wherein the second dielectric layer comprises silicon dioxide (see paragraphs# 65, 68-69).

Nansei et al teaches forming the layers in the cluster tool. However, the reference does not clearly teach using hydrogen and oxygen to oxidize the silicon nitride film and forming the layers in different chamber of cluster tool.

Nansei et al. in paragraph# 66 teaches oxidizing process by mixing the hydrogen and oxygen radical oxidation.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would oxidize the silicon nitride film by using hydrogen and

oxygen in process of Nansei et al. because oxidizing in hydrogen and oxygen would provide higher oxidation rate.

Lee et al. teaches cluster tool includes more than one processing chamber and transfer chamber (see col. 1, lines 54-67).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would recognize the cluster tool have more than one processing chamber as taught by Lee et al. in process of Nansei et al. because the process is known in the semiconductor art to reduce processing time with evacuating and re-pressurizing different processing chamber.

Claims 3, 6, 8-9, 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) in view of Lee et al. (U.S. Patent No. 6,365,518) as applied to claims 1-2, 4, 7, 10-12, 16 above in view of Wang (U.S. Patent No. 2005/0266637).

Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach radical oxidation processes are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-15 Torr (claims 3), annealing the blocking dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N.sub.2), nitrous oxide (N.sub.2O), nitrogen dioxide (NO.sub.2), nitric oxide (NO) and ammonia (NH.sub.3) at a temperature approximately in the range of 700-1100 degrees Celsius (claim 6, 13), the process chamber is a low-pressure chemical vapor deposition chamber (claim 9).

Wang teaches a method of forming a flash memories device forming radical oxidation processes are carried out at a temperature approximately in the range of 700-800 degrees Celsius at a pressure approximately in the range of 0.5-15 Torr (see paragraph# 27), annealing the blocking dielectric layer in an atmosphere comprising a gas selected from the group consisting of nitrogen (N.sub.2), nitrous oxide (N.sub.2O), nitrogen dioxide (NO.sub.2), nitric oxide (NO) and ammonia (NH.sub.3) at a temperature approximately in the range of 700-800 degrees Celsius (see paragraph# 21), the hydrogen gas and oxygen gas are mixed in an approximate ratio of 1:1 (see paragraph# 27), the process chamber is a low-pressure chemical vapor deposition chamber (see paragraph# 7).

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the temperature range, time range, thickness range and pressure of forming dielectric layers, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- the temperature range, time range, thickness range and pressure of forming dielectric layers), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- the temperature range, time range, thickness range and pressure of forming dielectric layers) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to forming radical oxidation at the specific temperature/pressure, annealing at a specific temperature/gas, and using LPCVD chamber to form layers for memory device in Nansei et al. as taught by Wang because forming radical oxidation at the specific temperature/pressure, annealing at a specific temperature/gas, and using LPCVD chamber to form layers for memory device is known in the semiconductor art to form conformal/desired layers for memory device.

Claims 5, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nansei et al. (U.S. Patent Publication No. 2006/0228899) in view of Lee et al. (U.S. Patent No. 6,365,518) as applied to claims 1-2, 4, 7, 10-12, 16 above in view of Rathor et al. (U.S. Patent No. 6,818,558).

Nansei et al. teaches a method of forming SONOS having a ONO stack. However, the reference does not teach the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5-3.5 nanometers and a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9-10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the second dielectric layer having a thickness approximately in the range of 3.5-4.5 nanometers (claim 5, 12).

Rathor et al. teaches forming charge storing dielectric for SONOS-type device having multiple layers (see figures 7-8E) wherein the bottom portion (816, see col. 12, lines 26-33), the top layer (818/820, see col. 12, lines 49-67, col. 13, lines 1-15).

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the thickness range of forming dielectric layers, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- the thickness range of forming dielectric layers), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- the thickness range of forming dielectric layers) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a charge-trapping oxy-nitride film with a desired thickness in process of Nansei et al. as taught by Rathor et al. because the process is known in the semiconductor art to form a SONOS type memory device structure comprising an oxy-nitride film with a desired thickness.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined

application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-16 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 5, 12 of copending Application No. 12/124,855. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the instant invention and the copending application teaches oxidizing a portion of a charge-trapping layer disposed above a substrate to form a blocking dielectric layer above the charge-trapping layer, the oxidizing performed by exposing the charge-trapping layer to a hydrogen and oxygen radical oxidation process, wherein the charge-trapping

layer comprises a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau, can be reached on (571) 272-1945. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

TTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

60909 7590 06/19/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	
ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
06/19/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000928

Office Action Summary	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6-9-14*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *16 and 19-34* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *21-34* is/are allowed.

7)☒ Claim(s) *16 and 19* is/are rejected.

8)☒ Claim(s) *20* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *20140609*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16 and 19 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Roizin et al (US 2005/0186741 A1, cited by Applicants).

Roizin discloses in figure 13 a method of forming a semiconductor device comprising: forming an oxide-nitride-oxide (ONO, 261,262,263) dielectric stack on a surface of a semiconductor substrate (210) in at least a first region (202) in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer; forming an oxide layer (263) on the surface of the substrate in a second region (201) in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and forming a doped polysilicon layer (1301) on the surface of a ONO dielectric stack and on a surface of the oxide laver of the MOS logic transistor to form a first high work function gate electrode on the surface of the ONO dielectric stack while concurrently forming a second high work function gate electrode on the oxide laver of the MOS logic transistor. See paragraphs [0029] and [0053]

In re claim 19, Roizin teaches the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, the doped polysilicon layer comprises a P+ dopant, and wherein the method further comprises patterning the doped

polysilicon layer, the ONO dielectric stack and the oxide layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 21-34 stand allowed.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

June 16, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

60909 7590 12/05/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	
ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
12/05/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000933

Office Action Summary	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *16-34* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *21-34* is/are allowed.

7)☒ Claim(s) *16-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *20120801*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Lue et al (US 2008/0291726 A1).

Lue discloses a method of forming a semiconductor device comprising: forming an ONO (120, 130, 140) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer; forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (GATE OXIDE as shown in figure 31) transistor is to be formed; and forming a high work function gate electrode on a surface of the ONO dielectric stack. Note the teachings of high work function gate in paragraph [0095] of Lue. It would have been obvious to one of ordinary skill in the art that the BLTs can be used as logic transistor.

In re claim 20, Lue teaches oxynitride layers in paragraph [0082].

Claims 21-34 are allowed.

The other references are cited to show other structures pertinent to Applicants' disclosure.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

December 2, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

60909 7590 09/28/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	
ART UNIT	PAPER NUMBER
2893	
MAIL DATE	DELIVERY MODE
09/28/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	13/539,466	POLISHCHUK ET AL.	
	Examiner	Art Unit	
	NIKOLAY YUSHIN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2012*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *11-20* is/are allowed.

7)☒ Claim(s) *1-5* is/are rejected.

8)☒ Claim(s) *6-10* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy et al., US 2009/0179253, in view of Zheng et al., US 6,912,163 and in view of Yan, US 2008/0135946.

In re Claim 1, Levy discloses a semiconductor device comprising: a memory transistor (Fig. 2) including: a channel 212 region electrically connecting a source region (210, left) and a drain region (210, right) formed in a substrate 108; an oxide-nitride-nitride-oxide (ONNO) stack 202 disposed above the channel region 212, the ONNO stack 204 comprising a multi-layer charge-trapping region (216, 220B, 220A) including an oxygen-rich first nitride layer 220B and an oxygen-lean second nitride layer 220A disposed above the first nitride layer 220B; and a gate electrode 214 formed over a surface of the ONNO stack 202 (Fig. 2; [0021-0030]).

Levy does not disclose that the gate electrode is high work function, as well as that the channel region comprising polysilicon.

Zheng teaches that N^+ -polysilicon and P^+ - polysilicon are high work function electrodes (column 5, lines 52-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Levy's polysilicon gate electrode 214 with Zheng's N^+ -polysilicon or P^+ - polysilicon electrode, to improve dielectric charge trapping memory devices as taught by Zheng (column 2, line 39).

However, Levy taken with Zhang does not teach that the channel region comprises polysilicon.

Yan teaches a semiconductor device comprising: a memory transistor (Fig. 1) wherein the channel region 220 comprises polysilicon ([0030-0036]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Levy's silicon channel 212 with Yan's polysilicon channel 220, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416* (See MPEP2144.07).

In re Claim 3, Levy taken with Zhang and Yan discloses the semiconductor device of claim 1, wherein the channel region comprises polysilicon (Yan: [0030-0036]).

The applicant's claim 3 does not distinguish over the Levy-Zhang -Yan references regardless of the process used to form polysilicon, because only the final product is relevant, not the recited process of recrystallization. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78

USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

The Federal Circuit recently revisited the question of whether a "product by process" claim can be anticipated by a reference that does not recite said process. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d at 1100. The Federal Circuit cited with approval this Office's current statement of the law, found in MPEP § 2113:

> [Even] though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.

Id. at 1101. The Federal Circuit held this statement to be consistent with its own views on this topic, as well as various Supreme Court rulings, notably *Gen. Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938) ("Although in some instances a claim may validly describe a

new product with some reference to the method of production, a patentee who does not distinguish his product from what is old except by reference, express or constructive, to the process by which he produced it, cannot secure a monopoly on the product by whatever means produced."). Id.

In re Claim 4, Levy taken with Zhang and Yan discloses the semiconductor device of claim 3, the high work function gate electrode comprises a P+ doped polysilicon layer (Zheng: column 5, lines 52-63).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, Zhang, and Yan as applied to claim 1 above, and further in view of Huerta et al., WO 2008/129478 (cited in this Office Action as US 2010/0117138).

In re Claim 2, Levy taken with Zhang and Yan discloses all limitations of claim 2, except for that the channel comprises a silicon nanowire.

Huerta teaches the semiconductor device wherein the channel comprises a silicon nanowire ([0030]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Levy-Zhang -Yan's silicon / polysilicon channel with Huerta's silicon nonowire, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416* (See MPEP2144.07).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, Zhang, and Yan as applied to claim 4 above, and further in view of Goebel et al., US 2003/0169629.

In re Claim 5, over Levy taken with Zhang and Yan discloses all limitations of claim 5 including that the ONNO stack 202 (Levy: Fig. 2) further includes a blocking dielectric layer 218 disposed above the multi-layer charge-trapping region (216, 220B, 220A) (Levy: Fig. 2; [0021-0030]) and wherein the blocking dielectric layer comprises a dielectric comprises a High Temperature Oxide (HTO) (Levy: [0030]), except for that the blocking dielectric layer comprises a dielectric comprises a **high K** High Temperature Oxide (HTO).

Goebel teaches the dielectric layer comprises a dielectric comprises a high K High Temperature Oxide, such as zirconium oxide, tantalum oxide, hafnium oxide ([0103]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Levy-Zhang -Yan's silicon oxide blocking dielectric layer 218 with Goebel's zirconium oxide, tantalum oxide, or hafnium oxide, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416* (See MPEP2144.07).

Allowable Subject Matter

Claims 6 -10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11-20 are allowed.

The following is an examiner's statement of reasons for allowance:

In re Claim 11, prior-art fails to disclose semiconductor device comprising: a memory transistor including "an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer." Therefore, the claimed differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 18, prior-art fails to disclose semiconductor device comprising: a memory transistor including "a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region; a tunnel dielectric layer abutting the vertical channel." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Jenne et al., US 8,222,688 (filed on 04/26/2010) discloses all limitations of claim 11 except for that the channel region comprising polysilicon, but this prior-art cannot be used in §103 rejection, because it is §102(e) reference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Thursday from 8 a.m. to 5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/159,315	01/20/2014	Igor Polishchuk	PM07027D1CIP1C1	1041

60909 7590 10/21/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	
ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
10/21/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000946

Office Action Summary	Application No. 14/159,315	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/20/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-40* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21-40* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☒ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *01/20/2014* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *09/30/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the claims that are directed to the same invention so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 21-40 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-16 of prior U.S. Patent No. 8,633,537. This is a statutory double patenting rejection.

In re Claim 21, claims 1, 3, 4, 5, and 7 of US 8,633,537 discloses a semiconductor device comprising: a memory transistor including: a channel region electrically connecting a source region and a drain region, the channel region comprising polysilicon; an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer; and a gate electrode (column 19, lines 43-54) comprising doped polysilicon (claims 3, 4, and 5) formed over a surface of the ONNO

stack (column 19, lines 54-55); and a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a gate electrode (column 19, lines 56-58) comprising doped polysilicon (claim 6, column 20, lines 10-12).

Claims 21-30 are rejected as being dependent on the rejected claim 21.

\In re Claim 31, claim 7 of US 8,633,537 discloses a semiconductor device comprising: a memory transistor including: a channel region electrically connecting a source region and a drain region, the channel region comprising polysilicon; an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer; and a gate electrode comprising doped polysilicon formed over a surface of the ONNO stack, wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer (column 20, lines 23-39).

Claims 32-34 are rejected as being dependent on the rejected claim 31.

In re Claim 35, claim 17 of US 8,633,537 discloses a semiconductor device comprising (column 21, line 11): a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region (column 21, lines 13-18); an oxide-nitride-nitride-oxide (ONNO) stack disposed about the vertical channel, the ONNO stack comprising (column 21, lines 19-20): a tunnel dielectric layer abutting the vertical channel; a charge-trapping region overlying the tunnel dielectric layer; and a blocking dielectric layer overlying the charge-trapping region; and a gate

electrode disposed about the ONNO stack, abutting the blocking dielectric layer (column 22, lines 1-9).

Claims 36-40 are rejected as being dependent on the rejected claim 35.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the memory transistor is at least partially formed within a substrate" while "the MOS logic transistor is formed in a layer overlying the substrate" must be shown or the feature(s) canceled from the claim 26. In addition, the "the memory transistor is formed in a layer overlying a substrate" while "the MOS logic transistor is at least partially formed within the substrate" must be shown or the feature(s) canceled from the claim 28. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 21 is objected to because of the following informalities: Claim 21 recites the limitation " **the** first nitride layer" in line 8. There is insufficient antecedent basis for this limitation in the claim. For purposes of a prompt examination the examiner reads claim 21 as the following:

"21. A semiconductor device comprising: a memory transistor including: a channel region electrically connecting a source region and a drain region, the channel region comprising polysilicon; an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the oxygen-rich first nitride layer; and a gate electrode comprising doped polysilicon formed over a surface of the ONNO stack; and a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a gate electrode comprising doped polysilicon."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 21-34 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 21 recites the limitation " **the** first nitride layer" in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claims 22-30 are rejected as being dependent on the rejected claim 21.

Claim 31 recites the limitations " the first nitride layer" and "the second nitride layer" in lines 7 and 10. There is insufficient antecedent basis for this limitation in the claim. Only "an **oxygen-rich** first nitride layer and an **oxygen-lean** second nitride layer" have been mentioned before.

Claims 32-34 are rejected as being dependent on the rejected claim 31.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 21, 24, and 25 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hagemeyer et al., US 2006/0008959 (corresponding to US 7,713,810), in view of Levy et al., US2009/0179253 (listed in IDS filed on 09/30/2014), and in view of Yan, US 2008/0135946 (listed in IDS filed on 09/30/2014).

In re Claim 21, Hagemeyer discloses a semiconductor device 221 (Fig. 2J) comprising: a memory transistor (a right-hand region) including: a channel region (between a left 219 and a right 219 in right-hand region) electrically connecting a source region (a left 222 in the right-hand region) and a drain region (a right 222 in right-hand region), a gate electrode 208 comprising doped polysilicon formed over a surface of the stack ((207,204) in the right-hand portion); and a metal oxide semiconductor (MOS) logic transistor (a left-hand region) including a gate oxide 207 and a gate electrode 208 comprising doped polysilicon (Fig. 2J; [0085], [0100-0105]).

Hagemeyer does not discloses that the channel region comprising polysilicon; an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the oxygen-rich first nitride layer; and a gate electrode comprising doped polysilicon formed over a surface of the ONNO stack.

The only difference between the Applicants' claim 21 and Hagemeyer's reference is in the specified structure of the memory transistor.

Levy teaches a semiconductor device comprising: a memory transistor (Fig. 2) including: a channel 212 region electrically connecting a source region (210, left) and a drain region (210, right) formed in a substrate 108; an oxide-nitride-nitride-oxide (ONNO) stack 202 disposed above the channel region 212, the ONNO stack 204 comprising a multi-layer charge-trapping region (216, 220B, 220A) including an oxygen-rich first nitride layer 220B and an oxygen-lean second nitride layer 220A disposed above the oxygen-rich first nitride layer 220B; and a gate electrode 214 formed over a surface of the ONNO stack 202 (Fig. 2; [0018-0030]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Hagemeyer's memory transistor with Levy's memory transistor, for improving device speed, increasing data retention, and extending the operating life of the device as taught by Levy ([0018]).

However, Hagemeyer taken with Levy does not teach that the channel region comprises polysilicon.

Yan teaches a semiconductor device comprising: a memory transistor (Fig. 1) wherein the channel region 220 comprises polysilicon ([0030-0036]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Hagemeyer-Levy's silicon channel with Yan's polysilicon channel, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416* (See MPEP2144.07).

In re Claim 24, Hagemeyer taken with Levy and Yan discloses the semiconductor device of claim 21, wherein the memory transistor (right-hand portion) (Hagemeyer's Fig. 2J) is at least partially formed within a substrate 201(Hagemeyer: Fig. 2J, [0104]).

In re Claim 25, Hagemeyer taken with Levy and Yan discloses the semiconductor device of claim 24, wherein the MOS logic transistor (left-hand portion) (Hagemeyer's Fig. 2J) is at least partially formed within the substrate 201(Hagemeyer: Fig. 2J, [0104]).

Claims 22 and 23 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hagemeyer, Levy and Yan as applied to claim 21 above, and further in view of Zheng et al., US 6,912,163 (listed in IDS filed on 09/30/2014).

In re Claim 22, Hagemeyer taken with Levy and Yan discloses all limitations of claim 22 except for that at least one of the gate electrode of the memory transistor and the gate electrode of the MOS logic transistor has a high work function.

Zheng teaches a semiconductor device wherein at least one of the gate electrode of a transistor has a high work function (column 5, line 34 – line 63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Hagemeyer-Levy- Yan's polysilicon gate electrode with Zheng's polysilicon gate electrode having a high work function, to improve dielectric charge trapping memory devices as taught by Zheng (column 2, line 39).

In re Claim 23, Hagemeyer taken with Levy, Yan and Zheng discloses the semiconductor device of claim 21, wherein at least one of the gate electrode of the memory transistor and the gate electrode of the MOS logic transistor has a work function of about 5.1 eV to about 5.2 eV

(Zheng: column 5, lines 60-62) that is within the claimed rang e of at least about 4.8 volts (eV), therefore anticipates the claimed range (MPEP 2131.01.I).

Claims 27, 29, and 30 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hagemeyer, Levy and Yan as applied to claim 21 above, and further in view of Agnello et al., US 6,287,913.

In re Claim 27, Hagemeyer taken with Levy and Yan discloses all limitations of claim 27 except for that the memory transistor is formed in a layer overlying a substrate.

Agnello teaches a semiconductor device wherein the memory transistor 100 is formed in a layer (30, 31, 62, 46) overlying a substrate 10 (Fig. 9; column 4, line 27 –column 6, line 63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute memory transistor of Hagemeyer-Levy-Yan with Agnello's memory transistor, for maintaining the high performance desired in high performance logic as taught by Agnello (column 1, lines 34-36).

In re Claim 29, Hagemeyer taken with Levy, Yan, and Agnello discloses the semiconductor device of claim 27, wherein the MOS logic transistor 200 is formed in a layer 52 overlying the substrate 10 (Agnello: Fig. 9; column 4, line 27 –column 6, line 63).

In re Claim 30, Hagemeyer taken with Levy, Yan, and Agnello discloses the semiconductor device of claim 27, wherein the MOS logic transistor 200 is formed in (layer 52) a different layer than the memory transistor (in layer (30, 31, 62, 46) (Agnello: Fig. 9; column 4, line 27 –column 6, line 63).

Allowable Subject Matter

Claims 26 and 28 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Friday from 9 a.m. to 6 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/307,858	06/18/2014	Igor Polishchuk	PM07027D1C1	7201

60909 7590 06/29/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGO, NGAN V

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
06/29/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000958

Office Action Summary	Application No. 14/307,858	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-40* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21-40* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *20150417*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☒ Other: *PTO-413*.

The present application is being examined under the pre-AIA first to invent provisions.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of

activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 21-40 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 2, and 7 of U.S. Patent No. 8,063,434 B1. Although the claims at issue are not identical, they are not patentably distinct from each other because the examined application claims 21-40 is either anticipated by, or would have been obvious over claims 1, 2, and 7 of U.S. Patent No. 8,063,434 B1. It is known that silicon nitride is a component of silicon oxynitride or it is known as equivalent materials to substitute one for the other.

Claims 21-40 are alternatively rejected on the ground of nonstatutory double patenting as being unpatentable over claims 3, 4, 6, and 14-16 of U.S. Patent No. 8,859,374 B1. Although the claims at issue are not identical, they are not patentably distinct from each other because the examined application claims 21-40 is either anticipated by, or would have been obvious over claims 3, 4, 6, and 14-16 of U.S.

Patent No. 8,859,374 B1. It is known that silicon nitride is a component of silicon oxynitride or it is known as equivalent materials to substitute one for the other.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/
Primary Examiner, Art Unit 2893

Ngan Ngo
June 25, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/605,231	01/26/2015	Krishnaswamy Ramkumar	PM07024CIP1C1	4843

60909 7590 07/07/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
07/07/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 000963

Office Action Summary	Application No. 14/605,231	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/18/15*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-40* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21-40* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Objections

Claims 29 is objected to because of the following informalities: Claim 29 is the same as claim 21. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramsbey et al. (U.S. Patent No. 6,433,383) in view of Yan (U.S. Patent Publication No. 2008/0135946) and further in view of Ranade (U.S. Patent Publication No. 2008/0121932).

Referring to figures 4-7, Ramsbey et al. teaches a memory device, comprising:

a tunnel oxide layer (15) overlying a channel connecting a source and a drain (13a/13b) of the memory device formed in a substrate (12);

a multi-layer charge storing layer (32/34) overlying the tunnel oxide layer (15), the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free (32, see figure 4c-7, col. 6, lines 35-55), and an oxygen-lean, second layer comprising a nitride on the first layer in which a composition of the second layer results in it being trap dense (34, see figures 4c-7, col. 6, lines 56-67, col. 7, lines 1-5); and

a high-temperature-oxide (HTO) layer (36) overlying the multi-layer charge storing layer (32/34), the HTO layer comprising an ***oxidized portion*** of the second layer (see col. 7, lines 6-22). The limitation "the HTO layer comprising an ***oxidized portion*** of the second layer" in claim 21 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding to claims 25, 33, wherein at least one of the first layer or the second layer of the multi-layer charge storing layer comprises silicon nitride or silicon oxy-nitride (32/34, see col. 6, lines 35 to col. 7, lines 5).

Regarding to claim 26, the oxidized portion of the second layer of the multi-layer charge storing layer comprises a thickness approximately in the range of 2 to 3 nanometers (32/34, see col. 6, lines 35 to col. 7, lines 5) .

Regarding to claim 27, the HTO layer comprises a thickness approximately in the range of 3.5 to 4.5 nanometers (36, see col. 7, lines 6-22).

Regarding to claims 28, 34, 39, the HTO layer comprises a nitrided HTO layer (36, see col. 7, lines 6-22). The limitation "the HTO layer comprising an ***nitrided*** HTO layer" in claim 21 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or

obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding to claim 29, a memory device, comprising:

a tunnel oxide layer (15) overlying a channel connecting a source and a drain (13a/13b) of the memory device formed in a substrate (12);

a multi-layer charge storing layer (32/34) overlying the tunnel oxide layer (15), the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free (32, see figure 4c-7, col. 6, lines 35-55), and an oxygen-lean, second layer comprising a nitride on the first layer in which a composition of the second layer results in it being trap dense (34, see figures 4c-7, col. 6, lines 56-67, col. 7, lines 1-5); and

a high-temperature-oxide (HTO) layer (36) overlying the multi-layer charge storing layer (32/34), the HTO layer comprising an oxidized portion of the second layer (see col. 7, lines 6-22). The limitation "the HTO layer comprising an oxidized portion of the second layer" in claim 21 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi

et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding to claim 35, a device comprising:

a vertical channel (between source/drain (13a/13b) extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region (13a/13b); and

an oxide-nitride-nitride-oxide (ONNO) stack (15/32/34/36) disposed about the vertical channel (between source/drain (13a/13b), the ONNO stack comprising:

a tunnel oxide layer (15) abutting the vertical channel (between source/drain (13a/13b);

a multi-layer charge storing layer (32/34) overlying the tunnel oxide layer (15), the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride abutting the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free (32, see figure 4c-7, col. 6, lines 35-55), and an oxygen-lean, second layer comprising a nitride overlying the first layer in which a composition of the second layer results in it being trap dense (34, see figures 4c-7, col. 6, lines 56-67, col. 7, lines 1-5); and

a high-temperature-oxide (HTO) layer (36) overlying the multi-layer charge storing layer (32/34), the HTO layer comprising an oxidized portion of the second layer (see col. 7, lines 6-22). The limitation "the HTO layer comprises an oxidized portion of the second layer" in claim 21 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding to claim 40, the first layer is separated from the second layer by an anti-tunneling layer comprising an oxide (32, see figure 4c-7, col. 6, lines 35-55, it is noted that layer 32 comprises oxide and oxynitride layer). Absent a showing of unexpected result, a change in sequence involves routine optimization of process of prior art and would have been obvious to one skilled in the art at the time the invention was made. A change in sequence/resversal of process steps is obvious under 35 USC 103 (exparte Rubin, 128 USPQ 440 (Bd. App. 1959)). See also in re Burhans, 154 F.2d 690,69 USPQ 330 (CCPA).

However, the reference does not clearly teach the channel comprises polysilicon, recrystallized polysilicon or silicon nanowire.

Yan teaches forming channel comprise polysilicon (see paragraph# 32, meeting claim 21-23, 30-31, 36-37). The limitation "the channel comprising ***recrystallized*** polysilicon" in claim 21 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form polysilicon channel in Ramsbey et al. as taught by Yan because determining the optimum material for the layer only involved routine skill in the art to form a desired memory device.

Ranade teaches forming channel comprise a silicon nanowire (see figures 2a-2n, paragraph# 25, meeting claims 24, 32, 38).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form silicon nanowire channel in Ramsbey et al. as taught by Ranade because determining the optimum material for the layer only involved routine skill in the art to form a desired memory device.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with

this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 21-40 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-19 of U.S. Patent No. 8,633,537. Although the claims at issue are not identical, they are not patentably distinct from each other because both the present invention and the patent teach a memory device, comprising: a tunnel oxide layer overlying a channel connecting a source and a drain of the memory device formed in a substrate; a multi-layer charge storing layer overlying the tunnel oxide layer, the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free, and an oxygen-lean, second layer comprising a nitride on the first layer in which a composition of the second layer results in it being trap dense; and a high-temperature-oxide (HTO) layer overlying the multi-layer charge storing layer, the HTO layer comprising an oxidized portion of the second layer.

Claims 21-40 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over and claims 21-23, 31-32, 35-37, and 39-40 of copending Application No. 14 /159,315 (publication# 2014/0264551). Although the claims at issue are not identical, they are not patentably distinct from each other because both the present invention and the application teach a memory device, comprising: a tunnel oxide layer overlying a channel connecting a source and a drain of the memory device formed in a substrate; a multi-layer charge storing layer overlying the tunnel oxide layer, the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free, and an oxygen-lean, second layer comprising a nitride on the first layer in which a composition of the second layer results in it being trap dense; and a high-temperature-oxide (HTO) layer overlying the multi-layer charge storing layer, the HTO layer comprising an oxidized portion of the second layer.

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

TTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 05/01/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 05/01/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	08/01/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 000976

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 05/01/2012
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	08/01/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1002, Page 000977

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

60909 7590 05/01/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 05/01/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 87 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 87 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 000978

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/124,855	RAMKUMAR, KRISHNASWAMY	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/19/12*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *5,12,21-23 and 25*.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Sandisk Technologies, Inc. - Ex. 1002, Page 000980

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 5, 12, 21-23, -25 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in forming charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5-3.5 nanometers and a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9-10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer having a thickness approximately in the range of 3.5-4.5 nanometers.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/THANH T NGUYEN/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 05/03/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 05/03/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	08/03/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 000983

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 05/03/2011
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	08/03/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1002, Page 000984

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

60909 7590 05/03/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 05/03/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 100 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 100 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 000985

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/124,855	RAMKUMAR, KRISHNASWAMY	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/18/11*.

2. ☒ The allowed claim(s) is/are *5 and 12*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Sandisk Technologies, Inc. - Ex. 1002, Page 000987

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 5, 12 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in forming the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion and wherein oxidizing the top silicon-rich silicon oxy-nitride portion to form the second dielectric layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau, can be reached on (571) 272-1945. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 07/28/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 07/28/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM2007024	3433

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/28/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Sandisk Technologies, Inc. - Ex. 1002, Page 000990

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 07/28/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM2007024	3433

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/28/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM2007024	3433

60909 7590 07/28/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 07/28/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 100 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 100 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Sandisk Technologies, Inc. - Ex. 1002, Page 000992

Notice of Allowability	Application No.	Applicant(s)	
	12/124,855	RAMKUMAR, KRISHNASWAMY	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/12/10*.

2. ☒ The allowed claim(s) is/are *5 and 12*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 5, 12 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in forming the charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion and wherein oxidizing the top silicon-rich silicon oxy-nitride portion to form the second dielectric layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau, can be reached on (571) 272-1945. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 08/01/2012
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 08/01/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	11/01/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 000996

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 08/01/2012
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	11/01/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1002, Page 000997

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/124,855	05/21/2008	Krishnaswamy Ramkumar	PM07024	3433

60909 7590 08/01/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 08/01/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 87 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 87 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 000998

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/124,855	RAMKUMAR, KRISHNASWAMY	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/10/12*.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *5, 12, 21-23, 25*.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/10/12
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 5, 12, 21-23, 25 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in forming charge-trapping layer comprises a bottom oxygen-rich silicon oxy-nitride portion having a thickness approximately in the range of 2.5-3.5 nanometers and a top silicon-rich silicon oxy-nitride portion having a thickness approximately in the range of 9-10 nanometers, and wherein oxidizing the portion of the charge-trapping layer comprises oxidizing the top approximately 2 nanometers to approximately 3 nanometers of the top silicon-rich silicon oxy-nitride portion to form the blocking dielectric layer having a thickness approximately in the range of 3.5-4.5 nanometers.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/THANH T NGUYEN/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 07/14/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGO, NGAN V

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 07/14/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM07027	5484

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$0	$1510	10/14/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001003

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 07/14/2011
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM07027	5484

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$0	$1510	10/14/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1002, Page 001004

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM07027	5484

60909 7590 07/14/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 07/14/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 309 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 309 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001005

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/152,518	POLISHCHUK ET AL.	
	Examiner	Art Unit	
	NGAN NGO	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *tne amendment filed 6-28-11*.

2. ☒ The allowed claim(s) is/are *23-31*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Ngan Ngo/
Primary Examiner, Art Unit 2893

Sandisk Technologies, Inc. - Ex. 1002, Page 001007

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

In the claims:

Cancel non-elected claims 16-20.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

7/13/2011

Notice of Allowability	Application No.	Applicant(s)	
	12/197,466	RAMKUMAR ET AL.	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/17/12*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-16, 20, 22-24*.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *5/31/12* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

This application is in condition for allowance except for the presence of claims 17-19 directed to Species non-elected without traverse. Applicant's representative, William E. Nuttle, cancel claims 17-19 on 5/31/12.

Accordingly, claims 17-19 have been cancelled.

The following is an examiner's statement of reasons for allowance:

Claims 1-16, 20, 22-24 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps wherein at least the second radical oxidation process comprises flowing hydrogen (H_2) and oxygen (O_2) gas into the first process chamber, forming radicals at a surface of the charge-trapping layer without an ignition event to pyrolyze the H_2O and O_2, and consuming a portion of the charge-trapping layer, to form a second dielectric layer, as claimed in claim 1; depositing, in a second process chamber of the cluster tool, an oxygen-rich silicon oxy-nitride portion of a charge-trapping layer above the first dielectric layer;" and (ii) "subjecting, in the first process chamber of the cluster tool, the charge-

trapping layer to a third radical oxidation process by flowing hydrogen (H_2) and oxygen (O_2) gas into the first process chamber, forming radicals at a surface of the charge-trapping layer to form a second dielectric layer above the charge-trapping layer by oxidizing and consuming a portion of the silicon-rich silicon oxy-nitride portion of the charge-trapping layer, as claimed in claim 11, depositing, in a second process chamber of the cluster tool, a charge-trapping layer above the first dielectric layer, the charge-trapping layer comprising a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion, as claimed in claim 20.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/THANH T NGUYEN/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 09/24/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 09/24/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/197,466	08/25/2008	Krishnaswamy Ramkumar	PM07024C1	2398

TITLE OF INVENTION: A METHOD OF FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	12/24/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001013

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 09/24/2012
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/197,466	08/25/2008	Krishnaswamy Ramkumar	PM07024C1	2398

TITLE OF INVENTION: A METHOD OF FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	12/24/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1002, Page 001014

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/197,466	08/25/2008	Krishnaswamy Ramkumar	PM07024C1	2398

60909 7590 09/24/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 09/24/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 502 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 502 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001015

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/197,466	RAMKUMAR ET AL.	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/6/12*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-16,20 and 22-24*.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/6/12
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Sandisk Technologies, Inc. - Ex. 1002, Page 001017

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

This application is in condition for allowance except for the presence of claims 17-19 directed to Species non-elected without traverse. Applicant's representative, William E. Nuttle, cancel claims 17-19 on 5/31/12.

Accordingly, claims 17-19 have been cancelled.

The following is an examiner's statement of reasons for allowance:

Claims 1-16, 20, 22-24 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps wherein at least the second radical oxidation process comprises flowing hydrogen (H_2) and oxygen (O_2) gas into the first process chamber, forming radicals at a surface of the charge-trapping layer without an ignition event to pyrolyze the H_2O and O_2, and consuming a portion of the charge-trapping layer, to form a second dielectric layer, as claimed in claim 1; depositing, in a second process chamber of the cluster tool, an oxygen-rich silicon oxy-nitride portion of a charge-trapping layer above the first dielectric layer;" and (ii) "subjecting, in the first process chamber of the cluster tool, the charge-

trapping layer to a third radical oxidation process by flowing hydrogen (H_2) and oxygen (O_2) gas into the first process chamber, forming radicals at a surface of the charge-trapping layer to form a second dielectric layer above the charge-trapping layer by oxidizing and consuming a portion of the silicon-rich silicon oxy-nitride portion of the charge-trapping layer, as claimed in claim 11, depositing, in a second process chamber of the cluster tool, a charge-trapping layer above the first dielectric layer, the charge-trapping layer comprising a bottom oxygen-rich silicon oxy-nitride portion and a top silicon-rich silicon oxy-nitride portion, as claimed in claim 20.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/THANH T NGUYEN/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 07/08/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGO, NGAN V

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 07/08/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/08/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001021

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 07/08/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/08/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	438-287000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001022

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

60909 7590 07/08/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 07/08/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001023

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 6-20-14*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *16,19 and 21-34*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NGAN NGO/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 08/26/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGO, NGAN V

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 08/26/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	11/26/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001026

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 08/26/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	11/26/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	438-287000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001027

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

60909 7590 08/26/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 08/26/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001028

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the IDS filed 8-11-14*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *16,19 and 21-34*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 20140811
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NGAN NGO/
Primary Examiner, Art Unit 2893

Sandisk Technologies, Inc. - Ex. 1002, Page 001030

The present application is being examined under the pre-AIA first to invent provisions.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

In the claims:

Claim 16, line 5, delete "including".

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

8/21/2014

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 05/24/2013
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 05/24/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$0	$0	$1780	08/26/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001033

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 05/24/2013
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$0	$0	$1780	08/26/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Sandisk Technologies, Inc. - Ex. 1002, Page 001034

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1002, Page 001035

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

60909 7590 05/24/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 05/24/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001036

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/539,458	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/9/13*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

   Interim copies:

   a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

Sandisk Technologies, Inc. - Ex. 1002, Page 001038

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 1-20 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in forming a multi-layer charge storing layer overlying the tunnel oxide layer, the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a stoichiometric composition of the first layer results in it being substantially trap free, and an oxygen-lean, second layer comprising a nitride on the first layer in which a stoichiometric composition of the second layer results in it being trap dense; and subjecting the substrate to a second oxidation process to consume a portion of the second layer and form a high-temperature-oxide (HTO) layer overlying the multi-layer charge storing layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/THANH T NGUYEN/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 08/04/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 08/04/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	11/04/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001041

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 08/04/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	11/04/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001042

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

60909 7590 08/04/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 08/04/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001043

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/539,458	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/20/13*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

   Interim copies:

   a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 6/20/13
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

Sandisk Technologies, Inc. - Ex. 1002, Page 001045

The present application is being examined under the pre-AIA first to invent provisions.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 1-20 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in forming a multi-layer charge storing layer overlying the tunnel oxide layer, the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a stoichiometric composition of the first layer results in it being substantially trap free, and an oxygen-lean, second layer comprising a nitride on the first layer in which a stoichiometric composition of the second layer results in it being trap dense; and subjecting the substrate to a second oxidation process to consume a portion of the second layer and form a high-temperature-oxide (HTO) layer overlying the multi-layer charge storing layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/THANH T NGUYEN/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 11/03/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/03/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/03/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001048

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 11/03/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

TITLE OF INVENTION: RADICAL OXIDATION PROCESS FOR FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/03/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001049

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,458	07/01/2012	Krishnaswamy RAMKUMAR	PM07024CIP1	7732

60909 7590 11/03/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/03/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001050

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/539,458	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/9/14*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

   Interim copies:

   a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

Sandisk Technologies, Inc. - Ex. 1002, Page 001052

The present application is being examined under the pre-AIA first to invent provisions.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 1-20 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in forming a multi-layer charge storing layer overlying the tunnel oxide layer, the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a stoichiometric composition of the first layer results in it being substantially trap free, and an oxygen-lean, second layer comprising a nitride on the first layer in which a stoichiometric composition of the second layer results in it being trap dense; and subjecting the substrate to a second oxidation process to consume a portion of the second layer and form a high-temperature-oxide (HTO) layer overlying the multi-layer charge storing layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/THANH T NGUYEN/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 04/28/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGO, NGAN V

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 04/28/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	07/28/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001055

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 04/28/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	07/28/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001056

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

60909 7590 04/28/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 04/28/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 336 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 336 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001057

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 2-4-14*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *16 and 19-34*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NGAN NGO/
Primary Examiner, Art Unit 2893

Sandisk Technologies, Inc. - Ex. 1002, Page 001059

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 09/04/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 09/04/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	12/04/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001060

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 09/04/2013
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	12/04/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Sandisk Technologies, Inc. - Ex. 1002, Page 001061

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1002, Page 001062

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

60909 7590 09/04/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 09/04/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 136 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 136 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001063

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/539,466	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed on 12/21/2012*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-5 and 7-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

Sandisk Technologies, Inc. - Ex. 1002, Page 001065

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 12/21/2012; 04/19/2013; 06/05/2013; 06/05/2013.

Sandisk Technologies, Inc. - Ex. 1002, Page 001066

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 12/21/2012 has been entered.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 12/21/2012; 04/19/2013, 06/05/2013, 06/05/2013 were filed after the mailing date of the Notice of Allowance on 11/27/2012. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

Claims 1-5 and 7-20 stand allowed for the reasons articulated in the Office Action mailed on 11/27/2013.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Friday from 8 a.m. to 5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

Electronic Acknowledgement Receipt

EFS ID:	29019424
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff
Filer Authorized By:	
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	25-APR-2017
Filing Date:	26-OCT-2016
Time Stamp:	13:09:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C3_IDS_04212017.pdf	1056285 2b29df5f5c122c7f295c61f3ed428362b6469a05	no	12

Warnings:

Information:					
2	Foreign Reference	CN101517714A.pdf	140321 133bafb125b0d7e069aa20ce068b065a3c44f045	no	2
Warnings:					
Information:					
3	Foreign Reference	CN101558481.pdf	107437 cd969584f36b6cf21925b2cdbaf56bfd638e8012	no	1
Warnings:					
Information:					
4	Foreign Reference	CN101859702.pdf	94821 5f02d93c64d31841ad324864b156f6690d51e133	no	1
Warnings:					
Information:					
5	Foreign Reference	CN104254921A.pdf	124620 368a15b657671cd0e2dcbb37d02b89c0907174aa	no	2
Warnings:					
Information:					
6	Foreign Reference	CN1801478.pdf	147196 4c59ac05df56b42e82966e7928f95c7c15963b7c	no	2
Warnings:					
Information:					
7	Foreign Reference	CN1832201.pdf	140891 67149bf229c84e375cd1f3fee0b520e32caca893	no	1
Warnings:					
Information:					
8	Foreign Reference	JP2005347679.pdf	193455 58de4c030861f678ae5ea04f59dbad99cd2b5de7	no	2
Warnings:					
Information:					

9	Foreign Reference	JP2007318112.pdf	209017 b3527f90fc45ddc1e6f0785812e12a0961db0b59	no	2
Warnings:					
Information:					
10	Foreign Reference	JP2007515060.pdf	206249 088d4bb32c7e168143d3ff3675b0ae96ce615166	no	2
Warnings:					
Information:					
11	Foreign Reference	JP2009260070.pdf	174171 12ce3d88cec8767ae927988e332856743a3578d2	no	2
Warnings:					
Information:					
12	Foreign Reference	KR20040070669.pdf	93947 19ba99f04d967c51a9b5963e194891c72023cfca	no	1
Warnings:					
Information:					
13	Foreign Reference	KR2006100092.pdf	91966 04e49b9b6cfe70152a63f0ff9fa4d5b1374fbde3	no	5
Warnings:					
Information:					
14	Foreign Reference	TW200703671.pdf	109964 b2734dc07cb23d48fd4f008c9d161075b1dc922c	no	2
Warnings:					
Information:					
15	Foreign Reference	TW200847343.pdf	212627 01b400f6c055c67212b7b99569ab8bf95f78afb5	no	2
Warnings:					
Information:					

16	Foreign Reference	WO2007064048.pdf	187724 f3925d4e9a22ab44d1ca1a2d587a51b6f1b439fd	no	2
Warnings:					
Information:					
17	Foreign Reference	WO2008129478.pdf	4747978 9a8d4a82f8b12b76f9c8c5d756d0b586db5290ab	no	58
Warnings:					
Information:					
18	Foreign Reference	WO2011162725.pdf	130375 48e56c9b6a3e98a5554da2c93125434cc15f7be3	no	2
Warnings:					
Information:					
19	Foreign Reference	WO2013148112A1.pdf	1847818 03ed9b4f094560237f526189e38aa742577e726c	no	60
Warnings:					
Information:					
20	Foreign Reference	WO2013148343.pdf	130025 7005d72ac42f5551f6f901b6e35cf2104cd01bd5	no	2
Warnings:					
Information:					
21	Non Patent Literature	PM07024CN_OA_01262011.pdf	94955 ee551bdf550e92f180fc90eeda18846fb591b017	no	6
Warnings:					
Information:					
22	Non Patent Literature	PM07024CIP1CN_SIPOOA_08192016.pdf	271259 4676b38f1b1f11c244d404d7eae9a1358407dc3b	no	8
Warnings:					
Information:					

23	Non Patent Literature	PM07024C1_AdvisoryAction_01312012.pdf	118671 dc3ff87b63eec307476d90d826232f27142fe9ed	no	3
Warnings:					
Information:					
24	Non Patent Literature	PM07024CIP1C1_AdvisoryAction_03092016.pdf	124840 3a428c4a92e23ac2584a273e1cba4653233b2bbc	no	3
Warnings:					
Information:					
25	Non Patent Literature	PM07024CIP1C1_AdvisoryAction_07052016.pdf	125826 a388136eda3ad8be9ab3d8496fb6908fb7677ef2	no	3
Warnings:					
Information:					
26	Non Patent Literature	PM07024_FinalRejection_01312012.pdf	262470 0d9d177e096cfb9aab0755f0486003c7d78ff65f	no	7
Warnings:					
Information:					
27	Non Patent Literature	PM07024_FinalRejection_05102010.pdf	388862 3974990eacd28a6e696f44e516bdfceac84d9e70	no	11
Warnings:					
Information:					
28	Non Patent Literature	PM07024C1_FinalRejection_11172011.pdf	476326 2279f27b9866a15416b5624f77cdd8ba47699440	no	13
Warnings:					
Information:					
29	Non Patent Literature	PM07027D1C1_FinalRejection_10082015.pdf	215527 dac37abd241390984dbc912c697b0658213dfcc9	no	6
Warnings:					
Information:					

30	Non Patent Literature	PM07024CIP1C1_FinalRejection_12172015.pdf	578220 ce6487a7c0b03f673ef3ce6cfceae50d48ba6be2	no	15
Warnings:					
Information:					
31	Non Patent Literature	PM07024CIP1_NonFinalOA_03132013.pdf	182223 255757eeff46e58840d2780ad8c3f7b1901e77d8	no	5
Warnings:					
Information:					
32	Non Patent Literature	PM07024CIP1_NonFinalOA_10022014.pdf	185781 77779fc6df1b448082b72f048090614c4ba3b3d6	no	5
Warnings:					
Information:					
33	Non Patent Literature	PM07024C2_NonFinalRejection_04032014.pdf	457082 d2e9a42396e1a75e4ba6546e7d5a3a8d5c907bd1	no	12
Warnings:					
Information:					
34	Non Patent Literature	PM07024C2_NonFinalRejection_07182014.pdf	197457 937e9d41047300df85cee693a7f8ba9c4a50063e	no	5
Warnings:					
Information:					
35	Non Patent Literature	PM07024_NonFinalRejection_01182011.pdf	174573 c5d977f1fe0865d41a93084b4bbebefb70140282	no	5
Warnings:					
Information:					
36	Non Patent Literature	PM07024_NonFinalRejection_08162011.pdf	303128 728de5ca426635c82c4cc0534ebb48d2545236ff	no	9
Warnings:					
Information:					

37	Non Patent Literature	PM07024_NonFinalRejection_10292009.pdf	326926 23aead5aa544c31c80b454c5e516bef4032a76c7	no	9
Warnings:					
Information:					
38	Non Patent Literature	PM07027_NonFinalRejection_03092011.pdf	141142 cdb488b0f3155c1d136c2e1e2aac9ddf47da90ba	no	4
Warnings:					
Information:					
39	Non Patent Literature	PM07027_NonFinalRejection_09292010.pdf	163626 d39f87b7b2517c287ba4ec3cfdab621dc490f8d1	no	5
Warnings:					
Information:					
40	Non Patent Literature	PM07024C1_NonFinalRejection_06012011.pdf	410200 dee1df35822a07d18476baf75c32a7f995f53896	no	11
Warnings:					
Information:					
41	Non Patent Literature	PM07027D1_NonFinalRejection_06192014.pdf	165036 da18d485aabfd7730d66470132430100a5ec9303	no	5
Warnings:					
Information:					
42	Non Patent Literature	PM07027D1_NonFinalRejection_12052013.pdf	155938 04f8be1c54d11d56b69507b0727f7dc26c9135fe	no	4
Warnings:					
Information:					
43	Non Patent Literature	PM07027D1CIP1_NonFinalRejection_09282012.pdf	345461 5b55937f96a593b9dfbe17c14a2a7c538aa92f76	no	9
Warnings:					
Information:					

44	Non Patent Literature	PM07027D1CIP1C1_NonFinalRejection_10212014.pdf	481843 523857cc71950d8d312ed0774c47267c0aaf7339	no	12
Warnings:					
Information:					
45	Non Patent Literature	PM07027D1C1_NonFinalRejection_06292015.pdf	191453 f51c60966ac3e60d22b6bb5b2a4aefbae7435dfe	no	5
Warnings:					
Information:					
46	Non Patent Literature	PM07024CIP1C1_NonFinalRejection_07072015.pdf	495475 9bfe8ff115f946c412f0f9ed1e1d8f8801e1a37b	no	13
Warnings:					
Information:					
47	Non Patent Literature	PM07024_NOA_05012012.pdf	382841 8fd789383c749fab7358dcba4bca28f417c58c09	no	7
Warnings:					
Information:					
48	Non Patent Literature	PM07024_NOA_05032011.pdf	372468 b75b0731c0ba077c9418c833235c18cc6162db6c	no	7
Warnings:					
Information:					
49	Non Patent Literature	PM07024_NOA_07282010.pdf	297560 e7d4b8c70c1e09d4adac247fbf8e74edcc7f49e6	no	6
Warnings:					
Information:					
50	Non Patent Literature	PM07024_NOA_08012012.pdf	386691 31d2c4ebb5c06e0ca8546b148fb77c42cc7c458c	no	7
Warnings:					
Information:					

51	Non Patent Literature	PM07027_NOA_07142011.pdf	359562 ca5e7c28b882982b55c57ab33013b09767dee259	no	6
Warnings:					
Information:					
52	Non Patent Literature	PM07024C1_NOA_06152012.pdf	139688 c0966f78ee4e53aa9a2cd44d6fa9e5e4f80362d0	no	4
Warnings:					
Information:					
53	Non Patent Literature	PM07024C1_NOA_09242012.pdf	415929 55bbb26eb0dc647ee814e36f2d5803273bac6eff	no	8
Warnings:					
Information:					
54	Non Patent Literature	PM07027D1_NOA_07082014.pdf	358169 8acac69ef7a610173562faf8ed62aad268f9cf75	no	5
Warnings:					
Information:					
55	Non Patent Literature	PM07027D1_NOA_08262014.pdf	390897 16dc7619bd435bc96ff5fd0c2aa4ee2dd4664f1f	no	7
Warnings:					
Information:					
56	Non Patent Literature	PM07024CIP1_NOA_05242013.pdf	948440 cb5cfbedc0e2a431e2232ce7cccea61b45d3bf20	no	8
Warnings:					
Information:					
57	Non Patent Literature	PM07024CIP1_NOA_08042014.pdf	411032 5a4f4ea70e6cc3094a4703fb5cc603e3adce29e4	no	7
Warnings:					
Information:					

58	Non Patent Literature	PM07024CIP1_NOA_11032014.pdf	410782 f6b1b280ed68bf1faa4f6ce2375df1025825c83b	no	7
Warnings:					
Information:					
59	Non Patent Literature	PM07027D1_NOA_04282014.pdf	351954 4faf4ba59a062d8789e4db8014d4d010265 5842a	no	5
Warnings:					
Information:					
60	Non Patent Literature	PM07027D1CIP1_NOA_09042013.pdf	407317 834ffb65f5f06c53b50cbfa031a12303d9dd 3926	no	9
Warnings:					
Information:					
		Total Files Size (in bytes):	22814517		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Sandisk Technologies, Inc. - Ex. 1002, Page 001079

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	1	Japanese Office Action for Japanese Application Number 2013-549612 (PM07002CIP1JP) dated 08/04/2015; 8 pages	
	2	Japanese Office Action for Japanese Application Number 2015-503338 (PM07002CIP2JP) dated 02/21/2017; 21 pages	
	3	SIPO Office Action for Application Number 200910134374.1 (PM07002CN) dated 01/21/2015; 5 pages	
	4	SIPO Office Action for Application Number 200910134374.1 (PM07002CN) dated 02/03/2016; 2 pages	
	5	SIPO Office Action for Application Number 200910134374.1 (PM07002CN) dated 07/29/2014; 5 pages	
	6	SIPO Office Action for Application Number 200910134374.1 (PM07002CN) dated 07/30/2015; 2 pages	
	7	SIPO Office Action for Application Number 200910134374.1 (PM07002CN) dated 09/22/2013; 4 pages	
	8	SIPO Office Action for Application Number 20120000107.5 (PM07002CIP1CN) dated 04/01/2015; 5 pages	
	9	SIPO Office Action for Application Number 20120000107.5 (PM07002CIP1CN) dated 05/12/2016; 5 pages	
	10	SIPO Office Action for Application Number 20120000107.5 (PM07002CIP1CN) dated 07/25/2014; 4 pages	
	11	SIPO Office Action for Application Number 20120000107.5 (PM07002CIP1CN) dated 10/09/2015; 2 pages	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	12	SIPO Office Action for Application Number 201280000107.5 (PM07002CIP1CN) dated 11/29/2016; 5 pages	
	13	SIPO Office Action for Application Number 2013800168932 (PM07002CIP2CN) dated 09/01/2016; 7 pages	
	14	TIPO Office Action for Application Number 102110223 (PM07002CIP2TW) dated 11/18/2016; 10 pages	
	15	TIPO Office Action for Taiwan Application Number 101101220 (PM07002CIP1TW) dated 10/15/2015; 4 pages	
	16	USPTO Advisory Action for Application Number 11/811,958 (PM07002) dated 03/16/2010; 4 pages	
	17	USPTO Advisory Action for Application Number 11/811,958 (PM07002) dated 04/20/2010; 6 pages	
	18	USPTO Advisory Action for Application Number 11/811,958 (PM07002) dated 05/14/2013; 4 pages	
	19	USPTO Advisory Action for Application Number 11/811,958 (PM07002) dated 06/02/2011; 5 pages	
	20	USPTO Advisory Action for Application Number 13/436,872 (PM07002CIP2) dated 08/04/2015; 2 pages	
	21	USPTO Final Rejection for Application Number 11/811,958 (PM07002) dated 01/06/2010; 17 pages	
	22	USPTO Final Rejection For Application Number 11/811,958 (PM07002) Dated 03/13/2013; 22 pages	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	23	USPTO Final Rejection for Application Number 11/811,958 (PM07002) dated 03/15/2011; 13 pages	
	24	USPTO Final Rejection for Application Number 13/007,533 (PM07002CIP1) dated 09/24/2012; 13 pages	
	25	USPTO Final Rejection for Application Number 13/436,872 (PM07002CIP2) dated 05/27/2015; 14 pages	
	26	USPTO Non Final Rejection for Application Number 11/811,958 (PM07002) dated 12/07/2011; 13 pages	
	27	USPTO Non Final Rejection for Application Number 13/007,533 (PM07002CIP1) dated 04/12/2012; 9 pages	
	28	USPTO Non-Final Rejection for Application Number 11/811,958 (PM07002) dated 05/13/2009; 14 pages	
	29	USPTO Non-Final Rejection for Application Number 11/811,958 (PM07002) dated 10/01/2012; 17 pages	
	30	USPTO Non-Final Rejection for Application Number 11/811,958 (PM07002) dated 10/07/2010; 12 pages	
	31	USPTO Non-Final Rejection for Application Number 13/436,872 (PM07002CIP2) dated 12/19/2014; 15 pages	
	32	USPTO Non-Final Rejection for Application Number 13/917,500 (PM07002C1) dated 01/05/2015; 13 pages	
	33	USPTO Non-Final Rejection for Application Number 14/172,775 (PM07002CIP1C1) dated 06/22/2015; 14 pages	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	34	USPTO Notice Of Allowance for Application Number 13/007,533 (PM07002CIP1) dated 03/07/2013; 8 pages	
	35	USPTO Notice of Allowance for Application Number 13/007,533 (PM07002CIP1) dated 06/18/2013; 9 pages	
	36	USPTO Notice of Allowance for Application Number 13/007,533 (PM07002CIP1) dated 09/06/2013; 9 pages	
	37	USPTO Notice Of Allowance for Application Number 13/007,533 (PM07002CIP1) dated 11/27/2012; 13 pages	
	38	USPTO Notice of Allowance for Application Number 13/007,533 (PM07002CIP1) dated 12/06/2013; 10 pages	
	39	USPTO Notice of Allowance for Application Number 13/436,872 (PM07002CIP2) dated 01/15/2016; 5 pages	
	40	USPTO Notice of Allowance for Application Number 13/436,872 (PM07002CIP2) dated 09/15/2015; 9 pages	
	41	USPTO Notice of Allowance for Application Number 13/917,500 (PM07002C1) dated 06/01/2015; 6 pages	
	42	USPTO Notice of Allowance for Application Number 13/917,500 (PM07002C1) dated 09/14/2015; 5 pages	
	43	USPTO Notice of Allowance for Application Number 13/917,500 (PM07002C1) dated 12/31/2015; 5 pages	
	44	USPTO Notice of Allowance for Application Number 14/172,775 (PM07002CIP1C1) dated 09/04/2015; 7 pages	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	45	USPTO Notice of Allowance for Application Number 14/172,775 (PM07002CIP1C1) dated 12/18/2015; 6 pages	
	46	USPTO Notice of Allowance for US Application Number 13/436,872 (PM07002CIP2) dated 05/11/2016; 5 pages	
	47	USPTO Requirement for Restriction for Application Number 13/007,533 (PM07002CIP1) dated 12/06/2011; 7 pages	
	48	USPTO Requirement Restriction for Application Number 12/197,466 (PM07024C1) dated 03/11/2011; 5 pages	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kin Hung Lai/	Date (YYYY-MM-DD)	2017-04-24
Name/Print	Kin Hung Lai	Registration Number	69251

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(English Translation)

Notification of Reasons for Refusal

Patent Application No.:	2013-549612
Dispatch Date:	August 4, 2015
	(Drafting date: July 24, 2015)
Patent Office Examiner:	M. Koyama 9458 5O00
Representatives:	To Attorneys, Mr. K. Sugimura (and 2 attorneys)
Applied Provisions:	Patent Law Sections 29(1), 29(2), and 36

The present application should be refused for the reasons mentioned below. If the applicant has any argument against the reasons, please submit such argument within 3 months from the dispatch date of this notification.

Reason:

1. (Novelty) The inventions of the claims mentioned below of the present application should not be granted a patent under Patent Law Section 29(1)(iii) on the basis of the inventions described in the documents mentioned below which were distributed in Japan or foreign countries or made available to the public through electric telecommunication lines in Japan or foreign countries prior to the filing of the present application.

2. (Inventive Step) The inventions of the claims mentioned below of the present application should not be granted a patent under Patent Law Section 29(2), since it could have easily been made by persons who have common knowledge in the technical field to which the inventions pertain, on the basis of the inventions described in the documents mentioned below which were distributed or made available to the public through electric telecommunication lines in Japan or foreign countries prior to the filing of the present application.

3. (Support Requirements) The subject application does not comply with the requirements under Patent Law Section 36(6)(i) on the following points in claims.

Sandisk Technologies, Inc. - Ex. 1002, Page 001087

Notes (see the list of Cited documents etc. below)

• Reason 1 (Novelty)

- Claim 1
- Cited Documents 1 and 2
- Remarks

Cited document 1 (paragraphs 0026, 0029, 0036, 0037, 0045, and fig. 5) discloses a SONOS structure comprising: a tunneling layer 516 on a substrate 208; a charge storing layer including an oxygen-rich oxynitride layer 518A with low trap density on the tunneling layer, and a trap dense oxygen-lean oxynitride layer 518B on the oxygen-rich oxynitride layer 518A; a blocking layer 520 on the oxynitride layer 518B; and a silicon containing gate layer 514 on the blocking layer.

Cited document 2 (paragraphs 0007, 0008, figs. 1, 2, and 5) discloses a semiconductor memory device comprising: a silicon dioxide film 14 on a semiconductor substrate 11; a nitrogen-containing silicon dioxide film 15 including an oxygen-rich oxynitride layer and a oxygen-lean oxynitride layer on the silicon dioxide film; a silicon dioxide film 16 on the nitrogen-containing silicon dioxide film 15; and a silicon containing gate electrode 17 on the silicon dioxide film 16.

Therefore, there is no significant difference between the invention according to claim 1 and the inventions disclosed in cited documents 1 and 2.

- Claims 2 and 3
- Cited Document 1
- Remarks

Fig. 7B of cited document 1 discloses that the concentration of oxygen of the oxygen-rich oxynitride layer 518A includes the range of about 15 % to about 40 %, and that the concentration of oxygen of the oxygen-lean oxynitride layer 518B includes the range of less than about 5 %.

Therefore, there is no significant difference between the inventions according to claims 2 and 3 and the invention disclosed in cited document 1.

- Claim 6
- Cited Documents 1 and 2
- Remarks

The semiconductor devices disclosed in cited documents 1 and 2 also comprise

Sandisk Technologies, Inc. - Ex. 1002, Page 001088

sources and drains on the substrate.

Therefore, there is no significant difference between the invention according to claim 6 and the inventions disclosed in cited documents 1 and 2.

- Claims 7 and 8
- Cited Document 1
- Remarks

The comments for claims 2 and 3 apply to claims 7 and 8.

Therefore, there is no significant difference between the inventions according to claims 7, 8 and the invention disclosed in cited document 1.

- Claim 11
- Cited Documents 1 and 2
- Remarks

Claim 11 describes the structure of claim 1 and the semiconductor device of claim 6 as a method for manufacturing a semiconductor device. The comments for claims 1 and 6 apply to claim 11.

Therefore, there is no significant difference between the invention according to claim 11 and the inventions disclosed in cited documents 1, 2.

- Claims 12, 13 and 15
- Cited Document 1
- Remarks

Claims 12, 13, and 15 describe the structure of claims 2, 3 and the semiconductor device of claims 7, 8 as a method for manufacturing a semiconductor device. The comments for claims 2, 3, 7, and 8 apply to claims 12, 13 and 15.

Therefore, there is no significant difference between the inventions according to claims 12, 13, and 15 and the invention disclosed in cited document 1.

- Claim 16
- Cited Documents 1 and 2
- Remarks

Since the semiconductor device of cited document 1 comprises multiple oxynitride layers similar to that of the present application, it is considered that the specified operating life of at least 20 years will be exceeded as in the present application.

Therefore, there is no significant difference between the invention according to

Sandisk Technologies, Inc. - Ex. 1002, Page 001089

claim 16 and the inventions disclosed in cited documents 1, 2.

- Claim 18
- Cited Document 1
- Remarks

Cited document 1 (paragraph 0056, 0057, figs. 5 and 9) discloses that the oxygen-rich oxynitride layer 518A is formed in a chemical vapor deposition (CVD) process using a process gas comprising a mixture gas of SiH_2Cl_2 and NH_3 mixed at a ratio in a range of about 1:7 to 7:1 and a mixture gas of N_2O and NH_3 mixed at a ratio in a range of about 8:1 to 1:8, and wherein the oxygen-lean oxynitride layer 518B is formed in a CVD process using a process gas comprising a mixture gas of SiH_2Cl_2 and NH_3 mixed at a ratio in a range of about 1:7 to 7:1 and a mixture gas of N_2O and NH_3 mixed at a ratio in a range of about 8:1 to 1:8.

Therefore, there is no significant difference between the inventions according to claim 18 and the invention disclosed in cited document 1.

- Claim 19
- Cited Document 1
- Remarks

Cited document 1 (paragraph 0058) discloses forming the first oxynitride layer and the second oxynitride layer sequentially in the same processing unit by modifying the flow rate of NH_3 gas.

Therefore, there is no significant difference between the invention according to claim 19 and the invention disclosed in cited document 1.

• Reason 2 (Novelty)
- Claims 1 to 3, 6 to 8, 11 to 13, 15, 16, 18, and 19
- Cited Documents 1 and 2
- Remarks

A person skilled in the art could have easily reached the inventions according to claims 1 to 3, 6 to 8, 11 to 13, 15, 16, 18, and 19 based on the inventions disclosed in cited documents 1 and 2.

- Claims 4, 9, and 19
- Cited Documents 1 and 2
- Remarks

Sandisk Technologies, Inc. - Ex. 1002, Page 001090

A person skilled in the art could have constituted, as necessary, a trap dense oxygen-lean oxynitride layer 518B so that it comprises a charge trap density at least 1000 times greater than an oxygen-rich oxynitride layer 518A with low trap density.

Therefore, a person skilled in the art could have easily reached the inventions according to claims 4, 9, and 17 based on the inventions disclosed in cited documents 1 and 2.

- Claims 5, 10, and 22
- Cited Documents 1 to 3
- Remarks

Cited document 3 (paragraph 0041) discloses a non-volatile semiconductor memory comprising a charge storing film including carbon in the silicon oxynitride film, and therefore a person skilled in the art could have included, as necessary, carbon in the second oxynitride layers disclosed in cited documents 1 and 2.

Therefore, a person skilled in the art could have easily reached the inventions according to claims 5, 10, and 22 based on the inventions disclosed in cited documents 1 to 3.

- Claim 14
- Cited Document 1
- Remarks

A person skilled in the art could have set, as necessary, the concentration of oxygen in the first oxynitride layer to about 35%.

Therefore, a person skilled in the art could have reached the invention according to claim 14 based on the invention disclosed in cited document 1.

- Claim 20
- Cited Documents 1, 2, and 4
- Remarks

Cited document 4 (paragraph 0033) discloses forming a tunneling silicon oxide film by ISSG oxidation of 900 °C.

Therefore, a person skilled in the art could have easily reached the invention according to claim 20 based on the inventions disclosed in cited documents 1, 2, and 4.

- Claim 21
- Cited Documents 1, 2, and 5

Sandisk Technologies, Inc. - Ex. 1002, Page 001091

- Remarks

Cited document 5 (paragraphs 0104 and 0117) discloses performing oxidation by using high density plasma treatment after forming a silicon oxynitride film.

Therefore, a person skilled in the art could have easily reached the invention according to claim 21 based on the inventions disclosed in cited documents 1, 2, and 5.

- Claim 23
- Cited Documents 1 to 3, and 6
- Remarks

Cited document 6 (paragraph 0054) discloses forming an oxynitride layer containing carbon using BTBAS and NH_3.

Therefore, a person skilled in the art could have easily reached the invention according to claim 23 based on the inventions disclosed in cited documents 1 to 3, and 6.

• Reason 3 (Support Requirements)

Claim 21 recites that "the blocking oxide layer is formed by high density plasma (HDP) oxidation of a portion of the second oxynitride layer". However, a description corresponding to the fact that a blocking oxide layer is formed by high density plasma (HDP) oxidation of a portion of the second oxynitride layer cannot be found in the specification.

Therefore, the invention according to claim 21 is not described in the detailed description of the invention.

List of Cited Documents

1. US2008/0290400
2. WO2007/064048
3. JP2009-260070A
4. JP2005-347679A
5. JP2007-318112A
6. JP2007-515060A

Record of Prior Art Documentary Search Results

- Fields of Search: IPC H01L21/336, H01L21/316, H01L21/318, H01L21/8247, H01L27/115, H01L29/788, H01L29/792

Sandisk Technologies, Inc. - Ex. 1002, Page 001092

- Request to the Applicant

Cited document 1 is a publication of an application that was filed by the same applicant or inventor as the present application, that was made available to the public at the time of filling the present application, and that can independently be a ground for denying novelty or inventive step of one or more of the claims of the present application.

It is useful for the applicant to properly evaluate the invention in advance based on such documents in order to formulate adequate claims, which also contributes to prompt and precise examination procedures. When filing an application or a request for examination, the applicant is requested to disclose such documents in the specification as prior art documents known to the applicant for proper evaluation of whether or not the invention for which a patent is sought has patentability based on these documents.

This record of this prior art documentary search results does not form part of the reason for refusal.

Family Document Information

1. US2008/0290400
   WO2008/147386
2. WO2007/064048
   US2007/064048
3. JP2009-260070A
   US2009/0261400
4. JP2005-347679A
   US2005/0272198
5. JP2007-318112A
   US2007/0252179
6. JP2007-515060B
   US2005/0109276
   WO2005/059200

Instructions in making Amendment

(1) Amended part of the description and claims, if any, must be underlined (Regulations under Patent Act, Form 13, Notes 6 and 7).

(2) Amendments must fall within the scope of the description, claims, or drawings of the original application. Further, when amending the claims, the purpose thereof is limited

Sandisk Technologies, Inc. - Ex. 1002, Page 001093

to deletion of claims, limitative restriction of claims, correction of errors in description, clarification of an ambiguous description (limited to the matters stated in the notice of reasons for refusal). In addition, the Applicant is invited to file an Argument to argue that all proposed amendments are legitimate, while indicating the relevant portions of the original specification, etc., to give particulars of the grounds upon which the amendment is sought.

(3) In amending claims, it may be advisable that amendment be made in a way pursuant to the provision under Patent Law Section 17bis(4).

Any inquiry concerning this notification or a request for an interview shall be addressed to:

Patent Examination Division 4 Electronic device Mitsuru Koyama
Phone 03 (3581) 1101 ext. 3514
Facsimile 03 (3580) 6907

Sandisk Technologies, Inc. - Ex. 1002, Page 001094

SUGIMURA
& Partners

OFFICE ACTION SUMMARY

Your Case No.: P168307.JP.01/SCHOUTEND
Patent Application No.: 2015-503338
Dispatch Date of O.A.: 21 February 2017
Due Date: 20 May 2017 in your local time (extendible up to three months)

Status: This action is non-final.

Disposition of Claims:

Claims 1-20 are pending in the application.
Claims 1-20 are as originally filed.
Claims 1-20 are rejected.

Rejected Claims:

Claims 1,8	Lack of novelty over Cited Document 1 (§29(1)(iii))
Claims 1,8	Lack of inventive step over Cited Document 1 (§29(2))
Claims 2-4	Lack of inventive step over Cited Documents 1-3 (§29(2))
Claims 5,6	Lack of inventive step over Cited Documents 1,4 (§29(2))
Claim 7	Lack of inventive step over Cited Documents 1-4 (§29(2))
Claims 9,11,14	Lack of inventive step over Cited Documents 1,4,5 (§29(2))
Claims 10,12	Lack of inventive step over Cited Documents 1-5 (§29(2))
Claim 13	Lack of inventive step over Cited Documents 1,4-7 (§29(2))
Claims 15,20	Lack of inventive step over Cited Documents 1,5 (§29(2))
Claims 16,17	Lack of inventive step over Cited Document 1,3,5 (§29(2))
Claims 18,19	Lack of inventive step over Cited Documents 1-3,5 (§29(2))
Claims 15-20	Violation of written description requirements (Clarity) (§36(6)(ii))

Cited Documents:

(Please visit the following URL: http://worldwide.espacenet.com/singleLineSearch?locale=en_EP and enter the numbers below to conduct a search) Upon your request, we will send you the cited documents.

Cited Document 1: US2011248332A1
Cited Document 2: JP2012019211A (US2012007167A1)
Cited Document 3: WO2010106922A1 (US2012068250A1)
Cited Document 4: JP2008172195A (US2008087942A1)
Cited Document 5: JP2009027134A (US2010283097A1)
Cited Document 6: JP2009295694A (US2009294836A1)
Cited Document 7: JP2009252774A (US2009242969A1)

Common Gate West Tower 36th floor, Kasumigaseki 3-2-1, Chiyoda-ku, Tokyo 100-0013 JAPAN
Telephone:81-3-3581-2241 Facsimile:81-3-3502-0031 E-mail:jpatent@sugimura.partners

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

Technology Fortune Center Suite B 1601A
8 Xueqing Road, Haidian District
Beijing 100192, PR CHINA
Tel: +86 (10) 8273-0790, (multiple lines)
Fax: +86 (10) 8273-0820, 8273-2710
Email: patent@afdip.com www.afdip.com

February 10, 2015

Xia Zheng
zhengxia@afdip.com
Tel: +86(10) 82737829
Cell: +86 13911598196

Attn.: Ms. Sinead Clark
Murgitroyd & Company-Glasgow
Scotland House, 165-169 Scotland Street
Glasgow G5 8PL
United Kingdom

Via Email Only

sinead.clark@murgitroyd.com

Re: Chinese Invention Patent Application No. 200910134374.1
In the name of Cypress Semiconductor Corporation
Title: Multiple layer oxynitride in ONO stack for improved SONOS retention
Your Ref.:123443.CN.01
Our Ref.:091202019-PET

Deadline for Responding to this Office Action: April 05, 2015 (Beijing Time)

Issue date: January 21, 2015 ; 2 month rejection

Dear Ms. Clark:

The State Intellectual Property Office of China recently has issued the Third Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below.

1. Go-beyond – Claims 1 and 7

The Examiner points out that the amendments made to claims 1 and 7 go beyond the scope recorded in the initial description and claims, and thus it is not in conformity with the provisions of Article 33 of Patent Law, since according to record of paragraph [0053] in description, the following technical features are not recorded in description and could not be determined directly and undoubtedly from the initial application documents:

"*steam annealing the second oxynitride layer to reduce a number of traps formed near a top surface thereof during a steam oxidation process used to concurrently form another oxide in a different area on the substrate*" in claim 1; and

"*a portion of the top oxynitride layer is consumed in thermally growing the second oxide layer*" in claim 7.

Regarding this issue, if the applicant thinks that the above amendments are definitely

Sandisk Technologies, Inc. - Ex. 1002, Page 001096

expressed by literal or graphic manner in the initial description, drawings and claims, or can be directly or definitely derived by a person skilled in the art on the initial description, drawings and claim as a whole, the applicant may argue, with reasonable grounds, without any further amendments.

If it is hard to persuade the Examiner, the applicant may amend the claims according to the contents literally recorded in the initial description and claims or definitely derived by a person skilled in the art on the initial description, drawings and claim as a whole.

2. Claims not Supported by the Description – Claim 1

The Examiner points out that claim 1 is not supported by the description, and thus is not in conformity with the provisions of Article 26(4) of Patent Law. The Examiner holds that according to record of examples in description (see paragraph [0050], [0051] and [0053] of its Description and Fig. 2), "*a silicon-rich, oxygen-lean first oxynitride layer*" in claim 1 is corresponding to "*bottom silicon-rich, oxygen-rich oxynitride layer 220B*" in the description, however, it is "oxygen-rich" in the description, while it is "oxygen-lean" in claim 1.

Regarding the issue that claim 1 is not supported by the description, we would like to bring the related regulations to your attention first. Please be advised that a claim being supported by the description here means that a person skilled in the art can reasonably obtain or generalize its technical scheme from the sufficiently disclosed contents of the description, pursuant to the provisions of Article 26(4) of Patent Law. If a person skilled in the art can reasonably predict that all the equivalents or obvious variants of the embodiments set forth in the description have the same properties or uses, the generalization of a claim can cover all the equivalents or obvious variants.

If the applicant wants to argue without any further amendment for this issue, it is suggested to argue, with reasonable grounds, why actually a person skilled in the art can reasonably obtain or generalize its technical scheme from the sufficiently disclosed contents of the description. For example, a person skilled in the art can reasonably predict that all the equivalents or obvious variants of the embodiments set forth in the description have the same properties or uses, the generalization of a claim can cover all the equivalents or obvious variants.

If it is hard to persuade the Examiner, then the applicant may amend the claim to narrow the scope.

3. Go-beyond – Claim 7

The Examiner points out that the amendments made to claim 7 go beyond the scope recorded in the initial description and claims, and thus it is not in conformity with the provisions of Article 33 of Patent Law, since according to record of paragraph [0054] in description, the technical feature of "*a thickness of the top oxynitride layer is greater than a thickness of the bottom oxynitride layer*" in claim 7 is generalization of initial recorded content.

Sandisk Technologies, Inc. - Ex. 1002, Page 001097

4. Improper Amendments – Claim 14

The Examiner points out that claim 14 is not in conformity with the provisions of Rule 51(3) of the Implementing Regulations of Patent Law since the technical scheme defined in such claim does not appear in the initial claims.

5. Based on the contents recorded in the initial description, the assumed comments on claims 1-13 are as followings:

5-1. Novelty – Claim 1

The Examiner points out that claim 1 does not possess novelty over Reference 1 (US2008/0290400A1, November 27, 2008), and thus is not in conformity with the provisions of Article 22(2) of Patent Law, since Reference 1 (paragraphs 0037, 0041, 0057, 0059 and 0060 of its Description, Claim 5 and Figs. 5 and 8A) discloses all technical features of the technical scheme in claim 1.

To overcome this issue, generally it is suggested to find the distinguishing technical features of the technical scheme of claim 1 from the technical scheme of Reference 1, or amend the technical scheme of claim 1 to include any distinguishing technical feature(s). If the present application and Reference 1 are in the different technical fields or the disclosure of Reference 1 cannot yield the same effect as the technical scheme of claim 1, please indicate so in the response.

Additionally, according to Chinese practice, on the basis that the novelty of a claim has been proved, it is also necessary to prove its inventiveness as the second step.

For the inventiveness, it is suggested to argue that the distinguishing technical features, found or included as in the above step, in claim 1 is non-obvious to a person skilled in the art and could produce advantageous technical effect as compared with the prior art.

In addition, if the followings exist for this invention, it is helpful to include them into the response:

- a person skilled in the art is hard to create the technical scheme of this invention due to some technical difficulties, technical prejudice or misleading from common thoughts;
- this invention brings unanticipated technical effects;
- this invention brings unanticipated success in the market; and
- other similar situations, such as long-felt but unsolved needs, failure of others.

Please consider the above information, analyze and give us your instruction. If you need any assistance, please let us know. We would be happy to assist.

5-2. Novelty – Claims 2-3

The Examiner points out that claims 2-3 do not possess novelty on the condition that claim 1 they refer to does not possess novelty since the additional technical features of claims 2-3 are disclosed by Reference 1 (see paragraph 0035 of its Description).

Sandisk Technologies, Inc. - Ex. 1002, Page 001098

5-3. Novelty – Claim 4

The Examiner points out that claim 4 does not possess novelty on the condition that claim 3 it refers to does not possess novelty since Reference 1 (see paragraph 0057 of its Description) discloses the relevant technical features of claim 4.

5-4. Novelty – Claim 5

The Examiner points out that claim 5 does not possess novelty on the condition that claim 4 it refers to does not possess novelty since the additional technical feature of claim 5 is disclosed by Reference 1 (see paragraph 0058 of its Description).

5-5. Novelty – Claim 6

The Examiner points out that claim 6 does not possess novelty on the condition that claim 4 it refers to does not possess novelty since the additional technical feature of claim 6 is disclosed by Reference 1 (see paragraph 0057 of its Description).

The solution for the novelty issue in the above groups of claims depends on the solution for claim 1, to argue or let claim 1 have novelty and inventiveness. Once claim 1 has novelty and inventiveness, all above dependent claims would have novelty and inventiveness too.

5-6. Novelty – Claim 7

The Examiner points out that claim 7 does not possess novelty over Reference 1, and thus is not in conformity with the provisions of Article 22(2) of Patent Law, since Reference 1 (paragraphs 0029-0030, 0039, 0041, 0056-0057 and 0059 of its Description and Figs. 5 and 8A) discloses all technical features of the technical scheme in claim 7.

To overcome this issue, you may follow the above similar suggestion as for claim 1.

5-7. Novelty – Claims 8-10

The Examiner points out that claims 8-10 do not possess novelty on the condition that the claims they refer to do not possess novelty since the additional technical features of claims 8-10 are disclosed by Reference 1 (see paragraph 0035 of its Description).

5-8. Novelty – Claim 11

The Examiner points out that claim 11 does not possess novelty on the condition that claim 9 it refers to does not possess novelty since the additional technical feature of claim 11 is disclosed by Reference 1 (see paragraphs 0047 and 0053 of its Description).

5-9. Novelty – Claim 12

The Examiner points out that claim 12 does not possess novelty on the condition that claim 9 it refers to does not possess novelty since Reference 1 (see paragraph 0057 of its

Sandisk Technologies, Inc. - Ex. 1002, Page 001099

Description) discloses the relevant technical features of claim 12.

5-10. Novelty – Claim 13

The Examiner points out that claim 13 does not possess novelty on the condition that claim 7 it refers to does not possess novelty since the additional technical feature of claim 13 is disclosed by Reference 1 (see paragraph 0057 of its Description).

The solution for the novelty issue in the above groups of claims depends on the solution for claim 7, to argue or let claim 7 have novelty and inventiveness. Once claim 7 has novelty and inventiveness, all above dependent claims would have novelty and inventiveness too.

Conclusive opinion

Based on the above opinions, the Examiner also holds, as marked in the form of this Office Action, that the application does not possess any patentable substantial contents, and if the applicant fails to expound reasons or the reasons expounded are not sufficient, this application will be rejected.

This generally is a conclusive opinion of the Examiner and in next the Examiner is likely to issue a final rejection if the response to this Action is not persuasive or no substantial amendments are made.

Please note that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. In China, whether an amendment goes beyond the scope is a big issue, and the examiners will examine this issue strictly, much more strictly than examiners in many other countries. And the scope recorded in the initial description and claims, according to the Examination Guidelines, includes contents found literally in the initial description and claims or determined directly and undoubtedly from the drawings and the contents literally recorded in the initial description and claims. Additionally, recently the Supreme Court corrects the strict ruling on the go-beyond issue of the State IP Office in one case and holds that the scope recorded in the initial description and claims should include (1) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims, and (2) contents directly or definitely derived by a person skilled in the art on the initial description, drawings and claim as a whole. Under such a circumstance, Chinese examiners may adjust their rules for such go-beyond issue.

A response and possible amendments must be submitted to the Office by **April 05, 2015 (Beijing Time)**. Please give us your further instructions as soon as possible.

The above official deadline can be extended once for one or two months. The cost for a one month extension is RMB940.00 (around US$150.00), including the official fee of RMB300.00 and an attorney fee of RMB640.00. The cost for a two-month extension is RMB1240.00 (around US$200.00), including the official fee of RMB600.00 and an attorney fee of RMB640.00.

Sandisk Technologies, Inc. - Ex. 1002, Page 001100

We also list the related regulations below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your prompt reply is highly appreciated.

Please kindly confirm receipt of this letter by return e-mail.

Sincerely yours,
AFD China Intellectual Property



Xia Zheng (patent@afdip.com)

/Lhm/Lqh

Enclosure: A copy of the Chinese Notification of the Third Office Action (5 pages-by E-mail Only).

Patent Law:

Article 22(2): Novelty means that, the invention or utility model does not form part of the prior art; nor has any entity or individual filed previously before the date of filing with the Patent Administration Department Under the State Council an application relating to the identical invention or utility model disclosed in patent application documents published or patent documents announced after the said date of filing.

Article 26(4): The claims shall be supported by the description and shall define the extent of the patent protection sought for in a clear and concise manner.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

Sandisk Technologies, Inc. - Ex. 1002, Page 001101

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

Technology Fortune Center Suite B 1601A
8 Xueqing Road, Haidian District
Beijing 100192, PR CHINA
Tel: +86 (10) 8273-0790, (multiple lines)
Fax: +86 (10) 8273-0820, 8273-2710
Email: patent@afdip.com www.afdip.com

February 24, 2016

Xia Zheng
zhengxia@afdip.com
Tel: +86(10) 82737829
Cell: +86 13911598196

Attn.:Ms. Flora Hachemi
Murgitroyd & Company-Glasgow
Scotland House, 165-169 Scotland Street
Glasgow G5 8PL
United Kingdom

Via Email Only

flora.hachemi@murgitroyd.com

Re: Chinese Invention Patent Application No. 200910134374.1
In the name of Cypress Semiconductor Corporation
Title: Multiple layer oxynitride in ONO stack for improved SONOS retention
Your Ref.:123443.CN.01
Our Ref.:091202019-PET

Deadline for Responding to this Office Action: April 18, 2016 (Beijing Time)

Issue date: February 03, 2016; 2 Months Rejection

Dear Ms. Hachemi:

The State Intellectual Property Office of China recently has issued the Fifth Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below.

1. Unclear Scope – Claim 7

The Examiner points out that the scope of claim 7 is unclear since the wording "the top oxynitride layer" in claim 7 lacks reference basis, and thus claim 7 is not in conformity with the provisions of Article 26(4) of Patent Law.

Please be advised that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. The Office currently examines go-beyond issue very strictly, more strictly than that in many other countries. The "scope recorded in the initial description and claims", pursuant to the Patent Examination Guidelines, includes (1) literal contents of the initial description and claims, and (2) contents determined directly and undoubtedly from the drawings and the literal contents of the initial description and claims.

According to the Supreme Court's ruling in one recent case, such "scope" should include

Sandisk Technologies, Inc. - Ex. 1002, Page 001102

(i) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims of the application, and (ii) contents directly or definitely derived by a person skilled in the art from the initial description, drawings and claims as a whole, which should correct the strict rules of the Office. However, in practice, examiners are still likely to examine the go-beyond issue strictly. The applicant had better take this in mind if deciding to make any amendments.

A response and possible amendments must be submitted to the Office by **April 18, 2016 (Beijing Time)**. Please give us your further instructions as soon as possible.

The above official deadline can be extended once for one or two months. The cost for a one month extension is RMB940.00 (around US$150.00), including the official fee of RMB300.00 and an attorney fee of RMB640.00. The cost for a two-month extension is RMB1240.00 (around US$200.00), including the official fee of RMB600.00 and an attorney fee of RMB640.00.

We also list the related regulations below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your prompt reply is highly appreciated.

Please kindly confirm receipt of this letter by return e-mail.

Sincerely yours,
AFD China Intellectual Property



Xia Zheng (patent@afdip.com)

/Lhm/Zf
Enclosure: (by E-mail only)
A copy of the Chinese Notification of the Fifth Office Action.

Patent Law:

Article 26(4): The claims shall be supported by the description and shall define the extent of the patent protection sought for in a clear and concise manner.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

Sandisk Technologies, Inc. - Ex. 1002, Page 001103

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

Technology Fortune Center Suite B 1601A
8 Xueqing Road, Haidian District
Beijing 100192, PR CHINA
Tel: +86 (10) 8273-0790, (multiple lines)
Fax: +86 (10) 8273-0820, 8273-2710
Email: patent@afdip.com www.afdip.com

August 19, 2014

Xia Zheng
zhengxia@afdip.com
Tel: +86(10) 82737829
Cell: +86 13911598196

Attn.: Ms. Sinead Clark
Cc: Mr. Larry Johnson
Ms. Penny Jackson
Murgitroyd & Company-Glasgow
Scotland House, 165-169 Scotland Street
Glasgow G5 8PL
United Kingdom

Via Email Only

sinead.clark@murgitroyd.com
larz@cypress.com
pbj@cypress.com

Re: Chinese Invention Patent Application No.: 200910134374.1
In the name of Cypress Semiconductor Corporation
Title: Multiple layer oxynitride in ONO stack for improved SONOS retention
Your Ref.: 123443.CN.01
Our Ref.: 091202019-PET

Deadline for Responding to this Office Action: October 13, 2014 (Beijing Time)

Dear Ms. Clark:

In connection with the captioned application, the State Intellectual Property Office of China has recently issued the Second Office Action. According to your instruction, we would like to summarize the Examiner's objections stated in this office action as below.

1. The technical scheme of claims 1, 11 and 14 are not supported by the description and are not in conformity with the provisions of Article 26(4) of Patent Law.

The technical scheme "蒸气(steam)退火" recorded in claims 1, 11 and 14 is different from the technical scheme "蒸汽(steam)退火" recorded in the specific embodiment of the description (see paragraphs 0044, 0048, 0053 of the description)*[AFD Remarks: Such issue is caused by the inconsistent translation for the word "steam" by the former agency. We will unify the Chinese translation when responding this OA to address this issue.]*

2. The technical scheme of claim 1 is not supported by the description and is not in conformity with the provisions of Article 26(4) of Patent Law. The technical scheme recorded in claim 1, i.e., "depositing on a substrate a silicon-rich nitride;

oxidizing the silicon-rich nitride to form a silicon-rich, oxygen-lean first oxynitride layer;

forming a second oxynitride layer over a surface of the first oxynitride layer to form a

Sandisk Technologies, Inc. - Ex. 1002, Page 001104

multi-layer charge storing layer", is different from the technical scheme recorded in the specific embodiments of the description (see paragraphs 0050, 0051 of the description).

3. The technical scheme of claim 1 is not supported by the description and is not in conformity with the provisions of Article 26(4) of Patent Law. The technical scheme recorded in claim 1 *[sic]*, i.e., "the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH_2Cl_2)/ammonia (NH_3) mixture and a nitrous oxide (N_2O)/NH3 mixture at a ratio of 8:1, and the second oxynitride layer is formed in a CVD process using a process gas comprising a N_2O/NH_3 mixture and a SiH_2Cl_2/NH_3 mixture at a ratio of 5:1", is different from the technical scheme recorded in the specific embodiments of the description (see paragraphs 0050, 0051 of the description).

Based on the similar reasons, claim 12 is not supported by the description and is not in conformity with the provisions of Article 26(4) of Patent Law.

4. Even if the claims are amended according to the technical scheme recorded in the specific embodiments of the description, the claims do not possess novelty and inventiveness.

4-1. Claim 1 seeks protection for a method of forming a charge storing layer of a semiconductor device. Reference 1 (US2008/0290400A1) discloses a method of forming a charge storing layer of a semiconductor device, wherein (see paragraphs 0037, 0057 of the description, claim 1 and FIG. 5) discloses the following technical contents: depositing on a substrate a silicon-rich oxygen-rich oxynitride layer 518A in a low pressure CVD, depositing on a silicon-rich oxygen-rich oxynitride layer 518A a silicon-rich oxygen-lean oxynitride layer 518B, the silicon-rich oxygen-rich oxynitride layer 518A and silicon-rich oxygen-lean oxynitride layer 518B constitute a multi-layer charge trapping layer; a top portion of silicon-rich oxygen-rich oxynitride layer 518 is oxidized or reoxidized which may prevent trap migration to the interface between the charge trapping layer and the blocking layer (see paragraph 0041 of the description and FIG. 8A), and the reoxidation may select steam as an oxidizing agent (see paragraph 0060 of the description), i.e., analogous to steam annealing the second oxynitride layer to reduce a number of traps formed near a top surface thereof in the present application. As can be seen, all the features of claim 1 is disclosed by Reference 1, the two belong to the same technical field, adopt the same technical scheme, solve the same technical problem and achieve the same effect. Thus, claim 1 does not possess novelty under Article 22(2) of Patent Law.

4-2. The additional technical features of claims 2-3 are disclosed by Reference 1 (see paragraph 0035 of the description). Thus, where the cited claim does not possess novelty, the above claims do not possess novelty.

4-3. The additional technical feature of claim 4 is disclosed by Reference 1 (see paragraph 0057 of the description). Thus, where the cited claim does not possess novelty, the above claim does not possess novelty.

4-4. The additional technical feature of claim 5 is disclosed by Reference 1 (see

Sandisk Technologies, Inc. - Ex. 1002, Page 001105

paragraph 0058 of the description). Thus, where the cited claim does not possess novelty, the above claim does not possess novelty.

4-5. The additional technical feature of claim 6 is disclosed by Reference 1 (see paragraph 0057 of the description). Thus, where the cited claim does not possess novelty, the above claim does not possess novelty.

4-6. Claim 7 seeks protection for a method of forming a semiconductor device including an oxide-nitride-oxide (ONO) structure. Reference 1 (US2008/0290400A1) discloses a method of forming a semiconductor device including an oxide-nitride-oxide (ONO) structure, wherein (see paragraphs 0029-0030 of the description and FIG. 5) specifically discloses the following technical features: forming a nitridized oxide layer 516 of the ONO structure, forming a two-layer charge storing layer comprising the silicon-rich oxygen-rich oxynitride layer 518A and silicon-rich oxygen-lean oxynitride layer 518B on nitridized oxide layer 516, wherein the silicon-rich oxygen-rich oxynitride layer 518A is formed using a process of chemical vapor deposition using a process gas comprising a first gas mixture of N2O and NH3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of SiH_2Cl_2 and NH3 mixed in a ratio of from about 1:7 to about 7:1, the silicon-rich oxygen-lean oxynitride layer 518B is formed using a process of chemical vapor deposition, wherein its process gas a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of SiH2Cl2 and NH3 mixed in a ratio of from about 1:7 to about 7:1 (see paragraph 0057 of the description), multiple nitride or oxynitride charge trapping layers are formed at operations 902 and 904 in a low pressure CVD process using ND_3 to replace NH_3 (see paragraph 0056 of the description); oxide layer 520 is formed on the charge trapping layer 518B. As can be seen, all the features of claim 7 is disclosed by Reference 1, the two belong to the same technical field, adopt the same technical scheme, solve the same technical problem and achieve the same effect. Thus, claim 7 does not possess novelty under Article 22(2) of Patent Law.

4-7./4-8./4-9./4-10. The additional technical features of claims 8-13 are disclosed by Reference 1 (see paragraphs 0035, 0047, 0053, and 0057 of the description). Thus, where the cited claims do not possess novelty, the above claims do not possess novelty.

4-11. Claim 14 seeks protection for a method of forming a semiconductor device including an oxide-nitride-oxide (ONO) structure *[sic]*. Reference 1 (US2008/0290400A1) discloses a method of forming a semiconductor device including an oxide-nitride-oxide (ONO) structure, wherein (see paragraphs 0029-0030 of the description and FIG. 5) specifically discloses the following technical features: forming a nitridized oxide layer 516 of the ONO structure, forming a two-layer charge storing layer comprising the silicon-rich oxygen-rich oxynitride layer 518A and silicon-rich oxygen-lean oxynitride layer 518B on nitridized oxide layer 516, wherein the silicon-rich oxygen-rich oxynitride layer 518A is formed using a process of chemical vapor deposition using a process gas comprising a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of SiH_2Cl_2 and NH_3 mixed in a ratio of from about 1:7 to about 7:1, the silicon-rich oxygen-lean oxynitride layer 518B is formed using a process of chemical vapor deposition, wherein its

Sandisk Technologies, Inc. - Ex. 1002, Page 001106

process gas a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of SiH_2Cl_2 and NH_3 mixed in a ratio of from about 1:7 to about 7:1 (see paragraph 0057 of the description), multiple nitride or oxynitride charge trapping layers are formed at operations 902 and 904 in a low pressure CVD process using ND_3 to replace NH_3 (see paragraph 0056 of the description); oxide layer 520 is formed on the charge trapping layer 518B. As can be seen, all the features of claim 14 is disclosed by Reference 1, the two belong to the same technical field, adopt the same technical scheme, solve the same technical problem and achieve the same effect. Thus, claim 14 does not possess novelty under Article 22(2) of Patent Law.

4-12./4-13./4-14. The additional technical features of claims 15-17 are disclosed by Reference 1 (see paragraphs 0035, 0036, and 0039 of the description). Thus, where the cited claim does not possess novelty, claims 15 and 17 do not possess novelty; where the cited claim does not possess novelty, claim 16 does not possess inventiveness.

Please note that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. In China, whether an amendment goes beyond the scope is a big issue, and the examiners will examine this issue strictly, much stricter than examiners in many other countries. And the scope recorded in the initial description and claims, according to the Examination Guidelines, includes contents found literally in the initial description and claims or determined directly and undoubtedly from the drawings and the contents literally recorded in the initial description and claims. Additionally, recently the Supreme Court corrects the strict ruling on the go-beyond issue of the State IP Office in one case and holds that the scope recorded in the initial description and claims should include (1) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims, and (2) contents directly or definitely derived by a person skilled in the art on the initial description, drawings and claim as a whole. Under such a circumstance, Chinese examiners may adjust their rules for such go-beyond issue.

A response and possible amendments must be submitted to the Office by **October 13, 2014(Beijing Time)**. Please give us your further instructions as soon as possible.

The above official deadline can be extended once for one or two months. The cost for a one month extension is RMB940.00, including the official fee of RMB300.00 and an attorney fee of RMB640.00. The cost for a two-month extension is RMB1240.00, including the official fee of RMB600.00 and an attorney fee of RMB640.00.

Please kindly note that our invoice for reporting this action will be sent to you in another our separate email.

Our other invoices for future prosecution of this application may also be sent to you separately after the completion of our reports in order to match our new invoice management policy. Your support and patience for our new policy will be very much appreciated. And we hope to make the transition for our new policy as smooth and seamless as possible.

Sandisk Technologies, Inc. - Ex. 1002, Page 001107