We also list related rules of Chinese Patent Law below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your promptly reply is highly appreciated.

Please kindly confirm receipt of this letter by fax or e-mail.

Sincerely yours,
AFD China Intellectual Property



Xia Zheng (patent@afdip.com)

/Zlx/Zxk

Enclosures:
The Notification of the Second Office Action (6 pages- by E-mail Only);

Patent Law:

Article 22(2): Novelty means that, the invention or utility model does not form part of the prior art; nor has any entity or individual filed previously before the date of filing with the Patent Administration Department Under the State Council an application relating to the identical invention or utility model disclosed in patent application documents published or patent documents announced after the said date of filing.

Article 22(3): Inventiveness means that, as compared with the prior art, the invention has prominent substantive features and represents a notable progress, and that the utility model has substantive features and represents progress.

Article 26(4): The claims shall be supported by the description and shall define the extent of the patent protection sought for in a clear and concise manner.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

Sandisk Technologies, Inc. - Ex. 1002, Page 001108

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August 11, 2015

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Attn.: Ms. Flora Hachemi
Murgitroyd & Company-Glasgow
Scotland House, 165-169 Scotland Street
Glasgow G5 8PL
United Kingdom

Via Email Only

flora.hachemi@murgitroyd.com

Re: Chinese Invention Patent Application No. 200910134374.1
In the name of Cypress Semiconductor Corporation
Title: Multiple layer oxynitride in ONO stack for improved SONOS retention
Your Ref.:123443.CN.01
Our Ref.:091202019-PET

Deadline for Responding to this Office Action: October 14, 2015 (Beijing Time)

Issue date: July 30, 2015; 2 month rejection

Dear Ms. Hachemi:

The State Intellectual Property Office of China recently has issued the Fourth Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below.

1. Go-beyond – Claim 7

The Examiner points out that the amendment made to claim 7 go beyond the scope recorded in the initial description and claims, and thus it is not in conformity with the provisions of Article 33 of Patent Law, since the wording "*a thickness of the top oxynitride layer is greater than a thickness of the bottom oxynitride layer*" is generalization from the initial disclosure.

The applicant submitted that according to the corresponding content in paragraph [0054] of the initial description, a person skilled in the art can directly and undoubtedly determine that a thickness of the top oxynitride layer is greater than a thickness of the bottom oxynitride layer 220B.

For this, the Examiner holds that: first, the initial description and claims of the present

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application do not literally record "a thickness of the top oxynitride layer is greater than a thickness of the bottom oxynitride layer"; secondly, "a thickness of the top oxynitride layer is greater than a thickness of the bottom oxynitride layer" protects the thickness ratio that is not recorded in the examples of the initial description, and protects the technical scheme that is not recorded in the initial application, and thus the amendment goes beyond the scope.

Please be advised that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. The Office currently examines go-beyond issue very strictly, more strictly than that in many other countries. The "scope recorded in the initial description and claims", pursuant to the Patent Examination Guidelines, includes (1) literal contents of the initial description and claims, and (2) contents determined directly and undoubtedly from the drawings and the literal contents of the initial description and claims.

According to the Supreme Court's ruling in one recent case, such "scope" should include (i) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims of the application, and (ii) contents directly or definitely derived by a person skilled in the art from the initial description, drawings and claims as a whole, which should correct the strict rules of the Office. However, in practice, examiners are still likely to examine the go-beyond issue strictly. The applicant had better take this in mind if deciding to make any amendments.

A response and possible amendments must be submitted to the Office by **October 14, 2015 (Beijing Time)**. Please give us your further instructions as soon as possible.

The above official deadline can be extended once for one or two months. The cost for a one month extension is RMB940.00 (around US$150.00), including the official fee of RMB300.00 and an attorney fee of RMB640.00. The cost for a two-month extension is RMB1240.00 (around US$200.00), including the official fee of RMB600.00 and an attorney fee of RMB640.00. We also list the related regulations below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your prompt reply is highly appreciated.

Please kindly confirm receipt of this letter by return e-mail.

Sincerely yours,
AFD China Intellectual Property



Xia Zheng (patent@afdip.com)

/Lc/Lxq

Sandisk Technologies, Inc. - Ex. 1002, Page 001110

Enclosure: A copy of the Chinese Notification of the Fourth Office Action (3 pages-by E-mail Only).

Patent Law:

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

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October 22, 2013

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United Kingdom

Via Email Only
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Re: Chinese Invention Patent Application No.: 200910134374.1
In the name of Cypress Semiconductor Corporation
Title: Multiple layer oxynitride in ONO stack for improved SONOS retention
Your Ref.: 123443.CN.01
Our Ref.: 091202019-PT

Deadline for Responding to this Office Action: February 07, 2014 (Beijing Time)

Dear Ms. Clark:

In connection with the captioned application, the State Intellectual Property Office of China has issued the First Office Action. According to your instruction, we would like to summarize the Examiner's objections stated in this office action as below.

I. Claims 1-5, 9-13, 16-18 and 20 do not possess novelty under Article 22(2) of Patent Law.

1. As to claim 1

Reference1 (US2008/0290400A1) discloses a forming method for the charge storage layer in semiconductor device, wherein (paragraphs 0037, 0057 of the description, claim 5 and FIG 5) discloses the following technical contents: depositing a silicon-rich silicon nitride on the substrate, oxidizing the silicon-rich silicon nitride to form silicon-rich, nitrogen-rich, mionectic silicon oxynitride layer 518B. As can be seen, all the technical features of claim 1 have already been disclosed by Reference 1. Both of them belong to the same technical field, adopt the same technical scheme, solve the same technical problem, and have the same predicted effect. Therefore, claim 1 does not possess novelty under Article 22(2) of Patent Law.

2. As to claim 9

Reference 1 (US2008/0290400A1) discloses a forming method for a semiconductor

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device of an oxide-nitride-oxide (ONO), wherein (paragraphs 0029-0030 of the description and FIG 5) discloses the following technical contents: nitride-oxide layer 516 which forms ONO structure; a plurality of charge trapping layers 518A and 518B comprising nitride are formed on nitride-oxide layer 516; a oxide layer 520 is formed on the charge trapping layers 518B. As can be seen, all the technical features of claim 9 have already been disclosed by Reference 1. Both of them belong to the same technical field, adopt the same technical scheme, solve the same technical problem, and have the same predicted effect. Therefore, claim 9 does not possess novelty under Article 22(2) of Patent Law.

3. As to claim 17

Reference 1 (US2008/0290400A1) discloses a semiconductor device of an oxide-nitride-oxide (ONO), wherein (paragraphs 0029-0030 of the description and FIG 5) discloses the following technical contents: nitride-oxide layer 516 which forms ONO structure; a plurality of charge trapping layers 518A and 518B comprising nitride are formed on nitride-oxide layer 516; a oxide layer 520 is formed on the charge trapping layers 518B. As can be seen, all the technical features of claim 17 have already been disclosed by Reference 1. Both of them belong to the same technical field, adopt the same technical scheme, solve the same technical problem, and have the same predicted effect. Therefore, claim 17 does not possess novelty under Article 22(2) of Patent Law.

4. As to claims 2-5, 10-13, 16, 18 and 20

The additional technical features of claims 2-5, 10-13, 16, 18 and 20 have already been disclosed by Reference 1. Where the cited claim does not possess novelty, claims 2-5, 10-13, 16, 18 and 20 do not possess novelty under Article 22(2) of Patent Law, either.

II. Claims 6-8, 14, 15 and 19 do not possess inventiveness under Article 22(3) of Patent Law

1. As to claims 6, 8, 15 and 19

The additional technical features of claims 6, 8, 15 and 19 have already been disclosed by Reference 1;

2. As to claims 7 and 14

The additional technical features of claims 7 and 14 are the conventional technical means in the art.

Therefore, where the cited claim does not possess novelty or inventiveness, claims 6-8, 14, 15 and 19 do not possess inventiveness under Article 22(3) of Patent Law

Please note that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. In China, whether an

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amendment goes beyond the scope is a big issue, and the examiners will examine this issue strictly, much stricter than examiners in many other countries. And the scope recorded in the initial description and claims, according to the Examination Guidelines, includes contents found literally in the initial description and claims or determined directly and undoubtedly from the drawings and the contents literally recorded in the initial description and claims. Additionally, recently the Supreme Court corrects the strict ruling on the go-beyond issue of the State IP Office in one case and holds that the scope recorded in the initial description and claims should include (1) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims, and (2) contents directly or definitely derived by a person skilled in the art on the initial description, drawings and claim as a whole. Under such a circumstance, Chinese examiners may adjust their rules for such go-beyond issue.

A response and possible amendments must be submitted to the Office by **February 07, 2014 (Beijing Time)**. Please give us your further instructions as soon as possible. The above official deadline can be extended once for one or two months. The cost for a one month extension is RMB940.00, including the official fee of RMB300.00 and an attorney fee of RMB640.00. The cost for a two-month extension is RMB1240.00, including the official fee of RMB600.00 and an attorney fee of RMB640.00.

In addition, the Examiner added a Search Report as the attachment of this Office Action. Kindly inform us if you would like us to translate the Report. The fee for translating the Report will be US$50.00.

Please kindly note that our invoice for reporting this action will be sent to you in another our separate email.

Our other invoices for future prosecution of this application may also be sent to you separately after the completion of our reports in order to match our new invoice management policy. Your support and patience for our new policy will be very much appreciated. And we hope to make the transition for our new policy as smooth and seamless as possible.

We also list related rules of Chinese Patent Law below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your promptly reply is highly appreciated.

Please kindly confirm receipt of this letter by fax or e-mail.

Sincerely yours,
AFD China Intellectual Property



Xia Zheng (patent@afdip.com)

/Mxf/Znx

Enclosures: (All by E-mail Only)
1. The Notification of the First Office Action (7 pages); and
2. Our invoice No. IP201312441 (1 page, to be sent to you later in our separate email).

Patent Law:

Article 22(2): Novelty means that, the invention or utility model does not form part of the prior art; nor has any entity or individual filed previously before the date of filing with the Patent Administration Department Under the State Council an application relating to the identical invention or utility model disclosed in patent application documents published or patent documents announced after the said date of filing.

Article 22(3): Inventiveness means that, as compared with the prior art, the invention has prominent substantive features and represents a notable progress, and that the utility model has substantive features and represents progress.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

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April 23, 2015

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United Kingdom

Via Email Only

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Re: National Phase in China of PCT/US2012/021583
In the name of Cypress Semiconductor Corporation
Title: Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers
CN Application No.: 201280000107.5
Your Ref.:123443.CN.02 Cypress Ref.: PM07002CIP1CN
Our Ref.:081306522-ET

Deadline for Responding to this Office Action: June 16, 2015 (Beijing Time)

Dear Ms. Clark:

The State Intellectual Property Office of China recently has issued the Second Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below.

1. Novelty – Claim 1

The Examiner points out that claim 1 does not possess novelty over Reference 1 (CN101517714A, August 26, 2009), and thus is not in conformity with the provisions of Article 22(2) of Patent Law, since Reference 1 (see pages 8-14 of its Description and Fig.5) discloses all technical features of the technical scheme in claim 1.

To overcome this issue, generally it is suggested to find the distinguishing technical features of the technical scheme of claim 1 from the technical scheme of Reference 1, or amend the technical scheme of claim 1 to include any distinguishing technical feature(s). If the present application and Reference 1 are in the different technical fields or the disclosure of Reference 1 cannot yield the same effect as the technical scheme of claim 1, please indicate so in the response.

Additionally, according to Chinese practice, on the basis that the novelty of a claim has

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been proved, it is also necessary to prove its inventiveness as the second step.

For the inventiveness, it is suggested to argue that the distinguishing technical features, found or included as in the above step, in claim 1 is non-obvious to a person skilled in the art and could produce advantageous technical effect as compared with the prior art.

In addition, if the followings exist for this invention, it is helpful to include them into the response:

- a person skilled in the art is hard to create the technical scheme of this invention due to some technical difficulties, technical prejudice or misleading from common thoughts;
- this invention brings unanticipated technical effects;
- this invention brings unanticipated success in the market; and
- other similar situations, such as long-felt but unsolved needs, failure of others.

Please consider the above information, analyze and give us your instruction. If you need any assistance, please let us know. We would be happy to assist.

2. Inventiveness – Claim 2

The Examiner points out that claim 2 does not possess inventiveness on the condition that claim 1 it refers to does not possess novelty and thus is not in conformity with the provisions of Article 22(2) of Patent Law, since the additional technical feature of claim 2 can be easily obtained by a person skilled in the art over the technical teaching provided by disclosure of Reference 1.

3. Inventiveness – Claims 3-5

The Examiner points out that claims 3-5 do not possess inventiveness on the condition that claim 2 they refer to does not possess novelty or inventiveness since the additional technical features of claims 3-5 can be easily obtained by a person skilled in the art over the technical teaching provided by disclosure of Reference 1.

4. Inventiveness – Claim 6

The Examiner points out that claim 6 does not possess inventiveness on the condition that claim 2 it refers to does not possess inventiveness since the additional technical feature of claim 6 can be easily obtained by a person skilled in the art over the technical teaching provided by disclosure of Reference 1 (see paragraph 12 of its Description).

5. Inventiveness – Claim 7

The Examiner points out that claim 7 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness [*sic, novelty*] since the additional technical feature of claim 7 can be easily obtained by a person skilled in the art over the technical teaching provided by disclosure of Reference 1.

6. Inventiveness – Claim 8

The Examiner points out that claim 8 does not possess inventiveness on the condition that claim 1 it refers to does not possess novelty, since Reference 1 discloses the relevant technical feature, and it can be easily obtained by a person skilled in the art through limited times of experiment to select the ratio of mixtures with small range from the ratio of mixtures with large range.

7. Inventiveness – Claim 9

The Examiner points out that claim 9 does not possess inventiveness on the condition that claim 8 it refers to does not possess inventiveness since the additional technical feature of claim 9 is disclosed by Reference 1 (see page 14 of its Description).

8. Inventiveness – Claim 10

The Examiner points out that claim 10 does not possess inventiveness on the condition that claim 1 it refers to does not possess novelty since the additional technical feature of claim 10 is conventional technical means in the art.

9. Novelty – Claim 11

The Examiner points out that claim 11 does not possess novelty on the condition that claim 1 it refers to does not possess novelty and disclosed by Reference 1 (see the last paragraph on page 14 of its Description) discloses the relevant technical features of claim 11.

10. Inventiveness – Claim 12

The Examiner points out that claim 12 does not possess inventiveness on the condition that claim 1 it refers to does not possess novelty since the additional technical feature of claim 12 is conventional choice of a person skilled in the art.

11. Novelty – Claim 13

The Examiner points out that claim 13 does not possess novelty on the condition that claim 1 it refers to does not possess novelty and Reference 1 discloses the relevant technical features of claim 13.

12. Inventiveness – Claim 14

The Examiner points out that claim 14 does not possess inventiveness either. The Examiner holds that Reference 3 (CN 101859702A, October 13, 2010) discloses the relevant technical feature (see paragraph 53 of its Description), according to technical teaching provided by Reference 3, a person skilled in the art can easily conceive of using the steam annealing process in Reference 1. And thus on the basis of Reference 1 in combination of Reference 2, the technical scheme of claim 14 is obvious to a person skilled in the art.

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Additionally, the Examiner points out that Reference 3 (see paragraph 58 of its Description) discloses that during the process of heat energy oxidation generating blocking oxide layer, the topmost oxynitride is consumed and oxidated efficiently.

The solution for the novelty issue in the above groups of claims depends on the solution for claim 1, to argue or let claim 1 have novelty and inventiveness. Once claim 1 has novelty and inventiveness, all above dependent claims would have novelty and inventiveness too.

Conclusive opinion

Based on the above opinions, the Examiner also holds, as marked in the form of this Office Action, that the application does not possess any patentable substantial contents, and if the applicant fails to expound reasons or the reasons expounded are not sufficient, this application will be rejected.

This generally is a conclusive opinion of the Examiner and in next the Examiner is likely to issue a final rejection if the response to this Action is not persuasive or no substantial amendments are made.

Please note that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. In China, whether an amendment goes beyond the scope is a big issue, and the examiners will examine this issue strictly, much more strictly than examiners in many other countries. And the scope recorded in the initial description and claims, according to the Examination Guidelines, includes contents found literally in the initial description and claims or determined directly and undoubtedly from the drawings and the contents literally recorded in the initial description and claims. Additionally, recently the Supreme Court corrects the strict ruling on the go-beyond issue of the State IP Office in one case and holds that the scope recorded in the initial description and claims should include (1) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims, and (2) contents directly or definitely derived by a person skilled in the art on the initial description, drawings and claim as a whole. Under such a circumstance, Chinese examiners may adjust their rules for such go-beyond issue.

A response and possible amendments must be submitted to the Office by **June 16, 2015 (Beijing Time)**. Please give us your further instructions as soon as possible.

The above official deadline can be extended once for one or two months. The cost for a one month extension is RMB940.00 (around US$150.00), including the official fee of RMB300.00 and an attorney fee of RMB640.00. The cost for a two-month extension is RMB1240.00 (around US$200.00), including the official fee of RMB600.00 and an attorney fee of RMB640.00.

We also list the related regulations below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your prompt reply is highly appreciated.

Please kindly confirm receipt of this letter by return e-mail.

Sincerely yours,
AFD China Intellectual Property



Xia Zheng (patent@afdip.com)

/Lhm/Zj/

Enclosure: A copy of the Chinese Notification of the Second Office Action (7 pages-by E-mail Only).

Patent Law:

Article 22(2): Novelty means that, the invention or utility model does not form part of the prior art; nor has any entity or individual filed previously before the date of filing with the Patent Administration Department Under the State Council an application relating to the identical invention or utility model disclosed in patent application documents published or patent documents announced after the said date of filing.

Article 22(3): Inventiveness means that, as compared with the prior art, the invention has prominent substantive features and represents a notable progress, and that the utility model has substantive features and represents progress.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

[redacted]

June 3, 2016

[redacted]

Attn.: [redacted]

Via Email Only

[redacted]

Re: National Phase in China of PCT/US2012/021583
In the name of Cypress Semiconductor Corporation
Title: Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers
CN Application No.: 201280000107.5
Your Ref.: [redacted] Cypress Ref.: PM07002CIP1CN
Our Ref.: [redacted]

Deadline for Responding to this Office Action: **July 27, 2016 (Beijing Time)**

Issue date: May 12, 2016; 2 month rejection

Dear Ms. Hachemi:

The State Intellectual Property Office of China recently has issued the Fourth Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below.

1. Inventiveness – Claim 1

The Examiner points out that claim 1 does not possess inventiveness over Reference 1 (CN101517714A) in view of known common knowledge in the art, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 1 (see page 8, paragraphs 3-4 on page 10 and page 14 of its Description and Figs. 5 and 9), the Examiner admits that the distinguishing technical feature of the technical scheme in claim 1 is the following:

the tunneling layer consists of silicon dioxide.

The Examiner holds that as mentioned in the "BACKGROUND ART" of the present application, it is known common knowledge in the art to use silicon dioxide to form the

[redacted]

tunneling layer. And thus on the basis of Reference 1 in combination of known common knowledge in the art, the technical scheme of claim 1 is obvious to a person skilled in the art.

2. Inventiveness – Claim 2

The Examiner points out that claim 2 does not possess inventiveness either. The Examiner holds that Reference 1 (see paragraphs 2-3 on page 8 of its Description) discloses relevant technical feature, then a person skilled in the art can realize that the lower density of trap will make it act as a barrier between charge trapped in the second charge trapping layer and the substrate to increase a retention performance of the multi-layer charge storing layer. According to the teaching, a person skilled in the art can easily conceive of selecting a certain concentration of oxygen to make the first charge storing layer have a substantially trap free density. And thus the technical scheme of claim 2 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

3. Inventiveness – Claims 3-5

The Examiner points out that claims 3-5 do not possess inventiveness either. The Examiner holds that Reference 1 (see paragraphs 2-3 on page 8 of its Description) discloses relevant technical features, and according to the teaching, a person skilled in the art can easily conceive that the multi-layer charge storing layer has the required performance when the concentration of oxygen in the first charge storing layer is 35% and the concentration of oxygen in the second charge storing layer is 5%. And thus the technical schemes of claims 3-5 do not possess inventiveness on the condition that claim 2 they refer to does not possess inventiveness.

4. Inventiveness – Claim 6

The Examiner points out that claim 6 does not possess inventiveness either. The Examiner holds that Reference 1 (see paragraphs 2-3 on page 8 of its Description) discloses relevant technical features; therefore, under the teaching of Reference 1, a person skilled in the art can easily obtain that *an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages increases to at least 20 years*. And thus the technical scheme of claim 6 does not possess inventiveness on the condition that claim 2 it refers to does not possess inventiveness.

5. Inventiveness – Claim 7

The Examiner points out that claim 7 does not possess inventiveness either. The Examiner holds that Reference 1 (see paragraphs 2-3 on page 8 of its Description) discloses relevant technical features, and according to the teaching, a person skilled in the art can easily obtain the additional technical feature of claim 7. And thus the technical scheme of claim 7 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

6. Inventiveness – Claim 8

The Examiner points out that claim 8 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 8 is conventional technical means in the art. And thus the technical scheme of claim 8 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

7. Inventiveness – Claim 9

The Examiner points out that claim 9 does not possess inventiveness either. The Examiner holds that Reference 1 (see the last paragraph on page 14 of its Description) discloses relevant technical feature. And thus the technical scheme of claim 9 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

8. Inventiveness – Claim 10

The Examiner points out that claim 10 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 10 is a conventional choice of a person skilled in the art. And thus the technical scheme of claim 10 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

9. Inventiveness – Claim 11

The Examiner points out that claim 11 does not possess inventiveness either. The Examiner holds that Reference 1 (see paragraph 2 on page 9 of its Description) discloses relevant technical feature. And thus the technical scheme of claim 11 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

10. Inventiveness – Claim 12

The Examiner points out that claim 12 does not possess inventiveness either. The Examiner holds that Reference 3 (CN101859702A; see paragraph 53 of its Description) discloses relevant technical features, and according to the teaching, a person skilled in the art can easily conceive of applying the steam annealing process to Reference 1. And thus on the basis of the combination of References 1 and 3 and known common knowledge in the art, the technical scheme of claim 12 is obvious to a person skilled in the art.

11. Inventiveness – Claim 13

The Examiner points out that claim 13 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 13 is a conventional choice of a person skilled in the art. And thus the technical scheme of claim 13 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

With respect to the applicant's observation

With respect to the applicant's observations filed for responding to the previous Action, the Examiner also points out that the observations are not persuasive and cannot overcome the

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defects in previous Action.

The Examiner particularly holds that:

(1) As for the tunneling layer, the silicon oxynitride tunneling layer is formed by a specific process in the present application, to realize performances such as reducing the programming voltage or increasing the programming speed, and as mentioned in the "BACKGROUND ART" of the present application, it is a conventional choice of a person skilled in the art to use monox, silicon nitride and silicon oxynitride, etc., as the tunneling layer; a person skilled in the art can easily conceive of selecting a conventional silicon dioxide as the tunneling layer according to the requirement of a device and the manufacturing process; (2) paragraph 2 on page 14 of the description of Reference 1 recites: "In one embodiment, multiple nitride or oxynitride charge trapping layers are formed at operations 902 and 904 in a low pressure CVD process using a silicon source, …, a nitrogen source, such as N_2, NH_3, N_2O or nitrogen trioxide (NO_3), and an oxygen-containing gas… Alternatively, gases in which hydrogen has been replaced by deuterium can be used, including, for example, the substitution of ND3 for NH_3. The substitution of deuterium for hydrogen advantageously passivates Si dangling bonds at the substrate interface, thereby increasing an NBTI (Negative Bias Temperature Instability) lifetime of SONOS-type devices", i.e., Reference 1 has disclosed that a process gas including a silicon source, an oxygen-containing gas and ND_3 is used in the CVD process for forming the charge trapping layer, wherein the substitution of deuterium for hydrogen advantageously passivates Si dangling bonds at the substrate interface, which plays the same role as the substitution of deuterium for hydrogen in the present application, i.e., using the ND_3 as a process gas. Therefore, the applicant's observations are not persuasive.

Conclusive opinion

Based on the above opinions, the Examiner also holds, as marked in the form of this Office Action, that the application does not possess any patentable substantial contents, and if the applicant fails to expound reasons or the reasons expounded are not sufficient, this application will be rejected.

This generally is a conclusive opinion of the Examiner and in next the Examiner is likely to issue a final rejection if the response to this Action is not persuasive or no substantial amendments are made.

Please be advised that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. The Office currently examines go-beyond issue very strictly, more strictly than that in many other countries. The "scope recorded in the initial description and claims", pursuant to the Patent Examination Guidelines, includes (1) literal contents of the initial description and claims, and (2) contents determined directly and undoubtedly from the drawings and the literal contents of the initial description and claims.

According to the Supreme Court's ruling in one recent case, such "scope" should include (i) contents definitely expressed by literal or graphic manner in the initial description,

Sandisk Technologies, Inc. - Ex. 1002, Page 001124

drawings and claims of the application, and (ii) contents directly or definitely derived by a person skilled in the art from the initial description, drawings and claims as a whole, which should correct the strict rules of the Office. However, in practice, examiners are still likely to examine the go-beyond issue strictly. The applicant had better take this in mind if deciding to make any amendments.

A response and possible amendments must be submitted to the Office by **July 27, 2016 (Beijing Time)**. Please give us your further instructions as soon as possible.

[redacted]

We also list the related regulations below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your prompt reply is highly appreciated.

Please kindly confirm receipt of this letter by return e-mail.

Sincerely yours,
AFD China Intellectual Property



[redacted]

/Lc/Zf

Enclosures: (All by E-mail only)
1. A copy of the Chinese Notification of the Fourth Office Action; and
2. Our invoice.

Patent Law:

Article 22(3): Inventiveness means that, as compared with the prior art, the invention has prominent substantive features and represents a notable progress, and that the utility model has substantive features and represents progress.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

Sandisk Technologies, Inc. - Ex. 1002, Page 001125

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

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September 1, 2014

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Attn.: Ms. Sinead Clark
Murgitroyd & Company-Glasgow
Scotland House, 165-169 Scotland Street
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United Kingdom

Via Email Only

sinead.clark@murgitroyd.com

Re: National Phase in China of PCT/US2012/021583
In the name of Cypress Semiconductor Corporation
Title: Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers
CN Application No.: 201280000107.5
Your Ref.: 123443.CN.02 Cypress Ref.: PM07002CIP1CN
Our Ref.: 081306522-ET

Deadline for Responding to this Office Action: December 09, 2014 (Beijing Time)

Dear Ms. Clark:

In connection with the captioned application, the State Intellectual Property Office of China has recently issued the First Office Action. According to your instruction, we would like to summarize the Examiner's objections stated in this office action as below.

1. Claim 1 seeks protection for a method of forming a semiconductor device. Reference 1 (CN101517714A) discloses a method of forming a semiconductor device (see pages 8-14 of the description and Fig. 5), comprising forming a tunnel oxide layer 516 on a silicon containing layer of a substrate; depositing on the tunnel oxide layer the first charge trapping layer 518A (analogous to a first charge storing layer) comprising a silicon-rich oxygen-rich oxynitride in which a stoichiometric composition of the oxynitride enables the first charge storing layer to have a lower density of trap (analogous to being substantially trap free); and depositing directly on the first charge trapping layer a second charge trapping layer comprising an oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer in which a stoichiometric composition of the oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer enables it to have a higher density trap; forming a blocking oxide layer 520 on the second charge trapping layer; and forming a silicon containing gate layer on the blocking oxide layer. The difference of claim 1 over Reference 1 is the second charge storing layer further comprises a concentration of carbon selected to increase a number of traps therein. Based on the distinguishing technical feature, the technical problem to be solved by claim 1 is how to increase the number of traps in the charge storing layer and increase the maintained time of charge. Reference 2 (US2010096687A1) discloses a method of forming a semiconductor

Sandisk Technologies, Inc. - Ex. 1002, Page 001126

device (see paragraphs 25 and 48 of the description and Fig. 1), comprising forming a tunnel oxide layer on a substrate 22; forming a charge storing layer 26 containing a silicon nitride layer on the tunnel oxide layer; forming a blocking layer on the charge storing layer, wherein the carbon with a certain concentration is doped in a silicon nitride of the charge storing layer such that the maintained time of charge of the charge storing layer is increased. meanwhile, Reference 2 (see paragraph 25 of the description) discloses that adding dopant will increase the number of available charge trap sites in the charge storing layer. That is, Reference 2 gives the teaching of doping carbon in the charge storing layer. According to the teaching, a person skilled in the art may readily conceive of doping carbon in the second charge trapping layer of Reference 1 to obtain the technical scheme sought for protection in claim 1. Thus, it is obvious for a person skilled in the art to conceive the technical scheme sought for protection in the claim over Reference 1 in combination with common technical knowledge in the art. Therefore, the claim does not possess prominent substantive features or represent a notable progress, and thus does not possess inventiveness under Article 22(3) of Patent Law.

2. The additional technical features of claims 2-8 and 11 are obvious to a person skilled in the art over Reference 1. The additional technical feature of claim 9 is disclosed by Reference 1 (see page 14 of the description). The additional technical feature of claims 10 and 12 are conventional technical means in the art. Thus, where the cited claims do not possess inventiveness, the above claims do not possess inventiveness.

3. Claim 13 seeks protection for a multi-layer charge storing layer. Reference 1 (see pages 8-14 of the description and Fig. 5) discloses a multi-layer charge storing layer, comprising the first charge trapping layer 518A (analogous to a first charge storing layer) comprising a silicon-rich oxygen-rich oxynitride in which a stoichiometric composition of the oxynitride enables the first charge storing layer to have a lower density of trap (analogous to being substantially trap free); and depositing directly on the first charge trapping layer a second charge trapping layer comprising an oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer in which a stoichiometric composition of the oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer enables it to have a higher density trap. The difference of claim 13 over Reference 1 is the second charge storing layer further comprises a concentration of carbon selected to increase a number of traps therein. Based on the distinguishing technical feature, the technical problem to be solved by claim 13 is how to increase the number of traps in the charge storing layer and increase the maintained time of charge. Reference 2 (US2010096687A1) discloses a method of forming a semiconductor device (see paragraphs 25 and 48 of the description and Fig. 1), comprising forming a tunnel oxide layer on a substrate 22; forming a charge storing layer 26 containing a silicon nitride layer on the tunnel oxide layer; forming a blocking layer on the charge storing layer, wherein the carbon with a certain concentration is doped in a silicon nitride of the charge storing layer such that the maintained time of charge of the charge storing layer is increased. Meanwhile, Reference 2 (see paragraph 25 of the description) discloses that adding dopant will increase the number of available charge trap sites in the charge storing layer. That is, Reference 2 gives the teaching of doping carbon in the charge storing layer. According to the teaching, a person skilled in the art may readily conceive of doping carbon in the second charge trapping layer of Reference 1 to obtain the technical scheme sought for protection in claim 13. Thus, it is obvious for a

Sandisk Technologies, Inc. - Ex. 1002, Page 001127

person skilled in the art to conceive the technical scheme sought for protection in the claim over Reference 1 in combination with common technical knowledge in the art. Therefore, the claim does not possess prominent substantive features or represent a notable progress, and thus does not possess inventiveness under Article 22(3) of Patent Law.

4. The additional technical feature of claim 14 is conventional technical means in the art. The additional technical feature of claims 15-18 are obvious to a person skilled in the art over Reference 1. Thus, where the cited claims do not possess inventiveness, the above claims do not possess inventiveness.

Please note that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. In China, whether an amendment goes beyond the scope is a big issue, and the examiners will examine this issue strictly, much stricter than examiners in many other countries. And the scope recorded in the initial description and claims, according to the Examination Guidelines, includes contents found literally in the initial description and claims or determined directly and undoubtedly from the drawings and the contents literally recorded in the initial description and claims. Additionally, recently the Supreme Court corrects the strict ruling on the go-beyond issue of the State IP Office in one case and holds that the scope recorded in the initial description and claims should include (1) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims, and (2) contents directly or definitely derived by a person skilled in the art on the initial description, drawings and claim as a whole. Under such a circumstance, Chinese examiners may adjust their rules for such go-beyond issue.

A response and possible amendments must be submitted to the Office by **December 09, 2014(Beijing Time)**. Please give us your further instructions as soon as possible.

The above official deadline can be extended once for one or two months. The cost for a one month extension is RMB940.00, including the official fee of RMB300.00 and an attorney fee of RMB640.00. The cost for a two-month extension is RMB1240.00, including the official fee of RMB600.00 and an attorney fee of RMB640.00.

Please kindly note that our invoice for reporting this action will be sent to you in another our separate email.

Our other invoices for future prosecution of this application may also be sent to you separately after the completion of our reports in order to match our new invoice management policy. Your support and patience for our new policy will be very much appreciated. And we hope to make the transition for our new policy as smooth and seamless as possible.

We also list related rules of Chinese Patent Law below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your promptly reply is highly appreciated.

Sandisk Technologies, Inc. - Ex. 1002, Page 001128

Please kindly confirm receipt of this letter by fax or e-mail.

Sincerely yours,
AFD China Intellectual Property



Xia Zheng (patent@afdip.com)

/Mxf/Zxk

Enclosures:
The Notification of the First Office Action (7 pages- by E-mail Only);

Patent Law:

Article 22(3): Inventiveness means that, as compared with the prior art, the invention has prominent substantive features and represents a notable progress, and that the utility model has substantive features and represents progress.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

AFD China
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October 26, 2015

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Via Email Only

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Re: National Phase in China of PCT/US2012/021583
In the name of Cypress Semiconductor Corporation
Title: Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers
CN Application No.: 201280000107.5
Your Ref.:123443.CN.02 Cypress Ref.: PM07002CIP1CN
Our Ref.:081306522-ET

Deadline for Responding to this Office Action: December 24, 2015 (Beijing Time)

Issue date: October 9, 2015 ; 2 month rejection

Dear Ms. Hachemi:

The State Intellectual Property Office of China recently has issued the Third Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below.

With respect to the applicant's observations filed for responding to the previous Action, the Examiner also points out that the observations are not persuasive and cannot overcome the defects in previous Action.

The Examiner particularly holds that as recited in paragraph 48 of the description of the present application, due to lean oxygen and rich silicon in the second charge storing layer 706A, the trap sites therein produce an electric field that will oppose the electric field produced by the trapped charges in the programmed device. Based on the same theory, the last paragraph on page 8 of Reference 1 discloses that the top oxynitride layer (i.e., the second charge storing layer) also is oxygen-lean and silicon-rich, and wherein the higher the silicon content is, the higher the trap density is, and the high trap density also leads to the produced second electric field to oppose the electric field (i.e., the first electric field) produced by the trapped charges in the programmed device. It can be seen that the technical features newly

Sandisk Technologies, Inc. - Ex. 1002, Page 001130

added in claim 1 by the applicant are also disclosed by Reference 1, and thus the amended claim 1 still does not possess novelty. Based on the similar reasons as in the Second Office Action, claims 11 and 13 do not possess novelty, and claims 2-10, 12 and 14 do not possess inventiveness.

Conclusive opinion

Based on the above opinions, the Examiner also holds, as marked in the form of this Office Action, that the application does not possess any patentable substantial contents, and if the applicant fails to expound reasons or the reasons expounded are not sufficient, this application will be rejected.

This generally is a conclusive opinion of the Examiner and in next the Examiner is likely to issue a final rejection if the response to this Action is not persuasive or no substantial amendments are made.

Please be advised that in a response to the OA, any amendments made to the claims must not go beyond the scope recorded in the initial description and claims. The Office currently examines go-beyond issue very strictly, more strictly than that in many other countries. The "scope recorded in the initial description and claims", pursuant to the Patent Examination Guidelines, includes (1) literal contents of the initial description and claims, and (2) contents determined directly and undoubtedly from the drawings and the literal contents of the initial description and claims.

According to the Supreme Court's ruling in one recent case, such "scope" should include (i) contents definitely expressed by literal or graphic manner in the initial description, drawings and claims of the application, and (ii) contents directly or definitely derived by a person skilled in the art from the initial description, drawings and claims as a whole, which should correct the strict rules of the Office. However, in practice, examiners are still likely to examine the go-beyond issue strictly. The applicant had better take this in mind if deciding to make any amendments.

A response and possible amendments must be submitted to the Office by **December 24, 2015 (Beijing Time)**. Please give us your further instructions as soon as possible.

The above official deadline can be extended once for one or two months. The cost for a one month extension is RMB940.00 (around US$150.00), including the official fee of RMB300.00 and an attorney fee of RMB640.00. The cost for a two-month extension is RMB1240.00 (around US$200.00), including the official fee of RMB600.00 and an attorney fee of RMB640.00.

We also list the related regulations below for your reference.

Should you have any questions, please do not hesitate to contact us.

We look forward to hearing from you. Your prompt reply is highly appreciated.

Please kindly confirm receipt of this letter by return e-mail.

Sincerely yours,
AFD China Intellectual Property



Xia Zheng (patent@afdip.com)

/Lc/Zf

Enclosures: (All by E-mail only)
1. A copy of the Chinese Notification of the Third Office Action; and
2. Our invoice.

Patent Law:

Article 22(2): Novelty means that, the invention or utility model does not form part of the prior art; nor has any entity or individual filed previously before the date of filing with the Patent Administration Department Under the State Council an application relating to the identical invention or utility model disclosed in patent application documents published or patent documents announced after the said date of filing.

Article 22(3): Inventiveness means that, as compared with the prior art, the invention has prominent substantive features and represents a notable progress, and that the utility model has substantive features and represents progress.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

[redacted]

November 29, 2016

[redacted]

Attn.: [redacted]

[redacted]

Via E-mail only

[redacted]

Re: National Phase in China of PCT/US2012/021583
In the name of Cypress Semiconductor Corporation
Title: Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers
CN Application No.: 201280000107.5
Your Ref.: 123443.CN.02 Cypress Ref.: PM07002CIP1CN
Our Ref.: [redacted]
Non-extendable deadline for Reexamination: February 18, 2017 (Beijing Time)
Issue date: November 03, 2016; 3 months rejection

Dear Ms. Hachemi:

The State Intellectual Property Office of China recently has issued a Decision of Rejection in connection with the captioned application. A copy of Chinese Decision is enclosed for your records. With respect to the Decision, we would like to bring your attention to the following.

Decision and brief opinions

The Office rejects this application since it is not in conformity with the related regulations.

The Examiner's opinions of rejection are briefly summarized as below.

Part I. Inventiveness issue for claims 1-10

1. Claim 1

The Examiner points out that claim 1 does not possess inventiveness over Reference 1 (CN101517714A) in view of known common knowledge in the art, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

[redacted]

Comparing with the disclosure of Reference 1 (see page 8, paragraphs 3-4 on page 10 and page 14 of its Description and Figs. 5 and 9), the Examiner indicates that the first charge trapping layer 518A is equivalent to the first charge storing layer in the present application and the electric field is equivalent to the first electrical field in the present application, and admits that the distinguishing technical feature of the technical scheme in claim 1 is that:

the tunneling layer consists of silicon dioxide; and the specific concentration of oxygen in the oxygen-lean oxynitride layer and oxygen-rich oxynitride layer.

The Examiner holds that it is known common knowledge in the art that the tunneling layer formed by silicon dioxide as stated in background of the present application. Reference 1 (see paragraphs 2-3 on page 8 of its Description) discloses relevant technical feature, and according to the technical teaching, a person skilled in the art can easily obtain that the multi-layer charge storing layer has the required performance when the concentration of oxygen in the first charge storing layer is 15-40% and the concentration of oxygen in the second charge storing layer is less than 5% through limited experiments, without paying any creative work. And thus on the basis of Reference 1 in combination of known common knowledge in the art, the technical scheme of claim 1 is obvious to a person skilled in the art.

2. Claim 2

The Examiner points out that claim 2 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 2 can be easily obtained by a person skilled in the art. And thus the technical scheme of claim 2 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

3-10. Claims 3-10

[*AFD remarks: The Examiner's comments on the inventiveness of claims 3-10 in this Decision of Rejection are substantially the same as those on the inventiveness of claims 6-13 and 11-13 in the Fourth Office Action. Please see our report for forwarding the Fourth Office Action for details.*]

Part II Examiner's opinions with respect to the Applicant's arguments

With respect to the applicant's arguments, the Examiner holds that

(1) According to the contents recorded in Claim 1 and paragraphs 43-45 of the description of the present application, the inventive concept of the present application is that the oxygen-rich first oxynitride layer in the bottom layer of the charge storing layer can produce substantially trap free and the oxygen-lean second oxynitride layer in the top layer of the charge storing layer can produce dense trap density. The present application neither provides that specific oxygen-rich and oxygen-lean concentration have unexpected technical effect with respect to other concentration, nor provides corresponding experimental data.

Sandisk Technologies, Inc. - Ex. 1002, Page 001134

Whereas the structure and the inventive concept of Reference 1 is the same as those of the present application, i.e., both are to obtain the layer with low density trap and the layer with high density trap by dividing the charge storing layer into the oxygen-rich layer and the oxygen-lean layer. Therefore, a person skilled in the art can easily obtain that the multi-layer charge storing layer has the required performance when the concentration of oxygen in the first charge storing layer is 15-40% and the concentration of oxygen in the second charge storing layer is less than 5% through limited experiments, without paying any creative work.

(2) The energy band diagram with homogeneous oxynitride layer is shown in Fig. 6 of the present application, and the energy band diagram with two oxynitride layers of oxygen-rich and oxygen-lean layers is shown in Fig. 8 of Reference 1, the two of which are different. And as recited in paragraph 48 of the description of the present application, since the second charge storing layer 706A is oxygen-lean and silicon-rich, the trap sites of which produces an electric field that will oppose the electric field produced by the trapped charges in the programmed device. Namely, the opposite electric field is due to the high density trap sites in the oxygen-lean layer. The structure of layers of Reference 1 is the same as that in the present application (see paragraphs 2-4 on page 8 of its Description) [,that is]: the silicon-rich and oxygen-rich oxynitride layer in the bottom layer has low density trap and the silicon-rich and oxygen-lean oxynitride layer in the top layer has high density trap. Based on the same principle, the high trap sites density in the oxygen-lean layer of the top layer will lead to that an produced second electric field will oppose the electric field (i.e. the first electric field) produced by the trapped charges in the programmed device.

To sum up, the observation submitted by the applicant is not persuasive.

Reexamination

The applicant can file a reexamination request before the Chinese Patent Reexamination Board by the **non-extendable deadline** of **February 18, 2017 (Beijing Time)**, if not satisfied with this decision.

[redacted]

Divisional application

If the applicant does not intend to file reexamination, the applicant will have the **final** opportunity, on the basis of the captioned application, to file divisional application(s) before the **non-extendable deadline** of **February 18, 2017 (Beijing Time)**. Once such deadline lapses, no divisional application can be filed on the basis of the captioned application.

[redacted]

If the applicant plans to file a divisional application, please let us have the instructions before two weeks prior to the above deadline, to ensure sufficient time for us to prepare and file the application. We will **not** take action if we do **not** receive your instruction.

To avoid piecemeal invoice, the cost for reporting this Decision will be charged after the filing the reexamination request.

Per our accounting records, our invoice [redacted] is still outstanding. Your prompt settlement will be very much appreciated. If you have already settled the balance please disregard the request on the payment for the outstanding invoices and let us have your copy of wire receipt or check for the payment. Thank you.

We also list related rules of Chinese Patent Law and/or its Implementing Regulations below for your reference.

Please give us your further instructions as soon as possible. We look forward to hearing from you. Your prompt reply will be highly appreciated.

We would very much appreciate if you provide us a copy of your amendment documents in WORD format with your instructions, which will be of much help for our further work.

Should you have any questions, please do not hesitate to contact us.

Please confirm receipt of this letter by return e-mail.

Sincerely yours,

AFD China Intellectual Property



[redacted]

/Zxk/Xaw

Enclosure: The Notification of the Decision of Rejection (by E-mail only).

Patent Law:

Article 22(3): Inventiveness means that, as compared with the prior art, the invention possesses prominent substantive features and represents a notable progress and that the utility model possesses substantive features and represents progress.

Article 38: Where, after the applicant has made the observations or amendments, the Patent Administration

[redacted]

Department Under the State Council finds that the application for a patent for invention is still not in conformity with the provisions of this Law, the application shall be rejected.

Article 41(1): The patent administration department under the State Council shall set up a Patent Reexamination Board. Where an applicant for patent is not satisfied with the decision of the said department rejecting the application, the applicant may, within three months from the date of receipt of the notification, request the Patent Reexamination Board to make a reexamination. The Patent Reexamination Board shall, after reexamination, make a decision and notify the applicant for patent.

Implementing Regulations of Patent Law:

Rule 53: In accordance with the provisions of Article 38 of the Patent Law, the circumstances where an application for a patent for invention shall be rejected by the Patent Administration Department under the State Council after examination as to substance are as follows:

(2) where the application does not comply with the provisions of Article 2, paragraph two, Article 20, paragraph one, Article 22, Article 26, paragraph three, four or five, or Article 31, paragraph one of the Patent Law, or of Rule 20, paragraph two of these Implementing Regulations;

(3) where the amendment to the application does not comply with the provisions of Article 33 of the Patent Law, or the divisional application does not comply with the provisions of Rule 43, paragraph one of these Implementing Regulations.

Rule 60: Where the applicant requests the Patent Reexamination Board to make a reexamination in accordance with the provisions of Article 41 of the Patent Law, it or he shall file a request for reexamination, state the reasons and, when necessary, attach the relevant supporting documents.

Where the request for reexamination does not comply with the prescribed form, the person making the request shall rectify it within the time limit fixed by the Patent Reexamination Board. If the requesting person fails to meet the time limit for making rectification, the request for reexamination shall be deemed not to have been filed.

[redacted]

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

[redacted]

September 30, 2016

[redacted]

Attn.: [redacted]
Murgitroyd & Company-Glasgow

Via Email Only
[redacted]

Re: National Phase in China of PCT/US2013/032339
In the name of Cypress Semiconductor Corporation
Title: Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers
CN Application No.: 2013800168932
Your Ref.: [redacted]
Our Ref.: [redacted]

Deadline for Responding to this Office Action: January 16, 2017 (Beijing Time)

Issue Date: September 1, 2016; 4 Months Rejection

Dear [redacted]:

The State Intellectual Property Office of China recently has issued the First Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below.

Part I Novelty

1. Claim 1

The Examiner points out that claim 1 does not possess novelty over Reference 1 (US8063434B1, November 22, 2011), and thus is not in conformity with the provisions of Article 22(2) of Patent Law, since Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3) discloses all technical features in the technical scheme of claim 1.

2. Claim 8

The Examiner points out that claim 8 does not possess novelty on the condition that claim 1 it refers to does not possess novelty and the additional technical feature of claim 8 is disclosed by Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3, especially lines 42-47 in column 3).

[redacted]

Part II Inventiveness

1. Claims 2-3

The Examiner points out that claims 2-3 do not possess inventiveness and thus are not in conformity with the provisions of Article 22(3) of Patent Law. The Examiner holds that the additional technical features of claims 2-3 constitute the distinguishing technical features over Reference 1, and Reference 2 (US2008/0048237A1, February 28, 2008) (see paragraph 132 of its Description) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1 to solve the technical problem. And thus on the basis of Reference 1 in combination of Reference 2, the technical schemes of claims 2-3 are obvious to a person skilled in the art.

2. Claim 4

The Examiner points out that claim 4 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 4 constitutes the distinguishing technical features over Reference 1, and Reference 3 (CN1801478A, July 12, 2006) (see lines 9-15 on page 2 of its Description and Figs. 1a-1b and 2c) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1 to solve the technical problem. And thus on the basis of Reference 1 in combination of Reference 3, the technical scheme of claim 4 is obvious to a person skilled in the art.

3. Claim 5

The Examiner points out that claim 5 does not possess inventiveness either. The Examiner holds that compared with the disclosure of Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3), the distinguishing technical feature in claim 5 is "*the memory device comprises a non-planar transistor including a gate having multiple surfaces abutting the channel*", and Reference 3 (see lines 9-15 on page 2 of its Description and Figs. 1a-1b and 2c) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1 to solve the technical problem. And thus on the basis of Reference 1 in combination of Reference 3, the technical scheme of claim 5 is obvious to a person skilled in the art.

4. Claims 6-7

The Examiner points out that claims 6-7 do not possess inventiveness either. The Examiner holds that Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3) discloses relevant technical features. Additionally, it is conventional technical means of a person skilled in the art that a gate layer is metal materials, and the blocking dielectric is a high K dielectric material. And thus the technical schemes of claims 6-7 do not possess inventiveness on the condition that the claims they refer to do not possess inventiveness.

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5. Claim 9

The Examiner points out that claim 9 does not possess inventiveness over Reference 1 in view of Reference 4 (US6709928B1, March 23, 2004) and known common knowledge in the art, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3), the Examiner indicates that a charge trapping oxynitride layer 318A is equivalent to a second oxynitride layer, and a trap free oxynitride layer 318B is equivalent to a first oxynitride layer, and admits that the distinguishing technical features of the technical scheme in claim 9 are the following:

(1) the gate has multiple surfaces abutting the channel; and

(2) the first oxynitride layer is separated from the second oxynitride layer by an anti-tunneling layer comprising an oxide.

The Examiner holds that as for the distinguishing technical feature (1), a fence and a gate of fin-type field effect transistor are conventional gate structures, in such two gate structures, there are more contact surfaces of the gate and the channel, and thus it can strengthen the control effect of the gate on the channel to some extent to ease short channel effect. Thus such technical distinguishing technical feature is conventional technical means of a person skilled in the art to avoid short channel effect. As for the distinguishing technical feature (2), Reference 4 (see lines 28-35 in column 4 and lines 37-47 in column 5 of its Description and Fig. 2B) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1 to solve the technical problem. And thus on the basis of Reference 1 in combination of Reference 4 and known common knowledge in the art, the technical scheme of claim 9 is obvious to a person skilled in the art.

6. Claim 10

The Examiner points out that claim 10 does not possess inventiveness either. The Examiner holds that Reference 3 (see lines 9-15 on page 2 of its Description and Figs. 1a-1b and 2c) discloses relevant technical features. And thus the technical scheme of claim 10 does not possess inventiveness on the condition that claim 9 it refers to does not possess inventiveness.

7. Claims 11-12

The Examiner points out that claims 11-12 do not possess inventiveness either. The Examiner holds that Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3) discloses relevant technical features. Additionally, it is conventional technical means of a person skilled in the art that the gate layer is metal material, the blocking dielectric is a high K dielectric material and the transistor is FinFET. And thus the technical schemes of claims 11-12 do not possess inventiveness on the condition that the claims they refer to do not possess inventiveness.

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8. Claim 13

The Examiner points out that claim 13 does not possess inventiveness either. The Examiner holds that Reference 5 (CN101558481A, October 14, 2009) (see Claim 4, lines 26-30 on page 3, paragraph 4 on page 4 of its Description and Fig. 4B) discloses relevant technical features. And thus the technical scheme of claim 13 does not possess inventiveness on the condition that claim 9 it refers to does not possess inventiveness.

9. Claim 14

The Examiner points out that claim 14 does not possess inventiveness either. The Examiner holds that Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3, especially lines 42-47 in column 3) discloses relevant technical features. And thus the technical scheme of claim 14 does not possess inventiveness on the condition that claim 9 it refers to does not possess inventiveness.

10. Claim 15

The Examiner points out that claim 15 does not possess inventiveness over Reference 6 (WO2011/162725A1, December 29, 2011) in view of Reference 1, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 6 (see paragraphs 128-132 of its Description and Fig. 6), the Examiner indicates that a carrier 602 is equivalent to semiconducting material, a source region is equivalent to a first diffusion region, a drain region 614a is equivalent to a second diffusion region and a gate insulator region 610 is equivalent to a tunnel oxide layer, and admits that the distinguishing technical features of the technical scheme in claim 15 are the following:

"a multi-layer charge storing layer abutting the tunnel oxide layer, the multi-layer charge storing layer including a first oxynitride layer comprising an oxygen-rich nitride closer to the tunnel oxide layer, and a second oxynitride layer comprising a silicon-rich, oxygen-lean nitride overlying the first oxynitride layer, wherein the second charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region".

The Examiner holds that Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1. And thus on the basis of Reference 6 in combination of Reference 1, the technical scheme of claim 15 is obvious to a person skilled in the art.

11. Claim 16

The Examiner points out that claim 16 does not possess inventiveness either. The Examiner holds that Reference 6 (see paragraphs 128-132 of its Description and Fig. 6) discloses relevant technical features. And thus the technical scheme of claim 16 does not

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possess inventiveness on the condition that claim 15 it refers to does not possess inventiveness.

12. Claim 17

The Examiner points out that claim 17 does not possess inventiveness either. The Examiner holds that Reference 4 (see lines 28-35 in column 4 and lines 37-47 in column 5 of its Description and Fig. 2B) discloses relevant technical features. And thus the technical scheme of claim 17 does not possess inventiveness on the condition that claim 16 it refers to does not possess inventiveness.

13. Claim 18

The Examiner points out that claim 18 does not possess inventiveness either. The Examiner holds that it is conventional technical means of a person skilled in the art that the blocking dielectric is a high K dielectric material. And thus the technical scheme of claim 18 does not possess inventiveness on the condition that claim 16 it refers to does not possess inventiveness.

14. Claim 19

The Examiner points out that claim 19 does not possess inventiveness either. The Examiner holds that Reference 4 (see lines 28-35 in column 4 and lines 37-47 in column 5 of its Description and Fig. 2B) discloses relevant technical features. And thus the technical scheme of claim 19 does not possess inventiveness on the condition that claim 18 it refers to does not possess inventiveness.

15. Claim 20

The Examiner points out that claim 20 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 20 is disclosed by Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3, especially lines 42-47 in column 3). And thus the technical scheme of claim 20 does not possess inventiveness on the condition that claim 15 it refers to does not possess inventiveness.

Part III Unclear Scope

1. Claim 15

The Examiner points out that the scope of claim 15 is unclear since the wording "the second charge-trapping layer" lacks reference basis, and thus is not in conformity with the provisions of Article 26(4) of Patent Law.

2. Claim 20

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The Examiner points out that the scope of claim 20 is unclear, and thus is not in conformity with the provisions of Article 26(4) of Patent Law, since the subject matter of claim 20 is inconsistent with the subject matter of claim 15 it refers to.

Conclusive opinion

Based on the above opinions, the Examiner also holds, as marked in the form of this Office Action, that the application does not possess any patentable substantial contents, and if the applicant fails to expound reasons or the reasons expounded are not sufficient, this application will be rejected.

This generally is a conclusive opinion of the Examiner and in next the Examiner is likely to issue a final rejection if the response to this Action is not persuasive or no substantial amendments are made.

[redacted]

[redacted]

A response and possible amendments must be submitted to the Office by **January 16, 2017 (Beijing Time)**. Please give us your further instructions as soon as possible.

[redacted]

[redacted]

We also list the related regulations below for your reference.

Should you have any questions, please do not hesitate to contact us.

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We look forward to hearing from you. Your prompt reply is highly appreciated.

Please kindly confirm receipt of this letter by return e-mail.

Sincerely yours,
AFD China Intellectual Property



[redacted]

[redacted]

Enclosures: (All by E-mail only)
1. A copy of the Chinese Notification of the First Office Action;
2. A copy of Reference documents.

Patent Law:

Article 22(2): Novelty means that, the invention or utility model does not form part of the prior art; nor has any entity or individual filed previously before the date of filing with the Patent Administration Department Under the State Council an application relating to the identical invention or utility model disclosed in patent application documents published or patent documents announced after the said date of filing.

Article 22(3): Inventiveness means that, as compared with the prior art, the invention has prominent substantive features and represents a notable progress, and that the utility model has substantive features and represents progress.

Article 26(4): The claims shall be supported by the description and shall define the extent of the patent protection sought for in a clear and concise manner.

Article 33: An applicant may amend his or its application for a patent, but the amendment to the application for a patent for invention or utility model may not go beyond the scope of disclosure contained in the initial description and claims, and the amendment to the application for a patent for design may not go beyond the scope of the disclosure as shown in the initial drawings or photographs.

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台一國際專利法律事務所
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November 18, 2016

[redacted]

Attn: Ms. Flora Hachemi

Re: Taiwan Patent Application No. 102110223
Applicant: CYPRESS SEMICONDUCTOR CORPORATION
Title: Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers
Case No: PM07002CIP2
Your Ref: P129040.TW.01/SCHOUTEND
Our Ref: [redacted]

Dear Sirs,

We received an Official Letter from the Taiwan Intellectual Property Office (TIPO) informing us that the referenced application will be rejected. Enclosed please find the Official Letter, the translation of the Official Letter, our comments, the citations and the currently pending claims for your reference.

A three-month term has been set for the applicant to supply defending arguments for further examination with the TIPO. The deadline to file a response is January 13, 2017 (Taiwan time) and is generally extensible by three calendar months by application before exhaustion. We would appreciate receiving your instructions and remarks by **January 09, 2017** so that we can file a timely response with the TIPO.

Best regards,

Wilson C [redacted]

Yen. Chuan [redacted]

WC/as
Encls.

[redacted]

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TRANSLATION OF THE OFFICIAL LETTER

SUBJECT:

After examination, the TIPO considers that the following issues apply to the referenced application. The applicant is requested to file an argument (in duplicate) or an amendment within three months from receipt of this Examination Report. If the applicant fails to reply within the time limit, the TIPO will continue the examination on the basis of the materials in hand.

EXPLANATION:

1. After examination, the Examiner deems that:

1.1 The present application is entitled "Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers". The present application contains 20 claims, of which claims 1, 9 and 15 are independent claims, and the other claims are dependent claims.

1.2 Claim 1 of the present application does not meet the requirement of Article 22, Paragraph 1, Item 1 of the Taiwan Patent Law according to citation 1. Claim 2 of the present application does not meet the requirement of Article 22, Paragraph 2 of the Taiwan Patent Law according to the combination of citations 1 and 2. Claim 3 of the present application does not meet the requirement of Article 22, Paragraph 2 of the Taiwan Patent Law according to the combination of citations 1 and 3. Claim 4 of the present application does not meet the requirement of Article 22, Paragraph 2 of the Taiwan Patent Law according to the combination of citations 1 and 4.

1.2.1 Regarding claim 1 of the present application, paragraphs [0068], [0072]-[0078] and figure 1 of citation 1 disclose a memory device comprising: a channel (108) formed from a semiconducting material (Si-substrate) overlying a surface on a substrate (102) connecting a source (104) and a drain (106) of the memory device; a tunnel oxide layer (112) overlying the channel (108); and a multi-layer charge storing layer (combined-114/116/117/118) including an oxygen-rich, first oxynitride layer (114) on the tunnel oxide layer (112) in which a stoichiometric composition of the first oxynitride layer (114) results in it being substantially trap free (paragraphs [0072]-[0078]), and an oxygen-lean, second oxynitride layer (116, paragraph [0068]) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer (116) results in it being trap dense (paragraphs

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[0072]-[0078]). Citation 1 discloses all the technical features of claim 1 of the present application, whereby said claim does not have novelty.

1.2.2 Regarding claim 2 of the present application, figure 1 of citation 2 discloses that the channel (41) comprises polysilicon. Accordingly, said claim is a combination of citations 1 and 2 and does not have unexpected effects. An ordinarily skilled person in the art may easily achieve said claim.

1.2.3 Regarding claim 3 of the present application, lines 29-45 in col. 5 of citation 3 disclose that the channel comprises recrystallized polysilicon, whereby said claim is a combination of citations 1 and 3 and does not have unexpected effects. An ordinarily skilled person in the art may easily achieve said claim.

1.2.4 Regarding claim 4 of the present application, paragraph [0159] of citation 4 discloses that the channel comprises a silicon nanowire, whereby said claim is a combination of citations 1 and 4 and does not have unexpected effects. An ordinarily skilled person in the art may easily achieve said claim.

1.3 Claim 9 of the present application does not meet the requirement of Article 22, Paragraph 2 of the Taiwan Patent Law according to a combination of citations 1 and 5. Claim 10 of the present application does not meet the requirement of Article 22, Paragraph 2 of the Taiwan Patent Law according to a combination of citations 1, 4 and 5.

1.3.1 Regarding claim 9 of the present application, paragraphs [0068], [0072]-[0078] and figure 1 of citation 1 disclose a memory device comprising: an electrically conducting channel (108) formed from a semiconducting material (Si-substrate) overlying a surface on a substrate (102) connecting a source (104) and a drain (106) of the memory device; and a gate (110) having multiple surfaces abutting the channel, the gate comprising: a tunnel oxide layer (112) overlying the channel (108); and a multi-layer charge storing layer(114, 116) including a first oxynitride layer (114) closer to the tunnel oxide layer (112), and a second oxynitride layer(116); lines 15-20 in col. 13, lines 36-42 in col. 14 and lines 5-10 in col. 15 and figure 15 of citation 5 disclose that the first oxynitride layer is separated from the second oxynitride layer by an anti-tunneling layer comprising an oxide. Accordingly, said claim is a combination of citations 1 and 5 and does not have unexpected effect. An ordinarily skilled person in the art may easily achieve said claim.

1.3.2 Regarding claim 10 of the present application, paragraph [0159] of citation 4 discloses that the channel comprises a silicon nanowire. Accordingly, said claim is a combination of citations 1, 4 and 5 and

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does not have unexpected effect. An ordinarily skilled person in the art may easily achieve said claim.

1.4 Citations:
1. US 2006/0261401 A1
2. US 5847411
3. US 5348903
4. US 2005/0110064 A1
5. US 6833582 B2

1.5 There are no further issues that prohibit the patentability of the current invention at the moment except the above mentioned rejection reasons. If there are new issues that prohibit the patentability of the current invention, we will inform the applicant of the rejection reasons.

2. If an amendment or a correction is made to the specification, claims and drawings, the applicant should handle the amendment or the correction according to Article 43 and Article 44, Item 3 of the Taiwan Patent Act and Article 36 to Article 38 of the Enforcement Rules of the Taiwan Patent Act, and draft a request for an amendment or a correction.

3. In the case where the applicant wishes to proceed with a face-to-face demonstration or explanation before the TIPO, please explicitly indicate "interview requested" in the response, and an official fee of NT$1000 must be paid. The place and time for an interview will be arranged if the TIPO considers an interview necessary.

4. Attached is a copy of the search report of the present application.

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Search Report of Patent Application No. 102110223

1.Filing Date: March 22, 2013		
2.Priority Date: March 31, 2012		
3.Classification of the Application (IPC): ***H01L27/115***(2006.01), ***H01L29/78***(2006.01)		
4.Technical Fields Searched (IPC): H01L27/115(2006.01), H01L29/78(2006.01)		
5.Database Searched (Key Words): TIPO domestic and foreign databases, EPO, USPTO, JPO		
Category	Citation of Document with Indication, Where Appropriate, of Relevant Passages	Relevant to Claim
X Y	1. US 2006/0261401 A1 2006/11/23 Figure 1 and paragraphs [0068], [0072]-[0078].	1 2-4, 9, 10
Y	2. US 5847411 1998/12/08 Figure 1.	2
Y	3. US 5348903 1994/09/20 Lines 29-45 in col. 5	3
Y	4. US 2005/0110064 A1 2005/05/26 Paragraph [0159]	4, 10
Y	5. US 6833582 B2 2004/12/21 Figure 15; lines 15-20 in col. 13, lines 36-42 in col. 14 and lines 5-10 in col. 15.	9, 10
Categories of Cited Documents: X: particularly relevant document that would refute the novelty or inventive step of the claimed invention when taken alone Y: particularly relevant document that would refute the novelty or inventive step of the claimed invention when combined with one or more other documents A: document defining the general state of the art D: document cited in the specification E: document filed prior to but published after the application was filed O: document of public use, sale or exhibition P: document published on a date falling between the filing date of the application and the priority date claimed L: document cited for other reasons		

Date of completion of the search: September 30, 2016

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RELATED ARTICLE OF THE PATENT ACT

Article 22 Substantial Conditions

An invention which is industrially applicable may be granted a patent upon application in accordance with this Act, except for the following:

1. the invention was disclosed in a publication prior to the filing of the patent application;

2. the invention was publicly exploited prior to the filing of the patent application; or

3. the invention was publicly known prior to the filing of the patent application.

Where an invention can be easily made by a person ordinarily skilled in the art based on prior art, a patent shall not be granted for such an invention notwithstanding the preceding paragraph.

Any of the following events shall not be deemed as one prescribed in Paragraph 1 or the preceding paragraph, which may preclude the grant of an invention patent, provided that the concerned patent application is filed within six months from the date of the event's occurrence:

1. the invention concerned was publicly disclosed as a result of conducting a test;

2. the invention was disclosed in a publication;

3. the invention was displayed at an exhibition held or recognized by the Government; or

4. the invention was disclosed without the consent of the applicant.

An applicant claiming exemption as set forth in Item 1 through Item 3 of the preceding paragraph shall state the fact and the relevant date in the patent application at the time of filing and submit evidentiary documents within the time limit specified by the Specific Patent Agency.

(Published on the website of the TIPO)

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OUR COMMENTS

1. Point 1.1 of the Examination Report is the examiner's summary of the examined version of the specification and claims and his accounting of the independent and dependent claims. No other response is required or anticipated.

2. With regard to point 1.2 in the Examination Report, our comments follow:

Article 22, Paragraph 1, Item 1 of the Patent Act stipulates that an invention which is industrially applicable may be granted a patent upon application in accordance with this Act, except for the invention which has been disclosed in a publication prior to the filing of the patent application.

Article 22, Paragraph 2 of the Patent Act stipulates that where an invention can be easily made by a person ordinarily skilled in the art based on prior art, a patent shall not be granted for such an invention notwithstanding the preceding paragraph.

The examiner deems that claim 1 of the present invention has been disclosed in citation 1; and claims 2-4, 9 and 10 of the present application can be easily achieved based on citations 1-5.

The disclosures of the main citation

Citation 1 relates to integrated circuits and in particular the present invention relates to non-volatile memory devices. As stated above, the silicon oxy-nitride (SiON) utilized in the above example provides additional charge trapping sites. The nitrogen-rich SiON has an atomic silicon concentration of approximately 38%-40%, an atomic oxygen concentration of approximately 20%, and an atomic nitrogen concentration of approximately 40%, resulting in a trapping layer with a dielectric constant of approximately 7, refractive index of approximately [gamma]=1.8 and a charge trap density of 8E12-1E13/cm2. In the above SiON, deep energy traps are associated with larger concentrations of Si-O-N bond "defects" in the silicon oxy-nitrides. **Such a trapping layer of an embodiment of the present invention would provide an effective charge density in the desired range of 5E12/cm^2 to 1E13/cm^2 without the adverse effects on retention due to coulomb blockade or quantum confinement.** It is noted that other charge trapping insulator materials may also be utilized in embodiments of the present invention as the charge trapping layer.(paragraph [0067] of citation 1)

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For one embodiment of the present invention, the charge blocking layers are preferably comprised of a single or composite layer of large K dielectric material layers such as Al2O3 (K=10) or Pr2O3 (K=30) or TiO2 (K=60) of thickness greater than 6 nm, to provide a large electron energy barrier and prevent direct tunneling of trapped charges to the control gate while helping minimize the overall EOT of the gate-stacks. **As stated above, charge blocking layers have been disclosed that allow for erasure of the data stored in the trapped charge on the trapping layer or floating gate of the memory cell by allowing the tunneling or injection of hole or electron carriers through the charge blocking layer from the control gate.** It is noted, however, that multiple insulators can be utilized in charge blocking layers of embodiments of the present invention, including, but not limited to insulators from the oxide, mixed oxide, nitride, oxynitrides, mixed oxynitrides, and silicate families. (paragraph [0068] of citation 1) For the normal mode device, FIG. 1A details the physical cross section of the gate stack structure and FIG. 1B details the corresponding band-gap diagram of a normal mode memory cell 100 in accordance with embodiments of the present invention. In FIG. 1A, a NFET memory cell 100 is shown formed on a substrate 102. The memory cell 100 has first and second source/drain regions 104, 106, in contact with a channel region 108, and a gate-stack 110 formed over the channel region 108. The gate-stack 110 contains a tunnel insulator layer 112 formed over the channel region 108, **a trapping layer/floating node 114** formed over the tunnel insulator layer 112, **a charge blocking layer 116 formed over the trapping layer 114**, an optional passivation layer 117, and a control gate 118. The tunnel insulator layer 1 12 includes two or more layers of materials layered to provide an asymmetric stepped band-gap profile. Other normal mode memory cell embodiments of the present invention may also provide a trapping layer 114 with deep traps and embedded metal nano-crystals, and a high K charge blocking layer 116.(paragraph [0072] of citation 1)

Comparison and comments:

(1) Regarding independent claim 1 of the present application, we found that citation 1 fails to disclose the technical feature "a multi-layer charge storing layer including an oxygen-rich, first oxynitride layer on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean, second oxynitride layer on the first oxynitride layer in which a stoichiometric composition of the second oxynitride

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layer results in it being trap dense" as disclosed in claim 1 of the present application. The examiner deems that "the trapping layer 114" of citation 1 may correspond to "an oxygen-rich, first oxynitride layer" as disclosed in claim 1 of the present application, and "the charge blocking layer 116" of citation 1 may correspond to "an oxygen-lean, second oxynitride layer"as disclosed in claim 1 of the present application. The trapping layer 114 of citation 1 is used to trap charges therein, but the oxygen-rich, first oxynitride layer of the present application is substantially trap free. In addition, the charge blocking layer 116 of citation 1 is used to blocking charges, but the oxygen-lean, second oxynitride layer of the present application is trap dense.

Accordingly, the main elements (such as an oxygen-rich, first oxynitride layer and an oxygen-lean, second oxynitride layer) disclosed in claim 1 of the present application are entirely different from the cited layers (the trapping layer 114 and the charge blocking layer 116) of citation 1, and therefore the present application has novelty in view of citation 1. In addition, the present application introduces an oxygen-rich, first oxynitride layer and an oxygen-lean, second oxynitride layer disclosed in claim 1 of the present application which exhibit improved programming and erase speed and data retention for a memory device. An ordinarily skilled person in the art cannot easily achieve said claim based on the citations and the present application has unexpected effects. Therefore, claim 1 of the present application is patentable over citations 1-5.

Furthermore, the dependent claims 2-8 of the present application will be patentable if claim 1 successfully overcomes the rejection reasons of the Examiner.

(2) Regarding independent claim 9 of the present application, we found citations 1 and 5 fail to disclose the technical feature "wherein the first oxynitride layer is a substantially trap free, oxygen-rich, oxynitride layer, and the second oxynitride layer is a trap dense, oxygen-lean, oxynitride layer further comprising a concentration of carbon selected to increase a number of traps therein" as disclosed in claim 14 of the present application. The applicant may consider incorporating said feature into claim 9 to clearly define claim 9 of the present application. In addition, said feature is also disclosed in claim 1 of the present application, whereby similar arguments as for claim 1 may also be applied to amended claim 9.

Furthermore, the dependent claims 10-13 of the present application will be

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patentable if amended claim 9 successfully overcomes the rejection reasons of the Examiner.

3. Furthermore the Taiwan Patent Examination Guidelines stipulate: the title of the patent for invention should clearly and *simply reflect the subject matters of the claims*. Therefore, we suggest amending the current title to "*MEMORY DEVICE*" to avoid a rejection due to the above mentioned issue.

4. With regard to point 2 in the Examination Report, the TIPO simply informs the applicant of some administrative regulations with respect to supplements and amendments, which will be handled at our end.

5. With regard to point 3 in the Examination Report, the TIPO simply informs the applicant that an interview with the examiner can be requested when a response is submitted to TIPO. The examiner will decide whether to hold such an interview or not. If you think that an interview with the examiner is needed, we will simultaneously request one in the response.

6. With regard to point 4 in the Examination Report, we have translated the Search Report into English and attached it to the end of the translation report for your reference.

Please inform us concurrently with your instructions for responding to the Official Letter if any other amendment to the present application is to be made with the response.

If a corresponding application has been allowed or any information that will be helpful in defense of the level of inventiveness or patentability of the present invention is available, please inform us accordingly.

We look forward to receiving your instructions at your earliest convenience so that we can prepare the response and file the same with the Intellectual Property Office in due course.

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October 15, 2015

Attn.: Ms. Flora Hachemi
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Glasgow G5 8PL
United Kingdom

Via E-mail Only
Tel: 0044 141 307 8400
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E-mail: flora.hachemi@murgitroyd.com

Re: New Invention Patent Application in Taiwan
In the name of Cypress Semiconductor
Title: Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers
TW application No.: 101101220
Your Ref.:P123443.TW.01
Our Ref.:111203848-TW

Dear Ms. Hachemi:

In connection with the above-referenced application, the Taiwan Intellectual Property Office (TIPO) recently issued the First Office Action, and the original Taiwanese text of which is attached for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below.

Part I. Claims 1, 6, 11 and 18 are not in conformity with the provisions of Article 26(2) of Taiwan Patent Act.

1. Claims 1, 6 and 11

The Examiner points out that the scopes of claims 1, 6 and 11 are unclear, since as to "an oxygen-rich, first oxynitride layer" and "an oxygen-lean, second oxynitride layer" recited in claims 1, 6 and 11, the range of "oxygen-rich" and "oxygen-lean" are not clearly defined.

2. Claim 18

The Examiner points out that the scope of claim 18 is unclear since the technical feature "SiH_2CI_2/NH_3 mixture" in claim 18 should be "SiH_2Cl_2/NH_3 mixture".

Part II. Claims 1, 6, 11-12, 16, 18-19 and 21 are not in conformity with the provisions of Article 22.1(1) of Taiwan Patent Act based on the disclosure of Reference 1; claims 2-4, 7-9, 13-15, 17 and 20 are not in conformity with the provisions of Article 22(2) of Taiwan Patent Act based on the disclosure of Reference 1; claims 5, 10 and 22-23 are not in conformity with

Sandisk Technologies, Inc. - Ex. 1002, Page 001155

the provisions of Article 22(2) of Taiwan Patent Act based on the disclosure of References 1-2.

The cited reference documents are as follows:

Reference 1: TW200847343A; December 1, 2008

Reference 2: CN1832201A; September 13, 2006

1. Claim 1

The Examiner points out that claim 1 does not possess novelty since Reference 1 (page 17, lines 4-24 and page 18, lines 1-8 of its Description, and Fig. 5) discloses the same invention as claim 1.

2. Claims 2-3

The Examiner points out that Reference 1 (page 17, lines 4-24 and page 18, lines 1-8 of its Description) discloses relevant technical feature, and claims 2-3 differ from Reference 1 in their additional technical features, which, however, can be easily accomplished by a person skilled in the art through simple modification according to oxygen content and the requirement of the traps.

3. Claim 4

The Examiner points out that Reference 1 (page 17, lines 4-24 and page 18, lines 1-8 of its Description) discloses relevant technical feature, and claim 4 differs from Reference 1 in the technical feature "a charge trap density at least 1000 times greater", which, however, can be easily accomplished by a person skilled in the art through simple modification according to the requirement of the traps.

4. Claim 5

The Examiner points out that claim 5 does not possess an inventive step. The Examiner holds that Reference 2 (see page 9, lines 26-31 and page 10, lines 1-2 of its Description, and Fig. 3) discloses relevant technical features, and thus the technical scheme of claim 5 can be easily accomplished by a person skilled in the art on the basis of a simple combination of References 1-2.

5. Claim 6

The Examiner points out that claim 6 does not possess novelty since Reference 1 (see page 17, lines 4-24 and page 18, lines 1-8 of its Description, and Fig. 5) discloses the same invention as claim 6.

6. Claims 7-8

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Please refer to the above point 2 in Part II for details.

7. Claim 9

Please refer to the above point 3 in Part II for details.

8. Claim 10

The Examiner points out that claim 10 does not possess an inventive step. The Examiner holds that Reference 2 (page 9, lines 26-31 and page 10, lines 1-2 of its Description, and Fig. 3) discloses relevant technical feature, and thus the technical scheme of claim 10 can be easily accomplished by a person skilled in the art on the basis of a simple combination of References 1-2.

9. Claim 11

The Examiner points out that claim 11 does not possess novelty since Reference 1 (see page 17, lines 4-24 and page 18, lines 1-8 of its Description, and Fig. 5) discloses the same invention as claim 11.

10. Claim 12

The Examiner points out that the additional technical feature of claim 12 is disclosed by Reference 1 (page 16, lines 14-24, page 17, and page 18, lines 1-8 of its Description).

11. Claims 13-15

The Examiner points out that Reference 1 (page 17, lines 4-24 and page 18, lines 1-8 of its Description) discloses relevant technical feature, and claims 13-15 differ from Reference 1 in their additional technical features, which, however, can be easily accomplished by a person skilled in the art through simple modification according to oxygen content and the requirement of the traps.

12. Claim 16

The Examiner points out that Reference 1 (page 9, lines 15-24 and page 10, lines 1-7 of its Description) has disclosed the additional technical feature of claim 16.

13. Claim 17

Please refer to the above point 3 in Part II for details.

14-15. Claims 18-19

The Examiner points out that Reference 1 (page 28, lines 5-22 of its Description) has disclosed the additional technical features of claims 18-19.

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16. Claim 20

The Examiner points out that the additional technical feature of claim 20 is merely well known technique in the art.

17. Claim 21

The Examiner points out that Reference 1 (page 21, lines 4-17 of its Description) discloses relevant technical feature, and claim 21 differs from Reference 1 in the technical feature "high density plasma (HDP) oxidation", which, however, is well known technique in the art,.

18. Claim 22

The Examiner points out that claim 22 does not possess an inventive step. The Examiner holds that Reference 2 (page 9, lines 26-31 and page 10, lines 1-2 of its Description, and Fig. 3) discloses relevant technical features, and thus the technical scheme of claim 22 can be easily accomplished by a person skilled in the art on the basis of a simple combination of References 1 and 2.

19. Claim 23

The Examiner points out that the additional technical feature of claim 23 is disclosed by Reference 1 (see page 28, lines 5-22 of its Description).

A response and possible amendments must be submitted to the Office by **December 8, 2015 (Beijing Time)**. Please give us your further instructions as soon as possible.

In addition, the Examiner added a Search Report as the attachment of this Office Action. Kindly inform us if you would like us to translate the Report. The fee for translating the report will be US$50.00.

Please kindly confirm receipt of this letter by return e-mail. Should you have any questions, please do not hesitate to contact us. We look forward to hearing from you. Your promptly reply is highly appreciated.

Sincerely yours,
AFD China Intellectual Property

Cuiling Du

Xia Zheng (patent@afdip.com)
Assisted by Cuiling Du (patent@afdip.com)

Wrf/Jhq
Enclosures: (All by E-mail only)
1. The Notification of the First Office Action;
2. Two sets of cited documents; and
3. Our invoice No. IFP20150327.

Sandisk Technologies, Inc. - Ex. 1002, Page 001158

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/811,958	06/13/2007	Sagy Levy	PM2007002	9184

60909 7590 03/16/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
03/16/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action

1. On cursory consideration, the request for reconsideration and the proposed amendment, which has NOT been entered, does not clearly appear to overcome the rejection.

   By adding limitation "…are formed using process gases comprising deuterated-amonia (ND3); and…." And removing limitation "...a thickness..." into claim 9 raises new issue for claim 12 – 16 and 25, which was not part of the rejected claims as set forth in previous office actions.

   Further, the amendment neither deemed to place the application for allowance nor place the application in better form for appear by materially reducing or simplifying the issue for appear as set forth under 37 CFR 1.116.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday - Thursday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 1-571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/
/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 11/811,958	**Applicant(s)** LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	**Art Unit** 2894	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 02 March 2010 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,6-9,12-16,and 21-26*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See attached detailed advisory action.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894

/MOHAMMAD CHOUDHRY/
Examiner, Art Unit 2894

Sandisk Technologies, Inc. - Ex. 1002, Page 001162

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/811,958	06/13/2007	Sagy Levy	PM2007002	9184

60909 7590 04/20/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
04/20/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action

On cursory consideration, the request for reconsideration, which has been entered, does not clearly appear to overcome the rejection.

Response to Arguments

1. Applicant's arguments with respect to claim 1 have been considered and found not persuasive.
2. Applicant argue as follows:

> By this response claim 9 has been amended to include features previously introduced in claim 25 that depends therefrom. In particular, claim 9 has been amended to include the feature of "the top oxynitride layer is formed using a process gas comprising a dichlorosilane (SiH_2Cl_2)/ deuterated-ammonia (ND_3) mixture and a nitrous oxide (N_2O)/ ND_3mixture, and the bottom oxynitride layer is formed using a process gas comprising a N_2O/ ND_3mixture and a SiH_2Cl_2/ ND_3 mixture."
>
> As the examiner previously examined and rejected claim 25 as being allegedly obvious over JENNE in view of MINE, a position with which applicants disagree, the applicants submit that the amendments to independent claim 9 do not raise new issues.

Arguments are moot in view of amended claim 9.

Applicant further argues as follows:

The examiner states on page 2 of the office action:

> With respect to claim 1, Jenne discloses in a second embodiment a method of forming a charge storing layer (304-0 of Figure 3D) of a semiconductor device (Figure 4), the method comprising steps of: depositing on a substrate (300 of Figure 3B) a silicon-rich nitride (Step 404 and 406 of Figure 4) and oxidizing (Col 6, Lines 42-43) the silicon-rich nitride layer.

Applicants disagree.

The full paragraph including 42-43 of Col. 6 cited by the examiner is reproduced below.

> Having described one method according to an embodiment, a second, more detailed embodiment will now be described. A second embodiment method is set forth in FIG. 4, and designated by the general reference character **400**. A method **400** may include growing a tunneling oxide (step **402**). According to one embodiment, a tunneling oxide may include cleaning a semiconductor substrate to expose a silicon surface. A silicon surface may then be subjected to an oxidizing environment to form a tunneling oxide.

Referring to the above paragraph, the applicants note that the oxidizing step referred to by the examiner refers to the step of growing an tunneling oxide (step **402**), which occurs *before* the step of depositing nitride (step **404**) and altering deposition variables to increase silicon concentration in a silicon nitride layer (step **406**). Thus, applicants submit that JENNE does not teach or suggest "oxidizing the silicon-rich nitride" to form a "first oxynitride layer."

Examiner respectfully disagrees for at least the following reason(s).

Jenne has disclosed that Silicon Nitride can be a silicon oxynitride (i.e. see column 4, lines 30 - 40) and has disclosed oxidization method as above. Oxidizing silicon nitride to obtain silicon oxynitride layer method is extremely well known in the art. Further to satisfy applicant's arguments, Examiner invites the applicant to pertinent art of Schwabe et al and Sung (Conclusion section below).

Applicant makes another argument as follows:

> Applicants respectfully disagree, and submit that in focusing on the particular ratios claimed the examiner failed to note that such process gases comprising deuterated-ammonia (NDD) are not taught or suggested by JENNE or MINE alone or in combination.

Examiner respectfully disagrees for at least the following reason(s).

Jenne has disclosed the claimed invention except for explicit disclosure of deuterated ammonia. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use deuterated ammonia instead of ammonia as known equivalent of ammonia for their use in the semiconductor

manufacturing as known nitriding gases and selection of any of these known equivalents would be within the level of ordinary skill in the art. Examiner invites the applicant to pertinent art of Senzaki (US 2005/0070126). For instance, in Senzaki, several other suitable nitridating gases include ammonia, deuterated ammonia, .sup.15N-ammonia, hydrazine, alkyl hydrazines, nitrogen dioxide, nitrous oxide, nitrogen radical, nitric oxide, N-oxides, amides, amines, and mixtures thereof.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Col 1, Lines 35 – 40 of Schwabe et al (US 4257832) and Col 10, Lines 1-6 of Sung (US 5550078) & Page 7, Para 0078 of Senzaki (US 2005/0070126).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday - Thursday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 1-571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/MC/

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 11/811,958	**Applicant(s)** LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	**Art Unit** 2894	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 02 April 2010 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,6-9,12-16 and 21-26*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: Please see attached detailed response..
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894

/MOHAMMAD CHOUDHRY/
Examiner, Art Unit 2894

Sandisk Technologies, Inc. - Ex. 1002, Page 001168

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/811,958	06/13/2007	Sagy Levy	PM07002	9184

60909 7590 05/14/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
05/14/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 001169

Advisory Action

On cursory consideration, amendment as filed on 05/01/2013 have been considered and preliminary search as recorded show that a thorough examination of prior art is required. Therefore, application cannot be allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 1-571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

Advisory Action Before the Filing of an Appeal Brief	**Application No.** *11/811,958*	**Applicant(s)** LEVY ET AL.
	Examiner MOHAMMAD CHOUDHRY	**Art Unit** 2898

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 05/01/2013 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance;

(2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:

a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because

a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);

b) ☐ They raise the issue of new matter (see NOTE below);

c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See attched response..

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

STATUS OF CLAIMS

14. The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: .

Claim(s) objected to: .

Claim(s) rejected: 29-34,36-41,43-45,49 and 53-55.

Claim(s) withdrawn from consideration: .

/JULIO J. MALDONADO/
Supervisory Patent Examiner, Art Unit 2898

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/811,958	06/13/2007	Sagy Levy	PM07002	9184

60909 7590 06/02/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
06/02/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Sandisk Technologies, Inc. - Ex. 1002, Page 001173

Continuation Sheet (PTO-303)

Advisory Action

On cursory consideration, the request for reconsideration, which HAS been entered, does not clearly appear to overcome the rejection.

Response to Arguments

1. Applicant's arguments with respect to claim 1 have been considered and found not persuasive. Applicant argues as follows:

> Applicants disagree and note that as shown in FIG. 1A of Bhattacharyya and described in paragraph [0075], the sole point in the detailed description at which the tunneling layer 112 is described as including SiON, the SiON layer of the tunneling layer 112 is the middle of 3 layers (labeled K_2 in FIG. 1A) and is formed over the first layer SiO_2 formed over the channel region 108, and underlying the third layer of HfO_2. Thus, applicants submit that the cited reference does not teach or suggest depositing on the first oxynitride layer an oxygen-lean second oxynitride layer.

Examiner respectfully disagrees for at least the following reason(s):

Applicant disclosure does not limit examiner's interpretation of 'on' to be 'directly' on. Ordinary meanings of 'on' can include inter layers. A second oxynitride layer is shown to be formed on the first oxynitride layer as taught in the applied prior art. Therefore, rejection of claims is maintained.

> Applicants further submit that claim 8 of Bhattacharyya relied on by the Examiner as allegedly teaching an "oxygen-lean second oxynitride layer," does not teach or suggest an "oxygen-lean second oxynitride layer" but to the contrary teaches an oxygen-rich silicon oxynitride (SiON) mapping layer.

Examiner respectfully disagrees for at least the following reason(s):

Claim 8 teaches forming second oxynitride layer to be 'one' of oxygen-rich silicon oxynitride or nitrogen-rich silicon oxynitride layer. It is clear from the disclosure that oxygen contents has to be lower when nitrogen contents are rich.

Therefore, rejection of the claims is maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday - Thursday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 1-571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 11/811,958	**Applicant(s)** LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	**Art Unit** 2894	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 13 May 2011 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See attached detailed response.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894

/MOHAMMAD CHOUDHRY/
Examiner, Art Unit 2894

Sandisk Technologies, Inc. - Ex. 1002, Page 001177

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

60909 7590 08/04/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
08/04/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 13/436,872	**Applicant(s)** LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	**Art Unit** 2816	**AIA (First Inventor to File) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 21 July 2015 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: Proposed amendment required consideration and/or further search. Further submission under AFCP 2.0 is improper as it appears to be broaden the scope of the amended claim..
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed: 9-13.
    Claim(s) objected to: .
    Claim(s) rejected: 1-8 and 21.
    Claim(s) withdrawn from consideration:

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/811,958	06/13/2007	Sagy Levy	PM2007002	9184

60909 7590 01/06/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
01/06/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/811,958	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6-9,12-17,19 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-9,12-17, 19, 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 6-9, 12-13, 15-16, 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenne et al (US 6709928), hereinafter refereed as Jenne in view of Mine et al (US 2004/0183122), hereinafter refereed as Mine.

With respect to claim 1, Jenne discloses in a second embodiment a method of forming a charge storing layer (304-0 of Figure 3D) of a semiconductor device (Figure 4), the method comprising steps of: depositing on a substrate (300 of Figure 3B) a silicon-rich nitride (Step 404 and 406 of Figure 4) and oxidizing (Col 6, Lines 42-43) the silicon-rich nitride layer.

Jenne does not explicitly disclose forming over a surface of the first oxynitride layer a silicon-rich, nitrogen-rich, oxygen-lean second oxynitride layer.

In an analogous art, Mine discloses forming a surface of the first oxynitride layer a silicon-rich, nitrogen-rich, oxygen-lean second oxynitride layer (i.e. Fig. 11 & ¶0084 - ¶0090)

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Jenne and for an oxynitride layer that is silicon-rich and oxygen-lean, as taught by Mine to suppress Gm degradation significantly(Page 10, ¶133, Lines 15-16).

With respect to claim 6 & 21 - 23, Jenne in view of Mine discloses a method according to claim 1, as above. Jenne further discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) (Col 7, Line 18) process using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide ('N20)/NH3 mixture at (Col 7, Lines 12-15).

Jenne does not disclose *exact* ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1.

However, Jenne discloses that NH3 flow rate 2-4 times greater than dichlorosilane and also N2O flow rate is 1-3 times greater than dichlorosilane. (Col 7, Lines 17–24) Jenne further discloses that these flow rates can be switched from 3 -1 or 4 - 2 times during formation of oxynitride layers (Col 7, Lines 42-43). Generally, differences in concentration or flow rate will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or flow rate is critical to the invention. Wherein top and bottom oxynitride layers comprises a combined overall thickness of from 70 A to 150 A. wherein a thicknesses of the second oxynitride layer is from 1 to 5 times greater than that of the first oxynitride layer. Wherein the first and second oxynitride layers comprises a

combined overall thickness of from 70 A to 150 A. wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3mixture at a ratio of about 5:1. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In Re Aller, 105 USPQ 233. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966).

Therefore, It is obvious to one of an ordinary skilled in the art at the time of invention to optimize the flow rate with precursor gases disclosed in Jenne's invention and form oxynitride single or multiple layers to enhance programming characteristics as well as data retention in memory (Col 2, Lines 50-55).

With respect to claim 7 & 24, Jenne in view of Mine discloses a method according to claim 6 & 23 respectively.

Jenne discloses the forming the first oxynitride layer and the second oxynitride layer (304-0 and 304-1 – and/or as equivalent to Mine's disclosed second oxynitride - of Fig. 3D) in CVD tool (Col 7, Line 14) by changing the ratio of the N20/NH3 and SiH2C12/NH3 mixtures (limitations addressed in claim 6 above).

Jenne dose not explicitly states forming a first oxynitride layer and second oxynitride layers sequentially in a single CVD tool. However, it has to be obvious to one of an ordinary skilled in the art at the time of invention to form layer 304-0 first prior to forming second layer 304-1 as shown in figure 2E). Further, if a single layer of oxynitride can be formed in a CVD tool, second layer can be formed using the same tool to lower manufacturing cost or to use CVD multiple times.

With respect to claim 8, Jenne in view of Mine discloses a method according to claim 6, as above.

Jenne further discloses forming one of the first oxynitride layers and the second oxynitride layer (i.e. Jenne; 304-1 – and/or as equivalent to Mine's disclosed second oxynitride) at temperature of at least about 780 °C (Col 7, Line 24).

With respect to claim 9, 26, Jenne disclose a method comprising steps of." forming a first oxide layer of the (302 of Fig. 3D & Col 6, Line 27); forming a multi-layer (304-0 & 304-1 of Fig. 3D) charge storing layer comprising nitride on a surface of the first oxide layer; and forming a second oxide layer (308 of Fig 3E) on a surface (308 is on 304-1 of Fig. 3E) of the multi-layer charge storing layer.

Jenne discloses a structure (Fig. 3E) with oxide-oxynitride-oxide where oxynitride can contains content of nitride capable of forming an oxide-nitride-oxide (ONO) structure.

Jenne does not *explicitly* disclose a multi-layer charge storing layer having at least two silicon oxynitride layers including a top oxynitride layer and a bottom oxynitiride layer having differing stochiometric composition of oxygen, nitrogen and silicon and where in a thickness of the top oxynitride layer is from 1 to 5 times great than that of the bottom oxynitride layer.

In an analogous art, Mine discloses a multi-layer charge storing layer (i.e. as shown in Fig. 11) having at least two silicon oxynitride layers (i.e. can be 5/6 of Fig. 11) including a top oxynitride layer and a bottom oxynitiride layer having differing stochiometric composition of oxygen (i.e. oxygen concentration shown for 5 of Fig. 11), nitrogen and silicon and where in a thickness (i.e. ¶0084 - ¶0090) of the top oxynitride layer is from 1 to 5 times great than that of the bottom oxynitride layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In Re Aller, 105 USPQ 233. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d

1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Jenne's disclosed invention and form optimum ONO structure thickness as disclosed by Mine, to achieve optimum charge trapping characteristics (i.e. Mine; ¶0090).

With respect to claim 12, Jenne in further view of Mine discloses a method according to claim 9, as above.

Jenne further discloses a top oxynitride layer and a bottom oxynitride layer as being silicon-rich, as above.

Jenne fails to disclose the top oxynitride layer is formed under conditions selected to form oxygen-lean oxynitride layer, and the bottom oxynitride layer is formed under conditions selected to form a oxygen-rich oxynitride layer.

In an analogous art, Mine discloses a top oxynitride (304c of Fig.4) layer is formed under conditions selected to form oxygen-lean (Page 9, ¶131) oxynitride layer, and a bottom oxynitride layer (304b of Fig.4) is formed under conditions selected to form a oxygen-rich oxynitride layer. If oxygen contents of top oxynitride are suggested to be lower than oxygen contents of the bottom oxynitride layer then, bottom oxynitride layer has to be oxygen rich as compare to top oxynitride layer as suggested by Mine (Page 9, ¶131).

It would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Jenne disclosed invention with oxygen-lean top oxynitride layer and

oxygen-rich bottom oxynitride layer, as taught by Mine to achieve optimum lamination to form the insulator film (Page 9, ¶131, Lines 8 – 9).

With respect to claim 13, Jeene in view of Mine discloses a method according to claim 12.

Jenne fails to disclose the top oxynitride layer is nitrogen-rich oxynitride layer.

In an analogous art, Mine disclose forming an oxynitride layer that can be nitrogen-rich if oxygen contents are lowered (Page 6, ¶86). In claim 12, applicant claimed to form top oxynitride layer as being oxygen lean. Hence, top oxynitride layer has to be nitrogen-rich.

It would have been obvious to form an oxynitride layer containing lean oxygen and rich nitrogen contents, as taught by Mine to form a oxynitride layer using CVD with enhanced oxygen, nitrogen and silicon concentration (Col 6, ¶83).

With respect to claim 15, Jenne in view of Mine discloses a method according to claim 12.

Jenne discloses the forming top (304-0 of Fig 3D) and bottom oxynitride layers (304-1 of Fig. 3D) oxynitride layer is formed in a chemical vapor deposition (CVD) (Col 7, Line 18) process using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide ('N20)/NH3 mixture at (Col 7, Lines 12-15).

Jenne does not disclose *exact* ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. However, Jenne discloses

that NH3 flow rate 2-4 times greater than dichlorosilane and also N2O flow rate is 1-3 times greater than dichlorosilane. (Col 7, Lines 17–24) Jenne further discloses that these flow rates can be switched from 3 -1 or 4 - 2 times during formation of oxynitride layers (Col 7, Lines 42-43). Generally, differences in concentration or flow rate will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or flow rate is critical to the invention.

It would have been obvious to one of an ordinary skilled in the art at the time of invention to optimize the flow rate with precursor gases disclosed in Jenne's invention and form oxynitride single or multiple layers to enhance programming characteristics as well as data retention in memory (Col 2, Lines 50-55).

With respect to claim 16, Jenne in further view of Mine discloses a method according to claim 9, as above.

Jenne further disclose at least two oxynitride layers are formed at temperature of at least about 780 °C (i.e. Col 7, Line 24).

With respect to claim 25, Jenne in further view of Mine discloses a method according to claim 12, wherein the top oxynitride layer is formed using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3mixture at a ratio of about 5:1, and the bottom oxynitride layer is formed using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3mixture at a ratio of about 8:1. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In Re Aller, 105 USPQ 233. Indeed, it has been held that mere

dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966).

3. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mine et al (US 2004/0183122), hereinafter Mine in further view of ITO et al (US 4543707, hereinafter Ito).

With respect to claim 17, Mine discloses a semiconductor device including an oxide-nitride-oxide (ONO) structure (Figure 4) comprising a multilayer memory layer between a first oxide layer (304a of Fig.4) and a second oxide layer (305 of Fig.4), wherein the multilayer memory layer. Forming silicon rich, oxygen rich bottom oxynitride layer and at least one silicon-rich, nitogren-rich, oxygen-lean oxynitride layer overlaying the bottom oxynitride layer (i.e. ¶0084 - ¶0090).

Mine does not explicitly shows forming at least three silicon oxynitride layers having differing stochiometric composition of oxygen, nitrogen, and silicon.

In an analogous art, Ito discloses forming a at least three silicon oxynitride layers (i.e. Fig. 7, 44, 46, 48, & 50 & Col 5, Lines 9 – 25) having different stochiometric composition of oxygen, nitrogen, and silicon. Although forming repeating layer structure has been address here with the reference, it has been held that mere duplication of the

essential working parts of a device involves only routine skill in the art. St Regis Paper Co. V Bennis Co, 193 USPQ 8. For instance, applicant admitting in the specification that adding more layer is not desirable and will impact yield (i.e. Page 15, Lines 10 -20).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Mine's disclosed invention and form a three silicon oxynitride layers to achieve optimum insulation characteristics (i.e. Ito; Col 5, Lines 9 - 25).

With respect to claim 18, Mine in further view of Ito discloses a semiconductor device according to claim 17, as above. Mine further discloses at least two oxynitride having Silicon, Oxygen, Nitrogen ,Hydrogen contents having differing stochiometric compositions of oxygen, nitrogen and/or silicon to form multiple oxynitride layers (i.e. Fig. 11, ¶0084 - ¶0090).

Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. Hence, it is obvious to one of an ordinary skilled in the art to have differing stochiometric compositions of oxygen, nitrogen and/or silicon to form multiple oxynitride layers to enhance programming characteristics (Col 2, Line 55).

With respect to claim 19, Mine in further view of Ito discloses a semiconductor device according to claim 17, as above. Mine further discloses different ways to improve data/charge retention characteristics using oxygen, nitrogen and silicon profiles across the at least two oxynitride layers. For instance, when a silicon oxynitride film was used

as a charge trapping film, the writing speed, the erasing speed, and the charge retention characteristics were all improved… (Page4, Col 63). At another instance, The charge retention characteristics were evaluated by writing information in the memory cell until a predetermined threshold value is reached (step 1), concretely, applying 1.8 V to the memory MOS transistor gate electrode (step 2), leaving the memory cell for 100,000 seconds at 85 deg.C, then comparing the threshold value just after the writing with that after the leaving at the high temperature (step 3) (Page 3, ¶50). It is clear that data retention specification is a function of operating temperature, applied voltage and material used as well as duration for which data can be retained.

It is obvious to one of an ordinary skilled in the art at the time of invention to modify a known technique to a known device as disclosed in Mine's invention and achieve data retention specification at an operating temperature of at least 125°C to enhance characteristics of a non-volatile memory device (Page 2, ¶17).

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jenne (US 6709928), hereinafter refereed as Jenne in view of Mine et al (US 2004/0183122), hereinafter refereed as Mine in further view of Wu et al, (US 6445030), hereinafter refereed as Wu.

With respect to claim 14, Jenne in view of Mine discloses a method according to claim 12, as above.

In an analogous art, Mine discloses a relation of T2<(N1 x T1)/N2, where T1 and T2 are thickness of top and bottom layer and N represent electron trap density of the

top and bottom film to form a multi-layer memory structure (Mine; Page 9, ¶131 & Page 7, ¶98).

Mine fails to disclose forming a tunnel oxide layer using a steam anneal.

In an analogous art, Wu discloses forming an oxide growth using CVD containing oxygen, water vapor and optionally one or more of inert gases (Wu; Col 5, Lines 17-22).

It would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Jenne and select different thickness of a oxynitride layers, as taught by Mine and form oxide layer using steam anneal, as taught by Wu to speedup erasing process and improve charge trapping/storing characteristics (Mine; Page 7, ¶98).

5. Claims 27 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mine et al (US 2004/0183122), hereinafter Mine in further view of ITO et al (US 4543707, hereinafter Ito) in further view of Gu (US 6157426, hereinafter Gu).

With respect to claim 27, Mine in view of Ito discloses a semiconductor device according to claim 17.

Mine in view of Ito fails to explicitly disclose the multilayer memory layer comprises up to *five* oxynitride layers each differing stochiometric composition of oxygen, nitrogen, and silicon.

In an analogous art, Gu discloses five oxynitride layers (i.e. Front page, 3 of disclosed figure) each differing stochiometric composition of oxygen, nitrogen, and silicon. Although forming repeating layer structure has been address here with the reference, it has been held that mere duplication of the essential working parts of a

device involves only routine skill in the art. St Regis Paper Co. V Bennis Co, 193 USPQ 8. For instance, applicant admitting in the specification that adding more layer is not desirable and will impact yield (i.e. Page 15, Lines 10 -20).

Therefore, it would have been obvious to one an ordinary skilled in the art at the time of invention to modify Mine in view of Ito's disclosed invention and form five layers of oxynitride layer to achieve optimum refractive index.

With respect to claim 28, Mine in further view of Ito and in further view of Gu discloses a semiconductor device according to claim 27, wherein the multilayer memory layer comprises a thickness of from 70 A to 150 A, wherein a combined thickness of the oxynitride layers other than the bottom oxynitride layer comprises a thickness of from 1 to 5 times that of the bottom oxynitride layer. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In Re Aller, 105 USPQ 233. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966).

Response to Arguments

Applicant's arguments with respect to claim *1, 6-9, 12-19 and 21-28* have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday - Thursday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 1-571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894

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CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2898	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/811,958	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2898	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/29/2012*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *29-34,36-41,43-45,49, and 53-55* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *29-34,36-41,43-45,49, and 53-55* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 29-34, 37-41, 44-45 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 11-21 & 23 of copending Application No. 13/007,533 (hereinafter referred to as '533). Although the conflicting claims are not identical, they are not patentably distinct from each other because;

With respect to claim 29. '533 discloses a method of forming a semiconductor device comprising: forming a multi-layer charge storing layer comprising depositing on a substrate an oxygen-rich, first oxynitride layer and depositing directly on the first oxynitride layer an oxygen- lean and silicon-rich second oxynitride layer; and wherein a stoichiometric composition of the first oxynitride layer comprises a high concentration of oxygen selected to increase retention performance of the multi-layer charge storing layer by acting as a barrier between charge trapped in the second oxynitride layer and the substrate (e.g. '533 - Claim 11).

With respect to claim 30. '533 discloses a method according to claim 29, wherein the increased retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years (e.g. '533 – Claim 16).

With respect to claim 31. '533 discloses a method according to claim 29, wherein the wherein the first oxynitride layer is formed in a chemical vapor deposition

(CVD) process using a process gas comprising a dichlorosilane (SiHzClz)/ammonia (NH3) mixture and a nitrous oxide (NzO)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a NzO/NH3 mixture and a SiHzClz/NH3 mixture at a ratio of about 5:1 (e.g. '533 - Claim 18).

With respect to claim 32. '533 discloses a method according to claim 31, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the NzO/NH3 and SiHzClz/NH3 mixtures (e.g. '533 - Claim 19).

With respect to claim 33. '533 discloses a method according to claim 29, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1 (e.g. '533 - Claim 18).

With respect to claim 34, '533 discloses a method according to claim 33, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20/ND3and SiH2C12/ND3 mixtures (e.g. '533 - Claim 19).

With respect to claim 37. '533 discloses a method of forming a semiconductor device comprising: forming a multi-layer charge storing layer comprising depositing on a

substrate an oxygen-rich, first oxynitride layer and depositing directly on the first oxynitride layer an oxygen- lean and silicon-rich second oxynitride layer; and wherein a difference in stoichiometric composition of the first oxynitride layer and the second oxynitride layer is selected to increase a difference between programming and erase voltages, thereby increasing data retention, improving speed of the semiconductor device and increase an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years (e.g. '533 - claim 11 and Claim 16).

With respect to claim 38. '533 discloses a method according to claim 37, wherein the wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiHzClz)/ammonia (NH3) mixture and a nitrous oxide (NzO)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1 (e.g. '533 – Claim 18).

With respect to claim 39. '533 discloses a method according to claim 38, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the NzO/NH3 and SiHzClz/NH3 mixtures (e.g. '533 – Claim 19).

With respect to claim 40. '533 discloses a method according to claim 37, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiHzCl2)/deuterated-

ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiHzCI2/ND3 mixture at a ratio of about 5:1 (e.g. '533 – Claim 18).

With respect to claim 41. '533 discloses a method according to claim 40, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20/ND3and SiHzCI2/ND3 mixtures (e.g. '533 – Claim 19).

With respect to claim 44. '533 discloses a method of forming a semiconductor device comprising: forming a multi-layer charge storing layer comprising depositing on a substrate in a chemical vapor deposition (CVD) process an oxygen-rich, first oxynitride layer using a process gas comprising a dichlorosilane (SiHzCI2)/ deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a first ratio and depositing directly on the first oxynitride layer an oxygen-lean and silicon-rich second oxynitride layer using a process gas comprising a N20/ ND3mixture and a SiHzCI2/ND3 mixture at a second ratio, wherein depositing the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20/ND3and SiH2C12/ ND3 mixtures~ and wherein a difference in stoichiometric composition of the first oxynitride layer and the second oxynitride layer is selected to increase a difference between programming and erase voltages, thereby increasing data retention, improving speed of the semiconductor device and increase an end-of-life (EOL) for the semiconductor device (e.g. '533 - Claims 1 & 19).

With respect to claim 45. '533 discloses a method according to claim 44, wherein the first ratio of the N20/ND3 and SiH2C12/ND3 mixtures is about 8:1, and wherein the second ratio of the N20/ND3 and SiH2C12/ND3 mixtures is about 5:1 (e.g. '533 – Claim 18).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29-30, 36-37, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya).

Re claim 29, 37, Bhattacharyya discloses a method of forming a semiconductor device (e.g. 100 of Fig.1A) comprising: forming a multi-layer charge storing layer (e.g. 112/114/116/117 and 118 of Fig. 1A), depositing on a substrate (e.g. p-Si substrate) an oxygen-rich, first oxynitride layer (e.g. 112 of Fig. 1A & Claim 3) and depositing directly (e.g. 112 is directly on 114) on the first oxynitride layer an oxygen-lean (e.g. 114 of Fig.1A & Claim 8) second oxynitride layer sequentially (e.g. are shown to deposited one after another of Fig.1A), a high concentration of oxygen selected to increase retention (e.g. …good charge retention….See abstract) performance of the multi-layer charge storing layer by acting as a barrier (e.g. charge trapping for instance) between charge

trapped in the second oxynitride layer and the substrate (e.g. device of Fig.1A being capable of), wherein a difference in stoichiometric composition of the first oxynitride layer and the second oxynitride layer is selected to increase a difference between programming and erase voltages, thereby increasing data retention, improving speed of the semiconductor device and increase an end-of-life (EOL) (e.g. See abstract, ...device of 1A to enhance life span) for the semiconductor device at a specified difference (e.g. abstract, direct tunneling program and erase) between program and erase voltages to at least about 20 years(e.g. method as disclosed is indeed to enhance life span and inherently capable of a mere use).

Bhattacharyya does not explicitly disclose the second oxynitride layer to be silicon-rich, oxygen layer in a single disclosed embodiment as above.

However, Bhattacharyya do disclose that second oxynitride layer to be made by silicon-rich nitride and nitride layer can be a substitute with oxynitride layer (e.g. Claim 28, Para 0061).

Therefore, it would have been obvious to one an ordinary skilled in the art at the time of invention to modify Bhattacharyya disclosed invention and form stacked oxynitirde layer with silicon-rich, oxygen lean oxynitirde layer to enhance life span of the semiconductor device (e.g. Abstract).

Re claim 30, Bhattacharyya discloses a method according to claim 29, wherein the increased retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between

program and erase voltages to at least about 20 years (e.g. the first/second and substrate disclosed above being capable of and see also Bhattacharyya; abstract).

Re claim 36, 43, Bhattacharyya discloses a method according to claim 29, wherein a thicknesses of the second oxynitride layer is from 1 to 5 times greater than that of the first oxynitride layer (e.g. Bhattacharyya; Fig. 1A).

Claims 31-34, 38-41, 44-45, 49, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya and Akwani et al (US 2002/0154878, hereinafter Akwani).

Re claim 31, Bhattacharyya discloses a method according to claim 29.

Bhattacharyya does not explicitly disclose wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 41) using a process gas (e.g. Akwani; Para 43) comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in

concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya’s disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Re claim 32 and 39, Bhattacharyya/Akwani discloses a method according to claim 31, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/NH3 and SiH2C12/NH3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 33, Bhattacharyya discloses a method according to claim 29.

Bhattacharyya does not explicitly disclose wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide

(N20)/ND3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas (e.g. Akwani; Para 0041/0043) comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture (e.g. Akwani; Para 0041/0043) at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya’s disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve optimum and cost effective deposition method.

Re claim 34, Bhattacharyya/Akwani discloses a method according to claim 33, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing

the ratio of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Re claim 38, Bhattacharyya discloses a method according to claim 37.

Bhattacharyya does not expliclity disclose wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 0041/0043) using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the

prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve optimum and cost effective deposition method.

Re claim 40, Bhattacharyya discloses a method according to claim 37.

Bhattacharyya does not explicitly disclose the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed (e.g. just as first layer is formed) in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1 (e.g. Akwani; Para 0041/0043), and wherein the second oxynitride layer is formed (e.g. just as first layer is formed) in a CVD process (e.g. Akwani; Para 0041/0043) using a process gas (e.g. Akwani; Para 0043) comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such

concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya’s disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve optimum and cost effective deposition method.

Re claim 41, Bhattacharyya/Akwani discloses a method according to claim 40, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. CVD is being capable of) in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio (e.g. as addressed below) of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Re claim 44, Bhattacharyya discloses a method of forming a semiconductor device (e.g. 100 of Fig.1A) comprising: forming a multi-layer charge storing layer (e.g. 112/114/116/117 and 118 of Fig. 1A), depositing on a substrate (e.g. p-Si substrate) an oxygen-rich, first oxynitride layer (e.g. 112 of Fig. 1A & Claim 3) and depositing directly

(e.g. 112 is directly on 114) on the first oxynitride layer an oxygen-lean (e.g. 114 of Fig.1A & Claim 8) second oxynitride layer sequentially (e.g. are shown to deposited one after another of Fig.1A). a high concentration of oxygen selected to increase retention (e.g. …good charge retention….See abstract) performance of the multi-layer charge storing layer by acting as a barrier (e.g. charge trapping for instance) between charge trapped in the second oxynitride layer and the substrate (e.g. device of Fig.1A being capable of).

Bhattacharyya does not explicitly discloses the second oxynitride layer to be silicon-rich, oxygen layer in a single disclosed embodiment as above and depositing the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20 (oxidizer)/ND3(nitrogen source) and SiH2Cl2 (silicon precursor)/ ND3 mixtures. wherein a difference in stoichiometric composition of the first oxynitride layer and the second oxynitride layer is selected to increase a difference between programming and erase voltages, thereby increasing data retention, improving speed of the semiconductor device and increase an end-of-life (EOL) for the semiconductor device.

However, Bhattacharyya do disclose that second oxynitride layer to be made by silicon-rich nitride and nitride layer can be a substitute with oxynitride layer (e.g. Claim 28, Para 0061). wherein a difference in stoichiometric composition of the first oxynitride layer and the second oxynitride layer is selected to increase a difference between programming and erase voltages, thereby increasing data retention, improving speed of the semiconductor device and increase an end-of-life (EOL) for the semiconductor

device (e.g. process is disclosed by Bhattacharayya and benefit of such process is expected and therefore not patentable).

Therefore, it would have been obvious to one an ordinary skilled in the art at the time of invention to modify Bhattacharyya disclosed invention and form stacked oxynitirde layer with silicon-rich, oxygen lean oxynitirde layer to enhance life span of the semiconductor device (e.g. Abstract).

Bhattacharyya does not explicitly discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20 (oxidizer)/ND3(nitrogen source) and SiH2Cl2 (silicon precursor)/ ND3 mixtures.

In an analogous art, Akwani discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. same material of first and second oxynitride and can be formed in the same tool & see also Para 47) in a single (e.g. CVD being capable of) CVD tool (e.g. Para 0041) using N20 [oxidizer]/ND3 [nitrogen source] and SiH2Cl2 [silicon precursor]/ ND3[nitrogen source] mixtures (e.g Para 0043). Akwani has clearly disclosed above gaseous mixtures used in formation of oxynitride layer and “It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art.” In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960) and Ex parte Quadranti,

25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992). Further, changing ratios or concentration of above gaseous mixtures not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Re claim 45, Bhattacharyya/Akwani discloses a method according to claim 44, wherein the first ratio (e.g. Akwani; Para 0041/0043 in view of below determination) of the N20/ND3 and SiH2C12/ND3 mixtures is about 8:1, and wherein the second ratio of the N20/ND3 and SiH2C12/ ND3 mixtures is about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 49, Bhattacharyya/Akwani discloses a method according to claim 44, wherein a thicknesses of the second oxynitride layer is from 1 to 5 times greater than that of the first oxynitride layer (e.g. Bhattacharyya; Fig. 1A).

With respect to claim 52, Bhattacharyya/Akwani discloses a method according to claim 44, wherein depositing on the first oxynitride layer an oxygen-lean second oxynitride layer comprises depositing the oxygen-lean second oxynitride layer directly on the first oxynitride layer (i.e. Bhattacharyya; 112 is also directly on 114 as shown in Fig.1A in view of Para 0078).

Claims 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, further in view of Kitakado et al (US 6461899, hereinafter Kitakado).

With respect to claim 53, Bhattacharyya discloses a method according to claim 29..

Bhattacharyya does not expliclity disclose depositing the second oxynitride layer comprises steam annealing the second oxynitride layer to reduce a number of traps formed near a top surface thereof.

In an analogous art, Kitakado disclose annealing a oxynitride layer (e.g. Col 7, lines 35 – 65).

Therefore, it would have been obvious to one an ordinary skilled the art at the time of invention to modify Bhattacharyys disclosed invention and form second oxynitirde layer using steam annealing to control densities. as taught by Kitado (e.g. Col 7, lines 35-65).

With respect to claim 54. Bhattacharyya/Kitakado discloses a method according to claim 53, further comprising forming a blocking oxide layer directly on the second oxynitride layer (e.g. Bhattacharyya; 116).

With respect to claim 55, Bhattacharyya/Kitakado discloses a method according to claim 54, wherein forming the blocking oxide layer comprises steam annealing the blocking oxide layer (e.g. Col 2, lines 53 – 58) to reduce back streaming of charge carriers through the blocking oxide layer.

Response to Arguments

Applicant's arguments filed 11/29/2012 have been fully considered but they are not persuasive. Applicant argues as follows:

> Applicants submit that Bhattacharyya discloses neither depositing an oxygen-lean second oxynitride layer directly on an oxygen-rich, first oxynitride layer, nor that the second oxynitride layer, in addition to being oxygen-lean is silicon-rich.

Examiner respectfully disagrees and submits the following:

Bhattacharyya has shown in claim 28, Para0061 that trapping layer can be made with silicon-rich nitride and nitride layer can be a substitute of oxynitride layer with oxygen content to be inherently lean when silicon is rich.

Therefore, rejection of the claims above is maintained.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 1-571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/
/JULIO J. MALDONADO/
Supervisory Patent Examiner, Art Unit 2898

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EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/811,958	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29 - 49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29 - 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29 – 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya) and Akwani et al (US 2002/0154878, hereinafter Akwani).

Re claim 29, 37, and 44, Bhattacharyya discloses a method of forming a semiconductor device (e.g. 100 of Fig.1A) including a multi-layer charge storing layer (e.g. 112/114/116/117 and 118 of Fig. 1A) comprising: depositing on a substrate (e.g. p-Si substrate) an oxygen-rich, first oxynitride layer (e.g. 112 of Fig. 1A & Claim 3) and depositing on the first oxynitride layer an oxygen-lean (e.g. 114 of Fig.1A & Claim 8) second oxynitride layer sequentially (e.g. are shown to deposited one after another of Fig.1A). [Distinct Claim 29 limitation STARTS here] a high concentration of oxygen selected to increase retention (e.g. …good charge retention….See abstract) performance of the multi-layer charge storing layer by acting as a barrier (e.g. charge trapping for instance) between charge trapped in the second oxynitride layer and the substrate (e.g. device of Fig.1A being capable of). [Distinct claim 37 limitation STARTS here] wherein a difference in concentration of oxygen between the first oxynitride layer and the second oxynitride layer is selected to increase an end-of-life (EOL) (e.g. See

abstract, ...device of 1A to enhance life span) for the semiconductor device at a specified difference (e.g. abstract, direct tunneling program and erase) between program and erase voltages to at least about 20 years [Distinct claim 37 limitation ENDS here].

Bhattacharyya does not explicitly discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20 (oxidizer)/ND3(nitrogen source) and SiH2Cl2 (silicon precursor)/ ND3 mixtures.

In an analogous art, Akwani discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. same material of first and second oxynitride and can be formed in the same tool & see also Para 47) in a single (e.g. CVD being capable of) CVD tool (e.g. Para 0041) using N20 [oxidizer]/ND3 [nitrogen source] and SiH2Cl2 [silicon precursor]/ ND3[nitrogen source] mixtures (e.g Para 0043). Akwani has clearly disclosed above gaseous mixtures used in formation of oxynitride layer and “It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art.” In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960) and Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992). Further, changing ratios or concentration of above gaseous mixtures not support the patentability of subject matter

encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya’s disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Re claim 30, Bhattacharyya/Akwani discloses a method according to claim 29, wherein the increased retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years (e.g. the first/second and substrate disclosed above being capable of and see also Bhattacharyya; abstract).

Re claim 31, Bhattacharyya/Akwani discloses a method according to claim 29, wherein the wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 41) using a process gas (e.g. Akwani; Para 43) comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical.

"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 32 and 39, Bhattacharyya/Akwani discloses a method according to claim 31, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/NH3 and SiH2C12/NH3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 33, Bhattacharyya/Akwani discloses a method according to claim 29, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas (e.g. Akwani; Para 0041/0043) comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture (e.g. Akwani; Para 0041/0043) at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the

prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 34, Bhattacharyya/Akwani discloses a method according to claim 33, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 35, 42 and 48, Bhattacharyya/Akwani discloses a method according to claim 29, wherein at least one of the first oxynitride layer and the second oxynitride layer is formed at temperature of at least about 780 ℃ (e.g. Akwani; oxidizing and CVD deposition shown and has to have a temperature). Further, differences in temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 36, 43, and 49, Bhattacharyya/Akwani discloses a method according to claim 29, wherein a thicknesses of the second oxynitride layer is from 1 to 5 times greater than that of the first oxynitride layer (e.g. Bhattacharyya; Fig. 1A).

Re claim 38, Bhattacharyya/Akwani discloses a A method according to claim 37, wherein the wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 0041/0043) using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 40, Bhattacharyya/Akwani discloses a method according to claim 37, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1 (e.g. Akwani; Para 0041/0043), and wherein the second oxynitride layer is formed (e.g. just as first layer is formed) in a CVD process (e.g. Akwani; Para 0041/0043) using a process gas (e.g. Akwani; Para 0043) comprising a N20/ND3mixture and a

SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 41, Bhattacharyya/Akwani discloses a method according to claim 40, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. CVD is being capable of) in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio (e.g. as addressed below) of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 45, Bhattacharyya/Akwani discloses a method according to claim 44, wherein the first ratio (e.g. Akwani; Para 0041/0043 in view of below determination) of the N20/ND3 and SiH2C12/ND3 mixtures is about 8:1, and wherein the second ratio of the N20/ND3 and SiH2C12/ ND3 mixtures is about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter

encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 46, Bhattacharyya/Akwani discloses a method according to claim 44, wherein a stoichiometric composition of the first oxynitride layer (e.g Bhattacharyya; Abstract) comprises a high concentration of oxygen (e.g. Bhattacharyya; first layer is indeed oxygen rich) selected to increase retention performance (e.g. Bhattacharyya; being capable of) of the multi-layer charge storing layer by acting as a barrier (Bhattaharyya is again being capable of) between charge trapped in the second oxynitride layer and the substrate.

Re claim 47, Bhattacharyya/Akwani discloses a method according to claim 46, wherein the increased retention performance of the multi-layer charge storing layer increases (e.g. Bhattacharyya; Abstract…increased life span) an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages (e.g. Bhattacharyya; Abstract; enhanced program and erase function) to at least about 20 years (e.g. Bhattacharyya; disclosed prior art being capable of).

Response to Arguments

Applicant's arguments filed 01/04/2011 have been fully considered but they are not persuasive. Applicant argues as follows:

> Applicants disagree and note that the structure shown in FIG. 1A of Bhattacharyya (reproduced below for convenience), shows not a "semiconductor device including a multi-layer charge storing layer" comprising both first and second oxynitride layers, but rather an oxide-nitride-oxide device having a single, conventional nitride charge trapping layer.

Examiner respectfully disagrees for at least the following reason(s).

Preamble of the claim(s) recites "a semiconductor device that includes a multi-layer charge storing layer comprising:" and it is the semiconductor device that is describing the structure and not the multi-charge storing layer. Therefore, collectively, structure of figure 1A can be called a multi-layer charge storing layer as device of figure 1A is indeed capable of storing a charge (e.g. See Para 0051).

Therefore, rejection of the independent claims is maintained.

Applicant further argues as follows:

> includes first *and* second oxynitride layers. Moreover, there is no teaching or suggestion the SiON trapping layer 114 in Bhattacharyya is *oxygen-rich*, as is the first oxynitride layer in the claimed invention, or *oxygen-lean* as is the second oxynitride layer.

Examiner respectfully disagrees for at least the following reason(s).

Please see tunnel insulating layer 112 as addressed in claim 1 above and referred to Bhattacharyya claim 3 that layer 112 can be made oxygen rich SiON among many other options.

Therefore, rejection of the independent claims is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday - Thursday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 1-571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894

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EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2898	

MAIL DATE	DELIVERY MODE
09/24/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	13/007,533	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2898	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2012*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) _____ is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *28-33* is/are allowed.

7)☒ Claim(s) *1-10,24-27* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 & 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya).

With respect to claim 1, Bhattacharyya discloses a silicon-oxide-oxynitride-oxide-silicon structure (e.g. SONOS – Fig.1A) comprising: a tunnel oxide layer (e.g. First layer of 112 & Para 0073) on a surface of a substrate (e.g. on top of P-Si Substrate) comprising silicon (e.g. P-“Si”); a multi-layer charge storing layer (e.g. 112/114/116/117) including an oxygen-rich, first oxynitride layer (e.g See K2-K3 of 112 & claim 3) on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free (e.g. oxygen-rich stoichiometric composition – inherently capable of), and an oxygen-lean, second oxynitride layer (e.g. 114 - Para 0074, showing layer to be nitrogen-rich SiON, making it oxygen lean) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense (e.g. as displayed - is indeed trapping layer); a blocking

oxide layer (e.g. 116) on the second oxynitride layer; and a silicon containing gate layer (e.g. 118) on the blocking oxide layer.

With respect to claim 6. Bhattacharyya discloses a semiconductor device (e.g. Fig.1A), comprising: substrate comprising silicon (e.g. P-Si) and having a surface (e.g. top surface of P-Si) with laterally spaced-apart source and drain regions (e.g. 104/106); a tunnel oxide layer (e.g. K1 of 112) on the surface of the substrate overlying the source and drain regions (e.g. K1 is indeed shown to overlap the 104/106); a multi-layer charge storing layer (e.g. 112/114/116/117) on the tunnel oxide layer and disposed laterally between (e.g. 112 is indeed between the source and drain) the spaced-apart source and drain regions, the multi-layer charge storing layer including an oxygen-rich first oxynitride layer (e.g. can be K2 – K3 of 112 and Claim 3) in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free (e.g. oxygen-rich stoichiometric composition – inherently capable of), and an oxygen-lean second oxynitride layer (e.g. 114 - Para 0074, showing layer to be nitrogen-rich SiON, making it oxygen lean) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense (e.g. as displayed – is indeed trapping layer); a blocking oxide layer (e.g. 116) on the second oxynitride layer; and a silicon containing gate layer (e.g. 118) on the blocking oxide layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 – 4, 7 - 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya.

With respect to claim 2 & 3, Bhattacharyya discloses the semiconductor device of claim 1, wherein a concentration of oxygen in the first oxynitride layer is about 15 to about 40%, and a wherein a concentration of oxygen in the second oxynitride layer is less than about 5%.

Bhattacharyya has disclosed claimed invention of claim1 except exact ranges of oxygen concentration in oxynitride layers. Applicant discloses multiple ranges of oxygen concentration in first and second oxynitride layers (e.g. see Para 044, 0045 and as originally filed claim 2) and has shown no criticality to varying changes concentration of oxygen that will make device inoperable. However, Bhattacharyya discloses that oxygen concentration can range to about 20% (e.g. Para 0067).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum oxygen concentration to increase charge retention device, as taught by Bhattacharyya (Abstract).

With respect to claim 4. Bhattacharyya discloses the structure of claim 1, wherein the second oxynitride layer comprises a charge trap density at least 1000 times greater than the first oxynitride layer.

Bhattacharyya has disclosed claimed invention of claim1 except the explicit disclosure of optimum thickness of both first and second oxynitride layers. However, in view of applicant specification (e.g. Para 0028), there is range specified of 7nm – 15 nm or it can be about 10 nm for first and second oxynitride layers. Bhattacharyya clearly disclose the range of both first and second oxynitiride layers to be about 10nm (e.g. Para 0071). Further, applicant has not shown any criticality to claimed thickness that will make the device inoperable. Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum thicknesses to increase charge retention, as taught by Bhattacharyya (Abstract).

With respect to claim 7 & 8, Bhattacharyya discloses the semiconductor device of claim 6, wherein a concentration of oxygen in the first oxynitride layer is about 15 to about 40%, and a wherein a concentration of oxygen in the second oxynitride layer is less than about 5%.

Bhattacharyya has disclosed claimed invention of claim1 except exact ranges of oxygen concentration in oxynitride layers. Applicant has discloses multiple ranges of oxygen concentration in first and second oxynitride layers (e.g. see Para 044, 0045 and as originally filed claim 2) and has shown no criticality to varying changes concentration of oxygen that will make device inoperable. However, Bhattacharyya discloses that oxygen concentration can range to about 20% (e.g. Para 0067).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum

oxygen concentration to increase charge retention device, as taught by Bhattacharyya (Abstract).

With respect to claim 9. Bhattacharyya discloses the structure of claim 6, wherein the second oxynitride layer comprises a charge trap density at least 1000 times greater than the first oxynitride layer.

Bhattacharyya has disclosed claimed invention of claim1 except the explicit disclosure of optimum thickness of both first and second oxynitride layers. However, in view of applicant specification (e.g. Para 0028), there is range specified of 7nm – 15 nm or it can be about 10 nm for first and second oxynitride layers. Bhattacharyya clearly disclose the range of both first and second oxynitiride layers to be about 10nm (e.g. Para 0071). Further, applicant has not shown any criticality to claimed thickness that will make the device inoperable. Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum thicknesses to increase charge retention device, as taught by Bhattacharyya (Abstract).

Claims 5 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, further in view of Thomas (US 2007/0121380, hereinafter Thomas).

With respect to claim 5 & 10. Bhattacharyya discloses the structure of claim 1 and 6 respectively.

Bhattacharyya does not explicitly disclose the second oxynitride layer further comprises a concentration of carbon selected to increase a number of traps therein.

In an analogous art, Thomas discloses a carbon particles that can be injected into insulating layer (e.g. Para 0017).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya disclosed invention and inject carbon concentration to prevent an increase in leakage current and improve charge retention (e.g. Para 0017).

Claim 24 & 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, further in view of Ramsbey et al (US 6433383, hereinafter Ramsbey).

With respect to claim 24 & 26, Bhattacharyya discloses the structure of claim 1.

Bhattacharyya does not explicitly disclose the first oxynitride layer comprises a homogeneous composition.

In an analogous art, Ramsbey discloses where oxygen rich oxynitride layer can be formed with uniform composition (Col, 7, lines 10 – 15).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharayya's disclosed invention and form oxynitride layer with uniform composition to optomize date retention capability of a memory cell (Col 6, lines 25 -30).

Claim 25 & 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, further in view of Hori et al (hereinafter Hori 20050236679).

With respect to claim 25 & 27, Bhattacharyya discloses the structure of claim 5.

Bhattacharayya does not explicitly disclose wherein the second oxynitride layer comprises a concentration of carbon of from about 5% to about 15%.

In an analogous art, Hori disclose forming a oxynitride layer with carbon (e.g. Para 0046) but does not explicitly discloses specific range as claimed. However, in order to give patentable weight applicant has to disclose clearly as to why claimed ranges are critical to the invention and may make the claimed invention inoperable.

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya disclosed invention and form oxynitride layer with carbon content induced to improve current leakage characteristics of the Sion (Hori; Para 0046).

Allowable Subject Matter

Claim 28 is allowed.

Claims 29 – 33

The following is a statement of reasons for the indication of allowable subject matter: Prior art of record does not explicitly disclose or render obvious “a second charge storing layer directly on the first charge storing layer comprising an oxygen-lean, silicon-rich and nitrogen-rich oxynitride in which a stoichiometric composition of the

oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer results in it being trap dense" in combination of all other limitation of claim 28.

.

Response to Arguments

Applicant's arguments filed 06/12/2012 have been fully considered but they are not persuasive. Regarding claim 1 and 6, applicant argues as follows:

> In particular, applicants note that Bhattacharyya discloses at some length two separate and distinct layers, K2 and K3, having differing compositions and different K values not a singular oxygen-rich, first oxynitride layer. (see e.g. paragraphs [0075], [0056] and band diagram of FIG. 1B.) Applicants further note that in the only embodiment described in Bhattacharyya wherein the tunneling layer includes an oxygen-rich oxynitride layer, it is described as the

Examiner respectfully disagrees and submits the following:

Applicant's claim language does not restrict examiner to interpret tunneling layer to have ONLY a single layer. Moreover, examiner recognize that claims are to be read in light of specification, however, specification limitations cannot be brought into the claims.

> Moreover, Applicants submit that modifying the teaching of Bhattacharyya to make the top most tunneling layer, K3, an oxygen-rich oxynitride layer would render the device of Bhattacharyya inoperative because the tunneling layers would no longer have increasing K

Claim 1 & 6 are rejected under 102, therefore, arguments regarding modification of Bhattacharyya invention are irrelvent and are moot.

> If the examiner is asserting that K2 taken alone can be the oxygen-rich, first oxynitride layer, applicants note that both claim 1 and claim 6 as amended state that the "second oxynitride layer" is "on the first oxynitride layer," not merely over the first oxynitride layer, and thus Bhattacharyya does not disclose "*each and every element* of the claimed invention, *arranged as in the claim*."

Claim 1 is not amended and therefore, response is moot. Claim 6 has been amended and therefore addressed below.

Examiner has re-visited the specification and in the disclosure the term 'on' does not specify that there is a direct contact with no intervening layers or intervening layers are present as shown below.

> [0021] Reference in the description to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. The appearances of the phrase "in one embodiment" in various places in the specification do not necessarily all refer to the same embodiment. The term "to couple" as used herein may include both to directly connect and to indirectly connect through one or more intervening components.

Therefore, broad meaning to the term ‘on’ has been given in claim interpreation and rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 1-571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JULIO J. MALDONADO/

Supervisory Patent Examiner, Art Unit 2898

/MC/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

60909 7590 05/27/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
05/27/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 001245

Office Action Summary	Application No. 13/436,872	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/27/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1 - 13 & 21* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *9-13* is/are allowed.

7)☒ Claim(s) *1 - 8 & 21* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1 rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 as amended “an annealed blocking oxide layer on the second oxynitride layer, the annealed blocking oxide layer comprising a top surface in which a number of traps has been reduced by steam annealing” does not have support in the specification. Please clarify.

Claims 2 – 8 and 21 are rejected by virtue of dependency on claim 1.

In view of above rejection, Double patenting and art rejection is maintained.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim Claims 1,6 and 8 of Polishchuk et al U.S. Patent No. 8,860,122 (hereinafter '122). Although the claims at issue is not identical, they are not patentably distinct from each other because.

With respect to claim 1. '122 discloses a memory device (Claim 1,6 and 8) comprising: a channel (channel) formed from a semiconducting material overlying a surface on a substrate connecting a source (source) and a drain (drain) of the memory device; a tunnel oxide layer (tunnel dielectric) overlying the channel; and a multi-layer charge storing layer (charge trapping layer) including an oxygen-rich, first oxynitride layer (oxygen-rich oxynitride layer) on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free (functionality in product claims), and an oxygen-lean, second oxynitride layer (oxygen-rich oxynitirde and obviously oxygen lean) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 of U.S. Patent No. (8,222,688, hereinafter '688), in view of Bhattacharyya (2006/0261401, hereinafter '401).

With respect to claim 1. A multi-layer charge storing layer (First and Second) including an oxygen-rich, first oxynitride layer (first nitride oxygen-rich layer) on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean, second oxynitride layer (second nitride/oxynitride layer - oxygen lean relative to oxygen rich) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense.

Bhattacharyya does not discloses a memory device comprising: a channel formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide layer overlying the channel.

In an analogous art, ***a*** memory device comprising: a channel (claim 1 – channel) formed from a semiconducting material overlying a surface on a substrate connecting a source (source) and a drain (drain) of the memory device; a tunnel oxide layer (tunnel insulator) overlying the channel.

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify '688's invention and form gate/source/drain to form charge retaining device.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 & 13 of U.S. Patent No (8,643,124, hereinafter '124).

With respect to claim 1. '124 discloses a memory device (Claims 1,and 13) comprising: a channel (channel) formed from a semiconductor material overlying a surface on a substrate connecting a source (source) and a drain (drain) of the memory device; a tunnel oxide layer (tunnel oxide) overlying the channel; and a multi-layer charge storing layer (charge storing layer) including an oxygen-rich, first oxynitride layer (first charge storing oxygen-rich oxynitride layer) on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free (functionality in product claims), and an oxygen-lean, second oxynitride layer (second oxygen-rich oxynitirde and obviously oxygen lean) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 & 21 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya).

With respect to claim 1, Bhattacharyya discloses a memory device (Fig. 1A) comprising: a channel (108) formed from a semiconducting material (Si-Substrate) overlying a surface (Top surface) on a substrate (102) connecting a source (104) and a drain (106) of the memory device; a tunnel oxide layer (112) overlying the channel; and a multi-layer charge storing layer (Combined – 114/116/117/118) including an oxygen-rich, first oxynitride layer (114) on the tunnel oxide layer, and an oxygen-lean, second oxynitride layer (116 – Para 0068) on the first oxynitride layer.

Bhattacharyya does not explicitly disclose that first oxynitride layer to function as a trap free and second oxynitride layer to function as trap dense. However, While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber,* 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997), Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to recite Bhattacharyya disclosed invention functionality while no distinct structural feature is being claimed.

With respect to claim 21. Bhattacharyya discloses the memory device of claim 1, the second oxynitride layer comprises a top surface in which a number of traps has been reduced by the steam annealing of the annealed blocking oxide layer (Bhattacharyya and claim directed to product is be distinguished over prior art by structure).

Claim 2 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Morii (US 5,847,411, hereinafter Morii).

With respect to claim 2, Bhattacharyya the memory device of claim 1.

Bhattacharyya does not disclose wherein the channel comprises polysilicon.

In an analogous art, Morii disclose a channel that comprises polysilicon.

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form channel that comprises polysilicon to improve mobility of a carrier in the channel.

Claim 3 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Pfiester et al(US 5,348,903, hereinafter Pfiester).

With respect to claim 3, Bhattacharyya discloses the memory device of claim 1.

Bhattacharyya does not disclose the channel comprises recrystallized polysilicon.

In an analogous art, Pfiester discloses a channel that can formed of polysilicon and recrystallized (col 5, line 29 – 40).

Therefore, it would have been obvious to one of an ordinary skilled in the art a the time of invention to modify Bhattacharyya's disclosed invention and form channel with recrystallized polysilicon to obtain a low channel electrical resistance (Col 5, lines 30 – 45).

Claim 4 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Duan et al (US 2005/0079659, hereinafter Duan).

With respect to claim 4, Bhattacharyya the memory device of claim 1.

Bhattacharyya does not disclose the channel comprises a silicon nanowire.

In an analogous art, Duan discloses a channel comprising silicon nanowire (Para 0159).

Therefore, it would have been obvious to one an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form channel with nanowires to enhance mobility (Para 0159).

Claim 5 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Chen et al (US 2005/0275010, hereinafter Chen).

With respect to claim 5, Bhattacharyya the memory device of claim 1, the gate comprises the tunnel oxide layer and the multi-layer charge storing layer.

Bhattacharyya does not disclose a non-planar transistor including a gate having multiple surfaces abutting the channel.

In an analogous art, Chen discloses a non-planar transistor including a gate having multiple surfaces abutting the channel (Figure 7g).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's invention and form gate in non-planar form to mitigate short channel affect (Para 0003).

With respect to claim 6, Bhattacharyya/Chen discloses the memory device of claim 5, wherein the gate further comprises a blocking dielectric (Para 0069) overlying the multi-layer charge storing layer, and a metal gate layer (Bhattacharyya; Para 0070) overlying the blocking dielectric layer.

With respect to claim 7, Bhattacharyya/Chen the memory device of claim 6, wherein the blocking dielectric comprises a high K dielectric (Bhattacharyya; Para0047).

Claim 8 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Lee et al (US 2003/0030100, hereinafter Lee).

With respect to claim 8, Bhattacharyya discloses the memory device of claim 1.

Bhattacharyya does not disclose wherein the second oxynitride layer further comprises a concentration of carbon selected to increase a number of traps therein.

In an analogous art, Lee disclose increasing concentration of carbon into the oxynitride layer (Para 0034).

Thereofore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form carbon into oxynitride layer to achieve narrow band than silicon oxynitride (Para 0034).

Allowable Subject Matter

Claim 9 is allowed.

Claims 10 – 13 are allowed by virtue of dependency on claim 9.

Response to Arguments

Applicant's response is moot regarding Priority of the claims as indicated in Non-Final office action mailed on 12/19/2014, therefore, Claims 4 – 5 and 9 – 11 get the priority date of 03/31/2012.

Applicant's arguments filed 01/27/2015 have been fully considered but they are not persuasive. Applicant argues as follows:

Applicant arguments are directed to amended claim 1 and therefore addressed in view of above 112 rejection and 103 rejection above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 1-571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/811,958	06/13/2007	Sagy Levy	PM07002	9184

60909 7590 12/07/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
12/07/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/811,958	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *29-34,36-41,43-47 and 49-52* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *29-34,36-41,43-47 and 49-52* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/15/2011 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29 – 34 and 36 – 41, 43 – 47 & 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya) and Akwani et al (US 2002/0154878, hereinafter Akwani).

Re claim 29, 37, and 44, Bhattacharyya discloses a method of forming a semiconductor device (e.g. 100 of Fig.1A) comprising: forming a multi-layer charge storing layer (e.g. 112/114/116/117 and 118 of Fig. 1A), depositing on a substrate (e.g. p-Si substrate) an oxygen-rich, first oxynitride layer (e.g. 112 of Fig. 1A & Claim 3) and depositing on the first oxynitride layer an oxygen-lean (e.g. 114 of Fig.1A & Claim 8)

second oxynitride layer sequentially (e.g. are shown to deposited one after another of Fig.1A). [Distinct Claim 29 limitation STARTS here] a high concentration of oxygen selected to increase retention (e.g. …good charge retention….See abstract) performance of the multi-layer charge storing layer by acting as a barrier (e.g. charge trapping for instance) between charge trapped in the second oxynitride layer and the substrate (e.g. device of Fig.1A being capable of). [Distinct claim 37 limitation STARTS here] wherein a difference in concentration of oxygen between the first oxynitride layer and the second oxynitride layer is selected to increase an end-of-life (EOL) (e.g. See abstract, ...device of 1A to enhance life span) for the semiconductor device at a specified difference (e.g. abstract, direct tunneling program and erase) between program and erase voltages to at least about 20 years [Distinct claim 37 limitation ENDS here].

Bhattacharyya does not explicitly discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20 (oxidizer)/ND3(nitrogen source) and SiH2Cl2 (silicon precursor)/ ND3 mixtures.

In an analogous art, Akwani discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. same material of first and second oxynitride and can be formed in the same tool & see also Para 47) in a single (e.g. CVD being capable of) CVD tool (e.g. Para 0041) using N20 [oxidizer]/ND3 [nitrogen source] and SiH2Cl2 [silicon precursor]/ ND3[nitrogen source] mixtures (e.g Para 0043). Akwani has clearly disclosed above gaseous mixtures used in formation of

oxynitride layer and “It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art.” In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960) and Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992). Further, changing ratios or concentration of above gaseous mixtures not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya’s disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Re claim 30, Bhattacharyya/Akwani discloses a method according to claim 29, wherein the increased retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years (e.g. the first/second and substrate disclosed above being capable of and see also Bhattacharyya; abstract).

Re claim 31, Bhattacharyya/Akwani discloses a method according to claim 29, wherein the wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 41) using a process gas (e.g. Akwani; Para 43) comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 32 and 39, Bhattacharyya/Akwani discloses a method according to claim 31, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/NH3 and SiH2C12/NH3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 33, Bhattacharyya/Akwani discloses a method according to claim 29, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas (e.g. Akwani; Para 0041/0043) comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture (e.g. Akwani; Para 0041/0043) at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 34, Bhattacharyya/Akwani discloses a method according to claim 33, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 36, 43, and 49, Bhattacharyya/Akwani discloses a method according to claim 29, wherein a thicknesses of the second oxynitride layer is from 1 to 5 times greater than that of the first oxynitride layer (e.g. Bhattacharyya; Fig. 1A).

Re claim 38, Bhattacharyya/Akwani discloses a A method according to claim 37, wherein the wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 0041/0043) using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 40, Bhattacharyya/Akwani discloses a method according to claim 37, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1 (e.g. Akwani; Para 0041/0043), and wherein the second oxynitride layer is formed (e.g. just as first layer is formed) in a CVD process (e.g. Akwani; Para 0041/0043) using a process gas (e.g. Akwani; Para 0043) comprising a N20/ND3mixture and a

SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 41, Bhattacharyya/Akwani discloses a method according to claim 40, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. CVD is being capable of) in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio (e.g. as addressed below) of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 45, Bhattacharyya/Akwani discloses a method according to claim 44, wherein the first ratio (e.g. Akwani; Para 0041/0043 in view of below determination) of the N20/ND3 and SiH2C12/ND3 mixtures is about 8:1, and wherein the second ratio of the N20/ND3 and SiH2C12/ ND3 mixtures is about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or

temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 46, Bhattacharyya/Akwani discloses a method according to claim 44, wherein a stoichiometric composition of the first oxynitride layer (e.g Bhattacharyya; Abstract) comprises a high concentration of oxygen (e.g. Bhattacharyya; first layer is indeed oxygen rich) selected to increase retention performance (e.g. Bhattacharyya; being capable of) of the multi-layer charge storing layer by acting as a barrier (Bhattaharyya is again being capable of) between charge trapped in the second oxynitride layer and the substrate.

Re claim 47, Bhattacharyya/Akwani discloses a method according to claim 46, wherein the increased retention performance of the multi-layer charge storing layer increases (e.g. Bhattacharyya; Abstract…increased life span) an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages (e.g. Bhattacharyya; Abstract; enhanced program and erase function) to at least about 20 years (e.g. Bhattacharyya; disclosed prior art being capable of).

With respect to claim 50, A method according to claim 29, wherein depositing on the first oxynitride layer an oxygen-lean second oxynitride layer comprises depositing the oxygen-lean second oxynitride layer directly on the first oxynitride layer (i.e. Bhattacharyya; 112 is also directly on 114 as shown in Fig.1A in view of Para 0078).

With respect to claim 51, A method according to claim 37, wherein depositing on the first oxynitride layer an oxygen-lean second oxynitride layer comprises depositing

the oxygen-lean second oxynitride layer directly on the first oxynitride layer (i.e. Bhattacharyya; 112 is also directly on 114 as shown in Fig.1A in view of Para 0078).

With respect to claim 52, A method according to claim 44, wherein depositing on the first oxynitride layer an oxygen-lean second oxynitride layer comprises depositing the oxygen-lean second oxynitride layer directly on the first oxynitride layer (i.e. Bhattacharyya; 112 is also directly on 114 as shown in Fig.1A in view of Para 0078).

Response to Arguments

Applicant's arguments filed 06/15/2011 have been fully considered but they are not persuasive. Regarding claims 29, 37 and 44, applicant argues as follows:

> Applicant submits that the cited references, alone or in combination, do not teach or suggest all features of independent claims 29, 37 and 44.
>
> Claims 29, 37 and 44 as amended all include the feature of "forming a multi-layer charge storing layer."
>
> Applicants submit that Bhattacharyya does not teach or suggest forming a multi-layer charge storing layer, but to the contrary teaches a three layer tunneling layer 112 (labeled K1, K2 and K3 in FIG. 1A) overlaid by a *single* trapping layer 114.

Examiner respectfully disagree(s) for at least the following reason(s).

Applicant in the specification shows the multi-layer charge storing layer to generally include at least two oxynitride layers having differing composition as shown below.

> As noted above, the multi-layer charge storing layer generally includes at least two oxynitride layers having differing compositions of silicon, oxygen and nitrogen,
>
> 8 Cypress ref: PM2007002

Examiner has shown in the prior art first oxynitride layer 112 of Fig.1A and 114 of Fig.1A as second oxynitride layer. Hence, it clearly meets the claim language read in light of specification.

Therefore, rejection of claims 29, 37 and 44 are maintained.

Applicant further makes an argument regarding newly added claims 50- 52 as follows:

> Applicants note that the definition of "on" includes "a function word to indicate position in contact with and supported by the top surface of."[3] Applicants further note that every embodiment shown and described in the present application illustrates the oxygen-lean second oxynitride layer is formed "directly on" the first oxynitride layer, and that the applicants have not used the word "on" differently either in the application or in the prosecution history. Thus, applicants submit that one of ordinary skill in the art would understand, in light of the specification that "on" as claimed herein means "in contact with and supported by," and requests the examiner give this ordinary and accustomed meaning to the word "on" in examining the claims of the present application.

Examiner respectfully submits the following:

Bhattacharyya does disclose that insulators can alos be made of mix of layers of oxynitride as shown below.

> [0078] It is noted, as detailed above, that multiple insulators can be utilized in tunnel layers of embodiments of the present invention, including, but not limited to insulators from the oxide, mixed oxide, nitride, oxynitride, mixed oxynitride, and silicate families.

Hence, selecting a material from what is already known in the art does not make the invention patentably distinct.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday - Thursday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 1-571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894

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13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

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CYPRESS SEMICONDUCTOR CORPORATION
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SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2898	

MAIL DATE	DELIVERY MODE
04/12/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	13/007,533	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2898	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-10* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-10* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/14/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 11-23 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/12/2011.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 & 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya).

With respect to claim 1, Bhattacharyya discloses a silicon-oxide-oxynitride-oxide-silicon structure (e.g. SONOS – Fig.1A) comprising: a tunnel oxide layer (e.g. First layer of 112 & Para 0073) on a surface of a substrate (e.g. on top of P-Si Substrate) comprising silicon (e.g. P-"Si"); a multi-layer charge storing layer (e.g. 112/114/116/117) including an oxygen-rich, first oxynitride layer (e.g. can be K2 – K3 of 112 & claim 3) on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free (e.g. oxygen-rich stoichiometric

composition – inherently capable of), and an oxygen-lean, second oxynitride layer (e.g. 114 - Para 0074, showing layer to be nitrogen-rich SiON, making it oxygen lean) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense (e.g. as displayed - is indeed trapping layer); a blocking oxide layer (e.g. 116) on the second oxynitride layer; and a silicon containing gate layer (e.g. 118) on the blocking oxide layer.

With respect to claim 6. Bhattacharyya discloses a semiconductor device (e.g. Fig.1A), comprising: substrate comprising silicon (e.g. P-Si) and having a surface (e.g. top surface of P-Si) with laterally spaced-apart source and drain regions (e.g. 104/106); a tunnel oxide layer (e.g. K1 of 112) on the surface of the substrate overlying the source and drain regions (e.g. K1 is indeed shown to overlap the 104/106); a multi-layer charge storing layer (e.g. 112/114/116/117) on the tunnel oxide layer and disposed laterally between (e.g. 112 is indeed between the source and drain) the spaced-apart source and drain regions, the multi-layer charge storing layer including an oxygen-rich first oxynitride layer (e.g. can be K2 – K3 of 112 and Claim 3) in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free (e.g. oxygen-rich stoichiometric composition – inherently capable of), and an oxygen-lean second oxynitride layer (e.g. 114 - Para 0074, showing layer to be nitrogen-rich SiON, making it oxygen lean) in which a stoichiometric composition of the second oxynitride layer results in it being trap dense (e.g. as displayed – is indeed trapping layer); a blocking oxide layer (e.g. 116) on the second oxynitride layer; and a silicon containing gate layer (e.g. 118) on the blocking oxide layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 – 4, 7 - 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya.

With respect to claim 2 & 3, Bhattacharyya discloses the semiconductor device of claim 1, wherein a concentration of oxygen in the first oxynitride layer is about 15 to about 40%, and a wherein a concentration of oxygen in the second oxynitride layer is less than about 5%.

Bhattacharyya has disclosed claimed invention of claim1 except exact ranges of oxygen concentration in oxynitride layers. Applicant discloses multiple ranges of oxygen concentration in first and second oxynitride layers (e.g. see Para 044, 0045 and as originally filed claim 2) and has shown no criticality to varying changes concentration of oxygen that will make device inoperable. However, Bhattacharyya discloses that oxygen concentration can range to about 20% (e.g. Para 0067).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum oxygen concentration to increase charge retention device, as taught by Bhattacharyya (Abstract).

With respect to claim 4. Bhattacharyya discloses the structure of claim 1, wherein the second oxynitride layer comprises a charge trap density at least 1000 times greater than the first oxynitride layer.

Bhattacharyya has disclosed claimed invention of claim1 except the explicit disclosure of optimum thickness of both first and second oxynitride layers. However, in view of applicant specification (e.g. Para 0028), there is range specified of 7nm – 15 nm or it can be about 10 nm for first and second oxynitride layers. Bhattacharyya clearly disclose the range of both first and second oxynitiride layers to be about 10nm (e.g. Para 0071). Further, applicant has not shown any criticality to claimed thickness that will make the device inoperable. Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum thicknesses to increase charge retention, as taught by Bhattacharyya (Abstract).

With respect to claim 7 & 8, Bhattacharyya discloses the semiconductor device of claim 6, wherein a concentration of oxygen in the first oxynitride layer is about 15 to about 40%, and a wherein a concentration of oxygen in the second oxynitride layer is less than about 5%.

Bhattacharyya has disclosed claimed invention of claim1 except exact ranges of oxygen concentration in oxynitride layers. Applicant has discloses multiple ranges of oxygen concentration in first and second oxynitride layers (e.g. see Para 044, 0045 and as originally filed claim 2) and has shown no criticality to varying changes concentration

of oxygen that will make device inoperable. However, Bhattacharyya discloses that oxygen concentration can range to about 20% (e.g. Para 0067).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum oxygen concentration to increase charge retention device, as taught by Bhattacharyya (Abstract).

With respect to claim 9. Bhattacharyya discloses the structure of claim 6, wherein the second oxynitride layer comprises a charge trap density at least 1000 times greater than the first oxynitride layer.

Bhattacharyya has disclosed claimed invention of claim1 except the explicit disclosure of optimum thickness of both first and second oxynitride layers. However, in view of applicant specification (e.g. Para 0028), there is range specified of 7nm – 15 nm or it can be about 10 nm for first and second oxynitride layers. Bhattacharyya clearly disclose the range of both first and second oxynitiride layers to be about 10nm (e.g. Para 0071). Further, applicant has not shown any criticality to claimed thickness that will make the device inoperable. Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum thicknesses to increase charge retention device, as taught by Bhattacharyya (Abstract).

Claims 5 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, further in view of Thomas (US 2007/0121380, hereinafter Thomas).

With respect to claim 5 & 10. Bhattacharyya discloses the structure of claim 1 and 6 respectively.

Bhattacharyya does not explicitly disclose the second oxynitride layer further comprises a concentration of carbon selected to increase a number of traps therein.

In an analogous art, Thomas discloses a carbon particles that can be injected into insulating layer (e.g. Para 0017).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya disclosed invention and inject carbon concentration to prevent an increase in leakage current and improve charge retention (e.g. Para 0017).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 1-571-272-1864. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JULIO J. MALDONADO/
Supervisory Patent Examiner, Art Unit 2898

/MC/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/811,958	06/13/2007	Sagy Levy	PM2007002	9184

60909 7590 05/13/2009

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
4126	

MAIL DATE	DELIVERY MODE
05/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/811,958	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD MOHSIN CHOUDHRY	4126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/17/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

U.S. Patent and Trademark Office

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 14 recites the limitation "the multi-layer memory" & "the tunnel oxide layer" in claim. There is insufficient antecedent basis for this limitation in the claim.

Following rejections are made as best understood and interpreted by the examiner in view of above claim rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1– 8, 12, 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenne et al (US 6709928), hereinafter refereed as Jenne in view of Mine et al (US 2004/0183122), hereinafter refereed as Mine.

With respect to claim 1, Jenne discloses in a second embodiment a method of forming a charge storing layer (304-0 of Figure 3D) of a semiconductor device (Figure 4), the method

comprising steps of: depositing on a substrate (300 of Figure 3B) a silicon-rich nitride (Step 404 and 406 of Figure 4) and oxidizing (Col 6, Lines 42-43) the silicon-rich nitride layer.

Jenne's second embodiment fails to disclose explicitly a silicon-rich and oxygen-rich layer as oxynitride layer.

In an analogous art, Mine discloses that silicon oxide film, silicon oxynitride layer (1), Silicon oxynitride layer (2) (304a, 304b and 304c of Fig. 4, respectively) are laminated to form a capacitor insulator film the memory MOS transistor (Page 9, ¶131) where oxygen concentration must be higher in silicon oxynitride layer 1 when compared with silicon oxynitride layer 2 (Page 9, ¶131, Lines 10-12).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to combine Jenne's disclosed inventions and form a silicon rich, oxygen rich oxynitride layer that can be effective in reducing Gm degradation significantly (Page 10, ¶133).

With respect to claim 2, Jenne in view of Mine discloses a method according to claim 1, as above.

Jenne further disclose the step of forming over a surface of the first oxynitride layer at least one additional layer (304-1 of Figure 3D & Col 6, Lines 5-12) to form a multi-layer charge storing layer.

With respect to claim 3, Jenne in view of Mine discloses a method according to claim 2, as above. Jenne further discloses the step of forming at least a one additional layer comprises the step of forming a second oxynitride layer (304-1 of Figure 3D & Col 6, Line 9).

With respect to claim 4, Jenne in view of Mine discloses a method according to claim 3, as above.

Jenne discloses at least two oxynitride layers (304-0 (first) and 304-1(second) of Fig. 3D) having Silicon, Oxygen, Nitrogen and Hydrogen contents (Col 4, Line 33).

Jenne further discloses that oxynitride or silicon nitride ratios between silicon and nitrogen may differ from stochiometric ratios (Col 4, Lines 30-31). Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. Hence, it is obvious to one of an ordinary skilled in the art to have differing stochiometric compositions of oxygen, nitrogen and/or silicon to form multiple oxynitride layers to enhance programming characteristics (Col 2, Line 55).

With respect to claim 5, Jenne in view of Mine discloses a method according to claim 3, as above.

Jenne further has disclosed silicon-rich oxynitride layer, as in claim 1 above.

Jenne fails to disclose a step of forming the second oxynitride layer comprises the step of forming a second oxynitride layer under conditions selected to form a oxygen-lean oxynitride layer.

In an analogous art, Mine discloses a second oxynitride layer (304c of Fig.4 & Page 9, ¶131, Lines 11-12) to have less oxygen concentration as compared to first oxynitride layer (304b of Fig.4).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Jenne and for an oxynitride layer that is silicon-rich and oxygen-lean, as taught by Mine to suppress Gm degradation significantly(Page 10, ¶133, Lines 15-16).

With respect to claim 6, Jenne in view of Mine discloses a method according to claim 5, as above.

Jenne further discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) (Col 7, Line 18) process using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide ('N20)/NH3 mixture at (Col 7, Lines 12-15).

Jenne does not disclose *exact* ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. However, Jenne discloses that NH3 flow rate 2-4 times greater than dichlorosilane and also N2O flow rate is 1-3 times greater than dichlorosilane. (Col 7, Lines 17–24) Jenne further discloses that these flow rates can be switched from 3 -1 or 4 - 2 times during formation of oxynitride layers (Col 7, Lines 42-43). Generally, differences in concentration or flow rate will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or flow rate is critical to the invention.

It is obvious to one of an ordinary skilled in the art at the time of invention to optimize the flow rate with precursor gases disclosed in Jenne's invention and form oxynitride single or multiple layers to enhance programming characteristics as well as data retention in memory (Col 2, Lines 50-55).

With respect to claim 7, Jenne in view of Mine discloses a method according to claim 6, as above.

Jenne discloses the forming the first oxynitride layer and the second oxynitride layer (304-0 and 304-1 of Fig. 3D) in CVD tool (Col 7, Line 14) by changing the ratio of the N20/NH3 and SiH2C12/NH3 mixtures (limitations addressed in claim 6 above).

Jenne dose not explicitly states forming a first oxynitride layer and second oxynitride layers sequentially in a single CVD tool. However, it has to be obvious to one of an ordinary skilled in the art at the time of invention to form layer 304-0 first prior to forming second layer 304-1 as shown in figure 2E). Further, if a single layer of oxynitride can be formed in a CVD tool, second layer can be formed using the same tool to lower manufacturing cost or to use CVD multiple times.

With respect to claim 8, Jenne in view of Mine discloses a method according to claim 6, as above.

Jenne further discloses forming one of the first oxynitride layers and the second oxynitride layer at temperature of at least about 780 °C (Col 7, Line 24).

With respect to claim 12, Jenne discloses a method according to claim 11, as above.

Jenne further discloses a top oxynitride layer and a bottom oxynitride layer as being silicon-rich, as above.

Jenne fails to disclose the top oxynitride layer is formed under conditions selected to form oxygen-lean oxynitride layer, and the bottom oxynitride layer is formed under conditions selected to form a oxygen-rich oxynitride layer.

In an analogous art, Mine discloses a top oxynitride (304c of Fig.4) layer is formed under conditions selected to form oxygen-lean (Page 9, ¶131) oxynitride layer, and a bottom oxynitride layer (304b of Fig.4) is formed under conditions selected to form a oxygen-rich oxynitride layer.

If oxygen contents of top oxynitride are suggested to be lower than oxygen contents of the bottom oxynitride layer then, bottom oxynitride layer has to be oxygen rich as compare to top oxynitride layer as suggested by Mine (Page 9, ¶131).

It would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Jenne disclosed invention with oxygen-lean top oxynitride layer and oxygen-rich bottom oxynitride layer, as taught by Mine to achieve optimum lamination to form the insulator film (Page 9, ¶131, Lines 8 – 9).

With respect to claim 13, Jeene in view of Mine discloses a method according to claim 12.

Jenne fails to disclose the top oxynitride layer is nitrogen-rich oxynitride layer.

In an analogous art, Mine disclose forming an oxynitride layer that can be nitrogen-rich if oxygen contents are lowered (Page 6, ¶86). In claim 12, applicant claimed to form top oxynitride layer as being oxygen lean. Hence, top oxynitride layer has to be nitrogen-rich.

It would have been obvious to form an oxynitride layer containing lean oxygen and rich nitrogen contents, as taught by Mine to form a oxynitride layer using CVD with enhanced oxygen, nitrogen and silicon concentration (Col 6, ¶83).

With respect to claim 15, Jenne in view of Mine discloses a method according to claim 12.

Jenne discloses the forming top (304-0 of Fig 3D) and bottom oxynitride layers (304-1 of Fig. 3D) oxynitride layer is formed in a chemical vapor deposition (CVD) (Col 7, Line 18)

process using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide ('N20)/NH3 mixture at (Col 7, Lines 12-15).

Jenne does not disclose *exact* ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. However, Jenne discloses that NH3 flow rate 2-4 times greater than dichlorosilane and also N2O flow rate is 1-3 times greater than dichlorosilane. (Col 7, Lines 17–24) Jenne further discloses that these flow rates can be switched from 3 -1 or 4 - 2 times during formation of oxynitride layers (Col 7, Lines 42-43). Generally, differences in concentration or flow rate will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or flow rate is critical to the invention.

It would have been obvious to one of an ordinary skilled in the art at the time of invention to optimize the flow rate with precursor gases disclosed in Jenne's invention and form oxynitride single or multiple layers to enhance programming characteristics as well as data retention in memory (Col 2, Lines 50-55).

3. Claims 9 – 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenne et al (US 6709928), hereinafter refereed as Jenne.

With respect to claim 9, disclose a method comprising steps of." forming a first oxide layer of the (302 of Fig. 3D & Col 6, Line 27); forming a multi-layer (304-0 & 304-1 of Fig. 3D) charge storing layer comprising nitride on a surface of the first oxide layer; and forming a second

oxide layer (308 of Fig 3E) on a surface (308 is on 304-1 of Fig. 3E) of the multi-layer charge storing layer.

Jenne discloses a structure (Fig. 3E) with oxide-oxynitride-oxide where oxynitride can contains content of nitride capable of forming an oxide-nitride-oxide (ONO) structure.

With respect to claim 10, Jenne discloses a method according to claim 9, as above.

Jenne further discloses the multi-layer (304-0 and 304-1 of Fig.3D) charge storing layer comprises at least two silicon oxynitride (Si2N20) layers. Jenne again discloses that 304-0 and 304-1 layers are formed of silicon nitride (Col 6, Lines 27-28) and can be formed of silicon oxynitride (Col 4, Lines 31-33).

With respect to claim 11, Jenne discloses a method according to claim 10, as above.

Jenne discloses at least two oxynitride layers (304-0 and 304-1 of Fig. 3D) having Silicon, Oxygen, Nitrogen and Hydrogen contents (Col 4, Line 33).

Jenne further discloses that oxynitride or silicon nitride ratios between silicon and nitrogen may differ from stochiometric ratios (Col 4, Lines 30-31). Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. Hence, it is obvious to one of an ordinary skilled in the art to have differing stochiometric compositions of oxygen, nitrogen and/or silicon to form multiple oxynitride layers to enhance programming characteristics (Col 2, Line 55).

With respect to claim 16, Jenne discloses a method according to claim 10, as above.

Jenne further disclose at least two oxynitride layers are formed at temperature of at least about 780 °C (Col 7, Line 24).

4. Claims 17 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mine et al (US 2004/0183122), hereinafter refereed as Mine in view of Jenne (US 6709928), hereinafter refereed as Jenne.

With respect to claim 17, Mine discloses a semiconductor device including an oxide-nitride-oxide (ONO) structure (Figure 4) comprising a multilayer memory layer between a first oxide layer (304a of Fig.4) and a second oxide layer (305 of Fig.4), wherein the multilayer memory layer comprises at least two (304b and 304c of Fig. 4) silicon oxynitride layers.

Mine does not explicitly state an ONO structure comprising a multilayer memory layer. However, it is obvious to one of an ordinary skilled in the art at the time of invention to describe the ONO structure as a multilayer memory layer as the both silicon oxynitride layers can be charge trap/storing layers which characteristic of a non-volatile or volatile memory.

With respect to claim 18, Mine discloses a semiconductor device according to claim 17, as above. Mine does not explicitly discloses at least two oxynitride having Silicon, Oxygen, Nitrogen ,Hydrogen contents having differing stochiometric compositions of oxygen, nitrogen and/or silicon to form multiple oxynitride layers.

In an analogous art, Jenne discloses that oxynitride or silicon nitride ratios between silicon and nitrogen (Col 4, Line 33) may differ from stochiometric ratios (Col 4, Lines 30-31). Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. Hence, it is obvious to one of an ordinary skilled in the

art to have differing stochiometric compositions of oxygen, nitrogen and/or silicon to form multiple oxynitride layers to enhance programming characteristics (Col 2, Line 55).

With respect to claim 19, Mine discloses a semiconductor device according to claim 17, as above. Mine further discloses different ways to improve data/charge retention characteristics using oxygen, nitrogen and silicon profiles across the at least two oxynitride layers. For instance, when a silicon oxynitride film was used as a charge trapping film, the writing speed, the erasing speed, and the charge retention characteristics were all improved… (Page4, Col 63). At another instance, The charge retention characteristics were evaluated by writing information in the memory cell until a predetermined threshold value is reached (step 1), concretely, applying 1.8 V to the memory MOS transistor gate electrode (step 2), leaving the memory cell for 100,000 seconds at 85 deg.C, then comparing the threshold value just after the writing with that after the leaving at the high temperature (step 3) (Page 3, ¶50). It is clear that data retention specification is a function of operating temperature, applied voltage and material used as well as duration for which data can be retained.

It is obvious to one of an ordinary skilled in the art at the time of invention to modify a known technique to a known device as disclosed in Mine's invention and achieve data retention specification at an operating temperature of at least 125°C to enhance characteristics of a non-volatile memory device (Page 2, ¶17).

With respect to claim 20, Mine discloses a semiconductor device according to claim 17, as above.

Mine further discloses at least two oxynitride layers include a top oxynitride layer (304c of Fig.4) and a bottom oxynitride layer (304b of Fig. 4) and a ratio of thicknesses to 1:4.5 (Page

9, ¶128). Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to use a known technique to improve with the ratio to 1:5 in similar devices in the same way to enhance characteristics of a non-volatile memory device (Page 2, ¶17).

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jenne (US 6709928), hereinafter refereed as Jenne in view of Mine et al (US 2004/0183122), hereinafter refereed as Mine in further view of Wu et al, (US 6445030), hereinafter refereed as Wu.

With respect to claim 14, Jenne in view of Mine discloses a method according to claim 12, as above.

In an analogous art, Mine discloses a relation of T2<(N1 x T1)/N2, where T1 and T2 are thickness of top and bottom layer and N represent electron trap density of the top and bottom film to form a multi-layer memory structure (Mine; Page 9, ¶131 & Page 7, ¶98).

Mine fails to disclose forming a tunnel oxide layer using a steam anneal.

In an analogous art, Wu discloses forming an oxide growth using CVD containing oxygen, water vapor and optionally one or more of inert gases (Wu; Col 5, Lines 17-22).

It would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Jenne and select different thickness of a oxynitride layers, as taught by Mine and form oxide layer using steam anneal, as taught by Wu to speedup erasing process and improve charge trapping/storing characteristics (Mine; Page 7, ¶98).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD MOHSIN CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday - Thursday 10:00 AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tu Nguyen can be reached on (571) 272-2424. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/THUY VINH TRAN/
Supervisory Patent Examiner, Art Unit 4126
05/11/09

/MC/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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60909 7590 10/01/2012

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198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
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10/01/2012	PAPER

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	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2898	

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- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2012*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *29-34,36-41,43-47 and 49-52* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *29-34,36-41,43-47 and 49-52* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

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12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

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6) ☐ Other: _____.

DETAILED ACTION

Applicant's arguments, see remarks, filed 04/09/2012, with respect to the rejection(s) of claim(s) 29-34, 36-41, 43-47 and 49-52 under 103 have been fully considered and found not persuasive as addressed below.

However, upon further review of the instant case, rejection of 12/07/2011 has been withdrawn for the following reasons and a new ground(s) of rejection is made.

Claims 29 & 37 rejection has been changed from 103 to 102(e) and dependent claims rejection changed accordingly.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 29-30, 36-37, 43, and 50-51 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya).

Re claim 29, 37, Bhattacharyya discloses a method of forming a semiconductor device (e.g. 100 of Fig.1A) comprising: forming a multi-layer charge storing layer (e.g. 112/114/116/117 and 118 of Fig. 1A), depositing on a substrate (e.g. p-Si substrate) an oxygen-rich, first oxynitride layer (e.g. 112 of Fig. 1A & Claim 3) and depositing directly (e.g. 112 is directly on 114) on the first oxynitride layer an oxygen-lean (e.g. 114 of Fig.1A & Claim 8) second oxynitride layer sequentially (e.g. are shown to deposited one

after another of Fig.1A), a high concentration of oxygen selected to increase retention (e.g. …good charge retention….See abstract) performance of the multi-layer charge storing layer by acting as a barrier (e.g. charge trapping for instance) between charge trapped in the second oxynitride layer and the substrate (e.g. device of Fig.1A being capable of), wherein a difference in concentration of oxygen between the first oxynitride layer and the second oxynitride layer is selected to increase an end-of-life (EOL) (e.g. See abstract, ...device of 1A to enhance life span) for the semiconductor device at a specified difference (e.g. abstract, direct tunneling program and erase) between program and erase voltages to at least about 20 years(e.g. method as disclosed is indeed to enhance life span and inherently capable of a mere use).

Re claim 30, Bhattacharyya discloses a method according to claim 29, wherein the increased retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years (e.g. the first/second and substrate disclosed above being capable of and see also Bhattacharyya; abstract).

Re claim 36, 43, Bhattacharyya discloses a method according to claim 29, wherein a thicknesses of the second oxynitride layer is from 1 to 5 times greater than that of the first oxynitride layer (e.g. Bhattacharyya; Fig. 1A).

With respect to claim 50, Bhattacharyya discloses method according to claim 29, wherein depositing on the first oxynitride layer an oxygen-lean second oxynitride layer comprises depositing the oxygen-lean second oxynitride layer directly on the first

oxynitride layer (i.e. Bhattacharyya; 112 is also directly on 114 as shown in Fig.1A in view of Para 0078).

With respect to claim 51, Bhattacharyya discloses a method according to claim 37, wherein depositing on the first oxynitride layer an oxygen-lean second oxynitride layer comprises depositing the oxygen-lean second oxynitride layer directly on the first oxynitride layer (i.e. Bhattacharyya; 112 is also directly on 114 as shown in Fig.1A in view of Para 0078).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31-34, 38-41, 44-47, 49, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya and Akwani et al (US 2002/0154878, hereinafter Akwani).

Re claim 31, Bhattacharyya discloses a method according to claim 29.

Bhattacharyya does not explicitly disclose wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a

CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 41) using a process gas (e.g. Akwani; Para 43) comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Re claim 32 and 39, Bhattacharyya/Akwani discloses a method according to claim 31, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/NH3 and SiH2C12/NH3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter

encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 33, Bhattacharyya discloses a method according to claim 29.

Bhattacharyya does not explicitly disclose wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas (e.g. Akwani; Para 0041/0043) comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture (e.g. Akwani; Para 0041/0043) at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or

workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve optimum and cost effective deposition method.

Re claim 34, Bhattacharyya/Akwani discloses a method according to claim 33, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Re claim 38, Bhattacharyya discloses a method according to claim 37.

Bhattacharyya does not expliclity disclose wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 0041/0043) using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve optimum and cost effective deposition method.

Re claim 40, Bhattacharyya discloses a method according to claim 37.

Bhattacharyya does not explicitly disclose the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed (e.g. just as first layer is formed) in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1 (e.g. Akwani; Para 0041/0043), and wherein the second oxynitride layer is formed (e.g. just as first layer is formed) in a CVD process (e.g. Akwani; Para 0041/0043) using a process gas (e.g. Akwani; Para 0043) comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve optimum and cost effective deposition method.

Re claim 41, Bhattacharyya/Akwani discloses a method according to claim 40, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. CVD is being capable of) in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio (e.g. as addressed below) of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not

support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Re claim 44, Bhattacharyya discloses a method of forming a semiconductor device (e.g. 100 of Fig.1A) comprising: forming a multi-layer charge storing layer (e.g. 112/114/116/117 and 118 of Fig. 1A), depositing on a substrate (e.g. p-Si substrate) an oxygen-rich, first oxynitride layer (e.g. 112 of Fig. 1A & Claim 3) and depositing directly (e.g. 112 is directly on 114) on the first oxynitride layer an oxygen-lean (e.g. 114 of Fig.1A & Claim 8) second oxynitride layer sequentially (e.g. are shown to deposited one after another of Fig.1A). a high concentration of oxygen selected to increase retention (e.g. …good charge retention….See abstract) performance of the multi-layer charge storing layer by acting as a barrier (e.g. charge trapping for instance) between charge trapped in the second oxynitride layer and the substrate (e.g. device of Fig.1A being capable of).

Bhattacharyya does not explicitly discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20 (oxidizer)/ND3(nitrogen source) and SiH2Cl2 (silicon precursor)/ ND3 mixtures.

In an analogous art, Akwani discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. same material of first and

second oxynitride and can be formed in the same tool & see also Para 47) in a single (e.g. CVD being capable of) CVD tool (e.g. Para 0041) using N20 [oxidizer]/ND3 [nitrogen source] and SiH2Cl2 [silicon precursor]/ ND3[nitrogen source] mixtures (e.g Para 0043). Akwani has clearly disclosed above gaseous mixtures used in formation of oxynitride layer and "It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960) and Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992). Further, changing ratios or concentration of above gaseous mixtures not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Re claim 45, Bhattacharyya/Akwani discloses a method according to claim 44, wherein the first ratio (e.g. Akwani; Para 0041/0043 in view of below determination) of

the N20/ND3 and SiH2C12/ND3 mixtures is about 8:1, and wherein the second ratio of the N20/ND3 and SiH2C12/ ND3 mixtures is about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 46, Bhattacharyya/Akwani discloses a method according to claim 44, wherein a stoichiometric composition of the first oxynitride layer (e.g Bhattacharyya; Abstract) comprises a high concentration of oxygen (e.g. Bhattacharyya; first layer is indeed oxygen rich) selected to increase retention performance (e.g. Bhattacharyya; being capable of) of the multi-layer charge storing layer by acting as a barrier (Bhattaharyya is again being capable of) between charge trapped in the second oxynitride layer and the substrate.

Re claim 47, Bhattacharyya/Akwani discloses a method according to claim 46, wherein the increased retention performance of the multi-layer charge storing layer increases (e.g. Bhattacharyya; Abstract…increased life span) an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages (e.g. Bhattacharyya; Abstract; enhanced program and erase function) to at least about 20 years.

Re claim 49, Bhattacharyya/Akwani discloses a method according to claim 44, wherein a thicknesses of the second oxynitride layer is from 1 to 5 times greater than that of the first oxynitride layer (e.g. Bhattacharyya; Fig. 1A).

With respect to claim 52, A method according to claim 44, wherein depositing on the first oxynitride layer an oxygen-lean second oxynitride layer comprises depositing the oxygen-lean second oxynitride layer directly on the first oxynitride layer (i.e. Bhattacharyya; 112 is also directly on 114 as shown in Fig.1A in view of Para 0078).

Response to Arguments

Applicant's arguments filed 04/09/2012 have been fully considered but they are not persuasive. Applicant argues as follows:

> Applicants submit that Bhattacharyya does not teach or suggest forming a multi-layer charge storing layer, but to the contrary teaches a three layer tunneling layer 112 (labeled K1, K2 and K3 in FIG. 1A) overlaid by a *single* trapping layer 114.

.Examiner respectfully disagrees and submits the following:

Applicant's claim language or specification does not restrict examiner to interpret tunneling layer to have ONLY a single layer.

Applicant further argues as follows:

> In contrast to the above, the device produced by the method of the claimed invention include a single tunneling layer through which charges move by Fowler-Nordheim (FN) tunneling or channel hot electron injection (CHEI), and a multi-layer charge storing layer, in which charges hop through an "oxygen-rich, first oxynitride layer" and become trapped in traps in an "oxygen-lean second oxynitride layer." Because the claimed device uses a standard tunneling layer with FN tunneling along with a multi-layer charge storing layer, it is capable of achieving increased charge retention and extended operating life while using higher, standard programming and erase voltages.

.Examiner respectfully disagrees and submits the following:

Bhattacharyya discloses Fowler-Nordheim programming and erasing operations via insulators at numerous instances (e.g. See at least Para 0035). Therefore, applicant's argument and an attempt to distinguish claimed invention using Fowler-Nordheim found NOT persuasive.

Applicant further argues as follows:

> application a tunneling layer is much thinner than a charge storage layer – typically four to six times thinner. Concerning function, the tunneling layer enables charge to be injected from the device channel to the charge storage layer which functions to store or trap the charges. Concerning the mechanism by which they function as noted above the tunneling layer functions by FN tunneling, or in the case of Bhattacharyya, while in the charge storage layer charges move from the interface of the tunneling layer to the charge traps by charge hopping.

Examiner respectfully disagrees and submits the following:

Product claims can only be distinguished using structural differences. However, claims 29,37, and 44 are indeed method claims. Further, thickness of tunneling layer is indeed not claimed.

Applicant yet further argues as follows:

> Lastly, the applicants submit that Bhattacharyya does not teach or suggest wherein the top most tunneling layer comprises an oxygen-rich oxynitride layer. Applicants acknowledge that as noted by the examiner Bhattacharyya discloses in claim 3 wherein the multilayer tunneling layer may include an oxygen-rich oxynitride layer – however applicants submit that this does not teach or suggest wherein the it is the top most tunneling layer, the one in contact with the charge storage layer 114 that comprises an oxygen-rich oxynitride layer. In particular, the applicants note that in the only embodiment described in Bhattacharyya wherein the tunneling layer includes an oxygen-rich oxynitride layer, it is described as the second of three

Examiner respectfully disagrees and submit the following:

Claim language does not restrict Examiner to 'a single layer' interpretation. Bhattacharyya layer 112 can be interpreted as single layer as shown in Abstract figure.

Therefore, rejection of independent claims is maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 1-571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JULIO J. MALDONADO/
Supervisory Patent Examiner, Art Unit 2898

/MC/

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11/811,958	06/13/2007	Sagy Levy	PM2007002	9184

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EXAMINER	
CHOUDHRY, MOHAMMAD M	
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2894	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/811,958	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/07/2010 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29 – 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya) and Akwani et al (US 2002/0154878, hereinafter Akwani).

Re claim 29, 37, and 44, Bhattacharyya discloses a method of forming a semiconductor device (e.g. 100 of Fig.1A) including a multi-layer charge storing layer (e.g. 112/114/116/117 and 118 of Fig. 1A) comprising: depositing on a substrate (e.g. p-Si substrate) an oxygen-rich, first oxynitride layer (e.g. 112 of Fig. 1A & Claim 3) and depositing on the first oxynitride layer an oxygen-lean (e.g. 114 of Fig.1A & Claim 8)

second oxynitride layer sequentially (e.g. are shown to deposited one after another of Fig.1A). [Distinct Claim 29 limitation STARTS here] a high concentration of oxygen selected to increase retention (e.g. …good charge retention….See abstract) performance of the multi-layer charge storing layer by acting as a barrier (e.g. charge trapping for instance) between charge trapped in the second oxynitride layer and the substrate (e.g. device of Fig.1A being capable of). [Distinct claim 37 limitation STARTS here] wherein a difference in concentration of oxygen between the first oxynitride layer and the second oxynitride layer is selected to increase an end-of-life (EOL) (e.g. See abstract, ...device of 1A to enhance life span) for the semiconductor device at a specified difference (e.g. abstract, direct tunneling program and erase) between program and erase voltages to at least about 20 years [Distinct claim 37 limitation ENDS here].

Bhattacharyya does not explicitly discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20 (oxidizer)/ND3(nitrogen source) and SiH2Cl2 (silicon precursor)/ ND3 mixtures.

In an analogous art, Akwani discloses depositing the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. same material of first and second oxynitride and can be formed in the same tool & see also Para 47) in a single (e.g. CVD being capable of) CVD tool (e.g. Para 0041) using N20 [oxidizer]/ND3 [nitrogen source] and SiH2Cl2 [silicon precursor]/ ND3[nitrogen source] mixtures (e.g Para 0043). Akwani has clearly disclosed above gaseous mixtures used in formation of

oxynitride layer and "It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960) and Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992). Further, changing ratios or concentration of above gaseous mixtures not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Re claim 30, Bhattacharyya/Akwani discloses a method according to claim 29, wherein the increased retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years (e.g. the first/second and substrate disclosed above being capable of and see also Bhattacharyya; abstract).

Re claim 31, Bhattacharyya/Akwani discloses a method according to claim 29, wherein the wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 41) using a process gas (e.g. Akwani; Para 43) comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 32 and 39, Bhattacharyya/Akwani discloses a method according to claim 31, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/NH3 and SiH2C12/NH3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 33, Bhattacharyya/Akwani discloses a method according to claim 29, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas (e.g. Akwani; Para 0041/0043) comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture (e.g. Akwani; Para 0041/0043) at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 34, Bhattacharyya/Akwani discloses a method according to claim 33, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 35, 42 and 48, Bhattacharyya/Akwani discloses a method according to claim 29, wherein at least one of the first oxynitride layer and the second oxynitride layer is formed at temperature of at least about 780 °C (e.g. Akwani; oxidizing and CVD deposition shown and has to have a temperature). Further, differences in temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 36, 43, and 49, Bhattacharyya/Akwani discloses a method according to claim 29, wherein a thicknesses of the second oxynitride layer is from 1 to 5 times greater than that of the first oxynitride layer (e.g. Bhattacharyya; Fig. 1A).

Re claim 38, Bhattacharyya/Akwani discloses a A method according to claim 37, wherein the wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 0041/0043) using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not

inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 40, Bhattacharyya/Akwani discloses a method according to claim 37, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1 (e.g. Akwani; Para 0041/0043), and wherein the second oxynitride layer is formed (e.g. just as first layer is formed) in a CVD process (e.g. Akwani; Para 0041/0043) using a process gas (e.g. Akwani; Para 0043) comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 41, Bhattacharyya/Akwani discloses a method according to claim 40, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially (e.g. CVD is being capable of) in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio (e.g. as addressed below) of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general

conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 45, Bhattacharyya/Akwani discloses a method according to claim 44, wherein the first ratio (e.g. Akwani; Para 0041/0043 in view of below determination) of the N20/ND3 and SiH2C12/ND3 mixtures is about 8:1, and wherein the second ratio of the N20/ND3 and SiH2C12/ ND3 mixtures is about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 46, Bhattacharyya/Akwani discloses a method according to claim 44, wherein a stoichiometric composition of the first oxynitride layer (e.g Bhattacharyya; Abstract) comprises a high concentration of oxygen (e.g. Bhattacharyya; first layer is indeed oxygen rich) selected to increase retention performance (e.g. Bhattacharyya; being capable of) of the multi-layer charge storing layer by acting as a barrier (Bhattaharyya is again being capable of) between charge trapped in the second oxynitride layer and the substrate.

Re claim 47, Bhattacharyya/Akwani discloses a method according to claim 46, wherein the increased retention performance of the multi-layer charge storing layer

increases (e.g. Bhattacharyya; Abstract…increased life span) an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages (e.g. Bhattacharyya; Abstract; enhanced program and erase function) to at least about 20 years (e.g. Bhattacharyya; disclosed prior art being capable of).

Response to Arguments

Applicant's arguments with respect to claims above have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday - Thursday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 1-571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

/Kimberly D Nguyen/

Supervisory Patent Examiner, Art Unit 2894

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EXAMINER
CHOUDHRY, MOHAMMAD M

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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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pbj@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 001324

Office Action Summary	Application No. 13/436,872	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/03/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

6)☒ Claim(s) *14* is/are allowed.

7)☒ Claim(s) *1-13* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Embodiment III in the reply filed on 09/03/2014 is acknowledged. The traversal is on the ground(s) that Embodiment II – (figures 8A – 8B) and III (figures 9A – 9B) overlap in scope and therefore are not mutually exclusive. This is found persuasive and withdrawn claims 11 – 12 are being examined along with claims 1 - 10 and 13 -14. Further, examiner note that claims 3 - 4 are mutually exclusive as channel can be either recrystallized polysilicon or a silicon nanorwire. However, to expedite the prosecution, further restriction is not imposed and claims are being examined.

The requirement is now deemed proper and is therefore made FINAL.

Priority

Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 as follows:

The later-filed application must be an application for a patent for an invention which is also disclosed in the prior application (the parent or original nonprovisional application or provisional application). The disclosure of the invention in the parent application and in the later-filed application must be sufficient to comply with the requirements of 35 U.S.C. 112(a) or the first paragraph of pre-AIA 35 U.S.C. 112,

except for the best mode requirement. See *Transco Products, Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994)

The disclosure of the prior-filed application, Application No. 11/811,958, fails to provide adequate support or enablement in the manner provided by 35 U.S.C. 112(a) or pre-AIA 35 U.S.C. 112, first paragraph for claims 4 – 5, 9 – 11 of this application.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim Claims 1,6 and 8 of Polishchuk et al U.S. Patent No. 8,860,122 (hereinafter '122). Although the claims at issue is not identical, they are not patentably distinct from each other because.

With respect to claim 1. '122 discloses a memory device (Claim 1,6 and 8) comprising: a channel (channel) formed from a semiconducting material overlying a surface on a substrate connecting a source (source) and a drain (drain) of the memory device; a tunnel oxide layer (tunnel dielectric) overlying the channel; and a multi-layer charge storing layer (charge trapping layer) including an oxygen-rich, first oxynitride layer (oxygen-rich oxynitride layer) on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free (functionality in product claims), and an oxygen-lean, second oxynitride layer (oxygen-

rich oxynitirde and obviously oxygen lean) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense.

Claims 9 & 10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 - 7, of Jenne et al U.S. Patent No. (US 8,710,578, hereinafter '578), in view of Chen et al (US 2005/0275010, hereinafter Chen).

With respect to claim 9. Jenne discloses a memory device (memory device – claim 1) comprising: an electrically conducting channel (channel) formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device(connecting); a tunnel oxide layer (tunnel oxide) overlying the channel; and a multi-layer charge storing layer (top and bottom trapping layer) including a first oxynitride layer (top charge trapping layer) closer to the tunnel oxide layer, and a second oxynitride layer, wherein the first oxynitride layer is separated from the second oxynitride layer (bottom trapping layer) by an anti-tunneling layer (anti tunneling layer) comprising an oxide.

Jenne does not disclose a non-planar transistor including a gate having multiple surfaces abutting the channel.

In an analogous art, Chen discloses a non-planar transistor including a gate having multiple surfaces abutting the channel (Figure 7g).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Jenne's invention and form gate in non-planar form to mitigate short channel affect (Para 0003).

With respect to claim 10, Jenne/Chen the memory device of claim 9, wherein the channel comprises a silicon nanowire (claim 7).

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 of U.S. Patent No. (8,222,688, hereinafter '688), in view of Bhattacharyya (2006/0261401, hereinafter '401).

With respect to claim 1. A multi-layer charge storing layer (First and Second) including an oxygen-rich, first oxynitride layer (first nitride oxygen-rich layer) on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean, second oxynitride layer (second nitride/oxynitride layer - oxygen lean relative to oxygen rich) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense.

Bhattacharyya does not discloses a memory device comprising: a channel formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device; a tunnel oxide layer overlying the channel.

In an analogous art, ***a*** memory device comprising: a channel (claim 1 – channel) formed from a semiconducting material overlying a surface on a substrate connecting a

source (source) and a drain (drain) of the memory device; a tunnel oxide layer (tunnel insulator) overlying the channel.

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify '688's invention and form gate/source/drain to form charge retaining device.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 & 13 of U.S. Patent No (8,643,124, hereinafter '124).

With respect to claim 1. '124 discloses a memory device (Claims 1,and 13) comprising: a channel (channel) formed from a semiconductor material overlying a surface on a substrate connecting a source (source) and a drain (drain) of the memory device; a tunnel oxide layer (tunnel oxide) overlying the channel; and a multi-layer charge storing layer (charge storing layer) including an oxygen-rich, first oxynitride layer (first charge storing oxygen-rich oxynitride layer) on the tunnel oxide layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free (functionality in product claims), and an oxygen-lean, second oxynitride layer (second oxygen-rich oxynitirde and obviously oxygen lean) on the first oxynitride layer in which a stoichiometric composition of the second oxynitride layer results in it being trap dense.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya).

With respect to claim 1, Bhattacharyya discloses a memory device (Fig. 1A) comprising: a channel (108) formed from a semiconducting material (Si-Substrate) overlying a surface (Top surface) on a substrate (102) connecting a source (104) and a drain (106) of the memory device; a tunnel oxide layer (112) overlying the channel; and a multi-layer charge storing layer (Combined – 114/116/117/118) including an oxygen-rich, first oxynitride layer (114) on the tunnel oxide layer, and an oxygen-lean, second oxynitride layer (116 – Para 0068) on the first oxynitride layer.

Bhattacharyya does not explicitly disclose that first oxynitride layer to function as a trap free and second oxynitride layer to function as trap dense. However, While

features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber,* 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997), Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to recite Bhattacharyya disclosed invention functionality while no distinct structural feature is being claimed.

Claim 2 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Morii (US 5,847,411, hereinafter Morii).

With respect to claim 2, Bhattacharyya the memory device of claim 1.

Bhattacharyya does not disclose wherein the channel comprises polysilicon.

In an analogous art, Morii disclose a channel that comprises polysilicon.

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form channel that comprises polysilicon to improve mobility of a carrier in the channel.

Claim 3 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Pfiester et al(US 5,348,903, hereinafter Pfiester).

With respect to claim 3, Bhattacharyya discloses the memory device of claim 1.

Bhattacharyya does not disclose the channel comprises recrystallized polysilicon.

In an analogous art, Pfiester discloses a channel that can formed of polysilicon and recrystallized (col 5, line 29 – 40).

Therefore, it would have been obvious to one of an ordinary skilled in the art a the time of invention to modify Bhattacharyya's disclosed invention and form channel with recrystallized polysilicon to obtain a low channel electrical resistance (Col 5, lines 30 – 45).

Claim 4 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Duan et al (US 2005/0079659, hereinafter Duan).

With respect to claim 4, Bhattacharyya the memory device of claim 1.

Bhattacharyya does not disclose the channel comprises a silicon nanowire.

In an analogous art, Duan discloses a channel comprising silicon nanowire (Para 0159).

Therefore, it would have been obvious to one an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form channel with nanowires to enhance mobility (Para 0159).

Claim 5 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Chen et al (US 2005/0275010, hereinafter Chen).

With respect to claim 5, Bhattacharyya the memory device of claim 1, the gate comprises the tunnel oxide layer and the multi-layer charge storing layer.

Bhattacharyya does not disclose a non-planar transistor including a gate having multiple surfaces abutting the channel.

In an analogous art, Chen discloses a non-planar transistor including a gate having multiple surfaces abutting the channel (Figure 7g).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's invention and form gate in non-planar form to mitigate short channel affect (Para 0003).

With respect to claim 6, Bhattacharyya/Chen discloses the memory device of claim 5, wherein the gate further comprises a blocking dielectric (Para 0069) overlying the multi-layer charge storing layer, and a metal gate layer (Bhattacharyya; Para 0070) overlying the blocking dielectric layer.

With respect to claim 7, Bhattacharyya/Chen the memory device of claim 6, wherein the blocking dielectric comprises a high K dielectric (Bhattacharyya; Para0047).

Claim 8 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, in view of Lee et al (US 2003/0030100, hereinafter Lee).

With respect to claim 8, Bhattacharyya discloses the memory device of claim 1.

Bhattacharyya does not disclose wherein the second oxynitride layer further comprises a concentration of carbon selected to increase a number of traps therein.

In an analogous art, Lee disclose increasing concentration of carbon into the oxynitride layer (Para 0034).

Thereofore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form carbon into oxynitride layer to achieve narrow band than silicon oxynitride (Para 0034).

Claim 9 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Mine et al (US 6,833,582, hereinafter Mine).

With respect to claim 9, Mine discloses a memory device (Fig. 1) comprising: an electrically conducting channel formed from a semiconducting material overlying a surface on a substrate connecting a source and a drain of the memory device (Col 9, lines 10 -16); and a gate having multiple surfaces abutting the channel (top side and bottom abutting the channel), the gate comprising: a tunnel oxide layer overlying the channel;

Mine does not explicitly disclose in Fig. 1A and a multi-layer charge storing layer including a first oxynitride layer closer to the tunnel oxide layer, and a second oxynitride layer, wherein the first oxynitride layer is separated from the second oxynitride layer by an anti-tunneling layer comprising an oxide (Fig. 15, Col 14, lines 36 – 42; Col 15, lines 5 – 10, Col 13, lines 15 -20).

However, Fig. 15 discloses and a multi-layer charge storing layer including a first oxynitride layer closer to the tunnel oxide layer, and a second oxynitride layer, wherein the first oxynitride layer is separated from the second oxynitride layer by an anti-tunneling layer comprising an oxide (Fig. 15, Col 14, lines 36 – 42; Col 15, lines 5 – 10, Col 13, lines 15 -20).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Fig.1 to achieve low voltage erasing opertion.

Claim 10 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Mine, in view of Duan et al (US 2005/0079659, hereinafter Duan).

With respect to claim 10, Bhattacharyya the memory device of claim 9.

Bhattacharyya does not disclose the channel comprises a silicon nanowire.

In an analogous art, Duan discloses a channel comprising silicon nanowire (Para 0159).

Therefore, it would have been obvious to one an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form channel with nanowires to enhance mobility (Para 0159).

With respect to claim 11, Mine discloses the memory device of claim 9, wherein the device comprises a finFET, and wherein the gate further comprises a blocking dielectric (504. Fig. 15) overlying the multi-layer charge storing layer, and a metal gate layer (MNOS - Background) overlying the blocking dielectric layer.

With respect to claim 12, The memory device of claim 11, wherein the blocking dielectric comprises a high K dielectric (Fig. 15).

With respect to claim 13, Mine discloses the memory device of claim 9, wherein the anti-tunneling layer comprises a portion of the first oxynitride layer that has been oxidized by radical oxidation (Mine disclosed the anti-tunneling layer. Claim is not a product by process and product must be distinguished by features).

Allowable Subject Matter

Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 1-571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Mohammad Choudhry/
AU 2816

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/917,500	06/13/2013	Sagy Charel Levy	PM07002C1	1009

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EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
01/05/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
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Sandisk Technologies, Inc. - Ex. 1002, Page 001339

Office Action Summary	Application No. 13/917,500	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/11/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21 - 39* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *29-39* is/are allowed.

7)☒ Claim(s) *21-28* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *10/29/2014,04/11/2014,04/08/2014,04/09/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 21 - 26 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 11-21 & 23 of copending Application No. 13/007,533 (hereinafter referred to as '533) in view of Yu et al (US 6624090, hereinafter Yu). Although the conflicting claims are not identical, they are not patentably distinct from each other because;

With respect to claim 21. '533 discloses a method of forming a semiconductor device comprising: forming a multi-layer charge storing layer comprising depositing on a substrate an oxygen-rich, first oxynitride layer and depositing directly on the first oxynitride layer an oxygen- lean and silicon-rich second oxynitride layer; and wherein a stoichiometric composition of the first oxynitride layer comprises a high concentration of oxygen selected to increase retention performance of the multi-layer charge storing layer by acting as a barrier between charge trapped in the second oxynitride layer and the substrate (e.g. '533 - Claim 11).

'533 does not explicitly disclose steam annealing the second oxynitirde layer to reduce a number of traps formed near top surface thereof.

In an analogous art, Yu discloses annealing oxyntride layer (Col 2, lines 30 – 40).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and anneal oxynitirde layer to increase penetration into the oxide layer below to increase reliability.

With respect to claim 22. '533/Yu discloses a method according to claim 21, wherein the increased retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years (e.g. '533 – Claim 16).

With respect to claim 23. '533/Yu discloses a method according to claim 21, wherein the wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiHzClz)/ammonia (NH3) mixture and a nitrous oxide (NzO)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a NzO/NH3 mixture and a SiHzClz/NH3 mixture at a ratio of about 5:1 (e.g. '533 - Claim 18).

With respect to claim 24. '533/Yu discloses a method according to claim 23, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the NzO/NH3 and SiHzClz/NH3 mixtures (e.g. '533 - Claim 19).

With respect to claim 25. '533/Yu discloses a method according to claim 21, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1 (e.g. '533 - Claim 18).

With respect to claim 26, '533/Yu discloses a method according to claim 25, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N20/ND3and SiH2C12/ND3 mixtures (e.g. '533 - Claim 19).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya), further in view of Yu et al (US 6624090, hereinafter Yu).

Re claim 21, Bhattacharyya discloses a method of forming a semiconductor device (e.g. 100 of Fig.1A) comprising: forming a multi-layer charge storing layer (e.g. 112/114/116/117 and 118 of Fig. 1A), depositing on a substrate (e.g. p-Si substrate) an oxygen-rich, first oxynitride layer (e.g. 112 of Fig. 1A & Claim 3) and depositing directly (e.g. 112 is directly on 114) on the first oxynitride layer an oxygen-lean (e.g. 114 of Fig.1A & Claim 8) second oxynitride layer sequentially (e.g. are shown to deposited one after another of Fig.1A), a high concentration of oxygen selected to increase retention (e.g. …good charge retention….See abstract) performance of the multi-layer charge storing layer by acting as a barrier (e.g. charge trapping for instance) between charge

trapped in the second oxynitride layer and the substrate (e.g. device of Fig.1A being capable of), wherein a difference in stoichiometric composition of the first oxynitride layer and the second oxynitride layer is selected to increase a difference between programming and erase voltages, thereby increasing data retention, improving speed of the semiconductor device and increase an end-of-life (EOL) (e.g. See abstract, ...device of 1A to enhance life span) for the semiconductor device at a specified difference (e.g. abstract, direct tunneling program and erase) between program and erase voltages to at least about 20 years(e.g. method as disclosed is indeed to enhance life span and inherently capable of a mere use).

Bhattacharyya does not explicitly disclose the second oxynitride layer to be silicon-rich, oxygen layer in a single disclosed embodiment as above.

However, Bhattacharyya do disclose that second oxynitride layer to be made by silicon-rich nitride and nitride layer can be a substitute with oxynitride layer (e.g. Claim 28, Para 0061).

Therefore, it would have been obvious to one an ordinary skilled in the art at the time of invention to modify Bhattacharyya disclosed invention and form stacked oxynitirde layer with silicon-rich, oxygen lean oxynitirde layer to enhance life span of the semiconductor device (e.g. Abstract).

Bhattacharyya further does not explicitly disclose steam annealing the second oxynitirde layer to reduce a number of traps formed near top surface thereof.

In an analogous art, Yu discloses annealing oxyntride layer (Col 2, lines 30 – 40).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and anneal oxynitirde layer to increase penetration into the oxide layer below to increase reliablity.

Re claim 22, Bhattacharyya/Yu discloses a method according to claim 21, wherein the increased retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years (e.g. the first/second and substrate disclosed above being capable of and see also Bhattacharyya; abstract).

With respect to claim 27, Bhattacharyya/Yu disclosed method according to claim 21, wherein a thicknesses of the second oxynitride layer is from 1 to 5 times greater than that of the first oxynitride layer(e.g. Bhattacharyya; Fig. 1A). Also, federal circuit held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. In *Gardnerv.TEC Syst., Inc.,* 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied,* 469 U.S. 830, 225 USPQ 232 (1984),

Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya/Yu and Akwani et al (US 2002/0154878, hereinafter Akwani).

Re claim 23, Bhattacharyya/Yu discloses a method according to claim 21.

Bhattacharyya/Yu does not explicitly disclose wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process (e.g. Akwani; Para 41) using a process gas (e.g. Akwani; Para 43) comprising a dichlorosilane (SiH2C12)/ammonia (NH3) mixture and a nitrous oxide (N20)/NH3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/NH3 mixture and a SiH2C12/NH3 mixture at a ratio of about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya’s disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Re claim 24, Bhattacharyya/Yu/Akwani discloses a method according to claim 23, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/NH3 and SiH2C12/NH3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Re claim 25, Bhattacharyya/Yu discloses a method according to claim 21.

Bhattacharyya does not explicitly disclose wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of about 5:1.

In an analogous art, Akwani discloses the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas (e.g. Akwani; Para 0041/0043) comprising a dichlorosilane (SiH2C12)/deuterated-ammonia (ND3) mixture and a nitrous oxide (N20)/ND3 mixture (e.g. Akwani; Para 0041/0043) at a ratio of about 8:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N20/ND3mixture and a SiH2C12/ND3 mixture at a ratio of

about 5:1. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya’s disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve optimum and cost effective deposition method.

Re claim 26, Bhattacharyya/Yu/Akwani discloses a method according to claim 25, wherein the forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool (e.g. Akwani; Para 0041/0043) by changing the ratio of the N20/ND3and SiH2C12/ND3 mixtures. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya/Yu and in view of Lee C W (KR 2006100092, hereinafter Lee).

With respect to claim 28, *Bhattacharyya* /Yu discloses a method according to claim 21.

Bhattacharyya /Yu does not explicitly disclose comprising forming a blocking oxide layer directly on the second oxynitride layer.

In an analogous art, Lee discloses comprising forming a blocking oxide layer directly on the second oxynitride layer (Derwent; Abstract).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya /Yu's disclosed invention and form blocking oxide on the oxynitirde as it is known to improve current performance of a gate.

Allowable Subject Matter

Claim 30 and 37 are allowed.

Claims 31 – 36 & 38 – 39 are allowed by virtue of dependency on claim 30 or 37.

Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

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/Mohammad Choudhry/
AU 2816

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/172,775	02/04/2014	Sagy Charel Levy	PM07002CIP1C1	8762

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Sandisk Technologies, Inc. - Ex. 1002, Page 001352

Office Action Summary	Application No. 14/172,775	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

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Status

1)☒ Responsive to communication(s) filed on *06/10/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-40* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21-30, 32-40* is/are rejected.

8)☒ Claim(s) *31* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *09/30/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 112

Claims 21, 25 & 35 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre- AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

The terms “silicon rich" and "nitrogen rich" in claims 21, 25 & 35 are relative terms which render the claim indefinite. The term "rich" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. "rich silicon/nitrogen" can refer as a relative term of degree to another layer’s concentration or can refer more than 50% concentration.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s)

because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims below rejected on the ground of nonstatutory double patenting as being unpatentable over claims as indicated below of U.S. Patent No. US 8643124

(hereinafter ‘124). Although the claims at issue are not identical, they are not patentably distinct from each other because.

Claims 21, 22, 25 - 27 and 35 & 36 are disclosed in claim 1 of ‘124.

Claim 23 & 24 disclosed in claim 8 of ‘124.

Claim 28 is discloses in claim 18 of ‘124.

Claim 29 & 30 disclosed in claim 8 & 9 of ‘124.

Claim 31 disclosed in claim 12 of ‘124.

Claim 32 disclosed in claim 18 of ‘124.

Claim 33 disclosed in claim 16 of ‘124.

Claim 34 disclosed in claim 15 of ‘124.

Claim 39 disclosed in claim 18 of ‘124.

Claim 40 disclosed in claim 1 of ‘124.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25, 27 – 28, 32 – 36, and 39 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya).

With respect to claim 25. Bhattacharyya discloses a method comprising: forming a tunnel oxide layer (e.g. first layer of 112 & Para 0073) on a substrate (e.g. on top of P-Si); forming on the tunnel oxide layer a multi-layer charge storing layer (e.g. 112/114/116/117) including at least a first charge storing layer comprising an oxygen-rich oxynitride (e.g. See K2-K3 of 112 & claim 3) overlying the tunnel oxide layer, and a second charge storing layer overlying the first charge storing layer comprising a silicon-rich and nitrogen-rich oxynitride layer (e.g. 114 - Para 0074, showing layer to be nitrogen-rich SiOn) that is oxygen-lean relative to the first charge storing layer, wherein second charge storage layer comprises a majority of charge traps distributed in the multi-layer charge storing layer. number of traps therein and comprises a majority of charge traps distributed in multi- layer charge storing layer; and forming a blocking oxide layer on the second oxynitride layer; and forming a gate layer (e.g. 118) on the blocking oxide layer (e.g. 116).

Bhattacharyya does not explicitly disclose the majority of charge traps distributed in multilayer charge storing layer. However, Bhattacharyya has explicilty

disclosed the product as claimed and inherently capable of having charge traps in charge storage layers.

With respect to claim 27 & 36. Bhattacharyya discloses the method of claim 25, wherein the second charge storing layer is deposited directly on the first charge storing layer (Bhattacharaya; second layer is indeed on first layer).

With respect to claim 28 & 39. The method of claim 25, wherein the second charge storing layer comprises charge trap density at least 1000 times greater than the first charge storing layer.

Bhattacharyya has disclosed claimed invention of claim1 except the explicit disclosure of optimum thickness of both first and second oxynitride layers. However, in view of applicant specification (e.g. Para 0028), there is range specified of 7nm - 15 nm or it can be about 10 nm for first and second oxynitride layers. Bhattacharyya clearly disclose the range of both first and second oxynitiride layers to be about 10nm (e.g. Para 0071). Further, applicant has not shown any criticality to claimed thickness that will make the device inoperable. Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum thicknesses to increase charge retention device, as taught by Bhattacharyya (Abstract).

With respect to claim 32. Bhattacharyya disclosed the method of claim 25, wherein the tunneling layer is formed by radical oxidation using a reaction between oxygen (O2) and hydrogen (H2) on the substrate at temperatures of at least 1000℃ (Generally, differences in concentration or temperature will not support the patentability

of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In reAller,* 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

With respect to claim 33 & 34. Bhattacharyya discloses the method of claim 25, Bhattacharyya has disclosed claimed invention of claim 33 & 34 except exact ranges of oxygen concentration in oxynitride layers. Applicant has discloses multiple ranges of oxygen concentration in first and second oxynitride layers (e.g. see Para 044, 0045 and as originally filed claim 2) and has shown no criticality to varying changes concentration of oxygen that will make device inoperable. However, Bhattacharyya discloses that oxygen concentration can range to about 20% (e.g. Para 0067).
Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum oxygen concentration to increase charge retention device, as taught by Bhattacharyya (Abstract).

Claims 21 - 22, 26 & 40 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyy, and Lee et al (US 2003/0030100, hereinafter Lee).

With respect to claim 21 & 22. Bhattacharyya discloses a method comprising: forming a tunnel oxide layer (e.g. first layer of 112 & Para 0073) on a substrate (e.g. on top of P-Si); forming on the tunnel oxide layer a multi-layer charge storing layer (e.g.

112/114/116/117) including at least a first charge storing layer comprising an oxygen-rich oxynitride (e.g. See K2-K3 of 112 & claim 3) overlying the tunnel oxide layer, and a second charge storing layer overlying the first charge storing layer comprising a silicon-rich and nitrogen-rich oxynitride layer (e.g. 114 - Para 0074, showing layer to be nitrogen-rich SiOn) that is oxygen-lean relative to the first charge storing layer, wherein second charge storage layer comprises a majority of charge traps distributed in the multi-layer charge storing layer. number of traps therein and comprises a majority of charge traps distributed in multi- layer charge storing layer; and forming a blocking oxide layer on the second oxynitride layer; and forming a gate layer (e.g. 118) on the blocking oxide layer (e.g. 116), wherein the second charge storing layer is deposited directly on the first charge storing layer (Bhattacharaya; second layer is indeed on first layer).

Bhattacharyya does not explicitly disclose the majority of charge traps distributed in multilayer charge storing layer and wherein the second charge storing layer further comprises a concentration of carbon selected to increase a number of traps therein.

In an analogous art, Lee discloses concentration of a carbon in charge storage layer (Abstract).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya disclosed invention and increase concentration of Carbon in a device to increase charge retention characteristics of a memory.

With respect to claim 26 & 40. Bhattacharyya discloses the method of claim 25.

Bhattacharyya does not discloses wherein the second charge storing layer further comprises a concentration of carbon selected to increase a number of traps therein.

In an analogous art, Lee discloses concentration of a carbon in charge storage layer (Abstract).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya disclosed invention and increase concentration of Carbon in a device to increase charge retention characteristics of a memory.

Claims 29 & 30 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyy, and Akwani et al (US 2002/0154878, hereinafter Akwani).

With respect to claim 29 & 30. Bhattacharyya discloses the method of claim 25.

Bhattacharyya does not explicitly disclose wherein the first charge storing layer is formed in a chemical vapor deposition (CVD) tool using a process gas comprising dichlorosilane (SiH2Cl2), deuterated-ammonia (ND3) and nitrous oxide (N20) and wherein forming the second charge storing is formed sequentially in the same CVD tool using a process gas comprising dichlorosilane (SiHzCl2), and ammonia (NH3).

In an analogous art, Akwani discloses wherein the first charge storing layer is formed in a chemical vapor deposition (CVD) tool using a process gas comprising dichlorosilane (SiH2Cl2), deuterated-ammonia (ND3) and nitrous oxide (N20) and wherein forming the second charge storing is formed sequentially in the same CVD tool

using a process gas comprising dichlorosilane (SiHzCl2), and ammonia (NH3) (e.g. Akwani; Para 41, Para 43).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Claims 23-24 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyy/Lee, and Akwani et al (US 2002/0154878, hereinafter Akwani).

With respect to claim 23 & 24. Bhattacharyya/Lee discloses the method of claim 25.

Bhattacharyya does not explicitly disclose wherein the first charge storing layer is formed in a chemical vapor deposition (CVD) tool using a process gas comprising dichlorosilane (SiH2Cl2), deuterated-ammonia (ND3) and nitrous oxide (N20) and wherein forming the second charge storing is formed sequentially in the same CVD tool using a process gas comprising dichlorosilane (SiHzCl2), and ammonia (NH3).

In an analogous art, Akwani discloses wherein the first charge storing layer is formed in a chemical vapor deposition (CVD) tool using a process gas comprising dichlorosilane (SiH2Cl2), deuterated-ammonia (ND3) and nitrous oxide (N20) and wherein forming the second charge storing is formed sequentially in the same CVD tool

using a process gas comprising dichlorosilane (SiHzCl2), and ammonia (NH3) (e.g. Akwani; Para 41, Para 43).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya/Lee's disclosed invention and form the oxynitride layer using CVD and gases as disclosed by Akwani to achieve cost effective deposition method.

Claims 37 and 38 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyy, and Gregor et al (US 6,023,093, hereinafter Gregor).

With respect to claim 37 & 38, Bhattacharyya discloses the multi-layer charge storing layer of claim 35.

Bhattacharyya does not explicitly discloses wherein the first charge storing layer comprises deuterium, wherein the second charge storing layer is substantially deuterium free.

In an analogous art, Gregor discloses affects of hydrogen isotope such as deuterium (Abstract and Col 5, lines 5 – 20).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and achieve more robustness under channel hot electron stress.

Allowable Subject Matter

Claim 31 objected to as being dependent upon a rejected base claim, but would be allowable if ALL of the limitations of claim 31and any intervening claims incorporated into base claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 1-571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 03/07/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 03/07/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$0	$2070	06/07/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001366

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$0	$2070	06/07/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2898	257-411000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Sandisk Technologies, Inc. - Ex. 1002, Page 001367

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

60909 7590 03/07/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 03/07/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001368

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	13/007,533	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2898	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/21/2012*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *11-21,23 and 28-33*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/21/2012 & 02/20/2013
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/ Examiner, Art Unit 2898	/JULIO J. MALDONADO/ Supervisory Patent Examiner, Art Unit 2898

Sandisk Technologies, Inc. - Ex. 1002, Page 001370

DETAILED ACTION

Election/Restrictions

Claims 28-33 are directed to an allowable product. Pursuant to the procedures set forth in MPEP § 821.04(b), claims 11-21 & 23 are directed to the process of making or using the allowable product, previously withdrawn from consideration as a result of a restriction requirement, are hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Because a claimed invention previously withdrawn from consideration under 37 CFR 1.142 has been rejoined, **the restriction requirement has groups I and II as set forth in the Office action mailed on 12/06/2011 is hereby withdrawn**. In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Allowable Subject Matter

Claims 11 & 28 are allowed.

Claims 12 – 21, 23, & 28 - 33 are allowed by virtue of dependency on claims 11 and 28.

The following is a statement of reasons for the indication of allowable subject matter: Prior art of record does not explicitly disclose or render obvious "a second charge storing layer directly on the first charge storing layer comprising an oxygen-lean, silicon-rich and nitrogen-rich oxynitride in which a stoichiometric composition of the oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer results in it being trap dense" in combination of all other limitation of claims 11 & 28.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 1-571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 06/18/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 06/18/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	09/18/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001374

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 06/18/2013
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	09/18/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2898	257-411000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Sandisk Technologies, Inc. - Ex. 1002, Page 001375

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1002, Page 001376

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

60909 7590 06/18/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 06/18/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001377

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Notice of Allowability	Application No. 13/007,533	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2898	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *05/21/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *11-21,23 and 28-33*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

   Interim copies:

   a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
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Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 05/21/2013
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/ Examiner, Art Unit 2898	/JULIO J. MALDONADO/ Supervisory Patent Examiner, Art Unit 2898

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 05/21/2013 has been entered.

Election/Restrictions

Claims 28-33 are directed to an allowable product. Pursuant to the procedures set forth in MPEP § 821.04(b), claims 11-21 & 23 are directed to the process of making or using the allowable product, previously withdrawn from consideration as a result of a restriction requirement, are hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Because a claimed invention previously withdrawn from consideration under 37 CFR 1.142 has been rejoined, **the restriction requirement has groups I and II as set forth in the Office action mailed on 12/06/2011 is hereby withdrawn**. In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present

application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Allowable Subject Matter

Claims 11 & 28 are allowed.

Claims 12 – 21, 23, & 28 - 33 are allowed by virtue of dependency on claims 11 and 28.

The following is a statement of reasons for the indication of allowable subject matter: Prior art of record does not explicitly disclose or render obvious "a second charge storing layer directly on the first charge storing layer comprising an oxygen-lean, silicon-rich and nitrogen-rich oxynitride in which a stoichiometric composition of the oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer results in it being trap dense" in combination of all other limitation of claims 11 & 28.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 1-571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/
/JULIO J. MALDONADO/

Supervisory Patent Examiner, Art Unit 2898

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 09/06/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 09/06/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	12/06/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

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HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

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IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001383

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
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Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 09/06/2013
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SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

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nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	12/06/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2898	257-411000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Sandisk Technologies, Inc. - Ex. 1002, Page 001384

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Sandisk Technologies, Inc. - Ex. 1002, Page 001385

UNITED STATES PATENT AND TRADEMARK OFFICE

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60909 7590 09/06/2013

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SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 09/06/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001386

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/007,533	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2898	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/29/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *11-21,23 and 28 - 33*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 07/29/2013
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/ Examiner, Art Unit 2898	/JULIO J. MALDONADO/ Supervisory Patent Examiner, Art Unit 2898

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 07/29/2013 has been entered.

Election/Restrictions

Claims 28-33 are directed to an allowable product. Pursuant to the procedures set forth in MPEP § 821.04(b), claims 11-21 & 23 are directed to the process of making or using the allowable product, previously withdrawn from consideration as a result of a restriction requirement, are hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Because a claimed invention previously withdrawn from consideration under 37 CFR 1.142 has been rejoined, **the restriction requirement has groups I and II as set forth in the Office action mailed on 12/06/2011 is hereby withdrawn**. In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are

advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Allowable Subject Matter

Claims 11 & 28 are allowed.

Claims 12 – 21, 23, & 28 - 33 are allowed by virtue of dependency on claims 11 and 28.

The following is a statement of reasons for the indication of allowable subject matter: Prior art of record does not explicitly disclose or render obvious "a second charge storing layer directly on the first charge storing layer comprising an oxygen-lean, silicon-rich and nitrogen-rich oxynitride in which a stoichiometric composition of the oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer results in it being trap dense" in combination of all other limitation of claims 11 & 28.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is

(571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

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/Mohammad Choudhry/
AU 2898
/JULIO J. MALDONADO/

Supervisory Patent Examiner, Art Unit 2898

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EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
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APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$0	$2070	02/27/2013

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HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

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Sandisk Technologies, Inc. - Ex. 1002, Page 001392

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Commissioner for Patents
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or Fax (571)-273-2885

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(Depositor's name)
(Signature)
(Date)

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1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Sandisk Technologies, Inc. - Ex. 1002, Page 001393

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

60909 7590 11/27/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 11/27/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

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PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001394

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	13/007,533	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2898	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/13/2012*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *11-21,23 and 28-33*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Shouxiang Hu/ Primary Examiner, Art Unit 2898	/MOHAMMAD CHOUDHRY/ Examiner, Art Unit 2898

Sandisk Technologies, Inc. - Ex. 1002, Page 001396

DETAILED ACTION

Election/Restrictions

Claims 28-33 are directed to an allowable product. Pursuant to the procedures set forth in MPEP § 821.04(b), claims 11-21 & 23 are directed to the process of making or using the allowable product, previously withdrawn from consideration as a result of a restriction requirement, are hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Because a claimed invention previously withdrawn from consideration under 37 CFR 1.142 has been rejoined, **the restriction requirement has groups I and II as set forth in the Office action mailed on 12/06/2011 is hereby withdrawn**. In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Allowable Subject Matter

Claims 11 & 28 are allowed.

Claims 12 – 21, 23, & 28 - 33 are allowed by virtue of dependency on claims 11 and 28.

The following is a statement of reasons for the indication of allowable subject matter: Prior art of record does not explicitly disclose or render obvious "a second charge storing layer directly on the first charge storing layer comprising an oxygen-lean, silicon-rich and nitrogen-rich oxynitride in which a stoichiometric composition of the oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer results in it being trap dense" in combination of all other limitation of claims 11 & 28.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 1-571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

/Shouxiang Hu/
Primary Examiner, Art Unit 2898

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 12/06/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 12/06/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	03/06/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001400

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 12/06/2013
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	03/06/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2898	257-411000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Sandisk Technologies, Inc. - Ex. 1002, Page 001401

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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Sandisk Technologies, Inc. - Ex. 1002, Page 001402

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

60909 7590 12/06/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 12/06/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

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PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001403

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notices of Allowance and Fee(s) Due mailed between October 1, 2013 and December 31, 2013

(Addendum to PTOL-85)

If the "Notice of Allowance and Fee(s) Due" has a mailing date on or after October 1, 2013 and before January 1, 2014, the following information is applicable to this application.

If the issue fee is being timely paid on or after January 1, 2014, the amount due is the issue fee and publication fee in effect January 1, 2014. On January 1, 2014, the issue fees set forth in 37 CFR 1.18 decrease significantly and the publication fee set forth in 37 CFR 1.18(d)(1) decreases to $0.

If an issue fee or publication fee has been previously paid in this application, applicant is not entitled to a refund of the difference between the amount paid and the amount in effect on January 1, 2014.

Notice of Allowability	Application No. 13/007,533	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2898	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/07/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *11-21,23 and 28-33*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/07/2013
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/SHOUXIANG HU/
Primary Examiner, Art Unit 2898

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 10/07/2013 has been entered.

Election/Restrictions

Claims 28-33 are directed to an allowable product. Pursuant to the procedures set forth in MPEP § 821.04(b), claims 11-21 & 23 are directed to the process of making or using the allowable product, previously withdrawn from consideration as a result of a restriction requirement, are hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Because a claimed invention previously withdrawn from consideration under 37 CFR 1.142 has been rejoined, **the restriction requirement has groups I and II as set forth in the Office action mailed on 12/06/2011 is hereby withdrawn**. In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are

advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Allowable Subject Matter

Claims 11 & 28 are allowed.

Claims 12 – 21, 23, & 28 - 33 are allowed by virtue of dependency on claims 11 and 28.

The following is a statement of reasons for the indication of allowable subject matter: Prior art of record does not explicitly disclose or render obvious "a second charge storing layer directly on the first charge storing layer comprising an oxygen-lean, silicon-rich and nitrogen-rich oxynitride in which a stoichiometric composition of the oxygen-lean, silicon-rich and nitrogen-rich oxynitride layer results in it being trap dense" in combination of all other limitation of claims 11 & 28.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is

(571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 1-571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mohammad Choudhry/
AU 2898

/Shouxiang Hu/
Primary Examiner, Art Unit 2898

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 01/15/2016

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/15/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	04/15/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001410

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 01/15/2016
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	04/15/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2816	257-299000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001411

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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60909 7590 01/15/2016

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/15/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001412

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/436,872	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

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1. ☒ This communication is responsive to *12/15/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *9-13*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

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1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/15/2015
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 09/15/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/15/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/15/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

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If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001415

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 09/15/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/15/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2816	257-299000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001416

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

60909 7590 09/15/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/15/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001417

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/436,872	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/20/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *9-13*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date *8/24/2015* .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/20/2015 has been entered.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with WILLIAM E. NUTTLE on 08/24/2015 & 09/08/2015.

Cancel claims 1- 8 & 21.

Amendments to the Specification:

Please amend the Specification as follows:

[0022] FIG. 11A ~~and 11B~~ through 11F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 10A; and

[0023] FIG. 12A ~~and 12B~~ through 12F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 10A.

[0085] Referring to FIG. 12A, in a gate last scheme a dielectric layer 1202, such as an oxide, is formed over a sacrificial layer 1204 on a surface on a substrate 1206, an opening etched through the dielectric and sacrificial layers and a vertical channel 1208 formed therein. As with embodiments described above, the vertical channel 1208 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material 1210, such as polycrystalline or monocrystalline silicon, or can include a separate, layer semiconducting material surrounding a cylinder of dielectric filler material (not shown). The dielectric layer 1202 can include any suitable dielectric material, such as a silicon oxide, capable of electrically isolating the subsequently formed gate layer of the memory device 1000 from an overlying electrically active layer or another memory device. The sacrificial layer 1204 can include any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 1202, substrate 1206 and vertical channel 1208.

[0085] Next, a gate layer 1222 is deposited into the second opening 1212 and the surface of the upper dielectric layer 1202 planarized to yield the intermediate structure illustrated in FIG. 12E. As with embodiments described above, the gate layer 1222 can include a metal deposited or a doped polysilicon. Finally, an opening 1224 is etched

through the gate layer 1222 to form control gate of separate memory devices 1226 as illustrated in FIG. 12F.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 1-571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOHAMMAD CHOUDHRY/

Primary Examiner, Art Unit 2816

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 06/01/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/01/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/917,500	06/13/2013	Sagy Charel Levy	PM07002C1	1009

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	09/01/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

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Sandisk Technologies, Inc. - Ex. 1002, Page 001424

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 06/01/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/917,500	06/13/2013	Sagy Charel Levy	PM07002C1	1009

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	09/01/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2816	438-261000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
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2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
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4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001425

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/917,500	06/13/2013	Sagy Charel Levy	PM07002C1	1009

60909 7590 06/01/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/01/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001426

Notice Requiring Inventor's Oath or Declaration	Application No. 13/917,500	Applicant(s) Sagy Charel Levy	
	Examiner CHOUDHRY, MOHAMMAD M	Art Unit 2816	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) MUST be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

- A properly executed inventor's oath or declaration has not been received for the following inventor(s): **Sagy Charel Levy**, **Krishnaswamy Ramkumar**, **Fredrick B. Jenne**, and **Sam G. Geha**.
  Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/917,500	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *01/27/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *21-27, 30-39*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 09/14/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/14/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/917,500	06/13/2013	Sagy Charel Levy	PM07002C1	1009

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/14/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001430

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 09/14/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/917,500	06/13/2013	Sagy Charel Levy	PM07002C1	1009

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/14/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2816	438-261000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001431

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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60909 7590 09/14/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
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EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
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Sandisk Technologies, Inc. - Ex. 1002, Page 001432

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Notice of Allowability	Application No. 13/917,500	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

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3. ☒ The allowed claim(s) is/are *21-27,30-39*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
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5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/01/2015
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 12/31/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/31/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/917,500	06/13/2013	Sagy Charel Levy	PM07002C1	1009

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	03/31/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001435

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 12/31/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/917,500	06/13/2013	Sagy Charel Levy	PM07002C1	1009

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	03/31/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2816	438-261000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001436

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/917,500	06/13/2013	Sagy Charel Levy	PM07002C1	1009

60909 7590 12/31/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/31/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001437

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/917,500	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/14/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *21-27,30-39*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/14/2015
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5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

Sandisk Technologies, Inc. - Ex. 1002, Page 001439

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 09/04/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/04/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/172,775	02/04/2014	Sagy Charel Levy	PM07002CIP1C1	8762

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/04/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

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HOW TO REPLY TO THIS NOTICE:

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If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

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Sandisk Technologies, Inc. - Ex. 1002, Page 001440

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 09/04/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

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Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/172,775	02/04/2014	Sagy Charel Levy	PM07002CIP1C1	8762

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/04/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2816	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
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1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
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Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001441

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/172,775	02/04/2014	Sagy Charel Levy	PM07002CIP1C1	8762

60909 7590 09/04/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/04/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001442

Notice Requiring Inventor's Oath or Declaration	Application No. 14/172,775	Applicant(s) Sagy Charel Levy	
	Examiner CHOUDHRY, MOHAMMAD M	Art Unit 2816	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) MUST be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

- A properly executed inventor's oath or declaration has not been received for the following inventor(s): **Sagy Charel Levy**, **Krishnaswamy Ramkumar**, **Frederick B. Jenne**, and **Sam G. Geha**.
  Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	14/172,775	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2816	

All participants (applicant, applicant's representative, PTO personnel):

(1) *MOHAMMAD CHOUDHRY*. (3)_____.

(2) *WILLIAM E. NUTTLE*. (4)_____.

Date of Interview: *27 August 2015*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☐ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☒103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *35-40*.

Identification of prior art discussed: _____.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Product claims discussed and amendment made. Applicant representative agreed to cancel claims 35 -40..

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/MOHAMMAD CHOUDHRY/ Primary Examiner, Art Unit 2816	

Notice of Allowability	Application No. 14/172,775	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *08/13/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *25-28,32-34*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date *08/27/2015* .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 12/18/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/18/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/172,775	02/04/2014	Sagy Charel Levy	PM07002CIP1C1	8762

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	03/18/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001447

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 12/18/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/172,775	02/04/2014	Sagy Charel Levy	PM07002CIP1C1	8762

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	03/18/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2816	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001448

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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EXAMINER	
CHOUDHRY, MOHAMMAD M	
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Sandisk Technologies, Inc. - Ex. 1002, Page 001449

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Notice of Allowability	Application No. 14/172,775	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/08/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *25-28,32-34*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 12/04/2015 & 12/08/2015.

Sandisk Technologies, Inc. - Ex. 1002, Page 001452

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 05/11/2016

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/11/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	08/11/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001453

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 05/11/2016
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

TITLE OF INVENTION: OXIDE-NITRIDE-OXIDE STACK HAVING MULTIPLE OXYNITRIDE LAYERS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	08/11/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOUDHRY, MOHAMMAD M	2816	257-299000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001454

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/436,872	03/31/2012	Sagy Levy	PM07002CIP2	6019

60909 7590 05/11/2016

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/11/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001455

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/436,872	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/15/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *9-13*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 04/15/2016
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/007,533	01/14/2011	Sagy Levy	PM07002CIP1	6897

60909 7590 12/06/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	
ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
12/06/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	13/007,533	LEVY ET AL.	
	Examiner	Art Unit	
	MOHAMMAD CHOUDHRY	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2011*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-23* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-23* are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-10 drawn to a device, classified in class 257, subclass 411+.

Group II. Claims, 11-23 drawn to process, classified in class 438, subclass 791+.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, Product as claimed in claim 1 and 6 having a blocking oxide layer can be formed by selective deposition or patterning a conformal layer method which is another and materially different process.

3. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

4. The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during

prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder**. Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday - Thursday 10:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 1-571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/197,466	08/25/2008	Krishnaswamy Ramkumar	PM07024C1	2398

60909 7590 03/11/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2893	

MAIL DATE	DELIVERY MODE
03/11/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/197,466	RAMKUMAR ET AL.	
	Examiner	Art Unit	
	THANH T. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2008*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-19* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

This application contains claims directed to the following patentably distinct species:

I- specie 1, referring to figures 5-6.

II- specie 2, referring to figures 7a-7b.

The species are independent or distinct because specie I and II are belongs to different embodiment. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, none is generic.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s) apply:

- *the inventions have acquired a separate status in the art in view of their different classification*
- *the inventions have acquired a separate status in the art due to their recognized divergent subject matter*
- *the inventions require a different field of search (e.g., searching different classes /subclasses or electronic resources, or employing different search strategies or search queries).*

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or a grouping of patentably indistinct species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species**,

including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the

application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau, can be reached on (571) 272-1945. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/

Primary Examiner, Art Unit 2893

Electronic Acknowledgement Receipt

EFS ID:	29020764
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	25-APR-2017
Filing Date:	26-OCT-2016
Time Stamp:	14:10:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C3_IDS_OAs_04212017.pdf	1054966 e3f9772ad7158bb537e4d1c9fffd49af7aa6cd0c	no	8

Warnings:

Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Non Patent Literature	PM07002CIP1JP_JPOfficeAction_08042015.pdf	420560 cb0cf397ff77a67f82742a10267d26121bcc3ce5	no	8
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3	Non Patent Literature	PM07002CIP2JP_JPOfficeAction2_02212017.pdf	187205 341ad4bddc2de6f97b08bc621a6391cdda65e735	no	1
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4	Non Patent Literature	PM07002CN_OA_01212015.pdf	2884742 70077ab8706e30959635b32526c37d66239bc3a5	no	6
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5	Non Patent Literature	PM07002CN_OA_02032016.pdf	77681 129eb14eceede727e463c999ea844af1f0ba1a3a	no	2
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6	Non Patent Literature	PM07002CN_OA_07292014.pdf	2779185 c0d506f35f57ca4063d366710045e2f53c611021	no	5
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7	Non Patent Literature	PM07002CN_OA_07302015.pdf	1039964 deab894b0e9b68911557cf8278028dae31f19407	no	3
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8	Non Patent Literature	PM07002CN_OA_10222013.pdf	110268 ad77ef02dd48c7c91d79ce7a8c38c74415ba443e	no	4
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9	Non Patent Literature	PM07002CIP1CN_OA_04012015.pdf	420734 93b611e7cf2ce16d51a5ddb050ecf8cfc4a10052	no	5
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10	Non Patent Literature	PM07002CIP1CN_OA_05122016.pdf	185689 813284cb1d18fb773cf0d5a4bfc9df76942758ad	no	5
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11	Non Patent Literature	PM07002CIP1CN_OA_07252014.pdf	2136461 0d782b8e9c6b4e8f9cda0390b17b5a5bf33948ee	no	4
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12	Non Patent Literature	PM07002CIP1CN_OA_10092015.pdf	82770 3c7e6af45d2168c342e88b178d8dd4353d1330d8	no	3
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13	Non Patent Literature	PM07002CIP1CN_SIPOOA_11292016.pdf	237557 e048f18291fb7fc81ac3792b825792e5fddc9344	no	5
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14	Non Patent Literature	PM07002CIP2CN_SIPOOA_09012016.pdf	8475233 1b6135264fb6ebdf88ad81ea1f6a91f1499fdd5c	no	7
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15	Non Patent Literature	PM07002CIP2TW_TIPOOA_11182016.pdf	344843 4416aa90da040303f224e5662a0c4d894b5489d2	no	10
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16	Non Patent Literature	PM07002CIP1TW_OA_10152015.pdf	72404 4420da833a4592fffecd59a9aeb630f1bccb05f3	no	4
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17	Non Patent Literature	PM07002_AdvisoryAction_03162010.pdf	134843 661b799ddf827e6807b6dd5382bfc1b088b1dc5b	no	4
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18	Non Patent Literature	PM07002_AdvisoryAction_04202010.pdf	213673 59e1a2467d84b7e8086be49e9cda408aa277e1c5	no	6
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19	Non Patent Literature	PM07002_AdvisoryAction_05142013.pdf	155112 dce47af70af7c5ef6734fe3071d6f5d18ee656ed	no	4
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22	Non Patent Literature	PM07002_FinalRejection_01062010.pdf	611597 b927571cc22f3c8839ccc1ad6052842b5b406c87	no	17
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23	Non Patent Literature	PM07002_FinalRejection_03132013.pdf	827023 275d8bd894c0ff119e06fe3db887f22b1e99db61	no	22
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24	Non Patent Literature	PM07002_FinalRejection_03152011.pdf	487472 bd6621cf0f77ca2510ed1cd56e54a1bfea46efbb	no	13
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25	Non Patent Literature	PM07002CIP1_FinalRejection_09242012.pdf	477589 ea8806d08b48284b074fdb8325e0e842e1b2233d	no	13
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26	Non Patent Literature	PM07002CIP2_FinalRejection_05272015.pdf	483593 8bd4fd5aed336767faa43327240638209dbad543	no	14
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32	Non Patent Literature	PM07002CIP2_NonFinalRejection_12192014.pdf	545131 3a29c8a070eb7a415356d32e98a28e193633cac9	no	15
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33	Non Patent Literature	PM07002C1_NonFinalRejection_01052015.pdf	490332 b8f6e6d860b1d3158d31a20e23d90738d466d86a	no	13
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34	Non Patent Literature	PM07002CIP1C1_NonFinalRejection_06222015.pdf	478493 f08eaec8263bb9400004f3950f3d7ad6ef2f0b78	no	14
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35	Non Patent Literature	PM07002CIP1_NOA_03072013.pdf	408418 f145f44e32f8333f22b0c68479e999a23fc1fbe7	no	8
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36	Non Patent Literature	PM07002CIP1_NOA_06182013.pdf	433082 95d6cbd1e5485b64b3465b83d8075fc10157064d	no	9
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43	Non Patent Literature	PM07002C1_NOA_09142015.pdf	357371 7e78f9ab7797c878aa7c6af7d4184a348702b981	no	5
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44	Non Patent Literature	PM07002C1_NOA_12312015.pdf	357282 891b03777406a45092a7f6ecee7059e2b7bcd434	no	5
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45	Non Patent Literature	PM07002CIP1C1_NOA_09042015.pdf	427236 3f9261ad98c2cda9685f6d277832a323a2564fb7	no	7
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46	Non Patent Literature	PM07002CIP1C1_NOA_12182015.pdf	361683 e0f3e5c5c098c94e88b1c33ad862b129756cd532	no	6
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Information:					
47	Non Patent Literature	PM07002CIP2_NOA_05112016.pdf	357052 1e7f63902f1993f58105ffc0cb3b8836fd9440e1	no	5
Warnings:					
Information:					
48	Non Patent Literature	PM07002CIP1_RestrictionRequirement_12062011.pdf	228720 986407cc26702f291b947149c40fc2ce3b5dccba	no	7
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Information:					
49	Non Patent Literature	PM07024C1_Restriction_03112011.pdf	185158 30e3d735b9fb9b0ee3529d1d54b3fee173ef38b5	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	33853408		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Sandisk Technologies, Inc. - Ex. 1002, Page 001479

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	1	"3.3V 64K x 18 Synchronous QuadPort Static RAM," Cypress Preliminary CY7C0430BV, Cypress Semiconductor Corporation, 03/27/2001; 36 pages	
	2	Hua-Ching Chien, Chin-Hsing Kao, Jui-Wen Chang and Tzung-Kuen Tsai_Two-bit SONOS type Flash using a band engineering in the nitride layer_Dated June 17, 2005_4 pages	
	3	Hung et al., High-performance gate-all-around polycrystalline silicon nanowire with silicon nanocrystals nonvolatile memory, Appl. Phys. Lett, 98 162108 (2011), pub date: 4/22/2011	
	4	Krishnaswamy Ramkumar_Cypress SONOS Technology_Dated July 6, 2011_9 pages	
	5	USPTO Notice Of Allowance for Application Number 13/539,466 (PM07027D1CIP1) dated 11/13/2013; 9 pages	
	6	USPTO Notice of Allowance for Application Number 13/539,466 (PM07027D1CIP1) dated 11/27/2012; 8 pages	
	7	USPTO Notice of Allowance for Application Number 13/620,071 (PM07024C2) dated 01/23/2015; 5 pages	
	8	USPTO Notice of Allowance for Application Number 13/620,071 (PM07024C2) dated 10/27/2014; 7 pages	
	9	USPTO Notice of Allowance for Application Number 14/159,315 (PM07027D1CIP1C1) dated 02/18/2015; 9 pages	
	10	USPTO Notice of Allowance for Application Number 14/159,315 (PM07027D1CIP1C1) dated 03/23/2015; 9 pages	
	11	USPTO Notice of Allowance for Application Number 14/307,858 (PM07027D1C1) dated 11/27/2015; 5 pages	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	12	USPTO Notice of Allowance for Application Number 14/811,346 (PM07027D1CIP1C2) dated 07/19/2016; 7 pages	
	13	USPTO Requirement for Restriction for Application Number 12/152,518 (PM07027) dated 06/09/2010; 5 pages	
	14	USPTO Requirement for Restriction for Application Number 14/307,858 (PM07027D1C1) dated 05/18/2015; 7 pages	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kin Hung Lai/	Date (YYYY-MM-DD)	2017-04-24
Name/Print	Kin Hung Lai	Registration Number	69251

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PRELIMINARY

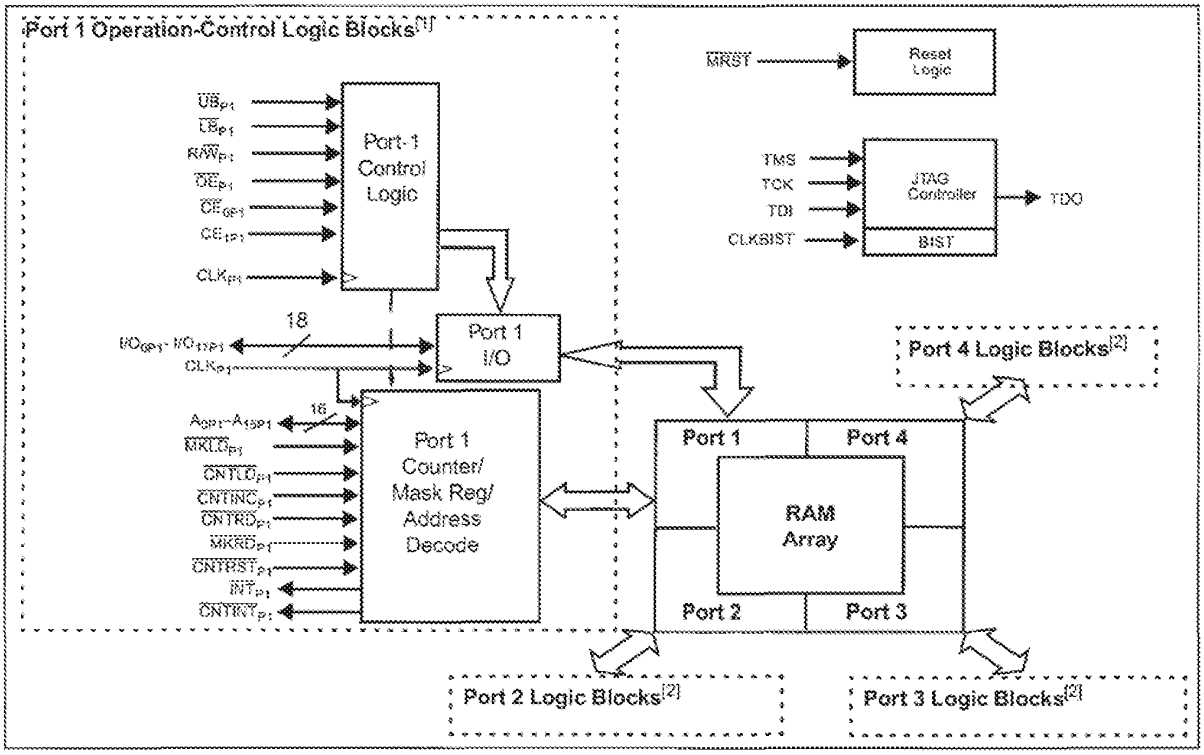
CY7C0430BV

3.3V 64K x 18 Synchronous QuadPort™ Static RAM

Features

- True four-ported memory cells which allow simultaneous access of the same memory location
- Synchronous Pipelined device
  - 64K x 18 organization
- Pipelined output mode allows fast 133-MHz operation
- High Bandwidth up to 10 Gbps (133 MHz x 18 bits wide x 4 ports)
- 0.25-micron CMOS for optimum speed/power
- High-speed clock to data access 4.7 ns (max.)
- 3.3V Low operating power
  - Active = 750 mA (maximum)
  - Standby = 5 mA (maximum)
- Counter wrap-around control
  - Internal mask register controls counter wrap-around
  - Counter-Interrupt flags to indicate wrap-around
- Counter readback on address lines
- Mask register readback on address lines
- Interrupt flags for message passing
- Master reset for all ports
- Width and depth expansion capabilities
- Dual Chip Enables on all ports for easy depth expansion
- Separate upper-byte and lower-byte controls on all ports
- 272-BGA package (27 mm x 27 mm 1.27-mm ball pitch)
- Commercial and Industrial temperature ranges
- IEEE 1149.1 JTAG boundary scan
- BIST (Built In Self Test) controller

Top Level Logic Block Diagram



QuadPort is a trademark of Cypress Semiconductor Corporation.

Notes:
1. Port 1 Control Logic Block is detailed on page 2.
2. Port 2, Port 3, and Port 4 Logic Blocks are similar to Port 1 Logic Blocks.

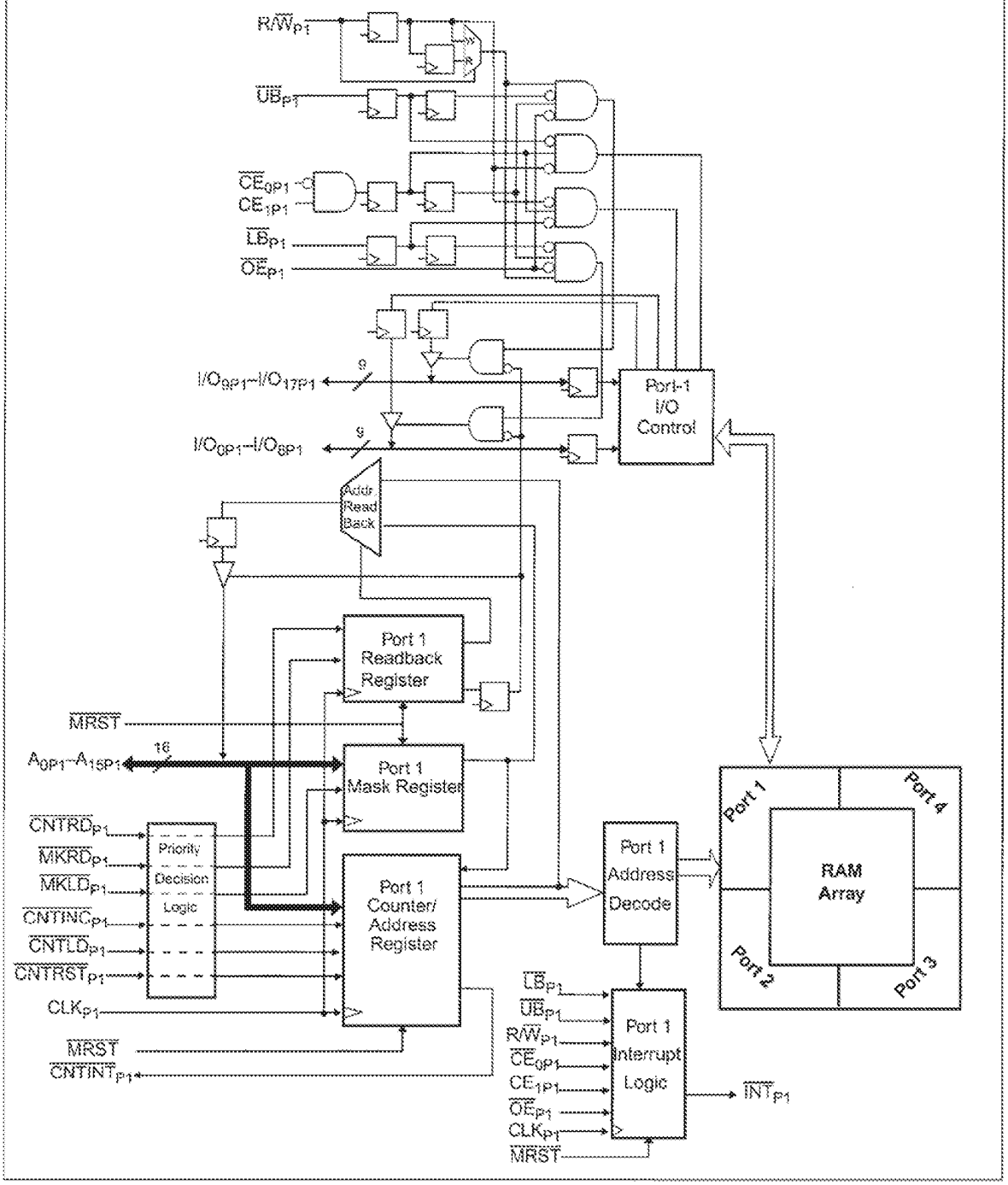
For the most recent information, visit the Cypress web site at www.cypress.com

Cypress Semiconductor Corporation • 3901 North First Street • San Jose • CA 95134 • 408-943-2600
March 27, 2001

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Port 1 Operation-Control Logic Block Diagram:

(Address Readback is independent of CEs)



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Functional Description

The CY7C0430BV is a 1-Mb synchronous true four-port Static RAM. This is a high-speed, low-power 3.3V CMOS four-port static RAM. Four ports are provided, permitting independent, simultaneous access for reads from any location in memory. Any port can write to a certain location while other ports are reading that location simultaneously, if the timing spec for port to port delay (t_{CCS}) is met. The result of writing to the same location by more than one port at the same time is undefined. Registers on control, address and data lines allow for minimal set-up and hold time.

Data is registered for decreased cycle time. Clock to data valid t_{CD2} = 4.7 ns. Each port contains a burst counter on the input address register. After externally loading the counter with the initial address the counter will self-increment the address internally (more details to follow). The internal write pulse width is independent of the duration of the R/$\overline{W}$ input signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE}_0$ or LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce the static power consumption. One cycle is required with chip enables asserted to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with an external address when the port's Counter Load pin ($\overline{CNTLD}$) is asserted LOW. When the port's Counter Increment pin ($\overline{CNTINC}$) is asserted, the address counter will increment on each subsequent LOW-to-HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until $\overline{CNTINC}$ is deasserted. The counter can address the entire memory array and will loop back to the start. Counter Reset ($\overline{CNTRST}$) is used to reset the burst counter. A counter-mask register is used to control the counter wrap. The counter and mask register operations are described in more details in the following sections.

The counter or mask register values can be read back on the bidirectional address lines by activating $\overline{MKRD}$ or $\overline{CNTRD}$ respectively.

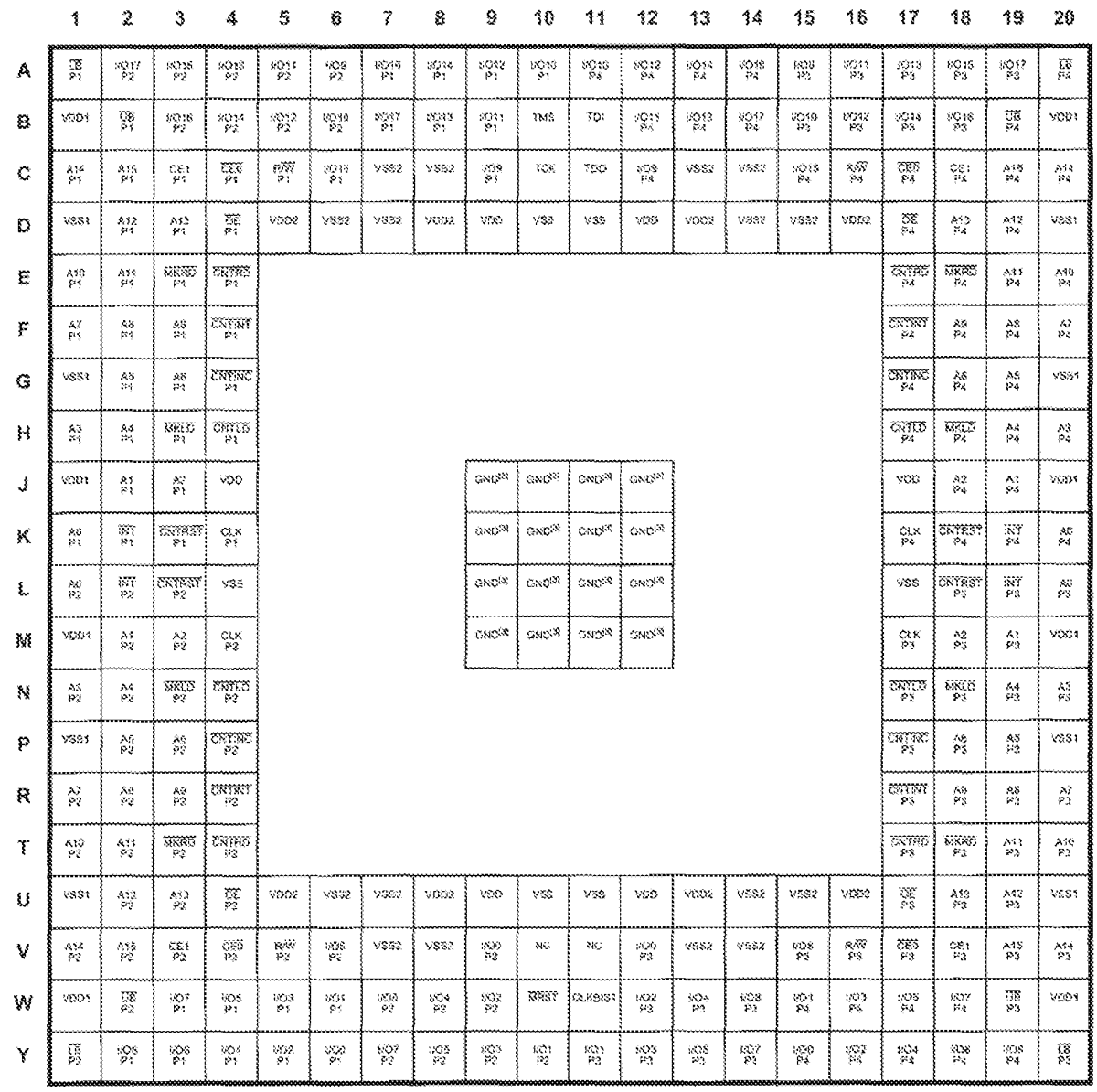
The new features added to the QuadPort™ as compared to standard synchronous dual-ports include: readback of burst-counter internal address value on address lines, counter-mask registers to control the counter wrap-around, readback of mask register value on address lines, interrupt flags for message passing, BIST, JTAG for boundary scan, and asynchronous Master Reset.

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Pin Configuration

272-Ball Grid Array (BGA)

Top View



Note:
3. Central Leads are for thermal dissipation only. They are connected to device V_{SS}.

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Selection Guide

	CY7C0430BV -133	CY7C0430BV -100
f_{MAX2} (MHz)	133	100
Max Access Time (ns) (Clock to Data)	4.7	5.0
Max Operating Current I_{CC} (mA)	750	600
Max Standby Current for I_{SB1} (mA) (All ports TTL Level)	200	150
Max Standby Current for I_{SB3} (mA) (All ports CMOS Level)	5.0	5.0

Pin Definitions

Port 1	Port 2	Port 3	Port 4	Description
A_{0P1}–A_{15P1}	A_{0P2}–A_{15P2}	A_{0P3}–A_{15P3}	A_{0P4}–A_{15P4}	Address Input/Output.
I/O_{0P1}–I/O_{17P1}	I/O_{0P2}–I/O_{17P2}	I/O_{0P3}–I/O_{17P3}	I/O_{0P4}–I/O_{17P4}	Data Bus Input/Output.
CLK_{P1}	CLK_{P2}	CLK_{P3}	CLK_{P4}	Clock Input. This input can be free running or strobed. Maximum clock input rate is f_{MAX}.
$\overline{LB}_{P1}$	$\overline{LB}_{P2}$	$\overline{LB}_{P3}$	$\overline{LB}_{P4}$	Lower Byte Select Input. Asserting this signal LOW enables read and write operations to the lower byte. For read operations both the $\overline{LB}$ and $\overline{OE}$ signals must be asserted to drive output data on the lower byte of the data pins.
$\overline{UB}_{P1}$	$\overline{UB}_{P2}$	$\overline{UB}_{P3}$	$\overline{UB}_{P4}$	Upper Byte Select Input. Same function as $\overline{LB}$, but to the upper byte.
$\overline{CE}_{0P1}$,CE_{1P1}	$\overline{CE}_{0P2}$,CE_{1P2}	$\overline{CE}_{0P3}$,CE_{1P3}	$\overline{CE}_{0P4}$,CE_{1P4}	Chip Enable Input. To select any port, both $\overline{CE}_0$ AND CE_1 must be asserted to their active states ($\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$).
$\overline{OE}_{P1}$	$\overline{OE}_{P2}$	$\overline{OE}_{P3}$	$\overline{OE}_{P4}$	Output Enable Input. This signal must be asserted LOW to enable the I/O data lines during read operations. $\overline{OE}$ is asynchronous input.
$R/\overline{W}_{P1}$	$R/\overline{W}_{P2}$	$R/\overline{W}_{P3}$	$R/\overline{W}_{P4}$	Read/Write Enable Input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
$\overline{MRST}$				Master Reset Input. This is one signal for All Ports. $\overline{MRST}$ is an asynchronous input. Asserting $\overline{MRST}$ LOW performs all of the reset functions as described in the text. A $\overline{MRST}$ operation is required at power-up.
$\overline{CNTRST}_{P1}$	$\overline{CNTRST}_{P2}$	$\overline{CNTRST}_{P3}$	$\overline{CNTRST}_{P4}$	Counter Reset Input. Asserting this signal LOW resets the burst address counter of its respective port to zero. $\overline{CNTRST}$ is second to $\overline{MRST}$ in priority with respect to counter and mask register operations.
$\overline{MKLD}_{P1}$	$\overline{MKLD}_{P2}$	$\overline{MKLD}_{P3}$	$\overline{MKLD}_{P4}$	Mask Register Load input. Asserting this signal LOW loads the mask register with the external address available on the address lines. $\overline{MKLD}$ operation has higher priority over $\overline{CNTLD}$ operation.
$\overline{CNTLD}_{P1}$	$\overline{CNTLD}_{P2}$	$\overline{CNTLD}_{P3}$	$\overline{CNTLD}_{P4}$	Counter Load Input. Asserting this signal LOW loads the burst counter with the external address present on the address pins.
$\overline{CNTINC}_{P1}$	$\overline{CNTINC}_{P2}$	$\overline{CNTINC}_{P3}$	$\overline{CNTINC}_{P4}$	Counter Increment Input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK.

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Pin Definitions (continued)

Port 1	Port 2	Port 3	Port 4	Description
$\overline{CNTRD}_{P1}$	$\overline{CNTRD}_{P2}$	$\overline{CNTRD}_{P3}$	$\overline{CNTRD}_{P4}$	Counter Readback Input. When asserted LOW, the internal address value of the counter will be read back on the address lines. During $\overline{CNTRD}$ operation, both $\overline{CNTLD}$ and $\overline{CNTINC}$ must be HIGH. Counter readback operation has higher priority over mask register readback operation. Counter readback operation is independent of port chip enables. If address readback operation occurs with chip enables active ($\overline{CE}_0$ = LOW, CE_1 = HIGH), the data lines (I/Os) will be three-stated. The readback timing will be valid after one no-operation cycle plus t_{CD2} from the rising edge of the next cycle.
$\overline{MKRD}_{P1}$	$\overline{MKRD}_{P2}$	$\overline{MKRD}_{P3}$	$\overline{MKRD}_{P4}$	Mask Register Readback Input. When asserted LOW, the value of the mask register will be readback on address lines. During mask register readback operation, all counter and $\overline{MKLD}$ inputs must be HIGH (see Counter and Mask Register Operations truth table). Mask register readback operation is independent of port chip enables. If address readback operation occurs with chip enables active ($\overline{CE}_0$ = LOW, CE_1 = HIGH), the data lines (I/Os) will be three-stated. The readback will be valid after one no-operation cycle plus t_{CD2} from the rising edge of the next cycle.
$\overline{CNTINT}_{P1}$	$\overline{CNTINT}_{P2}$	$\overline{CNTINT}_{P3}$	$\overline{CNTINT}_{P4}$	Counter Interrupt flag output. Flag is asserted LOW for one clock cycle when the counter wraps around to location zero.
$\overline{INT}_{P1}$	$\overline{INT}_{P2}$	$\overline{INT}_{P3}$	$\overline{INT}_{P4}$	Interrupt flag output. Interrupt permits communications between all four ports. The upper four memory locations can be used for message passing. Example of operation: $\overline{INT}_{P4}$ is asserted LOW when another port writes to the mailbox location of Port 4. Flag is cleared when Port 4 reads the contents of its mailbox. The same operation is applicable to Ports 1, 2, and 3.
TMS				JTAG Test Mode Select Input. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK.
TCK				JTAG Test Clock Input. This can be CLK of any port or an external clock connected to the JTAG TAP.
TDI				JTAG Test Data Input. This is the only data input. TDI inputs will shift data serially in to the selected register.
TDO				JTAG Test Data Output. This is the only data output. TDO transitions occur on the falling edge of TCK. TDO normally three-stated except when captured data is shifted out of the JTAG TAP.
CLKBIST				BIST Clock Input.
GND				Thermal ground for heat dissipation.
V_{SS}				Ground Input.
V_{DD}				Power Input.
V_{SS1}				Address lines ground Input.
V_{DD1}				Address lines power Input.
V_{SS2}				Data lines ground Input.
V_{DD2}				Data lines power Input.

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.5V to + 4.6V

DC Voltage Applied to Outputs in High Z State..... –0.5V to V_{CC}+0.5V

DC Input Voltage ..... –0.5V to V_{CC}+0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >1100V

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	3.3V ± 150 mV
Industrial	–40°C to +85°C	3.3V ± 150 mV

Electrical Characteristics Over the Operating Range

Parameter	Description		CY7C0430BV -133 Min.	-133 Typ.	-133 Max.	-100 Min.	-100 Typ.	-100 Max.	Unit
V_{OH}	Output HIGH Voltage (V_{CC} = Min., I_{OH} = –4.0 mA)		2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{CC} = Min., I_{OH} = +4.0 mA)				0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.0			2.0			V
V_{IL}	Input LOW Voltage				0.8			0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA) Outputs Disabled, $\overline{CE}$ = V_{IL}, f = f_{max}	Indust.		413	750		330	600	mA
		Com'l.							mA
I_{SB1}	Standby Current (4 Ports toggling at TTL Levels,0 active) $\overline{CE}_{1-4} \geq V_{IH}$, f = f_{MAX}	Indust.		80	200		60	150	mA
		Com'l.							mA
I_{SB2}	Standby Current (4 Ports toggling at TTL Levels, 1 active) $\overline{CE}_1$ | $\overline{CE}_2$ | $\overline{CE}_3$ | $\overline{CE}_4 \leq V_{IL}$, f = f_{MAX}	Indust.		170	349		128	263	mA
		Com'l.							mA
I_{SB3}	Standby Current (4 Ports CMOS Level, 0 active) $\overline{CE}_{1-4} \geq V_{IH}$, f = 0	Indust.		1.5	5		1.5	5	mA
		Com'l.							µA
I_{SB4}	Standby Current (4 Ports CMOS Level, 1 active and toggling) $\overline{CE}_1$ | $\overline{CE}_2$ | $\overline{CE}_3$ | $\overline{CE}_4 \leq V_{IL}$, f = f_{MAX}	Indust.		110	240		83	180	mA
		Com'l.							mA

JTAG TAP Electrical Characteristics Over the Operating Range

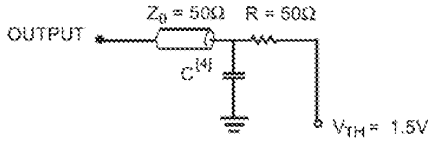
Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA	2.4		V
V_{OL1}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_X	Input Leakage Current	GND ≤ V_I ≤ V_{DD}	–100	100	µA

Capacitance

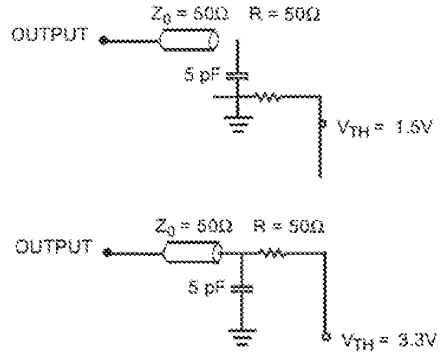
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	Output Capacitance		8	pF

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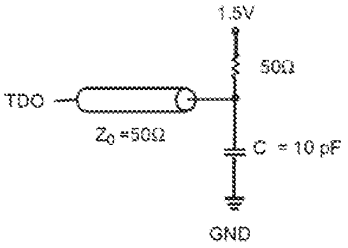
AC Test Load



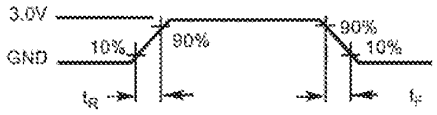
(a) Normal Load



(b) Three-State Delay



(c) TAP Load



ALL INPUT PULSES

Note:
4. Test Conditions: C = 10 pF.

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Switching Characteristics Over the Industrial Operating Range [7]

Parameter	Description	CY7C0430BV				Unit
		-133		-100		
		Min.	Max.	Min.	Max.	
f_{MAX2}	Maximum Frequency		133		100	MHz
t_{CYC2}	Clock Cycle Time	7.5		10		ns
t_{CH2}	Clock HIGH Time	3		4		ns
t_{CL2}	Clock LOW Time	3		4		ns
t_R	Clock Rise Time		2		3	ns
t_F	Clock Fall Time		2		3	ns
t_{SA}	Address Set-up Time	2.3		3		ns
t_{HA}	Address Hold Time	0.7		0.7		ns
t_{SC}	Chip Enable Set-up Time	2.3		3		ns
t_{HC}	Chip Enable Hold Time	0.7		0.7		ns
t_{SW}	R/$\overline{W}$ Set-up Time	2.3		3		ns
t_{HW}	R/$\overline{W}$ Hold Time	0.7		0.7		ns
t_{SD}	Input Data Set-up Time	2.3		3		ns
t_{HD}	Input Data Hold Time	0.7		0.7		ns
t_{SB}	Byte Set-up Time	2.3		3		ns
t_{HB}	Byte Hold Time	0.7		0.7		ns
t_{SCLD}	$\overline{CNTLD}$ Set-up Time	2.3		3		ns
t_{HCLD}	$\overline{CNTLD}$ Hold Time	0.7		0.7		ns
t_{SCINC}	$\overline{CNTINC}$ Set-up Time	2.3		3		ns
t_{HCINC}	$\overline{CNTINC}$ Hold Time	0.7		0.7		ns
t_{SCRST}	$\overline{CNTRST}$ Set-up Time	2.3		3		ns
t_{HCRST}	$\overline{CNTRST}$ Hold Time	0.7		0.7		ns
t_{SCRD}	$\overline{CNTRD}$ Set-up Time	2.3		3		ns
t_{HCRD}	$\overline{CNTRD}$ Hold Time	0.7		0.7		ns
t_{SMLD}	$\overline{MKLD}$ Set-up Time	2.3		3		ns
t_{HMLD}	$\overline{MKLD}$ Hold Time	0.7		0.7		ns
t_{SMRD}	$\overline{MKRD}$ Set-up Time	2.3		3		ns
t_{HMRD}	$\overline{MKRD}$ Hold Time	0.7		0.7		ns
t_{OE}	Output Enable to Data Valid		6.5		8	ns
t_{OLZ} [5]	$\overline{OE}$ to LOW Z	1		1		ns
t_{OHZ} [5]	$\overline{OE}$ to HIGH Z	1	6	1	7	ns
t_{CD2}	Clock to Data Valid		4.7		5	ns
t_{CA2}	Clock to Counter Address Readback Valid		4.7		5	ns
t_{CM2}	Clock to Mask Register Readback Valid		4.7		5	ns
t_{DC}	Data Output Hold After Clock HIGH	1		1		ns
t_{CKHZ} [6]	Clock HIGH to Output High Z	1	4.8	1	6.8	ns
t_{CKLZ} [6]	Clock HIGH to Output LOW Z	1		1		ns

Note:
5. This parameter is guaranteed by design, but it is not production tested.
6. Valid for both address and data outputs.

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Switching Characteristics Over the Industrial Operating Range (continued)[7]

Parameter	Description	CY7C0430BV				Unit
		-133		-100		
		Min.	Max.	Min.	Max.	
t_{SINT}	Clock to $\overline{INT}$ Set Time	1	7.5	1	10	ns
t_{RINT}	Clock to $\overline{INT}$ Reset Time	1	7.5	1	10	ns
t_{SCINT}	Clock to $\overline{CNTINT}$ Set Time	1	7.5	1	10	ns
t_{RCINT}	Clock to $\overline{CNTINT}$ Reset Time	1	7.5	1	10	ns
Master Reset Timing						
t_{RS}	Master Reset Pulse Width	7.5		10		ns
t_{RSR}	Master Reset Recovery Time	7.5		10		ns
t_{ROF}	Master Reset to Output Flags Reset Time		6.5		8	ns
Port to Port Delays						
t_{CCS}[7]	Clock to Clock Set-up Time (time required after a write before you can read the same address location)	6.5		9		ns

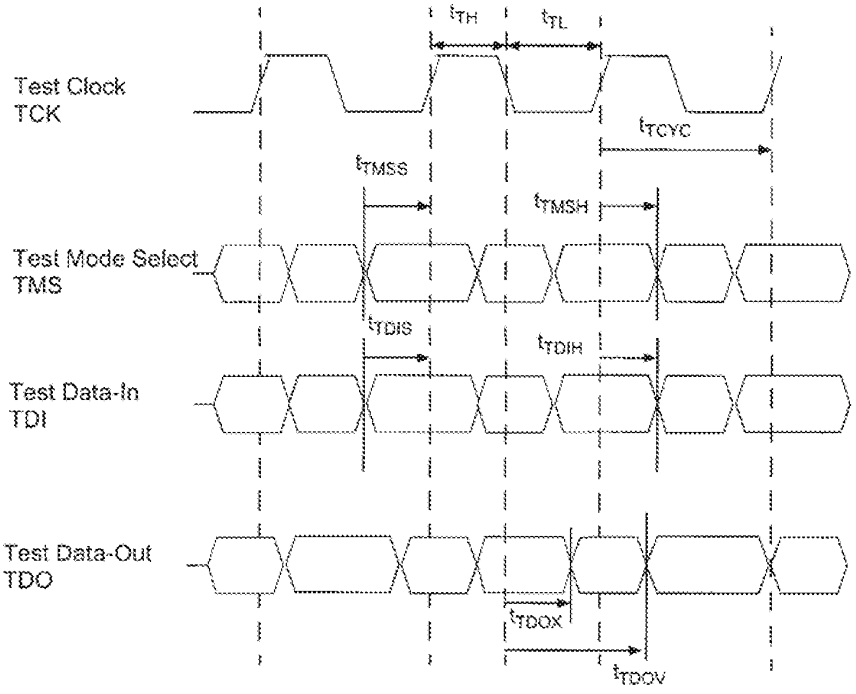
Note:

7. If data is simultaneously written and read to the same address location and t_{CCS} is violated, the data read from the address, as well as the subsequent data remaining in the address is undefined.

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JTAG Timing and Switching Waveforms

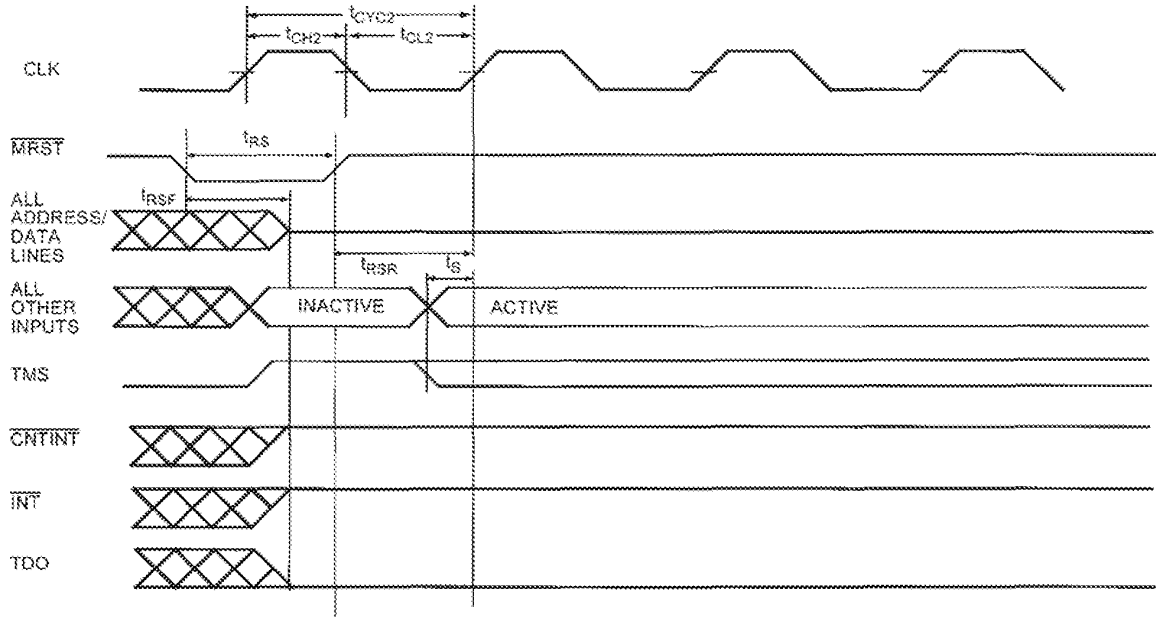
Parameter	Description	CY7C0430BV -133 Min.	CY7C0430BV -133 Max.	CY7C0430BV -100 Min.	CY7C0430BV -100 Max.	Unit
f_{JTAG}	Maximum JTAG TAP Controller Frequency		10		10	MHz
t_{TCYC}	TCK Clock Cycle Time	100		100		ns
t_{TH}	TCK Clock High Time	40		40		ns
t_{TL}	TCK Clock Low Time	40		40		ns
t_{TMSS}	TMS Setup to TCK Clock Rise	20		20		ns
t_{TMSH}	TMS Hold After TCK Clock Rise	20		20		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	20		20		ns
t_{TDIH}	TDI Hold after TCK Clock Rise	20		20		ns
t_{TDOV}	TCK Clock Low to TDO Valid		20		20	ns
t_{TDOX}	TCK Clock Low to TDO Invalid	0		0		ns
f_{BIST}	Maximum CLKBIST Frequency		50		50	MHz
t_{BH}	CLKBIST High Time	6		6		ns
t_{BL}	CLKBIST Low Time	6		6		ns



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Switching Waveforms

Master Reset[6]

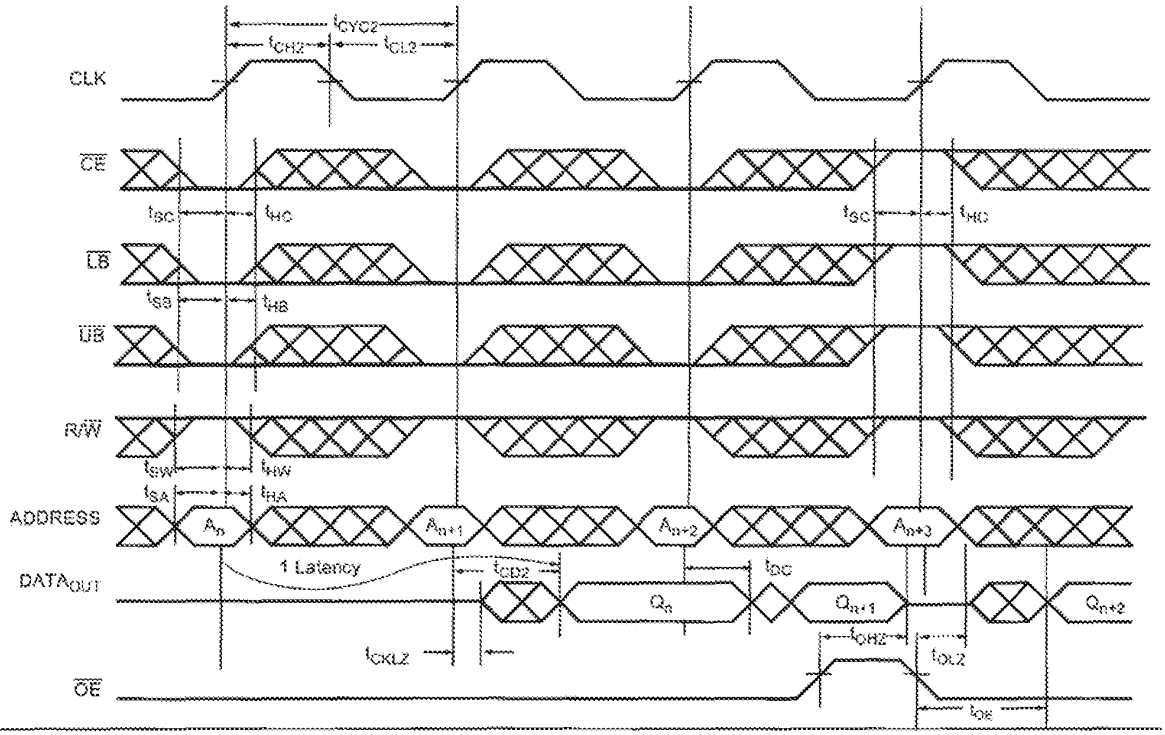


Note:
6. t_S is the set-up time required for all input control signals.

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Switching Waveforms (continued)

Read Cycle[9, 10, 11, 12, 13]



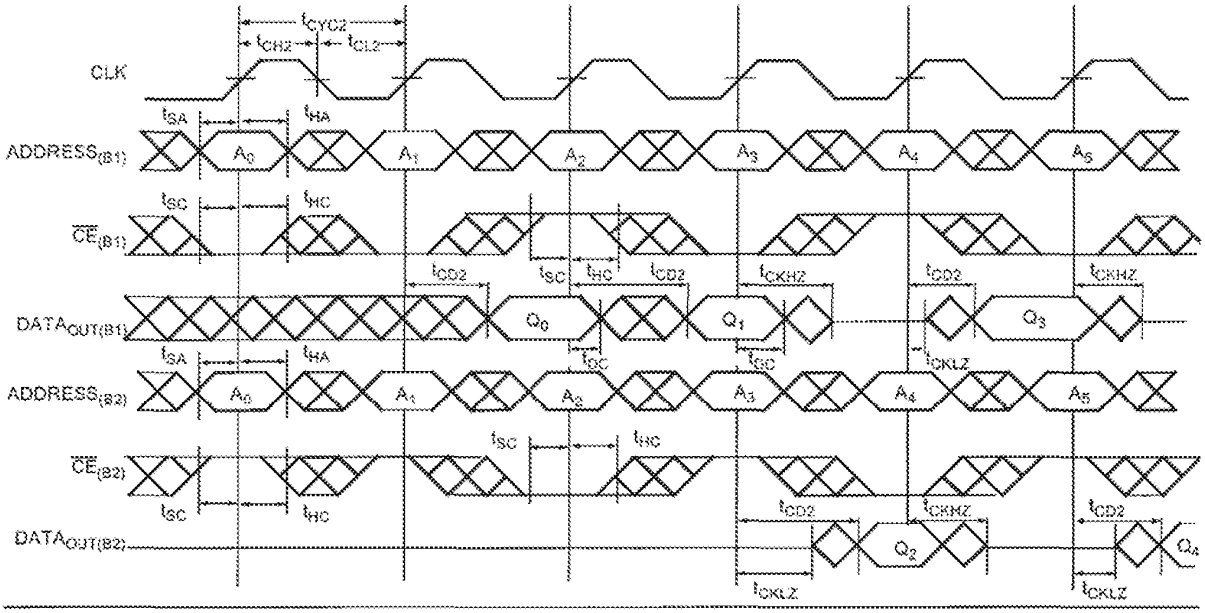
Notes:

9. $\overline{OE}$ is asynchronously controlled; all other inputs (excluding $\overline{MRST}$) are synchronous to the rising clock edge.
10. $\overline{CNTLD}$= V_{IL}, $\overline{MKLD}$= V_{IH}, $\overline{CNTINC}$ = x, and $\overline{MRST}$=$\overline{CNTRST}$ = V_{IH}.
11. The output is disabled (high-impedance state) by $\overline{CE}$=V_{IH} following the next rising edge of the clock.
12. Addresses do not have to be accessed sequentially. Note 10 indicates that address is constantly loaded on the rising edge of the CLK. Numbers are for reference only.
13. $\overline{CE}$ is internal signal. $\overline{CE}$ = VIL if $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}.

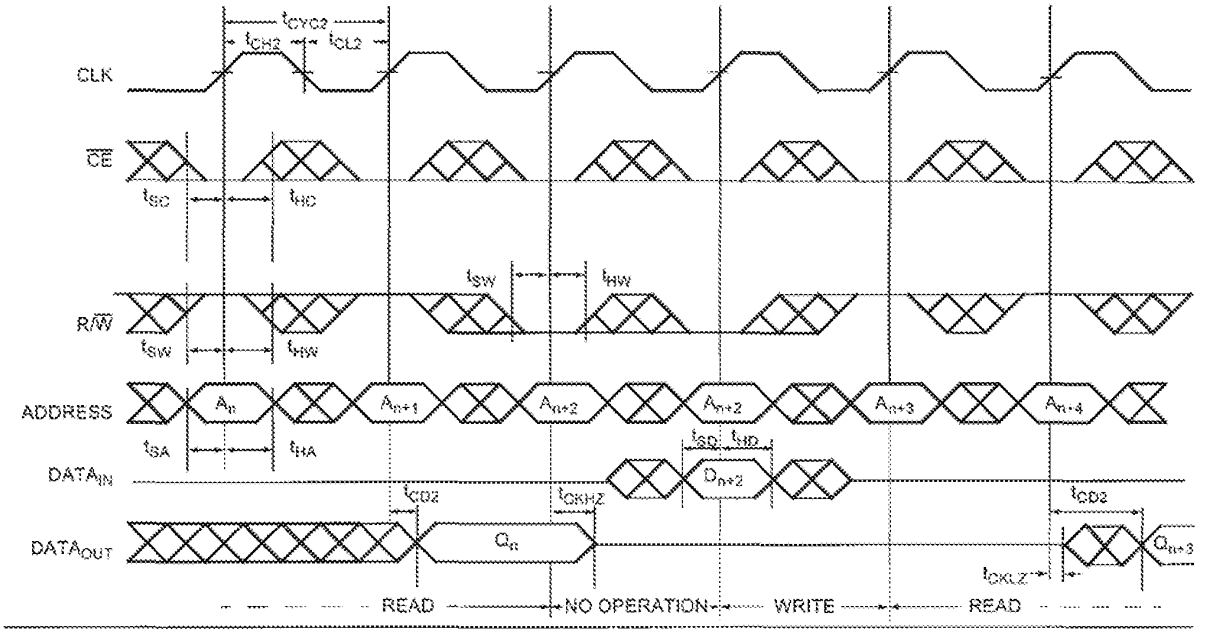
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Switching Waveforms (continued)

Bank Select Read[14, 15]



Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})[16, 17, 18, 19]



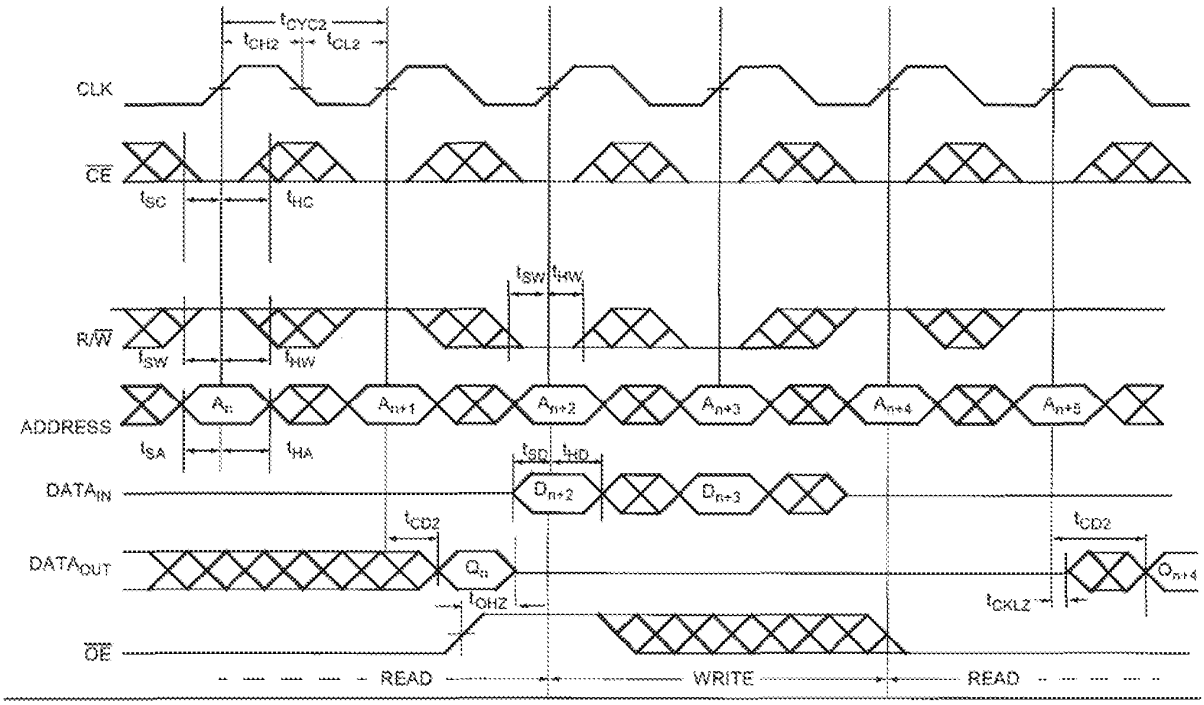
Notes:

14. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress Quadport device from this data sheet. $ADDRESS_{(B1)}$ = $ADDRESS_{(B2)}$.
15. $\overline{LB}$ = $\overline{UB}$ = $\overline{OE}$ = $\overline{CNTLD}$ = V_{IL}; $\overline{MRST}$= $\overline{CNTRST}$= $\overline{MKLD}$ = V_{IH}.
16. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
17. $\overline{LB}$ = $\overline{UB}$ = $\overline{CNTLD}$ = V_{IL}; $\overline{MRST}$= $\overline{CNTRST}$= $\overline{MKLD}$ =V_{IH}.
18. Addresses do not have to be accessed sequentially since $\overline{CNTLD}$= V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference only.
19. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

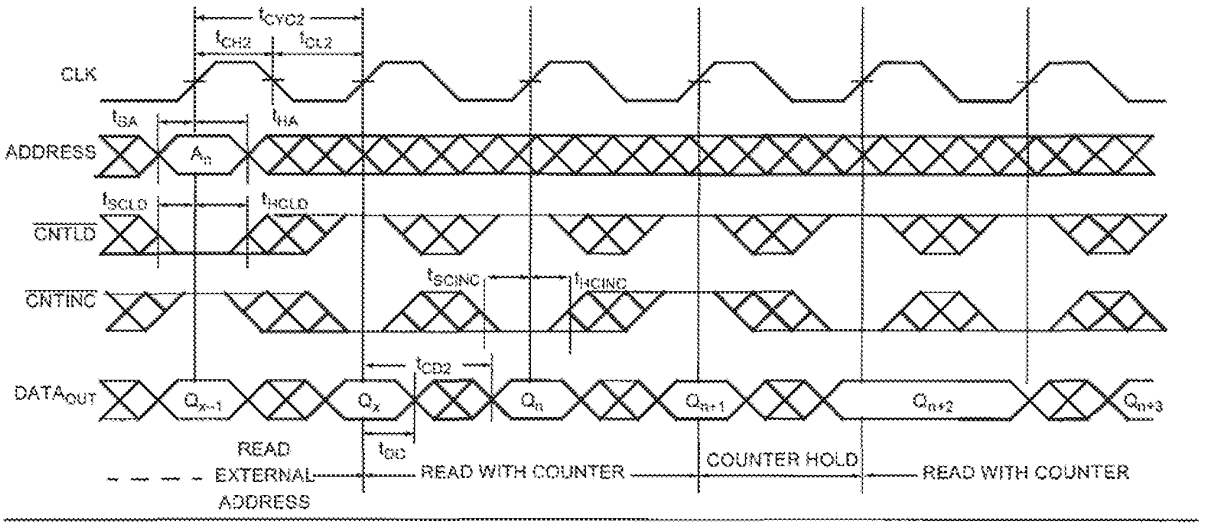
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Switching Waveforms (continued)

Read-to-Write-to-Read ($\overline{OE}$ Controlled)[16, 17, 18, 19]



Read with Address Counter Advance[20, 21]



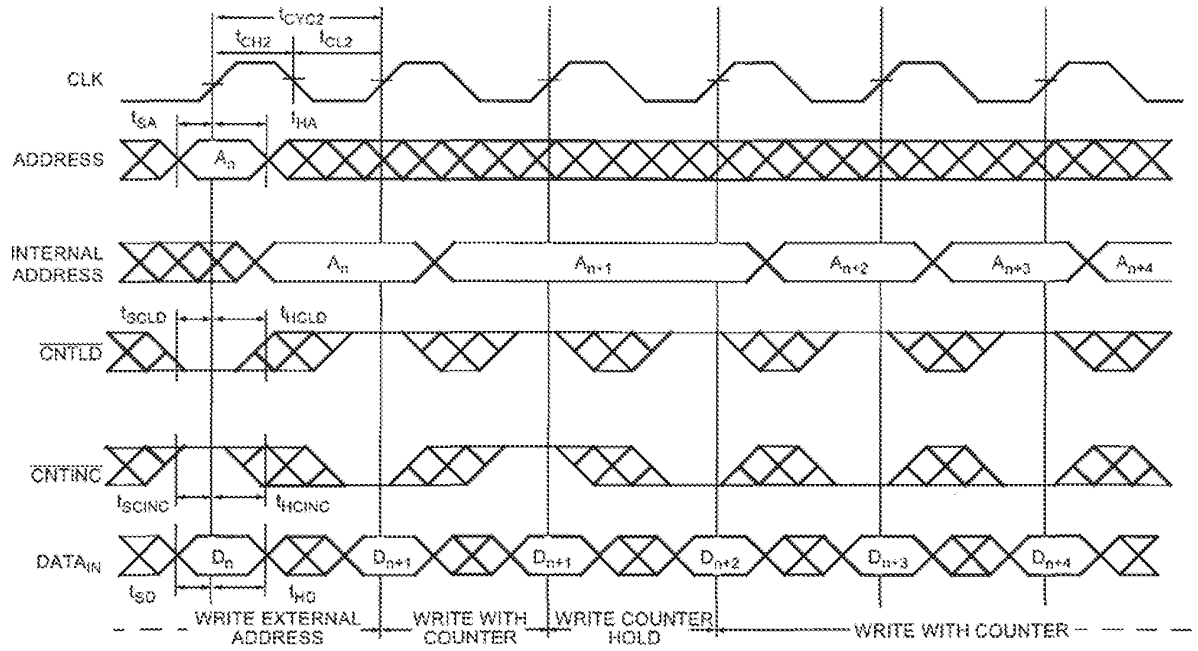
Notes:

20. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{LB}$ = $\overline{UB}$ = V_{IL}; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = $\overline{MKLD}$ = $\overline{MKRD}$ = $\overline{CNTRD}$ = V_{IH}.
21. The "Internal Address" is equal to the "External Address" when $\overline{CNTLD}$ = V_{IL}.

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Switching Waveforms (continued)

Write with Address Counter Advance [21, 22]

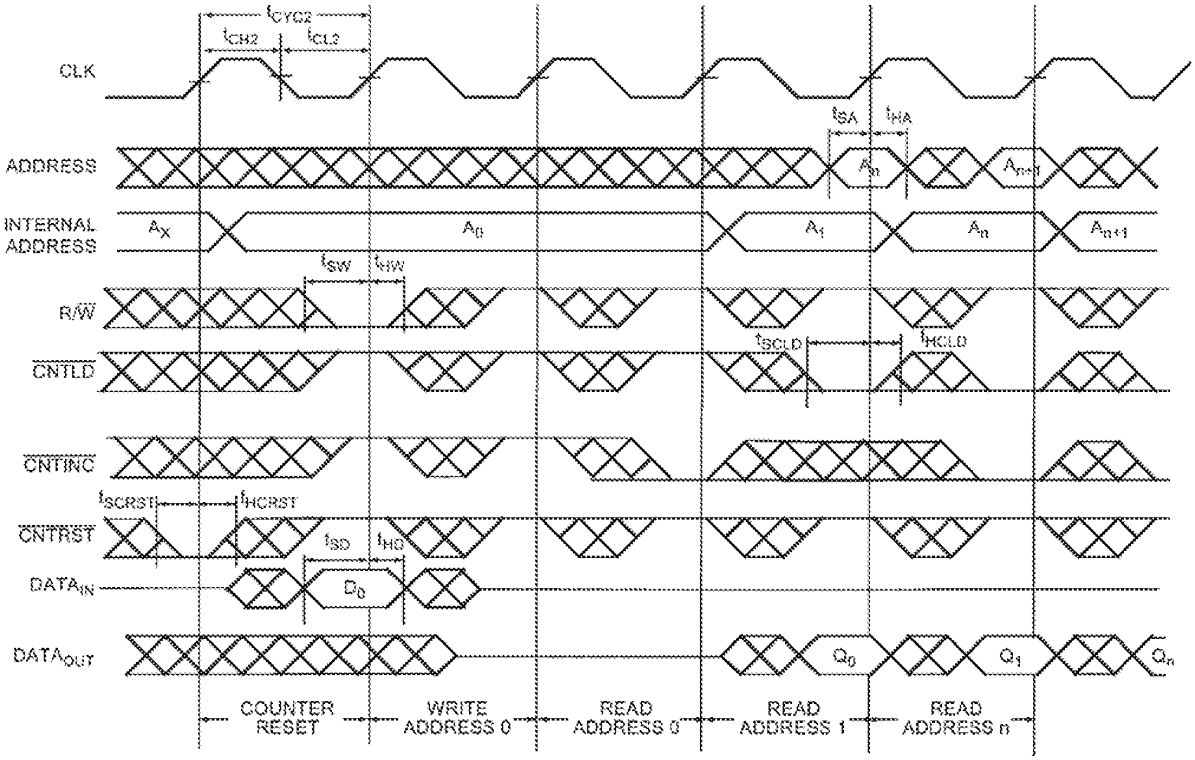


Note:
22. $\overline{CE_0}$ = $\overline{LB}$ = $\overline{UB}$ = R/$\overline{W}$ = V_{IL}; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = $\overline{MKLD}$ = $\overline{MKRD}$ = $\overline{CNTRD}$ = V_{IH}.

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Switching Waveforms (continued)

Counter Reset [18, 23, 24]



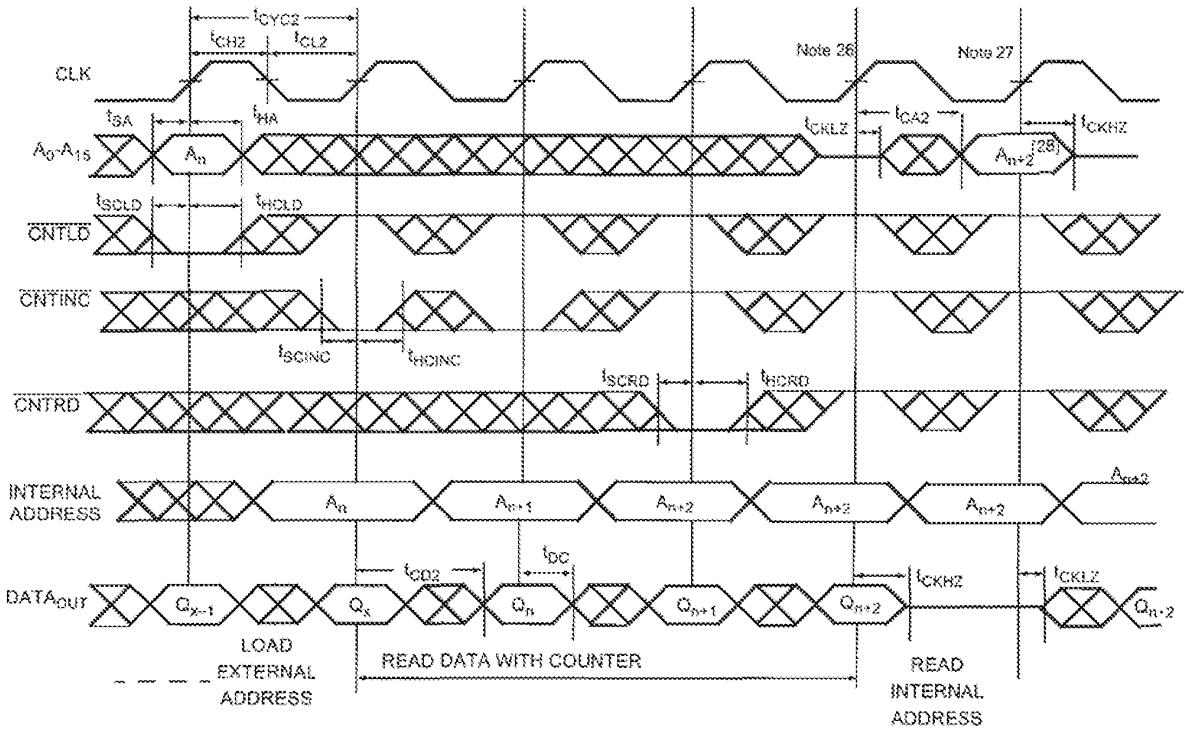
Notes:

23. $\overline{CE_0}$ = $\overline{LB}$ = $\overline{UB}$ = V_{IL}; CE_1 = $\overline{MRST}$ = $\overline{MRLD}$ = $\overline{MKRD}$ = $\overline{CNTRD}$ = V_{IH}.
24. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

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Switching Waveforms (continued)

Load and Read Address Counter[25]



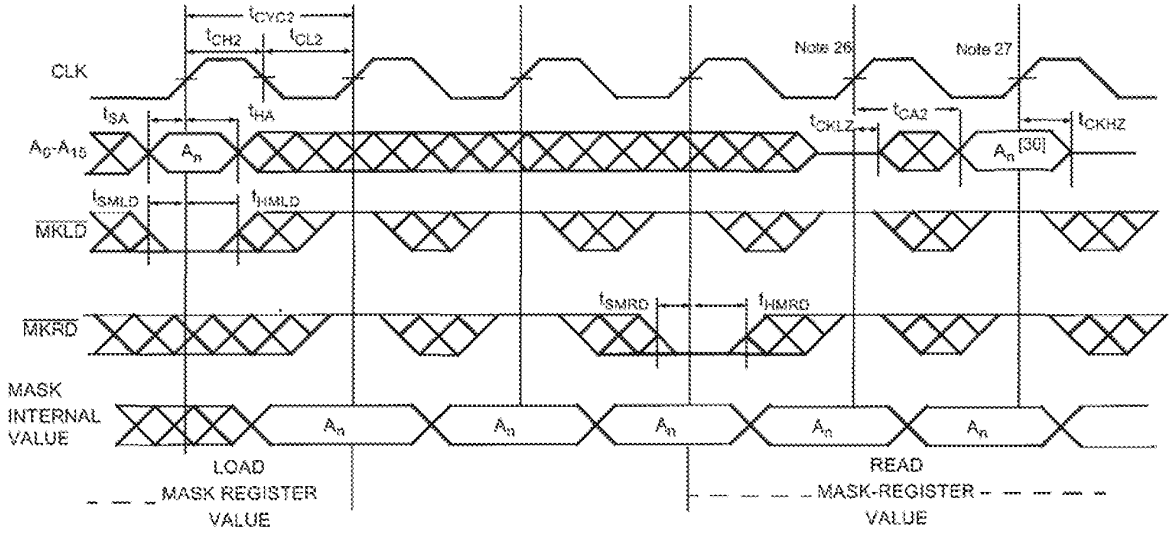
Notes:

25. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{LB}$ = $\overline{UB}$ = V_IL; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = $\overline{MKLD}$ = $\overline{MKRD}$ = V_{IH}.
26. Address in output mode. Host must not be driving address bus after time t_{CKLZ} in next clock cycle.
27. Address in input mode. Host can drive address bus after t_{CKHZ}.
28. This is the value of the address counter being read out on the address lines.

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Switching Waveforms (continued)

Load and Read Mask Register [29]

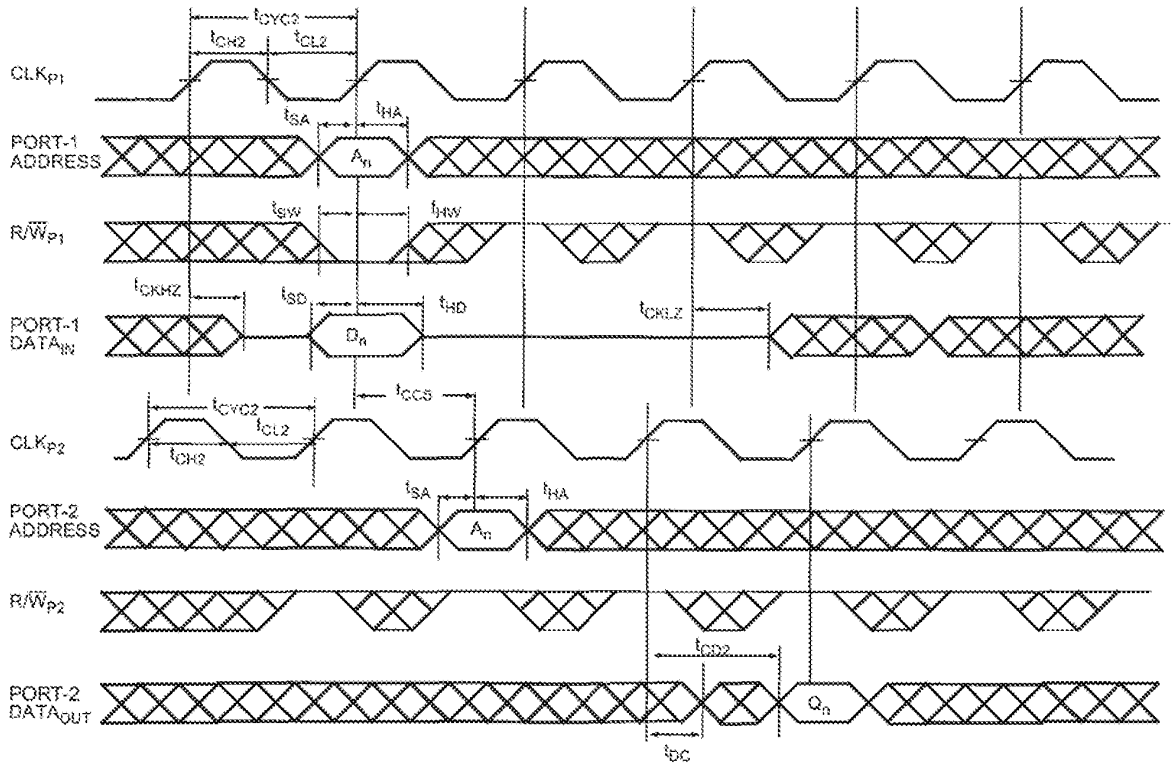


Notes:
29. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{LB}$ = $\overline{UB}$ = V_{IL}; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = $\overline{CNTLD}$ = $\overline{CNTRD}$ = $\overline{CNTINC}$ = V_{IH}.
30. This is the value of the Mask Register read out on the address lines.

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Switching Waveforms (continued)

Port 1 Write to Port 2 Read[31, 32, 33]



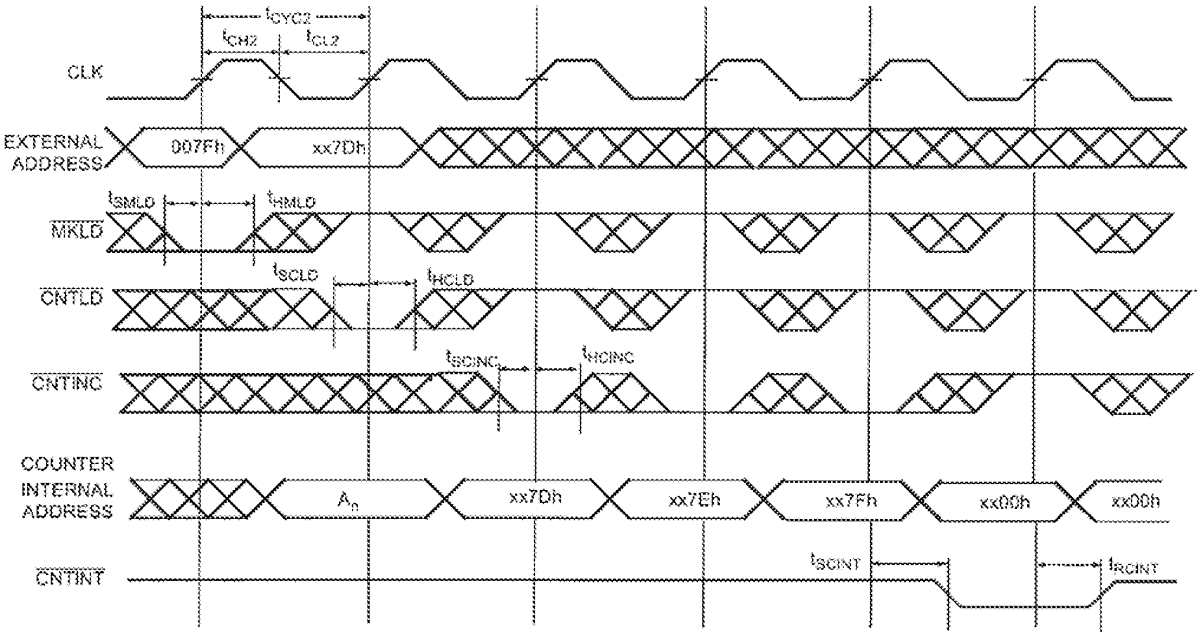
Notes:

31. $\overline{CE}_0$ = $\overline{OE}$ = $\overline{LB}$ = $\overline{UB}$ = $\overline{CNTLD}$ = V_{IL}; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = $\overline{MKLD}$ = $\overline{MKRD}$ = $\overline{CNTRD}$ = $\overline{CNTINC}$ = V_{IH}.
32. This timing is valid when one port is writing, and one or more of the three other ports is reading the same location at the same time. If t_{CCS} is violated, indeterminate data will be read out.
33. If t_{CCS} < minimum specified value, then Port 2 will read the most recent data (written by Port 1) only ($2^*t_{CYC2} + t_{CD2}$) after the rising edge of Port 2's clock. If $t_{CCS} \geq$ minimum specified value, then Port 2 will read the most recent data (written by Port 1) ($t_{CYC2} + t_{CD2}$) after the rising edge of Port 2's clock.

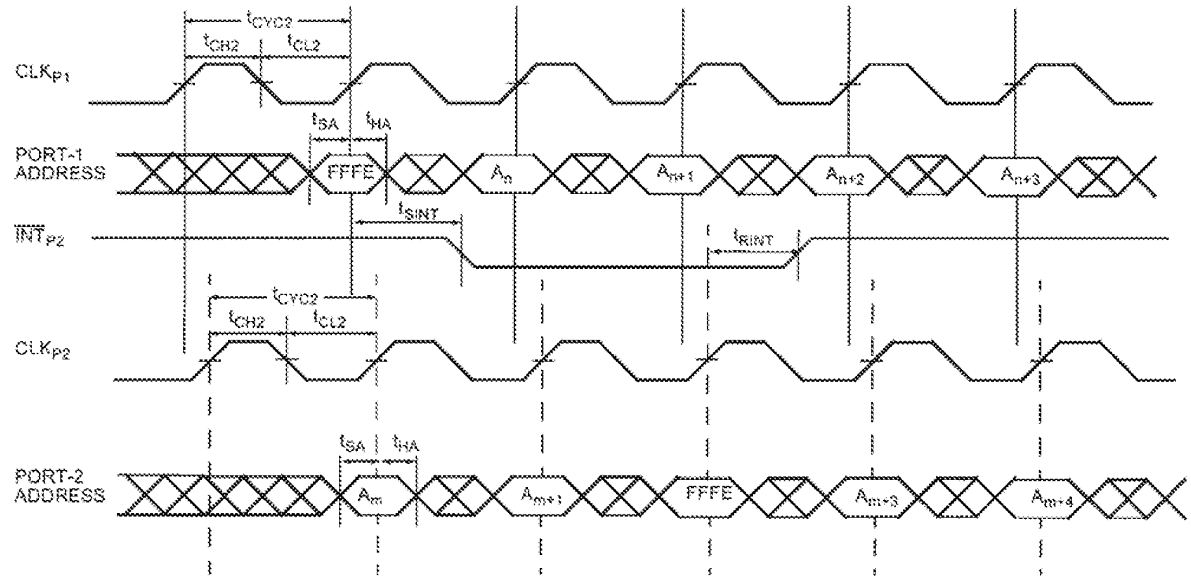
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Switching Waveforms (continued)

Counter Interrupt [34, 35, 36]



Mailbox Interrupt Timing [37, 38, 39, 40, 41]



Notes:

34. $\overline{CE_0} = \overline{OE} = \overline{LB} = \overline{UB} = V_{IL}$; $CE_1 = R/\overline{W} = \overline{CNTRST} = \overline{MRST} = \overline{CNTRD} = \overline{MKRD} = V_{IH}$.
35. $\overline{CNTINT}$ is always driven.
36. $\overline{CNTINC}$ goes LOW as the counter address masked portion is incremented from xx7Fh to xx00h. The "x" is "Don't Care."
37. $\overline{CE_0} = \overline{OE} = \overline{LB} = \overline{UB} = \overline{CNTLD} = V_{IL}$; $CE_1 = \overline{CNTRST} = \overline{MRST} = \overline{CNTRD} = \overline{CNTINC} = \overline{MKRD} = \overline{MKLD} = V_{IH}$.
38. Address "FFFE" is the mailbox location for Port 2.
39. Port 1 is configured for Write operation, and Port 2 is configured for Read operation.
40. Port 1 and Port 2 are used for simplicity. All four ports can write to or read from any mailbox.
41. Interrupt flag is set with respect to the rising edge of the write clock, and is reset with respect to the rising edge of the read clock.

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Table 1. Read/Write and Enable Operation (Any Port)[42, 43, 44]

Inputs					Outputs	Operation
$\overline{OE}$	CLK	$\overline{CE_0}$	CE_1	R/$\overline{W}$	I/O_9–I/O_{17}	
X	⎍	H	X	X	High-Z	Deselected
X	⎍	X	L	X	High-Z	Deselected
X	⎍	L	H	L	D_{IN}	Write
L	⎍	L	H	H	D_{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

Table 2. Address Counter and Counter-Mask Register Control Operation (Any Port)[42, 45, 46]

CLK	MRST	CNTRST	MKLD	CNTLD	CNTINC	CNTRD	MKRD	Mode	Operation
X	L	X	X	X	X	X	X	Master-Reset	Counter/Address Register Reset and Mask Register Set (resets entire chip as per reset state table)
⎍	H	L	X	X	X	X	X	Reset	Counter/Address Register Reset
⎍	H	H	L	X	X	X	X	Load	Load of Address Lines into Mask Register
⎍	H	H	H	L	X	X	X	Load	Load of Address Lines into Counter/Address Register
⎍	H	H	H	H	L	X	X	Incre-ment	Counter Increment
⎍	H	H	H	H	H	L	X	Read-back	Readback Counter on Address Lines
⎍	H	H	H	H	H	H	L	Read-back	Readback Mask Register on Address Lines
⎍	H	H	H	H	H	H	H	Hold	Counter Hold

Notes:
42. "X" = "Don't Care," "H" = V_{IH}, "L" = V_{IL}.
43. $\overline{OE}$ is an asynchronous input signal.
44. When $\overline{CE}$ changes state, deselection and read happen after one cycle of latency.
45. $\overline{CE_0}$ = $\overline{OE}$ = V_{IL}, CE_1 = R/$\overline{W}$ = V_{IH}.
46. Counter operation and mask register operation are independent of Chip Enables.

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Master Reset

The QuadPort undergoes a complete reset by taking its Master Reset ($\overline{MRST}$) input LOW. The Master Reset input can switch asynchronously to the clocks. A Master Reset initializes the internal burst counters to zero, and the counter mask registers to all ones (completely unmasked). A Master Reset also forces the Mailbox Interrupt ($\overline{INT}$) flags and the Counter Interrupt ($\overline{CNTINT}$) flags HIGH, resets the BIST controller, and takes all registered control signals to a deselected read state[47]. A Master Reset must be performed on the QuadPort after power-up.

Interrupts

The upper four memory locations may be used for message passing and permit communications between ports. *Table 3* shows the interrupt operation for all ports. For the 1-Meg QuadPort, the highest memory location FFFF is the mailbox for Port 1, FFFE is the mailbox for Port 2, FFFD is the mailbox for Port 3, and FFFC is the mailbox for Port 4. *Table 3* shows that in order to set Port 1 $\overline{INT}_{P1}$ flag, a write by any other port to address FFFF will assert $\overline{INT}_{P1}$ LOW. A read of FFFF location by Port 1 will reset $\overline{INT}_{P1}$ HIGH. When one port writes to the other port's mailbox, the Interrupt flag ($\overline{INT}$) of the port that the mailbox belongs to is asserted LOW. The Interrupt is reset when the owner (port) of the mailbox reads the contents of the mailbox. The interrupt flag is set in a flow-through mode (i.e., it follows the clock edge of the writing port). Also, the flag is reset in a flow-through mode (i.e., it follows the clock edge of the reading port).

Each port can read the other port's mailbox without resetting the interrupt. If an application does not require message passing, INT pins should be treated as no-connect and should be left floating. When two ports or more write to the same mailbox at the same time $\overline{INT}$ will be asserted but the contents of the mailbox are not guaranteed to be valid.

Table 3. Interrupt Operation Example

	Port 1		Port 2		Port 3		Port 4	
Function	$A_{0P1-15P1}$	$\overline{INT}_{P1}$	$A_{0P2-15P2}$	$\overline{INT}_{P2}$	$A_{0P3-15P3}$	$\overline{INT}_{P3}$	$A_{0P4-15P4}$	$\overline{INT}_{P4}$
Set Port 1 $\overline{INT}_{P1}$ Flag	X	L	FFFF	X	FFFF	X	FFFF	X
Reset Port 1 $\overline{INT}_{P1}$ Flag	FFFF	H	X	X	X	X	X	X
Set Port 2 $\overline{INT}_{P2}$ Flag	FFFE	X	X	L	FFFE	X	FFFE	X
Reset Port 2 $\overline{INT}_{P2}$ Flag	X	X	FFFE	H	X	X	X	X
Set Port 3 $\overline{INT}_{P3}$ Flag	FFFD	X	FFFD	X	X	L	FFFD	X
Reset Port 3 $\overline{INT}_{P3}$ Flag	X	X	X	X	FFFD	H	X	X
Set Port 4 $\overline{INT}_{P4}$ Flag	FFFC	X	FFFC	X	FFFC	X	X	L
Reset Port 4 $\overline{INT}_{P4}$ Flag	X	X	X	X	X	X	FFFC	H

Note:

47. During Master Reset the control signals will be set to a deselected read state: $\overline{CE}_{0I}$ = $\overline{LBI}$ = $\overline{UBI}$ = R/$\overline{W}$I = $\overline{MKLDI}$ = $\overline{MKRDI}$ = $\overline{CNTRDI}$ = $\overline{CNTRSTI}$ = $\overline{CNTLDI}$ = $\overline{CNTINCI}$ = V_{IH}; CE_{1I} = V_{IL}. The "I" suffix on all these signals denotes that these are the internal registered equivalent of the associated pin signals.

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Address Counter Control Operations

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for the fast interleaved memory applications. A port's burst counter is loaded with the port's Counter Load pin ($\overline{CNTLD}$). When the port's Counter Increment ($\overline{CNTINC}$) is asserted, the address counter will increment on each LOW to HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until $\overline{CNTINC}$ is deasserted. Depending on the mask register state, the counter can address the entire memory array and will loop back to start. Counter Reset ($\overline{CNTRST}$) is used to reset the Burst Counter (the Mask Register value is unaffected). When using the counter in readback mode, the internal address value of the counter will be read back on the address lines when Counter Readback Signal ($\overline{CNTRD}$) is asserted. *Figure 1* provides a block diagram of the readback operation. *Table 2* lists control signals required for counter operations. The signals are listed based on their priority. For example, Master Reset takes precedence over Counter Reset, and Counter Load has lower priority than Mask Register Load (described below). All counter operations are independent of Chip Enables ($\overline{CE_0}$ and CE_1). When the address readback operation is performed the data I/Os are three-stated (if CEs are active) and one-clock cycle (no-operation cycle) latency is experienced. The address will be read at time t_{CA2} from the rising edge of the clock following the no-operation cycle. The read back address can be either of the burst counter or the mask register based on the levels of Counter Read signal ($\overline{CNTRD}$) and Mask Register Read signal ($\overline{MKRD}$). Both signals are synchronized to the port's clock as shown in *Table 2*. Counter read has a higher priority than mask read.

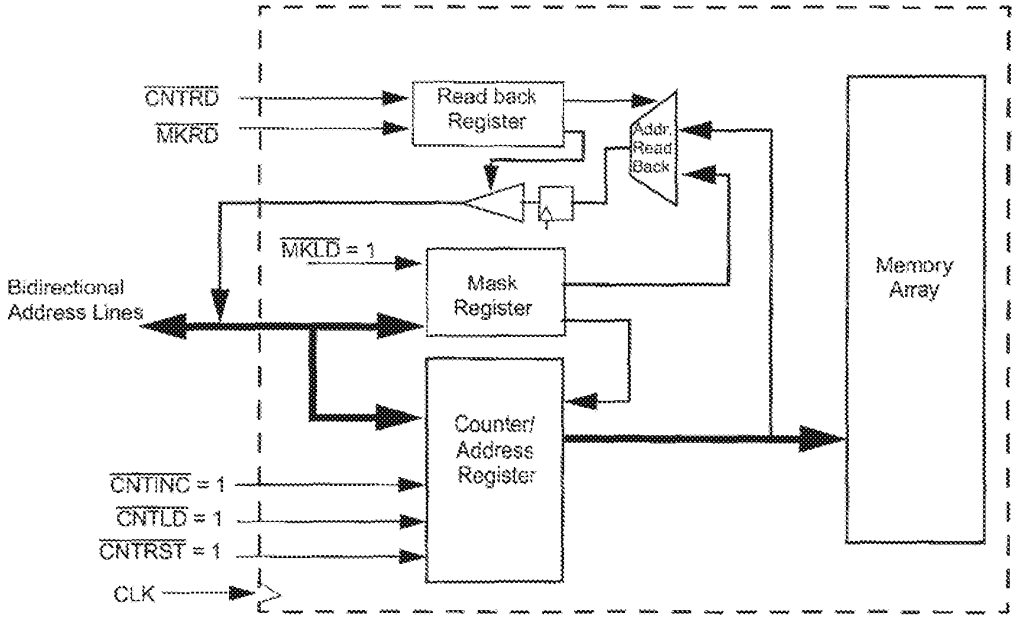


Figure 1. Counter and Mask Register Read Back on Address Lines

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Counter-Mask Register

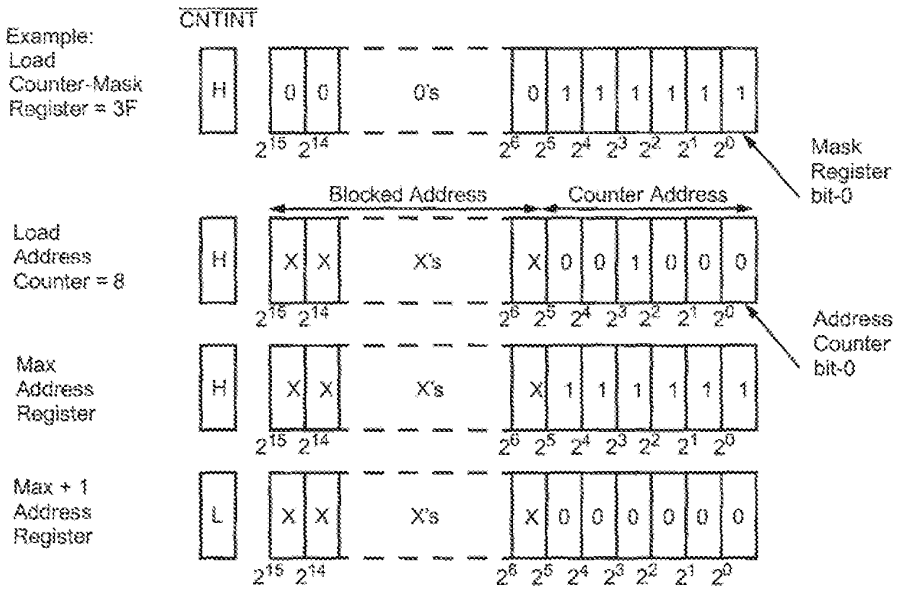


Figure 2. Programmable Counter-Mask Register Operation[48]

The burst counter has a mask register that controls when and where the counter wraps. An interrupt flag ($\overline{CNTINT}$) is asserted for one clock cycle when the unmasked portion of the counter address wraps around from all ones ($\overline{CNTINC}$ must be asserted) to all zeros. The example in *Figure 2* shows the counter mask register loaded with a mask value of 003F unmasking the first 6 bits with bit "0" as the LSB and bit "15" as the MSB. The maximum value the mask register can be loaded with is FFFF. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of XXX8. The "blocked" addresses (in this case, the 6th address through the 15th address) are loaded with an address but do not increment once loaded. The counter address will start at address XXX8. With $\overline{CNTINC}$ asserted LOW, the counter will increment its internal address value till it reaches the mask register value of 3F and wraps around the memory block to location XXX0. Therefore, the counter uses the mask-register to define wrap-around point. The mask register of every port is loaded when $\overline{MKLD}$ (mask register load) for that port is LOW. When $\overline{MKRD}$ is LOW, the value of the mask register can be read out on address lines in a manner similar to counter read back operation (see *Table 2* for required conditions).

When the burst counter is loaded with an address higher than the mask register value, the higher addresses will form the masked portion of the counter address and are called blocked addresses. The blocked addresses will not be changed or affected by the counter increment operation. The only exception is mask register bit 0. It can be masked to allow the address counter to increment by two. If the mask register bit 0 is loaded with a logic value of "0," then address counter bit 0 is masked and can not be changed during counter increment operation. If the loaded value for address counter bit 0 is "0," the counter will increment by two and the address values are even. If the loaded value for address counter bit 0 is "1," the counter will increment by two and the address values are odd. This operations allows the user to achieve a 36-bit interface using any two ports, where the counter of one port counts even addresses and the counter of the other port counts odd addresses. This even-odd address scheme stores one half of the 36-bit word in even memory locations, and the other half in odd memory locations. $\overline{CNTINT}$ will be asserted when the unmasked portion of the counter wraps to all zeros. Loading mask register bit 0 with "1" allows the counter to increment the address value sequentially.

Table 2 groups the operations of the mask register with the operations of the address counter. Address counter and mask register signals are all synchronized to the port's clock CLK. Master reset ($\overline{MRST}$) is the only asynchronous signal listed on *Table 2*. Signals are listed based on their priority going from left column to right column with $\overline{MRST}$ being the highest. A LOW on $\overline{MRST}$ will reset both counter register to all zeros and mask register to all ones. On the other hand, a LOW on $\overline{CNTRST}$ will only clear the address counter register to zeros and the mask register will remain intact.

There are four operations for the counter and mask register:

1. Load operation: When $\overline{CNTLD}$ or $\overline{MKLD}$ is LOW, the address counter or the mask register is loaded with the address value presented at the address lines. This value ranges from 0 to FFFF (64K). The mask register load operation has a higher priority over the address counter load operation.

Note:
48. The "X" in this diagram represents the counter upper-bits.

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2. Increment: Once the address counter is loaded with an external address, the counter can internally increment the address value by asserting $\overline{CNTINC}$ LOW. The counter can address the entire memory array (depend on the value of the mask register) and loop back to location 0. The increment operation is second in priority to load operation.
3. Readback: the internal value of either the burst counter or the mask register can be read out on the address lines when $\overline{CNTRD}$ or $\overline{MKRD}$ is LOW. Counter readback has higher priority over mask register readback. A no-operation delay cycle is experienced when readback operation is performed. The address will be valid after t_{CA2} (for counter readback) or t_{CM2} (for mask readback) from the following port's clock rising edge. Address readback operation is independent of the port's chip enables ($\overline{CE}_0$ and CE_1). If address readback occurs while the port is enabled (chip enables active), the data lines (I/Os) will be three-stated.
4. Hold operation: In order to hold the value of the address counter at certain address, all signals in *Table 2* have to be HIGH. This operation has the least priority. This operation is useful in many applications where wait states are needed or when address is available few cycles ahead of data.

The counter and mask register operations are totally independent of port chip enables.

IEEE 1149.1 Serial Boundary Scan (JTAG) and Memory Built-In-Self-Test (MBIST)

The CY7C0430BV incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 3.3V I/O logic levels. It is composed of three input connections and one output connection required by the test logic defined by the standard. Memory BIST circuitry will also be controlled through the TAP interface. All MBIST instructions are compliant to the JTAG standard. An external clock (CLKBIST) is provided to allow the user to run BIST at speeds up to 50 MHz. CLKBIST is multiplexed internally with the ports clocks during BIST operation.

Disabling the JTAG Feature

It is possible to operate the QuadPort without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. CLKBIST must be tied LOW to disable the MBIST. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port (TAP) - Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram (FSM)). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the QuadPort and may be performed while the device is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the QuadPort test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Four-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the following JTAG/BIST Controller diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain devices. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the QuadPort with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the QuadPort. The boundary scan register is loaded with the contents of the QP Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, and SAMPLE/PRELOAD instructions can be used to capture the contents of the Input and Output ring.

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Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the QuadPort and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Sixteen different instructions are possible with the 4-bit instruction register. All combinations are listed in *Table 6*, Instruction Codes. Seven of these instructions (codes) are listed as RESERVED and should not be used. The other nine instructions are described in detail below.

The TAP controller used in this QuadPort is fully compliant to the 1149.1 convention. The TAP controller can be used to load address, data or control signals into the QuadPort and can preload the Input or output buffers. The QuadPort implements all of the 1149.1 instructions except INTEST. *Table 6* lists all instructions.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST allows circuitry external to the QuadPort package to be tested. Boundary-scan register cells at output pins are used to apply test stimuli, while those at input pins capture test results.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the identification register. It also places the identification register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

High-Z

The High-Z instruction causes the bypass register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all QuadPort outputs into a High-Z state.

SAMPLE / PRELOAD

SAMPLE / PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE / PRELOAD instructions loaded into the instruction register and the TAP controller in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the QuadPort clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the QuadPort signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times. Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins. If the TAP controller goes into the Update-DR state, the sampled data will be updated.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

CLAMP

The optional CLAMP instruction allows the state of the signals driven from QuadPort pins to be determined from the boundary-scan register while the BYPASS register is selected as the serial path between TDI and TDO. CLAMP controls boundary cells to 1 or 0.

RUNBIST

RUNBIST instruction provides the user with a means of running a user-accessible self-test function within the QuadPort as a result of a single instruction. This permits all components on a board that offer the RUNBIST instruction to execute their self-tests concurrently, providing a quick check for the board. The QuadPort MBIST provides two modes of operation once the TAP controller is loaded with the RUNBIST instruction:

Non-Debug Mode (Go-NoGo)

The non-debug mode is a go-nogo test used simply to run BIST and obtain pass-fail information after the test is run. In addition to that, the total number of failures encountered can be obtained. This information is used to aid the debug mode (explained next) of operation. The pass-fail information and failure count is scanned out using the JTAG interface. An MBIST Result Register (MRR) will be used to store the pass-fail results. The MRR is a 25-bit register that will be connected between TDI and TDO during the internal scan (INT_SCAN) operation. The MRR will contain the total number of fail read cycles of the entire MBIST sequence. MRR[0] (bit 0) is the Pass/Fail bit. A "1" indicates some type of failure occurred, and a "0" indicates entire memory pass.

In order to run BIST in non-debug mode, the 2-bit MBIST Control Register (MCR) is loaded with the default value "00", and the TAP controller's finite state machine (FSM), which is synchronous to TCK, transitions to Run Test/Idle state. The entire MBIST test will be performed with a deterministic number of TCK cycles depending on the TCK and CLKBIST frequency.

$$t_{CYC} = \frac{t_{CYC}[CLKBIST]}{t_{CYC}[TCK]} \times m + SPC$$

t_{CYC} is total number of TCK cycles required to run MBIST.

SPC is the Synchronization Padding Cycles (4–6 cycles)

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m is a constant represents the number of read and write operations required to run MBIST algorithms (31195136).

Once the entire MBIST sequence is completed, supplying extra TCK or CLKBIST cycles will have no effect on the MBIST controller state or the pass-fail status.

Debug Mode

With the RUNBIST instruction loaded and the MCR loaded with the value of "01", and the FSM transitions to RUN_TEST/IDLE state, the MBIST goes into RUNBIST-debug mode. The debug mode will be used to provide complete failure analysis information at the board level. It is recommended that the user runs the non-debug mode first and then the debug mode in order to save test time and to set an upper bound on the number of scan outs that will be needed. The failure data will be scanned out automatically once a failure occurs using the JTAG TAP interface. The failure data will be represented by a 100-bit packet given below. The 100-bit Memory debug Register (MDR) will be connected between TDI and TDO, and will be shifted out on TDO, which is synchronized to TCK.

Figure 3 is a representation of the 100-bit MDR packet. The packet follows a 2-bit header that has a logic "1" value, and represents two TCK cycles. MDR[97:26] represent the BIST comparator values of all four ports (each port has 18 data lines). A value of "1" indicates a bit failure. The scanned out data is from LSB to MSB. MDR[25:10] represent the failing address (MSB to LSB). The state of the BIST controller is scanned out using MDR[9:4]. Bit 2 is the Test Done bit. A "0" in bit 2 means test not complete. The user has to monitor this bit at every packet to determine if more failure packets need to be scanned out at the end of the BIST operations. If the value is "0" then BIST must be repeated to capture the next failing packet. If it is "1," it means that the last failing packets have been scanned out. A trailer similar to the header represents the end of a packet.

MCR_SCAN

This instruction will connect the Memory BIST Control Register (MCR) between TDI and TDO. The default value (upon master reset) is "00". Shift_DR state will allow modifying the MCR to extend the MBIST functionality.

MBIST Control States

Thirty-five states are listed in *Table 7*. Four data algorithms are used in debug mode: moving inversion (MIA), march_2 (M2A), checkerboard (CBA), and unique address algorithm (UAA). Only Port 1 can write MIA, M2A, and CBA data to the memory. All four ports can read any algorithm data from the QP memory. Ports 2, 3, and 4 will only write UAA data.

Boundary Scan Cells (BSC)

Table 9 lists all QuadPort I/Os with their associated BSC. Notice that the cells have even numbers. Every I/O has two boundary scan cells. Bidirectional signals (address lines, data-lines) require two cells so that one (the odd cell) is used to control a three-state buffer. Input only and output only signals have an extra dummy cell (odd cells) that are used to ease device layout.

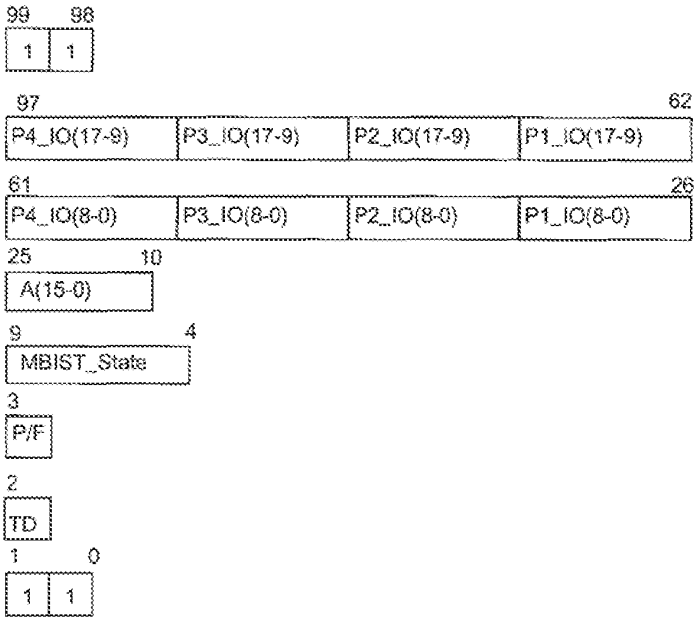
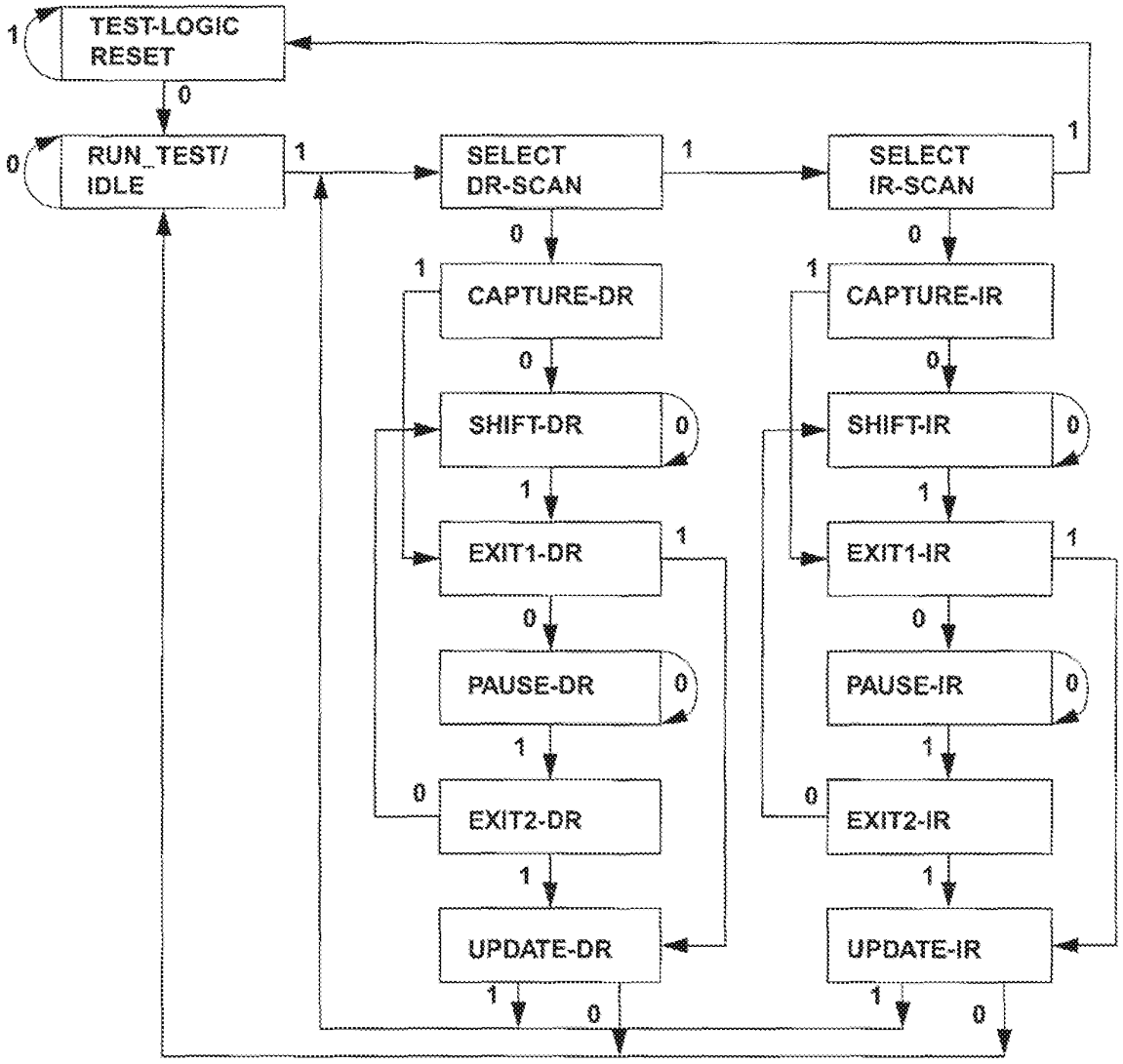


Figure 3. MBIST Debug Register Packet

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TAP Controller State Diagram (FSM)[49]



Note:
49. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

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JTAG/BIST TAP Controller Block Diagram

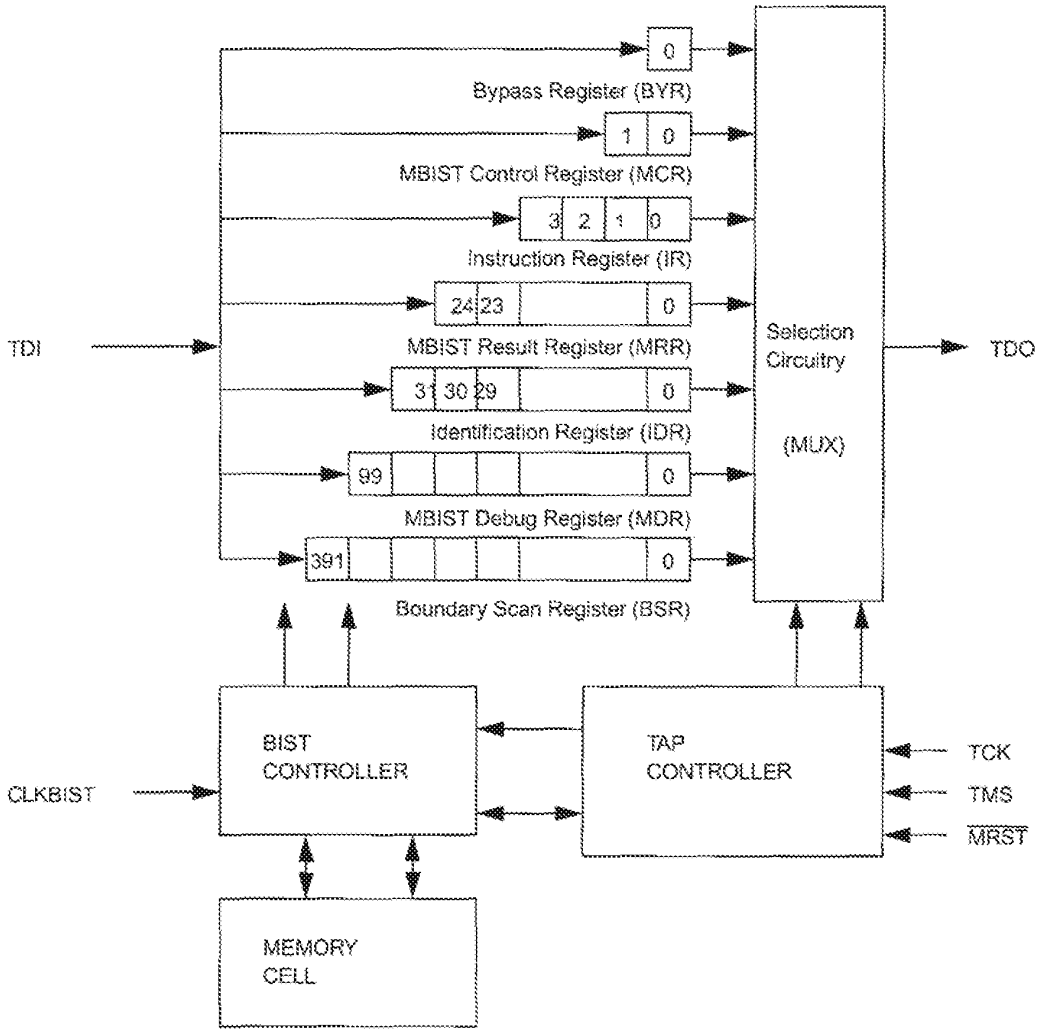


Table 4. Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	1h	Reserved for version number
Cypress Device ID (27:12)	C000h	Defines Cypress part number
Cypress JEDEC ID (11:1)	34h	Allows unique identification of QuadPort vendor
ID Register Presence (0)	1	Indicate the presence of an ID register

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Table 5. Scan Registers Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
MBIST Control (MCR)	2
MBIST Result (MRR)	25
MBIST Debug (MDR)	100
Boundary Scan (BSR)	392

Table 6. Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the Input/Output ring contents. Places the boundary scan register (BSR) between the TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0111	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0110	Places the BYR between TDI and TDO. Forces all QuadPort output drivers to a High-Z state.
CLAMP	0101	Controls boundary to 1/0. Uses BYR.
SAMPLE/PRELOAD	0001	Captures the Input/Output ring contents. Places the boundary scan register (BSR) between TDI and TDO.
RUNBIST	1000	Invokes MBIST. Places the MBIST Debug register (MDR) between TDI and TDO.
INT_SCAN	0010	Scans out pass-fail information. Places MBIST Result Register (MRR) between TDI and TDO.
MCR_SCAN	0011	Presets RUNBIST mode. Places MBIST Control Register (MCR) between TDI and TDO.
RESERVED	All other codes	Seven combinations are reserved. Do not use other than the above.

Table 7. MBIST Control States

States Code	State Name	Description
000001	movi_zeros	Port 1 write all zeros to the QP memory using Moving Inversion Algorithm (MIA).
000011	movi_1_upcnt	Up count from 0 to 64K (depth of QP). All ports read 0s, then Port 1 writes 1s to all memory locations using MIA, then all ports read 1s. MIA read0_write1_read1 (MIA_r0w1r1).
000010	movi_0_upcnt	Up count from 0 to 64K. All ports read 1s, then Port 1 writes 0s, then all ports read 0s (MIA_r1w0r0).
000110	movi_1_downcnt	Down count from 64K to 0. MIA_r0w1r1.
000111	movi_0_downcnt	Down count MIA_r1w0r0.
000101	movi_read	Read all 0s.
000100	mar2_zeros	Port 1 write all zeros to memory using March2 Algorithm (M2A).
001100	mar2_1_upcnt	Up count M2A_r0w1r1.

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Table 7. MBIST Control States (continued)

States Code	State Name	Description
001101	mar2_0_upcnt	Up count M2A_r1w0r0.
001111	mar2_1_downcnt	Down count M2A_r0w1r1.
001110	mar2_0_downcnt	Down count M2A_r1w0r0.
001010	mar2_read	Read all 0s.
001011	chkr_w	Port 1 writes topological checkerboard data to memory.
001001	chkr_r	All ports read topological checkerboard data.
001000	n_chkr_w	Port 1 write inverse topological checkerboard data.
011000	n_chkr_r	All ports read inverse topological checkerboard data.
011001	uaddr_zeros2	Port 2 write all zeros to memory using Unique Address Algorithm (UAA).
011011	uaddr_write2	Port 2 writes every address value into its memory location (UAA).
011010	uaddr_read2	All ports read UAA data.
011110	uaddr_ones2	Port 2 writes all ones to memory.
011111	n_uaddr_write2	Port 2 writes inverse address value into memory.
011101	n_uaddr_read2	All ports read inverse UAA data.
011001	uaddr_zeros3	Port 3 write all zeros to memory using Unique Address Algorithm (UAA).
011011	uaddr_write3	Port 3 writes every address value into its memory location (UAA).
011010	uaddr_read3	All ports read UAA data.
011110	uaddr_ones3	Port 3 writes all ones to memory.
011111	n_uaddr_write3	Port 3 writes inverse address value into memory.
011101	n_uaddr_read3	All ports read inverse UAA data.
011001	uaddr_zeros4	Port 4 write all zeros to memory using Unique Address Algorithm (UAA).
011011	uaddr_write4	Port 4 writes every address value into its memory location (UAA).
011010	uaddr_read4	All ports read UAA data.
011110	uaddr_ones4	Port 4 writes all ones to memory.
011111	n_uaddr_write4	Port 4 writes inverse address value into memory.
011101	n_uaddr_read4	All ports read inverse UAA data.
110010	complete	Test complete.

Table 8. MBIST Control Register (MCR)

MCR[1:0]	Mode
00	Non-Debug
01	Debug
10	Reserved
11	Reserved

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Table 9. Boundary Scan Order

Cell #	Signal Name	Bump (Ball) ID
2	A0_P4	K20
4	A1_P4	J19
6	A2_P4	J18
8	A3_P4	H20
10	A4_P4	H19
12	A5_P4	G19
14	A6_P4	G18
16	A7_P4	F20
18	A8_P4	F19
20	A9_P4	F18
22	A10_P4	E20
24	A11_P4	E19
26	A12_P4	D19
28	A13_P4	D18
30	A14_P4	C20
32	A15_P4	C19
34	$\overline{\text{CNTINT}}$_P4	F17
36	$\overline{\text{CNTRST}}$_P4	K18
38	$\overline{\text{MKLD}}$_P4	H18
40	$\overline{\text{CNTLD}}$_P4	H17
42	$\overline{\text{CNTINC}}$_P4	G17
44	$\overline{\text{CNTRD}}$_P4	E17
46	$\overline{\text{MKRD}}$_P4	E18
48	$\overline{\text{LB}}$_P4	A20
50	$\overline{\text{UB}}$_P4	B19
52	$\overline{\text{OE}}$_P4	D17
54	R/$\overline{\text{W}}$_P4	C16
56	CE1_P4	C18
58	$\overline{\text{CE0}}$_P4	C17
60	$\overline{\text{INT}}$_P4	K19
62	CLK_P4	K17
64	A0_P3	L20
66	A1_P3	M19
68	A2_P3	M18
70	A3_P3	N20
72	A4_P3	N19
74	A5_P3	P19
76	A6_P3	P18
78	A7_P3	R20
80	A8_P3	R19
82	A9_P3	R18

Table 9. Boundary Scan Order (continued)

Cell #	Signal Name	Bump (Ball) ID
84	A10_P3	T20
86	A11_P3	T19
88	A12_P3	U19
90	A13_P3	U18
92	A14_P3	V20
94	A15_P3	V19
96	$\overline{\text{CNTINT}}$_P3	R17
98	$\overline{\text{CNTRST}}$_P3	L18
100	$\overline{\text{MKLD}}$_P3	N18
102	$\overline{\text{CNTLD}}$_P3	N17
104	$\overline{\text{CNTINC}}$_P3	P17
106	$\overline{\text{CNTRD}}$_P3	T17
108	$\overline{\text{MKRD}}$_P3	T18
110	$\overline{\text{LB}}$_P3	Y20
112	$\overline{\text{UB}}$_P3	W19
114	$\overline{\text{OE}}$_P3	U17
116	R/$\overline{\text{W}}$_P3	V16
118	CE1_P3	V18
120	$\overline{\text{CE0}}$_P3	V17
122	$\overline{\text{INT}}$_P3	L19
124	CLK_P3	M17
126	IO0_P4	Y15
128	IO1_P4	W15
130	IO2_P4	Y16
132	IO3_P4	W16
134	IO4_P4	Y17
136	IO5_P4	W17
138	IO6_P4	Y18
140	IO7_P4	W18
142	IO8_P4	Y19
144	IO0_P3	V12
146	IO1_P3	Y11
148	IO2_P3	W12
150	IO3_P3	Y12
152	IO4_P3	W13
154	IO5_P3	Y13
156	IO6_P3	V15
158	IO7_P3	Y14
160	IO8_P3	W14
162	IO0_P1	Y6
164	IO1_P1	W6

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Table 9. Boundary Scan Order (continued)

Cell #	Signal Name	Bump (Ball) ID
166	IO2_P1	Y5
168	IO3_P1	W5
170	IO4_P1	Y4
172	IO5_P1	W4
174	IO6_P1	Y3
176	IO7_P1	W3
178	IO8_P1	Y2
180	IO0_P2	V9
182	IO1_P2	Y10
184	IO2_P2	W9
186	IO3_P2	Y9
188	IO4_P2	W8
190	IO5_P2	Y8
192	IO6_P2	V6
194	IO7_P2	Y7
196	IO8_P2	W7
198	A0_P2	L1
200	A1_P2	M2
202	A2_P2	M3
204	A3_P2	N1
206	A4_P2	N2
208	A5_P2	P2
210	A6_P2	P3
212	A7_P2	R1
214	A8_P2	R2
216	A9_P2	R3
218	A10_P2	T1
220	A11_P2	T2
222	A12_P2	U2
224	A13_P2	U3
226	A14_P2	V1
228	A15_P2	V2
230	$\overline{\text{CNTINT}}$_P2	R4
232	$\overline{\text{CNTRST}}$_P2	L3
234	$\overline{\text{MKLD}}$_P2	N3
236	$\overline{\text{CNTLD}}$_P2	N4
238	$\overline{\text{CNTINC}}$_P2	P4
240	$\overline{\text{CNTRD}}$_P2	T4
242	$\overline{\text{MKRD}}$_P2	T3
244	$\overline{\text{LB}}$_P2	Y1
246	$\overline{\text{UB}}$_P2	W2

Table 9. Boundary Scan Order (continued)

Cell #	Signal Name	Bump (Ball) ID
248	$\overline{\text{OE}}$_P2	U4
250	R/$\overline{\text{W}}$_P2	V5
252	CE1_P2	V3
254	$\overline{\text{CE0}}$_P2	V4
256	$\overline{\text{INT}}$_P2	L2
258	CLK_P2	M4
260	A0_P1	K1
262	A1_P1	J2
264	A2_P1	J3
266	A3_P1	H1
268	A4_P1	H2
270	A5_P1	G2
272	A6_P1	G3
274	A7_P1	F1
276	A8_P1	F2
278	A9_P1	F3
280	A10_P1	E1
282	A11_P1	E2
284	A12_P1	D2
286	A13_P1	D3
288	A14_P1	C1
290	A15_P1	C2
292	$\overline{\text{CNTINT}}$_P1	F4
294	$\overline{\text{CNTRST}}$_P1	K3
296	$\overline{\text{MKLD}}$_P1	H3
298	$\overline{\text{CNTLD}}$_P1	H4
300	$\overline{\text{CNTINC}}$_P1	G4
302	$\overline{\text{CNTRD}}$_P1	E4
304	$\overline{\text{MKRD}}$_P1	E3
306	$\overline{\text{LB}}$_P1	A1
308	$\overline{\text{UB}}$_P1	B2
310	$\overline{\text{OE}}$_P1	D4
312	R/$\overline{\text{W}}$_P1	C5
314	CE1_P1	C3
316	$\overline{\text{CE0}}$_P1	C4
318	$\overline{\text{INT}}$_P1	K2
320	CLK_P1	K4
322	IO9_P2	A6
324	IO10_P2	B6
326	IO11_P2	A5
328	IO12_P2	B5

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Table 9. Boundary Scan Order (continued)

Cell #	Signal Name	Bump (Ball) ID
330	IO13_P2	A4
332	IO14_P2	B4
334	IO15_P2	A3
336	IO16_P2	B3
338	IO17_P2	A2
340	IO9_P1	C9
342	IO10_P1	A10
344	IO11_P1	B9
346	IO12_P1	A9
348	IO13_P1	B8
350	IO14_P1	A8
352	IO15_P1	C6
354	IO16_P1	A7
356	IO17_P1	B7
358	IO9_P3	A15
360	IO10_P3	B15
362	IO11_P3	A16
364	IO12_P3	B16
366	IO13_P3	A17
368	IO14_P3	B17
370	IO15_P3	A18
372	IO16_P3	B18
374	IO17_P3	A19
376	IO9_P4	C12
378	IO10_P4	A11
380	IO11_P4	B12
382	IO12_P4	A12
384	IO13_P4	B13
386	IO14_P4	A13
388	IO15_P4	C15
390	IO16_P4	A14
392	IO17_P4	B14

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Ordering Information

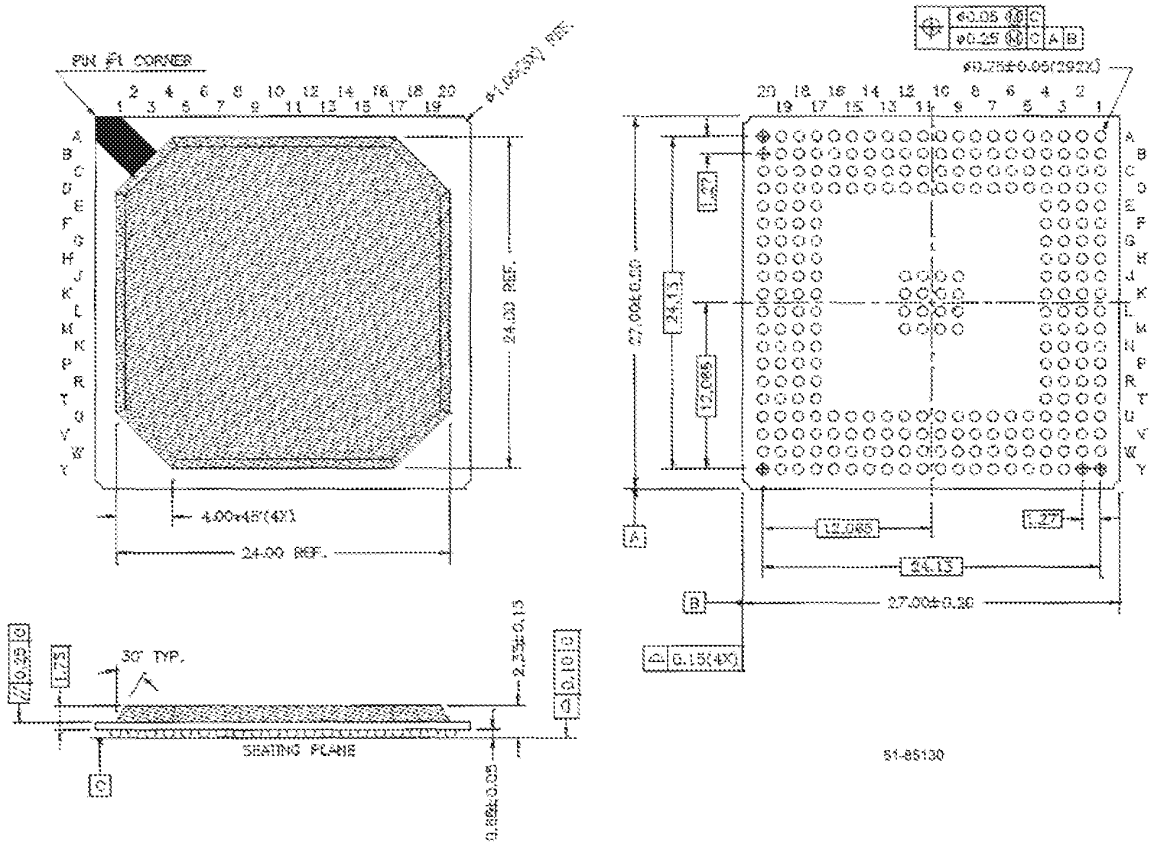
64K x 18 3.3V Synchronous QuadPort SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CY7C0430BV-133BGC	BG272	272-Ball Grid Array (BGA)	Commercial
	CY7C0430BV-133BGI	BG272	272-Ball Grid Array (BGA)	Industrial
100	CY7C0430BV-100BGC	BG272	272-Ball Grid Array (BGA)	Commercial
	CY7C0430BV-100BGI	BG272	272-Ball Grid Array (BGA)	Industrial

Document #: 38-01052-*C

Package Diagram

272-Lead Ball Grid Array (27 x 27 x 2.33 mm) BG272



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Two-bit SONOS type Flash using a band engineering in the nitride layer

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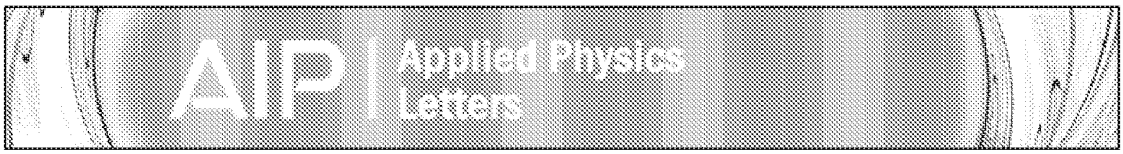
Abstract

A novel film in the trapping layer of SONOS device has been proposed. With gradually changing Si/N content ratio, the nitrogen-rich in middle (NRM) nitride has better performance and reliability than a conventional standard Si_3N_4 film. This new configuration can increase trapping efficiency by adding the probability of lateral hopping and reduce charge loss tunneling back to substrate from nitride. Besides, the characteristics of the two-bit operation are exhibited in this study. The SONOS of NRM nitride is suitable for a localized trapping storage promising non-volatile memory application.

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High-performance gate-all-around polycrystalline silicon nanowire with silicon nanocrystals nonvolatile memory

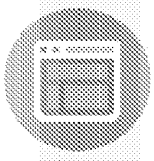
Min-Feng Hung, Yung-Chun Wu, and Zih-Yun Tang

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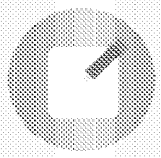


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High-performance gate-all-around polycrystalline silicon nanowire with silicon nanocrystals nonvolatile memory

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Department of Engineering and System Science, National Tsing Hua University, 30013 Hsinchu, Taiwan

(Received 24 February 2011; accepted 1 April 2011; published online 22 April 2011)

Nonvolatile memory (NVM) that is based on gate-all-around (GAA) and polycrystalline silicon (poly-Si) nanowires structure with silicon nanocrystals (NCs) as the storage nodes is demonstrated. The GAA poly-Si–SiO_2–Si_3N_4–SiO_2–poly-Si (SONOS) NVMs are also fabricated and compared. The GAA NCs NVMs have a 4.2 V of threshold voltage shift at 18 V for 1 ms, and are faster than the GAA SONOS NVMs do. In reliability studies, this NVM shows superior endurance after 10^4 program/erase (P/E) cycles, and loses only 14% of its charges lose after ten years at 85 °C. © *2011 American Institute of Physics*. [doi:10.1063/1.3582925]

Flash memory, an nonvolatile memory (NVM), is extensively adopted in portable products owing to its high density and low cost.[1] Recent efforts have witnessed the aggressive scaling down of flash memory, which follows Moore's law, making device fabrication increasingly difficult. Three-dimensional (3D) multilayer-stack memory based on poly-Si thin-film transistor (TFT) has subsequently been introduced for ultrahigh-density memory.[2,3] As has been well established, the multigate nanowires (NWs) structure significantly improves the performance of flash memory, and has been exploited in FinFET,[4] Trigate,[5] Pi-gate,[6] and even gate-all-around (GAA), for example.[7,8] The GAA structure has the highest electric field in the tunneling oxide, and therefore the highest program and erase speed. Nanocrystals (NCs) that were embedded in flash memory provide several advantages, including low-voltage operation, elimination of the drain-induced turn-on effect, elimination of the floating gate coupling effect, and reduction in stress induced leakage current effect. Accordingly, various NCs materials, including Si,[9,10] Ge,[11] metal,[12] and dielectrics[13] have been embedded in flash memory devices. Silicon NCs promote high P/E efficiency owing to their narrow bandgap, deep conduction band. Moreover, they are highly compatible with the current flash memory process and absence of metal contamination.

This investigation studies a poly-Si NWs NVM with GAA structure and Si-NCs electron storage nodes. The performance and reliability of this Si-NCs GAA NVM is compared with that without Si-NCs [poly-Si–SiO_2–Si_3N_4–SiO_2–poly-Si (SONOS) GAA NVM].

Figure 1 schematically depicts the GAA poly-Si NWs Si-NCs (GAA NCs) NVM device. An NW is magnified to show the hybrid Si-NCs. The thickness of each layer is marked in NW. Figure 2(a) is the high-resolution transmission electron microscopy (TEM) image of one NW. The poly-Si channels are in a rectangular shape surrounded by n^+ poly-Si gate to form the GAA structure. The width and height of the NWs are 60 and 25 nm [the effective width of the NW (W_{eff}) is 170 nm]. Figure 2(b) shows the top view of the Si-NCs surround by Si_3N_4. The diameter of the NCs is around 3 to 7 nm.

The GAA NCs NVMs devices were fabricated on a 6 in. silicon wafer with a 400-nm-thick thermal dioxide layer. A layer of 40-nm amorphous silicon (α-Si) deposited by low-pressure chemical-vapor deposition (LPCVD) at a temperature at 550 °C, followed by treating solid-phase crystallized process at 600 °C for 24 h in nitrogen ambient. The active layer with NWs was defined by electron beam (e-beam) and transferred by reactive ion etching. The samples were dipped in buffered oxide etch solution for forming suspending NWs. The tunneling oxide, nitride, amorphous Si (α-Si), and nitride are grown and deposited sequentially by LPCVD. Then the sample is annealed in high temperature to form the NCs. The 200-nm-thick *in situ* doped N^+ poly-silicon was deposited as a gate electrode, and patterned by e-beam and reactive ion etching (RIE). Finally, the standard passivation and metallization were performed. A control sample, SONOS NVM

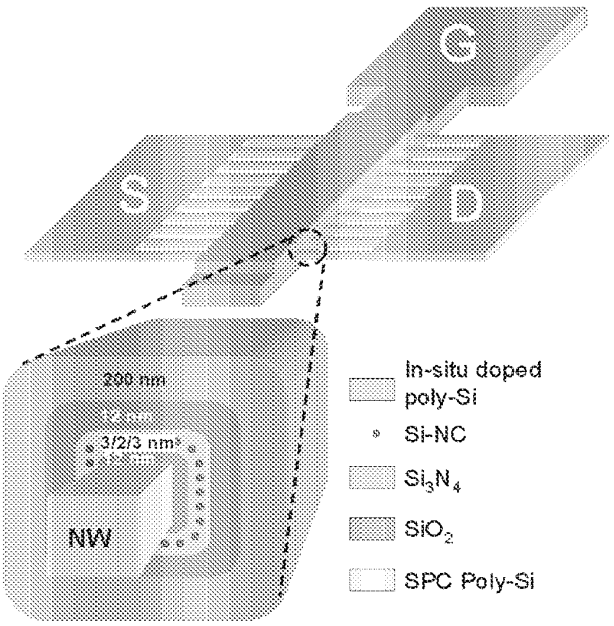


FIG. 1. (Color online) GAA poly-Si NWs NVM device, showing magnified NW, thickness of each layer, and Si NCs.

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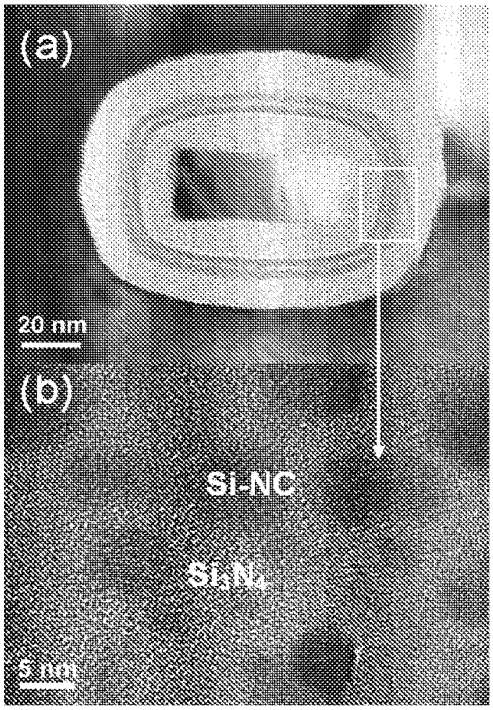


FIG. 2. (a) TEM image of one NW of the GAA poly-Si NWs NVM device with NCs. (b) TEM top view image of the Si-NCs surrounded by Si_3N_4. The diameter of the NCs is around 3 to 7 nm.

with the same GAA structure, was also formed as the above processes except the processes to form the hybrid Si-NCs. The thickness of the Si_3N_4 is 8 nm.

Figure 3 shows programming and erasing characteristics of the GAA poly-Si NWs NVM devices with and without NCs. Our tunneling oxide in this work is relatively thick, which is 12 nm at the edges and 9 nm at the corners. Thanks to the GAA structure enhancing the electric field in tunneling oxide,[14] the programming voltage is acceptable and similar with other papers, such as the Ref. 15 and 16. Additionally, four corners of the rectangular NWs enhance the electric field. Notably, the NCs NVM were programmed and erased faster than the SONOS NVM. The interface between NCs and nitride contains numerous trapping sites, which can store the tunneling charges.[17,18] Moreover, the Si NCs have deep conduction and valence bands. The tunneling distance for

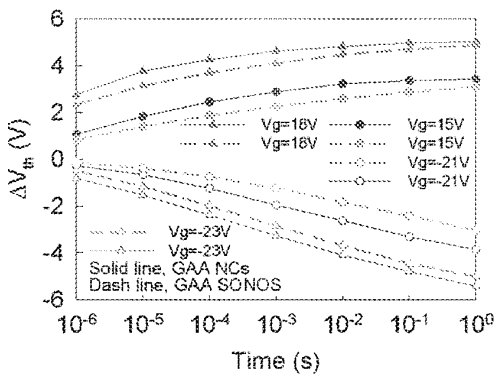


FIG. 3. (Color online) Program/erase characteristics of the GAA NCs and GAA SONOS NVM.

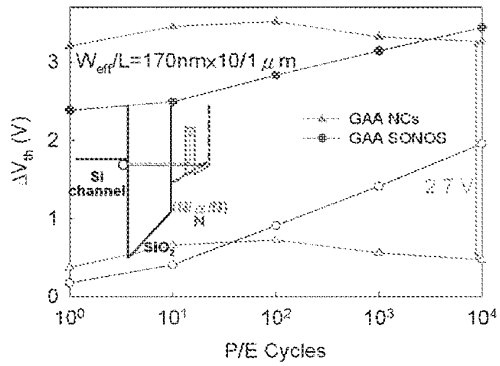


FIG. 4. (Color online) Endurance characteristics of the GAA NCs and GAA SONOS NVMs. The band diagram in erasing condition is embedded in figure.

both the electron and hole in NCs device is shorter than that in the SONOS device, so the former device has a higher electron/hole tunneling probability than the latter device.

The GAA structure enhances the electric field in the tunnel oxide, and therefore raises an issue of reliability. Figure 4 plots the endurance characteristics of the GAA NCs and GAA SONOS NVM devices. The programming and erasing conditions are V_g=15 V for 1 ms and V_g=−23 V for 0.1 s, respectively. The memory window of the GAA NCs NVM device barely decreases and shifts during 10k P/E cycles. The GAA SONOS device, however, exhibits significant upward shifting of the threshold voltage during 10k P/E cycles. These results can be explained as follows. First, the NCs device has a higher hole tunneling current because the tunneling depth therein is lower than in the SONOS device. The inset in Fig. 4 presents an energy band diagram of the NCs and SONOS NVM devices during erasing. Second, high density deep-traps in the interface and NCs capture the tunneling charge.[17,18] Most of the electrons and holes are trapped in the NCs or the interface; therefore, the tunneling holes can efficiently recombine with stored electrons.

Figure 5 shows the retention characteristics of GAA poly-Si NWs NVM device with Si-NCs and an Si_3N_4 trapping layer at 85 °C. By extrapolation at ten years, the memory window of the GAA Si-NCs NVM device remains 86% of its initial value, while that of GAA SONOS NVM remains 79% of its initial value. The GAA NCs NVM has better retention because of the deep conduction and valence bands of the Si NCs. Most of the injected charge can be

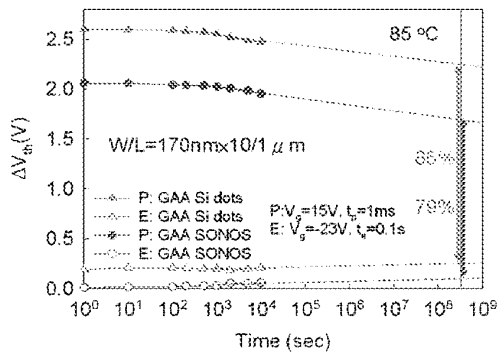


FIG. 5. (Color online) Retention characteristics of the GAA NCs and GAA SONOS NVMs.

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stored in NCs or in the interface between NCs and Si_3N_4.[17,18] The trapped charges in Si_3N_4 can also be redistributed to NCs by trap-assisted tunneling at high temperature. Therefore, most of the stored charge can be concentrated in a deep level of NCs.

In conclusion, with the same GAA structure, the NVM with NCs program and erase faster than the SONOS NVM does because of the high deep-trap density in NCs and short tunneling distance of charges to NCs. Furthermore, the use of Si NCs improves the endurance and retention of the device. The program and erase voltages can be further reduced by thinning the thickness of the tunneling oxide and the blocking oxide. The fabrication of a GAA NVM device is simple and highly compatible with the current flash process. This investigation would examine the NWs poly-Si TFT memories on future 3D stacked high-density applications.

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Cypress SONOS Technology

Cypress Semiconductor White Paper

By Krishnaswamy Ramkumar

Executive Summary

This white paper discusses the key features of Cypress SONOS technology, its performance, and reliability. It also presents a comparison between the SONOS technology and other Flash technologies.

Introduction

The demand for embedded Flash memory in System-on-Chip (SOC) designs has grown steeply in recent years as newer applications evolve in communications and consumer electronics. The memory content of complex SOC has increased due to increased demand on system performance. Flash memory is highly desirable in most applications to store critical data and code. Flash memory in a SOC enables field programming that provides great flexibility for the end user to make system level changes through software. Cypress's Programmable System-on-Chip (PSOC) is a great example of a versatile SOC whose functionality can be modified by code stored in the embedded flash memory. SOC designers, however, require the Flash memory to easily integrate with the rest of the circuitry without impacting the existing IP blocks so that existing design IP can be re-used. This requirement is challenging and was a barrier for the growth of SOCs with Flash memory.

SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) technology has been known as a Flash technology since the 1980s. However, in the past it was not very successful in competing against the floating gate technology for standalone nonvolatile memories. In recent years, with the increasing demand for embedded nonvolatile memory, SONOS, being easier to integrate with the logic technology, is becoming very attractive.

This document provides an overview of the Cypress SONOS technology, its features, and its integration into a logic process flow.

Flash Memories

Nonvolatile memories (NVM) retain stored information even if the power supply to the memory is switched off. There are different types of nonvolatile memories including Flash, read-only memory (ROM), one-time programmable (OTP), and multiple-time programmable (MTP) memories. Flash memory is the most versatile because it can be programmed and erased thousands of times with no degradation in the sense margin and data retention performance.

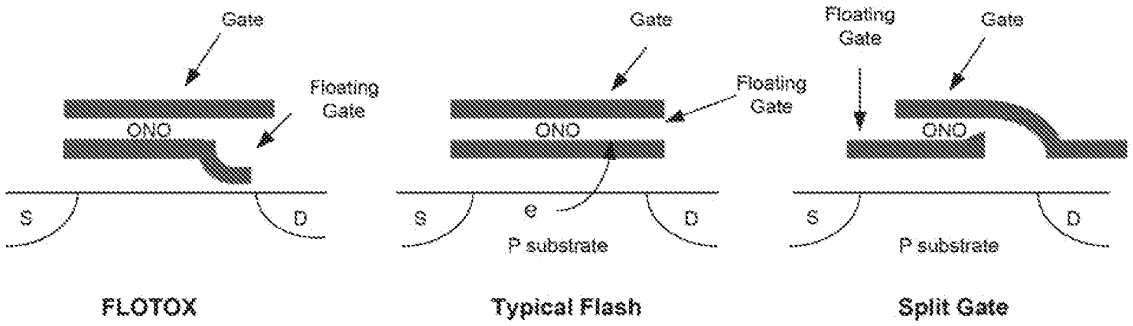
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Floating Gate Flash Memory Technology

Flash memory technology has evolved over the last 30 years to meet the demand for higher density and improved performance. Starting from UV erased PROMs, they have now evolved into page erased EEPROMs. Figure 1 shows the cross section structures of key Flash memory cells developed in the last 30 years. The charge storage layer is the same in all the generations. A floating gate in a metal-oxide-semiconductor field-effect transistor (MOS FET) is used to store the charge. The floating gate is sandwiched in between the channel and the control gate. It is separated from the channel by a thin tunnel oxide and from the control gate by an ONO dielectric. The method of injecting (programming of memory) and removing (erasing of memory) charge from the floating gate can be different and has led to different families of Flash memory.

The charge is injected from the channel to the floating poly through the "tunnel oxide." The injection is either by direct Fowler–Nordheim (FN) tunneling or channel hot electron injection (CHEI). The erasing is typically done by FN tunneling of the required type of charge from the channel to the floating gate. The FLOTOX cell uses a thin tunnel oxide at one end of the channel to enable FN tunneling of carriers. The more typical Flash cell has a device with thicker tunnel oxide but uses CHEI for programming. The split gate cell uses the same mechanism to program or erase but has a different structure.

Figure 1. Cross Section Structures of Flash Memory Cells



There are two types of Flash memory depending on the memory cell: NAND and NOR. The comparison of the two types is given in the following table. Floating gate Flash memory of both types is available from many manufacturers.

Table 1. Comparison between NAND and NOR Memory Cells

	NAND	NOR
Read access	Serial	Random
P/E methods	CHEI/FN	CHEI/FN
Cell size (F^2)	5–6	10–12
Application	Data storage	Code storage

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SONOS or Charge Trap Memory Technology

Interest in SONOS has increased in recent years because the scalability of floating gate NVM technology is reaching its limits beyond the 45 nm node. One of the challenges stems from the need to isolate the floating gate from surrounding layers. When device dimensions shrink, the insulating layers surrounding the gate must also shrink. This leads to increased capacitive coupling between memory bits and greater likelihood of small "pinhole" manufacturing defects in the insulating layers, creating a discharge path. The second challenge that arises from shrinking dimensions is the increasing mismatch between the voltage needed to cause tunneling and the normal circuit operating voltage. As the technology shrinks, circuits must operate at lower voltages to avoid device damage, but the voltage needed to induce tunneling does not drop proportionately. This makes it increasingly difficult to integrate erase and write circuitry into the rest of the memory device. The voltage mismatch also increases the likelihood of long term damage to the floating gate transistor with each write/erase cycle, an effect known as "wear out."

In contrast to the floating gate type, a SONOS memory uses an insulating layer such as silicon nitride with traps as the charge storage layer. The traps in the nitride capture the carriers injected from the channel and retain the charge. This type of memory is also known as "Charge Trap Memory." Since the charge storage layer is an insulator, this storage mechanism is inherently less sensitive to the "pinhole" defects and more robust for data retention. One of the key advantages of SONOS technology is the relatively low voltages required for program/erase as compared to Floating gate Flash. However, the retention performance of SONOS has been questioned in the past. SONOS also did not have multi-level or multi-bit capability previously. A very significant research effort has been underway the last 10 years to further improve the reliability of SONOS and develop multi-level and multi-bit capability. Much of the research effort is focused on the SONOS stack, where band gap engineering of ONO layers, high K dielectrics and metal gates have been evaluated. However, most of the SONOS technology in volume production still uses conventional materials such as silicon dioxide and silicon nitride. This technology is currently used in high volume manufacturing mainly for stand alone Flash memories. These memories typically use hot electron injection (HEI) mechanism for programming and Hot Hole injection or Band to Band Tunneling for erasing. They meet all the performance and reliability requirements and also have multi-bit capability.

Overview of Cypress SONOS Technology

Cypress's SONOS technology is an embedded nonvolatile technology that integrates the highly reliable SONOS transistor into a CMOS process flow with minimum additional mask layers and minimal impact on the electrical parameters of the existing CMOS FETs. Cypress uses a unique process for the SONOS transistor to achieve superior reliability. With integration simpler than that of floating gate Flash, the Cypress SONOS technology can enable a faster ramp to a high yield process flow. This technology is qualified in Cypress manufacturing plants and in multiple foundries. The Cypress SONOS cell is highly suitable for designing and manufacturing EEPROM and embedding Flash memory into logic integrated circuits. The Cypress SONOS technology uses fewer mask layers than floating gate technology. It is very compatible with CMOS logic technology, which makes it ideal for embedded Flash. Cypress SONOS technology has been in production since 2001 and over a billion chips that have true e-flash have been shipped to customers so far. The 0.35 um and 130 nm SONOS technologies are currently in high volume manufacturing and 65 nm SONOS technology is in development. This technology is also scalable to more advanced technology nodes such as 45 nm and 28 nm.

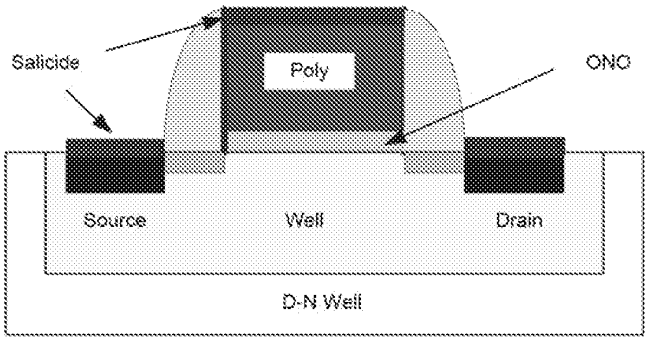
Cypress SONOS Transistor and Cell

The heart of the Cypress SONOS technology is the SONOS FET shown in Figure 2.

This is a MOS transistor with ONO stack as the gate dielectric. The ONO stack is designed to provide the required program or erase speeds and excellent reliability. The stack is engineered to yield a memory cell with outstanding endurance and retention characteristics. Further, the stack is suitable for high volume manufacturing with high Cpk. The SONOS transistor shares many of the key process steps with the CMOS transistors. Hence, many regions of the SONOS transistor, such as source, drain, and gate, are identical to those of the CMOS transistors. This makes the process architecture of the embedded SONOS technology significantly simpler.

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Figure 2. SONOS Transistor Schematic



The schematic shown in Figure 2 is a SONOS transistor that is fabricated using a typical logic CMOS process flow. The device has salicided gate, source, and drain regions and the gate stack is made up of salicided polysilicon. The device structure is slightly different in an SRAM flow with the gate stack having an insulator on top of the polysilicon to enable formation of self-aligned contacts. The source and drain regions are typically not salicided in an SRAM process.

The Cypress SONOS technology currently offers multiple cell options to fit into different application focuses, without compromising reliability.

SONOS Cell Operation

The SONOS cell is programmed by raising the gate voltage of the SONOS transistor to the required positive value. Electrons are injected from the substrate into the charge storage layer of the ONO stack by FN tunneling. The device is erased by applying the required negative voltage to the gate, which causes FN tunneling of holes from the substrate to the charge storage layer. The required program and erase voltage between the gate and substrate is obtained by applying appropriate voltages to the gate and the p-well. Typical voltages for a 10 V program and erase are shown in Table 2.

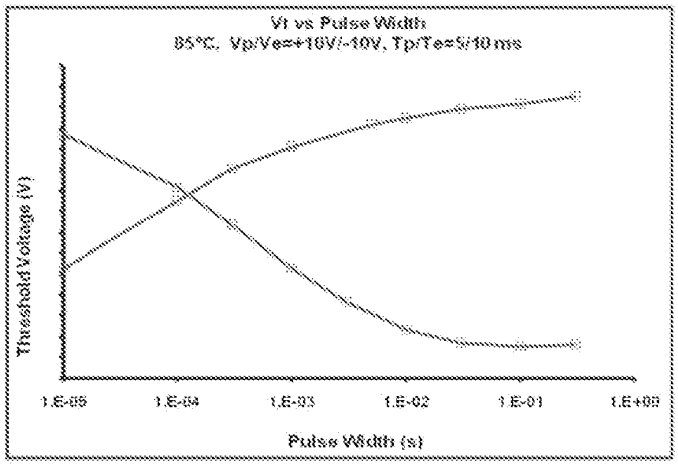
Table 2. Voltages for 130 nm SONOS Operation

	Program	Erase	Read
Vg	7 V	-7 V	0
Vpw	-3 V	3 V	0
Vs	-3 V	3 V	0
Vd	-3 V	3 V	1.2 V

A typical program and erase characteristic of the Cypress SONOS device at 85 °C is shown in Figure 3. High voltages required for program and erase are generated by on-chip charge pump circuits.

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Figure 3. Program and Erase Characteristics of Cypress SONOS FET



The current program speed is 1 to 3 ms and erase speed is 5 to 10 ms depending on cell option and macro architecture.

Cypress 130 nm SONOS Performance Specifications

The optimized Cypress SONOS technology guarantees the following specifications, which are all proved on silicon:

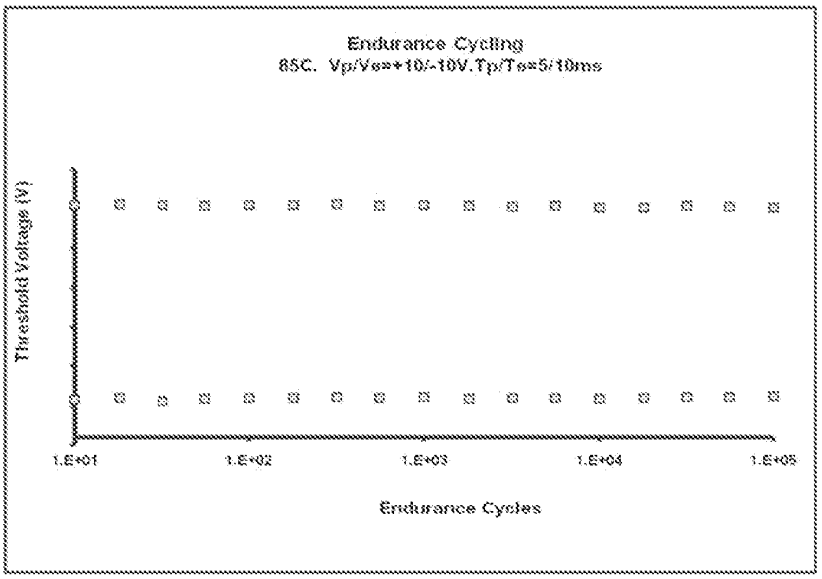
- Program time: 1 to 5 ms; Erase time: 3 to 10 ms
- Program Vt (BOL): ~1 V; Erase Vt (BOL): ~–1 V
- Minimum selected erased cell read current: 8 µA/cell
- Maximum selected programmed cell read current: 100 nA/cell
- Maximum unselected cell leakage at 100 °C: 4 nA/cell

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SONOS Cell Reliability

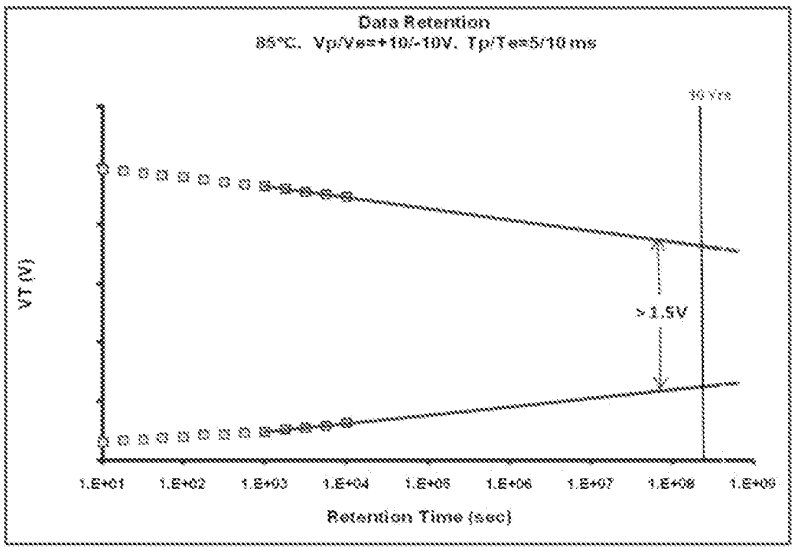
A key requirement for an NVM cell is reliability. The End-of-life (EOL) Vt window is determined by the degradation caused by program/erase cycles (Endurance) and Vt decay during storage (Data retention). Endurance is typically characterized by cycling a SONOS cell through the required number of program/erase cycles and measuring the shift of program and erase Vts. Retention is characterized by taking the SONOS cell through a fixed number of program/erase cycles and then measuring the change of Vt (program or erase) with time at an elevated temperature. Cypress SONOS technology guarantees retention of 20 years after 100 K cycles. Figure 4 and Figure 5 illustrate the typical endurance and retention characteristics.

Figure 4. Endurance Characteristics of Cypress SONOS FET



The endurance characteristics show that Vt shifts less than 100 mV after 100 K program/erase cycles at 85 °C

Figure 5. Retention Characteristics of Cypress SONOS FET



The retention characteristics show that the Cypress SONOS device has an EOL window greater than 1.5 V after 10 years at 85 °C.

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The memory macro is also characterized for reliability. Both at the device level and the macro level, the Cypress SONOS cell show the EOL window greater than 1 V. The reliability specifications fro Cypress SONOS technology, are given in Table 3.

Table 3. Reliability Specifications for SONOS Technology

Specification	Type of NVM	Endurance (Cycles)	Data Retention (Yrs)	Ave ambient Temperature (C)
Industrial	Flash	100 K	20	< 55
		10 K	10	< 85
	EEPROM	1 M	20	< 25
		100 K	20	< 55
		10 K	10	< 85

SONOS Integration

The SONOS module can easily be embedded into a logic process flow or an SRAM process flow with the addition of three to five masking layers. The integration scheme includes a dual gate oxide process, which enables the chip to be compatible with multiple supply voltages. The SONOS has been integrated into a state-of-the-art logic process flow, which includes salicided junctions, stress layers, and Cu-low K interconnects. The integration can be done at many of the technology nodes such as 130 nm, 90 nm, or 65 nm with very few changes except for cell shrink with more aggressive design rules. The optimized thermal budget of SONOS integration ensures a negligible impact on the electrical parameters of existing CMOS devices. This has been proven on very sensitive devices in the 65 nm technology. This means that with minimal changes, all the design IP of the original CMOS platform can be used in the embedded ICs. The integration of SONOS into a logic process flow uses significantly fewer masks than FG Flash, as shown in Table 4.

Table 4. Comparison of Additional Masks for FG Flash and SONOS Embedded into Logic Flow

Process Step	Embedded Floating Gate NVM	CY Embedded SONOS
Wells	+3 Masks	+1 Mask
Floating gate patterning	+1 Mask	
Other NVM related patterning	+2 Masks	+1 Mask
High voltage oxidation/patterning	+1 Mask	+1 Mask
NVM /source/drain implants	+2 Masks	+ 1 Mask
High voltage source/drain implant	+2 Masks	
Masking step adder	+11	+4

Compared to the split gate Flash technology, it is simpler and easier to integrate the Cypress SONOS into a logic CMOS process flow with fewer additional steps (see Table 5). Further, the yield on a SOC with SONOS is limited almost entirely by the CMOS portion of the die.

Table 5. Comparison of FG Flash, Split Gate Flash, and SONOS

Issue	Stack FG	Split Gate	CY SONOS
Poly layers	Double	Triple	Single
Floating gate patterning	Yes	Yes	No
Word line poly patterning	Yes	Yes	Yes
Steps for floating gate formation	4 to 5	10 to 12	0
Yield impacting additional process steps	2	3 to 5	1

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SONOS Integration into foundry 65 nm process

The integration of SONOS into the 65 nm process flow involves the foundry CMOS baseline, which is already in high volume production. The critical issues in this integration are (1) no impact to existing devices and design IP and (2) no degradation in yield. Device matching and no impact to design IP have been successfully demonstrated. It has been shown that there is no impact to the baseline yield due to the integration of SONOS.

The 65 nm SONOS technology has the additional challenge of even lower program/erase voltages. Since the baseline 65 nm technologies has an I/O voltage of 2.5 V, the program / erase voltages are limited to about 7 to 8 V. The SONOS stack has been re-optimized to meet the performance and reliability requirements at these lower program/erase voltages.

Cypress 65 nm SONOS Performance Goals:

The optimized Cypress 65 nm SONOS technology has the following performance goals:

- Program time: 1 to 5 ms; Erase time: 3 to 10 ms
- Program Vt (BOL): ~1 V; Erase Vt (BOL): ~–1 V
- Minimum selected erased cell read current: 3 uA
- Maximum selected programmed cell read current: 1 uA
- Maximum unselected cell leakage at 100 °C: 3.9 nA
- Data retention at 55 C after 10 K P/E cycles at 55 C: 20 yrs

SONOS Data Security

Because SONOS stores the charge in dielectric materials, ion scans and scanning electron microscopes cannot read the programming state of SONOS cells, as they can in floating gate cells. Therefore, SONOS has super capability to provide physical layer security.

Summary

The Cypress SONOS technology is a low cost, highly reliable approach to embed nonvolatile memory into logic platforms. The CMOS design IP is virtually unchanged by SONOS integration. This technology has unbeatable endurance and retention and is scalable to more advanced technology nodes with very little change in process integration.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

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CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/13/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	02/13/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

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(Signature)
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

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nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	02/13/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-324000

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EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/13/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 136 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 136 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notices of Allowance and Fee(s) Due mailed between October 1, 2013 and December 31, 2013

(Addendum to PTOL-85)

If the "Notice of Allowance and Fee(s) Due" has a mailing date on or after October 1, 2013 and before January 1, 2014, the following information is applicable to this application.

If the issue fee is being timely paid on or after January 1, 2014, the amount due is the issue fee and publication fee in effect January 1, 2014. On January 1, 2014, the issue fees set forth in 37 CFR 1.18 decrease significantly and the publication fee set forth in 37 CFR 1.18(d)(1) decreases to $0.

If an issue fee or publication fee has been previously paid in this application, applicant is not entitled to a refund of the difference between the amount paid and the amount in effect on January 1, 2014.

Notice of Allowability	Application No. 13/539,466	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed on 09/27/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-5 and 7-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/27/2013
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 09/27/2013 has been entered.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 09/27/2013 was filed after the mailing date of the Notice of Allowance on 11/27/2012. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

Claims 1-5 and 7-20 stand allowed for the reasons articulated in the Office Action mailed on 11/27/2013.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Friday from 8 a.m. to 5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 11/27/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/27/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$0	$0	$1770	02/27/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001544

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 11/27/2012
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$0	$0	$1770	02/27/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1002, Page 001545

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

60909 7590 11/27/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/27/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1002, Page 001546

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Notice of Allowability	Application No.	Applicant(s)	
	13/539,466	POLISHCHUK ET AL.	
	Examiner	Art Unit	
	NIKOLAY YUSHIN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed on 11/10/2012*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-5 and 7-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
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5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Examiner, Art Unit 2893

DETAILED ACTION

Status of Claims

Applicant's cancellation of claim 6 in the reply filed on 11/10/2012 is acknowledged.

Applicant's amendment of claims 1 and 8-10 in the reply filed on 11/10/2012 is acknowledged.

Claims 1-5 and 7-20 are under consideration in this Office Action.

Allowable Subject Matter

Claims 1-5 and 7-20 are allowed.

The following is an examiner's statement of reasons for allowance:

In re Claim 1, Levy et al., US 2009/0179253 taken with Zheng et al., US 6,912,163 and Yan, US 2008/0135946 discloses all limitations of claim 1 except for " a high work function gate electrode formed over a surface of the ONNO stack; and a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode." Therefore, the claimed differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 10, Levy taken with Zheng and Yan discloses all limitations of claim 10 except for " a high work function gate electrode formed over a surface of the ONNO stack, wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer." Therefore, the claimed differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 11, prior-art fails to disclose semiconductor device comprising: a memory transistor including "an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer." Therefore, the claimed differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 18, prior-art fails to disclose semiconductor device comprising: a memory transistor including "a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region; a tunnel dielectric layer abutting the vertical channel." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Friday from 8 a.m. to 5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/THOMAS L DICKEY/
Primary Examiner, Art Unit 2826

/NIKOLAY YUSHIN/
Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 01/23/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 01/23/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/620,071	09/14/2012	Krishnaswamy Ramkumar	PM07024C2	7190

TITLE OF INVENTION: METHOD OF FABRICATING A NONVOLATILE CHARGE TRAP MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	04/23/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001552

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 01/23/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

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13/620,071	09/14/2012	Krishnaswamy Ramkumar	PM07024C2	7190

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EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001553

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 01/23/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

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Sandisk Technologies, Inc. - Ex. 1002, Page 001554

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/620,071	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/11/14*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *17-21,23-28,30 and 31*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/11/14
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

Sandisk Technologies, Inc. - Ex. 1002, Page 001556

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 10/27/2014

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
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DATE MAILED: 10/27/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Sandisk Technologies, Inc. - Ex. 1002, Page 001557

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(Depositor's name)
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EXAMINER	ART UNIT	CLASS-SUBCLASS
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Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001558

UNITED STATES PATENT AND TRADEMARK OFFICE

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Sandisk Technologies, Inc. - Ex. 1002, Page 001559

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/620,071	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9/5/14*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *17-21,23-28,30 and 31*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

THANH T NGUYEN
Primary Examiner
Art Unit: 2893

The present application is being examined under the pre-AIA first to invent provisions.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 17-21, 23-28, 30-31 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in subjecting the substrate to a radical oxidation process to form a first portion of a dielectric layer on the first exposed crystal plane and a second portion of the dielectric layer on the second exposed crystal plane, wherein the thickness of the first portion of the dielectric layer is approximately equal to the thickness of the second portion of the dielectric layer, wherein the radical oxidation process comprises flowing hydrogen (H_2) and oxygen (O_2) gas into the oxidation chamber, forming radicals at a surface of the first exposed crystal plane and second exposed crystal plane without an ignition event to pyrolyze the H_2 and O_2, and consuming portions of the first exposed crystal plane and second exposed crystal plane, to form the dielectric layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/THANH T NGUYEN/

Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 02/18/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 02/18/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/159,315	01/20/2014	Igor Polishchuk	PM07027D1CIP1C1	1041

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/18/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001564

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 02/18/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/159,315	01/20/2014	Igor Polishchuk	PM07027D1CIP1C1	1041

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/18/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-326000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001565

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/159,315	01/20/2014	Igor Polishchuk	PM07027D1CIP1C1	1041

60909 7590 02/18/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 02/18/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001566

Notice Requiring Inventor's Oath or Declaration	Application No. 14/159,315	Applicant(s) Igor Polishchuk	
	Examiner YUSHIN, NIKOLAY K	Art Unit 2893	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) MUST be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

- A properly executed inventor's oath or declaration has not been received for the following inventor(s): **Igor Polishchuk**, **Sagy Charel Levy**, and **Krishnaswamy Ramkumar**.
  Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/159,315	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendments filed on 12/19/2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *21-23, 31-32, 35-37, and 39-40* . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

Sandisk Technologies, Inc. - Ex. 1002, Page 001569

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of Claims

Applicant's cancellation of claims 1- 20, 24-30, 33-34, and 38 in the reply filed on 12/19/2014 is acknowledged.

Applicant's amendment of claims 21, 31, 35, 39 and 40 in the reply filed on 12/19/2014 is acknowledged.

Claims 21-23, 31-32, 35-37, and 39-40 are under consideration in this Office Action.

Allowable Subject Matter

Claims 21-23, 31-32, 35-37, and 39-40 are allowed.

The following is an examiner's statement of reasons for allowance:

In re Claim 21, Hagemeyer et al., US 2006/00taken with Levy et al., US2009/0179253 and Yan, US 2008/0135946 discloses all limitations of claim 21 except for that "an oxygen-lean second nitride layer disposed above the oxygen-rich first nitride layer." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 31, prior-art fails to disclose a semiconductor device "wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the oxygen-rich first nitride layer from the oxygen-lean second nitride layer." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 35, prior-art fails to disclose a semiconductor device comprising "a gate electrode disposed about the ONNO stack, abutting the blocking dielectric layer, wherein the gate electrode comprises doped polysilicon." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Friday from 9 a.m. to 6 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 03/23/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 03/23/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/159,315	01/20/2014	Igor Polishchuk	PM07027D1CIP1C1	1041

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/23/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001573

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 03/23/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/159,315	01/20/2014	Igor Polishchuk	PM07027D1CIP1C1	1041

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/23/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-326000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001574

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/159,315	01/20/2014	Igor Polishchuk	PM07027D1CIP1C1	1041

60909 7590 03/23/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 03/23/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001575

Notice Requiring Inventor's Oath or Declaration	Application No. 14/159,315	Applicant(s) Igor Polishchuk	
	Examiner YUSHIN, NIKOLAY K	Art Unit 2893	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) MUST be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

- A properly executed inventor's oath or declaration has not been received for the following inventor(s): **Igor Polishchuk**, **Sagy Charel Levy**, and **Krishnaswamy Ramkumar**.
  Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/159,315	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed on 03/10/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *21-23,31,32,35-37,39 and 40*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
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4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

Sandisk Technologies, Inc. - Ex. 1002, Page 001578

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 03/10/2012 has been entered.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 03/10/2012 was filed after the mailing date of the Notice of Allowance on 02/18/2015. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

Claims 21-23, 31-32, 35-37, and 39-40 stand allowed in spite of the Opinion of PCT that has been made in respect to an original set of claims.

The following is an examiner's statement of reasons for allowance:

In re Claim 21, Hagemeyer et al., US 2006/00taken with Levy et al., US2009/0179253 and Yan, US 2008/0135946 discloses all limitations of claim 21 except for that "an oxygen-lean second nitride layer disposed above the oxygen-rich first nitride layer." Therefore, the claimed

device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 31, prior-art fails to disclose a semiconductor device "wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the oxygen-rich first nitride layer from the oxygen-lean second nitride layer." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 35, prior-art fails to disclose a semiconductor device comprising "a gate electrode disposed about the ONNO stack, abutting the blocking dielectric layer, wherein the gate electrode comprises doped polysilicon." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Friday from 9 a.m. to 6 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 11/27/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGO, NGAN V

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/27/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/307,858	06/18/2014	Igor Polishchuk	PM07027D1C1	7201

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/29/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001582

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 11/27/2015
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/307,858	06/18/2014	Igor Polishchuk	PM07027D1C1	7201

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	02/29/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2819	438-287000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001583

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/307,858	06/18/2014	Igor Polishchuk	PM07027D1C1	7201

60909 7590 11/27/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGO, NGAN V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/27/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001584

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/307,858	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2819	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the terminal disclaimer filed 10-28-15*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *21-40*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NGAN NGO/
Primary Examiner, Art Unit 2819

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 07/19/2016

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 07/19/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/811,346	07/28/2015	Igor Polishchuk	PM07027D1CIP1C2	6244

TITLE OF INVENTION: METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/19/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

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IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1002, Page 001587

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 07/19/2016
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/811,346	07/28/2015	Igor Polishchuk	PM07027D1CIP1C2	6244

TITLE OF INVENTION: METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/19/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-326000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Sandisk Technologies, Inc. - Ex. 1002, Page 001588

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/811,346	07/28/2015	Igor Polishchuk	PM07027D1CIP1C2	6244

60909 7590 07/19/2016

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 07/19/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

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Sandisk Technologies, Inc. - Ex. 1002, Page 001589

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/811,346	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed on 06/17/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *21-40*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____.
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Specification

The amendment to the specification filed 06/17/2016 has been entered.

Allowable Subject Matter

Claims 21-40 are allowed.

The following is an examiner's statement of reasons for allowance:

In re Claim 21, prior-art fails to disclose a method comprising "forming a tunnel dielectric layer over a channel region formed from a silicon containing layer projecting from a surface of a substrate." Therefore, the claimed method differs from prior art methods on this point and there is no evidence it would have been obvious to make this change.

In re Claim 29, prior-art fails to disclose a method comprising "forming a channel region in a silicon nanowire suspended layer over the surface of the substrate, the channel region connecting a source and a drain in the substrate." Therefore, the claimed method differs from prior art methods on this point and there is no evidence it would have been obvious to make this change.

In re Claim 35, prior-art fails to disclose a method comprising "forming on an inside sidewall of the tunnel dielectric layer a vertical channel comprising a semiconducting material extending from to the first doped diffusion region formed on the surface of the substrate through the opening to a top surface of the stack of layers." Therefore, the claimed method differs from prior art methods on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on 8 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM2007027	5484

60909 7590 06/09/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, DILINH P	
ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
06/09/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/152,518	POLISHCHUK ET AL.	
	Examiner	Art Unit	
	DILINH P. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-15, drawn to a semiconductor device, classified in class 257, subclass 324.

   II. Claims 16-20, drawn to a method for making a semiconductor device, classified in class 438, subclass 216.

2. The inventions are distinct, each from the other because of the following reasons:

3. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially process, such as a different product of claim 1 can be made without forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor logic transistor is to be formed.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

5. The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

6. In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder**. Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DILINH P. NGUYEN whose telephone number is (571)

272-1712. The examiner can normally be reached on 9:00 AM - 6:30 PM (Monday-Thursday).

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571) 272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DLN
6/3/10

/Sue A. Purvis/
Supervisory Patent Examiner, Art Unit 2826

UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/307,858	06/18/2014	Igor Polishchuk	PM07027D1C1	7201

60909 7590 05/18/2015

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGO, NGAN V

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
05/18/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Office Action Summary	Application No. 14/307,858	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) 1-20 are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

Restriction to one of the following inventions is required under 35 U.S.C. § 121:

I. Claims 1-15, drawn to a semiconductor device, classified in Subgroup H01L29/00.

II. Claims 16-20, drawn to a process for making a semiconductor device, classified in in Subgroup H01L21/00.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (M.P.E.P. § 806.05(f)). In the instant case the device of the group I invention could be made by processes materially different than those of the group II invention. For example, the device in claim 1 does not need the step of "forming an oxide layer…in a second region" in process claim 16.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable

over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an

allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngan Ngo whose telephone number is (571)272-1711. The examiner can normally be reached on 9AM-6PM Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

May 13, 2015

Electronic Acknowledgement Receipt

EFS ID:	29021170
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	25-APR-2017
Filing Date:	26-OCT-2016
Time Stamp:	14:25:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C3_IDS_NPL_04212017.pdf	1054631 3125b74a6239b58aa561ccbb91404dbde6166393	no	5

Warnings:

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A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Non Patent Literature	33V64Kx18SynchronousQuadPortStaticRAM_03272001.pdf	5331132 10f30e97b0be444e1ee7fe6576cdd4b0ffd18a24	no	36
Warnings:					
Information:					
3	Non Patent Literature	HuaChingChen_TwobitSONOSTypeFlash_06172005.pdf	177703 9acb9cf3b9119d31b4aea2eb032c9fe55dbc6228	no	2
Warnings:					
Information:					
4	Non Patent Literature	Hung_HighPerformanceGateAllAroundPolycrystalline_04222011.pdf	749557 f3721dd7cd9ae4832a151edc61d5724d6e0f8356	no	4
Warnings:					
Information:					
5	Non Patent Literature	KrishnaswamyRamkumar_CypressSONOSTechnology_07062011.pdf	1368082 93b18715cb90ece242a258f91a272ab450643c97	no	9
Warnings:					
Information:					
6	Non Patent Literature	PM07027D1CIP1_NOA_11132013.pdf	417795 8f33494 3f276f091104bba9cd7d11fe12ce1844e	no	9
Warnings:					
Information:					
7	Non Patent Literature	PM07027D1CIP1_NOA_11272012.pdf	427095 aae576a0c033ef13aed38ce64c0364d4d7dbea3e	no	8
Warnings:					
Information:					

8	Non Patent Literature	PM07024C2_NOA_01232015.pdf	356455 8b3e731976bb4d56220d570f121b26aa3afbce12	no	5
Warnings:					
Information:					
9	Non Patent Literature	PM07024C2_NOA_10272014.pdf	415414 ea2212adb23c7347233e0d58a74ea23180889a37	no	7
Warnings:					
Information:					
10	Non Patent Literature	PM07027D1CIP1C1_NOA_02182015.pdf	471952 954eecbab212eebd36052c5c235cb88fbddd388c	no	9
Warnings:					
Information:					
11	Non Patent Literature	PM07027D1CIP1C1_NOA_03232015.pdf	486470 12f337518472ccc5c940967a0cc2a2412a73bf7f	no	9
Warnings:					
Information:					
12	Non Patent Literature	PM07027D1C1_NOA_11272015.pdf	357542 af532d22e50645420ff5d43db157eb43cde56dd4	no	5
Warnings:					
Information:					
13	Non Patent Literature	PM07027D1CIP1C2_NOA_07192016.pdf	430152 2fdf409e0eb5ec80ebb503d329acda77c694e904	no	7
Warnings:					
Information:					
14	Non Patent Literature	PM07027_RestrictionRequirement_06092010.pdf	181538 11696deb25794d9cb3a96c3967b2477a27be02c5	no	5
Warnings:					
Information:					

15	Non Patent Literature	PM07027D1C1_RestrictionRequirement_05182015.pdf	241950 3e8bc7266ffd04146f960058e72f89d315e40c69	no	7
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			Total Files Size (in bytes):	12467468	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/335,180	Filing Date 10/26/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	**280**
☒ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	**600**
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	**720**
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	* 0	x $80 =	**0**
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	* 0	x $420 =	**0**
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	**1600**

APPLICATION AS AMENDED – PART II

AMENDMENT	12/19/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
AJAY R. DAVID

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3	6223

60909 7590 05/17/2017

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198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
05/17/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 001611

Office Action Summary	Application No. 15/335,180	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/26/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-40* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21- 33, 35, 38 and 40* is/are rejected.

8)☒ Claim(s) *34,36,37 and 39* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☒ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *10/26/2016* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *See Continuation Sheet*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Continuation of Attachment(s) 2). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :04/24/2017; 04/25/2017; 04/25/2017; 04/25/2017.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "a multi-layer blocking layer" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

[[~~METHOD OF MANUFACTURING FOR~~]] MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Claim Objections

Claim 21 is objected to because of the following informalities:

Claim 1 recites the limitation "**the** multi-layer charge trapping layer" in line 7. There is insufficient antecedent basis for this limitation in the claim.

For purposes of a prompt examination the examiner (based on a similarity with claims 33 and 38) reads claim 21 as the following:

"21. A memory device, comprising: a gate structure; a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and a tunnel dielectric layer, a multi-layer [[~~blocking~~]] charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel, wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 21-32 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 21 recites the limitation "**the** multi-layer charge trapping layer" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claims 22-32 are rejected as being dependent on the rejected claim 21.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21, 22, 29, 31, and 32 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Kim et al., US 2008/0272424.

In re Claim 21, Kim discloses a memory device (Fig. 2), comprising: a gate structure 250; a channel 204 positioned between and electrically connecting a first diffusion region (left 202) and a second diffusion region (right 202); and a tunnel dielectric layer 210, a multi-layer [[~~blocking~~]] charge trapping layer (220, 230), and a blocking dielectric layer 240 disposed between the gate structure 250 and the channel 204, wherein the multi-layer charge trapping layer comprises a first dielectric layer 230 disposed abutting a second dielectric layer 230, wherein the first dielectric layer 230 includes oxygen-rich nitride ([0042]) and the second dielectric layer 220 includes oxygen-lean nitride ([0041]) (Fig. 2; [0040-0044]).

In re Claim 22, Kim discloses the memory device of claim 21, wherein the channel, first (202 left) and second (202 right) diffusion regions are formed at least partially within a semiconductor material structure 200 (Fig. 2).

In re Claim 29, Kim discloses the memory device of claim 21, wherein the gate structure 250 includes a high work function gate electrode ([0044]).

In re Claim 31, Kim discloses the memory device of claim 29, wherein the high work function gate electrode 250 comprises a P+ doped polysilicon layer ([0044]).

In re Claim 32, Kim discloses the memory device of claim 21, wherein the blocking dielectric layer 240 comprises high K high temperature oxide (HTO) ([0043]).

Claims 21, 22 and 26 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Wang, US 2006/0113586.

In re Claim 21, Wang discloses a memory device, comprising: a gate structure (506 in Fig. 5; 606 in Fig. 6); a channel (500 in Fig. 5; 600 in Fig. 6) positioned between and electrically

connecting a first diffusion region (501 in Fig. 5; 601 in Fig. 6) and a second diffusion region (502 in Fig. 5; 602 in Fig. 6); and a tunnel dielectric layer (503 in Fig. 5; 603 in Fig. 6), a multi-layer [[~~blocking~~]] charge trapping layer ((504, 504a) in Fig. 5; (604a, 604b) in Fig. 6), and a blocking dielectric layer (505 in Fig. 5; 605 in Fig. 6) disposed between the gate structure (506 in Fig. 5; 606 in Fig. 6) and the channel (500 in Fig. 5; 600 in Fig. 6), wherein the multi-layer charge trapping layer ((504, 504a) in Fig. 5; (604a, 604b) in Fig. 6) comprises a first dielectric layer (504 in Fig. 5; 604b in Fig. 6) disposed abutting a second dielectric layer (504a in Fig. 5; 604a in Fig. 6), wherein the first dielectric layer (504 in Fig. 5; 604b in Fig. 6) includes oxygen-rich nitride and the second dielectric layer (504a in Fig. 5; 604a in Fig. 6) includes oxygen-lean nitride (Figs. 2, 5 and 6; [0026-0028], [0031-0032]).

In re Claim 22, Wang discloses the memory device of claim 21, wherein the channel (500 in Fig. 5; 600 in Fig. 6), first (501 in Fig. 5; 601 in Fig. 6) and second (502 in Fig. 5; 602 in Fig. 6) diffusion regions are formed at least partially within a semiconductor material structure (shown as 200 in Fig. 2).

In re Claim 26, Wang discloses the memory device of claim 21, wherein the first dielectric layer (504 in Fig. 5; 604b in Fig. 6) is disposed abutting the tunnel dielectric layer (503 in Fig. 5; 603 in Fig. 6) and inherently substantially trap free, and wherein the second dielectric layer (504a in Fig. 5; 604a in Fig. 6) is disposed abutting the blocking dielectric layer (505 in Fig. 5; 605 in Fig. 6) (Figs. 2, 5 and 6; [0026-0028], [0031-0032]). It is inherently because according to MPEP2112.01 — WHEN THE STRUCTURE RECITED IN THE REFERENCE IS SUBSTANTIALLY IDENTICAL TO THAT OF THE CLAIMS, CLAIMED PROPERTIES OR FUNCTIONS ARE PRESUMED TO BE INHERENT Where the claimed and prior art products

are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). In the instant case Wang's structure being identical to the claimed product, claimed property substantially trap free is inherent.

Claims 21, 26, 27, 29, and 31 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Lue et al., US 2007/0029625 (corresponding to US 7,576,386).

In re Claim 21, Lue discloses a memory device, comprising: a gate structure (125 in Fig. 1A; 225 in Fig. 1B); a channel (105 in Fig. 1A; 205 in Fig. 1B) positioned between and electrically connecting a first diffusion region (104 in Fig. 1A; 204 in Fig. 1B) and a second diffusion region (112 in Fig. 1A; 212 in Fig. 1B); and a tunnel dielectric layer (120 in Fig. 1A; 220 in Fig. 1B), a multi-layer [[~~blocking~~]] charge trapping layer ((124, 131, 132) in Fig. 1A; (224, 231, 232) in Fig. 1B), and a blocking dielectric layer (133 in Fig. 1A; 233 in Fig. 1B) disposed between the gate structure (125 in Fig. 1A; 225 in Fig. 1B) and the channel (105 in Fig. 1A; 205 in Fig. 1B), wherein the multi-layer charge trapping layer ((124, 131, 132) in Fig. 1A; (224, 231, 232) in Fig. 1B) comprises a first dielectric layer (124 in Fig. 1A; 224 in Fig. 1B) disposed abutting a second dielectric layer (132 in Fig. 1A; 232 in Fig. 1B), wherein the first dielectric layer (124 in Fig. 1A; 224 in Fig. 1B) includes oxygen-rich nitride (Silicon Oxynitride ([0031]) and the second dielectric layer (132 in Fig. 1A; 232 in Fig. 1B) includes oxygen-lean nitride (silicon nitride ([0032])) (Figs. 1; [0027-0052]).

In re Claim 26, Lue discloses the e memory device of claim 21, wherein the first dielectric layer (124 in Fig. 1A; 224 in Fig. 1B) is disposed abutting the tunnel dielectric layer (120 in Fig. 1A; 220 in Fig. 1B) and inherently substantially trap free, and wherein the second dielectric layer (132 in Fig. 1A; 232 in Fig. 1B) is disposed abutting the blocking dielectric layer (133 in Fig. 1A; 233 in Fig. 1B).

In re Claim 27, Lue discloses the memory device of claim 26, wherein the multi-layer charge trapping layer ((124, 131, 132) in Fig. 1A; (224, 231, 232) in Fig. 1B) further comprises an anti-tunneling layer (131 in Fig. 1A; 231 in Fig. 1B) disposed between the first and second dielectric layers, and wherein the anti-tunneling layer (131 in Fig. 1A; 231 in Fig. 1B) includes an oxide layer ([0032]; [0043]).

In re Claim 29, Lue discloses the memory device of claim 21, wherein the gate structure (125 in Fig. 1A; 225 in Fig. 1B) includes a high work function gate electrode.

In re Claim 31, Lue discloses the memory device of claim 29, wherein the high work function gate electrode (125 in Fig. 1A; 225 in Fig. 1B) comprises a P+ doped polysilicon layer.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 21, 23, and 24 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya, US 2006/0284236, in view of Kim et al., US 2008/0272424.

In re Claim 21, Bhattacharyya discloses a memory device 140 (Fig. 1B), comprising: a gate structure 152; a channel 148 positioned between and electrically connecting a first diffusion region 144 and a second diffusion region 146; and a tunnel dielectric layer 158, a multi-layer [[~~blocking~~]] charge trapping layer 160, and a blocking dielectric layer 162 disposed between the gate structure 152 and the channel 148 (Figs 1; [0047-0063])

Bhattacharyya does not disclose that the multi-layer charge trapping layer 160 comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.

The only difference between the Applicants' claim 21 and Bhattacharyya's reference is in the specified structure of the multi-layer charge trapping layer 160.

Kim discloses a memory device (Fig. 2), comprising: a gate structure 250; a channel 204 positioned between and electrically connecting a first diffusion region (left 202) and a second diffusion region (right 202); and a tunnel dielectric layer 210, a multi-layer [[~~blocking~~]] charge trapping layer (220, 230), and a blocking dielectric layer 240 disposed between the gate structure 250 and the channel 204, wherein the multi-layer charge trapping layer comprises a first dielectric layer 230 disposed abutting a second dielectric layer 230, wherein the first dielectric layer 230 includes oxygen-rich nitride ([0042]) and the second dielectric layer 220 includes oxygen-lean nitride ([0041]) (Fig. 2; [0040-0044]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Bhattacharyya's multi-layer charge trapping layer 160 with Kim's multi-layer charge trapping layer comprises a first dielectric layer 230 disposed abutting a second dielectric layer 230, wherein the first dielectric layer 230 includes oxygen-rich nitride ([0042]) and the second dielectric layer 220 includes oxygen-lean nitride ([0041]), to have a fast erase speed and improve retention characteristics as taught by Kim ([0003]).

In re Claim 23, Bhattacharyya taken with Kim discloses the memory device of claim 21, wherein the channel 148, first 144 and second diffusion 146 regions are disposed above a semiconductor material structure 142 (Bhattacharyya: Fig. 1B).

In re Claim 24, Bhattacharyya taken with Kim discloses the memory device of claim 21, wherein the channel 148, first 144 and second 146 diffusion regions are suspended above a semiconductor material structure 142 (Bhattacharyya: Fig. 1B).

Claims 28 and 30 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya and Kim as applied to claim 21 above, and further in view of Forbes, US 2007/0233007 (corresponding to US 7,425,491).

In re Claim 28, Bhattacharyya taken with Kim discloses all limitations of claim 28 except for that the channel includes a silicon nanowire channel.

Forbes teaches that a channel includes a silicon nanowire channel 507-C (Figs. 5-7; [0008-0009], [024-0033]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute the channel in Bhattacharyya – Kim's memory device with Forbes' silicon nanowire channel, to reduce the size of devices as taught by Forbes ([0003]).

In re Claim 30, Bhattacharyya taken with Kim and Forbes discloses the memory device of claim 28, further comprising: a gate-all-around (GAA) structure 510 wherein the silicon nanowire channel 507-C is enclosed on all four sides by the gate structure 510 (Figs. 5).

Claims 33 and 35 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hagemeyer et al., US 20060008959, in view of Wang.

In re Claim 33, Hagemeyer discloses a semiconductor device (Fig. 1I), comprising: a memory device (120a, 114a, 102, 117, 112, 108, 109, 103, 104, 114b, 120b) including, a gate structure (109, 108) including a first high work function gate electrode 108, a channel (between 114a and 114b) positioned between and electrically connecting a first diffusion region (120a, 114a) and a second diffusion region (120b, 114b), and a tunnel dielectric layer 102, a charge trapping layer 104, and a blocking dielectric layer 107 disposed between the gate structure (108,

109) and the channel (a part of 101 between 114a and 114b); and a metal oxide semiconductor (MOS) logic device (119a, 117, 108, 109, 117) including a gate oxide layer 107 and a second high work function gate electrode 108 disposed thereon (Figs.1; [0012-0023]).

Hagemeyer does not discloses that the charge trapping layer 104 is the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.

The only difference between the Applicants' claim 33 and Hagemeyer's reference is in the specified structure of the multi-layer charge trapping layer 104.

Wang discloses a memory device, comprising: a gate structure (506 in Fig. 5; 606 in Fig. 6); a channel (500 in Fig. 5; 600 in Fig. 6) positioned between and electrically connecting a first diffusion region (501 in Fig. 5; 601 in Fig. 6) and a second diffusion region (502 in Fig. 5; 602 in Fig. 6); and a tunnel dielectric layer (503 in Fig. 5; 603 in Fig. 6), a multi-layer charge trapping layer ((504, 504a) in Fig. 5; (604a, 604b) in Fig. 6), and a blocking dielectric layer (505 in Fig. 5; 605 in Fig. 6) disposed between the gate structure (506 in Fig. 5; 606 in Fig. 6) and the channel (500 in Fig. 5; 600 in Fig. 6), wherein the multi-layer charge trapping layer ((504, 504a) in Fig. 5; (604a, 604b) in Fig. 6) comprises a first dielectric layer (504 in Fig. 5; 604b in Fig. 6) disposed abutting a second dielectric layer (504a in Fig. 5; 604a in Fig. 6), wherein the first dielectric layer (504 in Fig. 5; 604b in Fig. 6) includes oxygen-rich nitride and the second dielectric layer (504a in Fig. 5; 604a in Fig. 6) includes oxygen-lean nitride (Figs. 2, 5 and 6; [0026-0028], [0031-0032]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Hagemeyer's multi-layer charge trapping layer with Wang's multi-layer charge trapping layer, to improve charge retention characteristics as taught by Wang ([0006]).

In re Claim 35, Hagemeyer taken with Wang discloses the semiconductor device of claim 33, wherein the MOS logic device (119a, 117, 108, 109, 117) (Hagemeyer: Fig. 1I) is formed at least partially within a semiconductor material structure 101.

Claim 38 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hagemeyer, in view of Kim.

In re Claim 38, Hagemeyer discloses a semiconductor device, comprising: a memory device (120a, 114a, 102, 117, 112, 108, 109, 103, 104, 114b, 120b) including, a gate structure (109, 108) including a first high work function gate electrode 108, a blocking dielectric layer 107 disposed abutting the gate structure (109, 108), wherein the channel (a part of 101 between 114a and 114b) is positioned between and electrically connecting a first diffusion region (114a, 120a) and a second diffusion region (114b, 120b); and a metal oxide semiconductor (MOS) logic device (119a, 117, 108, 109, 117) including a gate oxide layer 107 and a second high work function gate electrode 108 disposed thereon (Figs.1; [0012-0023]).

Hagemeyer does not discloses that charge trapping layer 104 disposed abutting the blocking dielectric layer 107 is a multi-layer charge trapping layer, wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric

layer includes oxygen-lean nitride, as well as a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer.

The only difference between the Applicants' claim 38 and Hagemeyer's reference is in the specified structure of the multi-layer charge trapping layer 104.

Kim discloses a memory device (Fig. 2), comprising: a gate structure 250; a channel 204 positioned between and electrically connecting a first diffusion region (left 202) and a second diffusion region (right 202); and a tunnel dielectric layer 210, a multi-layer [[~~blocking~~]] charge trapping layer (220, 230), and a blocking dielectric layer 240 disposed between the gate structure 250 and the channel 204, wherein the multi-layer charge trapping layer comprises a first dielectric layer 230 disposed abutting a second dielectric layer 230, wherein the first dielectric layer 230 includes oxygen-rich nitride ([0042]) and the second dielectric layer 220 includes oxygen-lean nitride ([0041]), a tunnel dielectric layer 210 disposed abutting the multi-layer charge trapping layer (220, 230) (Fig. 2; [0040-0044]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Hagemeyer's multi-layer charge trapping layer 104 with Kim's multi-layer charge trapping layer comprises a first dielectric layer 230 disposed abutting a second dielectric layer 230, wherein the first dielectric layer 230 includes oxygen-rich nitride ([0042]) and the second dielectric layer 220 includes oxygen-lean nitride ([0041]), to have a fast erase speed and improve retention characteristics as taught by Kim ([0003]).

Claims 38 and 40 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hagemeyer, in view of Lue.

In re Claim 38, Hagemeyer discloses a semiconductor device, comprising: a memory device (120a, 114a, 102, 117, 112, 108, 109, 103, 104, 114b, 120b) including, a gate structure (109, 108) including a first high work function gate electrode 108, a blocking dielectric layer 107 disposed abutting the gate structure (109, 108), wherein the channel (a part of 101 between 114a and 114b) is positioned between and electrically connecting a first diffusion region (114a, 120a) and a second diffusion region (114b, 120b); and a metal oxide semiconductor (MOS) logic device (119a, 117, 108, 109, 117) including a gate oxide layer 107 and a second high work function gate electrode 108 disposed thereon (Figs.1; [0012-0023]).

Hagemeyer does not discloses that charge trapping layer 104 disposed abutting the blocking dielectric layer 107 is a multi-layer charge trapping layer, wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride, as well as a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer.

The only difference between the Applicants' claim 38 and Hagemeyer's reference is in the specified structure of the multi-layer charge trapping layer 104.

Lue discloses a memory device, comprising: a gate structure (125 in Fig. 1A; 225 in Fig. 1B); a channel (105 in Fig. 1A; 205 in Fig. 1B) positioned between and electrically connecting a first diffusion region (104 in Fig. 1A; 204 in Fig. 1B) and a second diffusion region (112 in Fig. 1A; 212 in Fig. 1B); and a tunnel dielectric layer (120 in Fig. 1A; 220 in Fig. 1B), a multi-layer [[~~blocking~~]] charge trapping layer ((124, 131, 132) in Fig. 1A; (224, 231, 232) in Fig. 1B), and a blocking dielectric layer (133 in Fig. 1A; 233 in Fig. 1B) disposed between the gate structure

(125 in Fig. 1A; 225 in Fig. 1B) and the channel (105 in Fig. 1A; 205 in Fig. 1B), wherein the multi-layer charge trapping layer ((124, 131, 132) in Fig. 1A; (224, 231, 232) in Fig. 1B) comprises a first dielectric layer (124 in Fig. 1A; 224 in Fig. 1B) disposed abutting a second dielectric layer (132 in Fig. 1A; 232 in Fig. 1B), wherein the first dielectric layer (124 in Fig. 1A; 224 in Fig. 1B) includes oxygen-rich nitride (Silicon Oxynitride ([0031]) and the second dielectric layer (132 in Fig. 1A; 232 in Fig. 1B) includes oxygen-lean nitride (silicon nitride ([0032])) (Figs. 1; [0027-0052]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Hagemeyer's trapping layer 104 with Lue's multi-layer charge trapping layer, to improve charge retention as taught by Lue ([0008]).

In re Claim 40, Hagemeyer taken with Lue discloses the semiconductor device of claim 38, wherein the multi-layer charge trapping layer ((124, 131, 132) in Fig. 1A; (224, 231, 232) in Fig. 1B) further comprises an anti-tunneling layer (131 in Fig. 1A; 231 in Fig. 1B) disposed between the first (124 in Fig. 1A; 224 in Fig. 1B) and second (132 in Fig. 1A; 232 in Fig. 1B) dielectric layers, and wherein the anti-tunneling layer includes an oxide layer ([0032]; [0043]).

Allowable Subject Matter

Claims 34, 36, and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 25 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on 8 AM - 5 PM PST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

Notice of References Cited	Application/Control No. 15/335,180	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	Page 1 of 1

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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Signature	/Kin Hung Lai/	Date (YYYY-MM-DD)	2017-04-24
Name/Print	Kin Hung Lai	Registration Number	69251

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	Examiner Name	YUSHIN, NIKOLAY K
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Andrea Wheeler/	Date (YYYY-MM-DD)	2017-04-21
Name/Print	Andrea Wheeler	Registration Number	73780

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4667217	A	1987-05-19	Janning	Entire Document
	2	5773343	A	1998-06-30	Lee Sung et al.	Entire Document
	3	6001713	A	1999-12-14	Ramsbey et al.	Entire Document
	4	6518113	B1	2003-02-11	Buynoski	Entire Document
	5	6596590	B1	2003-07-22	Miura et al.	Entire Document
	6	6717860	B1	2004-04-06	Fujiwara	Entire Document
	7	7060594	B2	2006-06-13	Wang	Entire Document
	8	7279740	B2	2007-10-09	Bhattacharyya et al.	Entire Document

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	9	7646041	B2	2010-01-12	Chae et al.	Entire Document
	10	7692246	B2	2010-04-06	Dreeskornfeld et al.	Entire Document
	11	7927951	B2	2011-04-19	Kim et al.	Entire Document
	12	8008713	B2	2011-08-30	Dobuzinsky et al.	Entire Document
	13	8163660	B2	2012-04-24	Puchner et al.	Entire Document

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	1	2005093054		2005-05-05	Jung	Entire Document
	2	2005245034		2005-11-03	Fukuda et al.	Entire Document
	3	20060017092	A1	2006-01-26	Dong et al.	Entire Document
	4	20060051880	A	2006-03-09	Doczy et al.	Entire Document

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	5	20060081331	A1	2006-04-20	Campian	Entire Document
	6	20060228907	A1	2006-10-12	Cheng et al.	Entire Document
	7	2006113627		2006-06-01	Chen et al.	Entire Document
	8	2006220106	A	2006-10-05	Choi et al.	Entire Document
	9	20070012988	A	2007-01-18	Bhattacharyya	Entire Document
	10	20070272971	A	2007-11-29	Lee et al.	Entire Document
	11	20080087942	A1	2008-04-17	Hsu et al.	Entire Document
	12	20080237684	A1	2008-10-02	Specht et al.	Entire Document
	13	20080290398	A	2008-11-27	Polishchuk et al.	Entire Document
	14	2008150003		2008-06-26	Chen et al.	Entire Document
	15	2008237694		2008-10-02	Specht et al.	Entire Document

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	16	20090206385	A	2009-08-20	Kim et al.	Entire Document
	17	20090227116	A	2009-09-10	Joo Moon et al.	Entire Document
	18	20100252877	A1	2010-10-07	Nakanishi et al.	Entire Document

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	101517714	CN	A	2009-08-26	CYPRESS SEMICONDUCTOR CORP	Entire Document	
	2	101558481	CN	B	2012-05-30	Cypress Semiconductor Corporation	Entire Document	
	3	101859702	CN	A	2010-10-13	FREDERICK et al.	Entire Document	
	4	104254921	CN	A	2014-12-31	CYPRESS SEMICONDUCTOR CORP	Entire Document	
	5	1801478	CN	A	2006-07-12	TAIWAN SEMICONDUCTOR MFG	Entire Document	
	6	1832201	CN	A	2006-09-13	SAMSUNG ELECTRONICS CO LTD	Entire Document	

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	7	2005347679	JP		2005-12-15	RENESAS TECH CORP	Entire Document	
	8	2007318112	JP		2007-12-06	SEMICONDUCTOR ENERGY LAB	Entire Document	
	9	2007515060	JP	A	2007-06-07	Unknown	Entire Document	
	10	2009260070	JP		2009-11-05	TOSHIBA CORP	Entire Document	
	11	20040070669	KR	A	2004-08-11	ANAM SEMICONDUCTOR LTD	Entire Document	
	12	20060100092	KR		2006-09-20	LEE CHANG WON	Entire Document	
	13	200703671	TW	A	2007-01-16	MICRON TECHNOLOGY INC	Entire Document	
	14	200847343	TW	A	2008-12-01	Jenne et al.	Entire Document	
	15	2007064048	WO	A1	2007-06-07	Masuzaki et al.	Entire Document	
	16	2008129478	WO	A	2008-10-30	Huerta et al.	Entire Document	
	17	2011162725	WO	A1	2011-12-29	Singh et al.	Entire Document	

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	18	2013148112	WO	A1	2013-10-03	Jenne et al.	Entire Document	
	19	2013148343	WO	A1	2013-10-03	Levy et al.	Entire Document	

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	Chinese Office Action for Application Number 200880000820.3 (PM07024CN) dated 01/26/2011; 6 pages	
	2	SIPO Office Action for CN Application Number 201380031969.9 (PM07024CIP1CN) dated 08/19/2016; 8 pages	
	3	USPTO Advisory Action for Application Number 12/197,466 (PM07024C1) dated 01/31/2012; 3 pages	
	4	USPTO Advisory Action for Application Number 14/605,231 (PM07024CIP1C1) dated 03/09/2016; 3 pages	
	5	USPTO Advisory Action for Application Number 14/605,231 (PM07024CIP1C1) dated 07/05/2016; 3 pages	
	6	USPTO Final Rejection for Application Number 12/124,855 (PM07024) dated 01/31/2012; 7 pages	
	7	USPTO Final Rejection for Application Number 12/124,855 (PM07024) dated 05/10/2010; 11 pages	

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	8	USPTO Final Rejection for Application Number 12/197,466 (PM07024C1) dated 11/17/2011; 13 pages	
	9	USPTO Final Rejection for Application Number 14/307,858 (PM07027D1C1) dated 10/08/2015; 6 pages	
	10	USPTO Final Rejection for Application Number 14/605,231 (PM07024CIP1C1) dated 12/17/2015; 15 pages	
	11	USPTO Non Final Rejection for Application Number 13/539,458 (PM07024CIP1) dated 03/13/2013; 5 pages	
	12	USPTO Non Final Rejection for Application Number 13/539,458 (PM07024CIP1) dated 10/2/2014; 5 pages	
	13	USPTO Non Final Rejection for Application Number 13/620,071 (PM07024C2) dated 04/03/2014; 12 pages	
	14	USPTO Non Final Rejection for Application Number 13/620,071 (PM07024C2) dated 07/18/2014; 5 pages	
	15	USPTO Non-Final Rejection for Application Number 12/124,855 (PM07024) dated 01/18/2011; 5 pages	
	16	USPTO Non-Final Rejection for Application Number 12/124,855 (PM07024) dated 08/16/2011; 9 pages	
	17	USPTO Non-Final Rejection for Application Number 12/124,855 (PM07024) dated 10/29/2009; 9 pages	
	18	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 03/09/2011; 4 pages	

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	19	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 09/29/2010; 5 pages	
	20	USPTO Non-Final Rejection for Application Number 12/197,466 (PM07024C1) dated 06/01/2011; 11 pages	
	21	USPTO Non-Final Rejection for Application Number 13/288,919 (PM07027D1) dated 06/19/2014; 5 pages	
	22	USPTO Non-Final Rejection for Application Number 13/288,919 (PM07027D1) dated 12/05/2013; 4 pages	
	23	USPTO Non-Final Rejection for Application Number 13/539,466 (PM07027D1CIP1) dated 09/28/2012; 9 pages	
	24	USPTO Non-Final Rejection for Application Number 14/159,315 (PM07027D1CIP1C1) dated 10/21/2014; 12 pages	
	25	USPTO Non-Final Rejection for Application Number 14/307/858 (PM07027D1C1) dated 06/29/2015; 5 pages	
	26	USPTO Non-Final Rejection for Application Number 14/605,231 (PM07024CIP1C1) dated 07/07/2015; 13 pages	
	27	USPTO Notice of Allowance for Application Number 12/124,855 (PM07024) dated 05/01/2012; 7 pages	
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	30	USPTO Notice of Allowance for Application Number 12/124,855 (PM07024) dated 08/01/2012; 7 pages	
	31	USPTO Notice of Allowance for Application Number 12/152,518 (PM07027) dated 07/14/2011; 6 pages	
	32	USPTO Notice of Allowance for Application Number 12/197,466 (PM07024C1) dated 06/15/2012; 4 pages	
	33	USPTO Notice of Allowance for Application Number 12/197,466 (PM07024C1) dated 09/24/2012; 8 pages	
	34	USPTO Notice of Allowance for Application Number 13/288,919 (PM07027D1) dated 04/28/2014; 5 pages	
	35	USPTO Notice of Allowance for Application Number 13/288,919 (PM07027D1) dated 07/08/2014; 5 pages	
	36	USPTO Notice of Allowance for Application Number 13/288,919 (PM07027D1) dated 08/26/2014; 7 pages	
	37	USPTO Notice Of Allowance for Application Number 13/539,458 (PM07024CIP1) dated 05/24/2013; 8 pages	
	38	USPTO Notice of Allowance for Application Number 13/539,458 (PM07024CIP1) dated 08/04/2014; 7 pages	
	39	USPTO Notice of Allowance for Application Number 13/539,458 (PM07024CIP1) dated 11/03/2014; 7 pages	
	40	USPTO Notice Of Allowance for Application Number 13/539,466 (PM07027D1CIP1) dated 09/04/2013; 9 pages	

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EXAMINER SIGNATURE

Examiner Signature	/NIKOLAY K YUSHIN/	Date Considered	05/08/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kin Hung Lai/	Date (YYYY-MM-DD)	2017-04-24
Name/Print	Kin Hung Lai	Registration Number	69251

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15335180	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/10/2017								
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Sandisk Technologies, Inc. - Ex. 1002, Page 001684

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15335180	POLISHCHUK ET AL.
	Examiner	**Art Unit**
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✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/10/2017								
	37	✓								
	38	✓								
	39	O								
	40	✓								

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15335180	POLISHCHUK ET AL.
	Examiner	Art Unit
	NIKOLAY YUSHIN	2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/0676; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518; H01L29/66833; H01L29/7926; H01L29/792	05/10/2017	NY
B82Y10/00	05/10/2017	NY

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Keyword, inventor names, assignee searching - see search history	05/10/2017	NY

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893

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CONFIRMATION NO. 6223

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/335,180	10/26/2016 RULE	257	2893	PM07027D1CIP1C3

APPLICANTS

Cypress Semiconductor Corporation, San Jose, CA

INVENTORS

Igor Polishchuk, Fremont, CA;
Sagy Charel Levy, Zichron Yaakov, ISRAEL;
Krishnaswamy Ramkumar, San Jose, CA;

**** CONTINUING DATA ***************************

This application is a CON of 14/811,346 07/28/2015 PAT 9502543
which is a CON of 14/159,315 01/20/2014 PAT 9093318
which is a CON of 13/539,466 07/01/2012 PAT 8633537
which is a CIP of 13/288,919 11/03/2011 PAT 8859374
which is a DIV of 12/152,518 05/13/2008 PAT 8063434
which claims benefit of 60/940,160 05/25/2007

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

11/03/2016

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	CA	13	20	3

35 USC 119(a-d) conditions met ☐ Yes ☑ No ☐ Met after Allowance

Verified and Acknowledged /NIKOLAY K YUSHIN/ Examiner's Signature _____ Initials

ADDRESS

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709
UNITED STATES

TITLE

METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1740	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	1	(11/397527).APP.	USPAT; USOCR	AND	ON	2017/05/10 17:00
S1	53	(("POLISHCHUK") near3 ("Igor")).INV.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 15:47
S2	85	(("LEVY") near3 ("Sagy")).INV.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 16:53
S4	173	(("RAMKUMAR") near3 ("Krishnaswamy")).INV.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 16:54
S5	239	(("CYPRESS") near3 ("SEMICONDUCTOR") near3 ("CORPORATION")).AANM.	USPAT	AND	ON	2017/05/08 16:54
S6	53	(("POLISHCHUK") near3 ("Igor")).INV.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 16:54
S7	68	(("POLISHCHUK") near3 ("Igor")).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:54
S8	140	(("LEVY") near3 ("Sagy")).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:55
S9	260	(("RAMKUMAR") near3 ("Krishnaswamy")).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:55
S10	470	(("CYPRESS") near3 ("SEMICONDUCTOR") near3 ("CORPORATION")).AANM.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:55
S11	6260	(("CYPRESS") near3 ("SEMICONDUCTOR")).AS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	AND	ON	2017/05/08 16:55

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			DERWENT; IBM_TDB			
S12	177	(S7 OR S8 Or S9) AND (S10 OR S11)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:56
S13	145	S12 AND memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:56
S14	31	(memory gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 17:00
S15	4	(memory gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/08 17:00
S16	6	((14/811346) or (15/335180) or (14/159315) or (14/811346) or (13/288919) or (12/152518)).APP.	US-PGPUB; USPAT	OR	OFF	2017/05/08 17:03
S17	4	((14/811346) or (15/335180) or (14/159315) or (14/811346) or (13/288919) or (12/152518)).APP.	USPAT	OR	OFF	2017/05/08 17:03
S18	43	("20030122204" | "20030169629" | "20050186741" | "20050230766" | "20060008959" | "20060131636" | "20060202261" | "20070231991" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080135946" | "20080175053" | "20080290399" | "20080291726" | "20080293207" | "20090039414" | "20090045452" | "20090179253" | "20100041222" | "20100117138" | "20100117139" | "20100155823" | "20100295118" | "20110248332" | "6287913" | "6906390" | "6912163" | "7642585" | "7688626" | "7713810" | "7723789" | "7737488" | "7790516" | "7948799" | "7999295" | "8063434" | "8222688" | "8264028" | "8315095" | "8482052" | "8859374").PN. OR ("9502543").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 17:05
S19	64	("20030122204" | "20050230766" | "20060131636" | "20070246753" | "20070262451" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080290399" |	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 17:06

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		"20100041222" | "20100295118" | "6906390" | "6912163" | "7312496" | "7323742" | "7737488" | "7790516").PN. OR ("8063434").URPN.				
S20	330	((("20020154878") or ("20030227049") or ("20040104424") or ("20040227198") or ("20040251489") or ("20050098839") or ("20050224866") or ("20050245034") or ("20050266637") or ("20060113627") or ("20060192248") or ("20060220106") or ("20060237803") or ("20070051306") or ("20080150003") or ("20080286927") or ("20080293254") or ("20090179253") or ("20100041222") or ("20100117139") or ("20120068159") or ("5404791") or ("5500816") or ("5847411") or ("6023093") or ("6153543") or ("6162700") or ("6287913") or ("6429081") or ("6445030") or ("6833582") or ("6913961") or ("7250654") or ("7312496") or ("7601576") or ("7737488") or ("7790516") or ("8063434") or ("8067284") or ("8143129") or ("8264028") or ("8283261") or ("8860122") or ("7060594") or ("20040207002") or ("4104424") or ("4251489") or ("20060202263") or ("20070049048") or ("20070210371") or ("20080293207") or ("8029399") or ("20080296664") or ("20090045452") or ("20090294844") or ("20090302365") or ("20100117138") or ("20110018053") or ("20110237060") or ("4395438") or ("5405791") or ("6074915") or ("6136654") or ("6586349") or ("6670241") or ("6835621") or ("7084032") or ("7372113") or ("7390718") or ("7544565") or ("7588986") or ("7670963") or ("7713810") or ("8071453") or ("8318608") or ("8643124") or ("8993453") or ("9306025") or ("20070272971") or ("20090227116") or ("7927951") or ("20030183869") or ("20040183091") or ("20040183122") or ("20050056892") or ("20050205920") or ("20050227501") or ("20050230766") or ("20060228841") or ("20060261401") or ("6051880") or ("20070031999") or ("20070048916") or ("20070231991") or ("20080009115") or ("20080237694") or ("20090011609") or ("9152618") or ("2068250") or ("4843023") or ("4870470") or ("5793089") or ("6140187") or ("6277683") or ("6297173") or ("6399484") or ("6406960") or ("6444521") or ("6461899") or ("6661065") or ("6746968") or ("6818558") or ("7012299") or ("7018868") or ("7098154") or ("7238990") or ("7301185") or ("7315474") or ("7323742") or ("7521751") or ("7612403") or ("7646637") or ("8093128") or ("8222688") or ("8940645") or ("20060017092") or ("6001713") or ("6518113") or ("6717860") or ("7692246") or ("20010052615") or ("20030123307") or ("20030169629") or ("20040071030") or	US-PGPUB; USPAT	OR	OFF	2017/05/08 17:26

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		("20040129988")).PN. or (("20050070126") or ("20050079659") or ("20050236679") or ("20050275010") or ("20060008959") or ("20060228899") or ("20070029625") or ("20080048237") or ("20080135946") or ("20080293255") or ("8087942") or ("20100295118") or ("20110163371") or ("2007167") or ("4257832") or ("5408115") or ("5550078") or ("5817170") or ("6015739") or ("6025267") or ("6174774") or ("6297096") or ("6709928") or ("6713127") or ("6917072") or ("6946349") or ("6958511") or ("7115469") or ("7463530") or ("7479425") or ("7910429") or ("8710578") or ("9502543") or ("5245034") or ("20060051880") or ("20080290398") or ("20090206385") or ("20020141237") or ("20030122204") or ("20030124873") or ("3123307") or ("20040227196") or ("20050026637") or ("20050116279") or ("20060065919") or ("6261401") or ("20070200168") or ("20070262451") or ("20070268753") or ("7121380") or ("20080290400") or ("20090039414") or ("20090242969") or ("20130175604") or ("20140264551") or ("4490900") or ("5972765") or ("6114734") or ("6127227") or ("6157426") or ("6268299") or ("6365518") or ("6440797") or ("6586343") or ("6787419") or ("7033890") or ("7253046") or ("7450423") or ("7482236") or ("7576386") or ("7879738") or ("7948799") or ("8482052") or ("8633537") or ("8859374") or ("9355849") or ("20080087942") or ("8150003") or ("5773343") or ("3183869") or ("20050186741") or ("20060160303") or ("20060202261") or ("6081331") or ("20070121380") or ("20080121932") or ("20080146042") or ("20080272424") or ("20090152621") or ("20100155823") or ("0096687") or ("0283097") or ("20110248332") or ("5348903") or ("5464783") or ("5939333") or ("6217658") or ("6218700") or ("6335288") or ("6348380") or ("6468927") or ("6469343") or ("6602771") or ("6610614") or ("6677213") or ("6768856") or ("7015100") or ("7045424") or ("7338869") or ("7365389") or ("7535053") or ("7642585") or ("7999295") or ("8315095") or ("9349824") or ("20060228907") or ("8237694") or ("7279740") or ("20040067619") or ("20040094793") or ("20040129986") or ("20040173918") or ("20050110064") or ("20060111805") or ("60131636") or ("20060226490") or ("20060281331") or ("20070215940") or ("20070272916") or ("20080057644") or ("20080290399") or ("9294836") or ("4543707") or ("5573963") or ("5861347") or ("5937323")).PN. or (("6147014") or ("6150286") or ("6321134") or ("6624090") or ("6730566") or ("6768160") or					

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		("6774433") or ("6903422") or ("6906390") or ("7033957") or ("7042054") or ("0711248") or ("7172940") or ("7262457") or ("7688626") or ("20060081331") or ("6113627") or ("6220106") or ("4667217") or ("8008713") or ("20020020890") or ("20020109138") or ("20030030100") or ("4094793") or ("20050093054") or ("20050141168") or ("5026637") or ("20050275012") or ("20060113586") or ("20070066087") or ("20070246753") or ("20070267687") or ("20080175053") or ("20080258203") or ("20080291726") or ("8054346") or ("7248332") or ("20130309826") or ("20160300724") or ("5972804") or ("6020606") or ("6214689") or ("6433383") or ("6559026") or ("6599795") or ("6884681") or ("6912163") or ("7410857") or ("7636257") or ("7714379") or ("7723789") or ("9093318") or ("9449831") or ("5093054") or ("20070012988") or ("20080237684") or ("20100252877") or ("6596590") or ("7646041") or ("8163660")).PN.				
S21	44	((oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/08 17:30
S22	34	((oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride)) AND S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/08 17:31
S23	3	(("20090179253") or ("6912163") or ("20080135946")).PN.	US-PGPUB; USPAT	OR	OFF	2017/05/08 17:36
S24	31	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:15
S25	40	(tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:16
S26	41	(tunnel dielectric multi$1layer (charge ADJ trap$6) (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:16
S27	44	(multi$1layer (charge ADJ trap$6)	US-PGPUB;	AND	ON	2017/05/08

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		(oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			21:16
S28	44	((charge ADJ trap$6) (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:16
S29	44	((oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:16
S30	958	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:17
S31	930	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:17
S32	7	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/08 21:17
S33	354	S31 AND (H01L29/0676; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518; H01L29/66833; H01L29/7926).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:18
S39	933	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:01
S40	19	S39 AND (H01L29/0676).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	AND	ON	2017/05/09 09:01

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			IBM_TDB			
S41	68	S39 AND (H01L29/4234).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:02
S42	23	S39 AND (H01L29/4916).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:08
S43	34	S39 AND (H01L29/511).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:08
S44	215	S39 AND (H01L29/66833).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:08
S45	110	S39 AND (H01L29/7926).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:09
S46	276	S39 AND (H01L29/792).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:10
S47	422	S39 AND (H01L29/0676; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518; H01L29/66833; H01L29/7926; H01L29/792).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:10
S48	70	S39 AND (B82Y10/00).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:11
S49	0	("20090179253").PN.	USPAT	OR	OFF	2017/05/09 09:33
S50	1	("20090179253").PN.	US-PGPUB;	OR	OFF	2017/05/09

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			USPAT			09:33
S51	1	("20080135946").PN.	US-PGPUB; USPAT	OR	OFF	2017/05/09 09:35
S52	1	("20060008959").PN.	US-PGPUB; USPAT	OR	OFF	2017/05/09 09:35
S53	1	(("6912163") or ("20070272916") or ("20070268753")).PN.	USPAT	OR	OFF	2017/05/09 09:43
S54	3	(("6912163") or ("20070272916") or ("20070268753")).PN.	US-PGPUB; USPAT	OR	OFF	2017/05/09 09:43
S55	1	(11/830582).APP.	USPAT; USOCR	AND	ON	2017/05/09 09:50
S56	0	(11/811958).APP.	USPAT; USOCR	AND	ON	2017/05/09 09:55
S57	14	("20060261401" | "20080258203" | "6709928" | "20030123307" | "6445030" | "7450423" | "7042054" | "4543707" | "6157426" | "6677213" | "6958511" | "20020154878" | "6461899" | "6818558").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/09 09:57
S58	1	(11/131006).APP.	USPAT; USOCR	AND	ON	2017/05/09 10:08
S61	2	((oxygen$1rich ADJ nitride) (nitrogen$1rich ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 12:07
S62	7	("20020185711" | "20060113586" | "20080272424" | "20080293207" | "20100157680" | "20110101442" | "8222688").PN. OR ("9537016").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/09 12:12
S63	0	(10/998445).APP.	USPAT; USOCR	AND	ON	2017/05/09 12:18
S64	1	("5,371,734").PN.	US-PGPUB; USPAT	OR	OFF	2017/05/10 07:53
S65	1	("5,924,080").PN.	US-PGPUB; USPAT	OR	OFF	2017/05/10 07:56
S66	24	("2008/0272424").URPN.	USPAT	AND	ON	2017/05/10 14:17
S67	24	("2008/0272424").URPN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/10 14:17
S68	238	("20090179253" | "20030227049" | "20040104424" | "20050098839" | "20050224866" | "20050245034" | "20050266637" | "20060113627" | "20060192248" | "20060220106" | "20070051306" | "20080286927" | "20090039414" | "20100041222" | "5500816" | "6023093" | "6153543" | "6162700" | "6445030" | "6833582" | "6913961" | "7250654" | "7312496" | "7601576" | "7737488" | "7790516" |	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/10 14:22

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		"8063434" | "8067284" | "8143129" | "8283261" | "7060594" | "7799670" | "20040207002" | "4104424" | "4251489" | "20060202263" | "20070049048" | "20070210371" | "20070272971" | "20080293207" | "8029399" | "20080296664" | "20090302365" | "20100117138" | "4395438" | "5405791" | "6074915" | "6136654" | "6586349" | "6670241" | "6835621" | "7084032" | "7372113" | "7544565" | "7588986" | "7670963" | "8318608" | "20090227116" | "6297096" | "7910429" | "20040183122" | "20050205920" | "20050230766" | "20060228841" | "6051880" | "20070031999" | "20070048916" | "20080009115" | "20090011609" | "4843023" | "6140187" | "6277683" | "6297173" | "6399484" | "6406960" | "6429081" | "6444521" | "6518113" | "6661065" | "6746968" | "7012299" | "7018868" | "7098154" | "7238990" | "7301185" | "7315474" | "7323742" | "7521751" | "7612403" | "7646637" | "8222688" | "20010052615" | "20030169629" | "20040071030" | "20050070126" | "20050236679" | "20050275010" | "5245034" | "20060228899" | "6113586" | "20070029625" | "20080048237" | "20080135946" | "20080290398" | "20080293255" | "20100295118" | "5408115" | "5793089" | "5817170" | "6015739" | "6025267" | "6174774" | "6713127" | "6917072" | "6958511" | "7115469" | "7463530" | "7479425" | "8093128" | "6946349" | "20060017092" | "20030122204" | "20030124873" | "3123307" | "20040227196" | "6065919" | "20070262451" | "20070268753" | "20080087942" | "8150003" | "9011609" | "4490900" | "5972765" | "6114734" | "6268299" | "6365518" | "6586343" | "6787419" | "7253046" | "7482236" | "7576386" | "7879738" | "20090243001" | "20130175604" | "20080290400" | "6127227" | "6440797" | "7033890" | "7390718" | "3183869" | "20050186741" | "20060160303" | "6081331" | "20070121380" | "20080146042" | "8237694" | "20090152621" | "20110248332" | "5404791" | "5464783" | "5939333" | "6217658" | "6218700" | "6335288" | "6348380" | "6468927" | "6602771" | "6610614" | "6677213" | "6768856" | "7015100" | "7045424" | "7338869" | "7365389" | "7535053" | "7999295" | "7279740" | "6946349" | "20040067619" | "20040094793" | "20040129986" | "20040173918" | "20060111805" | "20060131636" | "20060226490" | "20060281331" | "6113627" | "20070272916" | "20080057644" | "20080290399" |						

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		"4870470" | "5573963" | "5861347" | "5937323" | "6147014" | "6150286" | "6321134" | "6730566" | "6768160" | "6774433" | "6903422" | "6906390" | "7033957" | "7042054" | "7112486" | "7172940" | "7262457" | "8008713" | "20130175600" | "20130178031" | "20110237060" | "20090179253" | "20020020890" | "4094793" | "20050141168" | "5026637" | "20050275012" | "5093054" | "20070066087" | "20070246753" | "20070267687" | "7048916" | "20080258203" | "20080272424" | "20100252877" | "5972804" | "6020606" | "6214689" | "6433383" | "6559026" | "6599795" | "6884681" | "6912163" | "7410857" | "7636257" | "7714379" | "7723789" | "20130175504").PN.				
S69	64	(gate channel tunnel dielectric block$6 (charge ADJ trap$6) layer) AND S68	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/10 14:23
S70	1	(11/197668).APP.	USPAT; USOCR	AND	ON	2017/05/10 14:38
S71	1004	(Yushin NEAR3 Nikolay).xp. OR (Yushin NEAR3 Nikolay).xa.	USPAT; USOCR	AND	ON	2017/05/10 16:01
S72	1004	(Yushin NEAR3 Nikolay).xp. OR (Yushin NEAR3 Nikolay).xa.	USPAT	AND	ON	2017/05/10 16:01
S73	14	S72 AND (channel silicon nanowire)	USPAT	SAME	ON	2017/05/10 16:01
S74	7	S72 AND (channel (silicon ADJ nanowire))	USPAT	SAME	ON	2017/05/10 16:02
S75	2	(11/397527).APP.	US-PGPUB; USPAT	OR	OFF	2017/05/10 16:03
S76	1	S75 AND (channel (silicon ADJ nanowire))	USPAT	SAME	ON	2017/05/10 16:04
S77	1	S75 AND (channel (silicon ADJ nanowire))	USPAT	AND	ON	2017/05/10 16:04

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

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	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	1	Japanese Office Action for Japanese Application Number 2013-549612 (PM07002CIP1JP) dated 08/04/2015; 8 pages	
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	3	SIPO Office Action for Application Number 200910134374.1 (PM07002CN) dated 01/21/2015; 5 pages	
	4	SIPO Office Action for Application Number 200910134374.1 (PM07002CN) dated 02/03/2016; 2 pages	
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	Attorney Docket Number	PM07027D1CIP1C3

	12	SIPO Office Action for Application Number 201280000107.5 (PM07002CIP1CN) dated 11/29/2016; 5 pages	
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	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kin Hung Lai/	Date (YYYY-MM-DD)	2017-04-24
Name/Print	Kin Hung Lai	Registration Number	69251

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Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/StoychoDDraganoff#56181/	Date (YYYY-MM-DD)	2017-05-25
Name/Print	Stoycho D. Draganoff	Registration Number	56181

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Espacenet

Bibliographic data: CN1107254 (A) — 1995-08-23

Process and apparatus for producing semiconductor integrated circuit

Inventor(s): ENAMI HIROMICHI [JP]; KATSUYAMA KIYOMI [JP]; KATSUYAMA MASANORI [JP] ± (HIROMICHI ENAMI, ; KIYOMI KATSUYAMA, ; MASANORI KATSUYAMA)

Applicant(s): HITACHI LTD [JP] ± (HITACHI, LTD)

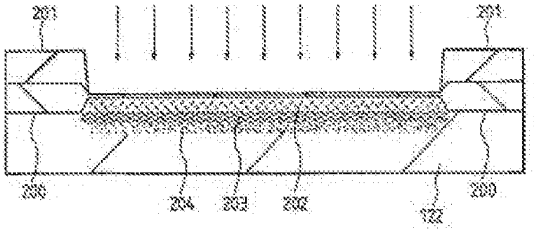
Classification: - international: ***H01L21/00; H01L21/265; H01L21/30; H01L21/302; H01L21/3065; H01L21/324;*** (IPC1-7): H01L21/322; H01L21/324; H01L21/70
- cooperative: **H01L21/3003**; **H01L21/67069**; **H01L21/67167**; **H01L21/67213**

Application number: CN1994119855 19941129

Priority number (s): JP19930300397 19931130

Also published as: JPH07153769 (A) TW269738 (B) US5543336 (A)

Abstract not available for CN1107254 (A)
Abstract of corresponding document: US5543336 (A)



A chamber 103 for introducing hydrogen without causing serious damage to a semiconductor wafer and a chamber 104 for eliminating the hydrogen introduced into the semiconductor wafer at relatively low temperature are installed at the succeeding stage of a plasma etching unit for effectively correcting the damage caused by plasma etching and ion implantation to a semiconductor substrate or an ion implanting unit. In order to introduce hydrogen into the semiconductor wafer without serious damage, a mixture of hydrocarbon gas and oxygen gas for accelerating the decomposition of the hydrocarbon gas is used for forming hydrogen radicals in a plasma and the hydrogen radicals are supplied to the semiconductor wafer at room temperature by a downstream system. The semiconductor wafer is heat-treated in an atmosphere of a vacuum or inactive gas in a

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temperature region of 200 DEG -500 DEG C. to eliminate the hydrogen introduced into the semiconductor wafer.

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AFD China
INTELLECTUAL PROPERTY LAW OFFICE

[redacted]

April 25, 2017

[redacted]

Attn.: [redacted]
Murgitroyd & Company-Glasgow

Via Email Only
[redacted]

Re: National Phase in China of PCT/US2013/032339
In the name of Cypress Semiconductor Corporation
Title: Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers
CN Application No.: 2013800168932
Your Ref.: [redacted]
Our Ref.: [redacted]
Deadline for Responding to this Office Action: July 6, 2017 (Beijing Time)
Issue date: April 21, 2017 (Beijing Time); 2 months rejection

Dear Mr. Schouten:

The State Intellectual Property Office of China recently has issued the Second Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below with our recommendation.

Examiner's Opinions in this OA

Part I. Inventiveness – Claims 1-20

[AFD remarks: The Examiner's comments on the inventiveness of claims 2-7, 10-14 and 16-20 are substantially the same as those in the First Office Action. We just copy the corresponding comments in the First Office Action for your reference.]

1. Claim 1

The Examiner points out that claim 1 does not possess inventiveness over Reference 1 (US8063434B1) in view of Reference 7 (CN1107254A, August 23, 1995), and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3), the Examiner admits

[redacted]

that the distinguishing technical feature of the technical scheme in claim 1 is the following:

"the annealed blocking dielectric layer comprising a top surface in which a number of traps has been reduced by steam annealing".

The Examiner holds that Reference 7 (see lines 17-20 on page 2 of its Description) discloses relevant technical feature. It can be seen that Reference 7 discloses that the steam annealing can reduce the defects and improve the stability of the interface state, which provides technical teaching for applying the technical feature into the blocking dielectric layer to reduce the defect of the interface. And thus on the basis of Reference 1 in combination of Reference 7, the technical scheme of claim 1 is obvious to a person skilled in the art. 2. Claims 2-3

2. Claims 2-3

The Examiner points out that claims 2-3 do not possess inventiveness either. The Examiner holds that the additional technical features of claims 2-3 constitute the distinguishing technical features over Reference 1, and Reference 2 (US2008/0048237A1) (see paragraph 132 of its Description) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1 to solve the technical problem. And thus on the basis of Reference 1 in combination of Reference 2, the technical schemes of claims 2-3 are obvious to a person skilled in the art.

3. Claim 4

The Examiner points out that claim 4 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 4 constitutes the distinguishing technical features over Reference 1, and Reference 3 (CN1801478A) (see lines 9-15 on page 2 of its Description and Figs. 1a-1b and 2c) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1 to solve the technical problem. And thus on the basis of Reference 1 in combination of Reference 3, the technical scheme of claim 4 is obvious to a person skilled in the art.

4. Claim 5

The Examiner points out that claim 5 does not possess inventiveness either. The Examiner holds that compared with the disclosure of Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3), the distinguishing technical feature in claim 5 is that "*the memory device comprises a non-planar transistor including a gate having multiple surfaces abutting the channel"*, and Reference 3 (see lines 9-15 on page 2 of its Description and Figs. 1a-1b and 2c) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1 to solve the technical problem. And thus on the basis of Reference 1 in combination of Reference 3, the technical scheme of claim 5 is obvious to a person skilled in the art.

5. Claims 6-7

The Examiner points out that claims 6-7 do not possess inventiveness either. The Examiner holds that Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3) discloses relevant technical features. Additionally, it is conventional technical means of a person skilled in the art that a gate layer is metal materials, and the blocking dielectric is a high K dielectric material. And thus the technical schemes of claims 6-7 do not possess inventiveness on the condition that the claims they refer to do not possess inventiveness.

6. Claim 8

The Examiner points out that claim 8 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 8 is disclosed by Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3, especially lines 42-47 in column 3). And thus the technical scheme of claim 8 does not possess inventiveness on the condition that claim 1 it refers to does not possess inventiveness.

7. Claim 9

The Examiner points out that claim 9 does not possess inventiveness over Reference 1 in view of Reference 4 (US6709928B1), Reference 7 and known common knowledge in the art, and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3), the Examiner indicates that a charge trapping oxynitride layer 318A is equivalent to a second oxynitride layer in the present application, and a trap free oxynitride layer 318B is equivalent to a first oxynitride layer in the present application, and admits that the distinguishing technical features of the technical scheme in claim 9 are the following:

(1) "a gate having multiple surfaces abutting the channel";

(2) "the first oxynitride layer is separated from the second oxynitride layer by an anti-tunneling layer comprising an oxide"; and

(3) "the annealed blocking dielectric layer comprising a top surface in which a number of traps has been reduced by steam annealing".

The Examiner holds that:

As for the distinguishing technical feature (1), a fence and a gate of fin-type field effect transistor are conventional structures of gates, in such two gate structures, there are more contact surfaces of the gate and the channel, and thus it can strengthen the control effect of the gate on the channel to some extent to ease short channel effect. Thus such technical distinguishing technical feature is conventional technical means of a person skilled in the art

to avoid short channel effect.

As for the distinguishing technical feature (2), Reference 4 (see lines 28-35 in column 4 and lines 37-47 in column 5 of its Description and Fig. 2B) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1 to solve the technical problem.

As for the distinguishing technical feature (3), Reference 7 (see lines 17-20 on page 2 of its Description) discloses relevant technical feature. It can be seen that Reference 7 discloses that steam annealing can reduce the defects and improve the stability of the interface state, which provides technical teaching for applying the technical feature into the blocking dielectric layer to reduce the defect of the interface.

And thus on the basis of Reference 1 in combination of Reference 4, Reference 7 and known common knowledge in the art, the technical scheme of claim 9 is obvious to a person skilled in the art.

6 *[sic, 8]*. Claim 10

The Examiner points out that claim 10 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 10 constitutes the distinguishing technical feature over Reference 1, and Reference 3 (see lines 9-15 on page 2 of its Description and Figs. 1a-1b and 2c) discloses relevant technical features, which provides technical teaching for applying the technical features into Reference 1 to solve the technical probme. And thus the technical scheme of claim 10 does not possess inventiveness on the condition that claim 9 it refers to does not possess inventiveness.

7 *[sic, 9]*. Claims 11-12

The Examiner points out that claims 11-12 do not possess inventiveness either. The Examiner holds that Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3) discloses relevant technical features. Additionally, it is conventional technical means of a person skilled in the art that the gate layer is metal material, the blocking dielectric is a high K dielectric material and the transistor is FinFET. And thus the technical schemes of claims 11-12 do not possess inventiveness on the condition that claim 9 they refer to does not possess inventiveness.

8 *[sic, 10]*. Claim 13

The Examiner points out that claim 13 does not possess inventiveness either. The Examiner holds that Reference 5 (CN101558481A) (see Claim 4, lines 26-30 on page 3, paragraph 4 on page 4 of its Description and Fig. 4B) discloses relevant technical features. And thus the technical scheme of claim 13 does not possess inventiveness on the condition that claim 9 it refers to does not possess inventiveness.

9 *[sic, 11]*. Claim 14

The Examiner points out that claim 14 does not possess inventiveness either. The

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Examiner holds that Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3, especially lines 42-47 in column 3) discloses relevant technical features. And thus the technical scheme of claim 14 does not possess inventiveness on the condition that claim 9 it refers to does not possess inventiveness.

10 *[sic, 12]*. Claim 15

The Examiner points out that claim 15 does not possess inventiveness over Reference 6 (WO2011/162725A1) in view of Reference 1 and Reference 7 and thus is not in conformity with the provisions of Article 22(3) of Patent Law.

Comparing with the disclosure of Reference 6 (see paragraphs 128-132 of its Description and Fig. 6), the Examiner indicates that a carrier 602 is equivalent to semiconducting material in the present application, a drain region 614a is equivalent to a second diffusion region in the present application, a source region 614b is equivalent to a first diffusion region in the present application and a gate insulator region 610 is equivalent to a tunnel oxide layer in the present application, and admits that the distinguishing technical features of the technical scheme in claim 15 are the following:

(1) "a multi-layer charge storing layer abutting the tunnel oxide layer, the multi-layer charge storing layer including a first oxynitride layer comprising an oxygen-rich nitride closer to the tunnel oxide layer, and a second charge-trapping layer comprising a silicon-rich, oxygen-lean nitride overlying the first oxynitride layer, wherein the second charge-trapping layer comprises a majority of a charge traps distributed in split charge-trapping region" and "blocking dielectric layer on the second charge-trapping layer"; and

(2) "the annealed blocking dielectric layer comprising a top surface in which a number of traps has been reduced by steam annealing".

The Examiner holds that

As for the distinguishing technical feature (1), Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3) discloses relevant technical features, providing technical teaching for applying the technical features into Reference 1.

As for the distinguishing technical feature (2), Reference 7 (see lines 17-20 on page 2 of its Description) discloses relevant technical feature. It can be seen that Reference 7 discloses that the steam annealing can reduce the defects and improve the stability of the interface state, which provides technical teaching for applying the technical feature into the blocking dielectric layer to reduce the defect of the interface.

And thus on the basis of Reference 6 in combination of Reference 1 and Reference 7, the technical scheme of claim 15 is obvious to a person skilled in the art.

11 *[sic, 13]*. Claim 16

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The Examiner points out that claim 16 does not possess inventiveness either. The Examiner holds that Reference 6 (see paragraphs 128-132 of its Description and Fig. 6) discloses relevant technical features. And thus the technical scheme of claim 16 does not possess inventiveness on the condition that claim 15 it refers to does not possess inventiveness.

12 *[sic, 14]*. Claim 17

The Examiner points out that claim 17 does not possess inventiveness either. The Examiner holds that Reference 4 (see lines 28-35 in column 4 and lines 37-47 in column 5 of its Description and Fig. 2B) discloses relevant technical features. And thus the technical scheme of claim 17 does not possess inventiveness on the condition that claim 16 it refers to does not possess inventiveness.

13 *[sic, 15]*. Claim 18

The Examiner points out that claim 18 does not possess inventiveness either. The Examiner holds that it is conventional technical means of a person skilled in the art that the blocking dielectric is a high K dielectric material. And thus the technical scheme of claim 18 does not possess inventiveness on the condition that claim 16 it refers to does not possess inventiveness.

14 *[sic, 16]*. Claim 19

The Examiner points out that claim 19 does not possess inventiveness either. The Examiner holds that Reference 4 (see lines 28-35 in column 4 and lines 37-47 in column 5 of its Description and Fig. 2B) discloses relevant technical features. And thus the technical scheme of claim 19 does not possess inventiveness on the condition that claim 18 it refers to does not possess inventiveness.

15 *[sic, 17]*. Claim 20

The Examiner points out that claim 20 does not possess inventiveness either. The Examiner holds that the additional technical feature of claim 20 is disclosed by Reference 1 (see lines 38-46 in column 2, lines 42-47 in column 3 and lines 43-63 in column 8 of its Description and Fig. 3, especially lines 42-47 in column 3). And thus the technical scheme of claim 20 does not possess inventiveness on the condition that claim 15 it refers to does not possess inventiveness.

Part II. With respect to the applicant's observation

The Examiner conducts the supplement search and adds Reference 7, it discloses that the steam annealing can reduce the defects and improve the stability of the interface state. Thus, Reference 7 provides technical teaching for applying the technical feature into the blocking dielectric layer to reduce the defect of the interface.

Conclusive opinion

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Based on the above opinions, the Examiner also holds, as marked in the form of this Office Action, that the application does not possess any patentable substantial contents, and if the applicant fails to expound reasons or the reasons expounded are not sufficient, this application will be rejected.

This generally is a conclusive opinion of the Examiner and in next the Examiner is likely to issue a final rejection if the response to this Action is not persuasive or no substantial amendments are made.

Our Comments and Recommendations

[redacted]

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Electronic Acknowledgement Receipt

EFS ID:	29319355
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	25-MAY-2017
Filing Date:	26-OCT-2016
Time Stamp:	19:10:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C3_IDS_05252017.pdf	1053850 20bdc1884a190b26a4b9c26416e981fc464248bb	no	4

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2	Foreign Reference	CN1107254.pdf	110756 e58c6a0ba2368e4a0a240a49fbe6fbea4a935bca	no	2
Warnings:					
Information:					
3	Non Patent Literature	PM07002CIP2CN_SIPOOA_04212017.pdf	247988 6411e3fbe69692178c152452fe0fccdb1f1fc7fd	no	7
Warnings:					
Information:					
		Total Files Size (in bytes):	1412594		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Examiner: Yushin, Nikolay K.
Polishchuk et al.	Art Group: 2893
Application No.: 15/335,180	Confirmation No.: 6223
Filed: October 26, 2016	
For: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION

In response to the Non-Final Office Action mailed 05/17/2017 (hereinafter "the Office Action") for the patent application referenced above (hereinafter "the Application"), please enter the following amendments and consider the following remarks.

Amendments begin on page 2 of this paper.

Remarks begin on page 8 of this paper.

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SPECIFICATION AMENDMENT

The Applicant respectfully submits amendment to the title of Instant Application to "~~METHOD OF MANUFACTURING FOR~~ MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE".

DRAWINGS

The Office Action objects to drawings under 37 CFR 1.83(a) as the "multi-layer blocking layer" in at least claim 21 is allegedly not shown.

The Applicant respectfully submits that **claim 21** has been amended to correct a minor typographical error and the term "multi-layer blocking layer" has been replaced by "multi-layer charge trapping layer", which is shown at least in FIG. 4A. Therefore, the Applicant respectfully requests the objection to drawings be withdrawn.

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AMENDMENTS TO THE CLAIMS:

Please amend the claims of the patent application as set forth below wherein new text is indicated with underlining and deleted text is indicated with strikethrough or with [[double-brackets]]:

What is claimed is:

1-20. (Canceled)

21. (Currently Amended) A memory device, comprising:

a gate structure;

a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and

a tunnel dielectric layer, a multi-layer charge trapping ~~blocking~~ layer, and a blocking dielectric layer disposed between the gate structure and the channel,

wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer[[,]] and an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer, and wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.

22. (Previously Presented) The memory device of claim 21, wherein the channel, first and second diffusion regions are formed at least partially within a semiconductor material structure.

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23. (Previously Presented) The memory device of claim 21, wherein the channel, first and second diffusion regions are disposed above a semiconductor material structure.

24. (Previously Presented) The memory device of claim 21, wherein the channel, first and second diffusion regions are suspended above a semiconductor material structure.

25. (Previously Presented) The memory device of claim 21, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure.

26. (Previously Presented) The memory device of claim 21, wherein the first dielectric layer is disposed abutting the tunnel dielectric layer and substantially trap free, and wherein the second dielectric layer is disposed abutting the blocking dielectric layer.

27. (Canceled)

28. (Previously Presented) The memory device of claim 21, wherein the channel includes a silicon nanowire channel.

29. (Previously Presented) The memory device of claim 21, wherein the gate structure includes a high work function gate electrode.

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30. (Previously Presented) The memory device of claim 28, further comprising:

a gate-all-around (GAA) structure wherein the silicon nanowire channel is enclosed on all four sides by the gate structure.

31. (Previously Presented) The memory device of claim 29, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.

32. (Previously Presented) The memory device of claim 21, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO).

33. (Currently Amended) A semiconductor device, comprising:

a memory device including,

a gate structure including a first high work function gate electrode,

a channel positioned between and electrically connecting a first diffusion region and a second diffusion region, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and

a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel, wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer

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includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride; and

a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.

34. (Canceled)

35. (Previously Presented) The semiconductor device of claim 33, wherein the MOS logic device is formed at least partially within a semiconductor material structure.

36. (Previously Presented) The semiconductor device of claim 35, wherein the channel is vertical and oriented substantially orthogonal to the semiconductor material structure.

37. (Currently Amended) The semiconductor device of claim [[34]] 33, wherein the first dielectric layer of the multi-layer charge trapping layer is disposed abutting the tunnel dielectric layer and substantially trap free, and wherein the second dielectric layer is disposed abutting the blocking dielectric layer.

38. (Currently Amended) A semiconductor device, comprising:

a memory device including,

a gate structure including a first high work function gate electrode,

a blocking dielectric layer disposed abutting the gate structure,

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a multi-layer charge trapping layer disposed abutting the blocking dielectric layer, wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride,

a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer, and

a channel disposed abutting the tunnel dielectric layer, wherein the channel is positioned between and electrically connecting a first diffusion region and a second diffusion region, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and

a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.

39. (Currently Amended) The semiconductor device of claim 38, ~~wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and~~ wherein the MOS logic device is formed at least partially on the semiconductor material structure.

40. (Previously Presented) The semiconductor device of claim 38, wherein the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first and second dielectric layers, and wherein the anti-tunneling layer includes an oxide layer.

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REMARKS

The Examiner is thanked for the performance of a thorough search and examination.

The Office Action rejects **claims 21-33, 35, 38, and 40**, and objects to **claims 34, 36-37, and 39**. In this response, **claims 21, 33, and 37-39** have been amended. No claim is added and **claims 27 and 34** are canceled herein. Therefore, the Applicant presents **claims 21-23, 24-33, and 35-40** for examination.

Claim Amendments

The amendments to the claims are fully supported by the specification as originally filed, and no new matter will be added by entry of the amendment. The Applicant has amended the claims, not because the Applicant agrees with the rejections or objections, but to clarify the subject matter that the Applicant intended to claim, to correct minor typographical errors, and/or to correct minor antecedent basis errors. The amendments to the claims are made to satisfy Applicant's preferences, not necessarily to satisfy any legal requirement(s) of the patent laws. The amendments clarify the claims and are not intended to limit the scope of equivalents to which any claim element may be entitled.

The proposed amendments and/or issues raised in the Office Action are addressed hereinafter.

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Allowable Subject Matter

The Office Action states that **claims 34, 36, and 39** contain allowable subject matter and will be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Office Action also states that **claim 25** contains allowable subject matter and will be allowable if the 112 rejection is overcome.

The Applicant thanks the Examiner for identifying allowable subject matter. The Applicant does not agree or disagree with the Office Action's reasons for such identification, and will acknowledge as such.

Claim Objection

The Office Action objects to **claim 21** because of an alleged informality. More specifically, the Office Action states that "the multi-layer charge-trapping layer" in line 7 lacks antecedent basis.

The Applicant respectfully submits that **claim 21** has been amended to correct a minor typographical error in line 5, in which "a multi-layer blocking layer" has been amended to "a multi-layer charge trapping layer". The Applicant respectfully requests the objection be withdrawn.

Claims Rejections – 35 USC § 112

The Office Action rejects **claims 21-32** under 35 USC 112(b) or 35 USC 112 (pre-AIA), second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter.

The Applicant respectfully submits that **claim 21** has been amended to correct a minor typographical error in line 5, in which "a multi-layer blocking layer" has been

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amended to "a multi-layer charge trapping layer". The Applicant respectfully requests the 112 rejection be withdrawn.

Claims Rejections – 35 USC § 102

The Office Action rejects **claims 21-22, 29, 31, and 32** under pre-AIA 35 USC 102(b) as allegedly being anticipated by U.S. Patent Application Publication No. US 2008/0272424 by Kim et al. (hereinafter "Kim").

The Office Action rejects **claims 21-22 and 26** under pre-AIA 35 USC 102(b) as allegedly being anticipated by U.S. Patent Application Publication No. US 2006/0113586 by Wang (hereinafter "Wang").

The Office Action rejects **claims 21, 26-27, 29, and 31** under pre-AIA 35 USC 102(b) as allegedly being anticipated by U.S. Patent Application Publication No. US 2007/0029625 by Lue et al. (hereinafter "Lue").

Claim 21

Features of **claim 21** includes:

> A memory device, comprising:
> a gate structure;
> a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and
> a tunnel dielectric layer, a multi-layer charge trapping blocking layer, and a blocking dielectric layer disposed between the gate structure and the channel,
> wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and **an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer,** and wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.
> (**Emphasis** Added)

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To anticipate under 35 U.S.C. §102, the prior art reference "[M]ust not only disclose all elements within the four corners of the document, but must also **disclose those elements arranged as in the claim**". Net Moneyln, Inc. v. Verisign, Inc., 545 F.3d 1359, 1369 (Fed. Cir. 2008) (citation and internal quotation marks omitted) [**Emphasis** added]**.**

The Applicant respectfully submits that features of **claim 27** have been incorporated substantially into **claim 21**, and rejections of both claims will be addressed simultaneously herein. The Applicant further submits that **claim 27** is only rejected based on Lue. Therefore, amended **claim 21** overcomes the 102 rejection based on Kim and Wang, respectively. **Claims 22, 29, 31-32 and claims 22, 26** also overcome the 102 rejection based on Kim and Wang respectively because they depend from **claim 21**.

The Office Action alleges that Lue discloses all features of amended claim 21, the Applicant respectfully disagrees. The Office Action alleges that Lue discloses a multi-layer charge trapping layer (124, 131, 132 in FIG. 1A) or (224, 231, 232 in FIG. 1B), and an anti-tunneling layer 131 and 231 respectively in FIGS. 1A and 1B. See Office Action, pg. 8, ln. 6-10.

FIGS. 1A and 1B of Lue are produced herein for illustrative purposes.

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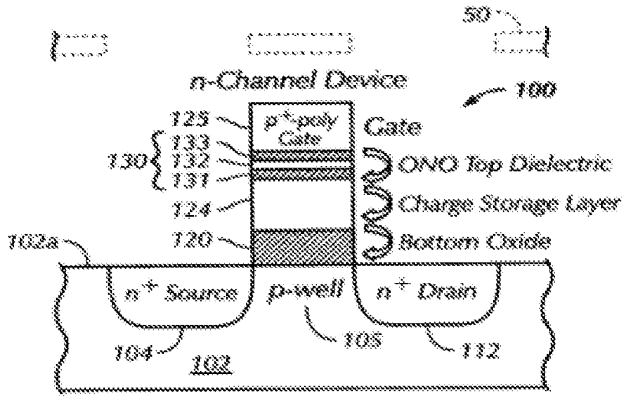
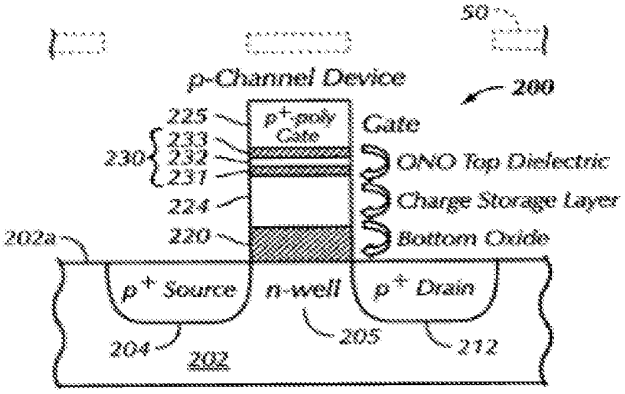


FIG. 1A



The Applicant respectfully submits that Lue does not disclose a multi-layer charge storage layer. Referring to Lue, as explicitly labeled in both FIGS. 1A and 1B, and their corresponding description, charge storage (trapping) layer 124 or 224 is **a single-layer structure**. Instead, Lue discloses a multi-layer "dielectric tunneling layer 130 functions as a tunneling dielectric for hole tunneling from the control gate 125 during an erase operation". See Lue, para. 33, ln. 1-3. Lue however does not disclose or even remotely suggest, as the Office Action appears to interpret, that the bottom two layers 131, 132 of the multi-layer dielectric tunneling layer 130 and the single-layer charge storage layer 124 forming a multi-layer charge trapping layer. On the contrary, Lue

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explicitly states that "Due to the reduced thickness of the first and second dielectric oxide layers 131, 133 and the dielectric nitride layer 132, **the dielectric tunneling layer 130 has negligible charge trapping efficiency** itself. Thus, the **relatively thin dielectric nitride layer 132 of the ONO top dielectric layer 130 does not trap charge** during memory programming and retention operations." See Lue, para. 33, ln. 3-8. (**Emphasis** Added). Therefore, one having ordinary skill in the art would not reasonably consider the single-layer charge storage layer 124 and two bottom layers of (non-charge-trapping) dielectric tunneling layer 131 and 132, to disclose the claimed features of, "the multi-layer **charge trapping layer** comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer" of **claim 21**.

Therefore, the Applicant respectfully submits that amended **claim 21** overcomes the 102 rejection based on Lue. **Claims 22-26 and 28-32** also overcome the same rejection because they depend from **claim 21**. The Applicant respectfully requests the 102 rejection be reconsidered and withdrawn.

Claims Rejections – 35 USC § 103

The Office Action rejects **claims 21 and 23-24** under pre-AIA 35 USC 103(a) as allegedly being obvious by U.S. Patent Application Publication No. US 2006/0284236 by Bhattacharyya (hereinafter "Bhattacharyya") in view of Kim.

The Office Action states that "Bhattacharyya does not disclose the multi-layer charge trapping layer 160" at all and relies on Kim to cure the deficiencies. See Office Action, pg. 9, ln. 16-18. The Applicant respectfully submits that Kim does not disclose at least the features of "an anti-tunneling layer disposed between the first and second

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dielectric layers, wherein the anti-tunneling layer includes an oxide layer" of the multi-layer charge trapping layer as Kim is not cited for the rejection to original **claim 27**.

Therefore, amended **claim 21** overcomes the 103 rejection based on Bhattacharyya in view of Kim. **Claims 23-24** overcome the same 103 rejection because they depend from **claim 21**. The Applicant respectfully requests the rejection be withdrawn.

The Office Action rejects **claims 28 and 30** under pre-AIA 35 USC 103(a) as allegedly being obvious by Bhattacharyya in view of Kim in further view of U.S. Patent No. US 7,425,491 by Forbes (hereinafter "Forbes").

The Applicant has explained above with reasons that Bhattacharyya in view of Kim does not disclose at the least the features of "an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer" of the multi-layer charge trapping layer of **claim 21**. Forbes does not cure those deficiencies as it is specifically cited to allegedly disclose the limitation of "silicon nanowire channel" for **claim 28** and "GAA structure" of **claim 30**.

Therefore, **claims 28 and 30** overcome the 103 rejection based on Bhattacharyya in view of Kim and Forbes. The Applicant respectfully requests the rejection be withdrawn.

The Office Action rejects **claims 33 and 35** under pre-AIA 35 USC 103(a) as allegedly being obvious by U.S. Patent Application Publication No. US 2006/0008959 by Hagemeyer et al. (hereinafter "Hagemeyer") in view of Wang.

The Applicant respectfully submits that allowable subject matter of **claim 34** "wherein the channel is vertical and oriented substantially perpendicular to a

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semiconductor material structure" has been incorporated substantially to **claim 33**. Therefore, **claim 33** overcomes the 103 rejection based on Hagemeyer in view of Wang.

Claim 35 overcomes the same 103 rejection because it depends from **claim 33**. The Applicant respectfully requests the rejection be withdrawn.

The Office Action rejects **claim 38** under pre-AIA 35 USC 103(a) as allegedly being obvious by Hagemeyer in view of Kim.

The Office Action rejects **claims 38 and 40** under pre-AIA 35 USC 103(a) as allegedly being obvious by Hagemeyer in view of Lue.

The Applicant respectfully submits that allowable subject matter of **claim 39** "wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure" has been incorporated substantially to **claim 38**. Therefore, **claim 38** overcomes the 103 rejection based on either Hagemeyer in view of Kim or Hagemeyer in view of Lue.

Claims 39-40 overcome the same 103 rejections because they depend from **claim 38**. The Applicant respectfully requests the rejection be withdrawn.

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Reservation of Rights

The Applicant believes that every assertion made in the Office Action has been addressed, however in the interest of clarity and brevity, the Applicant may not have asserted every available argument for each assertion made in the Office Action. The Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. The Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. The Applicant does not admit that any of the cited references or any other references of record is relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, the Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. The Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent Application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

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Conclusion

Claims 21-23, 24-33, and 35-40 are presented for examination. In view of the foregoing amendments and remarks, the Applicants respectfully submit that the presented claims are in condition for allowance. The Applicants respectfully request reconsideration of the Application and allowance of the presented claims.

Should the Examiner have any questions regarding this response or the Application in general, the Examiner is urged to contact the undersigned by telephone at (408) 545-6950. All correspondence should continue to be directed to the address given below.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Respectfully Submitted,

Date: 07/18/2017

/Kin Hung Lai/
Kin Hung LAI
Registration No. 69,251

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Sandisk Technologies, Inc. - Ex. 1002, Page 001738

Electronic Acknowledgement Receipt

EFS ID:	29839543
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Christine Morales
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	20-JUL-2017
Filing Date:	26-OCT-2016
Time Stamp:	12:05:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	PM07027D1CIP1C3_ResponsetoNonFinalOA_05172017.pdf	209777 29485b13092c4f402eec1fa79cc04271382bf0e2	no	17

Warnings:

Information:	
Total Files Size (in bytes):	209777

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5543336	A	1996-08-06	Enami et al.	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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	1	2008290400	A1	2008-11-27	Jenne et al.	Entire Document
	2	20100006922	A1	2010-01-14	Matsuoka et al.	Entire Document
	3	20100178759	A1	2010-07-15	Kim et al.	Entire Document

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

If you wish to add additional Foreign Patent Document citation information please click the Add button [Add]

NON-PATENT LITERATURE DOCUMENTS [Remove]

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	SIPO Office Action for Chinese Application Number 2013800319699 (PM07024CIP1CN) dated 05/31/2017; 11 pages	
	2	TIPO Office Action for Taiwan Application Number 106107213 (PM07002CIP2TWD1) dated 07/04/2017; 6 pages	

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Jordan/	Date (YYYY-MM-DD)	2017-07-28
Name/Print	Christopher Jordan	Registration Number	65809

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

AFD China
INTELLECTUAL PROPERTY LAW OFFICE

[redacted]

June 21, 2017

[redacted]

Attn.: [redacted]
Murgitroyd & Company-Glasgow

Via Email Only
[redacted]

Re: National Phase in China of PCT/US2013/048876
In the name of Cypress Semiconductor Corporation
Title: Radical Oxidation Process for Fabricating a Nonvolatile Charge Trap Memory Device
CN Application No.: 2013800319699
Your Ref.: [redacted]
Our Ref.: 081409910-E
Deadline for Responding to this Office Action: **August 15, 2017(Beijing Time)**
Issue date: May 31, 2017; 2 months rejection.

Dear [redacted]:

The State Intellectual Property Office of China recently has issued the Second Office Action in connection with the captioned application. A copy of the Chinese Notification is enclosed for your records.

With respect to the Examiner's opinions in this Action, we would like to provide the brief summarization as below with our recommendations.

1. Inventiveness – Claims 1-20

[AFD remarks: The Examiner's comments on the inventiveness of claims 3, 5-6, 11, 13-14 and 17-18 are substantially the same as those in the First Office Action. We just copy the corresponding comments in the First Office Action for your reference.]

Claim 1

Examiner's opinion:

Claim1 does not possess inventiveness over Reference 2 (US2008/0293255A1) in view of known common knowledge in the art; wherein a first dielectric layer 602 is a tunnel oxide layer in the present application, a second dielectric layer 606 is equivalent to a high-temperature-oxide (HTO) layer in the present application; and the distinguishing technical feature in claim 1 over Reference 2 (see paragraphs 0001-0106 of its

[redacted]

Description and Figs. 1-13B, especially paragraphs 0043, 0050 and 0057 of its Description), is the following:

"*wherein the channel comprises polysilicon*";

such distinguishing technical feature is the conventional choice in the art.

Our suggestion:

[redacted]

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[redacted]

Claim 9

Examiner's opinion:

Claim 9 does not possess inventiveness over Reference 2 in view of Reference 3 (KR10-2004-0070669A) and known common knowledge in the art; the distinguishing technical feature in claim 9 over Reference 2 (see paragraphs 0001-0106 of its Description and Figs. 1-13B, especially paragraphs 0043, 0050 and 0057 of its Description), is the following:

"*wherein the channel comprises polysilicon; wherein the first layer is separated from the second layer by an anti-tunneling layer comprising an oxide*";

Reference 3 (see line 1 on page 1 to the last line on page 5 of its Description and Figs. 1-3) discloses that a buffer nitride layer 103 (equivalent to a first layer in the present application) is separated from a trapping nitride layer 105 (equivalent to a second layer in

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the present application) by a buffer oxide layer 104 (equivalent to an anti-tunneling layer comprising an oxide); and provides technical teaching of providing a oxide layer between two nitride layers in the charge storage structure, finally forming S0N0N0S, thereby improving its maintaining feature so as to reduce charge leakage; under such teaching, a person skilled in the art has motivation to apply it to Reference 2, i.e. providing an anti-tunneling layer comprising an oxide between a bottom oxygen-rich silicon oxy-nitride section portion and a top silicon-rich silicon oxy-nitride section portion. Moreover, it is conventional choice in the art to select polysilicon as the channel material according to the need of practical application.

Our suggestion:

[redacted]

Claims 2, 4, 10 and 12

Examiner's opinion:

Claims 2, 4, 10 and 12 do not possess inventiveness on the condition that the claims they refer to do not possess inventiveness; it conventional technical means in the art that at least one of the first and the second oxidation process comprises a plasma oxidation process or an In-Situ Steam Generation (ISSG) process according to the need of the need of practical application.

Our suggestion:

[redacted]

Claims 3, 5-6, 11 and 13-14

Examiner's opinion:

Claims 3, 5-6, 11 and 13-14 do not possess inventiveness on the condition that the claims they refer to do not possess inventiveness; the additional technical features of claims 3, 5-6, 11 and 13-14 are conventional technical means in the art.

Our suggestion:

[redacted]

Claims 7 and 15

Examiner's opinion:

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Claims 7 and 15 do not possess inventiveness on the condition that the claims they refer to do not possess inventiveness; and the additional technical features of claims 7 and 15 are disclosed by Reference 2 (see paragraphs 0035-0092 of its Description and Figs. 2-10E).

Our suggestion:

[redacted]

Claim 8

Examiner's opinion:

Claim 8 does not possess inventiveness Reference 2 in view of Reference 3 (KR10-2004-0070669A) and known common knowledge in the art; Reference 3 (see line 1 on page 1 to the last line on page 5 of its Description and Figs. 1-3) discloses relevant technical features, providing technical teaching of providing a oxide layer between two nitride layers in the charge storage structure, finally forming S0N0N0S, thereby improving its maintaining feature so as to reduce charge leakage; under such teaching, a person skilled in the art has motivation to apply it to Reference 2, i.e. providing an anti-tunneling layer comprising an oxide between the oxygen rich silicon oxy-nitride section at the bottom and silicon rich silicon oxy-nitride section on the top.

Our suggestion:

[redacted]

Claim 16

Examiner's opinion:

Claim 16 does not possess inventiveness over Reference 4 (US 2009/0294844A1, December 3, 2009) in view of Reference 5 (CN101517714A), Reference 2 and known common knowledge in the art; wherein a dielectric layer 2303 is equivalent to a first dielectric layer in the present application, a dielectric layer 2305 is equivalent to a second dielectric layer in the present application, a source region 2303 is equivalent to a first doped diffusion region in the present application, a silicon oxide film 2401 is equivalent to a high-temperature-oxide (HTO) layer in the present application, a silicon nitride film 2402 is equivalent to a charge storing layer in the present application, a silicon oxide film 2404 is equivalent to a tunnel oxide layer in the present application, a silicon oxide film 2602 belongs to a layer of semiconducting material in the present application, a drain region 2603 is equivalent to a second doped diffusion region in the present application, and the distinguishing technical features in claim 16 over Reference 4 (see paragraphs 0001-0130 of its Description and Figs. 1-26), are the following:

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(1) the charge storing layer is a multi-layer charge storing layer, the multi-layer charge storing layer comprising an oxygen-lean, first oxynitride layer on the HTO layer in which a stoichiometric composition of the first oxynitride layer results in it being trap dense; and an oxygen-rich, second oxynitride layer on the first oxynitride layer in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free;

(2) "wherein at least one of the tunnel oxide layer and the HTO layer is formed using a radical oxidation process carried out at a temperature in a range of 600-900 degrees Celsius at a pressure in a range of 0.5-5 Torr for a duration in a range of 100-150 minutes"; and

(3) the channel comprises polysilicon; wherein the vertical channel fills out the opening completely.

As for the distinguishing technical feature (1), Reference 5 (see line 1 on page 1 to the last line on page 15 of its Description and Figs. 1-10) discloses that charge trapping layer is charge storing layer, a silicon oxynitride 518B is a first oxynitride layer in the present application, a silicon oxynitride 518A is a second oxynitride layer in the present application, a blocking layer 520 is equivalent to HTO layer in the present application. As can be seen, Reference 5 provides technical teaching of providing a multi-layer charge storing layer comprising comprising an oxygen-lean, first oxynitride layer and an oxygen-rich, second oxynitride layer, thereby, in case of maintaining good data maintaining, proportionately scaling the thickness of charge trapping layer. Under such teaching, a person skilled in the art has motivation to apply it to Reference 4, i.e. providing a multi-layer charge storing layer comprising an oxygen-lean, first oxynitride layer on the above silicon oxide film 2401 and an oxygen-rich, second oxynitride layer on the first oxynitride layer, without paying inventive work.

As for the distinguishing technical feature (2), Reference 2 (see paragraphs 0001-0106 of its Description and Figs. 1-13B) discloses relevant technical features, wherein a first dielectric layer 602 is a tunnel oxide layer in the present application, a second dielectric layer 606 is equivalent to a high-temperature-oxide (HTO) layer in the present application, which provides technical teaching for applying the distinguishing technical feature (2) to Reference 4.

As for the distinguishing technical feature (3), it is the conventional choice in the art to select polysilicon as the material of the channel. Moreover, it is conventional provision in the art that the vertical channel fills out the opening completely, such as the prior art (US2010/0178759A1, US2010/0006922A1, US 2010/0252877A1), which does not need to pay creative work.

Our suggestion:

[redacted]

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[redacted]

Claims 17-18

Examiner's opinion:

Claims 17-18 do not possess inventiveness on the condition that claim 16 they refer to does not possess inventiveness; and the additional technical features of claims 17-18 are conventional technical means in the art.

Our suggestion:

[redacted]

Claims 19-20

Examiner's opinion:

Claims 19-20 do not possess inventiveness over Reference 4 in combination with References 5 and 2-3 and known common knowledge in the art; Reference 3 (see line 1 on page 1 to the last line on page 5 of its Description and Figs. 1-3) discloses relevant technical features, providing technical teaching of providing a oxide layer between two nitride layers in the charge storage structure, finally forming S0N0N0S, thereby improving its maintaining feature so as to reduce charge leakage; under such teaching, a person skilled in the art has motivation to apply it to Reference 4. Moreover, in practical application, a person skilled in the art has motivation to form a high-temperature-oxide (HTO) layer by any other suitable manner, which belongs to conventional technical means in the art.

Our suggestion:

[redacted]

2. Observations filed by the applicant

Examiner's opinion:

the observations filed by the applicant are not persuasive and cannot overcome the defects in the previous Action:

(1) Reference 2 (see paragraphs 0043, 0050 and 0057 of its Description) has disclosed the newly added technical feature that "at least one of the first and or second oxidation processes is a radical oxidation process carried out at a temperature in the range of 600 –

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900 degrees Celsius at a pressure in the range of 0.5 – 5 Torr for a duration in the range of 100 – 150 minutes", and thus such technical feature do not constitute the distinguishing technical feature.

(2) As for the technical effect, the contents recorded in paragraph 0037 of the description of Reference 2 are that "*Formation of a dielectric layer by a radical oxidation process may provide higher quality films than processes involving steam growth, i.e. wet growth processes. Furthermore, a radical oxidation process carried out in a batch-processing chamber may provide high quality films without impacting the throughput (wafers/Hr) requirements that a fabrication facility may require. By carrying out the radical oxidation process at temperatures compatible with such a chamber, such as temperatures approximately in the range of 600-900 degrees Celsius, the thermal budget tolerated by the substrate and any other features on the substrate may not be impacted to the extent typical of processes over 1000 degrees Celsius…These dielectric layers may be of very high quality, even at a reduced thickness. In one embodiment, the tunnel dielectric layer and the blocking dielectric layer are both denser and are composed of substantially fewer hydrogen atoms/cm3 than a tunnel dielectric layer or a blocking dielectric layer formed by wet oxidation techniques. In accordance with another embodiment of the present invention, a dielectric layer formed by carrying out a radical oxidation process is less susceptible to crystal plane orientation differences in the substrate from which it is grown*", which are consistent with the contents recorded in lines 9 to 26 on page 6 (i.e. paragraph 0052) of the description of the present application. Thus, Reference 2 has disclosed the technical effect submitted by the applicant.

To sum up, the applicant's observations are not persuasive.

Our suggestion:

[redacted]

Conclusive opinion

Examiner's conclusive opinion:

the application does not possess any patentable substantial contents, and

if the applicant fails to expound reasons or the reasons expounded are not sufficient, this application will be rejected.

<End of Examiner's opinions>

[redacted]

[redacted]

AFD China Intellectual Property [redacted]

[redacted]



[redacted]

[redacted]

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[redacted]

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TRANSLATION OF THE PRELIMINARY EXAMINATION REPORT

SUBJECT:

After examination, the TIPO considers that the following issues apply to the referenced application. The applicant is requested to file an argument (in duplicate) or an amendment within three months from receipt of this Examination Report. If the applicant fails to reply within the time limit, the TIPO will continue the examination on the basis of the materials in hand.

EXPLANATION:

1. After examination, the examiner deems that:

1.1 The present application is entitled "Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers". The present application contains 20 claims, of which claims 1, 10 and 16 are independent claims, and the other claims are dependent claims.

1.2 Claims 1, 10 and 16 of the present application disclose "a method", but the method is indefinite, such that said claims do not meet the requirement of Article 26, Paragraph 2 of the Taiwan Patent Law.

1.3 According to the contents of citation 1, claims 1-4 and 8 of the present application do not meet the requirement of Article 22, Paragraph 1, Item 1 of the Taiwan Patent Law.

1.3.1 Regarding claim 1 of the present application, paragraphs [0025], [0033], [0044]-[0045] and figures 2-3 of citation 1 disclose a method comprising: forming, in a semiconducting material over a surface of a substrate (208), a channel (212) connecting a source (210) and a drain (210) of a memory device; and forming a gate (202) abutting the channel, wherein forming the gate comprises: forming a tunnel oxide layer (216) abutting the channel (212); forming a multi-layer charge storing layer (204) over the tunnel oxide layer (216), the multi-layer charge storing layer including a first nitride layer (220B) over the tunnel oxide layer (216) and a second nitride layer (220A) over the first nitride layer, wherein a

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stoichiometric composition of the first nitride layer (220B) results in it being substantially trap free ([0044]), and a stoichiometric composition of the second nitride layer (220A) results in it being trap dense ([0045]), forming a blocking dielectric layer (218) over the multi-layer charge storing layer (204), and treating the blocking dielectric layer (218) to reduce a number of traps in a top surface thereof ([0033]). Therefore, citation 1 discloses all technical features of claim 1 and said claim does not possess novelty.

1.3.2 Regarding claim 2 of the present application, paragraphs [0033], [0035] of citation 1 disclose that treating the blocking dielectric layer (218) comprises heating the blocking dielectric layer in a water vapor (...steam...).

1.3.3 Regarding claim 3 of the present application, paragraph [0033] of citation 1 discloses that treating the blocking dielectric layer (218) comprises steam annealing the blocking dielectric layer (218) (...steam annealing...).

1.3.4 Regarding claim 4 of the present application, paragraph [0033] of citation 1 discloses that steam annealing the blocking dielectric layer (218) reduces a number of traps in a top surface of the second nitride layer (220A).

1.3.5 Regarding claim 8 of the present application, paragraphs [0030], [0044] of citation 1 disclose that the first nitride layer (220B) comprises an oxygen-rich, oxynitride layer ([0044]), and the second nitride layer (220A) comprises an oxygen-lean, oxynitride layer (220B).

1.4 According to the contents of citation 1, claim 10 of the present application does not meet the requirement of Article 22, Paragraph 1, Item 1 of the Taiwan Patent Law.

1.4.1 Regarding claim 10 of the present application, paragraphs [0025], [0030]-[0033], [0044]-[0045] and figures 2-3 of citation 1 disclose a method comprising: forming, in a semiconducting material over a surface of a substrate (208), a channel (212) connecting a source (210) and a drain (210) of a memory device; forming a gate (202) abutting the channel, wherein forming the gate comprises: forming a tunnel oxide layer(216) abutting the channel (212); forming a multi-layer charge storing layer (204) over the tunnel oxide layer (216), the multi-layer charge storing layer (204) including a substantially trap free,

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oxygen-rich, first oxynitride layer (220B) over the tunnel oxide layer (216) ([0044]) and a trap dense, oxygen-lean, second oxynitride layer (220A) over the first oxynitride layer ([0030]); and forming a blocking dielectric layer (218) over the multi-layer charge storing layer (204), wherein the second oxynitride layer (220A) further comprises a concentration of carbon selected to increase a number of traps therein ([0031]). Therefore, citation 1 discloses all technical features of claim 10 and said claim does not possess novelty.

1.5 According to the contents of citation 1, claim 16 of the present application does not meet the requirement of Article 22, Paragraph 1, Item 1 of the Taiwan Patent Law.

1.5.1 Regarding claim 16 of the present application, paragraphs [0025], [0030]-[0033], [0044]-[0045] and figures 2-3 of citation 1 disclose a method comprising: forming, in a semiconducting material over a surface of a substrate (208), a channel (212) connecting a source (210) and a drain (210) of a memory device; and forming a gate (202) abutting the channel, wherein forming the gate (202) comprises: forming a tunnel oxide layer (216) abutting the channel (212), forming a multi-layer charge storing layer (204) over the tunnel oxide layer (216), the multi-layer charge storing layer (204) including a first nitride layer (220B) over the tunnel oxide layer (216) and a second nitride layer (220A) over the first nitride layer (220B), wherein the first nitride layer (220B) comprises a stoichiometric composition that results in it being substantially trap free ([0044]), and the second nitride layer (220A) comprises a stoichiometric composition, including a concentration of carbon ([0031]), that results in it being trap dense ([0045]), forming a blocking dielectric layer (218) over the multi-layer charge storing layer (204), and treating the blocking dielectric layer (218) to reduce a number of traps in a top surface thereof ([0033]). Therefore, citation 1 discloses all technical features of claim 16 and said claim does not possess novelty.

1.6 Citation:
1. US 2011/0248332 A1

1.7 There are no further issues that prohibit the patentability of the current invention at the moment except the above mentioned rejection reasons. If

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there are new issues that prohibit the patentability of the current invention, we will inform the applicant of the rejection reasons.

2. If an amendment or a correction is made to the specification, claims and drawings, the applicant should handle the amendment or the correction according to Article 43 and Article 44, Item 3 of the Taiwan Patent Act and Article 36 to Article 38 of the Enforcement Rules of the Taiwan Patent Act, and draft a request for an amendment or a correction.

3. In the case where the applicant wishes to proceed with a face-to-face demonstration or explanation before the TIPO, please explicitly indicate "interview requested" in the response, and an official fee of NT$1000 must be paid. The place and time for an interview will be arranged if the TIPO considers an interview necessary.

4. Attached is a copy of the Search Report of the present application.

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Search Report of Patent Application No. 106107213

1.Filing Date: March 22, 2013		
2.Priority Date: March 31, 2012		
3.Classification of the Application (IPC): ***H01L27/115*** (2006.01), ***H01L29/78***(2006.01)		
4.Technical Fields Searched (IPC): H01L27/115 (2006.01) H01L29/78 (2006.01)		
5.Database Searched (Key Words): TIPO domestic/abroad patent database, EPO, USPTO, JPO, Google Patent		
Category	Citation of Document with Indication, Where Appropriate, of Relevant Passages	Relevant to Claims
X	1. US 2011/0248332 A1 2011/10/13 Figures 2-3; paragraphs [0025], [0033], [0035], [0044]-[0045] of the specification	1-4, 8, 10, 16

Categories of Cited Documents:
X: particularly relevant document that would refute the novelty or inventive step of the claimed invention when taken alone
Y: particularly relevant document that would refute the novelty or inventive step of the claimed invention when combined with one or more other documents
A: document defining the general state of the art
D: document cited in the specification
E: document filed prior to but published after the application was filed
O: document of public use, sale or exhibition
P: document published on a date falling between the filing date of the application and the priority date claimed
L: document cited for other reasons

Date of completion of the search: June 30, 2017

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RELATED ARTICLE OF THE PATENT ACT

Article 22 Substantial conditions

An invention which is industrially applicable may be granted a patent upon application in accordance with this Act, except for the following:

1. the invention was disclosed in a publication prior to the filing of the patent application;

2. the invention was publicly exploited prior to the filing of the patent application; or

3. the invention was publicly known prior to the filing of the patent application.

Where an invention can be easily made by a person ordinarily skilled in the art based on prior art, a patent shall not be granted for such an invention notwithstanding the preceding paragraph.

Any of the following events shall not be deemed as one prescribed in Paragraph 1 or the preceding paragraph, which may preclude the grant of an invention patent, provided that the concerned patent application is filed within six months from the date of the event's occurrence:

1. the invention concerned was publicly disclosed as a result of conducting a test;

2. the invention was disclosed in a publication;

3. the invention was displayed at an exhibition held or recognized by the Government; or

4. the invention was disclosed without the consent of the applicant.

An applicant claiming exemption as set forth in Item 1 through Item 3 of the preceding paragraph shall state the fact and the relevant date in the patent application at the time of filing and submit evidentiary documents within the time limit specified by the Specific Patent Agency.

(Published on the website of the TIPO)

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6174758	B1	2001-01-16	Nachumovsky	Entire Document
	2	6462370	B2	2002-10-08	Kuwazawa	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020048200	A1	2002-04-25	Kuwazawa	Entire Document
	2	20050062098	A1	2005-03-24	Mahajani et al.	Entire Document

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

If you wish to add additional Foreign Patent Document citation information please click the Add button [Add]

NON-PATENT LITERATURE DOCUMENTS [Remove]

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	USPTO Final Rejection for US Application Number 14/605,231 (PM07024CIP1C1) dated 07/10/2017; 7 pages	
	2	USPTO Non-Final Rejection for US Application Number 15/376,282 (PM07027D1C4) dated 07/11/2017; 16 pages	

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Jordan/	Date (YYYY-MM-DD)	2017-07-28
Name/Print	Christopher Jordan	Registration Number	65809

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/605,231	01/26/2015	Krishnaswamy Ramkumar	PM07024CIP1C1	4843

60909 7590 07/10/2017

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
07/10/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Sandisk Technologies, Inc. - Ex. 1002, Page 001766

Office Action Summary	Application No. 14/605,231	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/11/16*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-25,29-33,35-38 and 40-45* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *21-25, 35-38, 40-44* is/are allowed.

7)☒ Claim(s) *29, 32-33, 45* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 21-25, 29, 32-33, 35-38, 40-45 have been considered but are moot of new ground rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29, 32-33, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramsbey et al. (U.S. Patent No. 6,433,383) in view of Mahajani et al. (U.S. Patent Publication No. 2005/0062098) and further in view of Ranade (U.S. Patent Publication No. 2008/0121932).

Ramsbey et al. teaches a memory device, comprising:

a tunnel oxide layer (15) overlying a channel connecting a source and a drain (13a/13b) of the memory device formed in a substrate (12);

a multi-layer charge storing layer (32/34) overlying the tunnel oxide layer (15), the multi-layer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the

tunnel oxide layer in which a composition of the first layer results in it being substantially trap free (32, see figure 4c-7, col. 6, lines 35-55), and an oxygen-lean, silicon nitride second layer on the first layer in which a composition of the second layer results in it being trap dense (34, see figures 4c-7, col. 6, lines 56-67, col. 7, lines 1-5); and

a high-temperature-oxide (HTO) layer (36) overlying the multi-layer charge storing layer (32/34), the HTO layer comprising an oxidized silicon nitride with a thickness approximately in the range of 2-3 nanometers, and an oxide overlaying the oxidized silicon nitride (see col. 7, lines 6-22). The limitation "the HTO layer comprising an oxidized silicon nitride" in claim 29 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); *and* particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding to claims 33, wherein at least one of the first layer or the second layer of the multi-layer charge storing layer comprises silicon nitride or silicon oxy-nitride (32/34, see col. 6, lines 35 to col. 7, lines 5).

Regarding to claim 45, the HTO layer further comprises a nitride HTO layer overlying the oxide of the HTO layer (see col. 7, lines 6-22, it is noted that layer 32 comprises oxide and oxynitride layer). Absent a showing of unexpected result, a change in sequence involves routine optimization of process of prior art and would have been obvious to one skilled in the art at the time the invention was made. A change in sequence/reversal of process steps is obvious under 35 USC 103 (exparte Rubin, 128 USPQ 440 (Bd. App. 1959)). See also in re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA).

However, the reference does not clearly teach the channel comprises recrystallized polysilicon.

Mahajani et al. teaches a SONOS device having a recrystallized polysilicon (called monocrystalline channel, see paragraph# 29, and claim 14). It is noted that this is a device claim, the final structure of the channel after recrystallized polysilicon is a monocrystalline channel (see paragraph# 153 of the instant invention).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form silicon nanowire channel in Ramsbey et al. as taught by Mahajani because determining the optimum material for the layer only involved routine skill in the art to form a desired memory device.

However, the reference does not clearly teach the channel comprises polysilicon, recrystallized polysilicon or silicon nanowire.

Ranade teaches forming channel comprise a silicon nanowire (see figures 2a-2n, paragraph# 25, meeting claim 32).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form silicon nanowire channel in Ramsbey et al. as taught by Ranade because determining the optimum material for the layer only involved routine skill in the art to form a desired memory device.

Allowable Subject Matter

Claims 21-25, 35-38, 40-44 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the device steps in forming a multi-layer charge storing layer overlying the tunnel oxide layer, the multilayer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free, and a second layer comprising a Zirconium or Yttrium based high K dielectric material on the first layer in which a composition of the second layer results in it being trap dense.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/Thanh T. Nguyen/
Primary Examiner, Art Unit 2893

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/376,282	12/12/2016	Igor Polishchuk	PM07027D1C4	6123

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198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
07/11/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Sandisk Technologies, Inc. - Ex. 1002, Page 001773

Office Action Summary	Application No. 15/376,282	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

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- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/12/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☒ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *See Continuation Sheet*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Continuation of Attachment(s) 2). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :06/22/2017; 04/25/2017; 04/24/2017; 04/24/2017; 04/24/2017; .

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Objections

Claim 1, 10, 16, and 19 are objected to because of the following informalities: Claim 1 recites the limitation "the gate" in line 10; Claim 10 recites the limitation "the second oxide layer" in line 7; Claim 16 recites the limitation "the first gate electrode" in line 1; Claim 19 recites the limitation "the gate" in line 10. There is insufficient antecedent basis for the limitations in the claims.

For purposes of a prompt examination the examiner reads claims 10 and 16 as the followings:

"1. A semiconductor device comprising: a non-volatile memory transistor comprising: a charge trapping layer, a tunnel dielectric disposed between the charge trapping layer and a substrate, and a blocking oxide disposed between the charge trapping layer and a first gate electrode; a logic transistor comprising: a second gate electrode, and an oxide disposed between the second gate electrode and the substrate; and an isolation structure disposed between the non-volatile memory transistor and the logic transistor.

10. A memory transistor comprising: a dielectric stack comprising, a first oxide layer formed on a substrate, a first nitride layer formed on the first oxide layer, a second nitride layer formed on the first nitride layer, and a second oxide [[~~nitride~~]] layer formed the second nitride layer; and a gate electrode formed on the second oxide layer of the dielectric stack.

16. The memory transistor of claim 10, wherein the [[~~first~~]] gate electrode is formed from a doped polysilicon with doped concentration such that the minimum energy to remove an electron from the gate electrode is from approximately 4.8-5.3 electron volts (eV).

19. A memory device comprising: a non-volatile memory transistor comprising: a charge trapping layer, a tunnel dielectric disposed between the charge trapping layer and a substrate, and a blocking oxide disposed between the charge trapping layer and a first gate electrode; a logic transistor comprising: a second gate electrode, and an oxide disposed between the second gate electrode and the substrate; and an isolation structure disposed between the non-volatile memory transistor and the logic transistor."

Appropriate correction is required.

Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10 - 13, 15, and 18 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Rathor et al., US 6,818,558.

In re Claim 10, Rathor discloses a memory transistor (Figs. 7 and 8) comprising: a dielectric stack (814, 816, 818, 820, 824) comprising, a first oxide layer 814 formed on a substrate 812, a first nitride layer 816 formed on the first oxide layer 814, a second nitride layer 818 formed on the first nitride layer 816, and a second oxide [[~~nitride~~]] layer 824 formed the second nitride layer 816; and a gate electrode 828 formed on the second oxide layer 824 of the dielectric stack (814, 816, 818, 820, 824) (Figs. 7 and 8; column 11, line 8 - column 14, line 47).

In re Claim 11, Rathor discloses the memory transistor of claim 10, wherein the first oxide layer 814 is a tunneling oxide (column 11, line 59).

In re Claim 12, Rathor discloses the memory transistor of claim 10, wherein the first nitride layer 816 comprises a substantially trap-free oxynitride (column 12, lines 26-48; column 13, lines 52-59).

In re Claim 13, Rathor discloses the memory transistor of claim 10, wherein the second nitride layer 818 comprises a charge-trapping oxynitride (column 13, lines 52-59).

In re Claim 15, Rathor discloses the memory transistor of claim 10, wherein the gate electrode 828 (being polysilicon, column 13, lines 60-66) is inherently high work function gate electrode. It is inherently because according to MPEP2112.01 WHEN THE STRUCTURE RECITED IN THE REFERENCE IS SUBSTANTIALLY IDENTICAL TO THAT OF THE CLAIMS, CLAIMED PROPERTIES OR FUNCTIONS ARE PRESUMED TO BE INHERENT. In the instant case the electrode 828 being polysilicon as the claimed one inherently possesses the claimed function - high work function.

In re Claim 18, Rathor discloses the memory transistor of claim 10 further comprising sidewall spacers 836 formed adjacent to the dielectric stack (814, 816, 818, 820, 824) and the gate electrode 828 (Fig. 8H).

Claims 10, 15, and 16 are rejected under pre-AIA 35 U.S.C. 102(a) as being anticipated by Yan, US 2008/0135946.

In re Claim 10, Yan discloses a memory transistor comprising: a dielectric stack 230 comprising, a first oxide layer 231 formed on a substrate 210, a first nitride layer 234 formed on the first oxide layer 231, a second nitride layer 235 formed on the first nitride layer 234, and a second oxide [[~~nitride~~]] layer 233 formed the second nitride layer 235; and a gate electrode 240 formed on the second oxide layer 233 of the dielectric stack 230 (Fig. 1; [0030-0039]).

In re Claim 15, Yan discloses the memory transistor of claim 10, wherein the gate electrode 240 (being polysilicon [0036]) is inherently high work function gate electrode. It is inherently because according to MPEP2112.01 WHEN THE STRUCTURE RECITED IN THE REFERENCE IS SUBSTANTIALLY IDENTICAL TO THAT OF THE CLAIMS, CLAIMED PROPERTIES OR FUNCTIONS ARE PRESUMED TO BE INHERENT. In the instant case the electrode 240 being polysilicon as the claimed one inherently possesses the claimed function - high work function.

In re Claim 16, Yan discloses the transistor of claim 10, wherein the [[~~first~~]] gate electrode 240 is formed from a doped polysilicon with doped concentration ([0036]) such that the minimum energy to remove an electron from the gate electrode is inherently from approximately 4.8-5.3 electron volts (eV). It is inherently because according to MPEP2112.01

WHEN THE STRUCTURE RECITED IN THE REFERENCE IS SUBSTANTIALLY IDENTICAL TO THAT OF THE CLAIMS, CLAIMED PROPERTIES OR FUNCTIONS ARE PRESUMED TO BE INHERENT. In the instant case Yan's gate electrode being formed from a doped polysilicon with doped concentration ([0036]), as claimed one, inherently possesses the claimed property - the minimum energy to remove an electron from the gate electrode is inherently from approximately 4.8-5.3 electron volts (eV).

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1- 3, 5- 9, 19, and 20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nachumovsky, US 6,174,758, in view of Rathor.

In re Claim 1, Nachumovsky discloses a semiconductor device 100 (Fig. 1) comprising: a non-volatile memory transistor 140; a logic transistor (120, 130) comprising: a second gate electrode (126, 136), and an oxide (125, 135) disposed between the second gate electrode (126, 136) and the substrate 110; and an isolation structure 150 disposed between the non-volatile memory transistor 140 and the logic transistor (120, 130) (Fig. 1; column 3, line 34 –column 4, line 45).

Nachumovsky does not specify that the non-volatile memory transistor 140 comprising: a charge trapping layer, a tunnel dielectric disposed between the charge trapping layer and a substrate, and a blocking oxide disposed between the charge trapping layer and a first gate electrode.

The only difference between the Applicants' claim 1 and Nachumovsky's reference is in the specified structure of the non-volatile memory transistor.

Rathor teaches a non-volatile memory transistor (812, 816, 818, 820, 828, 830, 836) (Fig. 8H) comprising: a charge trapping layer (816, 818, 820), a tunnel dielectric 814 disposed between the charge trapping layer (816, 818, 820) and a substrate 812 and a blocking oxide 824 disposed between the charge trapping layer (816, 818, 820) and a first gate electrode 828 (Figs. 7 and 8; column 11, line 8 - column 14, line 47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Nachumovsky's non-volatile memory transistor with Rathor's non-volatile memory transistor, to have lower programming voltages than other conventional nonvolatile devices, such as some types of floating gate devices as taught by Rathor (column 1, lines 49-56).

In re Claim 2, Nachumovsky taken with Rathor discloses the semiconductor device of claim 1, wherein the charge trapping layer (816, 818, 820) (Rathor: Fig. 8H; column 11, line 8 - column 14, line 47) comprises: a charge-trapping oxynitride layer 818; and a substantially trap-free oxynitride layer 816 disposed between the charge-trapping oxynitride layer 818 and the tunnel dielectric 814.

In re Claim 3, Nachumovsky taken with Rathor discloses all limitations of claim 3, including that the charge-trapping oxynitride layer 818 has a first thickness (Rathor: column 12, lines 57-59) and the substantially trap-free oxynitride layer 816 has a second thickness (Rathor: column 12, lines 57-59), except for that a ratio of the first thickness and the second thickness is approximately 4:1.

It is known in the art that the thickness is a result effective variable – because mass depends on it. Due to high level of knowledge and skills of personal capable to operate very sophisticated and expensive equipment in semiconductor technology, it would have been an obvious matter of design choice of one of ordinary skill in the semiconductor art to use the specified ratio of the thicknesses, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)* (MPEP2144.04).

In re Claim 5, Nachumovsky taken with Rathor discloses the semiconductor device of claim 1, further comprising: first sidewall spacers 836 (Rathor: Fig. 8H) formed adjacent to the non-volatile memory transistor (812, 816, 818, 820, 828, 830, 836) (Fig. 8H); and second sidewall spacers (129, 139) (Nachumovsky: Fig. 1) formed adjacent to the logic transistor (120, 130).

In re Claim 6, Nachumovsky taken with Rathor discloses the semiconductor device of claim 1, wherein the first gate electrode 828 (Rathor: Fig. 8H; column 13, lines 60-66) and the second gate electrodes (126, 136) (Nachumovsky: Fig. 1; column 3, lines 63-66; column 4, lines 7-10) (being made of polysilicon) are high work function gate electrodes. It is inherently because according to MPEP2112.01 WHEN THE STRUCTURE RECITED IN THE REFERENCE IS SUBSTANTIALLY IDENTICAL TO THAT OF THE CLAIMS, CLAIMED PROPERTIES OR FUNCTIONS ARE PRESUMED TO BE INHERENT. In the instant case the first and second electrode being polysilicon as the claimed one inherently possesses the claimed function - high work function.

In re Claim 7, Nachumovsky taken with Rathor discloses the semiconductor device of claim 1, wherein the non-volatile memory transistor 140 is an N-type transistor and wherein the logic transistor (120, 130) is a P-type transistor (Nachumovsky: Fig. 1; column 3, line 46 – column 4, line 20).

In re Claim 8, Nachumovsky taken with Rathor discloses the semiconductor device of claim 1, wherein the first 828 (Rathor: Fig. 8H; column 13, lines 60-66) and second gate (126, 136) (Nachumovsky: Fig. 1; column 3, lines 63-66; column 4, lines 7-10) electrodes are formed from a doped polysilicon with doped concentration such that the minimum energy to remove an

electron from the first and second gate electrodes is inherently from approximately 4.8-5.3 electron volts (eV). It is inherently because according to MPEP2112.01 WHEN THE STRUCTURE RECITED IN THE REFERENCE IS SUBSTANTIALLY IDENTICAL TO THAT OF THE CLAIMS, CLAIMED PROPERTIES OR FUNCTIONS ARE PRESUMED TO BE INHERENT. In the instant case the first and second electrodes being doped polysilicon as the claimed one inherently possesses the claimed function - high work function.

In re Claim 9, Nachumovsky taken with Rathor discloses the semiconductor device of claim 1, wherein the isolation structure 150 (Nachumovsky: Fig. 1) is one of a local oxidation silicon (LOCOS) region or structure, a **field oxidation** (FOX) region or structure, or a shallow trench isolation (STI) structure.

In re Claim 19, Nachumovsky discloses a memory device (Fig. 1) comprising: a non-volatile memory transistor 140 **comprising: a charge trapping layer, a tunnel dielectric disposed between the charge trapping layer and a substrate, and a blocking oxide disposed between the charge trapping layer and a first gate electrode**; a logic transistor (120, 130) comprising: a second gate electrode (126, 136), and an oxide (125, 135) disposed between the second gate electrode (126, 136) and the substrate 110; and an isolation structure 150 disposed between the non-volatile memory transistor 140 and the logic transistor (120, 130) (Fig. 1; column 3, line 34 –column 4, line 45).

Nachumovsky does not specify that the non-volatile memory transistor 140 comprising: a charge trapping layer, a tunnel dielectric disposed between the charge trapping layer and a

substrate, and a blocking oxide disposed between the charge trapping layer and a first gate electrode.

The only difference between the Applicants' claim 1 and Nachumovsky's reference is in the specified structure of the non-volatile memory transistor.

Rathor teaches a non-volatile memory transistor (812, 816, 818, 820, 828, 830, 836) (Fig. 8H) comprising: a charge trapping layer (816, 818, 820), a tunnel dielectric 814 disposed between the charge trapping layer (816, 818, 820) and a substrate 812 and a blocking oxide 824 disposed between the charge trapping layer (816, 818, 820) and a first gate electrode 828 (Figs. 7 and 8; column 11, line 8 - column 14, line 47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Nachumovsky's non-volatile memory transistor with Rathor's non-volatile memory transistor, to have lower programming voltages than other conventional nonvolatile devices, such as some types of floating gate devices as taught by Rathor (column 1, lines 49-56).

In re Claim 20, Nachumovsky taken with Rathor discloses the memory device of claim 19, wherein the charge trapping layer (816, 818, 820) (Rathor: Fig. 8H; column 11, line 8 - column 14, line 47) comprises: a charge-trapping oxynitride layer 818; and a substantially trap-free oxynitride layer 816 disposed between the charge-trapping oxynitride layer 818 and the tunnel dielectric 814.

Claims 4 and 14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Nachumovsky taken with Rathor as applied to claim 1 above, and Rathor as applied to claim 10

above, respectively, and further in view of Kuwazawa, US 2002/0048200 (corresponding to US 6,462,370).

In re Claim 4, Nachumovsky taken with Rathor discloses all limitations of claim 4 except for the blocking oxide layer 824 (Rathor: Fig. 8H) is a high- temperature-oxide (HTO) blocking oxide.

In re Claim 14, Rathor discloses all limitations of claim 14 except for that the second oxide layer 824 (Fig. 8H) is a high- temperature-oxide (HTO) blocking oxide.

Kuwazawa teaches a memory transistor wherein the oxide layer is a high- temperature-oxide (HTO) blocking oxide ([0013]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Rather's blocking/second oxide film 824 with Kuwazawa's high- temperature-oxide (HTO) blocking oxide, to improve the dielectric strength of the intermediate insulation film, the dielectric film and the other dielectric film as taught by Kuwazawa ([0013]).

Claim 17 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Rathor as applied to claim 10 above.

In re Claim 17, Rathor discloses all limitations of claim 17 including that the first nitride layer 816 has a first thickness (in range of 30-60 Å (column 12, lines 31-33)) and the second nitride layer 818 as a second thickness (in the general rage of 10-20 Å (column 12, lines 57-59)), and wherein a ratio of the first thickness and the second thickness ((30 Å ÷60 Å)/(10 Å ÷20 Å) is (3:1) ÷ (6:1)) overlaps the claimed value of approximately 4:1 (See MPEP2131.03.II). It is known in the art that the thickness is a result effective variable – because mass depends on it. Due to high level of knowledge and skills of personal capable to operate very sophisticated and

expensive equipment in semiconductor technology, it would have been an obvious matter of design choice of one of ordinary skill in the semiconductor art to use the specified ratio of the thicknesses, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)* (MPEP2144.04).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on 8 AM - 5 PM PST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

Electronic Acknowledgement Receipt

EFS ID:	29926342
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	METHOD OF MANUFACTURING FOR MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	28-JUL-2017
Filing Date:	26-OCT-2016
Time Stamp:	18:15:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C3_IDS_07282017.pdf	1054005 4819a4b22ed7a58effaaa4a6130aadb56963b62a	no	4

Warnings:

Information:					
2	Non Patent Literature	PM07024CIP1CN_SIPO_Office_Action_Brief_2OA_06212017.pdf	300854 cb3e797ab441484a87df939dcdd77f38477bf0e6	no	11
Warnings:					
Information:					
3	Non Patent Literature	PM07002CIP2TWD1_TIPOOfficeAction.pdf	168501 df3efb41628eb794b303d66d4641ebbe1a309a67	no	6
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C3_IDS2_07282017.pdf	1053996 bef056d3dd42b84c8326dfbd51588820e1c14633	no	4
Warnings:					
Information:					
5	Non Patent Literature	PM07024CIP1C1_FinalRejection_07102017.pdf	271197 2cb1d01ee86ae7f86e3de4a0a5df47fb454c9271	no	7
Warnings:					
Information:					
6	Non Patent Literature	PM07027D1C4_NonFinalRejection_07112017.pdf	564228 1ff8bee201209bd03407694d245b7218587e9947	no	16
Warnings:					
Information:					
		Total Files Size (in bytes):	3412781		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/335,180	Filing Date 10/26/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

	(Column 1)		(Column 2)	(Column 3)		
AMENDMENT	07/20/2017	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

	(Column 1)		(Column 2)	(Column 3)		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
LASHAWN MARKS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 10/04/2017

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 10/04/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3	6223

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/04/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 10/04/2017
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3	6223

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/04/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-326000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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60909 7590 10/04/2017

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 10/04/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1002, Page 001795

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/335,180	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendemts filed on 07/28/2017*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *21-26,28-33 and 35-40*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

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Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 07/28/2017; 07/28/2017; 05/25/2017.

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Specification

The amendment to the specification filed 07/28/2017 has been entered.

Status of Claims

Applicant's cancellation of claims 1-20, 27, and 34 in the reply filed on 7/28/2017 is acknowledged.

Applicant's amendment of claims 21, 33, and 37-39 in the reply filed on 7/28/2017 is acknowledged.

Claims 21-26, 28-33, and 35-40 are under consideration in this Office Action.

Allowable Subject Matter

Claims 21-26, 28-33, and 35-40 are allowed.

The following is an examiner's statement of reasons for allowance:

In re Claim 21, Kim et al., US 2008/0272424, as well as Wang, US 2006/0113586 and Lue et al., US 2007/0029625, discloses all limitations of claim 21 except for that "an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 33, Hagemeyer et al., US 20060008959, taken with Wang discloses all limitations of claim 33 except for that "the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and a tunnel dielectric layer, a multi-layer

charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 38, Hagemeyer taken with Kim discloses all limitations of claim 38 except for that "the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on 8 AM - 5 PM PST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	1	("20170092729").PN.	US-PGPUB; USPAT	OR	OFF	2017/09/26 15:04
L4	8	((13/288919) or (12/152518) or (13/539466) or (14/159315) or (14/811346) or (15/335180)).APP.	US-PGPUB; USPAT	OR	OFF	2017/09/26 15:07
L5	5	((13/288919) or (12/152518) or (13/539466) or (14/159315) or (14/811346) or (15/335180)).APP.	USPAT	OR	OFF	2017/09/26 15:07
L6	0	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) (anti$1tunnel ADJ layer) nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/09/26 15:30
L7	0	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) (anti$1tunnel$4 ADJ layer) nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/09/26 15:30
L8	34	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) (anti$1tunnel$4 ADJ layer) nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:31
L9	34	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) (anti$1tunnel$4 ADJ layer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:32
L10	34	(diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) (anti$1tunnel$4 ADJ layer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:33
L11	34	(gate channel diffus$6 tunnel dielectric (charge ADJ trap$6) (anti$1tunnel$4 ADJ layer) nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:33

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L12	34	(gate channel diffus$6 tunnel dielectric (charge ADJ trap$6) (anti$1tunnel$4 ADJ layer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:33
L14	34	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer anti$1tunnel$4 nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:37
L15	34	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) (oxide ADJ layer) anti$1tunnel$4 nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:38
L16	37	(gate channel diffus$6 dielectric multi$1layer block$6 (charge ADJ trap$6) (oxide ADJ layer) anti$1tunnel$4 nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:39
L17	37	(gate channel diffus$6 dielectric multi$1layer block$6 (charge ADJ trap$6) (oxide ADJ layer) (oxygen$1rich ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:40
L18	37	(gate channel diffus$6 dielectric multi$1layer (charge ADJ trap$6) (oxide ADJ layer) (oxygen$1rich ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:41
L19	37	(diffus$6 dielectric multi$1layer (charge ADJ trap$6) (oxide ADJ layer) (oxygen$1rich ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:42
L20	37	(diffus$6 dielectric (charge ADJ trap$6) (oxide ADJ layer) (oxygen$1rich ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:42
L21	37	(diffus$6 (charge ADJ trap$6) (oxide ADJ layer) (oxygen$1rich ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	AND	ON	2017/09/26 15:42

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			DERWENT; IBM_TDB			
L22	142	(diffus$6 (charge SAME trap$6) (oxide SAME layer) (oxygen$1rich SAME nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:43
L23	109	L22 AND (H01L29/0676; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518; H01L29/66833; H01L29/7926; H01L29/792).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:43
L24	103	L22 AND (H01L29/408; H01L29/04; H01L29/0676; H01L29/16; H01L29/513; H01L29/518; H01L29/6683; H01L29/785; H01L29/78696; H01L29/792; H01L29/7926; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:48
L25	74	L22 AND (H01L21/28282).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:50
L26	30	L22 AND (B82Y10/00).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:51
L27	30	L22 AND (B82Y$/00).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:53
L28	30	L22 AND (B82Y$/$).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:53
L29	108	L22 AND (H01L21/$).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 15:53
L30	85	L22 AND (H01L21/28282; H01L21/823463; H01L21/28273).cpc.	US-PGPUB; USPAT; USOCR;	AND	ON	2017/09/26 15:55

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S1	53	(("POLISHCHUK") near3 ("Igor")).INV.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 15:47
S2	85	(("LEVY") near3 ("Sagy")).INV.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 16:53
S4	173	(("RAMKUMAR") near3 ("Krishnaswamy")).INV.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 16:54
S5	239	(("CYPRESS") near3 ("SEMICONDUCTOR") near3 ("CORPORATION")).AANM.	USPAT	AND	ON	2017/05/08 16:54
S6	53	(("POLISHCHUK") near3 ("Igor")).INV.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 16:54
S7	68	(("POLISHCHUK") near3 ("Igor")).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:54
S8	140	(("LEVY") near3 ("Sagy")).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:55
S9	260	(("RAMKUMAR") near3 ("Krishnaswamy")).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:55
S10	470	(("CYPRESS") near3 ("SEMICONDUCTOR") near3 ("CORPORATION")).AANM.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:55
S11	6260	(("CYPRESS") near3 ("SEMICONDUCTOR")).AS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:55
S12	177	(S7 OR S8 Or S9) AND (S10 OR S11)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:56

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S13	145	S12 AND memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 16:56
S14	31	(memory gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 17:00
S15	4	(memory gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/08 17:00
S16	6	((14/811346) or (15/335180) or (14/159315) or (14/811346) or (13/288919) or (12/152518)).APP.	US-PGPUB; USPAT	OR	OFF	2017/05/08 17:03
S17	4	((14/811346) or (15/335180) or (14/159315) or (14/811346) or (13/288919) or (12/152518)).APP.	USPAT	OR	OFF	2017/05/08 17:03
S18	43	("20030122204" | "20030169629" | "20050186741" | "20050230766" | "20060008959" | "20060131636" | "20060202261" | "20070231991" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080135946" | "20080175053" | "20080290399" | "20080291726" | "20080293207" | "20090039414" | "20090045452" | "20090179253" | "20100041222" | "20100117138" | "20100117139" | "20100155823" | "20100295118" | "20110248332" | "6287913" | "6906390" | "6912163" | "7642585" | "7688626" | "7713810" | "7723789" | "7737488" | "7790516" | "7948799" | "7999295" | "8063434" | "8222688" | "8264028" | "8315095" | "8482052" | "8859374").PN. OR ("9502543").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 17:05
S19	64	("20030122204" | "20050230766" | "20060131636" | "20070246753" | "20070262451" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080290399" | "20100041222" | "20100295118" | "6906390" | "6912163" | "7312496" | "7323742" | "7737488" | "7790516").PN. OR ("8063434").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/08 17:06
S20	330	(("20020154878") or ("20030227049") or ("20040104424") or ("20040227198") or ("20040251489") or ("20050098839") or ("20050224866") or ("20050245034") or ("20050266637") or ("20060113627") or ("20060192248") or ("20060220106") or	US-PGPUB; USPAT	OR	OFF	2017/05/08 17:26

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("20060237803") or ("20070051306") or ("20080150003") or ("20080286927") or ("20080293254") or ("20090179253") or ("20100041222") or ("20100117139") or ("20120068159") or ("5404791") or ("5500816") or ("5847411") or ("6023093") or ("6153543") or ("6162700") or ("6287913") or ("6429081") or ("6445030") or ("6833582") or ("6913961") or ("7250654") or ("7312496") or ("7601576") or ("7737488") or ("7790516") or ("8063434") or ("8067284") or ("8143129") or ("8264028") or ("8283261") or ("8860122") or ("7060594") or ("20040207002") or ("4104424") or ("4251489") or ("20060202263") or ("20070049048") or ("20070210371") or ("20080293207") or ("8029399") or ("20080296664") or ("20090045452") or ("20090294844") or ("20090302365") or ("20100117138") or ("20110018053") or ("20110237060") or ("4395438") or ("5405791") or ("6074915") or ("6136654") or ("6586349") or ("6670241") or ("6835621") or ("7084032") or ("7372113") or ("7390718") or ("7544565") or ("7588986") or ("7670963") or ("7713810") or ("8071453") or ("8318608") or ("8643124") or ("8993453") or ("9306025") or ("20070272971") or ("20090227116") or ("7927951") or ("20030183869") or ("20040183091") or ("20040183122") or ("20050056892") or ("20050205920") or ("20050227501") or ("20050230766") or ("20060228841") or ("20060261401") or ("6051880") or ("20070031999") or ("20070048916") or ("20070231991") or ("20080009115") or ("20080237694") or ("20090011609") or ("9152618") or ("2068250") or ("4843023") or ("4870470") or ("5793089") or ("6140187") or ("6277683") or ("6297173") or ("6399484") or ("6406960") or ("6444521") or ("6461899") or ("6661065") or ("6746968") or ("6818558") or ("7012299") or ("7018868") or ("7098154") or ("7238990") or ("7301185") or ("7315474") or ("7323742") or ("7521751") or ("7612403") or ("7646637") or ("8093128") or ("8222688") or ("8940645") or ("20060017092") or ("6001713") or ("6518113") or ("6717860") or ("7692246") or ("20010052615") or ("20030123307") or ("20030169629") or ("20040071030") or ("20040129988")).PN. or (("20050070126") or ("20050079659") or ("20050236679") or ("20050275010") or ("20060008959") or ("20060228899") or ("20070029625") or ("20080048237") or ("20080135946") or ("20080293255") or ("8087942") or ("20100295118") or ("20110163371") or ("2007167") or ("4257832") or ("5408115") or ("5550078") or ("5817170") or ("6015739") or ("6025267") or ("6174774")

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		or ("6297096") or ("6709928") or ("6713127") or ("6917072") or ("6946349") or ("6958511") or ("7115469") or ("7463530") or ("7479425") or ("7910429") or ("8710578") or ("9502543") or ("5245034") or ("20060051880") or ("20080290398") or ("20090206385") or ("20020141237") or ("20030122204") or ("20030124873") or ("3123307") or ("20040227196") or ("20050026637") or ("20050116279") or ("20060065919") or ("6261401") or ("20070200168") or ("20070262451") or ("20070268753") or ("7121380") or ("20080290400") or ("20090039414") or ("20090242969") or ("20130175604") or ("20140264551") or ("4490900") or ("5972765") or ("6114734") or ("6127227") or ("6157426") or ("6268299") or ("6365518") or ("6440797") or ("6586343") or ("6787419") or ("7033890") or ("7253046") or ("7450423") or ("7482236") or ("7576386") or ("7879738") or ("7948799") or ("8482052") or ("8633537") or ("8859374") or ("9355849") or ("20080087942") or ("8150003") or ("5773343") or ("3183869") or ("20050186741") or ("20060160303") or ("20060202261") or ("6081331") or ("20070121380") or ("20080121932") or ("20080146042") or ("20080272424") or ("20090152621") or ("20100155823") or ("0096687") or ("0283097") or ("20110248332") or ("5348903") or ("5464783") or ("5939333") or ("6217658") or ("6218700") or ("6335288") or ("6348380") or ("6468927") or ("6469343") or ("6602771") or ("6610614") or ("6677213") or ("6768856") or ("7015100") or ("7045424") or ("7338869") or ("7365389") or ("7535053") or ("7642585") or ("7999295") or ("8315095") or ("9349824") or ("20060228907") or ("8237694") or ("7279740") or ("20040067619") or ("20040094793") or ("20040129986") or ("20040173918") or ("20050110064") or ("20060111805") or ("60131636") or ("20060226490") or ("20060281331") or ("20070215940") or ("20070272916") or ("20080057644") or ("20080290399") or ("9294836") or ("4543707") or ("5573963") or ("5861347") or ("5937323")).PN. or (("6147014") or ("6150286") or ("6321134") or ("6624090") or ("6730566") or ("6768160") or ("6774433") or ("6903422") or ("6906390") or ("7033957") or ("7042054") or ("0711248") or ("7172940") or ("7262457") or ("7688626") or ("20060081331") or ("6113627") or ("6220106") or ("4667217") or ("8008713") or ("20020020890") or ("20020109138") or ("20030030100") or ("4094793") or ("20050093054") or ("20050141168") or ("5026637") or ("20050275012") or ("20060113586") or					

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S21	44	((oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/08 17:30
S22	34	((oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride)) AND S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/08 17:31
S23	3	(("20090179253") or ("6912163") or ("20080135946")).PN.	US-PGPUB; USPAT	OR	OFF	2017/05/08 17:36
S24	31	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:15
S25	40	(tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:16
S26	41	(tunnel dielectric multi$1layer (charge ADJ trap$6) (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:16
S27	44	(multi$1layer (charge ADJ trap$6) (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:16
S28	44	((charge ADJ trap$6) (oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR;	AND	ON	2017/05/08 21:16

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S29	44	((oxygen$1rich ADJ nitride) (oxygen$1lean ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:16
S30	958	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:17
S31	930	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:17
S32	7	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/05/08 21:17
S33	354	S31 AND (H01L29/0676; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518; H01L29/66833; H01L29/7926).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/08 21:18
S39	933	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:01
S40	19	S39 AND (H01L29/0676).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:01
S41	68	S39 AND (H01L29/4234).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:02
S42	23	S39 AND (H01L29/4916).cpc.	US-PGPUB;	AND	ON	2017/05/09

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			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			09:08
S43	34	S39 AND (H01L29/511).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:08
S44	215	S39 AND (H01L29/66833).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:08
S45	110	S39 AND (H01L29/7926).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:09
S46	276	S39 AND (H01L29/792).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:10
S47	422	S39 AND (H01L29/0676; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518; H01L29/66833; H01L29/7926; H01L29/792).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:10
S48	70	S39 AND (B82Y10/00).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 09:11
S49	0	("20090179253").PN.	USPAT	OR	OFF	2017/05/09 09:33
S50	1	("20090179253").PN.	US-PGPUB; USPAT	OR	OFF	2017/05/09 09:33
S51	1	("20080135946").PN.	US-PGPUB; USPAT	OR	OFF	2017/05/09 09:35
S52	1	("20060008959").PN.	US-PGPUB; USPAT	OR	OFF	2017/05/09 09:35
S53	1	(("6912163") or ("20070272916") or ("20070268753")).PN.	USPAT	OR	OFF	2017/05/09 09:43
S54	3	(("6912163") or ("20070272916") or ("20070268753")).PN.	US-PGPUB; USPAT	OR	OFF	2017/05/09 09:43

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S55	1	(11/830582).APP.	USPAT; USOCR	AND	ON	2017/05/09 09:50
S56	0	(11/811958).APP.	USPAT; USOCR	AND	ON	2017/05/09 09:55
S57	14	("20060261401" | "20080258203" | "6709928" | "20030123307" | "6445030" | "7450423" | "7042054" | "4543707" | "6157426" | "6677213" | "6958511" | "20020154878" | "6461899" | "6818558").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/09 09:57
S58	1	(11/131006).APP.	USPAT; USOCR	AND	ON	2017/05/09 10:08
S61	2	((oxygen$1rich ADJ nitride) (nitrogen$1rich ADJ nitride))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/09 12:07
S62	7	("20020185711" | "20060113586" | "20080272424" | "20080293207" | "20100157680" | "20110101442" | "8222688").PN. OR ("9537016").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/09 12:12
S63	0	(10/998445).APP.	USPAT; USOCR	AND	ON	2017/05/09 12:18
S64	1	("5,371,734").PN.	US-PGPUB; USPAT	OR	OFF	2017/05/10 07:53
S65	1	("5,924,080").PN.	US-PGPUB; USPAT	OR	OFF	2017/05/10 07:56
S66	24	("2008/0272424").URPN.	USPAT	AND	ON	2017/05/10 14:17
S67	24	("2008/0272424").URPN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/10 14:17
S68	238	("20090179253" | "20030227049" | "20040104424" | "20050098839" | "20050224866" | "20050245034" | "20050266637" | "20060113627" | "20060192248" | "20060220106" | "20070051306" | "20080286927" | "20090039414" | "20100041222" | "5500816" | "6023093" | "6153543" | "6162700" | "6445030" | "6833582" | "6913961" | "7250654" | "7312496" | "7601576" | "7737488" | "7790516" | "8063434" | "8067284" | "8143129" | "8283261" | "7060594" | "7799670" | "20040207002" | "4104424" | "4251489" | "20060202263" | "20070049048" | "20070210371" | "20070272971" | "20080293207" | "8029399" | "20080296664" | "20090302365" | "20100117138" | "4395438" | "5405791" | "6074915" | "6136654" | "6586349" | "6670241" | "6835621" | "7084032" | "7372113" | "7544565" | "7588986" |	US-PGPUB; USPAT; USOCR	AND	ON	2017/05/10 14:22

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S69	64	(gate channel tunnel dielectric block$6 (charge ADJ trap$6) layer) AND S68	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/05/10 14:23
S70	1	(11/197668).APP.	USPAT; USOCR	AND	ON	2017/05/10 14:38
S71	1004	(Yushin NEAR3 Nikolay).xp. OR (Yushin NEAR3 Nikolay).xa.	USPAT; USOCR	AND	ON	2017/05/10 16:01
S72	1004	(Yushin NEAR3 Nikolay).xp. OR (Yushin NEAR3 Nikolay).xa.	USPAT	AND	ON	2017/05/10 16:01
S73	14	S72 AND (channel silicon nanowire)	USPAT	SAME	ON	2017/05/10 16:01
S74	7	S72 AND (channel (silicon ADJ nanowire))	USPAT	SAME	ON	2017/05/10 16:02
S75	2	(11/397527).APP.	US-PGPUB; USPAT	OR	OFF	2017/05/10 16:03
S76	1	S75 AND (channel (silicon ADJ nanowire))	USPAT	SAME	ON	2017/05/10 16:04
S77	1	S75 AND (channel (silicon ADJ nanowire))	USPAT	AND	ON	2017/05/10 16:04
S78	1	(11/397527).APP.	USPAT; USOCR	AND	ON	2017/05/10 17:00
S79	1	(15/335180).APP.	US-PGPUB; USPAT	OR	OFF	2017/09/26 12:36
S80	71	(("POLISHCHUK") near3 ("Igor")).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 12:37
S81	143	(("LEVY") near3 ("Sagy")).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 12:37
S82	270	(("RAMKUMAR") near3 ("Krishnaswamy")).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 12:37
S83	531	(("CYPRESS") near3 ("SEMICONDUCTOR") near3 ("CORPORATION")).AANM.	US-PGPUB; USPAT;	AND	ON	2017/09/26 12:37

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			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S84	6396	(("CYPRESS") near3 ("SEMICONDUCTOR")).AS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 12:37
S85	184	(S80 OR S81 Or S82) AND (S83 OR S84)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 12:37
S86	152	S85 AND memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 12:37
S87	988	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 12:37
S88	432	S87 AND (H01L29/0676; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518; H01L29/66833; H01L29/7926; H01L29/792).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2017/09/26 12:37
S89	7	(gate channel diffus$6 tunnel dielectric multi$1layer block$6 (charge ADJ trap$6) layer nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2017/09/26 12:38

EAST Search History (Interference)

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5543336	A	1996-08-06	Enami et al.	Entire Document

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	2008290400	A1	2008-11-27	Jenne et al.	Entire Document
	2	20100006922	A1	2010-01-14	Matsuoka et al.	Entire Document
	3	20100178759	A1	2010-07-15	Kim et al.	Entire Document

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	SIPO Office Action for Chinese Application Number 2013800319699 (PM07024CIP1CN) dated 05/31/2017; 11 pages	
	2	TIPO Office Action for Taiwan Application Number 106107213 (PM07002CIP2TWD1) dated 07/04/2017; 6 pages	

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Examiner Signature	/NIKOLAY K YUSHIN/	Date Considered	09/26/2017

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Jordan/	Date (YYYY-MM-DD)	2017-07-28
Name/Print	Christopher Jordan	Registration Number	65809

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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	1	1107254	CN	A	1995-08-23	ENAMI HIROMICHI et al.	Entire Document	

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	1	SIPO Office Action for International Application No. 2013800168932 (PM07002CIP2CN) dated 04/21/2017; 7 pages	

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EXAMINER SIGNATURE

Examiner Signature	/NIKOLAY K YUSHIN/	Date Considered	09/26/2017

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A certification statement is not submitted herewith.

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Signature	/StoychoDDraganoff#56181/	Date (YYYY-MM-DD)	2017-05-25
Name/Print	Stoycho D. Draganoff	Registration Number	56181

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CONFIRMATION NO. 6223

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/335,180	10/26/2016 RULE	257	2893	PM07027D1CIP1C3

APPLICANTS

Cypress Semiconductor Corporation, San Jose, CA

INVENTORS

Igor Polishchuk, Fremont, CA;
Sagy Charel Levy, Zichron Yaakov, ISRAEL;
Krishnaswamy Ramkumar, San Jose, CA;

**** CONTINUING DATA ***************************

This application is a CON of 14/811,346 07/28/2015 PAT 9502543
which is a CON of 14/159,315 01/20/2014 PAT 9093318
which is a CON of 13/539,466 07/01/2012 PAT 8633537
which is a CIP of 13/288,919 11/03/2011 PAT 8859374
which is a DIV of 12/152,518 05/13/2008 PAT 8063434
which claims benefit of 60/940,160 05/25/2007

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

11/03/2016

Foreign Priority claimed	☐ Yes ☑ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☑ No					
Verified and Acknowledged	/NIKOLAY K YUSHIN/ Examiner's Signature	Initials	CA	13	20	3

ADDRESS

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198 CHAMPION COURT
SAN JOSE, CA 95134-1709
UNITED STATES

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15335180	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

CPC						
Symbol					**Type**	**Version**
H01L		29	/	4234	F	2013-01-01
H01L		29	/	0676	I	2013-01-01
H01L		29	/	4916	I	2013-01-01
H01L		29	/	7926	I	2013-01-01
H01L		29	/	66833	I	2013-01-01
H01L		29	/	511	I	2013-01-01
H01L		29	/	518	I	2013-01-01
B82Y		10	/	00	A	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
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NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 18	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893 (Primary Examiner)	09/26/2017 (Date)	O.G. Print Claim(s) 21	O.G. Print Figure 7A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	NIKOLAY YUSHIN	2893

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		H	0	1	L	29 / 00 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 18	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893 (Primary Examiner)	09/26/2017 (Date)	O.G. Print Claim(s) 21	O.G. Print Figure 7A

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	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17	12	33										
	2		18		34										
	3		19	14	35										
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	5	1	21	13	37										
	6	2	22	16	38										
	7	3	23	17	39										
	8	4	24	18	40										
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	11		27												
	12	8	28												
	13	9	29												
	14	10	30												
	15	11	31												
	16	7	32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 18	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893 (Primary Examiner)	09/26/2017 (Date)	O.G. Print Claim(s) 21	O.G. Print Figure 7A

Sandisk Technologies, Inc. - Ex. 1002, Page 001827

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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	1	6174758	B1	2001-01-16	Nachumovsky	Entire Document
	2	6462370	B2	2002-10-08	Kuwazawa	Entire Document

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020048200	A1	2002-04-25	Kuwazawa	Entire Document
	2	20050062098	A1	2005-03-24	Mahajani et al.	Entire Document

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	1	USPTO Final Rejection for US Application Number 14/605,231 (PM07024CIP1C1) dated 07/10/2017; 7 pages	
	2	USPTO Non-Final Rejection for US Application Number 15/376,282 (PM07027D1C4) dated 07/11/2017; 16 pages	

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	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Jordan/	Date (YYYY-MM-DD)	2017-07-28
Name/Print	Christopher Jordan	Registration Number	65809

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.K.Y/

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.K.Y/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15335180	POLISHCHUK ET AL.
	Examiner	Art Unit
	NIKOLAY YUSHIN	2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/0676; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518; H01L29/66833; H01L29/7926; H01L29/792	05/10/2017	NY
B82Y10/00	05/10/2017	NY
H01L29/408; H01L29/04; H01L29/0676; H01L29/16; H01L29/513; H01L29/518; H01L29/6683; H01L29/785; H01L29/78696; H01L29/792; H01L29/7926; H01L29/4234; H01L29/4916; H01L29/511; H01L29/518	9/26/2017	NY

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Keyword, inventor names, assignee searching - see search history	05/10/2017	NY
Updated keyword searching - see search history	9/26/2017	NY

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
H01L29	408; 04; 0676; 16; 513; 518; 6683; 785; 78696; 792; 7926; 4234; 4916; 511; 518	9/26/2017	NY

	/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
B82Y10	00	9/26/2017	NY

	/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893

To: patents@cypress.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 60909

Oct 04, 2017 04:31:36 AM

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Application	Document	Mailroom Date	Attorney Docket No.
15335180	NOA	10/04/2017	PM07027D1CIP1C3
	1449	10/04/2017	PM07027D1CIP1C3
	1449	10/04/2017	PM07027D1CIP1C3
	1449	10/04/2017	PM07027D1CIP1C3

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UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3	6223

60909 7590 11/03/2017

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
11/03/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

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Sandisk Technologies, Inc. - Ex. 1002, Page 001835

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 15335180
Applicant : Polishchuk
Filing Date : 10/26/2016
Date Mailed : 11/03/2017

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED.

See attachment(s).

A copy of this notice MUST be returned with the reply. Please address response to "Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

/Anthony McPhail/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 15335180 **Drawings filed: 10/26/2016**

IDENTIFICATION OF DRAWING DEFICIENCIES

- [ ] There is a hole or the image thereof within the illustration. FIG(s)
- [ ] The illustration is penetrated or traversed by a solid or broken line that is not intended to be part of the drawing, such as a dark line caused by a flaw in the copying process. FIG(s)
- [ ] An ink stamp or the image thereof obscures part of the illustration. FIG(s)
- [ ] The drawing is marred by black smudges, obliterations, or fax/copier marks (for example, speckles or dots in a substantial portion of the drawing). FIG(s)
- [ ] Figure numbers are duplicated or missing. FIG(s)
- [ ] Drawing sheet or figure is missing. FIG(s)
- [ ] Numbers, letters, or reference characters in the drawing have been crossed out or are illegibly handwritten. FIG(s)
- [X] The character of the lines, numbers, and letters is poor. FIG(s) 4A, 4B
- [ ] The drawing's background shows that the original drawing was made on graph paper or other paper with a pattern or decoration. FIG(s)
- [ ] The FIG. number label is placed in a location that causes the drawing to be read upside down. FIG(s)
- [ ] Data, a reference number, or part of the drawing is truncated or missing, or a lead line has no reference number. FIG(s)
- [ ] The drawing and/or the FIG. label contain(s) foreign language. FIG(s)
- [ ] This utility application contains a photograph of a view that is capable of being illustrated as a line drawing. FIG(s)
- [ ] A petition under 37 CFR 1.84(a)(2) to accept color drawings has been granted, but the brief description of the drawings in the specification does not contain (or has not been amended to contain) the paragraph required by 37 CFR 1.84(a)(2)(iii).
- [ ] This reissue application contains added and/or amended drawings that are not labeled as “New” or “Amended” or “Canceled” as required by 37 CFR 1.173(b)(3). FIG(s)
- [ ] This Design reissue application contains a drawing that is labeled as “Canceled” but is not surrounded by brackets, or a drawing that is surrounded by brackets but is not labeled as “Canceled.” See 37 CFR 1.173(b)(3). FIG(s)
- [ ] OTHER:
- [ ] COMMENTS:

Application No. 15335180

IDENTIFICATION OF SPECIFICATION/DRAWING INCONSISTENCIES

☐ On Page of the specification there is a brief description of FIG. , but the drawings filed do not include a drawing with that designation. Applicant must respond either by supplying the omitted drawing or by amending the specification to remove all references to that drawing.

☐ The drawings filed include FIG. , but the specification's brief description of the drawings does not describe a drawing with that designation. Applicant must respond either by amending the specification to add a brief description of that drawing or by correcting the drawings to remove the drawing in question.

☐ In the utility application, drawings are present in the application and are referred to in the detailed description of the invention, but the specification does not contain a brief description of the several views as required by 37 CFR 1.74 and 37 CFR 1.77(b)(9).

☐ The design application does not contain a description of the figure or figures of the drawing as required by 37 CFR 1.153(a) and 37 CFR 1.154(b)(4).

☐ In the plant application, the specification does not contain a brief description of the drawing as required by 37 CFR 1.163(c)(8).

☒ Page 36 of the specification refers to FIG. 20A-F, but no drawing with that designation is described in the brief description of the drawings and no drawing with that designation is present in the application. Applicant must respond either by amending the specification to remove all references to that drawing, or by supplying that drawing and amending the specification to add a brief description of it.

☐ In the reissue application, FIG. , is labeled as "New" but is not described in the reissue specification's brief description of the drawings. Applicant must respond by amending the reissue specification's brief description of the drawings to add a brief description of the new drawing.

☐ OTHER:

☐ COMMENTS:

To: patents@cypress.com,,
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Cc: PAIR_eOfficeAction@uspto.gov
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SAN JOSE, CA 95134-1709
UNITED STATES

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The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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Application	Document	Mailroom Date	Attorney Docket No.
15335180	M327	11/03/2017	PM07027D1CIP1C3

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

Doc code: IDS
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PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090065849	A1	2009-03-12	Noda	Entire Document
	2	20100270609	A1	2010-10-28	Olsen et al.	Entire Document

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	USPTO Non-Final Rejection for Application Number 15/099,025 (PM07002C2) dated 10/06/2017; 11 pages	
	2	USPTO Non-Final Rejection for Application Number 15/189,668 (PM07002CIP2C1) dated 09/22/2017; 11 pages	
	3	USPTO Notice of Allowance for Application Number 14/605,231 (PM07024CIP1C1) dated 10/18/2017; 8 pages	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
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Signature	/Christopher Jordan/	Date (YYYY-MM-DD)	2017-11-28
Name/Print	Christopher Jordan	Registration Number	65809

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/099,025	04/14/2016	Sagy Charel Levy	PM07002C2	3848

60909 7590 10/06/2017

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
CHOUDHRY, MOHAMMAD M	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
10/06/2017	ELECTRONIC

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Sandisk Technologies, Inc. - Ex. 1002, Page 001844

Office Action Summary	Application No. 15/099,025	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status Yes

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A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/29/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *21-40* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *21-40* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *04/10/2017 & 04/20/2017, 04/21/2017,05/25/2017& 07/26/2017*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority Date: 25 May, 2007

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be

commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 21 – 40 are rejected on the ground of nonstatutory double patenting as being unpatentable over claim 21 & 25 of U.S. Patent No. 9.355.849, hereinafter Levy.

With respect to claim 21. Levy discloses a method of forming a semiconductor device, the method comprising: forming a tunneling oxide layer; forming a first layer of a multi-layer charge storing layer over the tunneling oxide layer, wherein the first layer comprises at least silicon and oxygen; forming a second layer of the multi-layer charge

storing layer over the first layer, wherein the second layer comprises at least silicon and nitrogen, wherein a stoichiometric composition of the first layer is different from a stoichiometric composition of the second layer; and forming a blocking oxide layer over the second layer of the multi-layer charge storing layer (Claim 21 and 25).

Claims 22 – 40 are rejected by virtue of dependency on claim 21.

Claims 21 – 40 are rejected on the ground of nonstatutory double patenting as being unpatentable over claim 21 & 25 of U.S. Patent No. 8,643,124, hereinafter Levy.

With respect to claim 21. Levy discloses a method of forming a semiconductor device, the method comprising: forming a tunneling oxide layer; forming a first layer of a multi-layer charge storing layer over the tunneling oxide layer, wherein the first layer comprises at least silicon and oxygen; forming a second layer of the multi-layer charge storing layer over the first layer, wherein the second layer comprises at least silicon and nitrogen, wherein a stoichiometric composition of the first layer is different from a stoichiometric composition of the second layer; and forming a blocking oxide layer over the second layer of the multi-layer charge storing layer (Claim 1) .

Claims 22 – 40 are rejected by virtue of dependency on claim 21.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any

correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 21, 26 - 28, 31 – 38 & 40 is/are rejected under 35 U.S.C. 103 as being unpatentable over Bhattacharyya (US 2006/0261401, hereinafter Bhattacharyya).

With respect to claim 21. Bhattacharyya discloses a method of forming a semiconductor device (e.g. SONOS – Fig. 1A), the method comprising: forming a tunneling oxide layer (first layer of 112 and Para 0073); forming a first layer of a multi-layer charge storing layer (112/114/116/117) over the tunneling oxide layer, wherein the first layer comprises at least silicon and oxygen (oxygen rich layer); forming a second layer of the multi-layer charge storing layer over the first layer, wherein the second layer comprises at least silicon and nitrogen(114 – Para 0074, showing layer to be nitrogen rich SiON). and forming a blocking oxide layer over the second layer of the multi-layer charge storing layer (e.g. 116) .

Although, Bhattacharrya does not explicitly disclose wherein a stoichiometric composition of the first layer is different from a stoichiometric composition of the second layer. However, it is obvious to one of an ordinary skilled in the art to claim two layers as

being different per stoichiometric composition being nitride and having different contents of nitrogen and oxygen.

With respect to claim 26 - 28. Bhattacharyya discloses the method of claim 21, wherein the first layer and the second layer of the multi-layer charge storing layer are formed sequentially without breaking vacuum in a deposition chamber wherein the first layer and the second layer of the multi-layer charge storing layer are formed at a same substrate temperature, wherein each of the first layer and the second layer of the multi-layer charge storing layer is formed at between 700℃ and 850℃. (E.g. both contains SION composition and can be formed in same in chamber without a break).

With respect to claim 31 - 32. Bhattacharyya has disclosed the method of claim 21, wherein the first layer of the multi-layer charge storing layer includes a thickness of between 10 Angstroms and 80 Angstrom & wherein a thickness ratio of the first layer relative to the second layer of the multi-layer charge storing layer is at least 1:4 (Bhattacharyya has disclosed in the claimed invention of claim 21 and mere changes in relative thickness does not make the disclosed device inoperable and applicant has not explicitly shown the criticality to claimed invention)

With respect to claim 33 – 37. Bhattacharyya discloses the method of claim 21, wherein a concentration of oxygen is greater in the first layer than in the second layer, wherein each of the first layer and the second layer of the multi-layer charge storing layer comprises silicon, nitrogen, and oxygen***,*** wherein the second layer of the multi-layer charge storing layer comprises a silicon-rich nitride, wherein the semiconductor device is a semiconductor memory device, wherein the tunneling oxide layer comprises

silicon dioxide (Si02) (Bhattacharyya has discloses specific concentrations of the silicon and nitrogen on several instances, for instance, 114 - Para 0074 showing layer to be nitrogen rich SION making it oxygen lean and an other instance K2 - K3 of 112 & 113).

With respect to claim 38 & 40. Bhattachryya discloses the method of claim 21, wherein the tunneling oxide layer includes a thickness of between 15 Angstroms and 22 Angstroms & The method of claim 21, wherein the blocking oxide layer includes a thickness of between 10 Angstroms and 80 Angstrom. Bhattacharyya has disclosed claimed invention of claiml except the explicit disclosure of optimum thickness of both first and second oxynitride layers. However, in view of applicant specification (e.g. Para 0028), there is range specified of 7nm - 15 nm or it can be about 10 nm for first and second oxynitride layers. Bhattacharyya clearly disclose the range of both first and second oxynitiride layers to be about l0nm (e.g.Para 0071). Further, applicant has not shown any criticality to claimed thickness that will make the device inoperable. Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Bhattacharyya's disclosed invention and claim optimum thicknesses to increase charge retention, as taught by Bhattacharyya (Abstract).

Claims 22 – 25 & 39 is/are rejected under 35 U.S.C. 103 as being unpatentable over Bhattacharyya in view of Halliyal et al (US 6958511, hereinafter Halliyal).

With respect to claim 22 - 25 & 39. Bhattacharyya discloses the method of claim 21.

Bhattacharyya does not explicitly disclose further comprising steam annealing at least the second layer of the multi-layer charge layer, and forming tunneling oxide layer comprises steam annealing, wherein the steam annealing reduces a number of traps formed near a top surface of the second layer of the multi-layer charge, wherein the steam annealing is performed after forming the blocking oxide layer, wherein steam annealing reduces a number of traps formed near a top surface of the blocking oxide layer.

In an analogous art, Halliyal discloses steam annealing at least the second layer of the multi-layer charge layer, and forming tunneling oxide layer comprises steam annealing, wherein the steam annealing reduces a number of traps formed near a top surface of the second layer of the multi-layer charge, wherein the steam annealing is performed after forming the blocking oxide layer, wherein steam annealing reduces a number of traps formed near a top surface of the blocking oxide layer (e.g. Para 11, lines 15 – 30) to control migration of a layer characteristics such from charge storing layer into a bottom oxide layer etc).

With respect to claim 29. Bhattacharyya discloses the method of claim 26, wherein forming the second layer comprises decrease a flow rate ratio of a nitrous oxide (N2O) / ammonia (NH3) gas mixture relative to dichlorosilane (Sit^Cli) / ammonia (NH3) gas mixture (Halliyal; Col 12 lines 10- 30).

With respect to claim 30. Bhattacharyya discloses The method of claim 21, wherein at least one of the first layer and the second layer of the multi-layer charge

storing layer is formed using deuterated-ammonia (ND3) (Halliyal; Col 12 – lines 10 – 20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 1-571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOHAMMAD CHOUDHRY/

Primary Examiner, Art Unit 2816

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/189,668	06/22/2016	Sagy LEVY	PM07002CIP2C1	6782

60909 7590 09/22/2017

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
CHOUDHRY, MOHAMMAD M

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
09/22/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@cypress.com

Sandisk Technologies, Inc. - Ex. 1002, Page 001855

Office Action Summary	Application No. 15/189,668	Applicant(s) LEVY ET AL.	
	Examiner MOHAMMAD CHOUDHRY	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/22/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *See Continuation Sheet*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Continuation of Attachment(s) 2). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :09/27/2016, 10/28/2016, 01/23/2017, 04/10/2017,04/17/2017,04/20/2017,04/21/2017,05/25/2017,07/27/2017

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DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file

provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1, 10 & 16 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1 - 5 of U.S. Patent No. 9,449,831 ('831). Although the claims at issue are not identical, they are not patentably distinct from each other because:

With respect to claim 1. '831 discloses a method comprising:

forming, in a semiconducting material over a surface of a substrate, a channel connecting a source and a drain of a memory device (...source and a drain); and

forming a gate abutting the channel, wherein forming the gate comprises: forming a tunnel oxide layer abutting the channel(…channel…);

forming a multi-layer charge storing layer (.....multi-layer charge....) over the tunnel oxide layer, the multi-layer charge storing layer including a first nitride layer over the tunnel oxide layer and a second nitride layer over the first nitride layer, wherein a stoichiometric composition of the first nitride layer results in it being substantially trap free, and a stoichiometric composition of the second nitride layer results in it being trap dense, forming a blocking dielectric layer over the multi-layer charge storing layer, and treating the blocking dielectric layer to reduce a number of traps in a top surface thereof (claim 3).

Claims 2 – 9 are rejected by virtue of dependency on claim 1.

With respect to claim 10. '831 discloses a method comprising:

forming, in a semiconducting material over a surface of a substrate, a channel connecting a source and a drain of a memory device; (...source and drain...)

forming a gate abutting the channel, wherein forming the gate comprises: forming a tunnel oxide layer abutting the channel (…abutting…);

forming a multi-layer charge storing layer over the tunnel oxide layer, the multi-layer charge storing layer including a substantially trap free, oxygen-rich, first oxynitride layer over the tunnel oxide layer and a trap dense, oxygen-lean, second oxynitride layer over the first oxynitride layer; and forming a blocking dielectric layer over the multi-layer charge storing layer, wherein the second oxynitride layer further comprises a concentration of carbon selected to increase a number of traps therein (…carbon…).

Claims 11 – 15 are rejected by virtue of dependency on claim 10.

With respect to claim 16. A method comprising: forming, in a semiconducting material over a surface of a substrate, a channel connecting a source and a drain of a memory device (...source and drain...); and

forming a gate abutting the channel, wherein forming the gate comprises: forming a tunnel oxide layer abutting the channel (…abutting…),

forming a multi-layer charge storing layer over the tunnel oxide layer, the multi-layer charge storing layer including a first nitride layer over the tunnel oxide layer and a second nitride layer over the first nitride layer, wherein the first nitride layer comprises a stoichiometric composition that results in it being substantially trap free, and the second nitride layer comprises a stoichiometric composition, including a concentration of carbon, that results in it being trap dense (…trap dense…),

forming a blocking dielectric layer over the multi-layer charge storing layer, and treating the blocking dielectric layer to reduce a number of traps in a top surface thereof (…a blocking dielectric…).

Claims 17 – 20 are rejected by virtue of dependency on claim 16.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Noda (US 2009/0065849, hereinafter Noda) in view of Olsen et al (US 2010/0270609, hereinafter Olsen).

With respect to claim 1. Noda discloses a method comprising:

forming, in a semiconducting material (20 of Fig. 2A – 2F) over a surface of a substrate, a channel (16) connecting a source (17) and a drain (18) of a memory device; and

forming a gate abutting the channel, wherein forming the gate comprises: forming a tunnel oxide layer (11) abutting the channel;

forming a multi-layer charge storing layer over the tunnel oxide layer, the multi-layer charge storing layer including a first nitride layer (12A) over the tunnel oxide layer and a second nitride layer (14) over the first nitride layer, wherein a stoichiometric composition of the first nitride layer results in it being substantially trap free (Para 0115),

and a stoichiometric composition of the second nitride layer results in it being trap dense.

Noda does not explicitly disclose forming a blocking dielectric layer over the multi-layer charge storing layer, and treating the blocking dielectric layer to reduce a number of traps in a top surface thereof.

In an analogous art, Olsen discloses forming a blocking dielectric layer over the multi-layer charge storing layer, and treating the blocking dielectric layer to reduce a number of traps in a top surface thereof (0025).

Therefore, it would have been obvious to one of an ordinary skilled in the art at the time of invention to modify Noda's disclosed structure and form blocking dielectric layer over multi-layer to reduce leakage.

Allowable Subject Matter

Claims 10 and 16 are allowed.

Claims 11 – 15 and 17 – 20 are allowed by virtue of dependency on claim 10 and 16.

Claims 2 – 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOHAMMAD CHOUDHRY whose telephone number is (571)270-5716. The examiner can normally be reached on Monday, Friday 10:00AM - 4:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 1-571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOHAMMAD CHOUDHRY/
Primary Examiner, Art Unit 2816

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SAN JOSE, CA 95134-1709

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 10/18/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/605,231	01/26/2015	Krishnaswamy Ramkumar	PM07024CIP1C1	4843

TITLE OF INVENTION: Radical Oxidation Process For Fabricating A Nonvolatile Charge Trap Memory Device

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/18/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 10/18/2017
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/605,231	01/26/2015	Krishnaswamy Ramkumar	PM07024CIP1C1	4843

TITLE OF INVENTION: Radical Oxidation Process For Fabricating A Nonvolatile Charge Trap Memory Device

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/18/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THANH T	2893	438-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/605,231	01/26/2015	Krishnaswamy Ramkumar	PM07024CIP1C1	4843

60909 7590 10/18/2017

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 10/18/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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Notice Requiring Inventor's Oath or Declaration	Application No. 14/605,231	Applicant(s) Krishnaswamy Ramkumar	
	Examiner NGUYEN, THANH T	Art Unit 2893	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) MUST be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

- A properly executed inventor's oath or declaration has not been received for the following inventor(s): **Krishnaswamy Ramkumar**, **Sagy Charel Levy**, and **Jeong Soo Byun**.
  Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/605,231	Applicant(s) RAMKUMAR ET AL.	
	Examiner THANH T. NGUYEN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/3/17*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *21-25, 35-38, 40-44*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

The present application is being examined under the pre-AIA first to invent provisions.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

Claims 21-25, 35-38, 40-44 are allowed because none of the prior art alone or in combination teaches or suggests the particular subset of the process steps in forming a multi-layer charge storing layer overlying the tunnel oxide layer, the multilayer charge storing layer comprising an oxygen-rich, first layer comprising a nitride on the tunnel oxide layer in which a composition of the first layer results in it being substantially trap free, and a second layer comprising a Zirconium or Yttrium based high K dielectric material on the first layer in which a composition of the second layer results in it being trap dense.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (571) 272-1664. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

/THANH T NGUYEN/

Primary Examiner, Art Unit 2893

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15335180
Filing Date	2016-10-26
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1C3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Sandisk Technologies, Inc. - Ex. 1002, Page 001874

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

	1	SIPO Office Action for Application Number 20120000107.5 (PM07002CIP1CN) dated 09/20/2017; 6 pages	
	2	SIPO Office Action for Application Number 201380031840.8 (PM07027D1CIP1CN) dated 09/25/2017; 6 pages	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15335180
	Filing Date	2016-10-26
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1C3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Jordan/	Date (YYYY-MM-DD)	2017-11-28
Name/Print	Christopher Jordan	Registration Number	65809

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

CONCISE EXPLANATION UNDER 37 CFR § 1.98(a)(3) OF FOREIGN LANGUAGE DOCUMENTS

To the Honorable Commissioner of Patents and Trademarks:

In connection with an Information Disclosure Statement filed on even date herewith, Applicant hereby submits the following concise explanation under 37 CFR § 1.98(a)(3) of a foreign language document or documents disclosed therein:

> Each foreign language document contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a related foreign application.

Pursuant to 37 CFR 1.97(g), the filing of the Information Disclosure Statement shall not be construed as a representation that a search has been made.

Pursuant to 37 CFR 1.97 (h), the filing of the Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b).

Respectfully submitted by:

Date: 11/28/2017

Signature: /Christopher Jordan/
Name: Christopher Jordan
Reg. No.: 65809

中华人民共和国国家知识产权局

100192

北京市海淀区学清路8号8座1601A
北京安信方达知识产权代理有限公司 高瑜,郑霞

发文日：

2017年09月20日

申请号或专利号：201280000107.5　　发文序号：2017091501177400

案件编号：　1F214397

发明创造名称：　具有多重氮氧化物层的氧化物-氮化物-氧化物堆叠

复审请求人：　赛普拉斯半导体公司

复　审　通　知　书

复审请求人：

专利复审委员会对上述专利申请的复审请求已经开始审理。

请在收到本通知书之日起1个月内陈述意见，期满未答复的，根据专利法实施细则第63条第1款的规定，该复审请求视为撤回。

在对专利复审委员会的复审通知书作出答复时，可以修改专利申请文件，修改应当符合专利法第33条、专利法实施细则第61条的规定及审查指南第4部分第2章第4.2节有关修改文本的审查的规定。修改的申请文件应当提交一式两份。

对专利复审委员会发出的复审通知书，复审请求人应当在收到该通知书之日起1个月内针对通知书指出的缺陷进行书面答复；期满未进行书面答复的，其复审请求视为撤回。复审请求人提交无具体答复内容的意见陈述书的，视为对复审通知书中的审查意见无反对意见。

通知的具体内容请见正文。

附：通知书正文5页。

注：陈述意见时请注明案件编号及专利申请号。

合议组组长：蒋媛婧　主审员：刘乐　参审员：刘博

中华人民共和国国家知识产权局 复审委员会 专利复审专用

200908
2009.10

纸件申请，回函请寄：100088 北京市海淀区蓟门桥西土城路6号　国家知识产权局专利局复审和无效审查部
电子申请，应当通过电子专利申请系统以电子文件形式提交相关文件。除另有规定外，以纸件等其他形式提交的文件视为未提交。

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复审通知书正文

国家知识产权局原审查部门以本发明专利申请不符合专利法第 22 条第 3 款的规定为由于 2016 年 11 月 03 日驳回了本发明专利申请（下称本申请）。应申请人赛普拉斯半导体公司（下称复审请求人）于 2017 年 02 月 17 日提出的复审请求，专利复审委员会成立合议组对本案进行审理，现提出如下审查意见：

（1） 审查文本的认定

复审请求人于 2017 年 02 月 17 日提交复审请求时提交了权利要求第 1-10 项的修改替换页。本次复审通知书所针对的文本为：复审请求人在 2012 年 03 月 27 日进入中国国家阶段时提交的说明书摘要、摘要附图及说明书附图图 1-7，2014 年 04 月 30 日提交的说明书第 1-56 段，以及 2017 年 02 月 17 日的权利要求 1-10 项。

（2） 关于专利法第 22 条第 3 款

本次复审通知书引用的对比文件与驳回决定所引用的对比文件相同，即：

对比文件1：公开号CN 101517714A，公开日2009年08月26日；

对比文件 3：公开号 CN 101859702A，公开日 2010 年 10 月 13 日。

1、权利要求 1-10 不具备专利法第 22 条第 3 款规定的创造性

1.1、权利要求1要求保护一种形成半导体装置的方法。

对比文件1公开了一种形成半导体装置的方法(参见说明书第8页，第10页第3-4段，第14页、图5，9)，包含在基板的含硅层上形成氮化氧化硅的隧道氧化物层516，在隧道氧化物层上沉积形成高硅、高氧的氮氧化物层的第一电荷俘获层518A（相当于第一电荷储存层），该氮氧化物按化学计量比组成使该第一电荷俘获层具有低密度陷阱，该电荷俘获层通过CVD工艺形成，使用包含硅源、含氧气体以及氘化氮ND3的处理气体形成，在该第一电荷俘获层上直接沉积包含低氧、高氮、高硅的氮氧化物层的第二电荷俘获层，该低氧、高氮、高硅的氮氧化物层按化学计量比组成使其具有高密度陷阱；在该第二电荷俘获层上形成阻挡氧化物层520，在该阻挡氧化物层上形成含硅的栅极层；另外，如本申请说明书第48段记载的，由于第二电荷储存层706A中贫氧富硅，其中陷阱位点将产生与程式化装置中捕获电荷产生电场相反的电场，而对比文件1和本申请的层结构相同（参见说明书第8页第2-4段），底层氮氧化物层具有高硅高氧以具有低密度陷阱，顶层氮氧化层具有高硅低氧以具有高密度陷阱，基于同样的原理，该高的陷阱位密度也必然会导致产生的第二电场产生与程式化装置中捕获电荷产生电场（即第一电场）相反。对比文件1第9页最后1段到第10页第1段也公开了，在形成阻挡层820（也即第二电荷储存层上形成阻挡氧化物层）后，通过氧化退火致密化阻挡层，能阻

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止陷阱迁移到电荷俘获层和阻挡层之间的界面（也即降低陷阱数目），也减小了擦除状态下阻挡氧化物的电场效应，次电场效应可以减小电子回流（也即降低第三电场）。说明书第15页第2段记载了，在第二电荷储存层518B之后沉积阻挡层520，之后在水蒸汽中再氧化来增密阻挡层氧化物（也即退火第二电荷储存层和阻挡氧化物层）。

权利要求1与对比文件1的区别：（1）第一电荷储存层实质上无陷阱；（2）隧道氧化物层由二氧化硅组成，以及退火降低了阻挡氧化物层和第二电荷储存层顶面附近的陷阱数目、降低了阻挡氧化物层上的第三电场。基于上述区别特征可以确定权利要求1相对于对比文件1实际所要解决的技术问题是：（1）防止数据保持性流失；（2）调节能带分布，延长电荷保存时间。对于区别技术特征（1），在对比文件1已经给出了第一电荷储存层具有低密度陷阱的启示下，进一步减小陷阱密度直至实质上无陷阱从而提高薄膜质量、防止数据保持性流失，这对于本领域技术人员而言是常规选择。

对于区别技术特征（2），对比文件3公开了含多层氮氧化物层的氧化物-氮化物-氧化物堆栈，并具体公开了（参见说明书[0046]-[0059]段，附图2-4）：在基板208的含Si层206上形成二氧化硅的隧道氧化物层216（参见说明书[0048]段）；在第二电荷储存层220A上形成阻挡氧化物层218；使用蒸汽退火第二电荷储存层220A和阻挡氧化物层218，减少了形成在两层顶层附近的陷阱，减小或消除了阻挡氧化物层上的电场（参见说明书[0053]段）。由此可见，对比文件3公开了权利要求1的区别技术特征（2），所起的作用均为调节能带分布以及延长电荷保存时间，也即对比文件3给出了将上述区别技术特征应用于对比文件1以进一步解决其技术问题的启示。

因此，在对比文件1的基础上结合对比文件3、公知常识得到权利要求1的技术方案是显而易见的，该权利要求不具有突出的实质性特点和显著的进步，不具备专利法第22条第3款规定的创造性。

1.2、权利要求2引用权利要求1，本领域技术人员在面对降低缺陷密度的技术问题时，在对比文件1已经给出了利用氧含量控制缺陷密度的技术教导下，能够依照缺陷密度需要合理调整氧含量获得所需缺陷密度，通过有限的试验得到第一电荷储存层中氧的浓度选择35%是显而易见的。所以，在其引用的权利要求不具备创造性或创造性时，该权利要求不符合专利法第22条第3款有关创造性的规定。

1.3、权利要求3引用权利要求1，对比文件1（参见说明书第8页第2-3段）公开了多层电荷储存层的制作方法与本申请的制作方法类似，且第二电荷俘获层的高密度陷阱增加了编程电压和擦除电压之间的差值，因而本领域技术人员在对比文件1的启示下容易得到半导体装

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置在程式电压和擦除电压之间的规定差值下的寿命终止增加至少20年。所以，在其引用的权利要求不具备创造性时，该权利要求不符合专利法第22条第3款有关创造性的规定。

1.4、权利要求4引用权利要求1，对比文件1（参见说明书第8页第2-3段）公开了第一电荷俘获层具有低密度陷阱，第二电荷俘获层具有高密度陷阱，并且第二电荷俘获层的陷阱密度越高，多层电荷储存层的性能越好，根据该启示，本领域技术人员容易得到使第二俘获层比第一电荷俘获层具有高至少1000倍的电荷陷阱密度。所以，在其引用的权利要求不具备创造性时，该权利要求不符合专利法第22条第3款有关创造性的规定。

1.5、权利要求5引用权利要求1，本领域技术人员在面对提高隧穿层质量的技术问题时，能够依照薄膜质量要求选用各种常用的氧化硅制备工艺并调整参数获得所需薄膜质量，在ISSG腔室中在至少1000℃的温度下使用在该基板上氧气(O2)与氢气(H2)之间的反应利用自由基氧化进行生长形成隧道氧化物层是显而易见的。所以，在其引用的权利要求不具备创造性时，该权利要求不符合专利法第22条第3款有关创造性的规定。

1.6、权利要求6引用权利要求1，对比文件1（参见说明书第14页最后一段）公开了阻挡氧化物层通过热能氧化第二电荷俘获层的一部分形成。所以，在其引用的权利要求不具备创造性时，该权利要求不符合专利法第22条第3款有关创造性的规定。

1.7、权利要求7引用权利要求1，本领域技术人员在面对提高氮化物电荷储存层质量的技术问题时，能够依照薄膜质量要求选用各种常用的氮化硅制备工艺并调整参数获得所需薄膜质量，在CVD制程中使用包含以7:1至1:7的比率混合的双叔丁基胺基硅烷(BTBAS)及氨(NH3)的处理气形成第二电荷储存层也是本领域技术人员的常规选择。所以，在其引用的权利要求不具备创造性时，该权利要求不符合专利法第22条第3款有关创造性的规定。

1.8、权利要求8引用权利要求1，对比文件1（参见说明书第9页第2段）公开了顶端氧氮化物（即第二电荷储存层）的厚度与底端氧氮化物（即第一电荷储存层）的厚度比为4：1（也即第二层厚度大于第一层厚度）。所以，在其引用的权利要求不具备创造性时，该权利要求不符合专利法第22条第3款有关创造性的规定。

1.9、权利要求9引用权利要求1，对比文件1第9页最后1段到第10页第1段也公开了，在形成阻挡层820后，通过氧化退火致密化阻挡层，能阻止陷阱迁移到电荷俘获层和阻挡层之间的界面，也减小了擦除状态下阻挡氧化物的电场效应，次电场效应可以减小电子回流，对比文件1第15页第2段公开了，步骤906沉积阻挡层之后步骤908再氧化来增密阻挡层氧化物，并且再氧化的气体包含水蒸气，也即蒸汽氧化，该退火氧化步骤必然能同时作用于阻挡氧化物层以及下方的第二电荷储存层，相同的材料、相同的工艺必然能起到相似的技术效果，也即

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能够降低陷阱数目和第三电场。而在基板上其他区域的蒸汽氧化过程中同步进行蒸汽退火以节省工序对本领域技术人员是显而易见的。因此，对比文件1公开了权利要求9的附加技术特征，所起作用均为减小缺陷、电场，因此该权利要求不具备创造性。

此外，对比文件3（参见说明书第53段）公开了具有ONO结构的半导体装置的制作方法，其中在用于同时在基板的的不同区域中形成另一氧化物的蒸汽氧化制程期间，蒸汽退火顶端氧氮化物合阻挡氧化物层218。上述技术特征在对比文件3中所起的作用和在本申请中所起的作用相同，都是为了提高阻挡氧化物层的品质。根据该启示，本领域技术人员容易想到在对比文件1中对于不同区域同时采用上述蒸汽退火工艺以节省工序。因此，结合对比文件1、3和公知常识，得到该权利要求要求保护的技术方案对于本领域的技术人员来说是显而易见的。所以，该权利要求不具有突出的实质性特点和显著的进步，不具备专利法第22条第3款规定的创造性。

1.10、权利要求10引用权利要求1，对比文件3的[0048]段记载了二氧化硅隧穿层216的具体制备工艺，与本申请的工艺，反应气体、温度等参数均相同，必然能实现相同的不含N的技术特征，因此对比文件3隐含公开了该附加技术特征，权利要求10不具备创造性。

（3） 对复审请求人相关意见的评述

复审申请人在意见陈述书中认为：对比文件1、对比文件3没有公开权利要求1中增加技术特征“在该第二电荷储存层上形成阻挡氧化物层；以及退火该第二电荷储存层和阻挡氧化物层以降低该阻挡氧化物层的顶面附近和该第二电荷储存层的顶面附近形成的陷阱数目，降低该阻挡氧化物层上的第三电场”。

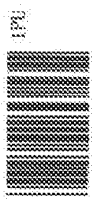
合议组认为：（1）对比文件1第9页最后1段到第10页第1段也公开了，在形成阻挡层820后，通过氧化退火致密化阻挡层，能阻止陷阱迁移到电荷俘获层和阻挡层之间的界面，也减小了擦除状态下阻挡氧化物的电场效应，此电场效应可以减小电子回流；对比文件1第15页第2段公开了，步骤906沉积阻挡层之后步骤098再氧化来增密阻挡层氧化物，并且再氧化的气体包含水蒸气，也即本申请[0033]段的蒸汽退火，该退火步骤必然能同时作用于阻挡氧化物层以及下方的第二电荷储存层，相同的材料、相同的工艺必然能起到相似的技术效果，也即能够降低陷阱数目和第三电场。

（2）此外，对比文件3说明书第53段明确公开了：“蒸气退火提高了顶端氧化层218（即阻挡氧化层）的质量，减少了形成在顶端氧化层的顶层附近和下面的顶端氧氮化物层220A的顶层附近的陷阱，因而减小或实质上消除会形成顶端氧化层的电场，而这将导致电荷载流

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子的回流以及避免影响电荷存储层的数据或电荷保持。”。因此，对比文件3也明确公开了该新增技术特征，所起作用相同。

因此，合议组对复审请求人的意见不予支持。



复审请求人应在收到本通知之日起一个月内作出答复。如果复审请求人不能在上述期限内提出本申请符合专利法及其实施细则规定的充分理由，或者所提交的修改文件仍不符合专利法及其实施细则的相关规定，合议组将作出维持驳回决定的复审决定。逾期不答复，该复审请求将被视为撤回。

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中华人民共和国国家知识产权局

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北京市海淀区学清路8号B座1601A 北京安信方达知识产权代理有限公司
张瑞 郑霞

发文日：

2017年09月25日

申请号或专利号：**201380031840.8**　　发文序号：**2017092002093520**

申请人或专利权人：赛普拉斯半导体公司

发明创造名称：具有多个电荷存储层的存储器晶体管

第二次审查意见通知书

1. ☒审查员已经收到申请人于2017年6月14日提交的意见陈述书，在此基础上审查员对上述专利申请继续进行实质审查。

☐根据国家知识产权局专利复审委员会于_____年_____月_____日作出的复审决定，审查员对上述专利申请继续进行实质审查。

☐_____

2. ☐经审查，申请人于_____提交的修改文件，不符合专利法实施细则第51条第3款的规定，不予接受。

3. 继续审查是针对下列申请文件进行的：

☐上述意见陈述书中所附的经修改的申请文件。

☒前次审查意见通知书所针对的申请文件以及上述意见陈述书中所附的经修改的申请文件替换文件。

☐前次审查意见通知书所针对的申请文件。

☐上述复审决定所确定的申请文件。

☐_____

4. ☒本通知书未引用新的对比文件。

☐本通知书引用下列对比文件(其编号续前，并在今后的审查过程中继续沿用)：

编号	文件号或名称	公开日期（或抵触申请的申请日）

5. 审查的结论性意见：

关于说明书：

☐申请的内容属于专利法第5条规定的不授予专利权的范围。

☐说明书不符合专利法第26条第3款的规定。

☐说明书的修改不符合专利法第33条的规定。

☐说明书的撰写不符合专利法实施细则第17条的规定。

☐_____

关于权利要求书：

☐权利要求_____不符合专利法第2条第2款的规定。

☐权利要求_____不符合专利法第9条第1款的规定。

纸件申请，回函请寄：100088 北京市海淀区蓟门桥西土城路6号　国家知识产权局专利局受理处收

电子申请，应当通过电子专利申请系统以电子文件形式提交相关文件。除另有规定外，以纸件等其他形式提交的文件视为未提交。

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□权利要求_____不具备专利法第 22 条第 2 款规定的新颖性。
☒权利要求 1-20 不具备专利法第 22 条第 3 款规定的创造性。
□权利要求_____不具备专利法第 22 条第 4 款规定的实用性。
□权利要求_____属于专利法第 25 条规定的不授予专利权的范围。
□权利要求_____不符合专利法第 26 条第 4 款的规定。
□权利要求_____不符合专利法第 31 条第 1 款的规定。
□权利要求_____的修改不符合专利法第 33 条的规定。
□权利要求_____不符合专利法实施细则第 19 条的规定。
□权利要求_____不符合专利法实施细则第 20 条的规定。
□权利要求_____不符合专利法实施细则第 21 条的规定。
□权利要求_____不符合专利法实施细则第 22 条的规定。
□_____

□申请不符合专利法第 26 条第 5 款或者实施细则第 26 条的规定。
□申请不符合专利法第 20 条第 1 款的规定。
□分案申请不符合专利法实施细则第 43 条第 1 款的规定。
上述结论性意见的具体分析见本通知书的正文部分。

6.基于上述结论性意见，审查员认为：

□申请人应当按照通知书正文部分提出的要求，对申请文件进行修改。
□申请人应当在意见陈述书中论述其专利申请可以被授予专利权的理由，并对通知书正文部分中指出的不符合规定之处进行修改，否则将不能授予专利权。
☒专利申请中没有可以被授予专利权的实质性内容，如果申请人没有陈述理由或者陈述理由不充分，其申请将被驳回。
□_____

7. 申请人应注意下列事项：

（1）根据专利法第 37 条的规定，申请人应当在收到本通知书之日起的 2 个月内陈述意见，如果申请人无正当理由逾期不答复，其申请将被视为撤回。

（2）申请人对其申请的修改应当符合专利法第 33 条的规定，不得超出原说明书和权利要求书记载的范围，同时申请人对专利申请文件进行的修改应当符合专利法实施细则第 51 条第 3 款的规定，按照本通知书的要求进行修改。

（3）申请人的意见陈述书和/或修改文本应当邮寄或递交国家知识产权局专利局受理处，凡未邮寄或递交给受理处的文件不具备法律效力。

（4）未经预约，申请人和/或代理人不得前来国家知识产权局与审查员举行会晤。

8．本通知书正文部分共有 4 页，并附有下列附件：

□引用的对比文件的复印件共_____份_____页。
□_____

审查员：孙鹏　　联系电话：020-28958385　　审查部门：专利审查协作广东中心电学发明审查部

纸件申请，回函请寄：100088 北京市海淀区蓟门桥西土城路 6 号　国家知识产权局专利局受理处收
电子申请，应当通过电子专利申请系统以电子文件形式提交相关文件。除另有规定外，以纸件等其他形式提交的文件视为未提交。

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第二次审查意见通知书

申请号:2013800318408

申请人于2017年06月14日提交了意见陈述书和经过修改的申请文件，审查员在阅读了上述文件后，对该申请继续进行审查，再次提出如下审查意见：

1、权利要求1不具备专利法第22条第3款规定的创造性：

权利要求1要求保护一种半导体设备，对比文件1（US 8071453B1）公开了一种半导体设备，并具体公开了（参见说明书第3栏第24行至第8栏第44行，附图1-10）存储晶体管108，其包含：沟道区116，其电气连接形成在衬底中的源区和漏区；氧化物-氮化物-氮化物-氧化物ONNO堆叠，其被布置在沟道区之上，且包括多层电荷俘获区，其包括富氧的第一氮化物层124A和被布置在第一氮化物层之上的第二氮化物层124B；以及栅电极142，其在ONNO堆叠的表面上形成，是高功函数栅电极，栅电极可以是掺杂的多晶硅层，由于其被掺杂，因而可以确定从栅电极中除去电了需要的最小能量被增加。权利要求1和对比文件1公开的内容相比区别技术特征在于：沟道包括多晶硅。基于区别技术特征，可以确定本申请实际要解决的技术问题是：如何设置沟道材料。然而对于本领域技术人员来说，多晶是本领域常规的沟道材料，其并不能产生任何预料不到的技术效果。由此可见在对比文件1的基础上结合公知常识得出权利要求1的技术方案，对本领域的技术人员来说是显而易见的。因此，权利要求1不具有突出的实质性特点和显著的进步，不具备专利法第22条第3款规定的创造性。

2、权利要求2、3不具备专利法第22条第3款规定的创造性：

权利要求2、3是权利要求1的从属权利要求，其对沟道的材料进行进一步限定。然而对于本领域技术人员来说，硅纳米线以及再结晶的多晶硅都是本领域常规的沟道材料，其并不能产生任何预料不到的技术效果。因此，在其引用的权利要求不具备创造性的前提下，权利要求2、3也不具有专利法第22条第3款规定的创造性。

3、权利要求4不具备专利法第22条第3款规定的创造性：

权利要求4是权利要求3的从属权利要求。对比文件1还公开了（参见说明书第8栏第11-17行）栅电极包含多晶硅。对比文件1虽然并未公开栅电极的掺杂类型，但对于本领域技术人员来说，栅电极的掺杂类型是可以根据需要合理设置的，无需付出创造性劳动。因此，在其引用的权利要求不具备创造性的前提下，权利要求4也不具有专利法第22条第3款规定的创造性。

4、权利要求5不具备专利法第22条第3款规定的创造性：

权利要求5是权利要求4的从属权利要求。对比文件1还公开了（参见说明书第7栏第25-35行）ONNO堆叠还包括阻挡电介质层134，其被布置在多层电荷俘获层上，且其包括电介质。对比文件1虽然并未公开其是高K高温氧化物，但对于本领域技术人员来说，高K高温氧化物是本领域常规的阻挡电介质层材料，其并不能产生任何预料不到的技术效果。因此，在其引用的权利要求不具备创造性的前提下，权利要求5也不具有专利法第22条第3款规定的创造性。

5、权利要求6不具备专利法第22条第3款规定的创造性：

权利要求6是权利要求1的从属权利要求。对比文件1还公开了（参见附图1A-1D）还包括在衬底上形成的金属氧化物半导体MOS逻辑晶体管105、106、107，其包括栅氧化层和高功函数栅电极。可见权利要求的附加技术特征也已被对比文件1所公开。因此，在其引用的权利要求不具备创造性的前提下，权利要求6也不具有专利法第22条第3款规定的创造性。

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6、权利要求 7、8 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 7、8 是权利要求 6 的从属权利要求，其分别对栅极的掺杂类型和存储器以及 MOS 晶体管的类型进行进一步限定。对比文件 1 虽然并未具体描述 MOS 晶体管以及存储器的晶体管类型，但对于本领域技术人员来说，可以根据器件性能需要合理地设置栅极的掺杂类型以及晶体管的类型，无需付出创造性劳动。因此，在其引用的权利要求不具备创造性的前提下，权利要求 7、8 也不具有专利法第 22 条第 3 款规定的创造性。

7、权利要求 9 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 9 是权利要求 6 的从属权利要求。对比文件 1 还公开了（参见附图 9-10）存储器晶体管的高功函数栅电极和 MOS 逻辑晶体管的高功函数栅电极两者皆由单个图案化的掺杂多晶硅层形成。可见权利要求的附加技术特征也已被对比文件 1 所公开。因此，在其引用的权利要求不具备创造性的前提下，权利要求 9 也不具有专利法第 22 条第 3 款规定的创造性。

8、权利要求 10 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 10 是权利要求 1 的从属权利要求。对比文件 1 还公开了（参见说明书第 5 栏第 58-67 行，附图 3C）多层电荷俘获层还包括中间氧化物层 124C'（即反隧穿层），其将第一氮化物层 124A' 和第二氮化物层 124B' 分开。可见权利要求的附加技术特征也已被对比文件 1 所公开。因此，在其引用的权利要求不具备创造性的前提下，权利要求 10 也不具有专利法第 22 条第 3 款规定的创造性。

9、权利要求 11 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 11 要求保护一种半导体设备，对比文件 1（US 8071453B1）公开了一种半导体设备，并具体公开了（参见说明书第 3 栏第 24 行至第 8 栏第 44 行，附图 1-10）存储晶体管 108，其包含：沟道区 116，其电气连接形成在衬底中的源区和漏区；氧化物-氮化物-氮化物-氧化物 ONNO 堆叠，其被布置在沟道区之上，隧穿电介质层 122，其布置在沟道区上；多层电荷俘获区，被布置在隧穿电介质层 122 上其包括富氧的第一氮化物层 124A' 和被布置在第一氮化物层之上的第二氮化物层 124B'，以及中间氧化物层 124C'（即反隧穿层）；中间氧化物层 124C' 将第一氮化物层和第二氮化物层分开；阻挡电介质层 134，其被布置在多层电荷俘获层之上；栅电极 142，其在 ONNO 堆叠的表面上形成，是高功函数栅电极，栅电极可以是掺杂的多晶硅层，由于其被掺杂，因而可以确定从栅电极中除去电子需要的最小能量被增加。权利要求 11 和对比文件 1 公开的内容相比区别技术特征在于：沟道包括多晶硅。基于区别技术特征，可以确定本申请实际要解决的技术问题是：如何设置沟道材料以及栅电极功函数。然而对于本领域技术人员来说，多晶是本领域常规的沟道材料，其并不能产生任何预料不到的技术效果。由此可见在对比文件 1 的基础上结合公知常识得出权利要求 11 的技术方案，对本领域的技术人员来说是显而易见的。因此，权利要求 11 不具有突出的实质性特点和显著的进步，不具备专利法第 22 条第 3 款规定的创造性。

10、权利要求 12 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 12 是权利要求 1 的从属权利要求，其对沟道的材料进行进一步限定。然而对于本领域技术人员来说，再结晶的多晶硅是本领域常规的沟道材料，其并不能产生任何预料不到的技术效果。因此，在其引用的权利要求不具备创造性的前提下，权利要求 12 也不具有专利法第 22 条第 3 款规定的创造性。

11、权利要求 13 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 13 是权利要求 12 的从属权利要求。对比文件 1 还公开了（参见说明书第 8 栏第 11-17 行）栅电极包含多晶硅。对比文件 1 虽然并未公开栅电极的掺杂类型，但对于本领域技术人员来说，栅电极的掺杂类型是可以根据需要合理设置的，无需付出创造性劳动。因此，在其引用的权利要求不具备创造性的前提下，

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权利要求 13 也不具有专利法第 22 条第 3 款规定的创造性。

12、权利要求 14 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 14 是权利要求 13 的从属权利要求。对比文件 1 虽然并未公开阻挡电介质层 134 是高 K 高温氧化物，但对于本领域技术人员来说，高 K 高温氧化物是本领域常规的阻挡电介质层材料，其并不能产生任何预料不到的技术效果。因此，在其引用的权利要求不具备创造性的前提下，权利要求 14 也不具有专利法第 22 条第 3 款规定的创造性。

13、权利要求 15 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 15 是权利要求 1 的从属权利要求，其对沟道的材料进行进一步限定。然而对于本领域技术人员来说，硅纳米线是本领域常规的沟道材料，其并不能产生任何预料不到的技术效果。因此，在其引用的权利要求不具备创造性的前提下，权利要求 15 也不具有专利法第 22 条第 3 款规定的创造性。

14、权利要求 16 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 16 是权利要求 11 的从属权利要求。对比文件 1 还公开了（参见说明书第 8 栏第 11-17 行）栅电极包含多晶硅。对比文件 1 虽然并未公开栅电极的掺杂类型，但对于本领域技术人员来说，栅电极的掺杂类型是可以根据需要合理设置的，无需付出创造性劳动。因此，在其引用的权利要求不具备创造性的前提下，权利要求 16 也不具有专利法第 22 条第 3 款规定的创造性。

15、权利要求 17 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 17 是权利要求 11 的从属权利要求。对比文件 1 还公开了（参见附图 1A-1D）还包括在衬底上形成的金属氧化物半导体 MOS 逻辑晶体管 105、106、107，其包括栅氧化层和高功函数栅电极。可见权利要求的附加技术特征也已被对比文件 1 所公开。因此，在其引用的权利要求不具备创造性的前提下，权利要求 17 也不具有专利法第 22 条第 3 款规定的创造性。

16、权利要求 18 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 18 要求保护一种半导体设备，对比文件 1（US 8071453B1）公开了一种半导体设备，并具体公开了（参见说明书第 3 栏第 24 行至第 8 栏第 44 行，附图 1-10）存储晶体管 108，其包含：沟道区 116，其电气连接形成在衬底中的源区和漏区；氧化物-氮化物-氮化物-氧化物 ONNO 堆叠，其被布置在沟道区之上，隧穿电介质层 122，其布置在沟道区上；多层电荷俘获区，被布置在隧穿电介质层 122 上其包括富氧的第一氮化物层 124A’和被布置在第一氮化物层之上的第二氮化物层 124B’；阻挡电介质层 134，其被布置在多层电荷俘获层之上；栅电极 142，其在 ONNO 堆叠的表面上形成，是高功函数栅电极，栅电极可以是掺杂的多晶硅层，由于其被掺杂，因而可以确定从栅电极中除去电子需要的最小能量被增加。权利要求 18 和对比文件 1 公开的内容相比区别技术特征在于：沟道是垂直沟道，包括多晶硅，且从在衬底的表面上形成的第一扩散区延伸到在衬底表面形成的第二扩散区，垂直沟道电气连接第一扩散区和第二扩散区。基于区别技术特征，可以确定本申请实际要解决的技术问题是：如何设置沟道方向以进一步提高集成度。对比文件 2（US 2002/0109138A1）公开了一种存储器结构，并具体公开了（参见说明书第 26-51 段，附图 2-6F）存储器晶体管包括垂直沟道 212，且从在衬底的表面上形成的第一扩散区 204 延伸到在衬底表面形成的第二扩散区 206，垂直沟道电气连接第一扩散区和第二扩散区；垂直沟道包括多晶（参见说明书第 40-42 段，沟道为再结晶的多晶硅）栅介质电荷捕获层 220，被布置在垂直沟道的周围。该特征在对比文件 2 中所起的作用与其在该申请中为解决其技术问题所起的作用相同，都是通过形成垂直沟道的存储器以进一步提高集成度。由此可见在对比文件 1 的基础上结合对比文件 2 得出权利要求 18 的技术方案，对本领域的技术人员来说是显而易见的。因此，权利要求 18 不具有突出的实质性特点和显著的进步，不具备专利法第 22 条第 3 款规定的创造性。

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17、权利要求 19 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 19 是权利要求 18 的从属权利要求。对比文件 1 还公开了（参见附图 1A-1D）还包括在衬底上形成的金属氧化物半导体 MOS 逻辑晶体管 105、106、107，其包括栅氧化层和高功函数栅电极。可见权利要求的附加技术特征也已被对比文件 1 所公开。因此，在其引用的权利要求不具备创造性的前提下，权利要求 19 也不具有专利法第 22 条第 3 款规定的创造性。

18、权利要求 20 不具备专利法第 22 条第 3 款规定的创造性：

权利要求 20 是权利要求 18 的从属权利要求。对比文件 1 还公开了（参见说明书第 5 栏第 58-67 行，附图 3C）多层电荷俘获层还包括中间氧化物层 124C'（即反隧穿层），其将第一氮化物层 124A'和第二氮化物层 124B'分开。可见权利要求的附加技术特征也已被对比文件 1 所公开。因此，在其引用的权利要求不具备创造性的前提下，权利要求 20 也不具有专利法第 22 条第 3 款规定的创造性。

关于申请人的意见陈述：

申请人在意见陈述中指出：尽管对比文件 1（US8071453B1）也提到了高功函数栅电极，但是其仅仅公开了由金属氮化物、金属碳化物和金属硅化物组成的高功函数栅电极的更普遍的使用方法，该高功函数栅电极包含高功函数金属如铪、锆、钛、钽、铝、钌、钯、铂、钴和镍。对比文件 1 没有教导或提示“高功函数栅电极，所述高功函数栅电极在所述 ONNO 堆叠的表面上形成，其中所述高功函数栅电极包括掺杂的多晶硅层”，更别说公开该掺杂的多晶硅层“被掺杂以使得从栅电极中除去电子需要的最小能量被增加”。

然而事实上，对比文件 1（US8071453B1）在说明书第 8 栏第 11-18 行明确公开了该高功函数栅电极可以是掺杂的多晶硅，对于 N 型掺杂的多晶硅来说，显然从其中除去电子需要的能量需要被增加。因此，申请人的意见陈述不具有说服力。

基于上述理由，该申请的独立权利要求以及从属权利要求都不具备创造性，同时说明书中也没有记载其他任何可以授予专利权的实质性内容，因而即使申请人对权利要求进行重新组合或根据说明书记载的内容作进一步的限定，该申请也不具备被授予专利权的前景。如果申请人不能在本通知书规定的答复期限内提出表明该申请具有创造性的充分理由，该申请将被驳回。

审查员姓名：孙鹏　　审查员代码：883272

纸件申请，回函请寄：100088 北京市海淀区蓟门桥西土城路 6 号　国家知识产权局专利局受理处收
电子申请，应当通过电子专利申请系统以电子文件形式提交相关文件。除另有规定外，以纸件等其他形式提交的文件视为未提交。

Sandisk Technologies, Inc. - Ex. 1002, Page 001890

Electronic Patent Application Fee Transmittal

Application Number:	15335180
Filing Date:	26-Oct-2016
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Attorney Docket Number:	PM07027D1CIP1C3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	31096080
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	30-NOV-2017
Filing Date:	26-OCT-2016
Time Stamp:	17:59:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$180
RAM confirmation Number	120117INTEFSW00005900503781
Deposit Account	503781
Authorized User	Timothy Croll
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C3_IDS_US_11282017.pdf	1054076 1423afe82723f461d666a34cdf287fbaf698f503	no	4
Warnings:					
Information:					
2	Non Patent Literature	PM07002C2_NonFinalRejection_10062017.pdf	398066 0f604295aa8dc33dcbd7ca35bd7f2a666d47fb9f	no	11
Warnings:					
Information:					
3	Non Patent Literature	PM07002CIP2C1_NonFinalRejection_09222017.pdf	340285 f3ddf23921519e086788e9af8c0484a0dce7c341	no	11
Warnings:					
Information:					
4	Non Patent Literature	PM07024CIP1C1_NOA_10182017.pdf	440965 3562a5675ebd8778f09b34f381e1e7427fbc150a	no	8
Warnings:					
Information:					
5	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1C3_IDS_For_11282017.pdf	1053872 92b0e96005cc51ade7066ca830d88aee978270cc	no	4
Warnings:					
Information:					

A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.

6	Miscellaneous Incoming Letter	PM07027D1CIP1C3_ConciseExplanationUnderRule1_11282017.pdf	32610 f2f4749a0930ea5680af9404ba50e37b0d5c13f8	no	1
Warnings:					
Information:					
7	Non Patent Literature	PM07002CIP1CN_SIPOOA_09202017.pdf	3291890 5d48d0a7beba6fcdeb0de538cb0092be8ac5b90f	no	6
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Information:					
8	Non Patent Literature	PM07027D1CIP1CN_SIPOOA_09252017.pdf	457901 2e44b27ab041bbda815d6f775afcce1f57ed60cc	no	6
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	30638 785a01da49ee4bca8401745a89643239a57e71f2	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	7100303		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PRINTER RUSH
(PTO ASSISTANCE)

Application: 15335180	Examiner: Yushin	GAU: 2893
From: Chuck Bowen	Location: RTFM	Creation Date: 12/15/2017

Week Date: 10/2/2017

DOC CODE	DOC DATE	MISCELLANEOUS
[ ] 1449		[ ] Continuing Data
[X] IDS	11/30/2017	[ ] Foreign Priority
[ ] CLM		[ ] Document Legibility
[ ] IIFW/FWCLM		[ ] Fees
[ ] SRFW		[ ] Petition (TC)
[ ] DRW		[ ] Other
[ ] OATH		
[ ] 312		
[ ] SPEC		

[RUSH] Message:

Please respond to the IDS's dated 11/30/17.

Thank you.

CB

[XRUSH] Response:

Initials: _____

Examiner: PUBS contact - James Leija, (703) 756-1197
NOTE: This form will be included as part of the official USPTO record with the response document coded as XRUSH.
REV: AUG 16

Sandisk Technologies, Inc. - Ex. 1002, Page 001896

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Group Art Unit: 2893
Igor Polishchuk, et al.	) Examiner: YUSHIN, NIKOLAY K
Application No.: 15/335,180	) Confirmation No.: 6223
Filed: 10-26-2016	)
For: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	)

AMENDMENT UNDER 37 C.F.R. § 1.312
&
RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant is in receipt of a Notice of Allowance and Fee Due Form, mailed October 04, 2017, and a Notice to File Corrected Application Papers ("NOTICE"), mailed November 03, 2017, in connection with the above-identified application. In response to the NOTICE, applicant hereby submits replacement sheets for FIG. 4A and FIG. 4B. Also in response to the NOTICE and pursuant to 37 C.F.R. § 1.312, the Examiner is respectfully requested to favorably consider and enter the following amendments to the present application.

Customer No.: 60909

Amendments to the Specification

Please replace paragraph [00106], under Detailed Description, with the following:

[00106] The memory transistor 800 of FIG. 8A can be made using either a gate first or a gate last scheme. FIGs. 9A-F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 8A. FIGs. ~~20A-F~~10A-F illustrate a gate last scheme for fabricating the non-planar mulitgate device of FIG. 8A.

Abstract

Please replace the Abstract with the following:

An example memory device includes a channel positioned between and electrically connecting a first diffusion region and a second diffusion region, and a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel. The multi-layer charge trapping layer includes a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers. The anti-tunneling layer includes an oxide layer. The first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.

Drawing

The Applicant submits herein REPLACEMENT SHEETS 5/13 and 6/13, featuring FIG. 4A and FIG. 4B, respectively. The Applicant respectfully submits that the replacement drawing sheets contain no new matter.

Sandisk Technologies, Inc. - Ex. 1002, Page 001898

Remarks

Please amend the Application as indicated in the Amendments to the Specification section.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.19, 1.20 and 1.21 that may be required to issue the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's agent, Kin Hung Lai, by telephone at (408) 545-6950. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

Date: 12/18/2017

By: /Kin Hung Lai/
Kin Hung Lai
Agent for Applicant
Registration No. 69,251

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134

Customer No.: 60909

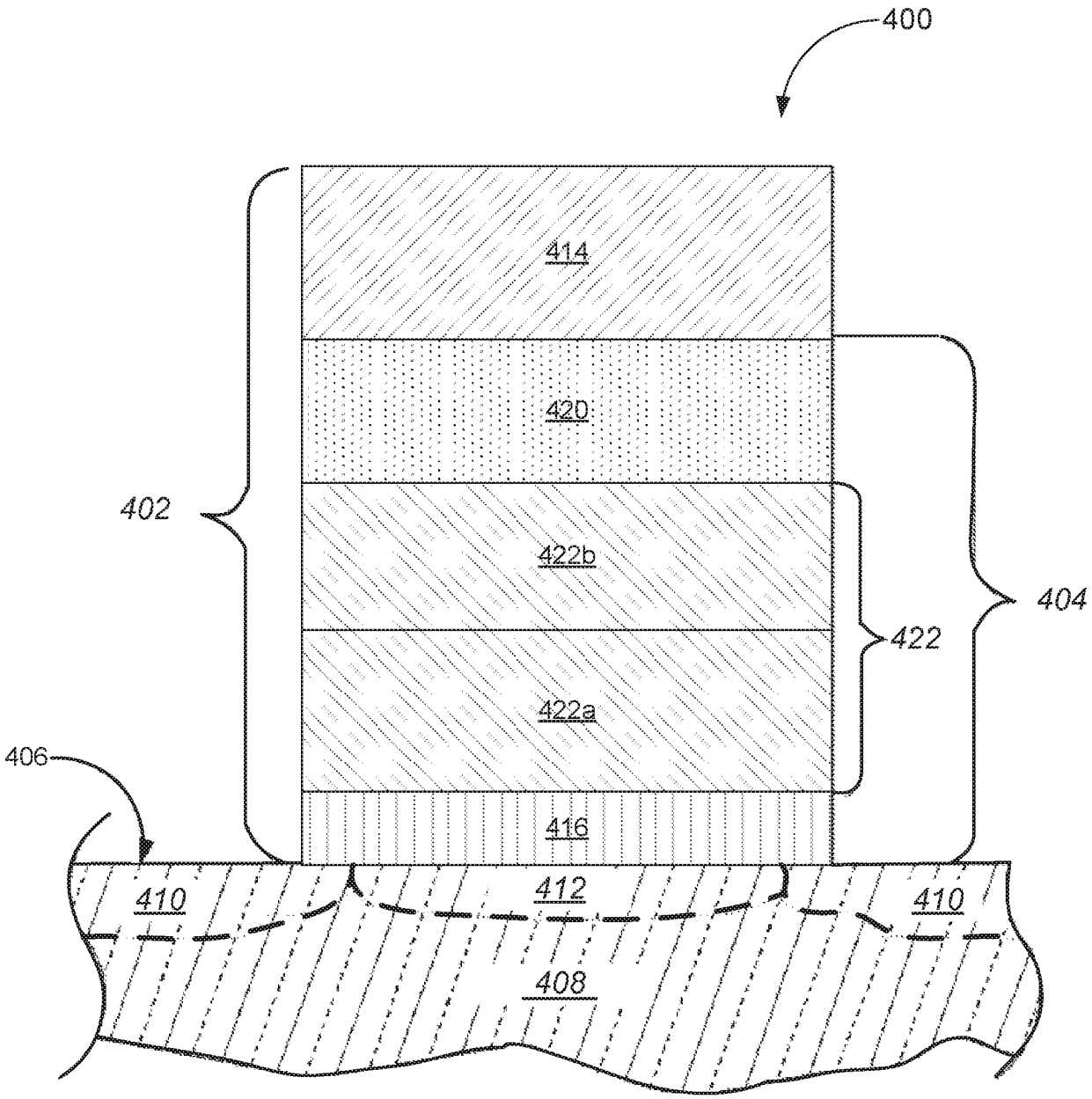


FIG. 4A

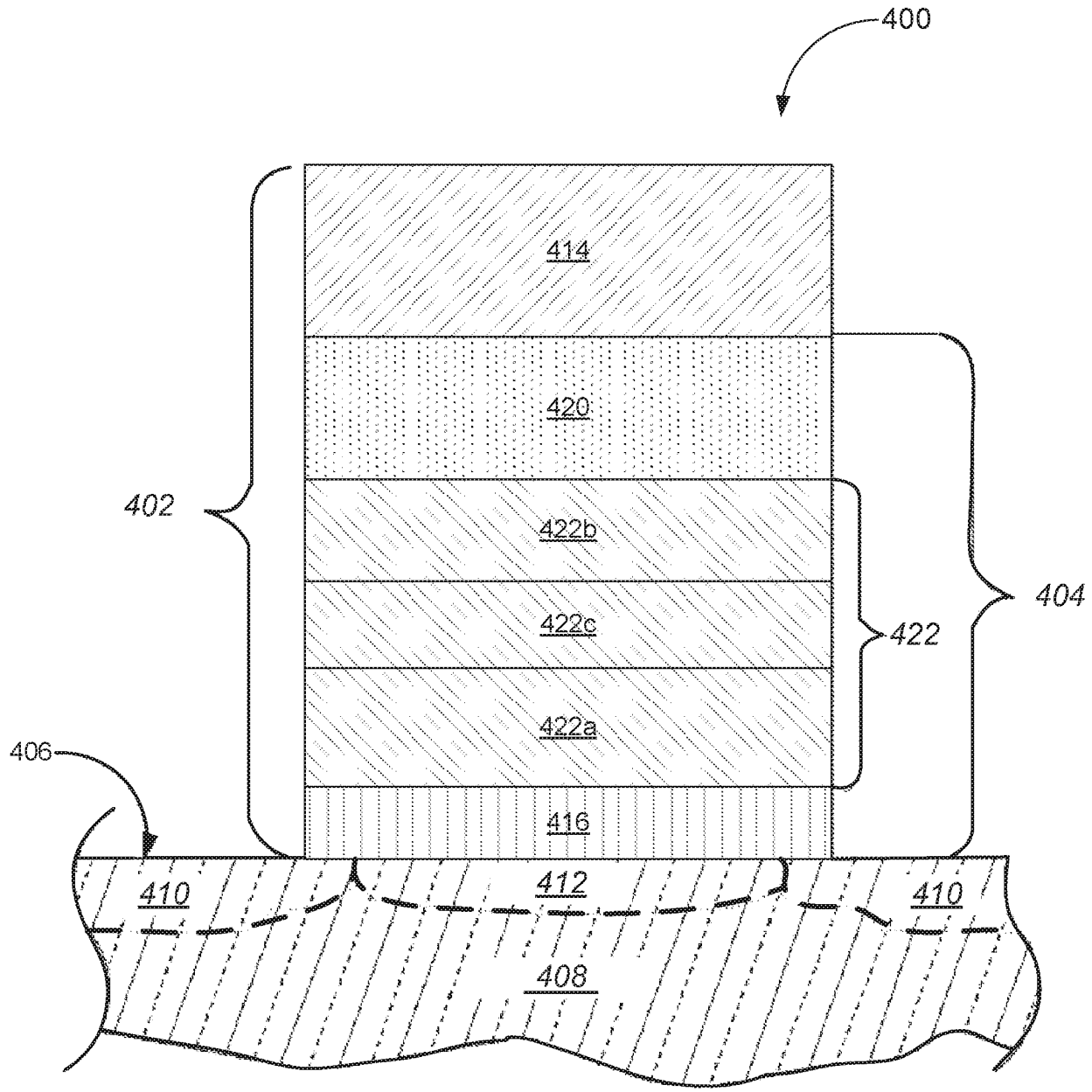


FIG. 4B

Electronic Patent Application Fee Transmittal

Application Number:	15335180
Filing Date:	26-Oct-2016
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Attorney Docket Number:	PM07027D1CIP1C3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	31256512
Application Number:	15335180
International Application Number:	
Confirmation Number:	6223
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1C3
Receipt Date:	18-DEC-2017
Filing Date:	26-OCT-2016
Time Stamp:	14:11:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$960
RAM confirmation Number	121917INTEFSW00000480503781
Deposit Account	503781
Authorized User	Timothy Croll
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	PM07027D1CIP1C3_PartBFeeTransmittal_12142017.pdf	809777 2992d671b94f0ec0f338f793a7538a6cee66ebd5	no	1
Warnings:					
Information:					
2	Amendment after Notice of Allowance (Rule 312)	PM07027D1CIP1C3_312Amendment_11282017_Final.pdf	71485 33ccc953a1465e3cf3d1b64e4fb27f163ea14826	no	3
Warnings:					
Information:					
3	Drawings-only black and white line drawings	PM07027D1CIP1C3_ReplacementDrawing4Aand4B_12182017.pdf	138853 beb3792f384f9c3ec142c35be75b16d86e13e180	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30645 a553f45b71e5616e7c4cbe83ed8472b3c240f360	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1050760		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 10/04/2017
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/335,180	10/26/2016	Igor Polishchuk	PM07027D1CIP1C3	6223

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/04/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-326000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Cypress Semiconductor Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): San Jose, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 503781 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Christopher Jordan/ Date 12/14/2017

Typed or printed name Christopher Jordan Registration No. 65809

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Application: 15335180	Examiner: Yushin	GAU: 2893
From: Chuck Bowen	Location: RTFM	Creation Date: 12/15/2017

Week Date: 10/2/2017

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