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(54) CHARGE TRAPPING DIELECTRIC STRUCTURE FOR NON-VOLATILE MEMORY

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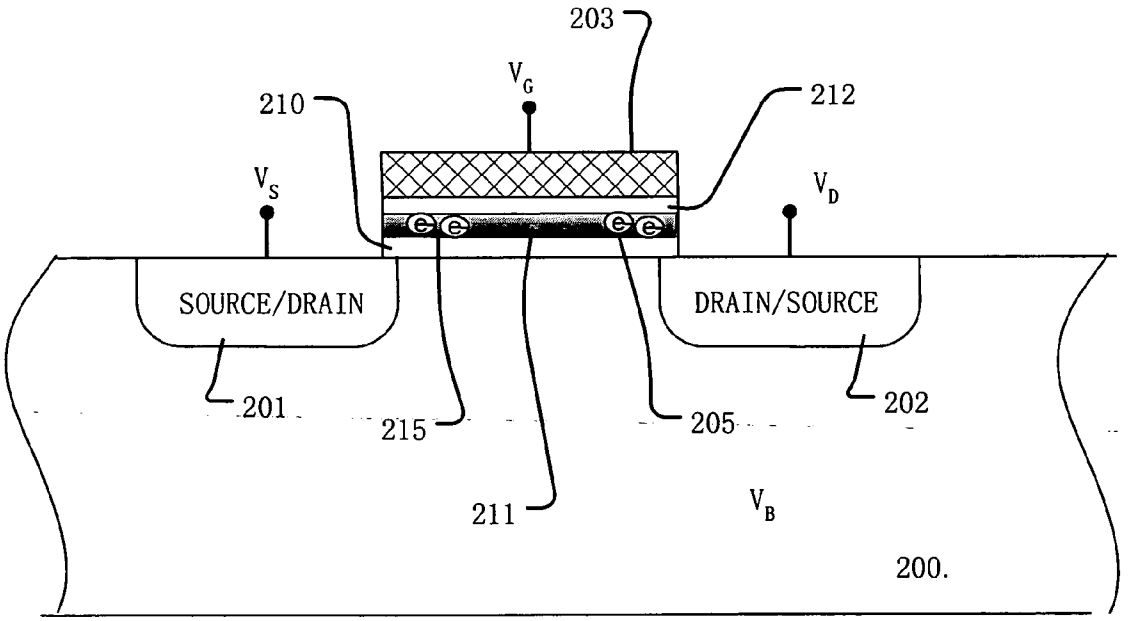
(57) **ABSTRACT**

An integrated circuit structure comprises a bottom dielectric layer on a substrate, a middle dielectric layer, and a top dielectric layer. The middle dielectric layer has a top surface and a bottom surface, and comprises a plurality of materials. Respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces are non-uniform and arranged to induce a variation in energy gap between the top and bottom surfaces. The variation in energy gap establishes an electric field between the top and bottom surfaces tending to oppose charge motion toward at least one of the top and bottom surfaces and prevent resultant charge leakage.



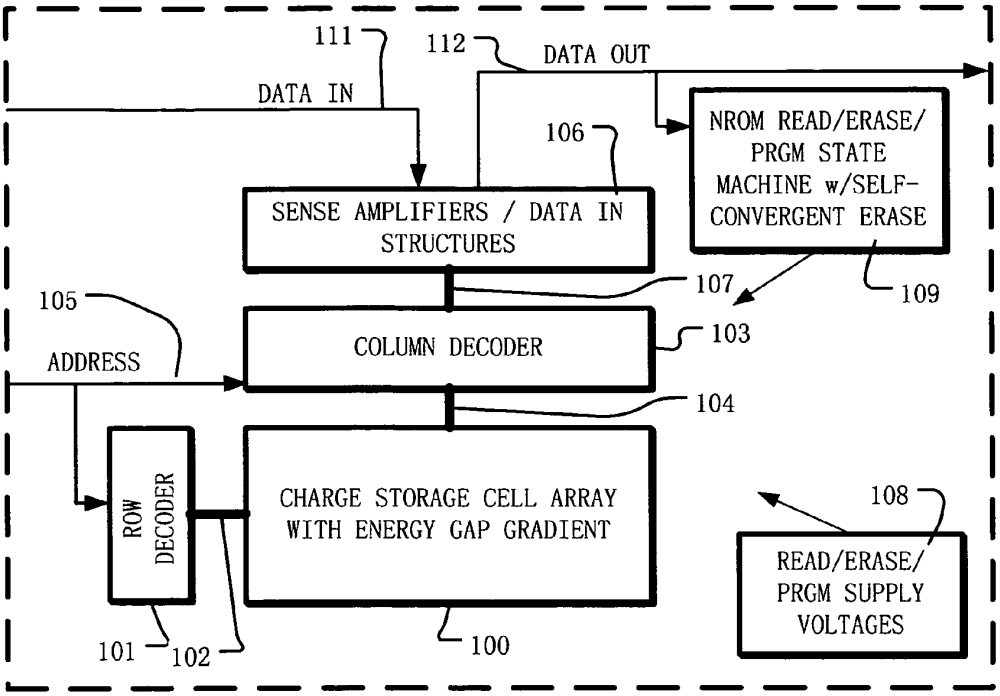

111
112
DATA OUT
DATA IN
106
NROM READ/ERASE/ PRGM STATE MACHINE w/SELF-CONVERGENT ERASE
SENSE AMPLIFIERS / DATA IN STRUCTURES
107
109
105
COLUMN DECODER
103
ADDRESS
104
ROW DECODER
CHARGE STORAGE CELL ARRAY WITH ENERGY GAP GRADIENT
108
READ/ERASE/ PRGM SUPPLY VOLTAGES
101
102
100

FIG-1

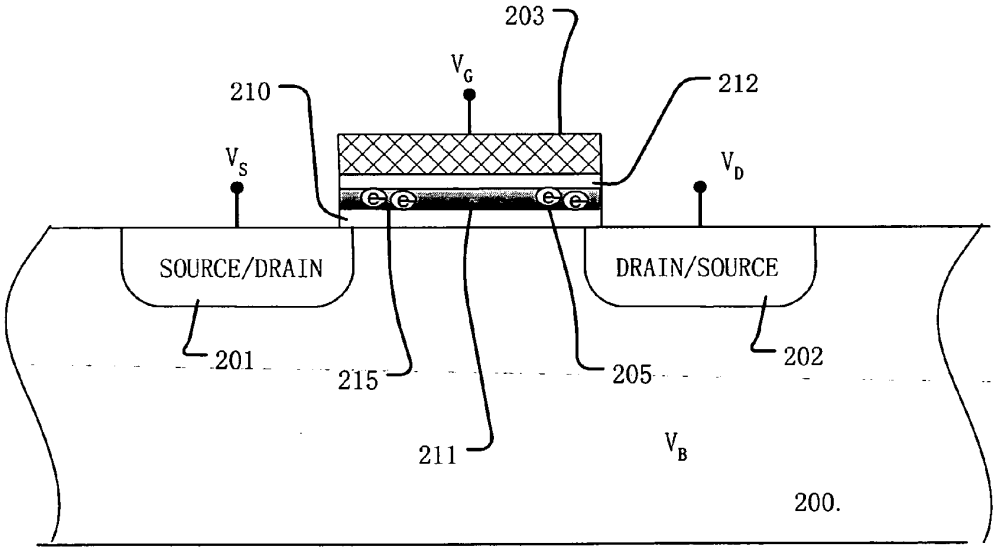

203
V_G
210
212
V_S
V_D
SOURCE/DRAIN
DRAIN/SOURCE
201
215
205
202
211
V_B
200.

FIG-2

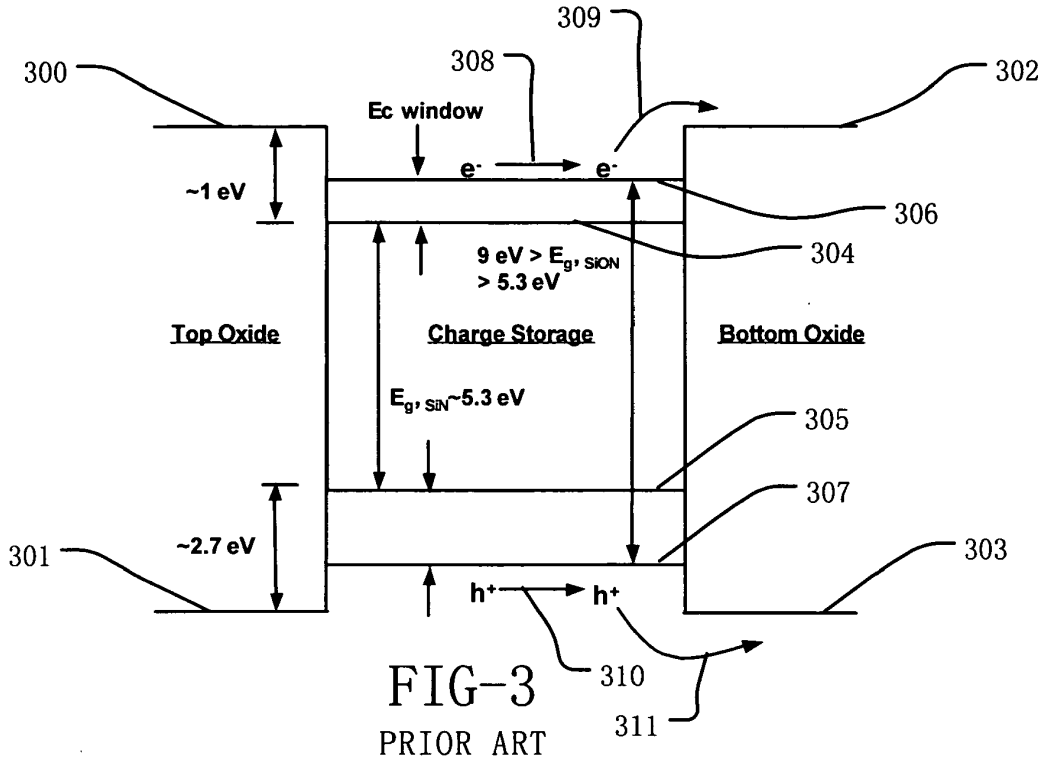


FIG-3
PRIOR ART

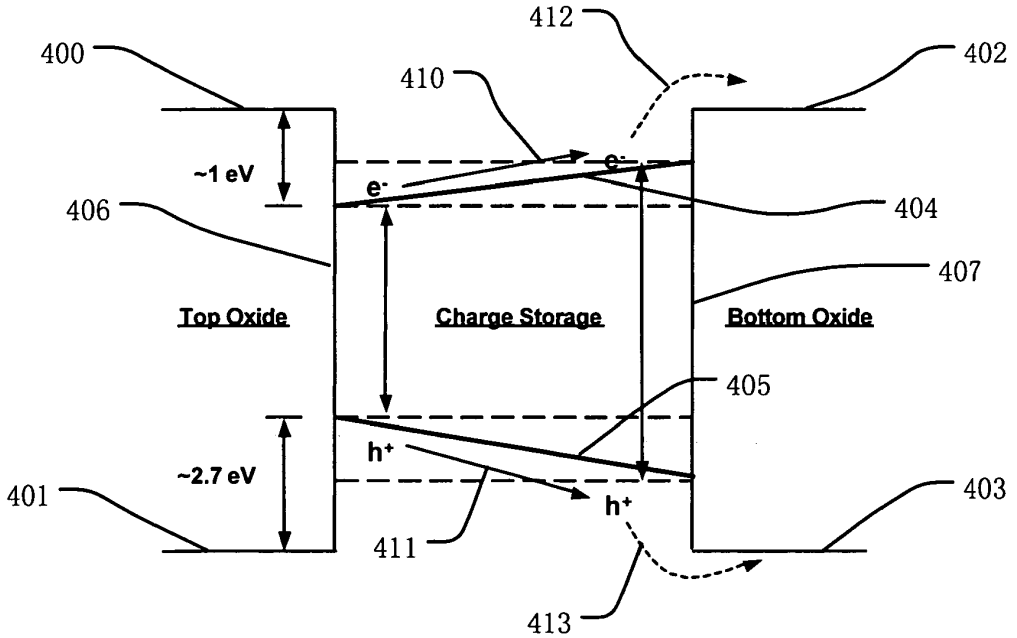


FIG-4

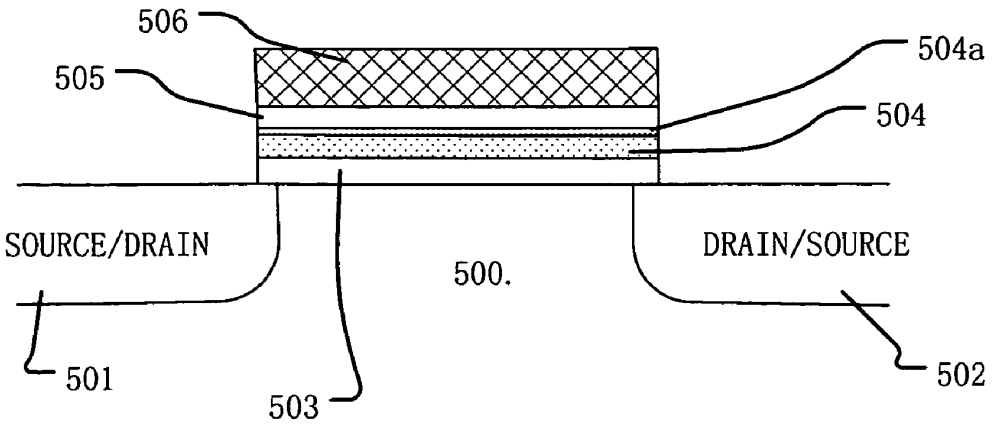

506
505
504a
504
SOURCE/DRAIN
500.
DRAIN/SOURCE
501
503
502

FIG-5

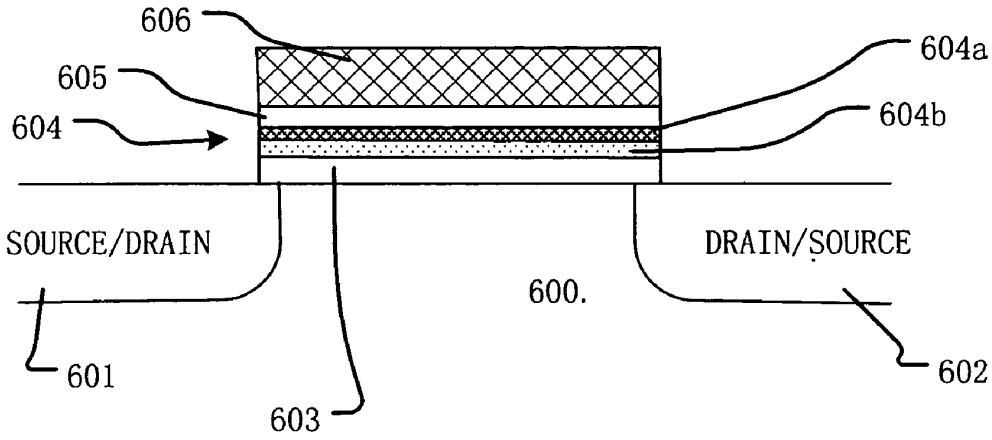

606
605
604
604a
604b
SOURCE/DRAIN
600.
DRAIN/SOURCE
601
603
602

FIG-6

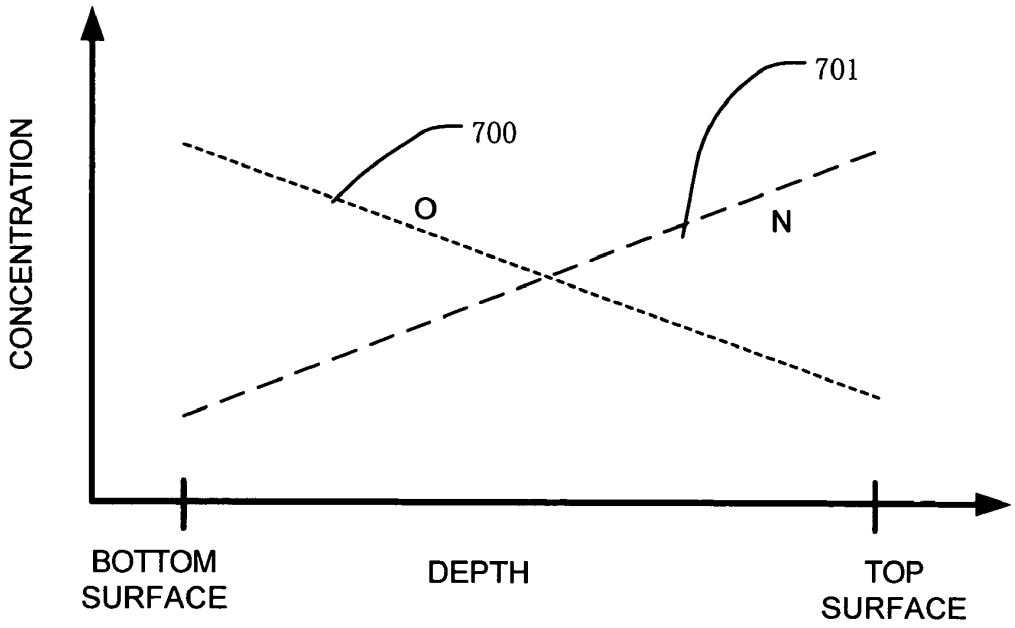

CONCENTRATION
700
701
O
N
BOTTOM SURFACE
DEPTH
TOP SURFACE

FIG-7

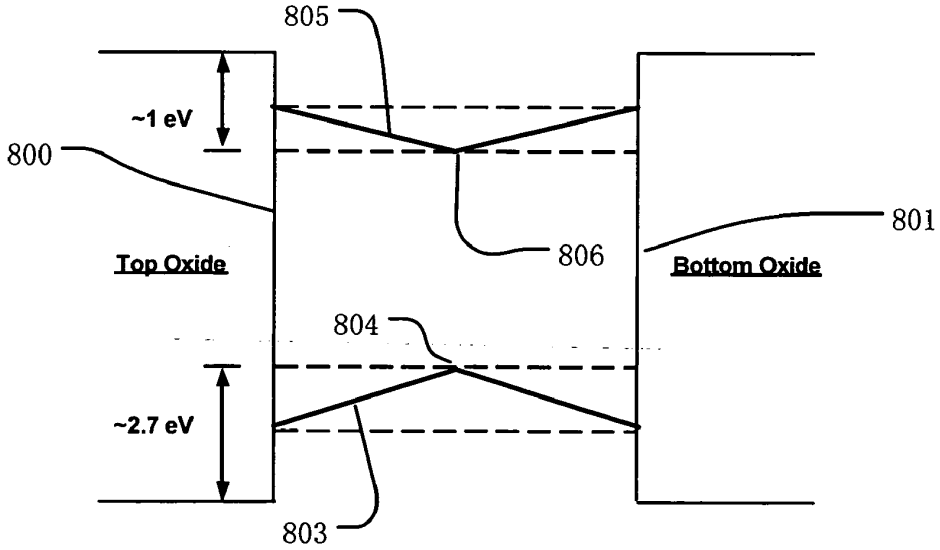

805
~1 eV
800
801
806
Top Oxide
Bottom Oxide
804
~2.7 eV
803

FIG-8

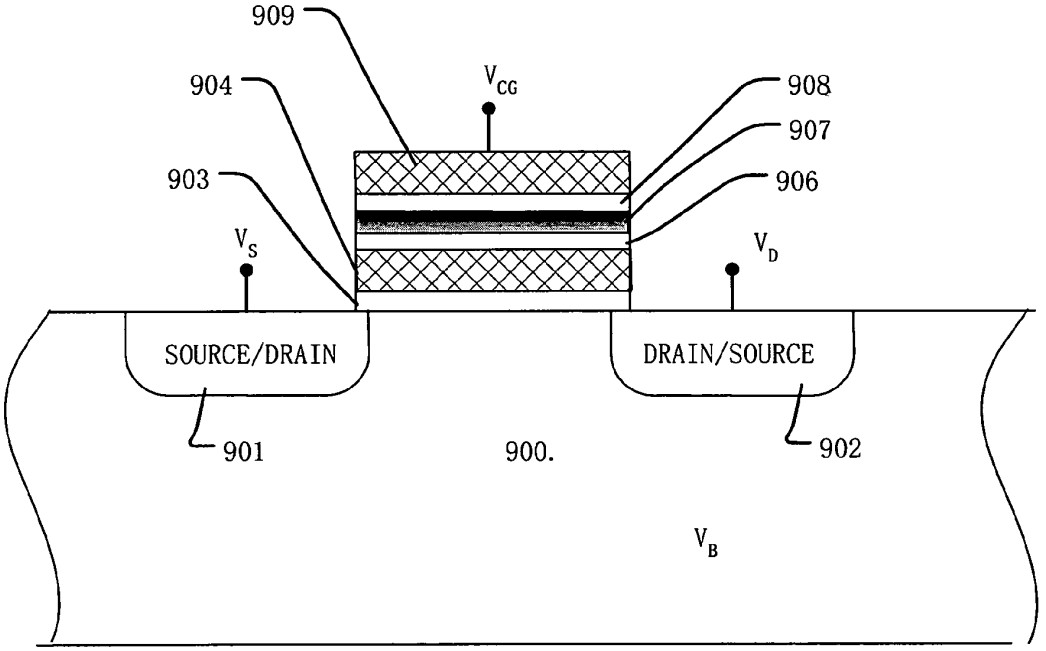

909
904
V_{CG}
908
907
903
906
V_S
V_D
SOURCE/DRAIN
DRAIN/SOURCE
901
900.
902
V_B

FIG-9

CHARGE TRAPPING DIELECTRIC STRUCTURE FOR NON-VOLATILE MEMORY

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to charge trapping dielectric structures and to non-volatile memory based on such structures.

[0003] 2. Description of Related Art

[0004] Electrically programmable and erasable non-volatile memory technologies based on charge storage structures known as EEPROM and flash memory are used in a variety of modern applications. A number of memory cell structures are used for EEPROM and flash memory. As the dimensions of integrated circuits shrink, greater interest is arising for memory cell structures based on charge trapping dielectric layers, because of the scalability and simplicity of the manufacturing processes. Memory cell structures based on charge trapping dielectric layers include structures known by the industry names NROM, SONOS, and PHINES, for example. These memory cell structures store data by trapping charge in a charge trapping dielectric layer, such as silicon nitride. As negative charge is trapped, the threshold voltage of the memory cell increases. The threshold voltage of the memory cell is reduced by removing negative charge from the charge trapping layer.

[0005] One problem associated with charge trapping structures used in non-volatile memory is data retention. For commercial products it is desirable for such devices to hold data for at least ten years without loss. However, leakage of trapped charge occurs in such devices due to defects in the materials which accumulate over long use, or which are inherent in the structures.

[0006] It is desirable to provide charge trapping structures for non-volatile memory with improved charge retention characteristics.

SUMMARY OF THE INVENTION

[0007] The present invention provides an integrated circuit structure and a method for manufacturing an integrated circuit structure that comprises a bottom dielectric layer on a substrate, a middle dielectric layer, and a top dielectric layer. The middle dielectric layer has a top surface and a bottom surface, and comprises a plurality of materials. Respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces are non-uniform and arranged to induce a variation in energy gap between the top and bottom surfaces. The variation in energy gap establishes an electric field between the top and bottom surfaces tending to oppose charge motion toward at least one of the top and bottom surfaces and prevent resultant charge leakage. In embodiments of the structure, the bottom dielectric layer and the top dielectric layer are characterized by respective energy gaps at the interfaces with the top and bottom surfaces of the middle dielectric layer that are greater than a maximum energy gap in the middle dielectric layer, and in some embodiments greater than the energy gap levels in the middle dielectric layer at such interfaces. Various embodiments of the integrated circuit structure provide for a variation in energy gap which includes a minimum energy gap spaced away from the top and bottom surfaces, such as in a central region of the middle dielectric layer, and maximum energy gaps near to both of the top and bottom surfaces. Other embodiments provide for variation in energy gap which includes a minimum energy gap near the top surface of the middle dielectric layer and a maximum energy gap near the bottom surface, or vice versa. In some embodiments, the variation in energy gap is substantially monotonically increasing from one to the other of the top and bottom surfaces.

[0008] The integrated circuit structure is used for example in non-volatile charge storage flash memory devices, where the middle dielectric layer acts as the charge storage layer. In yet other embodiments, an integrated circuit structure is used as an interpoly dielectric layer in a floating gate memory cell. Thus, embodiments of the technology described include unique memory cells incorporating the top, middle and bottom dielectric layers described above.

[0009] Materials suitable for the middle dielectric layer include a combination of silicon, oxygen and nitrogen, like silicon oxynitride SiO_xN_y, where x and y are variable. The materials are arranged for example so that the concentration in a first half of the middle dielectric layer near the top dielectric layer of material tending to decrease the energy gap (like nitrogen in a silicon oxynitride) is greater than the concentration of such material in a second half of the middle dielectric layer near the bottom dielectric layer, and so that the material tending to increase the energy gap (like oxygen in a silicon oxynitride) has a concentration that is lower in the first half of the middle dielectric layer near the top dielectric layer, and higher in a second half of the middle dielectric layer near the bottom dielectric layer. For example, for an embodiment comprising a combination of silicon, oxygen and nitrogen, the concentration of oxygen decreases from the bottom surface of the middle dielectric layer to the top surface of the middle dielectric layer, and the concentration of nitrogen increases from the bottom surface of the middle dielectric layer to the top surface. This structure opposes charge movement toward the bottom surface of the middle dielectric layer. In yet another embodiment, the materials are arranged so that the maximum energy gap is near the top surface of the middle dielectric layer and the minimum energy gap is near the bottom surface, to oppose charge movement towards the top surface. The materials can also be arranged to oppose charge movement towards both the top and bottom surfaces, by establishing a minimum energy gap in a central region of the middle dielectric layer, with maximums near both the top and bottom surfaces.

[0010] Methods for manufacturing a middle dielectric layer for the structures described herein include depositing a sequence of thin films having varying concentrations of materials and/or varying combinations of materials using techniques like atomic layer deposition, chemical vapor deposition, and so on. In embodiments where the middle dielectric layer comprises silicon oxynitride, a method for manufacturing includes formation of a first film of silicon oxynitride with a nominal concentration of silicon, oxygen and nitrogen, followed by exposing the first film to nitrogen in a manner that causes incorporation of nitrogen into the structure near the top surface of the middle dielectric layer. The resulting structure can be annealed to smooth out the concentration profiles. In another embodiment, where the middle dielectric layer comprises silicon oxynitride, a

method for manufacturing includes forming a first film of silicon oxynitride on the bottom dielectric, and forming a film of silicon nitride on the first film, followed by annealing the first and second films to smooth out the transition between the silicon oxynitride and the silicon nitride.

[0011] Other aspects and advantages of the present invention can be seen on review of the drawings, the detailed description and the claims, which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] **FIG. 1** is a simplified diagram of an integrated circuit including a charge storage memory cell array, where the memory cells have a dielectric layer with an energy gap gradient to oppose charge leakage.

[0013] **FIG. 2** is a simplified diagram of a charge trapping memory cell including a dielectric layer with an energy gap gradient to oppose charge leakage.

[0014] **FIG. 3** is a simplified energy gap diagram for a prior art charge trapping dielectric structure.

[0015] **FIG. 4** is a simplified energy gap diagram for a charge trapping dielectric structure, including a middle dielectric layer with an energy gap gradient to oppose charge leakage.

[0016] **FIG. 5** is a simplified illustration for the purposes of describing a method for manufacturing a charge trapping dielectric structure, including a middle dielectric layer with an energy gap gradient to oppose charge leakage.

[0017] **FIG. 6** is a simplified illustration for the purposes of describing another method for manufacturing a charge trapping dielectric structure, including a middle dielectric layer with an energy gap gradient to oppose charge leakage.

[0018] **FIG. 7** is a graph of concentration of materials from a bottom surface to a top surface of a middle dielectric layer in a charge trapping dielectric structure for a simplified embodiment.

[0019] **FIG. 8** is a simplified energy gap diagram for a charge trapping dielectric structure, including a middle dielectric -layer-with an-energy gap minimum in a central region, and energy gap maximums near both the top and bottom surfaces, to oppose charge leakage.

[0020] **FIG. 9** is a simplified diagram of a floating gate memory cell including a dielectric layer with an energy gap gradient to oppose charge leakage.

DETAILED DESCRIPTION

[0021] A detailed description of embodiments of the present invention is provided with reference to the **FIGS. 1-9**.

[0022] **FIG. 1** is a simplified block diagram of an integrated circuit including charge storage memory cells. The integrated circuit includes a memory array **100** implemented using charge trapping memory cells having a charge trapping dielectric structure with an energy gap gradient. An alternative includes a floating gate memory cell with an interpoly dielectric structure including a middle dielectric layer with an energy gap gradient. The energy gap gradient establishes a weak electric field at equilibrium, opposing charge leakage, and improves charge retention and durability of the memory device. A page/row decoder **101** is coupled to a plurality of word lines **102** arranged along rows in the memory array **100**. A column decoder **103** is coupled to a plurality of bit lines **104** arranged along columns in the memory array **100**. Addresses are supplied on bus **105** to column decoder **103** and page/row decoder **101**. Sense amplifiers and data-in structures in block **106** are coupled to the column decoder **103** via data bus **107**. Data is supplied via the data-in line **111** from input/output ports on the integrated circuit to the data-in structures in block **106**. Data is supplied via the data-out line **112** from the sense amplifiers in block **106** to input/output ports on the integrated circuit.

[0023] Resources for controlling the reading, programming and erasing of memory cells in the array **100** are included on the chip. These resources include read/erase/program supply voltage sources represented by block **108**, and the state machine **109**, which are coupled to the array **100**, the decoders **101**, **103** and other circuitry on the integrated circuit, which participates in operation of the device.

[0024] The supply voltage sources (block **108**) are implemented in various embodiments using charge pumps, voltage regulators, voltage dividers and the like as known in the art, for supplying various voltage levels, including negative voltages, used in the read, erase and program operations.

[0025] The state machine **109** supports read, erase and program operations. The state machine **109** can be implemented using special-purpose logic circuitry as known in the art. In alternative embodiments, the controller comprises a general-purpose processor, which may be implemented on the same integrated circuit, which executes a computer program to control the operations of the device. In yet other embodiments, a combination of special-purpose logic circuitry and a general-purpose processor may be utilized for implementation of the state machine.

[0026] **FIG. 2** is a simplified diagram of a charge trapping memory cell having a charge trapping dielectric layer with an energy gap gradient suitable for use in an integrated circuit as shown in **FIG. 1**. The memory cell is implemented in a semiconductor substrate **200**. The cell includes a source/drain **201** and a drain/source **202** formed by respective diffusion regions, separated by a channel in the substrate **200**. A gate **203** overlies the channel. Channel lengths in representative embodiments can be 0.25 microns and less, as minimum feature sizes scale downward in integrated circuit manufacturing. A charge storage element comprising middle dielectric layer **211** is isolated by a bottom dielectric layer **210** comprising an insulator such as silicon dioxide or silicon oxynitride between a region in the substrate **200** including the channel of the memory cell, and the middle dielectric layer **211**, and by a top dielectric layer **212** between the gate **203** and the middle dielectric layer **211**. The top and bottom dielectric layers typically have a thickness in the range of 30 to above 120 Angstroms depending on the operating arrangement selected, although other dielectric dimensions are applied for some memory cell embodiments.

[0027] The middle dielectric layer **211** in this example comprises a combination of materials including silicon, nitrogen and oxygen which make up a silicon oxynitride structure in which the concentrations of nitrogen and oxygen

vary across the thickness of the element between the top and bottom dielectrics **210** and **212**. In other embodiments, other charge trapping compositions, such as Al_2O_3, HfO_x, ZrO_x, or other metal oxides can be used to form memory cells with variations in concentrations of materials which create an energy gap gradient. The charge trapping layer can be continuous across the length of the channel as shown, or can consist of multiple isolated pockets of charge trapping material. Negative charge symbolized by charge traps **205**, **215** is trapped in the charge trapping layer, in response to hot electron injection, Fowler-Nordheim tunneling, and/or direct tunneling in various program procedures.

[**0028**] Materials used for the dielectric layers **210**, **211** and **212** may be formed using standard thermal silicon dioxide growth processes, in situ steam generation ISSG processes, along with or followed by nitridation by exposure to NO or N_2O, by chemical vapor deposition CVD, by plasma enhanced chemical vapor deposition PECVD, by tetraethoxysilane TEOS CVD, by high-density plasma chemical vapor deposition HPCVD, and other processes. Also, the materials can be formed by applying sputtering, pulsed vapor deposition PVD, jet vapor deposition JVD, and atomic layer deposition ALD. For background information about various possible deposition technologies, see, Rossnagel, S. M.; et al.; "From PVD to CVD to ALD for interconnects and related applications," Interconnect Technology Conference, 2001. Proceedings of the IEEE 2001 International, 4-6 Jun. 2001 Page(s): 3-5; Jelinek, M.; et al.; "Hybrid PLD technique for nitrogen rich CN, layers," Lasers and Electro-Optics Europe, 2000, Conference Digest 2000, Conference on 10-15 Sept. 2000. Page 1; and Wang, X, W.; et al.; "Ultra-thin silicon nitride films on Si by jet vapor deposition," VLSI Technology, Systems, and Applications, 1995. Proceedings of Technical Papers., 1995 International Symposium on, 3 1 May-2 Jun. 1995, Page(s): 49-52.

[**0029**] **FIG. 3** is a simplified energy level diagram for an equilibrium state of a prior art charge storage structure which includes a top layer comprising silicon dioxide (top oxide) and a bottom layer comprising silicon dioxide (bottom oxide). The charge storage layer in the illustrated example is silicon nitride or silicon oxynitride having an essentially uniform composition across the width of the layer. Thus, the conduction band **300** and the valence band **301** for the top oxide are separated by about 9 eV. Likewise, the conduction band **302** and the valence band **303** for the bottom oxide are separated by about 9 eV. The charge storage layer is designed so that its energy gap between the valence and conduction bands is less than that for the top oxide, and so that its energy gap between the valence and conduction bands is less than that for the bottom oxide. For an embodiment in which the charge storage layer comprises pure silicon nitride, the energy gap will be about 5.3 electron volt eV (conduction band **304** and valence band **305**). The energy level for the conduction band **304** for SiN is about 1 eV lower than that for pure silicon dioxide, as is used in the top oxide and bottom oxide in this example. The energy level for the valence band **305** for SiN is about 2.7 eV lower (holes have opposite polarity) than that for pure silicon dioxide, as is used in the top oxide and bottom oxide in this example. For embodiments in which the charge storage layer comprises silicon oxynitride SiO_xN_y, the energy gap varies with the concentrations of oxygen and nitrogen between a level less than the energy gap of pure silicon dioxide (9 eV) and a level greater than the energy gap of pure silicon nitride (5.3 eV). Thus, a silicon oxynitride charge trapping layer will have a conduction band **306** and a valance band **307**, separated by an energy gap of for one example, 7 eV. One mechanism for charge loss involves electrons (e−) that are excited from traps to the conduction band **306**, and move along the flat energy level (arrow **308**) of the conduction band to the interface with the bottom oxide, where they are able to jump (arrow **309**) to the higher level conduction band of the bottom oxide, and conduct to the substrate. Another mechanism for charge loss involves holes (h+) that are excited from traps to the valence band **307**, and move along the flat energy level (arrow **310**) of the valence band to the interface with the bottom oxide, where they are able to jump (arrow **311**) to the lower level conduction band of the bottom oxide, and conduct to the substrate.

[**0030**] **FIG. 4** is a simplified energy level diagram for an equilibrium state of a charge storage structure having an energy gap gradient. Although other dielectrics can be utilized, the structure in the illustrated embodiment includes a top layer comprising silicon dioxide (top oxide) and a bottom layer comprising silicon dioxide (bottom oxide). The charge storage layer in the illustrated embodiment comprises silicon oxynitride having a varying concentrations of oxygen and nitrogen across the width of the layer. Thus, the conduction band **400** and the valence band **401** for the top oxide are separated by about 9 eV. Also, the conduction band **402** in the valence band **403** for the bottom oxide are separated by about 9 eV. The conduction band **404** and the valence band **405** in the charge storage layer are sloped, having an energy gap near the interface **406** with top oxide that is about 5.3 eV, or higher depending on the concentrations of materials at the interface, and having an energy gap near the interface **407** with the bottom oxide that is less than about 9 eV. Electrons (e−) that are excited to the conduction band **404** have to conduct (arrow **410**) against the weak electric field that the gradient in energy gap creates before reaching the interface **407** with the bottom oxide, and are therefore less likely to escape. Likewise, holes (h+) which are excited to the valence band **405** have to conduct (arrow **411**) against the weak electric field that the gradient in the energy gap creates before reaching the interface **407** with the bottom oxide. Thus, both electrons and holes are less likely to contribute to leakage current represented by dotted arrows **412** and **413**, by this mechanism.

[**0031**] **FIG. 5** illustrates one representative structure for implementing a charge storage memory cell with a charge storage layer with a gradient in energy gap. A memory cell including the charge storage layer comprises a source/drain region **501** and a drain/source region **502** which are separated by a channel region **500** in a semiconductor substrate. A charge storage structure comprises a first dielectric layer **503** (bottom dielectric), second dielectric layer including films **504** and **504*a*** (charge storage layer), and a third dielectric layer **505** (top dielectric) under a gate **506**. The first dielectric layer **503** is preferably a silicon dioxide layer, formed by thermal oxidation. Other embodiments include a nitrided silicon dioxide, or a silicon oxynitride material for the bottom dielectric. The film **504** is preferably a silicon oxynitride, formed by the deposition process so that the energy gap at the interface with the bottom dielectric is less than in the bottom dielectric. The film **504*a*** having an increased concentration of nitrogen is formed using a nitridation treatment of the deposited silicon oxynitride material,

such as a plasma nitridation process. Thermal treatment of the top surface of film **504** of the second dielectric layer in a nitrogen environment resulting in nitrogen incorporation can also be used to provide film **504***a* in a silicon oxynitride film **504**. A thermal annealing process can be executed after the nitridation treatment to recover the plasma damage and make a more uniform slope in the distribution of materials in the charge storage layer. The thermal annealing temperature in range from 800° C. to 1100° C., with time range from 10 seconds to 120 seconds for rapid thermal process and 10 minutes to 1 hour for furnace thermal process are representative process parameters. The annealing ambient may include inert gas only or a combination of oxygen with the inert gas. The third dielectric is preferably a silicon-dioxide layer, formed by thermal oxidation. Other embodiments include a nitrided silicon dioxide, or a silicon oxynitride material. The materials are chosen so that the energy gap in the charge storage layer (second dielectric) is less than that of the top oxide near the interface with the top oxide, and less than that of the bottom oxide near the interface with the bottom oxide. Also, the material concentrations vary through the charge storage layer to create a sloped conduction band, a sloped valance band, or both a sloped conduction band and a sloped valance band, which tends to establish a weak electric field opposing charge leakage. For example, the average concentration of nitrogen in the film **504***a* is greater than the average concentration of nitrogen film **504** of charge storage layer closest to the bottom oxide in the illustrated embodiment.

[**0032**] Another embodiment is shown in **FIG. 6**, which illustrates a structure for implementing a charge storage memory cell with a charge storage layer with a gradient in energy gap. A memory cell including the charge storage layer comprises a source/drain region **601** and a drain/source region **602** which are separated by a channel region **600** in a semiconductor substrate. A charge storage structure comprises a first dielectric layer **603** (bottom dielectric), a second dielectric layer **604** including films **604***a* and **604***b* (charge storage layer), and a third dielectric layer **605** (top dielectric) under a gate **606**. The first dielectric layer **603** is preferably a silicon dioxide layer, formed by thermal oxidation. Other embodiments include a nitrided silicon dioxide, or a silicon oxynitride material for the bottom dielectric. The second dielectric layer **604** in this example comprises two films, **604***a* and **604***b*, that comprise different compounds. The second dielectric layer **604** comprises a deposited first film **604***a* of an oxynitride with band gap between 5.3 ev to 9 ev and a deposited second film **604***b* comprising a thin silicon nitride with band gap around 5.3 ev. Oxynitride film **604***a* in an alternative process is formed by a nitridation treatment on the surface of first dielectric **603**, and the silicon nitride film **604***b* in an alternative process comprises one or more oxynitride films with different nitrogen and oxygen concentrations. In yet other embodiments, a plurality of films comprising silicon oxynitride with successively increasing concentrations of nitrogen as they are formed can be utilized. A thermal annealing process can be executed after the second dielectric formation to make a more uniform slope in the distributions of oxygen and nitrogen. The thermal annealing temperature preferably ranges from 800° C. to 1100° C., with a time range from 10 seconds to 120 seconds for rapid thermal process, and 10 minutes to 1 hour for furnace thermal process. The annealing ambient includes inert gas only or the addition of oxygen to the inert gas. The third dielectric layer **605** is preferably a silicon dioxide layer, formed by thermal oxidation. Other embodiments include a nitrided silicon dioxide, or a silicon oxynitride. The materials are chosen so that the energy gap in the charge storage layer (second dielectric) varies and is less than that of the top oxide at the interface with the top oxide, and less than that of the bottom oxide at the interface with the bottom oxide.

[**0033**] **FIG. 7** illustrates heuristically the concentration profiles versus depth for oxygen on trace **700** and nitrogen on trace **701** for a charge storage structure such as that described above with respect to **FIGS. 4-6**, comprising silicon oxynitride. Although in an actual embodiment, the concentration profiles may not be so straight, and may not be monotonic, it is preferable that the concentration of nitrogen increase from a minimum near the bottom surface of the dielectric layer toward a maximum near the top surface, and that the concentration of oxygen decrease from a maximum near the bottom surface and a minimum near the top surface. It is recognized that there may be a buildup of nitrogen at the bottom interface depending on the method of manufacturing of the charge storage structure in the bottom of dielectric. However, the concentration distribution of nitrogen and oxygen can be controlled to overcome any effect of that build up, so that the effective structure has an energy gap gradient sufficient to oppose charge leakage at the bottom oxide interface.

[**0034**] **FIG. 8** illustrates yet another embodiment of a memory cell, including a dielectric structure which is engineered to oppose charge leakage at both the interface **800** with the top dielectric and the interface **801** with the bottom dielectric. Thus, in the illustrated embodiment, the valence band **803** in the charge storage layer has a minimum energy gap at a point **804** near the middle of the layer, and respective maximum energy gaps on either side of the minimum energy gap, such as at or near the interface **800** with the top dielectric and at or near the interface **801** with the bottom dielectric. Likewise the conduction band **805** in the charge storage layer has a minimum energy gap at a point **806** near the middle of the layer, and respective maximum energy gaps on either side of the minimum energy gap, such as at or near the interface **800** with the top dielectric and at or near the interface **801** with the bottom dielectric. The structure can be implemented such that the respective maximum energy gaps are close to the same, or such that they are quite different, depending on the manufacturing techniques applied and the needs of the particular implementation. Such structure could be implemented for example by depositing a nitrogen rich silicon oxynitride film between two or more oxygen rich silicon oxynitride films to form the charge storage layer.

[**0035**] **FIG. 9** is a simplified diagram of a floating gate memory cell having an interpoly dielectric layer comprising a dielectric stack on the floating gate structure, including a bottom dielectric layer **906**, a middle dielectric **907**, with an energy gap gradient, and a top dielectric layer **908**, where the energy gap gradient establishes a weak electric field at equilibrium that tends to oppose charge leakage from the floating gate **904** to the control gate **909**. The memory cell is implemented in a semiconductor substrate **900**. The cell includes a source/drain **901** and a drain/source **902** formed by respective diffusion regions, separated by a channel in the substrate **900**. A control gate **909** overlies the channel. A floating gate **904** is isolated by a tunnel dielectric layer **903**

from the channel. The interpoly dielectric comprises a bottom dielectric layer **906** on the floating gate **904**, a middle dielectric layer **907** and a top dielectric layer **908**. The substrate on which the bottom dielectric layer **906** rests is the floating gate polysilicon in this embodiment. The top and bottom dielectric layers **908** and **906** comprise materials such as silicon dioxide or silicon oxynitride.

[**0036**] The middle dielectric layer **907** in this example comprises a combination of materials including silicon, nitrogen and oxygen which make up a silicon oxynitride structure in which the concentrations of nitrogen and oxygen vary across the thickness of the element between the top and bottom dielectric layers **907** and **906**. The materials are arranged to establish an energy gap gradient that opposes charge leakage at the interface between the top dielectric layer **908**, and the control gate **909**. Other combinations of materials can be utilized as well, as discussed above.

[**0037**] While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will readily occur to those skilled in the art, which modifications and combinations will be within the spirit of the invention and the scope of the following claims.

What is claimed is:

1. A method for manufacturing an integrated circuit structure, comprising:

forming a bottom dielectric layer on a substrate;

forming a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform and arranged to induce a variation in energy gap establishing an electric field between the top and bottom surfaces tending to oppose charge motion toward at least one of the top and bottom surfaces; and

forming a top dielectric layer on the middle dielectric layer.

2. The method of claim 1, wherein the bottom dielectric layer and top dielectric layer are characterized by a first energy gap and a second energy gap respectively at respective interfaces with the bottom and top surfaces of the middle dielectric layer, and wherein the first and second energy gaps are greater than a maximum energy gap of the middle dielectric layer.

3. The method of claim 1, wherein the variation in energy gap includes a minimum energy gap spaced away from said at least one of the top and bottom surfaces, and a maximum energy gap near to said at least one of the top and bottom surfaces.

4. The method of claim 1, wherein the variation in energy gap includes a minimum energy gap spaced away from said top and bottom surfaces, and a first maximum energy gap near to said top surface and a second maximum energy gap near to said bottom surface.

5. The method of claim 1, wherein the variation in energy gap across the middle dielectric layer is substantially monotonically increasing from one to the other of the top and bottom surfaces.

6. The method of claim 1, wherein the plurality of materials comprise silicon, oxygen and nitrogen.

7. The method of claim 1, wherein the middle dielectric layer comprises silicon oxynitride.

8. The method of claim 1, wherein forming the middle dielectric layer comprises depositing one or more films by atomic layer deposition.

9. The method of claim 1, wherein forming the middle dielectric layer comprises forming a layer of silicon dioxide on the bottom dielectric, and exposing the top surface of the layer of silicon dioxide to a source of nitrogen to introduce a concentration of nitrogen near the top surface.

10. The method of claim 1, wherein forming the middle dielectric layer comprises forming a layer of silicon oxynitride on the bottom dielectric, and exposing the top surface of the layer of silicon oxynitride to a source of nitrogen to increase a concentration of nitrogen near the top surface.

11. The method of claim 1, wherein forming the middle dielectric layer comprises forming a forming a first film of silicon oxynitride on the bottom dielectric, and forming a film of silicon nitride on the first film, and annealing the first and second films.

12. The method of claim 1, wherein forming the middle dielectric layer comprises forming a sequence of films having varying concentrations of said materials.

13. A method for manufacturing an integrated circuit structure, comprising:

forming a bottom dielectric layer on a substrate;

forming a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

forming a top dielectric layer on the middle dielectric layer, wherein the middle dielectric layer comprises silicon oxynitride, and wherein the concentration of oxygen is higher in a region near the interface with the bottom dielectric than near the interface with the top dielectric, and the concentration of nitrogen is higher in a region near the interface with the top dielectric than near the interface with the bottom dielectric.

14. A method for manufacturing an integrated circuit structure, comprising:

forming a bottom dielectric layer on a substrate;

forming a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

forming a top dielectric layer on the middle dielectric layer;

wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to increase the energy gap is higher in one of

the first and the second halves than in the other of the first and the second halves.

15. A method for manufacturing an integrated circuit structure, comprising:

forming a bottom dielectric layer on a substrate;

forming
a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

forming
a top dielectric layer on the middle dielectric layer;

wherein
the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to decrease the energy gap is higher in one of the first and the second halves than in the other of the first and the second halves.

16. A method for manufacturing an integrated circuit structure, comprising:

forming
a bottom dielectric layer on a substrate;

forming
a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

forming
a top dielectric layer on the middle dielectric layer;

wherein
the concentration of materials with respect to concentration profile of a material tending to decrease the energy gap includes a maximum concentration spaced away from said top and bottom surfaces, and a first minimum concentration near to said top surface and a second minimum concentration near to said bottom surface.

17. A method for manufacturing an integrated circuit structure, comprising:

forming
a bottom dielectric layer on a substrate;

forming
a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

forming
a top dielectric layer on the middle dielectric layer;

wherein
the concentration of materials with respect to concentration profile of a material tending to increase the energy gap includes a minimum concentration spaced away from said top and bottom surfaces, and a

a
middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform and arranged to induce a variation in energy gap establishing an electric field between the top and bottom surfaces tending to oppose charge motion toward at least one of the top and bottom surfaces; and

a
top dielectric layer on the middle dielectric layer.

19. The integrated circuit structure of claim 18, wherein the bottom dielectric layer and top dielectric layer are characterized by a first energy gap and a second energy gap respectively at respective interfaces with the bottom and top surfaces of the middle dielectric layer, and wherein the first and second energy gaps are greater than a maximum energy gap of the middle dielectric layer.

20. The integrated circuit structure of claim 18, wherein the variation in energy gap includes a minimum energy gap spaced away from said at least one of the top and bottom surfaces, and a maximum energy gap near to said at least one of the top and bottom surfaces.

21. The integrated circuit structure of claim 18, wherein the variation in energy gap includes a minimum energy gap spaced away from said top and bottom surfaces, and a first maximum energy gap near to said top surface and a second maximum energy gap near to said bottom surface.

22. The integrated circuit structure of claim 18, wherein the variation in energy gap across the middle dielectric layer is substantially monotonically increasing from one to the other of the top and bottom surfaces.

23. The integrated circuit structure of claim 18, wherein the plurality of materials comprises silicon, oxygen and nitrogen.

24. The integrated circuit structure of claim 18, wherein the middle dielectric layer comprises silicon oxynitride.

25. The integrated circuit structure of claim 18, wherein the middle dielectric layer comprises silicon oxynitride, and wherein the concentration of oxygen is higher in a region near the interface with the bottom dielectric than near the interface with the top dielectric, and the concentration of nitrogen is higher in a region near the interface with the top dielectric than near the interface with the bottom dielectric.

26. The integrated circuit structure of claim 18, wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to increase the energy gap is higher in the second half than in the first half.

27. The integrated circuit structure of claim 18, wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to decrease the energy gap is higher in the first half than in the second half.

28. The integrated circuit structure of claim 18, wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to increase the energy gap is higher in the first half than in the second half.

29. The integrated circuit structure of claim 18, wherein the middle dielectric layer includes a first half near the top

dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to decrease the energy gap is higher in the second half than in the first half.

30. The integrated circuit structure of claim 18, wherein the middle dielectric layer comprises a plurality of films having varying concentrations of said materials.

31. An integrated circuit structure, comprising:

a bottom dielectric layer on a substrate;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer;

wherein the middle dielectric layer comprises silicon oxynitride, and wherein the concentration of oxygen is higher in a region near the interface with the bottom dielectric than near the interface with the top dielectric, and the concentration of nitrogen is higher in a region near the interface with the top dielectric than near the interface with the bottom dielectric.

32. An integrated circuit structure, comprising:

a bottom dielectric layer on a substrate;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer;

wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to increase the energy gap is higher in one of the first and the second halves than in the other of the first and the second halves.

33. An integrated circuit structure, comprising:

a bottom dielectric layer on a substrate;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer;

wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to decrease the energy gap is higher in one of the first and the second halves than in the other of the first and the second halves.

34. An integrated circuit structure, comprising:

a bottom dielectric layer on a substrate;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer;

wherein the concentration of materials with respect to concentration profile of a material tending to decrease the energy gap includes a maximum concentration spaced away from said top and bottom surfaces, and a first minimum concentration near to said top surface and a second minimum concentration near to said bottom surface.

35. An integrated circuit structure, comprising:

a bottom dielectric layer on a substrate;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer;

wherein the concentration of materials with respect to concentration profile of a material tending to increase the energy gap includes a minimum concentration spaced away from said top and bottom surfaces, and a first maximum concentration near to said top surface and a second maximum concentration near to said bottom surface.

36. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a bottom dielectric layer on the substrate over the channel region;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform and arranged to induce a variation in energy gap establishing an electric field between the top and bottom surfaces tending to oppose charge motion toward at least one of the top and bottom surfaces;

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer.

37. The integrated circuit memory device of claim 36, wherein the bottom dielectric layer and top dielectric layer are characterized by a first energy gap and a second energy gap respectively at respective interfaces with the bottom and top surfaces of the middle dielectric layer, and wherein the first and second energy gaps are greater than a maximum energy gap of the middle dielectric layer.

38. The integrated circuit memory device of claim 36, wherein the variation in energy gap includes a minimum energy gap spaced away from said bottom surface, and a maximum energy gap near to said top surface.

39. The integrated circuit memory device of claim 36, wherein the variation in energy gap includes a maximum energy gap spaced away from said bottom surface, and a minimum energy gap near to said top surface.

40. The integrated circuit memory device of claim 36, wherein the variation in energy gap includes a minimum energy gap spaced away from said top and bottom surfaces, and a first maximum energy gap near to said top surface and a second maximum energy gap near to said bottom surface.

41. The integrated circuit memory device of claim 36, wherein the variation in energy gap across the middle dielectric layer is substantially monotonically increasing from one to the other of the top and bottom surfaces.

42. The integrated circuit memory device of claim 36, wherein the plurality of materials comprises silicon, oxygen and nitrogen.

43. The integrated circuit memory device of claim 36, wherein the middle dielectric layer comprises silicon oxynitride.

44. The integrated circuit memory device of claim 36, wherein the middle dielectric layer comprises silicon oxynitride, and wherein the concentration of oxygen is higher in a region near the interface with the bottom dielectric than near the interface with the top dielectric, and the concentration of nitrogen is higher in a region near the interface with the top dielectric than near the interface with the bottom dielectric.

45. The integrated circuit memory device of claim 36, wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to increase the energy gap is higher in the second half than in the first half.

46. The integrated circuit memory device of claim 36, wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to decrease the energy gap is higher in the first half than in the second half.

47. The integrated circuit memory device of claim 36, wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to increase the energy gap is higher in the first half than in the second half.

48. The integrated circuit memory device of claim 36, wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to decrease the energy gap is higher in the second half than in the first half.

49. The integrated circuit memory device of claim 36, wherein the middle dielectric layer comprises a plurality of films having varying concentrations of said materials.

50. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a bottom dielectric layer on the substrate over the channel region;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the middle dielectric layer comprises silicon oxynitride, and wherein the concentration of oxygen is higher in a region near the interface with the bottom dielectric than near the interface with the top dielectric, and the concentration of nitrogen is higher in a region near the interface with the top dielectric than near the interface with the bottom dielectric.

51. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a bottom dielectric layer on the substrate over the channel region;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to increase the energy gap is higher in one of the first and the second halves than in the other of the first and the second halves.

52. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a bottom dielectric layer on the substrate over the channel region;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to decrease the energy gap is higher in one of the first and the second halves than in the other of the first and the second halves.

53. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a bottom dielectric layer on the substrate over the channel region;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the concentration of materials with respect to concentration profile of a material tending to decrease the energy gap includes a maximum concentration spaced away from said top and bottom surfaces, and a first minimum concentration near to said top surface and a second minimum concentration near to said bottom surface.

54. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a bottom dielectric layer on the substrate over the channel region;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the concentration of materials with respect to concentration profile of a material tending to increase the energy gap includes a minimum concentration spaced away from said top and bottom surfaces, and a first maximum concentration near to said top surface and a second maximum concentration near to said bottom surface.

55. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a tunnel dielectric layer over the channel region;

a floating gate structure over the tunnel dielectric layer;

a bottom dielectric layer on the substrate over the floating gate structure;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the middle dielectric layer comprises silicon oxynitride, and wherein the concentration of oxygen is higher in a region near the interface with the top dielectric than near the interface with the bottom dielectric, and the concentration of nitrogen is higher in a region near the interface with the bottom dielectric than near the interface with the top dielectric.

56. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a tunnel dielectric layer over the channel region;

a floating gate structure over the tunnel dielectric layer;

a bottom dielectric layer on the substrate over the floating gate structure;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to increase the energy gap is higher in one of the first and the second halves than in the other of the first and the second halves.

57. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a tunnel dielectric layer over the channel region;

a floating gate structure over the tunnel dielectric layer;

a bottom dielectric layer on the substrate over the floating gate structure;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the middle dielectric layer includes a first half near the top dielectric and a second half near the bottom dielectric, and wherein the concentration of a material tending to decrease the energy gap is higher in one of the first and the second halves than in the other of the first and the second halves.

58. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a tunnel dielectric layer over the channel region;

a floating gate structure over the tunnel dielectric layer;

a bottom dielectric layer on the substrate over the floating gate structure;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the concentration of materials with respect to concentration profile of a material tending to decrease the energy gap includes a maximum concentration spaced away from said top and bottom surfaces, and a first minimum concentration near to said top surface and a second minimum concentration near to said bottom surface.

59. An integrated circuit memory device, comprising:

a substrate;

source and drain regions in the substrate spaced apart by a channel region;

a tunnel dielectric layer over the channel region;

a floating gate structure over the tunnel dielectric layer;

a bottom dielectric layer on the substrate over the floating gate structure;

a middle dielectric layer on the bottom dielectric layer, the middle dielectric layer having a top surface and a bottom surface and comprising a plurality of materials with respective concentration profiles for at least two of the plurality of materials between the top and bottom surfaces that are non-uniform; and

a top dielectric layer on the middle dielectric layer; and

a gate on the top dielectric layer;

wherein the concentration of materials with respect to concentration profile of a material tending to increase the energy gap includes a minimum concentration spaced away from said top and bottom surfaces, and a first maximum concentration near to said top surface and a second maximum concentration near to said bottom surface.

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