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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	11/22/2011	8063434	PM07027	5484

60909 7590 11/02/2011
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 491 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Igor Polishchuk, Fremont, CA;
Sagy Levy, Zichron Ya'akov, ISRAEL;
Krishnaswamy Ramkumar, San Jose, CA;

11/21/2008 02:08 6502403500

WILLIAM NUTTLE

12152518 - GAU: 2893

PAGE 03/03

PTO/SB/08 (10-08)

Approved for use through 11/30/2008. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1
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Complete if Known

Application Number	12/152 518
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Filing Date	May 13, 2008
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First Named Inventor	Igor Polishchuk, et al.
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Art Unit	2812
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Examiner Name	
Attorney Docket Number	PM2007027

Change(s) applied

to document,

/J.C.J./

8/8/2011

Change(s) applied

to document.

/J.C.J./

8/6/2011

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

Examiner Signature	/Ngan Ngo/	Date Considered	09/24/2010
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. *Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. * Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to be (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PAGE 3/3 * RCVD AT 11/21/2008 4:15:55 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-5/43 * DNIS:2738300 * CSID:6502403500 * DURATION (mm:ss):00:46

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /NN/

Sandisk Technologies, Inc. - Ex. 1038, Page 000002



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM07027	5484
60909 7590 10/24/2011 CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709			EXAMINER NGO, NGAN V	
			ART UNIT 2893	PAPER NUMBER
			MAIL DATE 10/24/2011	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Rule 312 Communication	Application No.	Applicant(s)
	12/152,518	POLISHCHUK ET AL.
	Examiner	Art Unit

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on 14 October 2011 under 37 CFR 1.312 has been considered, and has been:
- a) ☒ entered.
 - b) ☐ entered as directed to matters of form not affecting the scope of the invention.
 - c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.
 - d) ☐ disapproved. See explanation below.
 - e) ☐ entered in part. See explanation below.


Publishing Division

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

60909 7590 07/14/2011
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM07027	5484

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$0	\$0	\$1510	10/14/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Cypress Semiconductor Corporation San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3781 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature *Larry Johnson*
Typed or printed name Larry Johnson

Date 10/14/11
Registration No. 56,861

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	12/152,518	Confirmation No. 5484
In re Application of	:	Igor Polishchuk	
Filed	:	May 13, 2008	
TC/A.U.	:	2893	
Examiner	:	NGAN V. NGO	
Docket No.	:	PM2007027	
Customer No.	:	60909	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 C.F.R. § 1.312

Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant is in receipt of a Notice of Allowance and Fee Due Form, mailed July 14, 2011, in connection with the above-identified application. The Issue Fee is due on or before October 14, 2011. Pursuant to 37 C.F.R. § 1.312, the Examiner is respectfully requested to favorably consider and enter the following amendments to the present application.

Amendments to the Abstract begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

Amendments to the Abstract:

Please amend the Abstract of Disclosure as follows:

An embodiment of a semiconductor device includes a non-volatile memory transistor including an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack comprising a multilayer charge storage layer including a silicon-rich, oxygen-lean top silicon oxynitride layer and a silicon-rich, oxygen-rich bottom silicon oxynitride layer, and a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a high work function gate electrode.

~~Semiconductor devices including non-volatile memory transistors and methods of fabricating the same to improve performance thereof are provided. In one embodiment, the memory transistor comprises an oxide-nitride-oxide (ONO) stack on a surface of a semiconductor substrate, and a high work function gate electrode formed over a surface of the ONO stack. Preferably, the gate electrode comprises a doped polysilicon layer, and the ONO stack comprises multi-layer charge storing layer including at least a substantially trap-free bottom oxynitride layer and a charge trapping top oxynitride layer. More preferably, the device also includes a metal oxide semiconductor (MOS) logic transistor formed on the same substrate, the logic transistor including a gate oxide and a high work function gate electrode. In certain embodiments, the dopant is a P⁺ dopant and the memory transistor comprises N-type (NMOS) siliconoxide-nitride-oxide-silicon (SONOS) transistor while the logic transistor a P-type (PMOS) transistor. Other embodiments are also disclosed.~~

REMARKS

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.19, 1.20 and 1.21 that may be required to issue the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

By: /Larry J. Johnson/
Larry J. Johnson
Attorney for Applicant
Registration No. 56,861

Electronic Patent Application Fee Transmittal				
Application Number:		12152518		
Filing Date:		13-May-2008		
Title of Invention:		MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
First Named Inventor/Applicant Name:		Igor Polishchuk		
Filer:		Larry Joel Johnson/Lauren Navarro		
Attorney Docket Number:		PM07027		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				1740

Electronic Acknowledgement Receipt	
EFS ID:	11194459
Application Number:	12152518
International Application Number:	
Confirmation Number:	5484
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Larry Joel Johnson/Lauren Navarro
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	PM07027
Receipt Date:	14-OCT-2011
Filing Date:	13-MAY-2008
Time Stamp:	19:47:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1740
RAM confirmation Number	6216
Deposit Account	503781
Authorized User	
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	PM07027_TransmittalLetter_10132011.pdf	157926 ebf56048ad9beb80710b98759268ca84a85795e	no	2

Warnings:

Information:

2	Issue Fee Payment (PTO-85B)	PM07027_TransmittalLetterPayment_10132011.pdf	423470 695dbd724ef24b8ecc814777ae264ec6228ce25c	no	1
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Warnings:

Information:

3	Amendment after Notice of Allowance (Rule 312)	PM07027_312_AmendmentPDF.pdf	30339 8cfc596b9181c1548879cc3e3ed1cbe41322f68	no	3
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Warnings:

Information:

4	Fee Worksheet (SB06)	fee-info.pdf	30276 8bb7f74e9a60a6d994c6dafcd0e2af83222a2f9	no	2
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Warnings:

Information:

Total Files Size (in bytes): 642011

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Examiner: NGO, NGAN V
	)	
Igor Polishchuk	)	Group Art Unit: 2893
	)	
Application No.: 12/152,518	)	Confirmation No.: 5484
	)	
Filed: 05-13-2008	)	
	)	
For: MEMORY TRANSISTOR WITH	)	
MULTIPLE CHARGE STORING	)	
LAYERS AND A HIGH WORK	)	
FUNCTION GATE ELECTRODE	)	

ISSUE FEE TRANSMITTAL

Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

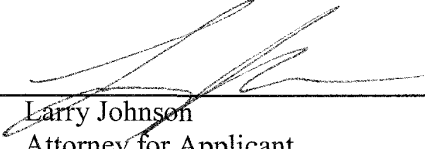
Applicant is in receipt of a Notice of Allowance and Fee Due Form, mailed July 14, 2011, in connection with the above-identified application. The Issue Fee is due on or before October 14, 2011. Applicant hereby submits the Issue Fee and/or the Publication Fee.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.19, 1.20 and 1.21 that may be required to issue the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Customer No.: 60909

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

Dated: 10/14/11 By: 
Larry Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Customer No.: 60909



UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 07/14/2011
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
NGO, NGAN V

ART UNIT PAPER NUMBER

2893

DATE MAILED: 07/14/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/152,518 05/13/2008 Igor Polishchuk PM07027 5484

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$0	\$0	\$1510	10/14/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

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or Fax (571)-273-2885**

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Certificate of Mailing or Transmission

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM07027	5484

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

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EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	257-324000

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- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM07027	5484

60909	7590	07/14/2011
CYPRESS SEMICONDUCTOR CORPORATION		
198 CHAMPION COURT		
SAN JOSE, CA 95134-1709		

EXAMINER	
NGO, NGAN V	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 07/14/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 309 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 309 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/152,518	POLISHCHUK ET AL.	
	Examiner	Art Unit	
	NGAN NGO	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 6-28-11.

2. ☒ The allowed claim(s) is/are 23-31.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ 7. ☒ Examiner's Amendment/Comment 8. ☐ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
--	--

/Ngan Ngo/ Primary Examiner, Art Unit 2893	
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Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

In the claims:

Cancel non-elected claims 16-20.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

7/13/2011

<i>Index of Claims</i> 	Application/Control No. 12152518	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant						☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE									
Final	Original	06/03/2010	09/25/2010	03/08/2011	07/11/2011						
	1	÷	✓	✓	-						
	2	÷	✓	✓	-						
	3	÷	✓	✓	-						
	4	÷	✓	✓	-						
	5	÷	✓	✓	-						
	6	÷	✓	-	-						
	7	÷	✓	-	-						
	8	÷	✓	✓	-						
	9	÷	✓	✓	-						
	10	÷	✓	✓	-						
	11	÷	✓	✓	-						
	12	÷	✓	✓	-						
	13	÷	✓	✓	-						
	14	÷	✓	✓	-						
	15	÷	✓	✓	-						
	16	÷	N	-	-						
	17	÷	N	-	-						
	18	÷	N	-	-						
	19	÷	N	-	-						
	20	÷	N	-	-						
	21			✓	-						
	22			✓	-						
1	23			=	=						
6	24			=	=						
7	25			=	=						
8	26			=	=						
9	27			=	=						
2	28				=						
3	29				=						
4	30				=						
5	31				=						

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	66270	oxynitride or oxynitride	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/07/11 13:58
L2	585798	((("257") or ("438")). CLAS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/07/11 13:58
L3	37495	L1 and L2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/07/11 13:58
L4	4256	L3 and (ono or sonos)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/07/11 13:58
L5	3570	L4 and memory and gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/07/11 13:58
L6	1795	L5 and trap\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/07/11 13:58
L7	3851	(257/324,325, E29.132,E29.309). CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/07/11 14:56

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	3	(257/324,325,E29.132, E29.309).CCLS.	UPAD	OR	OFF	2011/07/11 15:39

7/11/11 3:54:26 PM

C:\Documents and Settings\NNgo\My Documents\EAST\workspaces\12152518.wsp

Search Notes 	Application/Control No. 12152518	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner Ngan Ngo	Art Unit 2893

SEARCHED			
Class	Subclass	Date	Examiner
257	324, 325, E29.132, E29.309	7-11-11	NN

SEARCH NOTES		
Search Notes	Date	Examiner
BRS search using EAST. See printout	9-24-10	NN
BRS search using EAST. See printout	3-8-11	NN
BRS search using EAST. See printout	7-11-11	NN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	324, 325, E29.132, E29.309	7-11-11	NN

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Issue Classification 	Application/Control No. 12152518	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
257		324				H	0	1	L	29 / 792 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
257	325	E29.132	E29.309															

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3		19												
	4		20												
	5		21												
	6		22												
	7	1	23												
	8	6	24												
	9	7	25												
	10	8	26												
	11	9	27												
	12	2	28												
	13	3	29												
	14	4	30												
	15	5	31												
	16														

NONE		Total Claims Allowed:	
		9	
(Assistant Examiner)	(Date)		
/NGAN NGO/ Primary Examiner.Art Unit 2893	07/11/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	12/152,518	Confirmation No. 5484
In re Application of	:	Igor Polishchuk	
Filed	:	May 13, 2008	
TC/A.U.	:	2893	
Examiner	:	NGAN V. NGO	
Docket No.	:	PM2007027	
Customer No.	:	60909	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE OF NON-COMPLIANT AMENDMENT

INTRODUCTORY COMMENTS

This paper is responsive to the Notice Of Non-Compliant Amendment mailed on June 21, 2011, and in connection with an amendment submitted on 06 June 2011.

In this response the text of withdrawn claims 16-20 has been provided and identifiers of claims 23 and 27 corrected.

Amendments to the Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Claims:

1-15. (Canceled)

16. (Withdrawn) A method of forming a semiconductor device comprising steps of:
forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer;
forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and
forming a high work function gate electrode on a surface of the ONO dielectric stack.

17. (Withdrawn) A method according to claim 16, wherein step of forming a high work function gate electrode on a surface of the ONO dielectric stack comprises the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack.

18. (Withdrawn) A method according to claim 17, wherein the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack further comprises the step of also forming the doped polysilicon layer on a surface of the oxide layer of the MOS logic transistor form a high work function gate electrode thereon.

19. (Withdrawn) A method according to claim 18, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, the doped polysilicon layer comprises a P⁺ dopant, and wherein the method further comprises the steps of patterning the he doped polysilicon layer, the ONO dielectric stack and the oxide layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

20. (Withdrawn) A method according to claim 16, wherein the step of forming an ONO dielectric stack including a multi-layer charge storage layer comprises the steps of forming at least a substantially trap free bottom oxynitride layer followed by forming a charge trapping top oxynitride layer.

21-22. (Canceled)

23. (Previously Presented) A semiconductor device comprising:

a non-volatile memory transistor including an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack comprising a multi-layer charge storage layer including a silicon-rich, oxygen-lean top silicon oxynitride layer and a silicon-rich, oxygen-rich bottom silicon oxynitride layer; and

a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a high work function gate electrode.

24. (Currently Amended) A semiconductor device according to claim [[23]]28, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a N⁺ doped polysilicon layer to form an P-type (PMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a N-type (NMOS) logic transistor.

25. (Currently Amended) A semiconductor device according to claim [[23]]28, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a P⁺ doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (NMOS) logic transistor.

26. (Currently Amended) A semiconductor device according to claim [[23]]28, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor are formed from a single, patterned doped polysilicon layer.

27. (Previously Presented) A semiconductor device according to claim 23, wherein the top silicon oxynitride layer is a trap-rich silicon oxynitride layer and the bottom silicon oxynitride layer is a substantially trap free silicon oxynitride layer.

28. (New) A semiconductor device according to claim 23, wherein the non-volatile memory transistor comprises a high work function gate electrode formed over a surface of the ONO dielectric stack.

29. (New) A semiconductor device according to claim 28, wherein the top silicon oxynitride layer is a trap-rich silicon oxynitride layer and the bottom silicon oxynitride layer is a substantially trap free silicon oxynitride layer.

30. (New) A semiconductor device according to claim 23, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein the high work function gate electrode of the logic transistor comprise a N⁺ doped polysilicon layer to form a N-type (NMOS) logic transistor.

31. (New) A semiconductor device according to claim 23, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein the high work function gate electrode of the logic transistor comprise a P⁺ doped polysilicon layer to form a P-type (NMOS) logic transistor.

REMARKS

This paper is responsive to the Notice Of Non-Compliant Amendment mailed on June 2, 2011, and in connection with a non-final amendment submitted with a Request for Continued Examination (RCE) filed on 24 May 2011.

In this response the text of withdrawn claims 16-20 has been provided and identifiers of claims 23 and 27 corrected.

Conclusion

It is believed no fees are required for filing this amendment. However, if necessary, please charge any additional fees under 37 CFR §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, or apply any credits to PTO deposit account number: 50-3467.

Respectfully submitted,
Igor Polishchuk

Dated: June 28, 2011

By: /William E. Nuttle /
William E. Nuttle, Reg. No. 42,943
Attorney for the Applicant(s)

Electronic Acknowledgement Receipt	
EFS ID:	10408813
Application Number:	12152518
International Application Number:	
Confirmation Number:	5484
Title of Invention:	Memory transistor with multiple charge storing layers and a high work function gate electrode
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	William Edward Nuttle
Filer Authorized By:	
Attorney Docket Number:	PM07027
Receipt Date:	28-JUN-2011
Filing Date:	13-MAY-2008
Time Stamp:	18:47:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PM02007027_Resp_Non-Compliant_Amendment.pdf	78975 ecb20ee3207adf64821697180650a47e7ec150d7	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Supplemental Response or Supplemental Amendment	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	5
Warnings:			
Information:			
Total Files Size (in bytes):		78975	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/152,518		Filing Date 05/13/2008		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		X \$ =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		X \$ =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
			TOTAL		TOTAL					
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	06/28/2011	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0	X \$ =	OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$ =	OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE	OR	TOTAL ADD'L FEE	0	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE	OR	TOTAL ADD'L FEE		
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Legal Instrument Examiner:
/RUBY JOHNSON/



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60909 e 06/21/2011

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Paper No.

Application No.:	12/152,518 *12152518*	Date Mailed:	06/21/2011
First Named Inventor:	Polishchuk, Igor,	Examiner:	NGO, NGAN V
Attorney Docket No.:	PM07027	Art Unit:	2893
Confirmation No.:	5484	Filing Date:	05/13/2008

Please find attached an Office communication concerning this application or proceeding.

Commissioner for Patents

Notice of Non-Compliant Amendment (37 CFR 1.121)	Application No. 12/152,518	Applicant(s) POLISHCHUK ET AL.	
		Art Unit 2400	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The amendment document filed on 06 June, 2011 is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121 or 1.4. In order for the amendment document to be compliant, correction of the following item(s) is required.

THE FOLLOWING MARKED (X) ITEM(S) CAUSE THE AMENDMENT DOCUMENT TO BE NON-COMPLIANT:

- ☐ 1. Amendments to the specification:
 - ☐ A. Amended paragraph(s) do not include markings.
 - ☐ B. New paragraph(s) should not be underlined.
 - ☐ C. Other _____.
- ☐ 2. Abstract:
 - ☐ A. Not presented on a separate sheet. 37 CFR 1.72.
 - ☐ B. Other _____.
- ☐ 3. Amendments to the drawings:
 - ☐ A. The drawings are not properly identified in the top margin as "Replacement Sheet," "New Sheet," or "Annotated Sheet" as required by 37 CFR 1.121(d).
 - ☐ B. The practice of submitting proposed drawing correction has been eliminated. Replacement drawings showing amended figures, without markings, in compliance with 37 CFR 1.84 are required.
 - ☐ C. Other _____.
- ☒ 4. Amendments to the claims:
 - ☐ A. A complete listing of all of the claims is not present.
 - ☐ B. The listing of claims does not include the text of all pending claims (including withdrawn claims)
 - ☒ C. Each claim has not been provided with the proper status identifier, and as such, the individual status of each claim cannot be identified. Note: the status of every claim must be indicated after its claim number by using one of the following status identifiers: (Original), (Currently amended), (Canceled), (Previously presented), (New), (Not entered), (Withdrawn) and (Withdrawn-currently amended).
 - ☐ D. The claims of this amendment paper have not been presented in ascending numerical order.
 - ☒ E. Other: Claims, 23 & 27 the status identifier is incorrect.
- ☐ 5. Other (e.g., the amendment is unsigned or not signed in accordance with 37 CFR 1.4): For further explanation of the amendment format required by 37 CFR 1.121, see MPEP § 714.

TIME PERIODS FOR FILING A REPLY TO THIS NOTICE:

1. Applicant is given **no new time period** if the non-compliant amendment is an after-final amendment or an amendment filed after allowance, or a drawing submission (only). If applicant wishes to resubmit the non-compliant after-final amendment with corrections, the **entire corrected amendment** must be resubmitted.
2. Applicant is given **one month**, or thirty (30) days, whichever is longer, from the mail date of this notice to supply the correction, if the non-compliant amendment is one of the following: a preliminary amendment, a non-final amendment (including a submission for a request for continued examination (RCE) under 37 CFR 1.114), a supplemental amendment filed within a suspension period under 37 CFR 1.103(a) or (c), and an amendment filed in response to a Quayle action. If any of above boxes 1 to 4 are checked, the correction required is only the corrected section of the non-compliant amendment in compliance with 37 CFR 1.121.

Extensions of time are available under 37 CFR 1.136(a) only if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action.

Failure to timely respond to this notice will result in:

Abandonment of the application if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action; or

Non-entry of the amendment if the non-compliant amendment is a preliminary amendment or supplemental amendment.

Legal Instruments Examiner (LIE), if applicable /PEARLIE A. FENNELL/

Telephone No: (571)272-1006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	12/152,518	Confirmation No. 5484
In re Application of	:	Igor Polishchuk	
Filed	:	May 13, 2008	
TC/A.U.	:	2893	
Examiner	:	NGAN V. NGO	
Docket No.	:	PM2007027	
Customer No.	:	60909	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

This paper is responsive to the Office Action mailed on March 9, 2011, and is timely filed.

Amendments to the Claims are reflected in the listing of the claims which begin on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

Amendments to the Claims:

1-15. (Canceled)

16-20. (Withdrawn).

21-22. (Canceled)

23. (Allowed) A semiconductor device comprising:

a non-volatile memory transistor including an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack comprising a multi-layer charge storage layer including a silicon-rich, oxygen-lean top silicon oxynitride layer and a silicon-rich, oxygen-rich bottom silicon oxynitride layer; and

a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a high work function gate electrode.

24. (Currently Amended) A semiconductor device according to claim [[23]]28, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a N+ doped polysilicon layer to form an P-type (PMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a N-type (NMOS) logic transistor.

25. (Currently Amended) A semiconductor device according to claim [[23]]28, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a P+ doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (NMOS) logic transistor.

26. (Currently Amended) A semiconductor device according to claim [[23]]28, wherein both the high work function gate electrode of the memory transistor and the high work

function gate electrode of the logic transistor are formed from a single, patterned doped polysilicon layer.

27. (Allowed) A semiconductor device according to claim 23, wherein the top silicon oxynitride layer is a trap-rich silicon oxynitride layer and the bottom silicon oxynitride layer is a substantially trap free silicon oxynitride layer.

28. (New) A semiconductor device according to claim 23, wherein the non-volatile memory transistor comprises a high work function gate electrode formed over a surface of the ONO dielectric stack.

29. (New) A semiconductor device according to claim 28, wherein the top silicon oxynitride layer is a trap-rich silicon oxynitride layer and the bottom silicon oxynitride layer is a substantially trap free silicon oxynitride layer.

30. (New) A semiconductor device according to claim 23, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein the high work function gate electrode of the logic transistor comprise a N⁺ doped polysilicon layer to form a N-type (NMOS) logic transistor.

31. (New) A semiconductor device according to claim 23, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein the high work function gate electrode of the logic transistor comprise a P⁺ doped polysilicon layer to form a P-type (NMOS) logic transistor.

REMARKS

Claims 23-31 remain in this application, claims 16-20 having been withdrawn, claims 1-15 and 21-22 having been canceled, and claims 28-31 being added. Claims 24-26 are hereby amended.

The amendments and added claims are supported by the detailed description, figures and claims as originally filed, no new matter is being added, and entry of the amendments and added claims is requested.

Claim Rejections – 35 U.S.C. § 103:

Claims 1-5, 8-15, 21, and 22 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Nomoto et al (US Pat No.6,906,390) in view of Zheng et al (US Pat No. 6,912,163 82).

By this response claims 1-5, 8-15, 21, and 22 have been canceled thereby obviating the rejection with respect to these claims.

Allowable Subject Matter

The Examiner indicated Claims 23-27 as allowed.

Applicant thanks the examiner for allowance of these claims.

Applicant further submits that added dependent claims 28-31 are allowable as depending from allowed independent claim 23.

Claims 24-26 are hereby being amended to depend from added claim dependent 28 to provide antecedent basis for “the high work function gate electrode of the memory transistor.”

Accordingly, Applicants submit that claim 23, as well as claims 24-31 which are dependent therefrom, are in condition for allowance.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant’s silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or

legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record is relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, William E. Nuttle at (650) 207-3418.

It is believed no fees are required for filing this amendment. However, if necessary, please *charge any additional fees under 37 CFR §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application*, or apply any credits to our PTO deposit account number: 50-3781.

Respectfully submitted,
Igor Polishchuk

Dated: June 6, 2011

By: /William E. Nuttle /.
William E. Nuttle, Reg. No. 42,943
Attorney for the Applicant(s)

Electronic Acknowledgement Receipt	
EFS ID:	10245235
Application Number:	12152518
International Application Number:	
Confirmation Number:	5484
Title of Invention:	Memory transistor with multiple charge storing layers and a high work function gate electrode
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	William Edward Nuttle
Filer Authorized By:	
Attorney Docket Number:	PM07027
Receipt Date:	06-JUN-2011
Filing Date:	13-MAY-2008
Time Stamp:	22:13:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PM02007027ROA2.pdf	117541 b6f630dc21897f8d345cc245fa0ecdac995b a25	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	3
	Applicant Arguments/Remarks Made in an Amendment	4	5
Warnings:			
Information:			
Total Files Size (in bytes):		117541	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/152,518		Filing Date 05/13/2008		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		X \$ =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		X \$ =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL				TOTAL			
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	06/06/2011	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 9	Minus	** 20	= 0	X \$ =	OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	X \$ =	OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE	OR	TOTAL ADD'L FEE	0		
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE	OR	TOTAL ADD'L FEE			
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

Legal Instrument Examiner:
/PEARLIE A. FENNEL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM07027	5484
60909 7590 03/09/2011 CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709			EXAMINER NGO, NGAN V	
			ART UNIT 2893	PAPER NUMBER
			MAIL DATE 03/09/2011	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/152,518	Applicant(s) POLISHCHUK ET AL.	
	Examiner Ngan Ngo	Art Unit 2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 December 2010.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,8-15 and 21-27 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 23-27 is/are allowed.
6) ☒ Claim(s) 1-5,8-15,21 and 22 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date: _____ | 6) ☐ Other: _____ |

The amendment filed December 28, 2010 has been entered and made of record as paper no. 20101228.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, 8-15, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nomoto et al (US 6,906,390 B2) in view of Zheng et al (6,912,163 B2, of record).

Nomoto discloses in figures 2-3H a non-volatile memory transistor comprising: an oxide-nitride-oxide (BTM, CS, and TOP) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack comprising a multi-layer charge storage layer including a substantially trap free bottom silicon oxynitride layer (CS1) and a charge trapping top silicon oxynitride layer (CS2); and a gate electrode (G) formed of doped polysilicon over a surface of the ONO dielectric stack. Note lines 9-13, column 7 of Nomoto. Zheng teaches that gate electrode formed of doped polysilicon is high work function gate electrode. Therefore it would have been obvious to one of ordinary skill in the art that the gate electrode in Nomoto is a high work function gate electrode.

Claims 23-27 are allowed.

Applicant's arguments with respect to claims 1-5, 8-15, 21, and 22 have been considered but are moot in view of the new ground(s) of rejection.

The other references are cited to show other structures pertinent to Applicants' disclosure.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

March 9, 2011

Notice of References Cited	Application/Control No. 12/152,518	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.	
	Examiner Ngan Ngo	Art Unit 2893	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0122204 A1	07-2003	Nomoto et al.	257/406
*	B	US-6,906,390 B2	06-2005	Nomoto et al.	257/406
*	C	US-2005/0230766 A1	10-2005	Nomoto et al.	257/411
*	D	US-2008/0290399 A1	11-2008	Levy et al.	257/324
*	E	US-2010/0041222 A1	02-2010	Puchner et al.	438/591
*	F	US-2010/0295118 A1	11-2010	Bhattacharyya, Arup	257/325
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> *1215251 8*	Application/Control No. 12152518	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☐ T.D.
 ☐ R.1.47

CLAIM		DATE							
Final	Original	06/03/2010	09/25/2010	03/08/2011					
	1	÷	✓	✓					
	2	÷	✓	✓					
	3	÷	✓	✓					
	4	÷	✓	✓					
	5	÷	✓	✓					
	6	÷	✓	-					
	7	÷	✓	-					
	8	÷	✓	✓					
	9	÷	✓	✓					
	10	÷	✓	✓					
	11	÷	✓	✓					
	12	÷	✓	✓					
	13	÷	✓	✓					
	14	÷	✓	✓					
	15	÷	✓	✓					
	16	÷	N	-					
	17	÷	N	-					
	18	÷	N	-					
	19	÷	N	-					
	20	÷	N	-					
	21			✓					
	22			✓					
	23			=					
	24			=					
	25			=					
	26			=					
	27			=					

Search Notes *1215251 8*	Application/Control No. 12152518	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner Ngan Ngo	Art Unit 2893

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
BRS search using EAST. See printout	9-24-10	NN
BRS search using EAST. See printout	3-8-11	NN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	158	high adj work adj function adj gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/23 23:43
S2	102	S1 and (ono or sonos)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/23 23:44
S3	97	S2 and oxynitride	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/23 23:56
S4	0	12/152518	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/23 23:57
S6	158	high adj work adj function adj gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/24 20:06
S7	102	S6 and (ono or sonos)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/24 20:06
S8	97	S7 and oxynitride	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/24 20:06
S9	8	("20070246753" "20070262451" "7312496" "7323742").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/24 20:21

S10	0	12/152518	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/15 22:35
S11	62160	oxynitride or oxy- nitride	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/15 22:40
S12	568800	(("257") or ("438")). CLAS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/01/15 22:41
S13	35040	S11 and S12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/15 22:41
S14	4019	S13 and (ono or sonos)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/15 22:41
S15	3369	S14 and memory and gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/15 22:42
S16	1676	S15 and trap\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/15 22:43
S17	34	S15 and (trap\$5 near2 free)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/01/15 22:44
S19	3648	(257/324,325,E29.132, E29.309).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/01/16 11:51

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L1	9	(257/324,325,E29.132, E29.309).CCLS.	UPAD	OR	OFF	2011/01/16 16:44
S5	1	12/152518	USPAT; UPAD	OR	ON	2010/09/23 23:57
S18	1	12/152518	USPAT; UPAD	OR	ON	2011/01/15 22:35

1/ 16/ 11 6:04:55 PM

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	12/152,518	Confirmation No. 5484
In re Application of	:	Igor Polishchuk	
Filed	:	May 13, 2008	
TC/A.U.	:	2893	
Examiner	:	NGAN V. NGO	
Docket No.	:	PM2007027	
Customer No.	:	60909	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

This paper is responsive to the Office Action mailed on September 29, 2010, and is timely filed.

Amendments to the Claims are reflected in the listing of the claims which begin on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

1. (Currently Amended) A non-volatile memory transistor comprising:
an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate,
the ONO dielectric stack comprising a multi-layer charge storage layer including a
substantially trap free bottom silicon oxynitride layer and a charge trapping top silicon
oxynitride layer; and
high work function gate electrode formed over a surface of the ONO dielectric stack.
2. (Original) A memory transistor according to claim 1, wherein the high work function gate electrode comprises a doped polysilicon layer.
3. (Original) A memory transistor according to claim 2, wherein the semiconductor substrate comprises a silicon surface on which the ONO dielectric stack is formed to form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a SONOS memory transistor.
4. (Original) A memory transistor according to claim 3, wherein the doped polysilicon layer comprises a P+ dopant to form a NMOS SONOS memory transistor.
5. (Original) A memory transistor according to claim 4, wherein the P+ dopant comprises boron or difluoroborane (BF₂).
- 6-7. (Canceled)
8. (Currently Amended) A memory transistor according to claim [7]1, wherein the top silicon oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean silicon oxynitride layer, and the bottom silicon oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich silicon oxynitride layer.
9. (Currently Amended) A semiconductor device including a non-volatile memory transistor comprising:

an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack including a multi-layer charge storage layer comprising multiple silicon oxynitride layers; and

a high work function gate electrode formed over a surface of the ONO dielectric stack.

10. (Original) A semiconductor device according to claim 9, further comprising a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a high work function gate electrode.

11. (Original) A semiconductor device according to claim 10, wherein at least one of the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprises a doped polysilicon layer.

12. (Original) A semiconductor device according to claim 11, wherein the doped polysilicon layer comprises a P⁺ dopant.

13. (Original) A semiconductor device according to claim 12, wherein the P⁺ dopant comprises boron or difluoroborane (BF₂).

14. (Original) A semiconductor device according to claim 12, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a P⁺ doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

15. (Currently Amended) A semiconductor device according to claim 9, wherein the multi-layer charge storing layer comprises at least a substantially trap free bottom silicon oxynitride layer and a charge trapping top silicon oxynitride layer.

16-20. (Withdrawn).

21. (New) A memory transistor according to claim 3, wherein the doped polysilicon layer comprises a N⁺ dopant to form a PMOS SONOS memory transistor.

22. (New) A semiconductor device according to claim 11, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a N⁺ doped polysilicon layer to form an P-type (PMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a N-type (NMOS) logic transistor.

23. (New) A semiconductor device comprising:

a non-volatile memory transistor including an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack comprising a multi-layer charge storage layer including a silicon-rich, oxygen-lean top silicon oxynitride layer and a silicon-rich, oxygen-rich bottom silicon oxynitride layer; and

a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a high work function gate electrode.

24. (New) A semiconductor device according to claim 23, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a N⁺ doped polysilicon layer to form an P-type (PMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a N-type (NMOS) logic transistor.

25. (New) A semiconductor device according to claim 23, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a P⁺ doped polysilicon layer to form an

N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (NMOS) logic transistor.

26. (New) A semiconductor device according to claim 23, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor are formed from a single, patterned doped polysilicon layer.

27. (New) A semiconductor device according to claim 23, wherein the top silicon oxynitride layer is a trap-rich silicon oxynitride layer and the bottom silicon oxynitride layer is a substantially trap free silicon oxynitride layer.

REMARKS

Claims 1-5, 8-15 and 21-27 remain in this application, claims 16-20 having been withdrawn and claims 6-7 hereby being canceled and claims 21-27 being added. Claims 1, 8, 9 and 15 are hereby amended.

The amendments and added claims are supported by the detailed description, figures and claims as originally filed, no new matter is being added, and entry of the amendments and added claims is requested.

Claim Rejections – 35 U.S.C. § 102:

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being allegedly unpatentable over Zheng et al (US Pat No. 6,912,163 82).

By this response claim 1 has been amended to include the features of now canceled claim 7 and intervening claim 6.

Accordingly, Applicant submits that claim 1, as well as claims 2-5 which are dependent therefrom, are not anticipated by Zheng.

Claim Rejections – 35 U.S.C. § 103:

Claims 7-15 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Zheng in view of in view of Wang et al (US Pat. App. No. 2007/0272916 A1) and Lue et al (US Pat. App. No. 2007/0268753 A1).

By this response claims 7, 10 and 11 have been canceled thereby obviating the rejection with respect to these claims.

Rejection of the remaining claims will now be addressed by responding to the rejection of independent claims 1 and 9.

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations. (MPEP §2143.)

The Cited References Do Not Teach Or Suggest All Features Of The Claims

Applicant submits that the cited references, alone or in combination, do not teach or suggest all features of independent claims 1 and 9.

Claim 1

Claim 8 depends from claim 1. Claim 1 as amended provides: “an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack comprising a multi-layer charge storage layer including a substantially trap free bottom silicon oxynitride layer and a charge trapping top silicon oxynitride layer.”

With regard to these features, previously included in claim 7, the examiner states on page 3 of the office action that Wang “teaches that the charge storing layer can be formed of multi-layer of oxynitrides. Note paragraph [0024].”

Referring to paragraph [0024], Applicants submit that Wang does not teach or suggest a multi-layer charge storage layer including a substantially trap free bottom silicon oxynitride layer and a charge trapping top silicon oxynitride layer. Wang discloses the storage layer 24 preferably comprises aluminum nitride (AlN), and “in other embodiments, storage layer 24 may include other high-k dielectric materials including oxides, nitrides and oxynitrides, such as Si₃N₄, Al₂O₃, HfO₂, HfON, ZRON, and combinations thereof.” Thus, Wang does not teach or suggest a charge storage layer comprising silicon oxynitride layer at all, still less a charge storage layer comprising multiple silicon oxynitride layers.

Moreover, Wang does not teach or suggest a trap free bottom silicon oxynitride layer and charge trapping top silicon oxynitride layer. Rather, Wang discloses the charge storage layer “may also include nano crystal islands.” Note paragraph [0028]. Wang does not disclose the location or concentration of these ‘islands’ within the charge storage layer, however the description in paragraph [0028] of the “nano crystal islands being isolated by the dielectric materials,” and the dielectric materials being AlN or AlGa_N, and the band diagram of FIG. 7, is highly suggestive of their being located in the lower AlN or AlGa_N layers, and not the top Si₃N₄ layer. This is completely opposite the claimed features of “a trap free bottom silicon oxynitride layer and charge trapping top silicon oxynitride layer.”

Accordingly, Applicants submit that claim 1, as well as claims 2-5, 8 and 21 which are dependent therefrom, are patentable over the cited references.

Claim 9

Claim 9 as amended provides: “an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack including a multi-layer charge storage layer comprising multiple silicon oxynitride layers.”

For reasons given above with respect to claim 1, Applicants submit that Wang does not teach or suggest “a multi-layer charge storage layer comprising multiple silicon oxynitride layers.” In particular, Wang discloses the storage layer “may include other high-k dielectric materials including oxides, nitrides and oxynitrides, such as Si_3N_4 , Al_2O_3 , HfO_2 , HfON , ZrON , and combinations thereof.” Thus, Wang does not teach or suggest a charge storage layer comprising silicon oxynitride layer at all, still less a charge storage layer comprising multiple silicon oxynitride layers.

Accordingly, Applicants submit that claim 9, as well as claims 10-15 and 22 which are dependent therefrom, are patentable over the cited references.

Added Claims

Applicant further submits that added independent claim 23 includes features not taught or suggested by the cited references, and therefore are patentable over the cited references.

In particular, added independent claim 23 includes the features “a non-volatile memory transistor including an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack comprising a multi-layer charge storage layer including a silicon-rich, oxygen-lean top silicon oxynitride layer and a silicon-rich, oxygen-rich bottom silicon oxynitride layer.”

As noted above in connection with claims 1 and 9, Applicants submit that Wang does not teach or suggest a charge storage layer comprising a silicon oxynitride layer, still less a multi-layer charge storage layer including top and bottom silicon oxynitride layers.

Applicant further submits that none of the references cited by the examiner, alone or in combination, teach or suggest “a multi-layer charge storage layer including a silicon-rich, oxygen-lean top silicon oxynitride layer and a silicon-rich, oxygen-rich bottom silicon oxynitride layer.”

Accordingly, Applicants submit that claim 23, as well as claims 24-25 which are dependent therefrom, are patentable over the cited references.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record is relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, William E. Nuttle at (650) 207-3418.

It is believed no fees are required for filing this amendment. However, if necessary, please *charge any additional fees under 37 CFR §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application*, or apply any credits to our PTO deposit account number: 50-3781.

Respectfully submitted,
Igor Polishchuk

Dated: December 28, 2010

By: /William E. Nuttle, Reg. No. 42,943/
William E. Nuttle, Reg. No. 42,943
Attorney for the Applicant(s)

Electronic Acknowledgement Receipt	
EFS ID:	9127810
Application Number:	12152518
International Application Number:	
Confirmation Number:	5484
Title of Invention:	Memory transistor with multiple charge storing layers and a high work function gate electrode
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	William Edward Nuttle
Filer Authorized By:	
Attorney Docket Number:	PM07027
Receipt Date:	28-DEC-2010
Filing Date:	13-MAY-2008
Time Stamp:	18:47:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PM02007027_ROA.pdf	131172 6522e0f535e4cc9d2b52e91508c2cdc1eb62e1ed	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	9
Warnings:			
Information:			
Total Files Size (in bytes):		131172	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/152,518		Filing Date 05/13/2008		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	12/28/2010	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$ =		OR	X \$52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$ =		OR	X \$220=	0
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

Legal Instrument Examiner:
/MARY A. HOLMES/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM2007027	5484
60909 7590 09/29/2010 CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709			EXAMINER NGO, NGAN V	
			ART UNIT	PAPER NUMBER
			2893	
			MAIL DATE	DELIVERY MODE
			09/29/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/152,518	Applicant(s) POLISHCHUK ET AL.	
	Examiner Ngan Ngo	Art Unit 2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 July 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 16-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>20081121</u> . | 6) ☐ Other: _____ |

The election filed July 9, 2010 has been entered and made of record as paper no. 20100709.

Applicant's election without traverse of claims 1-15 in the reply filed on July 9, 2010 is acknowledged.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Zheng et al (US 6,912,163 B2).

Zheng discloses a non-volatile memory transistor comprising: an oxide-nitride-oxide (18) dielectric stack on a surface of a semiconductor substrate; and high work function gate electrode (34) formed over a surface of the ONO dielectric stack.

In re claim 2, the high work function gate electrode in Zheng comprises a doped polysilicon layer.

In re claim 3, the transistor in Zheng is a SONOS memory transistor.

In re claim 4, the doped polysilicon layer in Zheng comprises a P+ dopant to form an NMOS SONOS memory transistor. Note line 33, column 9 of Zheng.

Art Unit: 2893

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zheng et al (US 6,912,163 B2) in view of Wang et al (US 2007/0272916 A1) and Lue et al (US 2007/0268753 A1).

Zheng discloses all of the subject matter discussed above. Wang further teaches that the charge storing layer can be formed of multi-layer of oxynitrides. Note paragraph [0024]. Lue further discloses in figure 31 memory transistors and logic transistors including gate oxide and high work function gate electrodes formed on the same substrate. Therefore it would have been obvious to one of ordinary skill in the art to use the teachings of Zheng, Wang, and Lue to form the claimed device.

The other references are cited to show other structures pertinent to Applicant's disclosure.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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Art Unit: 2893

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

September 27, 2010

Notice of References Cited	Application/Control No. 12/152,518		Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.	
	Examiner Ngan Ngo		Art Unit 2893	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,912,163 B2	06-2005	Zheng et al.	365/185.29
*	B	US-2006/0131636 A1	06-2006	Jeon et al.	257/315
*	C	US-2007/0272916 A1	11-2007	Wang et al.	257/24
*	D	US-2007/0268753 A1	11-2007	Lue et al.	365/185.28
*	E	US-2007/0267687 A1	11-2007	Lue, Hang-Ting	257/321
*	F	US-2008/0009115 A1	01-2008	Willer et al.	438/257
*	G	US-7,737,488 B2	06-2010	Lai et al.	257/325
*	H	US-7,790,516 B2	09-2010	Willer et al.	438/129
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 12152518	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	06/03/2010	09/25/2010						
	1	÷	✓						
	2	÷	✓						
	3	÷	✓						
	4	÷	✓						
	5	÷	✓						
	6	÷	✓						
	7	÷	✓						
	8	÷	✓						
	9	÷	✓						
	10	÷	✓						
	11	÷	✓						
	12	÷	✓						
	13	÷	✓						
	14	÷	✓						
	15	÷	✓						
	16	÷	N						
	17	÷	N						
	18	÷	N						
	19	÷	N						
	20	÷	N						

Search Notes 	Application/Control No. 12152518	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner Ngan Ngo	Art Unit 2893

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
BRS search using EAST. See printout	9-24-10	NN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	158	high adj work adj function adj gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/23 23:43
L2	102	l1 and (ono or sonos)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/23 23:44
L3	97	l2 and oxynitride	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/23 23:56
L4	0	12/152518	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/09/23 23:57

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	1	12/152518	USPAT; UPAD	OR	ON	2010/09/23 23:57

9/ 24/ 10 12:02:46 AM

11/21/2008 02:08 6502403500

WILLIAM NUTTLE

12152518 - GAU: 2893

PAGE 03/03

PTO/SB/08 (10-08)

Approved for use through 11/30/2008. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1
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Complete if Known

Application Number	12/152,518
Filing Date	May 13, 2008
First Named Inventor	Igor Polishchuk, et al.
Art Unit	2812
Examiner Name	
Attorney Docket Number	PM2007027

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

Examiner Signature	/Ngan Ngo/	Date Considered	09/24/2010
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. *Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. * Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PAGE 3/3 * RCVD AT 11/21/2008 4:15:55 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-5/43 * DNIS:2738300 * CSID:6502403500 * DURATION (mm:ss):00:46

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /NN/

S/N 12/152,518

PATENT

Applicant: Igor Polishchuk

Serial No.: 12/152,518

Filed: May 13, 2008

Title: MEMORY TRANSISTOR WITH MULTIPLE
CHARGE STORING LAYERS AND A HIGH WORK
FUNCTION GATE ELECTRODE

Assignee: Cypress Semiconductor Corporation

Examiner: DILINH NGUYEN

Group Art Unit: 2893

Docket No.: PM2007027

Confirmation No.: 5484

RESPONSE TO RESTRICTION REQUIREMENT

MS Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

In response to the Restriction Requirement mailed June 9, 2010, Applicant submits the following.

IN THE CLAIMS

1. (Original) A non-volatile memory transistor comprising:
an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate;
and
high work function gate electrode formed over a surface of the ONO dielectric stack.
2. (Original) A memory transistor according to claim 1, wherein the high work function gate electrode comprises a doped polysilicon layer.
3. (Original) A memory transistor according to claim 2, wherein the semiconductor substrate comprises a silicon surface on which the ONO dielectric stack is formed to form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a SONOS memory transistor.
4. (Original) A memory transistor according to claim 3, wherein the doped polysilicon layer comprises a P+ dopant to form a NMOS SONOS memory transistor.
5. (Original) A memory transistor according to claim 4, wherein the P+ dopant comprises boron or difluoroborane (BF₂).
6. (Original) A memory transistor according to claim 1, wherein the ONO dielectric stack comprises a multi-layer charge storage layer.

7. (Original) A memory transistor according to claim 6, wherein the multi-layer charge storing layer comprises at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer.

8. (Original) A memory transistor according to claim 7, wherein the top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer, and the bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer.

9. (Original) A semiconductor device including a non-volatile memory transistor comprising:

an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack including a multi-layer charge storage layer; and

a high work function gate electrode formed over a surface of the ONO dielectric stack.

10. (Original) A semiconductor device according to claim 9, further comprising a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a high work function gate electrode.

11. (Original) A semiconductor device according to claim 10, wherein at least one of the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprises a doped polysilicon layer.

12. (Original) A semiconductor device according to claim 11, wherein the doped polysilicon layer comprises a P+ dopant.

13. (Original) A semiconductor device according to claim 12, wherein the P+ dopant comprises boron or difluoroborane (BF₂).

14. (Original) A semiconductor device according to claim 12, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a P+ doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

15. (Original) A semiconductor device according to claim 9, wherein the multi-layer charge storing layer comprises at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer.

16. (Withdrawn) A method of forming a semiconductor device comprising steps of:
forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer;

forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and

forming a high work function gate electrode on a surface of the ONO dielectric stack.

17. (Withdrawn) A method according to claim 16, wherein step of forming a high work function gate electrode on a surface of the ONO dielectric stack comprises the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack.

18. (Withdrawn) A method according to claim 17, wherein the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack further comprises the step of also forming the doped polysilicon layer on a surface of the oxide layer of the MOS logic transistor form a high work function gate electrode thereon.

19. (Withdrawn) A method according to claim 18, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, the doped polysilicon layer comprises a P+ dopant, and wherein the method further comprises the steps of patterning the he doped polysilicon layer, the ONO dielectric stack and the oxide layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

20. (Withdrawn) A method according to claim 16, wherein the step of forming an ONO dielectric stack including a multi-layer charge storage layer comprises the steps of forming

at least a substantially trap free bottom oxynitride layer followed by forming a charge trapping top oxynitride layer.

REMARKS

No claims have been added, amended or cancelled. As a result, claims 1-20 remain pending. Claims 16-20 have been withdrawn as non-elected. The Applicants reserve the right to reintroduce the non-elected claims in this Application, or in one or more divisional applications at a later date.

Restriction Requirement

In the Restriction Requirement mailed June 9, 2010, the Examiner has restricted the claims to one of the following inventions under 35 U.S.C. 121:

- I. Claims 1-15, drawn to a semiconductor device, classified in class 257, subclass 324.
- II. Claims 16-20, drawn to a method for making a semiconductor device, classified in class 438, subclass 216.

Applicant provisionally elects, without traverse, Group I, claims 1-15.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (408) 545-7194 to facilitate prosecution of this application.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Respectfully submitted,

Igor Polishchuk

By his Representatives,

Date July 9, 2010 By /Larry J. Johnson/
Larry J. Johnson
Reg. No. 56,861

Electronic Acknowledgement Receipt	
EFS ID:	7989528
Application Number:	12152518
International Application Number:	
Confirmation Number:	5484
Title of Invention:	Memory transistor with multiple charge storing layers and a high work function gate electrode
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	Andrew J. Bateman/Deborah Lucatorta
Filer Authorized By:	Andrew J. Bateman
Attorney Docket Number:	PM2007027
Receipt Date:	09-JUL-2010
Filing Date:	13-MAY-2008
Time Stamp:	20:36:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	PM2007027ResponsetoRestricti on07092010.pdf	182106 45835f46a3b1dad52b6982508e744bbdcd 21a2dd	no	8
Warnings:					
Information:					

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/152,518		Filing Date 05/13/2008		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	07/09/2010	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$ =		OR	X \$52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$ =		OR	X \$220=	0
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

Legal Instrument Examiner:
/ROZENIA HARMON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/152,518	05/13/2008	Igor Polishchuk	PM2007027	5484
60909 7590 06/09/2010 CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709			EXAMINER NGUYEN, DILINH P	
			ART UNIT	PAPER NUMBER
			2893	
			MAIL DATE	DELIVERY MODE
			06/09/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/152,518	Applicant(s) POLISHCHUK ET AL.	
	Examiner DILINH P. NGUYEN	Art Unit 2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 May 2008.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☐ Claim(s) _____ is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☒ Claim(s) 1-20 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date: _____ | 6) ☐ Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-15, drawn to a semiconductor device, classified in class 257, subclass 324.
 - II. Claims 16-20, drawn to a method for making a semiconductor device, classified in class 438, subclass 216.
2. The inventions are distinct, each from the other because of the following reasons:
3. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially process, such as a different product of claim 1 can be made without forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor logic transistor is to be formed.
4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

5. The examiner has required restriction between product and process claims.

Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

6. In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DILINH P. NGUYEN whose telephone number is (571)

Art Unit: 2893

272-1712. The examiner can normally be reached on 9:00 AM - 6:30 PM (Monday-Thursdays).

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571) 272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DLN
6/3/10

/Sue A. Purvis/
Supervisory Patent Examiner, Art Unit 2826



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 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5484

SERIAL NUMBER 12/152,518	FILING or 371(c) DATE 05/13/2008 RULE	CLASS 438	GROUP ART UNIT 2893	ATTORNEY DOCKET NO. PM2007027	
APPLICANTS Igor Polishchuk, Fremont, CA; Sagy Levy, Zichron Ya'akov, ISRAEL; Krishnaswamy Ramkumar, San Jose, CA; ** CONTINUING DATA ***** This appln claims benefit of 60/940,160 05/25/2007 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/11/2008					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /DILINH P NGUYEN/ Acknowledged Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 4	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709 UNITED STATES					
TITLE Memory transistor with multiple charge storing layers and a high work function gate electrode					
FILING FEE RECEIVED 1030	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

<i>Index of Claims</i> 	Application/Control No. 12152518	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner DILINH P NGUYEN	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	06/03/2010								
	1	÷								
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	3	÷								
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/152,518	05/13/2008	Igor Polishchuk	PM2007027

51885
WILLIAM NUTTLE
P.O. BOX 4240
FOSTER CITY, CA 94404

CONFIRMATION NO. 5484
POWER OF ATTORNEY NOTICE



Date Mailed: 01/22/2009

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/13/2009.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/mnguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/152,518	05/13/2008	Igor Polishchuk	PM2007027

CONFIRMATION NO. 5484

POA ACCEPTANCE LETTER

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709



Date Mailed: 01/22/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/13/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/mnguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

JAN. 13. 2009 9:54AM

Cypress Legal (408) 545-6911

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JAN 13 2009

CYPRESS SEMICONDUCTOR CORPORATION

FACSIMILE TRANSMITTAL SHEET

TO:	FROM:
EXAMINER	ANDREW J. BATEMAN,
	REG. NO. 45,573
FAX NUMBER:	DATE:
571-273-9300	JANUARY 13, 2009
COMPANY:	TOTAL NO. OF PAGES INCLUDING COVER:
U.S. PATENT AND TRADEMARK OFFICE	6
PHONE NUMBER:	SENDER'S REFERENCE NUMBER:
	PM2007027
RE:	USPTO APPLICATION NUMBER:
REVOCATION AND NEW POWER OF ATTORNEY	12/152,518

☐ URGENT ☐ FOR REVIEW ☐ PLEASE COMMENT ☐ PLEASE REPLY ☐ PLEASE RECYCLE

NOTES/COMMENTS:

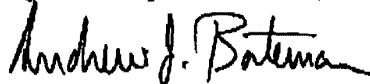
Application No.: 12/152,518
Filing Date: 05/13/2008
First Named Inventor: Igor Polishchuk
Art Unit: 2811
Confirmation No.: 5484
Examiner Name: N/A
Attorney Docket No.: PM2007027

Attached are the following documents being submitted in connection with the above-identified patent application:

REVOCATION AND NEW POWER OF ATTORNEY (1 page)
STATEMENT UNDER 37 CFR 3.73(b) (1 page)
COPY OF ASSIGNMENT (3 page)

If there are any questions regarding this submission, please contact Applicant's attorney, Andrew J. Bateman, by telephone at 408-943-6878.

Respectfully submitted,



Andrew J. Bateman
Attorney for Applicant
Reg. No. 45,573
Customer No. 60909

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PTO/SB/82 (01-08)

Approved for use through 12/31/2008. OMB 0851-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Application Number	12/152,618
	Filing Date	05/13/2008
	First Named Inventor	Igor Polishchuk
	Art Unit	2811
	Examiner Name	N/A
	Attorney Docket Number	PM2007027

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint the practitioners associated with the Customer Number:

60909

☒ Please change the correspondence address for the above-identified application to:☒ The address associated with
Customer Number:

60909

OR

☐ Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the:

☐ Applicant/Inventor.☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)**SIGNATURE of Applicant or Assignee of Record**

Signature

Name

Victoria Tidwell, Vice President of Legal Affairs and Associate General Counsel

Date

01/13/2009

Telephone

408-943-2979

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 36 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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NO. 3919 P. 3

JAN 13 2009

PTO/SB/88 (01-08)

Approved for use through 01/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Igor Polishchuk, et al.

Application No./Patent No.: 12/152,518 Filed/Issue Date: May 13, 2008

Entitled: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Cypress Semiconductor Corporation, a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest; or
2. ☐ an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is _____ %)

in the patent application/patent identified above by virtue of either:

A ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

(NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08)

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Andrew J. Bateman
Signature

January 13, 2009
Date

Andrew J. Bateman, Reg. No. 45,573
Printed or Typed Name

408-943-6878
Telephone Number

Attorney of Record
Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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NO. 3919 P. 4 20/03

JAN 13 2009

PATENT
PM2007027

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged, the undersigned, do hereby:

SELL, ASSIGN AND TRANSFER to CYPRESS SEMICONDUCTOR CORP. (the "Assignee"), having a place of business at 3901 North First Street, San Jose, CA, 95134 the entire right, title and interest for the United States and all foreign countries, in and to any and all improvements which are disclosed in the application for United States Letters Patent, which has been executed by the undersigned concurrently herewith, and is entitled "MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE", such application and all divisional, continuing, substitute, renewal, reissue and all other applications for patent which have been or shall be filed in the United States and all foreign countries on any of such improvements; all original and reissued patents which have been or shall be issued in the United States and all foreign countries on such improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and claim priority based on such application in the United States;

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to the Assignee;

WARRANT AND COVENANT that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been or will be made to others by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned;

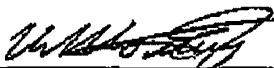
COVENANT that, when requested and at the expense of the Assignee, to carry out in good faith the intent and purpose of this assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all such improvements; execute all rightful oaths, declarations, assignments, powers of attorney and other papers; communicate to the Assignee all facts known to the undersigned relating to such improvements and the history thereof; and generally do everything possible which the Assignee shall consider desirable for securing, maintaining and enforcing proper patent protection for such improvements and for vesting title to such improvements in the Assignee; and

COVENANT AND AGREE that the above is and will be binding on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

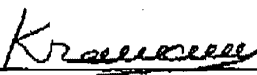
TO BE BINDING on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

PATENT
PM2007027

FURTHER COVENANT that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(Signature)  Date: 02/27/08
Igor Polishchuk

(Signature) _____ Date: _____
Sagy Levy

(Signature)  Date: 3/3/08
~~Krishnaswamy Ramkumar~~

Please direct all communication as follows:

Customer No. 51885
William E. Nuttle, Esq.
P.O. Box 4240
Foster City, CA 94404-0240
Ph: (650) 207-3418

JAN. 13. 2009 9:55AM

Cypress Legal (408) 545-6911

NO. 3919 P. 6

PATENT
PM2007027

FURTHER COVENANT that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(Signature) _____
Igor Polishchuk

Date: _____

(Signature) _____
Sagy Levy

Date: March 10-08

(Signature) _____
Krishnaswamy Rameshwar

Date: _____

Please direct all communication as follows:

Customer No. 51885
William E. Nuttle, Esq.
P.O. Box 4240
Foster City, CA 94404-0240
Ph: (650) 207-9418

Page 2 of 2

PAGE 6/11 * RCVD AT 1/13/2009 12:08:23 PM [Eastern Standard Time] * SVR:USPTO-EFXXF-6/34 * DNIS:2738300 * CSID: * DURATION (mm:ss):02:24

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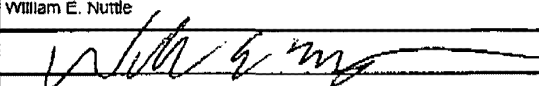
PTO/SB/21 (10-08)

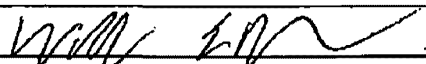
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	12/152,518
	Filing Date	May 13, 2008
	First Named Inventor	Igor Polishchuk
	Art Unit	2812
	Examiner Name	
	Attorney Docket Number	PM2007027
Total Number of Pages in This Submission		3

ENCLOSURES (Check all that apply)		
☐ Fee Transmittal Form ☐ Fee Attached ☐ Amendment/Reply ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☒ Information Disclosure Statement ☐ Certified Copy of Priority Document(s) ☐ Reply to Missing Parts/ Incomplete Application ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert to a Provisional Application ☐ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s) _____ ☐ Landscape Table on CD	☐ After Allowance Communication to TC ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☒ Other Enclosure(s) (please identify below): Form SB0008a
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm Name	William E. Nuttle	
Signature		
Printed name	William E. Nuttle	
Date	November 21, 2008	Reg. No. 42,943

CERTIFICATE OF TRANSMISSION/MAILING		
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:		
Signature		
Typed or printed name	William E. Nuttle	Date November 21, 2008

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Igor Polishchuk, et al. Serial No.: 12/152,518 Filed: May 13, 2008 Title: Memory Transistor With Multiple Charge Storing Layers And A High Work Function Gate Electrode	Examiner: Not Yet Assigned Art Unit: 2812 Atty. Dkt. No.: PM2007027
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Commissioner for Patents
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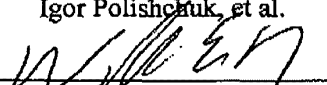
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This Information Disclosure Statement is being submitted under the section 37 CFR §1.97(b).

Consideration of the listed references and favorable action are respectfully solicited.

Respectfully submitted,
Igor Polishchuk, et al.

Dated: November 21, 2008By: 

William E. Nuttle, Reg. No. 42,943
Attorney for the Applicant(s)
P.O. Box 4240
Foster City, CA 94404

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Attorney Docket Number	PM2007027
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY,DOCKET,NO	TOT CLAIMS	IND CLAIMS
12/152,518	05/13/2008	2812	1030	PM2007027	20	3

CONFIRMATION NO. 5484

FILING RECEIPT



OC000000030937027

51885
WILLIAM NUTTLE
P.O. BOX 4240
FOSTER CITY, CA 94404

Date Mailed: 07/14/2008

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Applicant(s)

Igor Polishchuk, Fremont, CA;
Sagy Levy, Zichron Ya'akov, ISRAEL;
Krishnaswamy Ramkumar, San Jose, CA;

Assignment For Published Patent Application

Cypress Semiconductor Corporation

Power of Attorney: The patent practitioners associated with Customer Number 51885

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/940,160 05/25/2007

Foreign Applications

If Required, Foreign Filing License Granted: 07/11/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/152,518**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

Memory transistor with multiple charge storing layers and a high work function gate electrode

Preliminary Class

438

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01919
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PTO/SB/17 (10-07)

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Effective on 12/08/2004. Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818). FEE TRANSMITTAL For FY 2008		Complete if Known	
☐ Applicant claims small entity status. See 37 CFR 1.27		Application Number	
TOTAL AMOUNT OF PAYMENT (\$) 1070		Filing Date	May 13, 2008
		First Named Inventor	Igor Polishchuk
		Examiner Name	
		Art Unit	
		Attorney Docket No.	PM2007027

METHOD OF PAYMENT (check all that apply)

☒ Check
 ☐ Credit Card
 ☐ Money Order
 ☐ None
 ☐ Other (please identify): _____

☒ Deposit Account
 Deposit Account Number: 503467
 Deposit Account Name: William Nuttle, Esq.

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	310	155	510	255	210	105	1,030
Design	210	105	100	50	130	65	
Plant	210	105	310	155	160	80	
Reissue	310	155	510	255	620	310	
Provisional	210	105	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	210	105
Multiple dependent claims	370	185

Total Claims 20 - 20 or HP = 0 x 0 = 0
 HP = highest number of total claims paid for, if greater than 20.

Indep. Claims 3 - 3 or HP = 0 x 0 = 0
 HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
<u>20</u>	<u>0</u>	<u>0</u>	<u>0</u>	<u>0</u>

4. OTHER FEE(S)

	Fees Paid (\$)
Non-English Specification, \$130 fee (no small entity discount)	
Other (e.g., late filing surcharge): <u>Recordation of Assignment</u>	40

SUBMITTED BY		
Signature	Registration No. (Attorney/Agent) <u>42,943</u>	Telephone (650)207-3418
Name (Print/Type) <u>William E. Nuttle</u>	Date <u>May 13, 2008</u>	

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12/152518
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UTILITY
PATENT APPLICATION
TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	PM2007027
First Inventor	Igor Polishchuck
Title	Memory Transistor With Multiple Charge Storing Layers And A High Work Function Gate Electrode
Express Mail Label No.	EB 796954059 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ **Fee Transmittal Form** (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ **Applicant claims small entity status.**
See 37 CFR 1.27.
3. ☒ **Specification** [Total Pages 25]
Both the claims and abstract must start on a new page
(For information on the preferred arrangement, see MPEP 608.01(a))
4. ☒ **Drawing(s)** (35 U.S.C. 113) [Total Sheets 4]
5. **Oath or Declaration** [Total Sheets 6]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ A copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 18 completed)
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s)
name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or
Computer Program (Appendix)
☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
(if applicable, items a. - c. are required)
 - a. ☐ Computer Readable Form (CRF)
 - b. ☐ Specification Sequence Listing on:
 - i. ☐ CD-ROM or CD-R (2 copies); or
 - ii. ☐ Paper
 - c. ☐ Statements verifying identity of above copies

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ACCOMPANYING APPLICATION PARTS

9. ☒ **Assignment Papers** (cover sheet & document(s))
Name of Assignee Cypress Semiconductor Corporation
10. ☐ **37 CFR 3.73(b) Statement** (when there is an assignee) ☒ **Power of Attorney**
11. ☐ **English Translation Document** (if applicable)
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
☐ Copies of citations attached
13. ☐ **Preliminary Amendment**
14. ☒ **Return Receipt Postcard** (MPEP 503)
(Should be specifically itemized)
15. ☐ **Certified Copy of Priority Document(s)**
(if foreign priority is claimed)
16. ☒ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or equivalent.
17. ☐ **Other:** _____

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:

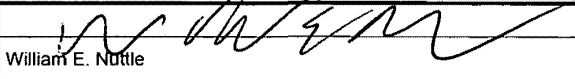
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Prior application information: Examiner _____ Art Unit: _____

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Signature		Date	May 13, 2008
Name (Print/Type)	William E. Nuttle	Registration No. (Attorney/Agent)	42,943

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NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)	First Named Inventor	Igor Polishchuk
	Title	Memory Transistor With Multiple Charge Storing Layers And A High Work Function Gate Electrode
	Attorney Docket No.	PM2007027

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).



 Signature

May 13, 2008

Date

William E. Nuttle

Typed or printed name

42,943

Registration Number, if applicable

(650)207-3418

Telephone Number

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

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If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

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**MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS
AND A HIGH WORK FUNCTION GATE ELECTRODE**

Inventors:

Igor Polishchuk

Sagy Levy

Krishnaswamy Ramkumar

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 60/940,160, entitled "SONOS Gate Stack With Multiple Oxynitride Layers And A High Workfunction Gate Electrode," filed May 25, 2007, which application is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

5 The present invention relates generally to semiconductor devices, and more particularly to integrated circuits including non-volatile semiconductor memories and methods of fabricating the same.

BACKGROUND OF THE INVENTION

10 Non-volatile semiconductor memories are devices that can be electrically erased and reprogrammed. One type of non-volatile memory that is widely used for general storage and transfer of data in and between computers and other electronic devices is flash memory, such as a split gate flash memory. A split gate flash memory transistor has an architecture similar to that of a conventional logic transistor, such as Metal-
15 Oxide-Semiconductor Field Effect Transistor (MOSFET), in that it also includes a control gate formed over a channel connecting a source and drain in a substrate. However, the memory transistor further includes a memory or charge trapping layer between the control gate and the channel and insulated from both by insulating or dielectric layers. A programming voltage applied to the control gate traps a charge on
20 the charge trapping layer, partially canceling or screening an electric field from the control gate, thereby changing a threshold voltage (V_T) of the transistor and

programming the memory cell. During read-out, this shift in V_T is sensed by the presence or absence of current flow through the channel with application of a predetermined read-out voltage. To erase the memory transistor, an erase voltage is applied to the control gate to restore, or reverse the shift in V_T .

5 An important measure of merit for flash memories is data retention time, which is the time for which the memory transistor can hold charge or remain programmed without the application of power. The charge stored or trapped in the charge trapping layer decreases over time due to leakage current through the insulating layers, thereby reducing the difference between a programmed threshold voltage (VTP) and an erased
10 threshold voltage (VTE) limiting data retention of the memory transistor.

 One problem with conventional memory transistors and methods of forming the same is that the charge trapping layer typically has poor or decreasing data retention over time, limiting the useful transistor lifetime. Referring to FIG. 1A, if the charge trapping layer is silicon (Si) rich there is a large, initial window or difference between
15 VTP, represented by graph or line **102**, and the VTE, represented by line **104**, but the window collapse very rapidly in retention mode to an end of life (EOL **106**) of less than about 1.E+07 seconds.

 Referring to FIG. 1B, if on the other hand the charge trapping layer is if a high quality nitride layer, that is one having a low stoichiometric concentration of Si, the rate
20 of collapse of the window or V_t slope in retention mode is reduced, but the initial program-erase window is also reduced. Moreover, the slope of V_t in retention mode is still appreciably steep and the leakage path is not sufficiently minimized to significantly improve data retention, thus EOL **106** is only moderately improved.

Another problem is that increasingly semiconductor memories combine logic transistors, such as MOSFET's, with memory transistors in integrated circuits (ICs) fabricated on a common substrate for embedded memory or System-On-Chip (SOC) applications. Many of the current processes for forming performance of memory transistors are incompatible with those used for fabricating logic transistors.

Accordingly, there is a need for memory transistors and methods of forming the same that provides improved data retention and increased transistor lifetime. It is further desirable that the methods of forming the memory device are compatible with those for forming logic elements in the same IC formed on a common substrate.

SUMMARY OF THE INVENTION

The present invention provides a solution to these and other problems, and offers further advantages over conventional memory transistors or devices and methods of forming the same.

In a first aspect, the present invention is directed to a non-volatile memory transistor including: (i) an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate; and (ii) high work function gate electrode formed over a surface of the ONO dielectric stack. Preferably, the high work function gate electrode comprises a doped polycrystalline silicon or polysilicon (poly) layer. More preferably, the doped polysilicon layer comprises a P⁺ dopant, such as boron or difluoroborane (BF₂), and the substrate comprises a silicon surface on which the ONO dielectric stack is formed to form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a NMOS SONOS memory transistor.

In certain embodiments, the ONO dielectric stack comprises a multi-layer charge storage layer including at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer. In one version of these embodiments, for example, the top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer, and the bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer.

In another aspect, the present invention is directed to a semiconductor device including both a non-volatile memory transistor and a metal oxide semiconductor (MOS) logic transistor and methods of forming the same. The memory transistor includes an ONO dielectric stack including a multi-layer charge storage layer formed on a surface of a semiconductor substrate, and a high work function gate electrode formed over a surface of the ONO dielectric stack. Preferably, the high work function gate electrode of the memory transistor comprises a doped polysilicon layer. More preferably, the MOS logic transistor also includes a high work function gate electrode formed over a gate oxide on the surface of the substrate.

In one embodiment, the high work function gate electrodes of the memory transistor and the MOS logic transistor comprise a P+ doped polysilicon layer deposited over the ONO stack and gate oxide on a silicon substrate to form an NMOS SONOS memory transistor and a P-type (PMOS) logic transistor. The multi-layer charge storing layer can include, for example, a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer.

In one embodiment, a method of forming such a semiconductor device comprises steps of: (i) forming an ONO dielectric stack on a surface of a semiconductor

substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer; (ii) forming an oxide layer on the surface of the substrate in a second region in which a MOS logic transistor is to be formed; and (iii) forming a high work function gate electrode on a surface of the ONO dielectric stack. Preferably, the step of forming a high work function gate electrode on a surface of the ONO dielectric stack comprises the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack. More preferably, the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack further comprises the step of also forming the doped polysilicon layer on a surface of the oxide layer of the MOS logic transistor form a high work function gate electrode thereon.

In certain embodiments, the semiconductor substrate includes a silicon surface over which the ONO dielectric stack is formed, and the step of forming a doped polysilicon layer comprises the step of forming a P+ doped polysilicon layer to form an NMOS SONOS memory transistor and a PMOS logic transistor. Generally, the polysilicon layer can be doped by ion implantation with boron or BF_2 , before or after patterning the polysilicon layer, the ONO dielectric stack and the oxide layer to form gate stacks of the memory transistor and the MOS logic transistor.

In other embodiments, the step of forming the ONO dielectric stack comprises the step of forming a multi-layer charge storage layer overlying a lower or tunnel oxide layer on the surface of the substrate, followed depositing or growing an upper or blocking oxide layer over the multi-layer charge storage layer. Preferably, the step of forming the multi-layer charge storage layer comprises the step of forming a

substantially trap free bottom oxynitride layer followed by forming a charge trapping top oxynitride layer overlying the trap free bottom oxynitride layer. More preferably, the bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer, and the top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer. Optionally, the charge trapping top oxynitride layer formed, for example, in a chemical vapor deposition (CVD) process using a process gas comprising Bis-TertiaryButylAminoSilane (BTBAS) selected to increase a concentration of carbon and thereby the number of traps therein.

BRIEF DESCRIPTION OF THE DRAWINGS

These and various other features and advantages of the present invention will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

FIG. 1A is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a large initial difference between programming and erase voltages but which loses charge quickly;

FIG. 1B is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a smaller initial difference between programming and erase voltages;

FIGs. 2A through 2D are partial cross-sectional side views of a semiconductor device illustrating a process flow for forming a semiconductor device including a logic

transistor and non-volatile memory transistor according to an embodiment of the present invention; and

FIG. 3 is a partial cross-sectional side view of a semiconductor device including a logic transistor and non-volatile memory transistor comprising high work function gate electrodes according to an embodiment of the present invention.

DETAILED DESCRIPTION

The present invention is directed generally to non-volatile memory transistor including a multi-layer charge storage layer and high work function gate electrode to increase data retention and/or to improve programming time and efficiency. The structure and method are particularly useful for embedded memory or System-On-Chip (SOC) applications in which a semiconductor device includes both a logic transistor and non-volatile memory transistor comprising high work function gate electrodes formed on a common substrate.

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures, and techniques are not shown in detail or are shown in block diagram form in order to avoid unnecessarily obscuring an understanding of this description.

Reference in the description to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase “in one embodiment” in various places in the specification do not

necessarily all refer to the same embodiment. The term “to couple” as used herein may include both to directly connect and to indirectly connect through one or more intervening components.

Briefly, a non-volatile memory transistor according to the present invention includes a high work function gate electrode formed over an oxide-nitride-oxide (ONO) dielectric stack. By high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased.

In certain preferred embodiments, the high work function gate electrode comprises a doped polycrystalline silicon or polysilicon (poly) layer, the fabrication of which can be readily integrated into standard complementary metal-oxide-semiconductor (CMOS) process flows, such as those used to fabricate metal-oxide-semiconductor (MOS) logic transistors, to enable fabrication of semiconductor memories or devices including both memory and logic transistors. More preferably, the same doped polysilicon layer can also be patterned to form a high work function gate electrode for the MOS logic transistor, thereby improving the performance of the logic transistor and increasing the efficiency of the fabrication process. Optionally, the ONO dielectric stack includes a multi-layer charge storage or charge trapping layer to further improve performance, and in particular data retention, of the memory transistor.

A semiconductor device including a non-volatile memory transistor comprising a high work function gate electrode and methods of forming the same will now be described in detail with reference to FIGs. 2A through 2D, which are partial cross-sectional side views of intermediate structures illustrating a process flow for forming a semiconductor device including both memory and logic transistors. For purposes of

clarity, many of the details of semiconductor fabrication that are widely known and are not relevant to the present invention have been omitted from the following description.

Referring to FIG. 2, fabrication of the semiconductor device begins with formation of an ONO dielectric stack **202** over a surface **204** of a wafer or substrate **206**. Generally, the ONO dielectric stack **202** includes a thin, lower oxide layer or tunneling oxide layer **208** that separates or electrically isolates a charge trapping or storage layer **210** from a channel region (not shown) of the memory transistor in the substrate **206**, and a top or blocking oxide layer **212**. Preferably, as noted above and as shown in FIGs. 2A-2D, the charge storage layer **210** is a multi-layer charge storage layer including at least a top, charge trapping oxynitride layer **210A** and a lower, substantially trap free oxynitride layer **210B**.

Generally, the substrate **206** may include any known silicon-based semiconductor material including silicon, silicon-germanium, silicon-on-insulator, or silicon-on-sapphire substrate. Alternatively, the substrate **206** may include a silicon layer formed on a non-silicon-based semiconductor material, such as gallium-arsenide, germanium, gallium-nitride, or aluminum-phosphide. Preferably, the substrate **206** is a doped or undoped silicon substrate.

The lower oxide layer or tunneling oxide layer **208** of the ONO dielectric stack **202** generally includes a relatively thin layer of silicon dioxide (SiO_2) of from about 15 angstrom ($\text{\AA}$) to about 22 $\text{\AA}$, and more preferably about 18 $\text{\AA}$. The tunneling oxide layer **208** can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using chemical vapor deposition (CVD). In a preferred embodiment, the tunnel oxide layer is formed or grown using a steam anneal. Generally,

the process includes a wet-oxidizing method in which the substrate **206** is placed in a deposition or processing chamber, heated to a temperature from about 700°C to about 850°C, and exposed to a wet vapor for a predetermined period of time selected based on a desired thickness of the finished tunneling oxide layer **208**. Exemplary process times are from about 5 to about 20 minutes. The oxidation can be performed at atmospheric or at low pressure.

In a preferred embodiment, the oxynitride layers **210A**, **210B**, of the multi-layer charge storage layer **210** are formed or deposited in separate steps utilizing different processes and process gases or source materials, and have an overall or combined thickness of from about 70 Å to about 150 Å, and more preferably about 100 Å. The lower, trap free oxynitride layer **210B** can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a process gas including a silicon source, such as silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane (SiH_2Cl_2), tetrachlorosilane (SiCl_4), a nitrogen source, such as nitrogen (N_2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas, such as oxygen (O_2) or N_2O . In one embodiment the trap free oxynitride layer **210B** is deposited in a low pressure CVD process using a process gas including dichlorosilane, NH_3 and N_2O , while maintaining the chamber at a pressure of from about 5 millitorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to

about 7:1, and can be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm).

The top, charge trapping oxynitride layer **210A** can be deposited over the bottom oxynitride layer **210B** in a CVD process using a process gas including Bis-TertiaryButylAminoSilane (BTBAS). It has been found that the use of BTBAS increases the number of deep traps formed in the oxynitride by increasing the carbon level in the charge trapping oxynitride layer **210A**. Moreover, these deep traps reduce charge losses due to thermal emission, thereby further improving data retention. More preferably, the process gas includes BTBAS and ammonia (NH₃) mixed at a predetermined ratio to provide a narrow band gap energy level in the oxynitride charge trapping layer. In particular, the process gas can include BTBAS and NH₃ mixed in a ratio of from about 7:1 to about 1:7. For example, in one embodiment the charge trapping oxynitride layer **210A** is deposited in a low pressure CVD process using BTBAS and ammonia NH₃ at a chamber pressure of from about 5 mT to about 500 mT, and at a substrate temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes.

It has been found that an oxynitride layer produced or deposited under the above conditions yields a trap-rich oxynitride layer **210A**, which improves the program and erase speed and increases of the initial difference (window) between program and erase voltages without compromising a charge loss rate of the memory transistor, thereby extending the operating life (EOL) of the device. Preferably, the charge trapping oxynitride layer **210A** has a charge trap density of at least about 1E10/cm², and more preferably from about 1E12/cm² to about 1E14/cm².

Alternatively, the charge trapping oxynitride layer **210A** can be deposited over the bottom oxynitride layer **210B** in a CVD process using a process gas including BTBAS and substantially not including ammonia (NH₃). In this alternative embodiment of the method, the step of depositing the top, charge trapping oxynitride layer **210A** is followed by a thermal annealing step in a nitrogen atmosphere including nitrous oxide (N₂O), NH₃, and/or nitrogen oxide (NO).

Preferably, the top, charge trapping oxynitride layer **210A** is deposited sequentially in the same CVD tool used to form the bottom, trap free oxynitride layer **210B**, substantially without breaking vacuum on the deposition chamber. More preferably, the charge trapping oxynitride layer **210A** is deposited substantially without altering the temperature to which the substrate **206** was heated during deposition of the trap free oxynitride layer **210B**.

A suitable thickness for the lower, trap free oxynitride layer **210B** has been found to be from about 10 Å to about 80 Å, and a ratio of thicknesses between the bottom layer and the top, charge trapping oxynitride layer has been found to be from about 1:6 to about 6:1, and more preferably at least about 1:4.

The top oxide layer **212** of the ONO dielectric stack **202** includes a relatively thick layer of SiO₂ of from about 20 Å to about 70 Å, and more preferably about 45 Å. The top oxide layer **212** can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using CVD. In a preferred embodiment, the top oxide layer **212** is a high-temperature-oxide (HTO) deposited using CVD process. Generally, the deposition process includes exposing the substrate **308** to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-

containing gas, such as O₂ or N₂O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

Preferably, the top oxide layer **212** is deposited sequentially in the same tool used to form the oxynitride layers **210A**, **210B**. More preferably, the oxynitride layers **210A**, **210B**, and the top oxide layer **212** are formed or deposited in the same tool used to grow the tunneling oxide layer **208**. Suitable tools include, for example, an ONO AVP, commercially available from AVIZA technology of Scotts Valley, California.

Referring to FIG. 2B, in those embodiments in which the semiconductor device is to further include a logic transistor, such as a MOS logic transistor, formed on the surface of the same substrate the ONO dielectric stack **202** is removed from a region or area of the surface **204** in which the logic transistor is to be formed, and an oxide layer **214** the formed thereon.

Generally, the ONO dielectric stack **202** is removed from the desired region or area of the surface **204** using standard photolithographic and oxide etch techniques. For example, in one embodiment a patterned mask layer (not shown) is formed from a photo-resist deposited on the ONO dielectric stack **202**, and the exposed region etched or removed using a low pressure radiofrequency (RF) coupled or generated plasma comprising fluorinated hydrocarbon and/or fluorinated carbon compounds, such as C₂H₂F₄ commonly referred to as Freon[®]. Generally, the processing gas further includes argon (Ar) and nitrogen (N₂) at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

The oxide layer **214** of the logic transistor can include a layer of SiO₂ having a thickness of from about 30 to about 70 Å, and can be thermally grown or deposited using CVD. In one embodiment, the oxide layer **214** is thermally grown using a steam oxidation process, for example, by maintaining the substrate **206** in a steam atmosphere at a temperature of from about 650°C to about 850°C for a period of from about 10 minutes to about 120 minutes.

Next, a doped polysilicon layer is formed on a surface of the ONO dielectric stack **202** and, preferably, the oxide layer **214** of the logic transistor. More preferably, the substrate **206** is a silicon substrate or has a silicon surface on which the ONO dielectric stack is formed to form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a SONOS memory transistor.

Referring to FIG. 2C, forming of the doped polysilicon layer begins with the deposition of a conformal polysilicon layer **216** having a thickness of from about 200 Å to about 2000 Å over the ONO dielectric stack **202** and the oxide layer **214**. The polysilicon layer **216** can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a silicon source or precursor. In one embodiment the polysilicon layer **216** is deposited in a low pressure CVD process using a silicon containing process gas, such as silane or dichlorosilane, and N₂, while maintaining the substrate **206** in a chamber at a pressure of from about 5 to 500 mT, and at a temperature of from about 600°C to about 1000°C for a period of from about 20 minutes to about 100 minutes to a substantially undoped polysilicon layer. The polysilicon layer **216** can be formed or grown directly as a doped polysilicon layer

through the addition of gases such as phosphine, arsine, diborane or difluoroborane (BF₂) to the CVD chamber during the low pressure CVD process.

In one embodiment, the polysilicon layer **216** is doped following the growth or formation in the LPCVD process using ion implantation process. For example, the polysilicon layer **216** can be doped by implanting boron (B⁺) or BF₂ ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm⁻² to about 1e16 cm⁻² to form an N-type (NMOS) SONOS memory transistor and, preferably, a P-type (PMOS) logic transistor having high work function gate electrodes. More preferably, the polysilicon layer **216** is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV.

Alternatively, the polysilicon layer **216** can be doped by ion implantation after patterning or etching the polysilicon layer and the underlying dielectric layers. It will be appreciated that this embodiment includes additional masking steps to protect exposed areas of the substrate **206** surface **204** and/or the dielectric layers from receiving undesired doping. However, generally such a masking step is included in existing process flows regardless of whether the implantation occurs before or after patterning.

Referring to FIG. 2D, the polysilicon layer **216** and the underlying dielectric stack **202** and oxide layer **214** are patterned or etched to form high work function gate electrodes **218** of the memory transistor **220** and logic transistor **222**. In one embodiment polysilicon layer **216** can be etched or patterned using a plasma comprising hydrobromic acid (HBr), chlorine (CL₂) and/or oxygen (O₂) at a pressure of about 25 mTorr, and a power of about 450 W. The oxide layers **208**, **212**, **214**, and oxynitride

layers **210A**, **210B**, can be etched using standard photolithographic and oxide etch techniques as described. For example, in one embodiment the patterned polysilicon layer **216** is used as a mask, and the exposed oxide layers **208**, **212**, **214**, and oxynitride layers **210A**, **210B**, etched or removed using low pressure RF plasma. Generally, the plasma is formed from a processing gas comprising a fluorinated hydrocarbon and/or fluorinated carbon compounds, and further including Ar and N₂ at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

Finally, the substrate is thermal annealed with a single or multiple annealing steps at a temperature of from about 800 °C to about 1050 °C for a time of from about 1 second to about 5 minutes to drive in ions implanted in the polysilicon layer **216**, and to repair damage to the crystal structure of the polysilicon layer caused by ion implantation. Alternatively, advanced annealing techniques, such as flash and laser, can be employed with temperatures as high as 1350 °C and anneal times as low as 1 millisecond.

A partial cross-sectional side view of a semiconductor device **300** including a logic transistor **302** and non-volatile memory transistor **304** comprising high work function gate electrodes according to an embodiment of the present invention is shown in FIG. 3. Referring to FIG. 3, the memory transistor **304** is formed on a silicon substrate **306** and comprises a high work function gate electrode **308** formed from a doped polysilicon layer overlying a dielectric stack **310**. The dielectric stack **310** overlies and controls current through a channel region **312** separating heavily doped source and drain (S/D) regions **314**. Preferably, the dielectric stack **310** includes a

tunnel oxide **316**, a multi-layer charge storage layer **318A**, **318B**, and a top or blocking oxide layer **320**. More preferably, the multi-layer charge storage layer **318A**, **318B**, includes at least a top, charge trapping oxynitride layer **318A** and a lower, substantially trap free oxynitride layer **318B**. Optionally, as shown in FIG. 3, the memory transistor **304** further includes one or more sidewall spacers **322** surrounding the gate stack to electrically insulate it from contacts (not shown) to the S/D regions **320** and from other transistors in the semiconductor device formed on the substrate **306**.

The logic transistor **302** comprises a gate electrode **324** overlying an oxide layer **326** formed over a channel region **328** separating heavily doped source and drain regions **330**, and, optionally, can include one or more sidewall spacers **332** surrounding the gate electrically insulate it from contacts (not shown) to the S/D regions. Preferably, as shown in FIG. 3, the gate electrode **324** of the logic transistor **302** also comprises a high work function gate electrode formed from a doped polysilicon layer.

Generally, the semiconductor device **300** further includes a number of isolation structures **334**, such as a local oxidation of silicon (LOCOS) region or structure, a field oxidation region or structure (FOX), or a shallow trench isolation (STI) structure to electrically isolate individual transistors formed on the substrate **306** from one another.

The foregoing description of specific embodiments and examples of the invention have been presented for the purpose of illustration and description, and although the invention has been described and illustrated by certain of the preceding examples, it is not to be construed as being limited thereby. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications, improvements and variations within the scope of the invention are

possible in light of the above teaching. It is intended that the scope of the invention encompass the generic area as herein disclosed, and by the claims appended hereto and their equivalents. The scope of the present invention is defined by the claims, which includes known equivalents and unforeseeable equivalents at the time of filing of this application.

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IN THE CLAIMS

WHAT IS CLAIMED IS:

1. A non-volatile memory transistor comprising:
an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor
5 substrate; and
high work function gate electrode formed over a surface of the ONO dielectric stack.
2. A memory transistor according to claim 1, wherein the high work
10 function gate electrode comprises a doped polysilicon layer.
3. A memory transistor according to claim 2, wherein the semiconductor
substrate comprises a silicon surface on which the ONO dielectric stack is formed to
form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a SONOS memory
15 transistor.
4. A memory transistor according to claim 3, wherein the doped polysilicon
layer comprises a P+ dopant to form a NMOS SONOS memory transistor.
- 20 5. A memory transistor according to claim 4, wherein the P+ dopant
comprises boron or difluoroborane (BF₂).
6. A memory transistor according to claim 1, wherein the ONO dielectric
stack comprises a multi-layer charge storage layer.

7. A memory transistor according to claim 6, wherein the multi-layer charge storing layer comprises at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer.

5

8. A memory transistor according to claim 7, wherein the top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer, and the bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer.

10

9. A semiconductor device including a non-volatile memory transistor comprising:

an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack including a multi-layer charge storage layer; and

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a high work function gate electrode formed over a surface of the ONO dielectric stack.

10. A semiconductor device according to claim 9, further comprising a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a high work function gate electrode.

20

11. A semiconductor device according to claim 10, wherein at least one of the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprises a doped polysilicon layer.

5 12. A semiconductor device according to claim 11, wherein the doped polysilicon layer comprises a P+ dopant.

13. A semiconductor device according to claim 12, wherein the P+ dopant comprises boron or difluoroborane (BF₂).

10 14. A semiconductor device according to claim 12, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a P+
15 doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

20 15. A semiconductor device according to claim 9, wherein the multi-layer charge storing layer comprises at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer.

16. A method of forming a semiconductor device comprising steps of:

forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer;

forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and

forming a high work function gate electrode on a surface of the ONO dielectric stack.

17. A method according to claim 16, wherein step of forming a high work function gate electrode on a surface of the ONO dielectric stack comprises the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack.

18. A method according to claim 17, wherein the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack further comprises the step of also forming the doped polysilicon layer on a surface of the oxide layer of the MOS logic transistor form a high work function gate electrode thereon.

19. A method according to claim 18, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, the doped polysilicon layer comprises a P+ dopant, and wherein the method further comprises the steps of patterning the he doped polysilicon layer, the ONO dielectric stack and the

oxide layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

5 20. A method according to claim 16, wherein the step of forming an ONO dielectric stack including a multi-layer charge storage layer comprises the steps of forming at least a substantially trap free bottom oxynitride layer followed by forming a charge trapping top oxynitride layer.

ABSTRACT OF THE DISCLOSURE

Semiconductor devices including non-volatile memory transistors and methods of fabricating the same to improve performance thereof are provided. In one embodiment, the memory transistor comprises an oxide-nitride-oxide (ONO) stack on a surface of a semiconductor substrate, and a high work function gate electrode formed over a surface of the ONO stack. Preferably, the gate electrode comprises a doped polysilicon layer, and the ONO stack comprises multi-layer charge storing layer including at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer. More preferably, the device also includes a metal oxide semiconductor (MOS) logic transistor formed on the same substrate, the logic transistor including a gate oxide and a high work function gate electrode. In certain embodiments, the dopant is a P+ dopant and the memory transistor comprises N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) transistor while the logic transistor a P-type (PMOS) transistor. Other embodiments are also disclosed.

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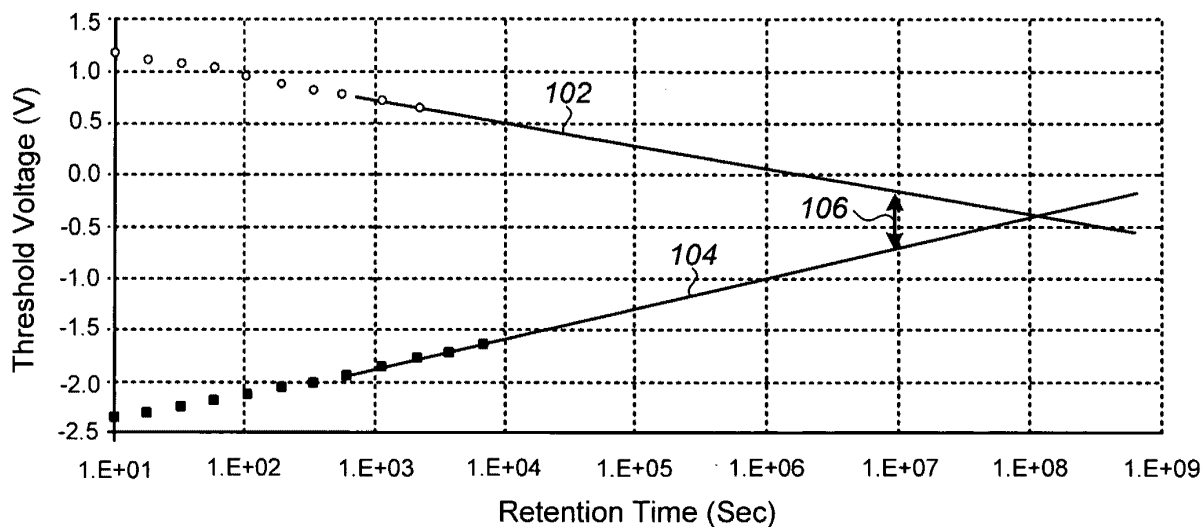


FIG. 1A

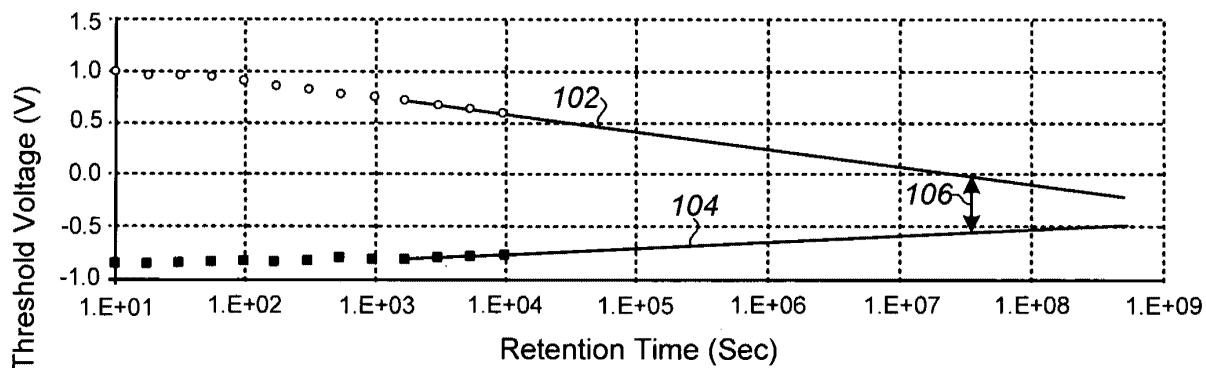


FIG. 1B

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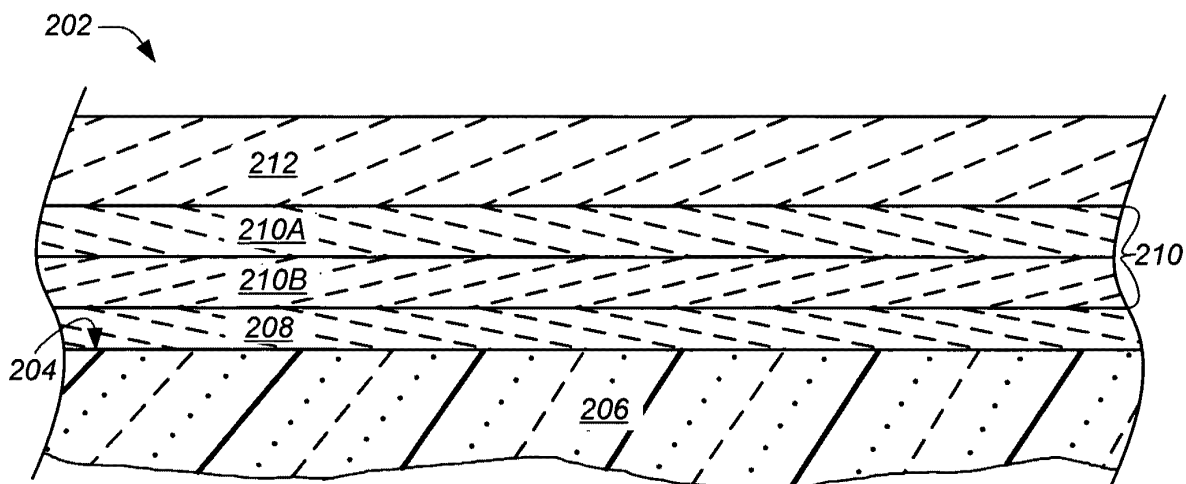


FIG. 2A

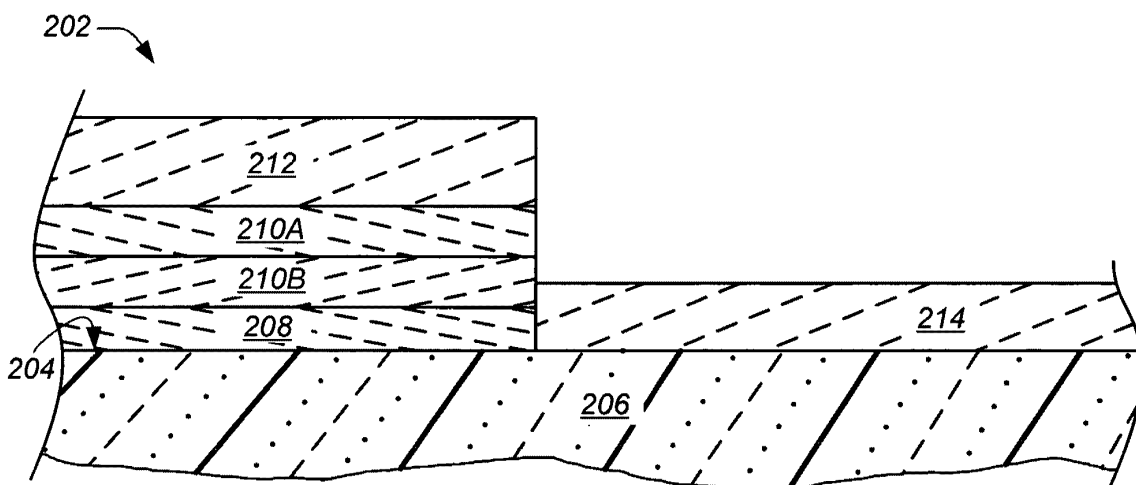


FIG. 2B

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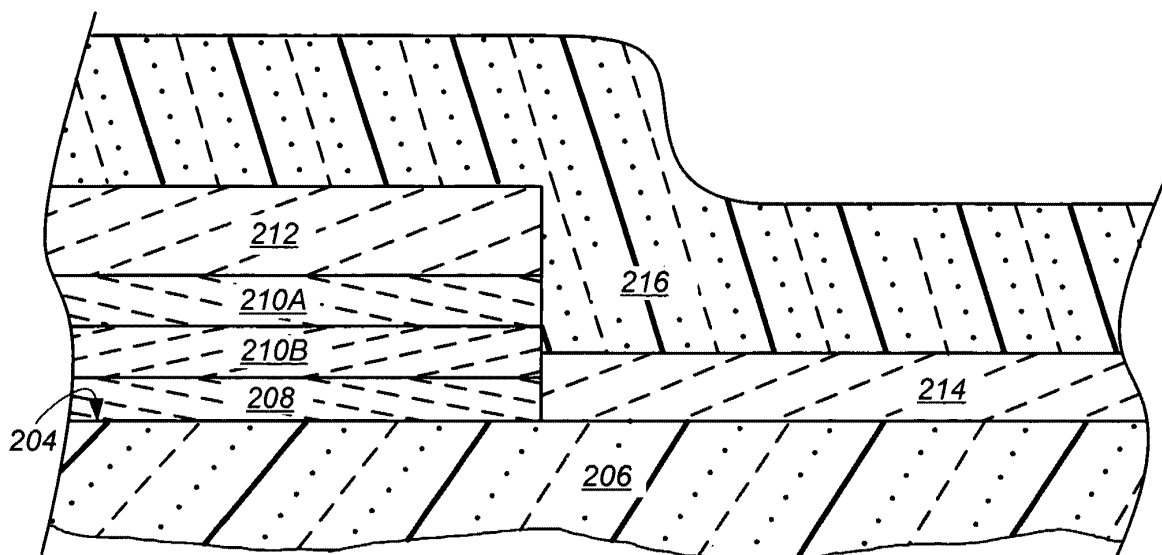


FIG. 2C

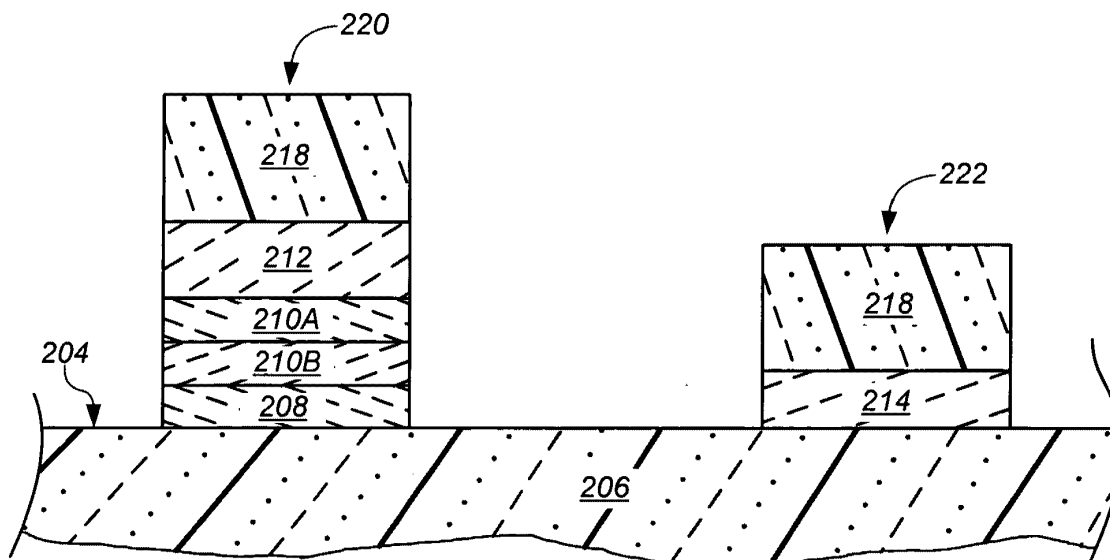


FIG. 2D

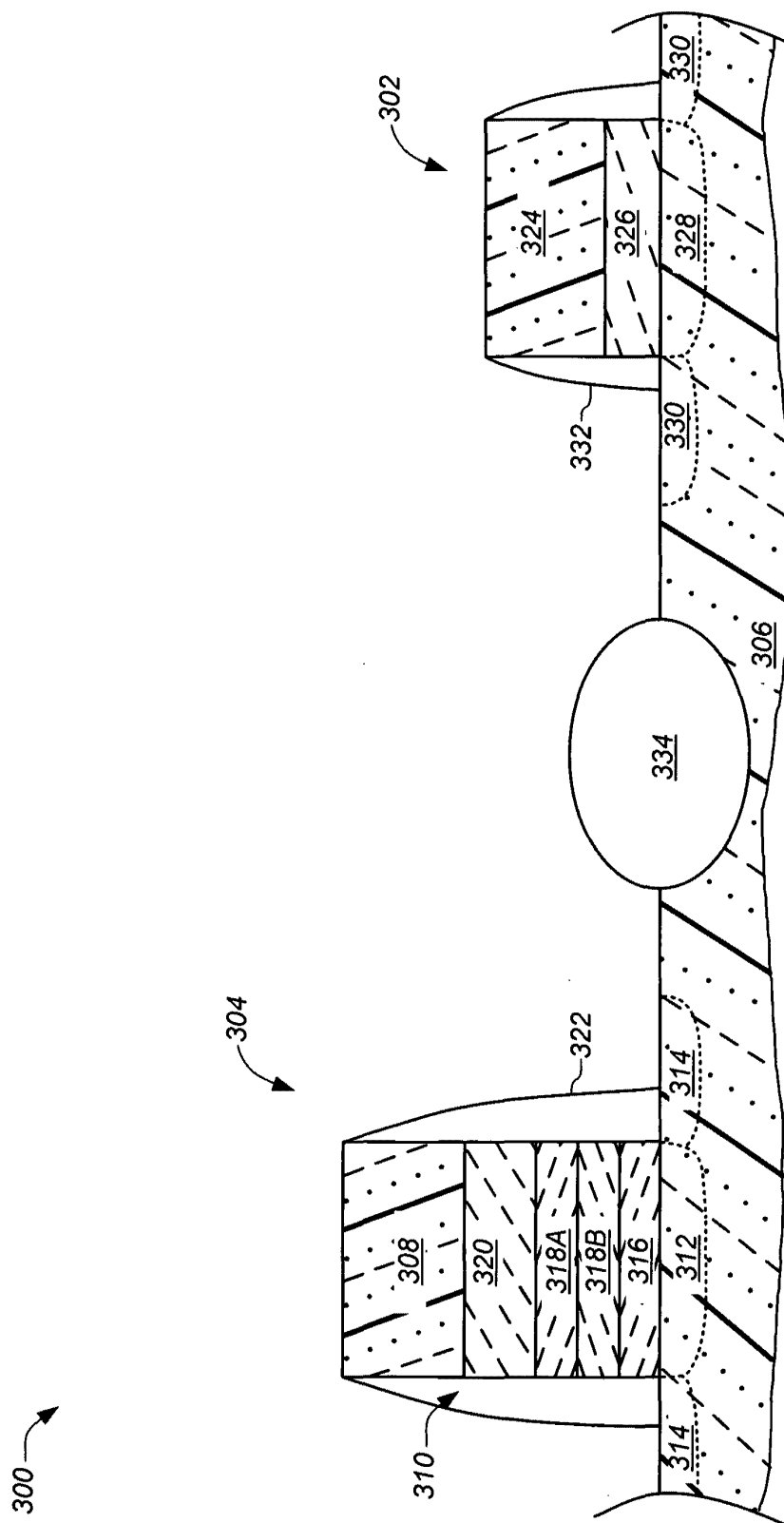


FIG. 3

PTO/SB/01 (07-07)

Approved for use through 06/30/2010, OMB 0651-0032

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**DECLARATION FOR UTILITY OR
DESIGN
PATENT APPLICATION
(37 CFR 1.63)**



Declaration
Submitted
With Initial
Filing

OR



Declaration
Submitted after Initial
Filing (surcharge
(37 CFR 1.16 (e))
required)

Attorney Docket
Number

PM2007027

First Named Inventor

Igor Polishchuk

COMPLETE IF KNOWN

Application Number

Filing Date

5/13/06

Art Unit

Examiner Name

I hereby declare that:

Each inventor's residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH
WORK FUNCTION GATE ELECTRODE**

(Title of the invention)

the specification of which



is attached hereto

OR



was filed on (MM/DD/YYYY)

as United States Application Number or PCT International

Application Number

and was amended on (MM/DD/YYYY)

(If applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐



Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 1 of 2]

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance completing the form, call 1-800-PTO-9199 and select option 2.

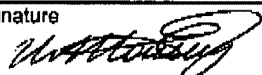
PTO/SB/01 (07-07)

Approved for use through 06/30/2010. OMB 0851-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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DECLARATION --Utility or Design Patent Application

Direct all correspondence to:		☒ The address associated with Customer Number:	51885		OR	☐ Correspondence address below
Name						
Address						
City			State		ZIP	
Country		Telephone		Email		
<p align="center">WARNING:</p> <p>Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.</p> <p>I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.</p>						
NAME OF SOLE OR FIRST INVENTOR:			☐ A petition has been filed for this unsigned inventor			
Given Name (first and middle (if any))			Family Name or Surname			
Igor			Polishchuk			
Inventor's Signature					Date	
					2/27/08	
Residence: City	State	Country	Citizenship			
Fremont	CA	U.S.A.	U.S.A.			
Mailing Address						
43355 Paseo Padre Pkwy.						
City	State	Zip	Country			
Fremont	CA	94539	U.S.A.			
☒ Additional inventors or a legal representative are being named on the 1 supplemental sheet(s) PTO/SB/02A or 02LR attached hereto.						

[Page 2 of 2]

PTO/SB/02A (07-07)

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DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet Page <u>1</u> of <u>1</u>
--------------------	--

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Sagv		Levy	
Inventor's Signature		Date	
Zichron Ya'aqov Residence: City	N/A State	Israel Country	Israel Citizenship
44 Yigal-Alon Street Mailing Address			
Zichron Ya'aqov City	N/A State	30900 Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Krishnaswamy		Ramkumar	
Inventor's Signature <i>Kraus</i>		Date <u>3/3/08</u>	
San Jose Residence: City	CA State	U.S.A. Country	U.S.A. Citizenship
1193 Lynbrook Way Mailing Address			
San Jose City	CA State	95129 Zip	U.S.A. Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)	Attorney Docket Number	PM2007027
	First Named Inventor	Igor Polishchuk
	COMPLETE IF KNOWN	
	Application Number	
	Filing Date	5/13/06
	Art Unit	
☒ Declaration Submitted With Initial Filing	OR	☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)
Examiner Name		

I hereby declare that:

Each inventor's residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH
WORK FUNCTION GATE ELECTRODE

(Title of the Invention)

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) [] as United States Application Number or PCT International

Application Number [] and was amended on (MM/DD/YYYY) [] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 1 of 2]

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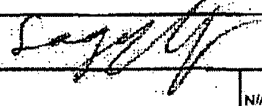
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DECLARATION — Utility or Design Patent Application

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Name				
Address				
City		State	ZIP	
Country	Telephone		Email	
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NAME OF SOLE OR FIRST INVENTOR:		☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))		Family Name or Surname		
Igor		Polishchuk		
Inventor's Signature			Date	
Residence: City	State	Country	Citizenship	
Fremont	CA	U.S.A.	U.S.A.	
Mailing Address 43355 Paseo Padre Pkwy.				
City	State	Zip	Country	
Fremont.	CA	94539	U.S.A.	
☒ Additional inventors or a legal representative are being named on the 1 supplemental sheet(s) PTO/SB/02A or 02LR attached hereto.				

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DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet <div style="text-align: right;">Page <u>1</u> of <u>1</u></div>
--------------------	---

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Sagv		Levy	
Inventor's Signature 		Date <u>03/10/08</u>	
Zichron Ya'akov Residence: City	N/A State	Israel Country	Israel Citizenship
44 Yigal-Alon Street, Mailing Address			
Zichron Ya'akov City	N/A State	30900 Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Krishnaswamy		Ramkumar	
Inventor's Signature		Date	
San Jose Residence: City	CA State	U.S.A. Country	U.S.A. Citizenship
1193 Lynbrook Way Mailing Address			
San Jose City	CA State	95129 Zip	U.S.A. Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

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PTO/SB/81 (01-06)

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**POWER OF ATTORNEY
and
CORRESPONDENCE ADDRESS
INDICATION FORM**

Application Number	not yet known
Filing Date	5/13/08
First Named Inventor	Igor Polishchuk
Title	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Art Unit	unknown
Examiner Name	unknown
Attorney Docket Number	PM2007027

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint:

☒ Practitioners associated with the Customer
Number:

51885

OR

☐ Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or
Individual Name

Address

City

State

ZIP

Country

Telephone

Fax

I am the:

☒ Applicant/Inventor.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.

Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature	<i>Igor Polishchuk</i>	Date	02/27/08
Name	Igor Polishchuk	Telephone	408 545 7199
Title and Company	Cypress Semiconductor		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ *Total of 3 forms are submitted.

This collection of information is required by 37 CFR 1.31 and 1.33. This information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS, SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22313-1480.

PTO/SB/81 (01-08)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION FORM	Application Number	not yet known
	Filing Date	5-13-08
	First Named Inventor	Igor Polishchuk
	Title	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
	Art Unit	unknown
	Examiner Name	unknown
	Attorney Docket Number	PM2007027

I hereby revoke all previous powers of attorney given in the above-identified application.

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Number: 51885

OR

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☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name			
Address			
City	State	ZIP	
Country			
Telephone	Fax		

I am the:

☒ Applicant/Inventor.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/06)

SIGNATURE of Applicant or Assignee of Record

Signature	Date
<i>Krishnaswamy Ramkumar</i>	3/3/08
Name	Telephone
Krishnaswamy Ramkumar	
Title and Company	
Sr. Member of Technical Staff: cypress semiconductor	

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ *Total of 3 forms are submitted.

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**POWER OF ATTORNEY
and
CORRESPONDENCE ADDRESS
INDICATION FORM**

Application Number	not yet known
Filing Date	5-13-06
First Named Inventor	Igor Polishchuk
Title	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Art Unit	unknown
Examiner Name	unknown
Attorney Docket Number	PM2007027

I hereby revoke all previous powers of attorney given in the above-identified application.

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Number:

51885

OR

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as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States
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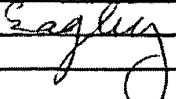
I am the:

☒ Applicant/Inventor.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.

Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature		Date	March-10-08
Name	Sagy Levy	Telephone	
Title and Company			

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more
than one signature is required. see below.

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PATENT APPLICATION SERIAL NO. _____

**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET**

05/19/2008 SSITHIB1 00000017 12152518

02 FC:1011	310.00	OP
03 FC:1111	510.00	OP
04 FC:1311	210.00	OP

PTO-1556
(5/87)

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number

12152512

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	0
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	0
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

RATE (\$)	FEE (\$)
N/A	\$155
N/A	\$255
N/A	\$105
X \$25 =	
X \$105 =	
\$130	
\$185	
TOTAL	

RATE (\$)	FEE (\$)
N/A	\$310
N/A	\$510
N/A	\$210
X \$50 =	
X \$210 =	
\$260	
\$370	
TOTAL	1030

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDI- TIONAL FEE (\$)
X \$25 =	
X \$105 =	
\$185	
TOTAL ADD'L FEE	

RATE (\$)	ADDI- TIONAL FEE (\$)
X \$50 =	
X \$210 =	
\$370	
TOTAL ADD'L FEE	

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDI- TIONAL FEE (\$)
X \$25 =	
X \$105 =	
\$185	
TOTAL ADD'L FEE	

RATE (\$)	ADDI- TIONAL FEE (\$)
X \$50 =	
X \$210 =	
\$370	
TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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01919
051308

PTO/SB/17 (10-07)

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Effective on 12/08/2004. Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818). FEE TRANSMITTAL For FY 2008		Complete if Known	
☐ Applicant claims small entity status. See 37 CFR 1.27		Application Number	
TOTAL AMOUNT OF PAYMENT (\$) 1070		Filing Date	May 13, 2008
		First Named Inventor	Igor Polishchuk
		Examiner Name	
		Art Unit	
		Attorney Docket No.	PM2007027

METHOD OF PAYMENT (check all that apply)

☒ Check
 ☐ Credit Card
 ☐ Money Order
 ☐ None
 ☐ Other (please identify): _____

☒ Deposit Account
 Deposit Account Number: 503467
 Deposit Account Name: William Nuttle, Esq.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
 ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17
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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	310	155	510	255	210	105	1,030
Design	210	105	100	50	130	65	
Plant	210	105	310	155	160	80	
Reissue	310	155	510	255	620	310	
Provisional	210	105	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	210	105
Multiple dependent claims	370	185

Total Claims 20 - 20 or HP = 0 x _____ = 0
 HP = highest number of total claims paid for, if greater than 20.

Indep. Claims 3 - 3 or HP = 0 x _____ = 0
 HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
_____	_____	_____	_____	_____

4. OTHER FEE(S)

	Fees Paid (\$)
Non-English Specification, \$130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Recordation of Assignment	40

SUBMITTED BY		
Signature	Registration No. (Attorney/Agent) 42,943	Telephone (650)207-3418
Name (Print/Type) William E. Nuttle		Date May 13, 2008

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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U.S. PTO
12/152518
05/13/2008

PTO/SB/05 (06-07)

Approved for use through 06/30/2010. OMB 0651-0032
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01919 U.S. PTO

UTILITY
PATENT APPLICATION
TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	PM2007027
First Inventor	Igor Polishchuck
Title	Memory Transistor With Multiple Charge Storing Layers And A High Work Function Gate Electrode
Express Mail Label No.	EB 796954059 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ **Fee Transmittal Form** (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ **Applicant claims small entity status.**
See 37 CFR 1.27.
3. ☒ **Specification** [Total Pages 25]
Both the claims and abstract must start on a new page
(For information on the preferred arrangement, see MPEP 608.01(a))
4. ☒ **Drawing(s)** (35 U.S.C. 113) [Total Sheets 4]
5. **Oath or Declaration** [Total Sheets 6]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ A copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 18 completed)
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s)
name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or
Computer Program (Appendix)
☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
(if applicable, items a. - c. are required)
 - a. ☐ Computer Readable Form (CRF)
 - b. ☐ Specification Sequence Listing on:
 - i. ☐ CD-ROM or CD-R (2 copies); or
 - ii. ☐ Paper
 - c. ☐ Statements verifying identity of above copies

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

ACCOMPANYING APPLICATION PARTS

9. ☒ **Assignment Papers** (cover sheet & document(s))
Name of Assignee Cypress Semiconductor Corporation
10. ☐ **37 CFR 3.73(b) Statement** (when there is an assignee) ☒ **Power of Attorney**
11. ☐ **English Translation Document** (if applicable)
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
☐ Copies of citations attached
13. ☐ **Preliminary Amendment**
14. ☒ **Return Receipt Postcard** (MPEP 503)
(Should be specifically itemized)
15. ☐ **Certified Copy of Priority Document(s)**
(if foreign priority is claimed)
16. ☒ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or equivalent.
17. ☐ **Other:** _____

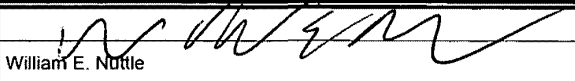
18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____
Prior application information: Examiner _____ Art Unit: _____

19. CORRESPONDENCE ADDRESS

☒ The address associated with Customer Number: 51885 OR ☐ Correspondence address below

Name			
Address			
City	State	Zip Code	
Country	Telephone	Email	

Signature		Date	May 13, 2008
Name (Print/Type)	William E. Nuttle	Registration No. (Attorney/Agent)	42,943

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