



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	10/14/2014	8859374	PM07027D1	3343

60909 7590 09/24/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 336 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

IGOR POLISHCHUK, Fremont, CA;
Sagy LEVY, Zichron Ya'akov, ISRAEL;
Krishnaswamy RAMKUMAR, San Jose, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

60909 7590 08/26/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	11/26/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	438-287000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Cypress Semiconductor Corporation

San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 503781 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Larry J. Johnson/

Date 09/03/2014

Typed or printed name Larry J. Johnson

Registration No. 56,861

Electronic Patent Application Fee Transmittal

Application Number:	13288919			
Filing Date:	03-Nov-2011			
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE			
First Named Inventor/Applicant Name:	IGOR POLISHCHUK			
Filer:	Larry Joel Johnson/Alma Fazlic			
Attorney Docket Number:	PM07027D1			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	20039411
Application Number:	13288919
International Application Number:	
Confirmation Number:	3343
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	IGOR POLISHCHUK
Customer Number:	60909
Filer:	Larry Joel Johnson/Alma Fazlic
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	PM07027D1
Receipt Date:	03-SEP-2014
Filing Date:	03-NOV-2011
Time Stamp:	19:26:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	5406
Deposit Account	503781
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	PM07027D1_IssueFeeLetter_09032014.pdf	17660 bd37c45669c2f2140605b85268402f58c8701c4	no	2

Warnings:

Information:

2	Issue Fee Payment (PTO-85B)	PM07027D1_IssueFee_09032014.pdf	1108212 4e40c2522175df58011260b5978042ed79561d10	no	1
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Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	30623 b125197790ae91ce0141806a69460c46db3d51a5	no	2
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Warnings:

Information:

Total Files Size (in bytes): 1156495

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Examiner: NGO, NGAN V
	)	
IGOR POLISHCHUK	)	Group Art Unit: 2893
	)	
Application No.: 13/288,919	)	Confirmation No.: 3343
	)	
Filed: 11-03-2011	)	
	)	
For: MEMORY TRANSISTOR WITH	)	
MULTIPLE CHARGE STORING	)	
LAYERS AND A HIGH WORK	)	
FUNCTION GATE ELECTRODE	)	

ISSUE FEE TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant is in receipt of a Notice of Allowance and Fees Due Form, mailed August 26, 2014 in connection with the above-identified application. The Issue Fee is due on or before November 26, 2014. Applicant hereby submits the Issue Fee.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.19, 1.20 and 1.21 that may be required to issue the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Customer No.: 60909

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry J. Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

Dated: 09/03/2014

By: /Larry J. Johnson/
Larry J. Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Customer No.: 60909



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 08/26/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER

NGO, NGAN V

ART UNIT

PAPER NUMBER

2893

DATE MAILED: 08/26/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	11/26/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 08/26/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	11/26/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	438-287000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

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NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343
60909	7590	08/26/2014	EXAMINER	
CYPRESS SEMICONDUCTOR CORPORATION			NGO, NGAN V	
198 CHAMPION COURT			ART UNIT	PAPER NUMBER
SAN JOSE, CA 95134-1709			2893	

DATE MAILED: 08/26/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the IDS filed 8-11-14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 16.19 and 21-34. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/oph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>20140811</u> 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	5. ☒ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	--

/NGAN NGO/ Primary Examiner, Art Unit 2893	
---	--

The present application is being examined under the pre-AIA first to invent provisions.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

In the claims:

Claim 16, line 5, delete "including".

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 13/288,919
Art Unit: 2893

Page 3

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

8/21/2014

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10	("20030169629" "20080135946" "20090179253" "20100117138" "8222688").PN.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/08/20 22:00
L8	6	11/811958	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/08/20 22:13
L9	2967	(438/287,288).CCLS.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2014/08/20 22:41
L11	4534	(257/324,326).CCLS.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/08/20 23:19

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	1	(438/287,288).CCLS.	UPAD	OR	OFF	2014/08/20 22:45
L12	1	(257/324,326).CCLS.	UPAD	OR	ON	2014/08/20 23:20

8/ 20/ 2014 11:20:25 PM**C:\Users\nngo\Documents\EAST\Workspaces\13288919.wsp**

<i>Index of Claims</i> 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant								☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE											
Final	Original	12/02/2013	04/11/2014	06/14/2014	06/30/2014	08/20/2014							
	1	-	-	-	-	-							
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	16	✓	=	✓	=	=							
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	18	✓	-	-	-	-							
	19	✓	=	✓	=	=							
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	32	=	=	=	=	=							
	33	=	=	=	=	=							
	34	=	=	=	=	=							

Issue Classification 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

CPC		
Symbol	Type	Version

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/NGAN NGO/ Primary Examiner.Art Unit 2893	08/20/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2C

Issue Classification 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
438		287				H	0	1	L	21 / 336 (2006.0)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
438	288																		

NONE		Total Claims Allowed:	
		16	
(Assistant Examiner)	(Date)		
/NGAN NGO/ Primary Examiner.Art Unit 2893	08/20/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2C

Issue Classification 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17	15	33										
	2		18	16	34										
	3	2	19												
	4		20												
	5	3	21												
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	11	9	27												
	12	10	28												
	13	11	29												
	14	12	30												
	15	13	31												
1	16	14	32												

NONE		Total Claims Allowed:	
		16	
(Assistant Examiner)	(Date)		
/NGAN NGO/ Primary Examiner.Art Unit 2893	08/20/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2C

Search Notes 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 27/085, 27/105, 27/11563, 27/11573	12-2-13	NN
Update all above	4-11-14	NN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	324, 326	12-2-13	NN
	Update all above	4-11-14	NN
438	287, 288	4-11-14	NN
	Update all above	6-30-14	NN
	Update all above	8-20-14	NN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search. See printout	12-2-13	NN
EAST search. See printout	4-11-14	NN
EAST search. See printout	6-14-14	NN
EAST search. See printout	6-30-14	NN
EAST search. See printout	8-20-14	NN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	324, 326	4-11-14	NN
438	287, 288	4-11-14	NN
	Update all above	6-30-14	NN

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INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Update all above	8-20-14	NN

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Receipt date: 08/11/2014

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13288919 - GAI-2893

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13288919	
	Filing Date		2011-11-03	
	First Named Inventor	Igor Polishchuk		
	Art Unit	2893		
	Examiner Name	YUSHIN, NIKOLAY K		
	Attorney Docket Number	PM07027D1		

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8222688	B1	2012-07-17	Jenne et al.	Entire Document

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	1	20030169629	A	2003-09-11	Goebel et al.	Entire Document
	2	20080135946	A	2008-06-12	Yan	Entire Document
	3	20090179253	A	2009-07-16	Levy et al.	Entire Document
	4	20100117138	A	2010-05-13	Huerta et al.	Entire Document

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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² i	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13288919	13288919 - GAU: 2893
	Filing Date		2011-11-03	
	First Named Inventor	Igor Polishchuk		
	Art Unit	2893		
	Examiner Name	YUSHIN, NIKOLAY K		
	Attorney Docket Number	PM07027D1		

	1							☐
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NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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EXAMINER SIGNATURE			
Examiner Signature	/Ngan Ngo/	Date Considered	08/20/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	13/288,919	Filing Date	2011-11-03	Docket Number (if applicable)	PM07027D1	Art Unit	2893
First Named Inventor	IGOR POLISHCHUK			Examiner Name	NGO, NGAN V		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☐ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____.
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503781

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/ Larry J. Johnson /	Date (YYYY-MM-DD)	2014-08-11
Name	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13288919	
	Filing Date		2011-11-03	
	First Named Inventor	Igor Polishchuk		
	Art Unit	2893		
	Examiner Name	YUSHIN, NIKOLAY K		
	Attorney Docket Number	PM07027D1		

U.S.PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	8222688	B1	2012-07-17	Jenne et al.	Entire Document		
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S.PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	20030169629	A	2003-09-11	Goebel et al.	Entire Document		
	2	20080135946	A	2008-06-12	Yan	Entire Document		
	3	20090179253	A	2009-07-16	Levy et al.	Entire Document		
	4	20100117138	A	2010-05-13	Huerta et al.	Entire Document		
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
FOREIGN PATENT DOCUMENTS							Remove	
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² i	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13288919
	Filing Date		2011-11-03
	First Named Inventor	Igor Polishchuk	
	Art Unit	2893	
	Examiner Name	YUSHIN, NIKOLAY K	
	Attorney Docket Number	PM07027D1	

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13288919
	Filing Date		2011-11-03
	First Named Inventor	Igor Polishchuk	
	Art Unit	2893	
	Examiner Name	YUSHIN, NIKOLAY K	
	Attorney Docket Number	PM07027D1	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/ Larry J. Johnson /	Date (YYYY-MM-DD)	2014-08-11
Name/Print	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13288919			
Filing Date:	03-Nov-2011			
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE			
First Named Inventor/Applicant Name:	IGOR POLISHCHUK			
Filer:	Larry Joel Johnson/Melissa Lico			
Attorney Docket Number:	PM07027D1			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
RCE - 2nd and Subsequent Request	1820	1	1700	1700
Total in USD (\$)				1700

Electronic Acknowledgement Receipt

EFS ID:	19835844
Application Number:	13288919
International Application Number:	
Confirmation Number:	3343
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	IGOR POLISHCHUK
Customer Number:	60909
Filer:	Larry Joel Johnson/Melissa Lico
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	PM07027D1
Receipt Date:	11-AUG-2014
Filing Date:	03-NOV-2011
Time Stamp:	19:08:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1700
RAM confirmation Number	5996
Deposit Account	503781
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	PM07027D1_TransmittalLetter_08112014.pdf	19147 3b91ce46939d156ffe27ab71e6e7d241715af264	no	2

Warnings:

Information:

2	Request for Continued Examination (RCE)	PM07027D1_RCE_08112014.pdf	697862 dc7de7b49a9f72a9fd95cf8bbeffa09657f4399	no	3
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Warnings:

Information:

3	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1_IDSform_08112014.pdf	612231 9013c615d72b320ced57e50625f00ee71b953d75	no	4
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Warnings:

Information:

4	Fee Worksheet (SB06)	fee-info.pdf	30166 b20bda901b839134f4c22fe6af3391306f9a7728	no	2
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Warnings:

Information:

Total Files Size (in bytes):	1359406
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
IGOR POLISHCHUK	)	Examiner: NGO, NGAN V
Application No.: 13/288,919	)	Group Art Unit: 2893
Filed: 11-03-2011	)	Confirmation No.: 3343
For: MEMORY TRANSISTOR WITH	)	
MULTIPLE CHARGE STORING	)	
LAYERS AND A HIGH WORK	)	
FUNCTION GATE ELECTRODE	)	

**REQUEST FOR CONTINUED EXAMINATION
AND INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the Request for Continued Examination to be considered with the IDS for the above referenced application. In compliance with the duty of disclosure under 37 CFR § 1.56 and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

Customer No.: 60909

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

/

/

Respectfully submitted,

Date: 08/11/2014

By: / Larry J. Johnson /

Larry J. Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Customer No.: 60909

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/288,919		Filing Date 11/03/2011		☐ To be Mailed	
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)			(Column 2)						

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$	=
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II									
(Column 1)			(Column 2)			(Column 3)			

AMENDMENT	08/11/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 16	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

(Column 1)			(Column 2)			(Column 3)			
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AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LAJUAN HICKSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 07/08/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER

NGO, NGAN V

ART UNIT

PAPER NUMBER

2893

DATE MAILED: 07/08/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	10/08/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 07/08/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	10/08/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	438-287000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343
60909	7590	07/08/2014	EXAMINER	
CYPRESS SEMICONDUCTOR CORPORATION			NGO, NGAN V	
198 CHAMPION COURT			ART UNIT	PAPER NUMBER
SAN JOSE, CA 95134-1709			2893	

DATE MAILED: 07/08/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 6-20-14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 16.19 and 21-34. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/oph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/NGAN NGO/ Primary Examiner, Art Unit 2893	
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Issue Classification 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	

CPC						
Symbol					Type	Version

CPC Combination Sets					
Symbol				Type	Version

NONE		Total Claims Allowed:	
		16	
(Assistant Examiner)	(Date)		
/NGAN NGO/ Primary Examiner.Art Unit 2893	06/30/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2C

Issue Classification 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
438		287				H	0	1	L	21 / 336 (2006.0)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
438	288																		

NONE		Total Claims Allowed:	
		16	
(Assistant Examiner)	(Date)		
/NGAN NGO/ Primary Examiner.Art Unit 2893	06/30/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2C

Issue Classification 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17	15	33										
	2		18	16	34										
	3	2	19												
	4		20												
	5	3	21												
	6	4	22												
	7	5	23												
	8	6	24												
	9	7	25												
	10	8	26												
	11	9	27												
	12	10	28												
	13	11	29												
	14	12	30												
	15	13	31												
1	16	14	32												

NONE		Total Claims Allowed:	
		16	
(Assistant Examiner)	(Date)		
/NGAN NGO/ Primary Examiner.Art Unit 2893	06/30/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2C

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	110124	oxide-nitride-oxide or ono or sonos	US-PGPUB; USPAT; USOCR	OR	ON	2014/06/30 01:37
L2	16394	L1 and (nonvolatile adj memory or non-volatile adj memory)	US-PGPUB; USPAT; USOCR	OR	ON	2014/06/30 01:37
L3	571715	((("257") or ("438")).CLAS.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2014/06/30 01:37
L4	9438	L2 and L3	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/06/30 01:37
L5	7273	L4 and (@pd<="20070525" or @ad<="20070525" or @rlad<="20070525")	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/06/30 01:37
L6	2879	(438/287,288).CCLS.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2014/06/30 01:57

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	1	(438/287,288).CCLS.	UPAD	OR	OFF	2014/06/30 02:39

6/30/2014 2:40:25 AM**C:\Users\ningo\Documents\EAST\Workspaces\13288919.wsp**

<i>Index of Claims</i> 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47									
CLAIM		DATE							
Final	Original	12/02/2013	04/11/2014	06/14/2014	06/30/2014				
	1	-	-	-	-				
	2	-	-	-	-				
	3	-	-	-	-				
	4	-	-	-	-				
	5	-	-	-	-				
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	7	-	-	-	-				
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	9	-	-	-	-				
	10	-	-	-	-				
	11	-	-	-	-				
	12	-	-	-	-				
	13	-	-	-	-				
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	15	-	-	-	-				
	16	✓	=	✓	=				
	17	✓	-	-	-				
	18	✓	-	-	-				
	19	✓	=	✓	=				
	20	✓	=	O	-				
	21	=	=	=	=				
	22	=	=	=	=				
	23	=	=	=	=				
	24	=	=	=	=				
	25	=	=	=	=				
	26	=	=	=	=				
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	28	=	=	=	=				
	29	=	=	=	=				
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	31	=	=	=	=				
	32	=	=	=	=				
	33	=	=	=	=				
	34	=	=	=	=				

Search Notes 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 27/085, 27/105, 27/11563, 27/11573	12-2-13	NN
Update all above	4-11-14	NN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	324, 326	12-2-13	NN
	Update all above	4-11-14	NN
438	287, 288	4-11-14	NN
	Update all above	6-30-14	NN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search. See printout	12-2-13	NN
EAST search. See printout	4-11-14	NN
EAST search. See printout	6-14-14	NN
EAST search. See printout	6-30-14	NN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	324, 326	4-11-14	NN
438	287, 288	4-11-14	NN
	Update all above	6-30-14	NN

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	13/288,919	Confirmation No. 3343
In re Application of	:	Igor Polishchuk, et al.	Customer No. 60909
Filed	:	November 3, 2011	
TC/A.U.	:	2893	
Examiner	:	NGO, NGAN V.	
Docket No.	:	PM07027D1	
Title	:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

This paper is responsive to the Non-Final Office Action mailed on June 19, 2014, and is timely filed.

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper

Amendments to the Claims:

1-15. (Canceled)

16. (Currently Amended) A method of forming a semiconductor device comprising:

forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed by forming at least a substantially trap free bottom oxynitride layer followed by forming a charge trapping top oxynitride layer, wherein the ONO dielectric stack including includes a multi-layer charge storage layer;

forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and

forming a doped polysilicon layer on the surface of a ONO dielectric stack and on a surface of the oxide layer of the MOS logic transistor to form a first high work function gate electrode on [[a]] the surface of the ONO dielectric stack while concurrently forming a second high work function gate electrode on the oxide layer of the MOS logic transistor.

17-18. (Canceled)

19. (Previously Presented) A method according to claim 16, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, the doped polysilicon layer comprises a P+ dopant, and wherein the method further comprises patterning the doped polysilicon layer, the ONO dielectric stack and the oxide layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

20. (Canceled)

21. (Previously Presented) A method comprising:

forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO

dielectric stack comprising a multi-layer charge storage layer including a silicon-rich, oxygen-lean top silicon oxynitride layer and a silicon-rich, oxygen-rich bottom silicon oxynitride layer;
forming a gate oxide on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and
forming a high work function gate electrode on the gate oxide.

22. (Previously Presented) The method of claim 21, further comprising forming a high work function gate electrode formed over a surface of the ONO dielectric stack of the non-volatile memory transistor.

23. (Previously Presented) The method of claim 22, wherein forming the ONO dielectric stack comprises forming a trap-rich top silicon oxynitride layer and a substantially trap free silicon bottom oxynitride layer.

24. (Previously Presented) The method of claim 22, wherein the substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein forming the high work function gate electrode of the non-volatile memory transistor comprises forming a P+ doped polysilicon layer to form a nMOS silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor.

25. (Previously Presented) The method of claim 24, wherein forming the high work function gate electrode of the logic transistor comprises forming a P+ doped polysilicon layer to form a pMOS logic transistor.

26. (Previously Presented) The method of claim 22, wherein the substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein forming the high work function gate electrode of the non-volatile memory transistor comprises forming a N+ doped polysilicon layer to form a pMOS silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor.

27. (Previously Presented) The method of claim 26, wherein forming the high work function gate electrode of the logic transistor comprises forming a N+ doped polysilicon layer to form a nMOS logic transistor.

28. (Previously Presented) The method of claim 22, wherein forming the high work function gate electrode of the non-volatile memory transistor and forming the high work function gate electrode of the logic transistor comprises forming and patterning a single, doped polysilicon layer.

29. (Previously Presented) The method of claim 21, wherein forming the ONO dielectric stack comprises forming a trap-rich top silicon oxynitride layer and a substantially trap free silicon bottom oxynitride layer.

30. (Previously Presented) The method of claim 21, wherein the substrate comprises a silicon surface, and wherein forming the high work function gate electrode of the logic transistor comprises forming a P+ doped polysilicon layer to form a pMOS logic transistor.

31. (Previously Presented) The method of claim 21, wherein the substrate comprises a silicon surface, and wherein forming the high work function gate electrode of the logic transistor comprises forming a N+ doped polysilicon layer to form a nMOS logic transistor.

32. (Previously Presented) A method comprising:
forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack comprising a multi-layer charge storage layer including a trap-rich top silicon nitride layer and a substantially trap free silicon bottom nitride layer;
forming a gate oxide on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and
forming a high work function gate electrode on the gate oxide.

33. (Previously Presented) The method of claim 32, further comprising forming a high work function gate electrode formed over a surface of the ONO dielectric stack of the non-volatile memory transistor.

34. (Previously Presented) The method of claim 33, wherein forming the high work function gate electrode of the non-volatile memory transistor comprises forming a P+ doped polysilicon layer to form a nMOS silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor, and wherein forming the high work function gate electrode of the logic transistor comprises forming a P+ doped polysilicon layer to form a pMOS logic transistor.

Remarks

Status of the Claims

Claim 16 is amended. Claims 1-15, 17, 18, and 20 are canceled. No new matter is added. Claims 21-34 are allowed.

Allowable Subject Matter

Claim 20 is objected to as being dependent upon the rejected base claim 16 but would be allowable if rewritten into independent form.

Claim Amendments

The amendments to the claims are fully supported by the specification as originally filed, and no new matter will be added by entry of the amendment(s). The Applicants have amended the claims to expedite prosecution by taking allowable subject matter and not because the Applicants acquiesce to the rejections set forth in the Office Action. The amendments are not intended to limit the scope of equivalents to which any claim element may be entitled.

Summary of the Office Action

Claims 16-19 are rejected under pre-AIA 35 U.S.C. 102(b) as allegedly being anticipated by Roizin et al (US 2005/0186741 A1, cited by applicants).

Claims 21-34 are allowed.

Response to Rejections and Objections

Claim 16 has been amended to include the allowable features of claim 20. Therefore, claim 16 and all the claims that depend therefrom are now in condition for allowance, and the rejections and objections associated with claims 16-20 are now moot.

Reservation of Rights

Applicants believe every assertion by the Office Action has been addressed, however in the interest of clarity and brevity, Applicants may not have asserted every available argument for each assertion made in the Office Action. Applicants' silence regarding any such assertion does not constitute any admission or acquiescence. Applicants reserve all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicants do not admit that any of the cited references or any other references of record is relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicants timely object to such reliance on Official Notice, and reserve all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicants reserve all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

Conclusion

Appl. No. 13/288,919
Amdt. dated June 20, 2014
Reply to the Office Action of June 19, 2014

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Larry J. Johnson at 408-545-7194.

It is believed no further fees are required for filing this amendment. However, if necessary, please charge any additional fees under 37 CFR §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, or apply any credits to our PTO deposit account number: 50-3781.

Respectfully submitted,
for Igor Polishchuk, et al.

Dated: June 20, 2014

By: /Larry J. Johnson/.
Larry J. Johnson, Reg. No. 56,861
Attorney for the Applicant(s)

Electronic Acknowledgement Receipt

EFS ID:	19369974
Application Number:	13288919
International Application Number:	
Confirmation Number:	3343
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	IGOR POLISHCHUK
Customer Number:	60909
Filer:	Larry Joel Johnson/Alma Fazlic
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	PM07027D1
Receipt Date:	20-JUN-2014
Filing Date:	03-NOV-2011
Time Stamp:	17:05:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	PM07027D1_ROA_06192014.pdf	40946 b53105d16362f1fd4706a576a0fe73a2431e4f3e	no	8

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/288,919		Filing Date 11/03/2011		☐ To be Mailed	
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)			(Column 2)						

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II									
(Column 1)			(Column 2)			(Column 3)			

AMENDMENT	06/20/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 16	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

(Column 1)			(Column 2)			(Column 3)			
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AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LASHAWN MORGAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343
60909 7590 06/19/2014 CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709			EXAMINER NGO, NGAN V	
			ART UNIT 2893	PAPER NUMBER
			NOTIFICATION DATE 06/19/2014	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Office Action Summary	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 6-9-14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☒ Claim(s) 16 and 19-34 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☒ Claim(s) 21-34 is/are allowed.

7) ☒ Claim(s) 16 and 19 is/are rejected.

8) ☒ Claim(s) 20 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some** c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 20140609.

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16 and 19 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Roizin et al (US 2005/0186741 A1, cited by Applicants).

Roizin discloses in figure 13 a method of forming a semiconductor device comprising: forming an oxide-nitride-oxide (ONO, 261,262,263) dielectric stack on a surface of a semiconductor substrate (210) in at least a first region (202) in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer; forming an oxide layer (263) on the surface of the substrate in a second region (201) in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and forming a doped polysilicon layer (1301) on the surface of a ONO dielectric stack and on a surface of the oxide layer of the MOS logic transistor to form a first high work function gate electrode on the surface of the ONO dielectric stack while concurrently forming a second high work function gate electrode on the oxide layer of the MOS logic transistor. See paragraphs [0029] and [0053]

In re claim 19, Roizin teaches the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, the doped polysilicon layer comprises a P+ dopant, and wherein the method further comprises patterning the doped

polysilicon layer, the ONO dielectric stack and the oxide layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 21-34 stand allowed.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Application/Control Number: 13/288,919
Art Unit: 2893

Page 4

Ngan Ngo

June 16, 2014

<i>Index of Claims</i> 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☐ T.D.
 ☐ R.1.47

CLAIM		DATE							
Final	Original	12/02/2013	04/11/2014	06/14/2014					
	1	-	-	-					
	2	-	-	-					
	3	-	-	-					
	4	-	-	-					
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	18	✓	-	-					
	19	✓	=	✓					
	20	✓	=	O					
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	32	=	=	=					
	33	=	=	=					
	34	=	=	=					

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	75	("20010052615" "20030183869" "20040173918" "20050070126" "20050186741" "20050266637" "20060281331" "6051880" "6081331" "20070048916" "20070215940" "20080048237" "20080290400" "20080293207" "20080293254" "20080293255" "8029399" "8237694" "20090039414" "20110018053" "20110163371" "20110248332" "20120068159" "20130175604" "4843023" "6214689" "6429081" "6469343" "6610614" "7045424" "7262457" "7576386" "7723789" "7999295" "8067284" "8318608").PN.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/06/14 02:48

EAST Search History (Interference)

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6/ 14/ 2014 3:23:27 AM**C:\ Users\ nngo\ Documents\ EAST\ Workspaces\ 13288919.wsp**

Search Notes 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 27/085, 27/105, 27/11563, 27/11573	12-2-13	NN
Update all above	4-11-14	NN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	324, 326	12-2-13	NN
	Update all above	4-11-14	NN
438	287, 288	4-11-14	NN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search. See printout	12-2-13	NN
EAST search. See printout	4-11-14	NN
EAST search. See printout	6-14-14	NN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	324, 326	4-11-14	NN
438	287, 288	4-11-14	NN

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Receipt date: 06/09/2014

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13288919 - GAIL-2893

Approved for use through 07/31/2012. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13288919
	Filing Date		2011-11-03
	First Named Inventor	Igor Polishchuk	
	Art Unit	2893	
	Examiner Name	YUSHIN, NIKOLAY K	
	Attorney Docket Number	PM07027D1	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	4843023	A	1989-06-27	Chiu et al.	Entire Document
	2	6214689	B1	2001-04-10	Lim et al.	Entire Document
	3	6429081	B1	2002-08-06	Doong et al.	Entire Document
	4	6469343	B1	2002-10-22	Miura et al.	Entire Document
	5	6610614	B2	2003-08-26	Niimi et al.	Entire Document
	6	7045424	B2	2006-05-16	Kim et al.	Entire Document
	7	7262457	B2	2007-08-28	Hsu et al.	Entire Document
	8	7576386	B2	2009-08-18	Lue et al.	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Receipt date: 06/09/2014		Application Number		13288919	13288919 - GAU: 2893
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			Art Unit		2893	
			Examiner Name		YUSHIN, NIKOLAY K	
			Attorney Docket Number		PM07027D1	

	9	7723789	B2	2010-05-25	Lin et al.	Entire Document
	10	7999295	B2	2011-08-16	Lai et al.	Entire Document
	11	8067284	B1	2011-11-29	Levy	Entire Document
	12	8318608	B2	2012-11-27	Ramkumar et al.	Entire Document

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	1	20010052615	A	2001-12-20	Fujiwara	Entire Document
	2	20030183869	A	2003-10-02	Crivelli et al.	Entire Document
	3	20040173918	A	2004-09-09	Kamal et al.	Entire Document
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	5	20050186741	A	2005-08-25	Roizin et al.	Entire Document

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			Attorney Docket Number	PM07027D1	

	6	20050266637	A	2005-12-01	Wang	Entire Document
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	13	20080290400	A	2008-11-27	Jenne et al.	Entire Document
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	Attorney Docket Number	PM07027D1		

	17	2008029399	A	2008-02-07	Tomita et al.	Entire Document
	18	2008237694	A	2008-10-02	Specht et al.	Entire Document
	19	20090039414	A	2009-02-12	Lue et al.	Entire Document
	20	20110018053	A	2011-01-27	Lo Guo et al.	Entire Document
	21	20110163371	A	2011-07-07	Song et al.	Entire Document
	22	20110248332	A	2011-10-13	Levy et al.	Entire Document
	23	20120068159	A	2012-03-22	Fujiki et al.	Entire Document
	24	20130175604	A	2013-07-11	Polishchuk et al.	Entire Document

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	1	2008129478	WO	A	2008-10-30	Huerta et al.	Entire Document	☐

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	Attorney Docket Number	PM07027D1		

	2	2011162725	WO	A	2011-12-29	Singh et al.	Entire Document	☐
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	1	"MAX 9000 Programmable Logic Device Family," Altera, July 1999, Version 6.01, pp. 1-40; 41 pages	☐	
	2	L. Richard Carley, "Trimming Analog Circuits Using Floating-Gate Analog MOS Memory," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, December 1989, pp. 1569-1575; 7 pages	☐	
	3	"1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer," Cypress Advance Information, 02/12/2004; 9 pages	☐	
	4	"10 Gigabit Ethernet Technology Overview White Paper", Revision 1.0, Retrieved from Internet: URL: http://www.10gea.org, May, 2001.	☐	
	5	"16K x 8/9 Dual-Port Static RAM with Sem, Int, Busy," Cypress Semiconductor Data Book, May 1995, CY7C006 and CY7C016, pp. 6:1-17; 10 pages	☐	
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	7	"1kHz to 30MHz Resistor Set SOT-23 Oscillator", Initial Release Final Electrical Specifications LTC1799, Linear Technology Corporation, Jan. 2001, pp. 1-4.	☐	
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9	"2K x 16 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C133 and CY7C143, pp. 6:63-73; 7 pages	☐
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11	"A Novel Integration Technology of EEPROM Embedded CMOS Logic VLSI Suitable for ASIC Applications", By Masataka Takebuchi et al., IEEE 1992 Custom Integrated Circuits Conference, pp. 9.6.1-9.6.4.	☐
12	"A Novel Robust and Low Cost Stack Chips Package and Its Thermal Performance", By Soon-Jin Cho et al., IEEE Transaction on Advanced Packaging, vol. 23, No. 2, May 2000, pp. 257-265.	☐
13	"A Planar Type EEPROM Cell Structure by Standard CMOS Process for Integration with Gate Array, Standard Cell, Microprocessor and for Neural Chips", By Katsuhiko Ohsaki et al., IEEE 1993 Custom Integrated Circuits Conference, pp-23.6.1-23.6.4.	☐
14	"A Single Chip Sensor & Image Processor for Fingerprint Verification" Anderson, S., et al., IEEE Custom Integrated Circuits Conference, May 12-15, 1991.	☐
15	"A Single Poly EPROM For Custom CMOS Logic Applications", By Reza Kazerounian et al., IEEE 1986 Custom Integrated Circuits Conference, pp. 59-62.	☐
16	"A Wide-Bandwidth Low-Voltage PLL for PowerPC.TM. Microprocessors", By Jose Alvarez et al., IEEE Journal of Solid-State Circuits, vol. 30, No. 4, Apr. 1995, pp. 383-391.	☐
17	"About SmaL Camera Technologies, Inc.", SmaL Camera Technologies, 2001, 1 page.	☐
18	"Achieving Uniform nMOS Device Power Distribution for Sub-micron ESD Reliability," Charvaka Duvvuy, Carlos Diaz, and Tim Haddock; 1992; 92-131 through 92-134, no month.	☐
19	"ADNS-2030 High Performance, Low Power Optical Mouse Sensor (Optimized for Cordless Mouse Applications)," Agilent Technologies, downloaded 10/10/2005, < http://www.home.agilent.com/USeng/nav/-536893734,536883737/pd.html >; 2 pages	☐

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20	"Agilent ADNK-2030 Solid-State Optical Mouse Sensor," Agilent Technologies Inc., Sample Kit, 2003; 1 page	☐
21	"Agilent ADNS-2030 Low Power Optical Mouse Sensor," Agilent Technologies Inc., Data Sheet, 2005; 34 pages	☐
22	"Agilent ADNS-2051 Optical Mouse Sensor," Agilent Technologies Inc., Product Overview, 2003; 2 pages	☐
23	"Agilent Optical Mouse Sensors," Agilent Technologies Inc., Selection Guide, 2004; 3 pages	☐
24	"Algorithm for Managing Multiple First-In, First-Out Queues from a Single Shared Random-Access Memory," IBM Technical Disclosure Bulletin, August 1989; 5 pages	☐
25	"Am99C10A 256.times.48 Content Addressable Memory", Advanced Micro Devices, Dec. 1992.	☐
26	"An Analog PLL-Based Clock and Data Recovery Circuit with High Input Jitter Tolerance", By Sam Yinshang Sun, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-24, pp. 325-330, Apr. 1989, pp. 383-385.	☐
27	"An EEPROM for Microprocessors and Custom Logic", By Roger Cuppens et al., IEEE Journal of Solid-State Circuits, vol. SC-20, No. 2, Apr. 1985, pp. 603-608.	☐
28	"An EPROM Cell Structure foe EPLDs Compatible with Single Poly Gate Process", By Kuniyushi Yoshikawa et al., Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 323-326.	☐
29	"An Experimental 5-V-Only 256-kbit CMOS EEPROM with a High-Performance Single-Polysilicon Cell", By Jun-Ichi Miyamoto et al., IEEE Journal of Solid State Circuits, vol. SC-21, No. 5, Oct. 1986, pp. 852-860.	☐
30	Application Number 14/159,315 (PM07027D1CIP1C1): "MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE" Igor Polishchuk et al., filed on 01/20/2014; 60 pages	☐

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	Art Unit	2893	
	Examiner Name	YUSHIN, NIKOLAY K	
	Attorney Docket Number	PM07027D1	

31	Chen et al., "Performance Improvement of SONOS Memory by Bandgap Engineering of Charge-Trapping Layer," IEEE Electron Device Letters, April 2004, Vol. 25, No. 4, pp. 205-207; 3 pages	☐
32	International Search Report for International Application Number PCT/US13/48885 (PM07027D1CIP1WO) dated 11/14/2013; 2 pages	☐
33	Lue et al., "BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability," IEEE, 2005; 4 pages	☐
34	Lue, Hang-Ting et al., "Reliability Model of Bandgap Engineered SONOS (be-SONOS)", IEEE, 2006, 4 pgs.	☐
35	USPTO Missing Parts for Application Number 13/539,466 (PM07027D1CIP1) dated 07/17/2012; 2 pages	☐
36	USPTO Non-Final Rejection for Application Number 13/539,466 (PM07027D1CIP1) dated 09/28/2012; 9 pages	☐
37	USPTO Notice of Allowance for Application Number 13/539,466 (PM07027D1CIP1) dated 11/27/2012; 8 pages	☐
38	USPTO Requirement for Restriction for Application Number 12/152,518 (PM07027) dated 06/09/2010; 5 pages	☐
39	Wang, Szu-Yu et al., "Reliability and processing effects of bandgap engineered SONOS flash memory", 2007 IEEE, International Reliability Symposium, April 18, 2007, 5 pgs.	☐
40	Wu et al., "SONOS Device with Tapered Bandgap Nitride Layer," IEEE Transactions on Electron Devices, May 2005, Vol. 52, No. 5, pp. 987-992; 6 pages	☐
41	Yang et al., "Reliability considerations in scaled SONOS nonvolatile memory devices, solid state Electronics", 43(1999) 2025-2032.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13288919	13288919 - GAU: 2893
	Filing Date		2011-11-03	
	First Named Inventor	Igor Polishchuk		
	Art Unit	2893		
	Examiner Name	YUSHIN, NIKOLAY K		
	Attorney Docket Number	PM07027D1		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13288919
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	First Named Inventor	Igor Polishchuk
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	1	4843023	A	1989-06-27	Chiu et al.	Entire Document
	2	6214689	B1	2001-04-10	Lim et al.	Entire Document
	3	6429081	B1	2002-08-06	Doong et al.	Entire Document
	4	6469343	B1	2002-10-22	Miura et al.	Entire Document
	5	6610614	B2	2003-08-26	Niimi et al.	Entire Document
	6	7045424	B2	2006-05-16	Kim et al.	Entire Document
	7	7262457	B2	2007-08-28	Hsu et al.	Entire Document
	8	7576386	B2	2009-08-18	Lue et al.	Entire Document

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	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1

	9	7723789	B2	2010-05-25	Lin et al.	Entire Document
	10	7999295	B2	2011-08-16	Lai et al.	Entire Document
	11	8067284	B1	2011-11-29	Levy	Entire Document
	12	8318608	B2	2012-11-27	Ramkumar et al.	Entire Document

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	1	20010052615	A	2001-12-20	Fujiwara	Entire Document
	2	20030183869	A	2003-10-02	Crivelli et al.	Entire Document
	3	20040173918	A	2004-09-09	Kamal et al.	Entire Document
	4	20050070126	A	2005-03-31	Senzaki	Entire Document
	5	20050186741	A	2005-08-25	Roizin et al.	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13288919
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	Attorney Docket Number	PM07027D1

	6	20050266637	A	2005-12-01	Wang	Entire Document
	7	20060281331	A	2006-12-14	Wang	Entire Document
	8	2006051880	A	2006-03-09	Doczy et al.	Entire Document
	9	2006081331	A	2006-04-20	Campian	Entire Document
	10	20070048916	A	2007-03-01	Suzuki et al.	Entire Document
	11	20070215940	A	2007-09-20	Ligon	Entire Document
	12	20080048237	A	2008-02-28	Iwata	Entire Document
	13	20080290400	A	2008-11-27	Jenne et al.	Entire Document
	14	20080293207	A	2008-11-27	Koutny Jr et al.	Entire Document
	15	20080293254	A	2008-11-27	Ramkumar et al.	Entire Document
	16	20080293255	A	2008-11-27	Ramkumar	Entire Document

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	Attorney Docket Number	PM07027D1		

	17	2008029399	A	2008-02-07	Tomita et al.	Entire Document
	18	2008237694	A	2008-10-02	Specht et al.	Entire Document
	19	20090039414	A	2009-02-12	Lue et al.	Entire Document
	20	20110018053	A	2011-01-27	Lo Guo et al.	Entire Document
	21	20110163371	A	2011-07-07	Song et al.	Entire Document
	22	20110248332	A	2011-10-13	Levy et al.	Entire Document
	23	20120068159	A	2012-03-22	Fujiki et al.	Entire Document
	24	20130175604	A	2013-07-11	Polishchuk et al.	Entire Document

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	1	2008129478	WO	A	2008-10-30	Huerta et al.	Entire Document	☐

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	2	2011162725	WO	A	2011-12-29	Singh et al.	Entire Document	☐
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	1	"MAX 9000 Programmable Logic Device Family," Altera, July 1999, Version 6.01, pp. 1-40; 41 pages						☐
	2	L. Richard Carley, "Trimming Analog Circuits Using Floating-Gate Analog MOS Memory," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, December 1989, pp. 1569-1575; 7 pages						☐
	3	"1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer," Cypress Advance Information, 02/12/2004; 9 pages						☐
	4	"10 Gigabit Ethernet Technology Overview White Paper", Revision 1.0, Retrieved from Internet: URL: http://www.10gea.org , May, 2001.						☐
	5	"16K x 8/9 Dual-Port Static RAM with Sem, Int, Busy," Cypress Semiconductor Data Book, May 1995, CY7C006 and CY7C016, pp. 6:1-17; 10 pages						☐
	6	"1K x 8 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C130/CY7C131 and CY7C140/ CY7C141, pp. 6:37-49; 8 pages						☐
	7	"1kHz to 30MHz Resistor Set SOT-23 Oscillator", Initial Release Final Electrical Specifications LTC1799, Linear Technology Corporation, Jan. 2001, pp. 1-4.						☐
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9	"2K x 16 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C133 and CY7C143, pp. 6:63-73; 7 pages	☐
10	"2K x 8 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C132/CY7C136 and CY7C142/ CY7C146, pp. 6:50-62; 8 pages	☐
11	"A Novel Integration Technology of EEPROM Embedded CMOS Logic VLSI Suitable for ASIC Applications", By Masataka Takebuchi et al., IEEE 1992 Custom Integrated Circuits Conference, pp. 9.6.1-9.6.4.	☐
12	"A Novel Robust and Low Cost Stack Chips Package and Its Thermal Performance", By Soon-Jin Cho et al., IEEE Transaction on Advanced Packaging, vol. 23, No. 2, May 2000, pp. 257-265.	☐
13	"A Planar Type EEPROM Cell Structure by Standard CMOS Process for Integration with Gate Array, Standard Cell, Microprocessor and for Neural Chips", By Katsuhiko Ohsaki et al., IEEE 1993 Custom Integrated Circuits Conference, pp-23.6.1-23.6.4.	☐
14	"A Single Chip Sensor & Image Processor for Fingerprint Verification" Anderson, S., et al., IEEE Custom Integrated Circuits Conference, May 12-15, 1991.	☐
15	"A Single Poly EPROM For Custom CMOS Logic Applications", By Reza Kazerounian et al., IEEE 1986 Custom Integrated Circuits Conference, pp. 59-62.	☐
16	"A Wide-Bandwidth Low-Voltage PLL for PowerPC.TM. Microprocessors", By Jose Alvarez et al., IEEE Journal of Solid-State Circuits, vol. 30, No. 4, Apr. 1995, pp. 383-391.	☐
17	"About SmaL Camera Technologies, Inc.", SmaL Camera Technologies, 2001, 1 page.	☐
18	"Achieving Uniform nMOS Device Power Distribution for Sub-micron ESD Reliability," Charvaka Duvvuy, Carlos Diaz, and Tim Haddock; 1992; 92-131 through 92-134, no month.	☐
19	"ADNS-2030 High Performance, Low Power Optical Mouse Sensor (Optimized for Cordless Mouse Applications)," Agilent Technologies, downloaded 10/10/2005, < http://www.home.agilent.com/USeng/nav/-536893734,536883737/pd.html >; 2 pages	☐

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	20	"Agilent ADNK-2030 Solid-State Optical Mouse Sensor," Agilent Technologies Inc., Sample Kit, 2003; 1 page	☐
	21	"Agilent ADNS-2030 Low Power Optical Mouse Sensor," Agilent Technologies Inc., Data Sheet, 2005; 34 pages	☐
	22	"Agilent ADNS-2051 Optical Mouse Sensor," Agilent Technologies Inc., Product Overview, 2003; 2 pages	☐
	23	"Agilent Optical Mouse Sensors," Agilent Technologies Inc., Selection Guide, 2004; 3 pages	☐
	24	"Algorithm for Managing Multiple First-In, First-Out Queues from a Single Shared Random-Access Memory," IBM Technical Disclosure Bulletin, August 1989; 5 pages	☐
	25	"Am99C10A 256.times.48 Content Addressable Memory", Advanced Micro Devices, Dec. 1992.	☐
	26	"An Analog PLL-Based Clock and Data Recovery Circuit with High Input Jitter Tolerance", By Sam Yinshang Sun, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-24, pp. 325-330, Apr. 1989, pp. 383-385.	☐
	27	"An EEPROM for Microprocessors and Custom Logic", By Roger Cuppens et al., IEEE Journal of Solid-State Circuits, vol. SC-20, No. 2, Apr. 1985, pp. 603-608.	☐
	28	"An EPROM Cell Structure foe EPLDs Compatible with Single Poly Gate Process", By Kuniyushi Yoshikawa et al., Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 323-326.	☐
	29	"An Experimental 5-V-Only 256-kbit CMOS EEPROM with a High-Performance Single-Polysilicon Cell", By Jun-Ichi Miyamoto et al., IEEE Journal of Solid State Circuits, vol. SC-21, No. 5, Oct. 1986, pp. 852-860.	☐
	30	Application Number 14/159,315 (PM07027D1CIP1C1): "MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE" Igor Polishchuk et al., filed on 01/20/2014; 60 pages	☐

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	33	Lue et al., "BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability," IEEE, 2005; 4 pages	☐
	34	Lue, Hang-Ting et al., "Reliability Model of Bandgap Engineered SONOS (be-SONOS)", IEEE, 2006, 4 pgs.	☐
	35	USPTO Missing Parts for Application Number 13/539,466 (PM07027D1CIP1) dated 07/17/2012; 2 pages	☐
	36	USPTO Non-Final Rejection for Application Number 13/539,466 (PM07027D1CIP1) dated 09/28/2012; 9 pages	☐
	37	USPTO Notice of Allowance for Application Number 13/539,466 (PM07027D1CIP1) dated 11/27/2012; 8 pages	☐
	38	USPTO Requirement for Restriction for Application Number 12/152,518 (PM07027) dated 06/09/2010; 5 pages	☐
	39	Wang, Szu-Yu et al., "Reliability and processing effects of bandgap engineered SONOS flash memory", 2007 IEEE, International Reliability Symposium, April 18, 2007, 5 pgs.	☐
	40	Wu et al., "SONOS Device with Tapered Bandgap Nitride Layer," IEEE Transactions on Electron Devices, May 2005, Vol. 52, No. 5, pp. 987-992; 6 pages	☐
	41	Yang et al., "Reliability considerations in scaled SONOS nonvolatile memory devices, solid state Electronics", 43(1999) 2025-2032.	☐

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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.			

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	Examiner Name	YUSHIN, NIKOLAY K
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

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INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PM727D1CIPWO	FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/US13/48885	International filing date (<i>day/month/year</i>) 01 July 2013 (01.07.2013)	(Earliest) Priority Date (<i>day/month/year</i>) 01 July 2012 (01.07.2012)
Applicant Cypress Semiconductor Corporation		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

a. With regard to the **language**, the international search was carried out on the basis of:

- ☒ the international application in the language in which it was filed.
☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

- ☐ the text is approved as submitted by the applicant.
☒ the text has been established by this Authority to read as follows:

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS

5. With regard to the **abstract**,

- ☒ the text is approved as submitted by the applicant.
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6. With regard to the **drawings**,

- a. the figure of the **drawings** to be published with the abstract is Figure No. 3
☒ as suggested by the applicant.
☐ as selected by this Authority, because the applicant failed to suggest a figure.
☐ as selected by this Authority, because this figure better characterizes the invention.
- b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US13/48885

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 29/792 (2013.01)

USPC - 438/591; 257/324, E29.308

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - H01L 29/792 (2013.01)

USPC - 438/920, 591; 257/321, 324, 325, E29.308, E29.309

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); Google Patents; Google Scholar; IP.COM; IEEE Xplore; Search Terms Used: non volatile memory, memory, NVM, charge trapping layers, SONOS, silicon oxynitride, tunneling layer, anti-tunneling layer, high K dielectric, thin film, nanowire*, FinFET, metal gate, nitrated oxide, capping, blocking, trench, channel, opening, vertical, ONO logic, MOS, HV MOS.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/0248332 A1 (LEVY S et al.) October 13, 2011, Figure 2, paragraphs [0022], [0025], [0045].	1 - 20
Y	US 7,999,295 B2 (LAI E et al.) August 16, 2011, column 3, lines 29 - 39, column 3, line 60 to column 4, line 4.	1-17, 20
Y	US 7,723,789 B2 (LIN H et al.) May 25, 2010, Figures 1A - 1H, column 2, line 63 to column 3, line 45.	2-5, 12-15, 18-20
Y	US 2008/0293207 A1 (KOUTNY JR W et al.) November 27, 2008, Abstract, Figures 3A, 3B, paragraphs [0050] - [0053].	6-9, 17, 19
Y	US 2009/0039414 A1 (LUE H et al.) February 12, 2009, Abstract.	4, 5, 13, 14, 16

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

21 October 2013 (21.10.2013)

Date of mailing of the international search report

14 NOV 2013

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-3201

Authorized officer:

Shane Thomas

PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774

Electronic Patent Application Fee Transmittal				
Application Number:		13288919		
Filing Date:		03-Nov-2011		
Title of Invention:		MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
First Named Inventor/Applicant Name:		IGOR POLISHCHUK		
Filer:		Andrew J. Bateman/Adnan Fazlic		
Attorney Docket Number:		PM07027D1		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description		Fee Code	Quantity	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	19247951
Application Number:	13288919
International Application Number:	
Confirmation Number:	3343
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	IGOR POLISHCHUK
Customer Number:	60909
Filer:	Andrew J. Bateman/Adnan Fazlic
Filer Authorized By:	Andrew J. Bateman
Attorney Docket Number:	PM07027D1
Receipt Date:	09-JUN-2014
Filing Date:	03-NOV-2011
Time Stamp:	14:59:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	1249
Deposit Account	503781
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	PM07027D1_RCE_06092014.pdf	700086	no	3
			1a6553e2e5f928f2d5b9c0e18196390df161021b		
Warnings:					
Information:					
2	Transmittal Letter	PM07027D1_TransmittalLetter_06092014.pdf	22978	no	2
			82621807bac5da9f20a3685a6ad90d5f4bdfc69a		
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1_IDS1_06092014.pdf	616081	no	11
			77abac9f4134ee8c6ed0f9ae31215244115f941e		
Warnings:					
Information:					
4	Non Patent Literature	Max90000.pdf	3556880	no	41
			696b6321188b4f4156f20d2a1db5c15f5445cc46		
Warnings:					
Information:					
5	Non Patent Literature	Carley.pdf	533744	no	7
			036ab667fc5d21eeab4a814efb4efde63964e9d0		
Warnings:					
Information:					
6	Non Patent Literature	JEDEC.pdf	283612	no	9
			48a3ff5d115fb028539e287014aa051d81426b4c		
Warnings:					
Information:					
7	Non Patent Literature	10Gigabit.pdf	690233	no	22
			744e03cdf8fc27f9a0ef7033dd374eb9491ae7		
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Information:					
8	Non Patent Literature	16K.pdf	2245125	no	10
			10ba370ff39353b533ce7f6d3b98bbc605f53c45		

Warnings:					
Information:					
9	Non Patent Literature	1K.pdf	1771532	no	8
			83339c99d3a6794d93c241476007c2b636b cc537		
Warnings:					
Information:					
10	Non Patent Literature	1KHz.pdf	520543	no	5
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11	Non Patent Literature	200MBaud.pdf	7973570	no	62
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Information:					
12	Non Patent Literature	2Kx16.pdf	1114327	no	7
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13	Non Patent Literature	2Kx8.pdf	1322043	no	8
			7c1cd672ba4736ca9727e54b20ce759d708 a460d		
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Information:					
14	Non Patent Literature	MasatakaTakebuchi.pdf	394805	no	4
			fa0ef4b41c300adc36d563c71f3f98b479eec 4e2		
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15	Non Patent Literature	SoonJinCho.pdf	777367	no	10
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16	Non Patent Literature	Katsuhiko.pdf	595407	no	4
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17	Non Patent Literature	Anderson.pdf	497313	no	4
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19	Non Patent Literature	JoseAlvarez.pdf	376330	no	2
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20	Non Patent Literature	SMaLCamera.pdf	230665	no	3
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22	Non Patent Literature	ADNS2030H.pdf	145337	no	2
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23	Non Patent Literature	ADNK2030.pdf	94208	no	1
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27	Non Patent Literature	Algorithm.pdf	413002	no	5
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28	Non Patent Literature	Am99C10A.pdf	2516054	no	26
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29	Non Patent Literature	YinshangSun.pdf	510333	no	6
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31	Non Patent Literature	KuniyushiYoshikawa.pdf	716692	no	5
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33	Non Patent Literature	PM07027D1CIP1C1_Application_01202014.pdf	2261963	no	60
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34	Non Patent Literature	Chen.pdf	447482	no	2
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35	Non Patent Literature	PM07027D1CIP1WO_SearchReport_11142013.pdf	101390	no	2
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Warnings:					
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Warnings:					
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37	Non Patent Literature	LueHangTing.pdf	435048	no	2
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38	Non Patent Literature	PM07027D1CIP1_MissingParts_07172012.pdf	56993	no	2
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Warnings:					
Information:					
39	Non Patent Literature	PM07027D1CIP1_NonFinalRejection_09282012.pdf	341889	no	9
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Warnings:					
Information:					
40	Non Patent Literature	PM07027D1CIP1_NOA_11272012.pdf	423415	no	8
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41	Non Patent Literature	PM07027_RequirementRestriction_06092010.pdf	177537	no	5
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42	Non Patent Literature	Wang.pdf	435845	no	2
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Information:					
45	Fee Worksheet (SB06)	fee-info.pdf	30590	no	2
			355949e3bfddc3c9360aa2cd4135b66e225ff167		
Warnings:					
Information:					
Total Files Size (in bytes):			40630576		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	13/288,919	Filing Date	2011-11-03	Docket Number (if applicable)	PM07027D1	Art Unit	2893
First Named Inventor	Igor Polishchuck			Examiner Name	NGO, NGAN V		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☐ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503781

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Larry J. Johnson/	Date (YYYY-MM-DD)	2014-06-09
Name	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	Examiner: NGO, NGAN V
Igor Polishchuk	)	
	)	Group Art Unit: 2893
Application No.: 13/288,919	)	
	)	Confirmation No.: 3343
Filed: 2011-11-03	)	
	)	
For: MEMORY TRANSISTOR WITH	)	
MULTIPLE CHARGE STORING	)	
LAYERS AND A HIGH WORK	)	
FUNCTION GATE ELECTRODE	)	

**REQUEST FOR CONTINUED EXAMINATION
AND INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the Request for Continued Examination to be considered with the IDS for the above referenced application. In compliance with the duty of disclosure under 37 CFR § 1.56 and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

Customer No.: 60909

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

/

/

Respectfully submitted,

Date: 06/09/2014

By: /Larry J. Johnson/

Larry J. Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Customer No.: 60909



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 04/28/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER

NGO, NGAN V

ART UNIT

PAPER NUMBER

2893

DATE MAILED: 04/28/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	07/28/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 04/28/2014
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	07/28/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343
60909	7590	04/28/2014	EXAMINER	
CYPRESS SEMICONDUCTOR CORPORATION			NGO, NGAN V	
198 CHAMPION COURT			ART UNIT	PAPER NUMBER
SAN JOSE, CA 95134-1709			2893	

DATE MAILED: 04/28/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 336 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 336 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 2-4-14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 16 and 19-34. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/oph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/NGAN NGO/ Primary Examiner, Art Unit 2893	
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Search Notes 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 27/085, 27/105, 27/11563, 27/11573	12-2-13	NN
Update all above	4-11-14	NN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	324, 326	12-2-13	NN
	Update all above	4-11-14	NN
438	287, 288	4-11-14	NN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search. See printout	12-2-13	NN
EAST search. See printout	4-11-14	NN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	324, 326	4-11-14	NN
438	287, 288	4-11-14	NN

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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	108379	oxide-nitride-oxide or ono or sonos	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/11 18:01
L2	16003	L1 and (nonvolatile adj memory or non-volatile adj memory)	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/11 18:01
L3	557009	((("257") or ("438")).CLAS.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2014/04/11 18:01
L4	9313	L2 and L3	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/04/11 18:01
L5	7258	L4 and (@pd<="20070525" or @ad<="20070525" or @rlad<="20070525")	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/04/11 18:01
L6	10895	(257/324,326).CCLS. or (H01I27/085 or H01I27/105 or H01I27/11563 or H01I27/11573).CPC.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/04/11 20:31
L7	4184	(257/324,326).CCLS.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/04/11 21:54
L9	2813	(438/287,288).CCLS.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2014/04/11 22:38
L10	2330	I9 not I7	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2014/04/11 22:38

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	1	(257/324,326).CCLS.	UPAD	OR	ON	2014/04/11 21:54
L11	1	(438/287,288).CCLS.	UPAD	OR	OFF	2014/04/11 22:57

4/ 11/ 2014 10:58:07 PM

C:\Users\ningo\Documents\EAST\Workspaces\13288919.wsp

<i>Index of Claims</i> 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47									
CLAIM		DATE							
Final	Original	12/02/2013	04/11/2014						
	1	-	-						
	2	-	-						
	3	-	-						
	4	-	-						
	5	-	-						
	6	-	-						
	7	-	-						
	8	-	-						
	9	-	-						
	10	-	-						
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	15	-	-						
	16	✓	=						
	17	✓	-						
	18	✓	-						
	19	✓	=						
	20	✓	=						
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	27	=	=						
	28	=	=						
	29	=	=						
	30	=	=						
	31	=	=						
	32	=	=						
	33	=	=						
	34	=	=						

Issue Classification 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	

CPC					Type	Version
Symbol						
H01L		27		085	F	
H01L		27		105	I	
H01L		27		11563	I	
H01L		27		11573	I	

CPC Combination Sets					Type	Set	Ranking	Version
Symbol								

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	17	
/NGAN NGO/ Primary Examiner.Art Unit 2893	04/11/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2C

Issue Classification 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
438		287				H	0	1	L	21 / 336 (2006.0)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
438	288																		

NONE		Total Claims Allowed:	
		17	
(Assistant Examiner)	(Date)		
/NGAN NGO/ Primary Examiner.Art Unit 2893	04/11/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2C

Issue Classification 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17	16	33										
	2		18	17	34										
	3	2	19												
	4	3	20												
	5	4	21												
	6	5	22												
	7	6	23												
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	11	10	27												
	12	11	28												
	13	12	29												
	14	13	30												
	15	14	31												
1	16	15	32												

NONE		Total Claims Allowed:	
		17	
(Assistant Examiner)	(Date)		
/NGAN NGO/ Primary Examiner.Art Unit 2893	04/11/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	13/288,919	Confirmation No. 3343
In re Application of	:	Igor Polishchuk, et al.	
Filed	:	November 3, 2011	
TC/A.U.	:	2893	
Examiner	:	NGO, NGAN V.	
Docket No.	:	PM07027D1	
Customer No.	:	60909	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

This paper is responsive to the Non-final Office Action mailed on December 5, 2013, and is timely filed.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks/Arguments begin on page 7 of this paper

Appl. No. 13/288,919
Amdt. dated February 4, 2014
Reply to the Office Action of December 5, 2013

Amendments to the Specification:

Please amend the paragraph beginning on page 2, line 2 with the following paragraph:

The present application is a divisional of U.S. Application No. 12/152,518, filed on May 13, 2008, now Patent No. , , 8,063,434 issued on November 22, 2011, which claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 60/940,160, entitled "SONOS Gate Stack With Multiple Oxynitride Layers And A High Workfunction Gate Electrode," filed May 25, 2007, both of which applications are hereby incorporated by reference in their entirety.

Amendments to the Claims:

1-15. (Canceled)

16. (Currently Amended) A method of forming a semiconductor device comprising:
forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer;

forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and

forming a doped polysilicon layer on the surface of a ONO dielectric stack and on a surface of the oxide layer of the MOS logic transistor to form a first high work function gate electrode on [[a]] the surface of the ONO dielectric stack while concurrently forming a second high work function gate electrode on the oxide layer of the MOS logic transistor.

17-18. (Canceled)

19. (Currently Amended) A method according to claim ~~18~~ 16, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, the doped polysilicon layer comprises a P+ dopant, and wherein the method further comprises patterning the doped polysilicon layer, the ONO dielectric stack and the oxide layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

20. (Previously Presented) A method according to claim 16, wherein forming an ONO dielectric stack including a multi-layer charge storage layer comprises forming at least a substantially trap free bottom oxynitride layer followed by forming a charge trapping top oxynitride layer.

21. (Previously Presented) A method comprising:
forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO

dielectric stack comprising a multi-layer charge storage layer including a silicon-rich, oxygen-lean top silicon oxynitride layer and a silicon-rich, oxygen-rich bottom silicon oxynitride layer;
forming a gate oxide on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and
forming a high work function gate electrode on the gate oxide.

22. (Previously Presented) The method of claim 21, further comprising forming a high work function gate electrode formed over a surface of the ONO dielectric stack of the non-volatile memory transistor.

23. (Previously Presented) The method of claim 22, wherein forming the ONO dielectric stack comprises forming a trap-rich top silicon oxynitride layer and a substantially trap free silicon bottom oxynitride layer.

24. (Previously Presented) The method of claim 22, wherein the substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein forming the high work function gate electrode of the non-volatile memory transistor comprises forming a P⁺ doped polysilicon layer to form a nMOS silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor.

25. (Previously Presented) The method of claim 24, wherein forming the high work function gate electrode of the logic transistor comprises forming a P⁺ doped polysilicon layer to form a pMOS logic transistor.

26. (Previously Presented) The method of claim 22, wherein the substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein forming the high work function gate electrode of the non-volatile memory transistor comprises forming a N⁺ doped polysilicon layer to form a pMOS silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor.

27. (Previously Presented) The method of claim 26, wherein forming the high work function gate electrode of the logic transistor comprises forming a N⁺ doped polysilicon layer to form a nMOS logic transistor.

28. (Previously Presented) The method of claim 22, wherein forming the high work function gate electrode of the non-volatile memory transistor and forming the high work function gate electrode of the logic transistor comprises forming and patterning a single, doped polysilicon layer.

29. (Previously Presented) The method of claim 21, wherein forming the ONO dielectric stack comprises forming a trap-rich top silicon oxynitride layer and a substantially trap free silicon bottom oxynitride layer.

30. (Previously Presented) The method of claim 21, wherein the substrate comprises a silicon surface, and wherein forming the high work function gate electrode of the logic transistor comprises forming a P⁺ doped polysilicon layer to form a pMOS logic transistor.

31. (Previously Presented) The method of claim 21, wherein the substrate comprises a silicon surface, and wherein forming the high work function gate electrode of the logic transistor comprises forming a N⁺ doped polysilicon layer to form a nMOS logic transistor.

32. (Previously Presented) A method comprising:

forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack comprising a multi-layer charge storage layer including a trap-rich top silicon nitride layer and a substantially trap free silicon bottom nitride layer;

forming a gate oxide on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and

forming a high work function gate electrode on the gate oxide.

33. (Previously Presented) The method of claim 32, further comprising forming a high work function gate electrode formed over a surface of the ONO dielectric stack of the non-volatile memory transistor.

34. (Previously Presented) The method of claim 33, wherein forming the high work function gate electrode of the non-volatile memory transistor comprises forming a P+ doped polysilicon layer to form a nMOS silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor, and wherein forming the high work function gate electrode of the logic transistor comprises forming a P+ doped polysilicon layer to form a pMOS logic transistor.

Remarks

Status of the Claims

Claims 16, 19-34 remain pending, claims 17 and 18 having been canceled to facilitate prosecution. Claims 16 and 19 have been amended.

No new matter is added and entry of the amendments is respectfully requested.

Summary of the Office Action

Claims 16-20 are rejected under pre-AIA 35 U.S.C. 103(a) as allegedly being unpatentable over Lue et al (US 2008/0291726).

Claims 21-34 are allowed.

Applicant thanks the examiner for allowance of claims 21-34.

Rejection of the remaining claims will now be addressed by responding to the rejection of independent claim 16 as amended

Rejection of the claims Under 103(a)

Claim 16 is rejected under pre-AIA 35 U.S.C. 103(a) as allegedly being unpatentable over Lue.

Claim 16 is directed to a method of forming a semiconductor device, and as amended includes the features of “forming a doped polysilicon layer on the surface of a ONO dielectric stack and on a surface of the oxide layer of the MOS logic transistor to form a first high work function gate electrode on the surface of the ONO dielectric stack while concurrently forming a second high work function gate electrode on the oxide layer of the MOS logic transistor.”

Applicants’ submit that paragraph [0095] in Lue, cited by the examiner as teaching high work function gate electrodes, refers in context only to the forming of a high work function gate electrode over the ONO structure of a memory device. (See paragraph [0096] and Table 2). Thus, Lue does not teach or suggest forming a “second high work function gate electrode on the oxide layer of the MOS logic transistor,” still less does Lue teach or suggest that this second high work function gate electrode is formed concurrently with the forming of a first high work function gate electrode on the surface of the ONO dielectric stack by “forming a doped polysilicon layer on the surface of a ONO dielectric stack and on a surface of the oxide layer of the MOS logic transistor.”

Accordingly, Applicants submit that claim 16 as amended, as well as claims 19 and 20 which are dependent therefrom, are patentable over the cited reference.

Reservation of Rights

Applicants believe every assertion by the Office Action has been addressed, however in the interest of clarity and brevity, Applicants may not have asserted every available argument for each assertion made in the Office Action. Applicants' silence regarding any such assertion does not constitute any admission or acquiescence. Applicants reserve all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicants do not admit that any of the cited references or any other references of record is relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicants timely object to such reliance on Official Notice, and reserve all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicants reserve all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, William E. Nuttle at (650) 207-3418.

It is believed no further fees are required for filing this amendment. However, if necessary, please charge any additional fees under 37 CFR §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that

Appl. No. 13/288,919
Amdt. dated February 4, 2014
Reply to the Office Action of December 5, 2013

may be required to maintain pendency of the present application, or apply any credits to our PTO
deposit account number: 50-3781.

Respectfully submitted,
for Igor Polishchuk, et al.

Dated: February 4, 2014

By: /William E. Nuttle/.
William E. Nuttle, Reg. No. 42,943
Attorney for the Applicant(s)
P.O. Box 4240
Foster City, CA 94404
Tel.: (650)207-3418

Electronic Acknowledgement Receipt

EFS ID:	18112861
Application Number:	13288919
International Application Number:	
Confirmation Number:	3343
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	IGOR POLISHCHUK
Customer Number:	60909
Filer:	William Edward Nuttle
Filer Authorized By:	
Attorney Docket Number:	PM07027D1
Receipt Date:	04-FEB-2014
Filing Date:	03-NOV-2011
Time Stamp:	16:59:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PM07027D1_ROA.pdf	89126 f14525be6cf40af4e7e1afa5a5f2a18b9877a2	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	9
Warnings:			
Information:			
Total Files Size (in bytes):		89126	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/288,919		Filing Date 11/03/2011		☐ To be Mailed	
---	--	--	--	---	--	----------------------------------	--	---------------------------------------	--

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)			(Column 2)						

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II									
(Column 1)			(Column 2)			(Column 3)			

AMENDMENT	02/04/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

(Column 1)			(Column 2)			(Column 3)			
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AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/TONYA MCBRIDE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1	3343
60909 7590 12/05/2013 CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709			EXAMINER NGO, NGAN V	
			ART UNIT 2893	PAPER NUMBER
			NOTIFICATION DATE 12/05/2013	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

larz@cypress.com
patents@cypress.com
pbj@cypress.com

Office Action Summary	Application No. 13/288,919	Applicant(s) POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☒ Claim(s) 16-34 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☒ Claim(s) 21-34 is/are allowed.

7) ☒ Claim(s) 16-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some** c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 20120801.

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 16-20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Lue et al (US 2008/0291726 A1).

Lue discloses a method of forming a semiconductor device comprising: forming an ONO (120, 130, 140) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer; forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (GATE OXIDE as shown in figure 31) transistor is to be formed; and forming a high work function gate electrode on a surface of the ONO dielectric stack. Note the teachings of high work function gate in paragraph [0095] of Lue. It would have been obvious to one of ordinary skill in the art that the BLTs can be used as logic transistor.

In re claim 20, Lue teaches oxynitride layers in paragraph [0082].

Claims 21-34 are allowed.

The other references are cited to show other structures pertinent to Applicants' disclosure.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ngan Ngo/

Primary Examiner, Art Unit 2893

Ngan Ngo

December 2, 2013

Notice of References Cited	Application/Control No. 13/288,919		Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.	
	Examiner NGAN NGO		Art Unit 2893	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2006/0202261 A1	09-2006	Lue et al.	257/324
*	B	US-2007/0268753 A1	11-2007	Lue et al.	365/185.28
*	C	US-2008/0175053 A1	07-2008	Lue et al.	365/185.05
*	D	US-2008/0291726 A1	11-2008	LUE et al.	365/185.05
*	E	US-2009/0045452 A1	02-2009	LUE et al.	257/321
*	F	US-7,642,585 B2	01-2010	Wang et al.	257/296
*	G	US-7,688,626 B2	03-2010	Lue et al.	365/185.05
*	H	US-2010/0117139 A1	05-2010	Lue, Hang-Ting	257/324
*	I	US-2010/0155823 A1	06-2010	LUE et al.	257/324
*	J	US-7,790,516 B2	09-2010	Willer et al.	438/129
*	K	US-7,948,799 B2	05-2011	Lue et al.	365/185.17
*	L	US-8,264,028 B2	09-2012	Lue et al.	257/324
*	M	US-8,315,095 B2	11-2012	Lue et al.	365/185.05

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 13/288,919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.	
	Examiner NGAN NGO	Art Unit 2893	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,482,052 B2	07-2013	Lue et al.	257/324
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	Q					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 27/085, 27/105, 27/11563, 27/11573	12-2-13	NN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	324, 326	12-2-13	NN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search. See printout	12-2-13	NN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 13288919	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.
	Examiner NGAN NGO	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant											☐ CPA											☐ T.D.											☐ R.1.47										
CLAIM			DATE																																								
Final	Original	12/02/2013																																									
	1	-																																									
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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	105711	oxide-nitride-oxide or ono or sonos	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/01 23:09
L2	15392	L1 and (nonvolatile adj memory or non-volatile adj memory)	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/01 23:09
L3	525465	((("257") or ("438")).CLAS.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2013/12/01 23:09
L4	9133	L2 and L3	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2013/12/01 23:09
L5	7217	L4 and (@pd<="20070525" or @ad<="20070525" or @rlad<="20070525")	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2013/12/01 23:09
L6	23459	(257/324,326).CCLS. or ((H01I27/085) or (H01I27/105) or (H01I27/11563) or (H01I27/11573)).IPCR.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2013/12/01 23:25

EAST Search History (Interference)

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12/ 2/ 2013 1:18:39 AM**C:\ Users\ nngo\ Documents\ EAST\ Workspaces\ 13288919.wsp**

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	"8063434"	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2013/12/01 17:37
L2	2	("8063434").PN.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2013/12/01 17:37
L3	18	("20030122204" "20050230766" "20060131636" "20070246753" "20070262451" "20070267687" "20070268753" "20070272916" "20080009115" "20080290399" "20100041222" "20100295118" "6906390" "6912163" "7312496" "7323742" "7737488" "7790516").PN. OR ("8063434").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/01 17:59
L4	105711	oxide-nitride-oxide or ono or sonos	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/01 18:04
L5	15392	l4 and (nonvolatile adj memory or non-volatile adj memory)	US-PGPUB; USPAT; USOCR	OR	ON	2013/12/01 18:04
L6	525465	((("257") or ("438")).CLAS.	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2013/12/01 18:05
L7	9133	l5 and l6	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2013/12/01 18:05
L8	7217	l7 and (@pd<="20070525" or @ad<="20070525" or @rlad<="20070525")	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2013/12/01 18:07
L9	61	l8 and high adj work adj function adj gate	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2013/12/01 18:08
L10	2	l9 and logic adj transistor	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2013/12/01 18:11
L11	0	("l8and(silicon-richoroxygen-leanoroxygen- richorsiliconadjrichoroxygenadjleanoroxygenadjrich)").PN.	US-PGPUB; USPAT; USOCR;	OR	OFF	2013/12/01 18:47

EAST Search History

			DERWENT; IBM_TDB			
L12	626	I8 and (silicon-rich or oxygen-lean or oxygen-rich or silicon adj rich or oxygen adj lean or oxygen adj rich)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2013/12/01 18:49
L13	7	I8 and ((silicon-rich and oxygen-lean and oxygen-rich) or (silicon adj rich and oxygen adj lean and oxygen adj rich))	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2013/12/01 18:50

EAST Search History (Interference)

< This search history is empty >

12/ 1/ 2013 6:53:11 PM



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BIB DATA SHEET

CONFIRMATION NO. 3343

SERIAL NUMBER 13/288,919	FILING or 371(c) DATE 11/03/2011 RULE	CLASS 257	GROUP ART UNIT 2893	ATTORNEY DOCKET NO. PM07027D1		
APPLICANTS INVENTORS IGOR POLISHCHUK, Fremont, CA; Sagy LEVY, Zichron Ya'akov, ISRAEL; Krishnaswamy RAMKUMAR, San Jose, CA; ** CONTINUING DATA ***** This application is a DIV of 12/152,518 05/13/2008 PAT 8063434 which claims benefit of 60/940,160 05/25/2007 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 11/14/2011						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /NGAN V NGO/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 4	TOTAL CLAIMS 19	INDEPENDENT CLAIMS 3
ADDRESS CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709 UNITED STATES						
TITLE MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE						
FILING FEE RECEIVED 1250	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

Receipt date: 08/01/2012

13288919 - GAI: 2893

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0851-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13288919
	Filing Date		2011-11-03
	First Named Inventor	Igor Polishchuk	
	Art Unit	2893	
	Examiner Name	YUSHIN, NIKOLAY K	
	Attorney Docket Number	PM07027D1	

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	6906390	B2	2005-06-14	Nomoto et al.	Entire Document
	2	6912163	B2	2005-06-28	Zheng et al.	Entire Document
	3	7312496	B2	2007-12-25	Hazama	Entire Document
	4	7323742	B2	2008-01-29	Georgescu	Entire Document
	5	7737488	B2	2010-06-15	Lai et al.	Entire Document
	6	7790516	B2	2010-09-07	Willer et al.	Entire Document

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U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear

Receipt date: 08/01/2012 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13288919	13288919 - GAU: 2893
	Filing Date		2011-11-03	
	First Named Inventor	Igor Polishchuk		
	Art Unit	2893		
	Examiner Name	YUSHIN, NIKOLAY K		
	Attorney Docket Number	PM07027D1		

1	20030122204	A	2003-07-03	Nomoto et al.	Entire Document
2	20050230766	A1	2005-10-20	Nomoto et al.	Entire Document
3	20060131636	A	2006-06-22	Jeon et al.	Entire Document
4	20070246753	A	2007-10-25	Chu et al.	Entire Document
5	20070262451	A	2007-11-15	Rachmady et al.	Entire Document
6	20070267687	A	2007-11-22	Lue	Entire Document
7	20070268753	A	2007-11-22	Lue et al.	Entire Document
8	20070272916	A1	2007-11-29	Wang et al.	Entire Document
9	20080009115	A1	2008-01-10	Willer et al.	Entire Document
10	20080290399	A	2008-11-27	Levy et al.	Entire Document
11	20100041222	A	2010-02-18	Puchner et al.	Entire Document

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	Examiner Name	YUSHIN, NIKOLAY K		
	Attorney Docket Number	PM07027D1		

	12	20100295118	A1	2010-11-25	Bhattacharyya	Entire Document
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NON-PATENT LITERATURE DOCUMENTS

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	1	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 03/09/2011; 4 pages	☐
	2	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 09/29/2010; 5 pages	☐
	3	USPTO Notice of Allowance for Application Number 12/152,518 (PM07027) dated 07/14/2011; 6 pages	☐

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Examiner Signature	/Ngan Ngo/	Date Considered	12/02/2013
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear

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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
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NON-PATENT LITERATURE DOCUMENTS

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	1	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 03/09/2011; 4 pages	☐
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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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(Not for submission under 37 CFR 1.99)

Application Number	13288919
Filing Date	2011-11-03
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Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13288919
Filing Date	2011-11-03
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Larry J. Johnson/	Date (YYYY-MM-DD)	2012-08-01
Name/Print	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
IGOR POLISHCHUK	)	Examiner: YUSHIN, NIKOLAY K
	)	
Application No.: 13/288,919	)	Group Art Unit: 2893
	)	
Filed: November 3, 2011	)	Confirmation No.: 3343
	)	
For: MEMORY TRANSISTOR WITH	)	
MULTIPLE CHARGE STORING	)	
LAYERS AND A HIGH WORK	)	
FUNCTION GATE ELECTRODE	)	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
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Sir:

In compliance with the duty of disclosure under 37 CFR § 1.56 and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

No fee is believed necessary for the submission of this Information Disclosure Statement. However, The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

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Should the Examiner have any questions, Applicants' undersigned attorney is reachable by telephone in our San Jose office at (408) 545-7194. The correspondence address of record appears below

Respectfully submitted,

Date: 08/01/2012 By: Larry J. Johnson
Larry J. Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Electronic Acknowledgement Receipt

EFS ID:	13397965
Application Number:	13288919
International Application Number:	
Confirmation Number:	3343
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	IGOR POLISHCHUK
Customer Number:	60909
Filer:	Larry Joel Johnson/Rosemary Saint-Vincent
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	PM07027D1
Receipt Date:	01-AUG-2012
Filing Date:	03-NOV-2011
Time Stamp:	18:43:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1_IDSform_08012012.pdf	1147857 52f0d8f0ac319c87b590ab9fed08ea36d434247a	no	6

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2	Transmittal Letter	PM07027D1_TransmittalLetter_08012012.pdf	288787 c0472b2d420f1da94f23ecb1200ac8fb8f6c129e	no	2
Warnings:					
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3	Non Patent Literature	PM07027_NOA_07142011.pdf	355660 7c941c7f5d2aa33c9e81c0ccb1bc3f8c752f9926	no	6
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4	Non Patent Literature	PM07027_NonFinalOA_03092011.pdf	137033 5705c2bff82b68b029e19df2c291670c5f65c8d4	no	4
Warnings:					
Information:					
5	Non Patent Literature	PM07027_NonFinalOA_09292010.pdf	159620 6f5b0de9ccad5172c5742ea653b37a1cd891c8d	no	5
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/288,919	11/03/2011	2812	1250	PM07027D1	19	3

CONFIRMATION NO. 3343

60909

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

FILING RECEIPT



OC000000050953682

Date Mailed: 11/18/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

IGOR POLISHCHUK, Fremont, CA;
Sagy LEVY, Zichron Ya'akov, ISRAEL;
Krishnaswamy RAMKUMAR, San Jose, CA;

Assignment For Published Patent Application

CYPRESS SEMICONDUCTOR CORPORATION, San Jose, CA

Power of Attorney: The patent practitioners associated with Customer Number 51885

Domestic Priority data as claimed by applicant

This application is a DIV of 12/152,518 05/13/2008 PAT 8,063,434
which claims benefit of 60/940,160 05/25/2007

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 11/14/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/288,919**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK
FUNCTION GATE ELECTRODE

Preliminary Class

438

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/288,919			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	620		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250		
TOTAL CLAIMS (37 CFR 1.16(i))	19	minus 20 = *				x 60 =	0.00		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 250 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250		
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
			TOTAL ADD'L FEE			TOTAL ADD'L FEE			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
			TOTAL ADD'L FEE			TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/288,919	11/03/2011	IGOR POLISHCHUK	PM07027D1

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

CONFIRMATION NO. 3343

POA ACCEPTANCE LETTER



Date Mailed: 11/18/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/03/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/fstephanos/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	To be assigned	Confirmation No.	unknown
In re Application of	:	Igor Polishchuk, et al.		
Filed	:	herewith		
TC/A.U.	:	unknown		
Examiner	:	unknown		
Docket No.	:	PM07027D1		
Customer No.	:	60909		

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Please amend the application as follows prior to examination on the merits.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Abstract begin on page 3 of this paper.

Amendments to the Claims are reflected in the listing of the claims which begin on page 4 of this paper.

Remarks/Arguments begin on page 8 of this paper.

Amendments to the Specification:

Please amend the paragraph beginning on page 2, line 2 with the following paragraph:

The present application is a divisional of U.S. Application No. 12/152,518, filed on May 13, 2008, now Patent No. __, __, __, issued on _____, which claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 60/940,160, entitled "SONOS Gate Stack With Multiple Oxynitride Layers And A High Workfunction Gate Electrode," filed May 25, 2007, both of which applications are hereby incorporated by reference in their entirety.

Amendments To The Abstract Of The Disclosure:

Please replace the Abstract Of the Disclosure on page 25 with the following paragraph:

Semiconductor devices including non-volatile memory transistors and methods of fabricating the same to improve performance thereof are provided. In one embodiment, the method comprises: (i) forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer; (ii) forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and (iii) forming a high work function gate electrode on a surface of the ONO dielectric stack. Other embodiments are also disclosed.

Amendments to the Claims:

1-15. (Canceled)

16. (Currently Amended) A method of forming a semiconductor device comprising ~~steps of:~~
forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer;
forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and
forming a high work function gate electrode on a surface of the ONO dielectric stack.

17. (Currently Amended) A method according to claim 16, wherein ~~step of~~ forming a high work function gate electrode on a surface of the ONO dielectric stack comprises ~~the step of~~ forming a doped polysilicon layer on a surface of the ONO dielectric stack.

18. (Currently Amended) A method according to claim 17, wherein ~~the step of~~ forming a doped polysilicon layer on a surface of the ONO dielectric stack further comprises ~~the step of~~ also forming the doped polysilicon layer on a surface of the oxide layer of the MOS logic transistor to form a high work function gate electrode thereon.

19. (Currently Amended) A method according to claim 18, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, the doped polysilicon layer comprises a P+ dopant, and wherein the method further comprises ~~the steps of~~ patterning the ~~he~~ doped polysilicon layer, the ONO dielectric stack and the oxide layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

20. (Currently Amended) A method according to claim 16, wherein ~~the step of~~ forming an ONO dielectric stack including a multi-layer charge storage layer comprises ~~the steps of~~ forming at least a substantially trap free bottom oxynitride layer followed by forming a charge trapping top oxynitride layer.

21. (New) A method comprising:

forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack comprising a multi-layer charge storage layer including a silicon-rich, oxygen-lean top silicon oxynitride layer and a silicon-rich, oxygen-rich bottom silicon oxynitride layer;

forming a gate oxide on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and

forming a high work function gate electrode on the gate oxide.

22. (New) The method of claim 21, further comprising forming a high work function gate electrode formed over a surface of the ONO dielectric stack of the non-volatile memory transistor.

23. (New) The method of claim 22, wherein forming the ONO dielectric stack comprises forming a trap-rich top silicon oxynitride layer and a substantially trap free silicon bottom oxynitride layer.

24. (New) The method of claim 22, wherein the substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein forming the high work function gate electrode of the non-volatile memory transistor comprises forming a P⁺ doped polysilicon layer to form a nMOS silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor.

25. (New) The method of claim 24, wherein forming the high work function gate electrode of the logic transistor comprises forming a P⁺ doped polysilicon layer to form a pMOS logic transistor.

26. (New) The method of claim 22, wherein the substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein forming the high work function gate electrode of the non-volatile memory transistor comprises forming a N⁺ doped polysilicon layer to form a pMOS silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor.

27. (New) The method of claim 26, wherein forming the high work function gate electrode of the logic transistor comprises forming a N⁺ doped polysilicon layer to form a nMOS logic transistor.

28. (New) The method of claim 22, wherein forming the high work function gate electrode of the non-volatile memory transistor and forming the high work function gate electrode of the logic transistor comprises forming and patterning a single, doped polysilicon layer.

29. (New) The method of claim 21, wherein forming the ONO dielectric stack comprises forming a trap-rich top silicon oxynitride layer and a substantially trap free silicon bottom oxynitride layer.

30. (New) The method of claim 21, wherein the substrate comprises a silicon surface, and wherein forming the high work function gate electrode of the logic transistor comprises forming a P⁺ doped polysilicon layer to form a pMOS logic transistor.

31. (New) The method of claim 21, wherein the substrate comprises a silicon surface, and wherein forming the high work function gate electrode of the logic transistor comprises forming a N⁺ doped polysilicon layer to form a nMOS logic transistor.

32. (New) A method comprising:

forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack comprising a multi-layer charge storage layer including a trap-rich top silicon nitride layer and a substantially trap free silicon bottom nitride layer;

forming a gate oxide on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and

forming a high work function gate electrode on the gate oxide.

33. (New) The method of claim 32, further comprising forming a high work function gate electrode formed over a surface of the ONO dielectric stack of the non-volatile memory transistor.

34. (New) The method of claim 33, wherein forming the high work function gate electrode of the non-volatile memory transistor comprises forming a P+ doped polysilicon layer to form a nMOS silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor, and wherein forming the high work function gate electrode of the logic transistor comprises forming a P+ doped polysilicon layer to form a pMOS logic transistor.

REMARKS

Claims 15-34 are pending. Claims 1-14 have been canceled, claims 15-20 have been amended and claims 21-34 have been added. No new matter has been added, and entry of the amendments and added claims is respectfully requested.

Amendments To The Abstract Of The Disclosure

The amendments to the abstract of the disclosure are supported by claim 15 as originally filed. No new matter is being added, and entry of the amended abstract of the disclosure is respectfully requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, William E. Nuttle at (650) 207-3418.

It is believed no fees are required for filing this amendment. However, if necessary, please *charge any additional fees under 37 CFR §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application*, or apply any credits to our PTO deposit account number: 50-3781.

Respectfully submitted,
Igor Polishchuk, et al.

Dated: November 3, 2011

By: /William E. Nuttle/.
William E. Nuttle, Reg. No. 42,943
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P.O. Box 4240
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Tel.: (650)207-3418

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
First Named Inventor/Applicant Name:		Igor Polishchuk		
Filer:		William Edward Nuttle		
Attorney Docket Number:		PM07027D1		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1250

Electronic Acknowledgement Receipt

EFS ID:	11334482
Application Number:	13288919
International Application Number:	
Confirmation Number:	3343
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	William Edward Nuttle
Filer Authorized By:	
Attorney Docket Number:	PM07027D1
Receipt Date:	03-NOV-2011
Filing Date:	
Time Stamp:	21:33:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1250
RAM confirmation Number	6917
Deposit Account	
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1		PM07027_Pat_App.pdf	201704 436bddd339cdf50388b8956793a82c095a2d8178	yes	29
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	19	
	Claims		20	24	
	Abstract		25	25	
	Drawings-only black and white line drawings		26	29	
Warnings:					
Information:					
2	Oath or Declaration filed	PM07027_Oath.pdf	492568 a223ed30aea1b5312df4dc7e4df6c478137c325	no	9
Warnings:					
Information:					
3	Application Data Sheet	PM07027_ADS.pdf	1906187 befdeabd55945d1c84935d0ceda21e1577f362fe	no	5
Warnings:					
Information:					
4	Preliminary Amendment	PM07027D1_Prelim_Amend.pdf	111948 dff53b970b88d66ca49ab3758f79c0134903f1bb	no	8
Warnings:					
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5	Fee Worksheet (SB06)	fee-info.pdf	33122 930cad5f1ac5a7073d18ff4bf5b66af11db3c8df	no	2
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New International Application Filed with the USPTO as a Receiving Office

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Express Mail Label No.: EB 796954059 US

**MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS
AND A HIGH WORK FUNCTION GATE ELECTRODE**

Inventors:

Igor Polishchuk

Sagy Levy

Krishnaswamy Ramkumar

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 60/940,160, entitled "SONOS Gate Stack With Multiple Oxynitride Layers And A High Workfunction Gate Electrode," filed May 25, 2007, which application is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

5 The present invention relates generally to semiconductor devices, and more particularly to integrated circuits including non-volatile semiconductor memories and methods of fabricating the same.

BACKGROUND OF THE INVENTION

10 Non-volatile semiconductor memories are devices that can be electrically erased and reprogrammed. One type of non-volatile memory that is widely used for general storage and transfer of data in and between computers and other electronic devices is flash memory, such as a split gate flash memory. A split gate flash memory transistor has an architecture similar to that of a conventional logic transistor, such as Metal-
15 Oxide-Semiconductor Field Effect Transistor (MOSFET), in that it also includes a control gate formed over a channel connecting a source and drain in a substrate. However, the memory transistor further includes a memory or charge trapping layer between the control gate and the channel and insulated from both by insulating or dielectric layers. A programming voltage applied to the control gate traps a charge on
20 the charge trapping layer, partially canceling or screening an electric field from the control gate, thereby changing a threshold voltage (V_T) of the transistor and

programming the memory cell. During read-out, this shift in V_T is sensed by the presence or absence of current flow through the channel with application of a predetermined read-out voltage. To erase the memory transistor, an erase voltage is applied to the control gate to restore, or reverse the shift in V_T .

5 An important measure of merit for flash memories is data retention time, which is the time for which the memory transistor can hold charge or remain programmed without the application of power. The charge stored or trapped in the charge trapping layer decreases over time due to leakage current through the insulating layers, thereby reducing the difference between a programmed threshold voltage (VTP) and an erased
10 threshold voltage (VTE) limiting data retention of the memory transistor.

 One problem with conventional memory transistors and methods of forming the same is that the charge trapping layer typically has poor or decreasing data retention over time, limiting the useful transistor lifetime. Referring to FIG. 1A, if the charge trapping layer is silicon (Si) rich there is a large, initial window or difference between
15 VTP, represented by graph or line **102**, and the VTE, represented by line **104**, but the window collapse very rapidly in retention mode to an end of life (EOL **106**) of less than about 1.E+07 seconds.

 Referring to FIG. 1B, if on the other hand the charge trapping layer is if a high quality nitride layer, that is one having a low stoichiometric concentration of Si, the rate
20 of collapse of the window or V_t slope in retention mode is reduced, but the initial program-erase window is also reduced. Moreover, the slope of V_t in retention mode is still appreciably steep and the leakage path is not sufficiently minimized to significantly improve data retention, thus EOL **106** is only moderately improved.

Another problem is that increasingly semiconductor memories combine logic transistors, such as MOSFET's, with memory transistors in integrated circuits (ICs) fabricated on a common substrate for embedded memory or System-On-Chip (SOC) applications. Many of the current processes for forming performance of memory transistors are incompatible with those used for fabricating logic transistors.

Accordingly, there is a need for memory transistors and methods of forming the same that provides improved data retention and increased transistor lifetime. It is further desirable that the methods of forming the memory device are compatible with those for forming logic elements in the same IC formed on a common substrate.

SUMMARY OF THE INVENTION

The present invention provides a solution to these and other problems, and offers further advantages over conventional memory transistors or devices and methods of forming the same.

In a first aspect, the present invention is directed to a non-volatile memory transistor including: (i) an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate; and (ii) high work function gate electrode formed over a surface of the ONO dielectric stack. Preferably, the high work function gate electrode comprises a doped polycrystalline silicon or polysilicon (poly) layer. More preferably, the doped polysilicon layer comprises a P⁺ dopant, such as boron or difluoroborane (BF₂), and the substrate comprises a silicon surface on which the ONO dielectric stack is formed to form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a NMOS SONOS memory transistor.

In certain embodiments, the ONO dielectric stack comprises a multi-layer charge storage layer including at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer. In one version of these embodiments, for example, the top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer, and the bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer.

In another aspect, the present invention is directed to a semiconductor device including both a non-volatile memory transistor and a metal oxide semiconductor (MOS) logic transistor and methods of forming the same. The memory transistor includes an ONO dielectric stack including a multi-layer charge storage layer formed on a surface of a semiconductor substrate, and a high work function gate electrode formed over a surface of the ONO dielectric stack. Preferably, the high work function gate electrode of the memory transistor comprises a doped polysilicon layer. More preferably, the MOS logic transistor also includes a high work function gate electrode formed over a gate oxide on the surface of the substrate.

In one embodiment, the high work function gate electrodes of the memory transistor and the MOS logic transistor comprise a P+ doped polysilicon layer deposited over the ONO stack and gate oxide on a silicon substrate to form an NMOS SONOS memory transistor and a P-type (PMOS) logic transistor. The multi-layer charge storing layer can include, for example, a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer.

In one embodiment, a method of forming such a semiconductor device comprises steps of: (i) forming an ONO dielectric stack on a surface of a semiconductor

substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer; (ii) forming an oxide layer on the surface of the substrate in a second region in which a MOS logic transistor is to be formed; and (iii) forming a high work function gate electrode on a surface of the ONO dielectric stack. Preferably, the step of forming a high work function gate electrode on a surface of the ONO dielectric stack comprises the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack. More preferably, the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack further comprises the step of also forming the doped polysilicon layer on a surface of the oxide layer of the MOS logic transistor form a high work function gate electrode thereon.

In certain embodiments, the semiconductor substrate includes a silicon surface over which the ONO dielectric stack is formed, and the step of forming a doped polysilicon layer comprises the step of forming a P+ doped polysilicon layer to form an NMOS SONOS memory transistor and a PMOS logic transistor. Generally, the polysilicon layer can be doped by ion implantation with boron or BF₂, before or after patterning the polysilicon layer, the ONO dielectric stack and the oxide layer to form gate stacks of the memory transistor and the MOS logic transistor.

In other embodiments, the step of forming the ONO dielectric stack comprises the step of forming a multi-layer charge storage layer overlying a lower or tunnel oxide layer on the surface of the substrate, followed depositing or growing an upper or blocking oxide layer over the multi-layer charge storage layer. Preferably, the step of forming the multi-layer charge storage layer comprises the step of forming a

substantially trap free bottom oxynitride layer followed by forming a charge trapping top oxynitride layer overlying the trap free bottom oxynitride layer. More preferably, the bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer, and the top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer. Optionally, the charge trapping top oxynitride layer formed, for example, in a chemical vapor deposition (CVD) process using a process gas comprising Bis-TertiaryButylAminoSilane (BTBAS) selected to increase a concentration of carbon and thereby the number of traps therein.

BRIEF DESCRIPTION OF THE DRAWINGS

These and various other features and advantages of the present invention will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

FIG. 1A is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a large initial difference between programming and erase voltages but which loses charge quickly;

FIG. 1B is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a smaller initial difference between programming and erase voltages;

FIGs. 2A through 2D are partial cross-sectional side views of a semiconductor device illustrating a process flow for forming a semiconductor device including a logic

transistor and non-volatile memory transistor according to an embodiment of the present invention; and

FIG. 3 is a partial cross-sectional side view of a semiconductor device including a logic transistor and non-volatile memory transistor comprising high work function gate electrodes according to an embodiment of the present invention.

DETAILED DESCRIPTION

The present invention is directed generally to non-volatile memory transistor including a multi-layer charge storage layer and high work function gate electrode to increase data retention and/or to improve programming time and efficiency. The structure and method are particularly useful for embedded memory or System-On-Chip (SOC) applications in which a semiconductor device includes both a logic transistor and non-volatile memory transistor comprising high work function gate electrodes formed on a common substrate.

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures, and techniques are not shown in detail or are shown in block diagram form in order to avoid unnecessarily obscuring an understanding of this description.

Reference in the description to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase “in one embodiment” in various places in the specification do not

necessarily all refer to the same embodiment. The term “to couple” as used herein may include both to directly connect and to indirectly connect through one or more intervening components.

5 Briefly, a non-volatile memory transistor according to the present invention includes a high work function gate electrode formed over an oxide-nitride-oxide (ONO) dielectric stack. By high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased.

10 In certain preferred embodiments, the high work function gate electrode comprises a doped polycrystalline silicon or polysilicon (poly) layer, the fabrication of which can be readily integrated into standard complementary metal-oxide-semiconductor (CMOS) process flows, such as those used fabricate metal-oxide-semiconductor (MOS) logic transistors, to enable fabrication of semiconductor memories or devices including both memory and logic transistors. More preferably, the same doped polysilicon layer can also be patterned to form a high work function gate
15 electrode for the MOS logic transistor, thereby improving the performance of the logic transistor and increasing the efficiency of the fabrication process. Optionally, the ONO dielectric stack includes a multi-layer charge storage or charge trapping layer to further improve performance, and in particular data retention, of the memory transistor.

20 A semiconductor device including a non-volatile memory transistor comprising a high work function gate electrode and methods of forming the same will now be described in detail with reference to FIGs. 2A through 2D, which are partial cross-sectional side views of intermediate structures illustrating a process flow for forming a semiconductor device including both memory and logic transistors. For purposes of

clarity, many of the details of semiconductor fabrication that are widely known and are not relevant to the present invention have been omitted from the following description.

Referring to FIG. 2, fabrication of the semiconductor device begins with formation of an ONO dielectric stack **202** over a surface **204** of a wafer or substrate **206**. Generally, the ONO dielectric stack **202** includes a thin, lower oxide layer or tunneling oxide layer **208** that separates or electrically isolates a charge trapping or storage layer **210** from a channel region (not shown) of the memory transistor in the substrate **206**, and a top or blocking oxide layer **212**. Preferably, as noted above and as shown in FIGs. 2A-2D, the charge storage layer **210** is a multi-layer charge storage layer including at least a top, charge trapping oxynitride layer **210A** and a lower, substantially trap free oxynitride layer **210B**.

Generally, the substrate **206** may include any known silicon-based semiconductor material including silicon, silicon-germanium, silicon-on-insulator, or silicon-on-sapphire substrate. Alternatively, the substrate **206** may include a silicon layer formed on a non-silicon-based semiconductor material, such as gallium-arsenide, germanium, gallium-nitride, or aluminum-phosphide. Preferably, the substrate **206** is a doped or undoped silicon substrate.

The lower oxide layer or tunneling oxide layer **208** of the ONO dielectric stack **202** generally includes a relatively thin layer of silicon dioxide (SiO_2) of from about 15 angstrom ($\text{\AA}$) to about 22 $\text{\AA}$, and more preferably about 18 $\text{\AA}$. The tunneling oxide layer **208** can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using chemical vapor deposition (CVD). In a preferred embodiment, the tunnel oxide layer is formed or grown using a steam anneal. Generally,

the process includes a wet-oxidizing method in which the substrate **206** is placed in a deposition or processing chamber, heated to a temperature from about 700°C to about 850°C, and exposed to a wet vapor for a predetermined period of time selected based on a desired thickness of the finished tunneling oxide layer **208**. Exemplary process times are from about 5 to about 20 minutes. The oxidation can be performed at atmospheric or at low pressure.

In a preferred embodiment, the oxynitride layers **210A**, **210B**, of the multi-layer charge storage layer **210** are formed or deposited in separate steps utilizing different processes and process gases or source materials, and have an overall or combined thickness of from about 70 Å to about 150 Å, and more preferably about 100 Å. The lower, trap free oxynitride layer **210B** can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a process gas including a silicon source, such as silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane (SiH_2Cl_2), tetrachlorosilane (SiCl_4), a nitrogen source, such as nitrogen (N_2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas, such as oxygen (O_2) or N_2O . In one embodiment the trap free oxynitride layer **210B** is deposited in a low pressure CVD process using a process gas including dichlorosilane, NH_3 and N_2O , while maintaining the chamber at a pressure of from about 5 millitorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to

about 7:1, and can be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm).

The top, charge trapping oxynitride layer **210A** can be deposited over the bottom oxynitride layer **210B** in a CVD process using a process gas including Bis-TertiaryButylAminoSilane (BTBAS). It has been found that the use of BTBAS increases the number of deep traps formed in the oxynitride by increasing the carbon level in the charge trapping oxynitride layer **210A**. Moreover, these deep traps reduce charge losses due to thermal emission, thereby further improving data retention. More preferably, the process gas includes BTBAS and ammonia (NH₃) mixed at a predetermined ratio to provide a narrow band gap energy level in the oxynitride charge trapping layer. In particular, the process gas can include BTBAS and NH₃ mixed in a ratio of from about 7:1 to about 1:7. For example, in one embodiment the charge trapping oxynitride layer **210A** is deposited in a low pressure CVD process using BTBAS and ammonia NH₃ at a chamber pressure of from about 5 mT to about 500 mT, and at a substrate temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes.

It has been found that an oxynitride layer produced or deposited under the above conditions yields a trap-rich oxynitride layer **210A**, which improves the program and erase speed and increases of the initial difference (window) between program and erase voltages without compromising a charge loss rate of the memory transistor, thereby extending the operating life (EOL) of the device. Preferably, the charge trapping oxynitride layer **210A** has a charge trap density of at least about 1E10/cm², and more preferably from about 1E12/cm² to about 1E14/cm².

Alternatively, the charge trapping oxynitride layer **210A** can be deposited over the bottom oxynitride layer **210B** in a CVD process using a process gas including BTBAS and substantially not including ammonia (NH₃). In this alternative embodiment of the method, the step of depositing the top, charge trapping oxynitride layer **210A** is followed by a thermal annealing step in a nitrogen atmosphere including nitrous oxide (N₂O), NH₃, and/or nitrogen oxide (NO).

Preferably, the top, charge trapping oxynitride layer **210A** is deposited sequentially in the same CVD tool used to form the bottom, trap free oxynitride layer **210B**, substantially without breaking vacuum on the deposition chamber. More preferably, the charge trapping oxynitride layer **210A** is deposited substantially without altering the temperature to which the substrate **206** was heated during deposition of the trap free oxynitride layer **210B**.

A suitable thickness for the lower, trap free oxynitride layer **210B** has been found to be from about 10 Å to about 80 Å, and a ratio of thicknesses between the bottom layer and the top, charge trapping oxynitride layer has been found to be from about 1:6 to about 6:1, and more preferably at least about 1:4.

The top oxide layer **212** of the ONO dielectric stack **202** includes a relatively thick layer of SiO₂ of from about 20 Å to about 70 Å, and more preferably about 45 Å. The top oxide layer **212** can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using CVD. In a preferred embodiment, the top oxide layer **212** is a high-temperature-oxide (HTO) deposited using CVD process. Generally, the deposition process includes exposing the substrate **308** to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-

containing gas, such as O₂ or N₂O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

Preferably, the top oxide layer **212** is deposited sequentially in the same tool used to form the oxynitride layers **210A**, **210B**. More preferably, the oxynitride layers **210A**, **210B**, and the top oxide layer **212** are formed or deposited in the same tool used to grow the tunneling oxide layer **208**. Suitable tools include, for example, an ONO AVP, commercially available from AVIZA technology of Scotts Valley, California.

Referring to FIG. 2B, in those embodiments in which the semiconductor device is to further include a logic transistor, such as a MOS logic transistor, formed on the surface of the same substrate the ONO dielectric stack **202** is removed from a region or area of the surface **204** in which the logic transistor is to be formed, and an oxide layer **214** the formed thereon.

Generally, the ONO dielectric stack **202** is removed from the desired region or area of the surface **204** using standard photolithographic and oxide etch techniques. For example, in one embodiment a patterned mask layer (not shown) is formed from a photo-resist deposited on the ONO dielectric stack **202**, and the exposed region etched or removed using a low pressure radiofrequency (RF) coupled or generated plasma comprising fluorinated hydrocarbon and/or fluorinated carbon compounds, such as C₂H₂F₄ commonly referred to as Freon[®]. Generally, the processing gas further includes argon (Ar) and nitrogen (N₂) at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

The oxide layer **214** of the logic transistor can include a layer of SiO₂ having a thickness of from about 30 to about 70 Å, and can be thermally grown or deposited using CVD. In one embodiment, the oxide layer **214** is thermally grown using a steam oxidation process, for example, by maintaining the substrate **206** in a steam atmosphere at a temperature of from about 650°C to about 850°C for a period of from about 10 minutes to about 120 minutes.

Next, a doped polysilicon layer is formed on a surface of the ONO dielectric stack **202** and, preferably, the oxide layer **214** of the logic transistor. More preferably, the substrate **206** is a silicon substrate or has a silicon surface on which the ONO dielectric stack is formed to form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a SONOS memory transistor.

Referring to FIG. 2C, forming of the doped polysilicon layer begins with the deposition of a conformal polysilicon layer **216** having a thickness of from about 200 Å to about 2000 Å over the ONO dielectric stack **202** and the oxide layer **214**. The polysilicon layer **216** can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a silicon source or precursor. In one embodiment the polysilicon layer **216** is deposited in a low pressure CVD process using a silicon containing process gas, such as silane or dichlorosilane, and N₂, while maintaining the substrate **206** in a chamber at a pressure of from about 5 to 500 mT, and at a temperature of from about 600°C to about 1000°C for a period of from about 20 minutes to about 100 minutes to a substantially undoped polysilicon layer. The polysilicon layer **216** can be formed or grown directly as a doped polysilicon layer

through the addition of gases such as phosphine, arsine, diborane or difluoroborane (BF₂) to the CVD chamber during the low pressure CVD process.

In one embodiment, the polysilicon layer **216** is doped following the growth or formation in the LPCVD process using ion implantation process. For example, the polysilicon layer **216** can be doped by implanting boron (B⁺) or BF₂ ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm⁻² to about 1e16 cm⁻² to form an N-type (NMOS) SONOS memory transistor and, preferably, a P-type (PMOS) logic transistor having high work function gate electrodes. More preferably, the polysilicon layer **216** is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV.

Alternatively, the polysilicon layer **216** can be doped by ion implantation after patterning or etching the polysilicon layer and the underlying dielectric layers. It will be appreciated that this embodiment includes additional masking steps to protect exposed areas of the substrate **206** surface **204** and/or the dielectric layers from receiving undesired doping. However, generally such a masking step is included in existing process flows regardless of whether the implantation occurs before or after patterning.

Referring to FIG. 2D, the polysilicon layer **216** and the underlying dielectric stack **202** and oxide layer **214** are patterned or etched to form high work function gate electrodes **218** of the memory transistor **220** and logic transistor **222**. In one embodiment polysilicon layer **216** can be etched or patterned using a plasma comprising hydrobromic acid (HBr), chlorine (CL₂) and/or oxygen (O₂) at a pressure of about 25 mTorr, and a power of about 450 W. The oxide layers **208**, **212**, **214**, and oxynitride

layers **210A**, **210B**, can be etched using standard photolithographic and oxide etch techniques as described. For example, in one embodiment the patterned polysilicon layer 216 is used as a mask, and the exposed oxide layers **208**, **212**, **214**, and oxynitride layers **210A**, **210B**, etched or removed using low pressure RF plasma. Generally, the plasma is formed from a processing gas comprising a fluorinated hydrocarbon and/or fluorinated carbon compounds, and further including Ar and N₂ at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

Finally, the substrate is thermal annealed with a single or multiple annealing steps at a temperature of from about 800 °C to about 1050 °C for a time of from about 1second to about 5 minutes to drive in ions implanted in the polysilicon layer **216**, and to repair damage to the crystal structure of the polysilicon layer caused by ion implantation. Alternatively, advanced annealing techniques, such as flash and laser, can be employed with temperatures as high as 1350 °C and anneal times as low as 1 millisecond.

A partial cross-sectional side view of a semiconductor device **300** including a logic transistor **302** and non-volatile memory transistor **304** comprising high work function gate electrodes according to an embodiment of the present invention is shown in FIG. 3. Referring to FIG. 3, the memory transistor **304** is formed on a silicon substrate **306** and comprises a high work function gate electrode **308** formed from a doped polysilicon layer overlying a dielectric stack **310**. The dielectric stack **310** overlies and controls current through a channel region **312** separating heavily doped source and drain (S/D) regions **314**. Preferably, the dielectric stack **310** includes a

tunnel oxide **316**, a multi-layer charge storage layer **318A**, **318B**, and a top or blocking oxide layer **320**. More preferably, the multi-layer charge storage layer **318A**, **318B**, includes at least a top, charge trapping oxynitride layer **318A** and a lower, substantially trap free oxynitride layer **318B**. Optionally, as shown in FIG. 3, the memory transistor **304** further includes one or more sidewall spacers **322** surrounding the gate stack to electrically insulate it from contacts (not shown) to the S/D regions **320** and from other transistors in the semiconductor device formed on the substrate **306**.

The logic transistor **302** comprises a gate electrode **324** overlying an oxide layer **326** formed over a channel region **328** separating heavily doped source and drain regions **330**, and, optionally, can include one or more sidewall spacers **332** surrounding the gate electrically insulate it from contacts (not shown) to the S/D regions. Preferably, as shown in FIG. 3, the gate electrode **324** of the logic transistor **302** also comprises a high work function gate electrode formed from a doped polysilicon layer.

Generally, the semiconductor device **300** further includes a number of isolation structures **334**, such as a local oxidation of silicon (LOCOS) region or structure, a field oxidation region or structure (FOX), or a shallow trench isolation (STI) structure to electrically isolate individual transistors formed on the substrate **306** from one another.

The foregoing description of specific embodiments and examples of the invention have been presented for the purpose of illustration and description, and although the invention has been described and illustrated by certain of the preceding examples, it is not to be construed as being limited thereby. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications, improvements and variations within the scope of the invention are

possible in light of the above teaching. It is intended that the scope of the invention encompass the generic area as herein disclosed, and by the claims appended hereto and their equivalents. The scope of the present invention is defined by the claims, which includes known equivalents and unforeseeable equivalents at the time of filing of this application.

5

IN THE CLAIMS

WHAT IS CLAIMED IS:

1. A non-volatile memory transistor comprising:
an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor
5 substrate; and
high work function gate electrode formed over a surface of the ONO dielectric
stack.
2. A memory transistor according to claim 1, wherein the high work
10 function gate electrode comprises a doped polysilicon layer.
3. A memory transistor according to claim 2, wherein the semiconductor
substrate comprises a silicon surface on which the ONO dielectric stack is formed to
form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a SONOS memory
15 transistor.
4. A memory transistor according to claim 3, wherein the doped polysilicon
layer comprises a P⁺ dopant to form a NMOS SONOS memory transistor.
- 20 5. A memory transistor according to claim 4, wherein the P⁺ dopant
comprises boron or difluoroborane (BF₂).
6. A memory transistor according to claim 1, wherein the ONO dielectric
stack comprises a multi-layer charge storage layer.

7. A memory transistor according to claim 6, wherein the multi-layer charge storing layer comprises at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer.

5

8. A memory transistor according to claim 7, wherein the top oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-lean oxynitride layer, and the bottom oxynitride layer is formed under conditions selected to form a silicon-rich, oxygen-rich oxynitride layer.

10

9. A semiconductor device including a non-volatile memory transistor comprising:

an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate, the ONO dielectric stack including a multi-layer charge storage layer; and

15

a high work function gate electrode formed over a surface of the ONO dielectric stack.

10. A semiconductor device according to claim 9, further comprising a metal oxide semiconductor (MOS) logic transistor including a gate oxide and a high work function gate electrode.

20

11. A semiconductor device according to claim 10, wherein at least one of the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprises a doped polysilicon layer.

5 12. A semiconductor device according to claim 11, wherein the doped polysilicon layer comprises a P+ dopant.

13. A semiconductor device according to claim 12, wherein the P+ dopant comprises boron or difluoroborane (BF₂).

10 14. A semiconductor device according to claim 12, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, and wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the logic transistor comprise a P+
15 doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

20 15. A semiconductor device according to claim 9, wherein the multi-layer charge storing layer comprises at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer.

16. A method of forming a semiconductor device comprising steps of:

forming an oxide-nitride-oxide (ONO) dielectric stack on a surface of a semiconductor substrate in at least a first region in which a non-volatile memory transistor is to be formed, the ONO dielectric stack including a multi-layer charge storage layer;

forming an oxide layer on the surface of the substrate in a second region in which a metal oxide semiconductor (MOS) logic transistor is to be formed; and

forming a high work function gate electrode on a surface of the ONO dielectric stack.

17. A method according to claim 16, wherein step of forming a high work function gate electrode on a surface of the ONO dielectric stack comprises the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack.

18. A method according to claim 17, wherein the step of forming a doped polysilicon layer on a surface of the ONO dielectric stack further comprises the step of also forming the doped polysilicon layer on a surface of the oxide layer of the MOS logic transistor form a high work function gate electrode thereon.

19. A method according to claim 18, wherein the semiconductor substrate comprises a silicon surface over which the ONO dielectric stack is formed, the doped polysilicon layer comprises a P⁺ dopant, and wherein the method further comprises the steps of patterning the he doped polysilicon layer, the ONO dielectric stack and the

oxide layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (PMOS) logic transistor.

- 5 20. A method according to claim 16, wherein the step of forming an ONO dielectric stack including a multi-layer charge storage layer comprises the steps of forming at least a substantially trap free bottom oxynitride layer followed by forming a charge trapping top oxynitride layer.

ABSTRACT OF THE DISCLOSURE

Semiconductor devices including non-volatile memory transistors and methods of fabricating the same to improve performance thereof are provided. In one embodiment, the memory transistor comprises an oxide-nitride-oxide (ONO) stack on a surface of a semiconductor substrate, and a high work function gate electrode formed over a surface of the ONO stack. Preferably, the gate electrode comprises a doped polysilicon layer, and the ONO stack comprises multi-layer charge storing layer including at least a substantially trap free bottom oxynitride layer and a charge trapping top oxynitride layer. More preferably, the device also includes a metal oxide semiconductor (MOS) logic transistor formed on the same substrate, the logic transistor including a gate oxide and a high work function gate electrode. In certain embodiments, the dopant is a P⁺ dopant and the memory transistor comprises N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) transistor while the logic transistor a P-type (PMOS) transistor. Other embodiments are also disclosed.

1/4

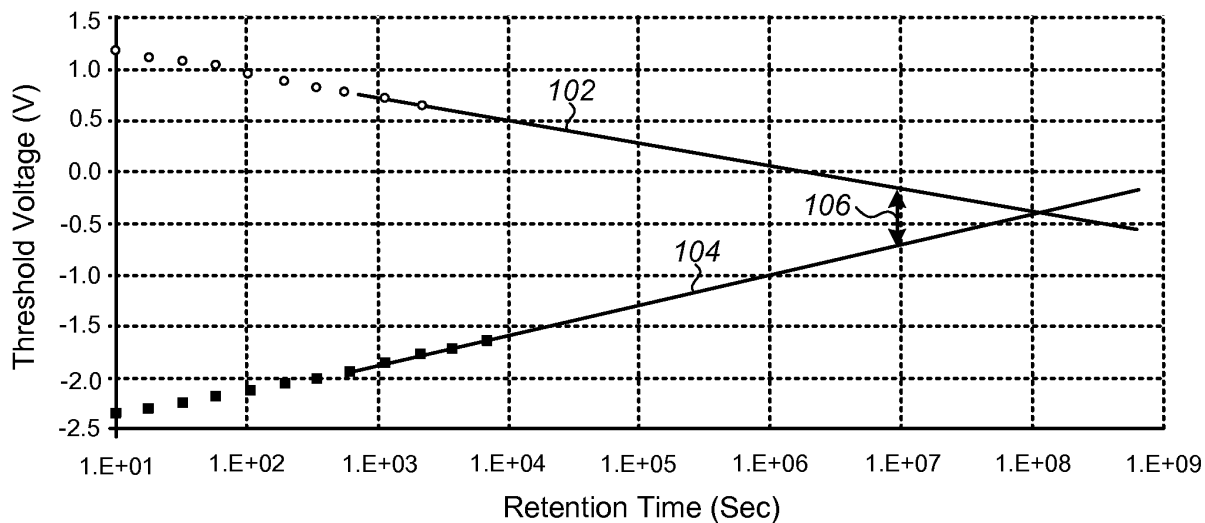


FIG. 1A

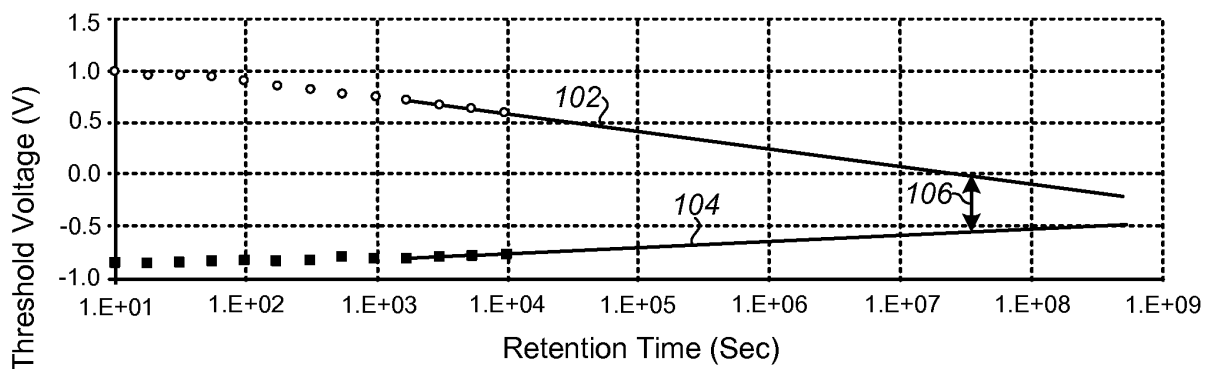


FIG. 1B

2/4

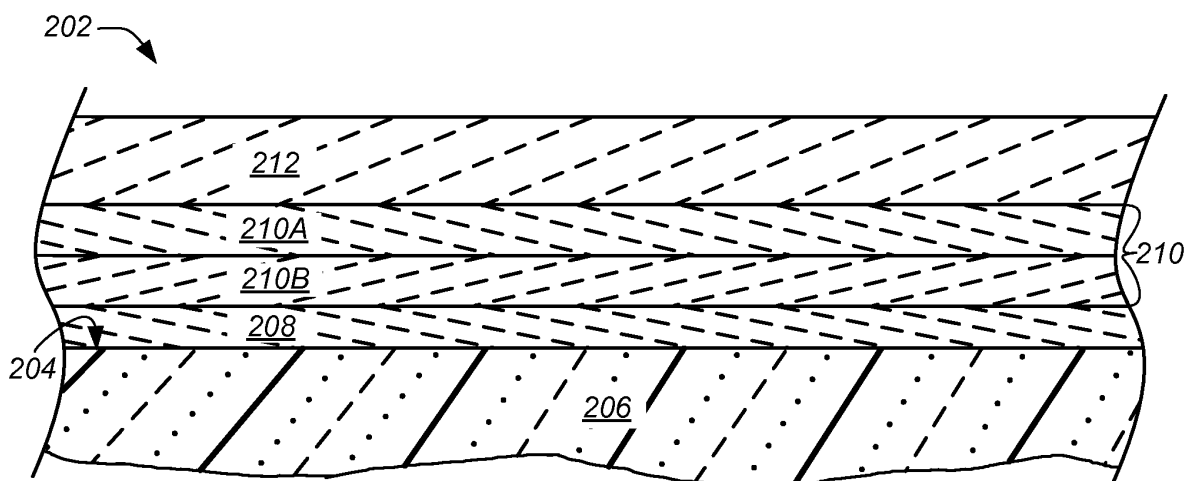


FIG. 2A

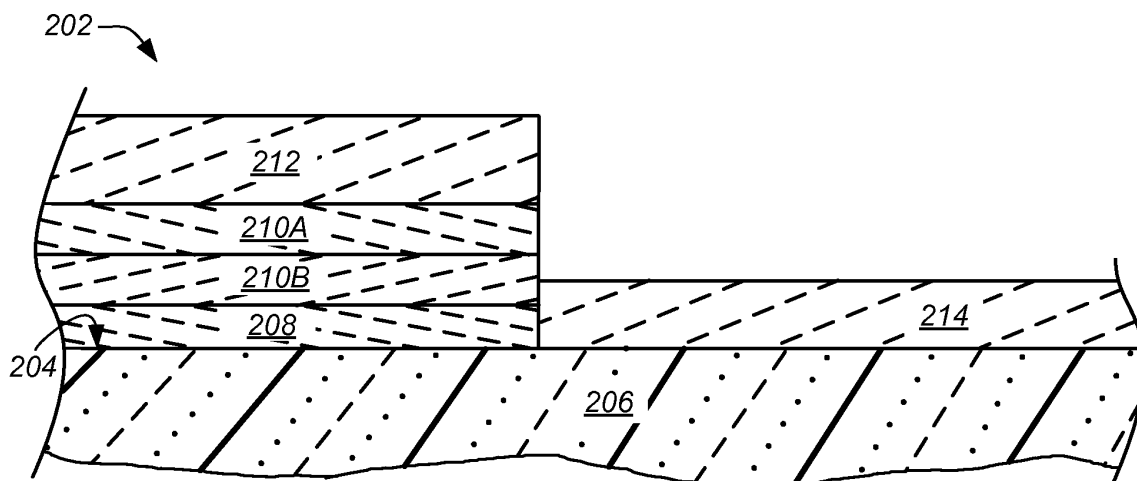


FIG. 2B

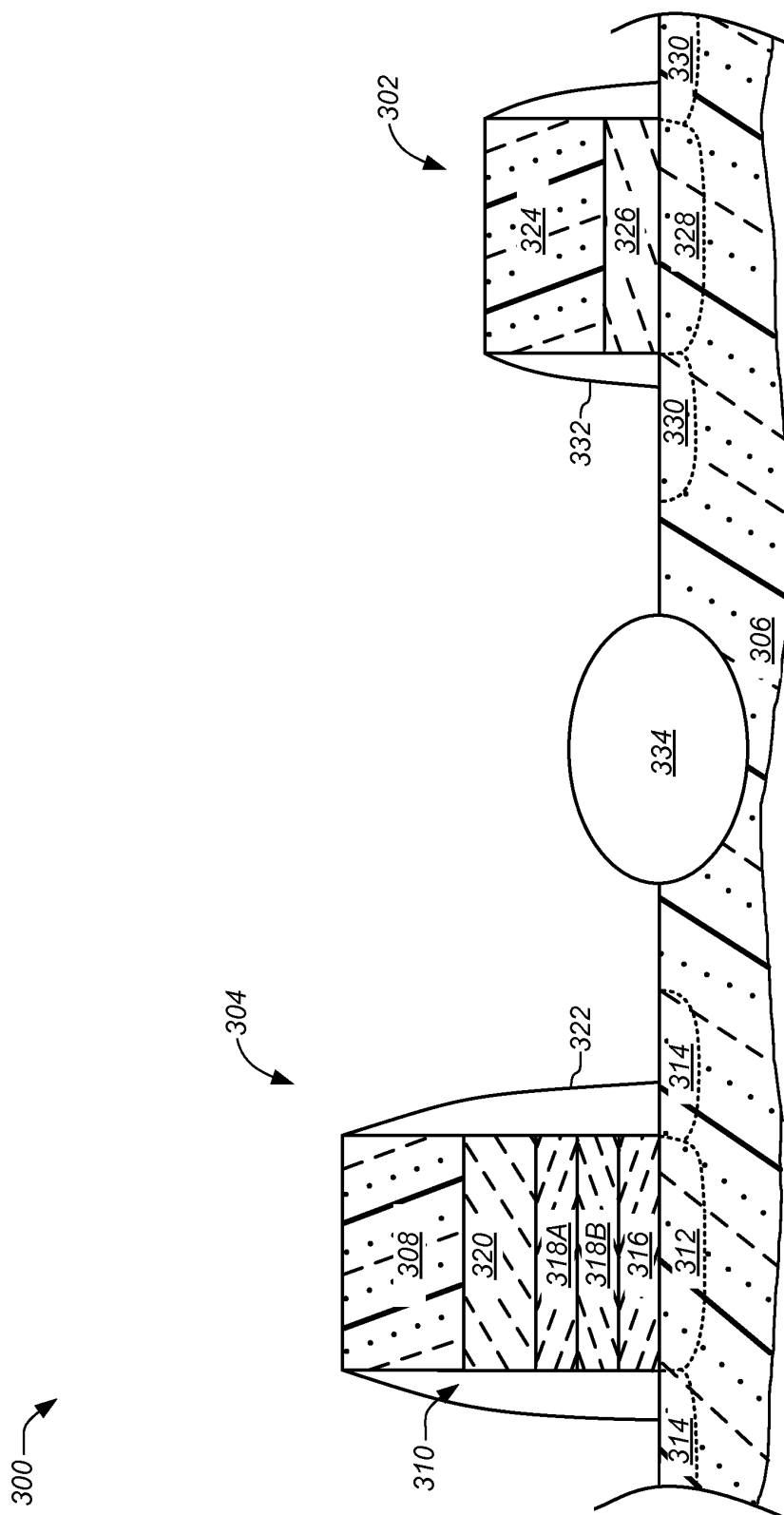


FIG. 3

PTO/SB/01 (07-07)

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First Named Inventor

Igor Polishchuk

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I hereby declare that:

Each inventor's residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH
WORK FUNCTION GATE ELECTRODE**

(Title of the invention)

the specification of which



is attached hereto

OR



was filed on (MM/DD/YYYY)

as United States Application Number or PCT International

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I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

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			☐	☐	☐
			☐	☐	☐
			☐	☐	☐



Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 1 of 2]

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR:

A petition has been filed for this unsigned inventor.

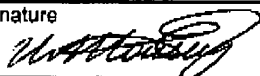
Given Name (first and middle (if any))

Family Name or Surname

Igor

Polishchuk

Inventor's Signature



Date

2/27/08

Residence: City

State

Country

Citizenship

Fremont

CA

U.S.A.

U.S.A.

Mailing Address

43355 Paseo Padre Pkwy.

City

State

Zip

Country

Fremont

CA

94539

U.S.A.



Additional inventors or a legal representative are being named on the 1 supplemental sheet(s) PTO/SB/02A or 02LR attached hereto.

[Page 2 of 2]

PTO/SB/02A (07-07)

Approved for use through 06/30/2010. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet
Page <u>1</u> of <u>1</u>	

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Sagy		Levy	
Inventor's Signature		Date	
Zichron Ya'akov Residence: City	N/A State	Israel Country	Israel Citizenship
44 Yigal-Alon Street Mailing Address			
Zichron Ya'akov City	N/A State	30900 Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Krishnaswamy		Ramkumar	
Inventor's Signature <i>Krishnaswamy</i>		Date <i>3/3/08</i>	
San Jose Residence: City	CA State	U.S.A. Country	U.S.A. Citizenship
1193 Lynbrook Way Mailing Address			
San Jose City	CA State	95129 Zip	U.S.A. Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)		Attorney Docket Number	PM2007027
		First Named Inventor	Igor Polishchuk
		COMPLETE IF KNOWN	
		Application Number	
		Filing Date	5/13/06
☒ Declaration Submitted With Initial Filing OR ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)		Art Unit	
		Examiner Name	

I hereby declare that:

Each inventor's residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

(Title of the Invention)

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) as United States Application Number or PCT International

 Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 1 of 2]

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

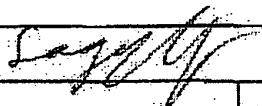
DECLARATION — Utility or Design Patent Application

Direct all correspondence to:	☒ The address associated with Customer Number:	51885	OR	☐ Correspondence address below
Name				
Address				
City		State	ZIP	
Country	Telephone		Email	
WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.				
NAME OF SOLE OR FIRST INVENTOR:		☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))		Family Name or Surname		
Igor		Polishchuk		
Inventor's Signature			Date	
Residence: City	State	Country	Citizenship	
Fremont	CA	U.S.A.	U.S.A.	
Mailing Address				
43355 Paseo Padre Pkwy.				
City	State	Zip	Country	
Fremont.	CA	94539	U.S.A.	
☒ Additional inventors or a legal representative are being named on the 1 supplemental sheet(s) PTO/SB/02A or 02LR attached hereto.				

[Page 2 of 2]

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet
	Page <u>1</u> of <u>1</u>

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Sagy		Levy	
Inventor's Signature 		Date <u>03/10/08</u>	
Zichron Ya'akov Residence: City	N/A State	Israel Country	Israel Citizenship
44 Yigal-Alon Street			
Mailing Address			
Zichron Ya'akov City	N/A State	30900 Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Krishnaswamy		Ramkumar	
Inventor's Signature		Date	
San Jose Residence: City	CA State	U.S.A. Country	U.S.A. Citizenship
1193 Lynbrook Way			
Mailing Address			
San Jose City	CA State	95129 Zip	U.S.A. Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/81 (01-06)

Approved for use through 12/31/2008. OMB 0651-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**POWER OF ATTORNEY
and
CORRESPONDENCE ADDRESS
INDICATION FORM**

Application Number	not yet known
Filing Date	5/13/08
First Named Inventor	Igor Polishchuk
Title	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Art Unit	unknown
Examiner Name	unknown
Attorney Docket Number	PM2007027

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint:

☒ Practitioners associated with the Customer

Number:

51885

OR

☐ Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or
Individual Name

Address

City

State

ZIP

Country

Telephone

Fax

I am the:

☒ Applicant/Inventor.☐ Assignee of record of the entire interest. See 37 CFR 3.71.

Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature	<i>Igor Polishchuk</i>	Date	02/27/08
Name	Igor Polishchuk	Telephone	408 545 7149
Title and Company	Cypress Semiconductor		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ *Total of 3 forms are submitted.

This collection of information is required by 37 CFR 1.31 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS, SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO/SB/01 (01-08)

Approved for use through 12/31/2008. OMB 0851-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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**POWER OF ATTORNEY
and
CORRESPONDENCE ADDRESS
INDICATION FORM**

Application Number	not yet known
Filing Date	5-13-08
First Named Inventor	Igor Polishchuk
Title	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
Art Unit	unknown
Examiner Name	unknown
Attorney Docket Number	PM2007027

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint:

☒ Practitioners associated with the Customer
Number:

51885

OR

☐ Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or
Individual Name

Address

City

State

ZIP

Country

Telephone

Fax

I am the:

☒ Applicant/Inventor.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.

Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/06)

SIGNATURE of Applicant or Assignee of Record

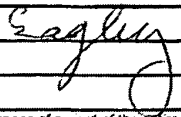
Signature	<i>Krishnaswamy Ramkumar</i>	Date	3/3/08
Name	Krishnaswamy Ramkumar	Telephone	
Title and Company	Sr. Member of Technical Staff: Cypress Semiconductor		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ *Total of 3 forms are submitted.

This collection of information is required by 37 CFR 1.31 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION FORM	Application Number	not yet known
	Filing Date	5-13-06
	First Named Inventor	Igor Polishchuk
	Title	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
	Art Unit	unknown
	Examiner Name	unknown
	Attorney Docket Number	PM2007027

I hereby revoke all previous powers of attorney given in the above-identified application.											
I hereby appoint:											
☒ Practitioners associated with the Customer Number:		51885									
OR											
☐ Practitioner(s) named below:											
<table border="1"><thead><tr><th>Name</th><th>Registration Number</th></tr></thead><tbody><tr><td> </td><td> </td></tr><tr><td> </td><td> </td></tr><tr><td> </td><td> </td></tr></tbody></table>		Name	Registration Number								
Name	Registration Number										
as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.											
Please recognize or change the correspondence address for the above-identified application to:											
☒ The address associated with the above-mentioned Customer Number											
OR											
☐ The address associated with Customer Number:											
OR											
☐ Firm or Individual Name											
Address											
City	State	ZIP									
Country											
Telephone	Fax										
I am the:											
☒ Applicant/Inventor.											
☐ Assignee of record of the entire interest. See 37 CFR 3.71.											
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)											
SIGNATURE of Applicant or Assignee of Record											
Signature		Date	March-10-08								
Name	Sagy Levy	Telephone									
Title and Company											
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.											
☒ *Total of 3 forms are submitted.											

This collection of information is required by 37 CFR 1.31 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	PM07027D1
		Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
Mr.	IGOR		POLISHCHUK		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Fremont	State/Province	CA	Country of Residence i	US
Citizenship under 37 CFR 1.41(b) i		US			
Mailing Address of Applicant:					
Address 1		43355 Paseo Padre Pkwy.			
Address 2					
City	Fremont	State/Province	CA		
Postal Code	94539	Country i	US		
Applicant 2					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
Mr.	Sagy		LEVY		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Zichron Ya'aqov	State/Province		Country of Residence i	IL
Citizenship under 37 CFR 1.41(b) i		US			
Mailing Address of Applicant:					
Address 1		44 Yigal-Alon Street			
Address 2					
City	Zichron Ya'aqov	State/Province			
Postal Code	30900	Country i	IL		
Applicant 3					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
Dr.	Krishnaswamy		RAMKUMAR		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	San Jose	State/Province	CA	Country of Residence i	US

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	PM07027D1
		Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		

Citizenship under 37 CFR 1.41(b) i		US	
Mailing Address of Applicant:			
Address 1	1193 Lynbrook Way		
Address 2			
City	San Jose	State/Province	CA
Postal Code	95129	Country	US
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.			Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	60909		
Email Address	pbj@cypress.com	Add Email	Remove Email
Email Address	larz@cypress.com	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
Attorney Docket Number	PM07027D1	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☒ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.
--

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	PM07027D1
		Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	60909		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	12152518	2008-05-13
Prior Application Status	Abandoned	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12152518	non provisional of	60940160	2007-05-25
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove		
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)
		☐ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.		Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1		Remove	
If the Assignee is an Organization check here. ☒			
Organization Name	Cypress Semiconductor Corporation		
Mailing Address Information:			
Address 1	198 Champion Court		
Address 2			
City	San Jose	State/Province	CA
Country ⁱ	US	Postal Code	95134
Phone Number	408-545-7194	Fax Number	408-545-6911

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	PM07027D1
		Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
Email Address	larz@cypress.com		
Additional Assignee Data may be generated within this form by selecting the Add button.		Add	

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/William Nuttle/			Date (YYYY-MM-DD)	2011-11-03
First Name	William	Last Name	Nuttle	Registration Number	42943

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/288,919		Filing Date 11/03/2011		☐ To be Mailed	
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APPLICATION AS FILED – PART I						OTHER THAN SMALL ENTITY			
(Column 1)		(Column 2)		SMALL ENTITY ☐		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)		
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380		
☒ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	620		
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250		
TOTAL CLAIMS (37 CFR 1.16(i))	19 minus 20 =	* 0	X \$ =		OR	X \$60 =	0		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	* 0	X \$ =		OR	X \$250 =	0		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
			TOTAL		TOTAL	1250			

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II						OTHER THAN SMALL ENTITY					
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	11/03/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X \$ =		OR	X \$60 =	0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$ =		OR	X \$250 =	0	
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	

(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/GLORIA NORRIS/

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