UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,633,537 B2
APPLICATION NO. : 13/539466
DATED : January 21, 2014
INVENTOR(S) : Igor Polishchuk et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification

Column 17, Line 40, "FIGS. 20A-F" to read as --FIGS. 10A-F--.

Signed and Sealed this
Fifth Day of June, 2018

Andrei Iancu
Director of the United States Patent and Trademark Office

PTO/SB/44 (09-07)
Approved for use through 01/31/2020. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,633,537

APPLICATION NO.: 13/539,466

ISSUE DATE : 01-21-2014

INVENTOR(S) : Igor Polishchuk, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 17, line 40, “FIGS. 20A-F” to read as --FIGS. 10A-F--.

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13539466
Filing Date:	01-Jul-2012
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Attorney Docket Number:	PM07027D1CIP1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
CERTIFICATE OF CORRECTION	1811	1	150	150

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**150**

Electronic Acknowledgement Receipt	
EFS ID:	32522137
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Daniel Pheng
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	03-MAY-2018
Filing Date:	01-JUL-2012
Time Stamp:	12:58:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$150
RAM confirmation Number	050318INTEFSW00012503503781
Deposit Account	503781
Authorized User	Timothy Croll
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	PM07027D1CIP1_RequestforCertofCorrect_05022018.pdf	82719 85e149cb4fc907a32e9746479861d0113ba9d0d8	no	3
Warnings:					
Information:					
2	Request for Certificate of Correction	PM07027D1CIP1_CertificateofCorrectionForm_sb0044_05022018.pdf	153196 9c2a479c181c0e1ffb26c8f9bc4689ebf49e21b2	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30462 84e727b77e608591903c8eb37c3b1f5e73ab69d7	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	266377		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Examiner: YUSHIN, NIKOLAY K
U.S. Patent No. 8,633,537	Art Group: 2893
Application No.: 13/539,466	Confirmation No.: 5842
Filed: July 01, 2012	
For: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Mail Stop Certificate of Corrections Branch
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

HONORABLE COMMISSIONER OF PATENTS & TRADEMARKS

Sir/Madame:

The following is a request for a certificate of correction in Serial Number 13/539,466, now U.S. Patent Number 8,633,537, under 35 USC 255, due to an error that appears in the printed patent due to a clerical mistake (typographical error). Enclosed please also find a PTO/SB/44 CERTIFICATE OF CORRECTION form and Certificate of Correction Fee Code 1811.

Sandisk Technologies, Inc. - Ex. 1040, Page 000008

In the Specifications

Column 17, line 40, “FIGS. 20A-F” to read as --FIGS. 10A-F--.

Sandisk Technologies, Inc. - Ex. 1040, Page 000009

Should the Examiner have any questions regarding this request, the Examiner is urged to contact the undersigned by telephone at (408) 545-6950. All correspondence should continue to be directed to the address given below.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required, and to credit any overpayments, to Deposit Account No. 50-3781.

Respectfully Submitted,

Date: 05/02/2018

___/Kin Hung Lai/____
Kin Hung Lai
Registration No. 69,251

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Sandisk Technologies, Inc. - Ex. 1040, Page 000010

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	01/21/2014	8633537	PM07027D1CIP1	5842

60909 7590 12/31/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 136 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Igor POLISHCHUK, Fremont, CA;
Sagy LEVY, Zichron-Yoakev, ISRAEL;
Krishnaswamy RAMKUMAR, San Jose, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 11/13/2013
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	02/13/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Cypress Semiconductor Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): San Jose, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 503781 (enclose an extra copy of this form).

Sandisk Technologies, Inc. - Ex. 1040, Page 000012

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Larry J. Johnson/ Date 12/16/2013

Typed or printed name Larry J. Johnson Registration No. 56861

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	13539466
Filing Date:	01-Jul-2012
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Filer:	Larry Joel Johnson/Alma Fazlic
Attorney Docket Number:	PM07027D1CIP1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2080**

Electronic Acknowledgement Receipt	
EFS ID:	17674190
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Customer Number:	60909
Filer:	Larry Joel Johnson/Alma Fazlic
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	16-DEC-2013
Filing Date:	01-JUL-2012
Time Stamp:	18:05:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2080
RAM confirmation Number	6632
Deposit Account	503781
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	PM07027D1CIP1_IssueFeeLetter_12162013.pdf	17673 4a10b66ebb45118a4bf7b24927be3be71233cf20	no	2
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	PM07027D1CIP1_IssueFee_12162013.pdf	108864 b582d9128e6e3bcf0ad83c25efa73ce6ab6447b4	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	32297 d7ccaf0f2638992c18e47c41366400ca9a521f06	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	158834		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Examiner: YUSHIN, NIKOLAY K
Igor POLISHCHUK	)	Group Art Unit: 2893
Application No.: 13/539,466	)	Confirmation No.: 5842
Filed: 07-01-2012	)	
For: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	)	

ISSUE FEE TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant is in receipt of a Notice of Allowance and Fees Due Form, mailed November 13, 2013 in connection with the above-identified application. The Issue Fee/Publication Fee is due on or before February 13, 2014. Applicant hereby submits the Issue Fee/Publication Fee.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.19, 1.20 and 1.21 that may be required to issue the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Customer No.: 60909

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry J. Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

Dated: 12/16/2013

By: /Larry J. Johnson/
Larry J. Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Customer No.: 60909

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1

CONFIRMATION NO. 5842

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

PUBLICATION NOTICE



Title:MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Publication No.US-2013-0307053-A1
Publication Date:11/21/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Sandisk Technologies, Inc. - Ex. 1040, Page 000020

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 11/13/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/13/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	02/13/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1040, Page 000021

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 11/13/2013
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	02/13/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Sandisk Technologies, Inc. - Ex. 1040, Page 000022

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

60909 7590 11/13/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/13/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 136 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 136 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1040, Page 000024

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notices of Allowance and Fee(s) Due mailed between October 1, 2013 and December 31, 2013

(Addendum to PTOL-85)

If the "Notice of Allowance and Fee(s) Due" has a mailing date on or after October 1, 2013 and before January 1, 2014, the following information is applicable to this application.

If the issue fee is being timely paid on or after January 1, 2014, the amount due is the issue fee and publication fee in effect January 1, 2014. On January 1, 2014, the issue fees set forth in 37 CFR 1.18 decrease significantly and the publication fee set forth in 37 CFR 1.18(d)(1) decreases to $0.

If an issue fee or publication fee has been previously paid in this application, applicant is not entitled to a refund of the difference between the amount paid and the amount in effect on January 1, 2014.

Notice of Allowability	Application No. 13/539,466	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed on 09/27/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-5 and 7-20* . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/27/2013
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 09/27/2013 has been entered.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 09/27/2013 was filed after the mailing date of the Notice of Allowance on 11/27/2012. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

Claims 1-5 and 7-20 stand allowed for the reasons articulated in the Office Action mailed on 11/27/2013.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Friday from 8 a.m. to 5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	Art Unit
	NIKOLAY YUSHIN	2893

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	314, 324, E29.132; E29.309	09/26/2012	NY

SEARCH NOTES		
Search Notes	Date	Examiner
Keyword, inventor names, assignee searching - see search history	09/26/2012	NY
Updated keyword searching - see search history	11/14/2012	NY
Updated keyword searching - see search history	08/26/2013	NY
References from IDSs filed on 12/21/2012; 04/19/2013; 06/05/2013; 06/05/2013	08/26/2013	NY
Updated keyword searching - see search history	11/04/2013	NY

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	324	11/14/2012	NY

	/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

CPC		
Symbol	**Type**	**Version**

CPC Combination Sets				
Symbol	**Type**	**Set**	**Ranking**	**Version**

(Assistant Examiner)	(Date)	**Total Claims Allowed:** 19	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893	11/04/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
257	324	H	0	1	L	29 / 792 (2006.01.01)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	E29.132	E29.309			

(Assistant Examiner)	(Date)	Total Claims Allowed: 19	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893	11/04/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	13	17												
2	2	17	18												
6	3	18	19												
7	4	19	20												
8	5														
	6														
3	7														
4	8														
5	9														
9	10														
10	11														
14	12														
15	13														
16	14														
11	15														
12	16														

(Assistant Examiner)	(Date)	**Total Claims Allowed:** 19	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893	11/04/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8A

Sandisk Technologies, Inc. - Ex. 1040, Page 000033

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5842

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/539,466	07/01/2012	257	2893	PM07027D1CIP1

APPLICANTS

Igor POLISHCHUK, Fremont, CA;
Sagy LEVY, Zichron-Yoakev, ISRAEL;
Krishnaswamy RAMKUMAR, San Jose, CA;

**** CONTINUING DATA ***************************

This application is a CIP of 13/288,919 11/03/2011
which is a DIV of 12/152,518 05/13/2008 PAT 8063434
which claims benefit of 60/940,160 05/25/2007

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

07/16/2012

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/NIKOLAY K YUSHIN/ Examiner's Signature	☐ Initials	CA	13	20	3

ADDRESS

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709
UNITED STATES

TITLE

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

FILING FEE RECEIVED		
1630	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Sandisk Technologies, Inc. - Ex. 1040, Page 000034

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
If you wish to add additional U.S. Patent citation information please click the Add button.						Add

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
If you wish to add additional U.S. Published Application citation information please click the Add button.						Add

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								Add

NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

/N.Y./	1	USPTO Advisory Action for Application Number 13/114,889 (PM07031D1) dated 08/02/2013; 2 pages	☐
/N.Y./	2	USPTO Non Final Rejection for Application Number 13/114,889 (PM07031D1) dated 09/05/2013; 11 pages	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Nikolay Yushin/	Date Considered	11/04/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature		Date (YYYY-MM-DD)	
Name/Print	Larry Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25	((IGOR) near2 (POLISHCHUK)).INV.	US-PGPUB; USPAT	AND	ON	2013/11/04 10:02
L2	38	((SAGY) near2 (LEVY)).INV.	US-PGPUB; USPAT	AND	ON	2013/11/04 10:02
L3	99	((KRISHNASWAMY) near2 (RAMKUMAR)).INV.	US-PGPUB; USPAT	AND	ON	2013/11/04 10:02
L4	91	(L1 OR L2 OR L3) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2013/11/04 10:02
L5	75	(L1 OR L2 OR L3) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	USPAT	AND	ON	2013/11/04 10:03
L6	5	("20060198190" | "6114734" | "6677213" | "6686242" | "7042054").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2013/11/04 10:04
L7	5	("5972765" | "6023093" | "6114734" | "6140187" | "6147014").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2013/11/04 10:04
L8	18	("20070139395" | "20080225015" | "20090051863" | "20090159344" | "20100044122" | "20100045632" | "20100182275" | "20100224424" | "20100292945" | "20100302206" | "20100328255" | "20110261003" | "20120229417" | "7663607" | "7920129" | "7940251" | "7965281" | "8217916").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2013/11/04 10:05
L9	97	("20020058410" | "20020142500" | "20030020111" | "20030143808" | "20040029354" | "20040214448" | "20040248393" | "20050287823" | "5045488" | "5385866" | "5387540" | "5393685" | "5633523" | "5670431" | "5721090" | "5756392" | "5798296" | "5817579" | "5837585" | "5877074" | "5937289" | "5939763" | "6002615" | "6087063" | "6107135" | "6115321" | "6117795" | "6121124" | "6127227" | "6133093" | "6137780" | "6165884" | "6177334" | "6180453" | "6188136" | "6194128" | "6207506" | "6207542" | "6232163" | "6245652" | "6248628" | "6258677" | "6274467" | "6277200" | "6278129" | "6284633" | "6287913" | "6303482" | "6303483" | "6306743" | "6342452" | "6372672" | "6380008" |	US-PGPUB; USPAT; USOCR	AND	ON	2013/11/04 10:06

Sandisk Technologies, Inc. - Ex. 1040, Page 000039

		"6410428" | "6420250" | "6429135" | "6429496" | "6448140" | "6451647" | "6465370" | "6465837" | "6479405" | "6486020" | "6506647" | "6528431" | "6541830" | "6542424" | "6552401" | "6559007" | "6602746" | "6617636" | "6624068" | "6635185" | "6680516" | "6686242" | "6686243" | "6686617" | "6706613" | "6713780" | "6728142" | "6740566" | "6767834" | "6797575" | "6800543" | "6803321" | "6812529" | "6828634" | "6833310" | "6897120" | "6984575" | "7041584" | "7060558" | "7192887" | "7229929" | "7252773" | "7351663" | "7371637").PN.				
S1	1	("8063434").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 09:50
S2	18	("20030122204" | "20050230766" | "20060131636" | "20070246753" | "20070262451" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080290399" | "20100041222" | "20100295118" | "6906390" | "6912163" | "7312496" | "7323742" | "7737488" | "7790516").PN. OR ("8063434").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 09:51
S3	19	((IGOR) near2 (POLISHCHUK)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:01
S4	7	("20010012667" | "20030178675" | "20030232507" | "20040082198" | "20100090294" | "20100167506" | "7799670").PN. OR ("8163660").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:04
S5	34	((SAGY) near2 (LEVY)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:05
S6	88	((KRISHNASWAMY) near2 (RAMKUMAR)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:07
S7	8	("20070029625" | "20070031999" | "20080286927" | "20090039414" | "7315474" | "7576386" | "7636257" | "7646637").PN. OR ("8222688").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:10
S8	78	(S3 OR S5 OR S6) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:19
S9	1	((oxide$1nitride$1nitride$1oxide OR ONNO) NEAR4 stack) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:28
S10	1	((oxide$1nitride$1nitride$1oxide OR ONNO) NEAR4 stack)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30
S11	655	((oxide$1nitride$1nitride$1oxide OR ONNO))	US-PGPUB; USPAT;	AND	ON	2012/09/26 10:30

Sandisk Technologies, Inc. - Ex. 1040, Page 000040

			USOCR			
S12	292	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30
S13	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (oxygen$1rich) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:31
S14	0	((oxide$1nitride$1nitride$1oxide OR ONNO)) SAME (oxygen$1rich)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:12
S15	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (oxygen$1rich)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:12
S16	0	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S2	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S17	1	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S8	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S18	1	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S6	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S19	2	(("6906390") or ("6912163")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 11:16
S20	29727	((oxide$1nitride$11oxide OR ONO)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S21	135	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S22	59	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S23	46	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:21
S24	46	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S23	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:21
S25	41	("4173766" | "5168334" | "5349221" | "5644533" | "5751037" | "5768192" | "5825686" | "5963465" | "5966603" | "6001709" | "6011725" | "6030871" | "6117730" | "6287917" | "6326268").PN. OR ("6465306").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:31

Sandisk Technologies, Inc. - Ex. 1040, Page 000041

S26	17	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) (substrate NEAR4 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:46
S27	6	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) (channel NEAR4 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:47
S28	467	((oxide$1nitride$11oxide OR ONO)) (channel NEAR2 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:48
S29	60	((oxide$1nitride$11oxide OR ONO)) (channel NEAR2 polysilicon)	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 11:49
S30	91	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory channel	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:02
S31	0	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) Near3 channel))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S32	1	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) NEAR3 substrate))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S33	2	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) SAME substrate))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S34	3	((oxide$1nitride$1nitride$1oxide OR ONNO)) (OXYGEN same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:16
S35	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (OXYGEN$1RICH same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:17
S36	256	(OXYGEN$1RICH same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:19
S37	119	(OXYGEN$1RICH same NITRIDE) MEMORY CHANNEL	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:20
S38	11	(OXYGEN$1RICH same NITRIDE) MEMORY (POLYSILICON near4 CHANNEL)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:20
S39	8	(OXYGEN$1RICH same NITRIDE) MEMORY (logic near4 MOS)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:45
S40	29	("20030227049" | "20040071030" | "20040129986" | "20050186741" | "20060202263" | "20060226490" |	US-PGPUB; USPAT;	AND	ON	2012/09/26 12:51

Sandisk Technologies, Inc. - Ex. 1040, Page 000042

		"20060281331" | "4843023" | "5405791" | "5573963" | "5793089" | "5861347" | "6025267" | "6074915" | "6174774" | "6277683" | "6429081" | "6599795" | "6730566" | "6946349" | "7015100" | "7045424" | "7098154" | "7172940" | "7250654" | "7253046" | "7262457" | "7544565" | "7588986").PN. OR ("8143129").URPN.	USOCR			
S41	29	("20030227049" | "20040071030" | "20040129986" | "20050186741" | "20060202263" | "20060226490" | "20060281331" | "4843023" | "5405791" | "5573963" | "5793089" | "5861347" | "6025267" | "6074915" | "6174774" | "6277683" | "6429081" | "6599795" | "6730566" | "6946349" | "7015100" | "7045424" | "7098154" | "7172940" | "7250654" | "7253046" | "7262457" | "7544565" | "7588986").PN. OR ("8143129").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:51
S42	20	(PMOS SAME SONOS SAME memory) (NMOS SAME logic)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:58
S43	11	(PMOS SAME SONOS SAME memory) (NMOS SAME logic) (polysilicon adj gate)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:59
S48	5	(high$1K NEAR4 (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 13:23
S49	51	(high$1K SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 13:25
S50	976	(dielectric SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:29
S51	151	((dielectric adj constant) SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:29
S52	41	((high adj dielectric adj constant) SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:30
S53	2691	257/314.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:41
S54	11	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S53	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:42
S55	13	(((oxide$1nitride$11oxide OR ONO)) ((oxygen$1rich) SAME nitride)) S53	US-PGPUB; USPAT;	AND	ON	2012/09/26 14:43

Sandisk Technologies, Inc. - Ex. 1040, Page 000043

			USOCR			
S56	2404	257/324.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:44
S57	24	(((oxide$1nitride$11oxide OR ONO)) ((oxygen$1rich) SAME nitride)) S56	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:44
S58	9	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S56	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:45
S59	13	("20060261401" | "20080258203" | "6709928" | "20030123307" | "6445030" | "7450423" | "7042054" | "4543707" | "6157426" | "6677213" | "6958511" | "20020154878" | "6818558").PN.	US-PGPUB; USPAT	AND	ON	2012/09/26 14:48
S60	186	257/E29.132.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:04
S61	1	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S60	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:05
S62	2	((oxide$1nitride$11oxide OR ONO) (oxygen$1rich SAME nitride)) S60	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:05
S63	2	((oxide$1nitride$11oxide OR ONO) oxygen$1rich nitride) S60	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
S64	2536	257/E29.309.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
S65	11	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S64	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
S66	11	((oxide$1nitride$11oxide OR ONO)) (channel SAME (recrystallized adj polysilicon))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:08
S67	20	((oxide$1nitride$11oxide OR ONO)) (channel SAME (silicon adj nano$1wire))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:10
S68	1	("20100117138").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:03
S69	1	("6093596").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:22

Sandisk Technologies, Inc. - Ex. 1040, Page 000044

S70	1	("6093590").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:22
S71	2278	((high adj dielectric adj constant) SAME (tantalum adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:28
S72	2278	((high adj dielectric adj constant) SAME (high adj dielectric adj constant) SAME (tantalum adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:29
S73	1480	S72 memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:29
S74	280	(((oxide$1nitride$11oxide OR ONO))) S73	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:30
S75	274	((oxide$1nitride$11oxide OR ONO) nitride) S73	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:31
S76	230	((oxide$1nitride$11oxide OR ONO) nitride) AND S73	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 16:31
S77	196	transistor S76	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:32
S78	20	((oxide$1nitride$11oxide OR ONO) nitride transistor) AND S73	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 16:32
S79	47	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/11/14 09:54
S80	6	("20050287763" | "20060202263" | "6274901" | "7067377").PN. OR ("7732276").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/11/14 09:56
S81	18	("20030122204" | "20050230766" | "20060131636" | "20070246753" | "20070262451" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080290399" | "20100041222" | "20100295118" | "6906390" | "6912163" | "7312496" | "7323742" | "7737488" | "7790516").PN. OR ("8063434").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/11/14 09:57
S94	25	((IGOR) near2 (POLISHCHUK)).INV.	US-PGPUB; USPAT	AND	ON	2013/08/26 08:39
S95	38	((SAGY) near2 (LEVY)).INV.	US-PGPUB; USPAT	AND	ON	2013/08/26 08:39

Sandisk Technologies, Inc. - Ex. 1040, Page 000045

S96	98	((KRISHNASWAMY) near2 (RAMKUMAR)).INV.	US-PGPUB; USPAT	AND	ON	2013/08/26 08:39
S97	90	(S94 OR S95 OR S96) ((OPTIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2013/08/26 08:39
S98	1	("20090152621").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2013/08/26 08:41
S99	59	(("6429081") or ("6946349") or ("8283261") or ("8318608") or ("20060281331") or ("20060081331") or ("20070066087") or ("5817170") or ("6015739") or ("6153543") or ("6214689") or ("6461899") or ("6586349") or ("6610614") or ("6818558") or ("6906390") or ("7112486") or ("7312496") or ("7323742") or ("7365389") or ("7463530") or ("7576386") or ("7670963") or ("7737488") or ("7790516") or ("20010052615") or ("20020020890") or ("20030122204") or ("2003183869") or ("20040173918") or ("20040094793") or ("20040104424") or ("200400251489") or ("20040094793") or ("20040104424") or ("20040251489") or ("20050070126") or ("2005026637") or ("20050266637") or ("20050093054") or ("20050098839") or ("20050141168") or ("20050205920") or ("20050230765") or ("20050245034") or ("20050275012") or ("20050245034") or ("20060111805") or ("20060113586") or ("20060113627") or ("200600131636") or ("200600220106") or ("200600051880") or ("200600065919") or ("200600113627") or ("200700513006") or ("20070048916") or ("20070049048") or ("20070246753") or ("20070262451") or ("20070267687") or ("20070268753") or ("20070272916") or ("20070048916") or ("20080029399") or ("20080009115") or ("20080150003") or ("20080237694") or ("20080272424") or ("20080290399") or ("20080237694") or ("20100041222") or ("20100295118")).PN.	US-PGPUB; USPAT	OR	OFF	2013/08/26 08:51
S100	6	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory	US-PGPUB; USPAT; USOCR	SAME	ON	2013/08/26 08:53

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S82	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR ONNO) stack multi$1layer charge$1trap$4 oxygen$1rich oxygen$1lean (work adj function adj gate adj electrode) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor)).CLM.	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:04

Sandisk Technologies, Inc. - Ex. 1040, Page 000046

S83	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR ONNO) stack multi$1layer charge$1trap$4 oxygen$1rich oxygen$1lean (work adj function adj gate adj electrode) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:04
S84	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR "ONNO") stack multi$1layer charge$1trap$4 oxygen$1rich oxygen$1lean (work adj function adj gate adj electrode) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:04
S85	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR "ONNO") stack multi$1layer charge$1trap$4 oxygen$1rich oxygen$1lean (work adj function) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:05
S86	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR "ONNO") stack multi$1layer oxygen$1rich oxygen$1lean (work adj function) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:05
S87	1	((oxide$1nitride$1nitride$1oxide OR "ONNO") stack multi$1layer oxygen$1rich oxygen$1lean)	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:05
S88	1	((oxide$1nitride$1nitride$1oxide OR "ONNO") stack oxygen$1rich oxygen$1lean)	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:06
S89	43	((oxide$1nitride$1nitride$1oxide OR "ONNO") stack)	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:06
S90	56	((memory adj transistor) polysilicon (work adj function) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:27
S91	1	S90 257/324.ccls.	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:28
S92	43	((oxide$1nitride$1nitride$1oxide OR "ONNO") stack)	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:40
S93	1	S92 257/324.ccls.	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:40

11/4/2013 10:08:58 AM

Sandisk Technologies, Inc. - Ex. 1040, Page 000047

C:\ Users\ nyushin\ Documents\ EAST\ Workspaces\ 13539466.wsp

Sandisk Technologies, Inc. - Ex. 1040, Page 000048

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	13/539,466	Filing Date	2012-07-01	Docket Number (if applicable)	PM07027D1CIP1	Art Unit	2893
First Named Inventor	Igor POLISHCHUK			Examiner Name	YUSHIN, NIKOLAY K		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503781

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Larry J. Johnson/	Date (YYYY-MM-DD)	2013-09-27
Name	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	Examiner: YUSHIN, NIKOLAY K
Igor POLISHCHUK	)	
	)	Group Art Unit: 2893
Application No.: 13/539,466	)	
	)	Confirmation No.: 5842
Filed: 07-01-2012	)	
	)	
For: Memory Transistor With Multiple Charge Storing Layers And A High Work Function Gate Electrode	)	

REQUEST FOR CONTINUED EXAMINATION AND INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the Request for Continued Examination to be considered with the IDS for the above referenced application. In compliance with the duty of disclosure under 37 CFR § 1.56 and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

Customer No.: 60909

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

/

/

Respectfully submitted,

Date: 09/27/2013

By: /Larry J. Johnson/

Larry J. Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Customer No.: 60909

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
If you wish to add additional U.S. Patent citation information please click the Add button.						Add

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
If you wish to add additional U.S. Published Application citation information please click the Add button.						Add

FOREIGN PATENT DOCUMENTS							Remove	
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button							Add	

NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Sandisk Technologies, Inc. - Ex. 1040, Page 000054

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	1	USPTO Advisory Action for Application Number 13/114,889 (PM07031D1) dated 08/02/2013; 2 pages	☐
	2	USPTO Non Final Rejection for Application Number 13/114,889 (PM07031D1) dated 09/05/2013; 11 pages	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature		Date (YYYY-MM-DD)	
Name/Print	Larry Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13539466
Filing Date:	01-Jul-2012
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Filer:	Andrew J. Bateman/Adnan Fazlic
Attorney Docket Number:	PM07027D1CIP1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE - 2nd and Subsequent Request	1820	1	1700	1700
		Total in USD ($)		**1700**

Electronic Acknowledgement Receipt	
EFS ID:	16981918
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Customer Number:	60909
Filer:	Andrew J. Bateman/Adnan Fazlic
Filer Authorized By:	Andrew J. Bateman
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	27-SEP-2013
Filing Date:	01-JUL-2012
Time Stamp:	16:40:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1700
RAM confirmation Number	4297
Deposit Account	503781
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	PM07027D1CIP1_RCE_09272013.pdf	699518 881431a1c130e7e6f1134692038c07038dfada46	no	3
Warnings:					
Information:					
2	Transmittal Letter	PM07027D1CIP1_TransmittalLetter_09272013.pdf	26756 7e8426be9ac2084b100f6f4237dad964cf1caa72	no	2
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1_IDS1_09272013.pdf	611466 86318f64f1319a0fe914f7d80ef50ca27751e565	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
4	Non Patent Literature	PM07031D1_AdvisoryAction_08022013.pdf	113860 cae302a5363de8b64850f2a643a34a20930fb618	no	2
Warnings:					
Information:					
5	Non Patent Literature	PM07031D1_NonFinalRejection_09052013.pdf	423436 79c145728936fe54a1b8948590648278860 8d615	no	11
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	30742 144827dbd231009643d2e91a25b981ba5c73d8d2	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1905778		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 09/04/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER
YUSHIN, NIKOLAY K

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 09/04/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	12/04/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Sandisk Technologies, Inc. - Ex. 1040, Page 000063

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 09/04/2013
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	12/04/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Sandisk Technologies, Inc. - Ex. 1040, Page 000064

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

60909 7590 09/04/2013

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 09/04/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 136 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 136 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1040, Page 000066

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/539,466	Applicant(s) POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed on 12/21/2012*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-5 and 7-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

Sandisk Technologies, Inc. - Ex. 1040, Page 000068

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 12/21/2012; 04/19/2013; 06/05/2013; 06/05/2013.

Sandisk Technologies, Inc. - Ex. 1040, Page 000069

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 12/21/2012 has been entered.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 12/21/2012; 04/19/2013, 06/05/2013, 06/05/2013 were filed after the mailing date of the Notice of Allowance on 11/27/2012. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

Claims 1-5 and 7-20 stand allowed for the reasons articulated in the Office Action mailed on 11/27/2013.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Friday from 8 a.m. to 5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Primary Examiner, Art Unit 2893

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	13539466
Filing Date	2012-07-01
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Receipt date: 06/05/2013	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
(**Not for submission under 37 CFR 1.99)**	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

/N.Y./	1	USPTP Non Final Rejection for Application Number 13/114889 (PM07031D1) dated 11/25/2011; 13 pages	☐
/N.Y./	2	Wang, Szu-Yu et al., "Reliability and processing effects of bandgap engineered SONOS flash memory", 2007 IEEE, International Reliability Symposium, April 18, 2007, 5 pgs.	☐
/N.Y./	3	Written Opinion of the International Searching Authority for International Application Number PCT/US07/20966 (PM07016WO) mailed 04/21/2008; 1 pages	☐
/N.Y./	4	Written Opinion of the International Searching Authority for International Application Number PCT/US07/20988 (PM07035WO) mailed 03/14/2008; 1 page	☐
/N.Y./	5	Written Opinion of the International Searching Authority for International Application Number PCT/US12/21583 (PM07002CIP1WO) mailed 05/8/2012; 4 pages	☐
/N.Y./	6	Wu et al., "SONOS Device with Tapered Bandgap Nitride Layer," IEEE Transactions on Electron Devices, May 2005, Vol. 52, No. 5, pp. 987-992; 6 pages	☐
/N.Y./	7	Yang et al., "Reliability considerations in scaled SONOS nonvolatile memory devices, solid state Electronics", 43(1999) 2025-2032.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Nikolay Yushin/	Date Considered	08/26/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	13539466
Filing Date	2012-07-01
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6429081	B1	2002-08-06	Doong Kelvin et al.	Entire Document
	2	6946349	B1	2005-09-20	Lee Jae et al.	Entire Document
	3	8283261	B2	2012-10-09	Ramkumar	Entire Document
	4	8318608	B2	2012-11-27	Ramkumar et al.	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060281331	A	2006-12-14	Wang	Entire Document
	2	2006081331	A	2006-04-20	Campian	Entire Document

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 06/05/2013	Application Number	13539466 13539466 - GAU: 2893
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	3	20070066087	A	2007-03-22	Jung	Entire Document

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Application Number 11/904,506 (PM07016): "SONOS ONO stack scaling," Fredrick B. Jenne, filed on 9/26/2007; 46 pages	☐
	2	Application Number 13/431,069 (PM09001CIP1): " SONOS Stack With Split Nitride Memory Layer" Fredrick Jenne et al., filed on 03/27/2012; 59 pages	☐
	3	Application Number 13/436,872 (PM07002CIP2): " Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers" Sagy Levy, Zichron-Yoakev et al., filed on 03/31/2012; 53 pages	☐
	4	Application Number 13/436,875 (PM07031D1CIP1): " Nonvolatile Charge Trap Memory Device Having A High Dielectric Constant Blocking Region" Igor Polishchuk et al., filed on 03/31/2012; 70 Pages	☐
	5	Application Number 13/436,878 (PM07065C2CIP1): " Integration Of Non-Volatile Charge Trap Memory Devices And Logic CMOS Devices" Krishnaswamy Ramkumar et al., filed on 03/31/2012; 90 pages	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 06/05/2013	Application Number	13539466 13539466 - GAU: 2893
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	6	Application Number 13/539,461 (PM07016CIP1): "SONOS ONO STACK SCALING," Fredrick Jenne, filed on 7/1/2012; 91 pages	☐
	7	Application Number 13/551,237 (PM09001C1): " SONOS Stack With Split NItride Memory Layer" Fredrick Jenne et al., filed on 07/17/2012; 37 Pages	☐
	8	Application Number 13/620,071 (PM07024C2): "Method of Fabricating A Nonvolatile Charge Trap Memory Device" Krishnaswamy Ramkumar et al., filled on 09-14-2012; 69 pages	☐
	9	Application Number 60/931,947 (PM07002P1): " Oxide-nitride- Oxide Stack Having Multiple Oxynitride Layers" Sagy Levy et al., filed on 05-25-2007; 27 pages	☐
	10	Application Number 60/931,948 (PM07013P1): " SONOS stack with oxynitride bilayer made of BTBAS and NH3" Sagy Levy et al., filed on 05/25/2007; 11 Pages	☐
	11	Application Number 60/940,128 (PM07035P1): " Single Wafer Process For ONO Stack" Krishnaswamy Ramkumar et al., filed on 05/25/2007; 3 pages	☐
	12	Application Number 61/007,566 (PM07031P1): " Nonvolatile Charge Trap Memory Device Having A High Dielectric Constant Blocking Region" Igor Polishchuk et al., filed on 12/12/2007; 37 pages	☐
	13	Application Number 61/599,258 (CD11072P1) " New Integration of SONOS Stack" Krishnaswamy Ramkumar et al., filed on 02-15-2012: 4 pages	☐
	14	Chen et al., "Performance Improvement of SONOS Memory by Bandgap Engineering of Charge-Trapping Layer," IEEE Electron Device Letters, April 2004, Vol. 25, No. 4, pp. 205-207; 3 pages	☐
	15	International Search Report for International Application Number PCT/US07/20966 (PM07016WO) dated 04/21/2008; 2 pages	☐
	16	International Search Report for International Application Number PCT/US07/20988 (PM07035WO) dated 03/14/2008; 2 pages	☐

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 06/05/2013	Application Number	13539466 13539466 - GAU: 2893
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	17	International Search Report for International Application Number PCT/US12/021583 (PM07002CIP1WO) dated 07/19/2012; 2 pages	☐
	18	Lue et al., "BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability," IEEE, 2005; 4 pages	☐
	19	Lue, Hang-Ting et al., "Reliability Model of Bandgap Engineered SONOS (be-SONOS)", IEEE, 2006, 4 pgs.	☐
	20	Non-Final Rejection for Application Number 13/114,889 (PM07031D1) dated 10/10/2012; 11 pages	☐
	21	PCT International Search Report and Written Opinion of the International Searching Authority, PCT/US07/20965 filed 9/28/07, mailed 4/21/08.	☐
	22	SIPO Office Action for Application Number 200780035963.3 (PM07016CN) dated 02/29/2012; 4 pages	☐
	23	USPTO Advisory Action for Application Number 11/904,506 (PM07016) dated 08/30/2011; 4 pages	☐
	24	USPTO Advisory Action for Application Number 13/114,889 (PM07031D1) dated 08/29/2012; 3 pages	☐
	25	USPTO Final Rejection for Application number 11/904506 (PM07016) dated 06/07/2011; 15 pages	☐
	26	USPTO Final Rejection for Application Number 12/005,813 (PM07011) dated 03/06/2012; 5 pages	☐
	27	USPTO Final Rejection for Application Number 12/030,644 (PM07031) dated 01/24/2011; 22 pages	☐

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 06/05/2013	Application Number	13539466 13539466 - GAU: 2893
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	28	USPTO Final Rejection for Application Number 13/114,889 (PM07031D1) dated 04/02/2013; 12 pages	☐
	29	USPTO Final Rejection for Application Number 13/114,889 (PM07031D1) dated 06/04/2012; 12 pages	☐
	30	USPTO Miscellaneous Internal Document for Application Number 12/030,644 (PM07031) dated 5/28/2010; 6 pages	☐
	31	USPTO Non Final Rejection for Application Number 11/904505 (PM07016) dated 02/03/2011; 13 pages	☐
	32	USPTO Non Final Rejection for Application Number 11/904506 (PM07016) dated 08/31/2010; 17 pages	☐
	33	USPTO Non Final Rejection for Application Number 12/005,813 (PM07011) dated 09/23/2011; 12 pages	☐
	34	USPTO Non Final Rejection for Application Number 12/030,644 (PM07031) dated 5/28/2010; 19 pages	☐
	35	USPTO Non Final Rejection for Application Number 12/767,105 (PM09001) dated 04/21/2011; 7 pages	☐
	36	USPTO Non Final Rejection for Application Number 12/767,105 (PM09001) dated 10/18/2011; 7 pages	☐
	37	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 03/09/2011; 4 pages	☐
	38	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 09/29/2010; 5 pages	☐

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 06/05/2013	Application Number	13539466 13539466 - GAU: 2893
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	39	USPTO Notice of Allowance for Application Number 12/152,518 (PM07027) dated 07/14/2011; 6 pages	☐
	40	USPTO Notice of Allowance for Application Number 12/185,751 (PM07065C2) dated 05/15/2013; 9 pages	☐
	41	USPTO Notice of Allowance for Application Number 12/767,105 (PM09001) dated 04/04/2012; 8 pages	☐
	42	USPTO Notice of Allowance for Application Number 12/767,105 (PM09001) dated 05/07/2012; 7 pages	☐
	43	USPTO Notice of Allowance for Application Number 13/539,458 (PM07024CIP1) dated 05/24/2013; 8 pages	☐
	44	USPTO Requirement for Restriction for Application Number 11/904,506 (PM07016) dated 04/13/2010; 7 pages	☐
	45	USPTO Requirement for Restriction for Application Number 12/767,105 (PM09001) dated 03/01/2011; 6 pages	☐
	46	USPTO Requirement for Restriction for Application Number 13/114,889(PM07031D1) dated 9/7/2011; 6 pages	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Nikolay Yushin/	Date Considered	08/26/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

CPC		
Symbol	**Type**	**Version**

CPC Combination Sets				
Symbol	**Type**	**Set**	**Ranking**	**Version**

(Assistant Examiner)	(Date)	**Total Claims Allowed:** 19	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893	08/26/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
257	324	H	0	1	L	29 / 792 (2006.01.01)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	E29.132	E29.309			

(Assistant Examiner)	(Date)	Total Claims Allowed: 19	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893	08/26/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	13	17												
2	2	17	18												
6	3	18	19												
7	4	19	20												
8	5														
	6														
3	7														
4	8														
5	9														
9	10														
10	11														
14	12														
15	13														
16	14														
11	15														
12	16														

(Assistant Examiner)	(Date)	**Total Claims Allowed:** 19	
/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893	08/26/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8A

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	Art Unit
	NIKOLAY YUSHIN	2893

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	314, 324, E29.132; E29.309	09/26/2012	NY

SEARCH NOTES		
Search Notes	Date	Examiner
Keyword, inventor names, assignee searching - see search history	09/26/2012	NY
Updated keyword searching - see search history	11/14/2012	NY
Updated keyword searching - see search history	08/26/2013	NY
References from IDSs filed on 12/21/2012; 04/19/2013; 06/05/2013; 06/05/2013	08/26/2013	NY

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	324	11/14/2012	NY

	/NIKOLAY YUSHIN/ Primary Examiner.Art Unit 2893

Receipt date: 12/21/2012
Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
If you wish to add additional U.S. Patent citation information please click the Add button.						Add

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/N.Y./	1	20090152621	A	2009-06-18	Polishchuk et al.	Entire Document
If you wish to add additional U.S. Published Application citation information please click the Add button.						Add

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								Add

NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Receipt date: 12/21/2012	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
(Not for submission under 37 CFR 1.99)	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Nikolay Yushin/	Date Considered	08/26/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Receipt date: 04/19/2013
Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	13539466
Filing Date	2012-07-01
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5817170	A	1998-10-06	Desu et al.	Entire Document
	2	6015739	A	2000-01-18	Gardner et al.	Entire Document
	3	6153543	A	2000-11-28	Chesire et al.	Entire Document
	4	6214689	B1	2001-04-10	Lim et al.	Entire Document
	5	6461899	B1	2002-10-08	Kitakado et al.	Entire Document
	6	6586349	B1	2003-07-01	Jeon et al.	Entire Document
	7	6610614	B2	2003-08-26	Niimi et al.	Entire Document
	8	6818558	B1	2004-11-16	Rathor et al.	Entire Document

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
(Not for submission under 37 CFR 1.99)	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	9	6906390	B2	2005-06-14	Nomoto et al.	Entire Document
	10	7112486	B2	2006-09-26	Cho et al.	Entire Document
	11	7312496	B2	2007-12-25	Hazama	Entire Document
	12	7323742	B2	2008-01-29	Georgescu	Entire Document
	13	7365389	B1	2008-04-29	Jeon et al.	Entire Document
	14	7463530	B2	2008-12-09	Lue et al.	Entire Document
	15	7576386	B2	2009-08-18	Lue et al.	Entire Document
	16	7670963	B2	2010-03-02	Ramkumar et al.	Entire Document
	17	7737488	B2	2010-06-15	Lai Sheng et al.	Entire Document
	18	7790516	B2	2010-09-07	Willer et al.	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	13539466
Filing Date	2012-07-01
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20010052615	A	2001-12-20	Fujiwara	Entire Document
	2	20020020890	A	2002-02-21	Willer	Entire Document
	3	20030122204	A	2003-07-03	Nomoto et al.	Entire Document
	4	2003183869	A	2003-10-02	Crivelli et al.	Entire Document
	5	20040173918	A	2004-09-09	Kamal et al.	Entire Document
	6	20040094793	A	2004-05-20	Noguchi et al.	Entire Document
	7	20040104424	A	2004-06-03	Yamazaki	Entire Document
	8	20040251489	A	2004-12-16	Jeon et al.	Entire Document
	9	2004094793	A	2004-05-20	Noguchi et al.	Entire Document
	10	2004104424	A1	2004-06-03	Yamazaki	Entire Document

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
(Not for submission under 37 CFR 1.99)	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	11	2004251489	A	2004-12-16	Jeon et al.	Entire Document
	12	20050070126	A	2005-03-31	Senzaki	Entire Document
	13	2005026637	A	2005-02-03	Fischer Michael et al.	Entire Document
	14	20050266637	A	2005-12-01	Wang	Entire Document
	15	20050093054	A	2005-05-05	Jung	Entire Document
	16	20050098839	A	2005-05-12	Lee et al.	Entire Document
	17	20050141168	A	2005-06-30	Lee et al.	Entire Document
	18	20050205920	A	2005-09-22	Jeon et al.	Entire Document
	19	20050230766	A1	2005-10-20	Nomoto et al.	Entire Document
	20	20050245034	A	2005-11-03	Fukuda et al.	Entire Document
	21	20050275012	A	2005-12-15	Nara et al.	Entire Document

EFS Web 2.1.17 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
(Not for submission under 37 CFR 1.99)	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	22	2005245034	A	2005-11-03	Fukuda et al.	Entire Document
	23	20060111805	A	2006-05-25	Yokoyama et al.	Entire Document
	24	20060113586	A	2006-06-01	Wang	Entire Document
	25	20060113627	A	2006-06-01	Chen et al.	Entire Document
	26	20060131636	A	2006-06-22	Jeon et al.	Entire Document
	27	20060220106	A	2006-10-05	Choi et al.	Entire Document
	28	2006051880	A	2006-03-09	Doczy et al.	Entire Document
	29	2006065919	A	2006-03-30	Fujiwara	Entire Document
	30	2006113627	A	2006-06-01	Chen et al.	Entire Document
	31	20070051306	A	2007-03-08	Ivanov et al.	Entire Document
	32	20070048916	A	2007-03-01	Suzuki et al.	Entire Document

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
(Not for submission under 37 CFR 1.99)	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	33	20070049048	A	2007-03-01	Rauf et al.	Entire Document
	34	20070246753	A	2007-10-25	Chu et al.	Entire Document
	35	20070262451	A	2007-11-15	Rachmady et al.	Entire Document
	36	20070267687	A	2007-11-22	Lue	Entire Document
	37	20070268753	A	2007-11-22	Lue et al.	Entire Document
	38	20070272916	A1	2007-11-29	Wang et al.	Entire Document
	39	2007048916	A	2007-03-01	Suzuki et al.	Entire Document
	40	2008029399	A	2008-02-07	Tomita et al.	Entire Document
	41	20080009115	A1	2008-01-10	Willer et al.	Entire Document
	42	20080150003	A	2008-06-26	Chen et al.	Entire Document
	43	20080237694	A	2008-10-02	Specht et al.	Entire Document

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
(Not for submission under 37 CFR 1.99)	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	44	20080272424	A	2008-11-06	Kim Yong et al.	Entire Document
	45	20080290399	A	2008-11-27	Levy et al.	Entire Document
	46	2008237694	A	2008-10-02	Specht et al.	Entire Document
	47	20100041222	A	2010-02-18	Puchner et al.	Entire Document
	48	20100295118	A1	2010-11-25	Bhattacharyya	Entire Document

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	"MAX 9000 Programmable Logic Device Family," Altera, July 1999, Version 6.01, pp. 1-40; 41 pages	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
(Not for submission under 37 CFR 1.99)	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	2	L. Richard Carley, "Trimming Analog Circuits Using Floating-Gate Analog MOS Memory," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, December 1989, pp. 1569-1575; 7 pages	☐
	3	Office Action Receive for Application Number 10-2007-7001931 (PM04006KR) dated 12/26/2012; 6 pages	☐
	4	USPTO Notice of Allowance for Application Number 11/983,578 (CD06045) dated 03/14/2013; 10 pages	☐
	5	USPTO Notice of Allowance for Application Number 12/207,104 (CD2007172) dated 04/30/2010; 7 pages	☐
	6	"1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer," Cypress Advance Information, 02/12/2004; 9 pages	☐
	7	"10 Gigabit Ethernet Technology Overview White Paper", Revision 1.0, Retrieved from Internet: URL: http:// www.10gea.org, May, 2001.	☐
	8	"16K x 8/9 Dual-Port Static RAM with Sem, Int, Busy," Cypress Semiconductor Data Book, May 1995, CY7C006 and CY7C016, pp. 6:1-17; 10 pages	☐
	9	"1K x 8 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C130/CY7C131 and CY7C140/ CY7C141, pp. 6:37-49; 8 pages	☐
	10	"1kHz to 30MHz Resistor Set SOT-23 Oscillator", Initial Release Final Electrical Specifications LTC1799, Linear Technology Corporation, Jan. 2001, pp. 1-4.	☐
	11	"200-MBaud HOTLink Transceiver," Cypress Semiconductor Corporation, Revised 2/13/2004, CY7C924ADX, Document #38-02008 Rev. *D; 62 pages	☐
	12	"2K x 16 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C133 and CY7C143, pp. 6:63-73; 7 pages	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
(Not for submission under 37 CFR 1.99)	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	13	"2K x 8 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C132/CY7C136 and CY7C142/ CY7C146, pp. 6:50-62; 8 pages	☐
	14	"A Novel Integration Technology of EEPROM Embedded CMOS Logic VLSI Suitable for ASIC Applications", By Masataka Takebuchi et al., IEEE 1992 Custom Integrated Circuits Conference, pp. 9.6.1-9.6.4.	☐
	15	"A Novel Robust and Low Cost Stack Chips Package and Its Thermal Performance", By Soon-Jin Cho et al., IEEE Transaction on Advanced Packaging, vol. 23, No. 2, May 2000, pp. 257-265.	☐
	16	"A Planar Type EEPROM Cell Structure by Standard CMOS Process for Integration with Gate Array, Standard Cell, Microprocessor and for Neural Chips", By Katsuhiko Ohsaki et al., IEEE 1993 Custom Integrated Circuits Conference, pp-23.6.1-23.6.4.	☐
	17	"A Single Chip Sensor & Image Processor for Fingerprint Verification" Anderson, S., et al., IEEE Custom Integrated Circuits Conference, May 12-15, 1991.	☐
	18	"A Single Poly EPROM For Custom CMOS Logic Applications", By Reza Kazerounian et al., IEEE 1986 Custom Integrated Circuits Conference, pp. 59-62.	☐
	19	"A Wide-Bandwidth Low-Voltage PLL for PowerPC.TM. Microprocessors", By Jose Alvarez et al., IEEE Journal of Solid-State Circuits, vol. 30, No. 4, Apr. 1995, pp. 383-391.	☐
	20	"About SMaL Camera Technologies, Inc.", SMaL Camera Technologies, 2001, 1 page.	☐
	21	"Achieving Uniform nMOS Device Power Distribution for Sub-micron ESD Reliability;" Charvaka Duvvuy, Carlos Diaz, and Tim Haddock; 1992; 92-131 through 92-134, no month.	☐
	22	"ADNS-2030 High Performance, Low Power Optical Mouse Sensor (Optimized for Cordless Mouse Applications)," Agilent Technologies, downloaded 10/10/2005, <http://www.home.agilent.com/USeng/nav/-536893734,536883737/pd.html>; 2 pages	☐
	23	"ADNS-2051 High-Performance Optical Mouse Sensor," Agilent Technologies, downloaded 10/10/2005, <http://www.home.agilent.com/USeng/nav/-536893734,536883737/pd.html>; 2 pages	☐

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013	Application Number	13539466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
(Not for submission under 37 CFR 1.99)	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	24	"Agilent ADNK-2030 Solid-State Optical Mouse Sensor," Agilent Technologies Inc., Sample Kit, 2003; 1 page	☐
	25	"Agilent ADNS-2030 Low Power Optical Mouse Sensor," Agilent Technologies Inc., Data Sheet, 2005; 34 pages	☐
	26	"Agilent ADNS-2051 Optical Mouse Sensor," Agilent Technologies Inc., Product Overview, 2003; 2 pages	☐
	27	"Agilent Optical Mouse Sensors," Agilent Technologies Inc., Selection Guide, 2004; 3 pages	☐
	28	"Algorithm for Managing Multiple First-In, First-Out Queues from a Single Shared Random-Access Memory," IBM Technical Disclosure Bulletin, August 1989; 5 pages	☐
	29	"Am99C10A 256.times.48 Content Addressable Memory", Advanced Micro Devices, Dec. 1992.	☐
	30	"An Analog PLL-Based Clock and Data Recovery Circuit with High Input Jitter Tolerance", By Sam Yinshang Sun, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-24, pp. 325-330, Apr. 1989, pp. 383-385.	☐
	31	"An EEPROM for Microprocessors and Custom Logic", By Roger Cuppens et al., IEEE Journal of Solid-State Circuits, vol. SC-20, No. 2, Apr. 1985, pp. 603-608.	☐
	32	"An EPROM Cell Structure foe EPLDs Compatible with Single Poly Gate Process", By Kuniyushi Yoshikawa et al., Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 323-326.	☐
	33	"An Experimental 5-V-Only 256-kbit CMOS EEPROM with a High-Performance Single-Polysilicon Cell", By Jun-Ichi Miyamoto et al., IEEE Journal of Solid State Circuits, vol. SC-21, No. 5, Oct. 1986, pp. 852-860.	☐
	34	Application Number 13/428,201 (CD11072): "Method of Integrating A Charge-Trapping Gate Stack Into A CMOS Flow" Krishnaswamy Ramkumar et al., filed on 03232012; 38 Pages	☐

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

Receipt date: 04/19/2013		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

If you wish to add additional non-patent literature document citation information please click the Add button			
EXAMINER SIGNATURE			
Examiner Signature	/Nikolay Yushin/	Date Considered	08/26/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /N.Y./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25	((IGOR) near2 (POLISHCHUK)).INV.	US-PGPUB; USPAT	AND	ON	2013/08/26 08:39
L2	38	((SAGY) near2 (LEVY)).INV.	US-PGPUB; USPAT	AND	ON	2013/08/26 08:39
L3	98	((KRISHNASWAMY) near2 (RAMKUMAR)).INV.	US-PGPUB; USPAT	AND	ON	2013/08/26 08:39
L4	90	(L1 OR L2 OR L3) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2013/08/26 08:39
L5	1	("20090152621").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2013/08/26 08:41
L6	59	(("6429081") or ("6946349") or ("8283261") or ("8318608") or ("20060281331") or ("20060081331") or ("20070066087") or ("5817170") or ("6015739") or ("6153543") or ("6214689") or ("6461899") or ("6586349") or ("6610614") or ("6818558") or ("6906390") or ("7112486") or ("7312496") or ("7323742") or ("7365389") or ("7463530") or ("7576386") or ("7670963") or ("7737488") or ("7790516") or ("20010052615") or ("20020020890") or ("20030122204") or ("2003183869") or ("20040173918") or ("20040094793") or ("20040104424") or ("200400251489") or ("20040094793") or ("20040104424") or ("20040251489") or ("20050070126") or ("2005026637") or ("20050266637") or ("20050093054") or ("20050098839") or ("20050141168") or ("20050205920") or ("20050230765") or ("20050245034") or ("20050275012") or ("20050245034") or ("20060111805") or ("20060113586") or ("20060113627") or ("200600131636") or ("200600220106") or ("200600051880") or ("200600065919") or ("200600113627") or ("200700513006") or ("20070048916") or ("20070049048") or ("20070246753") or ("20070262451") or ("20070267687") or ("20070268753") or ("20070272916") or ("20070048916") or ("20080029399") or ("20080009115") or ("20080150003") or ("20080237694") or ("20080272424") or ("20080290399") or ("20080237694") or ("20100041222") or ("20100295118")).PN.	US-PGPUB; USPAT	OR	OFF	2013/08/26 08:51

Sandisk Technologies, Inc. - Ex. 1040, Page 000097

L7	6	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory	US-PGPUB; USPAT; USOCR	SAME	ON	2013/08/26 08:53
S1	1	("8063434").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 09:50
S2	18	("20030122204" | "20050230766" | "20060131636" | "20070246753" | "20070262451" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080290399" | "20100041222" | "20100295118" | "6906390" | "6912163" | "7312496" | "7323742" | "7737488" | "7790516").PN. OR ("8063434").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 09:51
S3	19	((IGOR) near2 (POLISHCHUK)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:01
S4	7	("20010012667" | "20030178675" | "20030232507" | "20040082198" | "20100090294" | "20100167506" | "7799670").PN. OR ("8163660").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:04
S5	34	((SAGY) near2 (LEVY)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:05
S6	88	((KRISHNASWAMY) near2 (RAMKUMAR)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:07
S7	8	("20070029625" | "20070031999" | "20080286927" | "20090039414" | "7315474" | "7576386" | "7636257" | "7646637").PN. OR ("8222688").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:10
S8	78	(S3 OR S5 OR S6) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:19
S9	1	((oxide$1nitride$1nitride$1oxide OR ONNO) NEAR4 stack) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:28
S10	1	((oxide$1nitride$1nitride$1oxide OR ONNO) NEAR4 stack)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30
S11	655	((oxide$1nitride$1nitride$1oxide OR ONNO))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30
S12	292	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30
S13	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (oxygen$1rich) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:31
S14	0	((oxide$1nitride$1nitride$1oxide OR ONNO))	US-	AND	ON	2012/09/26

Sandisk Technologies, Inc. - Ex. 1040, Page 000098

		SAME (oxygen$1rich)	PGPUB; USPAT; USOCR			11:12
S15	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (oxygen$1rich)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:12
S16	0	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S2	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S17	1	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S8	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S18	1	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S6	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S19	2	(("6906390") or ("6912163")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 11:16
S20	29727	((oxide$1nitride$11oxide OR ONO)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S21	135	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S22	59	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S23	46	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:21
S24	46	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S23	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:21
S25	41	("4173766" | "5168334" | "5349221" | "5644533" | "5751037" | "5768192" | "5825686" | "5963465" | "5966603" | "6001709" | "6011725" | "6030871" | "6117730" | "6287917" | "6326268").PN. OR ("6465306").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:31
S26	17	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) (substrate NEAR4 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:46
S27	6	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) (channel NEAR4 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:47
S28	467	((oxide$1nitride$11oxide OR ONO)) (channel NEAR2 polysilicon)	US-PGPUB;	AND	ON	2012/09/26 11:48

Sandisk Technologies, Inc. - Ex. 1040, Page 000099

			USPAT; USOCR			
S29	60	((oxide$1nitride$11oxide OR ONO)) (channel NEAR2 polysilicon)	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 11:49
S30	91	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory channel	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:02
S31	0	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) Near3 channel))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S32	1	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) NEAR3 substrate))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S33	2	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) SAME substrate))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S34	3	((oxide$1nitride$1nitride$1oxide OR ONNO)) (OXYGEN same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:16
S35	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (OXYGEN$1RICH same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:17
S36	256	(OXYGEN$1RICH same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:19
S37	119	(OXYGEN$1RICH same NITRIDE) MEMORY CHANNEL	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:20
S38	11	(OXYGEN$1RICH same NITRIDE) MEMORY (POLYSILICON near4 CHANNEL)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:20
S39	8	(OXYGEN$1RICH same NITRIDE) MEMORY (logic near4 MOS)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:45
S40	29	("20030227049" | "20040071030" | "20040129986" | "20050186741" | "20060202263" | "20060226490" | "20060281331" | "4843023" | "5405791" | "5573963" | "5793089" | "5861347" | "6025267" | "6074915" | "6174774" | "6277683" | "6429081" | "6599795" | "6730566" | "6946349" | "7015100" | "7045424" | "7098154" | "7172940" | "7250654" | "7253046" | "7262457" | "7544565" | "7588986").PN. OR ("8143129").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:51
S41	29	("20030227049" | "20040071030" |	US-	AND	ON	2012/09/26

Sandisk Technologies, Inc. - Ex. 1040, Page 000100

		"20040129986" | "20050186741" | "20060202263" | "20060226490" | "20060281331" | "4843023" | "5405791" | "5573963" | "5793089" | "5861347" | "6025267" | "6074915" | "6174774" | "6277683" | "6429081" | "6599795" | "6730566" | "6946349" | "7015100" | "7045424" | "7098154" | "7172940" | "7250654" | "7253046" | "7262457" | "7544565" | "7588986").PN. OR ("8143129").URPN.	PGPUB; USPAT; USOCR			12:51
S42	20	(PMOS SAME SONOS SAME memory) (NMOS SAME logic)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:58
S43	11	(PMOS SAME SONOS SAME memory) (NMOS SAME logic) (polysilicon adj gate)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:59
S48	5	(high$1K NEAR4 (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 13:23
S49	51	(high$1K SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 13:25
S50	976	(dielectric SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:29
S51	151	((dielectric adj constant) SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:29
S52	41	((high adj dielectric adj constant) SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:30
S53	2691	257/314.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:41
S54	11	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S53	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:42
S55	13	(((oxide$1nitride$11oxide OR ONO)) ((oxygen$1rich) SAME nitride)) S53	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:43
S56	2404	257/324.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:44
S57	24	(((oxide$1nitride$11oxide OR ONO)) ((oxygen$1rich) SAME nitride)) S56	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:44

Sandisk Technologies, Inc. - Ex. 1040, Page 000101

S58	9	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S56	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:45
S59	13	("20060261401" | "20080258203" | "6709928" | "20030123307" | "6445030" | "7450423" | "7042054" | "4543707" | "6157426" | "6677213" | "6958511" | "20020154878" | "6818558").PN.	US-PGPUB; USPAT	AND	ON	2012/09/26 14:48
S60	186	257/E29.132.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:04
S61	1	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S60	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:05
S62	2	((oxide$1nitride$11oxide OR ONO) (oxygen$1rich SAME nitride)) S60	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:05
S63	2	((oxide$1nitride$11oxide OR ONO) oxygen$1rich nitride) S60	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
S64	2536	257/E29.309.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
S65	11	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S64	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
S66	11	((oxide$1nitride$11oxide OR ONO)) (channel SAME (recrystallized adj polysilicon))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:08
S67	20	((oxide$1nitride$11oxide OR ONO)) (channel SAME (silicon adj nano$1wire))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:10
S68	1	("20100117138").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:03
S69	1	("6093596").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:22
S70	1	("6093590").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:22
S71	2278	((high adj dielectric adj constant) SAME (tantalum adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:28
S72	2278	((high adj dielectric adj constant) SAME (high adj dielectric adj constant) SAME (tantalum	US-PGPUB;	AND	ON	2012/09/26 16:29

Sandisk Technologies, Inc. - Ex. 1040, Page 000102

		adj oxide))	USPAT; USOCR			
S73	1480	S72 memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:29
S74	280	(((oxide$1nitride$11oxide OR ONO))) S73	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:30
S75	274	((oxide$1nitride$11oxide OR ONO) nitride) S73	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:31
S76	230	((oxide$1nitride$11oxide OR ONO) nitride) AND S73	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 16:31
S77	196	transistor S76	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:32
S78	20	((oxide$1nitride$11oxide OR ONO) nitride transistor) AND S73	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 16:32
S79	47	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/11/14 09:54
S80	6	("20050287763" | "20060202263" | "6274901" | "7067377").PN. OR ("7732276").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/11/14 09:56
S81	18	("20030122204" | "20050230766" | "20060131636" | "20070246753" | "20070262451" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080290399" | "20100041222" | "20100295118" | "6906390" | "6912163" | "7312496" | "7323742" | "7737488" | "7790516").PN. OR ("8063434").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/11/14 09:57

8/ 26/ 2013 8:54:04 AM
C:\ Users\ nyushin\ Documents\ EAST\ Workspaces\ 13539466.wsp

Sandisk Technologies, Inc. - Ex. 1040, Page 000103

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5842

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/539,466	07/01/2012	257	2893	PM07027D1CIP1

APPLICANTS

Igor POLISHCHUK, Fremont, CA;
Sagy LEVY, Zichron-Yoakev, ISRAEL;
Krishnaswamy RAMKUMAR, San Jose, CA;

**** CONTINUING DATA ***************************

This application is a CIP of 13/288,919 11/03/2011
which is a DIV of 12/152,518 05/13/2008 PAT 8063434
which claims benefit of 60/940,160 05/25/2007

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
07/16/2012

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /NIKOLAY K YUSHIN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	13	20	3

ADDRESS

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709
UNITED STATES

TITLE

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

FILING FEE RECEIVED		
1630	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1

CONFIRMATION NO. 5842

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

NONPUBLICATION RESCISSION LETTER

OC000000063200455

Date Mailed: 08/15/2013

Communication Regarding Rescission Of Nonpublication Request and/or Notice of Foreign Filing

Applicant's rescission of the previously-filed nonpublication request and/or notice of foreign filing is acknowledged. The paper has been reflected in the Patent and Trademark Office's (USPTO's) computer records so that the earliest possible projected publication date can be assigned.

The projected publication date is 11/21/2013.

If applicant rescinded the nonpublication request before or on the date of "foreign filing,"[1] then no notice of foreign filing is required.

If applicant foreign filed the application after filing the above application and before filing the rescission, and the rescission did not also include a notice of foreign filing, then a notice of foreign filing (not merely a rescission) is required to be filed within 45 days of the date of foreign filing. See 35 U.S.C. § 122(b)(2)(B)(iii), and Clarification of the United States Patent and Trademark Office's Interpretation of the Provisions of 35 U.S.C. § 122(b)(2)(B)(ii)-(iv), 1272 Off. Gaz. Pat. Office 22 (July 1, 2003).

If a notice of foreign filing is required and is not filed within 45 days of the date of foreign filing, then the application becomes abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii). In this situation, applicant should either file a petition to revive or notify the Office that the application is abandoned. See 37 CFR 1.137(f). Any such petition to revive will be forwarded to the Office of Petitions for a decision. Note that the filing of the petition will not operate to stay any period of reply that may be running against the application.

Questions regarding petitions to revive should be directed to the Office of Petitions at (571) 272-3282.

[1] Note, for purpose of this notice, that "foreign filing" means "filing an application directed to the same invention in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing".

/sstephanos/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Sandisk Technologies, Inc. - Ex. 1040, Page 000105

PTO/SB/36 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

RESCISSION OF PREVIOUS NONPUBLICATION REQUEST
(35 U.S.C. 122(b)(2)(B)(ii))
AND, IF APPLICABLE,
NOTICE OF FOREIGN FILING
(35 U.S.C. 122(b)(2)(B)(iii))

Send completed form to:
Mail Stop PG Pub
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX: (571) 273-8300

Application Number	13/539,466
Filing Date	07-01-2012
First Named Inventor	Igor POLISHCHUK
Title	MEMORY TRANSISTOR WITH MULTIPLE CH
Atty Docket Number	PM07027D1CIP1
Art Unit	2893
Examiner	YUSHIN, NIKOLAY K

A request that the above-identified application not be published under 35 U.S.C. 122(b) (nonpublication request) was included with the above-identified application on filing pursuant to 35 U.S.C. 122(b)(2)(B)(i).
I hereby **rescind** the previous nonpublication request.

If a notice of foreign or international filing is or will be required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c), I hereby provide such notice. This notice is being provided no later than forty-five (**45**) days after the date of such foreign or international filing.

*If a notice of subsequent foreign or international filing required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c) was not filed within forty-five (**45**) days after the date of filing of the foreign or international application, the application is ABANDONED, and a petition to revive under 37 CFR 1.137(b) is required. See 37 CFR 1.137(f).*

/Larry J. Johnson/	08/08/2013
Signature	Date
Larry J. Johnson	56,861
Typed or printed name	Registration Number, if applicable
408-545-7194	
Telephone Number	

This request must be signed in compliance with 37 CFR 1.33(b).

If information or assistance is needed in completing this form, please contact the Pre-Grant Publication Division at (703)605-4283 or by e-mail at PGPub@USPTO.gov.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop PG Pub, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature /Alma Fazlic/		
Name (Print/Type) Alma Fazlic	Date	08/08/2013

This collection of information is required by 37 CFR 1.213(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop PG Pub, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	16535546
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Customer Number:	60909
Filer:	Stoycho Doncheff Draganoff/Alma Fazlic
Filer Authorized By:	Stoycho Doncheff Draganoff
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	08-AUG-2013
Filing Date:	01-JUL-2012
Time Stamp:	13:15:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Rescind Nonpublication Request for Pre Grant Pub	PM07027D1CIP1_RescissionOfNonPubRequest_08082013.pdf	261584 e7e86097d5fa9573df6419a888d168802c6e88ad	no	2

Warnings:	
Information:	

Total Files Size (in bytes):	261584

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6429081	B1	2002-08-06	Doong Kelvin et al.	Entire Document
	2	6946349	B1	2005-09-20	Lee Jae et al.	Entire Document
	3	8283261	B2	2012-10-09	Ramkumar	Entire Document
	4	8318608	B2	2012-11-27	Ramkumar et al.	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060281331	A	2006-12-14	Wang	Entire Document
	2	2006081331	A	2006-04-20	Campian	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	3	20070066087	A	2007-03-22	Jung	Entire Document

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Application Number 11/904,506 (PM07016): "SONOS ONO stack scaling," Fredrick B. Jenne, filed on 9/26/2007; 46 pages	☐
	2	Application Number 13/431,069 (PM09001CIP1): " SONOS Stack With Split Nitride Memory Layer" Fredrick Jenne et al., filed on 03/27/2012; 59 pages	☐
	3	Application Number 13/436,872 (PM07002CIP2): " Oxide-Nitride-Oxide Stack Having Multiple Oxynitride Layers" Sagy Levy, Zichron-Yoakev et al., filed on 03/31/2012; 53 pages	☐
	4	Application Number 13/436,875 (PM07031D1CIP1): " Nonvolatile Charge Trap Memory Device Having A High Dielectric Constant Blocking Region" Igor Polishchuk et al., filed on 03/31/2012; 70 Pages	☐
	5	Application Number 13/436,878 (PM07065C2CIP1): " Integration Of Non-Volatile Charge Trap Memory Devices And Logic CMOS Devices" Krishnaswamy Ramkumar et al., filed on 03/31/2012; 90 pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	6	Application Number 13/539,461 (PM07016CIP1): "SONOS ONO STACK SCALING," Fredrick Jenne, filed on 7/1/2012; 91 pages	☐
	7	Application Number 13/551,237 (PM09001C1): " SONOS Stack With Split NItride Memory Layer" Fredrick Jenne et al., filed on 07/17/2012; 37 Pages	☐
	8	Application Number 13/620,071 (PM07024C2): "Method of Fabricating A Nonvolatile Charge Trap Memory Device" Krishnaswamy Ramkumar et al., filled on 09-14-2012; 69 pages	☐
	9	Application Number 60/931,947 (PM07002P1): " Oxide-nitride- Oxide Stack Having Multiple Oxynitride Layers" Sagy Levy et al., filed on 05-25-2007; 27 pages	☐
	10	Application Number 60/931,948 (PM07013P1): " SONOS stack with oxynitride bilayer made of BTBAS and NH3" Sagy Levy et al., filed on 05/25/2007; 11 Pages	☐
	11	Application Number 60/940,128 (PM07035P1): " Single Wafer Process For ONO Stack" Krishnaswamy Ramkumar et al., filed on 05/25/2007; 3 pages	☐
	12	Application Number 61/007,566 (PM07031P1): " Nonvolatile Charge Trap Memory Device Having A High Dielectric Constant Blocking Region" Igor Polishchuk et al., filed on 12/12/2007; 37 pages	☐
	13	Application Number 61/599,258 (CD11072P1) " New Integration of SONOS Stack" Krishnaswamy Ramkumar et al., filed on 02-15-2012: 4 pages	☐
	14	Chen et al., "Performance Improvement of SONOS Memory by Bandgap Engineering of Charge-Trapping Layer," IEEE Electron Device Letters, April 2004, Vol. 25, No. 4, pp. 205-207; 3 pages	☐
	15	International Search Report for International Application Number PCT/US07/20966 (PM07016WO) dated 04/21/2008; 2 pages	☐
	16	International Search Report for International Application Number PCT/US07/20988 (PM07035WO) dated 03/14/2008; 2 pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	17	International Search Report for International Application Number PCT/US12/021583 (PM07002CIP1WO) dated 07/19/2012; 2 pages	☐
	18	Lue et al., "BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability," IEEE, 2005; 4 pages	☐
	19	Lue, Hang-Ting et al., "Reliability Model of Bandgap Engineered SONOS (be-SONOS)", IEEE, 2006, 4 pgs.	☐
	20	Non-Final Rejection for Application Number 13/114,889 (PM07031D1) dated 10/10/2012; 11 pages	☐
	21	PCT International Search Report and Written Opinion of the International Searching Authority, PCT/US07/20965 filed 9/28/07, mailed 4/21/08.	☐
	22	SIPO Office Action for Application Number 200780035963.3 (PM07016CN) dated 02/29/2012; 4 pages	☐
	23	USPTO Advisory Action for Application Number 11/904,506 (PM07016) dated 08/30/2011; 4 pages	☐
	24	USPTO Advisory Action for Application Number 13/114,889 (PM07031D1) dated 08/29/2012; 3 pages	☐
	25	USPTO Final Rejection for Application number 11/904506 (PM07016) dated 06/07/2011; 15 pages	☐
	26	USPTO Final Rejection for Application Number 12/005,813 (PM07011) dated 03/06/2012; 5 pages	☐
	27	USPTO Final Rejection for Application Number 12/030,644 (PM07031) dated 01/24/2011; 22 pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	28	USPTO Final Rejection for Application Number 13/114,889 (PM07031D1) dated 04/02/2013; 12 pages	☐
	29	USPTO Final Rejection for Application Number 13/114,889 (PM07031D1) dated 06/04/2012; 12 pages	☐
	30	USPTO Miscellaneous Internal Document for Application Number 12/030,644 (PM07031) dated 5/28/2010; 6 pages	☐
	31	USPTO Non Final Rejection for Application Number 11/904505 (PM07016) dated 02/03/2011; 13 pages	☐
	32	USPTO Non Final Rejection for Application Number 11/904506 (PM07016) dated 08/31/2010; 17 pages	☐
	33	USPTO Non Final Rejection for Application Number 12/005,813 (PM07011) dated 09/23/2011; 12 pages	☐
	34	USPTO Non Final Rejection for Application Number 12/030,644 (PM07031) dated 5/28/2010; 19 pages	☐
	35	USPTO Non Final Rejection for Application Number 12/767,105 (PM09001) dated 04/21/2011; 7 pages	☐
	36	USPTO Non Final Rejection for Application Number 12/767,105 (PM09001) dated 10/18/2011; 7 pages	☐
	37	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 03/09/2011; 4 pages	☐
	38	USPTO Non-Final Rejection for Application Number 12/152,518 (PM07027) dated 09/29/2010; 5 pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	39	USPTO Notice of Allowance for Application Number 12/152,518 (PM07027) dated 07/14/2011; 6 pages	☐
	40	USPTO Notice of Allowance for Application Number 12/185,751 (PM07065C2) dated 05/15/2013; 9 pages	☐
	41	USPTO Notice of Allowance for Application Number 12/767,105 (PM09001) dated 04/04/2012; 8 pages	☐
	42	USPTO Notice of Allowance for Application Number 12/767,105 (PM09001) dated 05/07/2012; 7 pages	☐
	43	USPTO Notice of Allowance for Application Number 13/539,458 (PM07024CIP1) dated 05/24/2013; 8 pages	☐
	44	USPTO Requirement for Restriction for Application Number 11/904,506 (PM07016) dated 04/13/2010; 7 pages	☐
	45	USPTO Requirement for Restriction for Application Number 12/767,105 (PM09001) dated 03/01/2011; 6 pages	☐
	46	USPTO Requirement for Restriction for Application Number 13/114,889(PM07031D1) dated 9/7/2011; 6 pages	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Larry J. Johnson/	Date (YYYY-MM-DD)	2013-06-04
Name/Print	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 16820P529PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 07/20966	International filing date *(day/month/year)* 28 September 2007 (28.09.2007)	(Earliest) Priority Date *(day/month/year)* 25 May 2007 (25.05.2007)
Applicant Cypress Semiconductor Corporation		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 1

☐ as suggested by the applicant.

☒ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/20966

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/31 (2008.01)
USPC - 438/769
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): H01L 21/31 (2008.01)
USPC: 438/769

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC(8): H01L 21/31 (2008.01)
USPC: 438/769; 438/758, 773, 786, 791, 954, 287; 257/E31.423, E29.309, 314, 257/288

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO WEST (USPT, PGPUB, EPAB, JPAB); -nonvolatile, ?non-volatile?, trap$, charge, memory, tunneling, layer, substrate, oxynitride, blocking, oxidiz$, anneal$, gate, ?trapped-charge?, densify$, anneal, oxide, oxidation, ratio, hydrogen, oxygen, wet, insulat$, SONOS, deposit$, ?oxygen-rich?, silicon, rich
Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2004/0094793 A1 (NOGUCHI, et al.) 20 May 2004 (20.05.2004), [Abstract], para[0005], [0021], [0024], [0027], [0042], [0045], [0046], [0048]-[0050], [0077], [0081], [0083], [0084], [0088], [0152], Fig. 1	1, 4, 8-10 --- 2, 3, 5-7, 11-20
Y	US 2005/0245034 A1 (FUKADA, et al.) 03 November 2005 (03.11.2005), para[0002], [0076]	2, 3, 7, 11-13, 15-20
Y	US 2006/0113627 A1 (CHEN, et al.) 01 June 2006 (01.06.2006), para[0020], [0026]-[0028]	5-7, 14
Y	US 2004/0104424 A1 (YAMAZAKI) 03 June 2004 (03.06.2004), [Abstract], para[0088], [0217], [0243]	15-17, 19, 20
Y	US 2007/0048916 A1 (SUZUKI, et al.) 01 March 2007 (01.03.2007), para[0038], [0045]	7

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 January 2008 (22.01.2008)	21 APR 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 16820P559PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 07/20988	International filing date *(day/month/year)* 28 September 2007 (28.09.2007)	(Earliest) Priority Date *(day/month/year)* 25 May 2007 (25.05.2007)
Applicant CYPRESS SEMICONDUCTOR CORPORATION		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 1

☐ as suggested by the applicant.

☒ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (April 2007)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/20988

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/76 (2008.01)
USPC - 257/314; 257/E29.308
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 257/314; 257/E29.308

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 257/314; 257/E29.308 - text delimited

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Electronic Databases Searched: USPTO WEST (PGPUB, EPAB, JPAB, USPT), Google patent, Google scholar. Search Terms Used: nonvola$ adj charge adj trap, nonvolatile, memory device, first and second and process and chamber, nonvolatile adj charge adj trap, tunnel, wafer, nitride or oxy-nitride or oxynitride, dielectric, cluster

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/0173918 A1 (Kamal et al.) 09 September 2004 (09.09.2004), entire document especially figure 2A and 2B; para [0002]; [0022]; [0029]; [0033]; [0036]; [0037];	1-20
Y	US 6,214,689 B1 (Lim et al.) 10 April 2001 (10.04.2001), entire document especially col 4, ln 26 -35	1-20
Y	US 2006/0111805 A1 (Yokoyama et al.) 25 May 2006 (25.05.2006), para [0125]; FIG.3	1-20
Y	US 5,817,170 A (Desu et al.) 06 October 1998 (06.10.1998), entire document, especially col 4, ln 02-05; col 4, ln 26-30	2, 3, 5-6, 8-9, 11-14, 16-17,20
A	US 2007/0051306 A1 (Ivanov et al.) 08 March 2007 (08.03.2007), entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 January 2008 (23.01.2008)	14 MAR 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference PM07002CIP1WO	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 12/21583	International filing date *(day/month/year)* 17 January 2012 (17.01.2012)	(Earliest) Priority Date *(day/month/year)* 14 January 2011 (14.01.2011)
Applicant CYPRESS SEMICONDUCTOR CORPORATION		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 2

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 12/21583

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/792; H01L 21/336 (2012.01)
USPC - 257/324; 257/E21.209; 257/E29.309; 438/257
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC -- 257/324; 257/E21.209; 257/E29.309; 438/257

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC -- 257/324; 257/E21.209; 257/E29.309; 438/257 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST (USPT, PGPB, JPAB,EPAB): Google
Search Terms Used: silicon oxide nitride oxide, oxynitride, source, drain, tunnel oxide, spaced apart, dichlorosilane, substrate, ammonia, oxygen, hydrogen

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2009/0179253 A1 (Levy et al.) 16 July 2009 (16.07.2009), entire document especially Abstract, para [0018], [0027], [0036], [0021], [0023], [0024]-[0026], [0034], [0025]-[0026]	1-20, 22 ---------- 21, 23
Y	US 6,153,543 A (Chesire et al.) 28 November 2000 (28.11.2000), entire document especially Abstract; col 5, ln 5-40	21, 23

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 April 2012 (24.04.2012)	08 MAY 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
Daniel E. Ovanezian
Blakely, Sokoloff, Taylor & Zafman LLP
1279 Oakmead Parkway
Sunnyvale, California 94085-4040

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing *(day/month/year)*	21 APR 2008
Applicant's or agent's file reference 16820P566PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US 07/20965	International filing date *(day/month/year)* 28 September 2007 (28.09.2007)
Applicant Cypress Semiconductor Corporation	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 14 35

   For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 16820P566PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 07/20965	International filing date *(day/month/year)* 28 September 2007 (28.09.2007)	(Earliest) Priority Date *(day/month/year)* 25 May 2007 (25.05.2007)
Applicant Cypress Semiconductor Corporation		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 4

☐ as suggested by the applicant.

☒ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/20965

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/792 (2008.01)
USPC - 257/324
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC - 257/324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 257/288, 314, 324, E21.423, E29.309; 438/287, 475; 365/129 -- text search, see search terms below

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST(PGPB,USPT,USOC,EPAB,JPAB); DialogPRO(Engineering); Google Scholar
Search Terms Used: charge, trap, gate, stack, deuterat, deuterium, deuter, layer, multi, two, second, plurality, dielectric, tunnel, top, free, thickness, ratio, nanometer, substrate, concentrat

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006/0192248 A1 (WANG) 31 August 2006 (31.08.2006), especially Figs 2-4; para [0009]-[0010], [0013], [0020]-[0025].	1-20
Y	US 2004/0251521 A1 (TANAKA et al.) 16 December 2004 (16.12.2004), especially Fig 17; para [0009], [0016], [0084], [0118]-[0121], [0143], [0168]-[0170], [0176]-[0180].	1-20
Y	US 6,670,241 B1 (KAMAL et al.) 30 December 2003 (30.12.2003), especially Fig 4; col 1, ln 8-9; col 2, ln 25-36, 60-63; col 4, ln 62-66; col 5, ln 8-10, 15-17.	5-7, 9-14, 18-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2008 (17.01.2008)	21 APR 2008

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	13539466
Filing Date	2012-07-01
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	1	USPTP Non Final Rejection for Application Number 13/114889 (PM07031D1) dated 11/25/2011; 13 pages	☐
	2	Wang, Szu-Yu et al., "Reliability and processing effects of bandgap engineered SONOS flash memory", 2007 IEEE, International Reliability Symposium, April 18, 2007, 5 pgs.	☐
	3	Written Opinion of the International Searching Authority for International Application Number PCT/US07/20966 (PM07016WO) mailed 04/21/2008; 1 pages	☐
	4	Written Opinion of the International Searching Authority for International Application Number PCT/US07/20988 (PM07035WO) mailed 03/14/2008; 1 page	☐
	5	Written Opinion of the International Searching Authority for International Application Number PCT/US12/21583 (PM07002CIP1WO) mailed 05/8/2012; 4 pages	☐
	6	Wu et al., "SONOS Device with Tapered Bandgap Nitride Layer," IEEE Transactions on Electron Devices, May 2005, Vol. 52, No. 5, pp. 987-992; 6 pages	☐
	7	Yang et al., "Reliability considerations in scaled SONOS nonvolatile memory devices, solid state Electronics", 43(1999) 2025-2032.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Larry J. Johnson/	Date (YYYY-MM-DD)	2013-06-04
Name/Print	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
Daniel E. Ovanezian
Blakely, Sokoloff, Taylor & Zafman LLP
1279 Oakmead Parkway
Sunnyvale, California 94805-4040

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 21 APR 2008
Applicant's or agent's file reference 16820P529PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US 07/20966	International filing date *(day/month/year)* 28 September 2007 (28.09.2007)
Applicant Cypress Semiconductor Corporation	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 14 35

   For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
Daniel E. Ovanezian
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94805-4040

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing *(day/month/year)*	14 MAR 2008
Applicant's or agent's file reference 16820P559PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US 07/20988	International filing date *(day/month/year)* 28 September 2007 (28.09.2007)
Applicant CYPRESS SEMICONDUCTOR CORPORATION	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 14 35

   For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	08 MAY 2012
Applicant's or agent's file reference PM07002CIP1WO	FOR FURTHER ACTION See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 12/21583	17 January 2012 (17.01.2012)	14 January 2011 (14.01.2011)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H01L 29/792; H01L 21/336 (2012.01)
USPC - 257/324; 257/E21.209; 257/E29.309; 438/257

Applicant CYPRESS SEMICONDUCTOR CORPORATION

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1 *bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	24 April 2012 (24.04.2012)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 12/21583

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

   ☐ on paper

   ☐ in electronic form

   b. (time)

   ☐ in the international application as filed

   ☐ together with the international application in electronic form

   ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 12/21583

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	2-5, 7-10, 13-15, 17, 20-23	YES
	Claims	1, 6, 11, 12, 16, 18, 19	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-23	NO
Industrial applicability (IA)	Claims	1-23	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1, 6, 11, 12, 16, 18, and 19 lack novelty under PCT Article 33(2) as being anticipated by US 2009/0179253 A1 to Levy et al. (hereinafter Levy).

Regarding claims 1, 6, and 11, Levy discloses a method of forming a semiconductor device including a silicon-oxide-oxynitride-oxide-silicon structure (Fig. 2) comprising:
-substrate comprising silicon (208) and having a surface (206) with laterally spaced-apart source and drain regions (210) (para [0021]);
-a tunnel oxide layer (216) on the surface of the substrate overlying the source and drain regions (para [0023]);
-a multi-layer charge storing layer on the tunnel oxide layer and disposed laterally between the spaced-apart source and drain regions, the multi-layer charge storing layer including an oxygen-rich first oxynitride layer (220B) in which a stoichiometric composition of the first oxynitride layer results in it being substantially trap free, and an oxygen-lean second oxynitride layer (220A) in which a stoichiometric composition of the second oxynitride layer results in it being trap dense (para [0021], [0024]-[0026]);
-a blocking oxide layer (218) on the second oxynitride layer (para [0021]); and
-a silicon containing gate layer on the blocking oxide layer. (para [0034]).

Regarding claim 12, Levy further discloses the method of claim 11, wherein the stoichiometric composition of the first oxynitride layer comprises a concentration of oxygen selected to increase a retention performance of the multi-layer charge storing layer by acting as a barrier between charge trapped in the second oxynitride layer and the substrate. (para [0018] and [0025]).

Regarding claim 16, Levy further discloses the method of claim 12, wherein the retention performance of the multi-layer charge storing layer increases an end-of-life (EOL) for the semiconductor device at a specified difference between program and erase voltages to at least about 20 years. (para [0036]).

Regarding claim 18, Levy further discloses the method of claim 11, wherein the first oxynitride layer is formed in a chemical vapor deposition (CVD) process using a process gas comprising a dichlorosilane (SiH2Cl2)/ammonia (NH3) mixture at a ratio in a range of about 5:1 to 15:1 and a nitrous oxide (N2O)/NH3 mixture at a ratio in a range of about 2:1 to 4:1, and wherein the second oxynitride layer is formed in a CVD process using a process gas comprising a N2O/NH3 mixture at a ratio in a range of about 1:6 to 1:8 and a SiH2Cl2/NH3 mixture at a ratio in a range of about 1.5: 1 to 3: 1. (para [0025]-[0026]).

Regarding claim 19, Levy further discloses the method of claim 18, wherein forming the first oxynitride layer and the second oxynitride layer are performed sequentially in a single CVD tool by changing the ratio of the N2O/NH3 and SiH2Cl2/NH3 mixtures. (para [0027]).

Claims 2-5, 7-10, 13-15, 17, 20, and 22 lack an inventive step under PCT Article 33(3) as being obvious over Levy.

Regarding claims 2, 3, 7, 8, and 13-15, Levy does not expressly teach wherein a concentration of oxygen in the first oxynitride layer is from about 15% to about 40% and wherein a concentration of oxygen in the second oxynitride layer is less than about 5%. However, Levy does teach optimizing the oxygen levels in both oxynitride layers (see para [0018]), thereby rendering the recited levels obvious to a skilled artisan through routine experimentation.

Regarding claims 4, 5, 9, 10, 17, and 22, Levy does not expressly each wherein the second oxynitride layer comprises a carbon concentration that increases the number of traps so that the charge trap density is at least 1000 times greater than the first oxynitride layer. However, Levy does teach optimizing the concentration of constituents within the oxynitride layers in order to reduce stored charge loss (see para [0018]). Thus, a skilled artisan would have found these limitations obvious based upon routine experimentation.

Regarding claim 20, Levy further discloses the method of claim 11, wherein the tunnel oxide layer is grown in an ISSG (InSituSteam Generation) chamber with a radical oxidation using a reaction between oxygen (O2) and hydrogen (H2) on the substrate. (para [0023] and [0028]). Levy does not expressly teach temperatures of at least 1000.C, but a skilled artisan would have found the recited temperature obvious based upon routine experimentation.

---------- See Supplemental Box ----------

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 12/21583

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
V.2 Citations and Explanations;

Claims 21 and 23 lack an inventive step under PCT Article 33(3) as being obvious over Levy in view of US 6,153,543 A to Chesire et al. (hereinafter Chesire).

Regarding claim 21, Levy teaches the method of claim 11 including a blocking oxide layer, but does not expressly teach the further claim limitation taught by Chesire of wherein said layer is formed by high density plasma (HDP) oxidation of a portion of the second oxynitride layer (see col 5, ln 5-40). It would have been obvious to a skilled artisan to utilize HDP oxidation to form the blocking oxide layer in order to provide a smooth layer with an optimal aspect ratio.

Regarding claim 23, Levy further teaches wherein the second oxynitride layer is formed in a CVD process using a process gas comprising Bis-TertiaryButylAminoSilane (BTBAS) and ammonia (NH3) mixed at a ratio of from about 7: 1 to about 1:7. (para [0024] and [0026]).

Claims 1-23 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

Electronic Acknowledgement Receipt

EFS ID:	15953912
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Customer Number:	60909
Filer:	Larry Joel Johnson/Rosemary Saint-Vincent
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	05-JUN-2013
Filing Date:	01-JUL-2012
Time Stamp:	12:29:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	CD06138_IDSform1_06042013.pdf	57314 ddab174182dde0822b9ac5baaaff0d53fdb49ff8	no	8

Warnings:	
Information:	

This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	PM07016_Application_09262007.pdf	9270961 1d09b7cad4a818a6526c2199a66217f1123b1991	no	46
Warnings:					
Information:					
3	Non Patent Literature	PM09001CIP1_Application_03272012.pdf	1761504 5df2b29fdd6b3c8a553927fa6304ba7ec77dcfcf	no	59
Warnings:					
Information:					
4	Non Patent Literature	PM07002CIP2_Application_03312012.pdf	1755924 6a55bb81aea0a80ec854d2741ecde25f7fb43ab5	no	53
Warnings:					
Information:					
5	Non Patent Literature	PM07031D1CIP1_Application_03312012.pdf	2504228 62cc95f230d8ac936bf689cd495e97ef832add9e	no	70
Warnings:					
Information:					
6	Non Patent Literature	PM07065C2CIP1_Application_03312012.pdf	3424373 b997b83bf7306ed7932248e145359930c8ee9e9b	no	90
Warnings:					
Information:					
7	Non Patent Literature	PM07016CIP1_Application_07012012.pdf	8538945 976cadda80824b1695986cc93829da4b0fe24b86	no	91
Warnings:					
Information:					
8	Non Patent Literature	PM09001C1_Application_07172012.pdf	920857 ad85c5d2f715ce0c7b8c884d4a2e44f728cb103c	no	32
Warnings:					
Information:					
9	Non Patent Literature	PM07024C2_Application_09142012.pdf	2578961 ea452b3453d1aa3f3bd42eea82d09bec36c7e5ed	no	76
Warnings:					
Information:					
10	Non Patent Literature	PM07002P1_Application_05252007.pdf	852450 21242dda1652773cf0ba153a39fc230ebd800c53	no	27

Warnings:					
Information:					
11	Non Patent Literature	PM07013P1_Application_0525 2007.pdf	290776 c0d1f0fc7e31719262c429d3d123e2966c113f5c	no	11
Warnings:					
Information:					
12	Non Patent Literature	PM07035P1_Application_0525 2007.pdf	135959 4221f3dd85f59e606e971a0fe2bffb5f7ceafd57	no	3
Warnings:					
Information:					
13	Non Patent Literature	PM07031P1_Application_1212 2007.pdf	1209208 0b491691001a91c00906a4746a4b830ede5fb4eb	no	37
Warnings:					
Information:					
14	Non Patent Literature	CD11072P1_Application_0215 2012.pdf	160058 5323c1728e99a04e104e3d8dd19912cb8389a4a9	no	4
Warnings:					
Information:					
15	Non Patent Literature	Chen_PerformanceImprovement.pdf	216807 875e5bf8a2754390edaedc3bfe6614c446bf0b47	no	3
Warnings:					
Information:					
16	Non Patent Literature	PM07016WO_SearchReport_04 212008.pdf	109557 294d067ac09c0d07036b13e874066c8926640def	no	2
Warnings:					
Information:					
17	Non Patent Literature	PM07035WO_SearchReport_03 142008.pdf	105948 36eb94c7c771d164a57b0704e1ebf4f93af38942	no	2
Warnings:					
Information:					
18	Non Patent Literature	PM07002CIP1WO_SearchReport_09192012.pdf	96595 f0607b99a78495691d7649b7e4e598d854a28f89	no	2
Warnings:					
Information:					
19	Non Patent Literature	Lue_BESONOSbandgap.pdf	343251 46a2d38f89c561668f217e67a4c36e64ed899ef5	no	4

Warnings:					
Information:					
20	Non Patent Literature	Lue_ReliabilityModel.pdf	340755 9b54f9dca03dca1a4f3f1718ac56017f568858873	no	4
Warnings:					
Information:					
21	Non Patent Literature	PM07031D1_NonFinalOA_10102012.pdf	390287 1646c67d121fbb5f1880f178e061ba228840a457	no	11
Warnings:					
Information:					
22	Non Patent Literature	PM07014WO_SearchReport_WrittenOpinion_04212008.pdf	174261 41ea5d13011a6298b2d0cf91d4cd2f12f9bea33a	no	3
Warnings:					
Information:					
23	Non Patent Literature	PM07016CN_OfficeAction_02292012.pdf	115832 4849f0a77c0b5b44230a6b202397e6058cbadec8	no	4
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
24	Non Patent Literature	PM07016_AdvisoryAction_08302011.pdf	964675 8d77cc3842eb1703fd76c52c9772717fa75040ad	no	4
Warnings:					
Information:					
25	Non Patent Literature	PM07031D1_AdvisoryAction_08292012.pdf	121459 0600e30f81eededd9738e48b7b158e10969bd11f	no	3
Warnings:					
Information:					
26	Non Patent Literature	PM07016_FinalRejection_06072011.pdf	3157022 bbb23e0e11055bb35a6e14fe67a7e862e8e4b397	no	15
Warnings:					
Information:					
27	Non Patent Literature	PM07011_FinalRejection_03062012.pdf	159759 d11722043fa1072b3a12708e6f2518d4cddd08d8	no	5
Warnings:					
Information:					

28	Non Patent Literature	PM07031_FinalRejection_01242011.pdf	750359 74a0323b00749359ad0a40909ea2ad91317ce5ac	no	22
Warnings:					
Information:					
29	Non Patent Literature	PM07031D1_FinalRejection_04022013.pdf	449166 90731243f7bd07966289d63982ce581d5b3c8ed2	no	12
Warnings:					
Information:					
30	Non Patent Literature	PM07031D1_FinalRejection_06042012.pdf	423294 a3e02c0c456da26281d61318c8e3ce0b3bf4e85f	no	12
Warnings:					
Information:					
31	Non Patent Literature	PM07031_MiscInternalDoc_05282010.pdf	186699 a311be90e26e6dac85e2b5edb507d9bbe95bdc50	no	6
Warnings:					
Information:					
32	Non Patent Literature	PM07016_NonFinalRejection_02032011.pdf	2512512 c34d6fc27bca8f60d73c2791962c541127665f9e	no	13
Warnings:					
Information:					
33	Non Patent Literature	PM07016_NonFinalRejection_08312010.pdf	3612011 182e3381857f925f8509abb0ac0efcacdf029cb3	no	17
Warnings:					
Information:					
34	Non Patent Literature	PM07011_NonFinalRejection_09232011.pdf	430966 e4721feebd1842fdf0cbca716ae1ba2178dae369	no	12
Warnings:					
Information:					
35	Non Patent Literature	PM07031_NonFinalOA_05282010.pdf	621585 ab447232928309f1622615d0190cc19f45e152ce	no	19
Warnings:					
Information:					
36	Non Patent Literature	PM09001_NonFinalRejection_04212011.pdf	221265 ebbbdb562ad63e62a864e9f7791da78e077e6f64	no	7
Warnings:					
Information:					

37	Non Patent Literature	PM09001_NonFinalRejection_10182011.pdf	271674 56156f26092f49c2b90b9dfd37e3a41765e8f017	no	7
Warnings:					
Information:					
38	Non Patent Literature	PM07027_NonFinalOA_03092011.pdf	137033 5705c2bff82b68b029e19df2c291670c5f65c8d4	no	4
Warnings:					
Information:					
39	Non Patent Literature	PM07027_NonFinalOA_09292010.pdf	159620 6f5b0de9ccad5172cf5742ea653b37a1cf891c8d	no	5
Warnings:					
Information:					
40	Non Patent Literature	PM07027_NOA_07142011.pdf	355660 7c941c7f5d2aa33c9e81c0ccb1bc3f8c752f9926	no	6
Warnings:					
Information:					
41	Non Patent Literature	PM07065C2_NOA_05152013.pdf	432235 906aeb6f21ee6a0b249b4cfdfb99669c7908ecd3	no	9
Warnings:					
Information:					
42	Non Patent Literature	PM09001_NOA_04042012.pdf	414560 e8bce6865cdc8065a1d5c1c8b2c794a0cacb4c3e	no	8
Warnings:					
Information:					
43	Non Patent Literature	PM09001_NOA_05072012.pdf	395488 1c83360cc63e73e33e1ae7dd69e3fe21af8bc08c	no	7
Warnings:					
Information:					
44	Non Patent Literature	PM07024CIP1_NOA_05242013.pdf	397873 915c60f72d9c7b8b35f04c86b0617594abe2995a	no	8
Warnings:					
Information:					
45	Non Patent Literature	PM07016_RequirementRestrictionOA_04132010.pdf	248624 c8baa75be27c9ad5bfcd5f88a1d6a6bfe5c67764	no	7
Warnings:					
Information:					

46	Non Patent Literature	PM09001_RequirementRestriction_03012011.pdf	222859 0876c18d4cc36d29ec9001fa37538913858 9e363	no	6
Warnings:					
Information:					
47	Non Patent Literature	PM07031D1_RequirementRestriction_09072011.pdf	212975 0b2f1fff6680ad9d008bb15f06b4da384574 065a	no	6
Warnings:					
Information:					
48	Information Disclosure Statement (IDS) Form (SB08)	CD06138_IDSform2_06042013.pdf	38630 00c5c1613fb178005e3dc62ff2678b4eb6af 884a	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
49	Non Patent Literature	PM07031D1_NonFinalRejection_11252011.pdf	449129 2804ef02b91c9600d5a0cb7ae12671bebc1 b509b	no	13
Warnings:					
Information:					
50	Non Patent Literature	Wang_ReliabilityProcessing.pdf	405949 0d661657bd08d35f92a770110dbf14b89c2 6594c	no	5
Warnings:					
Information:					
51	Non Patent Literature	PM07016WO_WrittenOpinion_04212008.pdf	72486 b0517905218277ebac895d1a45b64dfb23c 79846	no	1
Warnings:					
Information:					
52	Non Patent Literature	PM07035WO_WrittenOpinion_03142008.pdf	72023 91052247620b947e27c7d7b31592310fdef 301de	no	1
Warnings:					
Information:					
53	Non Patent Literature	PM07002CIP1WO_WrittenOpinion_05082012.pdf	172665 af060864be7bd5ae5db59d904f26ef9b7c2 68fc9	no	4
Warnings:					
Information:					
54	Non Patent Literature	Wu_SONOSdeviceTapered.pdf	485226 44b4830f79be5ce4bd33deed0ff4741e90f2 d51d	no	6

Warnings:					
Information:					
55	Non Patent Literature	Yang_ReliabiltyConsideratonsInScaledSONOS.pdf	256185 d967ff41d60a38c5117ef513f5259aea46ea1d64	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	54166477	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	13539466
Filing Date	2012-07-01
First Named Inventor	Igor Polishchuk
Art Unit	2893
Examiner Name	YUSHIN, NIKOLAY K
Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5817170	A	1998-10-06	Desu et al.	Entire Document
	2	6015739	A	2000-01-18	Gardner et al.	Entire Document
	3	6153543	A	2000-11-28	Chesire et al.	Entire Document
	4	6214689	B1	2001-04-10	Lim et al.	Entire Document
	5	6461899	B1	2002-10-08	Kitakado et al.	Entire Document
	6	6586349	B1	2003-07-01	Jeon et al.	Entire Document
	7	6610614	B2	2003-08-26	Niimi et al.	Entire Document
	8	6818558	B1	2004-11-16	Rathor et al.	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	9	6906390	B2	2005-06-14	Nomoto et al.	Entire Document
	10	7112486	B2	2006-09-26	Cho et al.	Entire Document
	11	7312496	B2	2007-12-25	Hazama	Entire Document
	12	7323742	B2	2008-01-29	Georgescu	Entire Document
	13	7365389	B1	2008-04-29	Jeon et al.	Entire Document
	14	7463530	B2	2008-12-09	Lue et al.	Entire Document
	15	7576386	B2	2009-08-18	Lue et al.	Entire Document
	16	7670963	B2	2010-03-02	Ramkumar et al.	Entire Document
	17	7737488	B2	2010-06-15	Lai Sheng et al.	Entire Document
	18	7790516	B2	2010-09-07	Willer et al.	Entire Document
If you wish to add additional U.S. Patent citation information please click the Add button.						
U.S.PATENT APPLICATION PUBLICATIONS						

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20010052615	A	2001-12-20	Fujiwara	Entire Document
	2	20020020890	A	2002-02-21	Willer	Entire Document
	3	20030122204	A	2003-07-03	Nomoto et al.	Entire Document
	4	2003183869	A	2003-10-02	Crivelli et al.	Entire Document
	5	20040173918	A	2004-09-09	Kamal et al.	Entire Document
	6	20040094793	A	2004-05-20	Noguchi et al.	Entire Document
	7	20040104424	A	2004-06-03	Yamazaki	Entire Document
	8	20040251489	A	2004-12-16	Jeon et al.	Entire Document
	9	2004094793	A	2004-05-20	Noguchi et al.	Entire Document
	10	2004104424	A1	2004-06-03	Yamazaki	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	11	2004251489	A	2004-12-16	Jeon et al.	Entire Document
	12	20050070126	A	2005-03-31	Senzaki	Entire Document
	13	2005026637	A	2005-02-03	Fischer Michael et al.	Entire Document
	14	20050266637	A	2005-12-01	Wang	Entire Document
	15	20050093054	A	2005-05-05	Jung	Entire Document
	16	20050098839	A	2005-05-12	Lee et al.	Entire Document
	17	20050141168	A	2005-06-30	Lee et al.	Entire Document
	18	20050205920	A	2005-09-22	Jeon et al.	Entire Document
	19	20050230766	A1	2005-10-20	Nomoto et al.	Entire Document
	20	20050245034	A	2005-11-03	Fukuda et al.	Entire Document
	21	20050275012	A	2005-12-15	Nara et al.	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	22	2005245034	A	2005-11-03	Fukuda et al.	Entire Document
	23	20060111805	A	2006-05-25	Yokoyama et al.	Entire Document
	24	20060113586	A	2006-06-01	Wang	Entire Document
	25	20060113627	A	2006-06-01	Chen et al.	Entire Document
	26	20060131636	A	2006-06-22	Jeon et al.	Entire Document
	27	20060220106	A	2006-10-05	Choi et al.	Entire Document
	28	2006051880	A	2006-03-09	Doczy et al.	Entire Document
	29	2006065919	A	2006-03-30	Fujiwara	Entire Document
	30	2006113627	A	2006-06-01	Chen et al.	Entire Document
	31	20070051306	A	2007-03-08	Ivanov et al.	Entire Document
	32	20070048916	A	2007-03-01	Suzuki et al.	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	33	20070049048	A	2007-03-01	Rauf et al.	Entire Document
	34	20070246753	A	2007-10-25	Chu et al.	Entire Document
	35	20070262451	A	2007-11-15	Rachmady et al.	Entire Document
	36	20070267687	A	2007-11-22	Lue	Entire Document
	37	20070268753	A	2007-11-22	Lue et al.	Entire Document
	38	20070272916	A1	2007-11-29	Wang et al.	Entire Document
	39	2007048916	A	2007-03-01	Suzuki et al.	Entire Document
	40	2008029399	A	2008-02-07	Tomita et al.	Entire Document
	41	20080009115	A1	2008-01-10	Willer et al.	Entire Document
	42	20080150003	A	2008-06-26	Chen et al.	Entire Document
	43	20080237694	A	2008-10-02	Specht et al.	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	44	20080272424	A	2008-11-06	Kim Yong et al.	Entire Document
	45	20080290399	A	2008-11-27	Levy et al.	Entire Document
	46	2008237694	A	2008-10-02	Specht et al.	Entire Document
	47	20100041222	A	2010-02-18	Puchner et al.	Entire Document
	48	20100295118	A1	2010-11-25	Bhattacharyya	Entire Document

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	"MAX 9000 Programmable Logic Device Family," Altera, July 1999, Version 6.01, pp. 1-40; 41 pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	2	L. Richard Carley, "Trimming Analog Circuits Using Floating-Gate Analog MOS Memory," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, December 1989, pp. 1569-1575; 7 pages	☐
	3	Office Action Receive for Application Number 10-2007-7001931 (PM04006KR) dated 12/26/2012; 6 pages	☐
	4	USPTO Notice of Allowance for Application Number 11/983,578 (CD06045) dated 03/14/2013; 10 pages	☐
	5	USPTO Notice of Allowance for Application Number 12/207,104 (CD2007172) dated 04/30/2010; 7 pages	☐
	6	"1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer," Cypress Advance Information, 02/12/2004; 9 pages	☐
	7	"10 Gigabit Ethernet Technology Overview White Paper", Revision 1.0, Retrieved from Internet: URL: http:// www.10gea.org, May, 2001.	☐
	8	"16K x 8/9 Dual-Port Static RAM with Sem, Int, Busy," Cypress Semiconductor Data Book, May 1995, CY7C006 and CY7C016, pp. 6:1-17; 10 pages	☐
	9	"1K x 8 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C130/CY7C131 and CY7C140/ CY7C141, pp. 6:37-49; 8 pages	☐
	10	"1kHz to 30MHz Resistor Set SOT-23 Oscillator", Initial Release Final Electrical Specifications LTC1799, Linear Technology Corporation, Jan. 2001, pp. 1-4.	☐
	11	"200-MBaud HOTLink Transceiver," Cypress Semiconductor Corporation, Revised 2/13/2004, CY7C924ADX, Document #38-02008 Rev. *D; 62 pages	☐
	12	"2K x 16 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C133 and CY7C143, pp. 6:63-73; 7 pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	13	"2K x 8 Dual-Port Static RAM," Cypress Semiconductor Data Book, May 1995, CY7C132/CY7C136 and CY7C142/ CY7C146, pp. 6:50-62; 8 pages	☐
	14	"A Novel Integration Technology of EEPROM Embedded CMOS Logic VLSI Suitable for ASIC Applications", By Masataka Takebuchi et al., IEEE 1992 Custom Integrated Circuits Conference, pp. 9.6.1-9.6.4.	☐
	15	"A Novel Robust and Low Cost Stack Chips Package and Its Thermal Performance", By Soon-Jin Cho et al., IEEE Transaction on Advanced Packaging, vol. 23, No. 2, May 2000, pp. 257-265.	☐
	16	"A Planar Type EEPROM Cell Structure by Standard CMOS Process for Integration with Gate Array, Standard Cell, Microprocessor and for Neural Chips", By Katsuhiko Ohsaki et al., IEEE 1993 Custom Integrated Circuits Conference, pp-23.6.1-23.6.4.	☐
	17	"A Single Chip Sensor & Image Processor for Fingerprint Verification" Anderson, S., et al., IEEE Custom Integrated Circuits Conference, May 12-15, 1991.	☐
	18	"A Single Poly EPROM For Custom CMOS Logic Applications", By Reza Kazerounian et al., IEEE 1986 Custom Integrated Circuits Conference, pp. 59-62.	☐
	19	"A Wide-Bandwidth Low-Voltage PLL for PowerPC.TM. Microprocessors", By Jose Alvarez et al., IEEE Journal of Solid-State Circuits, vol. 30, No. 4, Apr. 1995, pp. 383-391.	☐
	20	"About SMaL Camera Technologies, Inc.", SMaL Camera Technologies, 2001, 1 page.	☐
	21	"Achieving Uniform nMOS Device Power Distribution for Sub-micron ESD Reliability;" Charvaka Duvvuy, Carlos Diaz, and Tim Haddock; 1992; 92-131 through 92-134, no month.	☐
	22	"ADNS-2030 High Performance, Low Power Optical Mouse Sensor (Optimized for Cordless Mouse Applications)," Agilent Technologies, downloaded 10/10/2005, <http://www.home.agilent.com/USeng/nav/-536893734,536883737/pd.html>; 2 pages	☐
	23	"ADNS-2051 High-Performance Optical Mouse Sensor," Agilent Technologies, downloaded 10/10/2005, <http://www.home.agilent.com/USeng/nav/-536893734,536883737/pd.html>; 2 pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	24	"Agilent ADNK-2030 Solid-State Optical Mouse Sensor," Agilent Technologies Inc., Sample Kit, 2003; 1 page	☐
	25	"Agilent ADNS-2030 Low Power Optical Mouse Sensor," Agilent Technologies Inc., Data Sheet, 2005; 34 pages	☐
	26	"Agilent ADNS-2051 Optical Mouse Sensor," Agilent Technologies Inc., Product Overview, 2003; 2 pages	☐
	27	"Agilent Optical Mouse Sensors," Agilent Technologies Inc., Selection Guide, 2004; 3 pages	☐
	28	"Algorithm for Managing Multiple First-In, First-Out Queues from a Single Shared Random-Access Memory," IBM Technical Disclosure Bulletin, August 1989; 5 pages	☐
	29	"Am99C10A 256.times.48 Content Addressable Memory", Advanced Micro Devices, Dec. 1992.	☐
	30	"An Analog PLL-Based Clock and Data Recovery Circuit with High Input Jitter Tolerance", By Sam Yinshang Sun, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-24, pp. 325-330, Apr. 1989, pp. 383-385.	☐
	31	"An EEPROM for Microprocessors and Custom Logic", By Roger Cuppens et al., IEEE Journal of Solid-State Circuits, vol. SC-20, No. 2, Apr. 1985, pp. 603-608.	☐
	32	"An EPROM Cell Structure foe EPLDs Compatible with Single Poly Gate Process", By Kuniyushi Yoshikawa et al., Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 323-326.	☐
	33	"An Experimental 5-V-Only 256-kbit CMOS EEPROM with a High-Performance Single-Polysilicon Cell", By Jun-Ichi Miyamoto et al., IEEE Journal of Solid State Circuits, vol. SC-21, No. 5, Oct. 1986, pp. 852-860.	☐
	34	Application Number 13/428,201 (CD11072): "Method of Integrating A Charge-Trapping Gate Stack Into A CMOS Flow" Krishnaswamy Ramkumar et al., filed on 03232012; 38 Pages	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

If you wish to add additional non-patent literature document citation information please click the Add button			
EXAMINER SIGNATURE			
Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Larry J. Johnson/	Date (YYYY-MM-DD)	2013-04-19
Name/Print	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Sandisk Technologies, Inc. - Ex. 1040, Page 000157

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Igor Polishchuk	)	Examiner: YUSHIN, NIKOLAY K
	)	
Application No.: 13/539,466	)	Group Art Unit: 2893
	)	
Filed: July 1, 2012	)	Confirmation No.: 5842
	)	
For: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	)	
	)	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty of disclosure under 37 CFR § 1.56 and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

No fee is believed necessary for the submission of this Information Disclosure Statement. However, The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

/

/

/

/

/

/

Should the Examiner have any questions, Applicants' undersigned attorney is reachable by telephone in our San Jose office at (408) 545-7194. The correspondence address of record appears below

Respectfully submitted,

Date: 04/19/2013 By: \Larry J. Johnson\
Larry J. Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Electronic Acknowledgement Receipt

EFS ID:	15570945
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Customer Number:	60909
Filer:	Larry Joel Johnson/Rosemary Saint-Vincent
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	19-APR-2013
Filing Date:	01-JUL-2012
Time Stamp:	22:09:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1_IDSform_04192013.pdf	1974400 3325ef75e1b3e3ae2b4bbd856ec07b9b5ee07b42	no	13

Warnings:	
Information:	

This is not an USPTO supplied IDS fillable form					
2	Transmittal Letter	PM07027C1CIP1_TransmittalLetter_04192013.pdf	290150 e78d4b1d944a6956850c7617aacbd7a2fd79f0d3	no	2
Warnings:					
Information:					
3	Non Patent Literature	Altera_MAX9000ProgrammableLogicDeviceFamily.pdf	8913303 7c5133eeeb72d44045a7f4232080e5d0f35d0215	no	41
Warnings:					
Information:					
4	Non Patent Literature	Carley_TrimmingAnalogCircuits.pdf	616788 3e8796104af87001f67707f3d2900427b3d73528	no	7
Warnings:					
Information:					
5	Non Patent Literature	CD06045_NOA_03142013.pdf	2502767 b4ce117b403b1ff79cc4fb747e5af464a012f211	no	10
Warnings:					
Information:					
6	Non Patent Literature	CD07172_NOA_04302010.pdf	319701 3ef3d6c0d214792b684b0c3d8fafdb5084d14c00	no	7
Warnings:					
Information:					
7	Non Patent Literature	JEDECCompliantZeroDelayBuffer.pdf	286030 11990d72d14ce76686046b2daa8a1cddfe44b23e	no	9
Warnings:					
Information:					
8	Non Patent Literature	10GigabitEthernetTechnology_Rev1_May2001.pdf	1110289 cf030d9b4635749b25101ae6aac8d4916e797ca9	no	22
Warnings:					
Information:					
9	Non Patent Literature	16Kx89DualPortStaticRAMwithSem.pdf	1969739 d40685474f302abf933576c2deed7f78a3d9ccc4	no	10
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					

10	Non Patent Literature	1Kx8DualPortStaticRAM.pdf	1574522 8c9efee28305a17adc7057e8a0767f8dfa8b5ab6	no	8
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
11	Non Patent Literature	1khzTo30mhz_ResistorSetSOT23Oscillator.pdf	971585 f7d41d0de53eebdba243778636f27a0ec7375288	no	5
Warnings:					
Information:					
12	Non Patent Literature	200MBaudHOTlinkTransceiver.pdf	17316096 35c7125950131de0f31f39e1e8e106106ead7ba8	no	62
Warnings:					
Information:					
13	Non Patent Literature	2Kx16DualPortStaticRAM.pdf	3478006 fde09a46f3bafcb52c011f281250d62316f03fda	no	7
Warnings:					
Information:					
14	Non Patent Literature	2Kx8DualPortStaticRAM.pdf	4118783 cfb3040e79eccdc85f5c1e41a3efe14706de827a	no	8
Warnings:					
Information:					
15	Non Patent Literature	Takebuchi_NovelIntegrationTechPDF.pdf	745818 cb4c00e5327cb452598b75229a1acc1841022c2e	no	4
Warnings:					
Information:					
16	Non Patent Literature	Cho_NovelRobustLowCostStack.pdf	782770 a4832fdf15721cb0be2c06d232458ee105d28b46	no	10
Warnings:					
Information:					
17	Non Patent Literature	Ohsaki_PlanarTypeNeuralChipsPDF.pdf	1022642 c653d13e50a575924f2423394176f987d6afe541	no	4
Warnings:					
Information:					
18	Non Patent Literature	Anderson_AsingleChipSensorAndImageProcessor.pdf	1412868 664d8fe2d78e39ccfe26650591314db66272eb1a	no	4

Warnings:					
Information:					
19	Non Patent Literature	Kazerounian_AsinglePolyEPROMforCustomCMOS.pdf	1184198 ec8b6063dbbe407101d014d065f0652fbc7cc7c6	no	4
Warnings:					
Information:					
20	Non Patent Literature	PM04006KR_OA_12262011.pdf	1331198 a3ffad896f9ecd06ab1da1d9cc98c11f146d8120	no	6
Warnings:					
Information:					
21	Non Patent Literature	Alvarez_WideBandwidth.pdf	1170512 624bdf00c4b4e8fae585417ccca5e597cc91d337	no	2
Warnings:					
Information:					
22	Non Patent Literature	AboutSMaLCameraTechnologies.pdf	734160 355c8cf4fc6465e1b17b350ca5d756bd18691e3e	no	3
Warnings:					
Information:					
23	Non Patent Literature	Duvvury_AcheivingUniformnMOSDevicePowerDistrib.pdf	2041601 7adfa2413c0e4dc5f62602ac97d676363d005100	no	4
Warnings:					
Information:					
24	Non Patent Literature	ADNS2030HighPerformanceLowPowerOpticalMouseSensor.pdf	6237910 2353d3a58ff40214d04dc8d3499c7d26bfad02b4	no	34
Warnings:					
Information:					
25	Non Patent Literature	ADNS2051HighPerformanceOpticalMouseSensor.pdf	440822 d28eed31c140d9aaeb411bfe78152f3328e88fdf	no	2
Warnings:					
Information:					
26	Non Patent Literature	AgilentADNK2030SampleKit.pdf	292293 6e9cd9a3020640f04fc77a592d35d8cd563d4c54	no	1
Warnings:					
Information:					
27	Non Patent Literature	AgilentADNS2030LowPowerOpticalMouseSenosrDataSheet.pdf	6237916 2f701b93d4e53ce58fde003b520fb9e08b8c22e0	no	34

Warnings:					
Information:					
28	Non Patent Literature	AgilentADNS2051OpticalMouseSensorOverview.pdf	572657 4e2b6dccddd613b7710e6a3e8ecc9ae5398f24f0	no	2
Warnings:					
Information:					
29	Non Patent Literature	AgilentOpticalMouseSelectionGuide.pdf	506893 2e3560708341c44d31b464847997009063a0e40b	no	3
Warnings:					
Information:					
30	Non Patent Literature	AlgorithmForManagingMultipleFirstIn.pdf	1307372 b02d776b842781a16ba4f306917f5805a011c3fb	no	5
Warnings:					
Information:					
31	Non Patent Literature	Am99C10AContentAddressableMemory.pdf	8277596 27c1d1d84f8d848b2b7a86b791c139eede8c3e94	no	26
Warnings:					
Information:					
32	Non Patent Literature	Sun_AnAnalogPLLBasedClockAndDatRecoveryCircuit_1989.pdf	1560122 9cc5d4db0144ea1b54084e910a5ee7549965a794	no	6
Warnings:					
Information:					
33	Non Patent Literature	Cuppens_AnEEPROMforMicroprocessorsAndCustomLogic.pdf	3436269 72b12203e2f29592276ddca9749a7cadb4728b42	no	6
Warnings:					
Information:					
34	Non Patent Literature	Yoshikawa_AnEPROMcellStructure.pdf	1237223 17f9c0d992191de39d2e83e928e02074b390a011	no	5
Warnings:					
Information:					
35	Non Patent Literature	Miyamoto_AnExperimental5Vonly2565kbitCMOS.pdf	3264829 78876b7be1336949e2df86292b57fdfb04658e62	no	9
Warnings:					
Information:					
36	Non Patent Literature	CD11072_Application_03232012.pdf	1137472 a94e0ab2b0952309fe8d67fa9ac606016fa37db7	no	38

Warnings:	
Information:	
Total Files Size (in bytes):	90377300

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
If you wish to add additional U.S. Patent citation information please click the Add button.						Add

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090152621	A	2009-06-18	Polishchuk et al.	Entire Document
If you wish to add additional U.S. Published Application citation information please click the Add button.						Add

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								Add

NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13539466
	Filing Date	2012-07-01
	First Named Inventor	Igor Polishchuk
	Art Unit	2893
	Examiner Name	YUSHIN, NIKOLAY K
	Attorney Docket Number	PM07027D1CIP1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Larry J. Johnson/	Date (YYYY-MM-DD)	2012-12-21
Name/Print	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	13/539,466	Filing Date	2012-07-01	Docket Number (if applicable)	PM07027D1CIP1	Art Unit	2893
First Named Inventor	Igor POLISHCHUK			Examiner Name	YUSHIN, NIKOLAY K		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503781

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Larry J. Johnson/	Date (YYYY-MM-DD)	2012-12-21
Name	Larry J. Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13539466
Filing Date:	01-Jul-2012
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Filer:	Larry Joel Johnson/Lauren Navarro
Attorney Docket Number:	PM07027D1CIP1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	930	930
		Total in USD ($)		**930**

Electronic Acknowledgement Receipt	
EFS ID:	14541532
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Customer Number:	60909
Filer:	Larry Joel Johnson/Lauren Navarro
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	21-DEC-2012
Filing Date:	01-JUL-2012
Time Stamp:	13:18:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$930
RAM confirmation Number	15149
Deposit Account	503781
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	PM07027D1CIP1_TransmittalLetter_12212012.pdf	28611 a9332d960b08021b6efa718c5fb4c1ab18727aca	no	2
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	PM07027D1CIP1_IDSform_12212012.pdf	611599 465ebb267884c631f6c0a6744237636c12e8840f	no	4
Warnings:					
Information:					
3	Request for Continued Examination (RCE)	PM07027D1CIP1_RCE_12212012.pdf	699515 e4316e622ea8e53c5301ef44b1722045bd90ea5c	no	3
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30653 feb6e26793e7323dd7516b28d1d4e9375c83bd53	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1370378		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Igor POLISHCHUK	Examiner: YUSHIN, NIKOLAY K
Application No.: 13/539,466	Group Art Unit: 2893
Filed: July 1, 2012	Confirmation No.: 5842
For: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

REQUEST FOR CONTINUED EXAMINATION AND INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the Request for Continued Examination to be considered with the IDS for the above referenced application. In compliance with the duty of disclosure under 37 CFR § 1.56 and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

Customer No.: 60909

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

/

/

Respectfully submitted,

Date: 12/21/2012

By: /Larry J. Johnson/

Larry J. Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Customer No.: 60909

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 11/27/2012
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/27/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$0	$0	$1770	02/27/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Sandisk Technologies, Inc. - Ex. 1040, Page 000179

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 11/27/2012
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

TITLE OF INVENTION: MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$0	$0	$1770	02/27/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
YUSHIN, NIKOLAY K	2893	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sandisk Technologies, Inc. - Ex. 1040, Page 000180

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

60909 7590 11/27/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 11/27/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Sandisk Technologies, Inc. - Ex. 1040, Page 000181

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	13/539,466	POLISHCHUK ET AL.	
	Examiner	Art Unit	
	NIKOLAY YUSHIN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed on 11/10/2012*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-5 and 7-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/NIKOLAY YUSHIN/
Examiner, Art Unit 2893

DETAILED ACTION

Status of Claims

Applicant's cancellation of claim 6 in the reply filed on 11/10/2012 is acknowledged.

Applicant's amendment of claims 1 and 8-10 in the reply filed on 11/10/2012 is acknowledged.

Claims 1-5 and 7-20 are under consideration in this Office Action.

Allowable Subject Matter

Claims 1-5 and 7-20 are allowed.

The following is an examiner's statement of reasons for allowance:

In re Claim 1, Levy et al., US 2009/0179253 taken with Zheng et al., US 6,912,163 and Yan, US 2008/0135946 discloses all limitations of claim 1 except for " a high work function gate electrode formed over a surface of the ONNO stack; and a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode." Therefore, the claimed differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 10, Levy taken with Zheng and Yan discloses all limitations of claim 10 except for " a high work function gate electrode formed over a surface of the ONNO stack, wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer." Therefore, the claimed differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 11, prior-art fails to disclose semiconductor device comprising: a memory transistor including "an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer." Therefore, the claimed differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 18, prior-art fails to disclose semiconductor device comprising: a memory transistor including "a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region; a tunnel dielectric layer abutting the vertical channel." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Friday from 8 a.m. to 5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/THOMAS L DICKEY/
Primary Examiner, Art Unit 2826

/NIKOLAY YUSHIN/
Examiner, Art Unit 2893

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	("8063434").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 09:50
S2	18	("20030122204" | "20050230766" | "20060131636" | "20070246753" | "20070262451" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080290399" | "20100041222" | "20100295118" | "6906390" | "6912163" | "7312496" | "7323742" | "7737488" | "7790516").PN. OR ("8063434").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 09:51
S3	19	((IGOR) near2 (POLISHCHUK)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:01
S4	7	("20010012667" | "20030178675" | "20030232507" | "20040082198" | "20100090294" | "20100167506" | "7799670").PN. OR ("8163660").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:04
S5	34	((SAGY) near2 (LEVY)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:05
S6	88	((KRISHNASWAMY) near2 (RAMKUMAR)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:07
S7	8	("20070029625" | "20070031999" | "20080286927" | "20090039414" | "7315474" | "7576386" | "7636257" | "7646637").PN. OR ("8222688").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:10
S8	78	(S3 OR S5 OR S6) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:19
S9	1	((oxide$1nitride$1nitride$1oxide OR ONNO) NEAR4 stack) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:28
S10	1	((oxide$1nitride$1nitride$1oxide OR ONNO) NEAR4 stack)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30
S11	655	((oxide$1nitride$1nitride$1oxide OR ONNO))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30
S12	292	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory	US-PGPUB; USPAT;	AND	ON	2012/09/26 10:30

Sandisk Technologies, Inc. - Ex. 1040, Page 000187

			USOCR			
S13	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (oxygen$1rich) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:31
S14	0	((oxide$1nitride$1nitride$1oxide OR ONNO)) SAME (oxygen$1rich)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:12
S15	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (oxygen$1rich)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:12
S16	0	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S2	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S17	1	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S8	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S18	1	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S6	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S19	2	(("6906390") or ("6912163")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 11:16
S20	29727	((oxide$1nitride$11oxide OR ONO)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S21	135	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S22	59	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S23	46	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:21
S24	46	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S23	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:21
S25	41	("4173766" | "5168334" | "5349221" | "5644533" | "5751037" | "5768192" | "5825686" | "5963465" | "5966603" | "6001709" | "6011725" | "6030871" | "6117730" | "6287917" | "6326268").PN. OR ("6465306").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:31
S26	17	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) (substrate NEAR4 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:46

Sandisk Technologies, Inc. - Ex. 1040, Page 000188

S27	6	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) (channel NEAR4 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:47
S28	467	((oxide$1nitride$11oxide OR ONO)) (channel NEAR2 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:48
S29	60	((oxide$1nitride$11oxide OR ONO)) (channel NEAR2 polysilicon)	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 11:49
S30	91	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory channel	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:02
S31	0	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) Near3 channel))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S32	1	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) NEAR3 substrate))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S33	2	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) SAME substrate))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S34	3	((oxide$1nitride$1nitride$1oxide OR ONNO)) (OXYGEN same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:16
S35	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (OXYGEN$1RICH same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:17
S36	256	(OXYGEN$1RICH same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:19
S37	119	(OXYGEN$1RICH same NITRIDE) MEMORY CHANNEL	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:20
S38	11	(OXYGEN$1RICH same NITRIDE) MEMORY (POLYSILICON near4 CHANNEL)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:20
S39	8	(OXYGEN$1RICH same NITRIDE) MEMORY (logic near4 MOS)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:45
S40	29	("20030227049" | "20040071030" | "20040129986" | "20050186741" | "20060202263" | "20060226490" | "20060281331" | "4843023" | "5405791" | "5573963" | "5793089" | "5861347" | "6025267" | "6074915" | "6174774" | "6277683" | "6429081" | "6599795" |	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:51

Sandisk Technologies, Inc. - Ex. 1040, Page 000189

		"6730566" | "6946349" | "7015100" | "7045424" | "7098154" | "7172940" | "7250654" | "7253046" | "7262457" | "7544565" | "7588986").PN. OR ("8143129").URPN.				
S41	29	("20030227049" | "20040071030" | "20040129986" | "20050186741" | "20060202263" | "20060226490" | "20060281331" | "4843023" | "5405791" | "5573963" | "5793089" | "5861347" | "6025267" | "6074915" | "6174774" | "6277683" | "6429081" | "6599795" | "6730566" | "6946349" | "7015100" | "7045424" | "7098154" | "7172940" | "7250654" | "7253046" | "7262457" | "7544565" | "7588986").PN. OR ("8143129").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:51
S42	20	(PMOS SAME SONOS SAME memory) (NMOS SAME logic)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:58
S43	11	(PMOS SAME SONOS SAME memory) (NMOS SAME logic) (polysilicon adj gate)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:59
S48	5	(high$1K NEAR4 (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 13:23
S49	51	(high$1K SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 13:25
S50	976	(dielectric SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:29
S51	151	((dielectric adj constant) SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:29
S52	41	((high adj dielectric adj constant) SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:30
S53	2691	257/314.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:41
S54	11	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S53	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:42
S55	13	(((oxide$1nitride$11oxide OR ONO)) ((oxygen$1rich) SAME nitride)) S53	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:43
S56	2404	257/324.ccls.	US-PGPUB; USPAT;	AND	ON	2012/09/26 14:44

Sandisk Technologies, Inc. - Ex. 1040, Page 000190

			USOCR			
S57	24	(((oxide$1nitride$11oxide OR ONO)) ((oxygen$1rich) SAME nitride)) S56	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:44
S58	9	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S56	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:45
S59	13	("20060261401" | "20080258203" | "6709928" | "20030123307" | "6445030" | "7450423" | "7042054" | "4543707" | "6157426" | "6677213" | "6958511" | "20020154878" | "6818558").PN.	US-PGPUB; USPAT	AND	ON	2012/09/26 14:48
S60	186	257/E29.132.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:04
S61	1	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S60	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:05
S62	2	((oxide$1nitride$11oxide OR ONO) (oxygen$1rich SAME nitride)) S60	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:05
S63	2	((oxide$1nitride$11oxide OR ONO) oxygen$1rich nitride) S60	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
S64	2536	257/E29.309.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
S65	11	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S64	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
S66	11	((oxide$1nitride$11oxide OR ONO)) (channel SAME (recrystallized adj polysilicon))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:08
S67	20	((oxide$1nitride$11oxide OR ONO)) (channel SAME (silicon adj nano$1wire))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:10
S68	1	("20100117138").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:03
S69	1	("6093596").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:22
S70	1	("6093590").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:22

Sandisk Technologies, Inc. - Ex. 1040, Page 000191

S71	2278	((high adj dielectric adj constant) SAME (tantalum adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:28
S72	2278	((high adj dielectric adj constant) SAME (high adj dielectric adj constant) SAME (tantalum adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:29
S73	1480	S72 memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:29
S74	280	(((oxide$1nitride$11oxide OR ONO))) S73	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:30
S75	274	((oxide$1nitride$11oxide OR ONO) nitride) S73	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:31
S76	230	((oxide$1nitride$11oxide OR ONO) nitride) AND S73	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 16:31
S77	196	transistor S76	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:32
S78	20	((oxide$1nitride$11oxide OR ONO) nitride transistor) AND S73	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 16:32
S79	47	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/11/14 09:54
S80	6	("20050287763" | "20060202263" | "6274901" | "7067377").PN. OR ("7732276").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/11/14 09:56
S81	18	("20030122204" | "20050230766" | "20060131636" | "20070246753" | "20070262451" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080290399" | "20100041222" | "20100295118" | "6906390" | "6912163" | "7312496" | "7323742" | "7737488" | "7790516").PN. OR ("8063434").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/11/14 09:57

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	56	((memory adj transistor) polysilicon (work adj function) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:27
L2	1	l1 257/324.ccls.	US-	AND	ON	2012/11/14

Sandisk Technologies, Inc. - Ex. 1040, Page 000192

			PGPUB; USPAT; UPAD			10:28
L3	43	((oxide$1nitride$1nitride$1oxide OR "ONNO") stack)	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:40
L4	1	L3 257/324.ccls.	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:40
S82	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR ONNO) stack multi$1layer charge$1trap$4 oxygen$1rich oxygen$1lean (work adj function adj gate adj electrode) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor)).CLM.	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:04
S83	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR ONNO) stack multi$1layer charge$1trap$4 oxygen$1rich oxygen$1lean (work adj function adj gate adj electrode) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:04
S84	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR "ONNO") stack multi$1layer charge$1trap$4 oxygen$1rich oxygen$1lean (work adj function adj gate adj electrode) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:04
S85	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR "ONNO") stack multi$1layer charge$1trap$4 oxygen$1rich oxygen$1lean (work adj function) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:05
S86	0	((memory adj transistor) channel source drain region substrate polysilicon (oxide$1nitride$1nitride$1oxide OR "ONNO") stack multi$1layer oxygen$1rich oxygen$1lean (work adj function) ((metal adj oxide adj semiconductor) OR MOS) (logic adj transistor))	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:05
S87	1	((oxide$1nitride$1nitride$1oxide OR "ONNO") stack multi$1layer oxygen$1rich oxygen$1lean)	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:05
S88	1	((oxide$1nitride$1nitride$1oxide OR "ONNO") stack oxygen$1rich oxygen$1lean)	US-PGPUB; USPAT; UPAD	AND	ON	2012/11/14 10:06
S89	43	((oxide$1nitride$1nitride$1oxide OR "ONNO") stack)	US-PGPUB; USPAT;	AND	ON	2012/11/14 10:06

Sandisk Technologies, Inc. - Ex. 1040, Page 000193

			UPAD				

11/ 14/ 2012 10:56:59 AM
C:\ Users\ nyushin\ Documents\ EAST\ Workspaces\ 13539466.wsp

Sandisk Technologies, Inc. - Ex. 1040, Page 000194

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5842

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/539,466	07/01/2012	257	2893	PM07027D1CIP1

APPLICANTS

Igor POLISHCHUK, Fremont, CA;
Sagy LEVY, Zichron-Yoakev, ISRAEL;
Krishnaswamy RAMKUMAR, San Jose, CA;

**** CONTINUING DATA ***************************

This application is a CIP of 13/288,919 11/03/2011
which is a DIV of 12/152,518 05/13/2008 PAT 8,063,434
which claims benefit of 60/940,160 05/25/2007

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

07/16/2012

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/NIKOLAY K YUSHIN/ Examiner's Signature	☐ Initials	CA	13	20	3

ADDRESS

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709
UNITED STATES

TITLE

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

FILING FEE RECEIVED		
1630	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
13539466	POLISHCHUK ET AL.
Examiner	**Art Unit**
NIKOLAY YUSHIN	2893

ORIGINAL		INTERNATIONAL CLASSIFICATION														
CLASS	SUBCLASS	CLAIMED									NON-CLAIMED					
257	324	H	0	1	L	29 / 792 (2006.0)										

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	E29.132	E29.309			

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	13	17												
2	2	17	18												
6	3	18	19												
7	4	19	20												
8	5														
	6														
3	7														
4	8														
5	9														
9	10														
10	11														
14	12														
15	13														
16	14														
11	15														
12	16														

/NIKOLAY YUSHIN/ Examiner.Art Unit 2893	11/14/2012	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	19	
/THOMAS L DICKEY/ Primary Examiner.Art Unit 2826	11/16/2012	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8A

Sandisk Technologies, Inc. - Ex. 1040, Page 000196

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	Art Unit
	NIKOLAY YUSHIN	2893

SEARCHED

Class	Subclass	Date	Examiner
257	314, 324, E29.132; E29.309	09/26/2012	NY

SEARCH NOTES

Search Notes	Date	Examiner
Keyword, inventor names, assignee searching - see search history	09/26/2012	NY
Updated keyword searching - see search history	11/14/2012	NY

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
257	324	11/14/2012	NY

/NIKOLAY YUSHIN/ Examiner.Art Unit 2893	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	13/539,466	Confirmation No. 5842
In re Application of	:	Igor Polishchuk, et al.	
Filed	:	July 1, 2012	
TC/A.U.	:	2893	
Examiner	:	YUSHIN, NIKOLAY K	
Docket No.	:	PM07027D1CIP1	
Customer No.	:	60909	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

This paper is responsive to the Office Action mailed on September 28, 2012, and is timely filed.

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper

Sandisk Technologies, Inc. - Ex. 1040, Page 000198

Amendments to the Claims:

1. (Currently Amended) A semiconductor device comprising:

a memory transistor including:

a channel region electrically connecting a source region and a drain region formed in a substrate, the channel region comprising polysilicon;

an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer; and

a high work function gate electrode formed over a surface of the ONNO stack; and

a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode.

2. (Original) The semiconductor device of claim 1, wherein the channel comprises a silicon nanowire.

3. (Original) The semiconductor device of claim 1, wherein the channel region comprises recrystallized polysilicon.

4. (Currently Amended) The semiconductor device of claim 3, the high work function gate electrode of the memory transistor comprises a P+ doped polysilicon layer.

Sandisk Technologies, Inc. - Ex. 1040, Page 000199

5. (Original) The semiconductor device of claim 4, wherein the ONNO stack further includes a blocking dielectric layer disposed above the multi-layer charge-trapping region, and wherein the blocking dielectric layer comprises a dielectric comprises a high K High Temperature Oxide (HTO).

6. Cancelled

7. (Currently Amended) The semiconductor device of claim [6]_1, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a N+ doped polysilicon layer to form an P-type (PMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a N-type (NMOS) logic transistor.

8. (Currently Amended) The semiconductor device of claim [6]_1, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a P+ doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (NMOS) logic transistor.

9. (Currently Amended) The semiconductor device of claim [6]_1, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor are formed from a single, patterned doped polysilicon layer.

Sandisk Technologies, Inc. - Ex. 1040, Page 000200

10. (Currently Amended) ~~The semiconductor device of claim 1~~A semiconductor device comprising:

a memory transistor including:

a channel region electrically connecting a source region and a drain region formed in a substrate, the channel region comprising polysilicon;

an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer; and

a high work function gate electrode formed over a surface of the ONNO stack,

wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer.

11. (Original) A semiconductor device comprising:

a memory transistor including:

a channel region electrically connecting a source region and a drain region formed in a substrate, the channel region comprising polysilicon;

an oxide-nitride-nitride-oxide (ONONO) stack disposed above the channel region, the ONONO stack comprising:

a tunnel dielectric layer disposed above the channel region;

a multi-layer charge-trapping region including an oxygen-rich first nitride layer disposed above the tunnel dielectric layer, an oxygen-lean second nitride

Sandisk Technologies, Inc. - Ex. 1040, Page 000201

layer disposed above the first nitride layer, and an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer; and

a blocking dielectric layer disposed above the multi-layer charge-trapping region; and

a high work function gate electrode disposed above a surface of the ONONO stack.

12. (Original) The semiconductor device of claim 11, wherein the channel region comprises recrystallized polysilicon.

13. (Original) The semiconductor device of claim 12, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.

14. (Original) The semiconductor device of claim 13, wherein the blocking dielectric layer comprises a dielectric comprises a high K High Temperature Oxide (HTO).

15. (Original) The semiconductor device of claim 11, wherein the channel comprises a silicon nanowire.

16. (Original) The semiconductor device of claim 11, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.

Sandisk Technologies, Inc. - Ex. 1040, Page 000202

17. (Original) The semiconductor device of claim 11 further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode.

18. (Original) A semiconductor device comprising:

a memory transistor including:

a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region;

an oxide-nitride-nitride-oxide (ONNO) stack disposed about the vertical channel, the ONNO stack comprising:

a tunnel dielectric layer abutting the vertical channel;

a multi-layer charge-trapping region including a first nitride layer comprising an oxygen-rich nitride abutting the tunnel dielectric layer, and a second nitride layer comprising a silicon-rich, oxygen-lean nitride overlying the first nitride layer; and

a blocking dielectric layer overlying the multi-layer charge-trapping region; and

a high work function gate electrode disposed about the ONONO stack, abutting the blocking dielectric layer.

19. (Original) The semiconductor device of claim 18, further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode.

Sandisk Technologies, Inc. - Ex. 1040, Page 000203

20. (Original) The semiconductor device of claim 18, wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer.

Sandisk Technologies, Inc. - Ex. 1040, Page 000204

REMARKS

Claims 1-5, and 7-20 are pending. Claim 6 having been canceled to facilitate prosecution. Claims 1, 7, 8, 9 and 10 have been amended.

No new matter has been added, and entry of the amendments is respectfully requested.

Summary of the Office Action

Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Levy et al., US 2009/0179253, in view of Zheng et al., US 6,912,163 and in further view of Yan, US 2008/0135946.

Claim 2 is rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Levy, Zhang, and Yan, in further view of Huerta et al., WO 20081129478 (cited in this Office Action as US 2010/0117138).

Claim 5 is rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Levy, Zhang, and Yan, and in further view of Goebel et al., US 2003/0169629.

Claims 6-10 are objected to as being dependent upon a rejected base claim, but indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11-20 are allowed.

Rejection of Claims

By this amendment claim 1 has been amended to include all features of objected to claim 6.

Accordingly, Applicants submit that claim 1, and claims 2-5 and 7-9 which are dependent therefrom, are allowable over the cited references.

By this amendment objected to claim 10 has been amended to include all features of independent claim 1.

Accordingly, Applicants submit that claim 10 is allowable over the cited references.

Sandisk Technologies, Inc. - Ex. 1040, Page 000205

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, William E. Nuttle at (650) 207-3418.

Payment is included for amending claim 10 to independence, and it is believed no additional fees are required for filing this amendment. However, if necessary, please *charge any additional fees under 37 CFR §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application,* or apply any credits to our PTO deposit account number: 50-3781.

Respectfully submitted,
Igor Polishchuk, et al.

Dated: November 10, 2012

By: /William E. Nuttle/
William E. Nuttle, Reg. No. 42,943
Attorney for the Applicant(s)
P.O. Box 4240
Foster City, CA 94404
Tel.: (650)207-3418

Sandisk Technologies, Inc. - Ex. 1040, Page 000206

Electronic Patent Application Fee Transmittal

Application Number:	13539466
Filing Date:	01-Jul-2012
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Filer:	William Edward Nuttle
Attorney Docket Number:	PM07027D1CIP1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Independent claims in excess of 3	1201	1	250	250
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**250**

Electronic Acknowledgement Receipt

EFS ID:	14198567
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Customer Number:	60909
Filer:	William Edward Nuttle
Filer Authorized By:	
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	10-NOV-2012
Filing Date:	01-JUL-2012
Time Stamp:	11:40:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$250
RAM confirmation Number	7138
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		PM07027D1CIP1_ROA.pdf	116100 3cd947e13374f6e3e0182e27a3a49ec8c5443ca8	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	9

Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30433 1874a214fc24075c94d119e401e60eb9d5c67a4c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	146533		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
13/539,466	07/01/2012	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
FOR	NUMBER FILED	NUMBER EXTRA					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/10/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X $ =		OR	X $62=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X $ =		OR	X $250=	250
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	250

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/PHYLLIS CANTY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1	5842

60909 7590 09/28/2012

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER	
YUSHIN, NIKOLAY K	
ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
09/28/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	13/539,466	POLISHCHUK ET AL.	
	Examiner	Art Unit	
	NIKOLAY YUSHIN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2012*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *11-20* is/are allowed.

7)☒ Claim(s) *1-5* is/are rejected.

8)☒ Claim(s) *6-10* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy et al., US 2009/0179253, in view of Zheng et al., US 6,912,163 and in view of Yan, US 2008/0135946.

In re Claim 1, Levy discloses a semiconductor device comprising: a memory transistor (Fig. 2) including: a channel 212 region electrically connecting a source region (210, left) and a drain region (210, right) formed in a substrate 108; an oxide-nitride-nitride-oxide (ONNO) stack 202 disposed above the channel region 212, the ONNO stack 204 comprising a multi-layer charge-trapping region (216, 220B, 220A) including an oxygen-rich first nitride layer 220B and an oxygen-lean second nitride layer 220A disposed above the first nitride layer 220B; and a gate electrode 214 formed over a surface of the ONNO stack 202 (Fig. 2; [0021-0030]).

Levy does not disclose that the gate electrode is high work function, as well as that the channel region comprising polysilicon.

Zheng teaches that N^+ -polysilicon and P^+ - polysilicon are high work function electrodes (column 5, lines 52-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Levy's polysilicon gate electrode 214 with Zheng's N^+ -polysilicon or P^+ - polysilicon electrode, to improve dielectric charge trapping memory devices as taught by Zheng (column 2, line 39).

However, Levy taken with Zhang does not teach that the channel region comprises polysilicon.

Yan teaches a semiconductor device comprising: a memory transistor (Fig. 1) wherein the channel region 220 comprises polysilicon ([0030-0036]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Levy's silicon channel 212 with Yan's polysilicon channel 220, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416* (See MPEP2144.07).

In re Claim 3, Levy taken with Zhang and Yan discloses the semiconductor device of claim 1, wherein the channel region comprises polysilicon (Yan: [0030-0036]).

The applicant's claim 3 does not distinguish over the Levy-Zhang -Yan references regardless of the process used to form polysilicon, because only the final product is relevant, not the recited process of recrystallization. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78

USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

The Federal Circuit recently revisited the question of whether a "product by process" claim can be anticipated by a reference that does not recite said process. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d at 1100. The Federal Circuit cited with approval this Office's current statement of the law, found in MPEP § 2113:

> [Even] though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.

Id. at 1101. The Federal Circuit held this statement to be consistent with its own views on this topic, as well as various Supreme Court rulings, notably *Gen. Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938) ("Although in some instances a claim may validly describe a

new product with some reference to the method of production, a patentee who does not distinguish his product from what is old except by reference, express or constructive, to the process by which he produced it, cannot secure a monopoly on the product by whatever means produced."). Id.

In re Claim 4, Levy taken with Zhang and Yan discloses the semiconductor device of claim 3, the high work function gate electrode comprises a P+ doped polysilicon layer (Zheng: column 5, lines 52-63).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, Zhang, and Yan as applied to claim 1 above, and further in view of Huerta et al., WO 2008/129478 (cited in this Office Action as US 2010/0117138).

In re Claim 2, Levy taken with Zhang and Yan discloses all limitations of claim 2, except for that the channel comprises a silicon nanowire.

Huerta teaches the semiconductor device wherein the channel comprises a silicon nanowire ([0030]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Levy-Zhang -Yan's silicon / polysilicon channel with Huerta's silicon nonowire, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416* (See MPEP2144.07).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, Zhang, and Yan as applied to claim 4 above, and further in view of Goebel et al., US 2003/0169629.

In re Claim 5, over Levy taken with Zhang and Yan discloses all limitations of claim 5 including that the ONNO stack 202 (Levy: Fig. 2) further includes a blocking dielectric layer 218 disposed above the multi-layer charge-trapping region (216, 220B, 220A) (Levy: Fig. 2; [0021-0030]) and wherein the blocking dielectric layer comprises a dielectric comprises a High Temperature Oxide (HTO) (Levy: [0030]), except for that the blocking dielectric layer comprises a dielectric comprises a **high K** High Temperature Oxide (HTO).

Goebel teaches the dielectric layer comprises a dielectric comprises a high K High Temperature Oxide, such as zirconium oxide, tantalum oxide, hafnium oxide ([0103]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Levy-Zhang -Yan's silicon oxide blocking dielectric layer 218 with Goebel's zirconium oxide, tantalum oxide, or hafnium oxide, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416* (See MPEP2144.07).

Allowable Subject Matter

Claims 6 -10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11-20 are allowed.

The following is an examiner's statement of reasons for allowance:

In re Claim 11, prior-art fails to disclose semiconductor device comprising: a memory transistor including "an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer." Therefore, the claimed differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

In re Claim 18, prior-art fails to disclose semiconductor device comprising: a memory transistor including "a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region; a tunnel dielectric layer abutting the vertical channel." Therefore, the claimed device differs from prior art devices on this point and there is no evidence it would have been obvious to make this change.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Jenne et al., US 8,222,688 (filed on 04/26/2010) discloses all limitations of claim 11 except for that the channel region comprising polysilicon, but this prior-art cannot be used in §103 rejection, because it is §102(e) reference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKOLAY YUSHIN whose telephone number is (571)270-7885. The examiner can normally be reached on Monday through Thursday from 8 a.m. to 5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NIKOLAY YUSHIN/
Examiner, Art Unit 2893

Notice of References Cited	Application/Control No. 13/539,466	Applicant(s)/Patent Under Reexamination POLISHCHUK ET AL.	
	Examiner NIKOLAY YUSHIN	Art Unit 2893	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0179253	07-2009	Levy et al.	257/324
*	B	US-6,912,163	06-2005	Zheng et al.	365/185.29
*	C	US-2008/0135946	06-2008	Yan, Shuo-Ting	257/390
*	D	US-2010/0117138	05-2010	Huerta et al.	257/324
*	E	US-2003/0169629	09-2003	Goebel et al.	365/200
*	F	US-8,222,688	07-2012	Jenne et al.	257/324
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	WO 2008/129478	10-2008	PCT	Huerta et al.,	H01L 21/28
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

PCT

(43) International Publication Date
30 October 2008 (30.10.2008)

(10) International Publication Number
WO 2008/129478 A1

(51) International Patent Classification:
H01L 21/28 (2006.01) *H01L 29/792* (2006.01)
H01L 21/336 (2006.01) *G11C 16/04* (2006.01)
H01L 21/8246 (2006.01) *H01L 29/423* (2006.01)
H01L 21/8247 (2006.01) *H01L 29/06* (2006.01)
H01L 27/115 (2006.01) *H01L 29/78* (2006.01)
H01L 29/788 (2006.01)

(21) International Application Number:
PCT/IB2008/051478

(22) International Filing Date: 17 April 2008 (17.04.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
07106502.3 19 April 2007 (19.04.2007) EP

(71) Applicant *(for all designated States except US)*: **NXP B.V.** [NL/NL]; High Tech Campus 60, NL-NL - 5656 AG Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **HUERTA, Almudena** [ES/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **VAN DUUREN, Michiel Jos** [NL/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **AKIL, Nader** [FR/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **GOLUBOVIC, Dusan** [RS/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT). **BOUTCHICH, Mohamed** [FR/BE]; c/o NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT).

(74) Agents: **RÖGGLA, Harald** et al.; NXP Semiconductors Austria GmbH, Intellectual Property Department, Gutheil-Schoder-Gasse 8-12, A-1102 Vienna (AT).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

[Continued on next page]

(54) Title: NONVOLATILE MEMORY CELL COMPRISING A NANOWIRE AND MANUFACTURING METHOD THEREOF

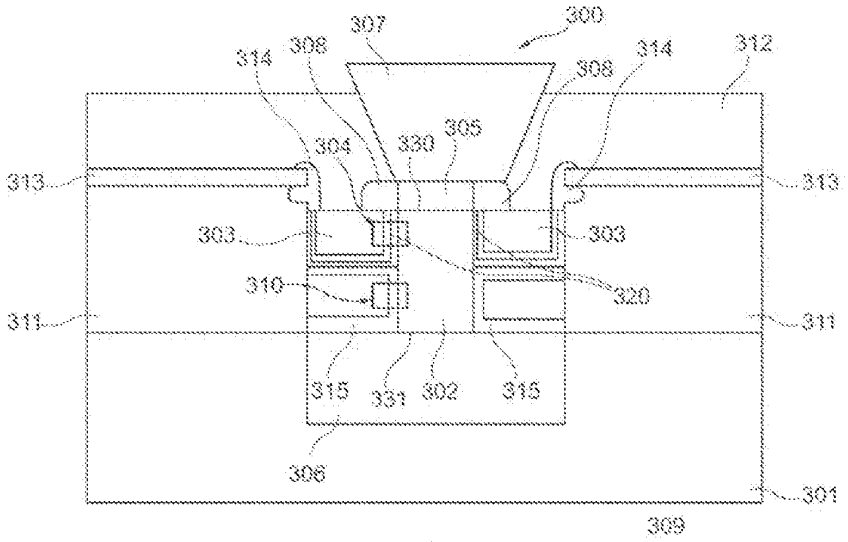


FIG. 3

(57) Abstract: A memory cell (300, 500), the memory cell (300, 500) comprising a substrate (301), a nanowire (302) extending along a vertical trench formed in the substrate (301), a control gate (303) surrounding the nanowire (302), and a charge storage structure (320, 501) formed between the control gate (303) and the nanowire (302).

WO 2008/129478 A1

Sandisk Technologies, Inc. - Ex. 1040, Page 000222

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BE, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

- *with international search report*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

NONVOLATILE MEMORY CELL COMPRISING A NANOWIRE AND MANUFACTURING METHOD THEREOF

FIELD OF THE INVENTION

The invention relates to a memory cell.

Moreover, the invention relates to a memory array.

Beyond this, the invention relates to a method of manufacturing a memory cell or a memory array comprising a plurality of memory cells.

BACKGROUND OF THE INVENTION

The storage of huge amount of information on computer systems becomes more and more important. Particularly, flash memory arrays may be employed for this purpose.

Two-transistor configurations in a memory cell with an access transistor and a memory transistor allow fast random access and low power program and erase by tunnelling.

Fig. 1 shows a conventional two-transistor configuration with a conventional floating gate memory cell 100.

In a silicon substrate 101, a source region 102, a source and drain region 103 and a drain region 104 are provided as highly doped portions. An access transistor 110 comprises a gate oxide layer 111, an access gate 112, an interpolydielectric (IPD) layer 113, a contact structure 114 and a polysilicon structure 115. Furthermore, a memory transistor 120 is provided which comprises a tunnel oxide layer 111, a floating gate 121, an interpolydielectric layer 113 and a control gate 122.

Thus, Fig. 1 shows a transistor configuration in which the memory transistor 120 is implemented with a floating gate 121. Typically, the gate oxide 111 is approximately 8 nm thick. The memory transistor 120 stores the information (charge) in the floating gate 121. Both tunnel oxide 111 and interpolydielectric 113 layer are thicker than 8 nm due to retention issues.

According to another conventional two-transistor memory architecture which is shown as a memory cell 200 in Fig. 2, an access transistor 210 is provided as well as a memory transistor 220. As a charge carrier storage structure, the memory transistor 220 includes an ONO layer 221, that is a silicon oxide - silicon nitride - silicon oxide layer sequence.

Sandisk Technologies, Inc. - Ex. 1040, Page 000224

Fig. 2 shows a so-called SONOS memory cell 200 (semiconductor - silicon oxide - silicon nitride - silicon oxide - semiconductor).

The access transistor 110, 210 (basically a MOSFET) which acts like a switch contributes to the selection/inhibition of a memory transistor 120, 220 in a memory array comprising a large number of memory cells 100, 200. The use of an access transistor 110, 210 allows the memory 100, 200 to be fully programmed and erased by Fowler-Nordheim tunnelling and allows to operate the individual memory cells 100, 200 without disturbing cross talk. The memory transistor 120, 220 stores the information that is encoded in stored electric charge. This charge can be injected in a polysilicon floating gate layer 121, a nitride layer of the ONO layer 221, nano-crystal dots, etc.

Fig. 2 therefore illustrates a transistor configuration in which the memory transistor 220 is implemented as a SONOS sequence. In this case, both the access transistor 210 and the memory transistor 220 have a single poly layer 112, 122. The gate oxide 111 of the access transistor 210 has a thickness of approximately 8 nm. The memory transistor 220 stores the information (charge) in a nitride layer 230 of approximately 6 nm thickness and is sandwiched between two insulator (SiO_2) layers, namely a bottom oxide 231 and a top oxide 232 of 2 nm and 8 nm thickness, respectively, whereas the three layers 230 to 232 form the ONO layer 221.

However, it is a problem that a standard planar flash memory cannot be scaled properly beyond 50 nm. Particularly, the scaling of tunnel and control dielectric thickness is limited by concerns for data-retention, yielding low coupling ratios and consequently high operating voltages. Moreover, one of the major limiting scaling parameters for two-transistor flash cells is the length of the access gate transistor 110, 210, which under worst case conditions (Fowler-Nordheim program inhibit) should have a leakage current not exceeding approximately 100 pA with as much as 5 V on its drain. These circumstances result in the fact that future scaled cells suffer of short channel effects and punch through phenomena, as well as of small on-current/off-current ratio, thus reducing the sensing margin.

A possible strategy is to increase the control of the gate over the channel with configurations such as double gate and FinFET transistors to increase the coupling efficiency between the control gate over the floating gate. Higher coupling is needed to scale down the programming voltages so as the memory cell dimensions. However, double gate and FinFET transistors are difficult in manufacture and operation.

US 2003/0015755 A1 discloses a vertical transistor, a memory arrangement

and a method for fabricating a vertical transistor. Particularly, US 2003/0015755 A1 discloses a vertical transistor which has a source region, a drain region, a gate region, and a channel region between the source region and the drain region, which are arranged in a vertical direction in a semiconductor substrate, the gate region having an electrical insulation from the source region, from the drain region and from the channel region and being arranged around the channel region in such a way that the gate region and the channel region form a coaxial structure.

However, with the procedure of forming a memory arrangement according to US 2003/0015755 A1, it may be difficult to obtain a sufficient integration density of memory cells. Furthermore, the manufacturing procedure according to US 2003/0015755 A1 is difficult and cost intensive.

OBJECT AND SUMMARY OF THE INVENTION

It is an object of the invention to provide a memory having a sufficient integration density.

In order to achieve the object defined above, a memory cell, a memory array, and a method of manufacturing a memory cell according to the independent claims are provided.

According to an exemplary embodiment of the invention, a memory cell is provided, the memory cell comprising a substrate, a nanowire (particularly an oblong nanowire) extending along a vertical trench formed in the substrate, a control gate surrounding the nanowire, and a charge storage structure formed between the control gate and the nanowire.

According to another exemplary embodiment of the invention, a memory array is provided, the memory array comprising a plurality of memory cells having the above-mentioned features and formed in the (common) substrate.

According to still another exemplary embodiment of the invention, a method of manufacturing a memory cell is provided, the method comprising forming a vertical trench in a substrate, forming a nanowire (particularly an oblong nanowire) extending along the vertical trench, forming a control gate surrounding the nanowire, and forming a charge storage structure between the control gate and the nanowire.

The term "memory cell" may particularly denote a physical structure (such as a layer sequence) which allows to store information in an electronic manner. An amount of

information stored in a memory cell may be 1 bit (which may be encoded, for instance, in the presence or absence of charge carriers in a dedicated structure) or may be more than 1 bit (which may be encoded, for instance, in the amount of stored charge and/or the type of the charge carriers, that is to say positively or negatively charged charge carriers).

The term "substrate" may denote any suitable material, such as a semiconductor, glass, plastic, etc. According to an exemplary embodiment, the term "substrate" may be used to define generally the elements for layers that underlie and/or overlie a layer or portions of interest. Also, the substrate may be any other base on which a layer is formed, for example a semiconductor wafer such as a silicon wafer or silicon chip.

The term "nanowire" may denote a wire-like structure of dimensions in the order of magnitude of several to several hundreds of nanometers (and may also cover larger or smaller dimensions). Many different types of nanowires may be used for embodiments of the invention, including semiconducting nanowires (for instance made of silicon, germanium, InP, GaN, etc.), metallic nanowires (for instance nickel, platinum, gold), and nanotubes, particularly carbon nanotubes (intrinsic or doped). According to an exemplary embodiment of the invention, such nanowires may form the channel of a transistor.

The term "oblong nanowire" may denote that the length of the nanowire is larger, particularly significantly larger, than a dimension perpendicular to the length extension. In other words, typical nanowires may exhibit aspect ratios (the ratio between length to width) of more than one, particularly of more than 2, more particularly of more than 5, or up to 1000 or more. For instance, a tubular nanowire may have a length of 50 nm to 70 nm and may have a diameter of 10 nm.

The term "charge storage structure" may particularly denote a structure that is specifically adapted to allow introducing electric charge in this structure by tunnelling or other programming procedures. The charge storage structure may be adapted in a manner that this charge is stored and remains stored within the structure for a sufficiently long time. Examples for appropriate charge storage structures are a floating gate, a nitride layer of an ONO layer sequence, etc.

The term "source/drain region" may particularly denote a source region or a drain region. Since the functionality of a source region and a drain region may depend on the operation mode of a transistor, for instance voltages applied thereto, the term source/drain region may denote a structure which can act as a source region or as a drain region.

The term "vertical trench" may denote an oblong blind hole formed in a surface

and extending inside of the substrate. In other words, a substrate usually has a main surface, and the trench is usually formed perpendicularly to this main surface. However, the term "vertical" may cover also embodiments in which a certain deviation from the 90° angle between trench and main surface of the substrate is present, but in which the trench still has a relatively steep orientation inside of the material of the substrate.

According to an exemplary embodiment of the invention, a method of producing memory cells is provided in which vertical nanowires are grown or are formed using an etching procedure as channels of transistors of the memory cells, wherein a gate stack may be partially or all-wrapped around the respective channel, for instance to form a coaxial structure. Furthermore, the nanowires may be grown within trenches surrounded by electrically insulating structures such as silicon oxide that provides electrical isolation between word lines in a memory array configuration. By taking this measure, it may be made possible to improve scaling issues. In other words, an area required for a memory array may be scaled down to a great extent with enhanced control over the channel. Beyond this, efficient process integration is possible to build memory arrays with vertical nanowire-based transistors.

A measure for advanced solid-state nanoelectronic devices is the surrounding gate geometry. Transistors having a surrounding gate structure have proper sub-threshold behaviour due to the high coupling efficiency and a significant reduction of short channel effects compared to double gate or FinFET devices. Silicon nanowire-based transistors exhibit advantageous properties. Moreover, vertically aligned nanowires are capable to reduce the processing complexity and result in ultra high transistor densities as the transistor geometry is pushed into the third dimension. 3D geometry also shows more relaxed conditions regarding transistor lengths that greatly helps as the access transistor should sustain 5V on its drain at low leakage current. By forming a nanowire within a trench, the growing or etching procedure may be very simple and may allow to mechanically protecting the relatively sensitive nanowire.

Such memory cells may be implemented in a SONOS (semiconductor - silicon oxide - silicon nitride - silicon oxide - semiconductor) or floating gate architecture with a single transistor or a two-transistor configuration in stand-alone flash memories. In other words, an array of 3D memory cells with one or two nanowire-based transistors may be provided for ultrahigh integration densities. Particularly, a vertical memory cell may be built around a nanowire with a gate stack of one or more transistors all wrapped around the nanowire.

More particularly, an easy process integration scheme is provided to build

arrays of three-dimensional memory cells comprising nanowire-based transistor configurations with one or two transistors. Such a cell design may enable the reduction of the whole memory array to a great extent. Moreover, as the gate stack may be all-wrapped around the nanowire, a high coupling coefficient may be obtained. By providing an all-wrapped around gate for a vertical nanowire, positioning the channel as a vertical nanowire may allow to obtain ultrahigh densities. As the gate may be all-wrapped around, there is full control of the gate over the channel that prevents short channel effects and increases the drive current density (improved access time). For an embodiment of a floating gate flash, the coupling characteristic between the control gate and the floating gate may be greatly improved, since the control gate may be all-wrapped around the floating gate. In an embodiment in which a nanowire is grown (for instance on a catalyst or precursor), there is no surface etching needed which results in a simple manufacturing architecture. In case of growing nanowire, the surface may be smooth so that it is possible to gain mobility (less traps).

By using a two-transistor configuration with an access transistor and a memory transistor, it may be possible to allow for a fast random access and a low power operation, since the program procedure and the erase procedure can be fully realized by tunnelling. The access transistor (basically a MOSFET transistor), which may act like a switch, may help in the selection/inhibition of the memory transistor within the array. The use of the access transistor may allow the memory to be fully programmed and erased by Fowler-Nordheim tunnelling.

It may be possible to select the dimensions of the nanowire width to be approximately ten (10) nm or several ten nanometers, which may be particularly advantageous in combination with the use of nitride spacers at the drain which reliably prevents any electrical contact between the drain and the gate, thus the nanowire can be much smaller than the contact. Therefore, an increased integration density may be obtained. It is also possible to manufacture the gate to be self-aligned to the trenches at the beginning of the process integration to isolate the word lines. When trenches are used, one mask may be saved which results in reduced costs. Thus, in order to define the source lines and the gates, this may be performed within one mask. The trench formation may require one additional mask, but then the source lines and the gate lines may be self-aligned to the trenches. Furthermore, the use of silicon nanowires may be cheap in manufacture.

According to an exemplary embodiment, a flash cell may be provided which is a non-volatile memory being able to store its information for a long period of time without

Sandisk Technologies, Inc. - Ex. 1040, Page 000229

refreshment.

Thus, it is possible to provide a memory array with an area that is scaled down to a great extent with enhanced control over the channel (reduced drain-induced barrier lowering, short channel effects, etc.) and drive current density (improved access time). A nanowire based memory cell according to an exemplary embodiment of the invention does not suffer from corner effects, in contrast to FinFET approaches.

The coupling efficiency between the control gate over the floating gate may be greatly improved as the control gate is all wrapped around the floating gate. The process integration is relatively easy and makes it feasible to build memory arrays with a large number of cells comprising vertical nanowire-based transistors. The process integration covers several memory cell implementations with a memory transistor implemented as a floating gate or as a SONOS, with or without an access transistor, etc.

The 3D geometry of a cell has the advantage that the channel current may flow vertically so that there is no need to scale down the length of the transistors. As the length of the transistor can be relatively long due to the vertical integration, it is possible to store multiple bits in the charge storage layer or structure, for instance with a SONOS memory transistor programmed by hot carrier injection (similar to an NROM).

Therefore, vertical nanowires may be grown as a channel of transistor of the memory cell, where the gate stack may be all-wrapped around a channel. The nanowire may be grown within trenches surrounded by silicon dioxide which may provide isolation between the bit lines in an array configuration.

Next, further exemplary embodiments of the memory cell will be explained. However, these embodiments also apply to the memory array and to the method.

The memory cell may comprise a first source/drain region (particularly a drain) coupled to a substrate external end portion of the nanowire and may comprise a second source/drain region (particularly a source) coupled to a substrate internal end portion of the nanowire. In other words, the end portion of the nanowire which is deepest buried within the trench connected to the substrate may form the second source/drain region, whereas the end portion of the nanowire which is closer to the main surface of the layer sequence (close to the bit lines) may form the first source/drain region. The first and second source/drain regions may be doped, for instance n^+-doped or p^+-doped. In contrast to this, the nanowire may be intrinsically or weakly doped, for instance may be n-doped or p-doped. Thus, the nanowire may form the channel portion of a nanowire-based field effect transistor.

Sandisk Technologies, Inc. - Ex. 1040, Page 000230

A contact structure may be coupled to the first source/drain region. Such a contact structure may be an electrically conductive portion which provides an electric coupling between the nanowire and an environment external to the memory cell which may be formed as a monolithically integrated circuit. Thus, such a contact structure may be a filled via and may be made of materials such as highly doped polysilicon, silicide, or may be made from a metallic material such as copper or nickel.

The memory cell may comprise an electrically insulating spacer structure surrounding the first source/drain region for securely electrically decoupling the first source/drain region from the control gate. Such an electrically insulating spacer structure may be formed on a laterally limited layer sequence, whereas the lateral walls of such a layer sequence may be covered with an electrically insulating material such as silicon dioxide (SiO_2) or silicon nitride (Si_3N_4). It may be highly advantageous to reliably decouple the source/drain region from the control gate to avoid undesired current paths or leakage currents.

The contact structure may be broader than the first source/drain region in a lateral direction. Such a lateral direction may be orthogonal to the vertical direction along which the nanowire extends. When the nanowire is smaller than the contact, an undesired electrically contact between the drain and the gate may be prevented.

The charge storage structure may comprise at least one of the group consisting of a floating gate, an ONO structure, a silicon nitride structure, and a nano-crystal dot structure. A floating gate may be an electrically conductive portion such as a polysilicon structure in which charge carriers may be stored by tunnelling or other programming procedures. An ONO structure is a silicon oxide - silicon nitride - silicon oxide layer sequence, wherein charge carriers may be permanently stored in the nitride layer by Fowler-Nordheim tunnelling or the like. A simple silicon nitride layer may also serve as a basis for a proper charge storage structure, for instance in an embodiment in which miniature dimension of the memory cell is desired. However, also nano-crystals may be used to store charge carriers such as electrons or holes.

The control gate may surround the nanowire along its entire circumference. In other words, the control gate may be provided with a blind hole through which the nanowire extends, thereby forming a coaxial nanowire gate structure. This may allow for an accurate control of the electrical conductivity of the nanowire by applying an electric voltage to the control gate.

A cross-section of the nanowire may have a diameter of less than 100 nm,

particularly of less than fifty (50) nm, more particularly of less than twenty (20) nm. According to a preferred embodiment, the nanowire has a diameter of 10 nm that allows to properly control conductivity by the surrounding gate.

Furthermore, an access gate may be provided surrounding the nanowire. The access can be part of an access transistor which may be considered as a switch which can be switched on or off by applying a voltage to the access gate. By such a two-transistor configuration, namely a configuration with an access gate and a control gate, a properly controllable memory system may be provided.

The access gate may be buried deeper within the trench than the control gate. In other words, a current flow may occur from the second source/drain region through the portion of the nanowire adjacent to the access gate, through the portion of the nanowire adjacent to the control gate, and to the first source/drain region, or vice versa.

The nanowire may be a semiconductor nanowire (such as made from silicon, germanium, etc.), a carbon nanotube (electrically conductive or semiconductive), a silicon nanowire or a group III-group V nanowire such as made of gallium arsenide.

Next, further exemplary embodiments of the memory array will be explained. However, these embodiments also apply to the memory cell and to the method.

The memory array may comprise a plurality of memory cells, particularly thousands or millions or billions or more of memory cells. These may be arranged in a matrix-like manner, wherein each of the individual memory cells can be addressed by bit lines and word lines, as known by the skilled person.

For programming, a memory cell may be selected by activating a specific access transistor, and by applying corresponding voltages to the control gate and to the source/drain connections so as to induce tunnelling or other programming effects which inject charge carriers in the charge carrier structure. After such a programming procedure, the charge carriers may remain permanently or for a long time in the charge carrier structure.

For reading out the stored information, a memory cell may again be selected by applying a readout voltage to the access gate. The current flow along the nanowire may then depend on the conductivity of the channel portion adjacent to the memory transistor, and therefore from the fact whether the charge carrier structure has been provided with charge carriers during a previous programming phase or not. Therefore, a current flowing between the source/drain regions depends on the stored information and is indicative of the stored information.

In order to avoid or suppress artefacts (when programming or reading out the memory cell or in a passive mode of the memory cell) due to leakage or tunnelling effects, electrically insulating regions may be formed between adjacent trenches formed in the same substrate. This may allow to reliably decouple different word lines.

A common control gate may be provided for a sub-group of at least two of the plurality of memory cells. For instance, a single assigned control gate may control a column or row of memory cells. This may allow for a secure readout and an efficient architecture.

The memory array may be a two-dimensional arrangement of the memory cells, but may also be a three-dimensional stack of memory cells. Particularly, the latter measure further increases the storage volume and the integration density.

Next, further exemplary embodiments of the method will be explained. However, these embodiments also apply to the memory cell and to the memory array.

The nanowire may be formed by a growing procedure. For this purpose, a precursor may be provided in the trench so as to define a location at which the growth of the nanowire starts. This is a very simple procedure that allows to accurately define a portion at which a nanowire grows.

Alternatively, the nanowire may be formed by an etching procedure using a wafer (n-type or p-type). In such a scenario, the trench may be filled with material forming the nanowire, and a subsequent etching procedure may then define the lateral extension of the nanowire.

The method may be carried out in CMOS technology. Since the described procedures are compatible with CMOS technology, it may be possible to form a memory purely in semiconductor technology.

In an embodiment of the invention in which a floating gate configuration is implemented, programming a memory cell may be performed by applying a voltage of 12 V to 15 V to the control gate, and by simultaneously grounding the two source/drain regions (i.e. source and drain). Then, charge carriers may be injected into the floating gate by Fowler-Nordheim tunnelling. Since embodiments of the invention significantly improve the coupling efficiency, the programming voltage may be reduced compared to conventional approaches. Reading out a memory cell may be performed by applying a voltage of 1 V to the control gate, by applying a voltage of 0.5 V to the drain and by grounding the source. A voltage of 1 V may be applied to the access gate. Erasing a memory cell may be performed by applying a voltage of -12 V to -15 V to the control gate, and by simultaneously grounding the two source/drain

regions (i.e. source and drain), so that charge carriers may be injected into or removed from the floating gate by Fowler-Nordheim tunnelling. The given voltage values are only examples and may vary over a broad interval. They may depend on dimensions, materials and electronic characteristics of the memory cell such as the threshold voltage of the transistor(s).

For any method step, any conventional procedure as known from semiconductor technology may be implemented. Forming layers or components may include deposition techniques like CVD (chemical vapour deposition), PECVD (plasma enhanced chemical vapour deposition), ALD (atomic layer deposition), or sputtering. Removing layers or components may include etching techniques like wet etching, vapour etching, etc., as well as patterning techniques like optical lithography, UV lithography, electron beam lithography, etc.

Embodiments of the invention are not bound to specific materials, so that many different materials may be used. For conductive structures, it may be possible to use metallization structures, silicide structures or polysilicon structures. For semiconductor regions or components, crystalline silicon may be used. For insulating portions, silicon oxide or silicon nitride may be used.

The structure may be formed on a purely crystalline silicon wafer or on an SOI wafer (Silicon On Insulator).

Any process technologies like CMOS, BIPOLAR, and BICMOS may be implemented.

The aspects defined above and further aspects of the invention are apparent from the examples of embodiment to be described hereinafter and are explained with reference to these examples of embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in more detail hereinafter with reference to examples of embodiment but to which the invention is not limited.

Fig. 1 shows a conventional two-transistor memory cell comprising an access transistor and a floating gate memory transistor.

Fig. 2 shows a conventional two-transistor memory cell comprising an access transistor and an ONO memory transistor.

Fig. 3 shows a cross-sectional view of a memory cell comprising an access

transistor and an ONO memory transistor according to an exemplary embodiment of the invention.

Fig. 4 shows a partial plan view of the memory cell of Fig. 3.

Fig. 5 shows a cross-sectional view of a memory cell comprising an access transistor and a floating gate memory transistor according to an exemplary embodiment of the invention.

Fig. 6 shows a partial plan view of the memory cell of Fig. 5.

Fig. 7 to Fig. 30 show layer sequences (cross-sectional views and partial plan views) obtained during carrying out a method of forming the memory cell of Fig. 3 according to an exemplary embodiment of the invention.

Fig. 7 to Fig. 17, Fig. 31 to Fig. 46 show layer sequences (cross-sectional views and partial plan views) obtained during carrying out a method of forming the memory cell of Fig. 5 according to an exemplary embodiment of the invention.

Fig. 47 to Fig. 58 show layer sequences (cross-sectional views and partial plan views) obtained during carrying out another method of forming a nanowire according to an exemplary embodiment of the invention.

DESCRIPTION OF EMBODIMENTS

The illustration in the drawing is schematical. In different drawings, similar or identical elements are provided with the same reference signs.

In the following, referring to Fig. 3, a memory cell 300 according to an exemplary embodiment of the invention will be explained.

The memory cell 300 comprises a substrate 301 that is an n-type silicon wafer. An oblong nanowire 302 extends along a vertical trench formed in the substrate 301. Furthermore, a control gate 303 is provided which surrounds the nanowire 302 in a coaxial manner along a portion of the vertical extension of the nanowire 302. A charge storage structure 304 is formed as an ONO layer sequence and is arranged between the control gate 303 and the nanowire 302. Actually, the charge will be stored in the nitride layer of the ONO layer sequence 304.

The memory cell 300 further comprises a first source/drain region 305 (which may particularly act as a drain) and is formed by an n^+-doped silicon material. The first source/drain region 305 is coupled to a substrate external end portion 330 of the nanowire

Sandisk Technologies, Inc. - Ex. 1040, Page 000235

302. The first source/drain region 305 may be a doped portion of the nanowire 302 or may be configured as a separate component. A buried second source/drain region 306 (which may particularly act as a source) is provided in the substrate 301 and is another n^+-doped portion. The second source/drain region 306 is coupled to a substrate internal end portion 331 of the nanowire 302. The second source/drain region 306 may be a portion of the substrate 301 or may be configured as a separate component. A contact structure 307 of an electrically conductive material is provided and is electrically coupled to the first source/drain region 305. Beyond this, an electrically insulating spacer structure 308 surrounds the first source/drain region 305 and is adapted for electrically decoupling the first source/drain region 305 from the control gate 303.

As can be taken from Fig. 3, the contact structure 307 is broader (in a horizontal direction of Fig. 3) than the first source/drain region 305. The control gate 303 circumferentially surrounds the nanowire 302 entirely, i.e. along its entire diameter. A diameter of the nanowire along a horizontal direction of Fig. 3 is approximately 10 nm.

Furthermore, an access gate 309 is provided below the control gate and is therefore buried deeper within the trench than the control gate 303. The access gate 309 surrounds the nanowire along its entire circumference and along a part of its vertical extension. Depending on a voltage to be externally applied to the access gate 309, the value of the electrical conductivity of a controllable portion 310 of the nanowire 302 may be adjusted so that the access gate 309 serves as an access transistor with the nanowire 302 acting as a channel region.

The memory cell 300 further comprises a lateral silicon oxide (SiO_2) structure 311. On a surface of the structure 300, an electrically insulating layer 312 is provided, which may also be made from silicon oxide (SiO_2). A silicon nitride layer 313 separates the electrically insulating layers 311 and 312. Furthermore, an electrically insulating spacer structure 314 is provided. With regard to its environment, the access gate 309 is electrically insulated by an encapsulation structure 315.

In a similar manner, the control gate 303 is partially encapsulated by the ONO layer sequence 304, that is to say by a sequence comprising a first silicon oxide layer, a silicon nitride layer and a second silicon oxide layer.

Fig. 3 shows a cross-section of the memory cell 300 with a two-transistor configuration, namely the described access transistor and the memory transistor, wherein the memory transistor is implemented in a SONOS design. Possible misalignments of the contact

Sandisk Technologies, Inc. - Ex. 1040, Page 000236

307 with respect to the source/drain region 305 are indicated schematically in Fig. 3.

The intrinsically doped silicon nanowire 302 with an approximate width/diameter of 10 nm or tens of nanometers forms the channel (n-channel) of the access transistor and of the memory transistor and connects drain region 305 and source region 306 which are n-type doped as well but to a higher extent compared to the nanowire 302. The control gate 303/ONO stack 304 (part of the memory transistor) and the access gate 309/gate oxide stack 310 (part of the access transistor) are all wrapped around the channel 302. Since the gate stack 304 and the access gate/gate oxide 310 are all around the channel 302, the controllability of the conductivity of the channel 302 is greatly enhanced. This may lead to a large density drive current and low-density leakage. In the memory cell design, it is taken into account that the contact 307 to the drain 305 may be much larger than the nanowire 302 and that it can also have some misalignment (non-self-aligned contact), this is why nitride spacers 308 may be formed at the drain side 305.

Fig. 4 shows a top view of the cross-section of Fig. 3 where the contact 307 and the silicon oxide passivation layer 312 are not present to make easier the visualization of all the different layers being part of the gate stack around the channel 302.

More particularly, the plan view of Fig. 4 shows a first word line 400 and a second word line 401. However, any desired number of word lines is possible.

An enlarged view 410 is indicated in the overview of Fig. 4 as well. Furthermore, the top oxide, nitride, bottom oxide layer sequence 304, the nanowire 302, the control gate 303 and a nitride spacer 308 are shown as well. Thus, Fig. 4 shows the top view of Fig. 3 without the contact 307 to the drain 305 and the silicon oxide passivation layer 312. The insert 410 shows the different layers within the gate stack all around the channel (nanowire) 302.

In the following, referring to Fig. 5, a memory cell 500 according to another exemplary embodiment of the invention will be explained.

The embodiment of Fig. 5 differs from the embodiment of Fig. 3 particularly in that the ONO layer 304 as a charge storage structure is substituted by a floating gate 501, that is to say by an electrically conductive structure which is surrounded by an electrically insulating encapsulation 502. Therefore, charge carriers (such as electrons or holes) stored in the electrically conductive floating gate 501 which may be made of a polysilicon material, may be kept for a long duration in the floating gate 501 to store information. The conductivity of the channel region 302 adjacent to the storage region 304 depends on the type and amount of

Sandisk Technologies, Inc. - Ex. 1040, Page 000237

charge carriers located within the floating gate 501.

Therefore, Fig. 5 shows a two-transistor floating gate memory cell configuration 500. In this embodiment, the memory transistor is implemented using the floating gate 501. The principle is similar as for the SONOS memory cell 300. However, in the embodiment of Fig. 5, the control gate 303 - IPD - floating gate 501 - tunnel oxide 502 stack of the memory transistor and the access gate 309 - gate oxide 502 stack of the access transistor are all wrapped around the nanowire 302 serving as a cylindrical channel region with an essentially circular cross-section.

Fig. 6 shows a top view 600 of the memory cell 500 of Fig. 5 without the contact 307 and the silicon passivation layer 312. The insert 610 shows the different layers within the gate stack all around the channel 302 (nanowire). As indicated in the insert 610, the floating gate 501, the tunnel oxide 502 and the nanowire 302 are (partially) covered by the nitride spacer 308.

In the following, referring to Fig. 7 to Fig. 58, embodiments will be explained as to how to build memory cells according to the invention in detail with the whole process integration scheme and some possible variations (such as growing nanowires versus silicon etching of nanowires, one transistor versus two transistor configurations, and floating gate versus SONOS configurations). Silicon oxide has been considered as the dielectric material in these embodiments, although other materials different from silicon oxide (for instance high-k materials or silicon nitride) can also be used for dielectric components. In each of Fig. 7 to Fig. 58, a top view is shown on the left-hand side and a cross-sectional view is shown on the right-hand side.

Fig. 7 shows a layer sequence 700 that consists of an n-type silicon wafer 301. Such an n-type wafer 301 may be used to make a contact to the lower source of a nanowire transistor configuration to be manufactured. A p-well type as a substrate (planar) is not needed in this embodiment, but may be used in other embodiments of the invention.

Fig. 8 shows a layer sequence 800 obtained after having deposited a layer of silicon oxide (SiO_2) 311 which may later serve to isolate the word lines. Thus, an electrically insulating layer 311 is formed on the substrate 301.

Fig. 9 shows a layer sequence 900 obtained after deposition of a layer of silicon nitride 901 on the silicon oxide layer 311.

Fig. 10 shows a layer sequence 1000 that is obtained after depositing and etching an auxiliary layer 1001 (such as a photoresist) for patterning the word lines.

Sandisk Technologies, Inc. - Ex. 1040, Page 000238

Fig. 11 shows a layer sequence 1100 that is obtained after removing an exposed portion of the layers 901, 311 using the patterned auxiliary layer 1001 as a mask. After having etched a trench 1101 in the layers 901, 311, an exposed portion of the substrate 301 is doped by an n^+-implantation to thereby generate an n^+-doped source region 306. Arrows 1102 indicate the implantation schematically.

Fig. 12 shows a layer sequence 1200 obtained after deposition of a precursor structure 1201 which will be later used to grow a nanowire. Gold may be used to form the precursor structure 1201. Less contaminate materials such as a titanium catalyst may be used as well. The precursor 1201 is deposited onto a specific position within the trench 1101.

Fig. 13 shows a layer sequence 1300 obtained after growing a nanowire 302 on the precursor 1201 which will later form the channel of the access and memory transistor of the memory cell to be manufactured. Optionally, the precursor 1201 is removed, and the auxiliary layer 1001 may be removed as well.

The layer sequence 1400 shown in Fig. 14 is obtained by forming (for instance by thermal oxidation) an electrically insulating layer 1401, for instance of silicon oxide, on the surface of the silicon nanowire 302 and of the source/drain region 306 within the trench 1101. As can be taken from Fig. 14, the grown silicon oxide material 1401 builds a gate oxide 1403 of the access transistor. In a surface region where a higher concentration of a dopant is present, namely on the surface of the source/drain region 306, the oxidation will result in a thicker silicon oxide layer 1402 as compared to a region at the surface of the nanowire 302 which is intrinsically doped. This effect is favourable for providing isolation between the polysilicon (deposited later on) and the source/drain region 306.

The layer sequence 1500 shown in Fig. 15 is obtained by depositing a polysilicon layer 1501 on the layer sequence 1400. The material of the polysilicon layer 1501 may later form the basis for an access gate.

In order to obtain the layer sequence 1600 shown in Fig. 16, the polysilicon structure 1501 is partially removed by CMP ("chemical mechanical polishing").

To obtain the layer sequence 1700 shown in Fig. 17, the polysilicon structure 1501 is then etched selectively to oxide and nitride. The remaining polysilicon will later form the basis for the gate region of the access transistor, denoted with reference numeral 309. The polysilicon material is in situ doped.

In order to obtain a layer sequence 1800 shown in Fig. 18, the exposed portion of the silicon oxide structure 1401 is etched, so that it is selectively removed from the

Sandisk Technologies, Inc. - Ex. 1040, Page 000239

nanowire 302, and indentations or recesses 1801 may be formed as well as a consequence of the etching procedure.

In order to obtain a layer sequence 1900 shown in Fig. 19, a bottom oxide 1901 of an ONO layer (in a configuration of a SONOS memory transistor) is grown, for instance by thermal oxidation. Again, in the polysilicon region 309, the formed oxide layer 1901 is thicker (see portion 1902) than in the nanowire 302 region providing an insulation (see portion 1903). Particularly, the portion 1902 serves as an electrically insulating portion, and the portion 1903 serves as a bottom oxide of the ONO stack (memory transistor in SONOS design).

In order to obtain a layer sequence 2000 as shown in Fig. 20, a nitride layer 2001 of the ONO stack to be formed is deposited. The deposition procedure may be performed in a manner that the thickness of the layer 2001 will be essentially uniform. Reference numeral 2002 indicates a portion of the nitride layer 2001 of the ONO stack (control gate in SONOS configuration), i.e. a portion in which charge may be stored for encoding information.

In order to obtain a layer sequence 2100 as shown in Fig. 21, a top silicon oxide layer 2101 is deposited, again essentially uniformly. Therefore, as indicated with reference numeral 2102, an ONO (oxide/nitride/oxide) stack is formed.

In order to obtain a layer sequence 2200 shown in Fig. 22, a polysilicon layer 2201 is deposited, forming a basis for a control gate polysilicon structure.

In order to obtain the layer sequence 2300 shown in Fig. 23, the further polysilicon layer 2201 is planarized by CMP ("chemical mechanical polishing").

The layer sequence 2400 shown in Fig. 24 is obtained by selectively etching the polysilicon structure 2201 relative to silicon oxide, thereby constituting the polysilicon control gate 303 of the memory transistor. The polysilicon gate 303 is in situ doped.

In order to obtain the layer sequence 2500 shown in Fig. 25, the exposed portions of the ONO layer 1901, 2001, 2101 are removed. It is not detrimental if the remained ONO layer 1901, 2001, 2101 is not aligned to the control gate 303 polysilicon material, whenever the ONO layer 1901, 2001, 2101 fully covers the region below the control gate 309. It should be prevented that the ONO layer 1901, 2001, 2101 is overetched below the control gate polysilicon material 303. As can be taken from Fig. 25, the described processing manufactures the memory transistor (SONOS) and the access transistor. The memory portion of the ONO layer 1901, 2001, 2101 which actually stores the charge is shown as a portion

Sandisk Technologies, Inc. - Ex. 1040, Page 000240

illustrated as a rectangular 304.

To obtain the layer sequence 2600 of Fig. 26, nitride spacers 308 are formed to make a contact to the drain (to be formed subsequently feasible). Nitride spacers 314 may be formed as well.

In order to obtain the layer sequence 2700 shown in Fig. 27, a shallow n^+-implantation procedure is performed in order to form the drain region (denoted with reference numeral 305, see Fig. 3 or Fig. 28). This is indicated by arrows 2701 in Fig. 27.

Consequently, an n^+-drain 305 is formed, as indicated in the layer sequence 2800 as shown in Fig. 28.

In order to obtain the layer sequence 2900 shown in Fig. 29, a silicon oxide layer 312 is deposited on the entire surface of the layer sequence 2800.

In order to obtain the layer sequence 3000 shown in Fig. 30, the electrically insulating layer 312 is patterned using a lithography procedure and an etching procedure, thereby forming a through hole in the layer 312 to thereby expose a surface of the drain region 305. Then, electrically conductive material is filled in the hole to form an electrically conductive contact 307.

In other words, manufacture of a contact to the drain 305 stopping at the nitride structure 308 is performed. The contact 307 may be wider than the nanowire 302, and possible misalignments (non-self-aligned contact) may be taken into account and are not harmful thanks to the nitride spacers 308.

The configuration shown in Fig. 30 essentially equals to the configuration shown in Fig. 3.

As an alternative to such an implementation of the memory transistor using a SONOS architecture, it is also possible to manufacture the memory transistor including a floating gate.

For this purpose, the manufacturing procedures described above referring to Fig. 7 to Fig. 17 can be performed and can be combined with the processing procedures that will be explained below referring to Fig. 31 to Fig. 46. As a result, a memory cell similar to that shown in Fig. 5 is obtainable.

Referring to Fig. 31, after forming the access gate 309 (common to SONOS), a tunnel oxide layer 3101 is grown, providing isolation at the polygate side 309.

The layer sequence 3200 shown in Fig. 32 is obtained by depositing polysilicon material for the floating gate, thereby forming a polysilicon layer 3201.

Sandisk Technologies, Inc. - Ex. 1040, Page 000241

The layer sequence 3300 shown in Fig. 33 is obtained by planarizing the polysilicon structure 3201 by CMP ("chemical mechanical polishing").

To obtain a layer sequence 3400 as shown in Fig. 34, the polysilicon structure 3201 is further etched and therefore selectively removed relative to silicon oxide to build the floating gate.

In order to obtain the layer sequence 3500 shown in Fig. 35, a top portion of the electrically insulating structure 3101 is removed by wet etching.

In order to obtain the layer sequence 3600 shown in Fig. 36, lateral silicon nitride spacers 308, 314 are formed to cover lateral walls of the first source/drain region to be able to contact without harming the device.

In order to obtain the layer sequence 3700 of Fig. 37, a polysilicon overetch procedure is performed, removing the non-exposed portions of the polysilicon material 3201 which is not covered by the nitride spacers 308, 314.

A layer sequence 3800 shown in Fig. 38 is obtained by depositing silicon oxide (SiO_2) as interpolydielectric material, thereby forming a layer 3801 covering the layer sequence 3700.

In order to obtain the layer sequence 3900 shown in Fig. 39, polysilicon material 3901 is deposited on the surface of the layer sequence 3800, thereby providing material for forming the control gate.

In order to obtain a layer sequence 4000 shown in Fig. 40, the polysilicon structure 3901 is planarized by performing a CMP procedure ("chemical mechanical polishing").

In order to obtain the layer sequence 4100 shown in Fig. 41, a control gate 303 are formed by selectively etching polysilicon material of the structure 3901 relative to silicon oxide.

By etching the silicon oxide material on the surface of the layer sequence 4100, the layer sequence 4200 shown in Fig. 42 is obtained.

Subsequently, as shown in a layer sequence 4300 in Fig. 43, an n^+-shallow implantation procedure is performed to form the drain 305 in an upper portion of the nanowire 302 (see Fig. 44). Arrows 4301 indicate this doping procedure schematically.

Consequently, the layer sequence 4400 shown in Fig. 44 shows the second source/drain region 305.

The layer sequence 4500 shown in Fig. 45 is obtained by depositing silicon

oxide material on the surface of the layer sequence 4400, thereby forming an electrically insulating layer 312.

Then, as can be taken from the layer sequence 4600 in Fig. 46, a contact to the drain 305 is provided by item 307. Again, possible misalignments of the contact 307, or the fact that the contact 307 for contacting the drain 305 is larger than the nanowire 302, is not harmful thanks to the nitride spacers 308.

The layer sequence 4600 essentially corresponds to the memory cell 500 shown in Fig. 5.

The above-described Fig. 7 to Fig. 13 explain a procedure of growing a nanowire 302.

Alternatively, the nanowire can also be manufactured by etching a silicon structure, which will be explained in the following.

Therefore, after having manufactured the layer sequence in a manner as shown in Fig. 47 to Fig. 58, the procedures of Fig. 14 to Fig. 46 can be performed in a similar manner.

Fig. 47 shows a view 4700 of a wafer 301.

In order to obtain the layer sequence 4800 shown in Fig. 48, a nitride layer 901 is deposited on the wafer 301 to create a stopping layer for a later CMP ("chemical mechanical polishing") procedure.

As indicated in Fig. 49 showing a layer sequence 4900, an active mask 4901 is applied as a template for forming trenches (such as STI trenches, "shallow trench isolation").

In order to obtain the layer sequence 5000 shown in Fig. 50, the entire wafer 301 is etched, thereby forming STI trenches 5001. The active mask 4901 may be removed.

As shown in Fig. 51 illustrating a layer sequence 5100, the trenches 5001 are filled with silicon oxide material, and an additional amount of silicon oxide material is deposited over this layer structure. Consequently, a silicon oxide layer 5101 is formed.

As shown in Fig. 52 illustrating a layer sequence 5200, silicon oxide material of layer 5101 is removed by CMP ("Chemical Mechanical Polishing"), wherein the silicon nitride material 901 is used as a stopping layer.

In order to obtain the layer sequence 5300 shown in Fig. 53, silicon nitride material 5301 is deposited on top of the layer sequence 5200.

Fig. 54 shows a layer sequence 5400 in which a patterned mask 5401 is shown. The inverse 5401 to the active mask 4901 (instead of light field dark field) is used to remove

the silicon nitride material of top of the silicon wafer 301.

Etching the layers 5301 and 901 results in the layer sequence 5500 shown in Fig. 55.

The nanowire 302 is then defined by etching silicon material of the substrate 301.

The result of such an etching procedure is shown as the layer sequence 5600 in Fig. 56.

Fig. 57 shows a layer sequence 5700 and arrows 5701 indicating an n^+-implantation to define the source and the drain. With a 0° tilt angle of the implantation, it is possible to avoid the doping of the nanowire 302.

A layer sequence 5800 illustrated in Fig. 58 shows the result with the two source/drain regions 305 and 306.

Starting with the layer sequence 5800, it is possible to continue with Fig. 14.

Finally, it should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be capable of designing many alternative embodiments without departing from the scope of the invention as defined by the appended claims. In the claims, any reference signs placed in parentheses shall not be construed as limiting the claims. The word "comprising" and "comprises", and the like, does not exclude the presence of elements or steps other than those listed in any claim or the specification as a whole. The singular reference of an element does not exclude the plural reference of such elements and vice-versa. In a device claim enumerating several means, several of these means may be embodied by one and the same item of software or hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. A memory cell (300, 500), the memory cell (300, 500) comprising
a substrate (301);
a nanowire (302) extending along a vertical trench formed in the substrate (301);
a control gate (303) surrounding at least a part of the nanowire (302);
a charge storage structure (320, 501) arranged between the control gate (303) and the nanowire (302).

2. The memory cell (300, 500) according to claim 1, comprising a first source/drain region (305) coupled to a substrate external end portion (330) of the nanowire (302) and comprising a second source/drain region (306) coupled to a substrate internal end portion (331) of the nanowire (302).

3. The memory cell (300, 500) according to claim 2, comprising a contact structure (307) coupled to the first source/drain region (305).

4. The memory cell (300, 500) according to claim 2, comprising an electrically insulating spacer structure (308) surrounding the first source/drain region (305) for electrically decoupling the first source/drain region (305) from the control gate (303).

5. The memory cell (300, 500) according to claim 3, wherein the contact structure (307) has a larger dimension than the first source/drain region (305) in a direction being perpendicular to the vertical extension of the trench.

6. The memory cell (300, 500) according to claim 1, wherein the charge storage structure comprises one of the group consisting of a floating gate (501), a silicon oxide-silicon nitride-silicon oxide layer sequence (320), a silicon nitride structure, and a nano-crystal dot structure.

Sandisk Technologies, Inc. - Ex. 1040, Page 000245

7. The memory cell (300, 500) according to claim 1, wherein the control gate (303) surrounds the nanowire (302) along the entire circumference of the nanowire (302).

8. The memory cell (300, 500) according to claim 1, wherein the nanowire (302) has a diameter of less than 100 nm, particularly of less than 50 nm, more particularly of less than 20 nm, in a direction perpendicular to the vertical extension of the trench.

9. The memory cell (300, 500) according to claim 1, comprising an access gate (309) surrounding at least a part of the nanowire (302), particularly surrounding the nanowire (302) along the entire circumference of the nanowire (302).

10. The memory cell (300, 500) according to claim 9, wherein the access gate (309) is arranged deeper within the trench than the control gate (303).

11. The memory cell (300, 500) according to claim 1, wherein the nanowire (302) comprises one of the group consisting of a semiconductor nanowire, a carbon nanotube, a silicon nanowire, and a group III-group V nanowire.

12. The memory cell (300, 500) according to claim 1, adapted as a flash memory cell (300, 500).

13. The memory cell (300, 500) according to claim 1, adapted as a multi-bit memory cell (300, 500).

14. A memory array (400, 600), the memory array (400, 600) comprising a plurality of memory cells (300, 500) according to claim 1 formed in the substrate (301).

15. The memory array (400, 600) according to claim 14, comprising electrically insulating regions (311) between adjacent trenches.

16. The memory array (400, 600) according to claim 14, wherein a common control gate (303) is provided in common for a sub-group of at least two of the plurality of memory cells (300, 500).

17. A method of manufacturing a memory cell (300, 500), the method comprising
forming a vertical trench in a substrate (301);
forming a nanowire (302) extending along the vertical trench;
forming a control gate (303) surrounding at least a part of the nanowire (302);
arranging a charge storage structure (320, 501) between the control gate (303) and the nanowire (302).

18. The method according to claim 17, wherein the nanowire (302) is formed by one of the group consisting of a growing procedure and an etching procedure.

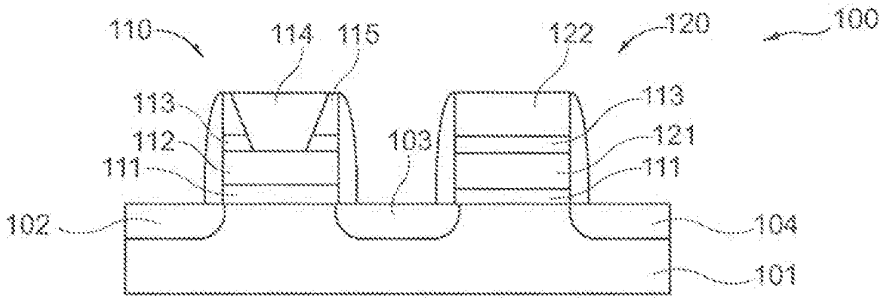


FIG. 1

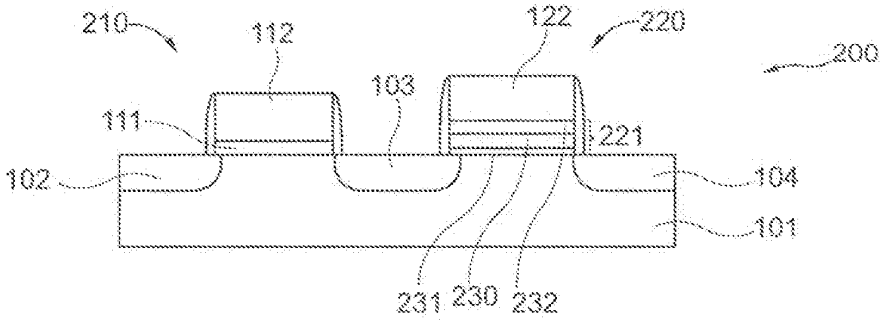


FIG. 2

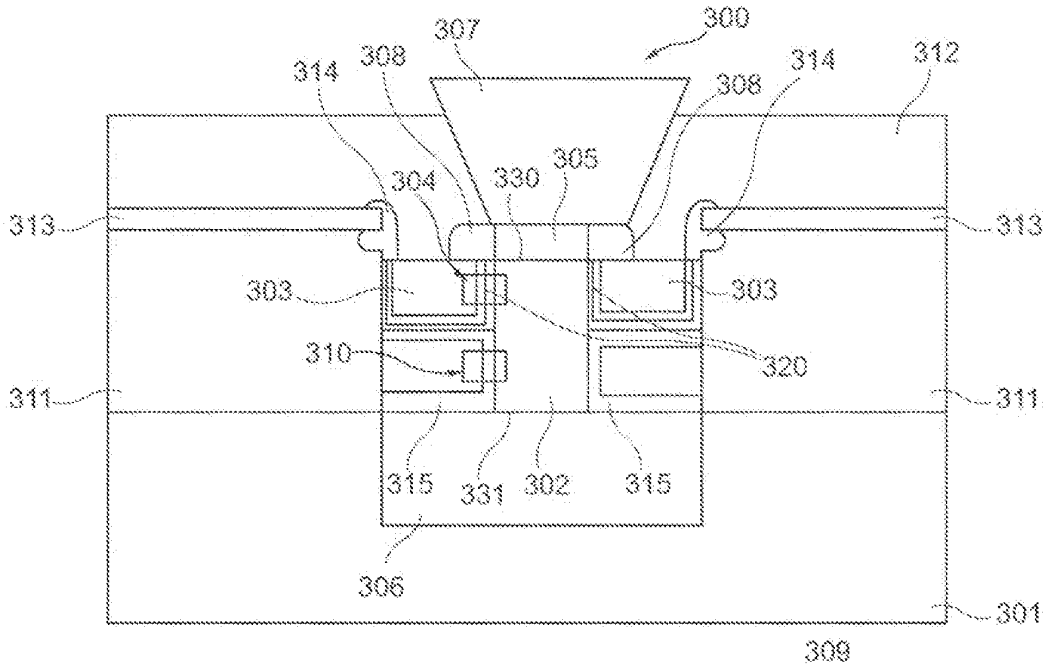


FIG. 3

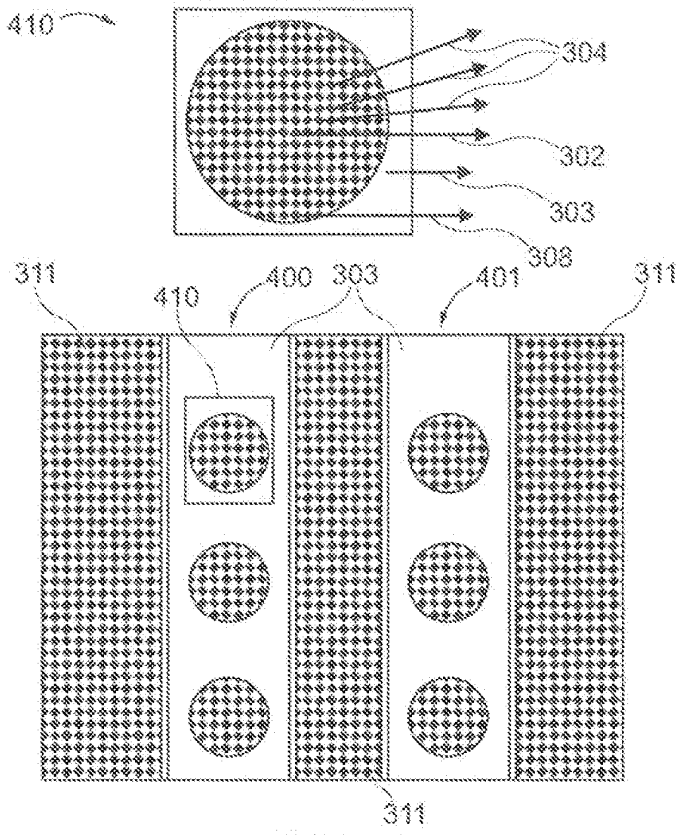

410
304
302
303
308
311
410
400
303
401
311
311

FIG. 4

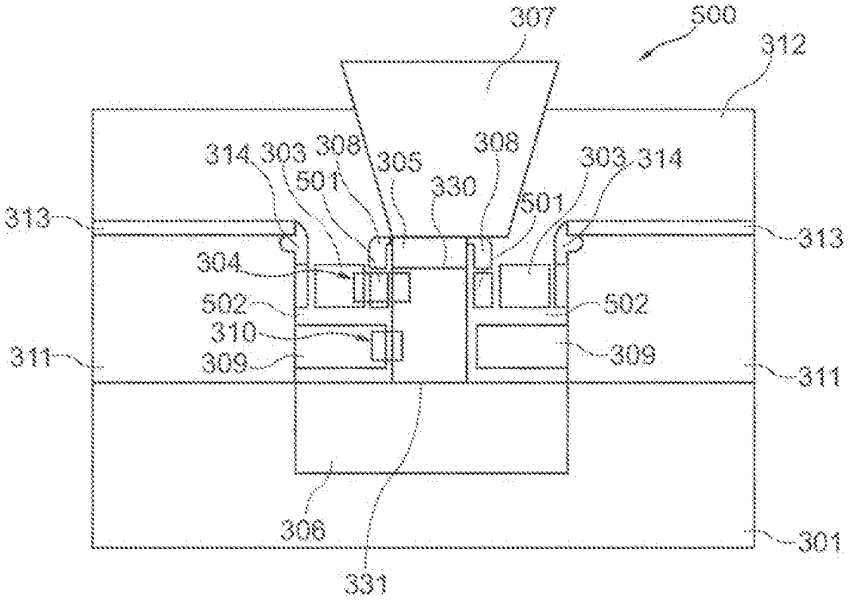

307
500
312
314
303
308
501
305
330
308
303
314
501
313
313
304
502
502
310
309
311
309
311
306
301
331

FIG. 5

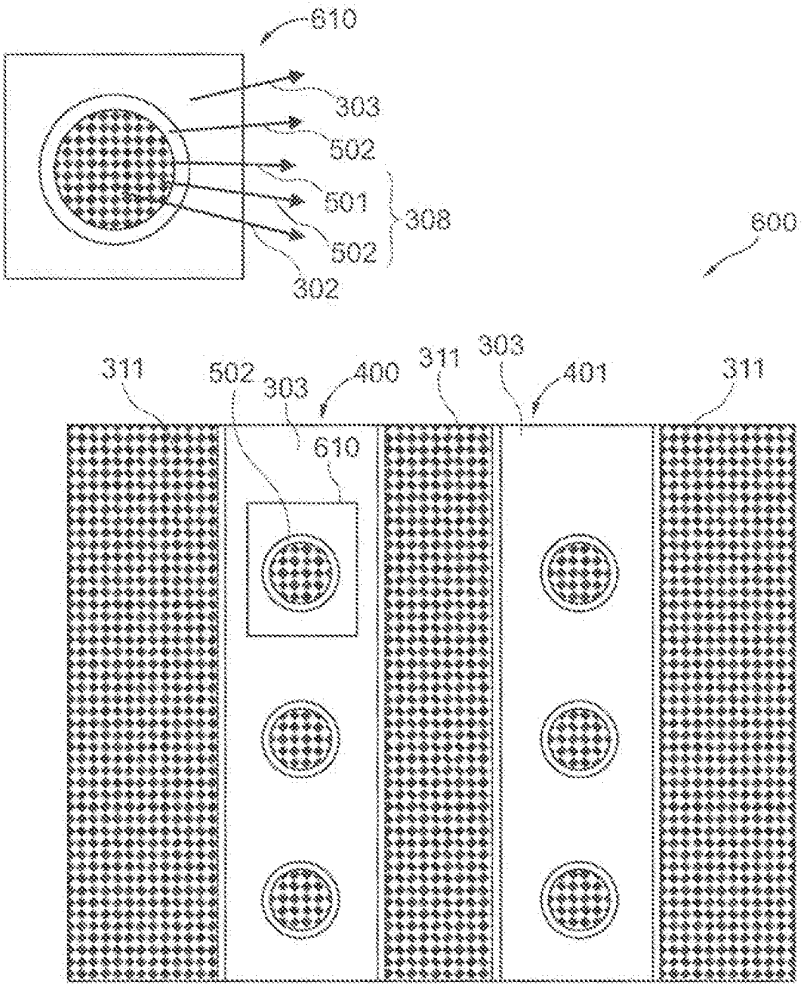

610
303
502
501
308
502
302
600
311
502
303
400
311
303
401
311
610

FIG. 6

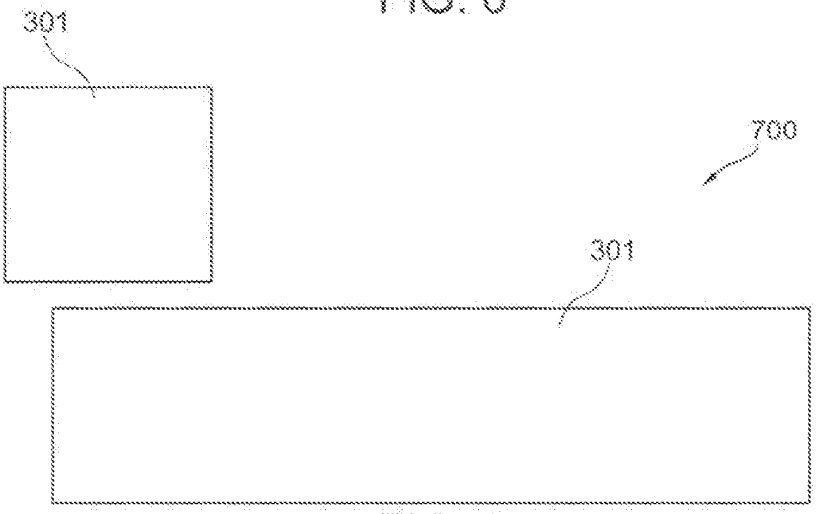

301
700
301

FIG. 7

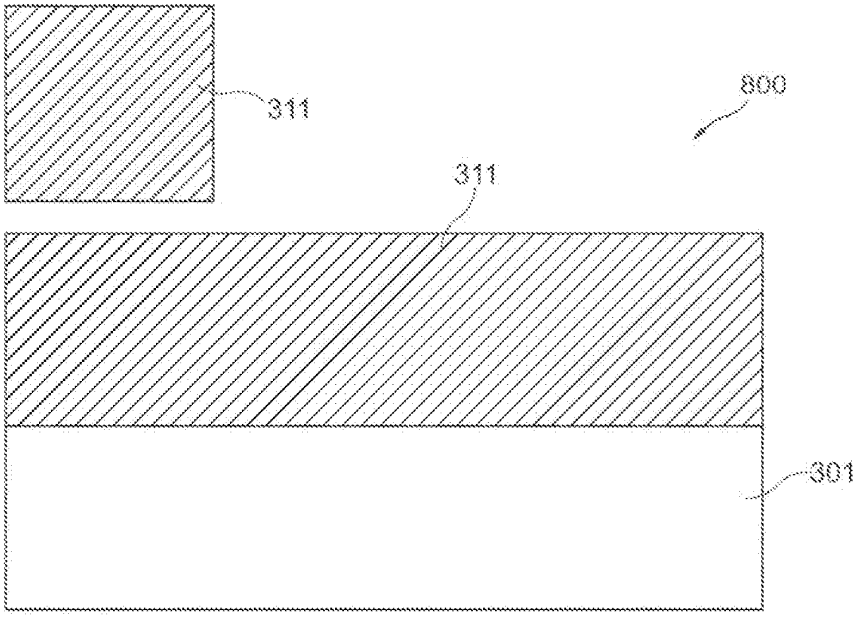


FIG. 8

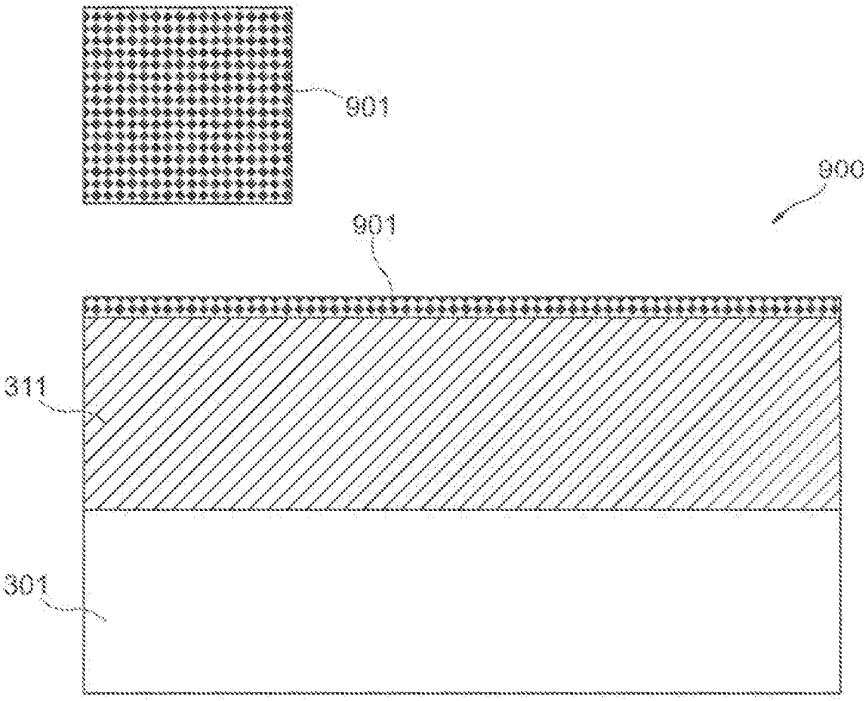


FIG. 9

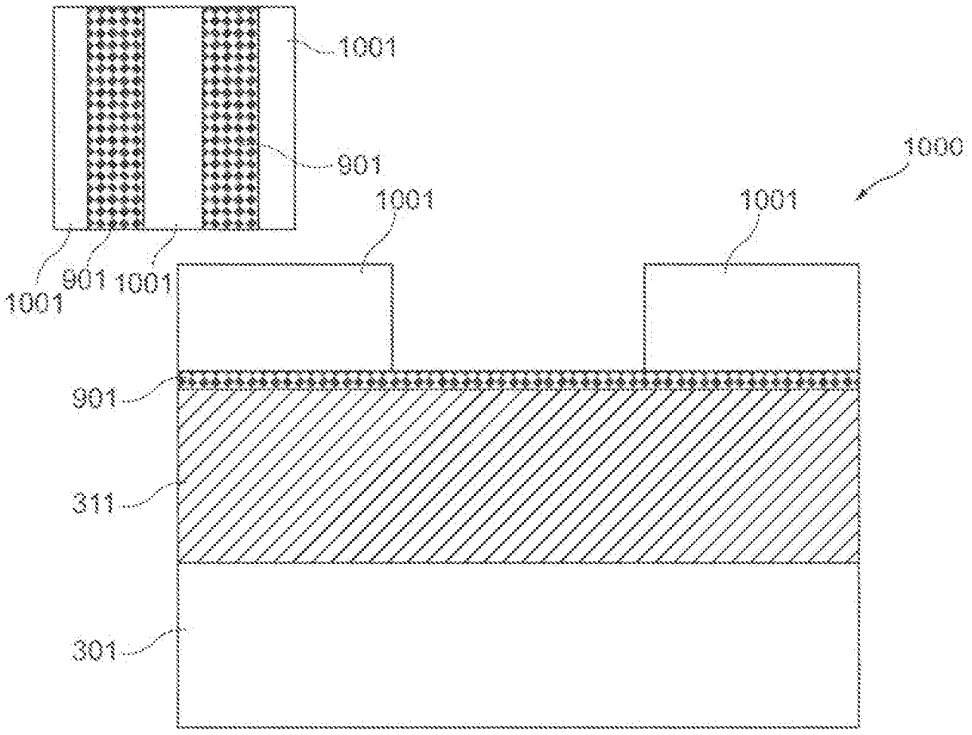

1001
901
1000
1001
1001
1001
901
1001
901
311
301

FIG. 10

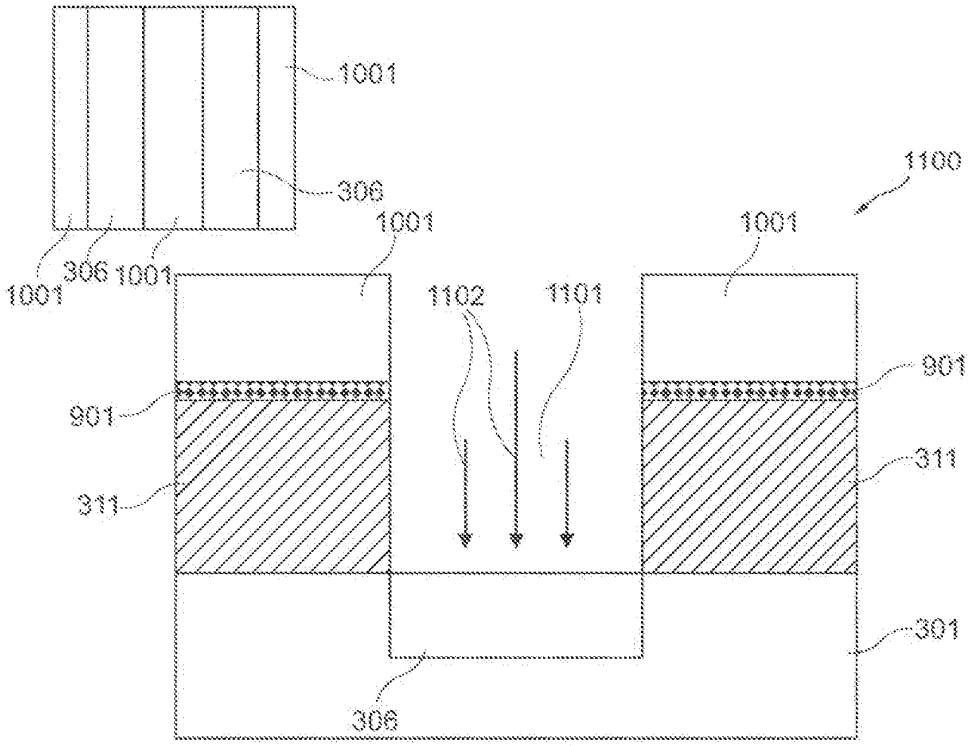

1001
1100
306
1001
1001
1001
306
1001
1102
1101
901
901
311
311
301
306

FIG. 11

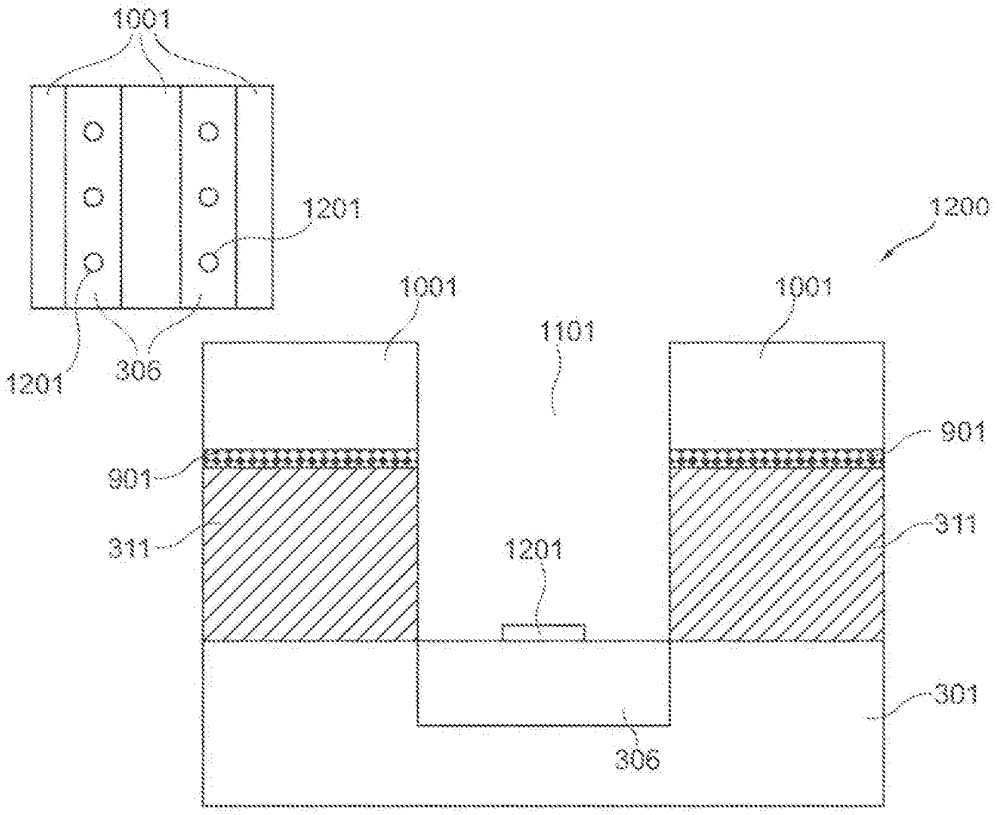

1001
1201
1200
1001
1001
1101
1201
306
901
901
311
311
1201
301
306

FIG. 12

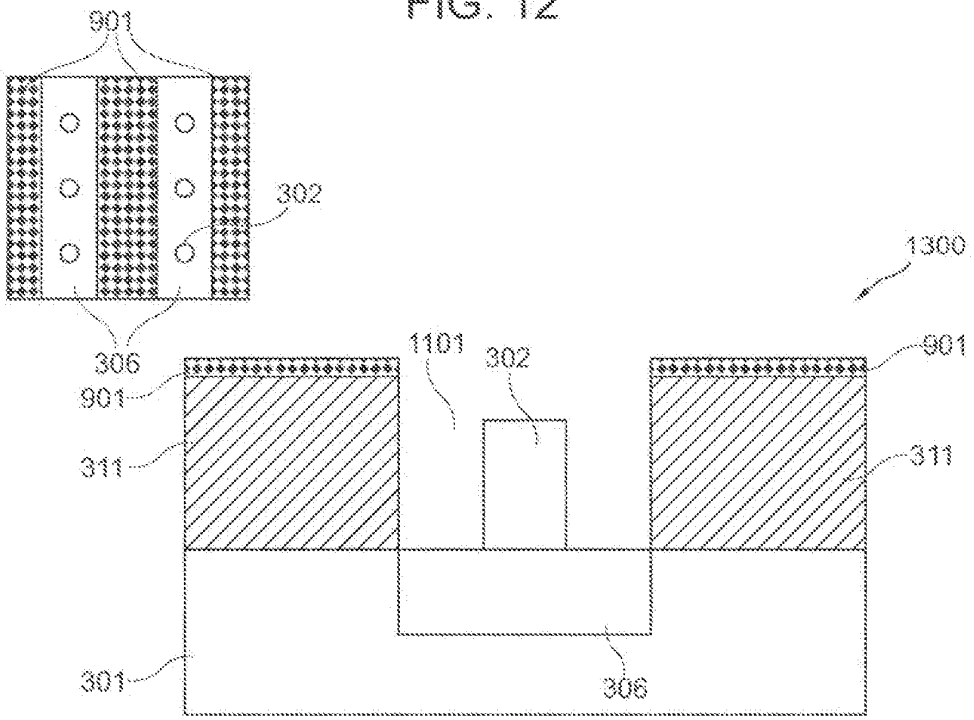

901
302
1300
306
1101
302
901
901
311
311
301
306

FIG. 13

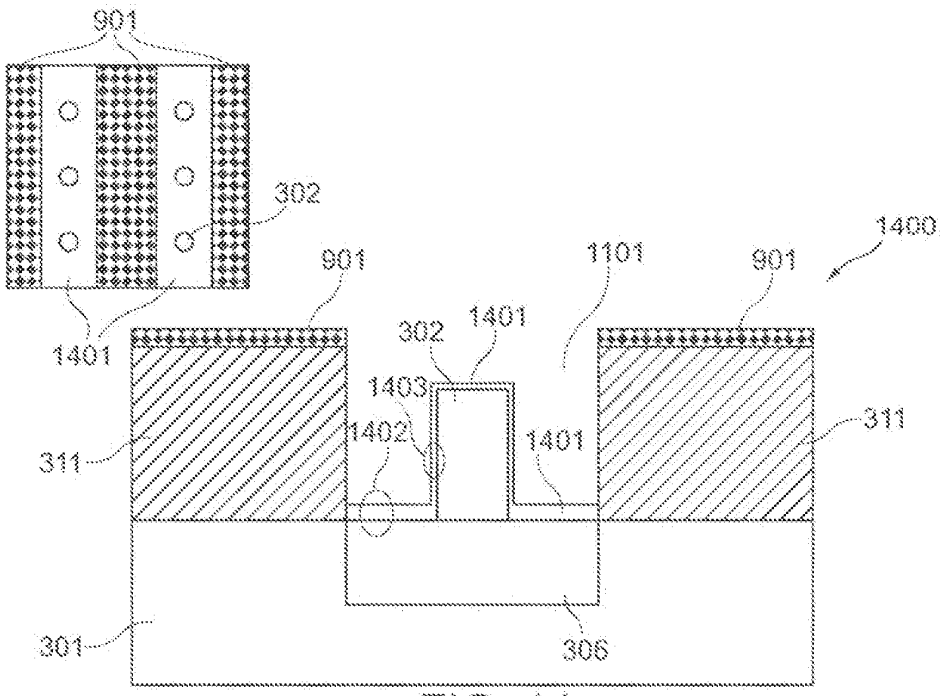

901
302
1400
901
1101
901
1401
302
1401
1403
1402
1401
311
311
301
306

FIG. 14

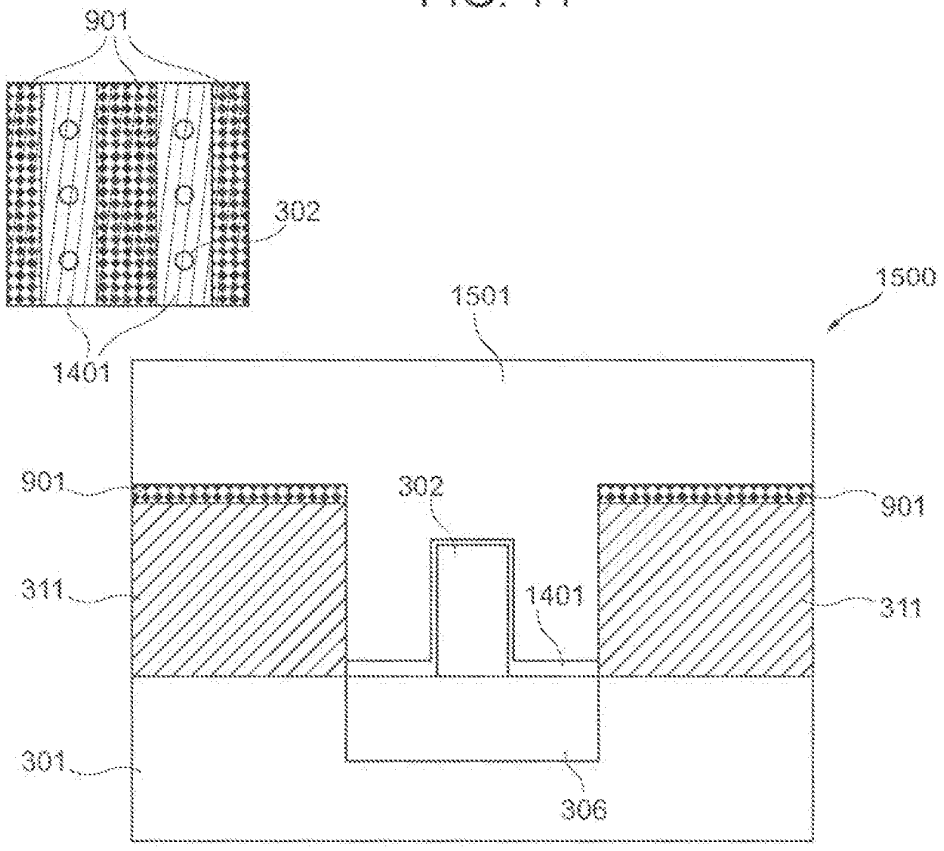

901
302
1500
1501
1401
901
302
901
311
1401
311
301
306

FIG. 15

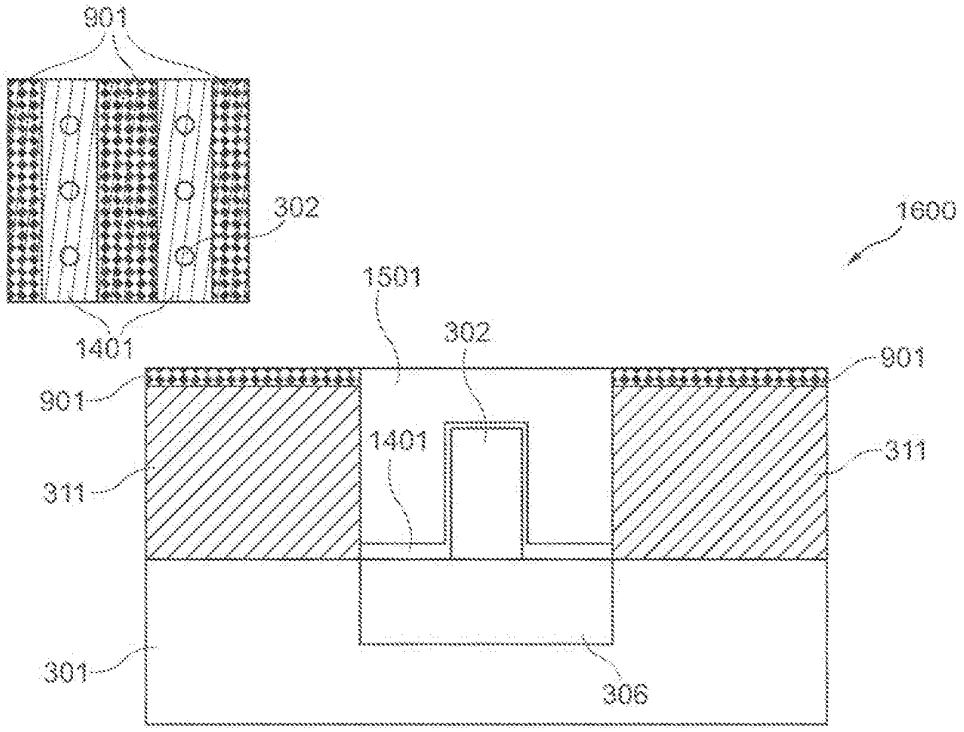

901
302
1600
1501
1401
302
901
901
1401
311
311
301
306

FIG. 16

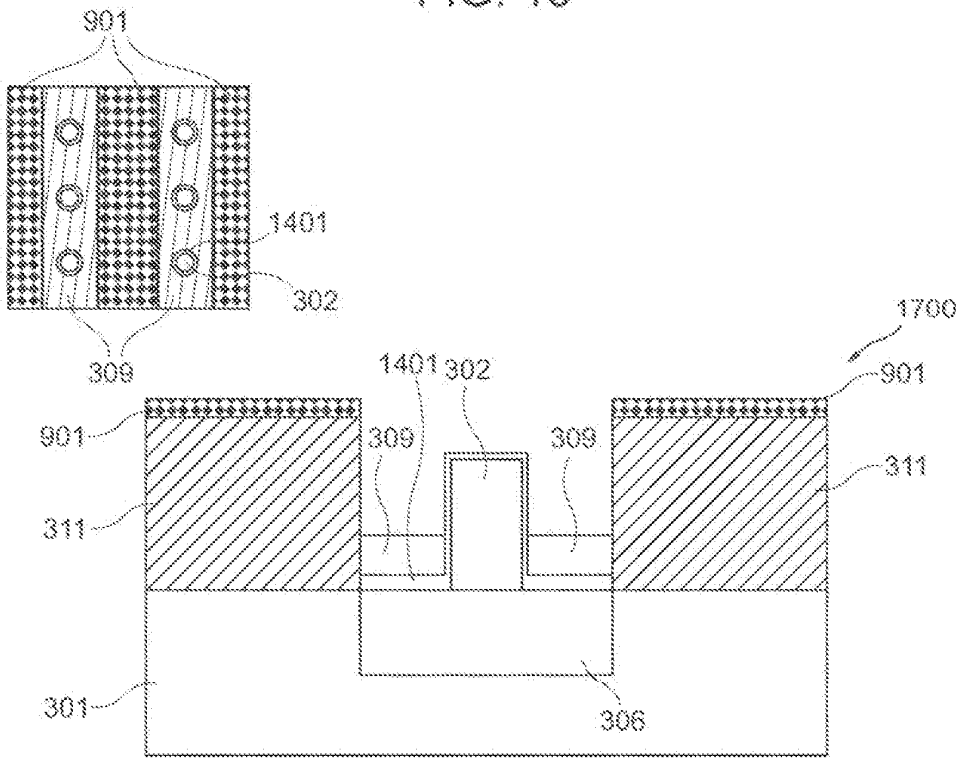

901
1401
302
1700
309
1401
302
901
901
309
309
311
311
301
306

FIG. 17

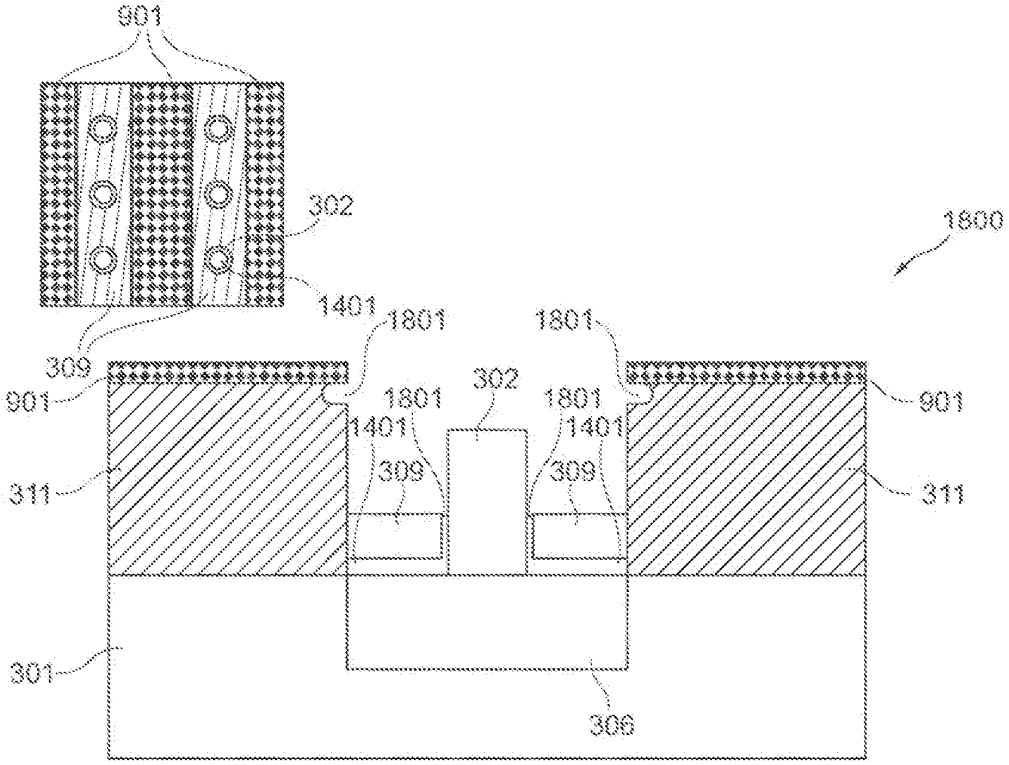

901
302
1800
1401
1801
1801
309
901
1801
302
1801
901
1401
1401
309
309
311
311
301
306

FIG. 18

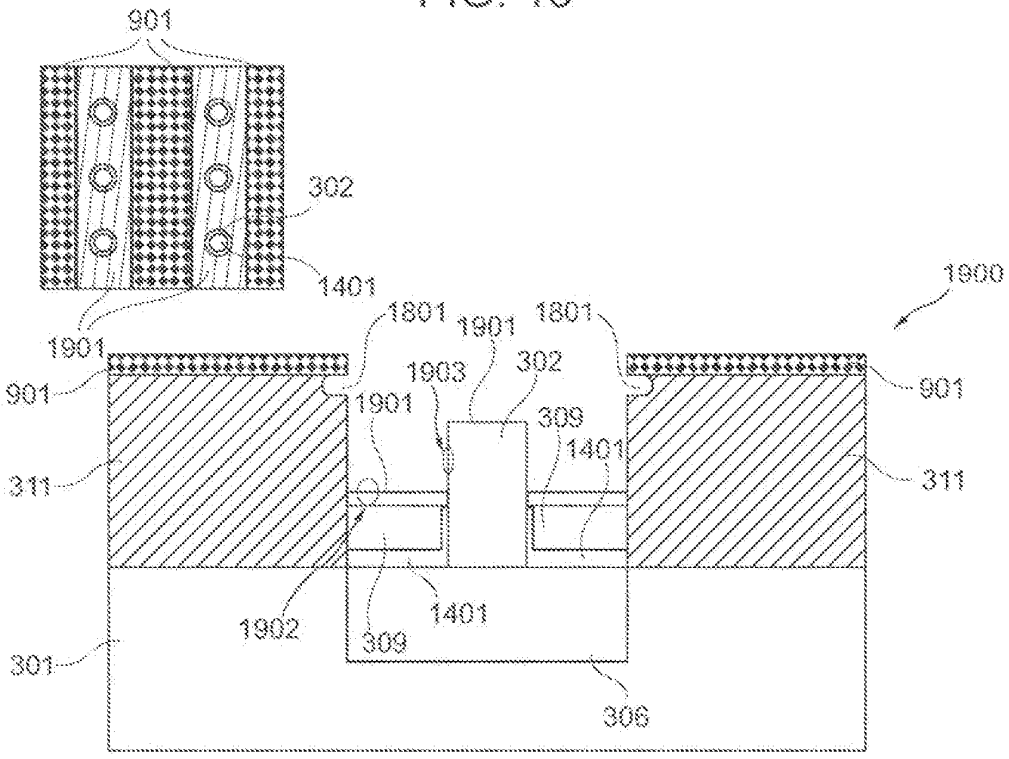

901
302
1900
1401
1801
1901
1801
1901
1903
302
901
901
1901
309
1401
311
311
1902
1401
309
301
306

FIG. 19

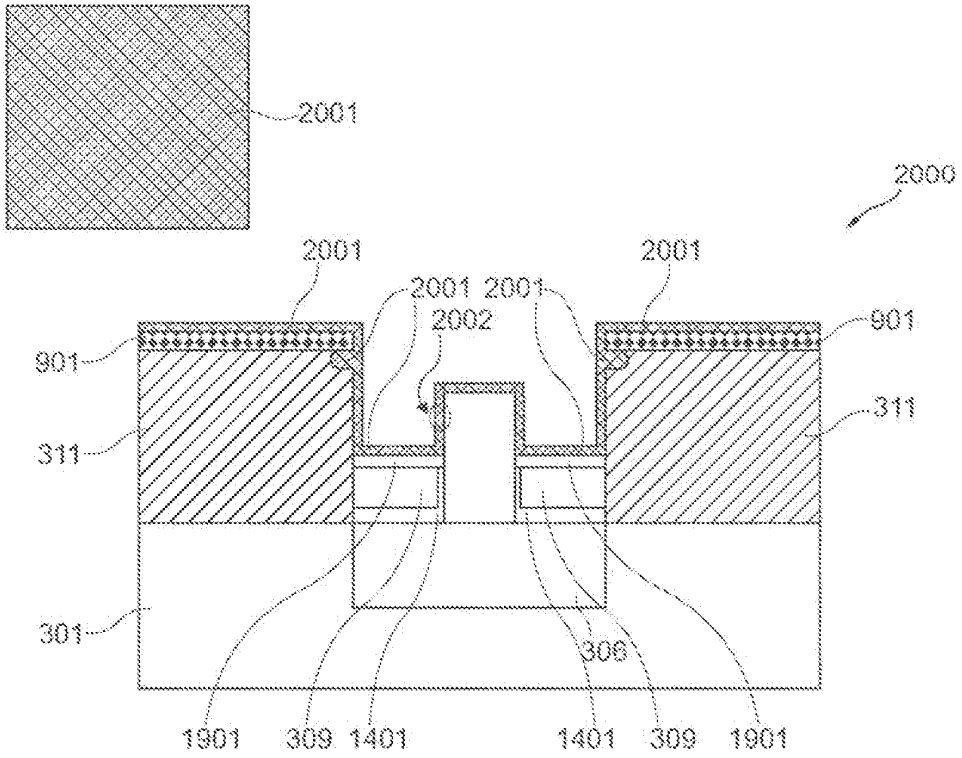

2001
2000
2001
2001
2001
2001
2002
901
901
311
311
301
306
1901
309
1401
1401
309
1901

FIG. 20

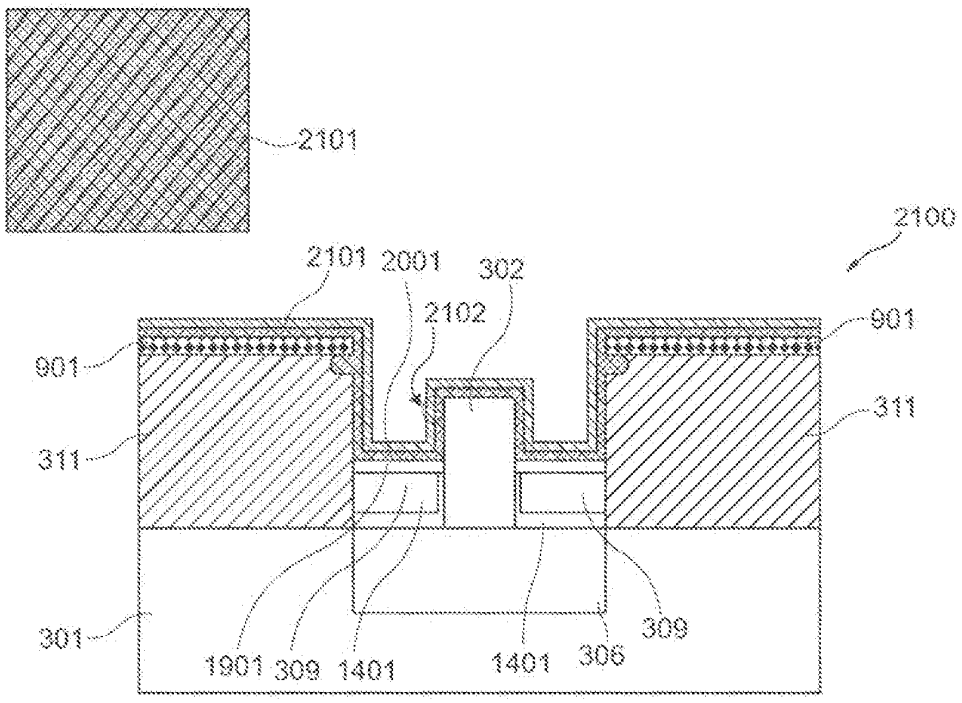

2101
2100
2101
2001
302
2102
901
901
311
311
301
309
1901
309
1401
1401
306

FIG. 21

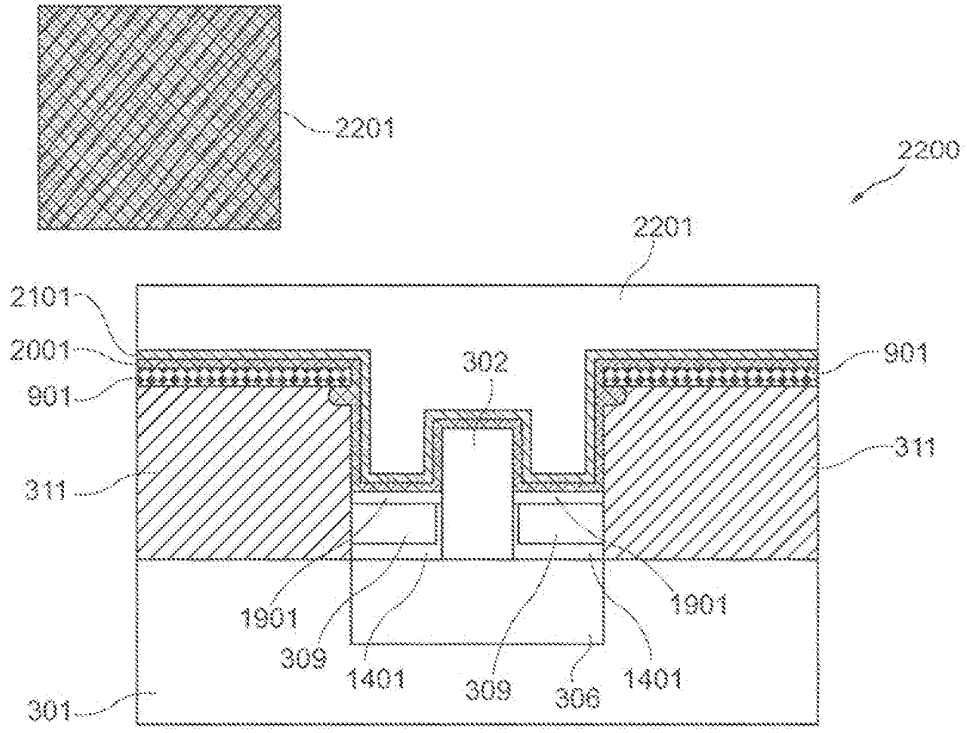

2201
2200
2201
2101
2001
901
302
901
311
311
1901
309
1401
309
306
1401
1901
301

FIG. 22

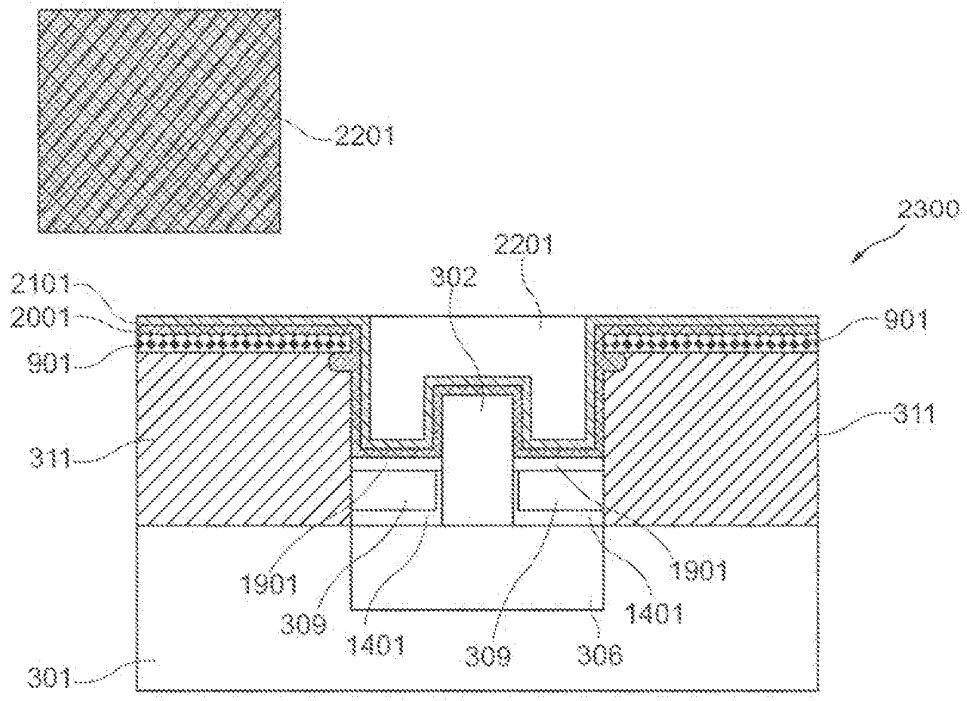

2201
2300
2201
2101
2001
901
302
901
311
311
1901
309
1401
1401
309
306
1901
301

FIG. 23

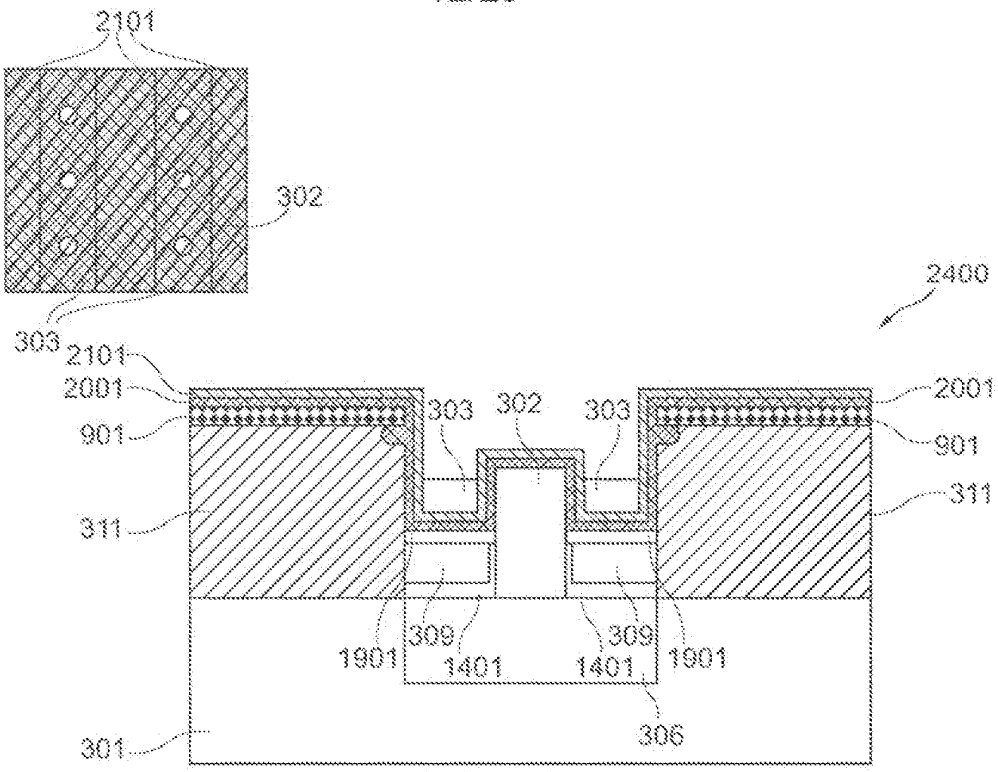

2101
302
303
2400
2101
2001
303
302
303
2001
901
901
311
311
309
309
1901
1401
1401
1901
306
301

FIG. 24

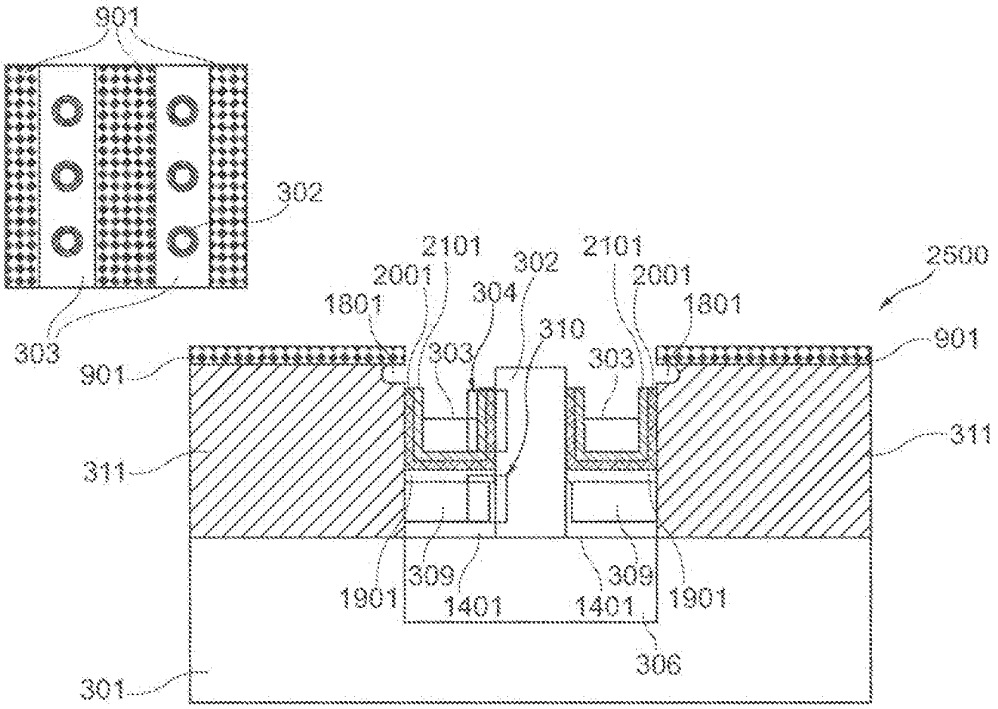

901
302
2101
2101
2500
2001
2001
302
304
1801
1801
310
303
303
303
901
901
311
311
309
309
1901
1401
1401
1901
306
301

FIG. 25

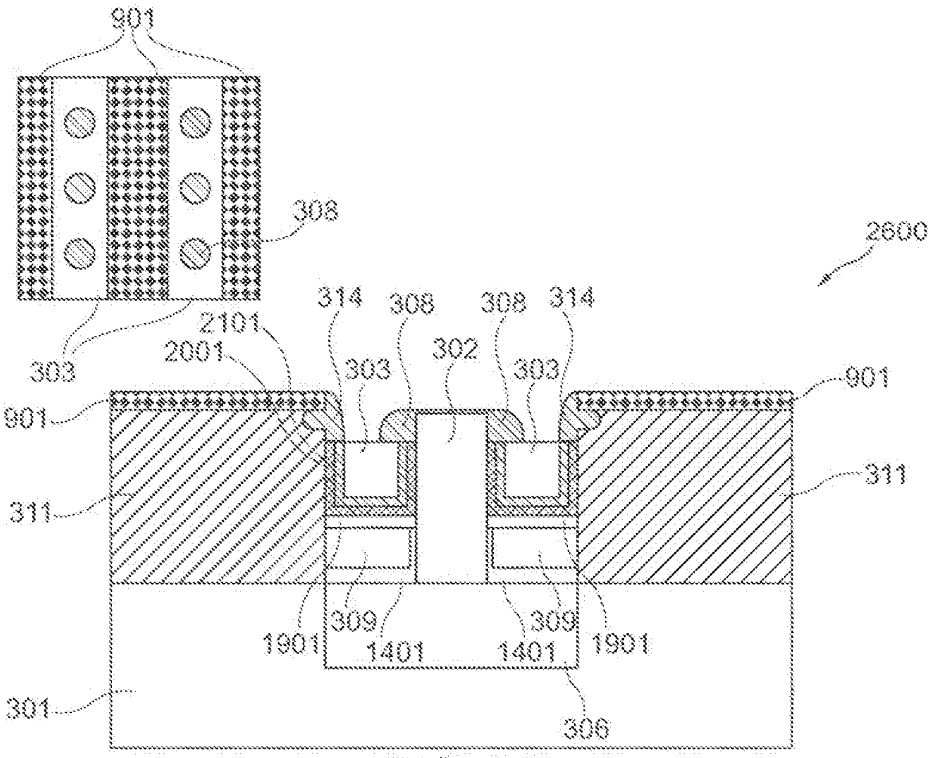

901
308
2600
314
308
308
314
2101
2001
303
302
303
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 26

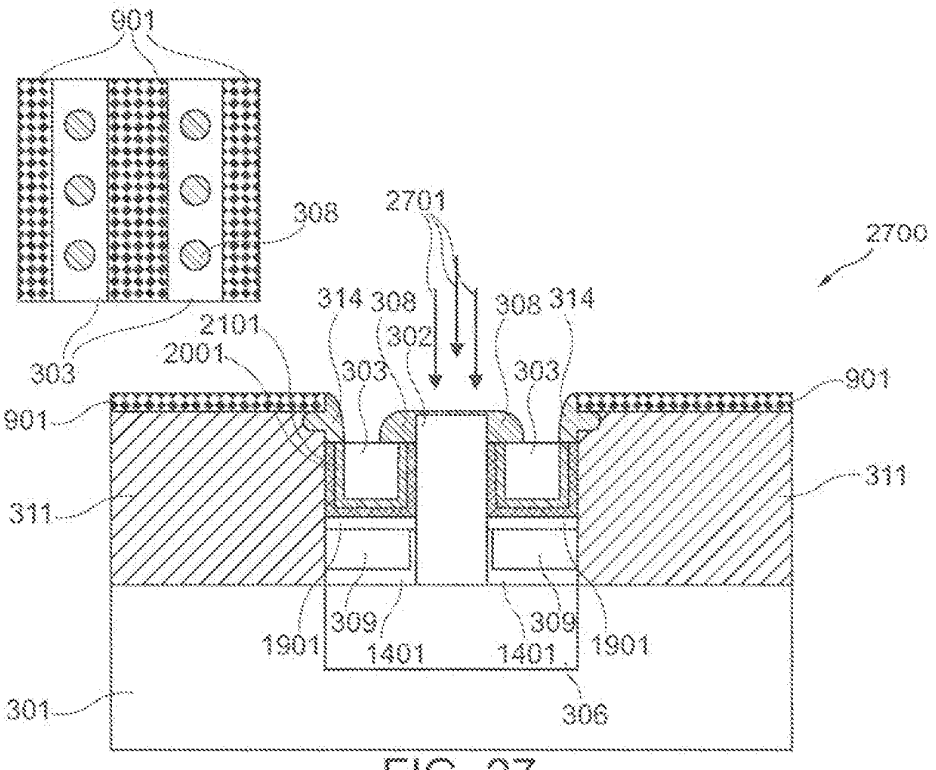

901
308
2701
2700
314
308
308
314
2101
2001
303
302
303
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 27

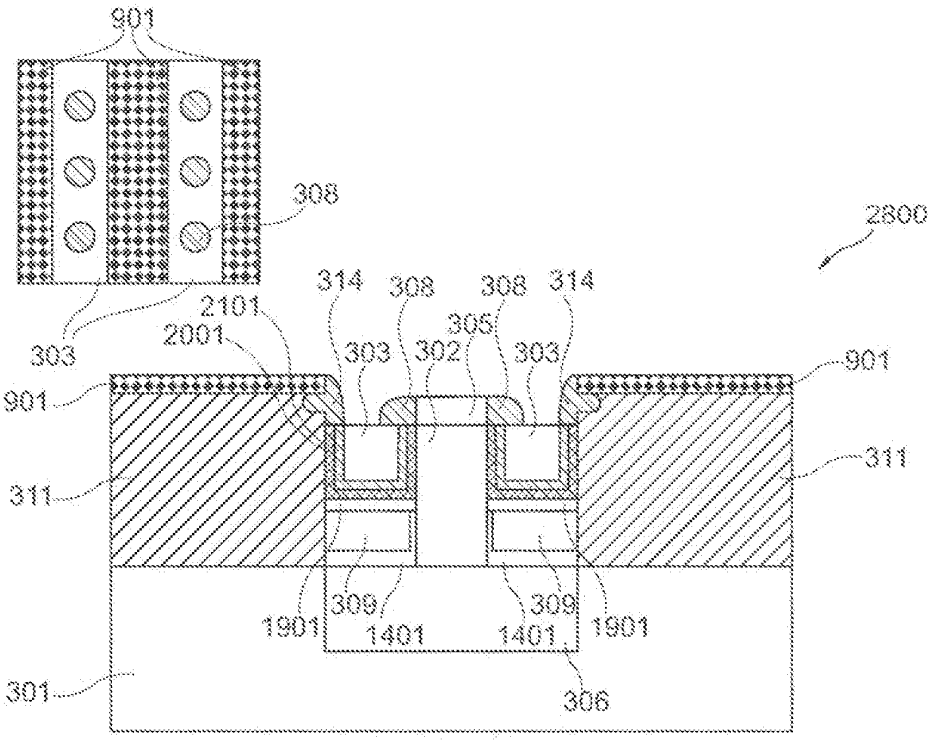

901
308
2800
314
308
308
314
2101
2001
303
305
303
302
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 28

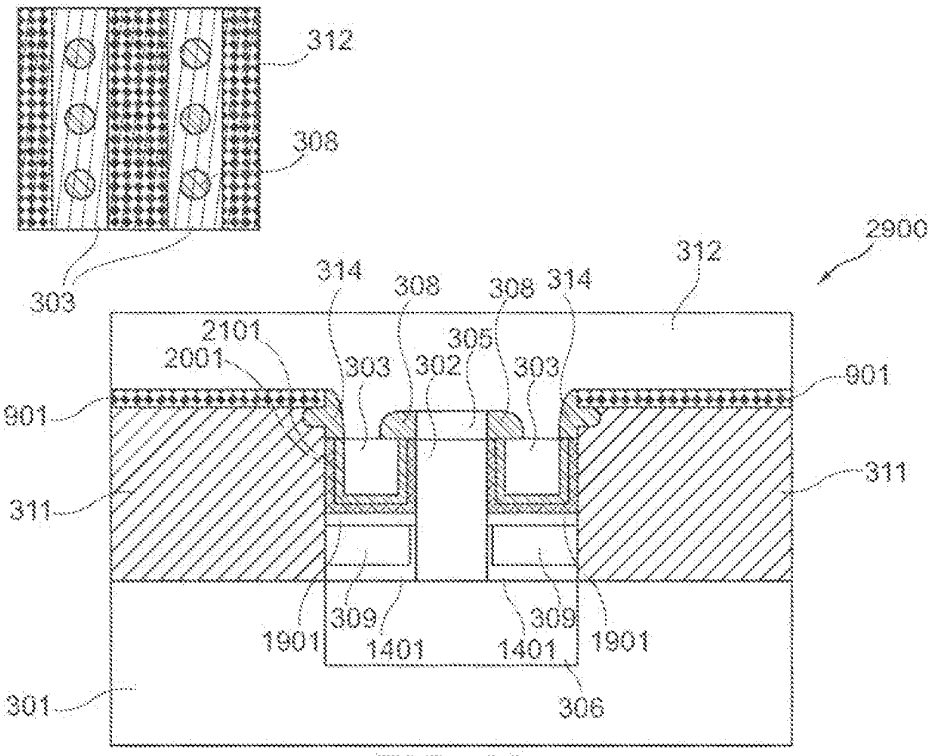

312
308
2900
303
314
308
308
314
312
2101
2001
305
303
302
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 29

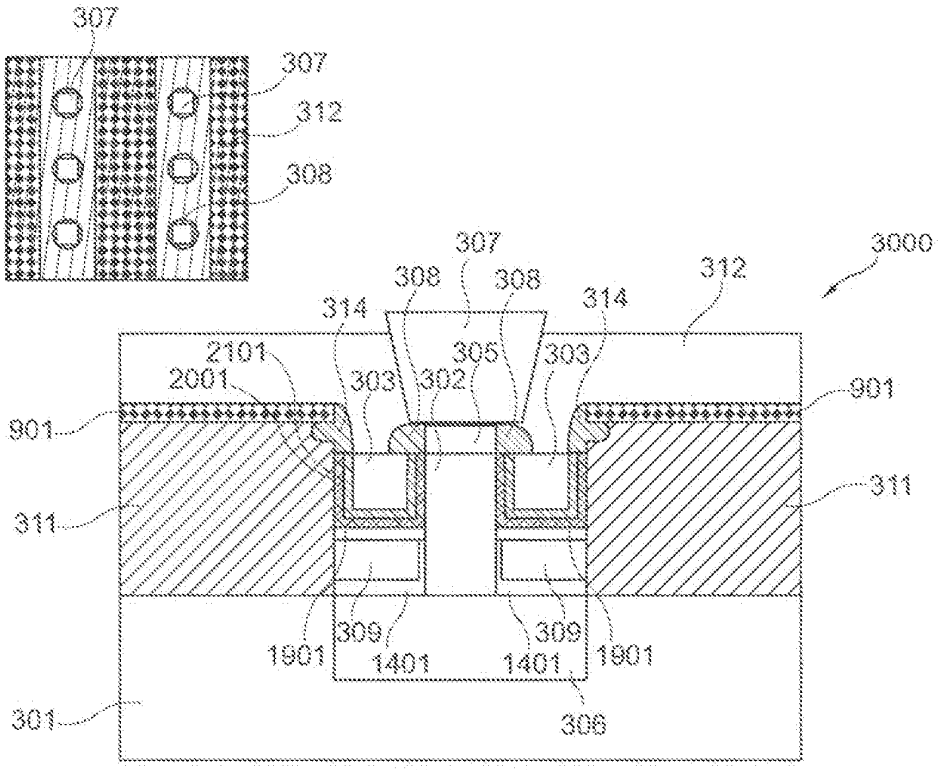

307
307
312
308
3000
307
308
308
312
314
314
2101
2001
303
302
305
303
901
901
311
311
309
309
1901
1401
1401
1901
301
306

FIG. 30

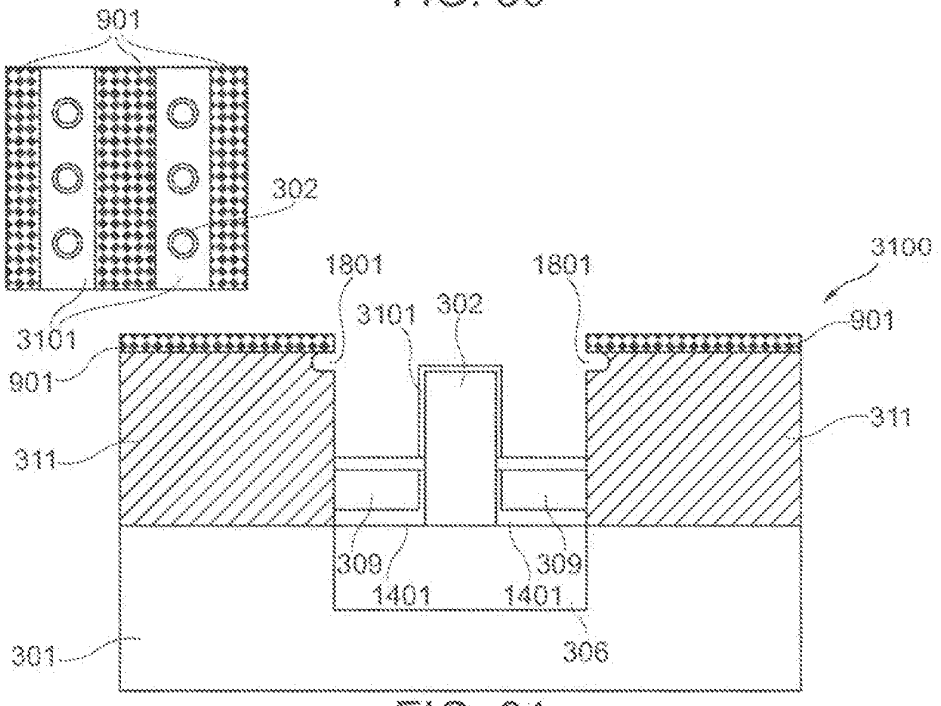

901
302
3100
1801
1801
3101
3101
302
901
901
311
311
309
309
1401
1401
301
306

FIG. 31

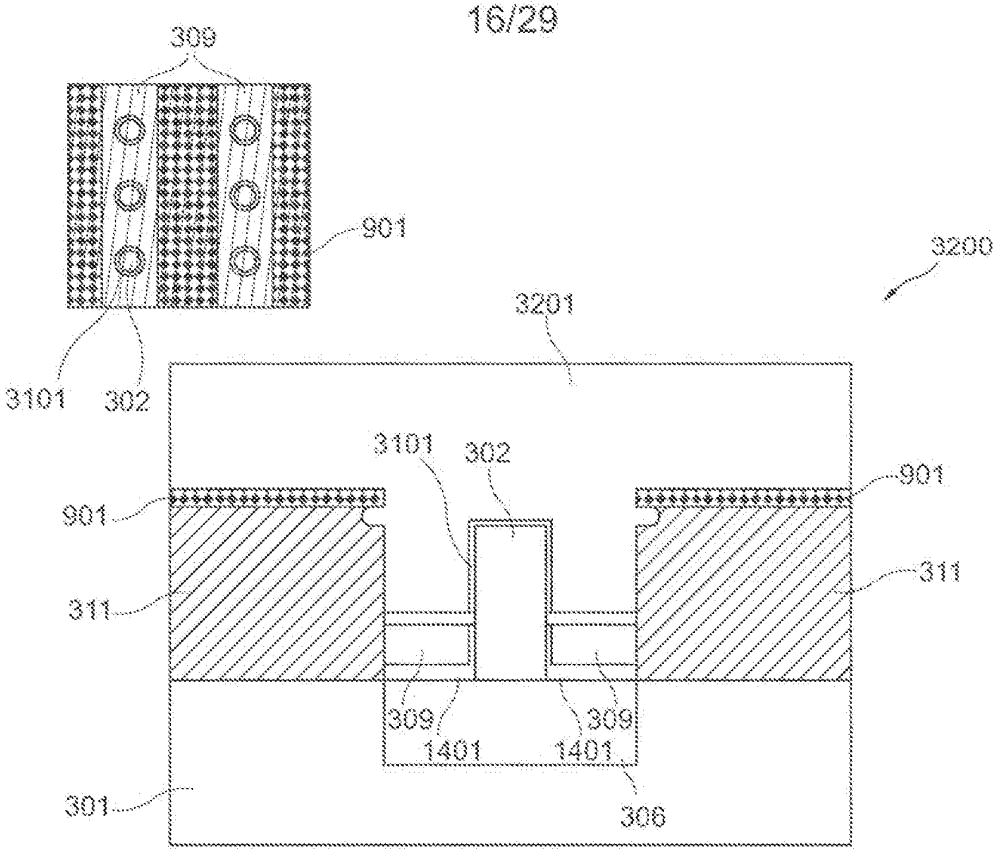

309
901
3200
3201
3101
302
3101
302
901
901
311
311
309
309
1401
1401
301
306

FIG. 32

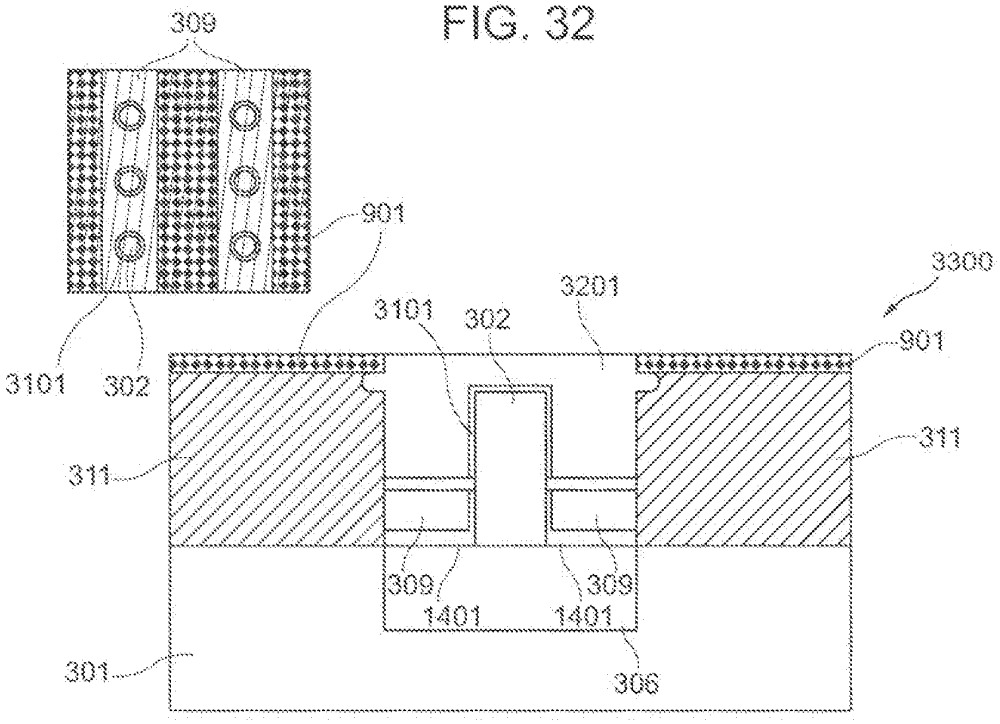

309
901
3300
3201
3101
302
3101
302
901
311
311
309
309
1401
1401
301
306

FIG. 33

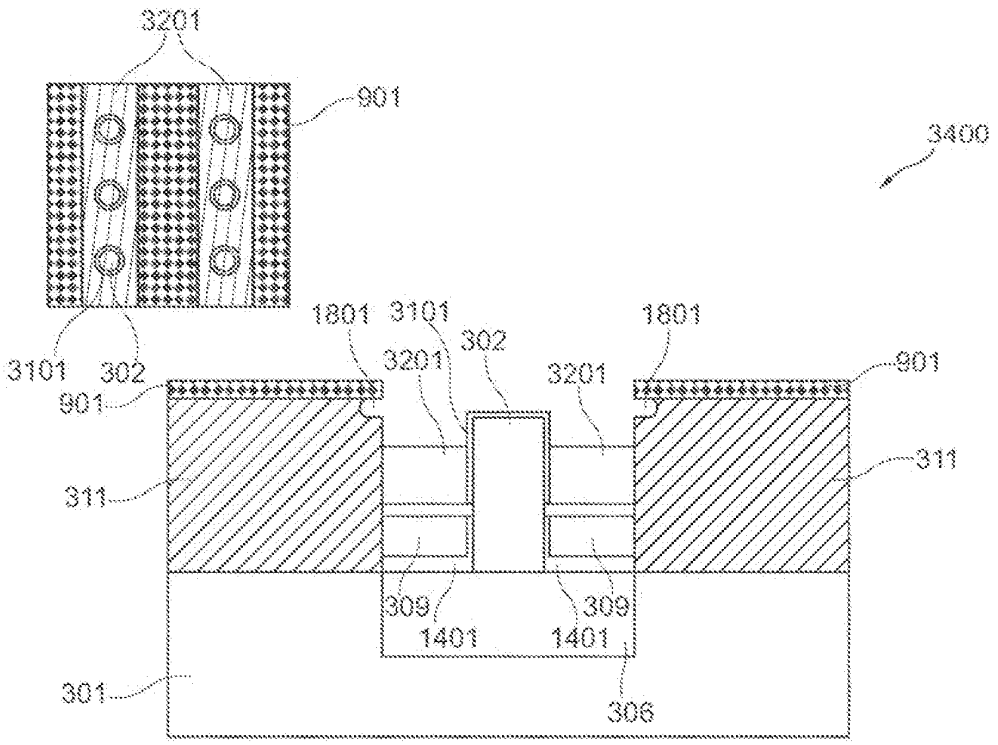

3201
901
3400
1801
3101
302
3201
3201
1801
3101
302
901
901
311
311
309
1401
1401
309
301
306

FIG. 34

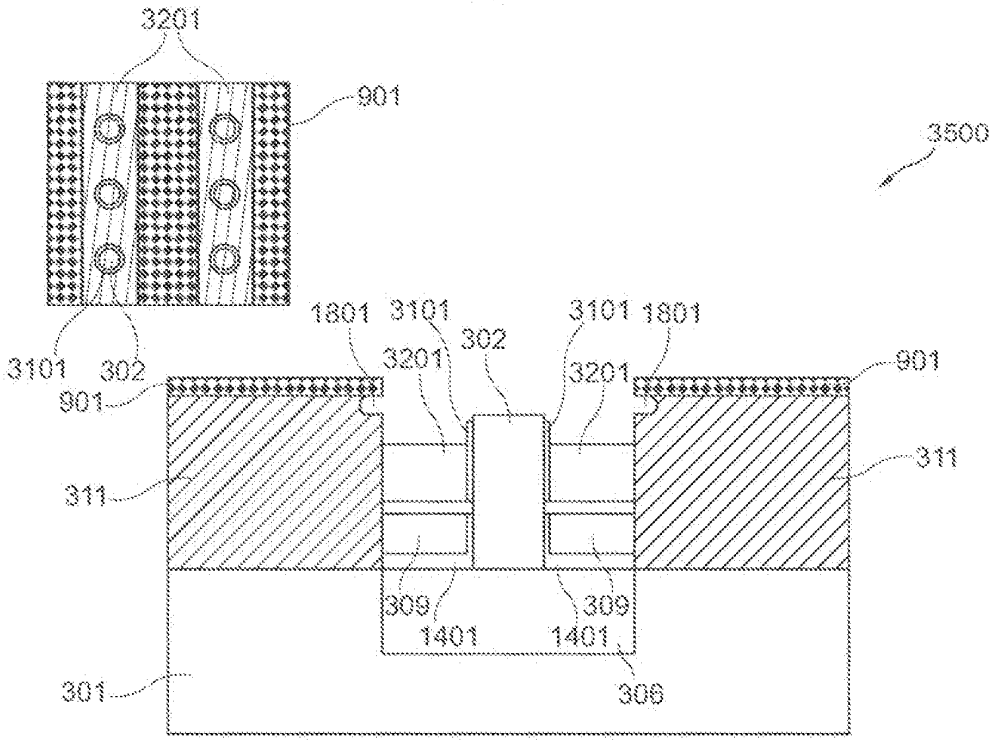

3201
901
3500
1801
3101
3101
1801
302
3201
3201
3101
302
901
901
311
311
309
1401
1401
309
301
306

FIG. 35

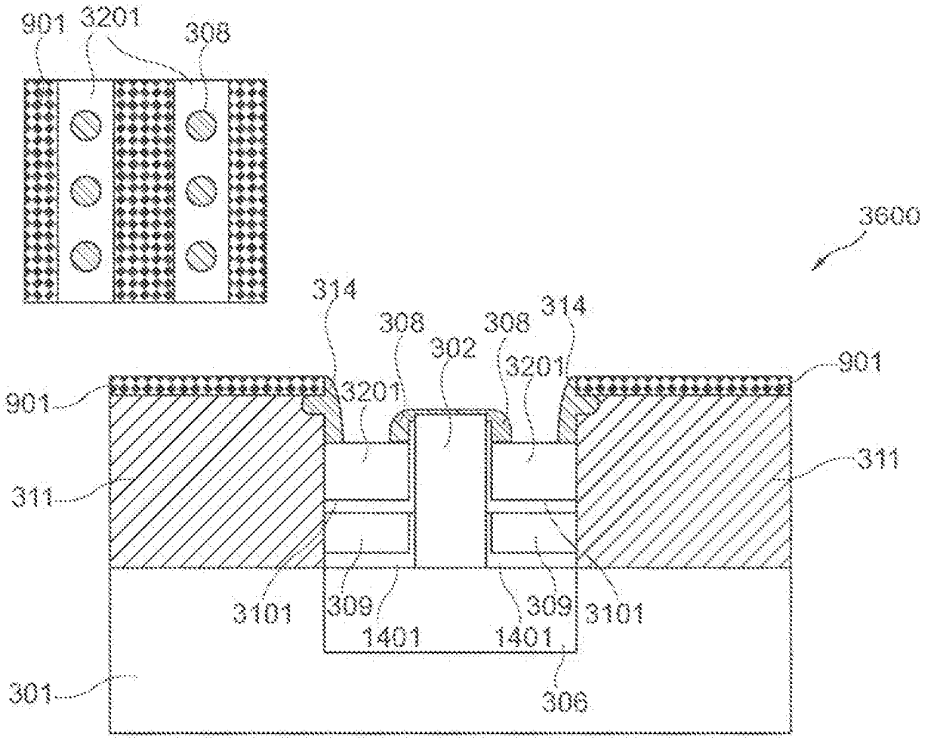

901
3201
308
3600
314
308
302
308
314
3201
3201
901
901
311
311
3101
309
1401
1401
309
3101
301
306

FIG. 36

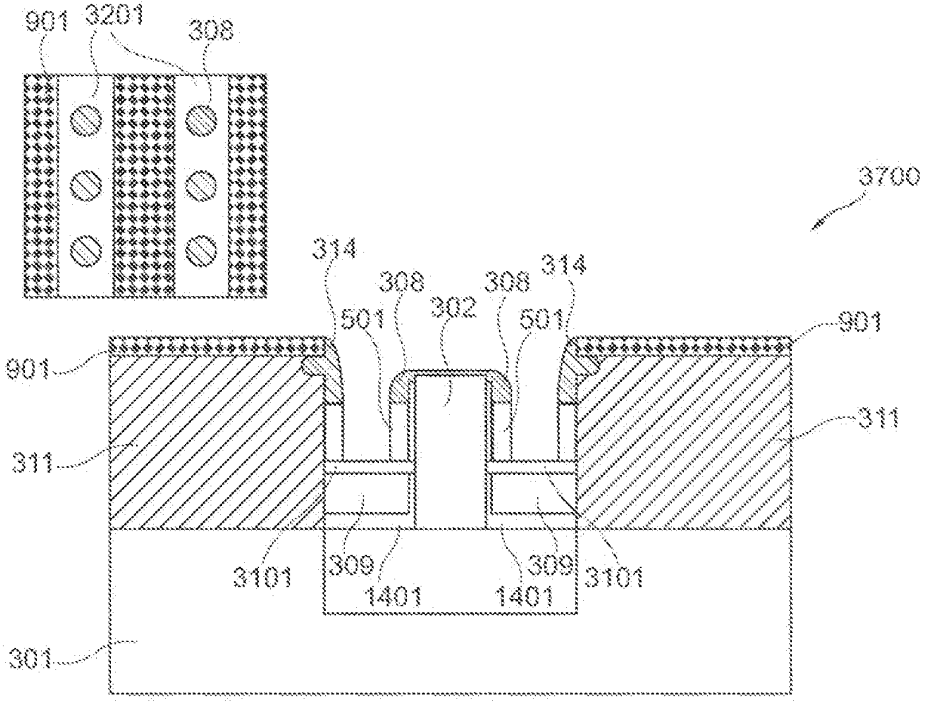

901
3201
308
3700
314
308
302
308
314
501
501
901
901
311
311
3101
309
1401
1401
309
3101
301

FIG. 37

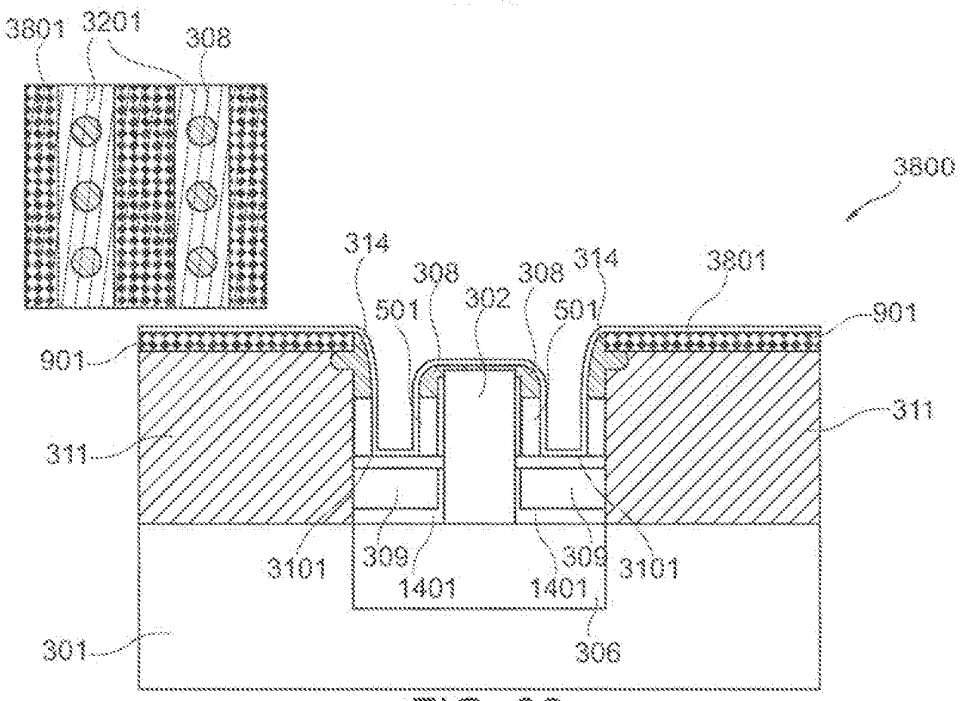

3801
3201
308
3800
314
308
308
314
3801
501
302
501
901
901
311
311
3101
309
309
3101
1401
1401
301
306

FIG. 38

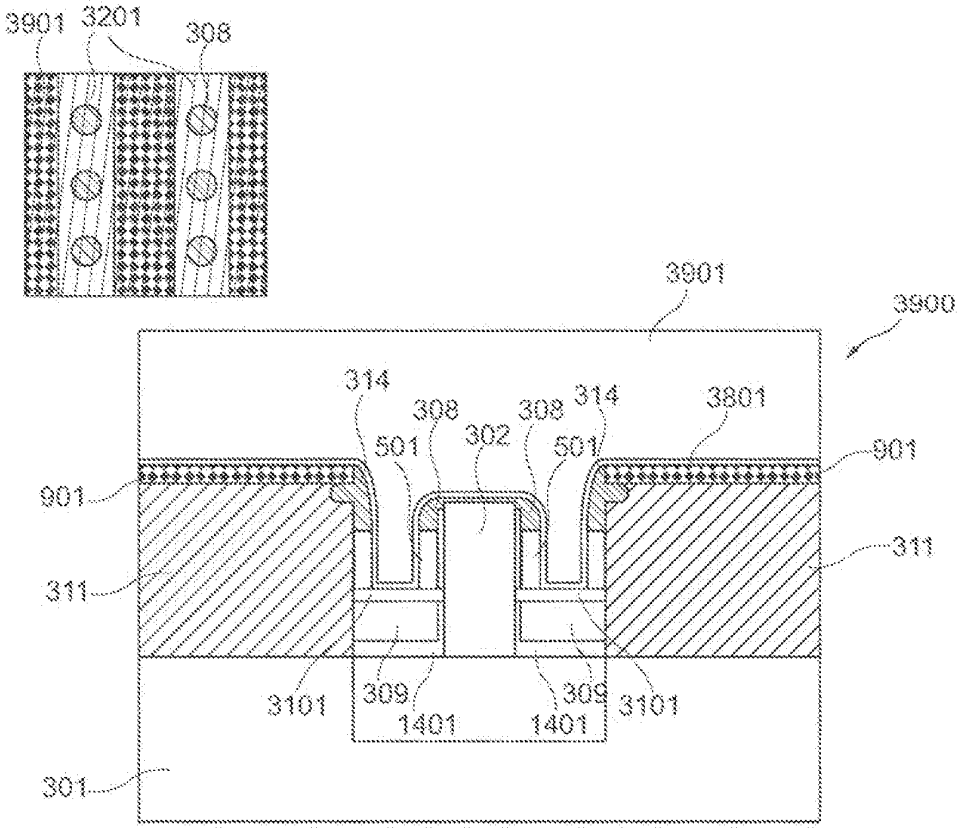

3901
3201
308
3901
3900
314
308
308
314
3801
501
302
501
901
901
311
311
3101
309
309
3101
1401
1401
301

FIG. 39

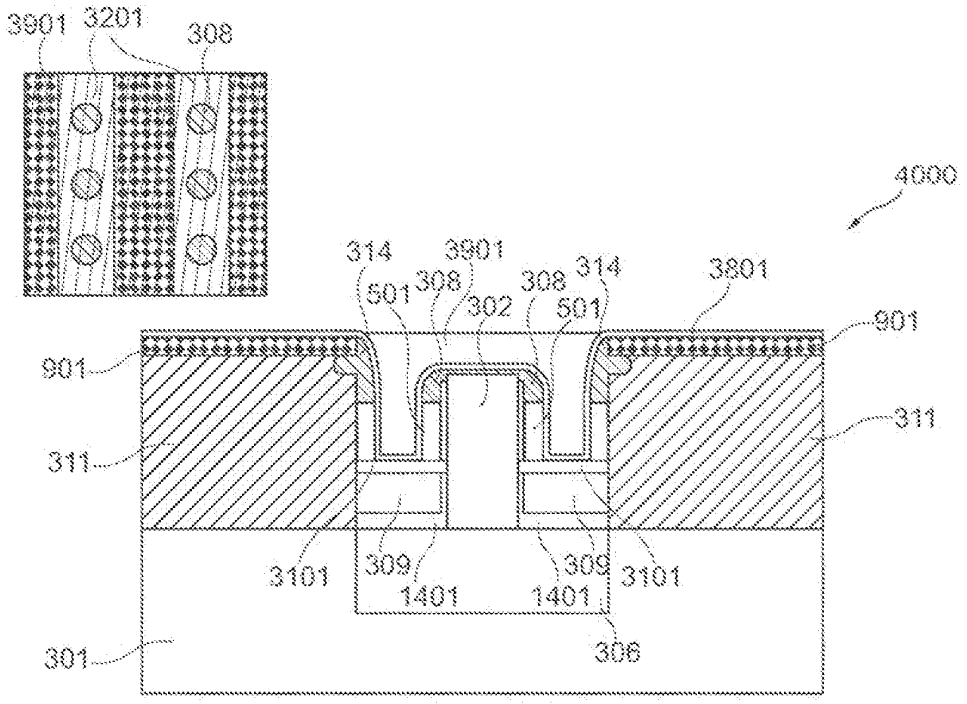

3901
3201
308
4000
314
3901
501
308
302
308
314
501
3801
901
901
311
311
3101
309
1401
1401
309
3101
301
306

FIG. 40

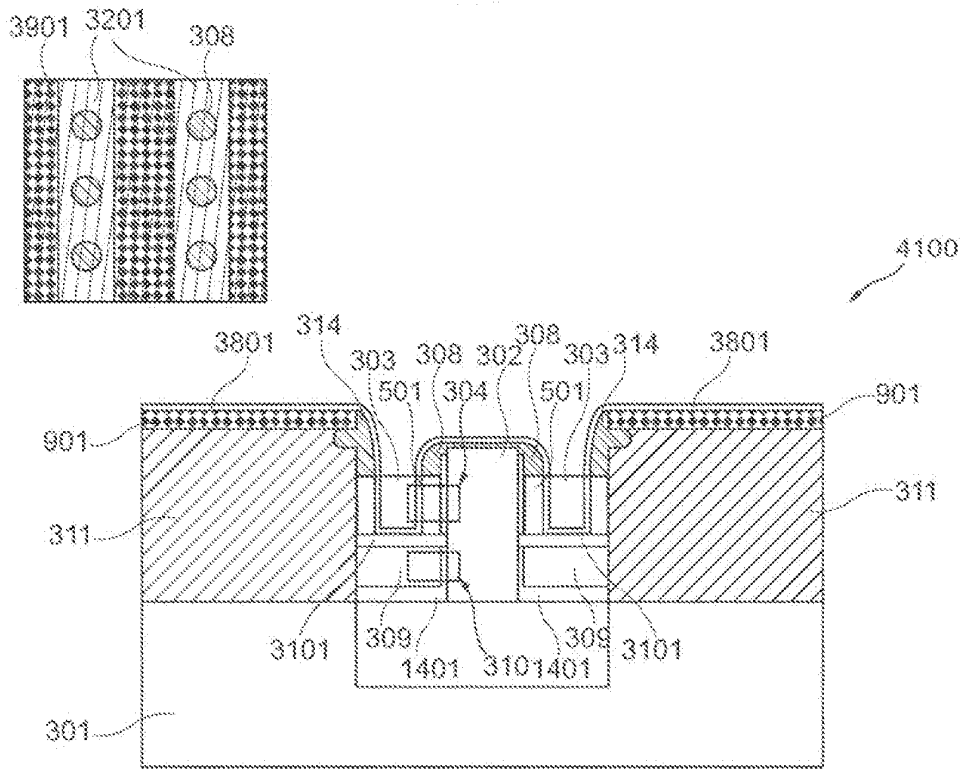

3901
3201
308
4100
3801
314
303
308
302
308
303
314
3801
501
304
501
901
901
311
311
3101
309
1401
3101
1401
309
3101
301

FIG. 41

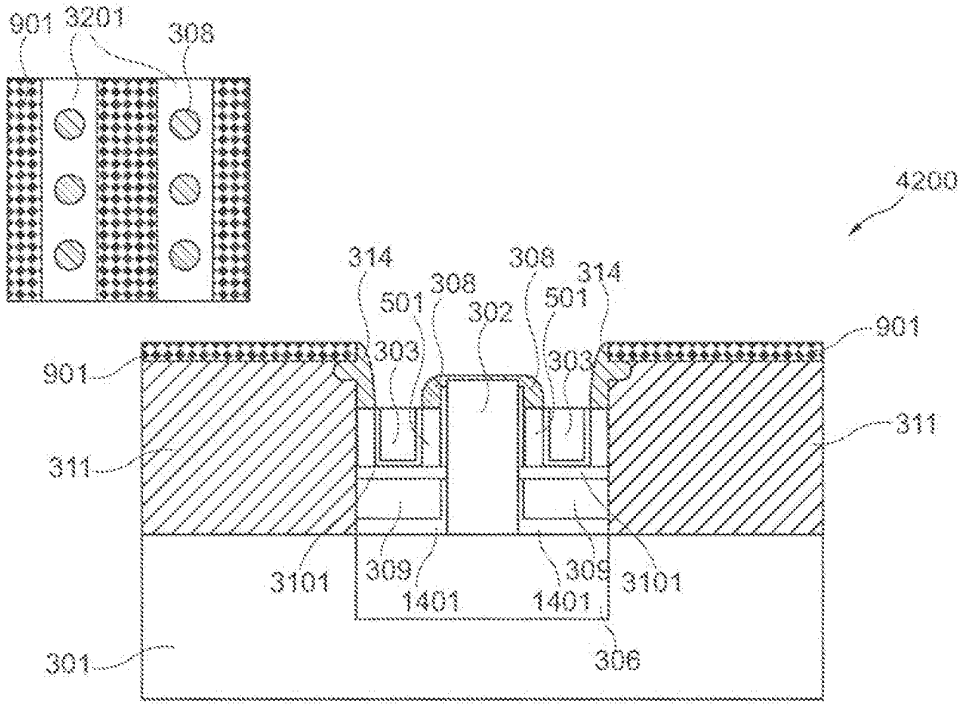

901
3201
308
4200
314
308
308
314
501
308
501
302
303
303
901
901
311
311
3101
309
309
3101
1401
1401
301
306

FIG. 42

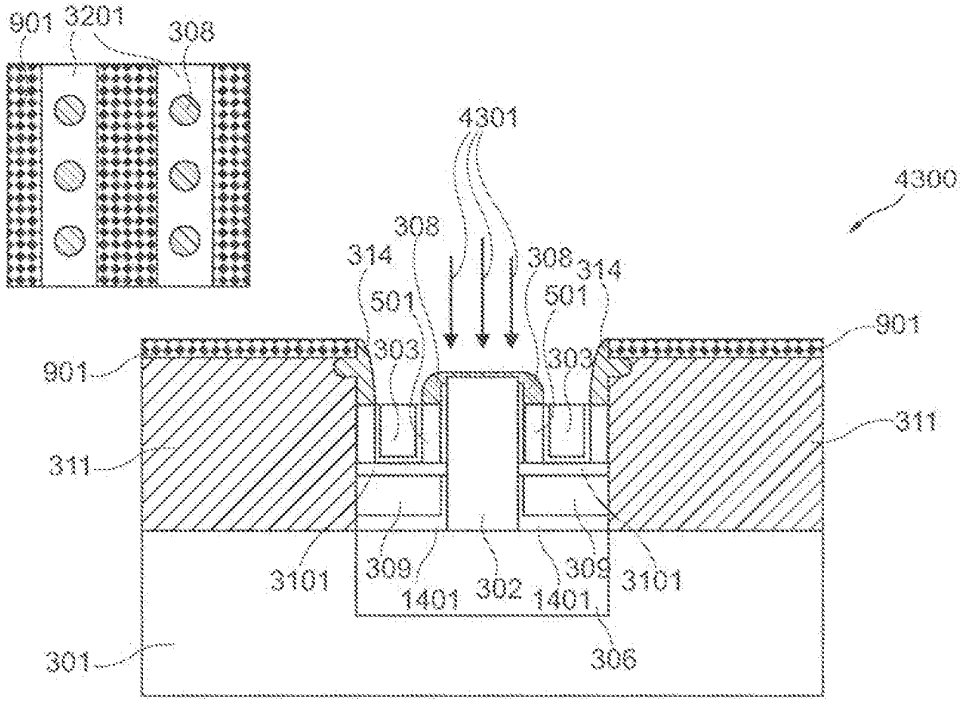

901
3201
308
4301
4300
308
314
308
314
501
501
303
303
901
901
311
311
3101
309
309
3101
1401
302
1401
301
306

FIG. 43

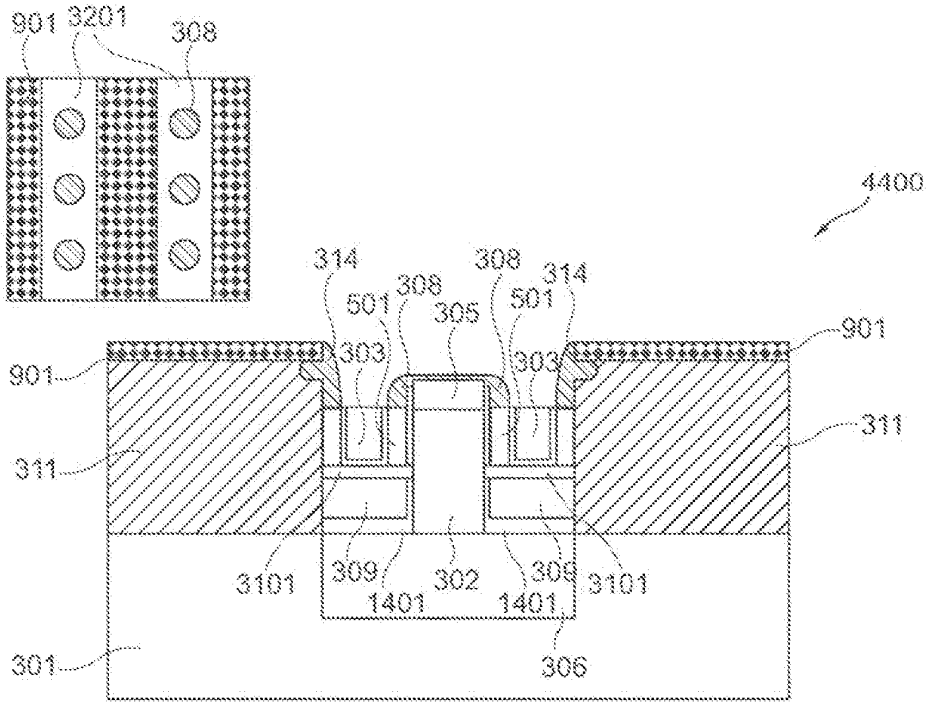

901
3201
308
4400
314
308
308
314
501
501
305
303
303
901
901
311
311
3101
309
302
309
3101
1401
1401
301
306

FIG. 44

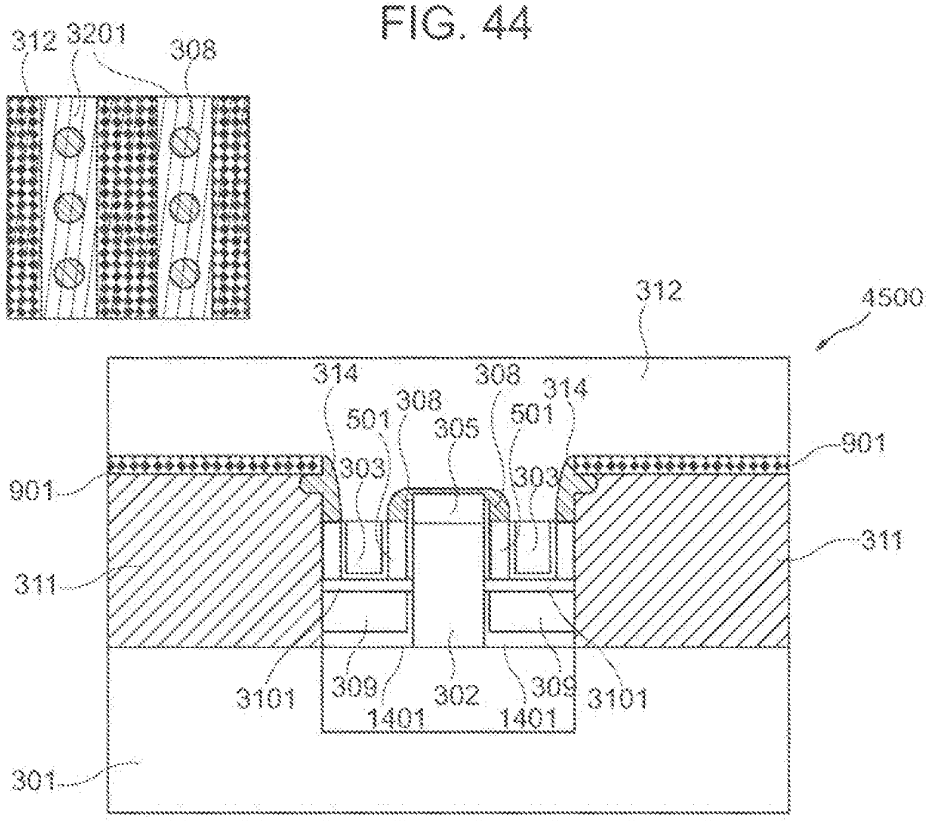

312
3201
308
312
4500
314
308
308
314
501
501
305
303
303
901
901
311
311
3101
309
302
309
3101
1401
1401
301

FIG. 45

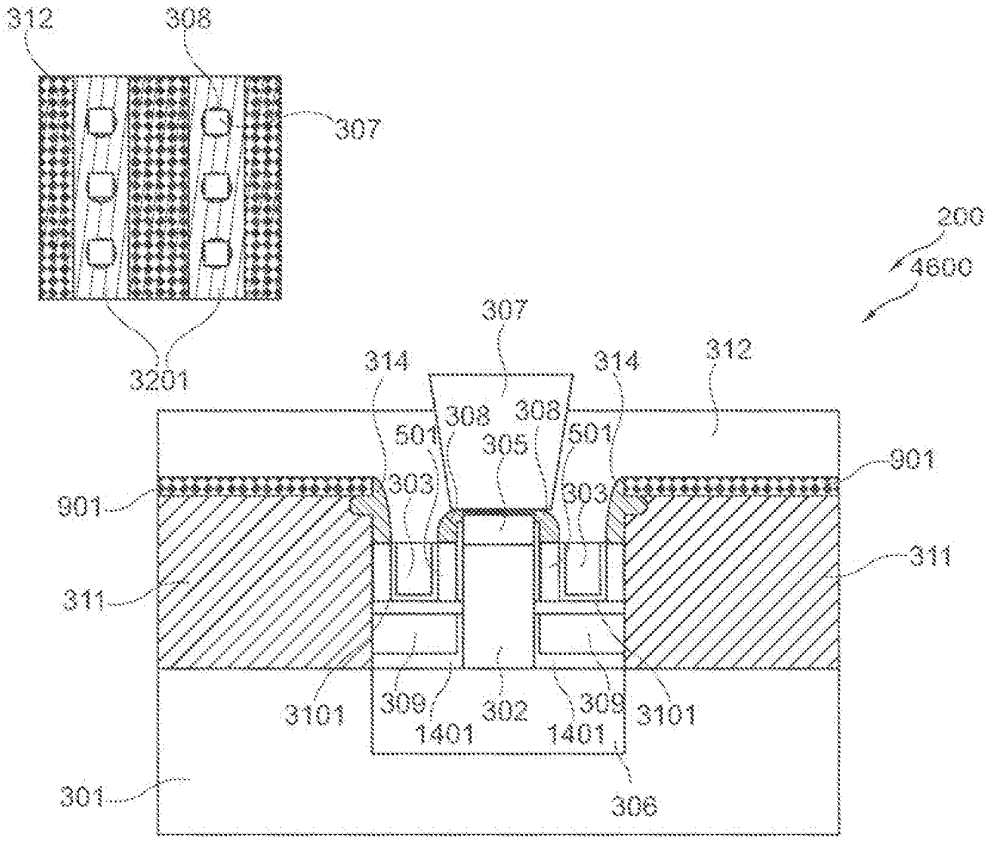

312
308
307
3201
200
4600
307
314
314
312
308
308
501
305
501
303
303
901
901
311
311
3101
309
302
309
3101
1401
1401
301
306

FIG. 46

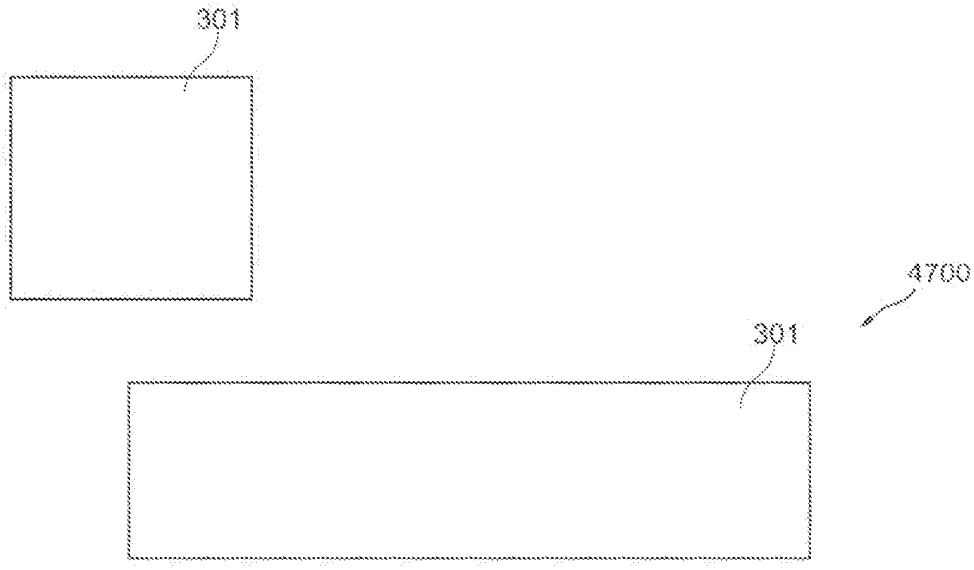

301
4700
301

FIG. 47

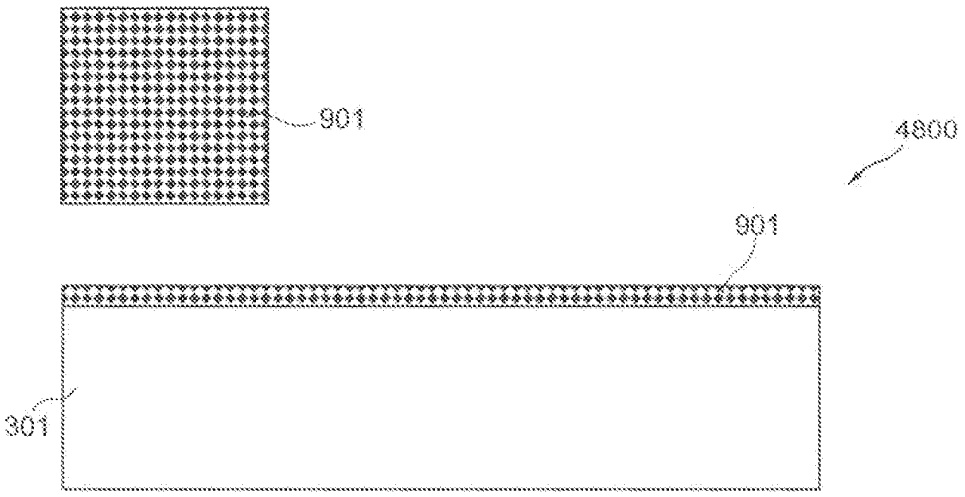


FIG. 48

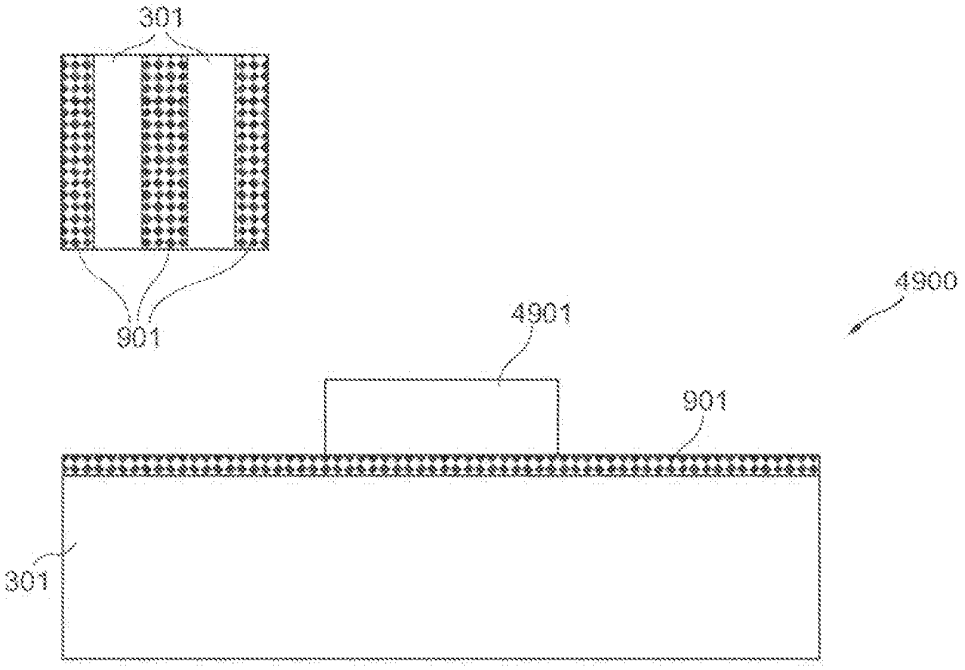


FIG. 49

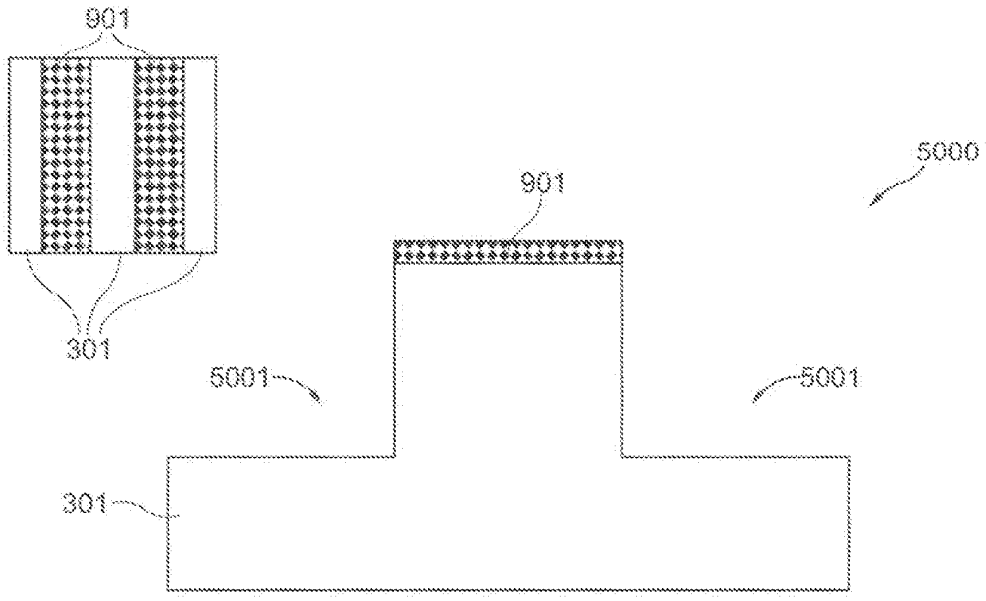


FIG. 50

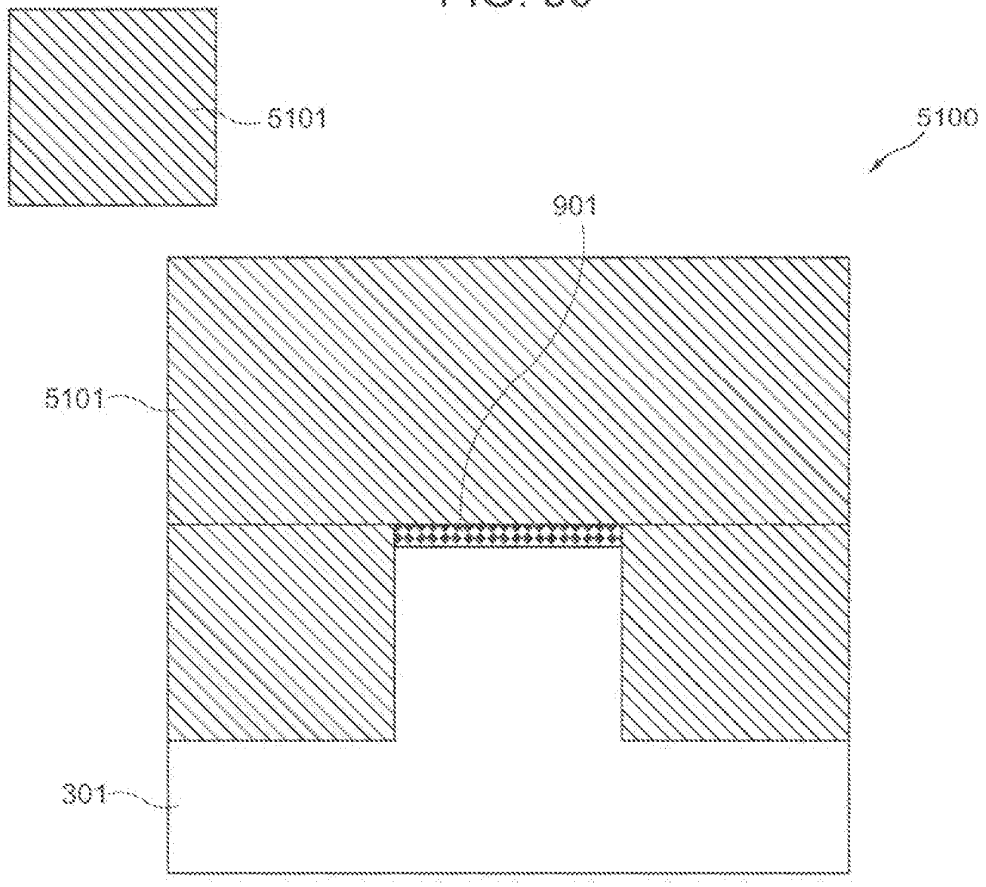


FIG. 51

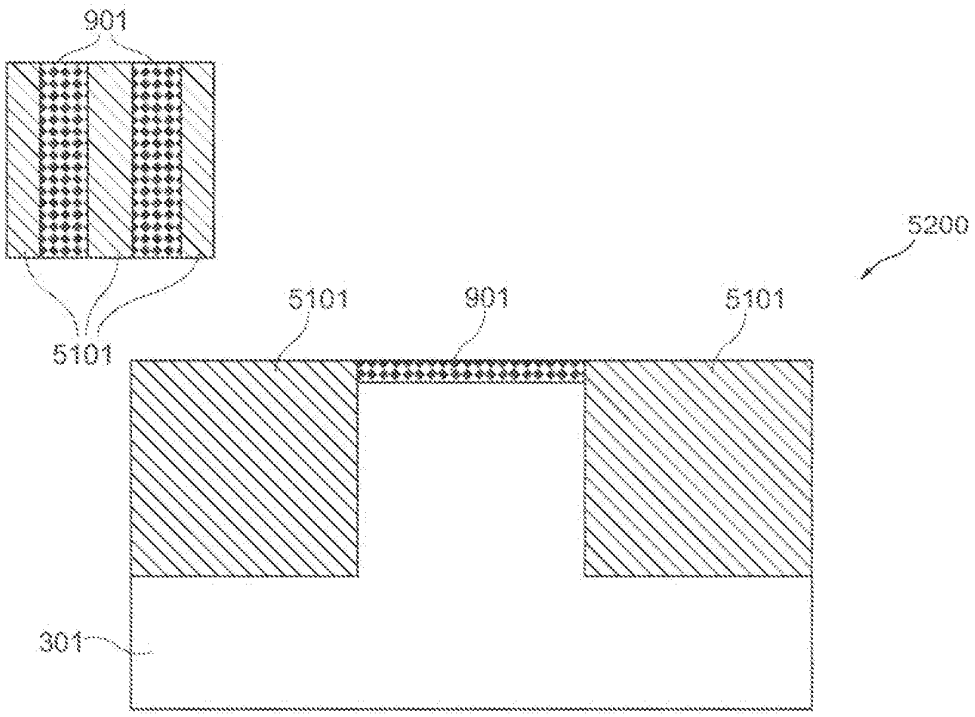

901
5101
5101
901
5101
5200
301

FIG. 52

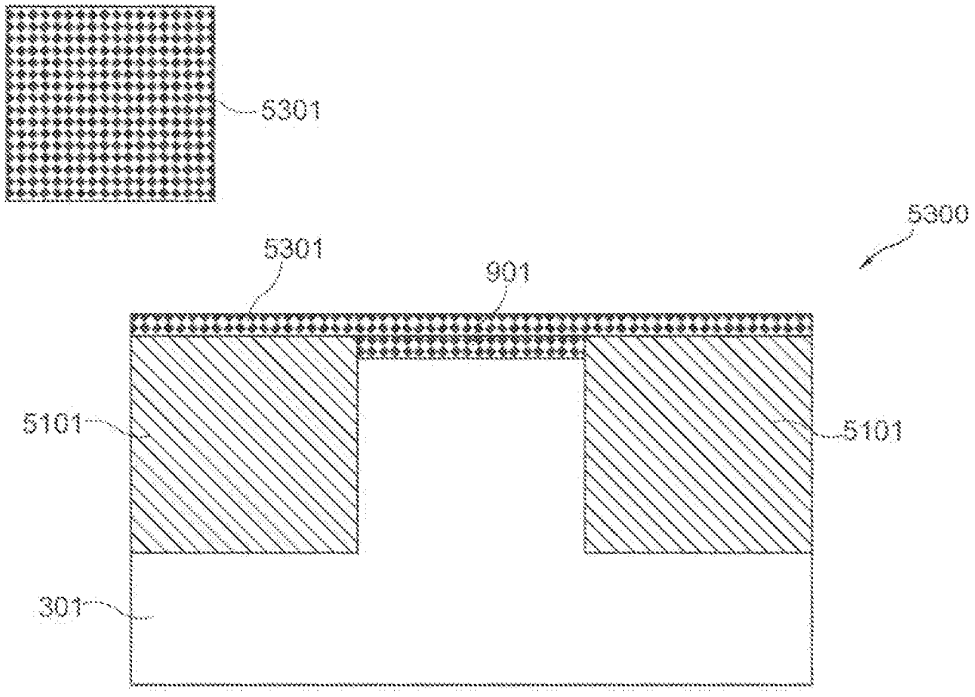

5301
5301
901
5300
5101
5101
301

FIG. 53

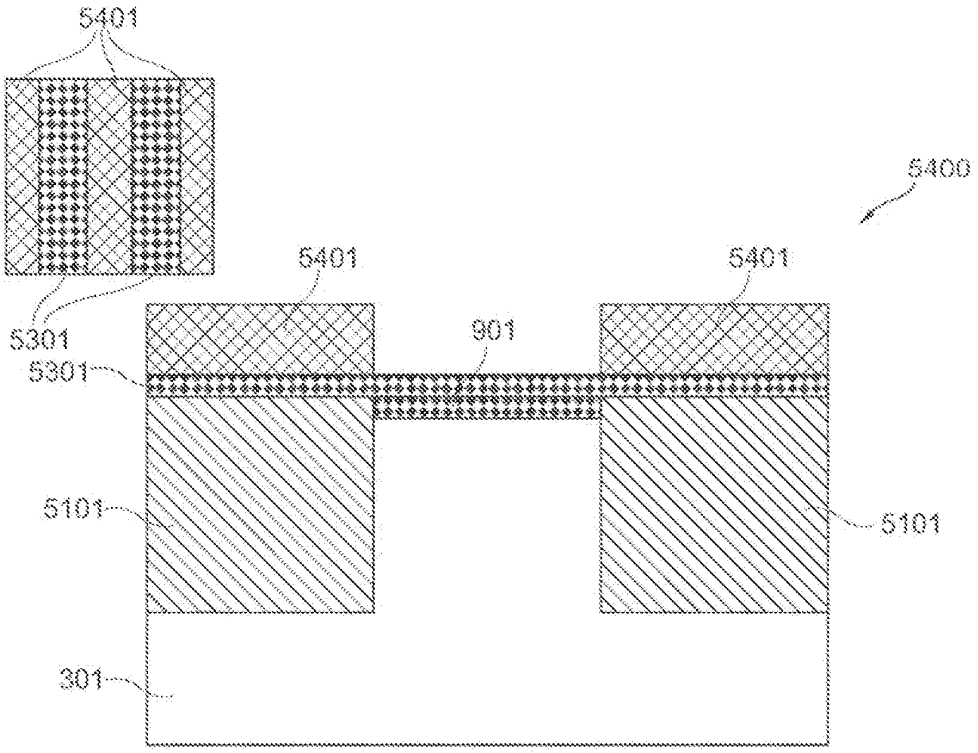

5401
5400
5401
5401
5301
901
5301
5101
5101
301

FIG. 54

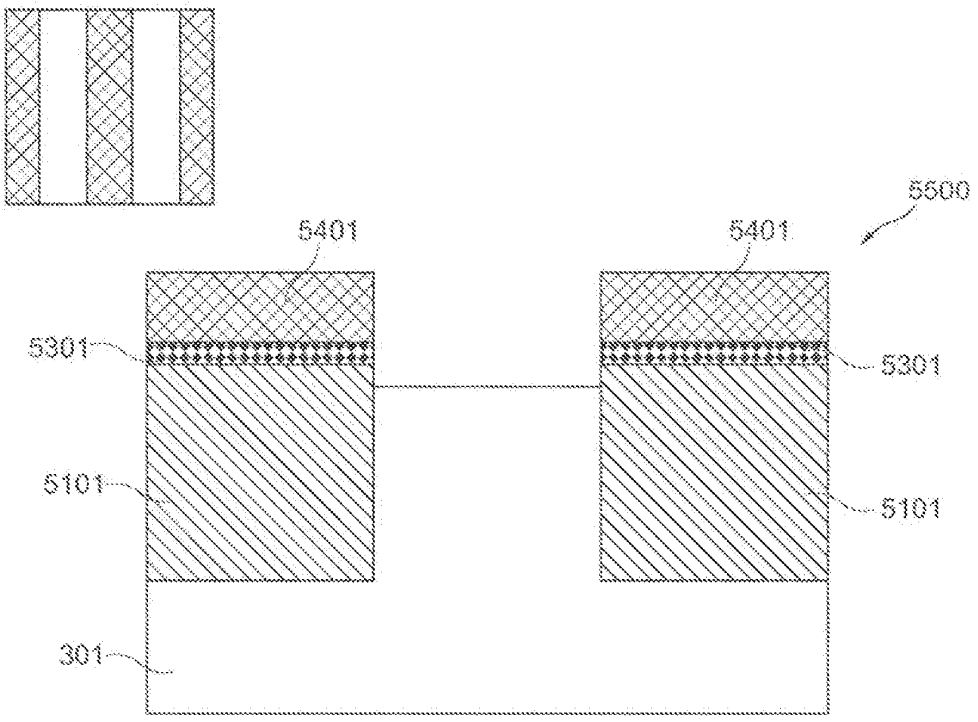

5500
5401
5401
5301
5301
5101
5101
301

FIG. 55

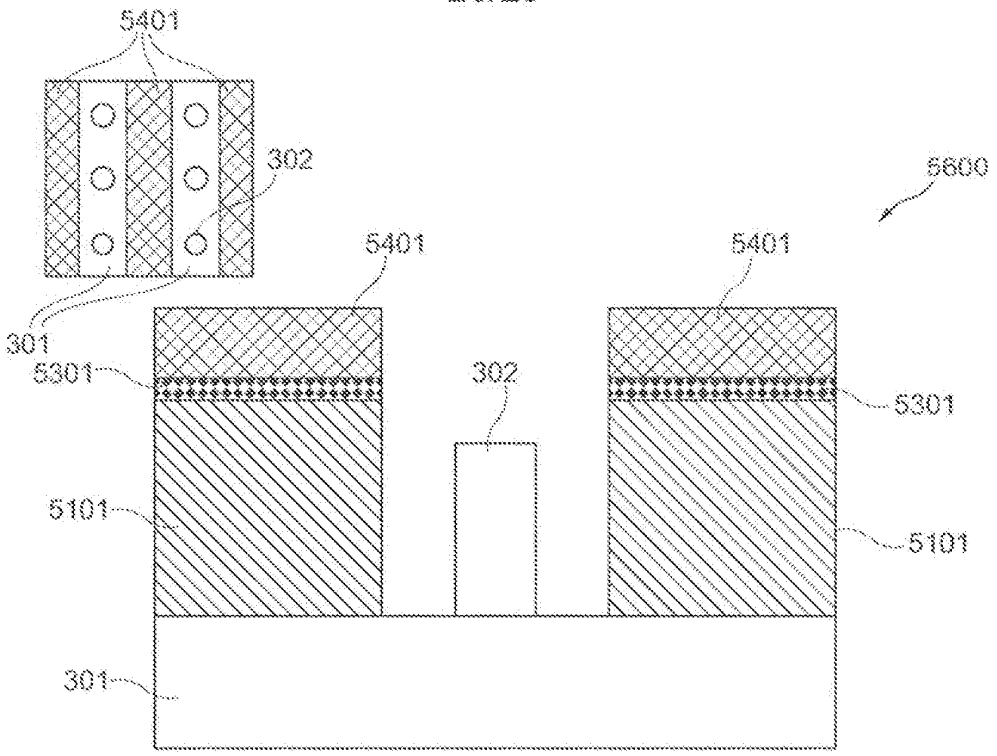

5401
302
5600
5401
5401
301
5301
302
5301
5101
5101
301

FIG. 56

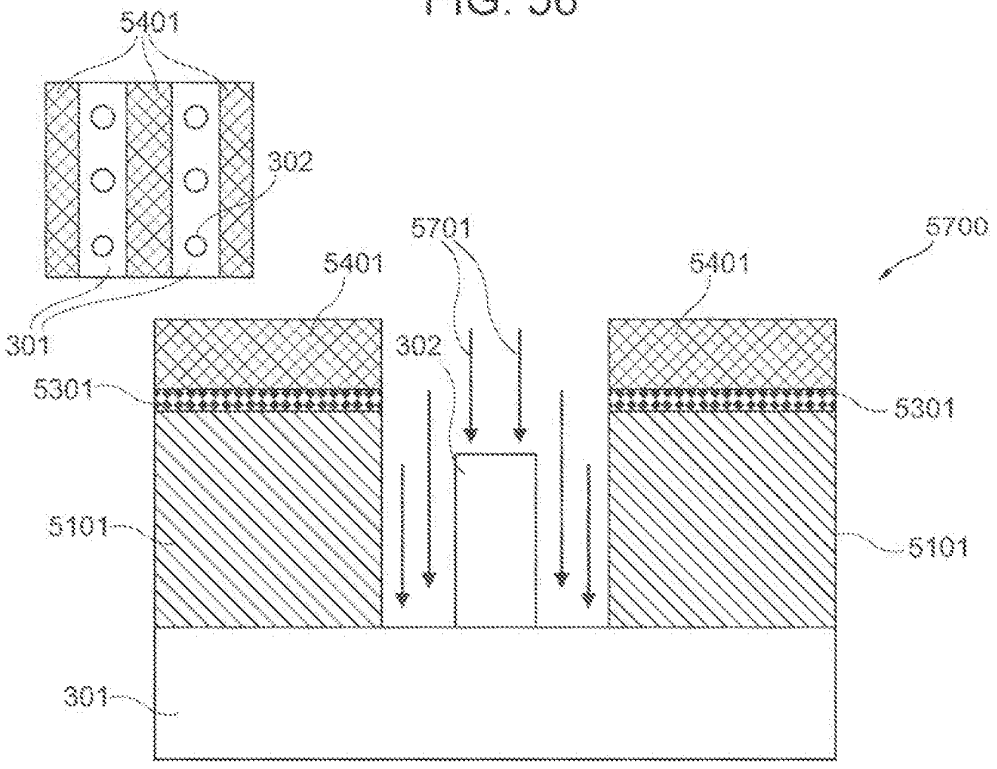

5401
302
5701
5700
5401
5401
301
302
5301
5301
5101
5101
301

FIG. 57

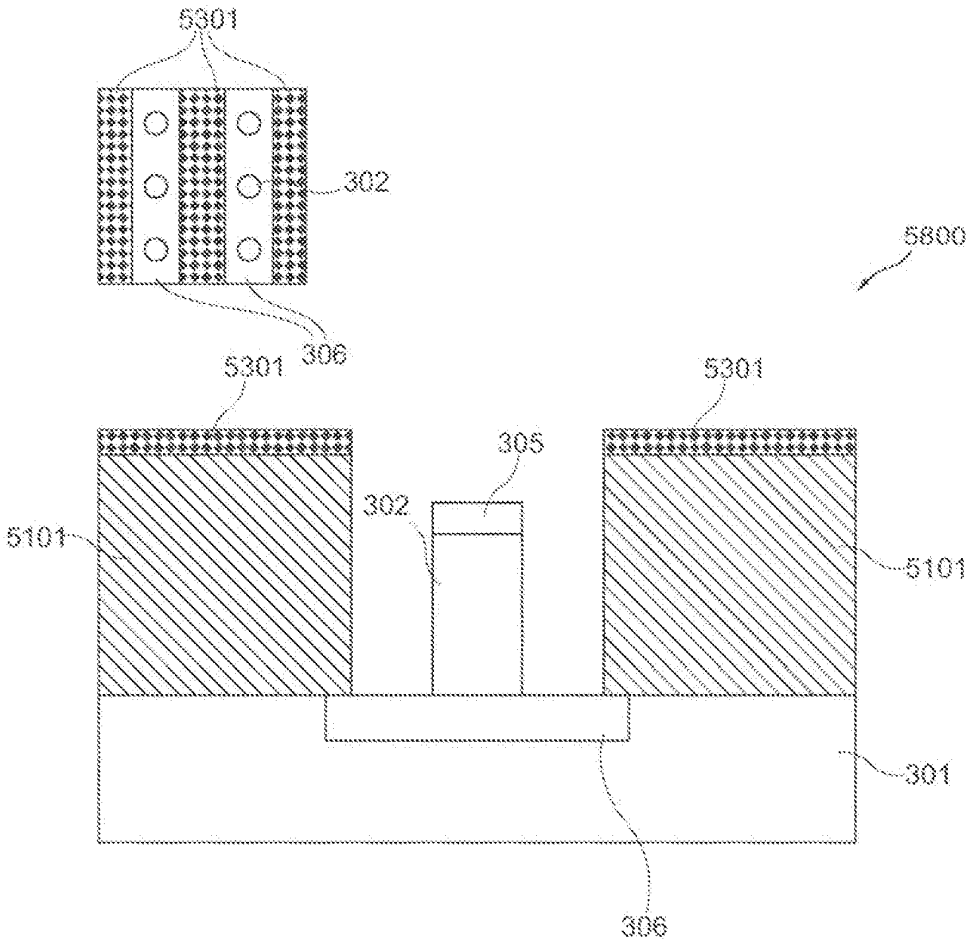


FIG. 58

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/051478

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/28 H01L21/336 H01L21/8246 H01L21/8247 H01L27/115
H01L29/788 H01L29/792 G11C16/04 H01L29/423 H01L29/06
H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PEIN H ET AL: "PERFORMANCE OF THE 3-D PENCIL FLASH EPROM CELL AND MEMORY ARRAY" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 42, no. 11, 1 November 1995 (1995-11-01), pages 1982-1991, XP000582412 ISSN: 0018-9383 the whole document	1-18
X	WO 2004/040667 A (INFINEON TECHNOLOGIES AG [DE]; GRAHAM ANDREW [DE]; HOFMANN FRANZ [DE];) 13 May 2004 (2004-05-13) the whole document	1-18
Y	EP 1 420 414 A (SAMSUNG ELECTRONICS CO LTD [KR]) 19 May 2004 (2004-05-19) the whole document	1-18

-/--

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 August 2008	18/08/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Neumann, Andreas

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/051478

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2005/124872 A (KONINKL PHILIPS ELECTRONICS NV [NL]; HIJZEN ERWIN A [BE]; BAKKERS ERIK) 29 December 2005 (2005-12-29) page 7, line 28 - page 8, line 19; figure 2	1-18
A	US 6 433 382 B1 (ORLOWSKI MARIUS [US] ET AL) 13 August 2002 (2002-08-13) column 3, line 57 - column 4, line 11; figure 1	9,10

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2008/051478

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 2004040667	A	13-05-2004	DE	10250829 A1	19-05-2004
			EP	1568087 A1	31-08-2005
			JP	2006504278 T	02-02-2006
			US	2006011972 A1	19-01-2006
EP 1420414	A	19-05-2004	CN	1501503 A	02-06-2004
			DE	60300477 D1	12-05-2005
			DE	60300477 T2	23-02-2006
			JP	4047797 B2	13-02-2008
			JP	2004172616 A	17-06-2004
			JP	2007329500 A	20-12-2007
			KR	20040043043 A	22-05-2004
			US	2004095837 A1	20-05-2004
WO 2005124872	A	29-12-2005	CN	1977385 A	06-06-2007
			EP	1759417 A1	07-03-2007
			JP	2008503081 T	31-01-2008
			US	2008029909 A1	07-02-2008
US 6433382	B1	13-08-2002	NONE		

Sandisk Technologies, Inc. - Ex. 1040, Page 000279

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	976	(dielectric SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:29
L2	151	((dielectric adj constant) SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:29
L3	41	((high adj dielectric adj constant) SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:30
L4	2691	257/314.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:41
L7	11	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) l4	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:42
L8	13	(((oxide$1nitride$11oxide OR ONO)) ((oxygen$1rich) SAME nitride)) l4	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:43
L9	2404	257/324.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:44
L10	24	(((oxide$1nitride$11oxide OR ONO)) ((oxygen$1rich) SAME nitride)) l9	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:44
L11	9	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) l9	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 14:45
L12	13	("20060261401" | "20080258203" | "6709928" | "20030123307" | "6445030" | "7450423" | "7042054" | "4543707" | "6157426" | "6677213" | "6958511" | "20020154878" | "6818558").PN.	US-PGPUB; USPAT	AND	ON	2012/09/26 14:48
L13	186	257/E29.132.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:04
L14	1	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) l13	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:05

Sandisk Technologies, Inc. - Ex. 1040, Page 000280

L15	2	((oxide$1nitride$11oxide OR ONO) (oxygen$1rich SAME nitride)) l13	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:05
L16	2	((oxide$1nitride$11oxide OR ONO) oxygen$1rich nitride) l13	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
L17	2536	257/E29.309.ccls.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
L18	11	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) l17	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:06
L20	11	((oxide$1nitride$11oxide OR ONO)) (channel SAME (recrystallized adj polysilicon))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:08
L21	20	((oxide$1nitride$11oxide OR ONO)) (channel SAME (silicon adj nano$1wire))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 15:10
L24	1	("20100117138").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:03
L25	1	("6093596").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:22
L26	1	("6093590").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 16:22
L27	2278	((high adj dielectric adj constant) SAME (tantalum adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:28
L28	2278	((high adj dielectric adj constant) SAME (high adj dielectric adj constant) SAME (tantalum adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:29
L29	1480	l28 memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:29
L31	280	(((oxide$1nitride$11oxide OR ONO))) l29	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:30
L32	274	((oxide$1nitride$11oxide OR ONO) nitride) l29	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:31
L33	230	((oxide$1nitride$11oxide OR ONO) nitride) AND l29	US-PGPUB; USPAT;	SAME	ON	2012/09/26 16:31

Sandisk Technologies, Inc. - Ex. 1040, Page 000281

			USOCR			
L35	196	transistor L33	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 16:32
L36	20	((oxide$1nitride$11oxide OR ONO) nitride transistor) AND I29	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 16:32
S1	1	("8063434").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 09:50
S2	18	("20030122204" | "20050230766" | "20060131636" | "20070246753" | "20070262451" | "20070267687" | "20070268753" | "20070272916" | "20080009115" | "20080290399" | "20100041222" | "20100295118" | "6906390" | "6912163" | "7312496" | "7323742" | "7737488" | "7790516").PN. OR ("8063434").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 09:51
S3	19	((IGOR) near2 (POLISHCHUK)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:01
S4	7	("20010012667" | "20030178675" | "20030232507" | "20040082198" | "20100090294" | "20100167506" | "7799670").PN. OR ("8163660").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:04
S5	34	((SAGY) near2 (LEVY)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:05
S6	88	((KRISHNASWAMY) near2 (RAMKUMAR)).INV.	US-PGPUB; USPAT	AND	ON	2012/09/26 10:07
S7	8	("20070029625" | "20070031999" | "20080286927" | "20090039414" | "7315474" | "7576386" | "7636257" | "7646637").PN. OR ("8222688").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:10
S8	78	(S3 OR S5 OR S6) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:19
S9	1	((oxide$1nitride$1nitride$1oxide OR ONNO) NEAR4 stack) ((OPINIONAIDED).AS. OR (CYPRESS).AS.)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:28
S10	1	((oxide$1nitride$1nitride$1oxide OR ONNO) NEAR4 stack)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30
S11	655	((oxide$1nitride$1nitride$1oxide OR ONNO))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30
S12	292	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:30

Sandisk Technologies, Inc. - Ex. 1040, Page 000282

S13	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (oxygen$1rich) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 10:31
S14	0	((oxide$1nitride$1nitride$1oxide OR ONNO)) SAME (oxygen$1rich)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:12
S15	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (oxygen$1rich)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:12
S16	0	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S2	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S17	1	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S8	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S18	1	(((oxide$1nitride$1nitride$1oxide OR ONNO))) S6	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:13
S19	2	(("6906390") or ("6912163")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/26 11:16
S20	29727	((oxide$1nitride$11oxide OR ONO)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S21	135	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S22	59	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich)) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:18
S23	46	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) memory	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:21
S24	46	(((oxide$1nitride$11oxide OR ONO)) SAME (oxygen$1rich) SAME nitride) S23	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:21
S25	41	("4173766" | "5168334" | "5349221" | "5644533" | "5751037" | "5768192" | "5825686" | "5963465" | "5966603" | "6001709" | "6011725" | "6030871" | "6117730" | "6287917" | "6326268").PN. OR ("6465306").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:31
S26	17	((oxide$1nitride$11oxide OR ONO)) (oxygen$1rich) (substrate NEAR4 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:46
S27	6	((oxide$1nitride$11oxide OR ONO))	US-	AND	ON	2012/09/26

Sandisk Technologies, Inc. - Ex. 1040, Page 000283

		(oxygen$1rich) (channel NEAR4 polysilicon)	PGPUB; USPAT; USOCR			11:47
S28	467	((oxide$1nitride$11oxide OR ONO)) (channel NEAR2 polysilicon)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 11:48
S29	60	((oxide$1nitride$11oxide OR ONO)) (channel NEAR2 polysilicon)	US-PGPUB; USPAT; USOCR	SAME	ON	2012/09/26 11:49
S30	91	((oxide$1nitride$1nitride$1oxide OR ONNO)) memory channel	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:02
S31	0	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) Near3 channel))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S32	1	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) NEAR3 substrate))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S33	2	(((oxide$1nitride$1nitride$1oxide OR ONNO)) memory ((poly$1silicon OR polysilican OR poly$1Si) SAME substrate))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:04
S34	3	((oxide$1nitride$1nitride$1oxide OR ONNO)) (OXYGEN same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:16
S35	1	((oxide$1nitride$1nitride$1oxide OR ONNO)) (OXYGEN$1RICH same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:17
S36	256	(OXYGEN$1RICH same NITRIDE)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:19
S37	119	(OXYGEN$1RICH same NITRIDE) MEMORY CHANNEL	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:20
S38	11	(OXYGEN$1RICH same NITRIDE) MEMORY (POLYSILICON near4 CHANNEL)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:20
S39	8	(OXYGEN$1RICH same NITRIDE) MEMORY (logic near4 MOS)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:45
S40	29	("20030227049" | "20040071030" | "20040129986" | "20050186741" | "20060202263" | "20060226490" | "20060281331" | "4843023" | "5405791" | "5573963" | "5793089" | "5861347" | "6025267" | "6074915" | "6174774" | "6277683" | "6429081" | "6599795" | "6730566" | "6946349" | "7015100" |	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:51

Sandisk Technologies, Inc. - Ex. 1040, Page 000284

		"7045424" | "7098154" | "7172940" | "7250654" | "7253046" | "7262457" | "7544565" | "7588986").PN. OR ("8143129").URPN.				
S41	29	("20030227049" | "20040071030" | "20040129986" | "20050186741" | "20060202263" | "20060226490" | "20060281331" | "4843023" | "5405791" | "5573963" | "5793089" | "5861347" | "6025267" | "6074915" | "6174774" | "6277683" | "6429081" | "6599795" | "6730566" | "6946349" | "7015100" | "7045424" | "7098154" | "7172940" | "7250654" | "7253046" | "7262457" | "7544565" | "7588986").PN. OR ("8143129").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:51
S42	20	(PMOS SAME SONOS SAME memory) (NMOS SAME logic)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:58
S43	11	(PMOS SAME SONOS SAME memory) (NMOS SAME logic) (polysilicon adj gate)	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 12:59
S48	5	(high$1K NEAR4 (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 13:23
S49	51	(high$1K SAME (High adj temperature adj oxide))	US-PGPUB; USPAT; USOCR	AND	ON	2012/09/26 13:25

9/ 26/ 2012 5:27:00 PM
C:\ Users\ nyushin\ Documents\ EAST\ Workspaces\ 13539466.wsp

Sandisk Technologies, Inc. - Ex. 1040, Page 000285

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5842

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/539,466	07/01/2012	257	2893	PM07027D1CIP1

APPLICANTS

Igor POLISHCHUK, Fremont, CA;
Sagy LEVY, Zichron-Yoakev, ISRAEL;
Krishnaswamy RAMKUMAR, San Jose, CA;

**** CONTINUING DATA ***************************

This application is a CIP of 13/288,919 11/03/2011
which is a DIV of 12/152,518 05/13/2008 PAT 8,063,434
which claims benefit of 60/940,160 05/25/2007

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

07/16/2012

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/NIKOLAY K YUSHIN/ Examiner's Signature	☐ Initials	CA	13	20	3

ADDRESS

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709
UNITED STATES

TITLE

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

FILING FEE RECEIVED		
1380	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Sandisk Technologies, Inc. - Ex. 1040, Page 000286

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/26/2012								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	O								
	7	O								
	8	O								
	9	O								
	10	O								
	11	=								
	12	=								
	13	=								
	14	=								
	15	=								
	16	=								
	17	=								
	18	=								
	19	=								
	20	=								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13539466	POLISHCHUK ET AL.
	Examiner	**Art Unit**
	NIKOLAY YUSHIN	2893

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
257	314, 324, E29.132; E29.309	09/26/2012	NY

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Keyword, inventor names, assignee searching - see search history	09/26/2012	NY

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

/NIKOLAY YUSHIN/ Examiner.Art Unit 2893	

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/539,466

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/539,466	07/01/2012	2812	1380	PM07027D1CIP1	20	3

CONFIRMATION NO. 5842

UPDATED FILING RECEIPT

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

OC000000055593013

Date Mailed: 07/26/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Igor POLISHCHUK, Fremont, CA;
Sagy LEVY, Zichron-Yoakev, ISRAEL;
Krishnaswamy RAMKUMAR, San Jose, CA;

Assignment For Published Patent Application

CYPRESS SEMICONDUCTOR CORPORATION, San Jose, CA

Power of Attorney: The patent practitioners associated with Customer Number 60909

Domestic Priority data as claimed by applicant

This application is a CIP of 13/288,919 11/03/2011
which is a DIV of 12/152,518 05/13/2008 PAT 8063434
which claims benefit of 60/940,160 05/25/2007

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 07/16/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/539,466**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Sandisk Technologies, Inc. - Ex. 1040, Page 000290

Title

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Preliminary Class

438

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

Sandisk Technologies, Inc. - Ex. 1040, Page 000291

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage, facilitate, and accelerate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	13/539,466	Confirmation No. 5842
In re Application of	:	Igor POLISHCHUK, et al.	
Filed	:	July 1. 2012	
TC/A.U.	:	2812	
Examiner	:	unknown	
Docket No.	:	PM07027D1CIP1	
Customer No.	:	60909	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO MISSING PARTS

Applicant hereby responds to the NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION FILED UNDER 37 C.P.R.§ 1.53(b)- FILING DATE GRANTED mailed July 17, 2012, enclosed please find the declaration and surcharge fee.

Sandisk Technologies, Inc. - Ex. 1040, Page 000293

Should the Patent Office have any questions regarding this response or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry Johnson, by telephone at (650) 207-3418. All correspondence should continue to be directed to the address associated with customer number 60909

The surcharge fee under 37 CFR 1.16(f) is included, and it is believed no fees are required for filing this response. However, if necessary, please *charge any additional fees under 37 CFR §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application,* or apply any credits to our PTO deposit account number: 50-3781.

Respectfully submitted,

Dated: July 19, 2012

By: /William E. Nuttle/
William E. Nuttle, Reg. No. 42,943
Attorney for the Applicant(s)

Sandisk Technologies, Inc. - Ex. 1040, Page 000294

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)		
☐ Declaration Submitted With Initial Filing OR ☒ Declaration Submitted After Initial Filing (surcharge (37 CFR 1.16(f)) required)	Attorney Docket Number	PM07027D1CIP1
	First Named Inventor	Igor Polishchuk
	COMPLETE IF KNOWN	
	Application Number	13/539,466
	Filing Date	July 1, 2012
	Art Unit	
	Examiner Name	

I hereby declare that: (1) Each inventor's residence, mailing address, and citizenship are as stated below next to their name; and (2) I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention titled:

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

(Title of the Invention)

the application of which

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) 07/01/2012 as United States Application Number or PCT International Application Number 13/539,466 and was amended on (MM/DD/YYYY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

Authorization To Permit Access To Application by Participating Offices

☒ If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified patent application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the above-identified patent application is filed to have access to the above-identified patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the above-identified patent application with respect to: 1) the above-identified patent application-as-filed; 2) any foreign application to which the above-identified patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified patent application; and 3) any U.S. application-as-filed from which benefit is sought in the above-identified patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

DECLARATION — Utility or Design Patent Application

Claim of Foreign Priority Benefits

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application number(s) are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

Claim of Provisional Priority Benefits

I hereby claim provisional priority benefits under 35, U.S.C. 119(e) of any United States provisional application(s) listed below.

Prior Provisional Application Number(s)	Country	Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
60/940,160	US	05/25/2007	☐	☐	☒
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

DECLARATION — Utility or Design Patent Application

Claim of Prior Application Priority Benefits

I hereby claim the benefit under Title 35, U.S.C. 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations 1.56, which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Prior Application Number(s)	Country	Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
12/152,518	US	05/13/2008	☐	☐	☒
13/288,919	US	11/03/2011	☐	☐	☒
			☐	☐	☐
			☐	☐	☐

Appointment of Patent Practitioners:

I hereby appoint the patent practitioners associated with the **Customer Number 60909** as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith.

If this patent application is assigned, then the undersigned hereby authorizes the patent attorneys and patent agents named herein to accept and follow instructions from the assignee(s) as to any action to be taken in the United States Patent and Trademark Office regarding this application without direct communication between the patent attorneys and patent agents and the undersigned. In the event of a change in the persons from whom instructions may be taken, at least one patent attorney or patent agent named herein will be so notified by the undersigned.

Direct all correspondence to (check one):

_X_ Customer Number 60909 OR

__ Correspondence Address Below:

CYPRESS SEMICONDUCTOR CORPORATION
198 Champion Court
San Jose, California 95134 U.S.A.
Telephone: (408) 545-7194
Fax: (408) 545-6911

DECLARATION — Utility or Design Patent Application

Direct all correspondence to:	☒	The address associated with Customer Number:	60909	OR ☐ Correspondence address below

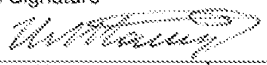
Name		
Cypress Semiconductor Corporation		
Address		
198 Champion Court		
City	State	Zip
San Jose	CA	95134
Country	Telephone	Email
US	408-545-7194	larz@cypress.com

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. Petitioner/applicant is advised that documents which form the record of a patent application (such as the PTO/SB/01) are placed into the Privacy Act system of records DEPARTMENT OF COMMERCE, COMMERCE-PAT-7, System name: *Patent Application Files*. Documents not retained in an application file (such as the PTO-2038) are placed into the Privacy Act system of COMMERCE/PAT-TM-10, System name: *Deposit Accounts and Electronic Funds Transfer Profiles*.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR:	☐ A petition has been filed for this unsigned inventor
Given Name (first and middle [if any])	Family Name or Surname
Igor	Polishchuk

Inventor's Signature	Date
	June 11, 2011

Residence: City	State	Country	Citizenship
Fremont	CA	US	US

Mailing Address			
43355 Paseo Padre Pkwy.			
City	State	Zip	Country
Fremont	CA	94539	US

☒ Additional inventors or a legal representative are being named on the 1 supplemental sheet(s) PTO/SB/02A or 02LR attached hereto

PTO/SB/02A (07-07)
Approved for use through 09/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Sagy		Levy	
Inventor's Signature	Sagy Levy		Date 11-9-10
Zichron-Yoakev Residence: City	State	IL Country	IL Citizenship
66 Yigal-Alon Street Mailing Address			
Zichron-Yoakev City	State	30900 Zip	IL Country

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Krishnaswamy		Ramkumar	
Inventor's Signature			Date
San Jose Residence: City	CA State	US Country	US Citizenship
1193 Lynbrook Way Mailing Address			
San Jose City	CA State	95129 Zip	US Country

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/02A (07-07)
Approved for use through 09/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Sagy	Levy		
Inventor's Signature		Date	
Zichron-Yoakev Residence: City	State	IL Country	IL Citizenship
66 Yigal-Alon Street Mailing Address			
Zichron-Yoakev City	State	30900 Zip	IL Country

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Krishnaswamy	Ramkumar		
Inventor's Signature Krameeee		Date 6/7/2012	
San Jose Residence: City	CA State	US Country	US Citizenship
1193 Lynbrook Way Mailing Address			
San Jose City	CA State	95129 Zip	US Country

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle (if any))	Family Name or Surname		
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	13539466
Filing Date:	01-Jul-2012
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Filer:	William Edward Nuttle
Attorney Docket Number:	PM07027D1CIP1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**130**

Electronic Acknowledgement Receipt

EFS ID:	13297263
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor POLISHCHUK
Customer Number:	60909
Filer:	William Edward Nuttle
Filer Authorized By:	
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	19-JUL-2012
Filing Date:	01-JUL-2012
Time Stamp:	19:34:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$130
RAM confirmation Number	6226
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Applicant Response to Pre-Exam Formalities Notice	PM07027D1CIP1_RESP_MISSING_PARTS.pdf	95149 5a70869a850ceb74889a1d5fc56ef3119ae089b7	no	2
Warnings:					
Information:					
2	Oath or Declaration filed	PM07027D1CIP1_Dec_Signed.pdf	923395 a50be0aa8e8930917017a060a7c604cb97bf4b3c	no	6
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30238 a03aa1dc87ab00004ef188ed2cb2a33ad591ab3d	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1048782	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/539,466	07/01/2012	Igor POLISHCHUK	PM07027D1CIP1

CONFIRMATION NO. 5842

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

FORMALITIES LETTER

OC000000055416561

Date Mailed: 07/17/2012

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $**130** for a non-small entity, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is $**130** for a non-small entity
- $**130** Surcharge.

Sandisk Technologies, Inc. - Ex. 1040, Page 000305

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/smunpanthovong/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Sandisk Technologies, Inc. - Ex. 1040, Page 000306

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/539,466

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/539,466	07/01/2012	2812	1250	PM07027D1CIP1	20	3

CONFIRMATION NO. 5842

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

FILING RECEIPT

OC000000055416560

Date Mailed: 07/17/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Igor POLISHCHUK, Fremont, CA;
Sagy LEVY, Zichron-Yoakev, ISRAEL;
Krishnaswamy RAMKUMAR, San Jose, CA;

Assignment For Published Patent Application

CYPRESS SEMICONDUCTOR CORPORATION, San Jose, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CIP of 13/288,919 11/03/2011
which is a DIV of 12/152,518 05/13/2008 PAT 8063434
which claims benefit of 60/940,160 05/25/2007

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 07/16/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/539,466**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Sandisk Technologies, Inc. - Ex. 1040, Page 000308

Title

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Preliminary Class

438

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

Sandisk Technologies, Inc. - Ex. 1040, Page 000309

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage, facilitate, and accelerate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE

Inventors:

Igor Polishchuk

Sagy Levy

Krishnaswamy Ramkumar

Prepared by:
WILLIAM NUTTLE
P.O. BOX 4240
FOSTER CITY, CALIFORNIA 94404
(650) 207-3404b

Sandisk Technologies, Inc. - Ex. 1040, Page 000311

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of co-pending U.S. application Ser. No. 13/288,919, filed November 3, 2011, which is a divisional of U.S. Application Ser. No. No. 12/152,518, filed on May 13, 2008, now Patent No. 8,063,434, issued on November 22, 2011, which claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 60/940,160, filed May 25, 2007, all of which application are hereby incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] The present invention relates generally to semiconductor devices, and more particularly to integrated circuits including non-volatile semiconductor memories and methods of fabricating the same.

BACKGROUND

[0003] Non-volatile semiconductor memories are devices that can be electrically erased and reprogrammed. One type of non-volatile memory that is widely used for general storage and transfer of data in and between computers and other electronic devices is flash memory, such as a split gate flash memory. A split gate flash memory transistor has an architecture similar to that of a conventional logic transistor, such as Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), in that it also includes a control gate formed over a channel connecting a source and drain in a substrate. However, the memory transistor further includes a memory or charge trapping layer between the control gate and the channel and insulated from both by insulating or

Sandisk Technologies, Inc. - Ex. 1040, Page 000312

dielectric layers. A programming voltage applied to the control gate traps a charge on the charge trapping layer, partially canceling or screening an electric field from the control gate, thereby changing a threshold voltage (V_T) of the transistor and programming the memory cell. During read-out, this shift in V_T is sensed by the presence or absence of current flow through the channel with application of a predetermined read-out voltage. To erase the memory transistor, an erase voltage is applied to the control gate to restore, or reverse the shift in V_T.

[0004] An important measure of merit for flash memories is data retention time, which is the time for which the memory transistor can hold charge or remain programmed without the application of power. The charge stored or trapped in the charge trapping layer decreases over time due to leakage current through the insulating layers, thereby reducing the difference between a programmed threshold voltage (VTP) and an erased threshold voltage (VTE) limiting data retention of the memory transistor.

[0005] One problem with conventional memory transistors and methods of forming the same is that the charge trapping layer typically has poor or decreasing data retention over time, limiting the useful transistor lifetime. Referring to FIG. 1A, if the charge trapping layer is silicon (Si) rich there is a large, initial window or difference between VTP, represented by graph or line 102, and the VTE, represented by line 104, but the window collapse very rapidly in retention mode to an end of life (EOL 106) of less than about 1.E+07 seconds.

[0006] Referring to FIG. 1B, if on the other hand the charge trapping layer is if a high quality nitride layer, that is one having a low stoichiometric concentration of Si, the rate of collapse of the window or Vt slope in retention mode is reduced, but the initial

Sandisk Technologies, Inc. - Ex. 1040, Page 000313

program-erase window is also reduced. Moreover, the slope of Vt in retention mode is still appreciably steep and the leakage path is not sufficiently minimized to significantly improve data retention, thus EOL 106 is only moderately improved.

[0007] Another problem is that increasingly semiconductor memories combine logic transistors, such as MOSFET's, with memory transistors in integrated circuits (ICs) fabricated on a common substrate for embedded memory or System-On-Chip (SOC) applications. Many of the current processes for forming performance of memory transistors are incompatible with those used for fabricating logic transistors.

[0008] Accordingly, there is a need for memory transistors and methods of forming the same that provides improved data retention and increased transistor lifetime. It is further desirable that the methods of forming the memory device are compatible with those for forming logic elements in the same IC formed on a common substrate.

SUMMARY OF THE INVENTION

[0009] The present invention provides a solution to these and other problems, and offers further advantages over conventional memory cells or devices and methods of fabricating the same.

[0010] Generally, the device includes a memory transistor comprising a polysilicon channel region electrically connecting a source region and a drain region formed in a substrate, an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, and a high work function gate electrode formed over a surface of the ONNO stack. In one embodiment, the ONNO stack includes a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second

Sandisk Technologies, Inc. - Ex. 1040, Page 000314

nitride layer disposed above the first nitride layer. In another embodiment, the multi-layer charge-trapping region further includes an oxide anti-tunneling layer separating the first nitride layer from the second nitride layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] These and various other features and advantages of the present invention will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

[0012] FIG. 1A is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a large initial difference between programming and erase voltages but which loses charge quickly;

[0013] FIG. 1B is a graph showing data retention for a memory transistor using a charge storage layer formed according to a conventional method and having a smaller initial difference between programming and erase voltages;

[0014] FIGs. 2A through 2D are partial cross-sectional side views of a semiconductor device illustrating a process flow for forming a semiconductor device including a logic transistor and non-volatile memory transistor according to an embodiment of the present invention;

[0015] FIG. 3 is a partial cross-sectional side view of a semiconductor device including a logic transistor and non-volatile memory transistor comprising high work function gate electrodes according to an embodiment of the present invention;

[0016] FIGs. 4A and 4B illustrates a cross-sectional view of a non-volatile memory device including an ONONO stack;

Sandisk Technologies, Inc. - Ex. 1040, Page 000315

[0017] FIG. 5 depicts a flowchart representing a series of operations in a method for fabricating a non-volatile charge trap memory device including an ONONO stack, in accordance with an embodiment of the present invention;

[0018] FIG. 6A illustrates a non-planar multigate device including a multi-layer charge-trapping region;

[0019] FIG. 6B illustrates a cross-sectional view of the non-planar multigate device of FIG. 6A;

[0020] FIGs. 7A and 7B illustrate a non-planar multigate device including a multi-layer charge-trapping region and a horizontal nanowire channel;

[0021] FIG. 7C illustrates a cross-sectional view of a vertical string of non-planar multigate devices of FIG. 7A;

[0022] FIGs. 8A and 8B illustrate a non-planar multigate device including a multi-layer charge-trapping region and a vertical nanowire channel;

[0023] FIGs. 9A through 9F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 8A; and

[0024] FIGs. 10A through 10F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 8A.

DETAILED DESCRIPTION

[0025] The present invention is directed generally to non-volatile memory transistor including a multi-layer charge storage layer and high work function gate electrode to increase data retention and/or to improve programming time and efficiency. The structure and method are particularly useful for embedded memory or System-On-

Sandisk Technologies, Inc. - Ex. 1040, Page 000316

Chip (SOC) applications in which a semiconductor device includes both a logic transistor and non-volatile memory transistor comprising high work function gate electrodes formed on a common substrate.

[0026] In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures, and techniques are not shown in detail or are shown in block diagram form in order to avoid unnecessarily obscuring an understanding of this description.

[0027] Reference in the description to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification do not necessarily all refer to the same embodiment. The term "to couple" as used herein may include both to directly connect and to indirectly connect through one or more intervening components.

[0028] Briefly, a non-volatile memory transistor according to the present invention includes a high work function gate electrode formed over an oxide-nitride-oxide (ONO) dielectric stack. By high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased.

[0029] In certain preferred embodiments, the high work function gate electrode comprises a doped polycrystalline silicon or polysilicon (poly) layer, the fabrication of which can be can be readily integrated into standard complementary metal-oxide-

Sandisk Technologies, Inc. - Ex. 1040, Page 000317

semiconductor (CMOS) process flows, such as those used fabricate metal-oxide-semiconductor (MOS) logic transistors, to enable fabrication of semiconductor memories or devices including both memory and logic transistors. More preferably, the same doped polysilicon layer can also be patterned to form a high work function gate electrode for the MOS logic transistor, thereby improving the performance of the logic transistor and increasing the efficiency of the fabrication process. Optionally, the ONO dielectric stack includes a multi-layer charge storage or charge trapping layer to further improve performance, and in particular data retention, of the memory transistor.

[0030] A semiconductor device including a non-volatile memory transistor comprising a high work function gate electrode and methods of forming the same will now be described in detail with reference to FIGs. 2A through 2D, which are partial cross-sectional side views of intermediate structures illustrating a process flow for forming a semiconductor device including both memory and logic transistors. For purposes of clarity, many of the details of semiconductor fabrication that are widely known and are not relevant to the present invention have been omitted from the following description.

[0031] Referring to FIG. 2, fabrication of the semiconductor device begins with formation of an ONO dielectric stack 202 over a surface 204 of a wafer or substrate 206. Generally, the ONO dielectric stack 202 includes a thin, lower oxide layer or tunneling oxide layer 208 that separates or electrically isolates a charge trapping or storage layer 210 from a channel region (not shown) of the memory transistor in the substrate 206, and a top or blocking oxide layer 212. Preferably, as noted above and as shown in FIGs. 2A-2D, the charge storage layer 210 is a multi-layer charge storage layer including at least a

Sandisk Technologies, Inc. - Ex. 1040, Page 000318

top, charge trapping oxynitride layer 210A and a lower, substantially trap free oxynitride layer 210B.

[0032] Generally, the substrate 206 may include any known silicon-based semiconductor material including silicon, silicon-germanium, silicon-on-insulator, or silicon-on-sapphire substrate. Alternatively, the substrate 206 may include a silicon layer formed on a non-silicon-based semiconductor material, such as gallium-arsenide, germanium, gallium-nitride, or aluminum-phosphide. Preferably, the substrate 206 is a doped or undoped silicon substrate.

[0033] The lower oxide layer or tunneling oxide layer 208 of the ONO dielectric stack 202 generally includes a relatively thin layer of silicon dioxide (SiO_2) of from about 15 angstrom (Å) to about 22 Å, and more preferably about 18 Å. The tunneling oxide layer 208 can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using chemical vapor deposition (CVD). In a preferred embodiment, the tunnel dielectric layer is formed or grown using a steam anneal. Generally, the process includes a wet-oxidizing method in which the substrate 206 is placed in a deposition or processing chamber, heated to a temperature from about 700°C to about 850°C, and exposed to a wet vapor for a predetermined period of time selected based on a desired thickness of the finished tunneling oxide layer 208. Exemplary process times are from about 5 to about 20 minutes. The oxidation can be performed at atmospheric or at low pressure.

[0034] In a preferred embodiment, the oxynitride layers 210A, 210B, of the multi-layer charge storage layer 210 are formed or deposited in separate steps utilizing different processes and process gases or source materials, and have an overall or

Sandisk Technologies, Inc. - Ex. 1040, Page 000319

combined thickness of from about 70 Å to about 150 Å, and more preferably about 100 Å. The lower, trap free oxynitride layer 210B can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a process gas including a silicon source, such as silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane (SiH_2Cl_2), tetrachlorosilane ($SiCl_4$), a nitrogen source, such as nitrogen (N_2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas, such as oxygen (O_2) or N_2O. In one embodiment the trap free oxynitride layer 210B is deposited in a low pressure CVD process using a process gas including dichlorosilane, NH_3 and N_2O, while maintaining the chamber at a pressure of from about 5 millitorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm).

[0035] The top, charge trapping oxynitride layer 210A can be deposited over the bottom oxynitride layer 210B in a CVD process using a process gas including Bis-TertiaryButylAminoSilane (BTBAS). It has been found that the use of BTBAS increases the number of deep traps formed in the oxynitride by increasing the carbon level in the charge trapping oxynitride layer 210A. Moreover, these deep traps reduce charge losses due to thermal emission, thereby further improving data retention. More preferably, the process gas includes BTBAS and ammonia (NH_3) mixed at a predetermined ratio to

Sandisk Technologies, Inc. - Ex. 1040, Page 000320

provide a narrow band gap energy level in the oxynitride charge trapping layer. In particular, the process gas can include BTBAS and NH_3 mixed in a ratio of from about 7:1 to about 1:7. For example, in one embodiment the charge trapping oxynitride layer 210A is deposited in a low pressure CVD process using BTBAS and ammonia NH_3 at a chamber pressure of from about 5 mT to about 500 mT, and at a substrate temperature of from about 700°C to about 850°C and more preferably at least about 780°C, for a period of from about 2.5 minutes to about 20 minutes.

[0036] It has been found that an oxynitride layer produced or deposited under the above conditions yields a trap-rich oxynitride layer 210A, which improves the program and erase speed and increases of the initial difference (window) between program and erase voltages without compromising a charge loss rate of the memory transistor, thereby extending the operating life (EOL) of the device. Preferably, the charge trapping oxynitride layer 210A has a charge trap density of at least about $1E10/cm^2$, and more preferably from about $1E12/cm^2$ to about $1E14/cm^2$.

[0037] Alternatively, the charge trapping oxynitride layer 210A can be deposited over the bottom oxynitride layer 210B in a CVD process using a process gas including BTBAS and substantially not including ammonia (NH_3). In this alternative embodiment of the method, the step of depositing the top, charge trapping oxynitride layer 210A is followed by a thermal annealing step in a nitrogen atmosphere including nitrous oxide (N_2O), NH_3, and/or nitrogen oxide (NO).

[0038] Preferably, the top, charge trapping oxynitride layer 210A is deposited sequentially in the same CVD tool used to form the bottom, trap free oxynitride layer 210B, substantially without breaking vacuum on the deposition chamber. More

Sandisk Technologies, Inc. - Ex. 1040, Page 000321

preferably, the charge trapping oxynitride layer 210A is deposited substantially without altering the temperature to which the substrate 206 was heated during deposition of the trap free oxynitride layer 210B.

[0039] A suitable thickness for the lower, trap free oxynitride layer 210B has been found to be from about 10 Å to about 80 Å, and a ratio of thicknesses between the bottom layer and the top, charge trapping oxynitride layer has been found to be from about 1:6 to about 6:1 , and more preferably at least about 1:4.

[0040] The top oxide layer 212 of the ONO dielectric stack 202 includes a relatively thick layer of SiO_2 of from about 20 Å to about 70 Å, and more preferably about 45 Å. The top oxide layer 212 can be formed or deposited by any suitable means including, for example, being thermally grown or deposited using CVD. In a preferred embodiment, the top oxide layer 212 is a high-temperature-oxide (HTO) deposited using CVD process. Generally, the deposition process includes exposing the substrate 306 to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-containing gas, such as O_2 or N_2O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

[0041] Preferably, the top oxide layer 212 is deposited sequentially in the same tool used to form the oxynitride layers 210A, 210B. More preferably, the oxynitride layers 210A, 210B, and the top oxide layer 212 are formed or deposited in the same tool used to grow the tunneling oxide layer 208. Suitable tools include, for example, an ONO AVP, commercially available from AVIZA technology of Scotts Valley, California.

Sandisk Technologies, Inc. - Ex. 1040, Page 000322

[0042] Referring to FIG. 2B, in those embodiments in which the semiconductor device is to further include a logic transistor, such as a MOS logic transistor, formed on the surface of the same substrate the ONO dielectric stack 202 is removed from a region or area of the surface 204 in which the logic transistor is to be formed, and an oxide layer 214 the formed thereon.

[0043] Generally, the ONO dielectric stack 202 is removed from the desired region or area of the surface 204 using standard photolithographic and oxide etch techniques. For example, in one embodiment a patterned mask layer (not shown) is formed from a photo-resist deposited on the ONO dielectric stack 202, and the exposed region etched or removed using a low pressure radiofrequency (RF) coupled or generated plasma comprising fluorinated hydrocarbon and/or fluorinated carbon compounds, such as $C_2H_2F_4$ commonly referred to as Freon®. Generally, the processing gas further includes argon (Ar) and nitrogen (N_2) at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

[0044] The oxide layer 214 of the logic transistor can include a layer of SiO_2 having a thickness of from about 30 to about 70 Å, and can be thermally grown or deposited using CVD. In one embodiment, the oxide layer 214 is thermally grown using a steam oxidation process, for example, by maintaining the substrate 206 in a steam atmosphere at a temperature of from about 650°C to about 850°C for a period of from about 10 minutes to about 120 minutes.

[0045] Next, a doped polysilicon layer is formed on a surface of the ONO dielectric stack 202 and, preferably, the oxide layer 214 of the logic transistor. More preferably, the substrate 206 is a silicon substrate or has a silicon surface on which the

Sandisk Technologies, Inc. - Ex. 1040, Page 000323

ONO dielectric stack is formed to form a silicon-oxide-nitride-oxide-silicon (SONOS) gate stack of a SONOS memory transistor.

[0046] Referring to FIG. 2C, forming of the doped polysilicon layer begins with the deposition of a conformal polysilicon layer 216 having a thickness of from about 200 Å to about 2000 Å over the ONO dielectric stack 202 and the oxide layer 214. The polysilicon layer 216 can be formed or deposited by any suitable means including, for example, deposition in a low pressure CVD process using a silicon source or precursor. In one embodiment the polysilicon layer 216 is deposited in a low pressure CVD process using a silicon containing process gas, such as silane or dichlorosilane, and N_2, while maintaining the substrate 206 in a chamber at a pressure of from about 5 to 500 mT, and at a temperature of from about 600°C to about 1000°C for a period of from about 20 minutes to about 100 minutes to a substantially undoped polysilicon layer. The polysilicon layer 216 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or difluoroborane (BF_2) to the CVD chamber during the low pressure CVD process.

[0047] In one embodiment, the polysilicon layer 216 is doped following the growth or formation in the LPCVD process using ion implantation process. For example, the polysilicon layer 216 can be doped by implanting boron (B^+) or BF_2 ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) SONOS memory transistor and, preferably, a P-type (PMOS) logic transistor having high work function gate electrodes. More preferably, the polysilicon layer 216 is doped to a concentration or dose selected so

Sandisk Technologies, Inc. - Ex. 1040, Page 000324

that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV.

[0048] Alternatively, the polysilicon layer 216 can be doped by ion implantation after patterning or etching the polysilicon layer and the underlying dielectric layers. It will be appreciated that this embodiment includes additional masking steps to protect exposed areas of the substrate 206 surface 204 and/or the dielectric layers from receiving undesired doping. However, generally such a masking step is included in existing process flows regardless of whether the implantation occurs before or after patterning.

[0049] Referring to FIG. 2D, the polysilicon layer 216 and the underlying dielectric stack 202 and oxide layer 214 are patterned or etched to form high work function gate electrodes 218 of the memory transistor 220 and logic transistor 222. In one embodiment polysilicon layer 216 can be etched or patterned using a plasma comprising hydrobromic acid (HBr), chlorine (CL_2) and/or oxygen (O_2) at a pressure of about 25 mTorr, and a power of about 450 W. The oxide layers 208, 212, 214, and oxynitride layers 210A, 210B, can be etched using standard photolithographic and oxide etch techniques as described. For example, in one embodiment the patterned polysilicon layer 216 is used as a mask, and the exposed oxide layers 208, 212, 214, and oxynitride layers 210A, 210B, etched or removed using low pressure RF plasma. Generally, the plasma is formed from a processing gas comprising a fluorinated hydrocarbon and/or fluorinated carbon compounds, and further including Ar and N_2 at flow rates selected to maintain a pressure in the etch chamber of from about 50 mT to about 250 mT during processing.

[0050] Finally, the substrate is thermal annealed with a single or multiple annealing steps at a temperature of from about 800 °C to about 1050 °C for a time of

Sandisk Technologies, Inc. - Ex. 1040, Page 000325

from about 1second to about 5 minutes to drive in ions implanted in the polysilicon layer 216, and to repair damage to the crystal structure of the polysilicon layer caused by ion implantation. Alternatively, advanced annealing techniques, such as flash and laser, can be employed with temperatures as high as 1350 °C and anneal times as low as 1 millisecond.

[0051] A partial cross-sectional side view of a semiconductor device 300 including a logic transistor 302 and non-volatile memory transistor 304 comprising high work function gate electrodes according to an embodiment of the present invention is shown in FIG. 3. Referring to FIG. 3, the memory transistor 304 is formed on a silicon substrate 306 and comprises a high work function gate electrode 308 formed from a doped polysilicon layer overlying a dielectric stack 310. The dielectric stack 310 overlies and controls current through a channel region 312 separating heavily doped source and drain (S/D) regions 314. Preferably, the dielectric stack 310 includes a tunnel dielectric layer 316, a multi-layer charge storage layer 318A, 318B, and a top or blocking oxide layer 320. More preferably, the multi-layer charge storage layer 318A, 318B, includes at least a top, charge trapping oxynitride layer 318A and a lower, substantially trap free oxynitride layer 318B. Optionally, as shown in FIG. 3, the memory transistor 304 further includes one or more sidewall spacers 322 surrounding the gate stack to electrically insulate it from contacts (not shown) to the S/D regions 320 and from other transistors in the semiconductor device formed on the substrate 306.

[0052] The logic transistor 302 comprises a gate electrode 324 overlying an oxide layer 326 formed over a channel region 328 separating heavily doped source and drain regions 330, and, optionally, can include one or more sidewall spacers 332 surrounding

Sandisk Technologies, Inc. - Ex. 1040, Page 000326

the gate electrically insulate it from contacts (not shown) to the S/D regions. Preferably, as shown in FIG. 3, the gate electrode 324 of the logic transistor 302 also comprises a high work function gate electrode formed from a doped polysilicon layer.

[0053] Generally, the semiconductor device 300 further includes a number of isolation structures 334, such as a local oxidation of silicon (LOCOS) region or structure, a field oxidation region or structure (FOX), or a shallow trench isolation (STI) structure to electrically isolate individual transistors formed on the substrate 306 from one another.

Implementations and Alternatives

[0054] In one aspect the present disclosure is directed to semiconductor devices including memory transistors with a high work function gate electrode and a multi-layer charge-trapping region. FIG. 4A is a block diagram illustrating a cross-sectional side view of an embodiment of one such memory transistor 400. The memory transistor 400 includes a ONNO stack 402 including an ONNO structure 404 formed over a surface 406 of a substrate 408. Substrate 408 includes one or more diffusion regions 410, such as source and drain regions, aligned to the gate stack 402 and separated by a channel region 412. Generally, the ONNO stack 402 includes a high work function gate electrode 414 formed upon and in contact with the ONNO structure 404. The high work function gate electrode 414 is separated or electrically isolated from the substrate 408 by the ONNO structure 404. The ONNO structure 404 includes a thin, lower oxide layer or tunnel dielectric layer 416 that separates or electrically isolates the ONNO stack 402 from the channel region 412, a top or blocking dielectric layer 420, and a multi-layer charge-trapping region 422.

Sandisk Technologies, Inc. - Ex. 1040, Page 000327

[0055] The nanowire channel region 412 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 412 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[0056] The high work function gate electrode 414 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. As noted above, the polysilicon layer of the high work function gate electrode 414 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or difluoroborane (BF_2) to the CVD chamber during the low pressure CVD process, or can be doped following the growth or formation in the CVD process using an ion implantation process. In either embodiment, the polysilicon layer of the high work function gate electrode 414 is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 414 is doped by implanting boron (B^+) or BF_2 ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) memory transistor.

[0057] The tunnel dielectric layer 416 may be any material and have any thickness suitable to allow charge carriers to tunnel into the multi-layer charge-trapping region 422 under an applied gate bias while maintaining a suitable barrier to leakage when the memory transistor 400 is unbiased. In one embodiment, the tunnel dielectric layer 416 is formed by a thermal oxidation process and is composed of silicon dioxide or

Sandisk Technologies, Inc. - Ex. 1040, Page 000328

silicon oxy-nitride, or a combination thereof. In another embodiment, the tunnel dielectric layer 416 is formed by chemical vapor deposition (CVD) or atomic layer deposition (ALD) and is composed of a dielectric layer which may include, but is not limited to, silicon nitride, hafnium oxide, zirconium oxide, hafnium silicate, hafnium oxy-nitride, hafnium zirconium oxide and lanthanum oxide. In a specific embodiment, the tunnel dielectric layer 416 has a thickness in the range of 1-10 nanometers. In a particular embodiment, the tunnel dielectric layer 416 has a thickness of approximately 2 nanometers.

[0058] In one embodiment, the blocking dielectric layer 420 comprises a high temperature oxide (HTO). The higher quality HTO oxide enables the blocking dielectric layer 420 to be scaled in thickness. In an exemplary embodiment, the thickness of the blocking dielectric layer 420 comprising a HTO oxide is between 2.5 nm and 10.0 nm.

[0059] In another embodiment, the blocking dielectric layer 420 is further modified to incorporate nitrogen. In one such embodiment, the nitrogen is incorporated in the form of an ONO stack across the thickness of the blocking dielectric layer 420. Such a sandwich structure in place of the conventional pure oxygen blocking dielectric layer advantageously reduces the EOT of the entire stack 402 between the channel region 412 and high work function gate electrode 414 as well as enable tuning of band offsets to reduce back injection of carriers. The ONO stack blocking dielectric layer 420 can then be incorporated with the tunnel dielectric layer 416 and the multi-layer charge trapping layer 422 comprising an oxygen-rich first nitride layer 422a, an oxygen-lean second nitride layer 422b and an anti-tunneling layer 422c.

Sandisk Technologies, Inc. - Ex. 1040, Page 000329

[0060] The multi-layer charge-trapping region 422 generally includes at least two nitride layers having differing compositions of silicon, oxygen and nitrogen, including an oxygen-rich, first nitride layer 422a, and a silicon-rich, nitrogen-rich, and oxygen-lean second nitride layer 422b, a silicon-rich. In some embodiments, such as that shown in FIG. 4B, the multi-layer charge-trapping region further includes an anti-tunneling layer 422c comprising an oxide, such as silicon dioxide, separating the oxygen-lean second nitride layer 422b from the oxygen-rich, first nitride layer 422a, to provide a ONONO stack 402 including an ONONO structure 404.

[0061] It has been found that an oxygen-rich, first nitride layer 422a decreases the charge loss rate after programming and after erase, which is manifested in a small voltage shift in the retention mode, while a silicon-rich, nitrogen-rich, and oxygen-lean second nitride layer 422b improves the speed and increases of the initial difference between program and erase voltage without compromising a charge loss rate of memory transistors made using an embodiment of the silicon-oxide-oxynitride-oxide-silicon structure, thereby extending the operating life of the device.

[0062] It has further been found the anti-tunneling layer 422c substantially reduces the probability of electron charge that accumulates at the boundaries of the oxygen-lean second nitride layer 422b during programming from tunneling into the first nitride layer 422a, resulting in lower leakage current than for a conventional non-volatile memory transistor.

[0063] The multi-layer charge-trapping region can have an overall thickness of from about 50 Å to about 150 Å, and in certain embodiments less than about 100 Å, with

Sandisk Technologies, Inc. - Ex. 1040, Page 000330

the with the thickness of the anti-tunneling layer 422c being from about 5 Å to about 20 Å, and the thicknesses of the nitride layers 404b, 404a, being substantially equal.

[0064] A method or forming or fabricating a semiconductor device including a memory transistor with a high work function gate electrode and a multi-layer charge-trapping region according to one embodiment will now be described with reference to the flowchart of FIG. 5.

[0065] Referring to FIG. 5, the method begins with forming a tunnel dielectric layer, such as a first oxide layer, over a silicon containing layer on a surface of a substrate (500). The tunnel dielectric layer can be formed or deposited by any suitable means, including a plasma oxidation process, In-Situ Steam Generation (ISSG) or a radical oxidation process. In one embodiment, the radical oxidation process involves flowing hydrogen (H_2) and oxygen (O_2) gas into a processing chamber or furnace to effect growth of a the tunnel dielectric layer by oxidation consumption of a portion of the substrate.

[0066] Next, an oxygen-rich first nitride layer of the multi-layer charge-trapping region is formed on a surface of the tunnel dielectric layer (502). In one embodiment, the oxygen-rich first nitride layer is formed or deposited in a low pressure CVD process using a silicon source, such as silane (SiH_4), chlorosilane (SiH_3Cl), dichlorosilane or DCS (SiH_2Cl_2), tetrachlorosilane ($SiCl_4$) or Bis-TertiaryButylAmino Silane (BTBAS), a nitrogen source, such as nitrogen (N_2), ammonia (NH_3), nitrogen trioxide (NO_3) or nitrous oxide (N_2O), and an oxygen-containing gas, such as oxygen (O_2) or N_2O. Alternatively, gases in which hydrogen has been replaced by deuterium can be used, including, for example, the substitution of deuterated-ammonia (ND_3) for NH_3. The substitution of deuterium for hydrogen advantageously passivates Si dangling bonds at

Sandisk Technologies, Inc. - Ex. 1040, Page 000331

the silicon-oxide interface, thereby increasing an NBTI (Negative Bias Temperature Instability) lifetime of the devices.

[0067] For example, the lower or oxygen-rich first nitride layer can be deposited over the tunnel dielectric layer by placing the substrate in a deposition chamber and introducing a process gas including N_2O, NH_3 and DCS, while maintaining the chamber at a pressure of from about 5 milliTorr (mT) to about 500 mT, and maintaining the substrate at a temperature of from about 700 degrees Celsius to about 850 degrees Celsius and in certain embodiments at least about 760 degrees Celsius, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 200 standard cubic centimeters per minute (sccm). It has been found that an oxynitride layer produced or deposited under these condition yields a silicon-rich, oxygen-rich first nitride layer.

[0068] Next, an anti-tunneling layer is formed or deposited on a surface of the first nitride layer (504). As with the tunnel dielectric layer, the anti-tunneling layer can be formed or deposited by any suitable means, including a plasma oxidation process, In-Situ Steam Generation (ISSG) or a radical oxidation process. In one embodiment, the radical oxidation process involves flowing hydrogen (H_2) and oxygen (O_2) gas into a batch-processing chamber or furnace to effect growth of the anti-tunneling layer by oxidation consumption of a portion of the first nitride layer.

[0069] The top or oxygen-lean second nitride layer of the multi-layer charge-trapping region is then formed on a surface of the anti-tunneling layer (506). The oxygen-

Sandisk Technologies, Inc. - Ex. 1040, Page 000332

lean second nitride layer can be deposited over the anti-tunneling layer in a CVD process using a process gas including N_2O, NH_3 and DCS, at a chamber pressure of from about 5 mT to about 500 mT, and at a substrate temperature of from about 700 degrees Celsius to about 850 degrees Celsius and in certain embodiments at least about 760 degrees Celsius, for a period of from about 2.5 minutes to about 20 minutes. In particular, the process gas can include a first gas mixture of N_2O and NH_3 mixed in a ratio of from about 8:1 to about 1:8 and a second gas mixture of DCS and NH_3 mixed in a ratio of from about 1:7 to about 7:1, and can be introduced at a flow rate of from about 5 to about 20 sccm. It has been found that a nitride layer produced or deposited under these condition yields a silicon-rich, nitrogen-rich, and oxygen-lean second nitride layer, which improves the speed and increases of the initial difference between program and erase voltage without compromising a charge loss rate of memory transistors made using an embodiment of the silicon-oxide-oxynitride-oxide-silicon structure, thereby extending the operating life of the device.

[0070] In some embodiments, the oxygen-lean second nitride layer can be deposited over the anti-tunneling layer in a CVD process using a process gas including BTBAS and ammonia (NH_3) mixed at a ratio of from about 7:1 to about 1:7 to further include a concentration of carbon selected to increase the number of traps therein. The selected concentration of carbon in the second oxynitride layer can include a carbon concentration of from about 5% to about 15%.

[0071] Next, a top, blocking oxide layer or blocking dielectric layer is formed on a surface of the oxygen-lean second nitride layer of the multi-layer charge-trapping region (508). As with the tunnel dielectric layer and the anti-tunneling layer the blocking

Sandisk Technologies, Inc. - Ex. 1040, Page 000333

dielectric layer can be formed or deposited by any suitable means, including a plasma oxidation process, In-Situ Steam Generation (ISSG) or a radical oxidation process. In one embodiment, the blocking dielectric layer comprises a high-temperature-oxide (HTO) deposited using CVD process. Generally, the deposition process includes exposing the substrate 306 to a silicon source, such as silane, chlorosilane, or dichlorosilane, and an oxygen-containing gas, such as O_2 or N_2O in a deposition chamber at a pressure of from about 50 mT to about 1000 mT, for a period of from about 10 minutes to about 120 minutes while maintaining the substrate at a temperature of from about 650°C to about 850°C.

[0072] Alternatively, the blocking dielectric layer is formed using an ISSG oxidation process. In one embodiment, the ISSG is performed in an RTP chamber, such as the ISSG chamber from Applied Materials described above, at pressures of from about 8 to 12 Torr and a temperature of about 1050 °C with an oxygen rich gas mixture hydrogen to which from about 0.5% to 33% hydrogen has been added.

[0073] It will be appreciated that in either embodiment the thickness of the second nitride layer may be adjusted or increased as some of the oxygen-lean second nitride layer will be effectively consumed or oxidized during the process of forming the blocking dielectric layer.

[0074] Finally, a high work function gate electrode is formed upon and in contact with the blocking dielectric layer (510). The high work function gate electrode includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. As noted above, the polysilicon layer of the high work function gate electrode can be formed or grown directly as a doped

Sandisk Technologies, Inc. - Ex. 1040, Page 000334

polysilicon layer through the addition of gases such as phosphine, arsine, diborane or difluoroborane (BF_2) to the CVD chamber during the low pressure CVD process, or can be doped following the growth or formation in the CVD process using an ion implantation process. In either embodiment, the polysilicon layer of the high work function gate electrode is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode is doped by implanting boron (B^+) or BF_2 ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) memory transistor.

[0075] With the completion of the gate stack fabrication, further processing may occur as known in the art to conclude fabrication of a SONOS-type memory device.

[0076] In another aspect the present disclosure is also directed to multigate or multigate-surface memory transistors including charge-trapping regions overlying two or more sides of a channel region formed on or above a surface of a substrate, and methods of fabricating the same. Multigate devices include both planar and non-planar devices. A planar multigate device (not shown) generally includes a double-gate planar device in which a number of first layers are deposited to form a first gate below a subsequently formed channel region, and a number of second layers are deposited thereover to form a second gate. A non-planar multigate device generally includes a horizontal or vertical channel region formed on or above a surface of a substrate and surrounded on three or more sides by a gate.

Sandisk Technologies, Inc. - Ex. 1040, Page 000335

[0077] FIG. 6A illustrates one embodiment of a non-planar multigate memory transistor including with a high work function gate electrode. Referring to FIG. 6A, the memory transistor 600, commonly referred to as a finFET, includes a channel region 602 formed from a thin film or layer of semiconducting material overlying a surface 604 on a substrate 606 connecting a source region 608 and a drain region 610 of the memory transistor. The channel region 602 is enclosed on three sides by a fin which forms a gate 612 of the device. The thickness of the gate 612 (measured in the direction from source region to drain region) determines the effective channel region length of the device. As with the embodiments described above, the channel region 602 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 602 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[0078] In accordance with the present disclosure, the non-planar multigate memory transistor 600 of FIG. 6A can include a high work function gate electrode and a multi-layer charge-trapping region. FIG. 6B is a cross-sectional view of a portion of the non-planar memory transistor of FIG. 6A including a portion of the substrate 606, channel region 602 and the gate 612 illustrating a high work function gate electrode 614 and a multi-layer charge-trapping region 616. The gate 612 further includes a tunnel dielectric layer 618 overlying a raised channel region 602, and a blocking dielectric layer 620 overlying the blocking dielectric layer to form a control gate of the memory transistor 600. The channel region 602 and gate 612 can be formed directly on substrate 606 or on an insulating or dielectric layer 622, such as a buried oxide layer, formed on or over the substrate.

Sandisk Technologies, Inc. - Ex. 1040, Page 000336

[0079] As with the embodiments described above, the high work function gate electrode 614 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. The polysilicon layer of the high work function gate electrode 614 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, and is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 614 is doped to a concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2}.

[0080] Referring to FIG. 6B, the multi-layer charge-trapping region 616 includes at least one lower or bottom oxygen-rich first nitride layer 616a including nitride closer to the tunnel dielectric layer 618, and an upper or top oxygen-lean second nitride layer 616b overlying the oxygen-rich first nitride layer. Generally, the oxygen-lean second nitride layer 616b includes a silicon-rich, oxygen-lean nitride layer and includes a majority of a charge traps distributed in the multi-layer charge-trapping region, while the oxygen-rich first nitride layer 616a includes an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the oxygen-lean second nitride layer to reduce the number of charge traps therein. By oxygen-rich it is meant wherein a concentration of oxygen in the oxygen-rich first nitride layer 616a is from about 15 to about 40%, whereas a concentration of oxygen in oxygen-lean second nitride layer 616b is less than about 5%.

[0081] In one embodiment, the blocking dielectric 620 also includes an oxide, such as an HTO, to provide an ONNO structure. The channel region 602 and the

Sandisk Technologies, Inc. - Ex. 1040, Page 000337

overlying ONNO structure can be formed directly on a silicon substrate 606 and overlaid with a high work function gate electrode 614 to provide a SONNOS structure.

[0082] In some embodiments, such as that shown in FIG. 6B, the multi-layer charge-trapping region 616 further includes at least one thin, intermediate or anti-tunneling layer 616c including a dielectric, such as an oxide, separating the oxygen-lean second nitride layer 616b from the oxygen-rich first nitride layer 616a. As noted above, the anti-tunneling layer 616c substantially reduces the probability of electron charge that accumulates at the boundaries of the oxygen-lean second nitride layer 616b during programming from tunneling into the first nitride layer 616a.

[0083] As with the embodiments described above, either or both of the oxygen-rich first nitride layer 616a and the oxygen-lean second nitride layer 616b can include silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The oxygen-lean second nitride layer 616b has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the oxygen-rich first nitride layer 616a, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

[0084] In those embodiments including an intermediate or anti-tunneling layer 616c including oxide, the anti-tunneling layer can be formed by oxidation of the bottom oxynitride layer, to a chosen depth using radical oxidation. Radical oxidation may be

Sandisk Technologies, Inc. - Ex. 1040, Page 000338

performed, for example, at a temperature of 1000-1100 degrees Celsius using a single wafer tool, or 800-900 degrees Celsius using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0085] Finally, in those embodiments including a blocking dielectric 620 including oxide the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of the blocking dielectric 620 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric 620 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the top nitride thickness may be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer. A third option is to oxidize the second nitride layer to a chosen depth using radical oxidation.

[0086] A suitable thickness for the oxygen-rich first nitride layer 616a may be from about 30Å to about 160Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 616c. A suitable thickness for the oxygen-lean second nitride layer 616b may be at least 30Å. In certain embodiments, the oxygen-lean second nitride layer 616b may be formed up to 130Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric 620. A ratio of thicknesses between the oxygen-rich first nitride layer 616a and oxygen-lean second nitride layer 616b is approximately 1:1 in some embodiments, although other ratios are also possible.

Sandisk Technologies, Inc. - Ex. 1040, Page 000339

[0087] In other embodiments, either or both of the oxygen-lean second nitride layer 616b and the blocking dielectric 620 may include a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0088] In another embodiment, shown in FIGs. 7A and 7B, the memory transistor can include a nanowire channel region formed from a thin film of semiconducting material overlying a surface on a substrate connecting a source region and a drain region of the memory transistor. By nanowire channel region it is meant a conducting channel region formed in a thin strip of crystalline silicon material, having a maximum cross-sectional dimension of about 10 nanometers (nm) or less, and more preferably less than about 6 nm.

[0089] Referring to FIG. 7A, the memory transistor 700 includes a horizontal nanowire channel region 702 formed from a thin film or layer of semiconducting material on or overlying a surface on a substrate 706, and connecting a source region 708 and a drain region 710 of the memory transistor. In the embodiment shown, the device has a gate-all-around (GAA) structure in which the nanowire channel region 702 is enclosed on all sides by a gate 712 of the device. The thickness of the gate 712 (measured in the direction from source region to drain region) determines the effective channel region length of the device. As with the embodiments described above, the nanowire channel region 702 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 702 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

Sandisk Technologies, Inc. - Ex. 1040, Page 000340

[0090] In accordance with the present disclosure, the non-planar multigate memory transistor 700 of FIG. 7A can include a high work function gate electrode and a multi-layer charge-trapping region. FIG. 7B is a cross-sectional view of a portion of the non-planar memory transistor of FIG. 7A including a portion of the substrate 706, nanowire channel region 702 and the gate 712 illustrating a high work function gate electrode 714 and a multi-layer charge-trapping region 716a-716c. Referring to FIG. 7B, the gate 712 further includes a tunnel dielectric layer 718 overlying the nanowire channel region 702, and a blocking dielectric layer 720.

[0091] As with the embodiments described above, the high work function gate electrode 714 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. The polysilicon layer of the high work function gate electrode 714 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, and is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 714 is doped to a concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2}.

[0092] The multi-layer charge-trapping region 716a-716c includes at least one inner oxygen-rich first nitride layer 716a comprising nitride closer to the tunnel dielectric layer 718, and an outer oxygen-lean second nitride layer 716b overlying the oxygen-rich first nitride layer. Generally, the outer oxygen-lean second nitride layer 716b comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps

Sandisk Technologies, Inc. - Ex. 1040, Page 000341

distributed in the multi-layer charge-trapping region, while the oxygen-rich first nitride layer 716a comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the outer oxygen-lean second nitride layer to reduce the number of charge traps therein.

[0093] In some embodiments, such as that shown, the multi-layer charge-trapping region 716 further includes at least one thin, intermediate or anti-tunneling layer 716c comprising a dielectric, such as an oxide, separating outer oxygen-lean second nitride layer 716b from the oxygen-rich first nitride layer 716a. The anti-tunneling layer 716c substantially reduces the probability of electron charge that accumulates at the boundaries of outer oxygen-lean second nitride layer 716b during programming from tunneling into the oxygen-rich first nitride layer 716a, resulting in lower leakage current.

[0094] As with the embodiment described above, either or both of the oxygen-rich first nitride layer 716a and the outer oxygen-lean second nitride layer 716b can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer. The second nitride layer of the multi-layer charge storing structure is then formed on the middle oxide layer. The outer oxygen-lean second nitride layer 716b has a stoichiometric composition of oxygen, nitrogen and/or silicon different from that of the oxygen-rich first nitride layer 716a, and may also be formed or deposited by a CVD process using a process gas including DCS/NH_3 and N_2O/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich, oxygen-lean top nitride layer.

Sandisk Technologies, Inc. - Ex. 1040, Page 000342

[0095] In those embodiments including an intermediate or anti-tunneling layer 716c comprising oxide, the anti-tunneling layer can be formed by oxidation of the oxygen-rich first nitride layer 716a, to a chosen depth using radical oxidation. Radical oxidation may be performed, for example, at a temperature of 1000-1100 degrees Celsius using a single wafer tool, or 800-900 degrees Celsius using a batch reactor tool. A mixture of H_2 and O_2 gasses may be employed at a pressure of 300-500 Tor for a batch process, or 10-15 Tor using a single vapor tool, for a time of 1-2 minutes using a single wafer tool, or 30 min -1 hour using a batch process.

[0096] Finally, in those embodiments in which the blocking dielectric 720 comprises oxide, the oxide may be formed or deposited by any suitable means. In one embodiment the oxide of blocking dielectric layer 720 is a high temperature oxide deposited in a HTO CVD process. Alternatively, the blocking dielectric layer 720 or blocking oxide layer may be thermally grown, however it will be appreciated that in this embodiment the thickness of the outer oxygen-lean second nitride layer 716b may need to be adjusted or increased as some of the top nitride will be effectively consumed or oxidized during the process of thermally growing the blocking oxide layer.

[0097] A suitable thickness for the oxygen-rich first nitride layer 716a may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 716c. A suitable thickness for the outer oxygen-lean second nitride layer 716b may be at least 30Å. In certain embodiments, the outer oxygen-lean second nitride layer 716b may be formed up to 70Å thick, of which 30-70Å may be consumed by radical oxidation to form the blocking dielectric layer 720. A ratio of thicknesses between the oxygen-rich

Sandisk Technologies, Inc. - Ex. 1040, Page 000343

first nitride layer 716a and the outer oxygen-lean second nitride layer 716b is approximately 1:1 in some embodiments, although other ratios are also possible.

[0098] In other embodiments, either or both of the outer oxygen-lean second nitride layer 716b and the blocking dielectric layer 720 may comprise a high K dielectric. Suitable high K dielectrics include hafnium based materials such as HfSiON, HfSiO or HfO, Zirconium based material such as ZrSiON, ZrSiO or ZrO, and Yttrium based material such as Y_2O_3.

[0099] Figure 7C illustrates a cross-sectional view of a vertical string of non-planar multigate devices 700 of FIG. 7A arranged in a Bit-Cost Scalable or BiCS architecture 726. The architecture 726 consists of a vertical string or stack of non-planar multigate devices 700, where each device or cell includes a channel region 702 overlying the substrate 706, and connecting a source region and a drain region (not shown in this figure) of the memory transistor, and having a gate-all-around (GAA) structure in which the nanowire channel region 702 is enclosed on all sides by a gate 712. The BiCS architecture reduces number of critical lithography steps compared to a simple stacking of layers, leading to a reduced cost per memory bit.

[00100] In another embodiment, the memory transistor is or includes a non-planar device comprising a vertical nanowire channel region formed in or from a semiconducting material projecting above or from a number of conducting, semiconducting layers on a substrate. In one version of this embodiment, shown in cut-away in FIG. 8A, the memory transistor 800 comprises a vertical nanowire channel region 802 formed in a cylinder of semiconducting material connecting a source region 804 and drain region 806 of the device. The channel region 802 is surrounded by a tunnel

Sandisk Technologies, Inc. - Ex. 1040, Page 000344

dielectric layer 808, a multi-layer charge-trapping region 810, a blocking dielectric layer 812 and a high work function gate electrode 814 overlying the blocking dielectric layer to form a control gate of the memory transistor 800. The channel region 802 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or can include an annular layer formed over a cylinder of dielectric filler material. As with the horizontal nanowires described above, the channel region 802 can comprise polysilicon or recrystallized polysilicon to form a monocrystalline channel region. Optionally, where the channel region 802 includes a crystalline silicon, the channel region can be formed to have <100> surface crystalline orientation relative to a long axis of the channel region.

[00101] As with the embodiments described above, the high work function gate electrode 814 includes a doped polysilicon layer formed or deposited in a low pressure CVD process and having a thickness of from about 200 Å to about 2000 Å. The polysilicon layer of the high work function gate electrode 814 can be formed or grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, and is doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. In an exemplary embodiment, the polysilicon layer of the high work function gate electrode 814 is doped to a concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2}.

[00102] In some embodiments, such as that shown in FIG. 8B, the multi-layer charge-trapping region 810 includes at least an inner or oxygen-rich first nitride layer 810a closest to the tunnel dielectric layer 808, and an outer or oxygen-lean second nitride

Sandisk Technologies, Inc. - Ex. 1040, Page 000345

layer 810b. Optionally, as in the embodiment shown, the oxygen-rich first nitride layer 810a and the oxygen-lean second nitride layer 810b are separated by an intermediate oxide or anti-tunneling layer 810c comprising oxide.

[00103] Either or both of the oxygen-rich first nitride layer 810a and the oxygen-lean second nitride layer 810b can comprise silicon nitride or silicon oxynitride, and can be formed, for example, by a CVD process including N_2O/NH_3 and DCS/NH_3 gas mixtures in ratios and at flow rates tailored to provide a silicon-rich and oxygen-rich oxynitride layer.

[00104] Finally, either or both of the oxygen-lean second nitride layer 810b and the blocking dielectric layer 812 may comprise a high K dielectric, such as HfSiON, HfSiO, HfO, ZrSiON, ZrSiO, ZrO, or Y_2O_3.

[00105] A suitable thickness for the oxygen-rich first nitride layer 810a may be from about 30Å to about 80Å (with some variance permitted, for example ±10 A), of which about 5-20Å may be consumed by radical oxidation to form the anti-tunneling layer 820. A suitable thickness for the oxygen-lean second nitride layer 810b may be at least 30Å, and a suitable thickness for the blocking dielectric layer 812 may be from about 30-70Å.

[00106] The memory transistor 800 of FIG. 8A can be made using either a gate first or a gate last scheme. FIGs. 9A-F illustrate a gate first scheme for fabricating the non-planar multigate device of FIG. 8A. FIGs. 20A-F illustrate a gate last scheme for fabricating the non-planar multigate device of FIG. 8A.

[00107] Referring to FIG. 9A, in a gate first scheme a first or lower dielectric layer 902, such as an oxide, is formed over a first, doped diffusion region 904, such as a source

Sandisk Technologies, Inc. - Ex. 1040, Page 000346

region or a drain region, in a substrate 906. A high work function gate electrode 908 is formed over the first dielectric layer 902 to form a control gate of the device, and a second or upper dielectric layer 910 formed thereover. As with embodiments described above, the high work function gate electrode 908 can be formed by depositing and/or doping polysilicon layer having a thickness of from about 200 Å to about 2000 Å and a dopant concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2} so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. The polysilicon layer can be deposited in a low pressure CVD process as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, or can be doped using an ion implantation process following deposition.

[00108] The first and second dielectric layers 902, 910, can be deposited by CVD, radical oxidation or be formed by oxidation of a portion of the underlying layer or substrate. Generally the thickness of the high work function gate electrode 908 is from about 40- 50Å, and the first and second dielectric layers 902, 910, from about 20- 80Å.

[00109] Referring to FIG. 9B, a first opening 912 is etched through the overlying high work function gate electrode 908, and the first and second dielectric layers 902, 910, to the diffusion region 904 in the substrate 906. Next, layers of a tunneling oxide 914, charge-trapping region 916, and blocking dielectric 918 are sequentially deposited in the opening and the surface of the upper dielectric layer 910 planarized to yield the intermediate structure shown in FIG. 9C.

[00110] Although not shown, it will be understood that as in the embodiments described above the charge-trapping region 916 can include a multi-layer charge-trapping region comprising at least one lower or oxygen-rich first nitride layer closer to the tunnel

Sandisk Technologies, Inc. - Ex. 1040, Page 000347

dielectric layer 914, and an upper or oxygen-lean second nitride layer overlying the oxygen-rich first nitride layer. Generally, the oxygen-lean second nitride layer comprises a silicon-rich, oxygen-lean nitride layer and comprises a majority of a charge traps distributed in the multi-layer charge-trapping region, while the oxygen-rich first nitride layer comprises an oxygen-rich nitride or silicon oxynitride, and is oxygen-rich relative to the oxygen-lean second nitride layer to reduce the number of charge traps therein. In some embodiments, the multi-layer charge-trapping region 916 further includes at least one thin, intermediate or anti-tunneling layer comprising a dielectric, such as an oxide, separating the oxygen-lean second nitride layer from the oxygen-rich first nitride layer.

[00111] Next, a second or channel region opening 920 is anisotropically etched through tunneling oxide 914, charge-trapping region 916, and blocking dielectric 918, FIG. 9D. Referring to FIG. 9E, a semiconducting material 922 is deposited in the channel region opening to form a vertical channel region 924 therein. The vertical channel region 924 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material, or, as shown in FIG. 9E, can include a separate, layer semiconducting material 922 surrounding a cylinder of dielectric filler material 926.

[00112] Referring to FIG. 9F, the surface of the upper dielectric layer 910 is planarized and a layer of semiconducting material 928 including a second, doped diffusion region 930, such as a source region or a drain region, formed therein deposited over the upper dielectric layer to form the device shown.

[00113] Referring to FIG. 10A, in a gate last scheme a dielectric layer 1002, such as an oxide, is formed over a sacrificial layer 1004 on a surface on a substrate 1006, an opening etched through the dielectric and sacrificial layers and a vertical channel region

Sandisk Technologies, Inc. - Ex. 1040, Page 000348

1008 formed therein. As with embodiments described above, the vertical channel region 1008 can include an annular region in an outer layer of a substantially solid cylinder of semiconducting material 1010, such as polycrystalline or monocrystalline silicon, or can include a separate, layer semiconducting material surrounding a cylinder of dielectric filler material (not shown). The dielectric layer 1002 can comprise any suitable dielectric material, such as a silicon oxide, capable of electrically isolating the subsequently formed high work function gate electrode of the memory transistor 800 from an overlying electrically active layer or another memory transistor.

[00114] Referring to Figure 10B, a second opening 1012 is etched through the etched through the dielectric and sacrificial layers 1002, 1004, to the substrate 1006, and the sacrificial layer 1004 at least partially etched or removed. The sacrificial layer 1004 can comprise any suitable material that can be etched or removed with high selectivity relative to the material of the dielectric layer 1002, substrate 1006 and vertical channel region 1008. In one embodiment the sacrificial layer 1004 comprises an oxide that can be removed by Buffered Oxide Etch (BOE etch).

[00115] Referring to Figure 10C and 10D, a tunnel dielectric layer 1014, a multi-layer charge-trapping region 1016A-C, and a blocking dielectric layer 1018 are sequentially deposited in the opening, and the surface of the dielectric layer 1002 planarized to yield the intermediate structure shown in Figure 10C. As in the embodiments described above, the multi-layer charge trapping layer 1016A-C is a split multi-layer charge trapping layer including at least an inner oxygen-rich first nitride layer 1016A closest to the tunnel dielectric layer 1014, and an outer, oxygen-lean second

Sandisk Technologies, Inc. - Ex. 1040, Page 000349

nitride layer 1016B. Optionally, the first and second charge trapping layers can be separated by an intermediate oxide or anti-tunneling layer 1016C.

[00116] Next, a high work function gate electrode 1022 is deposited into the second opening 1012 and the surface of the upper dielectric layer 1002 planarized to yield the intermediate structure illustrated in Figure 10E. As with the embodiments described above, the high work function gate electrode 1022 includes a doped polysilicon layer having a dopant concentration of from about 1e14 cm^{-2} to about 1e16 cm^{-2} so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 eV to about 5.3 eV. The polysilicon layer of the high work function gate electrode 1022 is grown directly as a doped polysilicon layer through the addition of gases such as phosphine, arsine, diborane or BF_2, to the CVD process. Finally, an opening 1024 is etched through the gate layer 1022 to form control gates of separate memory devices 1026A and 1026B.

[00117] The foregoing description of specific embodiments and examples of the invention have been presented for the purpose of illustration and description, and although the invention has been described and illustrated by certain of the preceding examples, it is not to be construed as being limited thereby. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications, improvements and variations within the scope of the invention are possible in light of the above teaching. It is intended that the scope of the invention encompass the generic area as herein disclosed, and by the claims appended hereto and their equivalents. The scope of the present invention is defined by the claims, which includes known equivalents and unforeseeable equivalents at the time of filing of this application.

Sandisk Technologies, Inc. - Ex. 1040, Page 000350

IN THE CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a memory transistor including:

a channel region electrically connecting a source region and a drain region formed in a substrate, the channel region comprising polysilicon;

an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, the ONNO stack comprising a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer; and

a high work function gate electrode formed over a surface of the ONNO stack.

2. The semiconductor device of claim 1, wherein the channel comprises a silicon nanowire.

3. The semiconductor device of claim 1, wherein the channel region comprises recrystallized polysilicon.

4. The semiconductor device of claim 3, the high work function gate electrode comprises a P+ doped polysilicon layer.

Sandisk Technologies, Inc. - Ex. 1040, Page 000351

5. The semiconductor device of claim 4, wherein the ONNO stack further includes a blocking dielectric layer disposed above the multi-layer charge-trapping region, and wherein the blocking dielectric layer comprises a dielectric comprises a high K High Temperature Oxide (HTO).

6. The semiconductor device of claim 1, further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode.

7. The semiconductor device of claim 6, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a N+ doped polysilicon layer to form an P-type (PMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a N-type (NMOS) logic transistor.

8. The semiconductor device of claim 6, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor comprise a P+ doped polysilicon layer to form an N-type (NMOS) silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor and a P-type (NMOS) logic transistor.

Sandisk Technologies, Inc. - Ex. 1040, Page 000352

9. The semiconductor device of claim 6, wherein both the high work function gate electrode of the memory transistor and the high work function gate electrode of the MOS logic transistor are formed from a single, patterned doped polysilicon layer.

10. The semiconductor device of claim 1, wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer.

11. A semiconductor device comprising:

a memory transistor including:

a channel region electrically connecting a source region and a drain region formed in a substrate, the channel region comprising polysilicon;

an oxide-nitride-nitride-oxide (ONONO) stack disposed above the channel region, the ONONO stack comprising:

a tunnel dielectric layer disposed above the channel region;

a multi-layer charge-trapping region including an oxygen-rich first nitride layer disposed above the tunnel dielectric layer, an oxygen-lean second nitride layer disposed above the first nitride layer, and an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer; and

a blocking dielectric layer disposed above the multi-layer charge-trapping region; and

Sandisk Technologies, Inc. - Ex. 1040, Page 000353

a high work function gate electrode disposed above a surface of the ONONO stack.

12. The semiconductor device of claim 11, wherein the channel region comprises recrystallized polysilicon.

13. The semiconductor device of claim 12, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.

14. The semiconductor device of claim 13, wherein the blocking dielectric layer comprises a dielectric comprises a high K High Temperature Oxide (HTO).

15. The semiconductor device of claim 11, wherein the channel comprises a silicon nanowire.

16. The semiconductor device of claim 11, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.

17. The semiconductor device of claim 11 further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode.

18. A semiconductor device comprising:

Sandisk Technologies, Inc. - Ex. 1040, Page 000354

a memory transistor including:

a vertical channel comprising polysilicon extending from a first diffusion region formed on a surface on a substrate to a second diffusion region formed over the surface of the substrate, the vertical channel electrically connecting the first diffusion region to the second diffusion region;

an oxide-nitride-nitride-oxide (ONNO) stack disposed about the vertical channel, the ONNO stack comprising:

a tunnel dielectric layer abutting the vertical channel;

a multi-layer charge-trapping region including a first nitride layer comprising an oxygen-rich nitride abutting the tunnel dielectric layer, and a second nitride layer comprising a silicon-rich, oxygen-lean nitride overlying the first nitride layer; and

a blocking dielectric layer overlying the multi-layer charge-trapping region; and

a high work function gate electrode disposed about the ONONO stack, abutting the blocking dielectric layer.

19. The semiconductor device of claim 18, further comprising a metal oxide semiconductor (MOS) logic transistor on the substrate, wherein the MOS logic transistor comprises a gate oxide and a high work function gate electrode.

Sandisk Technologies, Inc. - Ex. 1040, Page 000355

20. The semiconductor device of claim 18, wherein the multi-layer charge-trapping region further comprises an anti-tunneling layer comprising an oxide separating the first nitride layer from the second nitride layer.

Sandisk Technologies, Inc. - Ex. 1040, Page 000356

ABSTRACT

A semiconductor devices including non-volatile memories and methods of fabricating the same to improve performance thereof are provided. Generally, the device includes a memory transistor comprising a polysilicon channel region electrically connecting a source region and a drain region formed in a substrate, an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, and a high work function gate electrode formed over a surface of the ONNO stack. In one embodiment the ONNO stack includes a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer. Other embodiments are also disclosed.

Sandisk Technologies, Inc. - Ex. 1040, Page 000357

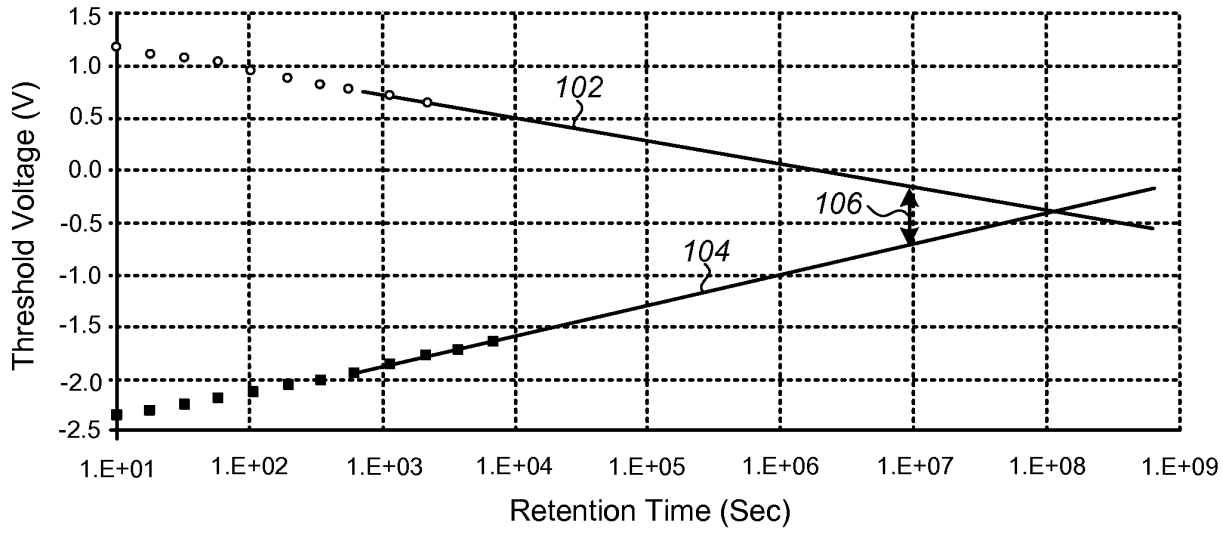

1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
Threshold Voltage (V)
102
104
106
1.E+01
1.E+02
1.E+03
1.E+04
1.E+05
1.E+06
1.E+07
1.E+08
1.E+09
Retention Time (Sec)

FIG. 1A

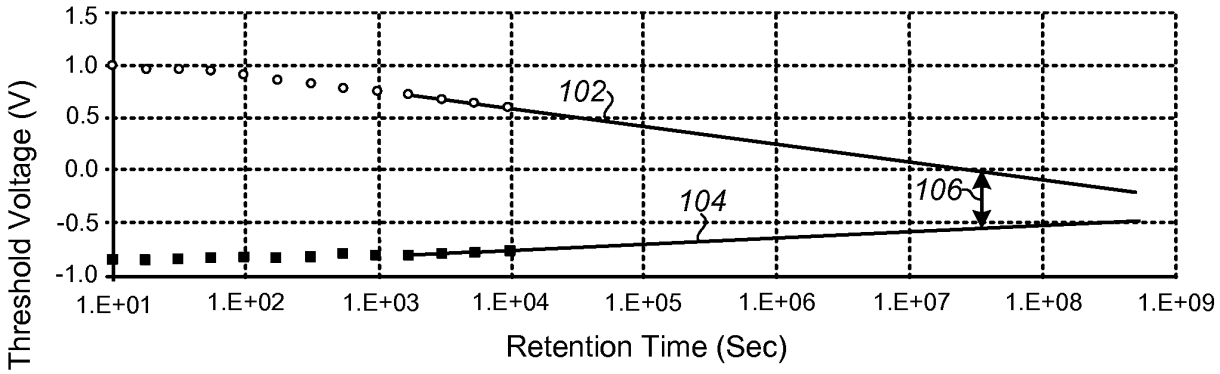

1.5
1.0
0.5
0.0
-0.5
-1.0
Threshold Voltage (V)
102
104
106
1.E+01
1.E+02
1.E+03
1.E+04
1.E+05
1.E+06
1.E+07
1.E+08
1.E+09
Retention Time (Sec)

FIG. 1B

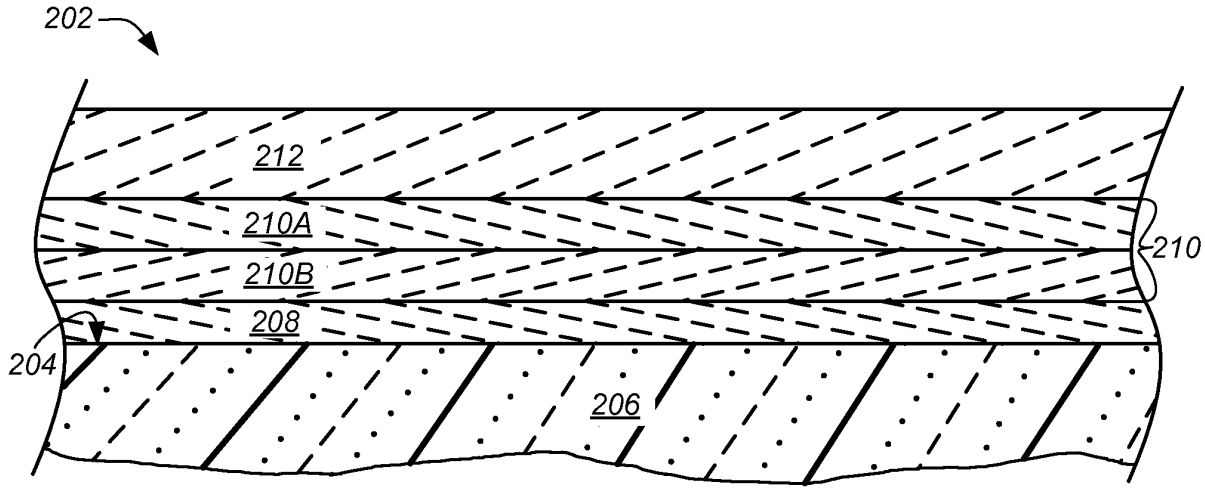

202
212
210A
210B
208
210
204
206

FIG. 2A

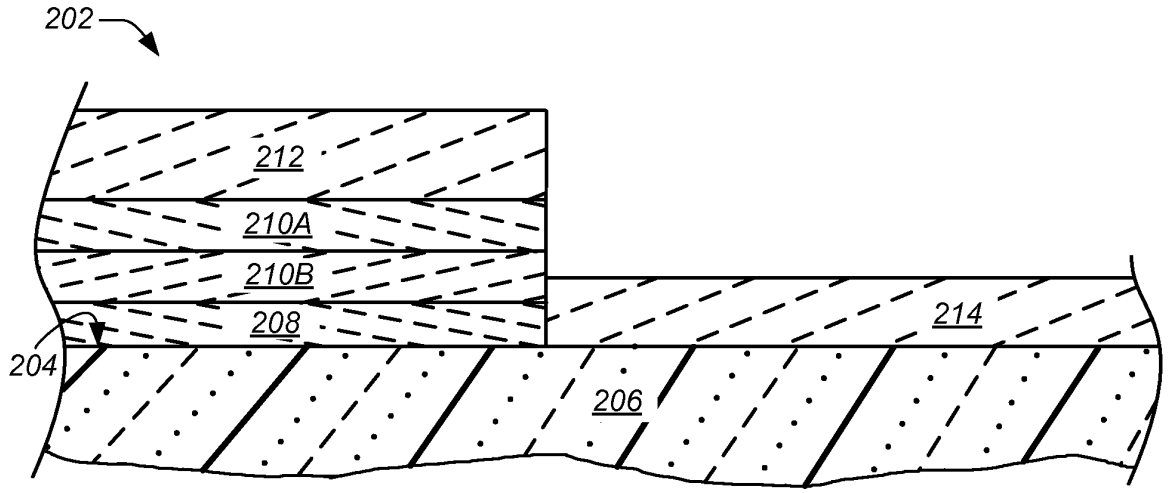

202
212
210A
210B
208
214
204
206

FIG. 2B

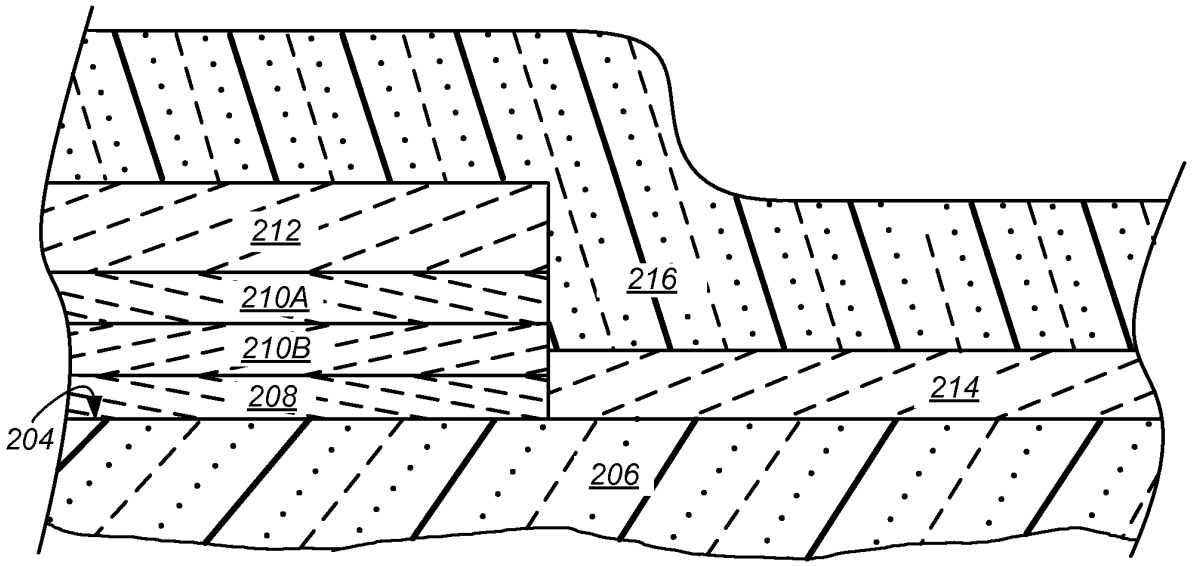

212
210A
210B
208
216
214
204
206

FIG. 2C

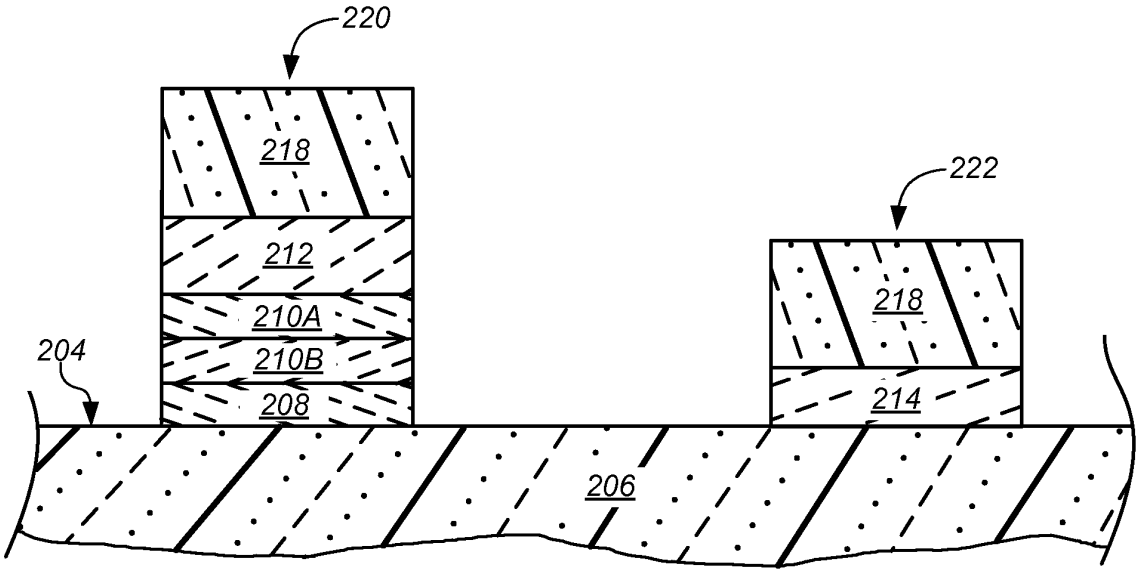

220
218
212
210A
210B
208
222
218
214
204
206

FIG. 2D

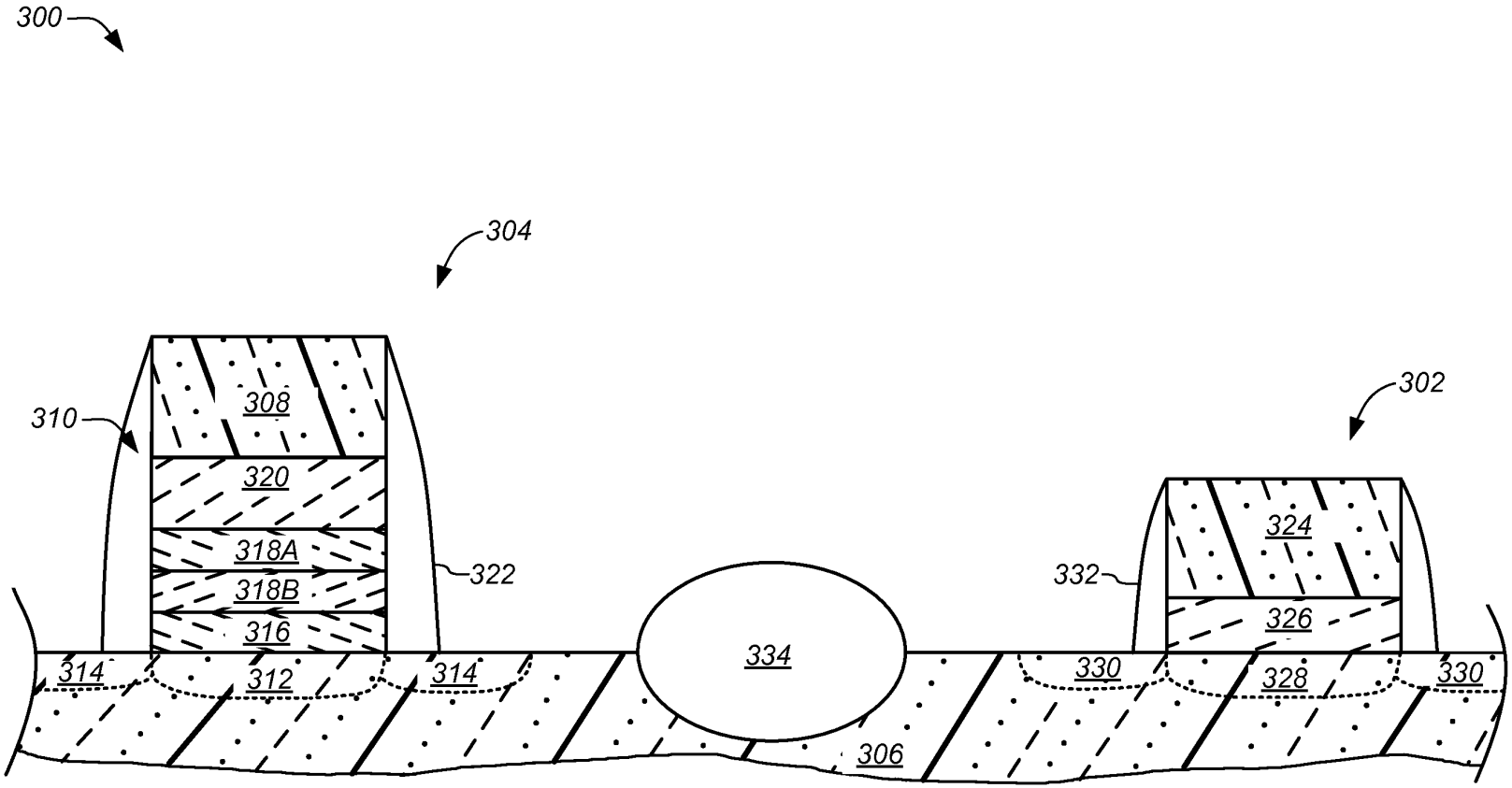


FIG. 3

Sandisk Technologies, Inc. - Ex. 1040, Page 000361

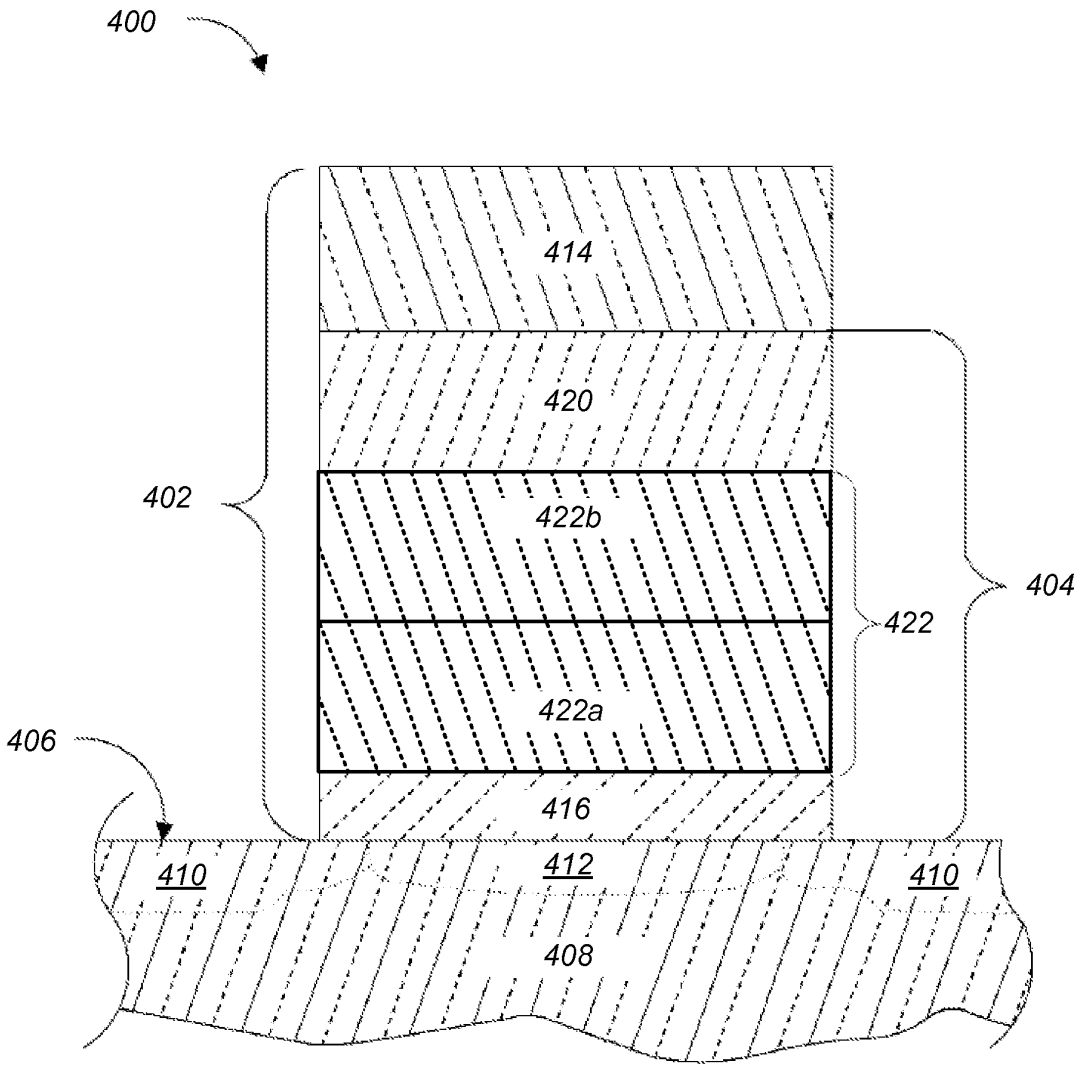


FIG. 4A

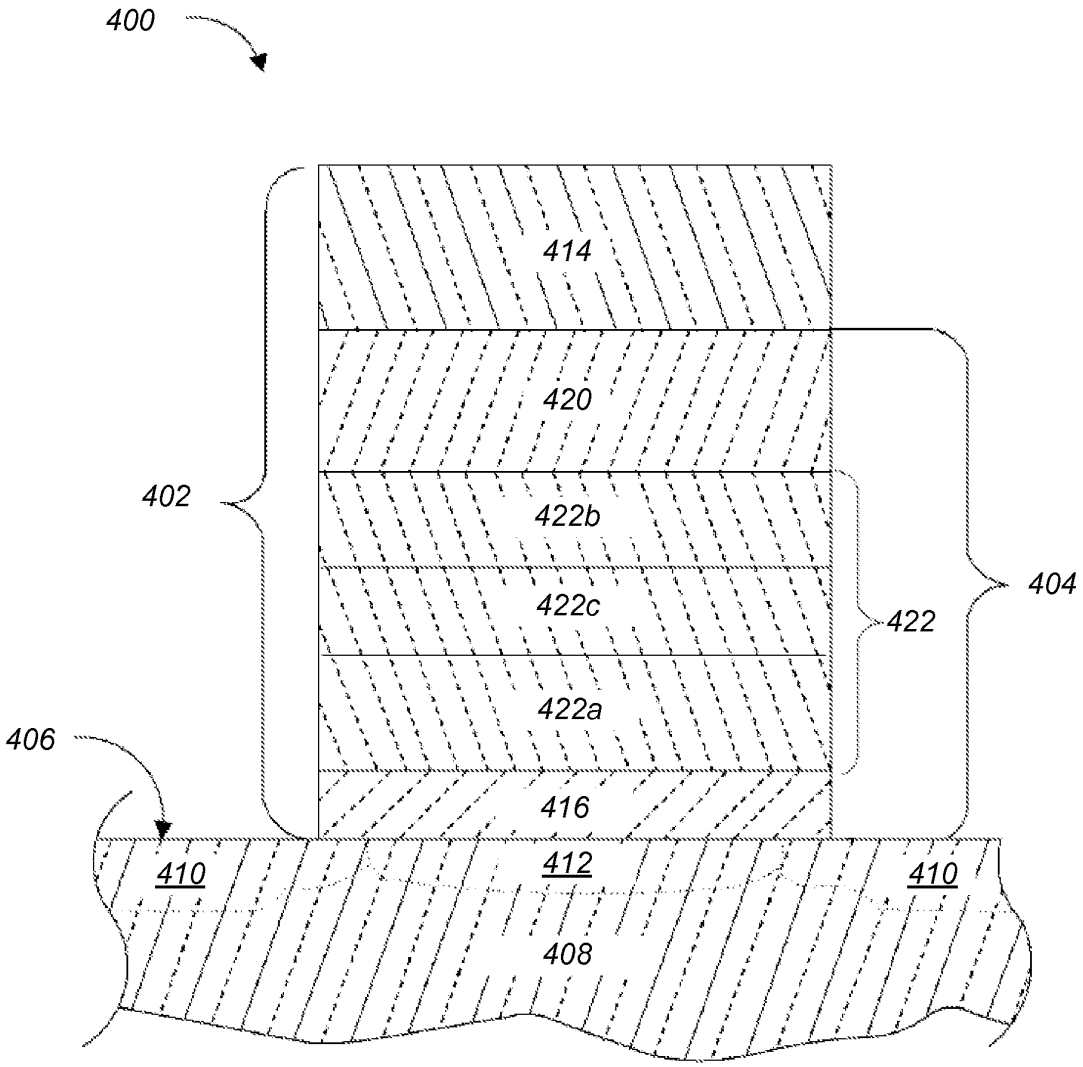


FIG. 4B

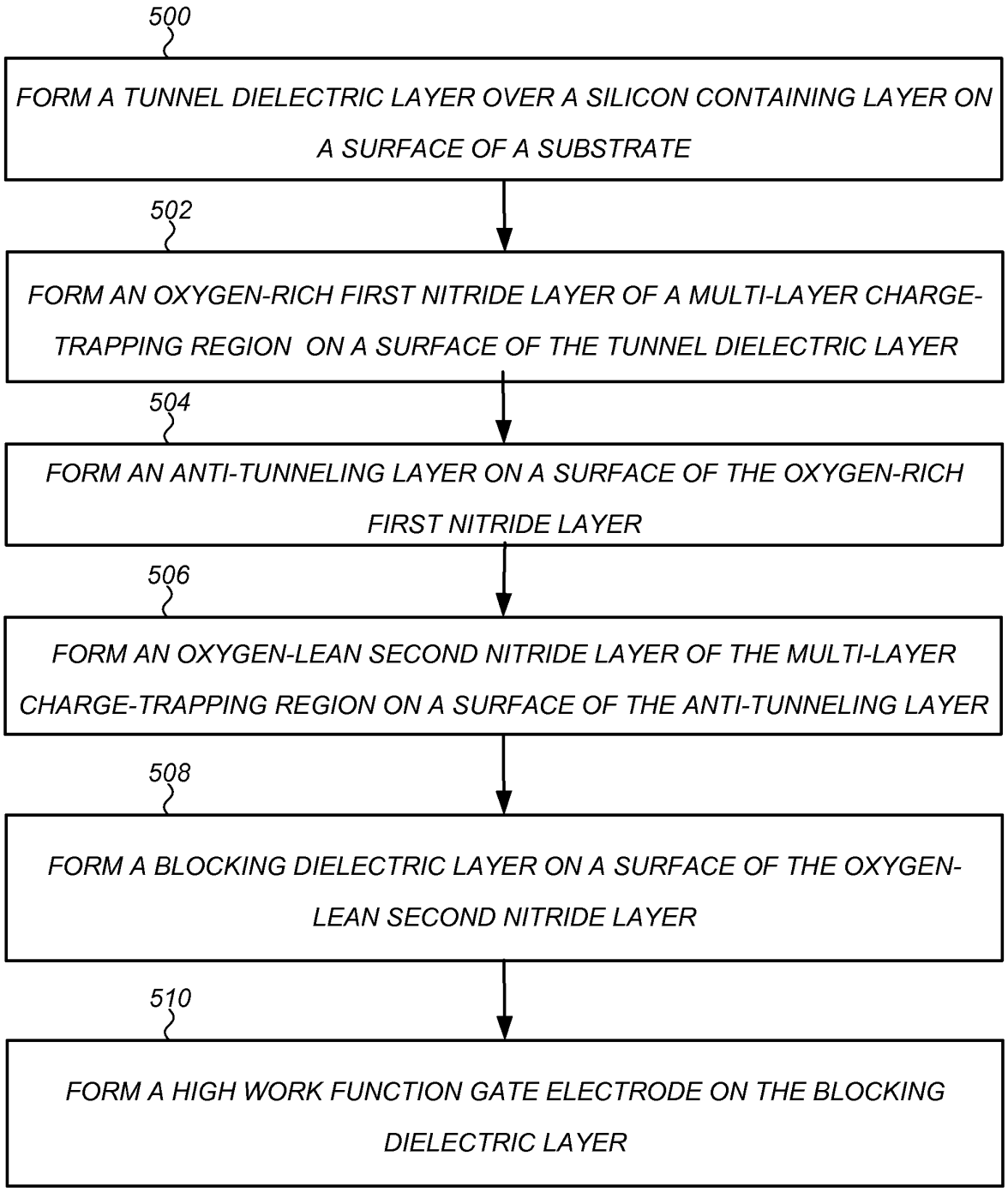

500
FORM A TUNNEL DIELECTRIC LAYER OVER A SILICON CONTAINING LAYER ON A SURFACE OF A SUBSTRATE
502
FORM AN OXYGEN-RICH FIRST NITRIDE LAYER OF A MULTI-LAYER CHARGE-TRAPPING REGION ON A SURFACE OF THE TUNNEL DIELECTRIC LAYER
504
FORM AN ANTI-TUNNELING LAYER ON A SURFACE OF THE OXYGEN-RICH FIRST NITRIDE LAYER
506
FORM AN OXYGEN-LEAN SECOND NITRIDE LAYER OF THE MULTI-LAYER CHARGE-TRAPPING REGION ON A SURFACE OF THE ANTI-TUNNELING LAYER
508
FORM A BLOCKING DIELECTRIC LAYER ON A SURFACE OF THE OXYGEN-LEAN SECOND NITRIDE LAYER
510
FORM A HIGH WORK FUNCTION GATE ELECTRODE ON THE BLOCKING DIELECTRIC LAYER

FIG. 5

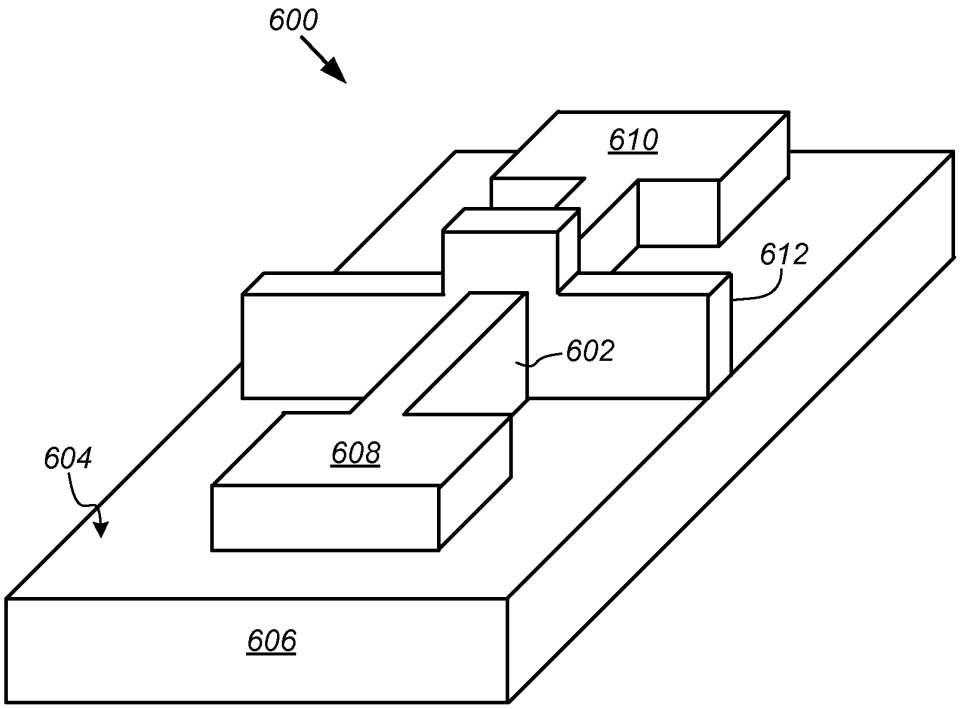


FIG. 6A

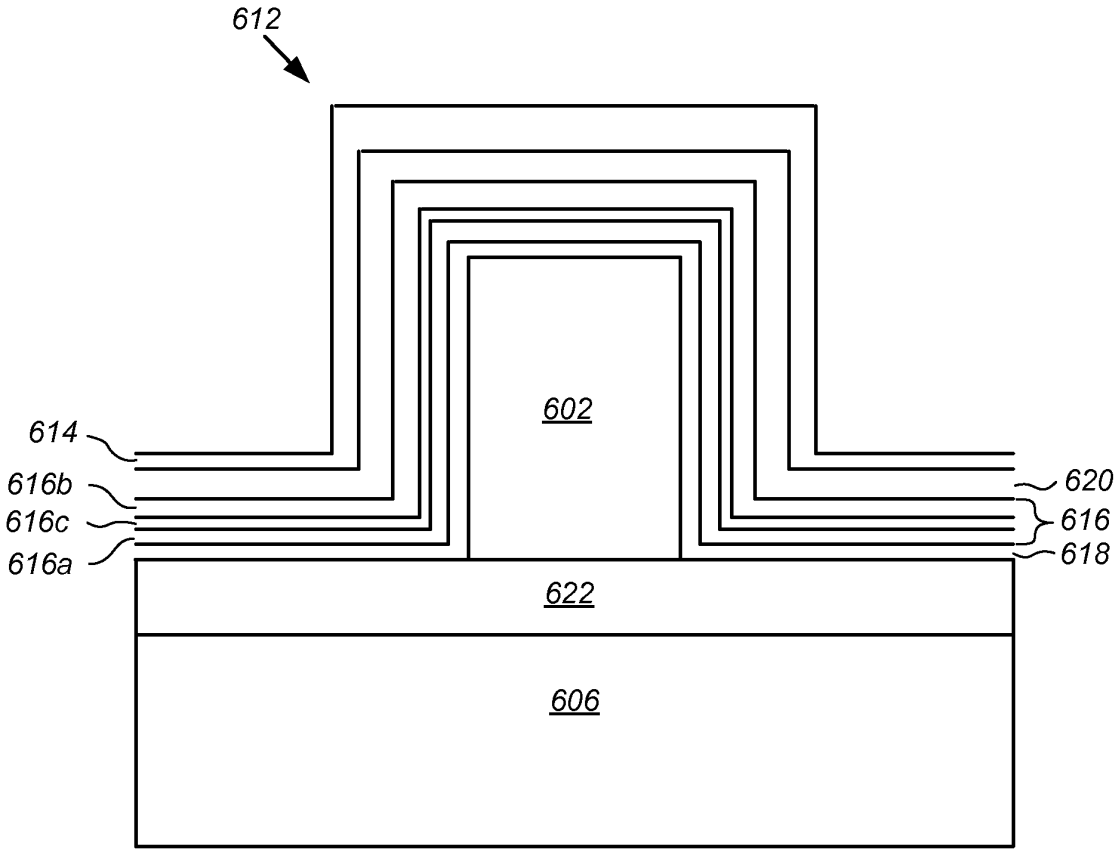


FIG. 6B

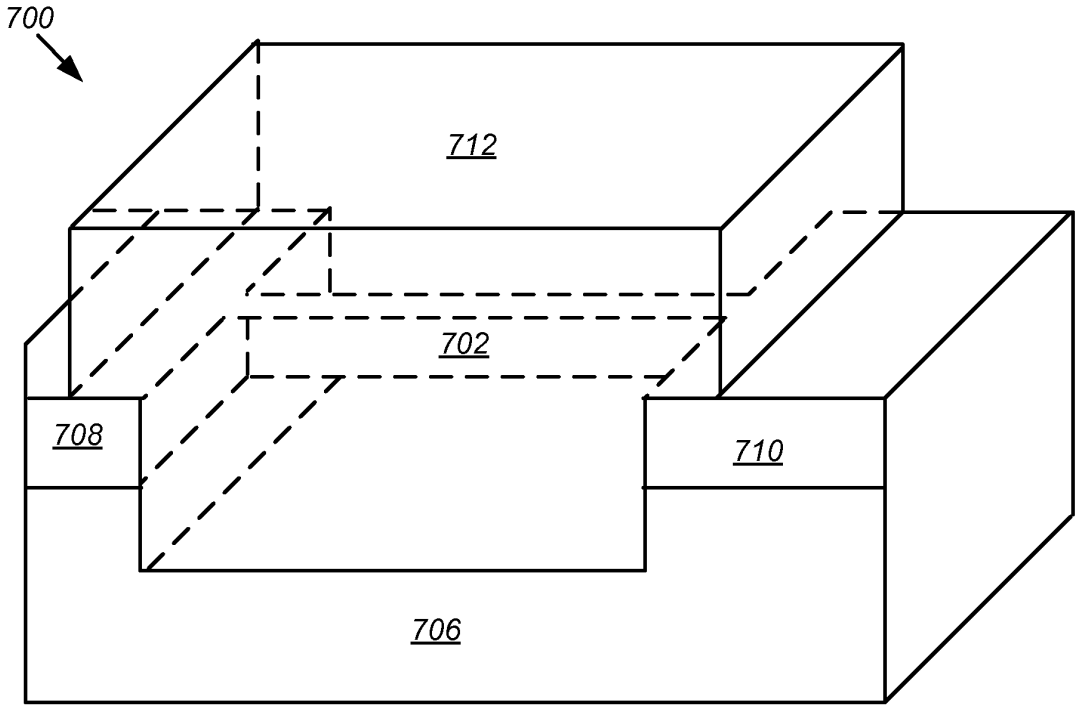


FIG. 7A

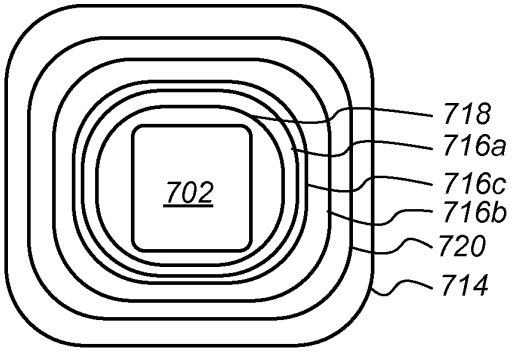


FIG. 7B

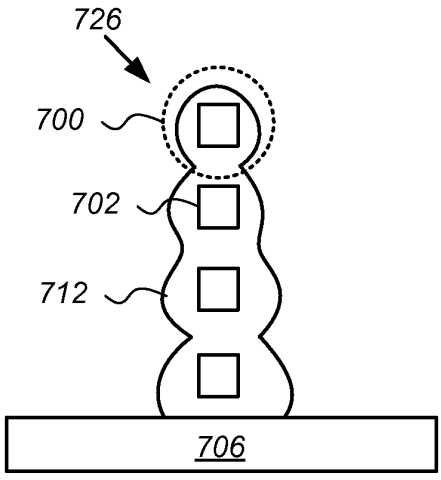


FIG. 7C

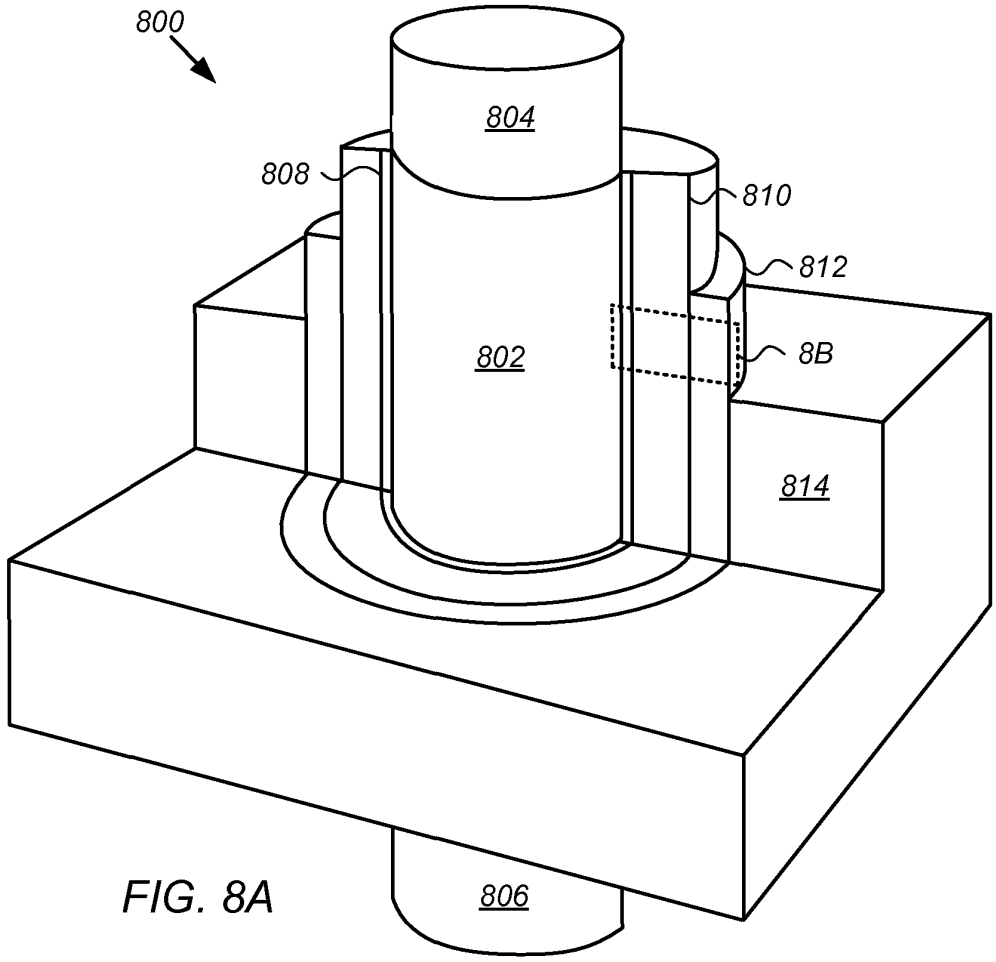


FIG. 8A

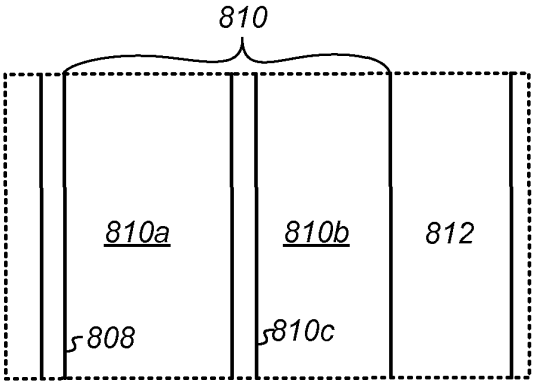


FIG. 8B

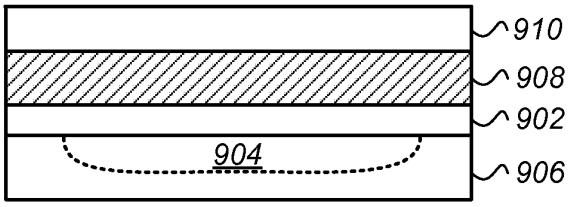


FIG. 9A

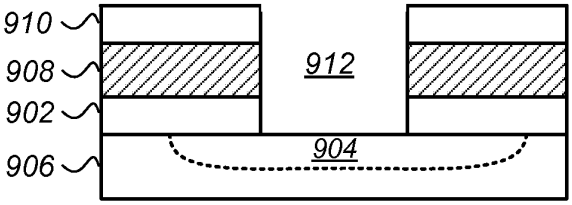


FIG. 9B

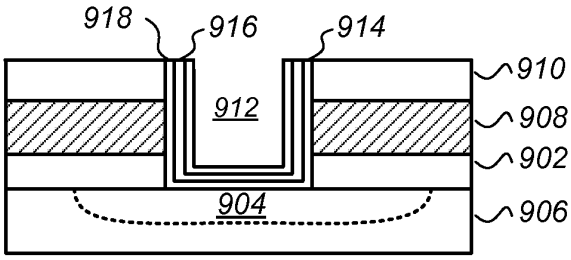


FIG. 9C

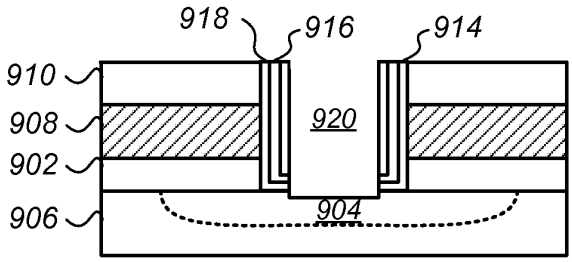


FIG. 9D

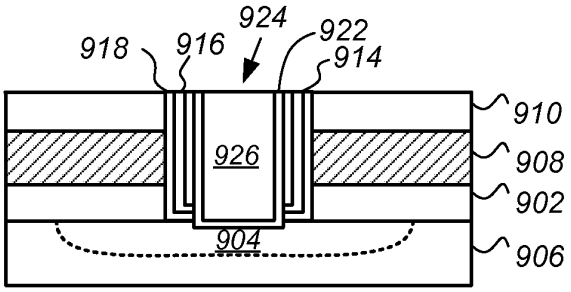


FIG. 9E

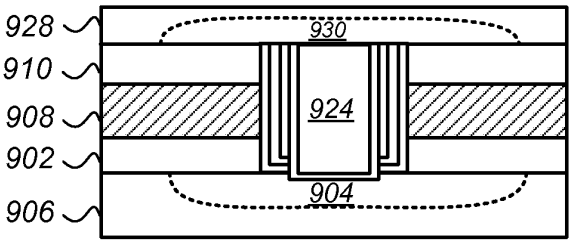


FIG. 9F

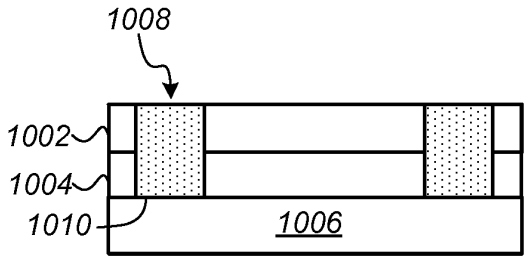


FIG. 10A

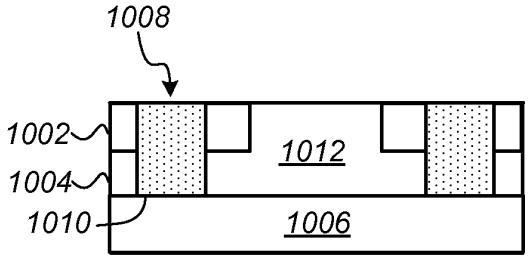


FIG. 10B

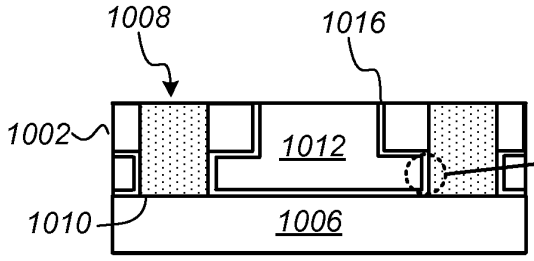


FIG. 10C

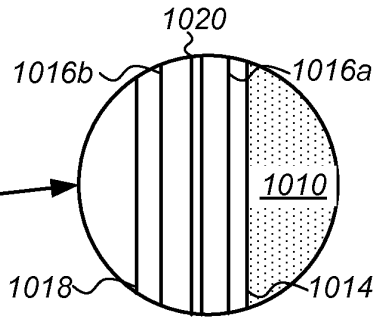


FIG. 10D

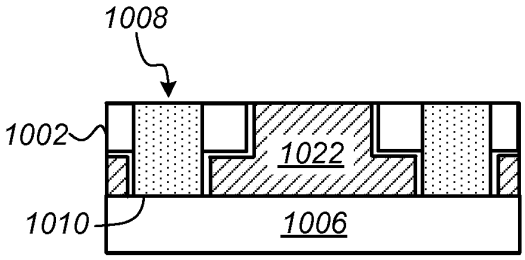


FIG. 10E

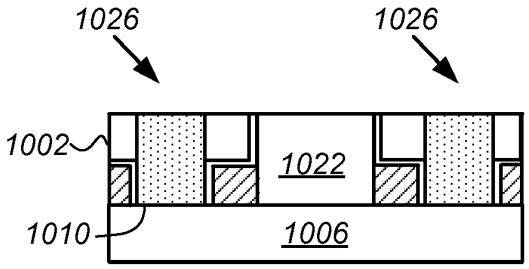


FIG. 10F

PTO/SB/35 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)

First Named Inventor	Igor Polishchuk
Title	Memory Transistor With Multiple Charge Storing Layers And A High Work Function Gate Electrode
Attorney Docket Number	PM07027D1CIP1

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

/William Nuttle/ — Signature

July 1, 2012 — Date

William E. Nuttle — Typed or printed name

42,943 — Registration Number, if applicable

(650)207-3418 — Telephone Number

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

This collection of information is required by 37 CFR 1.213(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/14 (11-08)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Igor		POLISHCHUK	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Fremont	State/Province	CA	Country of Residence[i]	US

Citizenship under 37 CFR 1.41(b)[i]: US

Mailing Address of Applicant:

Address 1	43355 Paseo Padre Pkwy.		
Address 2			
City	Fremont	State/Province	CA
Postal Code	94539	Country[i]	US

Applicant 2 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sagy		LEVY	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Zichron-Yoakev	Country Of Residence[i]	IL

Citizenship under 37 CFR 1.41(b)[i]: IL

Mailing Address of Applicant:

Address 1	66 Yigal-Alon Street		
Address 2			
City	Zichron-Yoakev	State/Province	IL
Postal Code	30900	Country[i]	IL

Applicant 3 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
Dr.	Krishnaswamy		RAMKUMAR	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Jose	State/Province	CA	Country of Residence[i]	US

PTO/SB/14 (11-08)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Citizenship under 37 CFR 1.41(b) [i]	US		
Mailing Address of Applicant:			
Address 1	1193 Lynbrook Way		
Address 2			
City	San Jose	**State/Province**	CA
Postal Code	95134	**Country**[i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	60909		
Email Address	pbj@cypress.com	Add Email	Remove Email
Email Address	larz@cypress.com	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE		
Attorney Docket Number	PM07027D1CIP1	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☒ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

PTO/SB/14 (11-08)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	60909		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	13288919	2011-11-03

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13288919	Division of	12152518	2008-05-13	8063434	2011-11-22

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12152518	non provisional of	60940160	2007-05-25

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			◉ Yes ○ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	Cypress Semiconductor Corporation

PTO/SB/14 (11-08)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PM07027D1CIP1
	Application Number	
Title of Invention	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE	

Mailing Address Information:			
Address 1	198 Champion Court		
Address 2			
City	San Jose	**State/Province**	CA
Country [i]	US	Postal Code	95134
Phone Number	408-545-7194	Fax Number	408-545-6911
Email Address	larz@cypress.com		
Additional Assignee Data may be generated within this form by selecting the **Add** button.		Add	

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/William Nuttle/			Date (YYYY-MM-DD)	2012-07-01
First Name	William	Last Name	Nuttle	Registration Number	42943

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Sandisk Technologies, Inc. - Ex. 1040, Page 000376

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Filer:	William Edward Nuttle
Attorney Docket Number:	PM07027D1CIP1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1250**

Electronic Acknowledgement Receipt

EFS ID:	13153011
Application Number:	13539466
International Application Number:	
Confirmation Number:	5842
Title of Invention:	MEMORY TRANSISTOR WITH MULTIPLE CHARGE STORING LAYERS AND A HIGH WORK FUNCTION GATE ELECTRODE
First Named Inventor/Applicant Name:	Igor Polishchuk
Customer Number:	60909
Filer:	William Edward Nuttle
Filer Authorized By:	
Attorney Docket Number:	PM07027D1CIP1
Receipt Date:	01-JUL-2012
Filing Date:	
Time Stamp:	15:40:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1250
RAM confirmation Number	9737
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		PM07027D1CIP1_Pat_App.pdf	189799 4e9ad38092d69937d4335ac8c21a7bc77cb7b7e1	yes	47

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	40
	Claims	41	46
	Abstract	47	47

Warnings:					
Information:					
2	Drawings-only black and white line drawings	PM07027D1CIP1_FIGs.pdf	123605 3dcffcd5deef125459a9368e75bf3db1351f9162	no	13
Warnings:					
Information:					
3	Nonpublication request from applicant.	PM07027D1CIP1_Non_Pub.pdf	127763 c29b385332ff704cd6e2d0912e1f72ea49b1758b	no	1
Warnings:					
Information:					
4	Application Data Sheet	PM07027D1CIP1_ADS.pdf	1024393 54db1af202b9a21ed225dc4fd9014b949df55ce3	no	5
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	33127 bea29f7f2a7713d9374a624c461e65768d186c52	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1498687		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.