

EXHIBIT C: P.R. 3-1(B) CHART FOR U.S. PATENT NO. 9,929,240

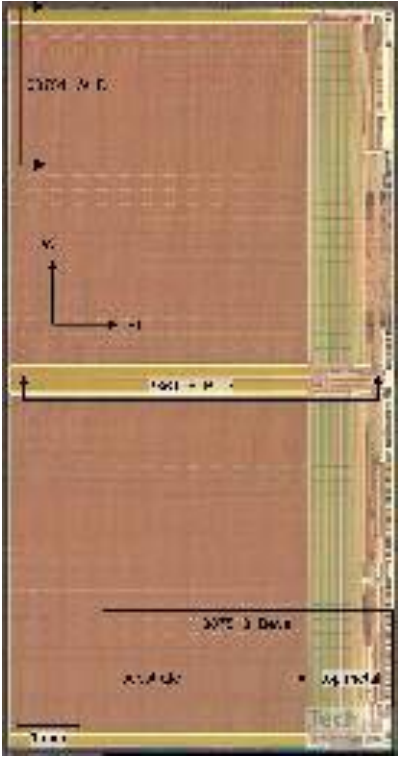
Declaratory judgment defendants IPValue Management, Inc. and Longitude Flash Memory Solutions Ltd. (collectively “IPValue”) provides this chart based upon information that is presently available to them. IPValue has not had access to the accused infringers’ confidential design documents or to other materials that may become available during discovery. IPValue reserves the right to change or provide more detail to the infringement theories set forth below, based upon information that it learns during this case, subject to the Court’s rules and orders.

Definitions:

The term ’240 Accused Instrumentalities is defined in Section I.B of IPValue’s Disclosure of Asserted Claims and Infringement Contentions. As shown in the chart below, the structure of the memory transistors is similar across each of the 64L, 96L, 112L, 162L, and 218L 3D NAND products. Any reference to any specific accused product in the chart below is representative of all ’240 Accused Instrumentalities.

<i>Claim Element</i>	<i>’240 Accused Instrumentalities</i>
1. A memory device, comprising:	To the extent the preamble is deemed limiting, the ’240 Accused Instrumentalities comprise a memory device. For example, the WDS960G2G0C SSD contains a semiconductor die containing 112-Layer 3D NAND Flash Memory¹: 

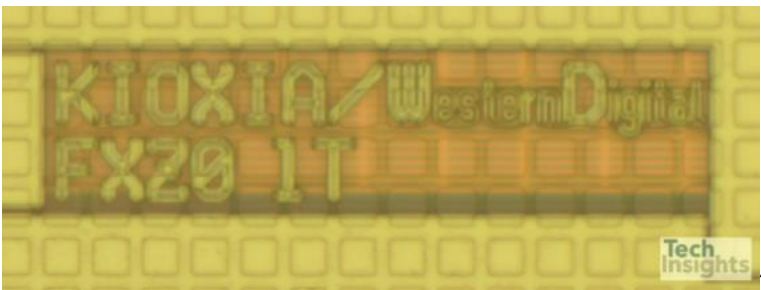
¹ TechInsights, Kioxia/Western Digital WDS960G2G0C SSD, SanDisk 060946 1T00 (FXH8 512G Die), 112-Layer 3D NAND Flash Memory, 18 nm Process Node, Advanced Memory Essentials, AME-2106-802, Published: November 19, 2021 (“TechInsights 112L Report”)

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	A micrograph of a semiconductor die, likely a NAND flash memory die, showing a grid of memory cells. The die is rectangular with a brownish-gold color. There are several markings on the die, including a large '1' in the top left corner, a smaller '1' in the top right corner, and a '1' in the bottom right corner. The markings are in a stylized font. The die is mounted on a substrate, and the edges of the die are visible. Die markings on this and other '240 Accused Instrumentalities indicate that they are each made by a joint venture owned by Toshiba/Kioxia and Sandisk/Western Digital:

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	 12 Package Optical - Package X-ray - Die Optical\TH58LJT0T24BADE_FST0_256G_336534_DieMik-100X.png ²  ³

² Image of Western Digital Green SSD (P/N WDS480G2G0A) (96L)

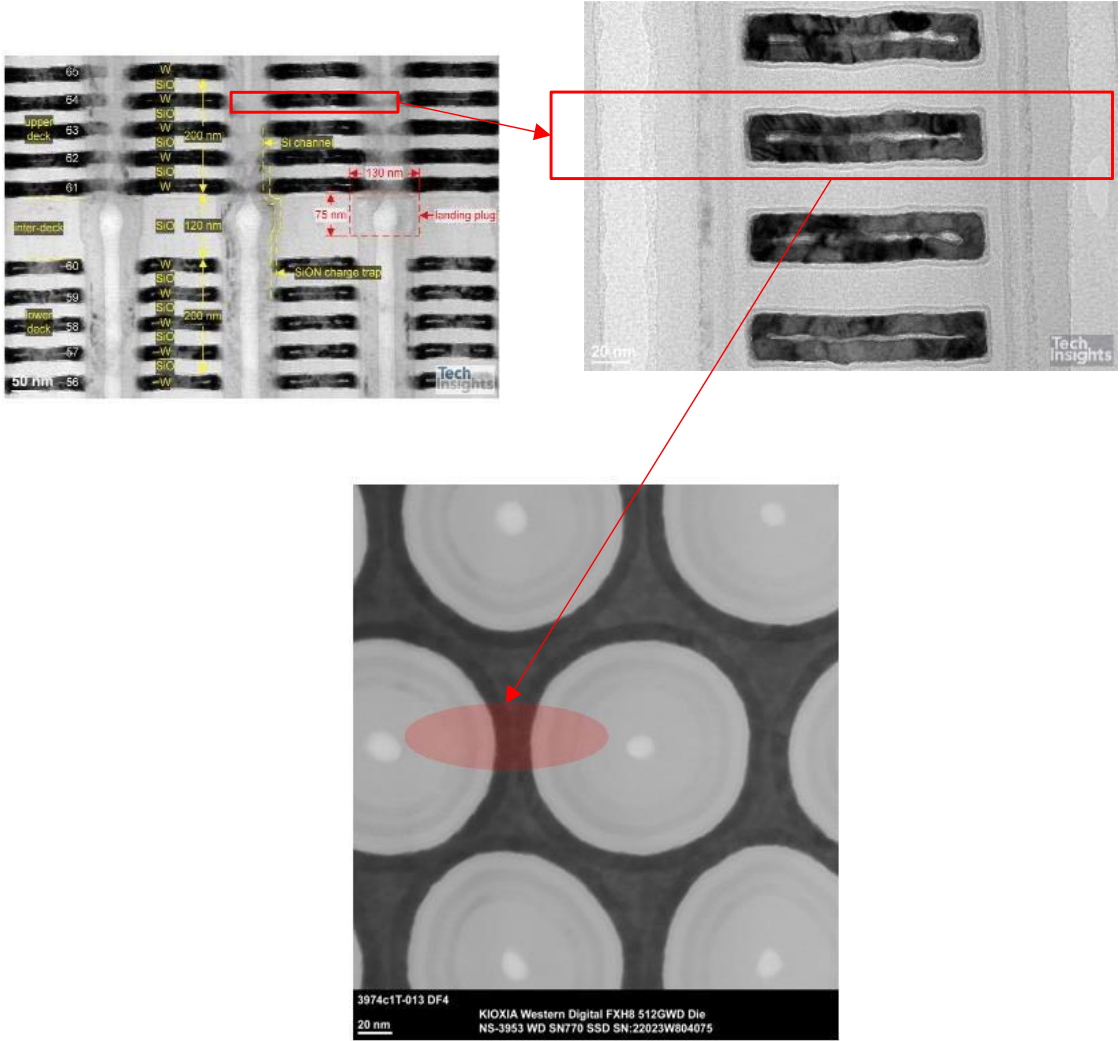
³ TechInsights 112L Report

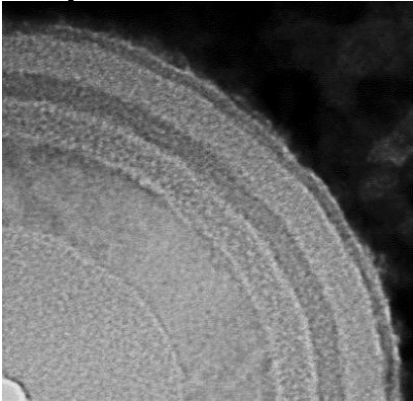
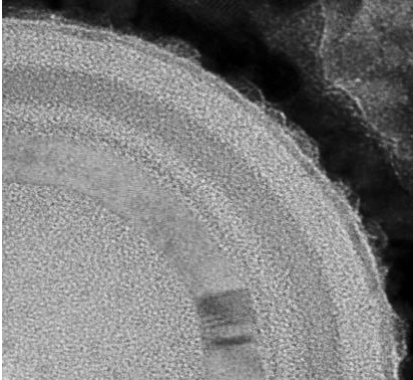
Claim Element	'240 Accused Instrumentalities
	 Tech Insights 4  Tech Insights 5 The following images each show multiple memory transistors, in different cross sections of a 112L accused product⁶:

⁴ TechInsights, Toshiba TH58LKT3B46BA8S (KIOXIA/Western Digital Corp. FXZ0_1T die), 162-Layer 3D NAND Flash Memory, Advanced Memory Essentials, AME-2310-803, Published: February 29, 2024 (“TechInsights 162L Report”)

⁵ TechInsights, KIOXIA/WDC FYU6_1T 218L (BiCS8), Triple-Level Cell (TLC) 1 Tb 3D NAND Flash, Advanced Memory Essentials, AME-2407-801, Published: November 29, 2024 (“TechInsights 218L Report”)

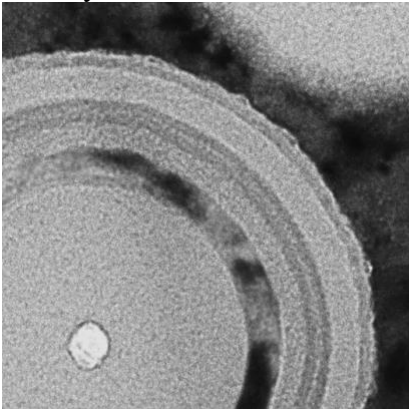
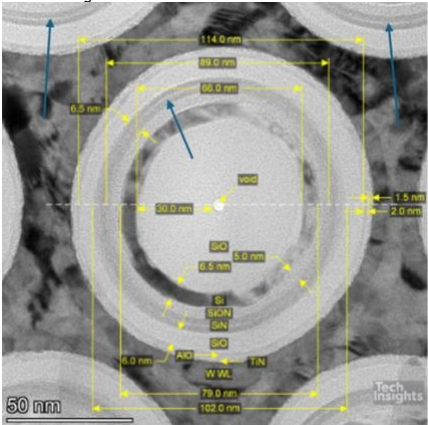
⁶ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 3974c1T-013 DF4 20 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN-22023W804075

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	Similar memory transistor structures are present in each of the '240 Accused Instrumentalities, as shown in the following cross section images. 64-layer⁷:  96-layer⁸: 

⁷ TechInsights, Memory DRAM & NAND Tri-Annual Briefing #1, 2022, Report ID: BRF-2112-810, May 2022, p. 47,

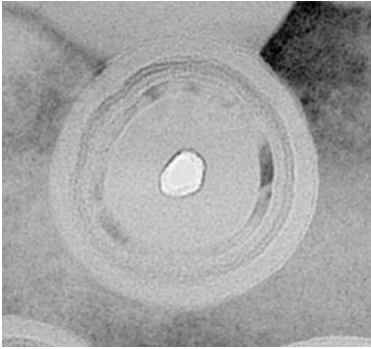
⁸ *Id.*

Claim Element	'240 Accused Instrumentalities
	112-layer⁹:  162-layer¹⁰:  218-layer¹¹:

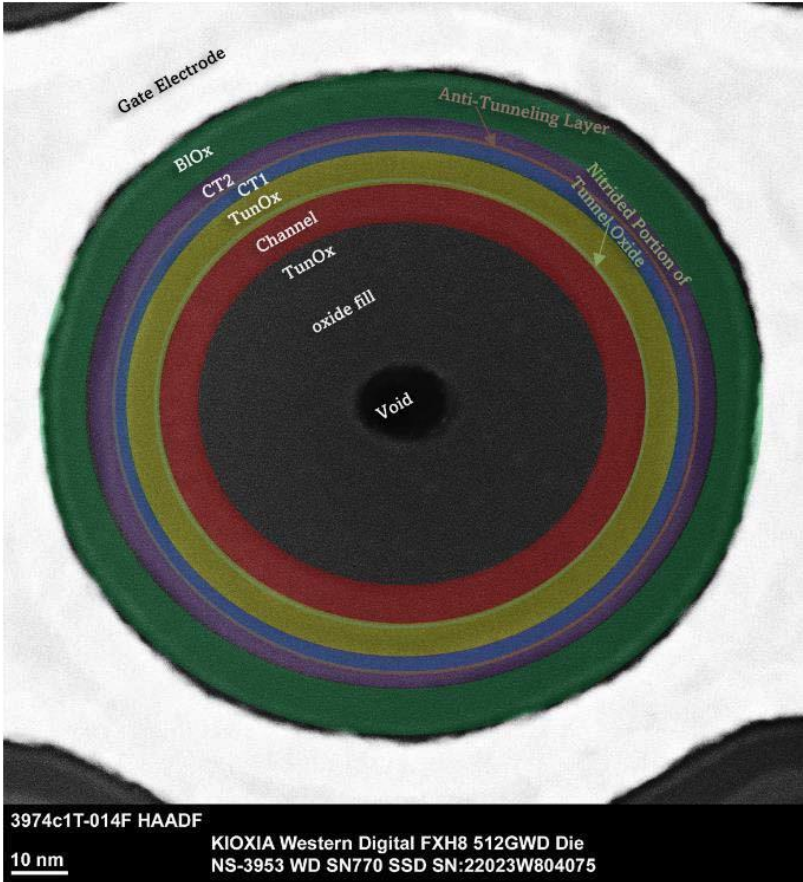
⁹ *Id.*

¹⁰ TechInsights 162L Report

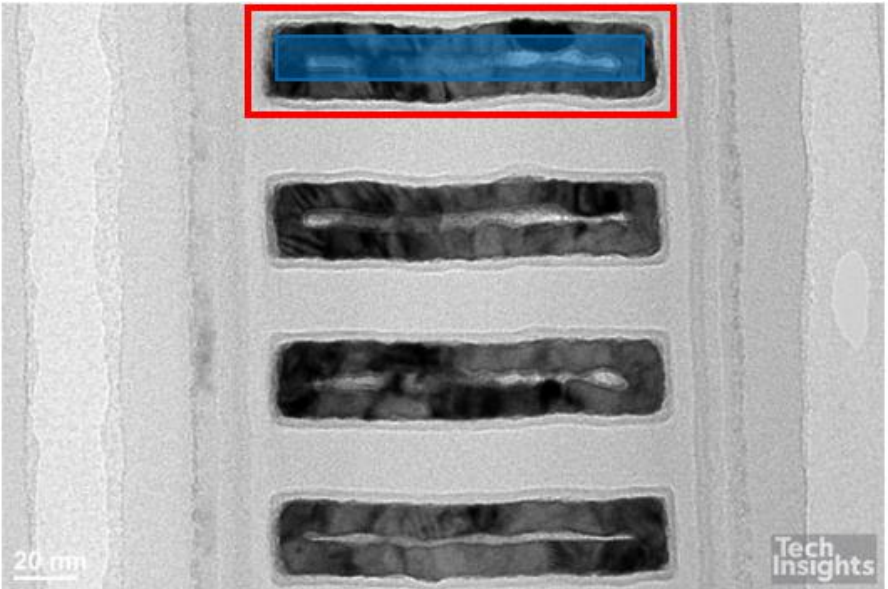
¹¹ TechInsights 218L Report

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	
[1a] a gate structure;	The '240 Accused Instrumentalities comprise a gate structure. For example, the gate electrode ("Gate Electrode") is formed from tungsten ¹² :

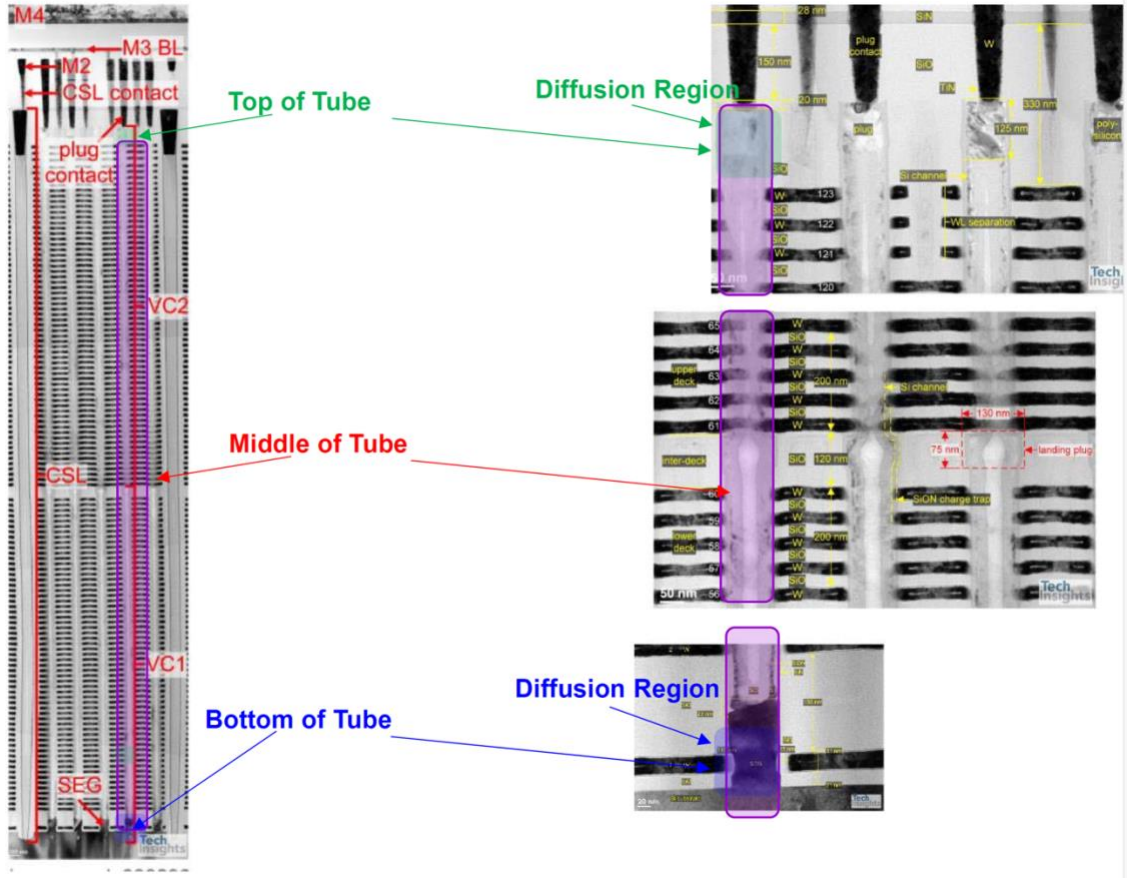
¹² TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 This gate structure is similarly indicated by the red box in the following image from a cross section in the perpendicular plane to the above image¹³:

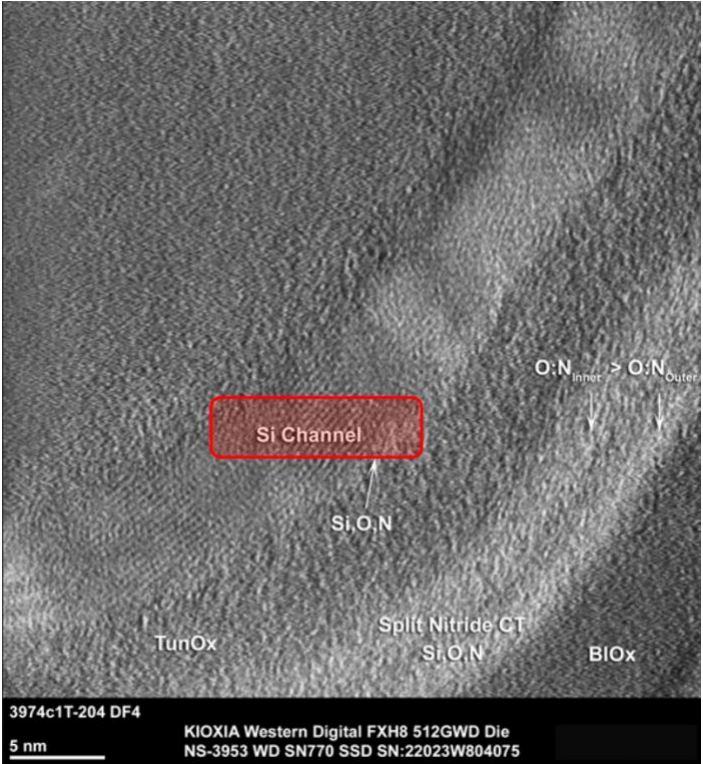
¹³ TechInsights 112L Report

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	
[1b] a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and	The '240 Accused Instrumentalities comprise a channel positioned between and electrically connecting a first diffusion region and a second diffusion region. For example, the '240 Accused Instrumentalities contain vertical tube structures between a bottom first diffusion region and a top second diffusion region¹⁴:

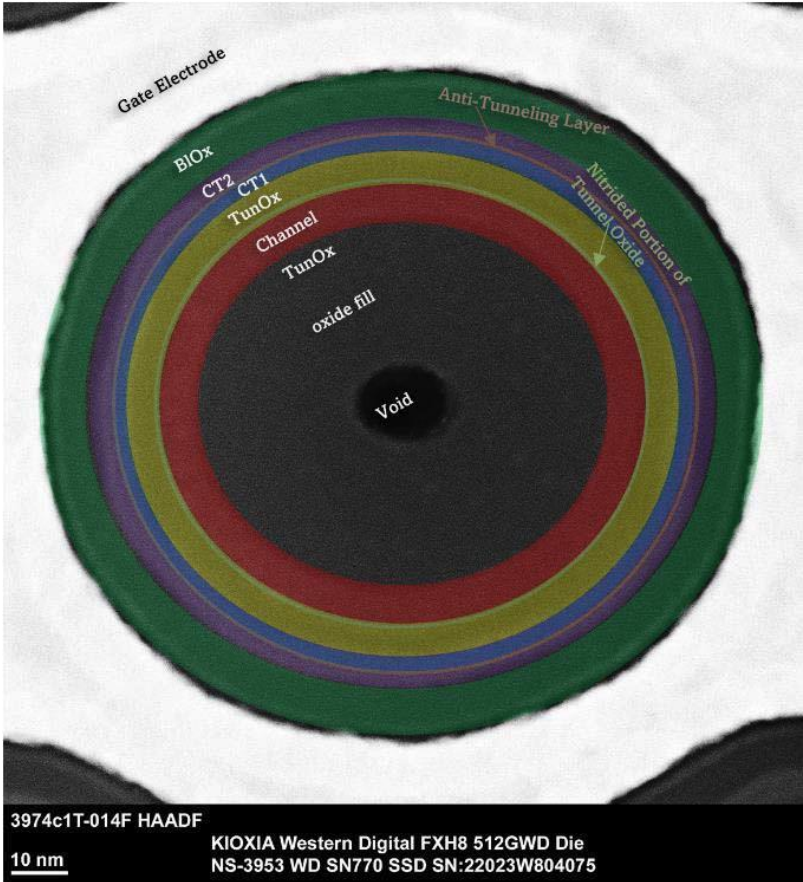
¹⁴ TechInsights 112L Report

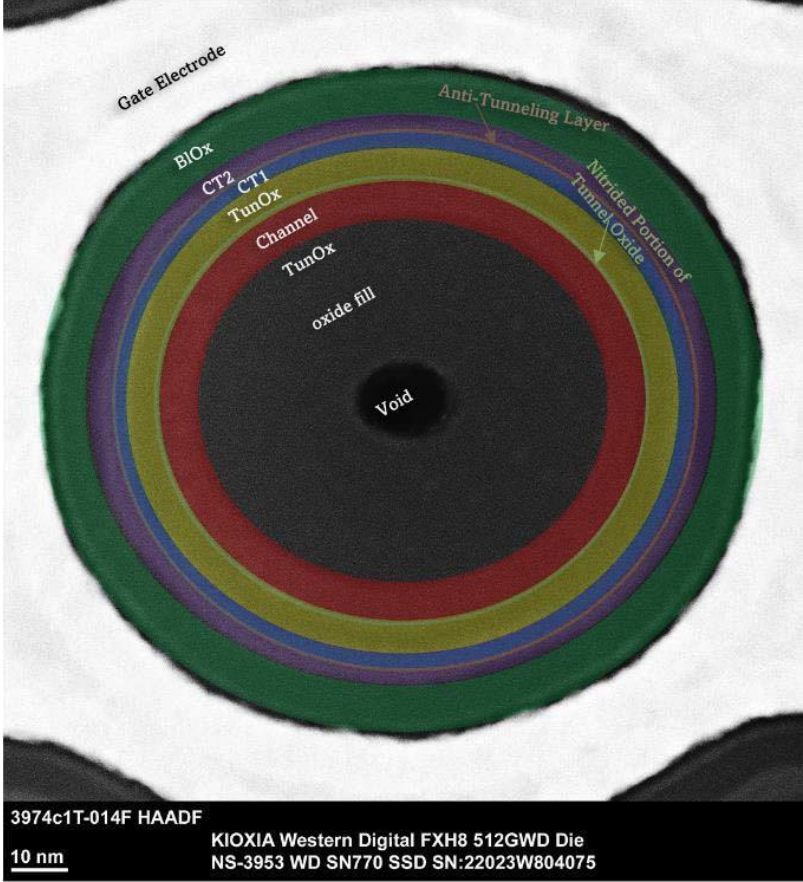
Claim Element	'240 Accused Instrumentalities
	 The vertical tubes contain a silicon channel that electrically connect the first and second diffusion regions¹⁵:

¹⁵ *Id.*

Claim Element	'240 Accused Instrumentalities
	
[1c] a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel,	The '240 Accused Instrumentalities comprise a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel. For example, the tunnel dielectric layer (yellow "TunOx"), multi-layer charge trapping layer ("CT1," "Anti-Tunneling Layer," "CT2"), and blocking dielectric layer ("BIOx") are disposed between the gate structure ("Gate Electrode") and the channel ("Channel")¹⁶:

¹⁶ TechInsights 112L Report

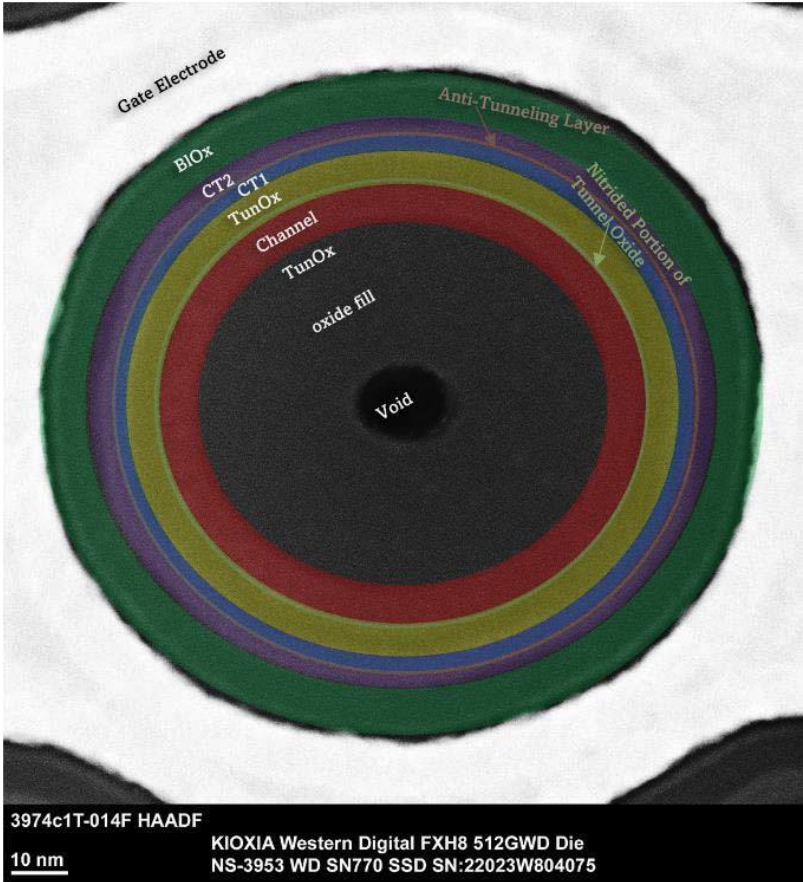
Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
[1d] wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers,	In the '240 Accused Instrumentalities the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers. For example, the multi-layer charge trapping layer comprises a first dielectric layer ("CT1" or "CT2") disposed abutting

Claim Element	'240 Accused Instrumentalities
	a second dielectric layer (“CT2” or “CT1”) and an anti-tunneling layer (“Anti-Tunneling Layer”) disposed between the first and second dielectric layers ¹⁷:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

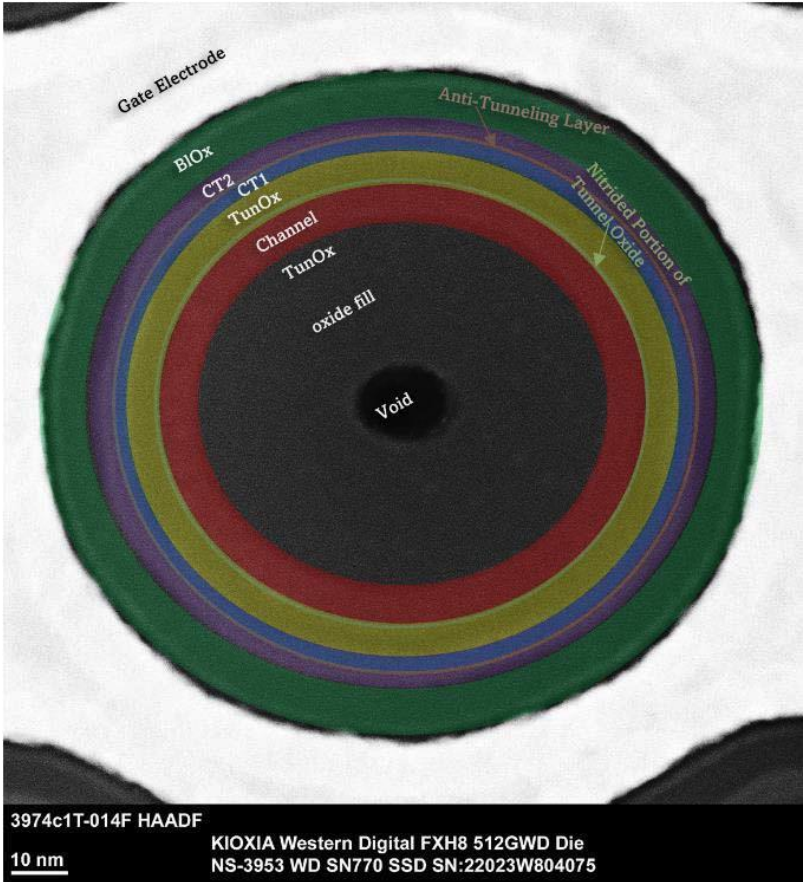
¹⁷ TechInsights 112L Report

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[1e] wherein the anti-tunneling layer includes an oxide layer, and	In the '240 Accused Instrumentalities the anti-tunneling layer includes an oxide layer. For example, an anti-tunneling layer (“Anti-Tunneling Layer”) includes an oxide layer ¹⁸ :

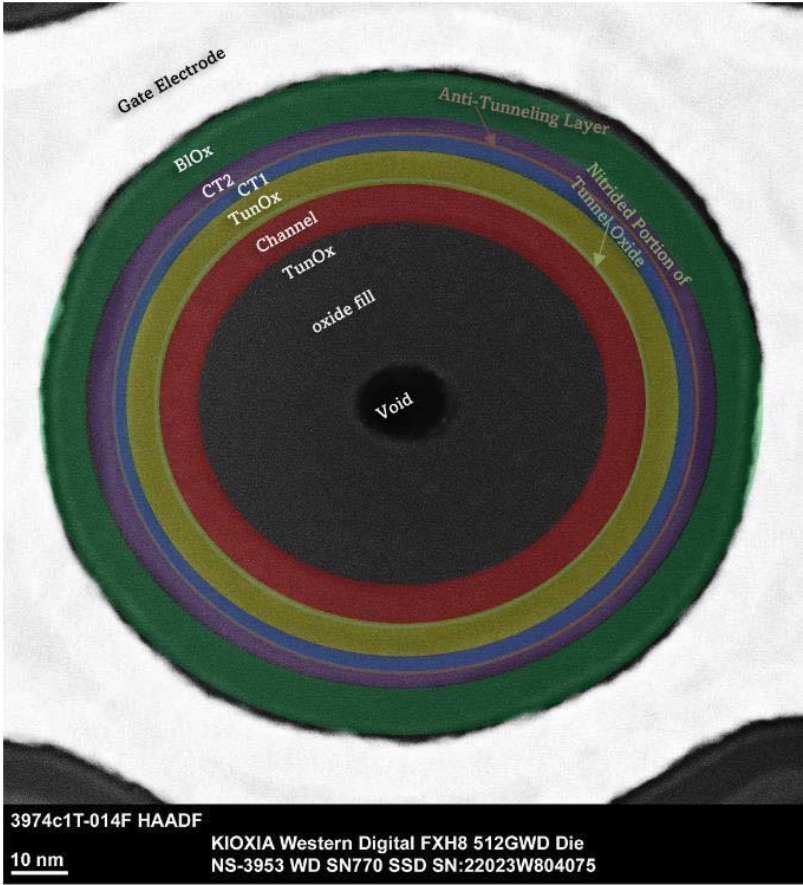
¹⁸ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
[1f] wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.	In the '240 Accused Instrumentalities the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride. For example, the first dielectric layer ("CT1" or "CT2") includes oxygen-rich nitride and the second dielectric layer ("CT2" or "CT1") includes oxygen-lean nitride ¹⁹:

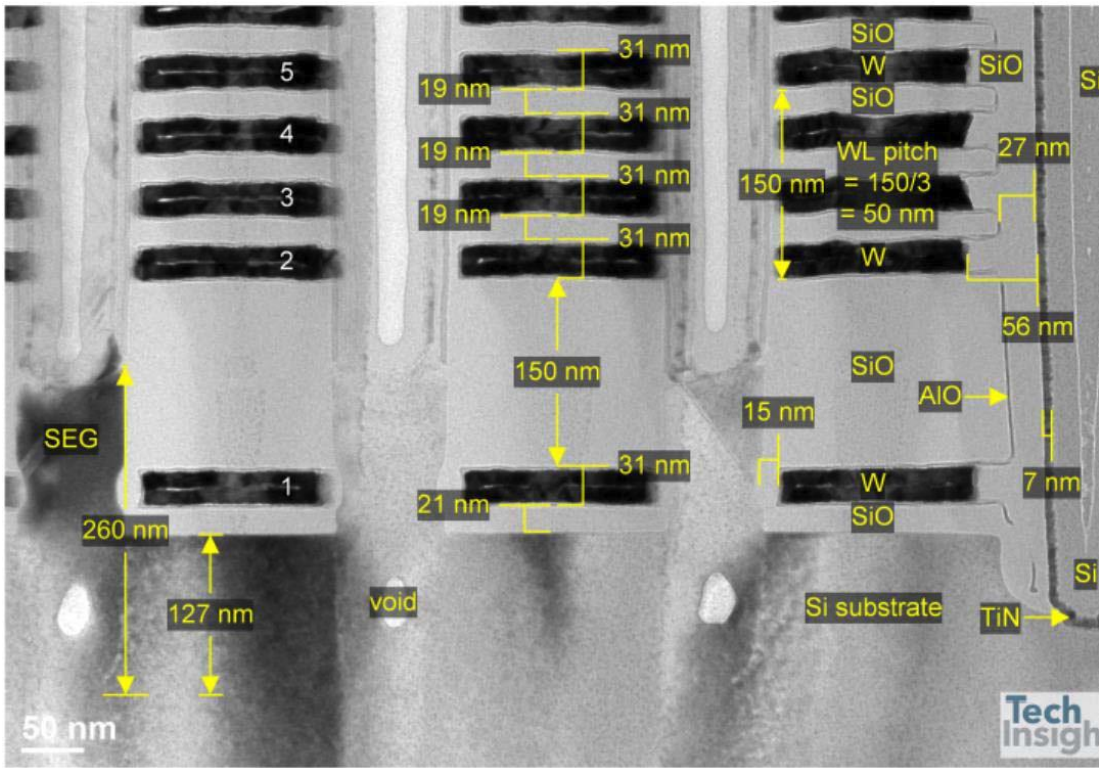
¹⁹ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
3. The memory device of claim 1, wherein the channel, first and second diffusion regions are disposed above a semiconductor material structure.	In the '240 Accused Instrumentalities the channel, first and second diffusion regions are disposed above a semiconductor material structure. For example, the channel ("Channel"), first ("CT1" or "CT2") and second ("CT2" or "CT1") diffusion regions²⁰:

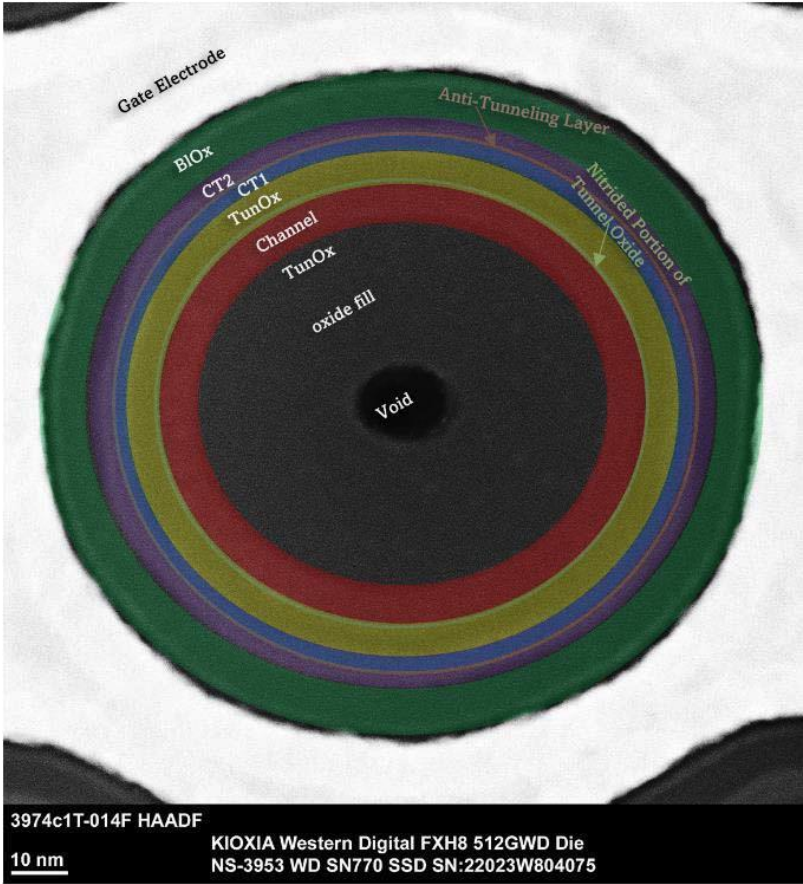
²⁰ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 are disposed above the silicon substrate²¹:

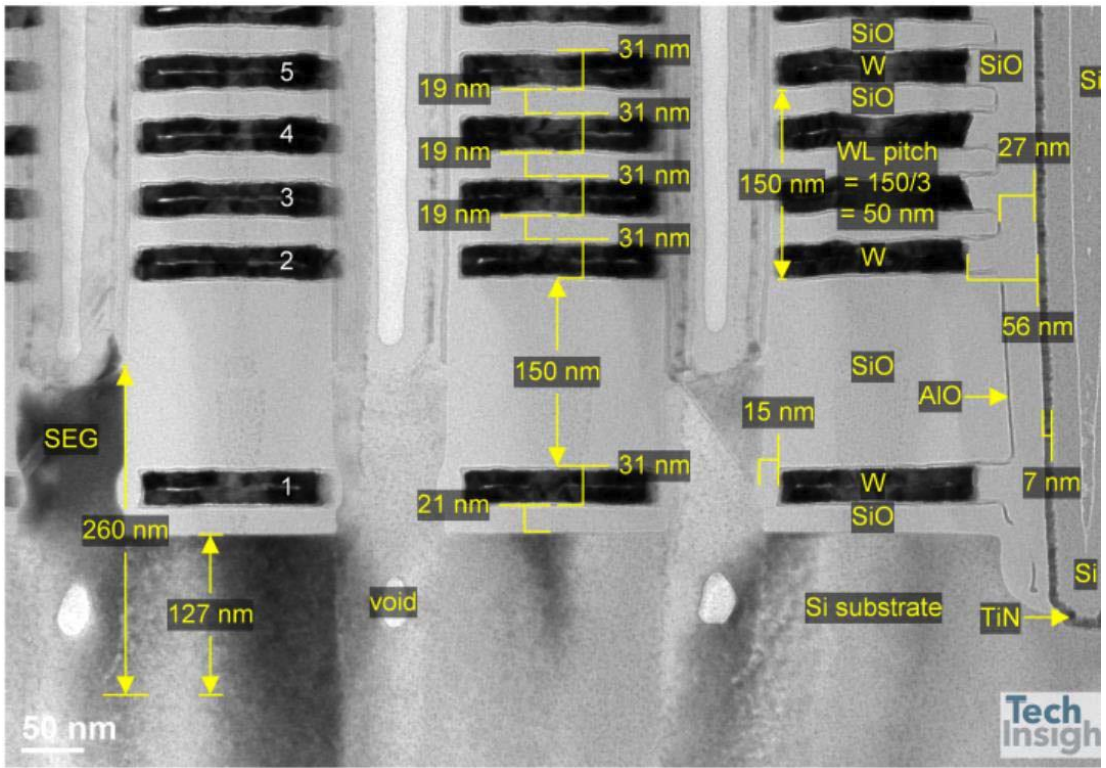
²¹ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
4. The memory device of claim 1, wherein the channel, first and second	In the '240 Accused Instrumentalities the channel, first and second diffusion regions are suspended above a semiconductor material structure. For example, the channel ("Channel"), first ("CT1" or "CT2") and second ("CT2" or "CT1") diffusion regions²²:

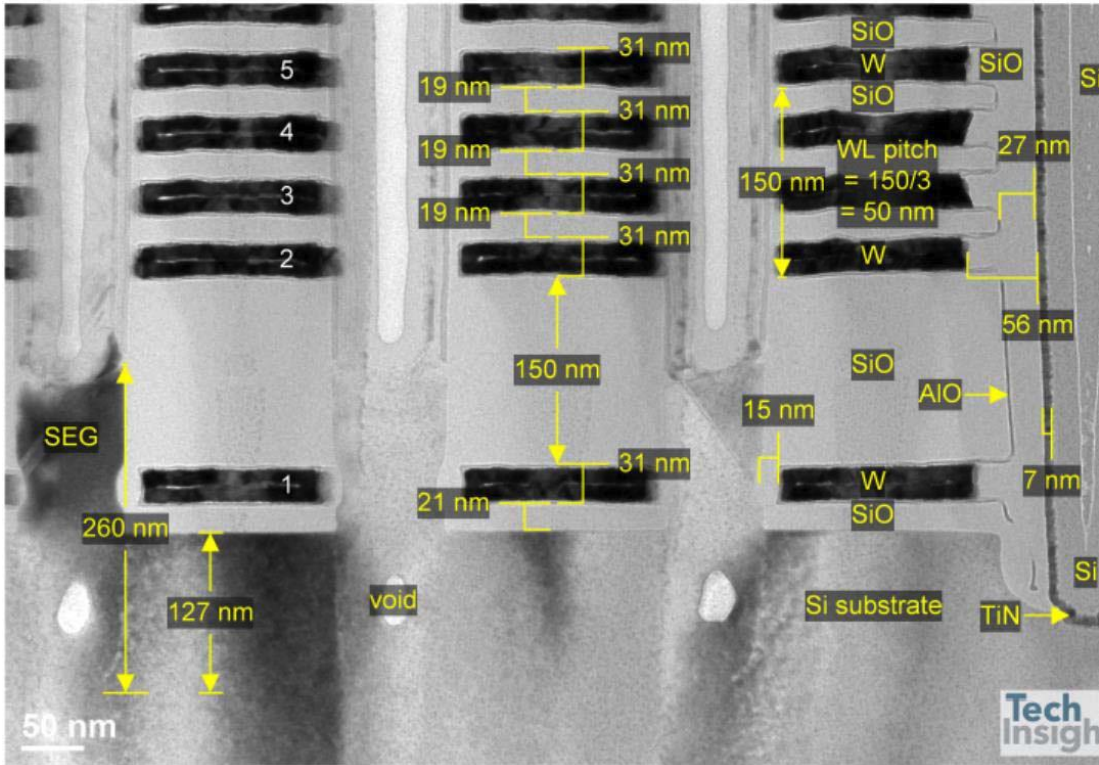
²² TechInsights 112L Report

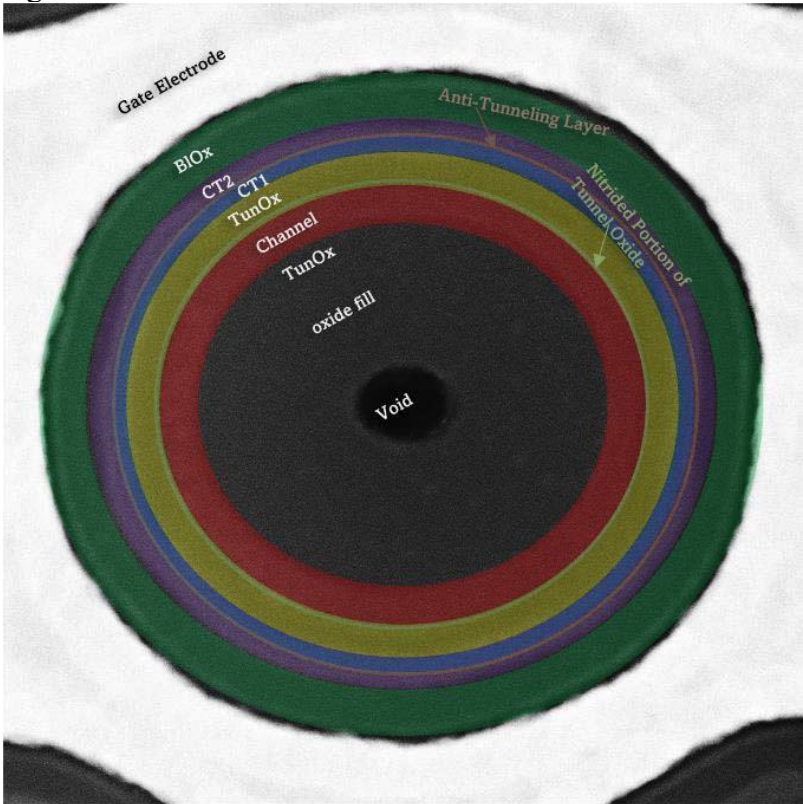
Claim Element	'240 Accused Instrumentalities
diffusion regions are suspended above a semiconductor material structure.	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 are suspended above the silicon substrate²³:

²³ TechInsights 112L Report

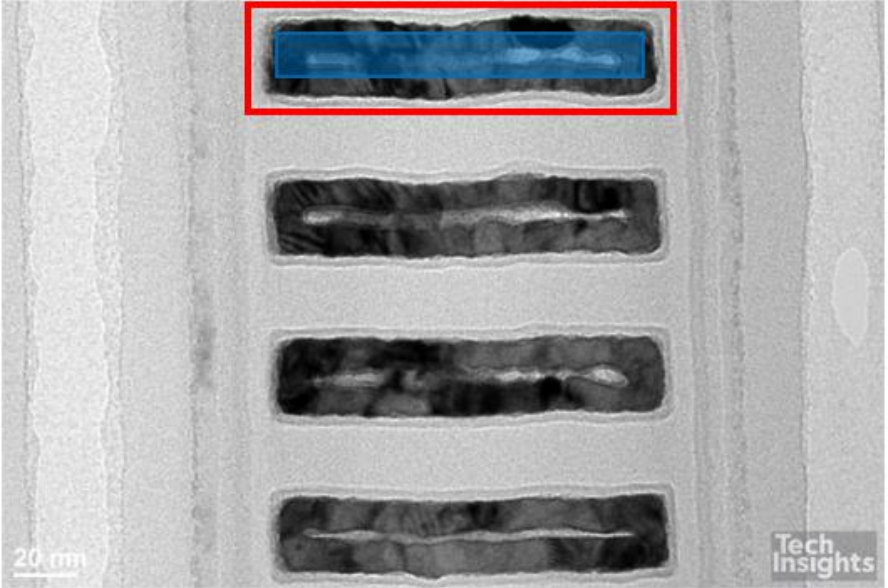
Claim Element	'240 Accused Instrumentalities
	 The image is a cross-sectional scanning electron micrograph (SEM) of a memory device. It shows a vertical channel structure. On the left, a series of horizontal lines are labeled 1 through 5. A label 'SEG' points to a specific layer. Dimensions are indicated with yellow arrows: 260 nm for the height of a section, 127 nm for the width of a channel, and 50 nm for a scale bar. In the center, a 'void' is labeled. To the right, various layers are labeled: SiO, W, SiO, WL pitch, W, SiO, AIO, W, SiO, and Si substrate. Dimensions for these layers include 31 nm, 19 nm, 150 nm, 27 nm, 56 nm, 15 nm, 7 nm, and 21 nm. A calculation is shown: WL pitch = 150/3 = 50 nm. A 'TiN' layer is also labeled at the bottom right. The 'Tech Insights' logo is in the bottom right corner. As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
5. The memory device of claim 1, wherein the channel is vertical and	In the '240 Accused Instrumentalities the channel is vertical and oriented substantially perpendicular to a semiconductor material structure. For example, the vertical channel is substantially perpendicular to the silicon substrate²⁴.

²⁴ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
oriented substantially perpendicular to a semiconductor material structure.	 The image is a cross-sectional scanning electron micrograph (SEM) of a memory device structure. It shows multiple horizontal layers and vertical structures. Key features and dimensions labeled include: Layers and Dimensions: - Top layers: 5, 4, 3, 2, 1 (numbered). - Dimensions: 19 nm, 31 nm, 150 nm, 27 nm, 56 nm, 7 nm, 15 nm, 21 nm, 127 nm, 260 nm. - Materials: SiO, W, WL pitch = 150/3 = 50 nm, SiO, AIO, Si substrate, TiN. Other Labels: SEG, void. Scale Bar: 50 nm. Logo: Tech Insight.
7. The memory device of claim 1, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO).	In the '240 Accused Instrumentalities the blocking dielectric layer comprises high K high temperature oxide (HTO). For example, the blocking dielectric layer ("BLOx") comprises aluminum oxide, a high K high temperature oxide.

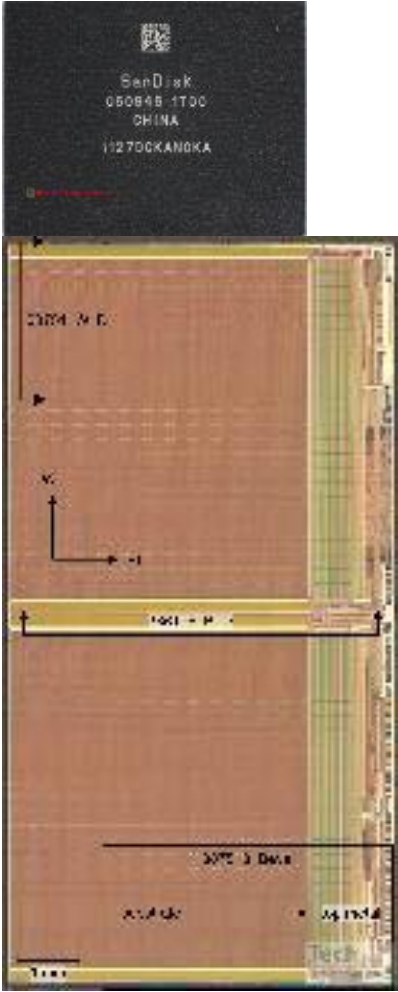
Claim Element	'240 Accused Instrumentalities
9. The memory device of claim 1, wherein the gate structure includes a high work function gate electrode.	In the '240 Accused Instrumentalities the gate structure includes a high work function gate electrode. For example, the gate electrode ("Gate Electrode") is formed from tungsten, a high work function material²⁵:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

²⁵ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	This gate structure is similarly indicated by the red box in the following image from a cross section in the perpendicular plane to the above image²⁶:  As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
12. A semiconductor device, comprising:	To the extent the preamble is deemed limiting, the '240 Accused Instrumentalities comprise a semiconductor device. For example, the WDS960G2G0C SSD contains a semiconductor die containing 112-Layer 3D NAND Flash Memory²⁷:

²⁶ TechInsights 112L Report

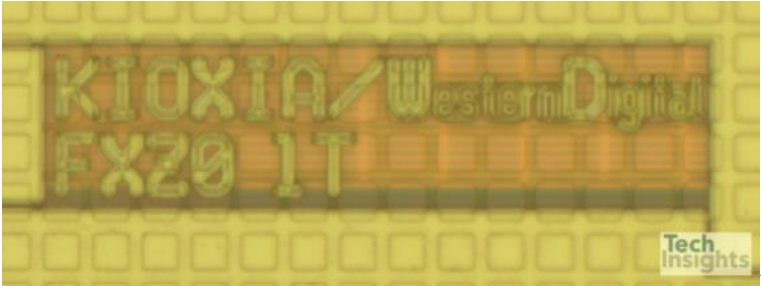
²⁷ TechInsights, Kioxia/Western Digital WDS960G2G0C SSD, SanDisk 060946 1T00 (FXH8 512G Die), 112-Layer 3D NAND Flash Memory, 18 nm Process Node, Advanced Memory Essentials, AME-2106-802, Published: November 19, 2021 ("TechInsights 112L Report")

Claim Element	'240 Accused Instrumentalities
	 Die markings on this and other '240 Accused Instrumentalities indicate that they are each made by a joint venture owned by Toshiba/Kioxia and Sandisk/Western Digital:

Claim Element	'240 Accused Instrumentalities
	²⁸ 12 Package Optical - Package X-ray - Die Optical\TH58LJT0T24BADE_FST0_256G_336534_DieMk-100X.png ²⁹

²⁸ Image of Western Digital Green SSD (P/N WDS480G2G0A) (96L)

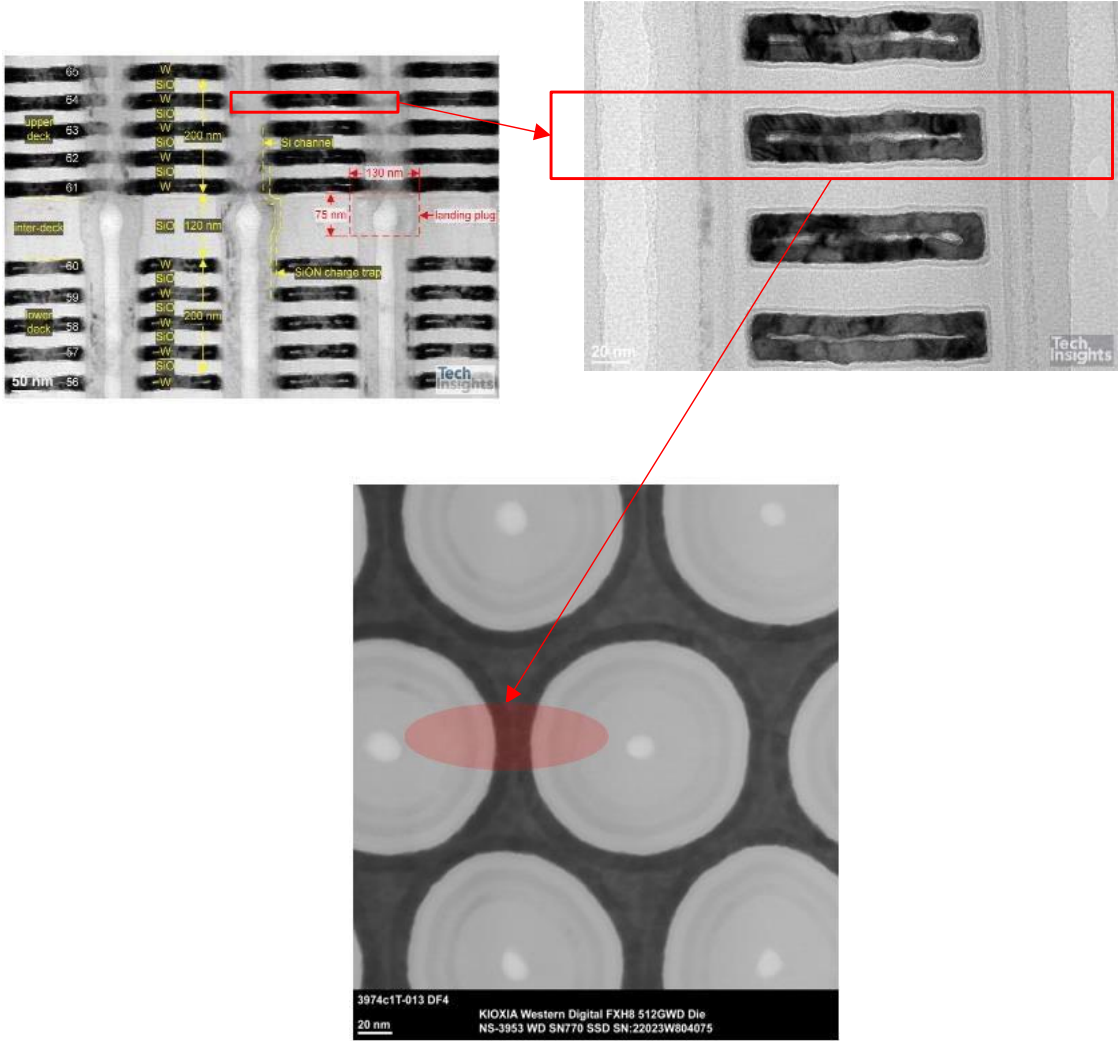
²⁹ TechInsights 112L Report

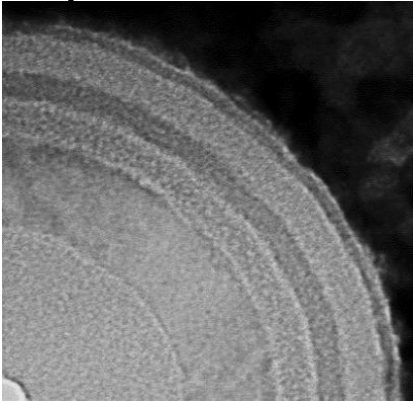
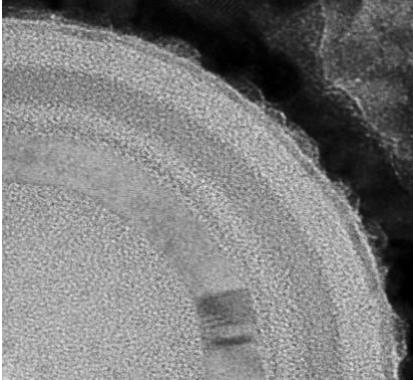
Claim Element	'240 Accused Instrumentalities
	 
[12a] a memory device including,	The '240 Accused Instrumentalities comprise a memory device. For example, the following images each show multiple memory transistors, in different cross sections of a 112L accused product³²:

³⁰ TechInsights, Toshiba TH58LKT3B46BA8S (KIOXIA/Western Digital Corp. FXZ0_1T die), 162-Layer 3D NAND Flash Memory, Advanced Memory Essentials, AME-2310-803, Published: February 29, 2024 (“TechInsights 162L Report”)

³¹ TechInsights, KIOXIA/WDC FYU6_1T 218L (BiCS8), Triple-Level Cell (TLC) 1 Tb 3D NAND Flash, Advanced Memory Essentials, AME-2407-801, Published: November 29, 2024 (“TechInsights 218L Report”)

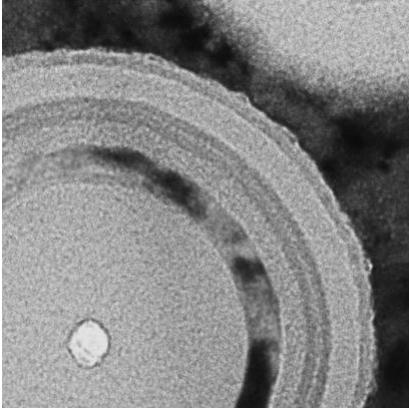
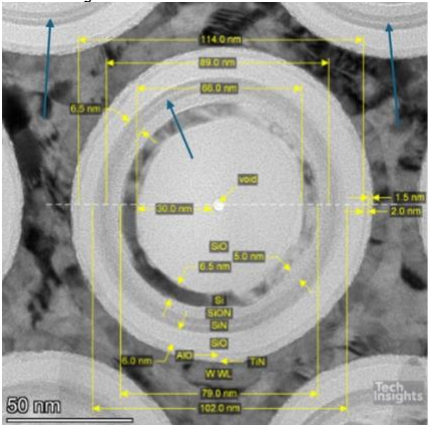
³² TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 The images show cross-sectional views of a NAND flash die. The top image is a high-magnification view of a single cell, showing the Si channel, SiON charge trap, and landing plug. The middle image shows a larger area with labels for upper deck, inter-deck, and lower deck. The bottom image shows a circular array of cells, with a red oval highlighting a specific cell. Red arrows connect the labels in the top image to the corresponding features in the middle and bottom images.

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	Similar memory transistor structures are present in each of the '240 Accused Instrumentalities, as shown in the following cross section images. 64-layer³³:  96-layer³⁴: 

³³ TechInsights, Memory DRAM & NAND Tri-Annual Briefing #1, 2022, Report ID: BRF-2112-810, May 2022, p. 47,

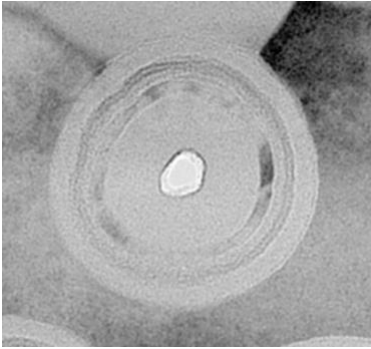
³⁴ *Id.*

Claim Element	'240 Accused Instrumentalities
	112-layer³⁵:  162-layer³⁶:  218-layer³⁷:

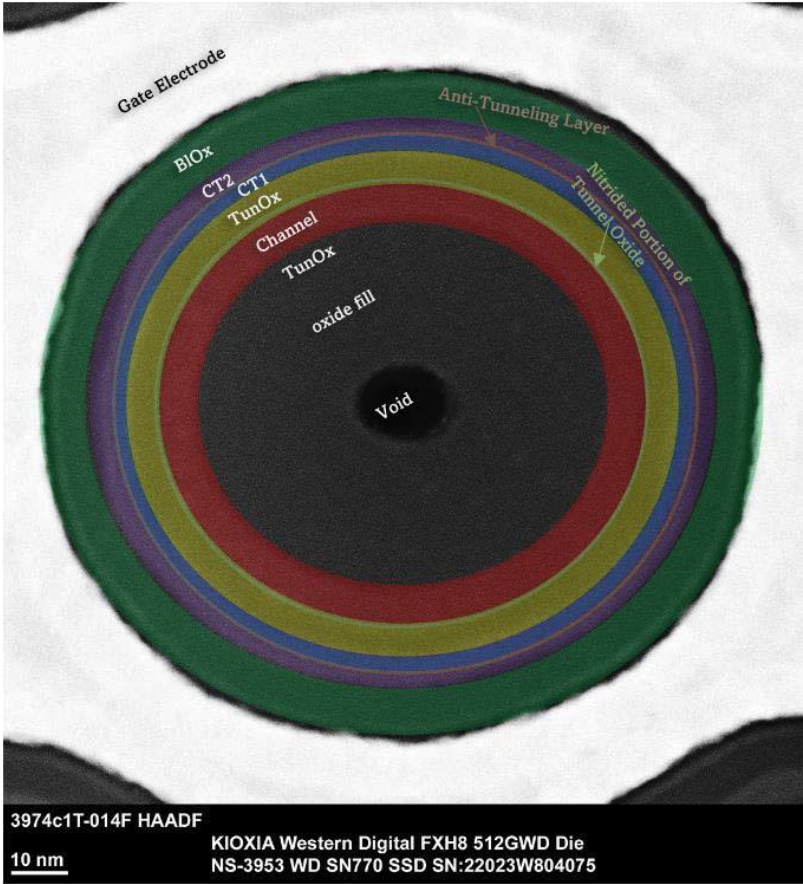
³⁵ *Id.*

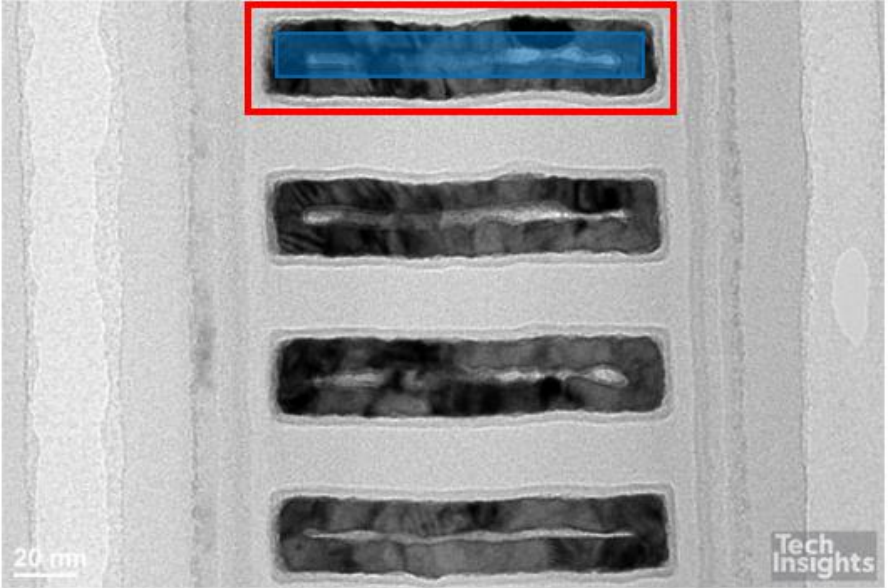
³⁶ TechInsights 162L Report

³⁷ TechInsights 218L Report

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	
[12b] a gate structure including a first high work function gate electrode,	The '240 Accused Instrumentalities comprise a gate structure including a first high work function gate electrode. For example, the gate electrode (“Gate Electrode”) is formed from tungsten, a high work function material ³⁸ :

³⁸ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 The diagram shows a cross-section of a memory cell with the following layers from the center outwards: Void: The central core. oxide fill: The layer immediately surrounding the void. Channel: The layer surrounding the oxide fill. TunOx: The layer surrounding the channel. Nitrided Portion of Tunnel Oxide: A specific region of the tunnel oxide layer. Anti-Tunneling Layer: The layer surrounding the nitrided portion. CT1 and CT2: Control gate layers. TunOx: Another tunnel oxide layer. BiOx: Barrier oxide layer. Gate Electrode: The outermost layer. 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

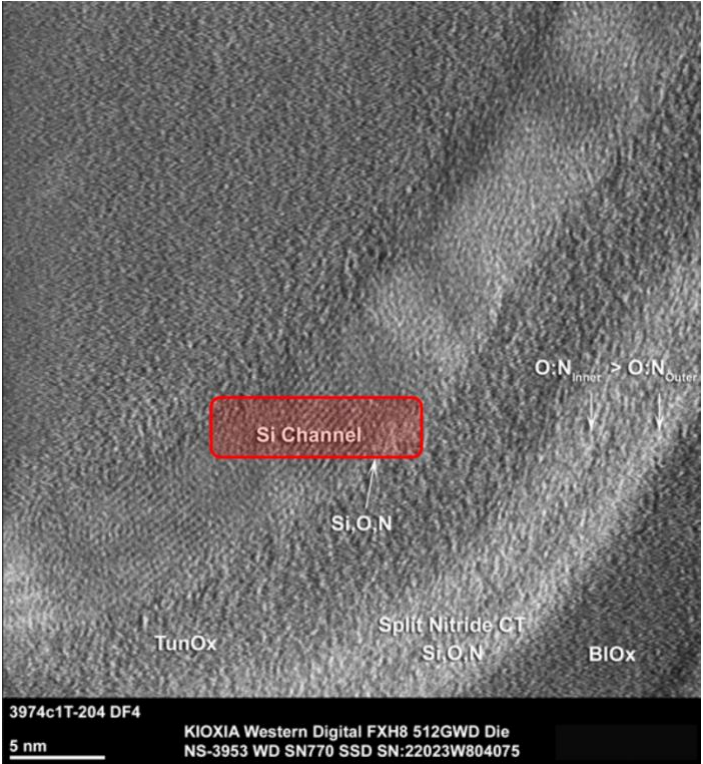
Claim Element	'240 Accused Instrumentalities
	This gate structure is similarly indicated by the red box in the following image from a cross section in the perpendicular plane to the above image³⁹:  As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[12c] a channel positioned between and electrically connecting a first diffusion region and a second diffusion region,	The '240 Accused Instrumentalities comprise a channel positioned between and electrically connecting a first diffusion region and a second diffusion region. For example, the '240 Accused Instrumentalities contain vertical tube structures between a bottom first diffusion region and a top second diffusion region⁴⁰:

³⁹ TechInsights 112L Report

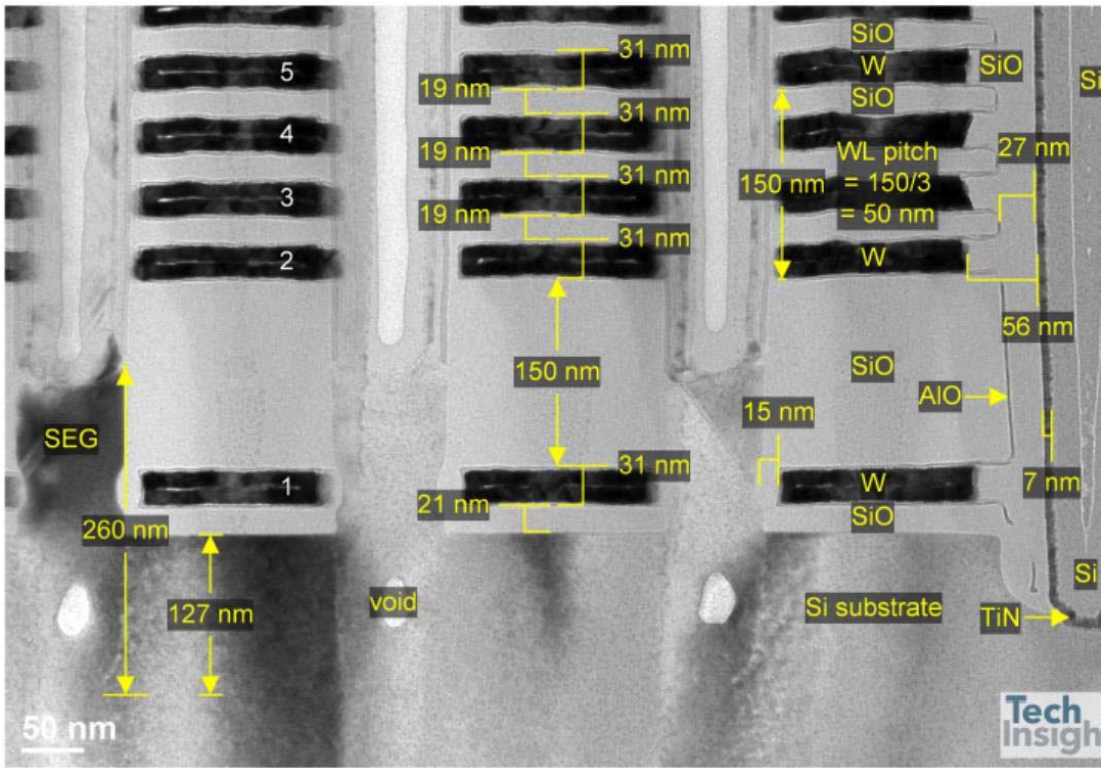
⁴⁰ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	The vertical tubes contain a silicon channel that electrically connect the first and second diffusion regions⁴¹:

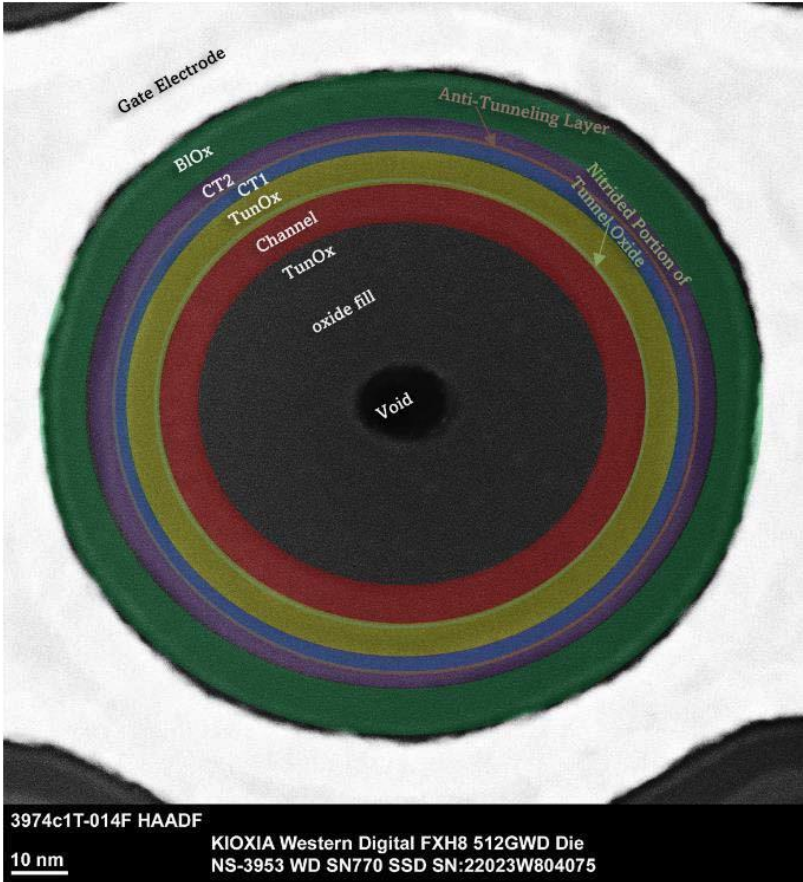
⁴¹ *Id.*

Claim Element	'240 Accused Instrumentalities
	
[12d] wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and	In the '240 Accused Instrumentalities the channel is vertical and oriented substantially perpendicular to a semiconductor material structure. For example, the vertical channel is substantially perpendicular to the silicon substrate ⁴² :

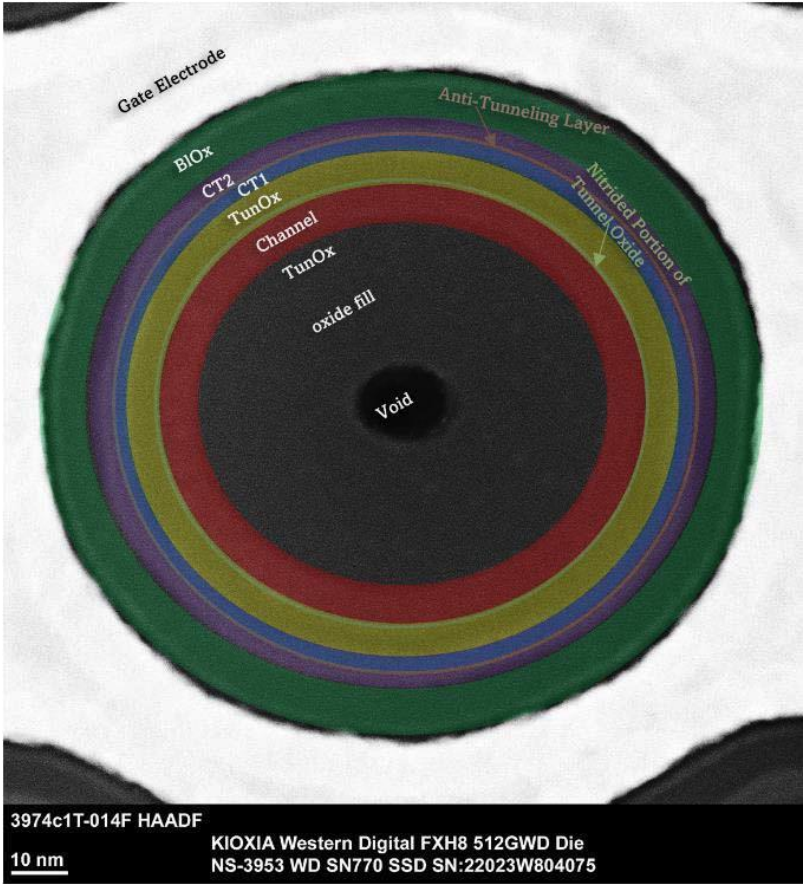
⁴² TechInsights 112L Report

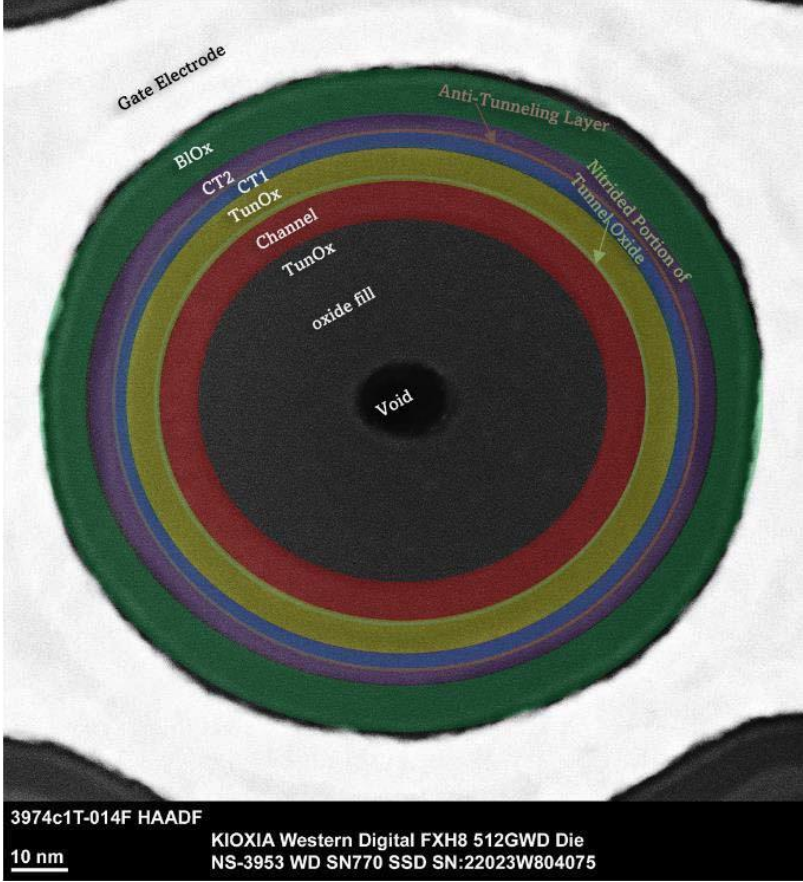
Claim Element	'240 Accused Instrumentalities
	 The image is a cross-sectional scanning electron micrograph (SEM) of a semiconductor device. It shows a Si substrate at the bottom, covered by a TiN layer. Above the TiN is a SiO₂ layer, followed by a W layer, and another SiO₂ layer. A WL pitch of 150 nm is indicated, which is divided into three 50 nm segments. Other layers include SiO₂, W, and SiO₂ with thicknesses of 27 nm, 56 nm, 15 nm, and 7 nm. A void is present in the center. A SEG layer is shown with a thickness of 260 nm. Other dimensions include 19 nm, 31 nm, 150 nm, 21 nm, and 127 nm. A 50 nm scale bar is at the bottom left. The TechInsights logo is at the bottom right.
[12e] a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel,	The '240 Accused Instrumentalities comprise] a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel. For example, the tunnel dielectric layer (yellow "TunOx"), multi-layer charge trapping layer ("CT1," "Anti-Tunneling Layer," "CT2"), and blocking dielectric layer ("BlOx") are disposed between the gate structure ("Gate Electrode") and the channel ("Channel")⁴³:

⁴³ TechInsights 112L Report

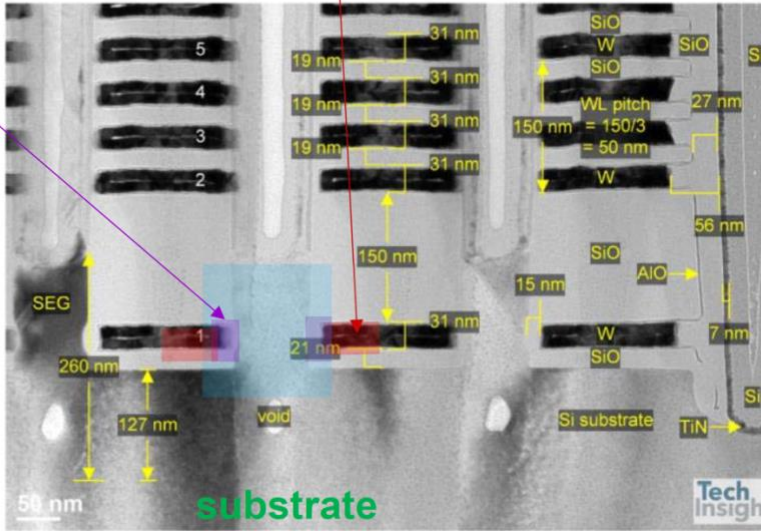
Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
[12f] wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,	In the '240 Accused Instrumentalities the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer. For example, the multi-layer charge trapping layer comprises a first dielectric layer ("CT1" or "CT2") disposed abutting a second dielectric layer ("CT2" or "CT1")⁴⁴:

⁴⁴ TechInsights 112L Report

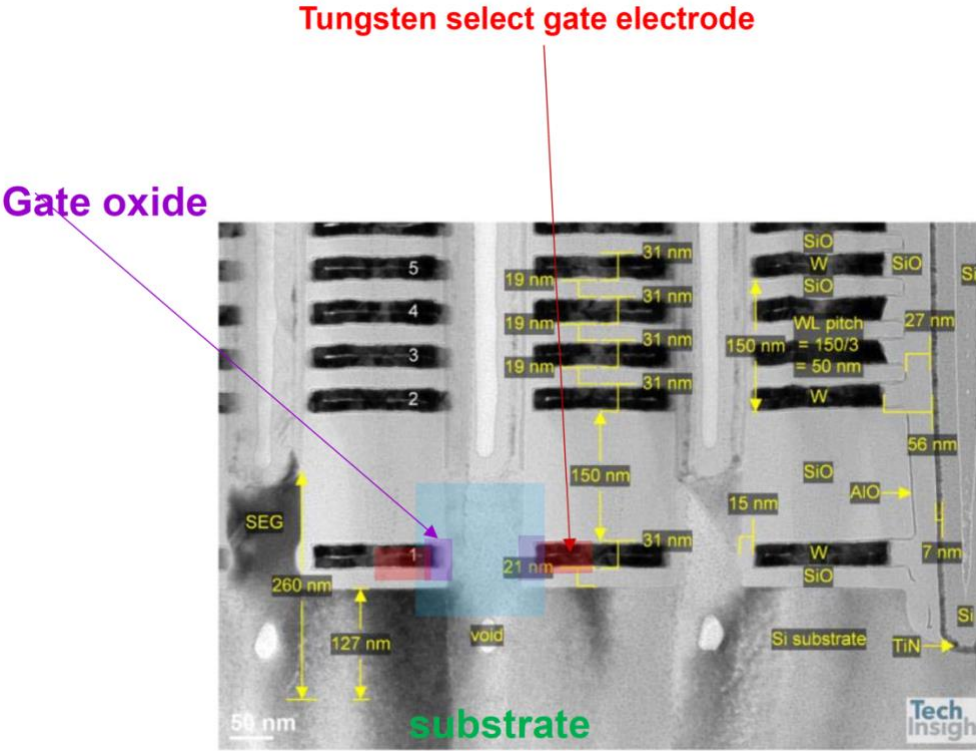
Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[12g] wherein the first dielectric layer includes oxygen-rich nitride and the	In the '240 Accused Instrumentalities the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride. For example, the first

Claim Element	'240 Accused Instrumentalities
second dielectric layer includes oxygen-lean nitride; and	dielectric layer ("CT1" or "CT2") includes oxygen-rich nitride and the second dielectric layer ("CT2" or "CT1") includes oxygen-lean nitride ⁴⁵:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075
[12h] a metal oxide semiconductor (MOS) logic device including a gate	The '240 Accused Instrumentalities comprise a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode

⁴⁵ TechInsights 112L Report

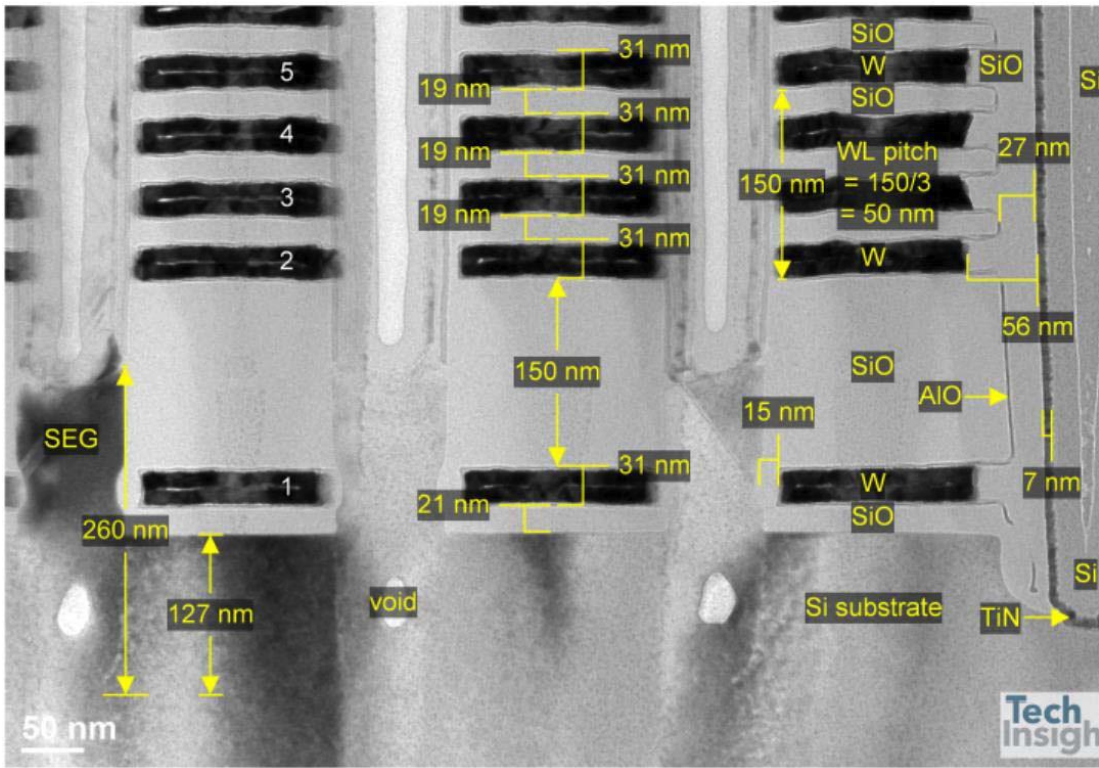
Claim Element	'240 Accused Instrumentalities
oxide layer and a second high work function gate electrode disposed thereon.	disposed thereon. For example, there are MOS logic transistors on the silicon substrate, which comprise a gate oxide layer (“Gate oxide”) and a high work function gate electrode (“Tungsten select gate electrode”) disposed thereon⁴⁶:  The image is a cross-sectional scanning electron micrograph (SEM) of a MOS logic transistor. It shows a silicon (Si) substrate at the base, covered by a thin layer of titanium nitride (TiN). Above the TiN is a layer of silicon dioxide (SiO₂) with a thickness of 7 nm. A layer of aluminum oxide (AlO) with a thickness of 15 nm is also present. The gate stack consists of a gate oxide layer (labeled 'Gate oxide' with a purple arrow) and a tungsten select gate electrode (labeled 'Tungsten select gate electrode' with a red arrow). The gate oxide has a thickness of 21 nm. The tungsten select gate electrode has a thickness of 31 nm. The gate stack is surrounded by a layer of silicon dioxide (SiO₂) with a thickness of 56 nm. The word 'void' is labeled in the center of the gate stack. Other dimensions shown include 260 nm, 127 nm, 19 nm, 150 nm, 31 nm, 27 nm, and 50 nm. The image is watermarked with 'TechInsigh' in the bottom right corner. As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.

⁴⁶ TechInsights 112L Report

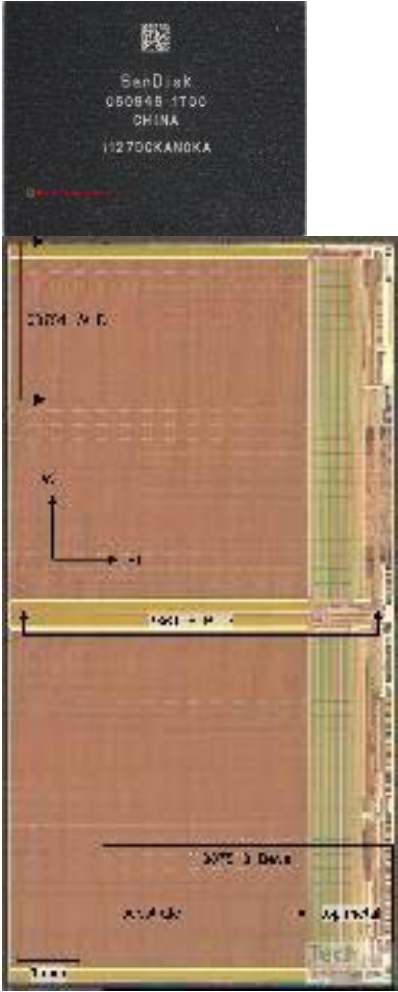
Claim Element	'240 Accused Instrumentalities
14. The semiconductor device of claim 12, wherein the MOS logic device is formed at least partially within a semiconductor material structure.	In the '240 Accused Instrumentalities the MOS logic device is formed at least partially within a semiconductor material structure. For example, the MOS logic device is formed at least partially within the silicon substrate⁴⁷: 
15. The semiconductor device of claim 14, wherein the channel is vertical and oriented substantially	In the '240 Accused Instrumentalities the channel is vertical and oriented substantially orthogonal to the semiconductor material structure. For example, the vertical channel is substantially perpendicular to the silicon substrate⁴⁸:

⁴⁷ TechInsights 112L Report

⁴⁸ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
orthogonal to the semiconductor material structure.	 The image is a cross-sectional scanning electron micrograph (SEM) of a 3D NAND Flash Memory structure. It shows multiple layers of material, including SiO₂, W (tungsten), Si, and SiO₂. Dimensions are labeled in nanometers (nm): 5, 4, 3, 2, 1, 260 nm, 127 nm, 19 nm, 31 nm, 150 nm, 21 nm, 15 nm, 27 nm, 56 nm, 7 nm, and 50 nm. A 'void' is indicated in the center. A 'SEG' (select gate) is labeled on the left. A 'Si substrate' is labeled at the bottom right. A 'TiN' (titanium nitride) layer is also indicated. The 'WL pitch' (word line pitch) is calculated as 150 nm / 3 = 50 nm. The image is watermarked with 'Tech Insights' in the bottom right corner.
16. A semiconductor device, comprising:	To the extent the preamble is deemed limiting, the '240 Accused Instrumentalities comprise a semiconductor device. For example, the WDS960G2G0C SSD contains a semiconductor die containing 112-Layer 3D NAND Flash Memory ⁴⁹ :

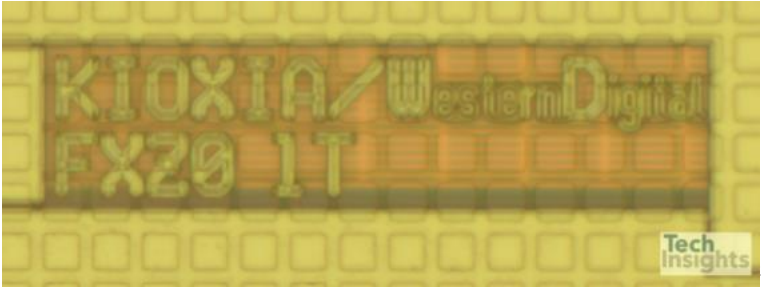
⁴⁹ TechInsights, Kioxia/Western Digital WDS960G2G0C SSD, SanDisk 060946 1T00 (FXH8 512G Die), 112-Layer 3D NAND Flash Memory, 18 nm Process Node, Advanced Memory Essentials, AME-2106-802, Published: November 19, 2021 ("TechInsights 112L Report")

Claim Element	'240 Accused Instrumentalities
	 Die markings on this and other '240 Accused Instrumentalities indicate that they are each made by a joint venture owned by Toshiba/Kioxia and Sandisk/Western Digital:

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	 12 Package Optical - Package X-ray - Die Optical\TH58LJT0T24BADE_FST0_256G_336534_DieMik-100X.png 50  51

⁵⁰ Image of Western Digital Green SSD (P/N WDS480G2G0A) (96L)

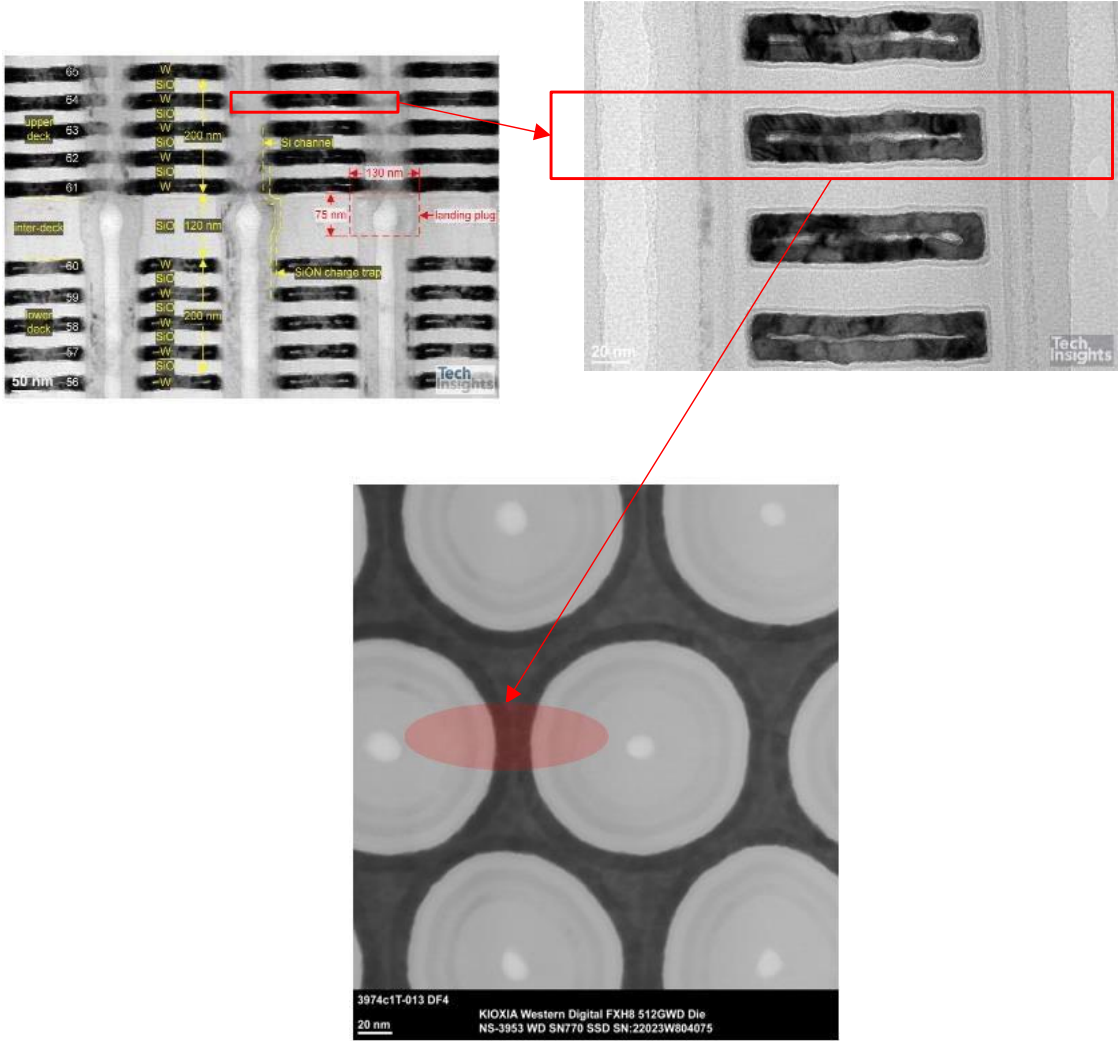
⁵¹ TechInsights 112L Report

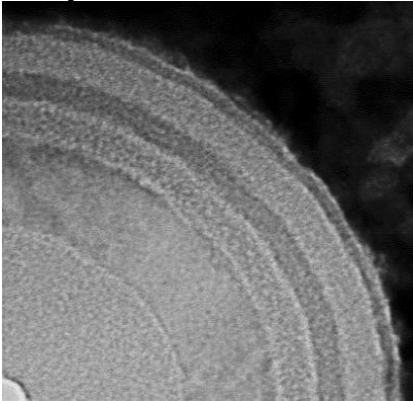
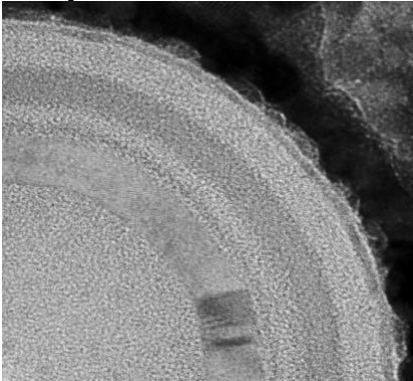
Claim Element	'240 Accused Instrumentalities
	 
[16a] a memory device including,	The '240 Accused Instrumentalities comprise a memory device. For example, the following images each show multiple memory transistors, in different cross sections of a 112L accused product⁵⁴:

⁵² TechInsights, Toshiba TH58LKT3B46BA8S (KIOXIA/Western Digital Corp. FXZ0_1T die), 162-Layer 3D NAND Flash Memory, Advanced Memory Essentials, AME-2310-803, Published: February 29, 2024 (“TechInsights 162L Report”)

⁵³ TechInsights, KIOXIA/WDC FYU6_1T 218L (BiCS8), Triple-Level Cell (TLC) 1 Tb 3D NAND Flash, Advanced Memory Essentials, AME-2407-801, Published: November 29, 2024 (“TechInsights 218L Report”)

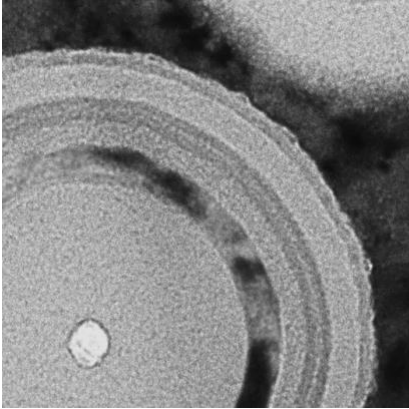
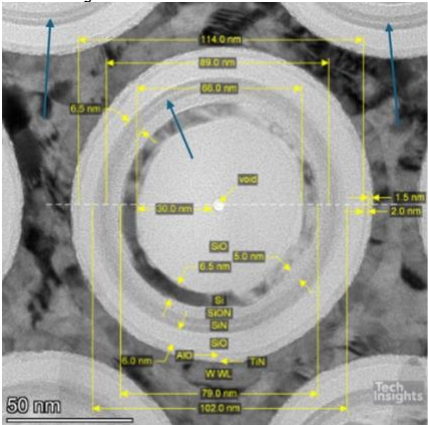
⁵⁴ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 The images illustrate the structure of the '240 accused instrumentalities. The top-left image is a cross-sectional SEM view of a NAND flash array, showing multiple layers and dimensions. Labels include: W, SiC, SiON, Si channel, SiON charge trap, landing plug, and dimensions of 200 nm, 120 nm, 75 nm, and 130 nm. The top-right image is a magnified view of a single cell, showing the Si channel and SiON charge trap. The bottom image is a high-magnification view of a single cell, showing the Si channel and SiON charge trap. A red oval highlights a specific feature in the bottom image. The bottom image includes a 20 nm scale bar and technical data: 3974c1T-013 DF4, KIOXIA Western Digital FXH8 512GWD Die, NS-3953 WD SN770 SSD SN-22023W804075.

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	Similar memory transistor structures are present in each of the '240 Accused Instrumentalities, as shown in the following cross section images. 64-layer⁵⁵:  96-layer⁵⁶: 

⁵⁵ TechInsights, Memory DRAM & NAND Tri-Annual Briefing #1, 2022, Report ID: BRF-2112-810, May 2022, p. 47,

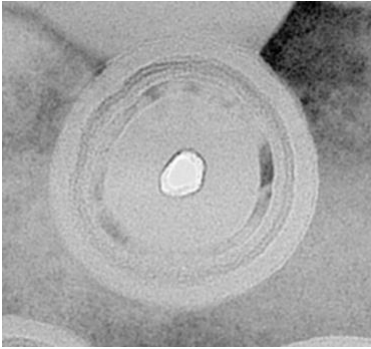
⁵⁶ *Id.*

Claim Element	'240 Accused Instrumentalities
	112-layer⁵⁷:  162-layer⁵⁸:  218-layer⁵⁹:

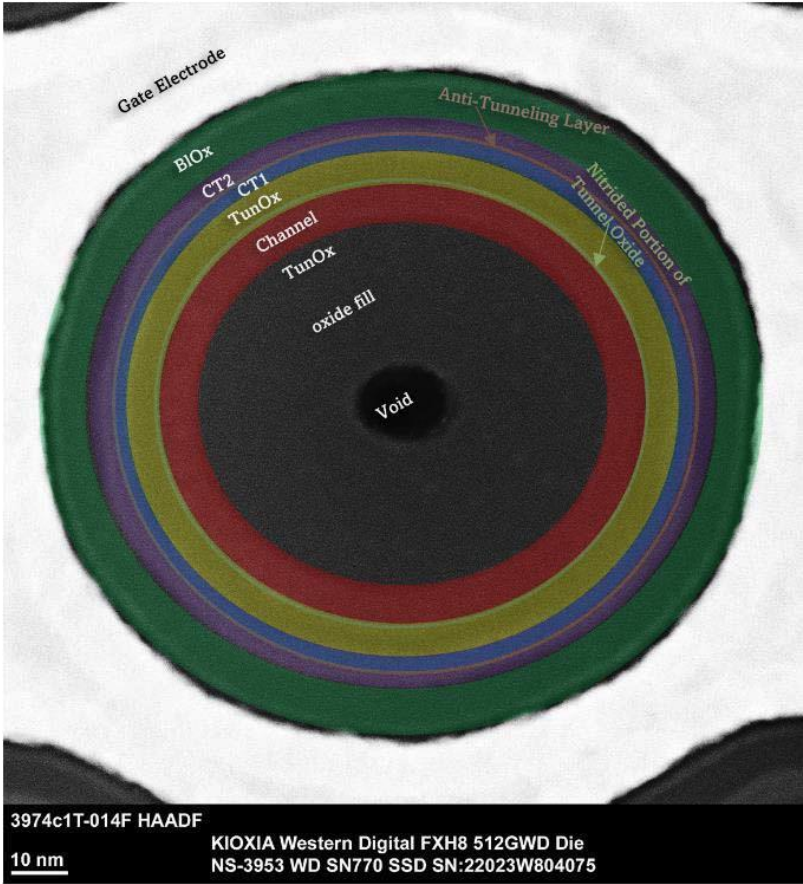
⁵⁷ *Id.*

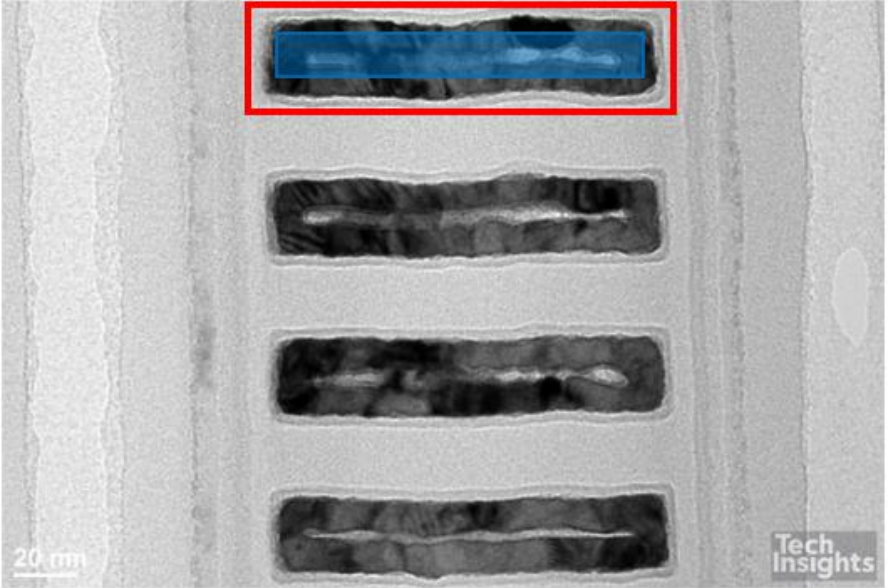
⁵⁸ TechInsights 162L Report

⁵⁹ TechInsights 218L Report

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	 A grayscale micrograph showing a circular gate structure on a substrate. The structure consists of a central circular region surrounded by concentric rings. The central region is slightly darker than the surrounding rings.
[16b] a gate structure including a first high work function gate electrode,	The '240 Accused Instrumentalities comprise a gate structure including a first high work function gate electrode. For example, the gate electrode (“Gate Electrode”) is formed from tungsten, a high work function material ⁶⁰ :

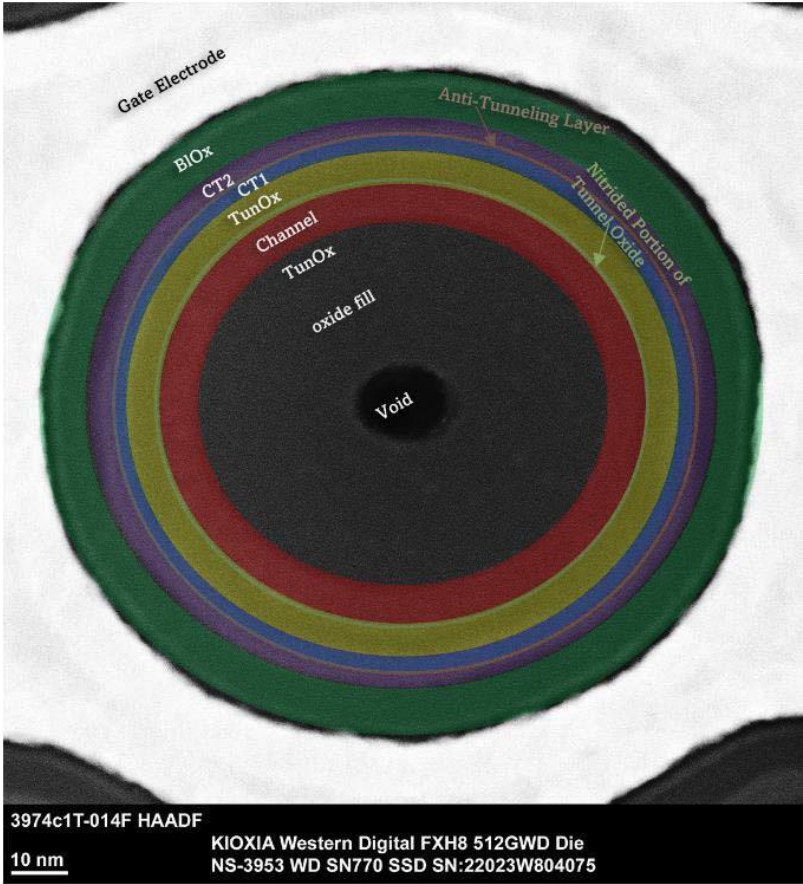
⁶⁰ TechInsights 112L Report

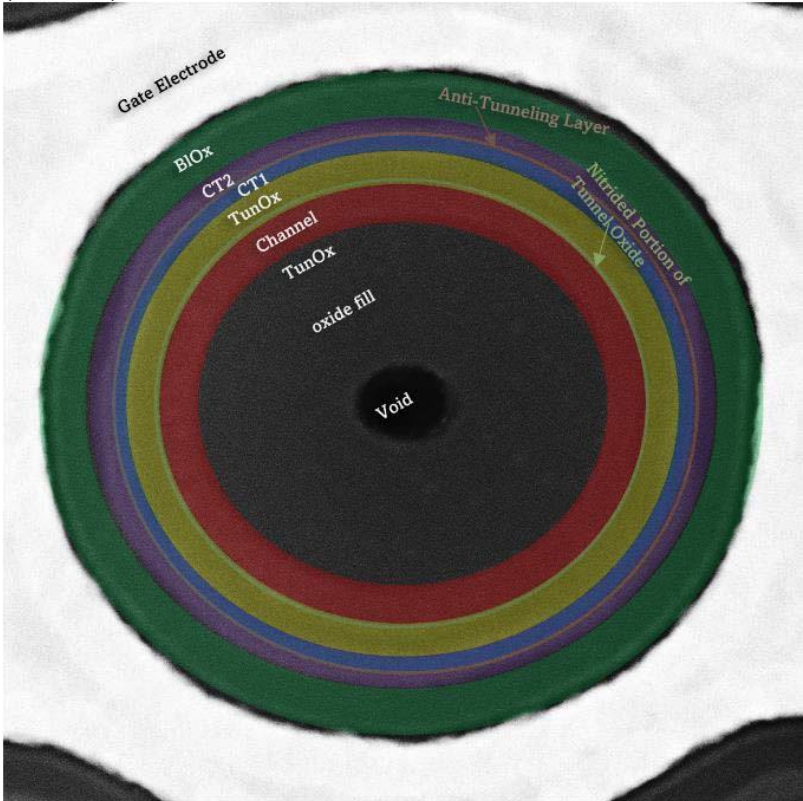
Claim Element	'240 Accused Instrumentalities
	 The diagram shows a cross-section of a memory cell with the following layers from the center outwards: Void: The central core. oxide fill: The layer immediately surrounding the void. Channel: The layer surrounding the oxide fill. TunOx: The layer surrounding the channel. Nitrided Portion of Tunnel Oxide: A specific region of the tunnel oxide layer. Anti-Tunneling Layer: The layer surrounding the nitrided portion. CT1 and CT2: Control gate layers. TunOx: Another tunnel oxide layer. BiOx: Barrier oxide layer. Gate Electrode: The outermost layer. 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

Claim Element	'240 Accused Instrumentalities
	This gate structure is similarly indicated by the red box in the following image from a cross section in the perpendicular plane to the above image⁶¹:  As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[16c] a blocking dielectric layer disposed abutting the gate structure,	The '240 Accused Instrumentalities comprise a blocking dielectric layer disposed abutting the gate structure. For example, the blocking dielectric layer ("BIOx") abuts the gate structure ("Gate Electrode")⁶²:

⁶¹ TechInsights 112L Report

⁶² TechInsights 112L Report

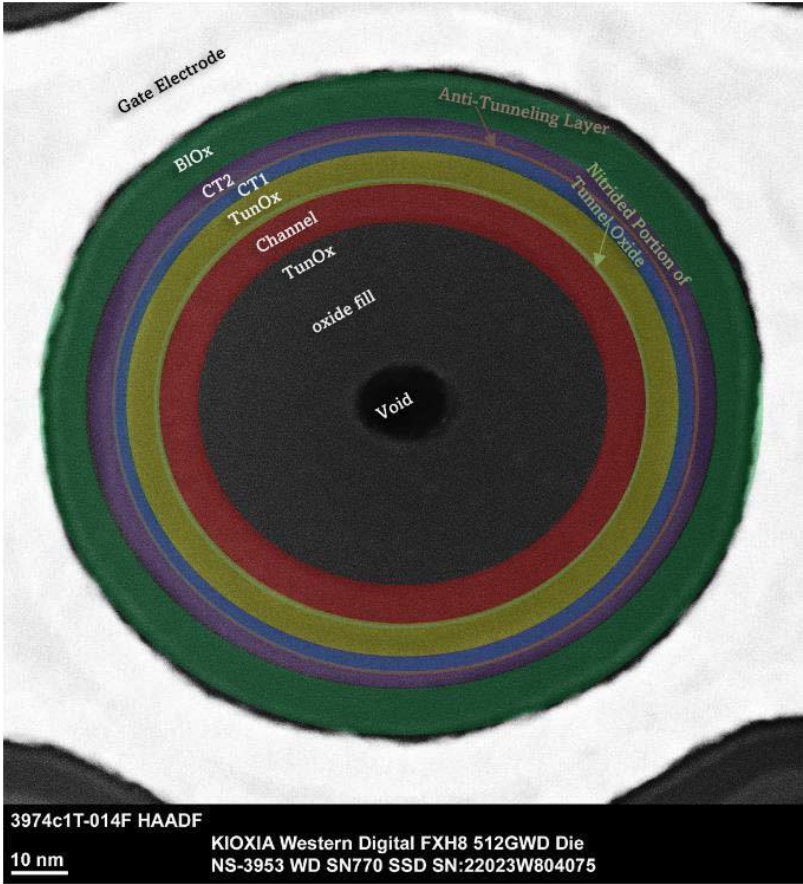
Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.

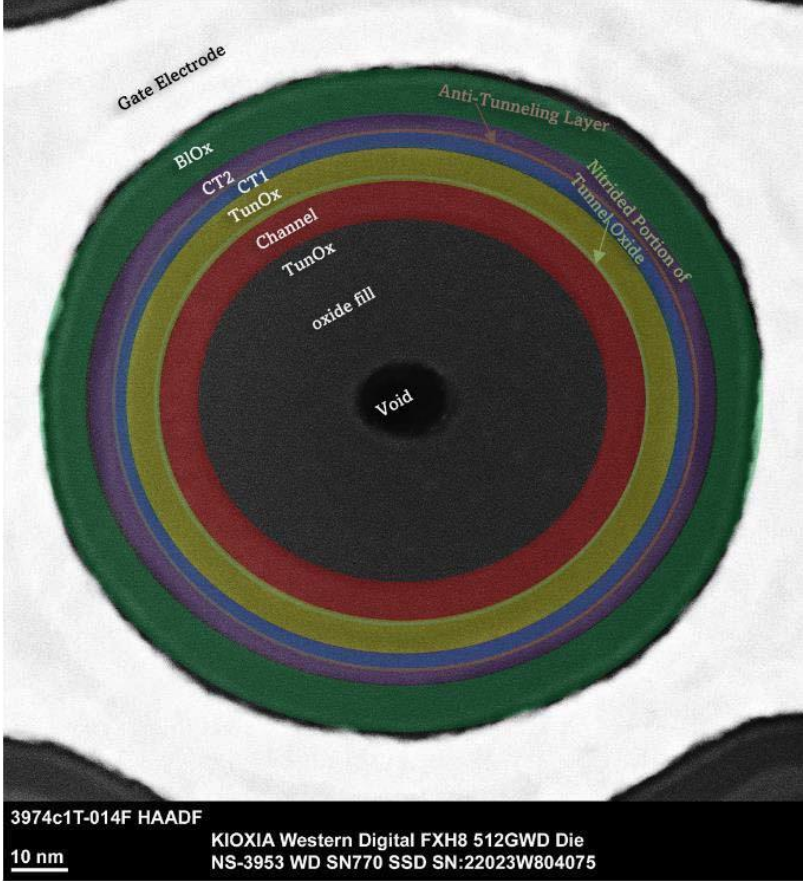
Claim Element	'240 Accused Instrumentalities
[16d] a multi-layer charge trapping layer disposed abutting the blocking dielectric layer,	The '240 Accused Instrumentalities comprise a multi-layer charge trapping layer disposed abutting the blocking dielectric layer. For example, the multi-layer charge trapping layer ("CT1," "Anti-Tunneling Layer," "CT2") is disposed abutting the blocking dielectric layer ("BIOx")⁶³:  The diagram is a cross-sectional view of a memory cell, likely a NOR-type flash. It shows a central circular void surrounded by concentric layers. From the center outwards, the layers are: oxide fill, Channel, TunOx, CT1, CT2, BIOx, and Gate Electrode. An Anti-Tunneling Layer is shown as a thin layer between the BIOx and the Gate Electrode. A Nitrided Portion of Tunnel Oxide is also indicated. The diagram is labeled with '3974c1T-014F HAADF' and '10 nm' scale bar. Below the diagram, text identifies the source as 'KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075'.

⁶³ TechInsights 112L Report

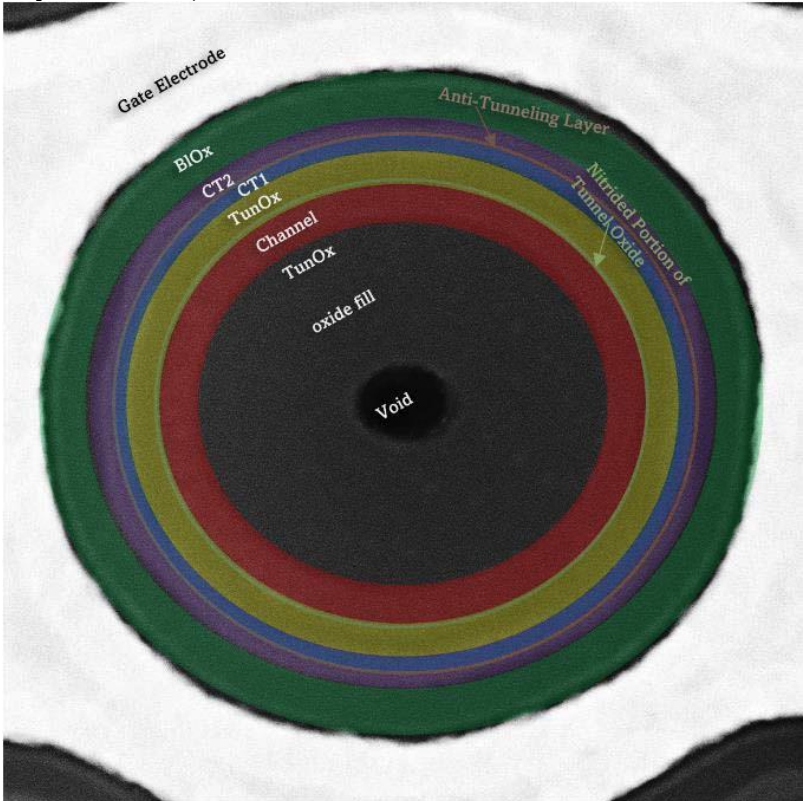
<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[16e] wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,	In the '240 Accused Instrumentalities the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer. For example, the multi-layer charge trapping layer comprises a first dielectric layer (“CT1” or “CT2”) disposed abutting a second dielectric layer (“CT2” or “CT1”) ⁶⁴ :

⁶⁴ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[16f] wherein the first dielectric layer includes oxygen-rich nitride and the	In the '240 Accused Instrumentalities the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride. For example, the first

Claim Element	'240 Accused Instrumentalities
second dielectric layer includes oxygen-lean nitride,	dielectric layer (“CT1” or “CT2”) includes oxygen-rich nitride and the second dielectric layer (“CT2” or “CT1”) includes oxygen-lean nitride ⁶⁵:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

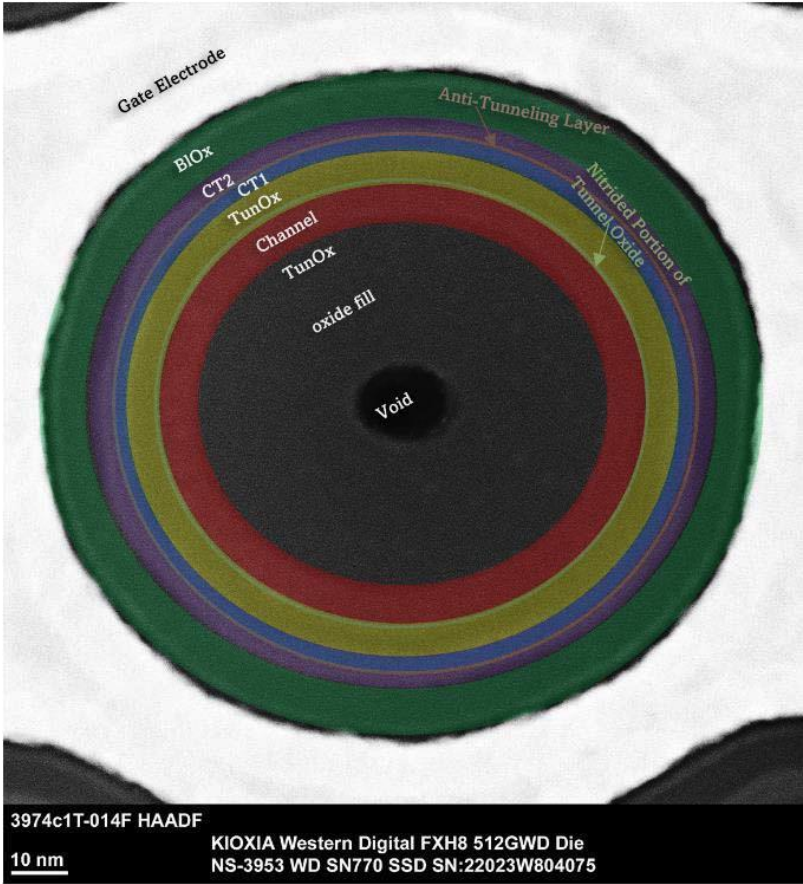
⁶⁵ TechInsights 112L Report

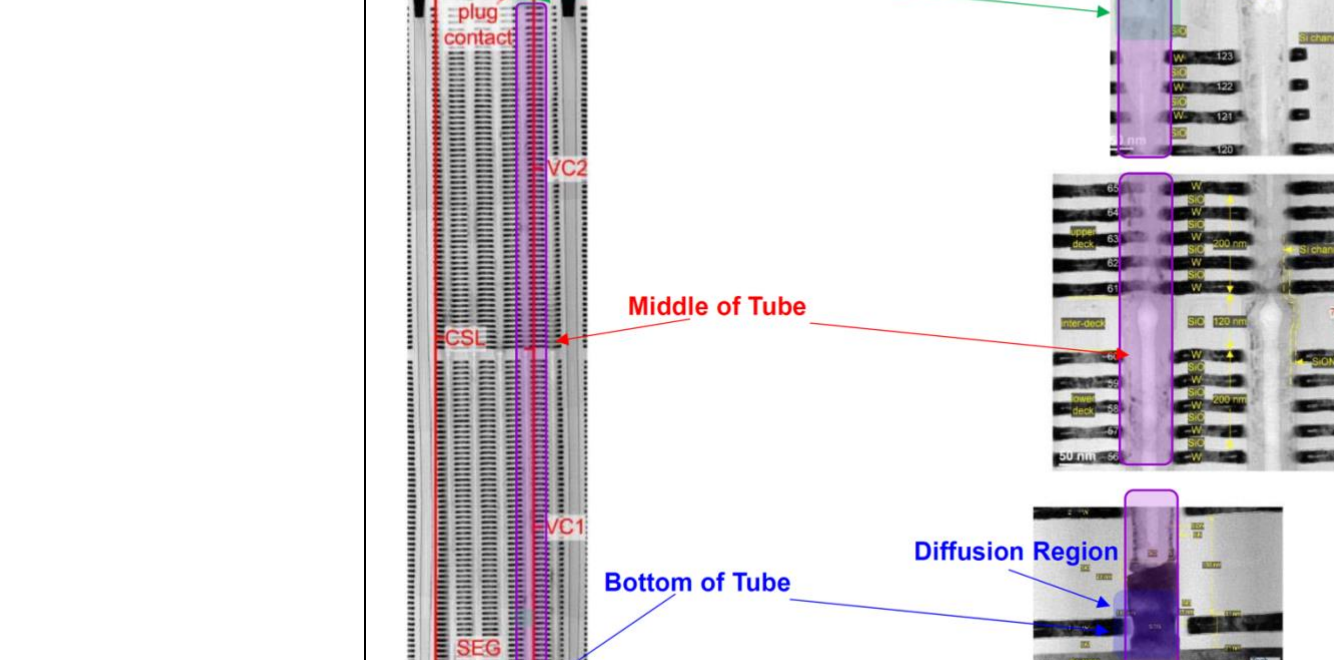
Claim Element	'240 Accused Instrumentalities
[16g] a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer, and	The '240 Accused Instrumentalities comprise a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer. For example, the tunnel dielectric layer ("TunOx") is disposed abutting the multi-layer charge trapping layer ("CT1," "Anti-Tunneling Layer," "CT2")⁶⁶:  3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075

⁶⁶ TechInsights 112L Report

<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i>
	As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[16h] a channel disposed abutting the tunnel dielectric layer,	The '240 Accused Instrumentalities comprise a channel disposed abutting the tunnel dielectric layer. For example, the channel ("Channel") is disposed abutting the tunnel dielectric layer (yellow "TunOx") ⁶⁷ :

⁶⁷ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075 As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
[16i] wherein the channel is positioned between and electrically	In the '240 Accused Instrumentalities the channel is positioned between and electrically connecting a first diffusion region and a second diffusion region. For example, the '240

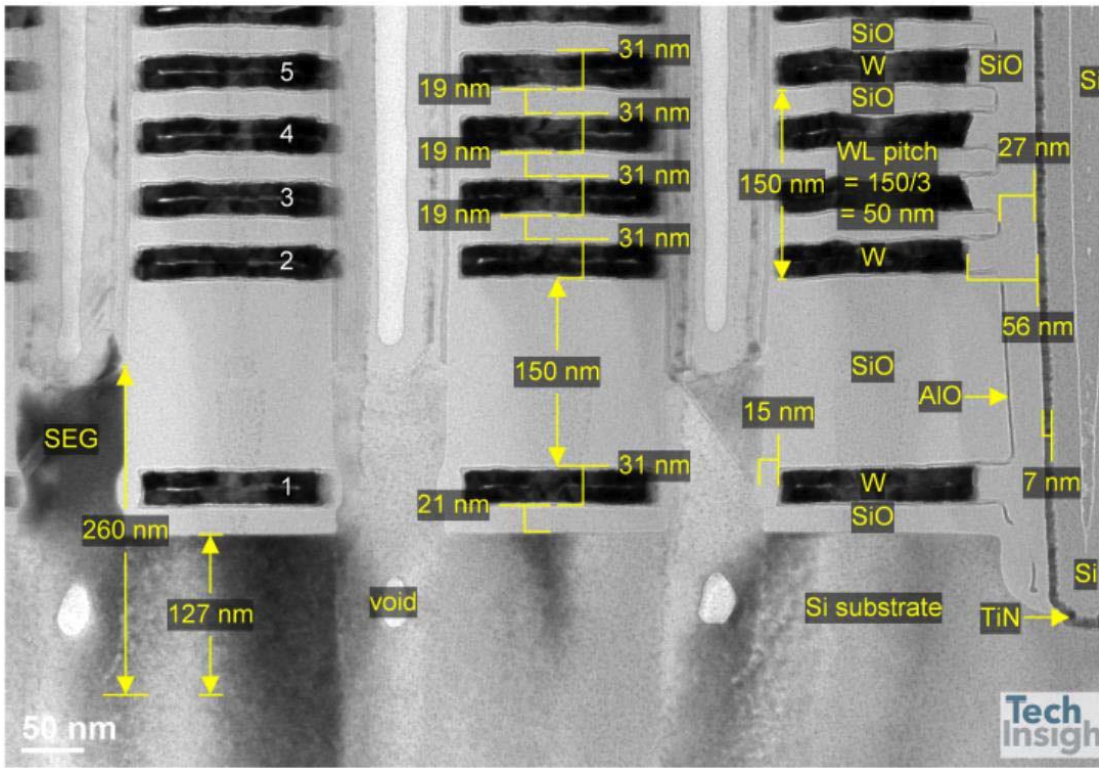
<i>Claim Element</i>	<i>'240 Accused Instrumentalities</i> connecting a first diffusion region and a second diffusion region, Accused Instrumentalities contain vertical tube structures between a bottom first diffusion region and a top second diffusion region⁶⁸: 
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⁶⁸ TechInsights 112L Report

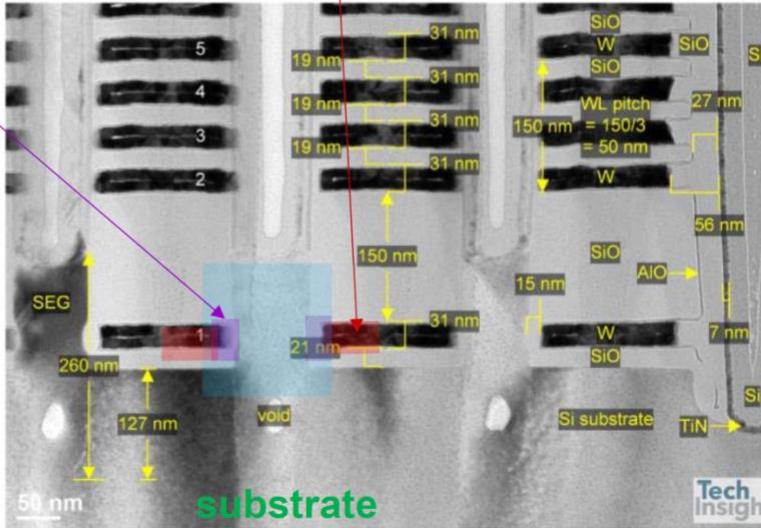
Claim Element	'240 Accused Instrumentalities
	The vertical tubes contain a silicon channel that electrically connects the first and second diffusion regions⁶⁹: 
[16j] wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and	In the '240 Accused Instrumentalities the channel is vertical and oriented substantially perpendicular to a semiconductor material structure. For example, the vertical channel is substantially perpendicular to the silicon substrate⁷⁰:

⁶⁹ *Id.*

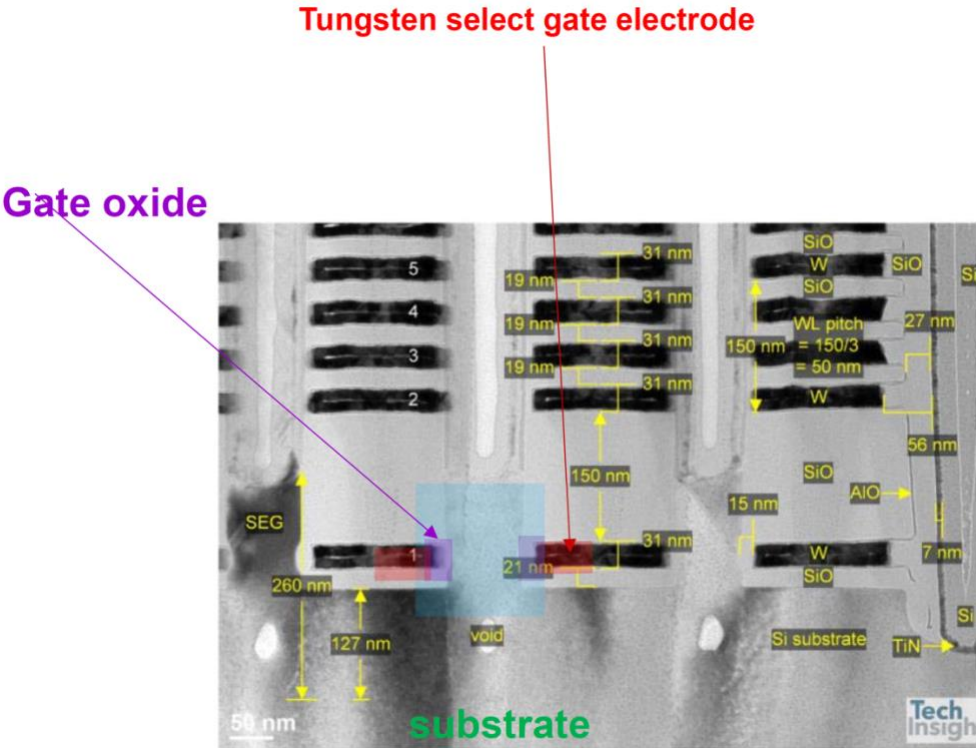
⁷⁰ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	 The image is a cross-sectional scanning electron micrograph (SEM) of a MOS logic device. It shows several layers and structures with dimensions labeled in nanometers (nm). On the left, a series of horizontal lines are numbered 1 through 5. A 'SEG' (Tungsten select gate electrode) is labeled with a dimension of 260 nm. Below it, a dimension of 127 nm is shown. A 'void' is indicated in the center. On the right, various layers are labeled: SiO, W, SiO, WL pitch (calculated as 150 nm / 3 = 50 nm), W, SiO, AIO, W, SiO, and Si substrate. Dimensions include 31 nm, 19 nm, 150 nm, 21 nm, 15 nm, 27 nm, 56 nm, and 7 nm. A 'TiN' layer is also labeled. A 50 nm scale bar is at the bottom left. The 'Tech Insights' logo is at the bottom right.
[16k] a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.	The '240 Accused Instrumentalities comprise a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon. For example, there are MOS logic transistors on the silicon substrate, which comprise a gate oxide layer (“Gate oxide”) and a high work function gate electrode (“Tungsten select gate electrode”) disposed thereon⁷¹:

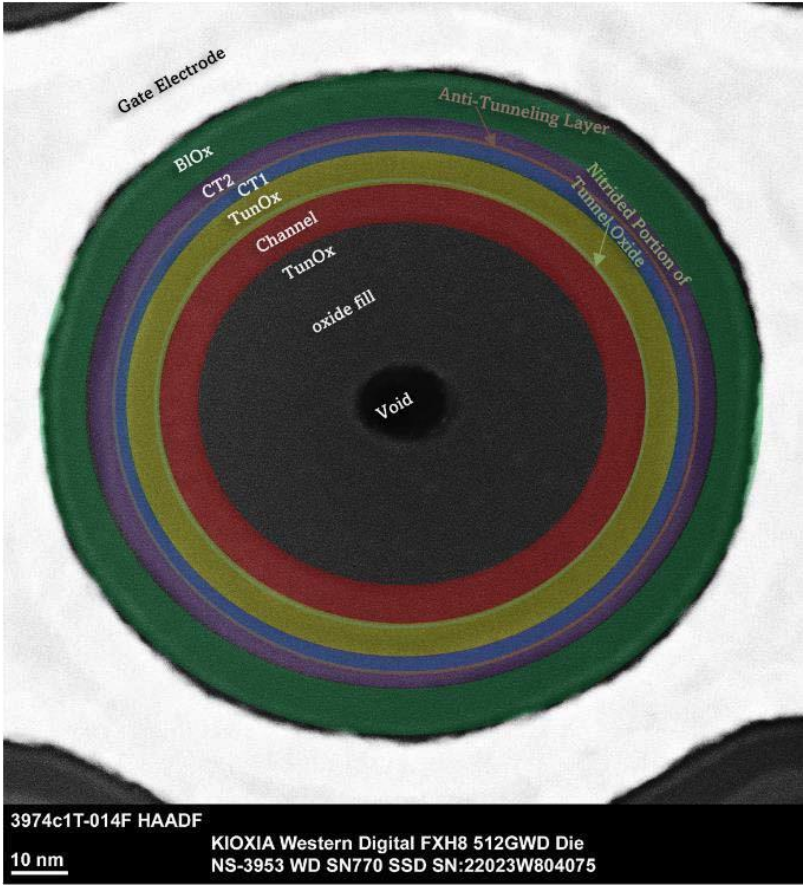
⁷¹ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
	Tungsten select gate electrode Gate oxide  As shown above, this limitation is literally present, but to the extent that the Counterclaim Defendants contend otherwise, it is in the alternative present under the doctrine of equivalents.
17. The semiconductor device of claim 16, wherein the MOS logic	In the '240 Accused Instrumentalities the MOS logic device is formed at least partially on the semiconductor material structure. For example, the MOS logic device is formed at least partially on the silicon substrate ⁷² :

⁷² TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
device is formed at least partially on the semiconductor material structure.	
18. The semiconductor device of claim 16, wherein the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first and second dielectric layers, and wherein the anti-	In the '240 Accused Instrumentalities the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first and second dielectric layers and the anti-tunneling layer includes an oxide layer. For example, the multi-layer charge trapping layer further comprises an anti-tunneling layer (“Anti-Tunneling Layer”) disposed between the first (“CT1” or “CT2”) and second (“CT2” or “CT1”) dielectric layers and the anti-tunneling layer (“Anti-Tunneling Layer”) includes an oxide layer⁷³:

⁷³ TechInsights 112L Report

Claim Element	'240 Accused Instrumentalities
tunneling layer includes an oxide layer.	 3974c1T-014F HAADF 10 nm KIOXIA Western Digital FXH8 512GWD Die NS-3953 WD SN770 SSD SN:22023W804075