

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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Sandisk Technologies, Inc.,  
Petitioner,

v.

Longitude Flash Memory Solutions Ltd.,  
Patent Owner.

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Case No. IPR2025-01283

U.S. Patent No. 9,929,240

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**PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NO. 9,929,240**

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## **EXHIBIT LIST**

| <b>Exhibit No.</b> | <b>Description</b>                                                                                                                                                                  |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>1001</b>        | U.S. Patent No. 9,929,240 to Polishchuk et al. (“the ’240 patent”)                                                                                                                  |
| <b>1002</b>        | Prosecution file history for the ’240 patent, U.S. Patent Application No. 15/335,180 (“Pros. Hist.”)                                                                                |
| <b>1003</b>        | Declaration Jack C. Lee                                                                                                                                                             |
| <b>1004</b>        | U.S. Patent Application Publication No. 2012/0068255 to Changhyun Lee, et al. (“Lee ’255”)                                                                                          |
| <b>1005</b>        | Korean Patent Publication No. 2011-0118961 to Gi Hong Lee et al. and Certified English Translation of Korean Patent Publication No. 2011-0118961 to Gi Hong Lee et al. (“Lee ’961”) |
| <b>1006</b>        | U.S. Patent Application Publication No. 2006/0065919A1 to Ichiro Fujiwara (“Fujiwara”)                                                                                              |
| <b>1007</b>        | L. Lukasiak and A. Jakubowski, History of Semiconductors, Journal of Telecommunications and Information Technology, Vol. 3 (2010) (“Lukasiak”)                                      |
| <b>1008</b>        | U.S. Patent No. 4,203,158 to Dov Frohman-Bentchkowsky, et al. (“Frohman-Bentchkowsky”)                                                                                              |
| <b>1009</b>        | U.S. Patent Application Publication No. 2006/0255399 to Ju-Hyung Kim, et al. (“Kim ’399”)                                                                                           |
| <b>1010</b>        | U.S. Patent Application Publication No. 2003/0122204 to Kazumasa Nomoto, et al. (“Nomoto”)                                                                                          |
| <b>1011</b>        | U.S. Patent Application Publication No. 2009/0179253 to Levy, et al. (“Levy”)                                                                                                       |
| <b>1012</b>        | U.S. Patent Application Publication No. 2011/0045647 to Jin-Hwa Heo, et al. (“Heo”)                                                                                                 |
| <b>1013</b>        | U.S. Patent Application Publication No. 2011/0281429 to Udayan Ganguly, et al. (“Ganguly”)                                                                                          |
| <b>1014</b>        | US 2006/0113586 to Wang (“Wang ’586”)                                                                                                                                               |

| <b>Exhibit No.</b> | <b>Description</b>                                                                                                                                                                                                                                           |
|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>1015</b>        | U.S. Patent No. 6,897,533 to Jean Yee-Mei Yang, et al. (“Yang ’533”)                                                                                                                                                                                         |
| <b>1016</b>        | U.S. Patent Application Publication No. 2006/0198189 to Hang-Ting Lue, et al. (“Lue ’189”)                                                                                                                                                                   |
| <b>1017</b>        | U.S. Patent Application Publication No. 2009/0059676 to Shen Chih Lai, et al. (“Lai ’676”)                                                                                                                                                                   |
| <b>1018</b>        | Erh-Kun Lai, et al., <i>A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory</i> , Proceedings of the 2006 International Electron Devices Meeting (IEEE Dec. 2006) (“Lai Article”)                                                      |
| <b>1019</b>        | U.S. Patent Application Publication No. 2005/0006696A1 to Mitsuhiro Noguchi, et al. (“Noguchi”)                                                                                                                                                              |
| <b>1020</b>        | Antonio Arreghini, et al., <i>Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells</i> , IEEE Transactions on Electron Devices, Vol. 55, No. 5 (May 2008) (“Arreghini”)                 |
| <b>1021</b>        | U.S. Patent Application Publication No. 2010/0157680A1 to Masaaki Higuchi, et al. (“Higuchi”)                                                                                                                                                                |
| <b>1022</b>        | U.S. Patent Application Publication No. 2008/0128790 to Jin-Hyo Jung (“Jung”)                                                                                                                                                                                |
| <b>1023</b>        | U.S. Patent Application Publication No. 2003/0198106 to Jeong-Hyuk Choi (“Choi”).                                                                                                                                                                            |
| <b>1024</b>        | U.S. Patent Application Publication No. 2009/0026460 to Tien-Fan Ou, et al. (“Ou”)                                                                                                                                                                           |
| <b>1025</b>        | Falong Zhou, et al., <i>VDNROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications</i> , Proceeding of 2006 European Solid-State Device Research Conference (IEEE Sept. 2006) (“VDNROM”) |
| <b>1026</b>        | H. Tanaka, et al., <i>Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory</i> , 2007 IEEE Symposium on VLSI Technology (June 2007) (“Tanaka”)                                                                       |

| <b>Exhibit No.</b> | <b>Description</b>                                                                                                                                                                                             |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>1027</b>        | Toshiba Press Release, Toshiba Develops New NAND Flash Technology (June 12, 2007) (“Toshiba PR”)                                                                                                               |
| <b>1028</b>        | U.S. Patent Application Publication No. 2010/0178759A1 to JinGyun Kim, et al. (“Kim ’759”)                                                                                                                     |
| <b>1029</b>        | Moon Kyung Kim, et al., <i>A Comparison of N+ Type and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories</i> , Material Research Society Symposium Proceedings, Vol. 997 (MRS 2007) (“Kim Article”) |
| <b>1030</b>        | U.S. Patent Application Publication No. 2006/0118858 to Sang-hun Jeon (“Jeon”)                                                                                                                                 |
| <b>1031</b>        | U.S. Patent Application Publication No. 2005/0237809 to Yen-Hao Shih, et al. (“Shih”)                                                                                                                          |
| <b>1032</b>        | U.S. Patent Application Publication No. 2012/0276696 to Jun-Kyu Yang, et al. (“Yang ’696”)                                                                                                                     |
| <b>1033</b>        | U.S. Patent Application Publication No. 2013/0270625 to Byong-hyun Jang, et al. (“Jang”)                                                                                                                       |
| <b>1034</b>        | U.S. Patent Application Publication No. 2012/0068247 to Changhyun Lee, et al. (“Lee ’247”)                                                                                                                     |
| <b>1035</b>        | U.S. Patent Application Publication No. 2012/0299086 to Jaegoo Lee (“Lee ’086”)                                                                                                                                |
| <b>1036</b>        | U.S. Patent Application Publication No. 2011/0316064 to Jung Ho Kim, et al. (“Kim ’064”)                                                                                                                       |
| <b>1037</b>        | U.S. Provisional Application No. 60/940,160 (“’160 Provisional App.”)                                                                                                                                          |
| <b>1038</b>        | Prosecution file history for the ’434 patent (U.S. Application No. 12/152,518) (“’434 Pros. Hist.”)                                                                                                            |
| <b>1039</b>        | Prosecution file history for the ’374 patent (U.S. Application No. 13/288,919) (“’374 Pros. Hist.”)                                                                                                            |
| <b>1040</b>        | Prosecution file history for the ’537 patent (U.S. Application No. 13/539,466) (“’537 Pros. Hist.”)                                                                                                            |
| <b>1041</b>        | U.S. Patent No. 6,912,163 to Wei Zheng, et al. (“Zheng”)                                                                                                                                                       |
| <b>1042</b>        | S.M. Sze and K. Ng, <i>Physics of Semiconductor Devices</i> (3 <sup>rd</sup> Ed.                                                                                                                               |

| <b>Exhibit No.</b> | <b>Description</b>                                                                                                                              |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
|                    | Wiley-Interscience 2007) (“Sze”)                                                                                                                |
| <b>1043</b>        | U.S. Patent Application Publication No. 2010/0019312 to Katsuyuki Sekine, et al. (“Sekine”)                                                     |
| <b>1045</b>        | Declaration of June Munford                                                                                                                     |
| <b>1046</b>        | IEEE Declaration of Gordon MacPherson                                                                                                           |
| <b>1047</b>        | Intentionally Omitted                                                                                                                           |
| <b>1048</b>        | U.S. Patent Application Publication No. 2012/0061744 to Sung-Min Hwang et al (“Hwang”)                                                          |
| <b>1049</b>        | Excerpts from The American Heritage Dictionary of the English Language (5 <sup>th</sup> Ed. 2011) (American Heritage Excerpts)                  |
| <b>1050</b>        | US 2008/0272424 to Kim et al. (“Kim ’424”)                                                                                                      |
| <b>1051</b>        | US 2007/0029625 to Lue et al. (“Lue ’625”)                                                                                                      |
| <b>1052</b>        | US 2006/0008959 to Hagemeyer et al., (“Hagermeyer”)                                                                                             |
| <b>1053</b>        | Prosecution file history for the ’336 patent (U.S. Application No. 15/864,832) (“’336 Pros. Hist.”)                                             |
| <b>1054</b>        | Infringement Contentions from <i>SanDisk Corp. v. IPValue Management, Inc., et al.</i> , No. 25-cv-02389 (N.D. Cal.) (Infringement Contentions) |
| <b>1055</b>        | Excerpts from Merriam-Webster's Collegiate Dictionary (11th Ed. 2003) (Merriam-Webster Excerpts)                                                |
| <b>1056</b>        | Excerpts from New Oxford American Dictionary (3rd Ed. 2010) (New Oxford Excerpts)                                                               |
| <b>1057</b>        | US 5,998,826 to Hung et al. (“Hung”)                                                                                                            |
| <b>1058</b>        | US 2009/0268522 to Maejima (“Maejima”)                                                                                                          |
| <b>1059</b>        | EP 0 810 667 A2 by Hyundai (“Hyundai”)                                                                                                          |
| <b>1060</b>        | US 2003/0135690 to Lee et al. (“Lee ’690”)                                                                                                      |

Petitioner respectfully requests that the Board institute *inter partes* review and cancel claims 1, 3-7, 9, and 11-18 (the “Challenged Claims”) of U.S. Patent No. 9,929,240 (the ’240 patent).

## **I. TECHNICAL BACKGROUND**

The ’240 patent is directed generally to non-volatile memory (or “NVM”), which is a type of computer memory that can retain stored information even after power is removed. Ex. 1001 (’240 patent), 1:33-37; Ex. 1003, ¶¶48-49. More specifically, the ’240 patent purports to improve the data retention capabilities of silicon–oxide–nitride–oxide–silicon (“SONOS”) flash memory devices. Ex. 1001 (’240 patent), 1:65-2:7, 2:38-50; Ex. 1003, ¶¶18-19, 56. As discussed below, SONOS-type flash memory devices were well-known at the time of the application for the ’240 patent.

### **A. Floating Gate Flash Memory**

Flash memory is a type of semiconductor NVM that was invented in the 1980s. Ex. 1003, ¶50. Early flash memory devices were based on a “floating gate” metal–oxide–semiconductor field-effect transistor (MOSFET) design. *Id.*, ¶51. The design included an electrically insulated gate that “floats” between two oxide layers, as shown here:

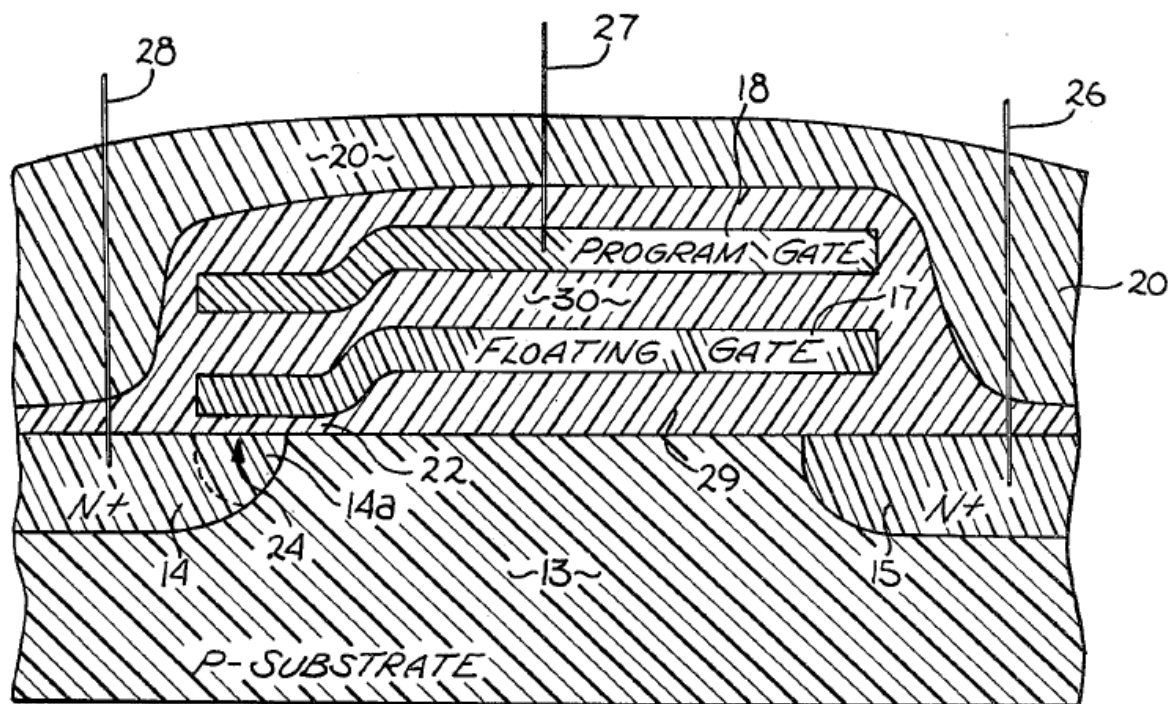


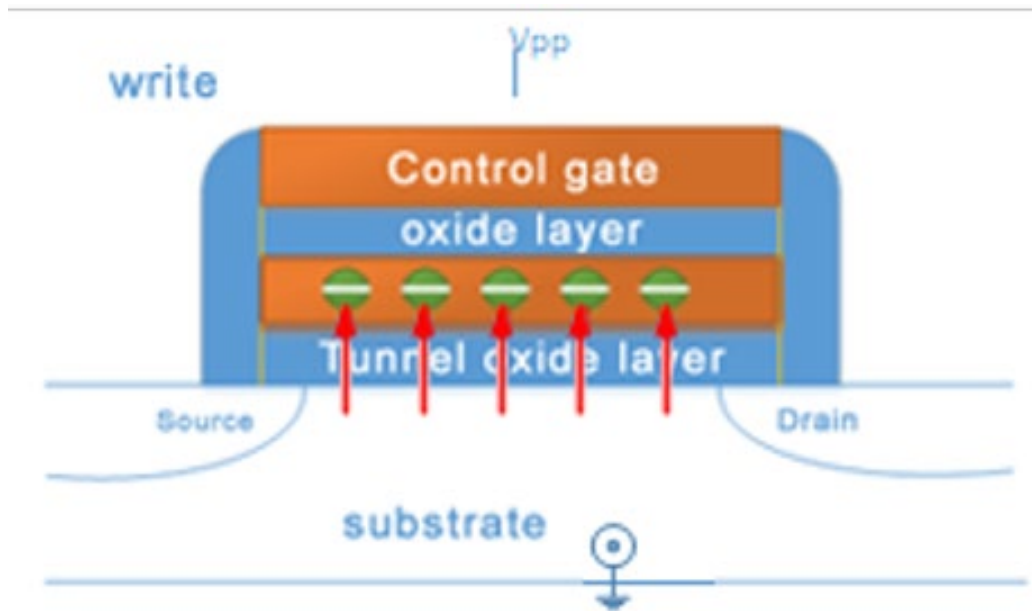
*Fig. 1*

Ex. 1008 (Frohman-Bentchkowsky), Fig. 1; *see also id.*, 4:1-31; Ex. 1003, ¶51.

Because the floating gate is electrically isolated, any electron placed in the gate will be trapped there after voltage is removed. *See, e.g.*, Ex. 1008 (Frohman-Bentchkowsky), 1:18-23, 3:55-57, 5:5-7; Ex. 1003, ¶52. This allows a floating gate transistor to function as NVM. In the simplest example, the presence of sufficient electrons in the floating gate will cause the memory to be read as a “1,” while the absence of electrons in the floating gate will cause the memory to be read as a “0.”

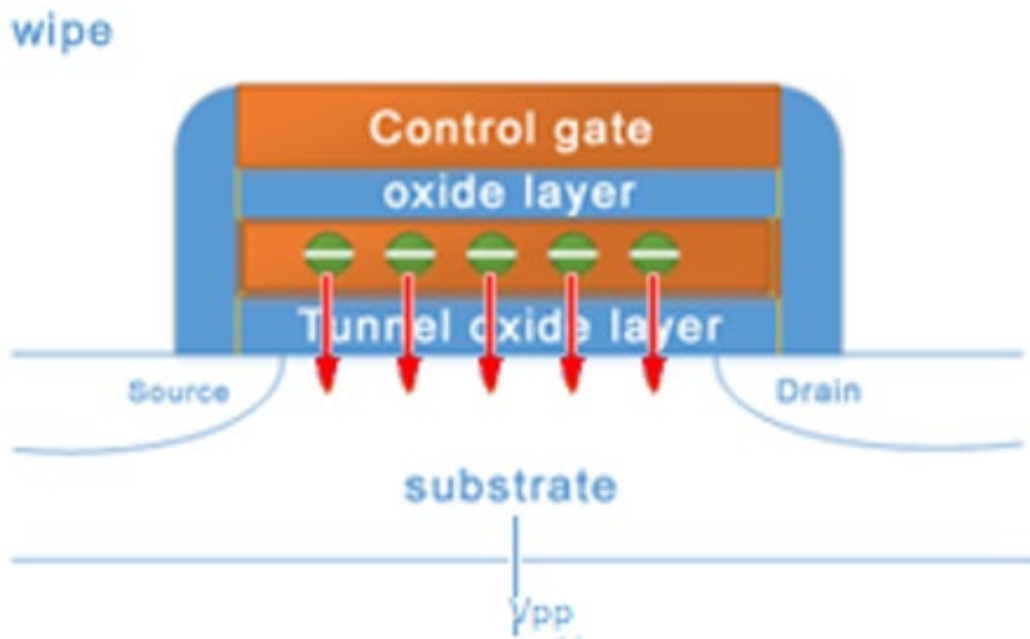
Ex. 1013 (Ganguly), 1:20-23.

During a program/write operation, electrons can be placed in the floating gate using a “tunneling” procedure, where an electric field is applied that causes electrons from the substrate to “tunnel” through an oxide layer to the floating gate:



Ex. 1003, ¶53.

During an erase/wipe operation, the opposite electric field is applied, causing the electrons trapped in the control gate to “tunnel” back to the substrate:

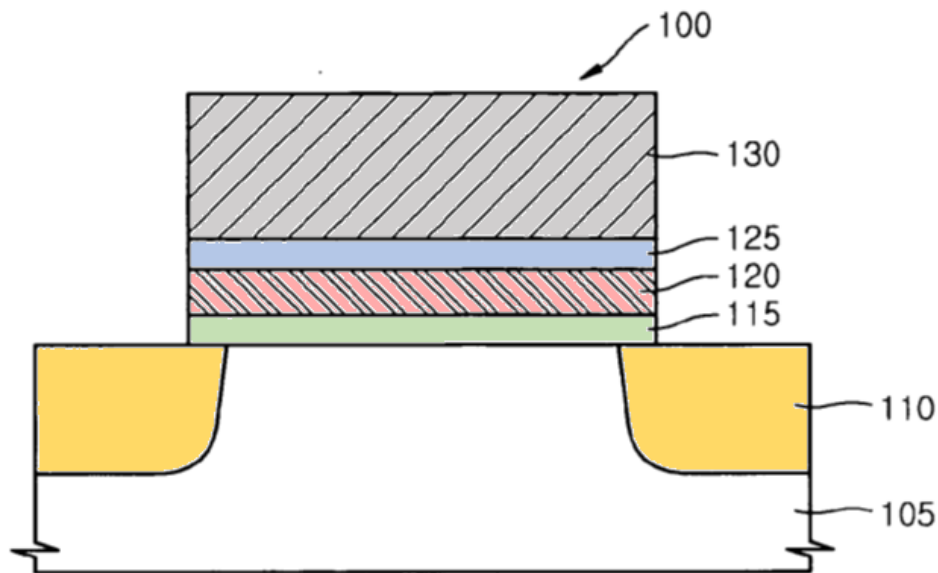


Ex. 1003, ¶54.

#### **B. SONOS-Type Flash Memory**

By the early 2000s, flash memory devices were commonly designed to use charge-trapping SONOS technology. *See, e.g.,* Ex. 1010 (Nomoto), Fig. 3H, [0032]-[0038]; Ex. 1003, ¶55. As noted above, “SONOS” is a reference to the layers of the NVM device: silicon-oxide-nitride-oxide-silicon. SONOS-type flash memory is similar to floating gate memory except that a non-conductive silicon nitride layer is used to trap charges rather than the floating gate. Ex. 1003, ¶56. An example of a “conventional” SONOS memory device is provided in Kim ’399 (Ex. 1009), which was filed on February 15, 2006:

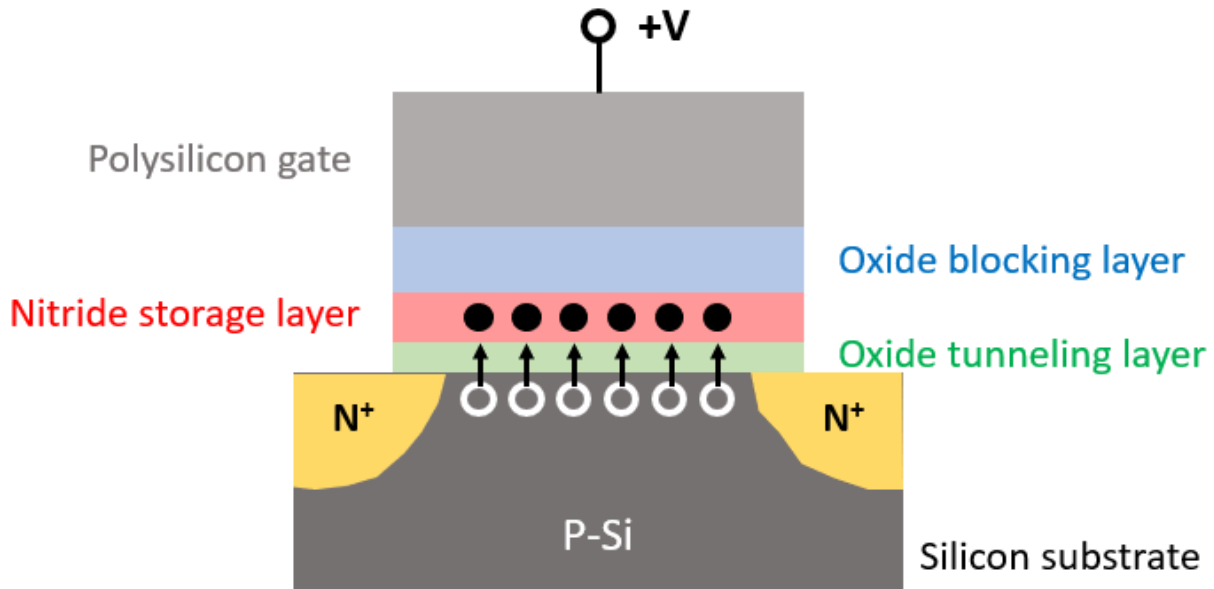
**FIG. 1 (CONVENTIONAL ART)**



Ex. 1009 (Kim '399), Fig. 1, [0006]-[0008]; Ex. 1003, ¶56.

As reflected above, a conventional SONOS memory device in 2006 included: (i) a silicon semiconductor substrate 105 with source/drain regions 110; (ii) an oxide tunnel insulating film 115 (green); (iii) a nitride charge trapping film 120 (red); (iv) a silicon oxide blocking insulating film 125 (blue); and (v) silicon control gate 130 (gray). Ex. 1003, ¶¶56-57.

Like floating gate memory, SONOS charge trap memory transistors work by “tunneling” electrons into and out of the nitride charge trapping layer. Ex. 1003, ¶58. During a programming step, a positive voltage is applied to the gate, which causes electrons from the substrate to tunnel through the tunnel oxide and into the nitride storage layer:



Ex. 1003, ¶58.

When the voltage is removed, the electrons remain in the nitride storage layer. Ex. 1003, ¶58. To perform an erase/clear step, a negative voltage is applied to the gate, which causes electrons to tunnel from the nitride storage layer back through the tunnel oxide into the silicon substrate. *Id.*, ¶59.

### C. Well-Known Configurations of SONOS-Type Flash Memory

Prior to July 2012, a person of ordinary skill in the art (a “POSITA”) would have been familiar with several routine configurations of SONOS-type flash memory devices and the predictable benefits of those configurations. *See* Ex. 1003, Part III.C.4-7. For example, a POSITA would have been familiar with:

- Configuring SONOS devices to include multiple charge storage layers, such as SONNOS configurations. Ex. 1003, ¶¶60-66 (discussing Ex.

- 1011 (Levy), Ex. 1010 (Nomoto), Ex. 1012 (Heo), Ex. 1009 (Kim '399), Ex. 1013 (Ganguly), and Ex. 1014 (Wang)).
- Configuring SONOS devices to include an intermediate oxide layer between two nitride layers, such as SONONOS configurations. Ex. 1003, ¶¶67-72 (discussing Ex. 1015 (Lue '189), Ex. 1015 (Yang '533), Ex. 1017 (Lai '676), Ex. 1018 (Lai Article), Ex. 1019 (Noguchi), and Ex. 1020 (Arreghini)).
  - Using high work function materials for the gate electrodes of SONOS/SONNOS/SONONOS devices. Ex. 1003, ¶¶89-91 (discussing Ex. 1029 (Kim Article), Ex. 1015 (Lue '189), Ex. 1017 (Lai '676), Ex. 1012 (Heo), Ex. 1030 (Jeon), and Ex. 1031 (Ou)).
  - Arranging SONOS/SONNOS/SONONOS devices to have vertical configurations. Ex. 1003, ¶¶73-88 (discussing Ex. 1021 (Higuchi), Ex. 1028 (Kim '759), Ex. 1023 (Choi), Ex. 1031 (Ou), Ex. 1022 (Jung), Ex. 1025 (VDNROM), Ex. 1043 (Sekine), Ex. 1026 (Tanaka), and Ex. 1027 (Zhou)).

## **II. THE '240 PATENT**

### **A. Overview of Alleged Invention**

The '240 patent issued on March 27, 2018 from an application filed on October 26, 2016. *See* Ex. 1001 ('240 patent), 000001. The '240 patent purports to improve the data retention capabilities of SONOS memory devices using an “oxide-nitride-nitride-oxide (ONNO) stack” with a “multi-layer charge-trapping region.” Ex. 1001 ('240 patent), 1:65-2:7, 2:38-50; Ex. 1003, ¶¶18-19, 55. Figure

4A, annotated below, depicts one embodiment of the ONNO stack of the '240 patent:

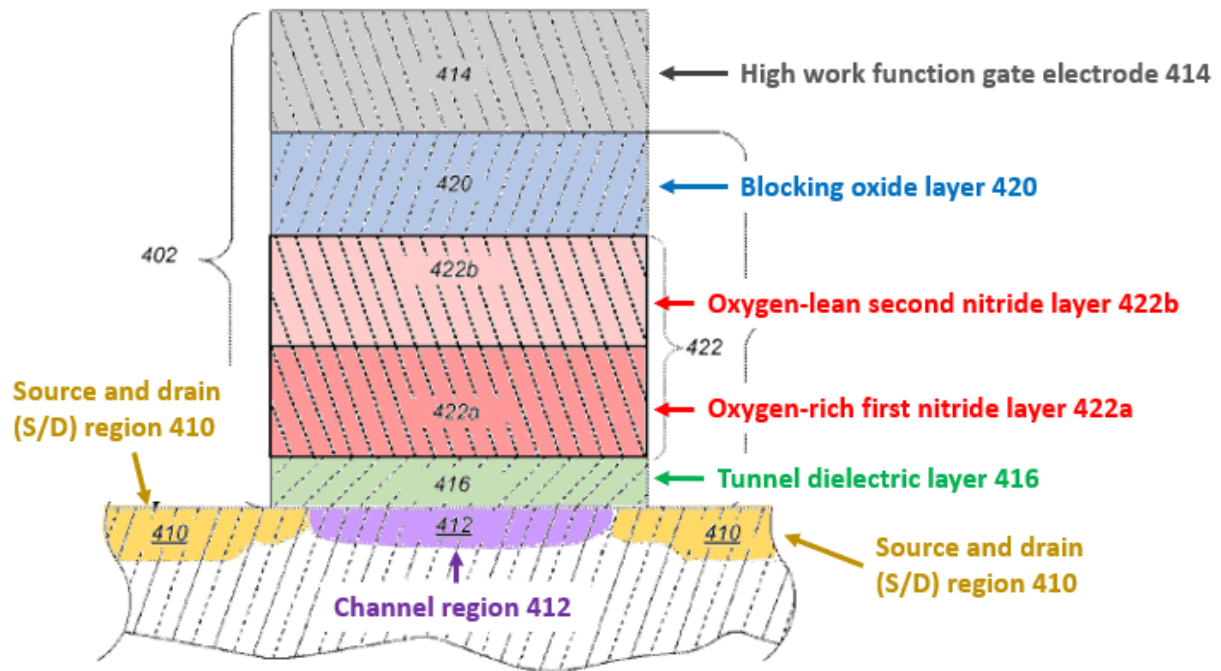


FIG. 4A

Ex. 1001 ('240 patent), Fig. 4A; *see also* Ex. 1003 ¶¶20-21.

As reflected above, figure 4A includes “one or more diffusion regions 410” (gold) that are “separated by a channel region 412” (purple). Ex. 1001 ('240 patent), 8:55-58; Ex. 1003, ¶22. In this figure, the ONNO stack is aligned above the horizontal channel region. *Id.* The stack includes “tunnel dielectric layer 416” (green), “multi-layer charge trapping region 422” (red), “blocking dielectric layer 420” (blue), and “high work function gate electrode 414” (gray). Ex. 1001 ('240 patent), 8:52-10:15; Ex. 1003, ¶22.

The '240 patent further states that the ONNO stack may be modified to have an intermediate oxide layer between the two nitride layers, forming an ONONO structure. Ex. 1001 ('240 patent), Fig. 4B, 10:5-12; Ex. 1003, ¶24. An example of this configuration, with the intermediate oxide layer annotated in orange, is shown in figure 4B:

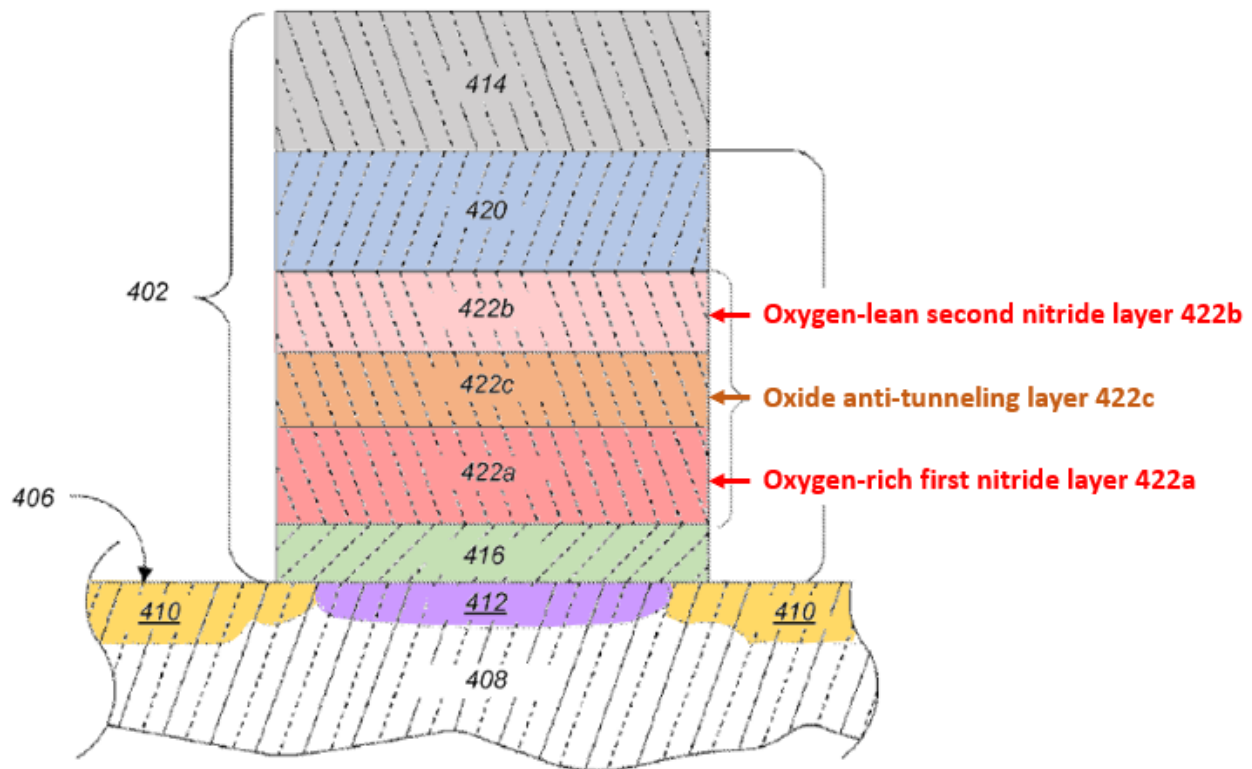
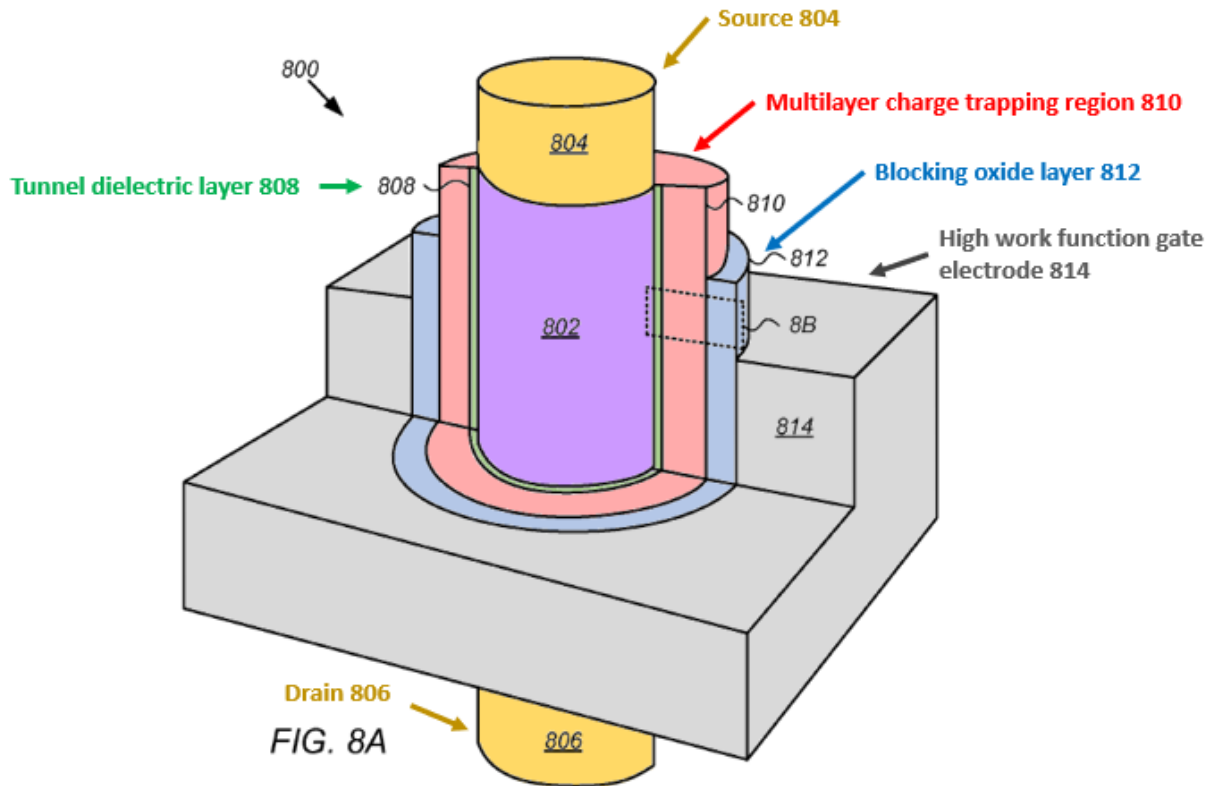


**FIG. 4B**

Ex. 1001 ('240 patent), Fig. 4B; Ex. 1003, ¶24.

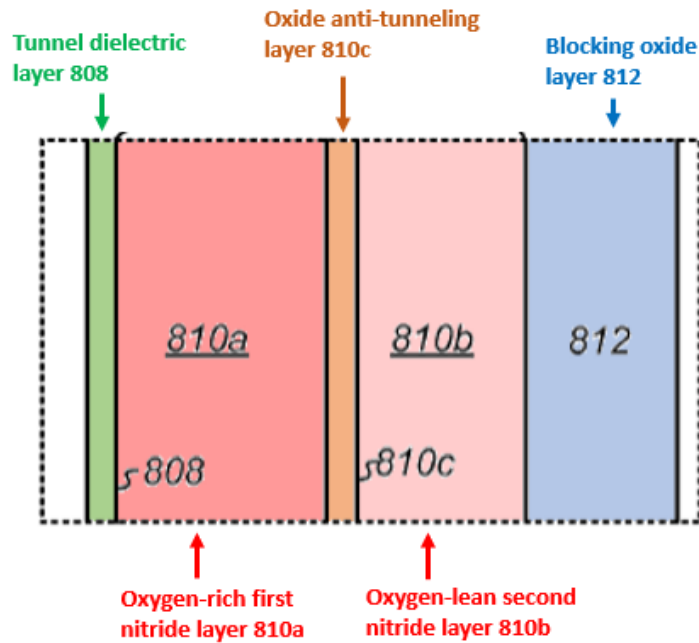
While figures 4A and 4B depict horizontally-oriented memory transistors, the '240 patent states that there are alternative implementations of the ONNO (or ONONO) stack. Ex. 1001 ('240 patent), 8:47-20:3; Ex. 1003, ¶¶26-29. For example, figures 8A and 8B are directed to a vertically-oriented (“three-

dimensional” or “3D”) memory transistor structure with an ONONO stack. Ex. 1001 (’240 patent), Figs. 8-10, 17:11-20:3; Ex. 1003, ¶¶30-31. Figure 8A shows a transistor with a channel region (purple) that extends vertically between diffusion regions (gold):



Ex. 1001 (’240 patent), Fig. 8A, 17:10-18:8; Ex. 1003, ¶30.

Figure 8B depicts a magnified view of the cross section of the ONONO stack from figure 8A:



Ex. 1001 ('240 patent), Fig. 8B, 17:49-56; ¶¶32-33.

Figures 9 and 10 depict methods of fabricating vertical channel memory devices, including a “gate first” method (Fig. 9) and “gate last” method (Fig. 10).

Ex. 1001 ('240 patent), 3:30-33, 18:14-19:14; Ex. 1003, ¶¶34-35.

## B. Prosecution History

Igor Polishchuk, Sagy Charel Levy, and Krishnaswamy Ramkumar (collectively, “the Applicants”) filed the application for the '240 patent on October 26, 2016, which included application claims 1-20. Ex. 1002 (Pros. Hist.), 00004247. Subsequently, the Applicants submitted information disclosure statements listing more than 500 prior art references (*id.*, 000148-182, 000620-631, 001079-1086, 001479-1483, 001707-1710, 001741-1744, 001762-1765, 001840-1843, 001874-1877) and amended the application to replace original claims 1-20

with new claims 21-40 (*id.*, p.104-110). After the preliminary amendment, Applicants advanced three independent claims: 21, 33, and 38 (corresponding to issued claims 1, 12, and 16). Ex. 1002 (Pros. Hist.), 000105-109, 001827; Ex. 1003, ¶¶36-38.

The Examiner rejected independent application claims 21, 33, and 38, finding it would have been obvious to a POSITA to combine NVM references teaching multi-layer charge trapping regions, high work function gate electrodes, and integrated MOS logic transistors. Ex. 1002 (Pros. Hist.), 001616-1628; Ex. 1003, ¶40. While rejecting the independent claims, the Examiner allowed the dependent claims reciting vertical channels (25, 34, 36, and 39). *Id.*, 001629. Ex. 1003, ¶¶38-39. Although SONOS devices with vertical channels were well-known in the prior art (*see* Ex. 1003, ¶¶73-88), the Examiner did not apply any of those references during examination.

Rather than disputing the Examiner's obviousness determinations with respect to the independent claims, Applicants filed amendments to those claims. Ex. 1002 (Pros. Hist.) (Pros. Hist.), 001722-1738. Applicants amended claims 33 and 38 (issued claims 12 and 16) to add vertical channel limitations. *id.*, 001726-1728, 001735-1736. Applicants amended claim 21 (issued claim 1) to require that the multi-layer charge trapping region include an intermediate "anti-tunneling layer." *Id.*, 001724, 001731-1735; Ex. 1003, ¶¶41-42.

On October 4, 2017, the Examiner issued a Notice of Allowability for application claims 21-40. Ex. 1002 (Pros. Hist.), 001793-1801; Ex. 1003, ¶43. In providing the reasons for allowance, the Examiner stated the following elements were absent from the prior art:

- For application claim 21 (issued claim 1), the prior art “discloses all limitations of claim 21 except for . . . ‘an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer.” Ex. 1002 (Pros. Hist.), 001799; Ex. 1003, ¶44.
- For application claim 33 (issued claim 12), the Examiner stated that the prior art discloses everything except for “the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer disposed between the gate structure and the channel.” Ex. 1002 (Pros. Hist.), 001799-1800; Ex. 1003, ¶45.
- For application claim 38 (issued claim 16), the Examiner stated that the prior art discloses everything except for “the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.” Ex. 1002 (Pros. Hist.), 001800; Ex. 1003, ¶46.

### C. Priority Date

The earliest possible priority date for the Challenged Claims of the '240 patent is **July 1, 2012**, the date of the filing of U.S. Patent Application No. 13/539,466, which issued as U.S. Patent No. 8,633,573. Ex. 1003, ¶47.

On its face, the '240 patent purports to claim priority to a provisional patent application filed on May 25, 2007 through a chain of related applications represented in the following chart:

|   | App No.    | Filing Date | Patent No. |                                              |
|---|------------|-------------|------------|----------------------------------------------|
| A | 60/940,160 | 5/25/2007   | n/a        | “the '160 provisional”                       |
| B | 12/152,518 | 5/13/2008   | 8,063,434  | “the '434 patent”                            |
| C | 13/288,919 | 11/3/2011   | 8,859,374  | “the '374 patent,” divisional of B           |
| D | 13/539,466 | 7/1/2012    | 8,633,537  | “the '537 patent,” continuation-in-Part of C |
| E | 14/159,315 | 1/20/2014   | 9,093,318  | “the '318 patent,” continuation of D         |
| F | 14/811,346 | 7/28/2015   | 9,502,543  | “the '543 patent,” continuation of E         |
| G | 15/335,180 | 10/26/2016  | 9,929,240  | “the '240 patent,” continuation of F         |

Ex. 1001 ('240 patent), 1:8-22; Ex. 1003, ¶¶97-98.

To obtain the benefit of the filing date of the earlier related applications, the Challenged Claims must have written description support those applications. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010); *Augustine Med., Inc. v. Gaymar Indus., Inc.*, 181 F.3d 1291, 1302-03 (Fed. Cir. 1999) (“A

CIP application contains subject matter from a prior application and may also contain additional matter not disclosed in the prior application . . . Different claims of such an application may therefore receive different effective filing dates.”). The written description support must have “sufficient detail that one skilled in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought.” *Anascape, Ltd. v. Nintendo of Am., Inc.*, 601 F.3d 1333, 1335 (Fed. Cir. 2010). The question is whether the subject matter is disclosed in the specification, not whether the subject matter would have been obvious. *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1571-1572 (Fed. Cir. 1997).

Here, the Challenged Claims each include limitations that lack written support in the applications filed prior to July 1, 2012—the ’160 Provisional Application (filed May 25, 2007), the ’518 Application (filed May 13, 2008), and the ’919 Application (filed November 3, 2011) (collectively, the “Earlier Applications”). Ex. 1003, ¶99.

Independent claim 1 requires a memory device that includes “an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer.” Ex. 1001 (’240 patent), claim 1; Ex. 1003, ¶100. The Earlier Applications do not provide written description support for this limitation. To the contrary, the Earlier Applications disclose first and second dielectric layers that are adjacent to each other without any intermediate layer

between. *See, e.g.*, Ex. 1037 ('160 Provisional App.), 9-10 (Fig. 1); Ex. 1038 ('434 Pros. Hist.), 000137-139 (Fig. 2A-3) ; Ex. 1039 ('374 Pros. Hist), 000197-199 (Figs. 2A-3); Ex. 1003, ¶¶101-102. Applicants first added figures and written description of an intermediate anti-tunneling layers in the continuation-in-part application for the '537 patent, which was filed on July 1, 2012. *See* Ex. 1040 ('537 Pros. Hist.), pp. 218-278; *compare id. with* Ex. 1038 ('434 Pros. Hist.), pp. pp. 111-139 *and* Ex. 1039 ('374 Pros. Hist.), pp. 158-199.

Independent claims 12 and 16 require memory devices with channels, “wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure.” Ex. 1001 ('240 patent), claims 12, 16. The Earlier Applications are also silent as to this claim limitation. *See* Ex. 1037; Ex. 1038; Ex. 1039 ('374 Pros. Hist.); Ex. 1003, ¶¶103-105. The Earlier Applications exclusively disclose horizontally-oriented semiconductor devices. *See, e.g.*, Ex. 1038 ('434 Pros. Hist.), 000139; Ex. 1003, ¶104. The Applicants first added subject matter concerning vertically-oriented memory devices—e.g., figures 8-10 of the '240 patent—on July 1, 2012 in connection with a continuation-in-part application that later issued as the '537 patent. *See* Ex. 1040 ('537 Pros. Hist.), 000218-278; *compare id. with* Ex. 1038 ('434 Pros. Hist.), 000111-139; Ex. 1039 ('374 Pros. Hist.), 000158-199; Ex. 1003, ¶105.

Because features of the independent claims of the '240 patent (claims 1, 12, and 16) are not disclosed in any of the Earlier Applications, the earliest possible priority date for the '240 patent is July 1, 2012. Ex. 1003, ¶106.

### **III. FIELD AND LEVEL OF ORDINARY SKILL**

The '240 patent is in the field of non-volatile semiconductor memory. *See, e.g.,* Ex. 1001 ('240 patent), 1:26-29; Ex. 1003, ¶107. Each of the Challenged Claims is directed to either a “semiconductor device, comprising a memory device” (*see id.*, claims 12, 16) or a “memory device” (*see id.*, claim 1).

A POSITA in the relevant field as of July 1, 2012 would have had at least (1) a master's degree in electrical engineering, materials science, physics, or a related degree, and at least 3-5 years of experience in semiconductor devices and fabrication technologies; or (2) a bachelor's degree in electrical engineering, materials science, physics, or a related degree, and at least 5-6 years of experience in semiconductor devices and fabrication technologies. Ex. 1003, ¶¶105-106.

In view of the types of problems encountered in the art and prior art solutions to those problems, a POSITA in the relevant timeframe above would have been familiar with:

- Floating gate flash memory technology (*see* Ex. 1003, ¶¶50-54, 107);
- The structure and composition of SONOS-type memory devices (*see id.*, ¶¶55-59, 107);

- SONNOS and SONONOS configurations of SONOS-type memory devices (*see id.*, ¶¶73-88, 107);
- Vertically-oriented configurations of SONOS-type memory transistors, including 3D NAND structures (*see id.*, ¶¶73-88, 107); and
- The use of high work function materials, such as p+ doped polysilicon, to form gate electrodes for SONOS-type memory devices (*see id.*, ¶¶89-91, 107).

#### IV. CLAIM CONSTRUCTION

##### A. “oxygen-rich nitride” and “oxygen-lean nitride”

Independent claims 1, 12, and 16 recite “oxygen-lean” and “oxygen-rich” nitride layers. The ’240 patent does not provide a general definition of these terms, but does provide an example of “oxygen-rich” and “oxygen-lean” in connection with the embodiment depicted in figure 6:

By oxygen-rich it is meant wherein a concentration of oxygen in the oxygen-rich first nitride layer 616a is from about 15 to about 40%, whereas a concentration of oxygen in [an] oxygen-lean second nitride layer 616b is less than about 5%.

Ex. 1001 (’240 patent), 13:53-57; Ex. 1003, ¶¶109-110.

Based on this statement, a POSITA would have understood that (i) a nitride layer with about 5% or less oxygen is within the bounds of “oxygen-lean”; and (ii)

a nitride layer with about 15% or more oxygen is within the bounds of “oxygen-rich.” Ex. 1003, ¶111.

**B. “high work function gate electrode”**

Independent claims 12 and 16 (and dependent claims 9 and 11) of the '240 patent require “a high work function gate electrode.” This term was well-known to a POSITA prior to July 2012. Ex. 1003, ¶¶89-91, 112. The '240 patent uses “high work function gate electrode” according to its ordinary meaning: “[b]y high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased.” Ex. 1001 ('240 patent), 4:1-3. The '240 patent states that polysilicon doped with p-type impurities (e.g., boron) is an example of a high work function gate material. Ex. 1001 ('240 patent), 7:27-35; Ex. 1003, ¶113. Again, this is consistent with a POSITA's understanding of the term prior to July 2012. Ex. 1012 (Heo), [0046]; Ex. 1017 (Lai '676), [0067], [0072]; Ex. 1041 (Zheng), 5:36-37, 5:52-62; Ex. 1003, ¶¶112, 229, n. 8.

A POSITA thus would have understood “high work function gate electrode” in the context of the '240 patent to have its ordinary meaning, which encompasses gate electrodes comprised of, for example, polysilicon doped with p-type impurities and other materials known as high work function materials. Ex. 1012 (Heo), [0046]; Ex. 1017 (Lai '676), [0067], [0072]; Ex. 1041 (Zheng), 5:36-37, 5:52-62; Ex. 1003, ¶¶114, 229.

**C. “semiconductor material structure”**

Independent claims 12 and 16 and dependent claims 3, 4, 5, 14, 15, and 17 recite various limitations in relation to a “semiconductor material structure.” The claims do not set forth what makes up the “semiconductor material structure.” While the ’240 patent’s specification explains that a substrate may be formed of a “semiconductor material” (Ex. 1001 (’240 patent), 4:45-52) it does not explicitly set forth what else, if anything, would be included in a “semiconductor material structure.” Ex. 1003, ¶¶115-116.

During the prosecution of a descendent of the ’240 patent, Applicants stated that:

the words and phrases “memory device” and “semiconductor material structure,” as used throughout the present claims and application are synonymous with the words and phrases “memory transistor” and “semiconductor substrate” - which are explicitly supported in connection with Figs. 3 and 8-10, in the above cited paragraphs.

Ex. 1053 (’336 Pros. Hist.), 137); Ex. 1003, ¶117. This understanding is also consistent with how “semiconductor material structure” is used in the claims of the ’240 patent. Ex. 1003, ¶¶118-125; Ex. 1001 (’240 patent), claims 12, 16, 5, 14, 17, 2, 4 Figs. 9, 3, 6A, 7A, 18:9-22. Further, Patent Owner has identified a silicon

substrate as a “semiconductor material structure” in parallel litigation. Ex. 1054 (Infringement Contentions), 000017-18.

In view of the prosecution history, a POSITA would have considered “semiconductor material structure” to mean semiconductor substrate. Ex. 1003, ¶¶118-125.

## V. IDENTIFICATION OF CHALLENGE

### A. Statutory Grounds

Petitioner requests *inter partes* review and cancelation of the Challenged Claims on the following grounds:

| Grounds | Claims        | Statutory Basis   | Prior Art                                  |
|---------|---------------|-------------------|--------------------------------------------|
| 1       | 1, 3-7, 9, 11 | § 103 Obviousness | Lee '255, Lee '961<br>and Fujiwara         |
| 2       | 12-18         | § 103 Obviousness | Lee '255, Lee '961,<br>Fujiwara, and Hwang |

Under 35 U.S.C. § 103, a party may not obtain a patent “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious” to a POSITA at the time of the invention. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). “The combination of familiar elements according to known methods is likely to be

obvious when it does no more than yield predictable results.” *Id.* As discussed below, the challenged claims of the ’240 patent are obvious under § 103.

## **B. Relied-Upon Prior Art**

### **1. Lee ’255 (Ex. 1004)**

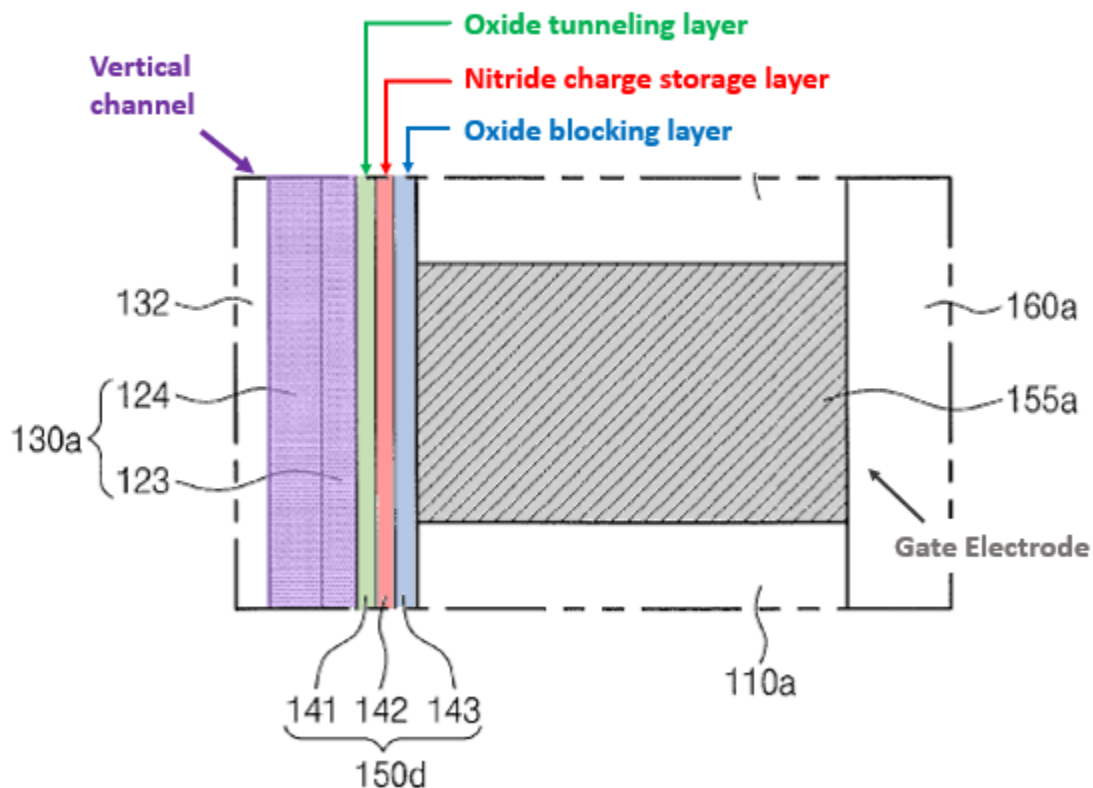
Lee ’255 is a U.S. Patent Application Publication that was published on March 22, 2012 from an application filed on August 29, 2011. Ex. 1004 (Lee ’255), 000001. Lee ’255 is prior art under § 102(a) because the invention was described in a U.S. patent application that was filed and published before July 1, 2012. Ex. 1003, ¶127.

Lee ’255 was not cited or considered during prosecution of the ’240 patent. *See generally* Ex. 1002; *see also* Ex. 1003, ¶128.

Lee ’255 teaches “a three-dimensional (3D) semiconductor memory device” and method for fabricating the same. Ex. 1004 (Lee ’255), [0002]-[0004]; Ex. 1003, ¶129. For example, figure 4A of Lee ’255 depicts a 3D memory device with a vertical channel 130a (purple) that passes through a stack of layers (110a, 155L, 155a, 155U) formed over a substrate 100 (light gray):



Fig. 4B



Ex. 1004 (Lee '255), Fig. 4B, [0057], [0074]; Ex. 1003, ¶130.

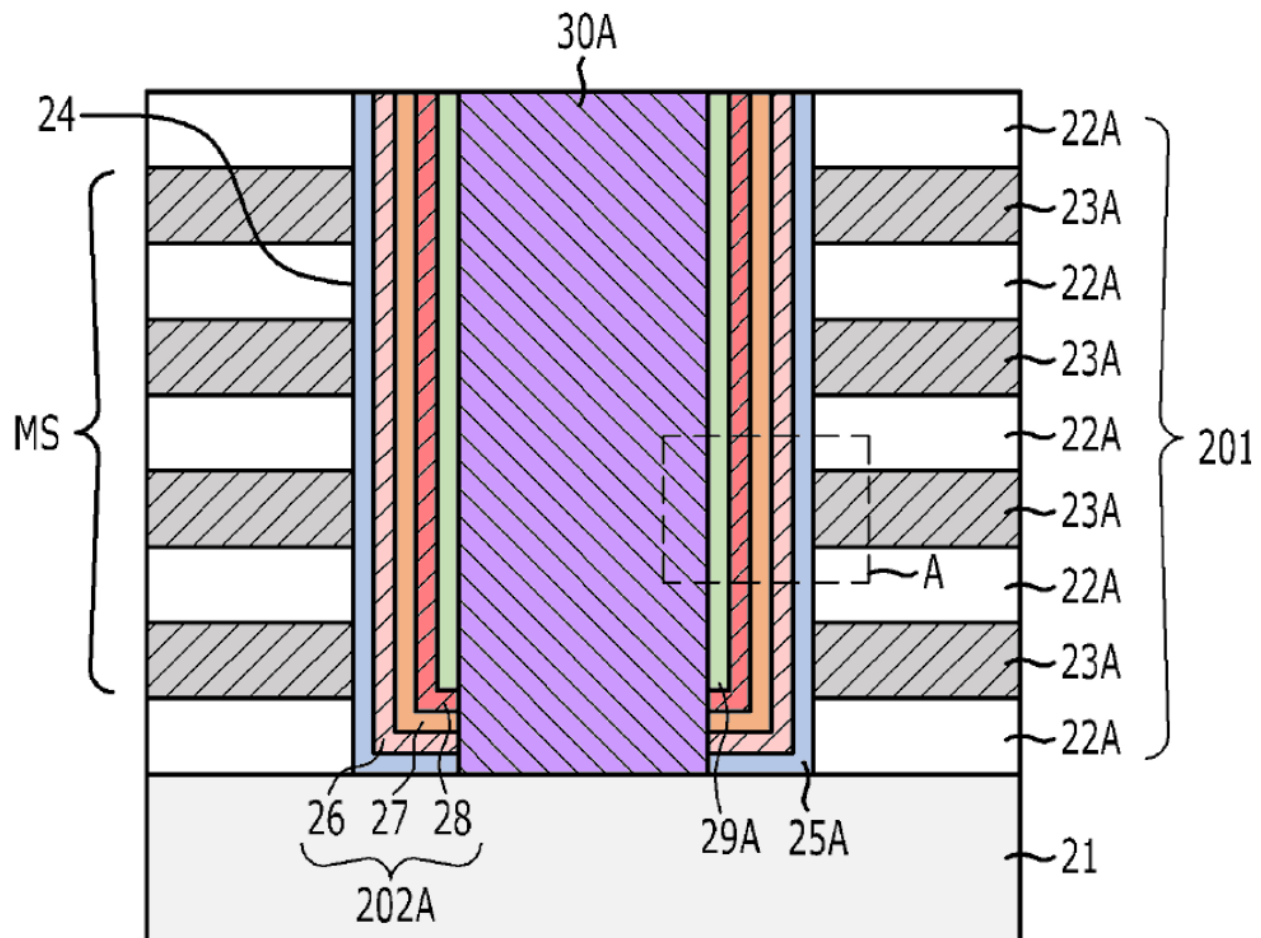
Lee '255 is analogous art to the '240 patent because it teaches improvements to NVM devices generally, and charge trap memory devices specifically. Ex. 1003, ¶131.

## 2. Lee '961 (Ex. 1005)

Lee '961 is a Korean Patent Publication. *See* Ex. 1005 (Korean language original and certified English translation of same). Lee '961 is prior art under § 102(a) because Lee '961 was published on November 2, 2011. Lee '961 was not

cited or considered during prosecution of the '240 patent. *See generally* Ex. 1002; *see also* Ex. 1003, ¶¶132-133.

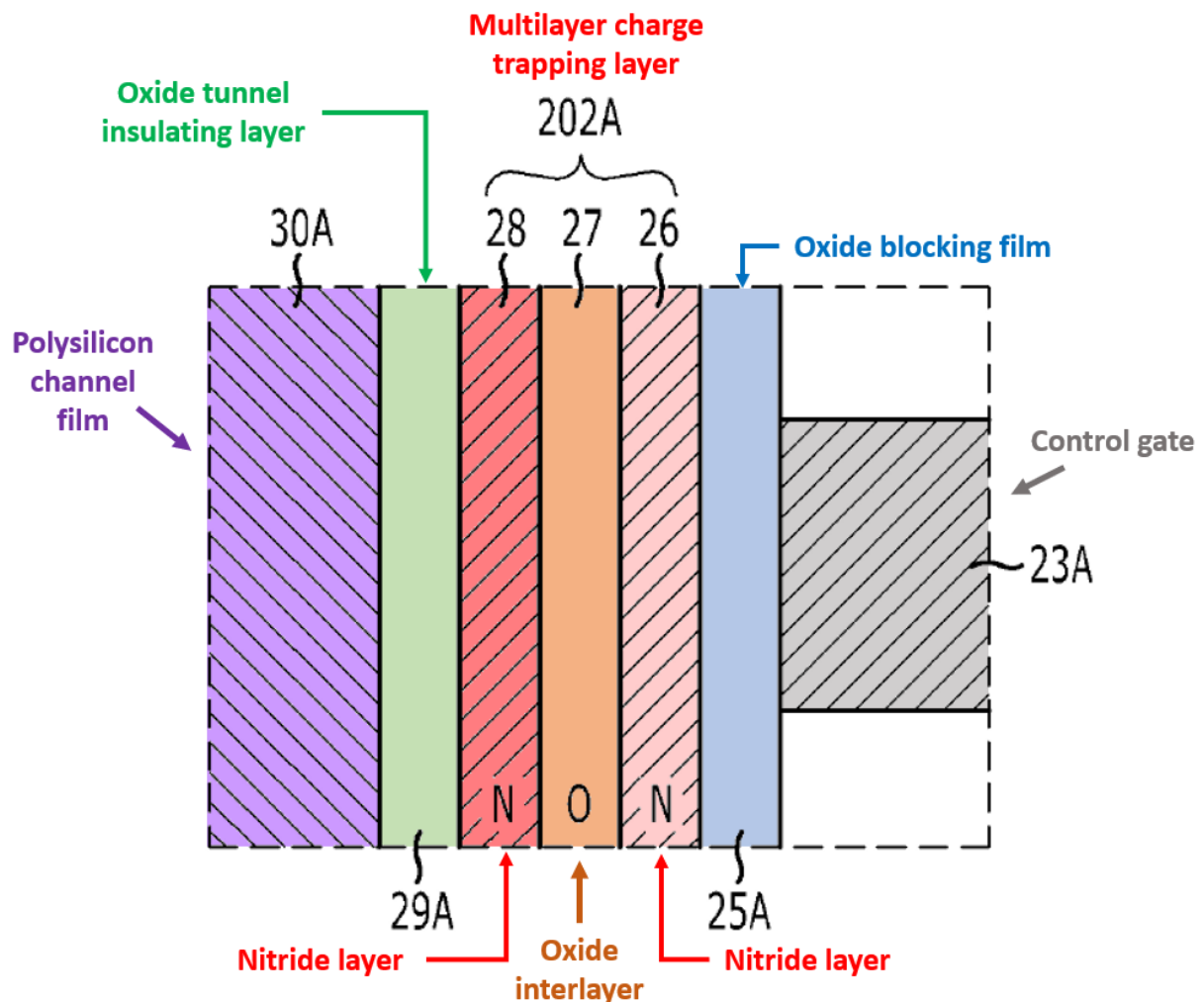
Lee '961 teaches a 3D charge trap memory device with a stack of layers (201) formed over a substrate (21) as shown in annotated figure 2a below. The stack includes alternating insulating layers (22A) and gate electrodes (23A):



Ex. 1005 (Lee '961), Fig. 2a, [0017]-[0019]; Ex. 1003, ¶134.

Lee '961 teaches a vertical 3D structure where a polysilicon channel is surrounded by oxide tunnel insulating layer 29A, multilayered charge trap layer

202A, and oxide blocking film 25A. Ex. 1005 (Lee '961), [0017]-[0019]; Ex. 1003, ¶135. As shown in annotated figure 2b below, multilayer charge trap layer 202A includes nitride layer 28, oxide interlayer 27, and nitride layer 26:



Ex 1005 (Lee '961), Fig. 2b, [0020]; Ex. 1003, ¶135.

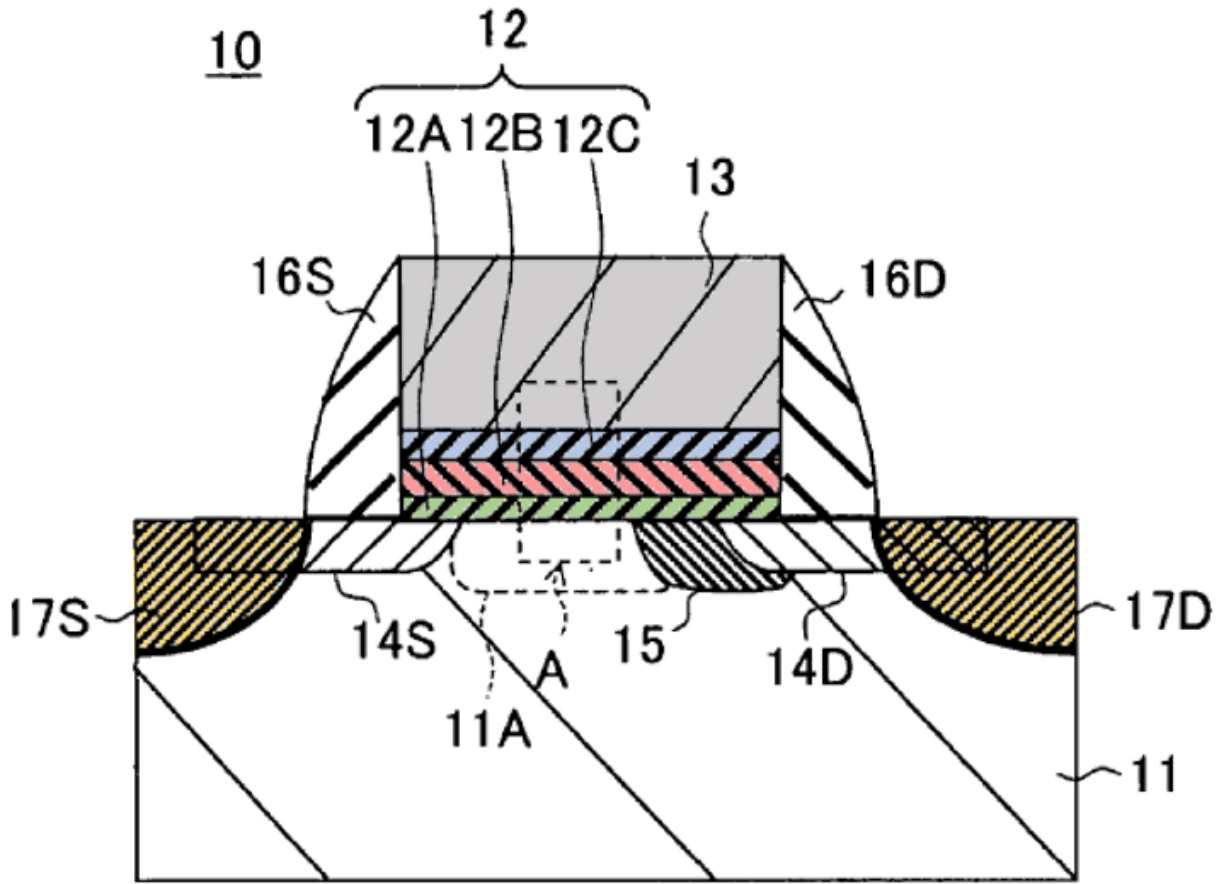
Like Lee '255, Lee '961 is analogous art to the '240 patent because it teaches improvements to NVM devices generally, and charge trap memory devices specifically. Ex. 1003, ¶136.

### **3. Fujiwara (Ex. 1006)**

Fujiwara is a U.S. Patent Application Publication that was published on March 30, 2006 from an application filed on September 16, 2005. Ex. 1006 (Fujiwara), 000001. Fujiwara is prior art under §102(a) because it was published before July 1, 2012. Ex. 1003, ¶137.

Fujiwara was listed on an information disclosure statement submitted during prosecution of the '240 patent, along with more than 500 other prior art references. The Examiner did not cite or apply Fujiwara in any Office Action, nor provide any substantive analysis of Fujiwara in allowing the claims of the '240 patent. Ex. 1003, ¶138.

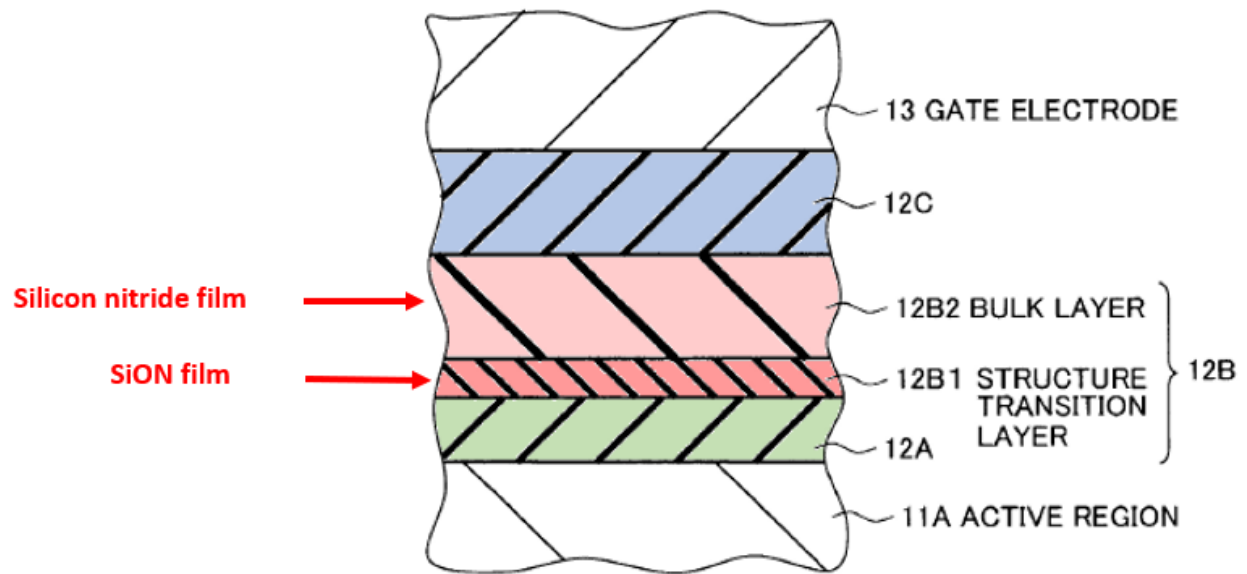
Fujiwara teaches a charge-trapping memory transistor with multiple nitride layers. Ex. 1006 (Fujiwara), [0037]-[0038], [0197], [0220]; Ex. 1003, ¶139. Fujiwara teaches a memory transistor with: (i) semiconductor substrate 11 with source 17S and drain 17D; (ii) first/bottom silicon oxide film 12A; (iii) silicon nitride charge storage layer 12B; (iv) second/top silicon oxide film 12C; and (v) gate 13:



Ex. 1006 (Fujiwara), Fig. 2, [0072]-[0084], [0146]-[0154]; Ex. 1003, ¶140.

Fujiwara further teaches that the silicon nitride charge storage layer 12B can be made of two nitride layers – lower silicon oxynitride (SiON) structure transition layer 12B1 and upper silicon nitride charge storage layer 12B2, where the SiON structure transition layer 12B1 is provided to: (i) improve the film quality of layer 12B; and (ii) improve data retention characteristics.

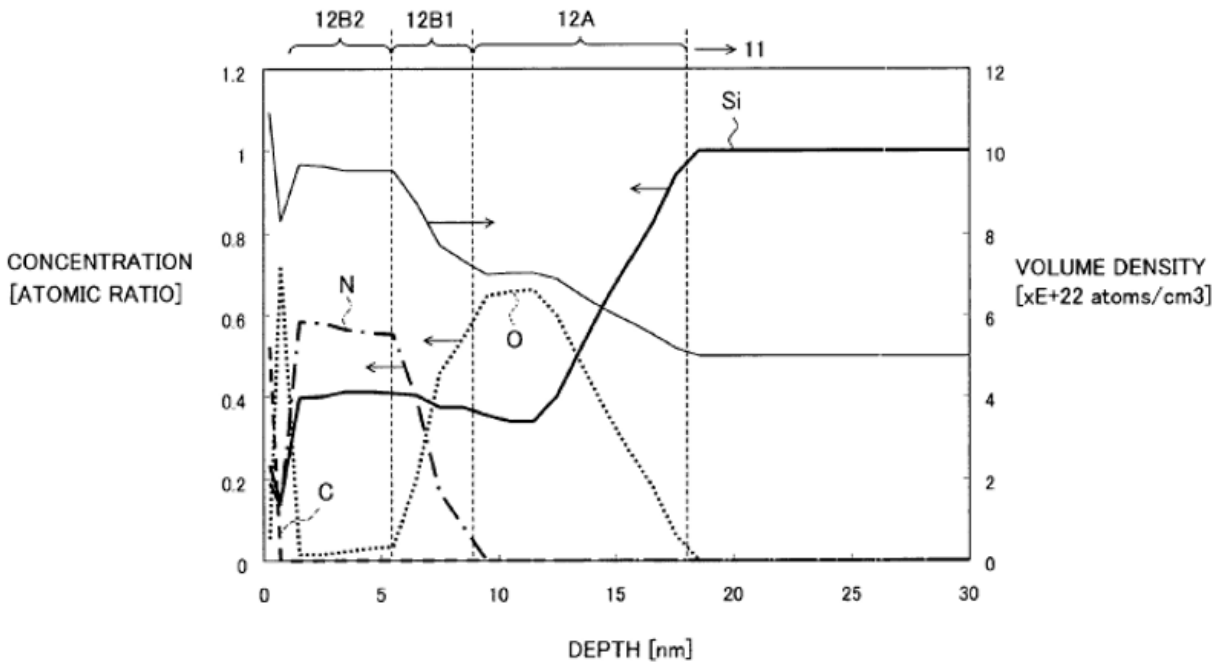
FIG. 21



Ex. 1006 (Fujiwara), Fig. 21, [0197]-[0208]; Ex. 1003, ¶141.

Fujiwara also teaches the relative oxygen (O), nitrogen (N), and silicon (Si) concentrations in each layer in Fig. 22:

FIG. 22



Ex. 1006 (Fujiwara), Fig. 22, [0200]; Ex. 1003, ¶142.

As with Lee '255 and Lee '961, Fujiwara is analogous art to the '240 patent because it teaches improvements to NVM devices generally, and charge trap memory devices specifically. Ex. 1003, ¶143.

#### 4. Hwang (Ex. 1048)

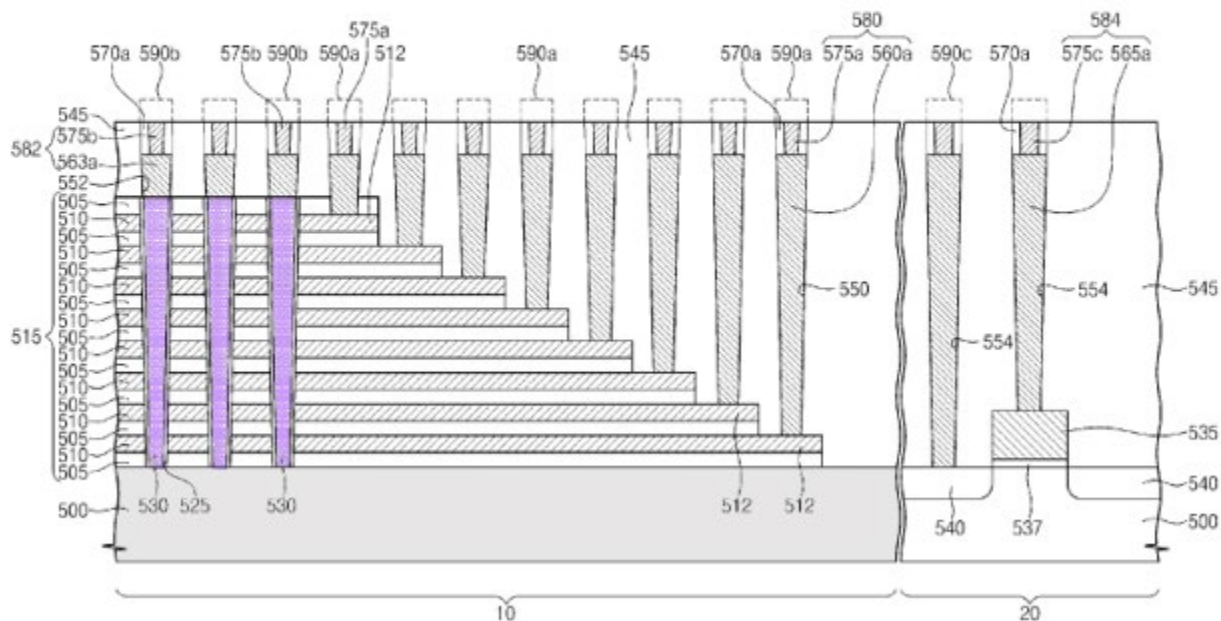
Hwang is a U.S. Patent Application Publication that was published on March 15, 2012 from an application filed on September 9, 2011. Ex. 1048, 000001. Hwang identifies five inventors: Sung-Min Hwang, Hansoo Kim, Changseok Kang, Wonseok Cho, and Jae-Joo Shim. Hwang is prior art under §102(a) because

it was published before July 1, 2012 from an application filed by others. Ex. 1003, ¶144.

Hwang was not cited or considered during prosecution of the '240 patent. *See generally* Ex. 1002; *see also* Ex. 1003, ¶148.

Hwang teaches “three dimensional semiconductor memory devices.” Ex. 1048 (Hwang), [0007]. For example, the 3D memory device depicted in Fig. 6 (annotated below) includes a vertical channel 530 (purple) that passes through an alternating stack of insulating (505) and gate (510) patterns formed over a substrate 500 (gray).

Fig. 6



Ex. 1048 (Hwang), Fig. 6, [0112]; Ex. 1003, ¶145.

Hwang also teaches the provision of MOS logic transistors in peripheral circuit region 20 and the electrical connections thereto. Ex. 1048 (Hwang), [0112]-[0113]. Figure 6 shows such a MOS logic transistor on the right-hand side of the figure, including peripheral gate 535, peripheral gate dielectric layer 537, peripheral source/drain regions 540, and an unlabeled channel between source/drain regions 540. *Id.*; Ex. 1003, ¶147.

A POSITA would have understood that Hwang is analogous art to the '240 patent because it teaches improvements to non-volatile memory devices generally, and charge trap memory devices specifically. Ex. 1003, ¶149.

## **VI. INVALIDITY GROUNDS**

### **A. Ground 1: Obviousness over Lee '255, Lee '961, and Fujiwara**

A POSITA would have found claims 1, 3-7, 9 and 11 of the '240 patent obvious over the teachings of Lee '255, Lee '961, and Fujiwara. Ex. 1003 ¶¶151-231.

Lee '255 teaches a 3D vertical SONOS charge trap-type NVM device. Ex. 1004 (Lee '255), Figs. 4A, 4B, [0003]. Lee '255 teaches most of the limitations of Challenged Claims, including, (i) a high work function gate electrode; (ii) a vertical channel; (iii) an ONO stack along the channel that includes a tunnel dielectric layer, a nitride charge trapping layer, and a blocking dielectric layer; and (iv) a MOS logic device. Ex. 1004 (Lee '255), [0050]-[0074]; Ex. 1003, ¶152.

Lee '961 also teaches a 3D vertical SONOS charge trap-type NVM device. Ex. 1005 (Lee '961), [0002]-[0006]. Lee '961 teaches that prior art 3D memory devices similar to the device taught in Lee '255 can suffer from leakage of charges. *Id.*, Fig. 1, [0006]. To provide improved data retention properties, Lee '961 teaches including a SONONOS configuration with a “multilayered charge trap layer.” Ex. 1005 (Lee '961), [0010]; *see also id.*, [0012], [0015], [0017], [0020]; Ex. 1003, ¶153.

Fujiwara, like Lee '255 and Lee '961, relates to SONOS charge trapping-type nonvolatile memory devices. Ex. 1006 (Fujiwara), [0003]. In particular, Fujiwara teaches that using an oxygen-rich lower nitride layer and an oxygen-lean upper nitride layer promotes charge retention. Ex. 1006 (Fujiwara), [0197]-[0218], Figs. 21, 22; Ex. 1003, ¶154.

As discussed below, a POSITA would have been motivated to modify the nitride charge trapping layer of Lee '255 to incorporate the “multilayered charge trap layer” configuration taught in Lee '961. Ex. 1003, ¶¶155, 185-196. A POSITA would have been motivated to further modify the combination of Lee '255 and Lee '961 based on Fujiwara's teachings regarding optimized oxygen concentrations in multiple nitride layers to achieve improved charge retention. Ex. 1003, ¶¶156, 191-208.

The combination of Lee '255, Lee '961, and Fujiwara differs from prior art considered during prosecution. Ex. 1003, ¶157. In allowing claims 1, 12, and 16, the Examiner did not analyze Lee '255, Lee '961, or Fujiwara, individually or in combination. *See generally*, Ex. 1002 (Pros. Hist.); Ex. 1003, ¶157. Had the Examiner considered the combination of Lee '255, Lee '961, and Fujiwara, he would have determined that the references teach the features that he found missing from the prior art, including a multilayer charge-trapping region used with a vertical channel and including an anti-tunneling layer. Ex. 1002 (Pros. Hist.), 000110-111; Ex. 1003, ¶157.

### 1. Independent claim 1

|                                            |
|--------------------------------------------|
| <b>[1pre] A memory device, comprising:</b> |
|--------------------------------------------|

Lee '255 teaches *a memory device*<sup>1</sup> because Lee '255 teaches “a three-dimensional (3D) **semiconductor memory device** and a method of fabricating the same.” Ex. 1004 (Lee '255), [0002] (emphasis added); *see also, e.g., id.*, Abstract, Figs. 1A-5B, [0074]; Ex. 1003, ¶158.

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<sup>1</sup> Petitioner uses italics throughout the analysis of the invalidity grounds to identify claim language and distinguish claim language from quotations to the prior art.

|                                      |
|--------------------------------------|
| <b>[1a]</b> <b>a gate structure;</b> |
|--------------------------------------|

Lee '255 teaches limitation [1a] because Lee '255 teaches a memory device that includes gate electrodes 155a (each *a gate structure*). Ex. 1004 (Lee '255), Figs. 1A, 4A, 4B, and 5A, [0051], [0055]-[0058], [0059] (“Gate patterns 155a1 and 155a between the uppermost gate pattern 155U and the lowermost gate pattern 155L may correspond to cell gates”), [0060]; Ex. 1003, ¶159.

The arrangement of gate electrodes 155a is shown, for example, in annotated figures 4A and 4B (detail C in FIG. 4A) below, where the gates 155a are highlight in dark gray shading:

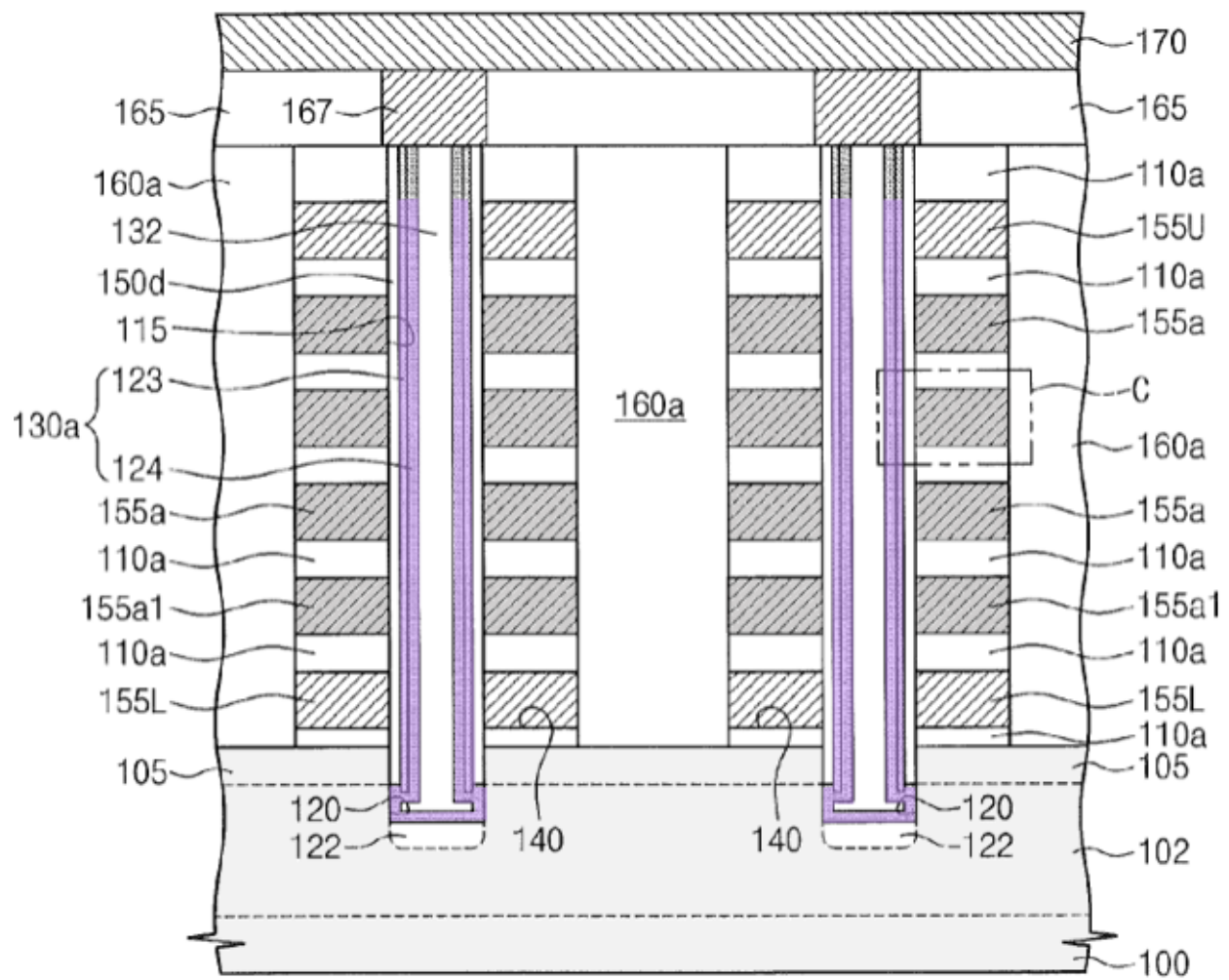
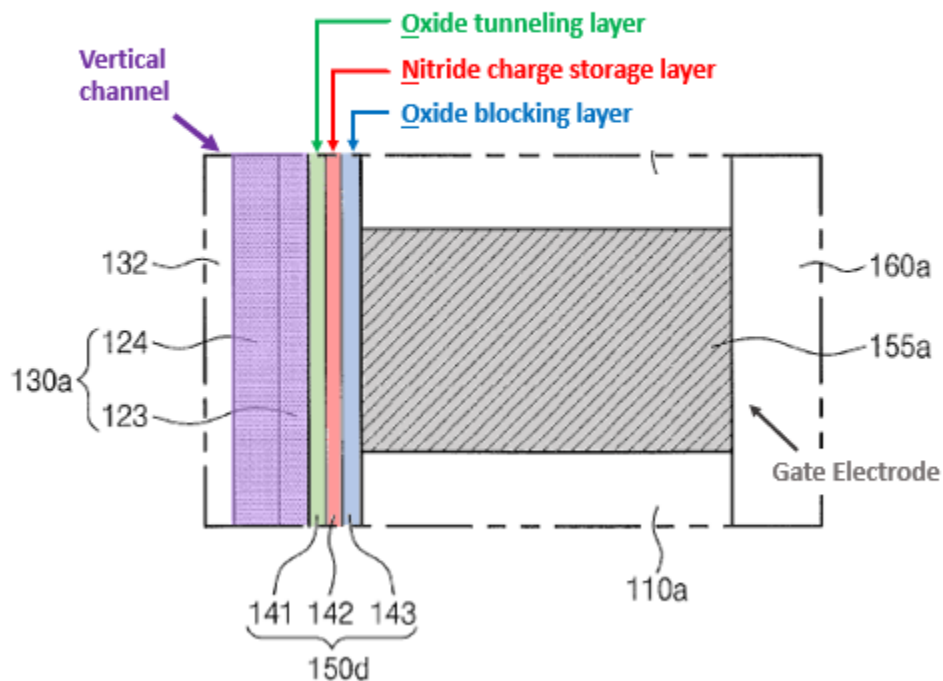


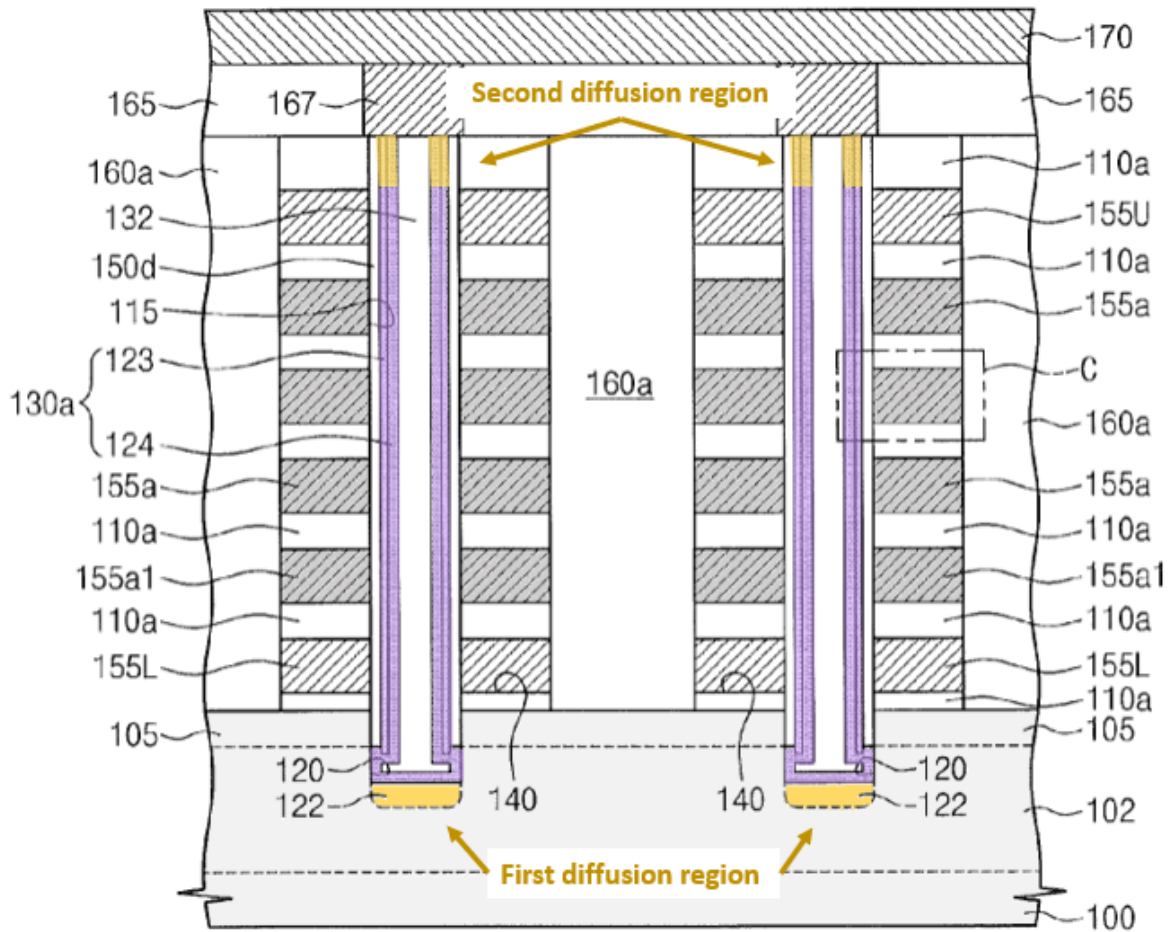
Fig. 4B



Ex. 1005 (Lee '255), Figs. 1A, 4A, 4B, [0051]-[0060], [0074]; Ex. 1003, ¶160.

**[1b] a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and**

Lee '255 teaches *a channel* because it teaches “**vertical channel regions** that are defined in the sidewall of vertical active pattern” 130/130a. Ex. 1004 (Lee '255), [0059], [0058]. The vertical active pattern 130/130a (*a channel*), highlighted in purple, is arranged in the device so as to “pass through each of the stack-structures” (*id.*, [0061]), as depicted in figure 4A:



Ex. 1004 (Lee '255), Fig. 4A; *see also id.*, [0052]; Ex. 1003, ¶162.

Lee '255 teaches a *first diffusion region* because Lee '255 teaches a high concentration (i.e., heavily doped) region 122, formed by introducing a first conductive dopant into well region 102. Ex. 1004 (Lee '255), FIG. 4A, 6B, [0053], [0067], [0081]. Region 122 is shaded in gold and labeled in annotated figure 4A, above. Ex. 1003, ¶163. Lee '255 also teaches a *second diffusion region*, because Lee '255 teaches a drain doped with a second conductive dopant formed in the upper portion of vertical active pattern 130/130a, with its lower surface adjacent to

the uppermost gate pattern 155U. Ex. 1004 (Lee '255), [0063]. This drain region is shaded in gold and labeled in annotated figure 4A, above. Ex. 1003, ¶164.

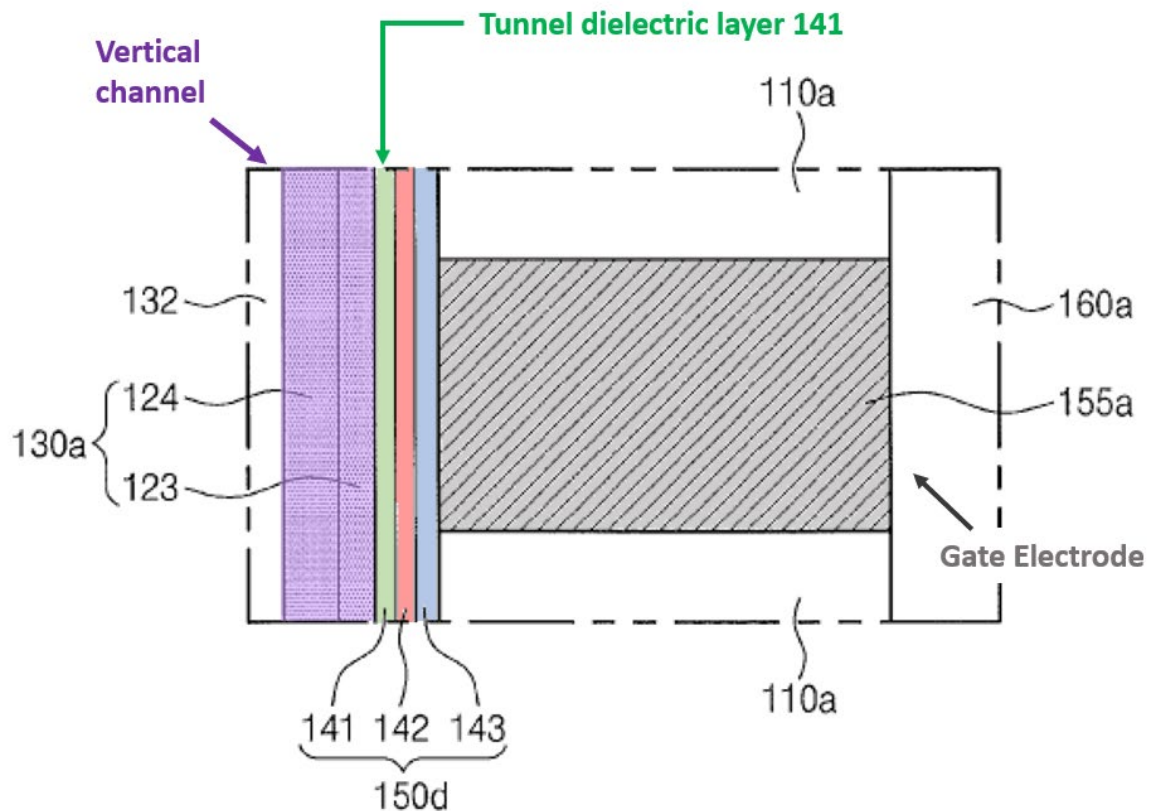
A POSITA would have understood that *diffusion regions*—e.g., sources and drains—are regions doped with conductive dopants so that charge carriers (electrons or holes) flow to or from those regions through a channel. *See, e.g.*, Ex. 1042 (Sze), 000016; Ex. 1001 ('240 patent), 8:32-34, 8:18-20 (identifying the source and drain regions as “heavily doped” and separated by the channel); Ex. 1003, ¶165.

Lee '255 teaches that active pattern 130/130a (a channel) is *positioned between and electrically connecting* high concentration region 122 (*first diffusion region*) and a drain (*second diffusion region*), as shown in figure 4A, above, since these regions are formed of conductive materials and arranged for current flow. Ex. 1004 (Lee '255), [0064], [0053] (“the first **conductive** dopant concentration of the portion 122”), [0063] (“a drain being doped with the second **conductive** dopant”); Ex. 1003, ¶166. A POSITA would also have understood these elements as electrically connected because in charge trapping memory devices, electrons flow in the vertical channel between diffusion regions to enable electrons tunneling into charge capture layers. *See e.g.*, Ex. 1008, 4:32-45; Ex. 1003, ¶166. Patent Owner has also identified a structure similar to that of figure 4A of Lee '255 as satisfying limitation [1b]. *See* Ex. 1054 (Infringement Contentions), 000010-11.

**[1c] a tunnel dielectric layer,**

Lee '255 teaches limitation [1c] because it teaches that its “gate dielectric layer 150d” includes “tunnel dielectric layer 141.” Ex. 1004 (Lee '255), Fig. 4A/B, [0055]-[0057].

**Fig. 4B**

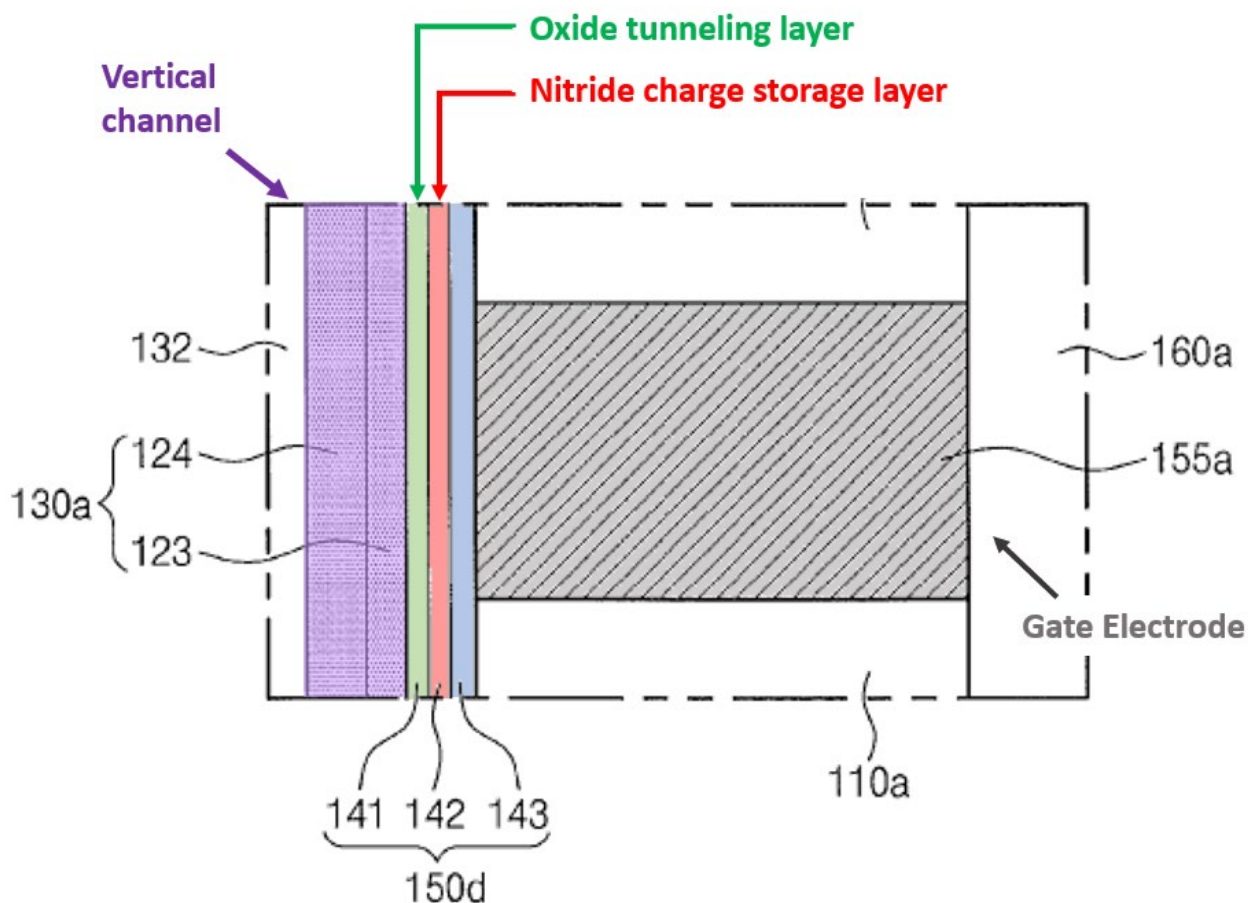


Ex. 1004 (Lee '255), Figs. 4B; Ex. 1003, ¶167.

[1d] a multi-layer charge trapping layer, and

The combination of Lee '255 and Lee '961 teaches limitation [1d]. Lee '255 teaches a *charge trapping layer* because it teaches that its “gate dielectric layer 150d” includes a nitride “charge storage layer 142.” Ex. 1004 (Lee '255), Fig. 4B, [0055]-[0057]. Lee '255 teaches that charge storage layer 142 has “traps for storing electric charges.” *Id.*, [0057].

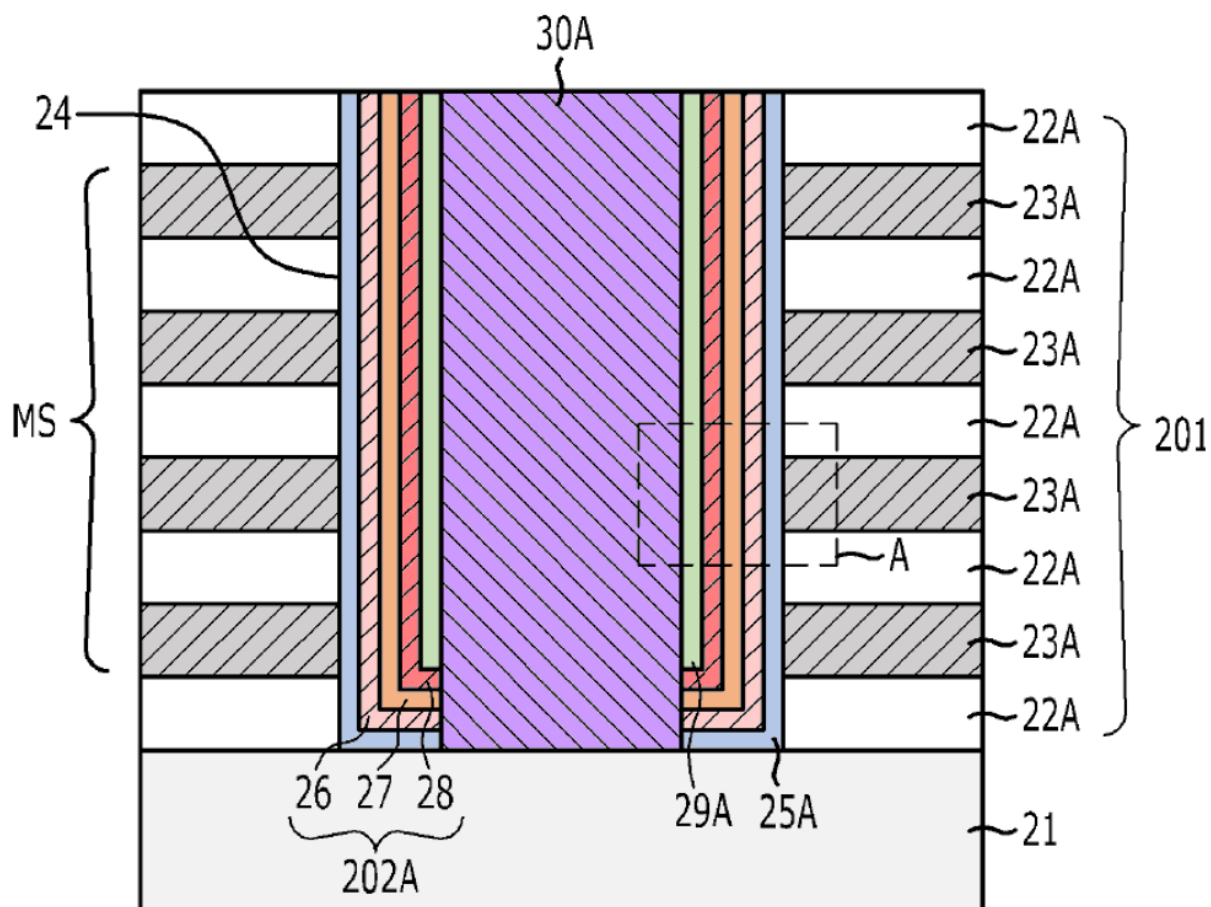
Fig. 4B



Ex. 1004 (Lee '255), Figs. 4B, *see also id.*, [0074]-[0075]; Ex. 1003, 169. A charge “trapping” layer and charge “storage” layer would have been synonymous to a POSITA as those terms and concepts are used interchangeably in the prior art. Ex. 1003, ¶168.

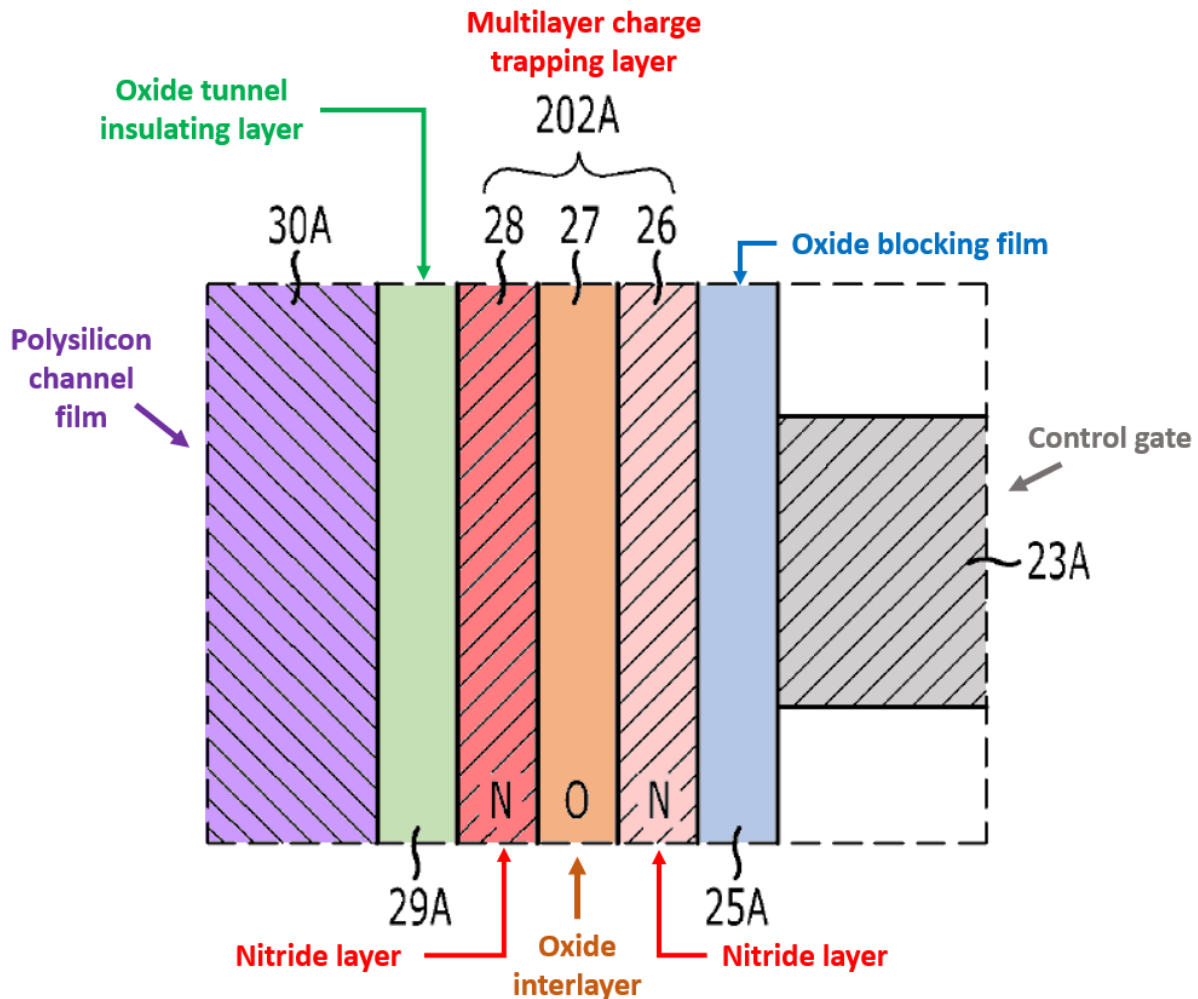
While figure 4B of Lee '255 depicts gate dielectric layer 150d with three layers (141–143), Lee '255 teaches that additional oxide or oxynitride layers may be incorporated, such as those disclosed in Lee '961. Ex. 1004 (Lee '255), [0057]; Ex. 1003, ¶170.

Lee '961 teaches a “multilayered charge trap layer” 202A (*a multi-layer charge trapping layer*) that “improv[es] the data retention properties of non-volatile memory devices” such as the device of Lee '255. Ex. 1005 (Lee '961), [0008], [0010]. Figure 2a depicts Lee '961's multilayered charge trap layer 202A:



Ex. 1005 (Lee '961), Fig. 2a; Ex. 1003, ¶171.

Lee '961's *multi-layer charge trapping layer* 202A is further depicted in figure 2b, which is a magnified view of box "A" from figure 2a:



Ex. 1005 (Lee '961), Figures 2b, [0013], [0018]-[0021]; Ex. 1003, ¶172.

As reflected above, Lee '961 teaches an ONONO stack, where the multi-layer charge trapping layer is positioned between an oxide tunneling dielectric layer (layer 29A, green) and a blocking dielectric layer (layer 25A, blue). Ex. 1005 (Lee '961), Figs. 2a, 2b, [0017]-[0019]. Lee '961 further discloses the charge trap layer 202A has a multilayer structure with a nitride first trap layer (layer 28, red), an oxide interlayer (layer 27, orange), and a nitride second trap layer (layer 26, pink). Ex. 1005 (Lee '961), [0020], [0015]; Ex. 1003, ¶173.

A POSITA would be motivated to modify Lee '255's charge trapping layer to use a multilayer structure based on Lee '961. Ex. 1003, ¶¶174. A POSITA would have been motivated to apply Lee '961's ONONO stack teachings to the ONO stack of Lee '255 because Lee '961 includes an express teaching, suggestion, and motivation to use the multi-layer charge trapping region to improve SONOS configurations such as those taught in Lee '255. Ex. 1005 (Lee '961), Fig. 1, [0004]-[0006]; Ex. 1003, ¶¶175-176. In particular, Lee '255 teaches that memory devices with ONO stacks such as those taught in Lee '255 suffer from poor charge retention due to lateral spreading of charges in the single silicon nitride trapping film. *Id.* Lee '961 teaches that a solution to this problem is the multilayered charge trap layer (202A): "The present invention described above has the effect of improving the data retention properties of non-volatile memory devices by applying a multilayered charge trap layer comprising a plurality of trap layers and interlayers." Ex. 1005 (Lee '961), [0010]; Ex. 1003, ¶176.

Applying the multi-layer charge trapping region of Lee '961 to the memory device of Lee '255 would also have amounted to (i) combining prior art elements according to known methods to yield predictable results; and (ii) use of known techniques to improve a similar device in the same way. Ex. 1003, ¶177. The data retention benefits of using the multilayer charge trapping region of Lee '961 were well-known to a POSITA prior to July 2012. *Id.* Indeed, at that time, using

multilayer charge trapping structures was a routine and conventional strategy for improving charge retention, as reflected in numerous prior art references. Ex. 1003, ¶¶177, 60-88, *see, e.g.*, Ex. 1010 (Nomoto), [0035], [0044]-[0045], [0073]-[0088]; Ex. 1011 (Levy), [0025]-[0026]; Ex. 1012 (Heo), [0058]-[0068]; Ex. 1006 (Fujiwara), Fig. 21, [0197]-[0208]; Ex. 1009 (Kim '399), [0034], [0046]-[0047]; Ex. 1013 (Ganguly), [0020], [0048]-[0049]; Ex. 1017 (Lai '676), [0015], [0068]-[0077]; Ex. 1021 [0007], [0133]-[0134], [0141]-[0142]; Ex. 1014 (Wang '586), [0006], [0022], [0031]-[0032]; Ex. 1020 000003 (Fig. 3), 000006.

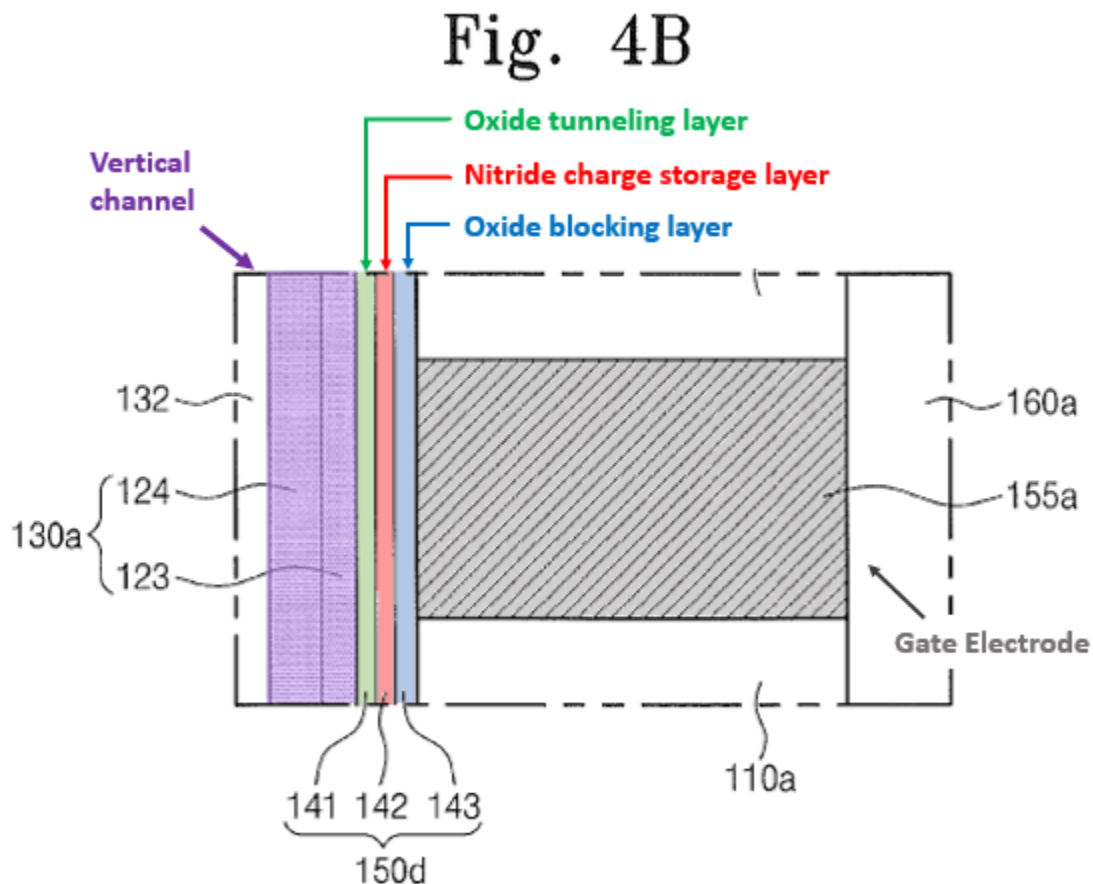
Applying the multilayer charge trap of Lee '961 to the memory device of Lee '255 also would have been obvious to try prior to July 2012. The selection of various trap configurations (e.g., ONO, ONNO, or ONONO) were routine design choices. Ex. 1003, ¶¶178, 55-88. These alternatives represented a finite number of predictable options available to a POSITA to optimize charge trap memory devices. Ex. 1003, ¶178.

A POSITA would have reasonably expected success in modifying Lee '255's memory device to incorporate Lee '961's multilayer charge trapping region, as both references disclose similar 3D charge trap memory structures. Ex. 1003, ¶¶179, 55-88; Ex. 1004 (Lee '255), Fig. 4A; Ex. 1005 (Lee '961), Fig. 1, [0002]-[0010]. Adopting Lee '961's multilayer structure in Lee '255 would merely involve using established techniques to deposit additional layers during fabrication,

which Lee '255 already contemplates. Ex. 1004 (Lee '255), [0057]; Ex. 1003, ¶179.

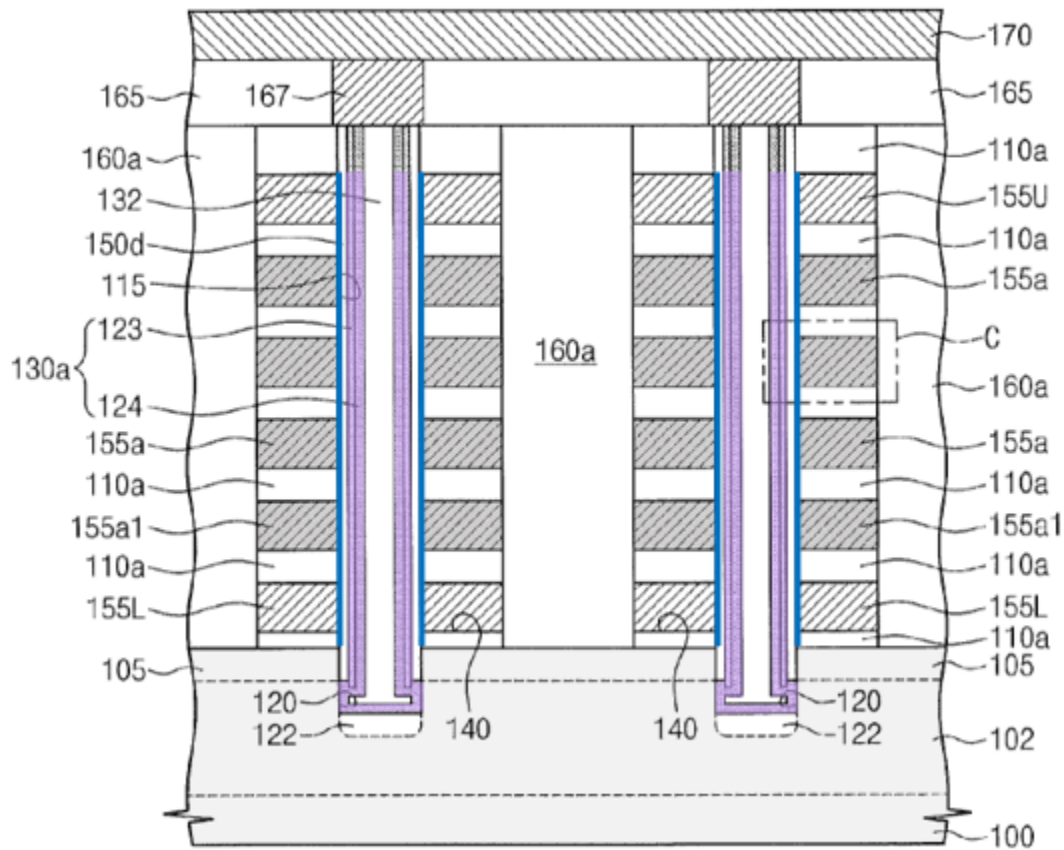
|             |                                                                                         |
|-------------|-----------------------------------------------------------------------------------------|
| <b>[1e]</b> | <b>a blocking dielectric layer disposed between the gate structure and the channel,</b> |
|-------------|-----------------------------------------------------------------------------------------|

Lee '255 teaches limitation [1e] because it teaches that the “gate dielectric layer 150d” includes an oxide “blocking dielectric layer 143” (*a blocking dielectric layer*) that is positioned between gate 155a (*a gate structure*) and vertical active pattern 130/130a (*the channel*). Ex. 1004 (Lee '255), Fig. 4B, [0055]-[0057]; Ex. 1003, ¶181. This is shown, for example, in figure 4B:



Ex. 1004 (Lee '255), Fig. 4B. Ex. 1003, ¶181.

As reflected above, Lee '255 teaches that the *blocking dielectric layer* (blocking dielectric layer 143) is *disposed between the gate structure and the channel* because “blocking dielectric layer 143 is part of gate dielectric layer 150d” (Ex. 1004 (Lee), [0056]), which Lee '255 teaches is arranged “between a sidewall of the vertical active pattern 130 and each of the gate patterns 155L, 155a1, 155a and 155U” (*id.*, [0055]) such that the blocking dielectric layer 143 is “adjacent to each of the gate patterns 155L, 155a1, 155a, and 155U” (*id.*, [0056]). This arrangement is shown in annotated Fig. 4B above, where dielectric layer 150d (containing blocking dielectric layer 143 (indicated by blue lines)) is arranged between gray-shaded gate electrode 155a (*gate structure*) and purple-shaded active pattern 130/130a (*channel*). The position of the blocking layer is also highlighted in blue in the below annotated version of Fig. 4A, showing the blocking layer is between the gate structure (gray) and the channel (purple):

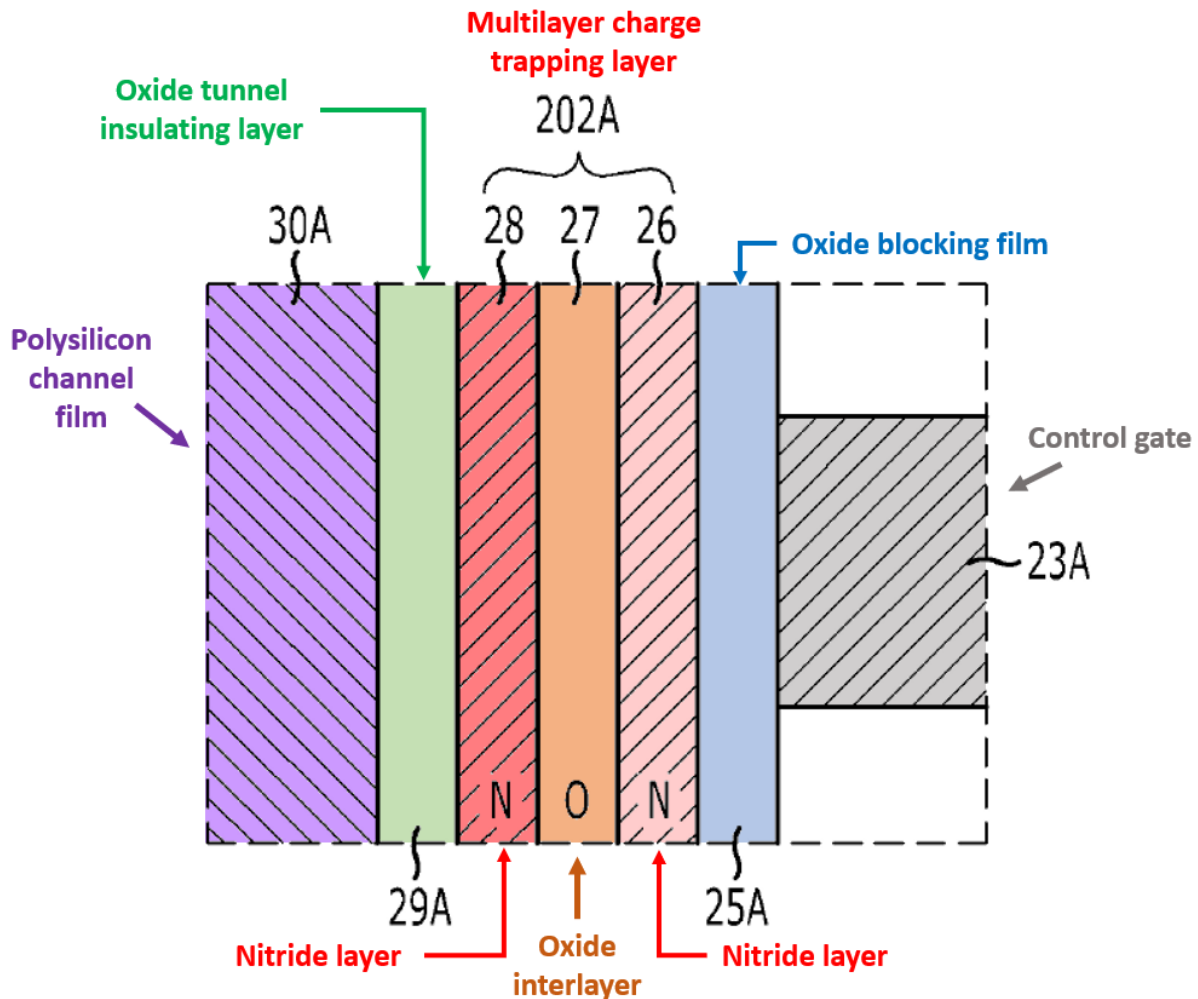


Ex. 1004 (Lee '255), Fig. 4A; Ex. 1003, ¶¶182-183.

As discussed above, a POSITA would have been motivated to modify the charge storage layer 142 of Lee '255 based on Lee '961's teachings of a multilayer charge storage layer. The resulting multilayer charge storage layer would maintain its position between the tunneling layer and blocking dielectric layer in the combination of Lee '255 and Lee '961. This placement of the charge trapping layer is taught in both Lee '255 (*see* Ex. 1004 (Lee '255), Fig. 4B) and Lee '961 (*see* Ex. 1005 (Lee '961), Fig. 2b). Ex. 1003, ¶184.

|             |                                                                                                                                                                                                                                                                                        |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>[1f]</b> | <b>wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer, and</b> |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

The combination of Lee '255 and Lee '961 teaches limitation [1f]. Ex. 1003, ¶185. As discussed above in connection with limitation [1d], a POSITA would have been motivated to modify the charge storage layer of Lee '255 to implement the multi-layer structure of Lee '961. Lee '961 teaches that the multi-layer charge trapping layer comprises *a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers* because it teaches that its multilayer charge trap layer 202A (*multi-layer charge trapping layer*) includes a nitride trap layer 28 (*a first dielectric layer*) and a nitride trap layer 26 (*a second dielectric layer*) with an oxide interlayer 27 (*an anti-tunneling layer*) that is *disposed between* the nitride trap layer 28 (*first dielectric layer*) and nitride trap layer 26 (*second dielectric layer*). Ex. 1005 (Lee '961), [0020]; *see also id.*, Fig. 2b, [0015], Ex. 1003, ¶186. This is shown in figure 2b of Lee '961:



Ex. 1005 (Lee '961), Fig. 2b; Ex. 1003, ¶187.

Lee '961 further teaches that *the anti-tunneling layer includes an oxide layer* because it teaches that “interlayer (27) comprises an oxide film.” Ex. 1005, [0020].

A POSITA would have understood silicon nitride trap layers 26, 28 of Lee '961 are *dielectric layers* at least because element [1g] (*see below*) specifies that the *dielectric layers* include nitride. Moreover, a POSITA would have understood silicon nitride layers on SONOS-type structures to be dielectrics. *See generally* Part I.B. and, e.g., Ex. 1014 (Wang '586), [0004], [0009], Ex. 1051 (Lue '625),

[0032], Ex. 1023 (Choi), [0031], Ex. 1030 (Jeon), [0044], Ex. 1031 (Shih), [0005], [0069], Ex. 1041 (Zheng), 2:50-51, 5:4-11, 11:44-45; Ex. 1003, ¶188.

A POSITA would have understood the foregoing configuration of a multilayer charge trap layer 202A (*multi-layer charge trapping layer*) that includes a nitride trap layer 28 (*a first dielectric layer*), a nitride trap layer 26 (*a second dielectric layer*), and an intervening oxide interlayer 27 (*an anti-tunneling layer*) to teach *the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers*. The claim language here explicitly contemplates the presence of an intervening *anti-tunneling layer* between the “abutting” dielectric layers, and a POSITA would therefore have understood “abutting” in the context of this claim language of the ’240 patent to include an intervening *anti-tunneling layer*. See also Ex. 1001 (’240 patent), Figs. 8A, 8B. Ex. 1003, ¶189.

A POSITA would have understood oxide interlayer 27 is the *anti-tunneling layer* because Lee ’961 teaches that the interlayer 27 prevents the loss (leakage) of charges that would otherwise accumulate at an interface region. Ex. 1005 (Lee ’961), [0031]-[0033]; Ex. 1003, ¶190. A POSITA would have understood that preventing the leakage of charges is anti-tunneling. See, e.g., Ex. 1017, [0071]. The function of the oxide interlayer of Lee ’961 is also consistent with the function

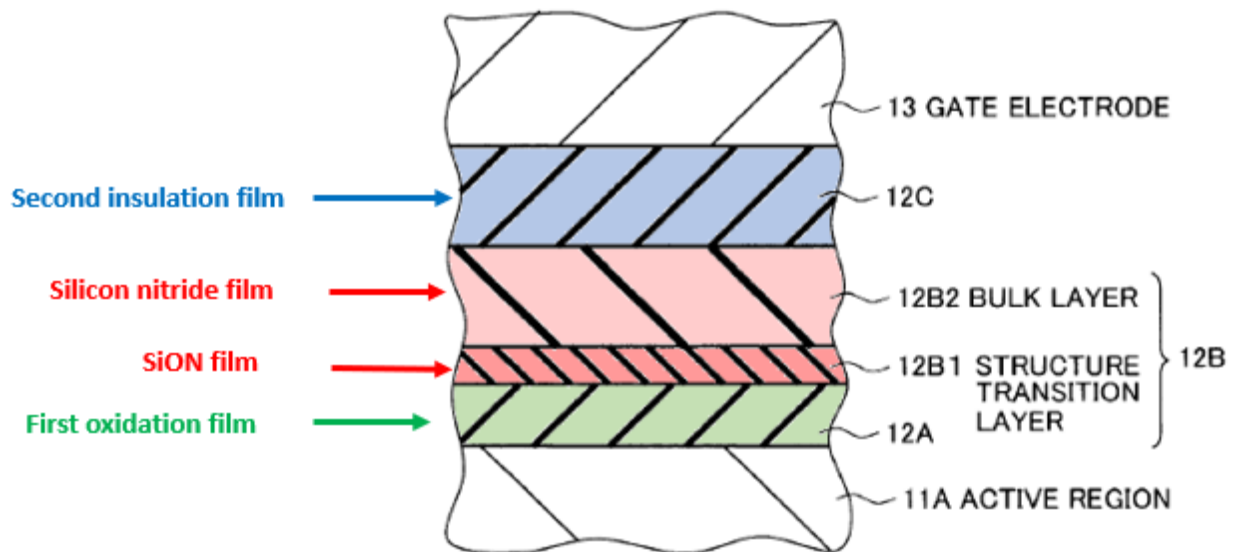
of an anti-tunneling layer described in the '240 patent. Ex. 1001 ('240 patent), 10:23-38; Ex. 1003, ¶190.

|                                                                                                                                                      |
|------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>[1g]            wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.</b> |
|------------------------------------------------------------------------------------------------------------------------------------------------------|

The combination of Lee '255, Lee '961, and Fujiwara teaches limitation [1g]. As set forth under limitations [1d] and [1f], the combination of Lee '255 and Lee '961 teaches *a multi-layer charge storing region* (Lee '961's multilayer charge trap layer 202A) that includes *a first dielectric layer* (nitride trap layer 28) disposed abutting *a second dielectric layer* (nitride trap layer 26). Ex. 1003, ¶¶191-192. A POSITA would have been motivated to further modify this combination to incorporate Fujiwara's teachings of optimal oxygen concentrations in nitride charge trapping layers. Ex. 1003, ¶193, 60-72.

Similar to Lee '961, Fujiwara teaches *a multi-layer charge storing region* that includes a silicon nitride "bulk layer" 12B2 (a [*first*] *oxygen-lean nitride layer*) and a silicon oxynitride (SiON) "transition layer" 12B1 (a [*second*] *oxygen-rich nitride layer*), as shown in Fig. 21:

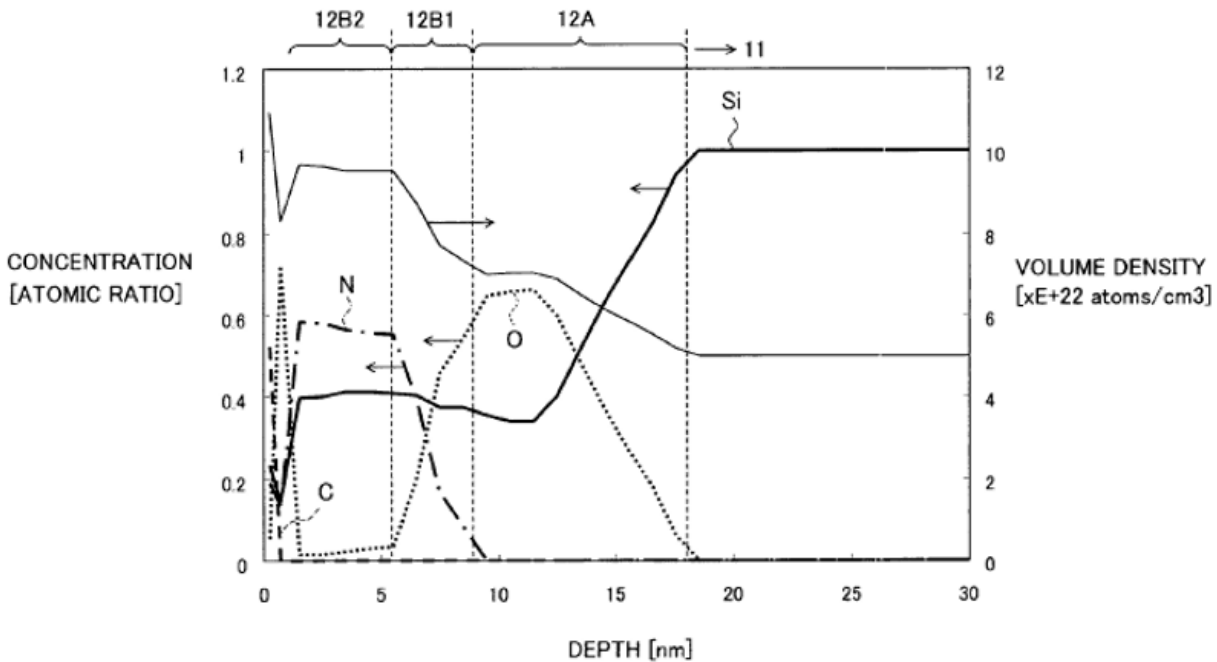
FIG. 21



Ex. 1006 (Fujiwara), Fig. 21; *see also id.*, Fig. 2, [0074], [0198]–[0201], [0212], [0215]–[0218]; Ex. 1003, ¶¶196–197.

Fujiwara teaches that the “transition layer (SiON) film” 12B1 is a *first dielectric layer that includes oxygen-rich nitride* and the nitride “bulk layer” 12B2 is a *second dielectric layer that includes oxygen-lean nitride*) based on the disclosed atomic composition profiles of those layers depicted in figure 22:

FIG. 22



Ex. 1006 (Fujiwara), Fig. 22 (dotted line representing oxygen (“O”)); *see also id.*, [0200]; Ex. 1003, ¶¶201.

As reflected above, layer 12B1 (the SiON transition layer) is the *first dielectric layer* and contains *oxygen-rich nitride*, with nitride peaks reaching around 50 atomic % oxygen internally and exceeding 15% for most of its depth. Layer 12B2 (the Si<sub>3</sub>N<sub>4</sub> bulk layer) is the *second dielectric layer* that includes *oxygen-lean nitride*, containing less than 5 atomic % oxygen throughout. *See also* Ex. 1006, Fig. 23; Ex. 1003, ¶202.

A POSITA would have been motivated to further modify the combination of Lee '255 and Lee '961 to apply the teachings of Fujiwara to optimize the oxygen

concentrations of the nitride layers of the multi-layer charge-trapping region. Ex. 1003, ¶¶203-204.

It would have been obvious for a POSITA to use Fujiwara to improve the memory transistor configuration of Lee '255 and Lee '961 because Fujiwara provides an express teaching, suggestion, and motivation to combine—that using the oxygen-rich and oxygen-lean nitride layers enhances charge retention in SONOS devices, which aligns with the goals of Lee '961 and Lee '255. Ex. 1006 (Fujiwara), [0197]; *compare* Ex. 1005 (Lee '961), [0008], [0010] *with* Ex. 1006 (Fujiwara), [0197], [0205]; Ex. 1003, ¶¶205.

Applying the teachings of Fujiwara to Lee '255 / Lee '961 also would have amounted to combining prior art elements according to known methods to obtain predictable benefits because using an oxygen-rich first nitride layer and a silicon-rich, oxygen-lean second nitride layer to improve charge retention characteristics in both SONNOS and SONONOS configurations was routine. Ex. 1003, ¶¶206-207 (citing Ex. 1012 (Heo), [0058]-[0068]; Ex. 1017 (Lai '676), [0015], [0068]-[0077]; Ex. 1011 (Levy), [0025]-[0026]; Ex. 1013 (Ganguly), Fig. 3, [0048]-[0050]; and Ex. 1021 [0007], [0133]-[0134], [0141]-[0142]).

A POSITA also would have expected success in applying Fujiwara's teachings concerning optimized oxygen concentrations to the multilayer charge trapping region of Lee '255 / Lee '961 because the underlying materials,

equipment, and processes are all mainstream. Ex. 1003, ¶208. While Lee '961 teaches an intermediate oxide layer between the two nitride charge trapping layers, a POSITA would have understood Lee 961's configuration to confirm the compatibility of Lee '961's lower nitride layer with Fujiwara's oxygen-rich nitride layer and also to provide the ideal location for the deposition of the intermediate oxide layer abutting the oxygen-rich nitride layer. Ex. 1003, ¶207. A POSITA would have understood that achieving the oxygen concentrations taught in Fujiwara would merely have required application of routine deposition processes that were well-known prior to July 2012. *Id.*

## **2. Dependent Claims 3-7, 9, 11**

- 3. The memory device of claim 1, wherein the channel, first and second diffusion regions are disposed above a semiconductor material structure.**
- 4. The memory device of claim 1, wherein the channel, first and second diffusion regions are suspended above a semiconductor material structure.**

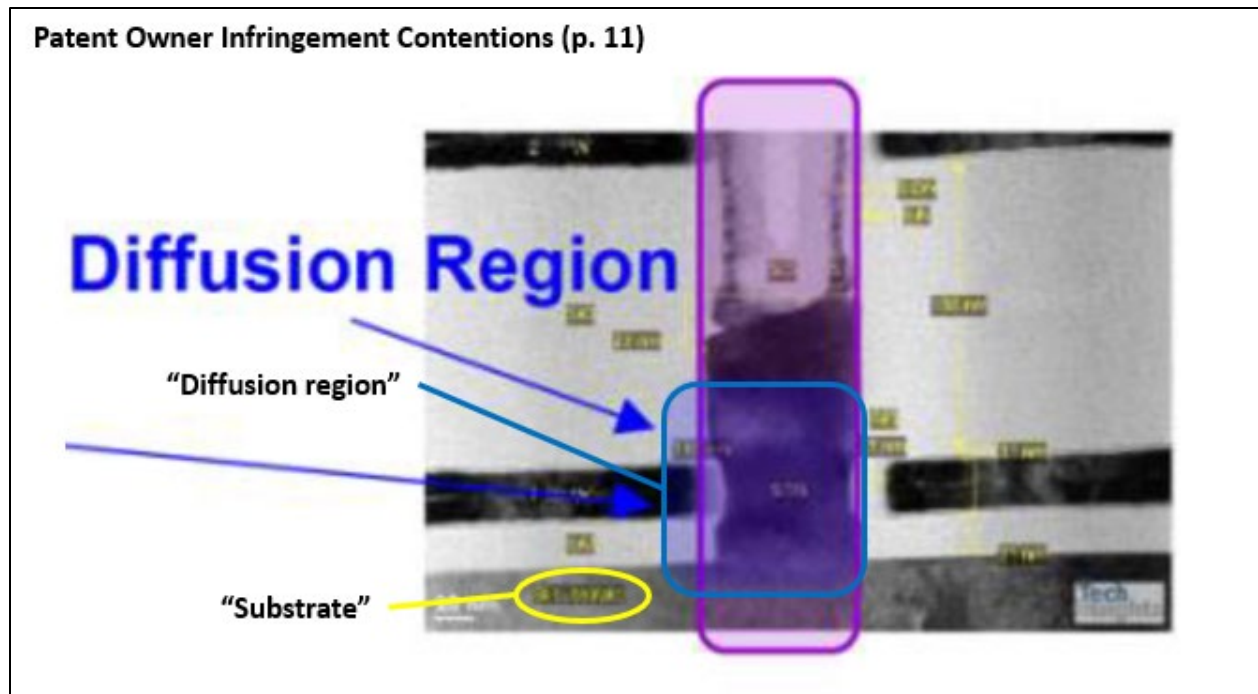
Lee '255 also teaches the additional limitations of claims 3 and 4. Ex. 1003, ¶¶209-216. In particular, in figure 12E, Lee '255 teaches the use of doped lower active pattern 250 in conjunction with high concentration region 122, (together, a *diffusion region*):

A POSITA would have found it obvious to employ doped lower active patterns 250 of figure 12E in connection with figure 4A of Lee '255 because Lee '255 teaches that the lower active patterns are available configurations within the inventive concept that provide improved reliability. Ex. 1004 (Lee '255), [0113], [0118]; Ex. 1003, ¶216. A POSITA also would have recognized that substituting the doped lower active pattern 250 into other Lee '255 embodiments was a routine design choice. Ex. 1003, ¶216.

As reflected above, figure 12E of Lee '255 teaches a channel and first and second diffusion regions that are *disposed above a semiconductor material structure* (claim 3) because at least a portion of the channel region (purple) and the diffusion regions (gold) is arranged above the top surface of a substrate (light gray). Lee '255 also teaches that the channel and the diffusion regions are suspended above a substrate because at least a portion of those features are arranged above the top surface of substrate 100 and are laterally supported (*suspended*) by the alternating gate 155 and dielectric 110 layers. Ex. 1004 (Lee '255), Fig. 12E; Ex. 1003, ¶¶214-215.

In parallel district court proceedings, Patent Owner alleges that structure similar to that of Lee '255 satisfies claims 3 and 4 of the '240 patent. In particular, Patent Owner identifies the following structure as infringing claims 3 and 4:

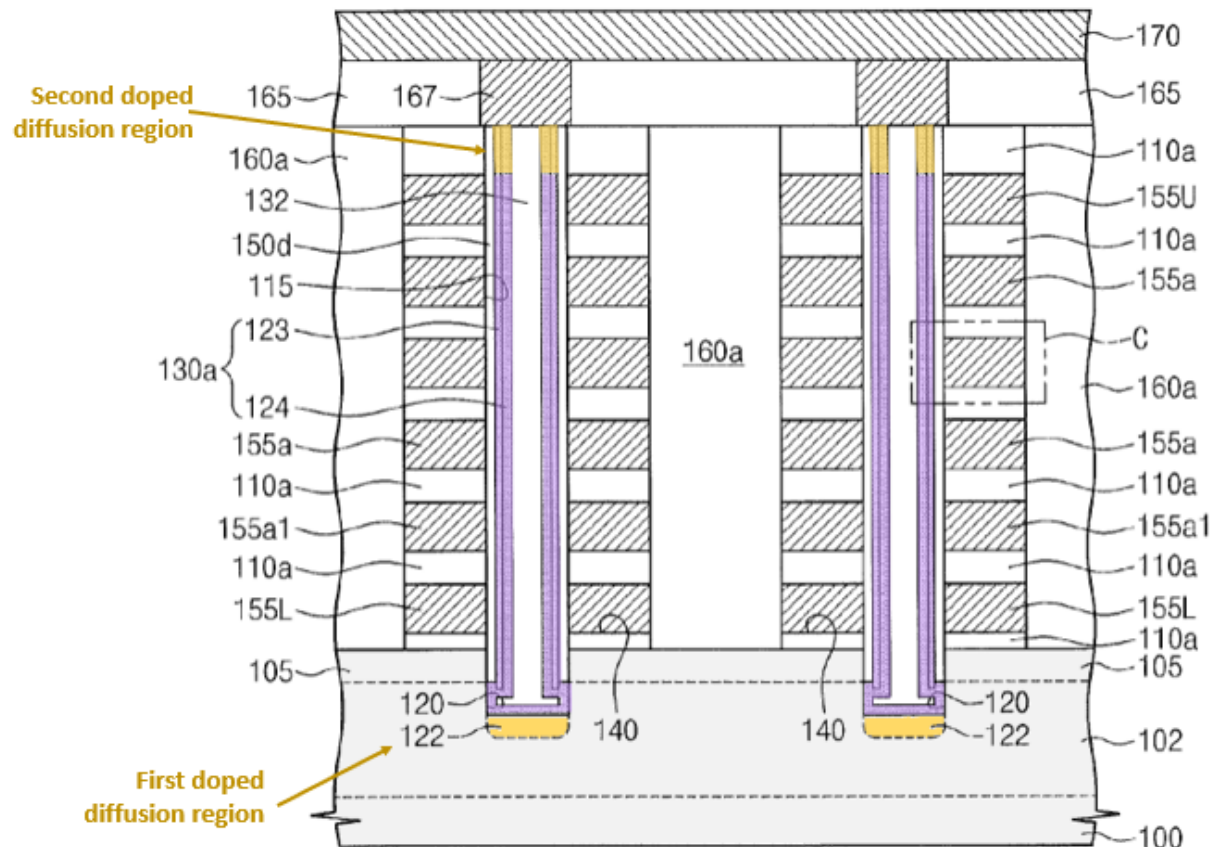




Ex. 1054 (Infringement Contentions), 000011 (annotated); Ex. 1003, ¶212.

- 5. The memory device of claim 1, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure.**

Lee '255 teaches the additional limitations of claim 5 because it teaches that vertical active pattern 130/130a (the *channel*) is *vertical and oriented substantially perpendicular to a semiconductor material structure* because it extends vertically from and perpendicular to the plane of substrate 100 (the *semiconductor material structure*, see Ex. 1003, ¶¶218), as shown in annotated Fig. 4A below.



Ex. 1004 (Lee '255), Fig. 4A; *see also id.*, [0052]; Ex. 1003, ¶218.

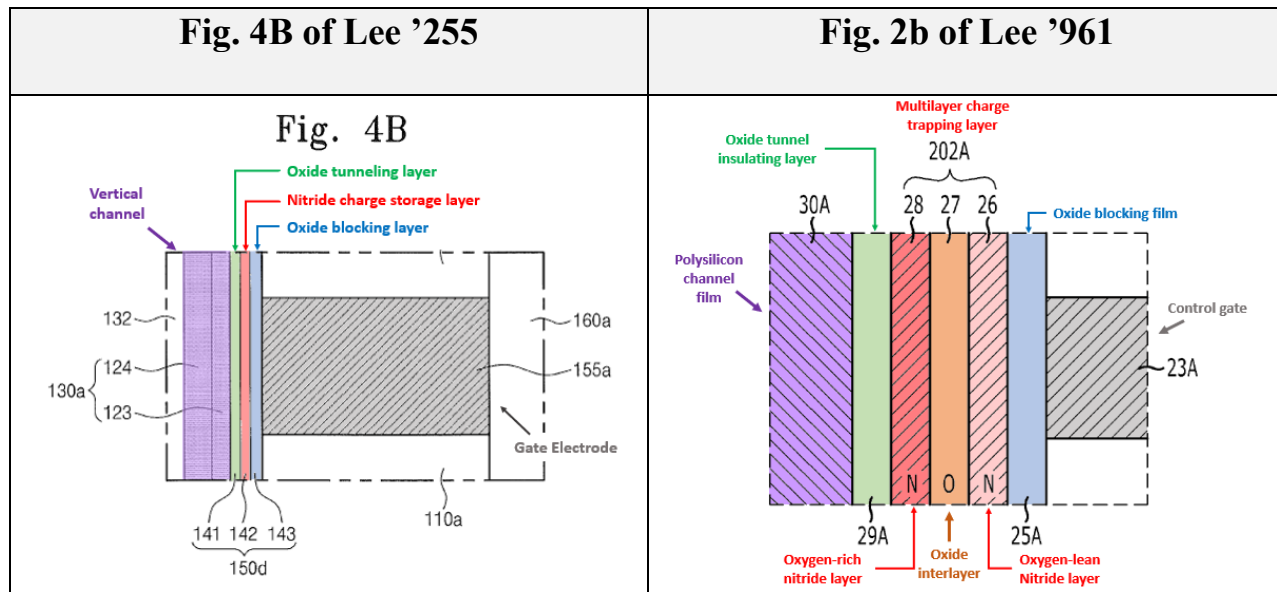
**[6pre]. The memory device of claim 1,**

The combination of Lee '255, Lee '961, and Fujiwara teaches limitation [6pre] for at least the reasons discussed for claim 1, above.

**[6a] wherein the first dielectric layer is disposed abutting the tunnel dielectric layer and substantially trap free, and**

The combination of Lee '255, Lee '961, and Fujiwara teaches limitation [6a] because, as set forth in limitations [1c]-[1g], the combined teachings of these references will result in the memory device of Lee '255 modified to have a multi-layer charge trapping region as taught in Lee '961, where the nitride charge

trapping layers have the optimal oxygen concentrations taught in Fujiwara. The ONONO structure of the resulting combination would resemble figure 2b of Lee '961, but with Lee '255's channel (vertical active pattern 130/130), tunnel dielectric layer (tunnel dielectric layer 141), and gate structure (gate layer 155a):



Ex. 1005 (Lee '961), Fig. 2b, [0020]; Ex. 1003, ¶221.

As reflected above, the combination of Lee '255, Lee '961, and Fujiwara teaches a *first dielectric layer* (nitride trap layer 28) adjacent to (*disposed abutting*) a *tunnel dielectric layer* (oxide tunneling layer 141). Ex. 1003, ¶222; *see also* Limitations [1c], [1d], [1f], above.

Further, in the foregoing combination of Lee '255, Lee '961, and Fujiwara, Fujiwara also teaches that the *first dielectric layer* (nitride trap layer 28) is *substantially trap free* because it specifically teaches that its lower (oxygen-rich) nitride layer (12B1) is “low in the charge trap and high in the data retention

characteristic.” Ex. 1006 (Fujiwara), [0205], [0201], [0210]; Ex. 1003, ¶223. Fujiwara further teaches that the “main structure of the charge storage layer” is provided by the upper nitride film 12B2, which a POSITA would have understood to mean that film 12B1 has lesser trapping functionality. Ex. 1006 (Fujiwara), [0215], [0199]. Fujiwara teachings that the oxygen-rich nitride layer is substantially trap-free mirror those of the ’240 patent. *See* Ex. 1001, 6:4-10, 8:26-26; Ex. 1003, ¶223.

|             |                                                                                                |
|-------------|------------------------------------------------------------------------------------------------|
| <b>[6b]</b> | <b>wherein the second dielectric layer is disposed abutting the blocking dielectric layer.</b> |
|-------------|------------------------------------------------------------------------------------------------|

The combination of Lee ’255, Lee ’961, and Fujiwara teaches limitation [6b] because, as reflected in the configuration shown in limitation [6a], the combination of Lee ’255, Lee ’961, and Fujiwara teaches *the second dielectric layer* (nitride trap layer 26) is adjacent (*disposed abutting*) blocking dielectric layer 143 (*a blocking dielectric layer*). Ex. 1003, ¶224.

|           |                                                                                                                           |
|-----------|---------------------------------------------------------------------------------------------------------------------------|
| <b>7.</b> | <b>The memory device of claim 1, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO).</b> |
|-----------|---------------------------------------------------------------------------------------------------------------------------|

Lee ’255 teaches the additional limitation of claim 7 because Lee ’255 teaches that blocking dielectric layer 143 (see limitation [1e]) may be a “high-k dielectric layer” that is comprised of “aluminum-oxide.” Ex. 1004 (Lee ’255), [0057]; Ex. 1003, ¶227. Patent Owner has asserted in parallel district court

litigation that aluminum oxide is a *high K high temperature oxide*. Ex. 1054 (Infringement Contentions), 000022; Ex. 1003, ¶¶225-226.

- 9. The memory device of claim 1, wherein the gate structure includes a high work function gate electrode.**
- 11. The memory device of claim 9, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.**

Lee '255 teaches the additional limitations of claims 9 and 11 because it teaches gates 155a “include a conductive material” such as doped silicon, tantalum, or tantalum nitride. Ex. 1004 (Lee '255), [0062]. In the context of the SONONOS configuration, a POSITA would have understood that doped silicon and tantalum nitride are *high work function* materials and that the doped silicon would be *P+ doped polysilicon*. See, e.g., *supra* § IV.B; Ex. 1001 (the '240 patent), 7:27-38; Ex. 1012 (Heo), [0046]; Ex. 1017 (Lai '676), [0067], [0072]; Ex. 1041 (Zheng), 5:52-62, 6:32-59; Ex. 1003, ¶229.

To the extent Patent Owner argues that the gate materials taught in Lee '255 do not teach the limitations of claims 9 and/or 11, Lee '961 teaches “[t]he control gate electrode (23A) includes a polysilicon film, particularly **a doped polysilicon film doped with N-type impurities or P-type impurities.**” Ex. 1005 (Lee '961), [0018]. Ex. 1003, ¶230.

A POSITA would have been motivated to apply the high work function gate electrode of Lee '961 to the memory device of Lee '255, and expected success in

doing so, because the use of such material would have amounted to (i) combining prior art elements according to known methods to yield predictable results; and (ii) use of known techniques to improve a similar device in the same way. Ex. 1003, ¶231. As explained, the use of high work function gate electrodes in SONOS-type memory devices was well-established and the benefits of such a design choice were widely recognized. *See, e.g., supra* §IV.B; Ex. 1029 (Kim Article), 000005; Ex. 1030 (Jeon), Fig. 1, [0009]; Ex. 1016 (Lue '189), [0084], [0086]; Ex. 1012 (Heo), [0064]; Ex. 1031 (Shih), [0071]; Ex. 1041 (Zheng), 1:14-18; Ex. 1003, ¶231.

**B. Ground 2: Obviousness over Lee '255, Lee '961, Fujiwara, and Hwang**

A POSITA would have also found claims 12-18 of the '240 patent are rendered obvious based on the teachings of Lee '255, Lee '961, Fujiwara, and Hwang. Ex. 1003 ¶¶232-288.

As set forth in connection with claim 1, *supra*, the combination of Lee '255, Lee '961, and Fujiwara results in a vertically-oriented 3D memory device (as taught in Lee '255) with a multi-layer charge trapping region (as taught in Lee '961) and optimized oxygen concentrations in the nitride layers (as taught in Fujiwara). *See* Part VI.A.

Independent claims 12 and 16 of the '240 patent largely overlap with claim 1, but claims 12 and 16 additionally require *a metal oxide semiconductor (MOS) logic device*. *See* limitations [12j], [16j], below. A POSITA would have understood

that vertically-oriented 3D memory devices, such as taught in Lee '255, are routinely connected to MOS logic devices that control the operation of the memory devices. Ex. 1003, ¶234. Hwang teaches such a peripheral MOS logic device. *See* V.B, *supra*; Ex. 1048 (Hwang), Fig. 6, [0112], [0113], [0116], [0158]; Ex. 1003, ¶233-234.

As is set forth below, a POSITA would have been motivated to apply Hwang's teachings of a peripheral MOS logic device to the combination of Lee '255, Lee '961, and Fujiwara and would have expected success in doing so. Ex. 1003, ¶¶235, 252-256.

### 1. Independent Claim 12

|                |                                                                       |
|----------------|-----------------------------------------------------------------------|
| <b>[12pre]</b> | <b>A semiconductor device, comprising: a memory device including,</b> |
|----------------|-----------------------------------------------------------------------|

Lee '255 teaches *a semiconductor device comprising: a memory device* because Lee '255 teaches “a three-dimensional (3D) semiconductor memory device and a method of fabricating the same.” *See, e.g.*, Ex. 1004 (Lee '255), [0002]; *see also, e.g., id.*, Abstract, Figs. 1A-5B, [0074]; Ex. 1003, ¶237.

|              |                         |
|--------------|-------------------------|
| <b>[12a]</b> | <b>a gate structure</b> |
|--------------|-------------------------|

This limitation is the same as [1a], and is obvious for the same reasons. Ex. 1003, ¶238.

**[12b] including a first high work function gate electrode,**

This limitation is similar to claim 9, and is obvious for the same reasons. Ex. 1003, ¶239.

**[12c] a channel positioned between and electrically connecting a first diffusion region and a second diffusion region,**

This limitation is the same as limitation [1b], and is obvious for the same reasons. Ex. 1003, ¶240.

**[12d] wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and**

This limitation is identical to claim 5, and is obvious for the same reasons. Ex. 1003, ¶241.

**[12e] a tunnel dielectric layer,**

This limitation is the same as limitation [1c], and is obvious for the same reasons. Ex. 1003, ¶242.

**[12f] a multi-layer charge trapping layer, and**

This limitation is the same as limitation [1d], and is obvious for the same reasons. Ex. 1003, ¶243.

**[12g] a blocking dielectric layer disposed between the gate structure and the channel,**

This limitation is the same as limitation [1e], and is obvious for the same reasons. Ex. 1003, ¶244.

**[12h] wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,**

This limitation is obvious for the same reasons set forth in limitation [1f]. Ex. 1003, ¶245.

**[12i] wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride; and**

This limitation is the same as limitation [1g], and is obvious for the same reasons. Ex. 1003, ¶246.

**[12j] a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.**

Lee '255, in combination with Hwang, teaches limitation [12j]. As a threshold matter, a POSITA would have understood that the memory transistors of Lee '255 were designed to work in conjunction with a peripheral MOS logic device because MOS logic transistors were conventional and necessary in any NAND flash architecture to provide electrical connections and system control. Ex. 1003, ¶247, 254.

Fig. 6

Hwang teaches that its peripheral MOS logic transistor includes peripheral

-77-

may include an oxide layer, a nitride layer, an oxynitride layer, and/or a high-k dielectric layer.” Ex. 1048 (Hwang), [0113]. The foregoing teaches *a metal oxide semiconductor (MOS) logic device (MOS logic transistor) including a gate oxide layer* (peripheral gate dielectric layer 537 that can be made of oxide). Ex. 1003, ¶249; *see also* Ex. 1007 (Lukasiak), pp.000003-4, Fig. 4.

Hwang further teaches a *second high work function gate electrode disposed thereon* because Hwang teaches that “the peripheral gate 535 may include at least one of a doped semiconductor layer (e.g., a **doped silicon layer**), a conductive metal nitride layer (e.g., a titanium nitride layer or a **tantalum nitride layer**)” Ex. 1048 (Hwang), Fig. 6 (showing gate 535 disposed on gate dielectric layer 537), [0113]; Ex. 1003, ¶250.

In the context of the SONONOS configuration, a POSITA would have understood that doped silicon and tantalum nitride are *high work function* materials, or would have considered it obvious to utilize *high work function* materials for the gate electrodes (both for the memory and logic transistors), for at least the reasons set forth in claim 9, Ground 1. Ex. 1003, ¶251.

A POSITA would have been motivated to further modify the combination of Lee ’255, Lee ’961, and Fujiwara to apply the teachings of Hwang to optimize the electrical interconnections of the combined device. Ex. 1003, ¶252.

First, it would have been obvious for a POSITA to consult the teachings of Hwang in seeking to implement and improve the memory transistor configuration of Lee '255, Lee '961, and Fujiwara because Hwang is also directed improving the configuration of SONOS-type memory devices. Ex. 1048 (Hwang), [0007], [0047], [0112], [0158]; Ex. 1003, ¶¶253.

Further, a POSITA would have been motivated to apply Hwang's electrical connection and peripheral MOS transistor teachings to the Lee '255 / Lee '961 / Fujiwara combination in Ground 1 to provide an appropriate electrical connection and control system and obtain the benefit expressly taught in Hwang—simplified fabrication and improved reliability and integration. Ex. 1048 (Hwang), [0158]; Ex. 1003, ¶254. A POSITA would have recognized that, while not explicitly shown in Lee '255, peripheral MOS logic transistors such as those shown in Hwang are conventional and standard features to control Lee '255's memory cell transistors and allow the device to function and thus that incorporating Hwang's peripheral MOS logic transistor teachings in the Lee '255 / Lee '961 / Fujiwara combination would have been an obvious and routine design choice. *Id.* A POSITA would also have understood that this combination of Hwang with Lee '255, Lee '961, and Fujiwara amounts to applying the teachings of Hwang for their intended purpose to improve similar devices in the same way. *Id.*

The benefit of using the peripheral logic teachings of Hwang in a 3D memory device would have been predictable to a POSITA prior to July 2012. Ex. 1003, ¶255. Hwang teaches the same 3D arrangement of a vertical string of memory cell transistors individually defined by gate layers, and select gates arranged in the lowermost and uppermost gate patterns, that are utilized in the Lee '255 configuration. Ex. 1048 (Hwang), [0060]. Thus, a POSITA would have recognized the teachings as compatible. Moreover, the routine nature of these configurations are shown in many prior art references. Vertically-arranged memory cell strings were common. *See, e.g.*, Ex. 1034 (Lee '247), Fig. 1; Ex. 1035 (Lee '086), Fig. 1; Ex. 1036 (Kim '064), Fig. 1, Ex. 1032 (Yang '696), Fig. 1; Ex. 1033 (Jang), Fig. 1; Ex. 1026 (Tanaka), Fig. 4; and Ex. 1028 (Kim '759), Fig. 6. Ex. 1003, ¶255. Hwang's structural and electrical teachings also utilized common arrangements. *See, e.g.*, Ex. 1058 (Maejima) [0010], [0061], [0064]; Ex. 1026 (Tanaka), FIG. 7. Therefore, a POSITA would have understood that the structural and electrical features of Lee '255 and Hwang were common and interchangeable.

A POSITA also would have expected success in applying Hwang's electrical connection teachings to the 3D memory frameworks of Lee '255, Lee '961, and Fujiwara because they share underlying device architectures. Ex. 1003, ¶256. Integrating Hwang's connection strategy required no new materials, fabrication

steps, or circuit innovations, just the application of well-established 3D NAND connection techniques known by 2012. *Id.*

## 2. Dependent Claims 13-15

**[13pre]. The semiconductor device of claim 12,**

This limitation is obvious for the same reasons as limitation [6pre]. Ex. 1003, ¶257.

**[13a] wherein the first dielectric layer of the multi-layer charge trapping layer is disposed abutting the tunnel dielectric layer and substantially trap free, and**

This limitation is obvious for the same reasons as limitation [6a]. Ex. 1003, ¶258.

**[13b] wherein the second dielectric layer is disposed abutting the blocking dielectric layer.**

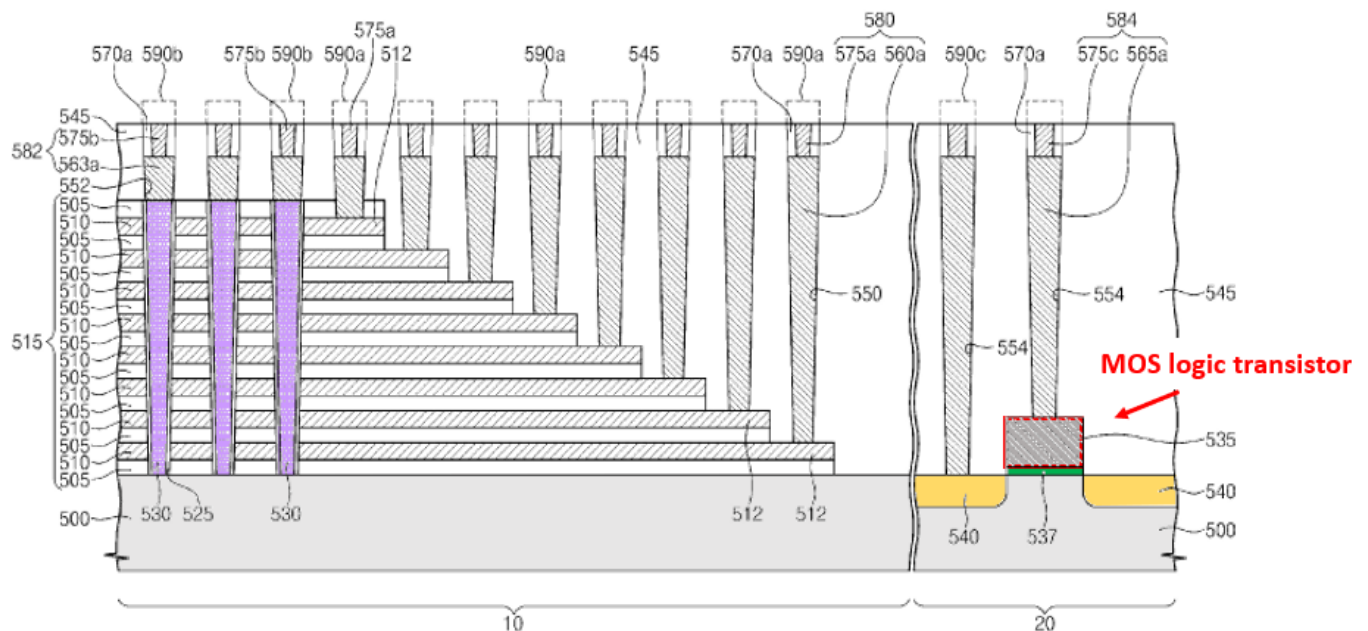
This limitation is obvious for the same reasons as limitation [6b]. Ex. 1003, ¶259.

**14. The semiconductor device of claim 12, wherein the MOS logic device is formed at least partially within a semiconductor material structure.**

Hwang teaches claim 14 because it teaches a MOS transistor made up of peripheral gate 535, peripheral gate dielectric layer 537, source/drain regions 540, and the channel between source/drain regions 240 (*the MOS logic device as set forth in claim 12*) arranged at least partially within (e.g., at least source/drain

regions 540 and the channel therebetween are below the top surface of) substrate 500 (*the semiconductor material structure*). This arrangement is shown in annotated figure 6, below:

Fig. 6



Ex. 1048 (Hwang), Fig. 6,  $[0113]$ ; Ex. 1003, ¶261.

A POSITA would have understood that the positioning of the *MOS logic device* of Hwang vis-à-vis its substrate 500 mirrors the positioning of MOS logic transistor 302 and substrate 306 in Fig. 3 of the '240 patent (as shown in Fig. 3 below). Ex. 1003, ¶262. A POSITA would have been motivated to consult Hwang because, like Lee '255 and Lee '961, it addresses 3D NAND SONOS-type

architectures and its integration of select MOS devices with the substrate aligns with conventional NAND design practices.

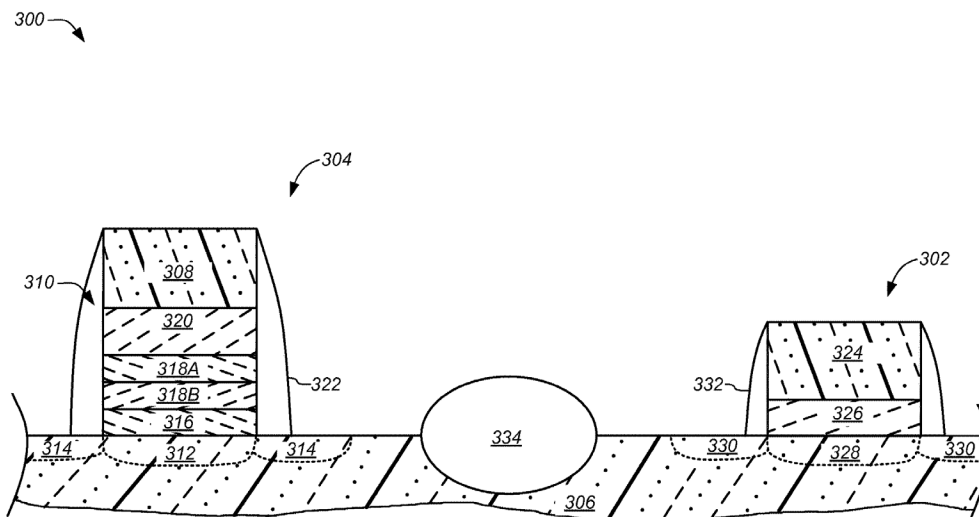


FIG. 3

Ex. 1001 ('240 patent), Fig. 3, 8:10-40.

**15. The semiconductor device of claim 14, wherein the channel is vertical and oriented substantially orthogonal to the semiconductor material structure.**

This claim is almost identical to limitation [12d], differing only in that claim 15 recites the channel is “oriented substantially **orthogonal** to the semiconductor material structure” instead of limitation [12d]’s “oriented substantially **perpendicular** to a semiconductor material structure.” But a POSITA would have understood “orthogonal” and “perpendicular” to have similar meanings, and thus would have considered claim 15 obvious for the same reasons as limitation [12d]. *See, e.g.*, Ex. 1049 (American Heritage Excerpts) (defining “orthogonal” as

“[r]elating to or composed of right angles” and “perpendicular” as “[b]eing at right angles to the horizontal; vertical”); Ex. 1055 (Merriam-Webster Excerpts); Ex. 1056 (New Oxford Excerpts); Ex. 1003, ¶264.

### 3. Independent Claim 16

|                |                                                                       |
|----------------|-----------------------------------------------------------------------|
| <b>[16pre]</b> | <b>A semiconductor device, comprising: a memory device including,</b> |
|----------------|-----------------------------------------------------------------------|

This limitation is the same as limitation [12pre], and is obvious for the same reasons. Ex. 1003, ¶265.

|              |                         |
|--------------|-------------------------|
| <b>[16a]</b> | <b>a gate structure</b> |
|--------------|-------------------------|

This limitation is the same as limitation [12a], and is obvious for the same reasons. Ex. 1003, ¶266.

|              |                                                             |
|--------------|-------------------------------------------------------------|
| <b>[16b]</b> | <b>including a first high work function gate electrode,</b> |
|--------------|-------------------------------------------------------------|

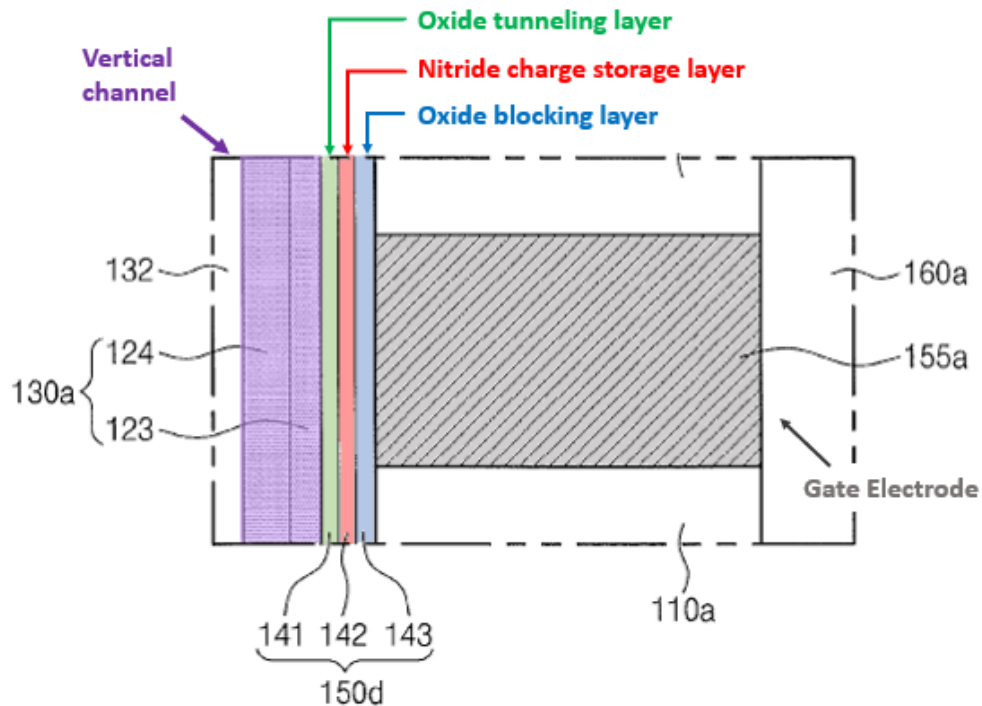
This limitation is the same as limitation [12b], and is obvious for the same reasons. Ex. 1003, ¶267.

|              |                                                                          |
|--------------|--------------------------------------------------------------------------|
| <b>[16c]</b> | <b>a blocking dielectric layer disposed abutting the gate structure,</b> |
|--------------|--------------------------------------------------------------------------|

This limitation is similar to limitation [1e], but recites the blocking layer is “disposed abutting the gate structure” rather than [1e]’s recitation that it is “disposed between the gate structure and the channel.” Limitation [16c] is obvious for the same reasons as [1e] and because Lee ’255 teaches that the blocking

dielectric layer 143 (*blocking dielectric layer*), is positioned adjacent (*disposed abutting*) gate electrode 155a (*gate structure*).

Fig. 4B



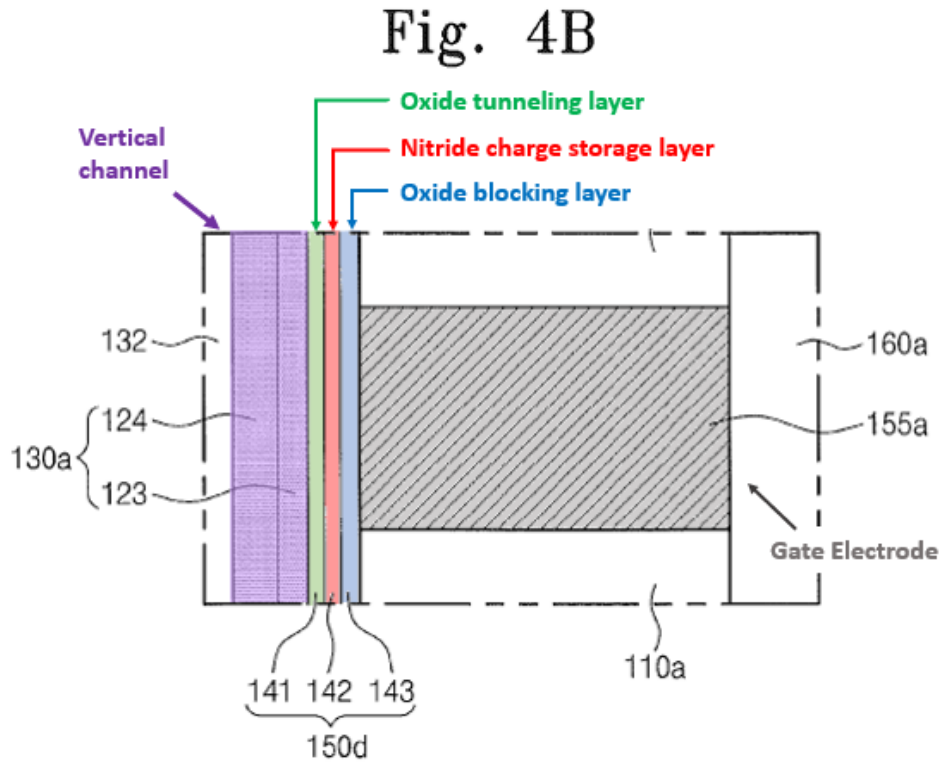
Ex. 1004 (Lee '255), Fig. 4B; Ex. 1003, ¶268.

As set forth in [1e], Lee '961 teaches the same arrangement, reinforcing the teachings of Lee '255 in the combination. Ex. 1003, ¶269.

**[16d] a multi-layer charge trapping layer disposed abutting the blocking dielectric layer,**

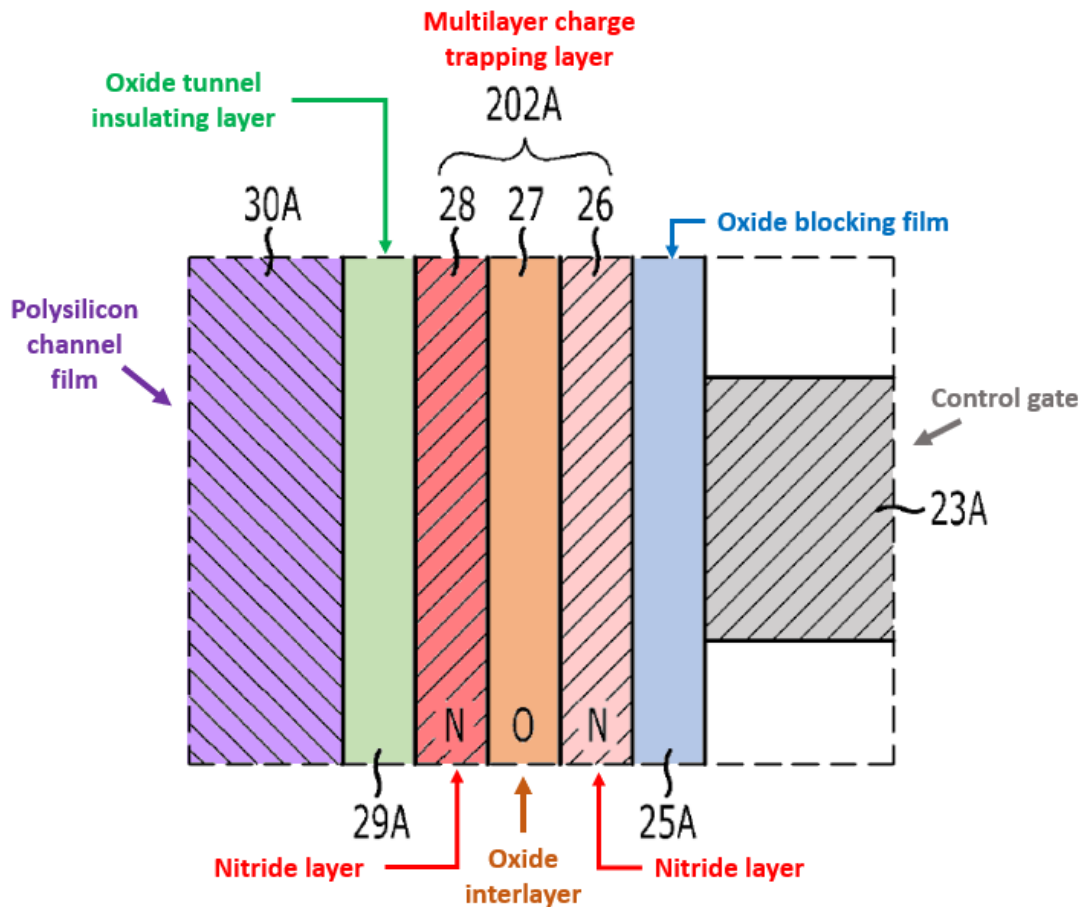
This limitation recites “a multi-layer charge trapping layer” like limitation [1d], but additionally recites that it is “disposed abutting the blocking dielectric layer.” Limitation [16d] is obvious for the same reasons as [1d]. Ex. 1003, ¶270.

First, Lee '255 teaches, as shown in annotated figure 4B below, that its charge storage layer 142 (*charge trapping layer*) is positioned adjacent (*disposed abutting*) blocking dielectric layer 143 (*blocking dielectric layer*).



Ex. 1004 (Lee '255), Fig. 4B; Ex. 1003, ¶271.

Second, Lee '961 teaches, as shown in annotated figure 2b below, that its multilayered charge trap layer 202A (*a multi-layer charge trapping layer*) is adjacent (*disposed abutting*) blocking dielectric layer 25A (*blocking dielectric layer*):



Ex. 1005 (Lee '961), Fig. 2b; Ex. 1003, ¶272.

As explained in connection with limitation [1d], a POSITA would have been motivated to model a multilayer charge storage region in Lee '255 on region 202A of Lee '961. A POSITA would have understood that the position of the modified charge trapping region in Lee '255 would remain unchanged—i.e., it would be formed adjacent blocking dielectric layer (blue), as is shown in figure 2b of Lee '961. Ex. 1003, ¶273.

|              |                                                                                                                                      |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <b>[16e]</b> | <b>wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,</b> |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------|

This limitation is obvious for the same reasons as limitation [1f]. Ex. 1003, ¶274.

|              |                                                                                                                                      |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <b>[16f]</b> | <b>wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride,</b> |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------|

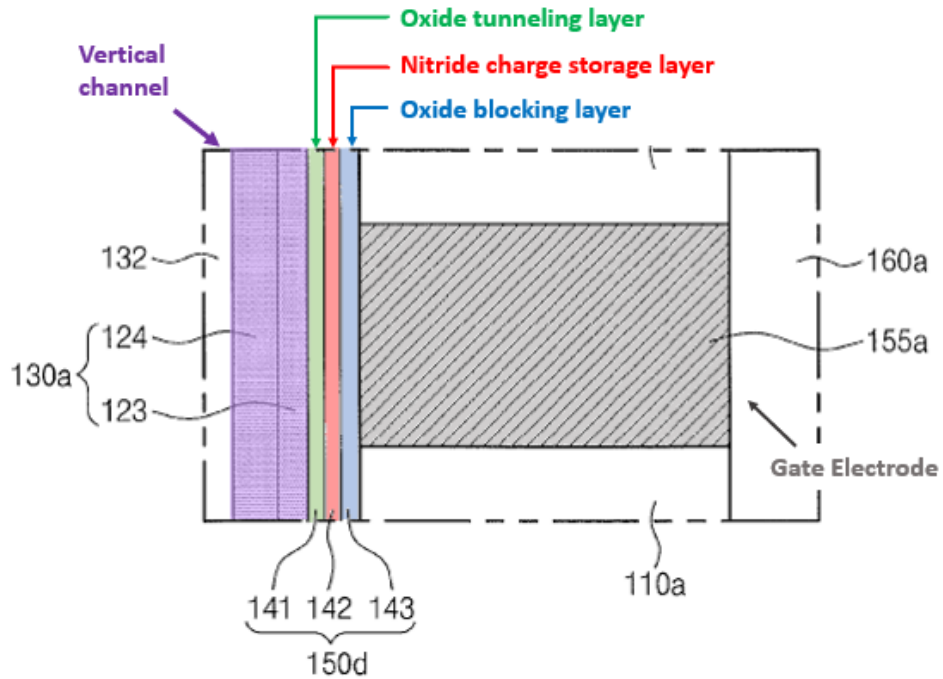
This limitation is obvious for the same reasons as limitation [1g]. Ex. 1003, ¶275.

|              |                                                                                               |
|--------------|-----------------------------------------------------------------------------------------------|
| <b>[16g]</b> | <b>a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer, and</b> |
|--------------|-----------------------------------------------------------------------------------------------|

This limitation is similar to [1c] but additionally recites that the tunnel dielectric layer is “disposed abutting the multi-layer charge trapping layer.” Limitation [16g] is obvious for the same reasons as [1c]. Ex. 1003, ¶276.

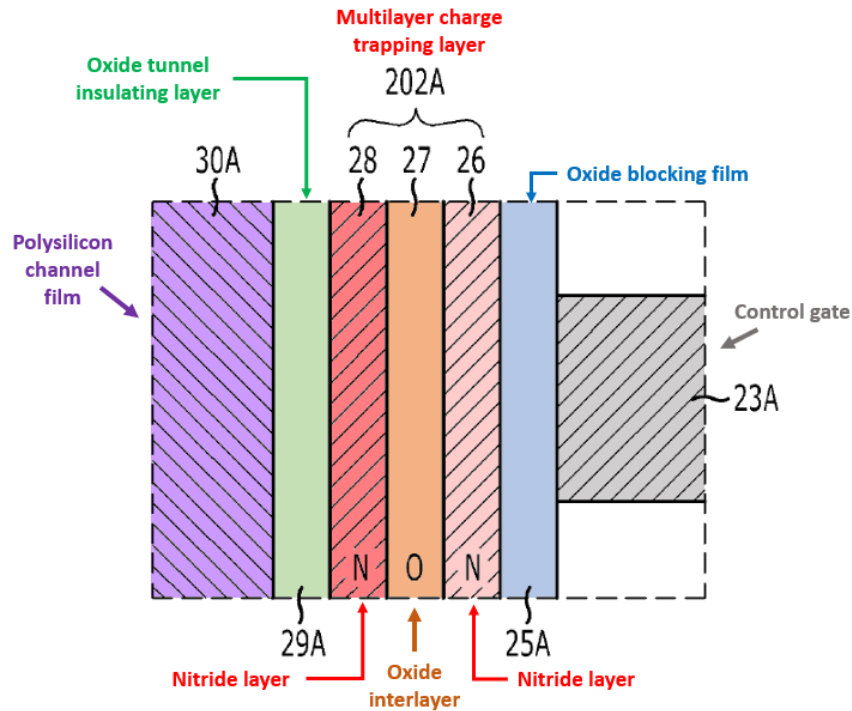
First, Lee ’255 teaches, as shown in figure 4B below, that its tunnel dielectric layer 141 (*tunnel dielectric layer*) is adjacent (*disposed abutting*) charge storage layer 142 (*charge trapping layer*).

Fig. 4B



Ex. 1004 (Lee '255), Fig. 4B. Ex. 1003, ¶277.

Second, Lee '961 teaches, as shown in figure 2b below, that its tunnel insulating layer 29A (*a tunnel dielectric layer*) is adjacent (*disposed abutting*) multilayered charge trap layer 202A (*a multi-layer charge trapping layer*).



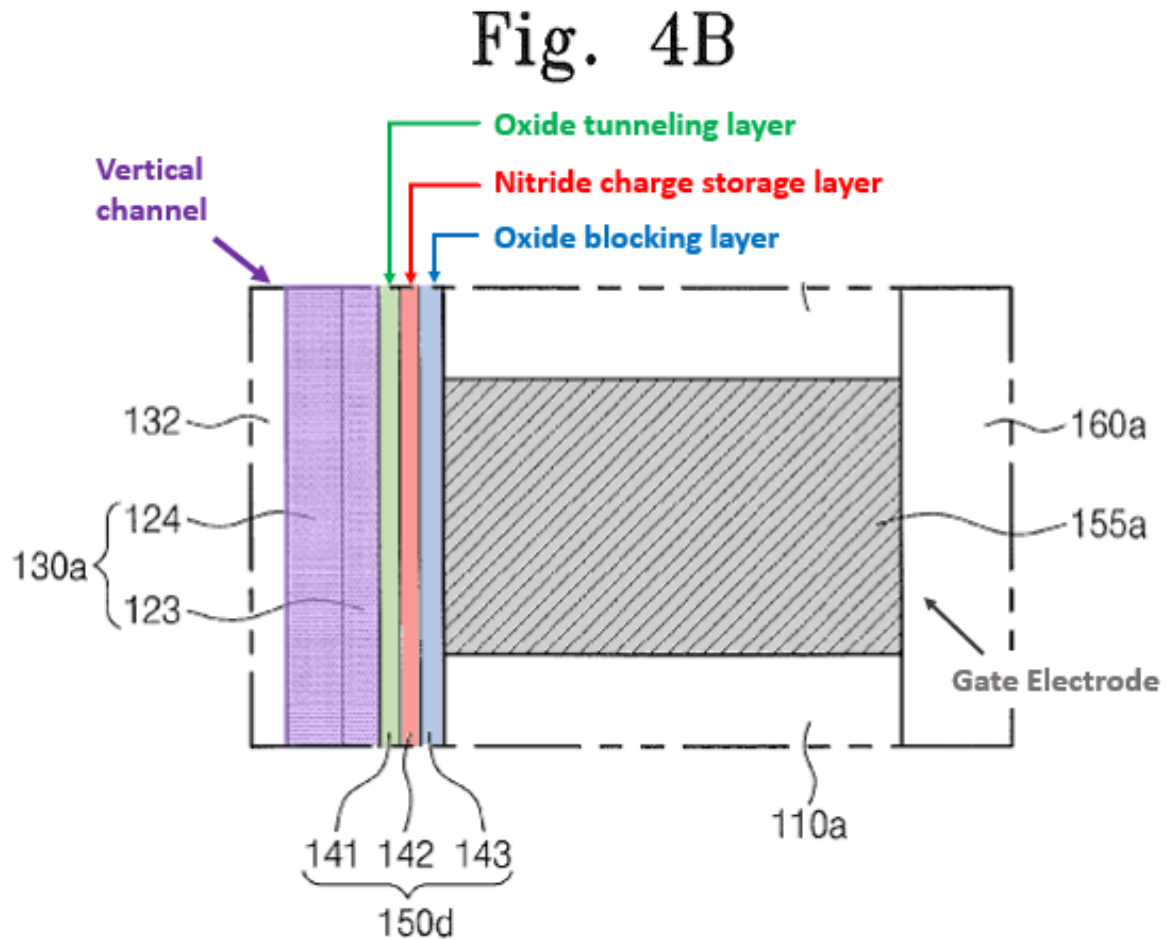
Ex. 1005 (Lee '961), Fig. 2b; Ex. 1003, ¶278.

As explained in connection with limitations [1d] and [1f], a POSITA would have been motivated to model a multilayer charge storage region in Lee '255 on region 202A of Lee '961 and the position of the modified charge trapping region in Lee '255 would have remained the same: adjacent tunnel dielectric layer (green), as is shown in figure 2b of Lee '961. Ex. 1003, ¶279.

**[16h] a channel disposed abutting the tunnel dielectric layer, wherein the channel is positioned between and electrically connecting a first diffusion region and a second diffusion region,**

This limitation is similar to limitation [1b], but additionally recites that the channel is “disposed abutting the tunnel dielectric layer.” Limitation [16h] is obvious for the same reasons as [1b] and because Lee '255 teaches that the *channel*

(vertical active pattern 130/130a) is adjacent (*disposed abutting*) the tunnel dielectric layer 141 (*tunnel dielectric layer*):



Ex. 1004 (Lee '255), Fig. 4B; Ex. 1003, ¶¶280-281.

**[16i] wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and**

This limitation is the same as claim 5, and is obvious for the same reasons.

Ex. 1003, ¶282.

|              |                                                                                                                                                     |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>[16j]</b> | <b>a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.</b> |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|

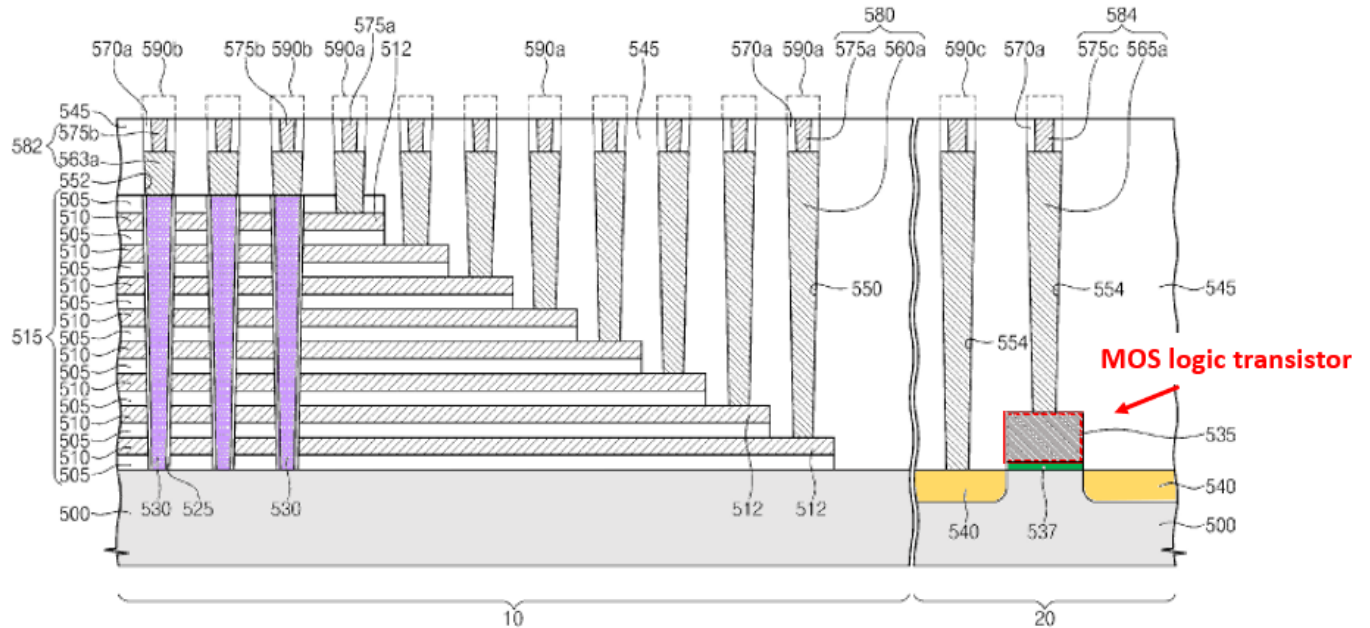
This limitation is the same as limitation [12j], and is obvious for the same reasons. Ex. 1003, ¶283.

#### **4. Dependent Claims 17, 18**

|            |                                                                                                                                                 |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>17.</b> | <b>The semiconductor device of claim 16, wherein the MOS logic device is formed at least partially on the semiconductor material structure.</b> |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------|

Hwang teaches claim 17 because it teaches a MOS transistor made up of peripheral gate 535, peripheral gate dielectric layer 537, source/drain regions 540, and the channel between source/drain regions 240 (*the MOS logic device* as set forth in claim 12) arranged at least partially on (e.g., peripheral gate 535 and peripheral gate dielectric layer 537 are above the top surface of) substrate 500 (*the semiconductor material structure*). Ex. 1003, ¶285. This arrangement is shown in annotated Fig. 6, below:

Fig. 6



Ex. 1048 (Hwang), Fig. 6, [0113]; Ex. 1003, ¶285.

A POSITA would have understood that the positioning of the *MOS logic device* of Hwang vis-à-vis its substrate 500 mirrors the positioning of MOS logic transistor 302 and substrate 306 in Fig. 3 of the '240 patent (as shown in Fig. 3 below). Ex. 1003, ¶286. A POSITA would have been motivated to consult Hwang because, like Lee '255 and Lee '961, it addresses 3D NAND SONOS-type architectures and its integration of select MOS devices with the substrate aligns with conventional NAND design practices.

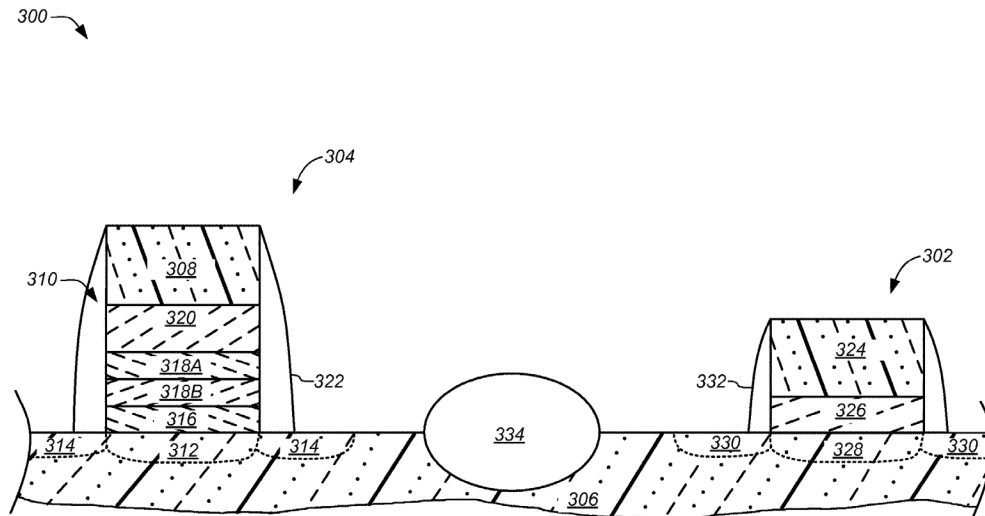


FIG. 3

Ex. 1001 ('240 patent), Fig. 3, 8:10-40.

- |                   |                                                                                                                                                                                                                                                                    |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p><b>18.</b></p> | <p><b>The semiconductor device of claim 16, wherein the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first and second dielectric layers, and wherein the anti-tunneling layer includes an oxide layer.</b></p> |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

This limitation is the same as limitation [1i], and is obvious for the same reasons. Ex. 1003, ¶287-288.

## VII. CONCLUSION

For the foregoing reasons, Petitioner requests *inter partes* review and that the claims 1, 3-7, 9, and 11-18 of the '240 patent be canceled as unpatentable.

## VIII. STANDING

Petitioner certifies that Petitioner is not barred or estopped from requesting this *inter partes* review and the '240 patent is eligible for it.

## IX. MANDATORY NOTICES AND FEES

**Real Party In Interest:** The real parties-in-interests here are Sandisk Technologies, Inc. and SanDisk Corporation. No other parties directed, controlled, or funded this Inter Partes Review proceeding (IPR).

**Related Matters:** The '240 patent is the subject of the following civil actions and administrative proceedings:

- *Sandisk Corp. v. IPValue Management, Inc., et al.*, 5:25-cv-02389 (N.D. Cal.).
- *IPValue Management, Inc., et al. v. Western Digital Corp., et al.*, 8:25-cv-00119 (C.D. Cal.).
- *Sandisk Technologies, Inc. v. Longitude Memory Flash Solutions Ltd.*, IPR2025-01281

**Lead and Backup Counsel:** Pursuant to 37 C.F.R. § 42.8(b)(3) and 42.10(a), Petitioner designates Harper Batts (Reg. No. 56,160) as lead counsel and Jeffrey Liang (Reg. No. 69,043), Chris Ponder (Reg. No. 77,167) and Jonathan DeFosse (provisionally recognized PTAB attorney, *pro hac vice* requested) as back-up counsel, each of Sheppard, Mullin, Richter & Hampton LLP.

**Service Information:** Petitioner consents to service by electronic mail addressed to:

hbatts@sheppardmullin.com,  
cponder@sheppardmullin.com,  
jliang@sheppardmullin.com,  
jdefosse@sheppardmullin.com, and  
LegalTM-Sandisk-LFMS-IPRs@sheppardmullin.com

Petitioner's counsel may also be served by mail or hand delivery at Sheppard, Mullin, Richter & Hampton LLP, 1540 El Camino Real, Suite 120, Menlo Park, CA 94025. Petitioner's counsel may be reached by telephone at (650) 815-2673 and by facsimile at (650) 815-4668.

**Fees:** The Office is authorized to charge fees for this Petition to Deposit Account 50-4561, Ref. 104X-409022.

Respectfully submitted,

SHEPPARD, MULLIN,  
RICHTER & HAMPTON LLP

/Harper Batts/  
Harper Batts (Reg. No. 56,160)

## **CLAIM APPENDIX**

| <b>Claim 1</b> |                                                                                                                                                                                                                  |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1pre]         | A memory device, comprising:                                                                                                                                                                                     |
| [1a]           | a gate structure;                                                                                                                                                                                                |
| [1b]           | a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and                                                                                             |
| [1c]           | a tunnel dielectric layer;                                                                                                                                                                                       |
| [1d]           | a multi-layer charge trapping layer, and                                                                                                                                                                         |
| [1e]           | a blocking dielectric layer disposed between the gate structure and the channel                                                                                                                                  |
| [1f]           | wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers |
| [1g]           | wherein the anti-tunneling layer includes an oxide layer, and wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.                      |
| <b>Claim 3</b> |                                                                                                                                                                                                                  |
| 3              | The memory device of claim 1, wherein the channel, first and second diffusion regions are disposed above a semiconductor material structure.                                                                     |
| <b>Claim 4</b> |                                                                                                                                                                                                                  |
| 4              | The memory device of claim 1, wherein the channel, first and second diffusion regions are suspended above a semiconductor material structure.                                                                    |
| <b>Claim 5</b> |                                                                                                                                                                                                                  |
| 5              | The memory device of claim 1, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material                                                                               |

|                 |                                                                                                                                 |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------|
|                 | structure.                                                                                                                      |
| <b>Claim 6</b>  |                                                                                                                                 |
| [6pre]          | The memory device of claim 1,                                                                                                   |
| [6a]            | wherein the first dielectric layer is disposed abutting the tunnel dielectric layer and substantially trap free, and            |
| [6b]            | wherein the second dielectric layer is disposed abutting the blocking dielectric layer.                                         |
| <b>Claim 7</b>  |                                                                                                                                 |
| 7               | The memory device of claim 1, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO).              |
| <b>Claim 9</b>  |                                                                                                                                 |
| 9               | The memory device of claim 1, wherein the gate structure includes a high work function gate electrode.                          |
| <b>Claim 11</b> |                                                                                                                                 |
| 11              | The memory device of claim 9, wherein the high work function gate electrode comprises a P <sup>+</sup> doped polysilicon layer. |
| <b>Claim 12</b> |                                                                                                                                 |
| [12pre]         | A semiconductor device, comprising: a memory device including,                                                                  |
| [12a]           | a gate structure                                                                                                                |
| [12b]           | including a first high work function gate electrode,                                                                            |
| [12c]           | a channel positioned between and electrically connecting a first diffusion region and a second diffusion region,                |
| [12d]           | wherein the channel is vertical and oriented substantially perpendicular                                                        |

|                 |                                                                                                                                                               |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                 | to a semiconductor material structure, and                                                                                                                    |
| [12e]           | a tunnel dielectric layer,                                                                                                                                    |
| [12f]           | a multi-layer charge trapping layer, and                                                                                                                      |
| [12g]           | a blocking dielectric layer disposed between the gate structure and the channel,                                                                              |
| [12h]           | wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,                                 |
| [12i]           | wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride; and                             |
| [12j]           | a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.                  |
| <b>Claim 13</b> |                                                                                                                                                               |
| [13pre]         | The semiconductor device of claim 12,                                                                                                                         |
| [13a]           | wherein the first dielectric layer of the multi-layer charge trapping layer is disposed abutting the tunnel dielectric layer and substantially trap free, and |
| [13b]           | wherein the second dielectric layer is disposed abutting the blocking dielectric layer.                                                                       |
| <b>Claim 14</b> |                                                                                                                                                               |
| 14              | The semiconductor device of claim 12, wherein the MOS logic device is formed at least partially within a semiconductor material structure.                    |
| <b>Claim 15</b> |                                                                                                                                                               |
| 15              | The semiconductor device of claim 14, wherein the channel is vertical and oriented substantially orthogonal to the semiconductor material structure.          |

|                 |                                                                                                                                                                                        |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                 |                                                                                                                                                                                        |
| <b>Claim 16</b> |                                                                                                                                                                                        |
| [16pre]         | A semiconductor device, comprising: a memory device including,                                                                                                                         |
| [16a]           | a gate structure                                                                                                                                                                       |
| [16b]           | including a first high work function gate electrode,                                                                                                                                   |
| [16c]           | a blocking dielectric layer disposed abutting the gate structure,                                                                                                                      |
| [16d]           | a multi-layer charge trapping layer disposed abutting the blocking dielectric layer,                                                                                                   |
| [16e]           | wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,                                                          |
| [16f]           | wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride,                                                          |
| [16g]           | a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer, and                                                                                                 |
| [16h]           | a channel disposed abutting the tunnel dielectric layer, wherein the channel is positioned between and electrically connecting a first diffusion region and a second diffusion region, |
| [16i]           | wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and                                                                    |
| [16j]           | a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.                                           |
| <b>Claim 17</b> |                                                                                                                                                                                        |
| 17              | The semiconductor device of claim 16, wherein the MOS logic device is formed at least partially on the semiconductor material structure.                                               |

**Claim 18**

|    |                                                                                                                                                                                                                                                      |
|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18 | The semiconductor device of claim 16, wherein the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first and second dielectric layers, and wherein the anti-tunneling layer includes an oxide layer. |
|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## **CERTIFICATE OF SERVICE**

The undersigned hereby certifies that on October 14, 2025, true and correct copies of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,929,240 and Exhibits 1001-1060 were served in its entirety on the Patent Owner at the following address of record as listed on Patent Center via Priority Mail Express® or Express Mail:

Cypress Semiconductor Corporation  
198 Champion Court  
San Jose, CA 95134

*Correspondence Address*

Longitude Flash Memory Solutions Ltd.  
Plaza 255 Suite 2A  
Blanchardstown Corporate Park 2  
Blanchardstown  
Dublin 15, D15 YH6H

*Patent Owner's Address*

The undersigned certifies that true and correct copies of the Petition for *Inter Partes* Review of U.S. Patent No. 9,929,240 and Exhibits 1001-1060 were also sent via electronic mail to the attorneys of record for Plaintiff in the concurrent litigation matters:

***Counsel for Patent Owner***  
***Longitude Flash Memory***  
***Solutions, Ltd.***  
**Russ August & Kabat**  
Neil A. Rubin  
nrubin@raklaw.com

James A. Milkey  
jmilkey@raklaw.com  
Philip X. Wang  
pwang@raklaw.com  
ipvalue@raklaw.com

SHEPPARD, MULLIN,  
RICHTER & HAMPTON LLP

/Harper Batts/  
Harper Batts (Reg. No. 56,160)  
Attorney for Petitioner

Date: October 14, 2025

1540 El Camino Real, Suite 120  
Menlo Park, CA 94025  
Tel: (650) 815-2673

**CERTIFICATE OF COMPLIANCE WITH  
TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS,  
AND TYPE STYLE REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 12,106 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 365 in 14-point Times New Roman.

Respectfully submitted,

SHEPPARD, MULLIN,  
RICHTER & HAMPTON LLP

/Harper Batts/  
Harper Batts (Reg. No. 56,160)  
Attorney for Petitioner

Date: October 14, 2025

1540 El Camino Real, Suite 120  
Menlo Park, CA 94025  
Tel: (650) 815-2673