IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

Sandisk Technologies, Inc.,
Petitioner,

v.

Longitude Flash Memory Solutions Ltd.,
Patent Owner.

_____

Case No. IPR2025-01283

U.S. Patent No. 9,929,240

_____

DECLARATION OF JACK C. LEE IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,929,240

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I, Jack C. Lee, declare as follows:

1. I have been retained as an independent expert on behalf of Sandisk Technologies, Inc. in connection with the above-captioned Petition for *Inter Partes* Review. In this declaration, I give my opinions as to whether certain claims of U.S. Patent No. 9,929,240 (the '240 patent) are unpatentable. I provide technical bases for these opinions as appropriate.

2. This declaration contains statements of my opinions formed to date and the bases and reasons for those opinions. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

I. BACKGROUND AND QUALIFICATIONS

A. Summary of Relevant Experience and Qualifications

3. My curriculum vitae ("CV") is attached hereto as Appendix 1 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

4. I am an expert in the field of semiconductor process technology and semiconductor design with more than 40 years' experience as a researcher, educator, and consultant. The opinions below draw on my education, training, and experience.

5. I earned a B.S. with highest honors (1980) and M.S. (1981) in Electrical Engineering, from the University of California, Los Angeles, and a Ph.D. in Electrical Engineering (1988) from the University of California, Berkeley.

6. From 1979 to 1984, I served as a Member of Technical Staff at the TRW Microelectronics Center, where I worked on high-speed bipolar device/circuit design, fabrication, and testing and was promoted to Engineering Group Leader in 1983.

7. While at UC Berkeley I received several academic honors, including the 1988 IEEE International Reliability Physics Symposium Best Paper Award and a competitive lectureship with a dedicated teaching assistantship.

8. After completing my doctorate, I joined the faculty at the University of Texas at Austin in August 1988. I have taught undergraduate and graduate courses in semiconductor device fabrication and design, supervised more than forty Ph.D. students, and since 2000 I have held the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering. I became Professor Emeritus in September 2023.

9. My current research and teaching interests include advanced MOSFETs such as FinFETs, memory devices including non-volatile NAND structures, high-K gate dielectrics and high work function gate electrodes, ultra-thin dielectrics such as silicon nitride, tunneling and blocking oxides, reliability

physics, modeling, packaging, photovoltaic technologies, and alternative channel materials.

10. I have been invited to present tutorials, short courses, and plenary talks on various topics including high-K gate stacks in leading conferences such as the Symposium on VLSI Technology and the IEEE International Electron Devices Meeting (IEDM). My research group at UT Austin was among the first to develop hafnium-based high-K for nanoscale MOSFETs, and I have published extensively on HfO_2, HfSiON, hafnium silicate, interfacial engineering, and dielectric reliability.

11. My research has been supported by the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, and Texas Emerging Technology Funds, among others.

12. I have authored more than 600 journal and conference papers, co-authored eight books or book chapters, and am a named inventor on nine U.S. patents. My work has received multiple best-paper and inventor awards.

13. In 2002, I was elected an IEEE fellow for my "contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices," and I served as an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

14. I regularly consult for semiconductor companies and consortia, teach industrial short courses, and organize international conferences, including the International Symposium on VLSI Technologies and IEDM.

B. Compensation

15. For my efforts in connection with the preparation of this declaration, I have been compensated at my standard rate for this type of consulting activity. My compensation is in no way contingent on the results of these or any other proceeding relating to the above-captioned patent.

C. Materials and Other Information Considered

16. I have considered information from various sources in forming my opinions. I have reviewed and considered each of the exhibits listed in the attached Appendix 2 (Materials Considered) in forming my opinions, along with any other documents or information otherwise identified herein.

II. UNDERSTANDING OF THE LAW

17. I am not an attorney. In forming my opinions herein, I applied the relevant legal principles provided to me by counsel, summarized in Appendix 4.

III. BACKGROUND

A. Overview of the ’240 Patent

18. I understand that the ’240 patent was issued on March 27, 2018, from an application filed on October 26, 2016. *See* Ex. 1001 (’240 patent),000001. It is directed to alleged improvements in the design and fabrication of non-volatile

semiconductor memory devices. *See* Ex. 1001 ('240 patent), 1:26-29. While the '240 patent acknowledges that such devices were already "widely used" at the time of its filing (Ex. 1001 ('240 patent), 1:33-37), it asserts that existing designs had "poor or decreasing data retention over time, limiting the useful transistor lifetime" (Ex. 1001 ('240 patent), 1:65-2:7) and that processes for fabricating conventional memory transistors were "incompatible with those used for fabricating logic transistors" (*Id*., 2:17-24).

19. The '240 patent states that designing a memory transistor to include an "oxide-nitride-nitride-oxide (ONNO) stack" and a "high work function gate electrode" provides a solution to the problems with conventional memory transistors:

> Generally, the device includes a memory transistor comprising a polysilicon channel region electrically connecting a source region and a drain region formed in a substrate, an oxide-nitride-nitride-oxide (ONNO) stack disposed above the channel region, and a high work function gate electrode formed over a surface of the ONNO stack. In one embodiment, the ONNO stack includes a multi-layer charge-trapping region including an oxygen-rich first nitride layer and an oxygen-lean second nitride layer disposed above the first nitride layer. In another embodiment, the multi-layer charge trapping region further includes an oxide anti-tunneling layer

separating the first nitride layer from the second nitride layer.

Ex. 1001 ('240 patent), 2:35-50.

20. Figure 3 of the '240 patent depicts an embodiment of the alleged invention. *See* Ex. 1001 ('240 patent), 8:10-14. It shows a semiconductor device with a memory transistor (304) and a logic transistor (302). *Id*., 3:6-10. The memory transistor includes: a channel region (312) extending horizontally between source/drain diffusion regions (314); an ONNO stack (310) disposed above the channel region with (i) an oxide tunneling layer (316) (one of the "O" layers of the ONNO stack); (ii) a "multi-layer charge storage layer" (318A, 318B) (the two "N" layers of the ONNO stack); and (iii) a blocking oxide layer (320) (the other "O" layer of the ONNO stack); and a high work function gate electrode (308). *Id*., 8:14-31. The logic transistor (302) has an oxide layer (326) and a high work function gate electrode (324). *Id*., 8:32-40. I have annotated figure 3 here:

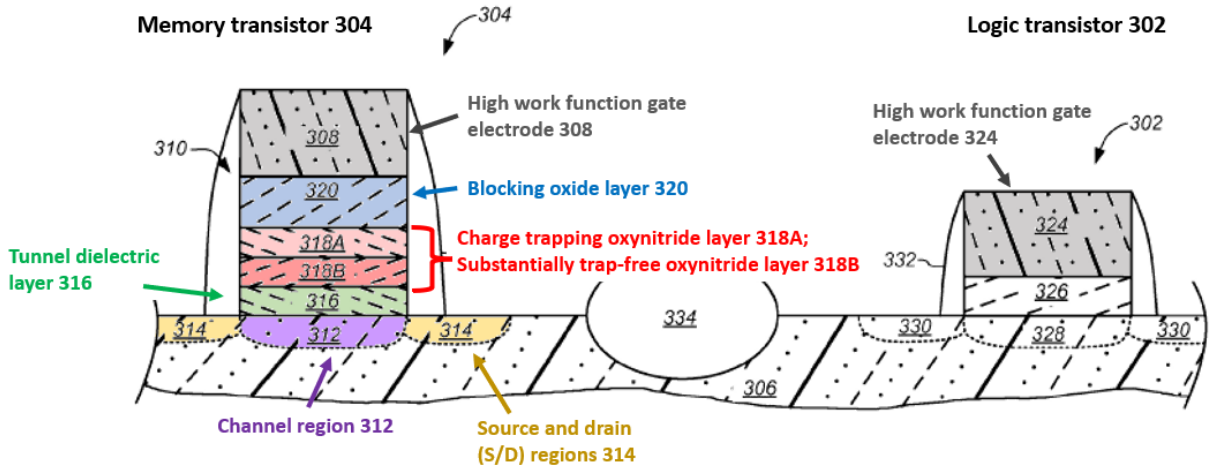


FIG. 3

Ex. 1001 (’240 patent), Fig. 3.

21. Figure 4A provides a larger cross-sectional view of a memory transistor according to the alleged invention, showing an ONNO structure with multi-layer charge-trapping region 422 made up of nitride layers 422a and 422b. Ex. 1001 (’240 patent), 3:11-12. Again, I have annotated figure 4A here:

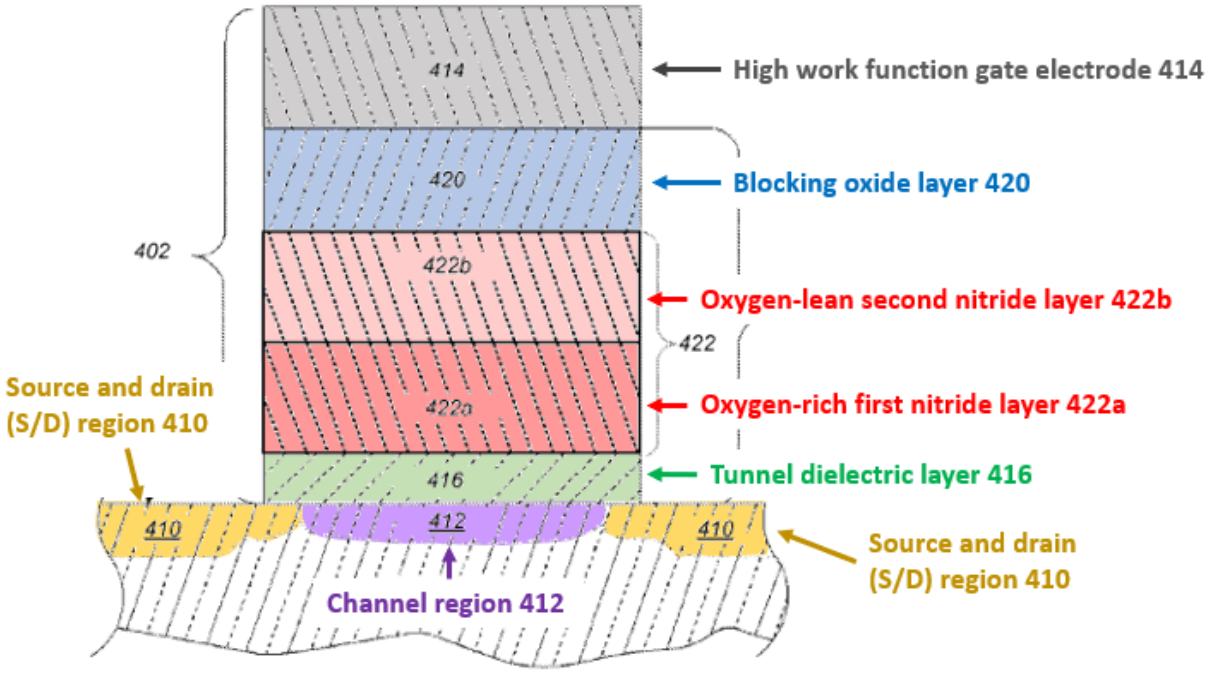


FIG. 4A

Ex. 1001 (’240 patent), Fig. 4A.

22. The ’240 patent provides additional details concerning the above-annotated features of the alleged invention:

- **Diffusion (Source/Drain) Regions 314/410 (Gold).** The memory transistor includes “one or more diffusion regions 410, such as source

and drain regions." Ex. 1001 ('240 patent), 8:55-57; *see also id.*, 8:19-20 ("heavily doped source and drain (S/D) regions 314").

- **Channel Region 312/412 (Purple)**. Electric current flows through a "channel region 312" between the source and drain. Ex. 1001 ('240 patent), 8:18-20. The channel region may be formed of polysilicon. *Id*., 9:1-6.
- **ONNO Stack (Green/Red/Blue)**. The memory transistor includes an oxide-nitride-nitride-oxide (ONNO) stack comprising (i) an oxide "tunnel dielectric layer" (316/416) (green); (ii) a nitride "multi-layer charge storage layer" (318/422) (red); and (iii) a "blocking oxide layer" (320/420) (blue). Ex. 1001 ('240 patent), 8:20-25; 8:63-67.
- **Oxygen Concentrations in the "Multilayer Charge Trapping Layer" (Red)**. The "multilayer charge trapping layer" (red) includes an "oxygen-rich first nitride layer" (318B/422a) and a "silicon-rich, nitrogen-rich, oxygen-lean second nitride layer" (318A/422b). Ex. 1001 ('240 patent), 8:18-31; 8:53-67; 10:1-5. "Either or both" of the "charge trapping" nitride layers "can include silicon nitride or silicon oxynitride." *Id*., 14:7-10.
- **High Work Function Gate Electrode (Gray)**. The memory transistor includes a "high work function gate electrode 308" (Ex. 1001 ('240 patent), 8:14-18), meaning "that the minimum energy needed to remove an electron from the gate electrode is increased" (*Id*., 4:1-3). The high work function gate electrode, for example, may be formed of polysilicon that is "doped to a concentration or dose selected so that the minimum energy needed to remove an electron from the gate electrode is from at least about 4.8 electron volts (eV) to about 5.3 eV." *Id*., 9:19-22.

23. ONNO configurations like those of Figures 3 and 4A were well-known by July 2012 (*see* Part III.C.4), as was the use of high work function gate electrodes (*see* Part III.C.7).

24. Figure 4B depicts an alternative embodiment of the alleged invention where the multi-layer charge trapping layer includes an intermediate oxide anti-tunneling layer (422c) (orange) separating the two nitride layers (oxygen-rich nitride layer 422a, oxygen-lean nitride layer 422b) (red). Ex. 1001 ('240 patent), 10:5-12. This results in an ONONO variation of the ONNO stack. *Id*. Again, I have annotated figure 4B here:

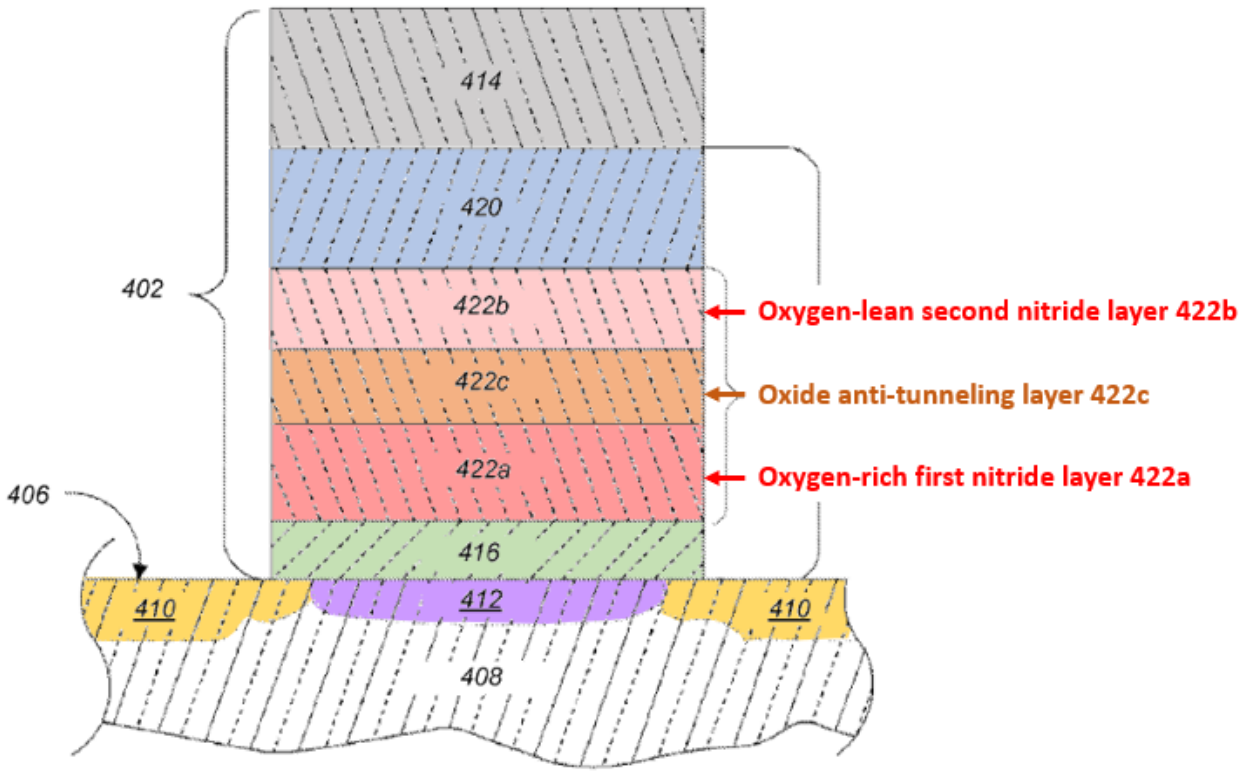


FIG. 4B

25. ONONO configurations like that of figure 4B were well-known by July 2012. *See* Part III.C.5.

26. The '240 patent includes a lengthy section entitled "Implementations and Alternatives" that discloses different ways to arrange the features of the alleged invention discussed above (e.g., diffusion regions, channel region, ONNO or ONONO stack, high work function gate electrode) in designing a memory transistor. Ex. 1001 ('240 patent), 8:47-20:3.

27. Figures 4A and 4B (annotated above) depict a memory transistor similar to figure 3, where a channel region extends horizontally between diffusion regions and the ONNO or ONONO stack is disposed above the channel region.

28. Figures 6A, 6B, 7A, and 7B are also directed to horizontal channels between diffusion regions, but with an ONONO stack surrounding the channel region. Ex. 1001 ('240 patent), 12:61-17:10. For example, figures 6A and 6B are annotated here using the same colors to represent the diffusion regions (gold), channel region (purple), ONONO stack (green/red/orange/red/blue), and high work function gate electrode (gray):

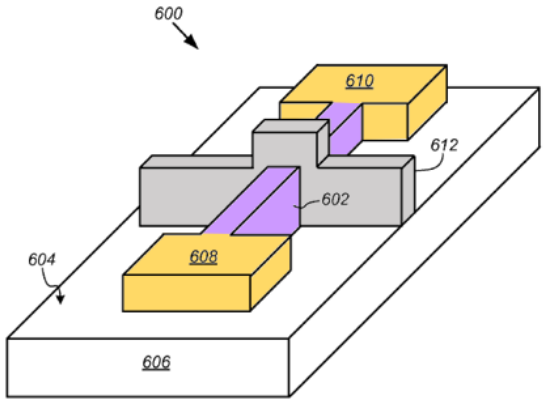


FIG. 6A

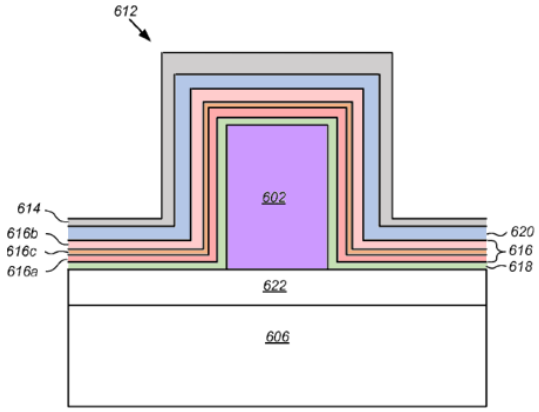
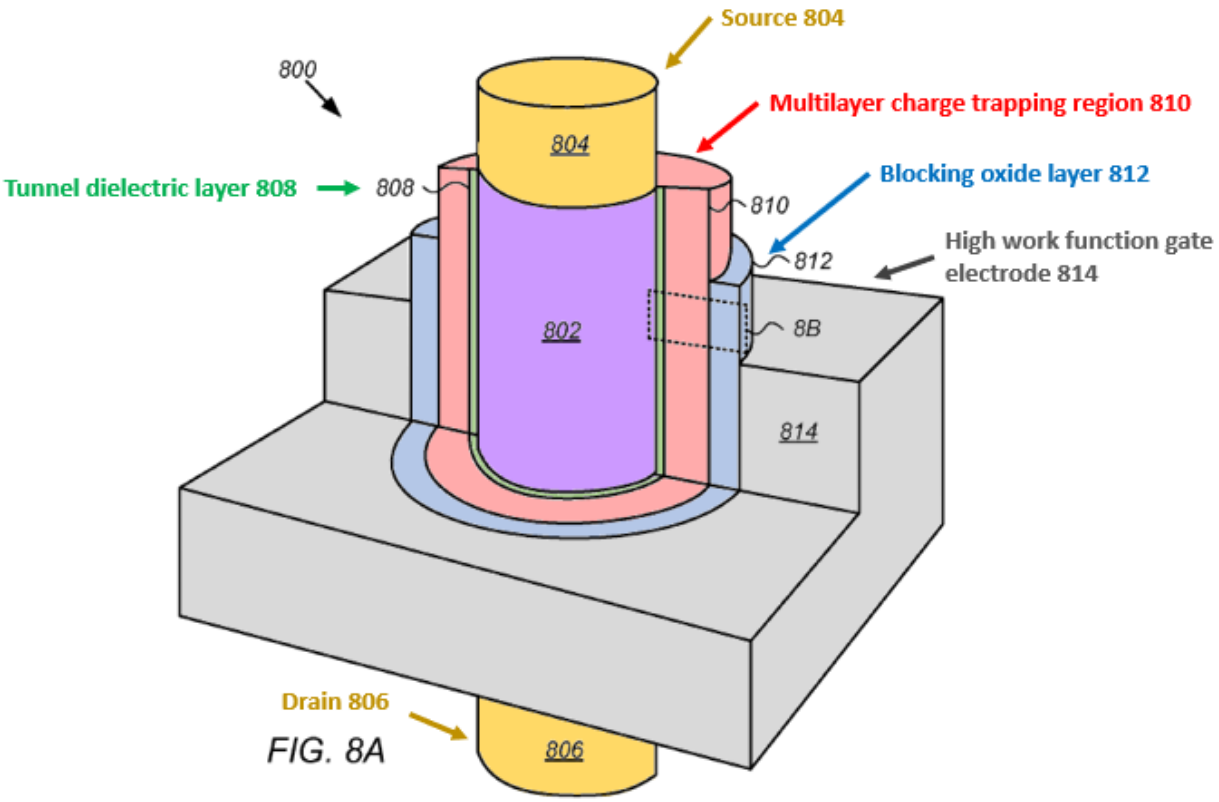


FIG. 6B

Ex. 1001 ('240 patent), Figs. 6A, 6B.

29. A POSITA would have understood that the above figures illustrate a "fin" SONONOS configuration that was well-known by July 2012. *See* Part III.C.6.

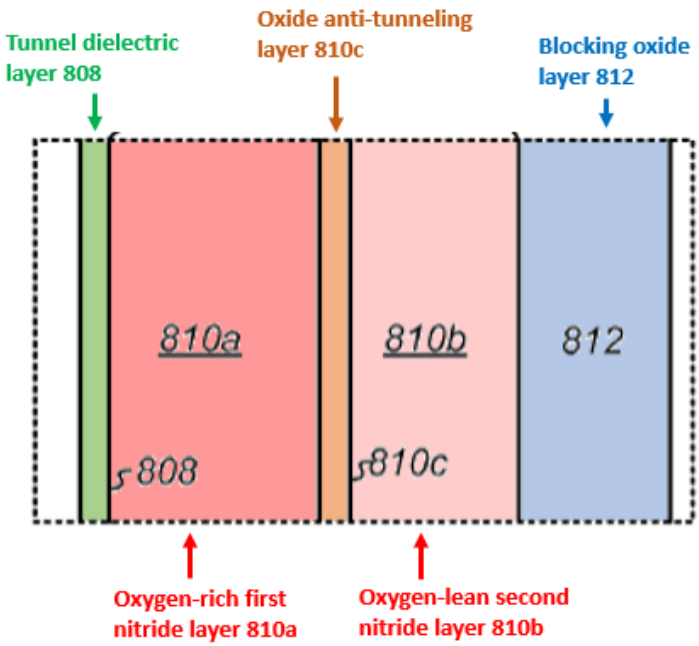
30. Figures 8-10 are directed to vertically oriented memory transistors. Ex. 1001 ('240 patent), 17:11-20:3. For example, figure 8A shows a transistor where the channel region (802) extends vertically between diffusion regions (806) and (804) and the ONONO stack (808/810/812) is disposed about the channel region (802). Ex. 1001 ('240 patent), 17:10-18:8. I have annotated figure 8 here with the same colors as above:



See Ex. 1001 ('240 patent), Fig. 8A.

31. A POSITA would have understood that figure 8A depicts a three-dimensional ("3D") SONONOS configuration, which was well-known by July 2012. *See* Part III.C.6.

32. Figure 8B depicts a cross section of the ONONO stack from figure 8A (see hashed line in figure 8A referring to "8B"):



Ex. 1001 ('240 patent), Fig. 8B.

33. The '240 patent describes the ONONO stack of figure 8 as follows:

> In some embodiments, such as that shown in FIG. 8B, the multi-layer charge trapping region 810 includes at least an inner or oxygen-rich first nitride layer 810a closest to the tunnel dielectric layer 808 and an outer or oxygen-lean second nitride layer 810b. Optionally, as in the embodiment shown, the oxygen-rich first nitride layer 810a and the oxygen-lean second nitride layer 810b are separated by an intermediate oxide or anti-tunneling layer 810c comprising oxide.

Ex. 1001 ('240 patent), 17:49-56.

34. Lastly, figures 9 and 10 depict vertical channel manufacturing processes, including a "gate first" method in figure 9 and a "gate last" method in

figure 10. Ex. 1001 ('240 patent), 3:30-33. In either case, figures 9 and 10 show vertical channels as they are made according to the alleged invention in relationship to the surrounding structure. Ex. 1001 ('240 patent), 18:14-19:14.

35. In short, the '240 patent's contribution is limited to conventional SONOS/SONONOS structures, i.e., ONNO and ONONO stacks, oxygen-rich and oxygen-lean nitride layering, optional anti-tunneling oxide, and high-work-function gates, applied across planar, fin-type, and vertical transistor configurations. Each of these elements was already well-known by July 2012, as discussed below. See Part III.C.

B. Prosecution History of the '240 Patent

36. I understand the '240 patent was filed by Igor Polishchuk, Sagy Charel Levy, and Krishnaswamy Ramkumar (collectively, "the Applicants") as U.S. Patent Application No. 15/335,180 (the '180 Application) on October 26, 2016. *See* Ex. 1002 (Pros. Hist.),000001-000072. I understand that the original application included application claims 1-20 (*id*.,000042-000047), but that Applicants subsequently filed a preliminary amendment replacing those claims with application claims 21-40 (*id*.,000104-000110).

37. I understand that Applicants submitted information disclosure statements during prosecution listing large numbers of prior art references (more than 500 references in total). *See, e.g.*, Ex. 1002 (Pros. Hist.), 000148-000182,

000621-000631, 001079-001086, 001479-001483, 001707-001710, 001741-001744, 001762-001765, 001840-001843, 001874-001877.

38. After the preliminary amendment, Applicants advanced three independent claims: 21, 33, and 38 (corresponding to issued claims 1, 12, and 16 after substantive amendment). Ex. 1002 (Pros. Hist.), 000105-000109, 001827. Each independent claim, as filed, recites the basic features of a SONOS memory device, such as a channel, blocking dielectric layer, tunnel dielectric layer, and gate, along with a "multi-layer charge trapping layer compris[ing] a first dielectric layer disposed abutting a second dielectric layer, wherein the first dielectric layer includes oxygen-rich nitride, and the second dielectric layer includes oxygen-lean nitride." Claims 33 and 38 additionally require that the gate is "high work function" and the presence in the memory device of a MOS logic device and claim 38 adds requirements that certain layers "abut" one another. *Id*. Various dependent claims

were also advanced, including some specifying that the channels were vertical[1] and some specifying the presence of an anti-tunneling layer.[2] *Id*.

39. The Examiner rejected each of the independent claims, and many of the dependent claims, in view of several prior art references teaching SONOS memory devices with horizontal channels. Ex. 1002 (Pros. Hist.), 001611-001630. Although SONOS devices with vertical channels were prior art to the '240 patent (*see* Part. III.C.6), the Examiner did not apply those references and found the dependent claims reciting vertical channels (25, 34, 36, and 39) to be allowable. *Id.*, 001629.

40. The Examiner rejected independent application claims 21, 33, and 38, based on various combinations of: (i) the (horizontal) multi-layer charge trapping region teachings of Kim '424 (Ex. 1050 (Fig. 2 embodiment)), Wang '586 (Ex. 1009 (Fig. 5/6 embodiments)), and Lue '625 (Ex. 1051 (Fig. 1 embodiment)); (ii) the high work function gate electrode teachings of Kim '424, Lue '625, and

---

[1] *See* claims 25, 34, and 39 ("the channel is vertical and oriented substantially perpendicular to a semiconductor material structure"), and 36 ("the channel is vertical and oriented substantially orthogonal to the semiconductor material structure").

[2] *See* claims 27 and 40 ("the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first and second dielectric layers, and wherein the anti-tunneling layer includes an oxide layer").

Hagemeyer (Ex. 1052 (Fig. 1l embodiment)); and (ii) the MOS logic device teachings of Hagemeyer. Ex. 1002 (Pros. Hist.), 001616-001628.

41. In response, Applicants did not dispute the unpatentability of the independent claims as filed. Rather, Applicants amended each of the independent claims. Ex. 1002 (Pros. Hist.), 001722-001738. Regarding application claims 33 and 38, Applicants amended these claims to include the vertical channel limitations. *Id*., 001726-001728, 001735-001736.

42. As for application claim 21, Applicants: (i) amended it to include the "anti-tunneling layer" originally recited in application claim 27; and (ii) argued for its patentability over Lue '625, which was the only reference applied by the Examiner against claim 27. Ex. 1002 (Pros. Hist.), 001724, 001731-001735. But Applicants did not argue that Lue '625 does not teach an "anti-tunneling layer." Rather, Applicants argued that Lue '625 does not disclose the claimed "multi-layer charge storage layer" as a whole because Lue '625 explicitly teaches that dielectric layer 132—which would be analogous to the top oxygen-lean nitride for storing charges in the '240 patent—does not trap charges. *Id*.

43. On October 4, 2017, the Examiner issued a Notice of Allowability for application claims 21-40. Ex. 1002 (Pros. Hist.), 001793-001801.

44. In the Statement of Reasons for Allowance for application claim 21 (issued claim 1), the Examiner stated that Kim '424, Wang '586, and Lue '625

"disclose[] all limitations of claim 21 except for . . . 'an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer." Ex. 1002 (Pros. Hist.), 001799.

45. For application claim 33 (issued claim 12), the Examiner stated that Hagemeyer and Wang '586 disclose everything except for that "the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and a tunnel dielectric layer, a multi-layer charge trapping layer, and a blocking dielectric layer are disposed between the gate structure and the channel." Ex. 1002 (Pros. Hist.), 001799-001800.

46. For application claim 38 (issued claim 16), the Examiner stated that Hagemeyer and Kim '424 disclose everything except for that "the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and a metal oxide semiconductor (MOS) logic device including a gate oxide layer, and a second high work function gate electrode disposed thereon." Ex. 1002 (Pros. Hist.), 001800.

C. Technical Background Relevant to the '240 Patent

47. As I set forth in Part V, below, I understand that July 1, 2012, is the earliest possible priority date for the claims of the '240 patent. In this section, I provide technical background relevant to understanding the general knowledge of a

person of ordinary skill in the art (a "POSITA") as of that date.[3] I also cross-reference and rely on this technical background in explaining my opinions that certain claims of the '240 patent would have been obvious to a POSITA as of July 2012.

1. Non-Volatile Memory

48. Non-volatile memory (or "NVM") is a type of computer memory that can retain stored information even after power is removed. In contrast, volatile memory needs constant power to retain data. Well-known examples of non-volatile memory include hard disk drives (HDDs) and read-only memory (ROM) chips.

49. Regardless of the specific technology, every NVM cell incorporates a physical "state holder" that is energetically stable at room temperature, i.e., it takes substantial energy (more than ambient thermal noise) to disturb it. In magnetic disks, that state is the orientation of magnetic domains; in phase-change memories, it is whether a chalcogenide bit-line segment has crystallized; in flash and other charge-trap devices, it is a packet of electrons parked behind an insulating barrier. Writing data to a NVM applies a stimulus (e.g., magnetic field, heat pulse, high electric field, etc.) strong enough to flip the state. Reading data stored in the NVM

[3] I provide my understanding of the level of ordinary skill in the art in Part VI, below.

senses the state through resistance, capacitance, or another indicator. When external power is removed, the barrier remains, so the state—and thus the data—persists for years.

2. Floating Gate Flash Memory

50. "Flash memory" is a common type of semiconductor NVM. Flash memory was invented in the 1980s and is based on metal–oxide–semiconductor field-effect transistor (MOSFET) technology. MOSFETs are typically composed of a semiconductor material with a source, drain, and gate, as shown in the following basic example:

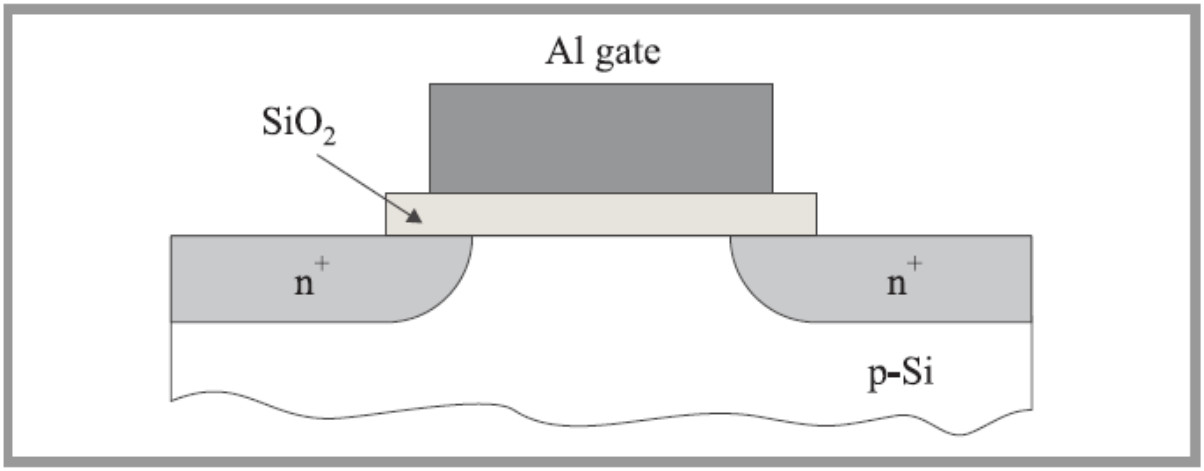


Fig. 4. A cross section of a metal-oxide-semiconductor transistor.

Ex. 1007 (Lukasiak), 000004, Fig. 4.

51. Early flash memory devices dating back to the 1980s were based on a "floating gate" MOSFET design, sometimes referred to as "FGMOS." The design was similar to the regular MOSFET above except FGMOS devices have an

additional electrically insulated gate that "floats" between two oxide layers, as shown here:

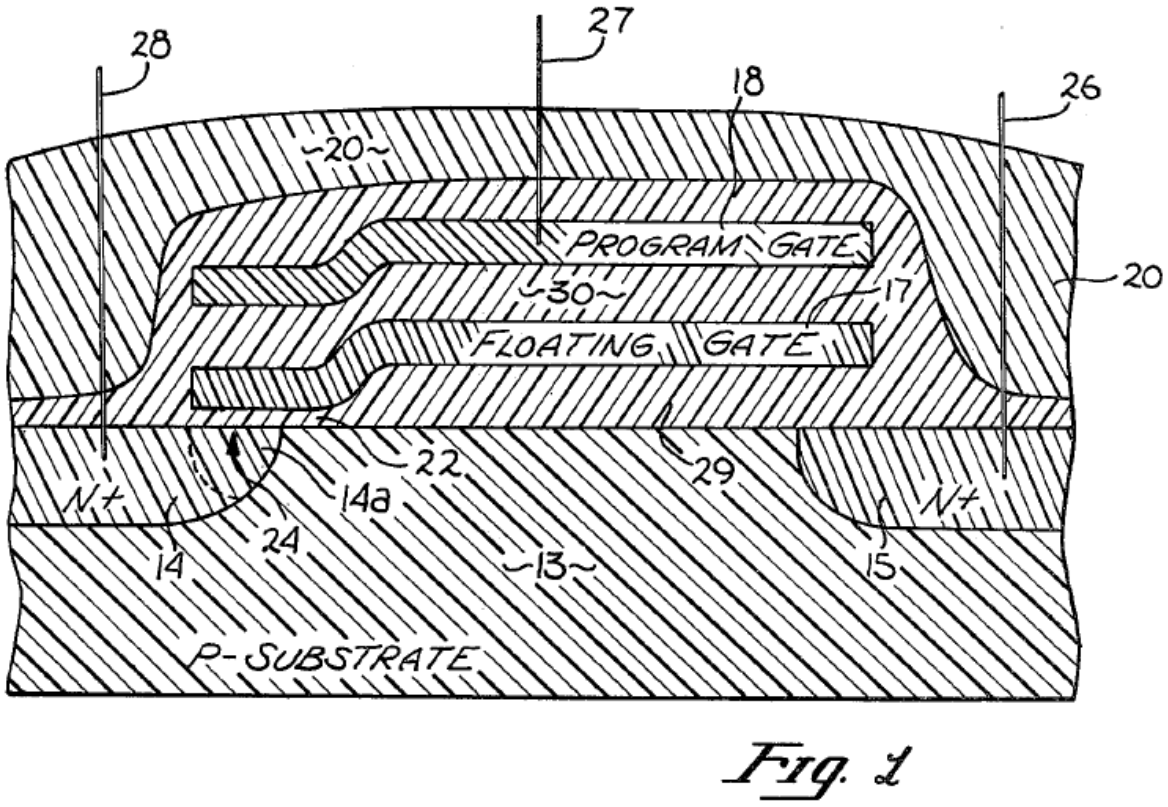
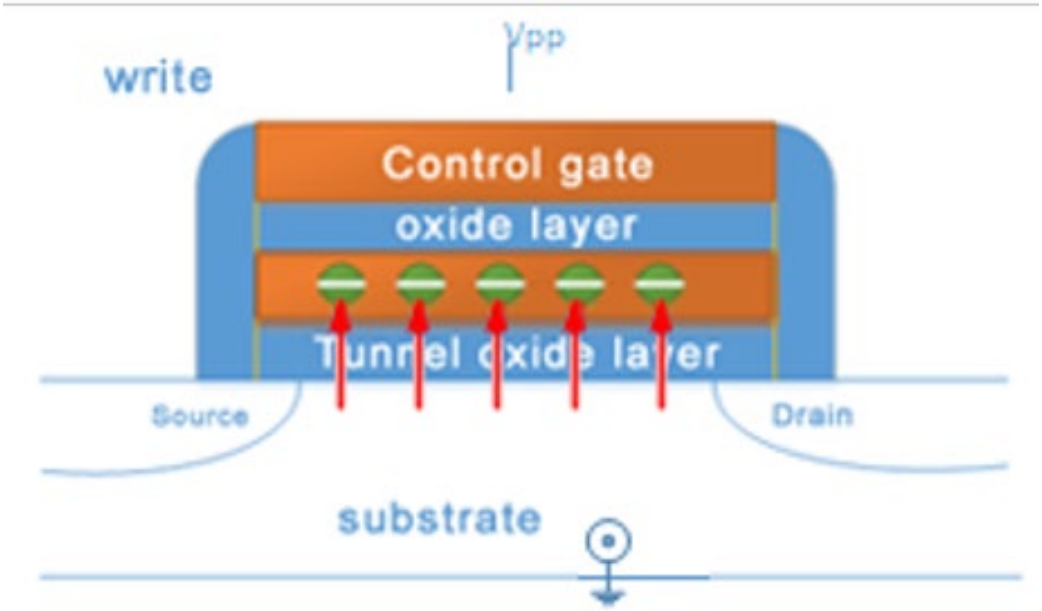


Fig. 1

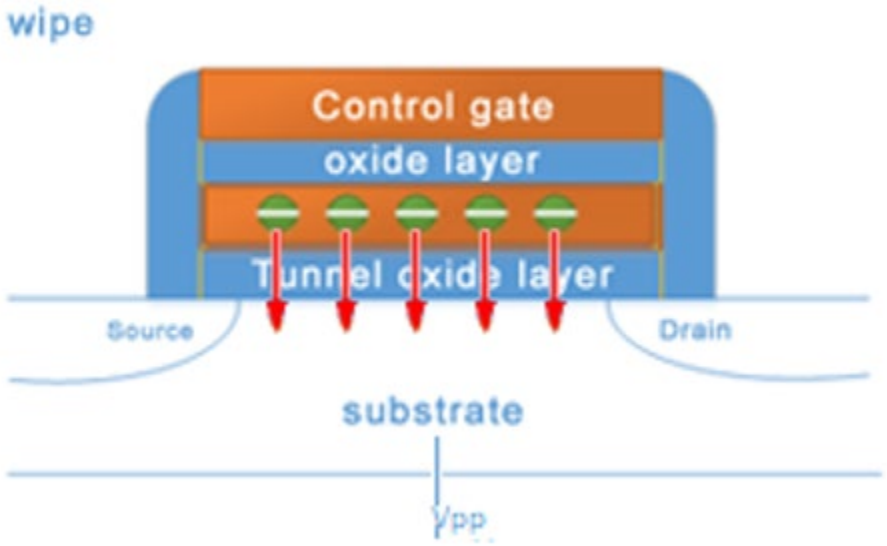
Ex. 1008 (Frohman-Bentchkowsky), Fig. 1; *see also id.*, 4:1-31.

52. Because the floating gate is electrically isolated, any electron placed in the gate will be trapped there—even after voltage is removed. *See, e.g.*, Ex. 1008 (Frohman-Bentchkowsky), 1:18-23, 3:55-57, 5:5-7. This property is what allows the floating gate transistor to function as a non-volatile memory. In the simplest example, the presence of sufficient electrons in the floating gate will cause the memory to be read as a "1," while the absence of electrons in the floating gate will cause the memory to be read as a "0." *Id.*, 1:20-23.

53. Electrons can be placed in the floating gate by various methods, including by "tunneling," where an electric field is applied between the substrate and control gate that causes electrons from the substrate to "tunnel" through the tunnel oxide layer and move into the floating gate. This is called a program/write operation and is depicted here:



54. The electrons can be removed from the floating gate by applying an opposite electric field, which will cause the electrons trapped in the control gate to "tunnel" back to the substrate through the tunnel oxide layer. This is called a clear/erase/wipe operation and is shown here:

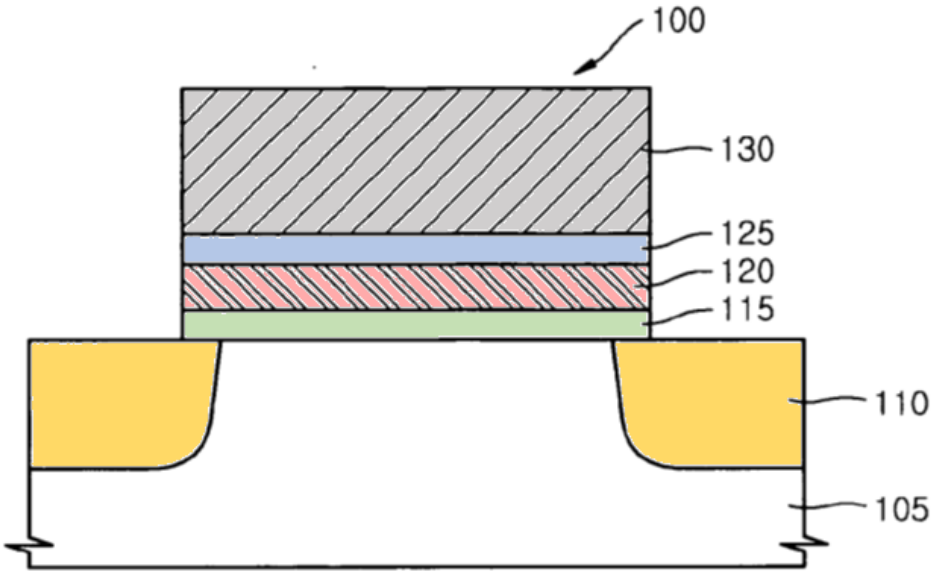


3. "SONOS" Flash Memory

55. By the early 2000s, flash memory devices were also fabricated using charge-trap "SONOS" (silicon–oxide–nitride–oxide–silicon) transistors. The '240 patent is directed to SONOS-type devices.

56. SONOS-type flash memory is similar to floating gate memory except that the floating gate is replaced with a non-conductive silicon nitride layer containing a large number of charge trapping sites. An example of a SONOS memory device is provided in Kim '399 (Ex. 1009), which was filed on February 15, 2006:

FIG. 1 (CONVENTIONAL ART)

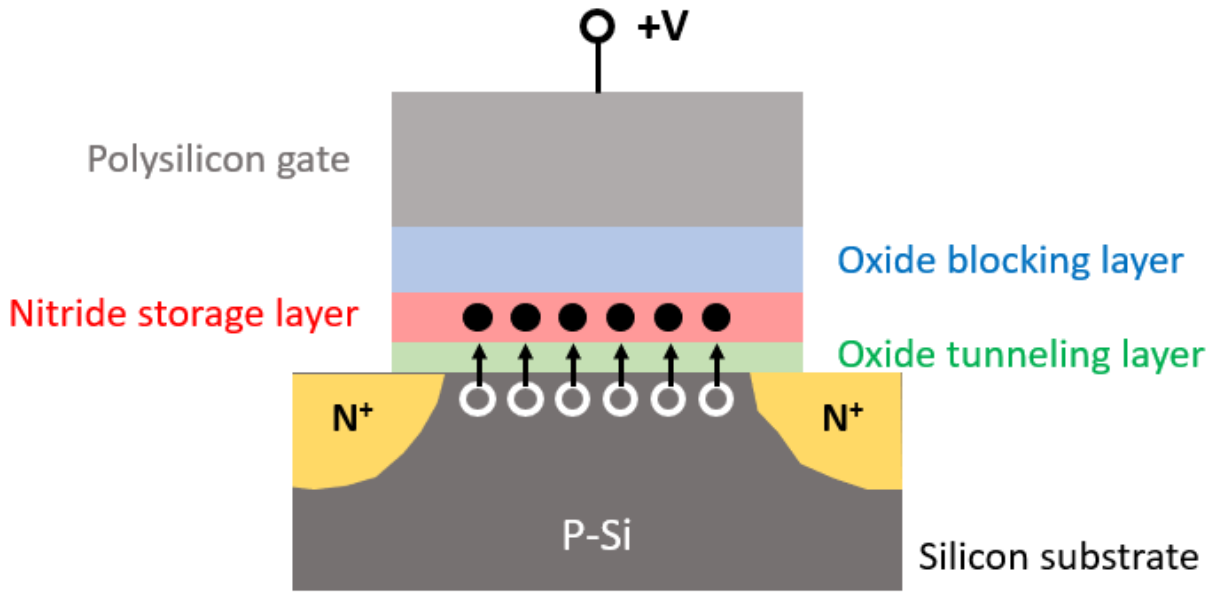


Ex. 1009 (Kim '399), Fig. 1, [0006]-[0008].

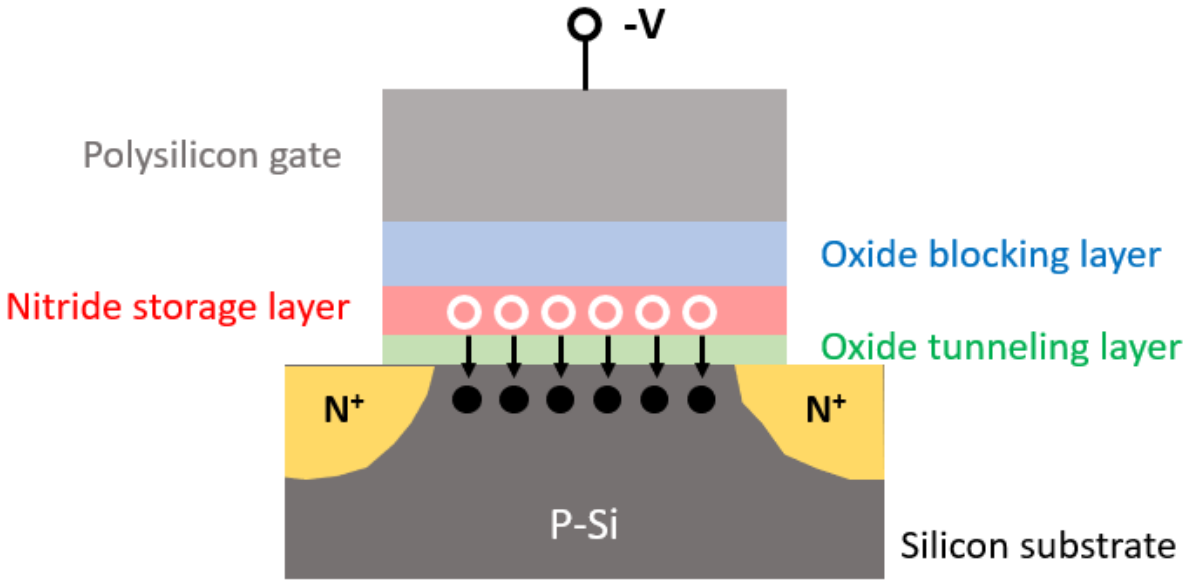
57. As reflected above, the conventional SONOS memory device shown in figure 1 of Kim '399 includes: (i) silicon semiconductor substrate 105 with source/drain regions 110; (ii) oxide tunnel insulating film 115 (green); (iii) nitride charge trapping film 120 (red); (iv) silicon oxide blocking insulating film 125 (blue); and (v) polysilicon control gate 130 (gray).

58. Like floating gate memory, SONOS charge trap memory transistors work by moving electrons, representing data bits (i.e., 1s and 0s), into and out of the nitride charge trapping layer by "tunneling." During a writing/programming step, a positive voltage is applied to the gate, which causes electrons from the substrate to tunnel through the tunnel oxide and into the nitride storage layer.

When the voltage is removed, the electrons remain in the nitride storage layer (even when power to the device is turned off), prevented from moving by the structure of the nitride storage layer and the tunneling and blocking oxides on either side. This is shown in the following figure:



59. To perform an erase/clear step, a negative voltage is applied to the gate, which causes electrons to tunnel from the nitride storage layer back through the tunnel oxide into the silicon substrate. This is shown in the following figure:

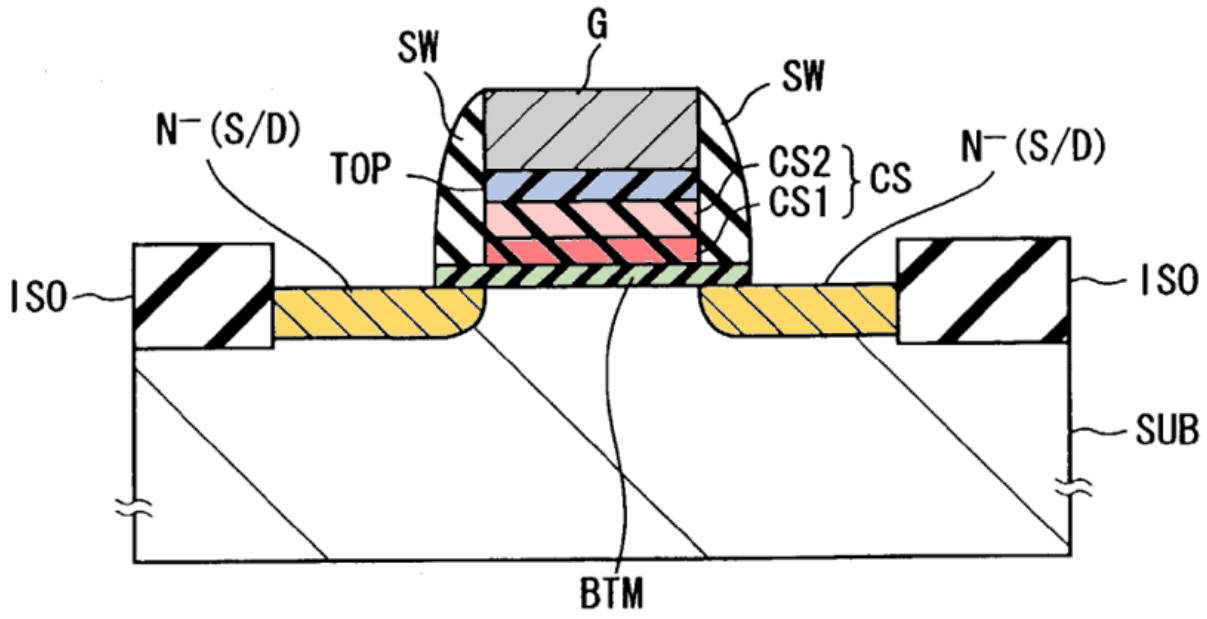


4. SONNOS configurations

60. With the conventional SONOS structure well-established by the mid-2000s, the industry turned to engineering alternative configurations of the SONOS "stack" to optimize performance. For example, a POSITA would have been very familiar prior to July 2012 with a variation that added a second nitride layer to the conventional SONOS stack to create a SONNOS device.

61. It was well understood prior to July 2012 that making the two N layers of different compositions and trap densities, such as by making the lower layer of oxynitride (SiOxNy) and the top layer of nitride, could improve charge storage by preventing electron leakage from the top nitride layer. Nomoto (Ex. 1010), a 2003 U.S. patent application publication, reflects one such device:

FIG.3H



Ex. 1010 (Nomoto), Fig. 3H.

62. As reflected above, Nomoto's figure 3H depicts a SONNOS structure: (i) silicon substrate ("SUB") with source and drain ("S/D"); (ii) a silicon dioxide (SiO_2) bottom dielectric film ("BTM"); (iii) a first nitride film ("CS1"); (iv) second nitride film ("CS2"); (v) silicon dioxide (SiO_2) top dielectric film ("TOP"); and (vi) doped polycrystalline silicon gate electrode ("G"). Ex. 1010 (Nomoto), [0032]-[0038]. Nomoto teaches that the two nitride layers have different compositions (*id.*, [0035], [0044]-[0045]) so that the charge trap density of CS2 is higher than CS1 (*id.*, [0073]-[0088]). Nomoto teaches that the top nitride film (CS2) acts as the primary charge storage layer, while the lower nitride film (CS1) acts as a barrier

that reduces leakage of charges from CS2. Ex. 1010 (Nomoto), [0035]; *see also id.*, [0088] (explaining benefits of two nitride layers).

63. To achieve nitride layers with different trap densities (as in Nomoto), it was well-understood prior to July 2012 to employ (i) an oxygen-lean nitride top layer primarily responsible for storing charges; and (ii) an oxygen-rich nitride bottom layer to prevent electron leakage from the oxygen-lean top layer. For example, Levy (Ex. 1011), reflects this configuration:

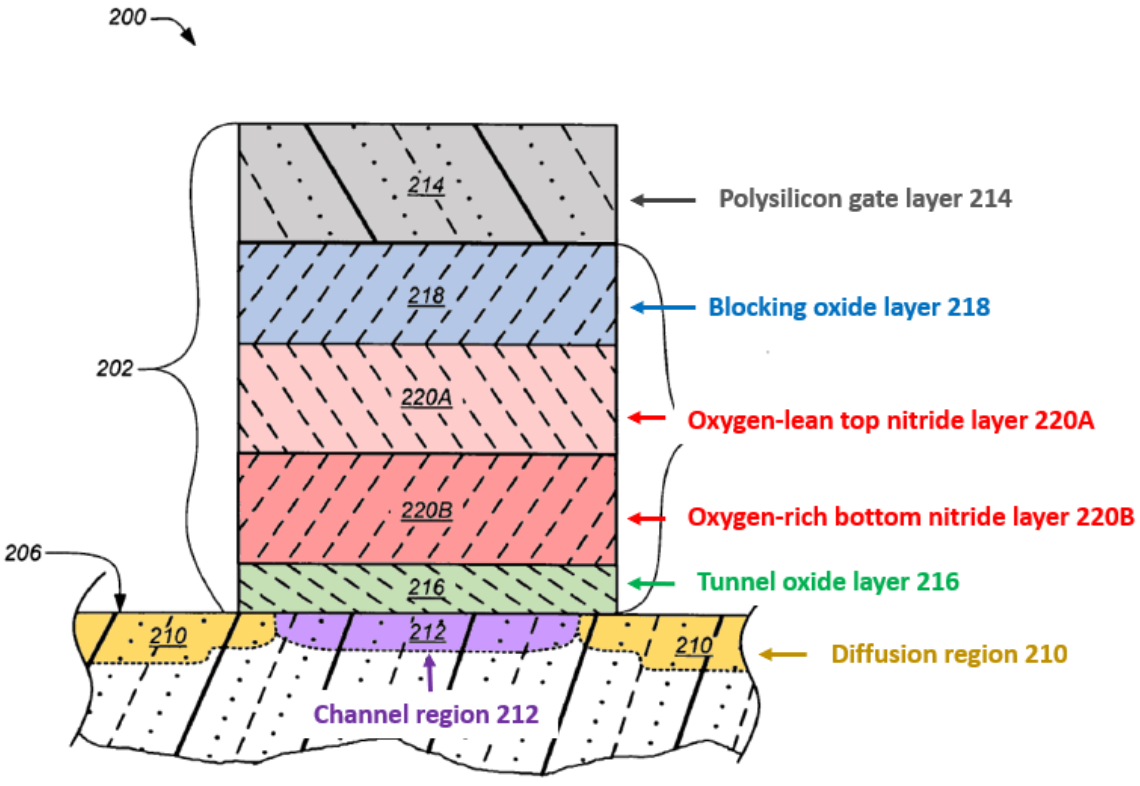


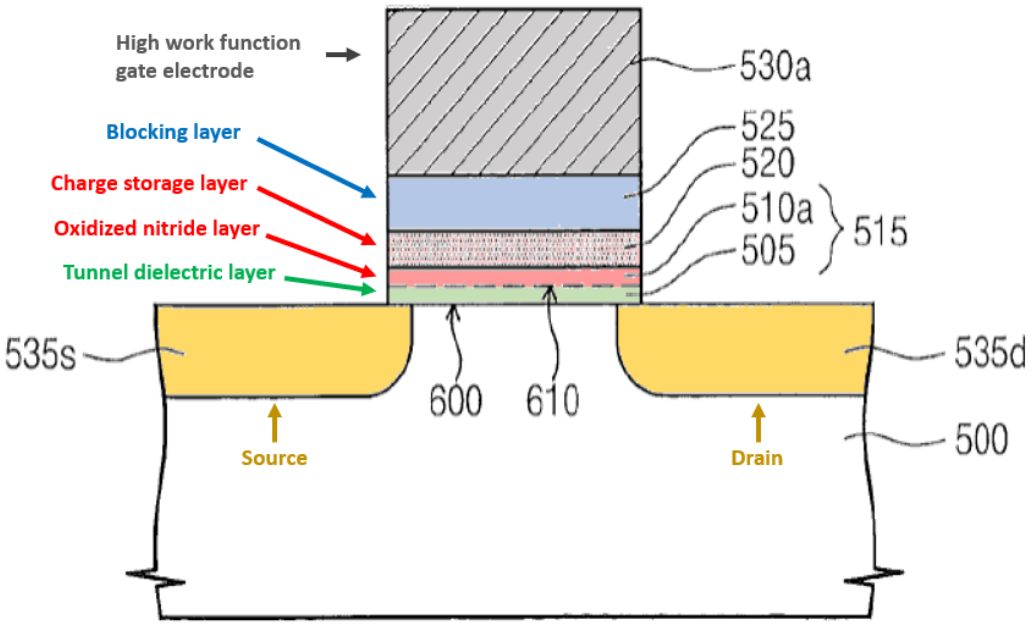
FIG. 2

Ex. 1011 (Levy), Fig. 2; *see also id.*, [0021], [0025]-[002].

64. Consistent with Nomoto, Levy teaches that "a silicon-rich, oxygen-rich, bottom oxynitride layer" decreases the charge loss rate after programming and erase. Ex. 1011 (Levy), [0025].[4]

65. Heo (Ex. 1012) teaches a similar configuration, where an "oxidized nitride layer" is arranged adjacent to the nitride charge storage layer to prevent charge leakage, as shown in annotated figure 8:

Fig. 8



[4] I understand that Levy is a 2009 publication of a 2007 U.S. patent application that shares two inventors with the '240 patent—Sagy Levy and Krishnaswamy Ramkumar. I understand that Levy is prior art to the '240 patent because it was published more than one year before the earliest possible priority date of the claims of the '240 patent (July 1, 2012). *See* Part V, below. As reflected above, figure 2 of Levy mirrors figure 4A of the '240 patent.

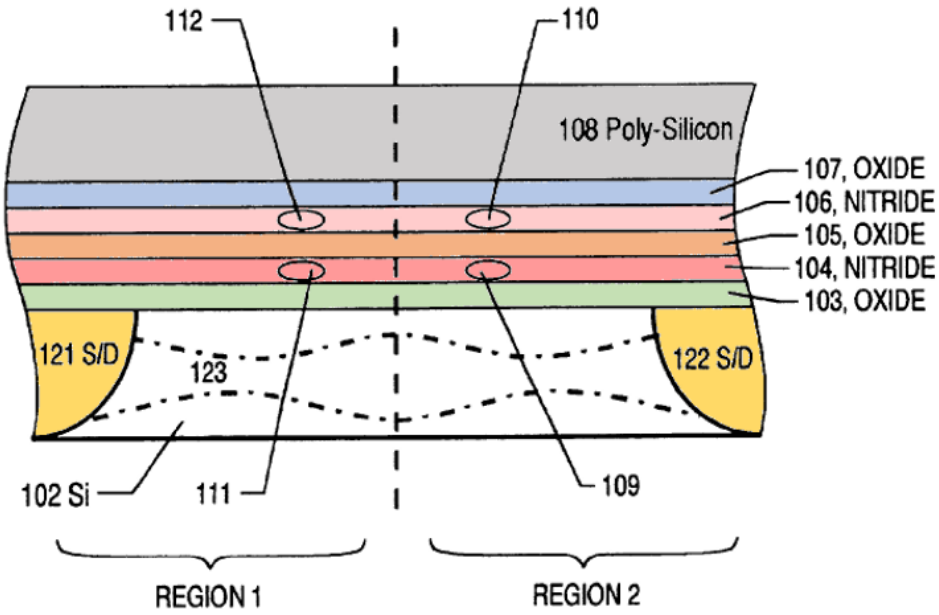
Ex. 1012 (Heo), [0030], [0068].

66. A POSITA would have been aware of numerous other prior art references reflecting SONNOS structures similar to Nomoto, Levy, and Heo—i.e., two nitride layers having differing oxygen concentrations to promote charge retention. *See, e.g.*, Ex. 1009 (Kim '399), Fig. 3 (showing SONOS-type device with multiple nitride layers), [0034] (teaching bottom nitride layer may be silicon oxynitride and top layer may be silicon nitride), [0046]-[0047] (teaching that use of multiple nitride layers suppresses charge loss); Ex. 1013 (Ganguly), Fig. 3, [0048]-[0050] (teaching first nitride layer is oxygen-rich and engineered to have a lower charge trap density in order to promote charge retention in the second nitride layer); and Ex. 1014 (Wang '586), [0031]-[0032] (teaching multi-layer charge storage structures including a silicon oxynitride bottom and nitrided silicon oxynitride top (figure 5) or a silicon oxynitride bottom and nitride top (figure 6)).

5. SONONOS configurations

67. Another well-known variation of SONOS-type memory devices prior to July 2012 was inserting an intermediate oxide layer between two nitride layers to form a SONONOS structure. For example, Yang '533 (Ex. 1015) is a U.S. Patent filed in 2002 and issued in 2005 that teaches a SONONOS structure for a memory cell/transistor 100 having: (i) a substrate with source 121, drain 122, and channel 123; (ii) oxide layer 103; (iii) charge trapping nitride layer 104; (iv) oxide

layer 105; (v) charge trapping nitride layer 106; (vi) oxide layer 107; and (vii) poly gate 108. 1:60-2:3, 2:64-3:8. Each nitride layer has one or more storage regions. Ex. 1015 (Yang '533), 3:9-29.



Ex. 1015 (Yang '533), Fig. 1.

68. Another example can be found in Ex. 1016 (Lue '189), filed and published in 2006, which teaches SONONOS cells having: (i) substrates 101/201 with source 102/202 and drain 104/204 and channel 106/206; (ii) lower/first oxide layer 122/222; (iii) first/small hole-tunneling-barrier height nitride layer 124.224; (iv) second/upper oxide layer 126/226; (v) second/charge-trapping (or charge storage) nitride layer 130/230; (vi) third/insulating oxide layer 140/240; and (vii) polysilicon gate 150/2550. Ex. 1016 (Lue '189), [0057]-[0060].

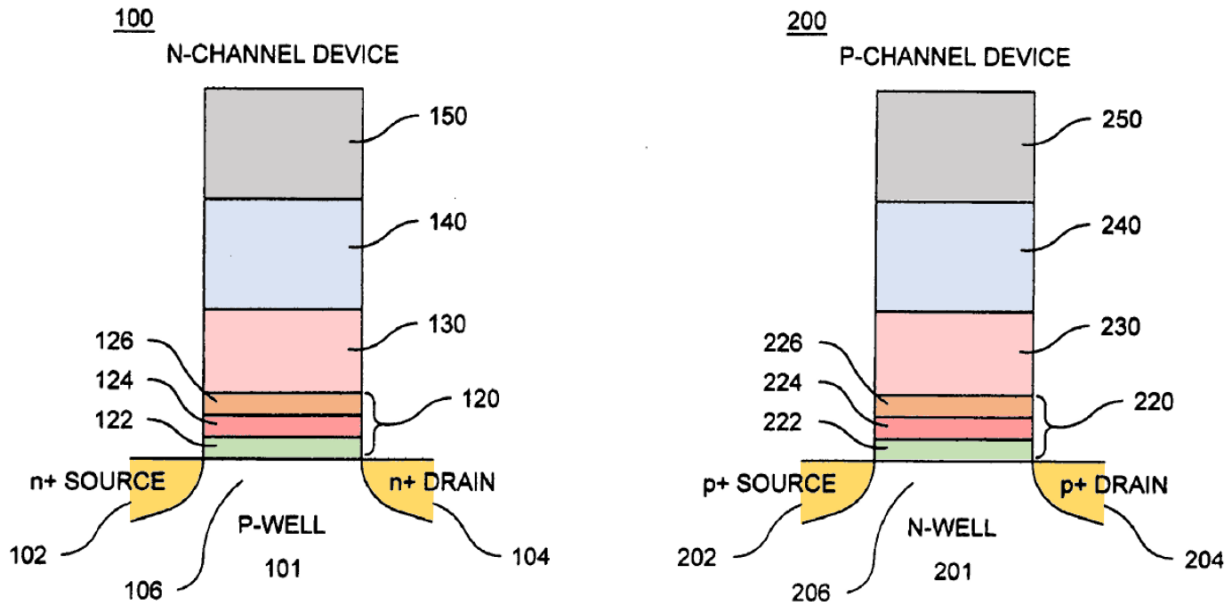
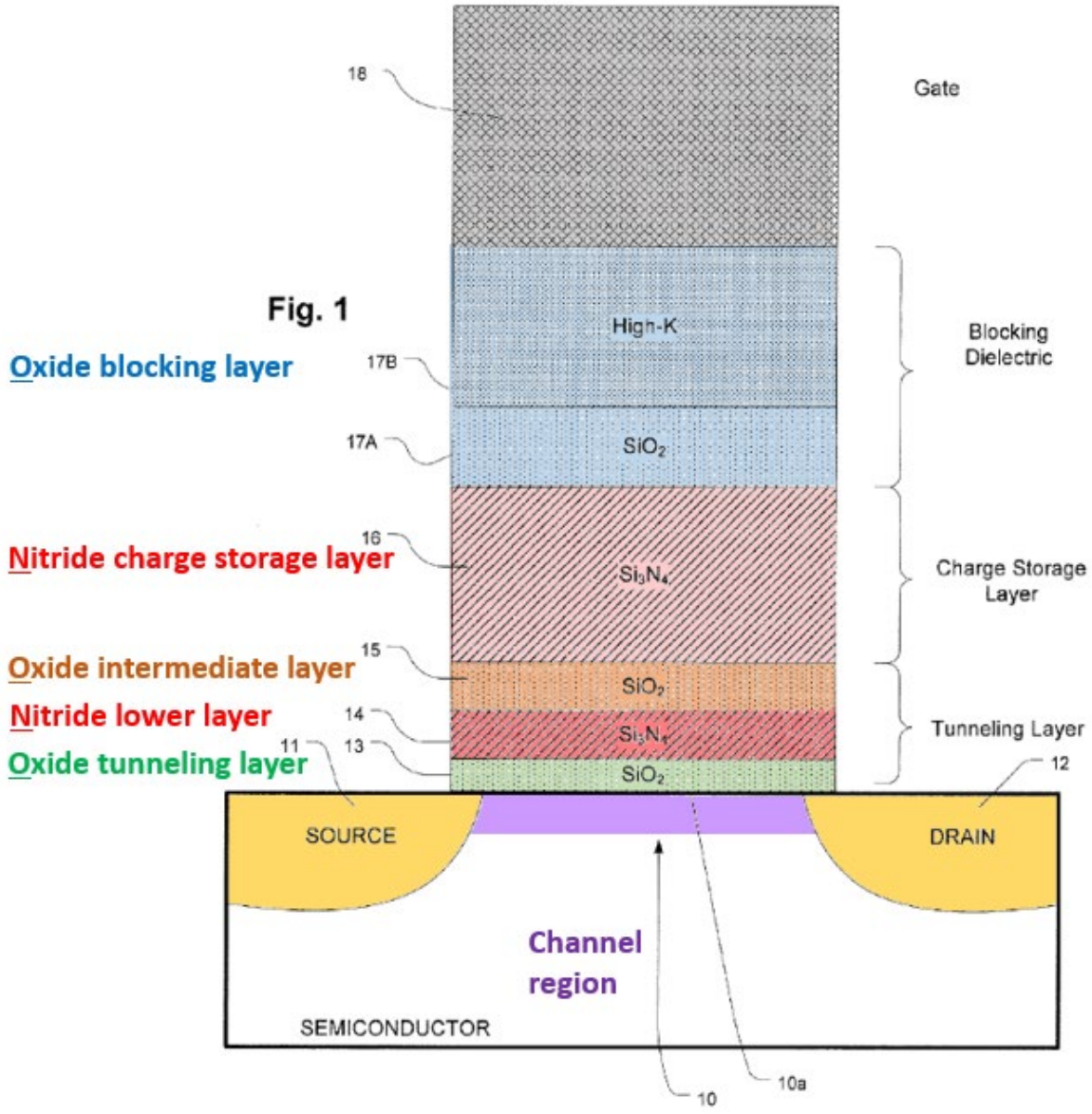


Fig. 1a *Fig. 1b*

Ex. 1016 (Lue '189), Figs. 1a, 1b.

69. Lue '189 teaches that the O1/N1/O2 tunneling dielectric structure 120 allows hole tunneling from the substrate to the charge-storage layer during an erase/reset operation of the memory device and preferably does not trap charges during memory operations. Ex. 1016 (Lue '189), [0059]. This allows fast erase speeds while improving charge retention. Ex. 1016 (Lue '189), [0055], [0061].

70. Lai '676 (Ex. 1017) teaches a similar configuration that is intended to provide improved data retention. Ex. 1017 (Lai '676), [0003], [0015]. In particular, Lai '676 teaches using a SONONOS configuration for trapping charges in its figure 1:



Ex. 1017 (Lai ‘676), Fig. 1.

71. As reflected above, Lai ’676’s SONONOS configuration includes a silicon dioxide tunneling layer 13 (green), a silicon oxynitride band offset layer 14 (red), a silicon dioxide isolation layer 15 (orange), a silicon nitride charge trapping layer 16 (pink), a silicon dioxide blocking dielectric layer 17A/B (blue), and a

doped polysilicon or metal high work function gate 18 (gray). Ex. 1017 (Lai '676), [0067]-[0069], [0074], [0075]-[0077].

72. In addition to Yang '533, Lue '189, and Lai '676, many other references reflect a POSITA's general knowledge prior to July 2012 of SONONOS memory transistors—i.e., SONOS-type memory transistors with an oxide layer separating two nitride layers—and the benefits of using such structures. *See, e.g.*, Ex. 1018 (Lai Article), 000003 (col. 1-2), Table 1, Fig. 1 (teaching SONONOS configuration to provide good data retention); Ex. 1019 (Noguchi), Fig. 1, [0068]-[0069], [0072], [0241]; and Ex. 1020 (Arreghini), 000003 (Fig. 3), 000006 (SONONOS devices "show a faster programming and erasing compared with SONOS cells").

6. Vertically-oriented SONOS-type memory transistors

73. As reflected in figure 1 of Kim '399 (Ex. 1009), early SONOS-type memory transistors typically had ONO stacks formed above channels extending horizontally between sources and drains.

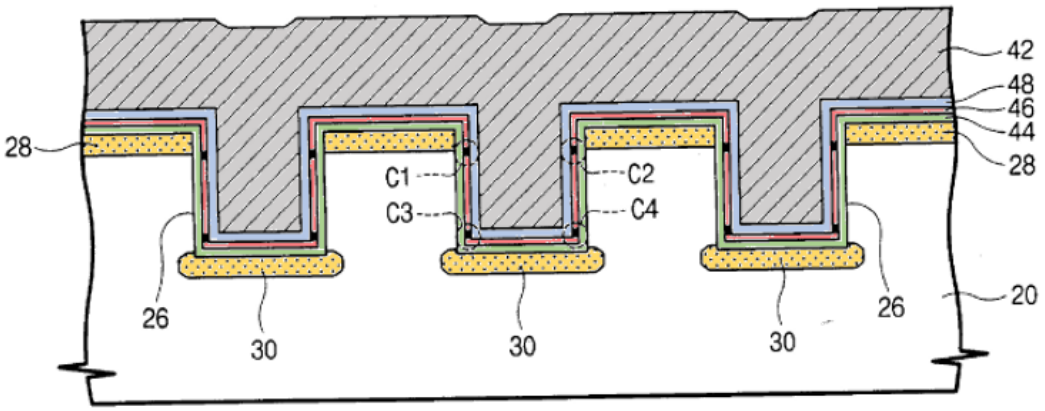
74. By the mid-2000s, a POSITA would have been aware of SONOS-type memory transistors with vertical structures —i.e., transistors with a channel extending vertically (perpendicular to the substrate), where the ONO stack is arranged along the sides of the vertical channel. A POSITA would have understood that this vertical structure could increase the storage capacity of the

memory device because electrons can be stored in the layers on both sides of the channel, rather than in just one horizontal layer above a channel.

75. Despite the difference in channel orientation, a POSITA would have understood that the vertical SONOS memory transistors operate using the same charge trapping principles as the horizontal SONOS memory transistors. This is reflected in numerous references—like the '240 patent itself—that apply the same charge-trapping layers in both vertically-oriented and horizontally-oriented devices. *See, e.g.*, Higuchi (Ex. 1021), Figs. 1A, 1B, 18A, 18B; Ex. 1022 (Jung), Figs. 1-3. Ex. 1025 (VDNROM) ("[T]he fabrication of this VDNROM device is basically compatible with planar CMOS technology"); Ex. 1028 (Kim '759), Figs. 1, 2 (horizontal embodiments), [0070] (vertically stacked ONO structure using same processes as horizontal embodiments); Ex. 1043 (Sekine), [0176]-[0181] (teaching planar structures of figures 1-36 may be applied to vertical 3D memory arrangements of figures 37-61).

76. A POSITA's general knowledge of vertically-oriented SONOS memory transistors prior to July 2012 are reflected, for example, in Choi (Ex. 1023), filed and published in 2003, which teaches a SONOS/SONNOS "trench" memory:

Fig. 9A



Ex. 1023 (Choi), Fig. 9A.

77. Choi teaches that the memory device includes: (i) substrate 20 with grooves 26 and diffusion areas 28 and 30 forming a vertical channel; (ii) silicon oxide tunnel insulating layer 44; (iii) charge trap insulating layer 46 with "at least one silicon nitride layer"; (iv) silicon oxide blocking insulating layer 48; and (v) doped polysilicon or metal gate conductive layer 42. Ex. 1023 (Choi), [0025], [0031]-[0033]. Choi teaches that this configuration is an improvement over the horizontal prior art because it may include more data storage "in the same horizontal dimensions as the conventional art. *Id.*, [0034], [0005], [0006], [0025].

78. Ou (Ex. 1024), filed in 2007 and published in 2009, provides further reflection of a POSITA's knowledge of vertically-oriented SONOS-type memory

transistors prior to July 2012. Figure 4A of Ou depicts, for example, a SONONOS memory device with a vertical channel:

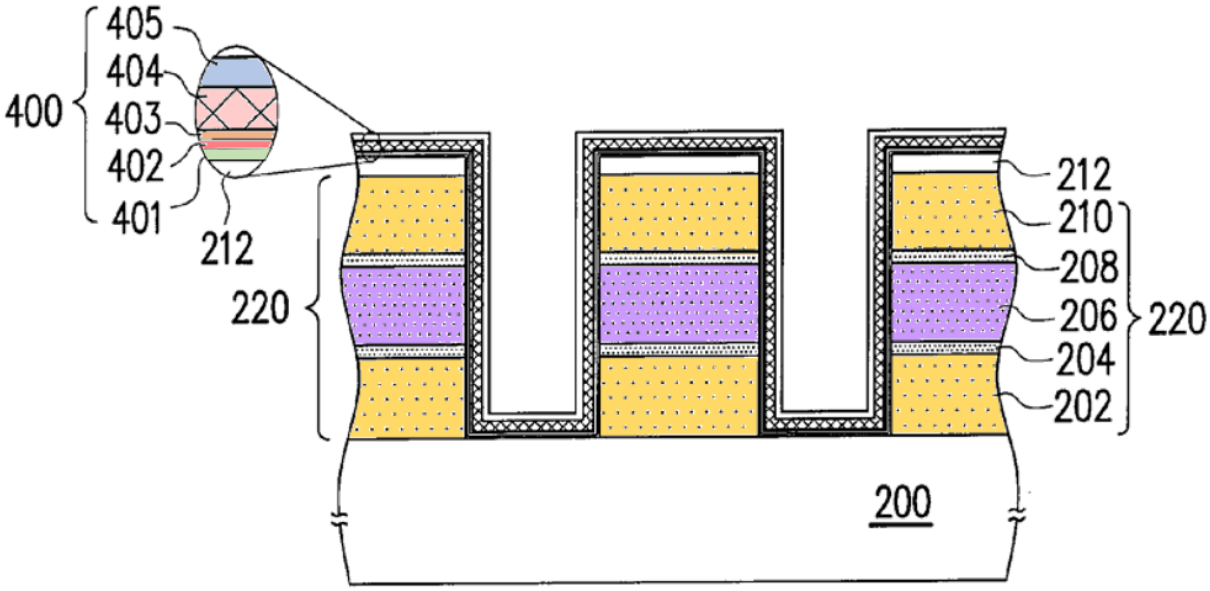


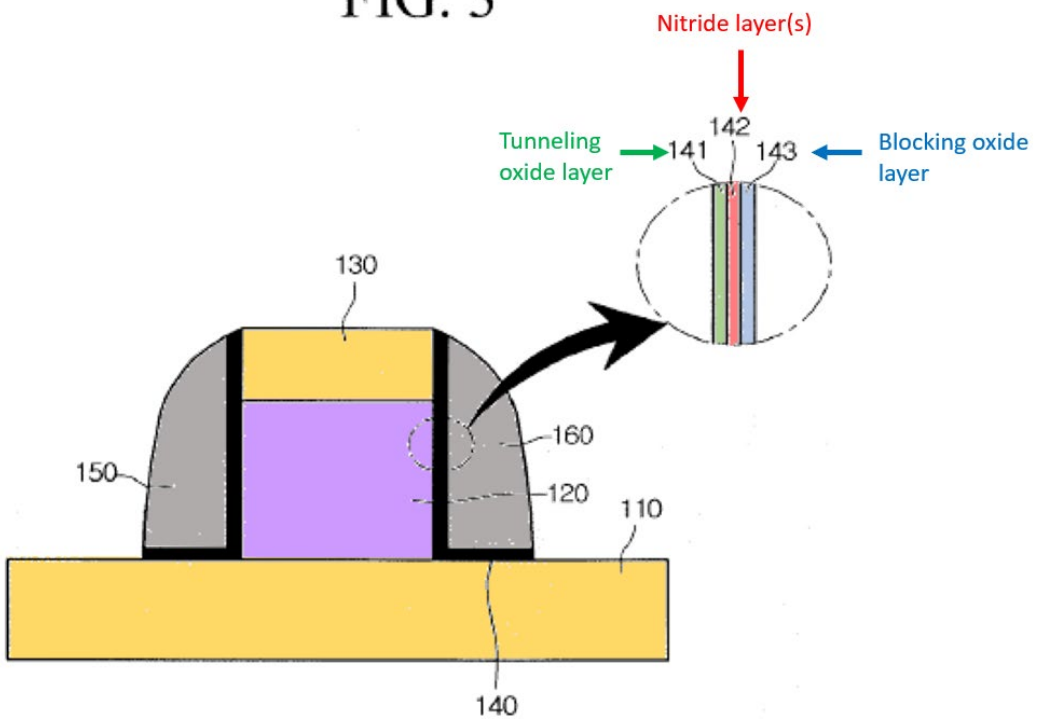
FIG. 4A

Ex. 1024 (Ou), Fig. 4A.

79. This embodiment has semiconductor layers (202, 206, and 210) that act as a source, channel, and drain (*id.*, [0068]); (ii) a first oxide layer (O1) 401 (green); (iii) a first nitride layer (N1) 402 (red); (iv) a second oxide layer (O2) 403 (orange); (v) a second nitride layer (N2) 404 (red); (vi) a third oxide layer (O3) 405 (blue). *Id.*, Fig. 4A, [0066]; *see also id.*, Fig. 4B, [0067] (teaching doped polysilicon gate formed abutting third oxide layer).

80. Jung (Ex. 1022), filed in 2007 and published in 2008, shows another type of vertically-oriented SONOS-type memory in its figure 3 (annotated below), with a vertical polysilicon channel projecting up from a substrate that utilizes either an ONO stack 140 as shown in figure 3, or an ONONO stack of SiO_2—Si_3N_4—SiO_2—Si_3N_4—SiO_2 as identified in paragraph [0015]. Ex. 1022 (Jung), Figs. 3, 8, [0011]-[0015], [0025], [0026].

FIG. 3



Ex. 1022 (Jung), Fig. 3.

81. VDNROM (Ex. 1025), published in 2006, is similar. Figure 1 of VDNROM (annotated below) depicts a vertically-oriented projecting channel surrounded by an ONONO stack:

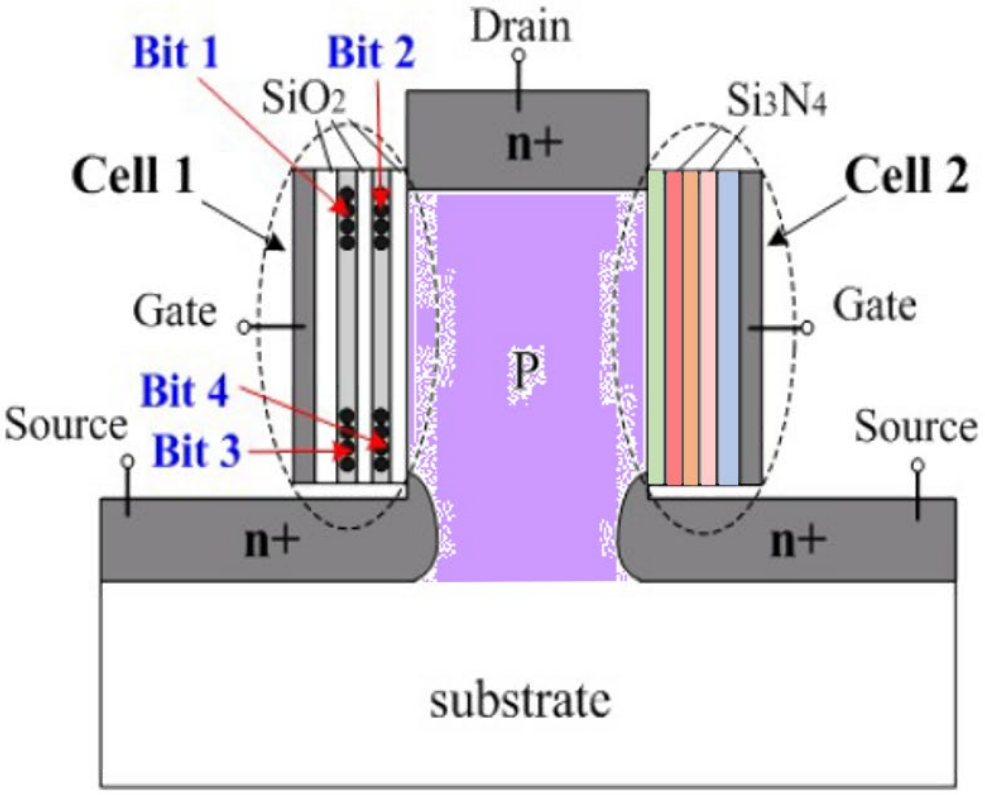
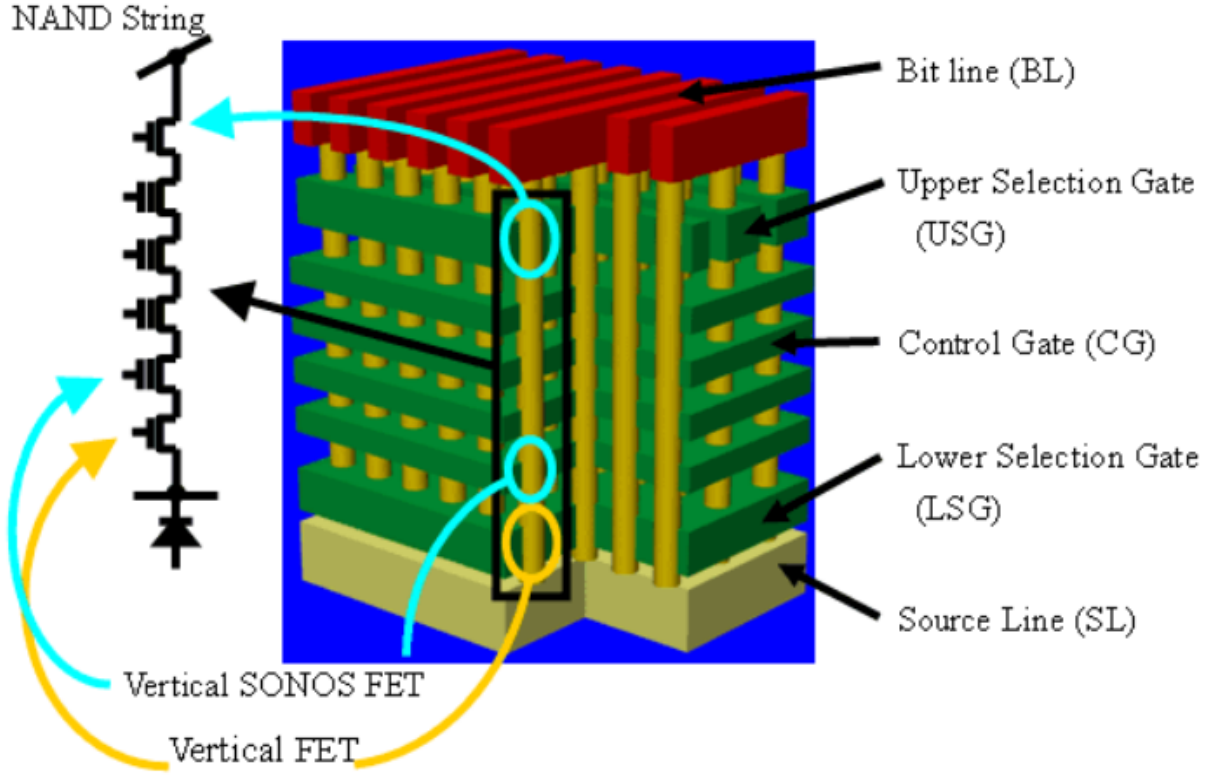


Fig. 1 Schematic cross sectional view of the proposed 4 bits/cell VDNROM flash memory.

Ex. 1025 (VDNROM), 000001, Fig. 1.

82. By the mid-2000s, a POSITA would also have been aware of three-dimensional flash memory configurations ("3D NAND strings") with vertical channels. For example, Toshiba announced its Bit Cost Scalable ("BiCS") 3D NAND technology in 2007. Ex. 1026 (Tanaka), 000001; Ex. 1027 (Toshiba PR). In a press release announcing details of its vertical SONOS structure, Toshiba provided a figure showing the 3D NAND architecture:



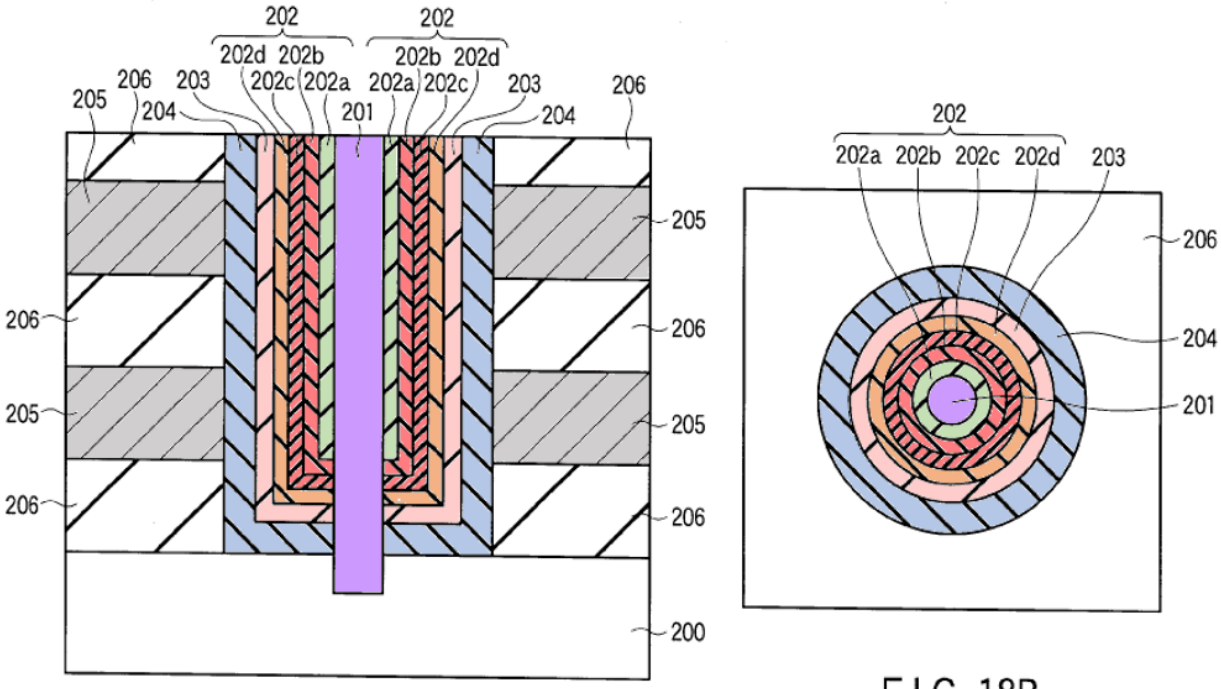
Ex. 1027 (Toshiba PR) ("Toshiba's new method has a SONOS structure—silicon-oxide-nitride-oxide-silicon—and the electrical charge is held in a silicon-nitride film, which is formed inside gate holes").[5]

83. Higuchi (Ex. 1021), a June 2010 U.S. patent application publication, is representative of a POSITA's general knowledge of the vertical 3D NAND

[5] The '240 patent describes "Bit-Cost Scalable or BiCS architecture" as part of the alleged invention. *See* Ex. 1001 ('240 patent), 16:65-17:10. I understand that the portions of the '240 patent referring to BiCS were first added on July 1, 2012, more than five years after Toshiba announced BiCS architecture in June 2007. *See* Ex. 1026 (Tanaka); Ex. 1027 (Toshiba PR).

structure prior to July 2012. Higuchi teaches that its invention is an improvement over conventional horizontal SONONOS structures and provides inventive embodiments of both horizontal (e.g., Figs. 1-16) and vertical (e.g., Figs. 17-26) traps, demonstrating that the teachings are equally applicable to either configuration.

84. For example, Higuchi teaches a vertical 3D NAND memory transistor with a SONONOS configuration in figure 18:



F I G. 18A

F I G. 18B

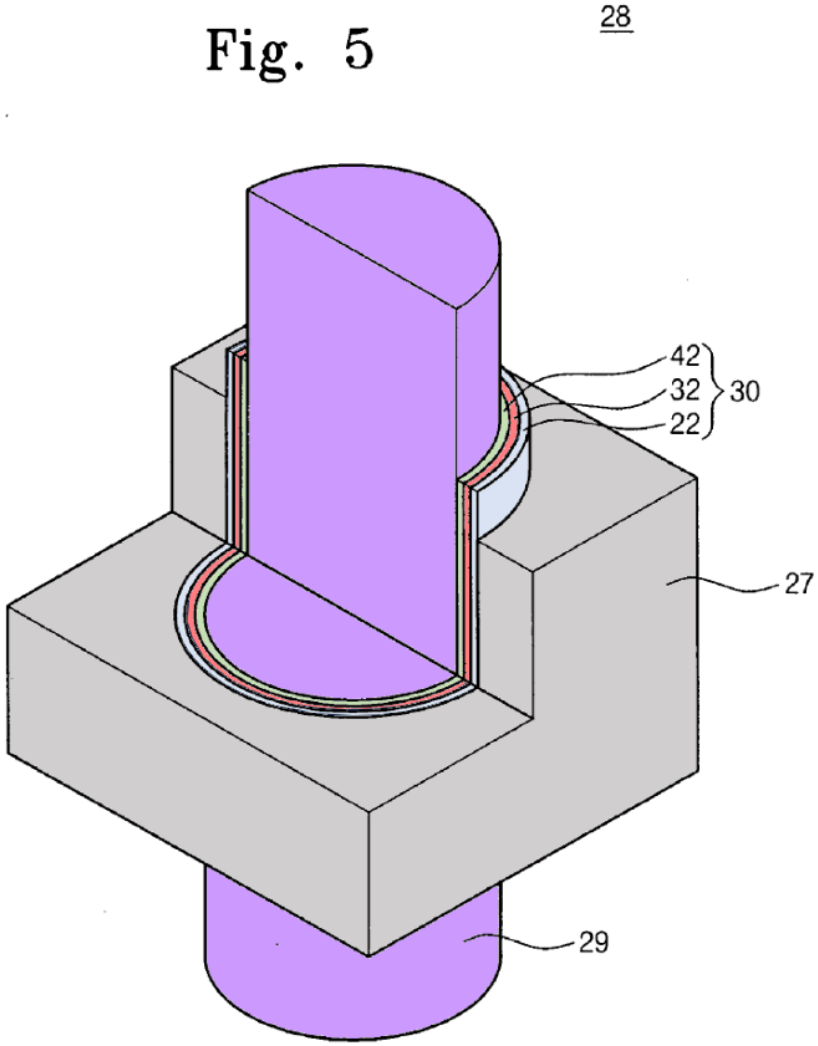
Ex. 1021 (Higuchi), Fig. 18A, 18B, [0131]-[0142].

85. Higuchi explains that this vertical SONONOS structure includes: (i) semiconductor region (silicon region) 201; (ii) oxide film 202a (silicon oxide); (iii) nitride film 202b (silicon nitride); (iv) oxynitride film 202c; (v) oxide film 202d

(silicon oxide); (vi) nitride charge-storage insulating film 203; (vii) block insulating film 204; and (viii) control gate electrode 205. Ex. 1021 (Higuchi), [0133]-[0134].

86. Kim '759 (Ex. 1028), a July 2010 U.S. patent application publication, is also representative of a POSITA's knowledge of vertical SONOS memory structures prior to July 2012. For example, Kim '759 teaches a vertical NAND memory transistor in its figure 5 that is similar to figure 8A of the '240 patent:

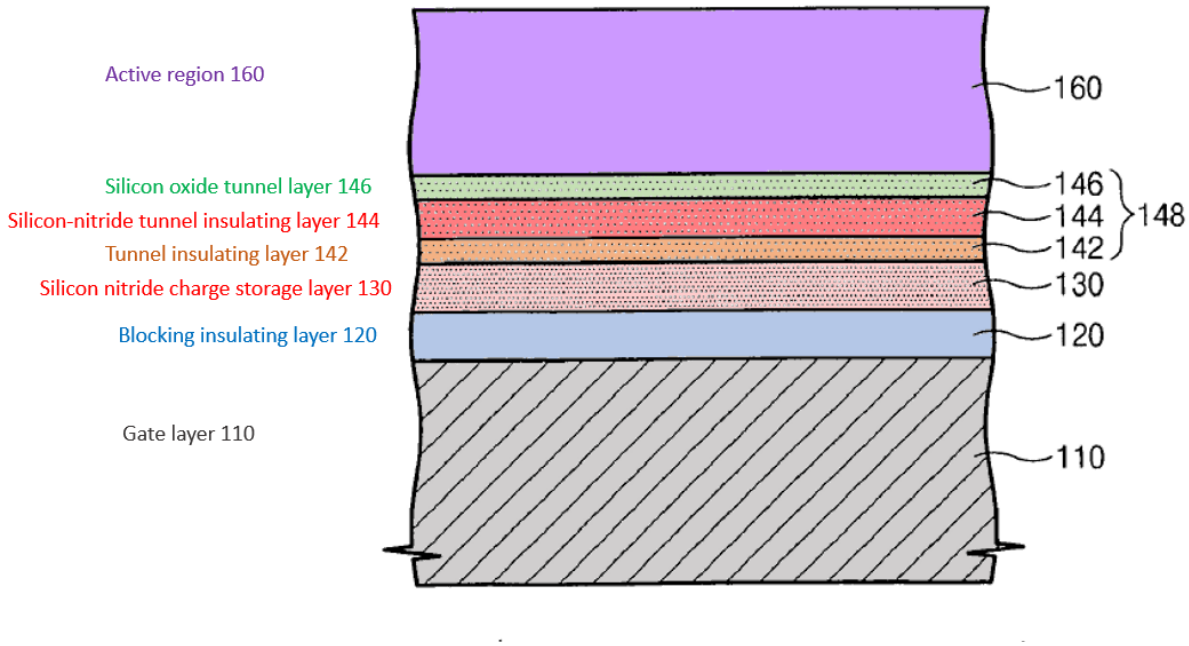
Fig. 5



Ex. 1028 (Kim '759), Fig. 5; *compare id. with* Ex. 1001 ('240 patent), Fig. 8A.

87. Kim ’759 teaches that the vertical SONOS memory device may be configured with a SONONOS structure with an oxide blocking layer (120), a silicon nitride charge storage layer (130), two tunnel insulating layers (142 and 144), and an oxide tunneling layer (146):

Fig. 2C



Ex. 1028 (Kim ’759), Fig. 2C, [0037]-[0048]; *compare id. with* Ex. 1001 (’240 patent), Fig. 8B.

88. Further examples of vertically-oriented SONOS-type memories are found in Yang ’696 (Ex. 1032), Jang (Ex. 1033), Lee ’247 (Ex. 1034), Lee ’086 (Ex. 1035), and Kim ’064 (Ex. 1036).

7. High work function gate electrodes

89. A POSITA would have had general knowledge of the use of high work function gate electrodes with SONOS-type memory transistors prior to July 2012.

90. For example, the Kim Article (Ex. 1029), a 2007 article entitled, "A Comparison of N+ Type and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories," teaches that the use of a boron-doped p+ polysilicon gate in a SONOS memory device provides improved erase speed as compared to a n+ polysilicon gate, due to the p+ polysilicon gate having a higher work function. *See, e.g.*, Ex. 1029 (Kim Article), 000005, Fig. 7 ("The erase speed of p^+ polysilicon gate memory is much faster than that of n^+ polysilicon gate memory.").

91. Beyond the Kim Article, there are many other representative examples of a POSITA's general knowledge of the routine use of high work function gate electrodes with SONOS memory transistors. *See, e.g.*, Ex. 1016 (Lue '189), [0084] (in preferred embodiments, high work function gates can be formed of metals, metal nitrides, or P^+ polysilicon), [0086] ("High work function gate materials suppress gate electron injection into the trapping layer. . . . [T]he memory cells according to high work function gate material embodiments of the present invention are particularly suitable for use in NAND applications where elevated threshold voltages in the erased/reset state can be undesirable."); Ex. 1017 (Lai

‘676), ¶¶[0007], [0052] (“higher work-function metal gate has lower erase saturation”), [0067] (“For some applications, it is preferable to use materials having work functions higher than 4 eV, preferably higher than 4.5 eV”), [0124] (“A high work-function metal gate (such as Pt) is necessary to suppress the gate injection for these type cells.”); Ex. 1012 (Heo ‘647), [0064] (teaching the use of a high work function gate electrode to improve the efficiency and ease of operation of the flash memory); Ex. 1030 (Jeon ‘858), Fig. 1, [0009] (“The control gate 14 includes either N^+ polysilicon with a work function of 4.1 eV or p^+ polysilicon with a work function of 5.1 eV.”); Ex. 1031 (Shih ‘809), [0071] (“In some embodiments, the gate comprises a material having a work function greater than the intrinsic work function of n-type silicon. . . for example, greater than about 5 eV. Representative gate materials include p-type poly TiN, Pt, and other high work function metals and materials.”); and Ex. 1041 (Zheng ‘163), 5:52-62 (P+ polysilicon is “particularly well suited” for use in high work function gate electrodes); id., 6:32-59 (tantalum and tantalum nitride used for high work function gate electrodes).

IV. CHALLENGED CLAIMS

92. I understand that Petitioners are challenging the validity of claims 1, 3-7, 9, and 11-18 of the ’240 patent (the “Challenged Claims”), which are

reproduced in Appendix 3. In forming my opinions, I have considered all of the claims of the ’240 patent, as well as portions of the prosecution history.

V. PRIORITY DATE OF CHALLENGED CLAIMS

93. In performing my analysis, I have used July 1, 2012—the filing date of the application for U.S. Patent No. 8,633,537 (the ’537 patent)—as the relevant priority date for the reasons set forth below.

94. On its face, the ’240 patent identifies six related U.S. patent applications:

	App No.	Filing Date	Patent No.	
A	60/940,160	5/25/2007	n/a	“the ’160 provisional”
B	12/152,518	5/13/2008	8,063,434	“the ’434 patent”
C	13/288,919	11/3/2011	8,859,374	“the ’374 patent;” divisional of B
D	13/539,466	7/1/2012	8,633,537	“the ’537 patent;” continuation-in-Part of C
E	14/159,315	1/20/2014	9,093,318	“the ’318 patent;” continuation of D
F	14/811,346	7/28/2015	9,502,543	“the ’543 patent;” continuation of E
G	15/335,180	10/26/2016	9,929,240	“the ’240 patent;” continuation of F

95. I understand that a patent cannot claim priority to earlier applications if, from the perspective of an ordinary artisan, the patent claims include new matter not present in those earlier applications. *See* Appendix 4 (Understanding of the Law).

96. To determine the earliest possible priority date for the claims of the ’240 patent, I reviewed the three earliest-filed applications—the ’160

provisional application (filed May 25, 2007), the application for the ’434 patent (filed May 13, 2008), and the application for the ’374 patent (filed November 3, 2011) (collectively, the “Earlier Applications”). *See* Ex. 1037 (’160 Provisional App.); Ex. 1038 (’434 Pros. Hist.); Ex. 1039 (’374 Pros. Hist.). In my opinion, from the point of view of an ordinary artisan, these Earlier Applications do not support the claims of the ’240 patent.

97. Regarding independent claim 1, as discussed above, it recites a memory device that includes “an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer.” Ex. 1001 (’240 patent), claim 1. In my opinion, the Earlier Applications do not describe memory devices with the claimed intermediate “anti-tunneling layer.”

98. The Earlier Applications are silent as to any “anti-tunneling layer” disposed between a first and second dielectric layer. Rather, the embodiments of the Earlier Applications disclose that the first and second dielectric layers are adjacent to each other without any intermediate layer between. *See, e.g.*, Ex. 1037 (’160 Provisional App.), 9-10 (Fig. 1); Ex. 1038 (’434 Pros. Hist.), 000137-000139 (Figs. 2A-3) ; Ex. 1039 (’374 Pros. Hist), 000197-000199 (Figs. 2A-3). For Example, figure 3 of the application that resulted in the ’434 patent shows that the

first and second dielectric layers (318A, 318B) are adjacent without an intermediate anti-tunneling layer:

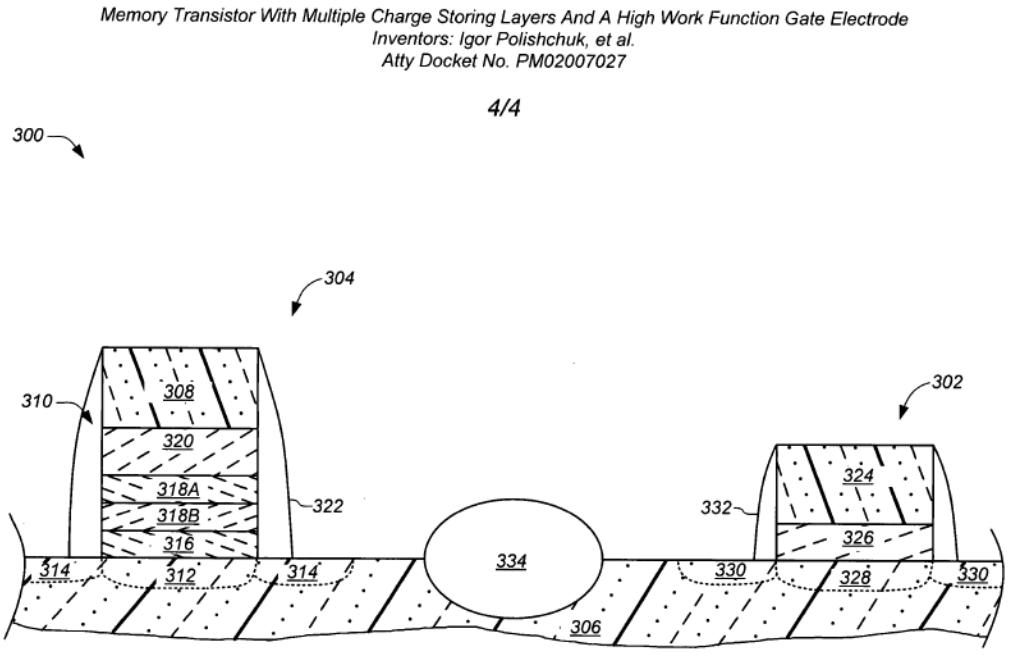


FIG. 3

Ex. 1038 (’434 Pros. Hist.), 000139. This figure is the same as figure. 3 of the ’374 patent (and its underlying application) and figure 3 of the ’240 patent.

99. The Earlier Applications do not include the embodiments of the ’240 patent that have an “anti-tunneling layer,” such as the embodiments of figures 4B, 6B, 7B, or 8B and the accompanying written description (*see* Ex. 1001 (’240 patent), 13:12-18:8). Rather, those figures and the accompanying written description of the anti-tunneling layers were first added in the continuation-in-part application for the ’537 patent, which was filed on July 1, 2012. *See* Ex. 1040

('537 Pros. Hist.), [000218-000278]; *compare id. with* Ex. 1038 ('434 Pros. Hist.), [000111-000139] *and* Ex. 1039 ('374 Pros. Hist.),[000158-000199].

100. Regarding independent claims 12 and 16, as discussed above, these claims recite memory devices with channels, "wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure." Ex. 1001 ('240 patent), claims 12, 16. In my opinion, the Earlier Applications do not describe memory devices with such a "vertical" channel.

101. The Earlier Applications are silent as to any "vertical" channel that is "oriented substantially perpendicular to a semiconductor material structure." Rather, the memory transistors disclosed in the Earlier Applications are exclusively horizontally-oriented (i.e., the channels extend horizontally between diffusion regions parallel to a substrate). For example, the channel 312 in figure 3 of the application for the '434 patent reproduced above (which is the same as figure 3 of the application for the '374 patent and figure 3 of the '240 patent), shows such a horizontal channel.

102. The Earlier Applications do not include any of the vertical channel embodiments of the '365 patent, which are found in figures 8A-8B, 9A-9F and 10A-10F and the accompanying written description (*see* Ex. 1001 ('240 patent), 17:11-20:3). Rather, those figures and the accompanying written description of the vertical channel embodiments were first added in the continuation-in-part

application for the ’537 patent, which was filed on July 1, 2012. *See* Ex. 1040 (’537 Pros. Hist.),[000218-000278]; *compare id. with* Ex. 1038 (’434 Pros. Hist.), [000111-000139]; Ex. 1039 (’374 Pros. Hist.),[000158-199].

103. Because features of the independent claims of the ’240 patent (claims 1, 12, and 16) are not disclosed in any of the Earlier Applications, I understand that the earliest possible priority date for the claims of the ’240 patent is July 1, 2012—the date the application for the ’537 patent was filed.

VI. LEVEL OF ORDINARY SKILL IN THE ART

104. The ’240 patent is in the field of non-volatile semiconductor memory. *See, e.g.*, Ex. 1001 (’240 patent), 1:26-29. Each of the Challenged Claims is directed to either a “semiconductor device, comprising a memory device …” (*see id.*, claims 12, 16) or a “memory device” (*see id.*, claim 1). In determining the characteristics of a hypothetical person of ordinary skill in the art (a “POSITA”) in the area of the ’240 patent as of July 1, 2012, I considered several things, including various prior art techniques relating to the structure and fabrication of memory transistors and the rapidity with which innovations were made in those areas. I also considered the sophistication of the technologies involved, and the educational background and experience of those actively working in the field at the time. I also considered the level of education that would be necessary to understand the ’240 patent. Finally, I placed myself back in the relevant period of time and

considered the engineers that I have worked with in the field of non-volatile semiconductor memory.

105. I am familiar with the knowledge and capability that a POSITA would have possessed in the field of the '240 patent as of July 1, 2012, based on my personal experience with semiconductor devices and fabrication in relation to both academia and industry. It is my opinion that a POSITA as of July 1, 2012 would have had at least (1) a master's degree in electrical engineering, materials science, physics, or a related degree, and at least 3-5 years of experience in semiconductor devices and fabrication technologies; or (2) a bachelor's degree in electrical engineering, materials science, physics, or a related degree, and at least 5-6 years of experience in semiconductor devices and fabrication technologies.

106. As reflected in my curriculum vitae (attached as Appendix 1), my expertise met or exceeded a POSITA's as of July 2012.

107. In view of the types of problems encountered in the art and prior art solutions to those problems, it is my opinion that a POSITA with the level of skill described above would have been familiar with the following:

- Floating gate flash memory technology (*see* Part III.C.2);
- The structure and composition of SONOS-type memory devices (*see* Part III.C.3, above);
- SONNOS and SONONOS configurations of SONOS-type memory devices (*see* Parts III.C.4 and 5, above);

- Vertically-oriented configurations of SONOS-type memory transistors (*see* Part III.C.6); and
- The use of high work function materials, such as p+ doped polysilicon, to form gate electrodes for SONOS-type memory devices (see Part III.C.7).

VII. CLAIM CONSTRUCTION

108. For purposes of this declaration, I have considered the claim language, specification, and prosecution history to determine the meaning of the claim language as it would have been understood by a POSITA at the time of the invention.

A. "oxygen-rich nitride" and "oxygen-lean nitride"

109. Independent claims 1, 12, and 16 of the '240 patent each recite that "the first dielectric layer includes oxygen-rich nitride, and the second dielectric layer includes oxygen-lean nitride."

110. The '240 patent does not expressly define the boundaries of what is an "oxygen-rich nitride" or "oxygen-lean nitride." But the '240 patent states, with respect to the figure 6 embodiment only, that:

> By oxygen-rich it is meant wherein a concentration of oxygen in the oxygen-rich first nitride layer 616a is from about 15 to about 40%, whereas a concentration of oxygen in [an] oxygen-lean second nitride layer 616b is less than about 5%.

Ex. 1001 ('240 patent), 13:53-57.

111. Regardless of the outer boundaries of "oxygen-lean nitride" and "oxygen-rich nitride," a POSITA would have understood, based on the figure 6 embodiment, that (i) a layer including a nitride with about 5% or less oxygen is within the bounds of "oxygen-lean nitride"; and (ii) a layer including a nitride with about 15% or more oxygen is within the bounds of "oxygen-rich nitride."

B. "high work function gate electrode"

112. Independent claims 12 and 16 (and dependent claims 9 and 11) of the '240 patent require a "high work function gate electrode." This term was well-known to a POSITA prior to July 2012. *See* Part III.C.7 (providing numerous examples of "high work function" gate electrodes, including p+ doped polysilicon and metal gates).

113. The '240 patent does not define "high work function gate" in a way that departs from the common understanding of that term. To the contrary, the specification confirms that, "[b]y high work function gate electrode it is meant that the minimum energy needed to remove an electron from the gate electrode is increased." Ex. 1001 ('240 patent), 4:1-3. The '240 patent also gives the following examples of "high work function":

> In one embodiment, the polysilicon layer 216 is doped following the growth or formation in the LPCVD process using ion implantation process. For example, the polysilicon layer 216 can be doped by implanting boron

> (B^+) or BF_2 ions at an energy of from about 5 to about 100 kilo-electron volts (keV), and a dose of from about 1e14 cm^{-2} to about 1e16 cm^{-2} to form an N-type (NMOS) SONOS memory transistor and, preferably, a P-type (PMOS) logic transistor having high work function gate electrodes.

Ex. 1001 ('240 patent), 7:27-35. Dependent claim 11 also specifies that "high work function gate electrode comprises a P+ doped polysilicon layer." *Id*., claim 11.

114. As such, POSITA would have understood "high work function gate electrode" in the context of the '240 patent to have its ordinary meaning and encompass gate electrodes comprised of, for example, polysilicon doped with p-type impurities, such as boron, as well as other materials known as high work function materials in the prior art. *See* Part III.C.7.

C. "semiconductor material structure"

115. Independent claims 12 and 16 and dependent claims 2-5, 14, 15, and 17 recite various limitations in relation to a "semiconductor material structure."

116. The claims do not set forth what makes up the "semiconductor material structure." While the '240 patent's specification explains that a substrate may be formed of a "semiconductor material" (Ex. 1001 ('240 patent), 4:45-52) it does not explicitly set forth what else, if anything, would be included in a "semiconductor material structure."

117. As an initial matter, it is my understanding that, during the prosecution of a descendent of the ’240 patent, Applicants stated that:

> the words and phrases “memory device” and “semiconductor material structure,” as used throughout the present claims and application are synonymous with the words and phrases “memory transistor” and “semiconductor substrate” - which are explicitly supported in connection with figures 3 and 8-10, in the above cited paragraphs.

Ex. 1053 (’336 Pros. Hist.), 137). Thus, a POSITA would take Applicants at their word – that “semiconductor material structure” means “semiconductor substrate.”

118. This understanding is also consistent with how “semiconductor material structure” is used in the claims of the ’240 patent.

119. For example, independent claims 12 and 16 (and dependent claim 5) each recite that “the channel is vertical and oriented substantially perpendicular to a semiconductor material structure.” The only embodiment of the ’240 patent that shows the orientation of a vertical channel *vis-à-vis* a substrate is the figure 9 embodiment, reproduced below.

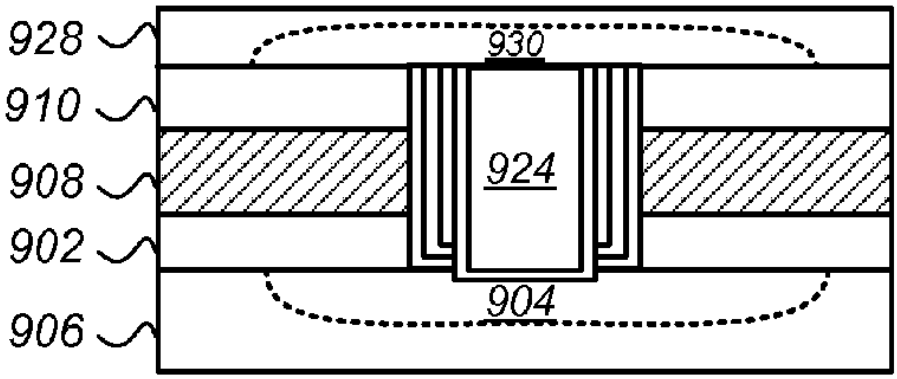


FIG. 9F

120. In the figure 9 embodiment, vertical channel 924 is oriented perpendicular to substrate 906, passing through dielectric layers 902, 910 and gate electrode 908. Ex. 1001 (’240 patent), 18:9-22.

121. The claims also recite the position of a “MOS logic device” relative to the “semiconductor material structure” (e.g., claim 14’s “the MOS logic device is formed at least partially within a semiconductor material structure” and claim 17’s “the MOS logic device is formed at least partially on the semiconductor material structure”). The only example of a MOS logic device arranged *vis-à-vis* a substrate is shown in the figure 3 embodiment of the ’240 patent, reproduced below.

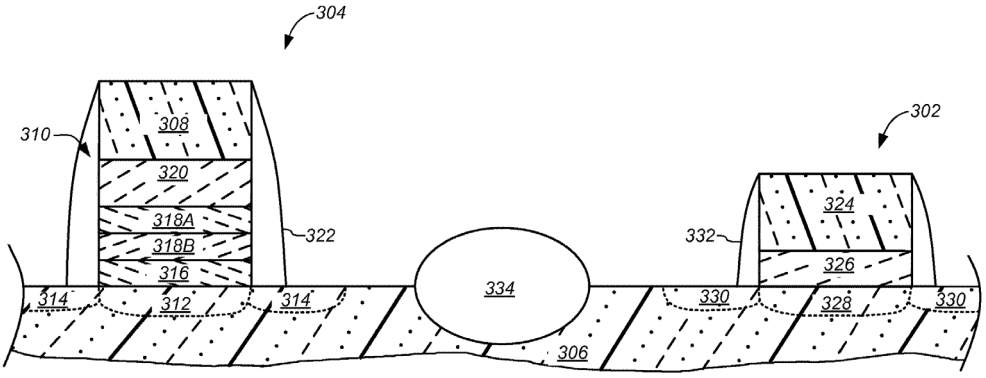


FIG. 3

122. In this embodiment, logic transistor 302, which includes gate electrode 324, oxide layer 326 and channel region 328 and source/drain regions 330 formed in substrate 306, is formed both partially within and partially on substrate 306.

123. Further, the claims also recite the position of channel and diffusion regions relative to the "semiconductor material structure" (e.g., claim 2's "wherein the channel, first and second diffusion regions are formed at least partially within a semiconductor material structure," claim 3's "wherein the channel, first and second diffusion regions are disposed above a semiconductor material structure," and claim 4's "wherein the channel, first and second diffusion regions are suspended above a semiconductor material structure").

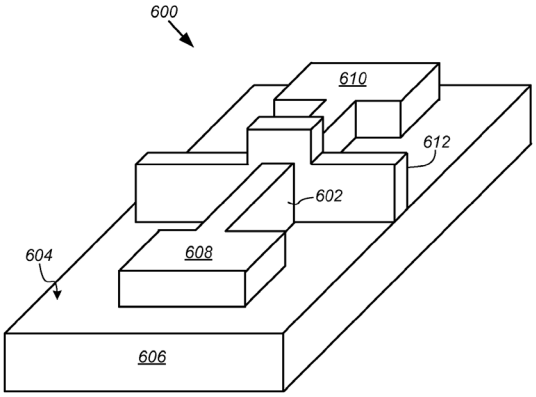


FIG. 6A

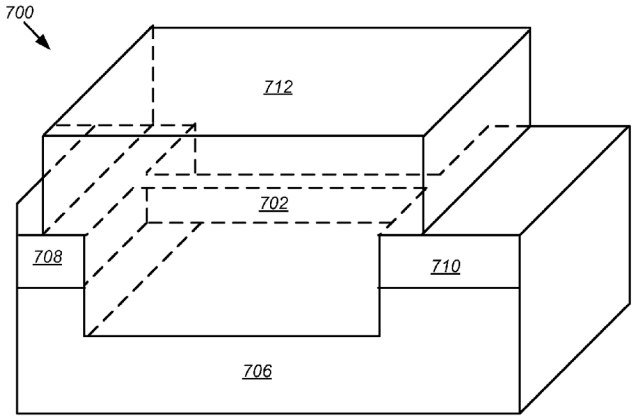


FIG. 7A

124. The figure 3 embodiment reproduced above portrays a source, drain, and channel formed "at least partially within" substrate 306 as discussed above. And the figure 6A and 7A embodiments show sources (608, 708), drains (610, 710), and channels (602, 702) formed "above" and "suspended above" substrates 606, 706, respectively.

125. In view of the foregoing, a POSITA would have considered "semiconductor material structure" to mean semiconductor substrate. I understand that this construction is consistent with the interpretation of "semiconductor material structure" that Patent Owner has advanced in parallel litigation. *See* Ex. 1054 (Infringement Contentions), 000018 (equating a silicon substrate with a "semiconductor material structure").

VIII. SUMMARY OF ASSERTED PRIOR ART

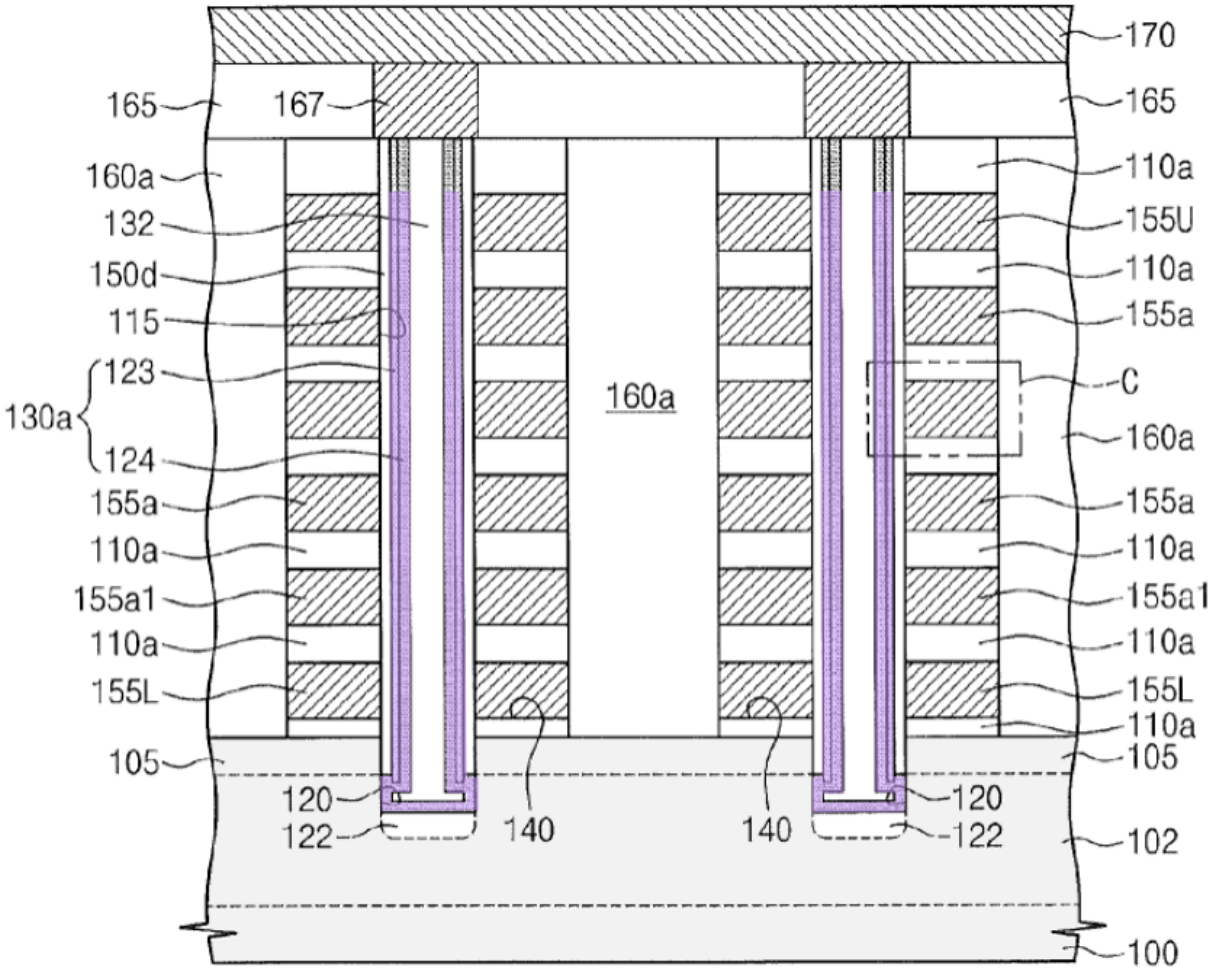
126. As is evident from the background provided above, there are many prior art patents and publications that teach the features of the '240 patent. Multiple pre-2012 references already taught ONNO/ONONO stacks, oxygen-rich and oxygen-lean nitride layering, anti-tunneling oxides, high-work-function gates, and the integration of memory and MOS logic transistors on the same substrate, all as routine techniques for balancing retention, program/erase speed, and CMOS compatibility. Along with the materials discussed in the background and listed in Appendix 2, I have reviewed and considered the following prior art in forming my opinions in this matter.

A. Lee '255 (Exhibit 1004)

127. Lee '255 (Exhibit 1004) is a copy of U.S. Patent Application Publication 2012/0068255, entitled "Three-Dimensional Semiconductor Memory Devices." Lee was published on March 22, 2012, from an application filed on August 29, 2011. Lee identifies three inventors: Changhyun Lee, Byoungkeun Son, and Hyejin Cho. I understand that Lee '255 is considered prior art to the challenged claims because it was filed by another and published before July 1, 2012.

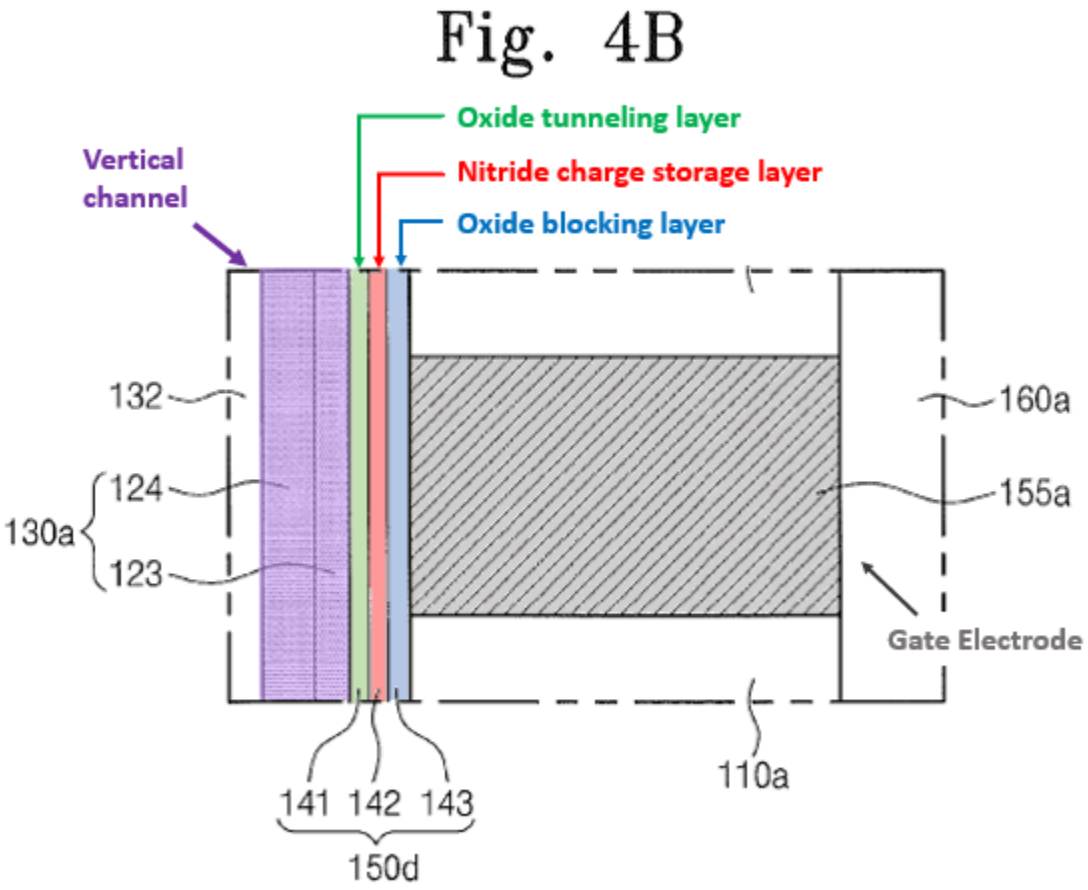
128. I understand that Lee '255 was not cited or considered during prosecution of the '240 patent.

129. Lee ’255 teaches “a semiconductor device and a method of fabricating the same and, more particularly, . . . a three-dimensional (3D) semiconductor memory device.” Ex. 1004 (Lee ’255), [0002]-[0004]. For example, the 3D memory device depicted in figure 4A (annotated below) includes a vertical channel 130a (purple) that passes through a stack of layers (110a, 155L, 155a, 155U) formed over a substrate 100 (gray). *Id.*, [0052]-[0054], [0063].



Ex. 1004 (Lee), FIG. 4A.

130. To store charges, Lee '255 teaches that a gate dielectric layer 150d is formed to surround the vertical channel 130a. The gate dielectric layer 150d includes an oxide tunneling layer 141 (green), a nitride charge storage layer 142 (red), and an oxide blocking layer 143 (blue), as shown in this annotated version of figure 4B:



Ex. 1004 (Lee '255), Fig. 4B, [0057], [0074].

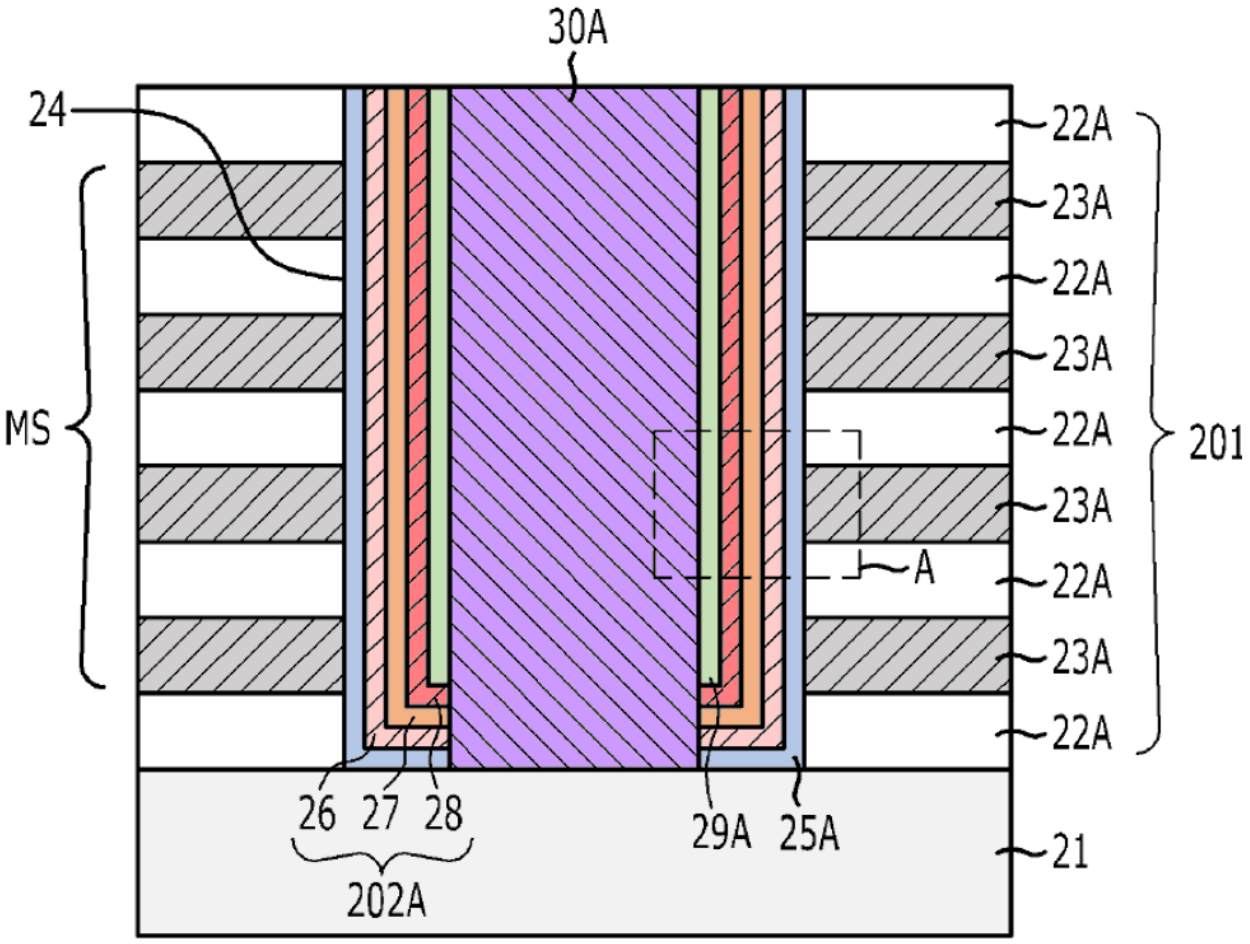
131. A POSITA would have understood that Lee '255 is analogous art to the '240 patent because it teaches improvements to non-volatile memory devices generally, and charge trap memory devices specifically.

B. Lee ’961 (Exhibit 1005)

132. Lee ’961 (Exhibit 1005) is a copy of Korean Patent Publication No. 2011-0118961, entitled “Non-Volatile Memory Devices and Methods of Making Them,” and the certified English translation of the same. Lee ’961 was published on November 2, 2011, from an application filed on April 26, 2010. Lee ’961 identifies three inventors: Gi Hong Lee, Jae Hyung Koo, and Beom Yong Kim. I understand that Lee ’961 is considered prior art to the challenged claims because it was published before July 1, 2012.

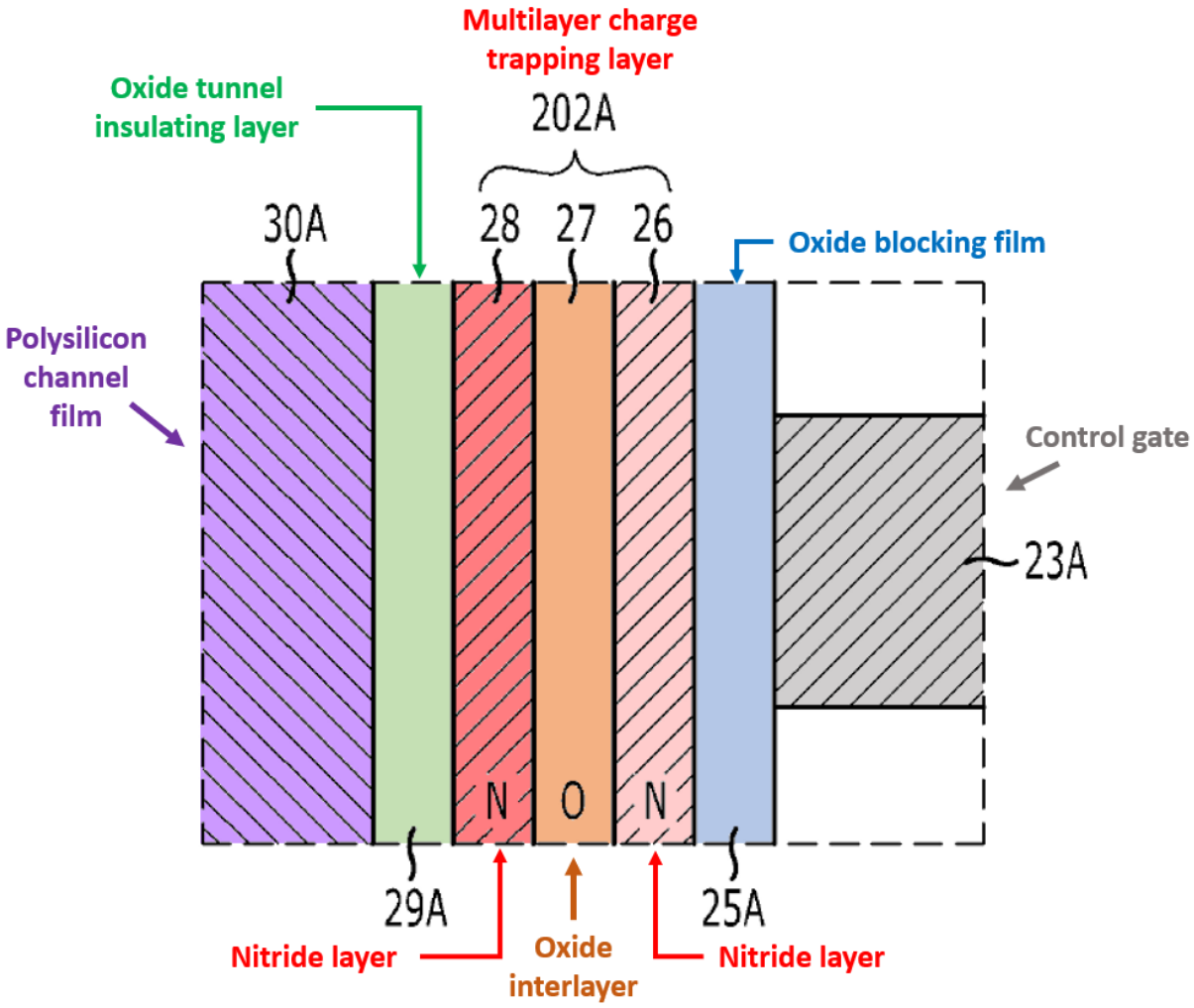
133. I understand that Lee ’961 was not cited or considered during prosecution of the ’240 patent.

134. Lee ’961 teaches a 3D charge trap memory device with a stack of layers (201) formed over a substrate (21) as shown in annotated figure 2a below. The stack including alternating insulating layers (22A) and gate electrodes (23A):



Ex. 1005 (Lee ’961), Fig. 2a, [0017]-[0019].

135. As reflected above, Lee ’961 teaches a vertical 3D structure where a polysilicon channel is surrounded by a tunnel insulating layer 29A (silicon oxide), multilayered charge trap layer 202A, and blocking film 25A (silicon oxide). Ex. 1005 (Lee ’961), [0017]-[0019]. As shown in annotated figure 2b below, multilayer charge trap layer 202A includes nitride layer 28, oxide interlayer 27, and nitride layer 26:



Ex 1005 (Lee '961), Fig. 2b, [0020].

136. A POSITA would have understood that Lee '961 is analogous art to the '240 patent because it teaches improvements to non-volatile memory devices generally, and charge trap memory devices specifically.

C. Fujiwara (Exhibit 1006)

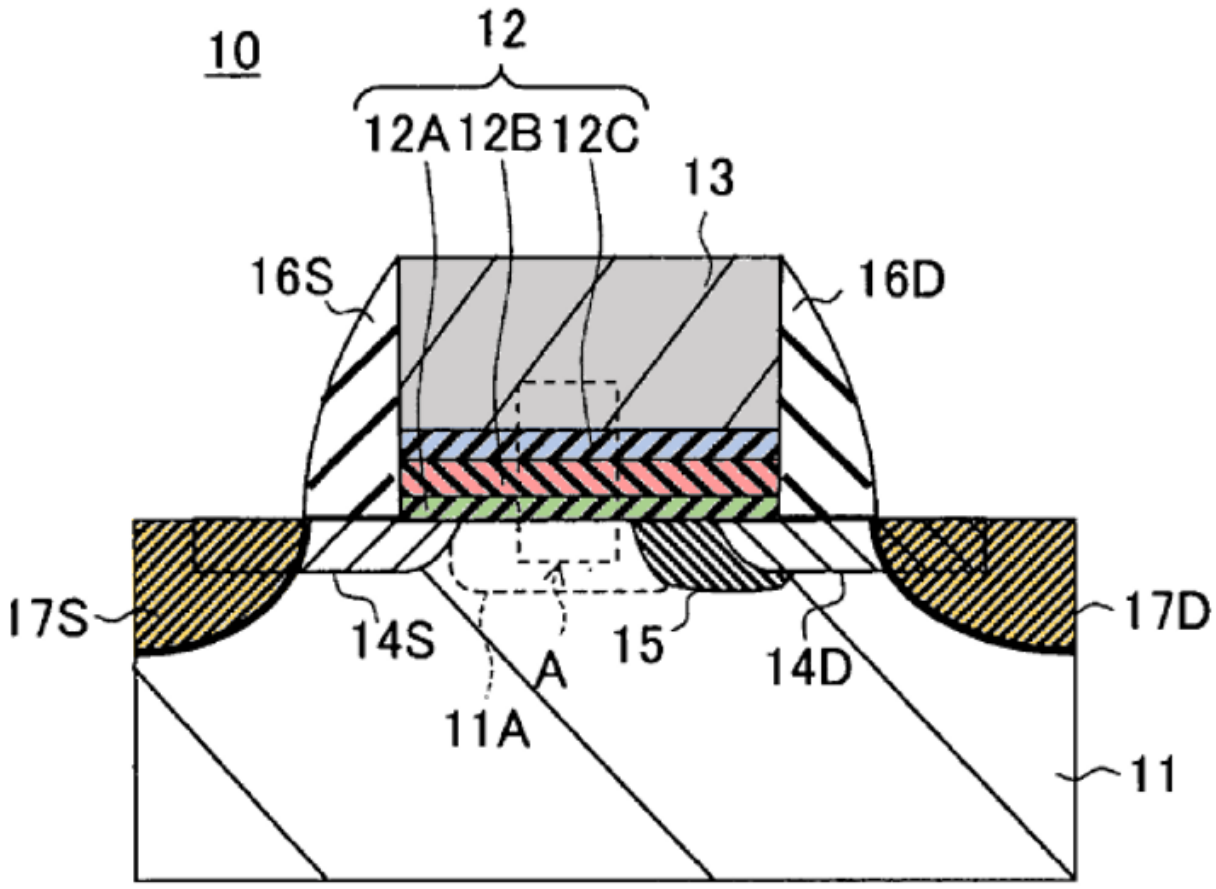
137. Fujiwara (Exhibit 1006) is a copy of U.S. Patent Publication 2006/0065919 A1, entitled "Nonvolatile Memory Device and Method for Producing the Same." Fujiwara was published on March 30, 2006, from an

application filed on September 16, 2005. Fujiwara identifies a single inventor, Ichiro Fujiwara. I understand that Fujiwara is considered prior art to the challenged claims because it was published more than one year prior to July 1, 2012.

138. I understand that Applicants listed Fujiwara on an information disclosure statement submitted during the prosecution of the '240 patent, along with more than 500 other references Applicants listed on such statements. I understand that the Examiner did not cite or apply Fujiwara in any Office Action, nor provide any substantive analysis of Fujiwara in allowing the claims of the '240 patent. *See* Part III.C.

139. Fujiwara teaches a charge-trapping memory transistor with multiple nitride layers that provide improved data retention characteristics. Ex. 1006 (Fujiwara), [0037]-[0038], [0197], [0220].

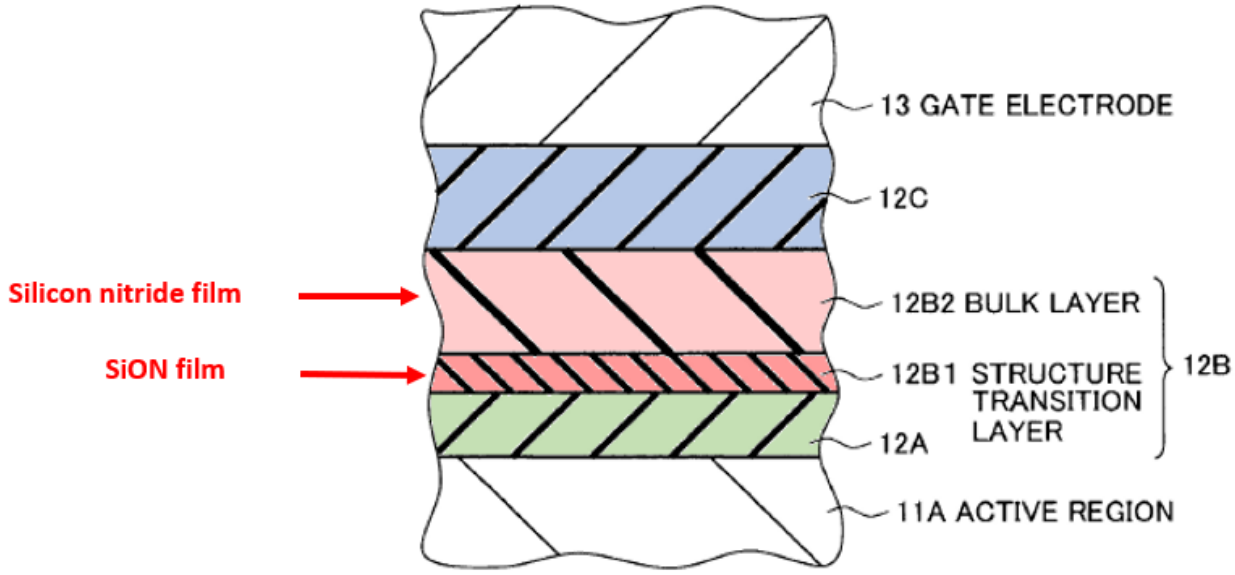
140. For example, in figures 2, 21, and 22, Fujiwara teaches a memory transistor with: (i) semiconductor substrate 11 with source 17S and drain 17D; (ii) first/bottom silicon oxide film 12A; (iii) silicon nitride charge storage layer 12B; (iv) second/top silicon oxide film 12C; and (v) gate 13:



Ex. 1006 (Fujiwara), Fig. 2, [0072]-[0084], [0146]-[0154].

141. In figure 21, Fujiwara teaches that the silicon nitride charge storage layer 12B can be made of two nitride layers – lower SiON structure transition layer 12B1 and upper SiN_x charge storage layer 12B2, where the SiON structure transition layer 12B1 is provided to: (i) improve the film quality of layer 12B; and (ii) improve data retention characteristics.

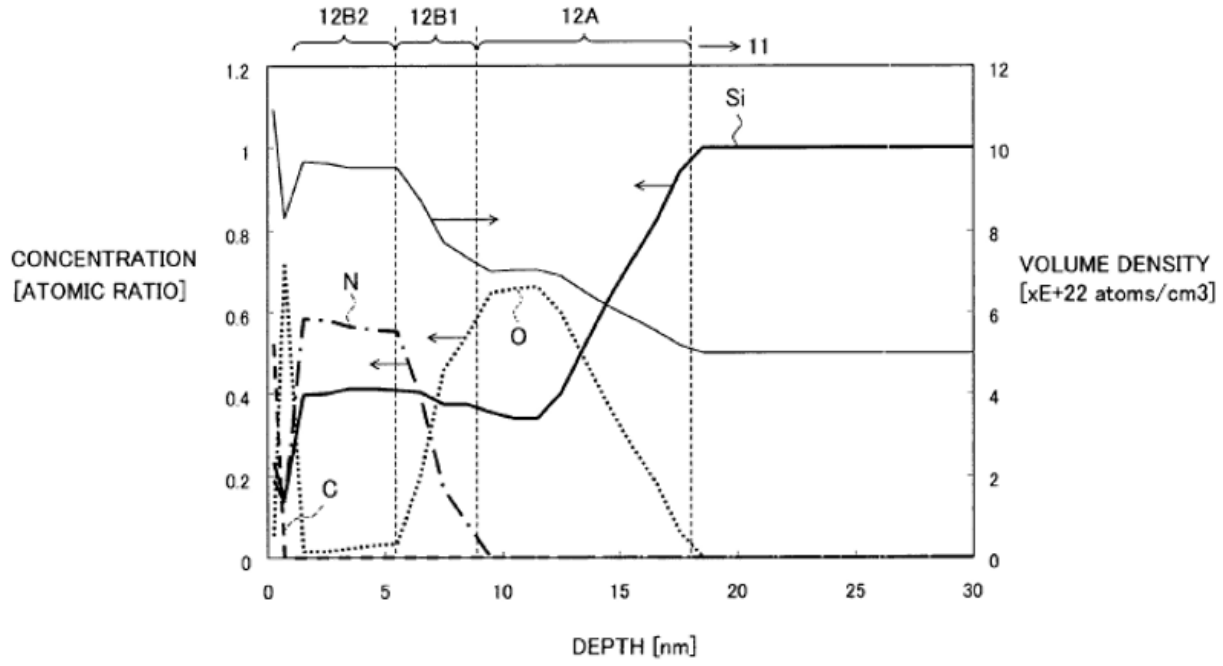
FIG. 21



Ex.1016 (Fujiwara), Fig. 21, [0197]-[0208].

142. Figure 22 of Fujiwara teaches the relative oxygen (O), nitrogen (N), and silicon (Si) concentrations in each layer. Figure 22 teaches that layer 12B2 is silicon-rich (e.g., ~40% concentration through its thickness) and oxygen lean (e.g., less than about 5% throughout its thickness). Figure 22 further teaches that layer 12B1 is oxygen-rich, with atomic concentrations reaching about 50%.

FIG. 22



Ex. 1006 (Fujiwara), Fig. 22, [0200].

143. A POSITA would have understood that Fujiwara is analogous art to the '240 patent because it teaches improvements to non-volatile memory devices generally, and charge trap memory devices specifically.

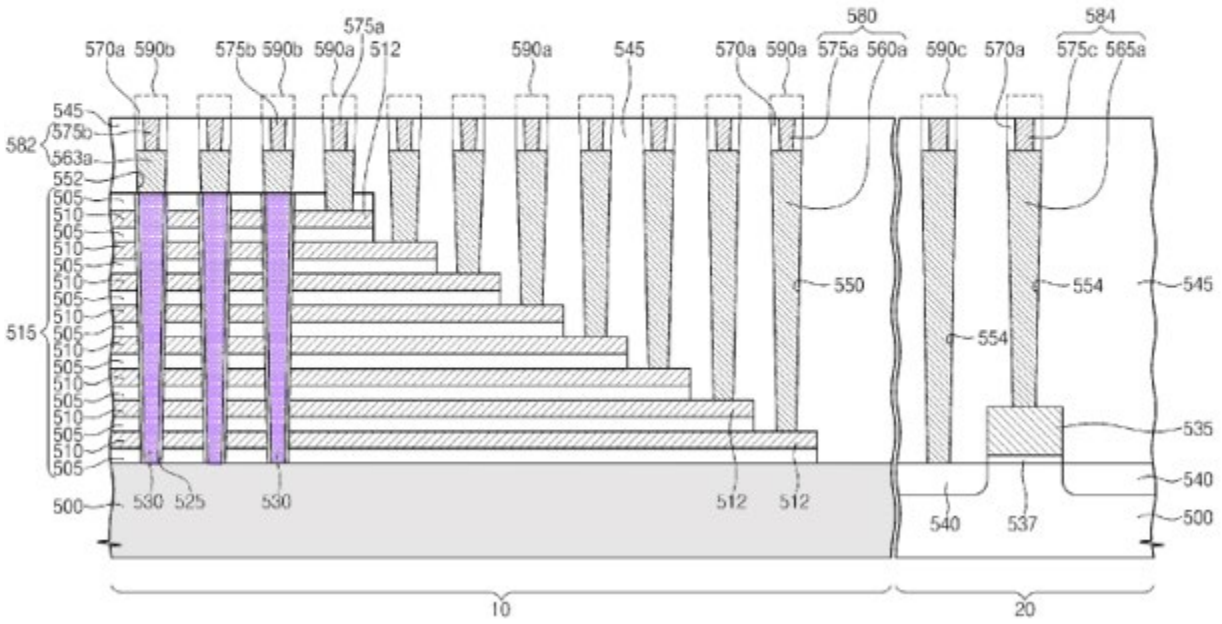
D. Hwang (Exhibit 1048)

144. Hwang (Exhibit 1048) is a copy of U.S. Patent Application Publication 2012/0061744, entitled "Three-Dimensional Semiconductor Memory Devices." Hwang was published on March 15, 2012, from an application filed on September 9, 2011. Hwang identifies five inventors: Sung-Min Hwang, Hansoo Kim, Changseok Kang, Wonseok Cho, and Jae-Joo Shim. I understand that

Hwang is considered prior art to the challenged claims because it was filed by another and published before July 1, 2012.

145. Hwang teaches "three-dimensional semiconductor memory devices." Hwang (Ex. 1048), [0007]. For example, the 3D memory device depicted in figure 6 (annotated below) includes a vertical channel 530 (purple) that passes through an alternating stack of insulating (505) and gate (510) patterns formed over a substrate 500 (gray).

Fig. 6



Ex. 1048 (Hwang), Fig. 6, [0112].

146. To store charges, Hwang teaches that data storing layers 525 are provided, which include an oxide tunneling dielectric layer, a nitride charge storing layer, and an oxide blocking dielectric layer. *Id.*, [0047], [0112].

147. Hwang's figure 6 embodiment also provides detail regarding the electrical connections for gate patterns 510 and vertical channels 530 that allow its 3D memory device to function. In this embodiment, each gate layer is electrically connected to first contact portion 560a and second contact portion 575a via a pad portion 512 that extends laterally beyond the gate layer above, forming a "step structure." *Id*., [0116]. Hwang also teaches the provision of MOS logic transistors in peripheral circuit region 20 and the electrical connections thereto. *Id*., [0112]-[0113]. Figure 6 shows such a MOS logic transistor made up of peripheral gate 535, peripheral gate dielectric layer 537, peripheral source/drain regions 540 formed in the substrate, and an unlabeled channel between source/drain regions 540. *Id*.

148. I understand that Hwang was not cited or considered during prosecution of the '240 patent.

149. A POSITA would have understood that Hwang is analogous art to the '240 patent because it teaches improvements to non-volatile memory devices generally, and charge trap memory devices specifically.

IX. ANALYSIS OF INVALIDITY GROUNDS

150. Based on my review and analysis of the materials cited herein, my opinions regarding the understanding of a POSITA before July 1, 2012, and my

training and experience, it is my opinion that the challenged claims of the '240 patent are invalid based on the following grounds:

Ground	Claims	Basis	Prior Art
1	1, 3-7, 9, 11	§ 103 Obviousness	Lee '255, Lee '961, Fujiwara
2	12-18	§ 103 Obviousness	Lee '255, Lee '961, Fujiwara, Hwang

A. Ground 1: Obviousness over Lee '255, Lee '961, and Fujiwara

151. It is my opinion that claims 1, 3-7, and 9-11 of the '240 patent are rendered obvious based on the teachings of Lee '255, Lee '961, and Fujiwara.

152. Lee '255 teaches a 3D vertical SONOS charge trap-type nonvolatile memory device. Ex. 1004 (Lee '255), Figs. 4A, 4B, [0003]. As discussed below, Lee '255 teaches most of the limitations found in the challenged claims, including, (i) a high work function gate electrode; (ii) a vertical channel; (iii) an ONO stack along the channel that includes a tunnel dielectric layer, a nitride charge trapping layer, and a blocking dielectric layer; and (iv) a MOS logic device. *See id.*, e.g., [0050]-[0074].

153. Lee '961 also teaches a 3D vertical SONOS charge trap-type nonvolatile memory device. Ex. 1005 (Lee '961), [0002]-[0006]. Lee '961 teaches that prior art 3D memory devices similar to the device taught in Lee '255 can suffer from leakage of charges. *Id.*, Fig. 1, [0006]. To provide improved data

retention properties, Lee '961 teaches modifying prior art devices to include a SONONOS configuration with a "multilayered charge trap layer"—"[t]he present invention described above has the effect of improving data retention properties of non-volatile memory devices by applying a multilayered charge trap layer comprising a plurality of trap layers and interlayers." Ex. 1005 (Lee '961), [0010]; *see also id.*, [0012], [0015], [0017], [0020].

154. Fujiwara, like Lee '255 and Lee '961, relates to SONOS charge trapping-type nonvolatile memory devices. Ex. 1006 (Fujiwara), [0003] ("The present invention relates to a nonvolatile memory device provided with a metal-oxide-nitride-oxide semiconductor (MONOS) type").[6] Fujiwara, like Lee '961, teaches that retention in charge-trapping type memory devices can be improved by using the multilayer charge storage layer configuration shown in its figure 21. Ex. 1006 (Fujiwara), [0197], [0205]. In particular, Fujiwara teaches that using an oxygen-rich lower nitride layer and an oxygen-lean upper nitride layer promotes charge retention. Ex. 1006 (Fujiwara), [0197]-[0218], Figs. 21, 22.

[6] A POSITA would have understood that "MONOS" (Metal-Oxide-Nitride-Oxide-Silicon) and "SONOS" (Silicon-Oxide-Nitride-Oxide-Silicon) are equivalent types of metal-oxide-semiconductor field effect transistors (MOSFET) with the primary distinction being the material used for the gate electrode (metal versus silicon). *See*, *e.g.*, Ex. 1012 (Lukasiak), 000006.

155. As discussed below, a POSITA would have been motivated to modify the nitride charge trapping layer of Lee '255 to incorporate the "multilayered charge trap layer" configuration disclosed in Lee '961 to achieve the performance benefits that Lee '961 expressly attributes to that structure—namely, improved data retention and suppression of charge spreading. A POSITA would have been motivated to further modify the combination of Lee '255 and Lee '961 in view of Fujiwara's teachings concerning optimized oxygen concentrations when using multiple nitride layers (e.g., like those of the Lee '255 / Lee '961 combination) in a charge-trapping nonvolatile memory device to provide the further retention benefits taught by Fujiwara. It is my opinion that this combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claims 1, 3-7, 9 and 11 of the '240 patent.

156. A POSITA also would have expected success in implementing the multilayer charge-trap structure of Lee '961 and the oxygen concentration teachings of Fujiwara in the stack of Lee '255 because this combination could be accomplished with routine process modifications, using well-established deposition tools and parameters. I provide further details on this motivation to combine and expectation of success in connection with specific claim limitations below.

157. The combination of Lee ’255, Lee ’961, and Fujiwara presents a materially different teaching from the prior art considered during prosecution of the ’240 patent. Based on my review of the file history, I understand that the Examiner allowed claims 1, 12, and 16 (application claims 21, 33, and 38) based on his understanding that none of the prior art references of record disclosed: (i) a multi-layer charge trapping layer used with a vertical channel (application claims 33 and 38); or (ii) a multi-layer charge trapping layer that includes an anti-tunneling layer between nitride layers (application claim 21). Ex. 1002 (Pros. Hist.), 110-111. As I explain in more detail below, the combination of Lee ’255 (neither of record nor applied during prosecution), Lee ’961 (neither of record nor applied during prosecution), and Fujiwara (not applied during prosecution), teaches the structural features that the Examiner found missing. Together, these references disclose a multilayer charge-trapping region used with a vertical channel and including an anti-tunneling layer, as claimed in the ’240 patent.

1. Independent Claim 1

[1pre]	**A memory device, comprising:**

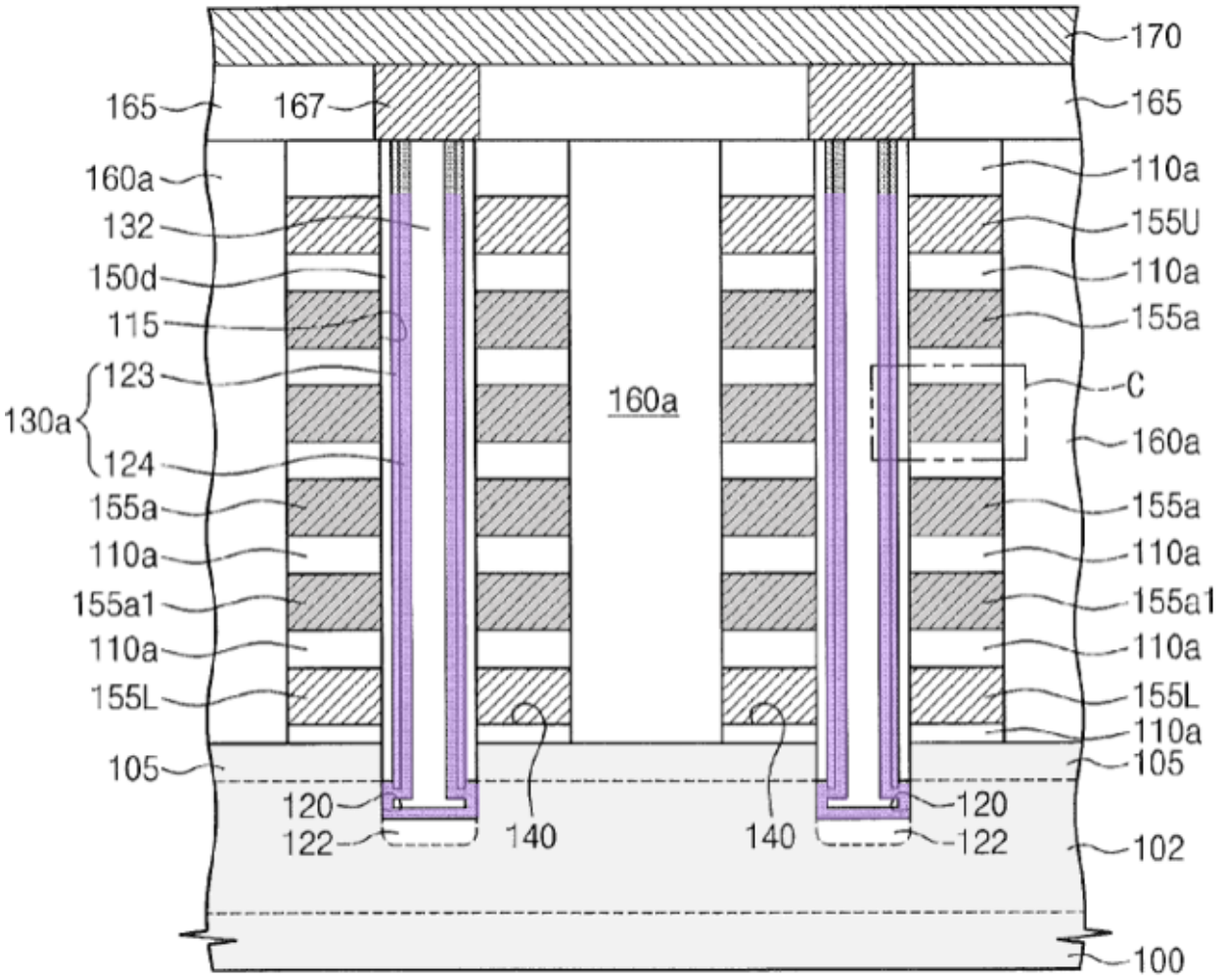
158. I understand that a preamble does not always limit the claim. *See* Appendix 4. To the extent Patent Owner argues this preamble is limiting, it is my opinion that Lee ’255 teaches *a memory device* because Lee ’255 teaches “a three-dimensional (3D) semiconductor memory device and a method of fabricating the

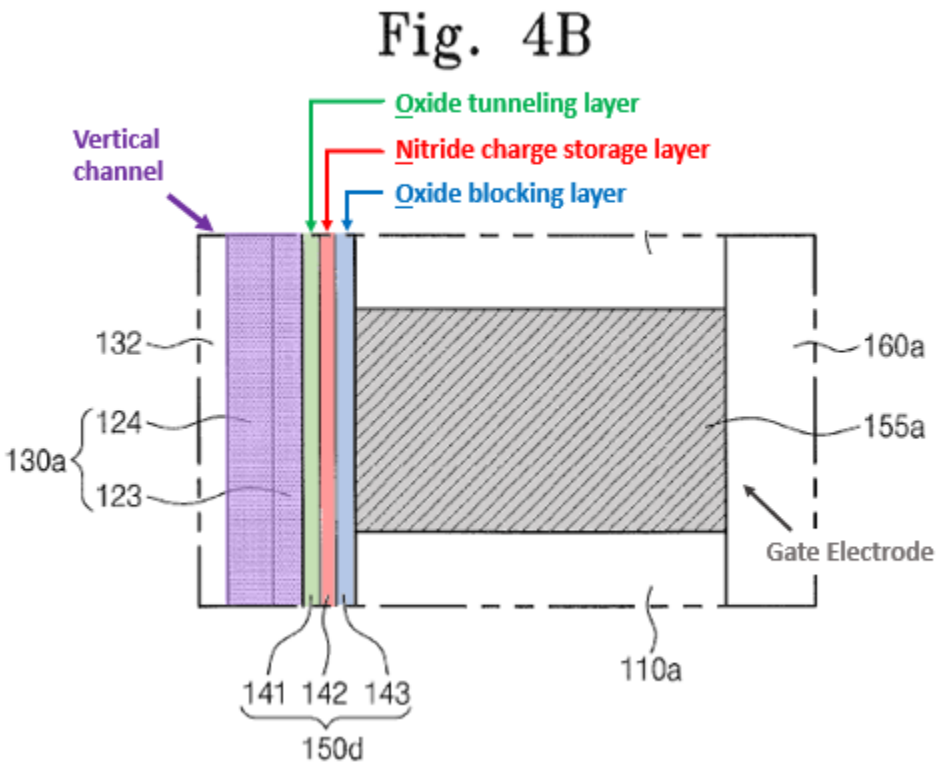
same." *See, e.g.*, Ex. 1004 (Lee '255), ¶[0002]; *see also, e.g., id.*, Abstract, Figs. 1A-5B, [0074] (teaching "3D semiconductor memory device").

[1a]	**a gate structure;**

159. It is my opinion that Lee '255 teaches limitation [1a] because it teaches that its memory device includes gate electrodes 155a (each *a gate structure*). Ex. 1004 (Lee '255), Figs. 1A, 4A, 4B, and 5A, [0051] (3D memory device includes "stack-structure, including insulation patterns 110a and gate patterns 155L, 155a1, 155a, and 155U that are stacked alternately and repeatedly"), [0055]-[0058], [0059] ("Gate patterns 155a1 and 155a between the uppermost gate pattern 155U and the lowermost gate pattern 155L may correspond to cell gates"), [0060].

160. The arrangement of gate electrodes 155a taught by Lee '255 is shown, for example, in annotated figures 4A and 4B (detail C in figure 4A) below, where the gates 155a are highlighted in dark gray shading:


170
165
167
165
160a
110a
132
155U
150d
110a
115
155a
123
130a
160a
C
124
160a
155a
155a
110a
110a
155a1
155a1
110a
110a
155L
155L
110a
105
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120
120
122
140
140
122
102
100



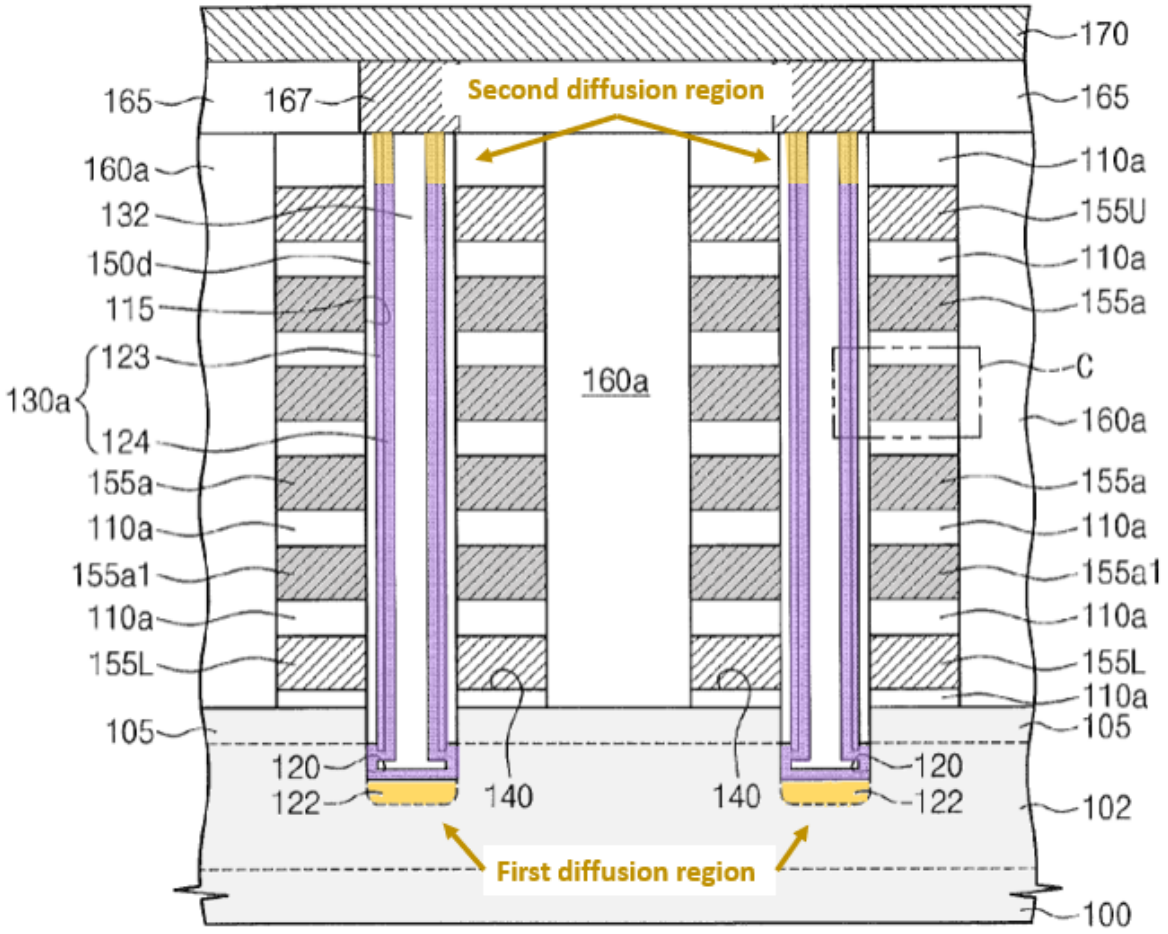
Ex. 1005 (Lee '255), Figs. 1A, 4A, 4B, [0051]-[0060], [0074].

[1b]	**a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and**

161. It is my opinion that Lee '255 teaches limitation [1b] for at least the following reasons.

162. Lee '255 teaches *a channel* because it teaches "**vertical channel regions** that are defined in the sidewall of vertical active pattern" 130/130a. Ex. 1004 (Lee '255), [0058], [0059]. These vertical active patterns 130/130a (channel) are arranged in the device so as to "pass through each of the stack-structures." *Id.*,

[0061]. This arrangement is shown, for example, in annotated figure 4A below, where the *channels* (vertical active patterns 130/130a) are shown in purple shading:



Ex. 1004 (Lee '255), Fig. 4A; *see also id.*, [0052].

163. Lee '255 teaches *a first diffusion region* because it teaches the provision of high concentration (i.e., heavily doped) regions 122. Ex. 1004 (Lee '255), FIG. 4A, 6B, [0053], [0067], [0081] ("[H]igh concentration region 122 may be formed by providing the first conductive dopant into the well region 102 through the bottom surface of the recess region 120. The high concentration

region 122 of the first conductive dopant may be higher than another portion of the well region 102."). This high concentration region 122 (*first diffusion region*) is shaded in gold and labeled in annotated figure 4A above.

164. Lee '255 teaches *a second diffusion region* because it teaches that a "drain being doped with the second conductive dopant may be formed in the upper portion of the vertical active pattern 130. A lower surface of the drain may be disposed on a level adjacent to an upper surface of the uppermost gate pattern 155U." Ex. 1004 (Lee '255), [0063]. This drain region (*second diffusion region*) is shaded in gold and labeled in annotated figure 4A above.

165. A POSITA would have understood that *diffusion regions*—e.g., sources and drains—are regions doped with conductive dopants so that charge carriers (electrons or holes) flow to or from those regions through a channel. *See, e.g.*, Ex. 1042 (Sze), 000016. The '240 patent confirms this understanding. *See, e.g.*, Ex. 1001 ('240 patent), 8:32-34 (diffusion regions are a source and drain separated from each other by a channel), 8:18-20 (identifying the source and drain regions as "heavily doped" and separated by the channel).

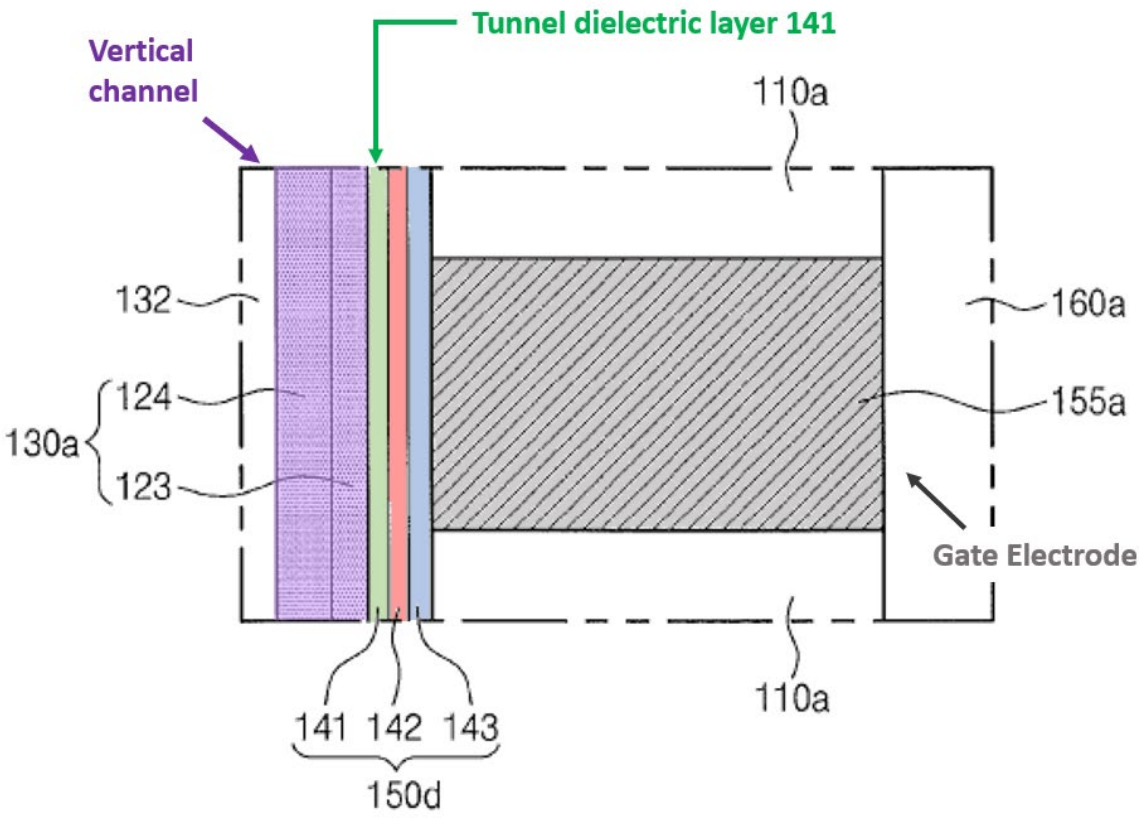
166. Lee '255 teaches that active patterns 130/130a are *positioned between and electrically connecting* high concentration regions 122 (*first diffusion region*) and drains (*second diffusion region*) because it teaches that the high concentration region 122, the active pattern 130/130a and the drain are physically arranged as

shown in figure 4A above and are formed of conductive materials and are connected for current flow. Ex. 1004 (Lee '255), [0064] ("a current flowing through the vertical active pattern 130"), [0053] ("the first **conductive** dopant concentration of the portion 122"), [0063] ("a drain being doped with the second **conductive** dopant"). A POSITA also would have understood these elements to be electrically connected because that is how a charge trapping memory device functions—i.e., electrons must flow in the vertical channel between the diffusion regions to permit tunneling of the electrons into the charge capture layers. *See, e.g.*, Ex. 1008 (Frohman-Bentchkowsky), 4:32-45; *see also* Part III.C.3 (explaining the operation of SONOS memory transistors). I also understand that Patent Owner has alleged that the same type of channel and diffusion regions taught in Lee '255 satisfy limitation [1b]. *See* Ex. 1054 (Infringement Contentions),[000010-000011].

[1c]	**a tunnel dielectric layer,**

167. It is my opinion that Lee '255 teaches limitation [1c] because it teaches that its "gate dielectric layer 150" includes "tunnel dielectric layer 141." Ex. 1004 (Lee '255), Fig. 4A/B, [0055]-[0057]. This arrangement is shown, for example, in the annotated version of Lee '255's figure 4B below, where the tunnel dielectric layer 141 (*tunnel dielectric layer*) is shaded in green:

Fig. 4B

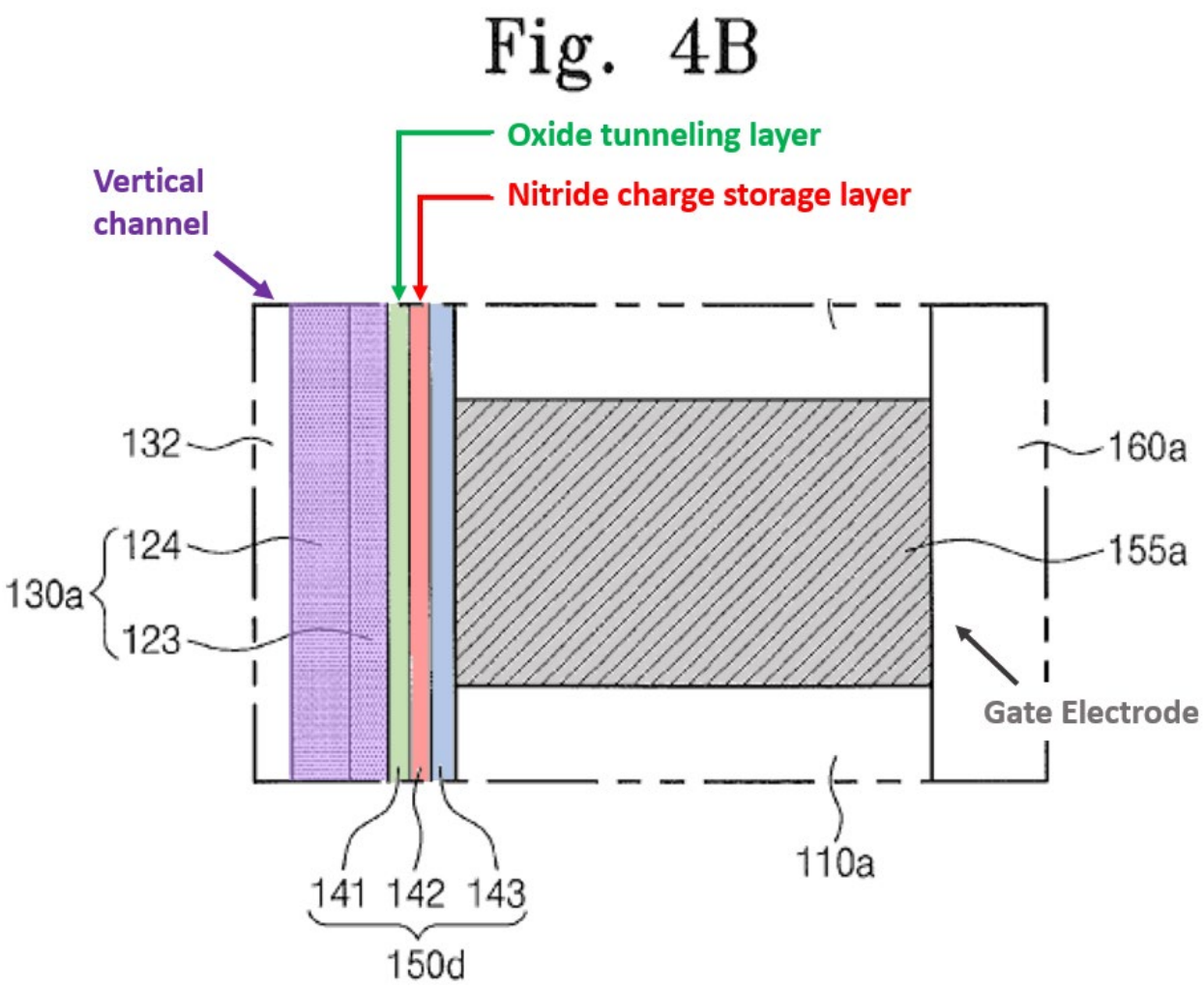


Ex. 1004 (Lee ’255), Figs. 4B.

[1d]	**a multi-layer charge trapping layer, and**

168. It is my opinion that the combination of Lee ’255 and Lee ’961 teaches limitation [1d]. As discussed below, Lee ’255 teaches a *charge trapping layer* (charge storage layer 142) and Lee ’961 teaches *a multi-layer charge trapping layer* to improve the operation of memory devices such as those taught in Lee ’255. A POSITA would have been motivated to modify Lee ’255’s charge storage layer based on Lee ’961’s multi-layer charge storing layer teachings.

169. Lee ’255 teaches a *charge trapping layer* because it teaches that its “gate dielectric layer 150” includes a nitride “charge storage layer 142.” Ex. 1004 (Lee ’255), Fig. 4B, [0055]-[0057]. Lee ’255 expressly teaches that this charge storage layer is for trapping charges. Ex. 1004 (Lee ’255), [0057] (“The charge storage layer 142 may include a dielectric material having traps for storing electric charges, for example, the charge storage layer 142 may include nitride and/or metal-oxide.”). Moreover, a charge “trapping” layer and charge “storage” layer would have been synonymous to a POSITA as those terms and concepts are used interchangeably in the prior art. *See* Part III.C. This nitride charge storage layer 142 is shaded in red in annotated figure 4B, below:

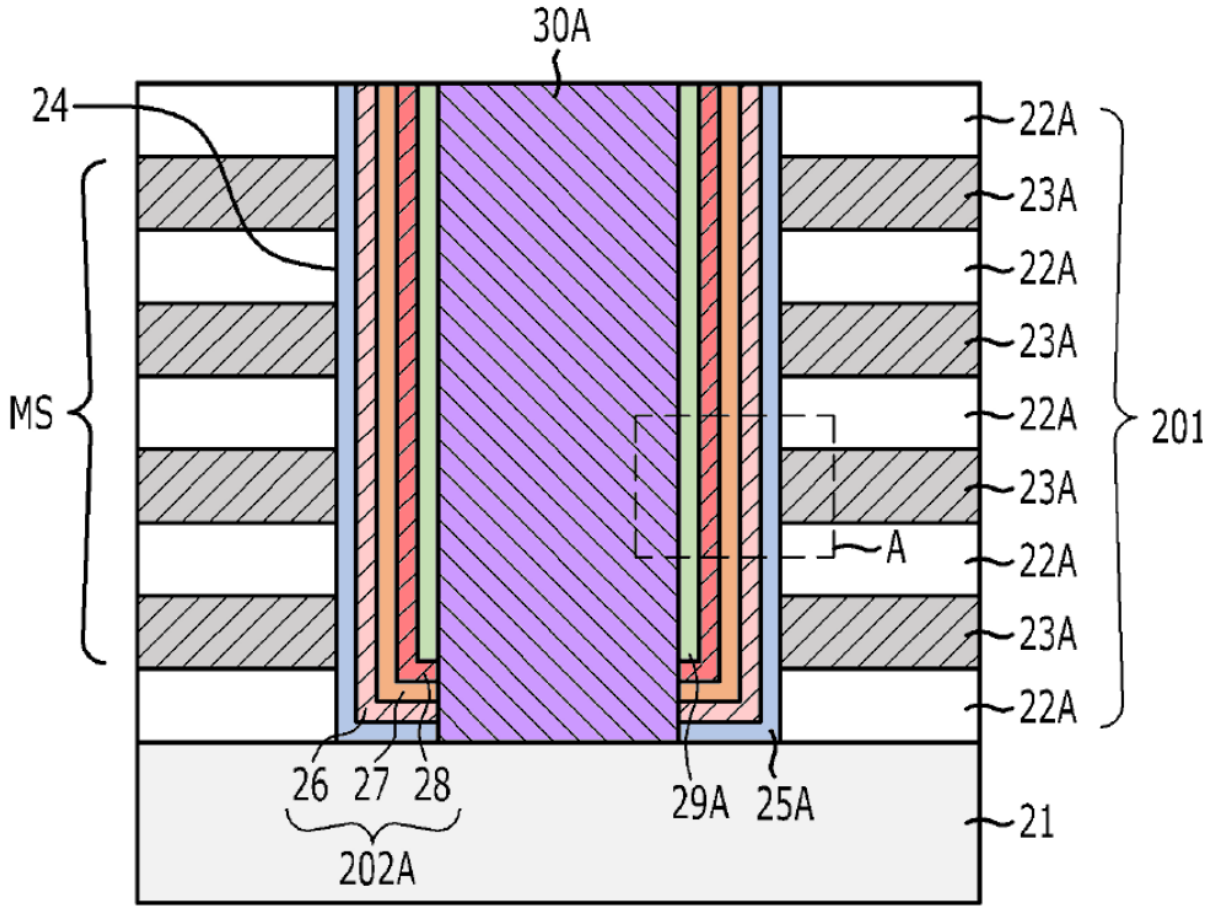


Ex. 1004 (Lee '255), Figs. 4B, *see also id.*, [0055]-[0057], [0074]-[0075].

170. While figure 4B of Lee '255 depicts a "gate dielectric layer 150d" with three layers (141-143), Lee '255 teaches that the structure is compatible with additional layers. For example, Lee '255 teaches incorporating additional oxide or oxynitride layers. Ex. 1004 (Lee '255), [0057].

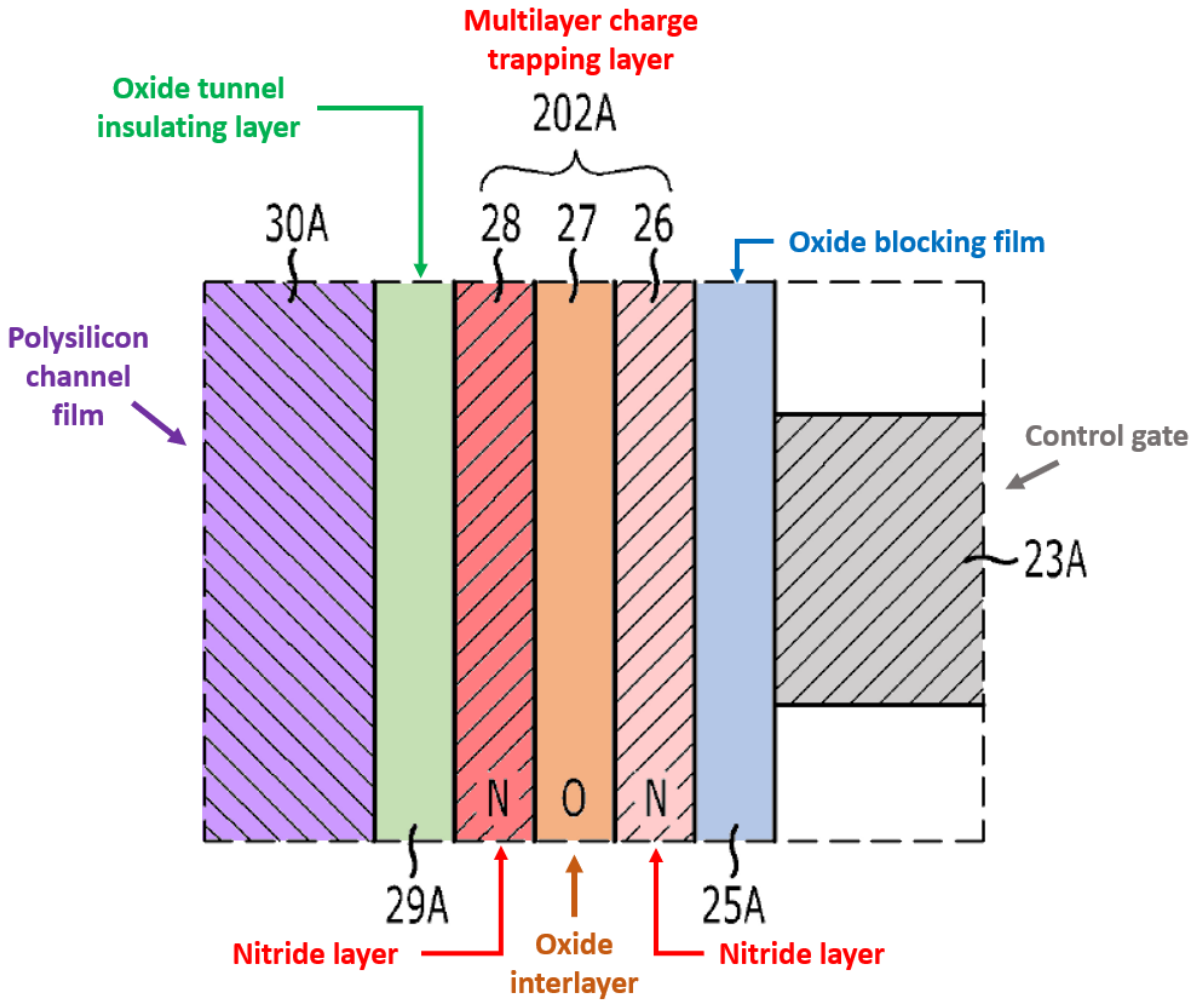
171. Lee '961 teaches a "multilayered charge trap layer" 202A (*a multi-layer charge trapping layer*) that "improv[es] the data retention properties of non-volatile memory devices" such as the device of Lee '255. Ex. 1005 (Lee '961),

[0008], [0010]. Fig. 2a of Lee '961 depicts the vertical structure of its 3D memory device:



Ex. 1005 (Lee '961), FIG. 2a.

172. Lee '961's *multi-layer charge trapping layer* (multilayered charge trap layer 202A) is further depicted in figure 2b, which is a magnified view of box "A" from figure 2a:



Ex. 1005 (Lee '961), Figures 2b, [0013], [0018]-[0021].

173. Like Lee '255, Lee '961 teaches that the charge trapping layer is positioned between a tunneling dielectric layer (green) and a blocking dielectric layer (blue). Ex. 1005 (Lee '961), FIGS. 2a, 2b, [0017]-[0019]. Lee '961 teaches that "[t]he charge trap layer 202A has a multilayer structure" (*a multi-layer charge trapping layer*). Ex. 1005 (Lee '961), [0020]. For example, the multilayer charge trap layer 202A may include a nitride first trap layer 26, an oxide interlayer 27, and a nitride second trap layer 28. Ex. 1005 (Lee '961), [0020]; *see also id.*, [0015].

174. A POSITA would have been motivated to modify Lee '255's charge trapping layer to incorporate a multilayer charge trapping layer based on the teachings of Lee '961.

175. It would have been obvious for a POSITA to consult the teachings of Lee '961 in seeking to improve the memory transistor configuration of Lee '255 because both Lee '961 and Lee '255 are directed to improving the operation of SONOS-type charge trapping memory transistors. Indeed, Lee '255 mirrors the type of devices that Lee '961 seeks to improve. *Compare* Ex. 1004 (Lee '255), Fig. 4A *with* Ex. 1005 (Lee '961), Fig. 1.

176. A POSITA would also have been motivated to apply Lee '961's ONONO stack teachings to the ONO stack of Lee '255 based on the express teachings, suggestion, and motivation to combine found in Lee '961. Specifically, Lee '961 teaches that SONOS configurations such as Lee '255's suffered from poor charge retention due to lateral spreading of charges in the single silicon nitride trapping film. Ex. 1005 (Lee '961), [0004]-[0006]. Lee '961 teaches that a solution to this problem is the multilayered charge trap layer (202A), which improves data retention. Ex. 1005 (Lee '961), [0010] ("The present invention described above has the effect of improving the data retention properties of non-volatile memory devices by applying a multilayered charge trap layer comprising a plurality of trap layers and interlayers.").

177. The data retention benefits of using the multilayer charge trapping region of Lee '961 also would have been predictable to a POSITA prior to July 2012. As set forth above in Parts III.C.4-6, using multilayer charge trapping structures was already a conventional strategy for improving retention prior to July 2012. *See* Parts III.C.4-6, above; *see also, e.g.*, Ex. 1010 (Nomoto), [0035], [0044]-[0045], [0073]-[0088] (teaching that a multi-layer charge trap with two nitride layers having different compositions (CS1, CS2) provides improved retention); Ex. 1011 (Levy), [0025]-[0026] (a multi-layer charge trap with an oxygen-lean top nitride layer and oxygen-rich bottom nitride layer "decrease[s] the charge loss rate after programming and after erase"); Ex. 1012 (Heo), [0058]-[0068] (teaching that using a bottom oxidized nitride layer with a top nitride layer improves "the data retention properties and/or durability of the non-volatile memory device"); Ex. 1006 (Fujiwara), Fig. 21, [0197]-[0208] (explaining retention benefits of using two nitride charge trapping layers); Ex. 1009 (Kim '399), [0034], [0046]-[0047] (teaching that use of bottom silicon oxynitride layer and top silicon nitride layer suppresses charge loss); Ex. 1013 (Ganguly), [0020], [0048]-[0049] (teaching that having lower nitride layer with up to 50% oxygen and an upper "silicon-rich silicon nitride" results in "increased retention"); Ex. 1017 (Lai '676), [0015], [0068]-[0077] (teaching that an NON charge trapping region with an upper silicon nitride layer 16, middle oxide layer 15, and lower

silicon oxynitride layer 14 improves retention); Ex. 1021 (Higuchi) [0007], [0133]-[0134], [0141]-[0142] (teaching that a NON charge trapping region with an upper silicon nitride layer 203, middle oxide layer 202d, and lower silicon oxynitride layer 203c improves retention); Ex. 1014 (Wang '586), [0006], [0022], [0031]-[0032] (teaching multi-layer charge storage structures including a silicon oxynitride bottom and nitrided silicon oxynitride top (figure 5) or a silicon oxynitride bottom and nitride top (figure 6) provides improved retention); Ex. 1020 (Arreghini) 000003 (figure 3), 000006 (teaching benefits of multi-layer charge trapping region). As such, applying the multilayer charge trapping region of Lee '961 to modify the charge trapping layer of Lee '255 would have amounted to (i) combining prior art elements according to known methods to yield predictable results; and (ii) use of known techniques to improve a similar device in the same way.

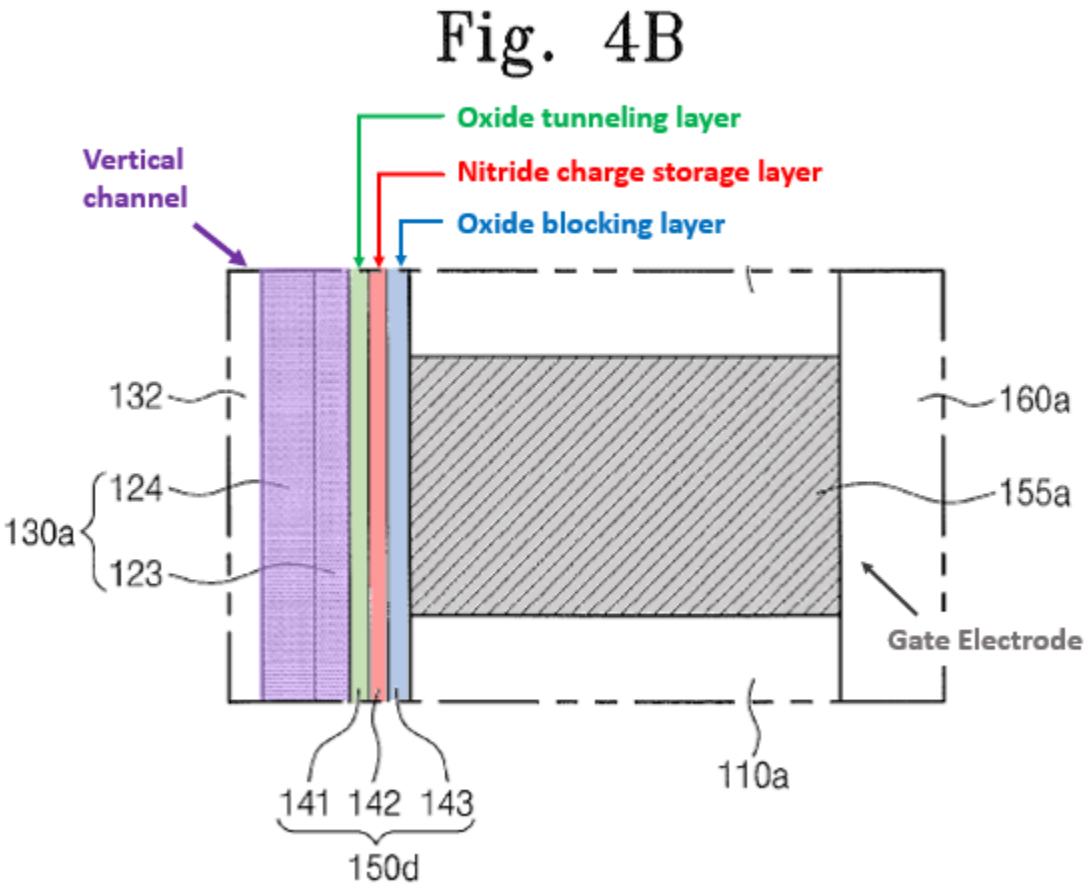
178. Applying the multilayer charge trap of Lee '961 to the memory device of Lee '255 also would have been obvious to try prior to July 2012. The selection of various trap configurations (e.g., ONO, ONNO, or ONONO) were routine design choices. *See* Part III.A.3-6. These alternatives represented a finite number of predictable options available to a POSITA to optimize charge trap memory devices.

179. A POSITA would have also had a reasonable expectation of success in modifying the memory device of Lee '255 based on the teachings of Lee '961 to incorporate a multilayer charge trapping region. Both Lee '255 and Lee '961 are directed to very similar 3D charge trap memory devices with common features: vertical channels, stacks of insulating and gate layers, tunneling oxides, charge trap layers, and blocking oxides. The memory structures in both references use similar materials and layouts and address similar technical challenges. *See* Part. III.C.3-6. As I noted above, Lee '961 expressly aims to improve the type of memory architecture used in Lee '255 by introducing a multilayer charge trap structure. Ex. 1005 (Lee '961), Fig. 1, [0002]-[0010]. Applying Lee '961's teachings of a multilayer charge trapping region to the structure of Lee '255 would have amounted to depositing additional layers as part of the fabrication process. This is an alternative that Lee '255 already contemplates. *See* Ex. 1004 (Lee '255), [0057]. Moreover, a POSITA would have understood that applying the teachings of Lee '961 to Lee '255 would involve using established techniques for material selection, layer formation, and stack integration that were routine and well-known to a POSITA prior to July 2012.

[1e]	**a blocking dielectric layer disposed between the gate structure and the channel,**

180. It is my opinion that Lee '255 teaches limitation [1e].

181. Lee ’255 teaches that the “gate dielectric layer 150d” includes an oxide “blocking dielectric layer 143” (*a blocking dielectric layer*). Ex. 1004 (Lee ’255), Fig. 4B, [0055]-[0057]. This arrangement is shown, for example, in annotated figure 4B below, where the blocking dielectric layer 143 (*blocking dielectric layer*) is shaded in blue:

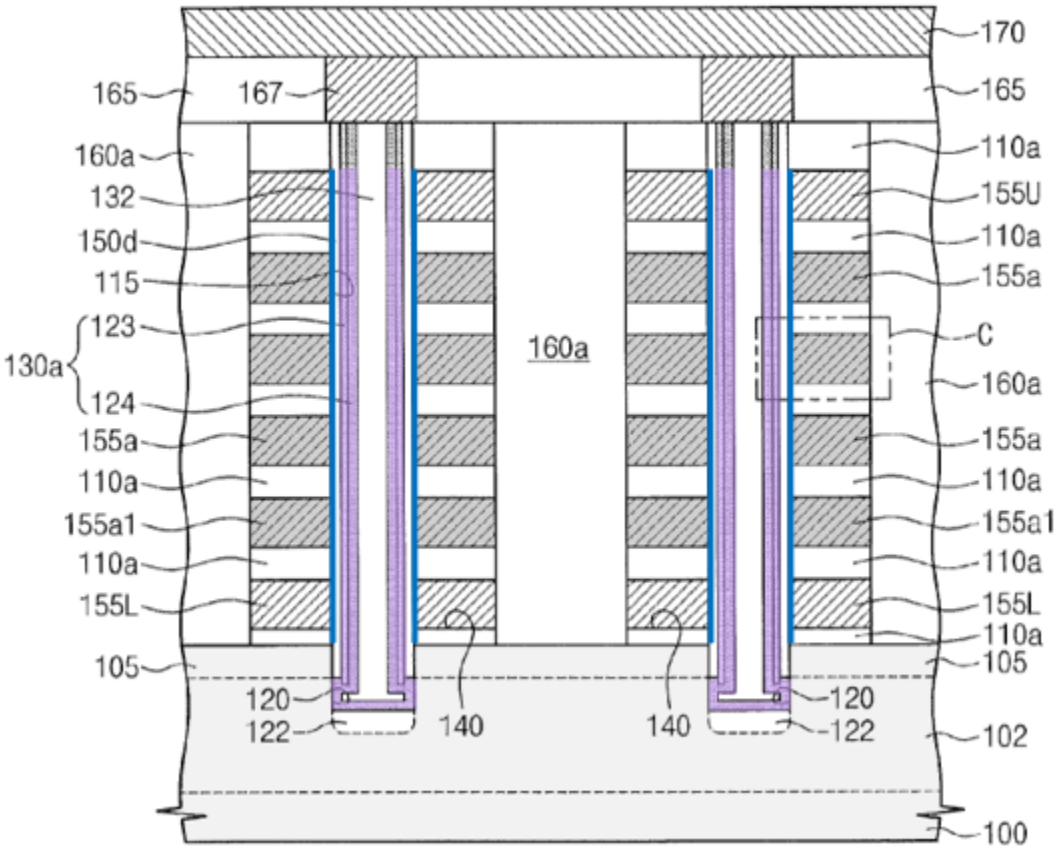


Ex. 1004 (Lee ’255), Fig. 4B.

182. Lee ’255 teaches that its *blocking dielectric layer* (blocking dielectric layer 143) is *disposed between the gate structure and the channel* because “blocking dielectric layer 143” is part of gate dielectric layer 150d (Ex. 1004 (Lee),

[0056]), which Lee '255 teaches is arranged "between a sidewall of the vertical active pattern 130 and each of the gate patterns 155L, 155a1, 155a and 155U" (*id*., [0055]) such that the blocking dielectric layer 143 is "adjacent to each of the gate patterns 155L, 155a1, 155a, and 155U" (*id*., [0056]). This arrangement is shown in annotated figure 4B above, where dielectric layer 150d (containing blocking dielectric layer 143) is arranged between gray-shaded gate electrode 155a (*gate structure*) and purple-shaded active pattern 130/130a (*channel*):

183. I have also added blue lines to figure 4A to illustrate the position of the blocking dielectric layer 143 in that figure:



Ex. 1004 (Lee ’255), Fig. 4A.

184. As I explained in connection with limitation [1f], above, a POSITA would have been motivated to modify the charge storage layer 142 of Lee ’255 based on Lee ’961’s teachings of a multilayer charge storage layer. The resulting multilayer charge storage layer would maintain its position between the tunneling layer and blocking dielectric layer in the combination of Lee ’255 and Lee ’961. This placement of the charge trapping layer is taught in both Lee ’255 (*see* Ex. 1004 (Lee ’255), Fig. 4B) and Lee ’961 (*see* Ex. 1005 (Lee ’961), Fig. 2b). Thus, the implementation and positioning of blocking dielectric layer 143 would be unaffected by the combination.

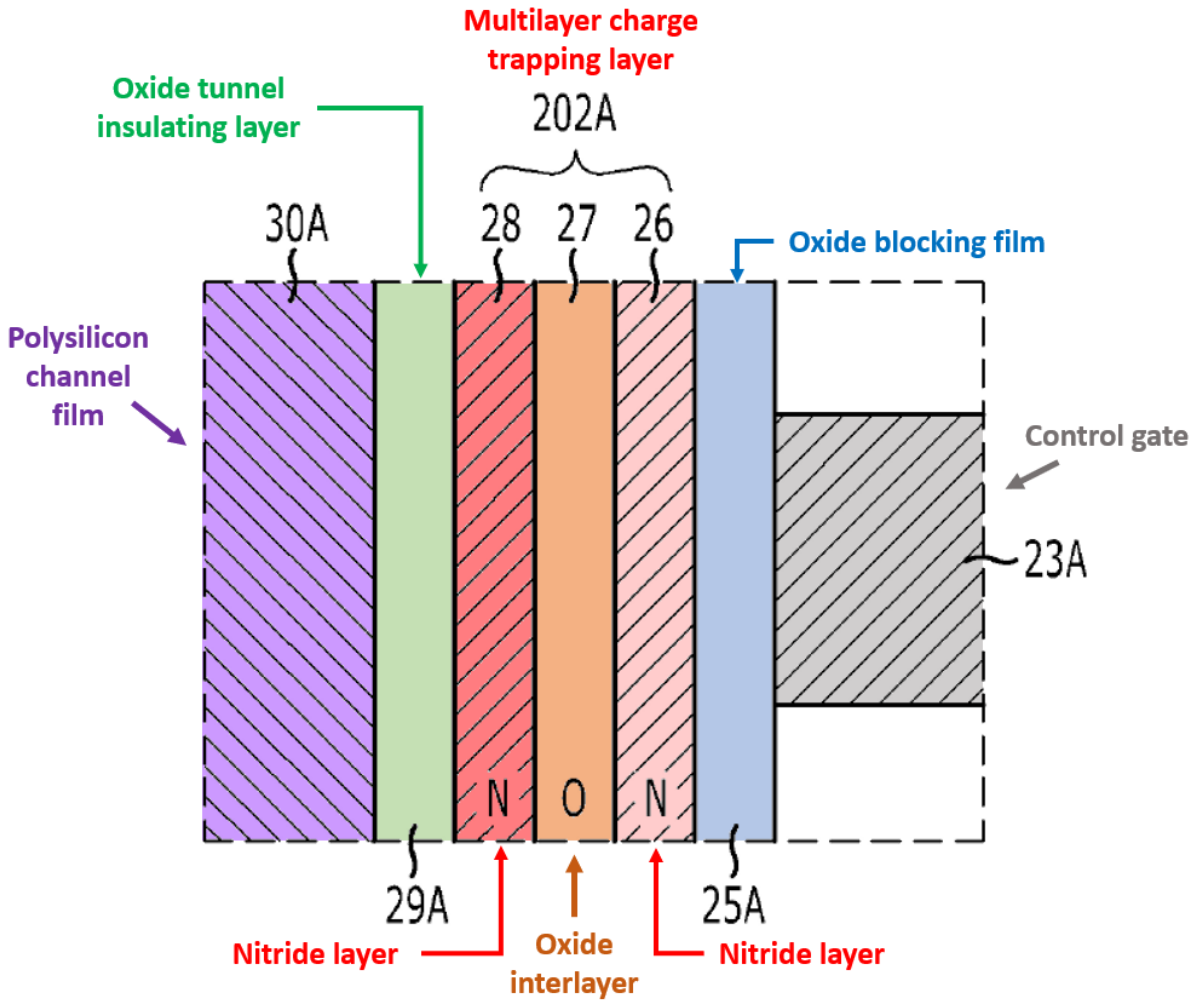
[1f]	**wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer, and**

185. It is my opinion that the combination of Lee ’255 and Lee ’961 teaches limitation [1f].

186. Lee ’961 teaches *a multi-layer charge trapping layer* for the reasons discussed in connection with limitation [1d]. Lee ’961 further teaches that its *multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers* because it teaches that its multilayer charge trap

layer 202A (*multi-layer charge trapping layer*) includes a nitride trap layer 28 (*a first dielectric layer*) and a nitride trap layer 26 (*a second dielectric layer*) with an oxide interlayer 27 (*an anti-tunneling layer*) that is *disposed between* the nitride trap layer 28 (*first dielectric layer*) and nitride trap layer 26 (*second dielectric layer*). Ex. 1005 (Lee '961), [0020]; *see also id.*, Fig. 2b, [0015]. Lee '961 further teaches that *the anti-tunneling layer includes an oxide layer* because it teaches that "interlayer (27) comprises an oxide film." *Id*., [0020].

187. The arrangement of these layers is shown, for example, in annotated figure 2a below, where nitride trap layer 28 is shaded in darker red, oxide interlayer is shaded in orange, and nitride trap layer 26 is shaded in lighter red.



Ex. 1005 (Lee '961), Fig. 2b.

188. A POSITA would have understood silicon nitride trap layers 26, 28 to be *dielectric layers* at least because element [1i] below specifies that the dielectric layers include nitride. Moreover, a POSITA would have understood silicon nitride layers on SONOS-type structures to be dielectrics. *See generally* Part III.C. and, *e.g.*, Ex. 1014 (Wang), [0004], [0009], Ex. 1051 (Lue '625), [0032], Ex. 1023 (Choi), [0031], Ex. 1030 (Jeon), [0044], Ex. 1031 (Shih), [0005], [0069], Ex. 1041 (Zheng), 2:50-51, 5:4-11, 11:44-45.

189. A POSITA would have understood the foregoing configuration of a multilayer charge trap layer 202A (*multi-layer charge trapping layer*) that includes a nitride trap layer 28 (*a first dielectric layer*), a nitride trap layer 26 (*a second dielectric layer*), and an intervening oxide interlayer 27 (*an anti-tunneling layer*) to teach *the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers* . The claim language here explicitly contemplates the presence of an intervening *anti-tunneling layer* between the "abutting" dielectric layers, and a POSITA would therefore have understood "abutting" in the context of this claim language of the '240 patent to include an intervening *anti-tunneling layer*. *See also* Ex. 1001 ('240 patent), Figs. 8A, 8B.

190. A POSITA would have understood oxide interlayer 27 is the *anti-tunneling layer* because Lee '961 teaches that the interlayer 27 prevents the loss (leakage) of charges that would otherwise accumulate at an interface region. Ex. 1005 (Lee '961), [0031]-[0033]. This understanding aligns with the function of the anti-tunneling layer of the '240 patent: "It has further been found the anti-tunneling layer 422c substantially reduces the probability of electron charge that accumulates at the boundaries of the oxygen-lean second nitride layer 422b during programming from tunneling into the first nitride layer 422a, **resulting in lower leakage current** than for a conventional non-volatile memory transistor." Ex.

1001 (’240 patent), 10:23-38. Further, a POSITA would also have understood that the provision of an intermediate oxide between two nitride layers in a SONONOS configuration would function as an anti-tunneling layer. *See* Part III.C.5 and specifically Lai ’676 (Ex. 1017), teaching that its isolation layer 15 functions to “block leakage during low fields.” Ex. 1048 (Lai ’676), [0071].

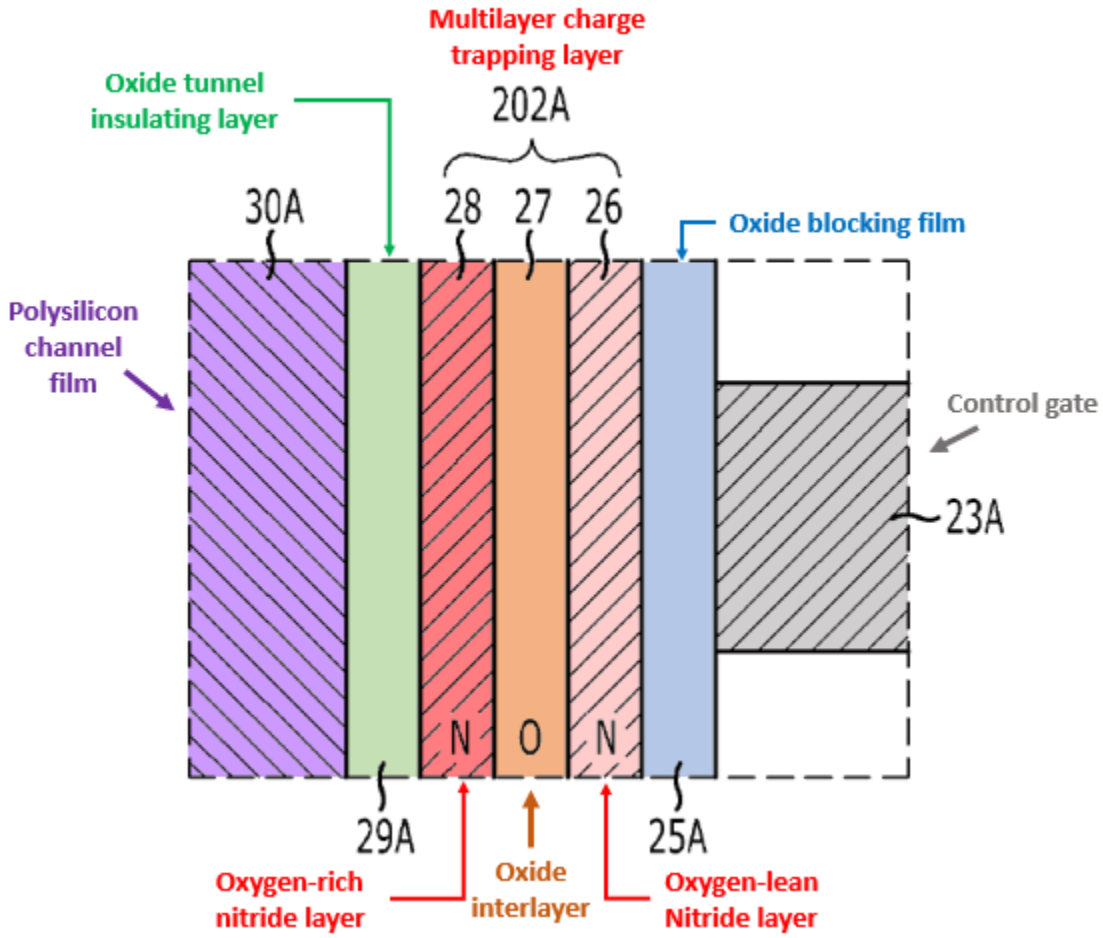
[1g]	**wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride.**

191. It is my opinion that the combination of Lee ’255, Lee ’961, and Fujiwara teaches limitation [1g].

192. As set forth above, the combination of Lee ’255 and Lee ’961 teaches a *multi-layer charge storing region* (Lee ’961’s multilayer charge trap layer 202A) that includes a *first dielectric layer* (nitride trap layer 28) *disposed abutting a second dielectric layer* (nitride trap layer 26) for the reasons set forth in limitation [1f], which I incorporate herein.

193. A POSITA would have considered it obvious prior to July 2012 to modify the multi-layer charge storage region of Lee ’255 / Lee ’961 to make nitride layer 26 (of Lee ’961) oxygen-lean and nitride layer 28 (of Lee ’961) oxygen-rich to further improve charge retention, as this was a well-known design strategy to achieve those goals. *See* Part III.C-4-5.

194. This would result in the arrangement shown, for example, in annotated figure 2a below, where nitride trap layer 28 (*first dielectric layer* that *includes oxygen-rich nitride*) is shaded in darker red, oxide interlayer is shaded in orange, and nitride trap layer 26 (*second dielectric layer* that *includes oxygen-lean nitride*) is shaded in lighter red.



Ex. 1005 (Lee '961), Fig. 2b, [0020].

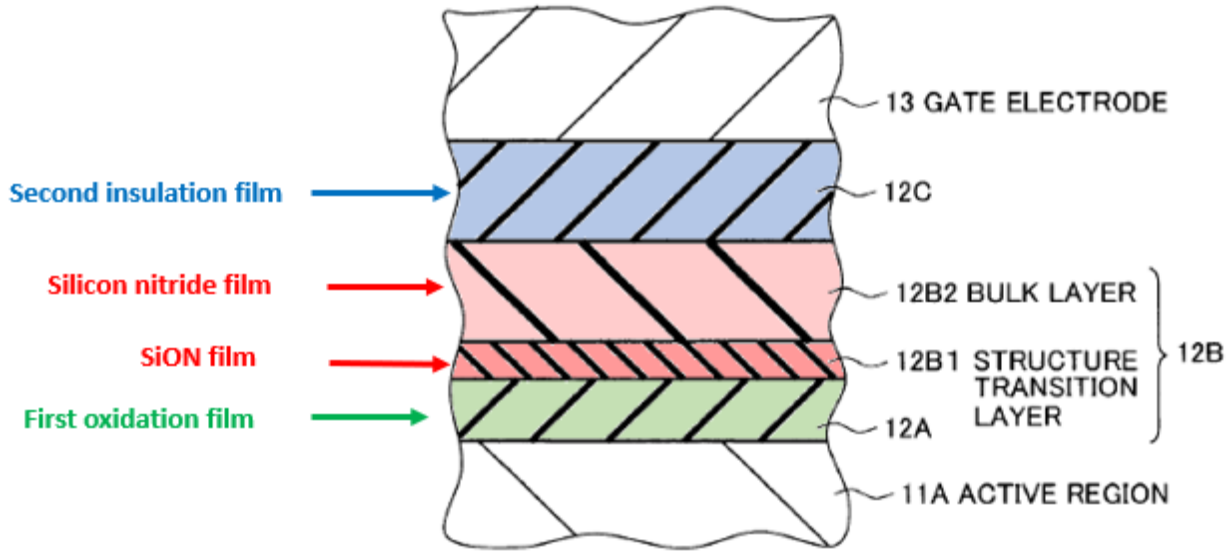
195. In particular, a POSITA would have considered it obvious to provide such an arrangement based on the teachings of Fujiwara, which teaches, like

Lee ’961, that using a multilayer charge storage layer configuration improves charge retention. Ex. 1006 (Fujiwara), [0197].

196. Fujiwara teaches a multi-layer nitride film 12B (*multi-layer charge storing region*) that includes two nitride layers—a silicon oxynitride (SiON) “transition layer” 12B1 (*first dielectric layer* that *includes oxygen-rich nitride*) and a silicon nitride “bulk layer” 12B2 (*second dielectric layer* that *includes oxygen-lean nitride*). *Id*., Fig. 2, Fig. 21, [0074], [0198] – [0201], [0212], [0215]-[0217].

197. This arrangement is shown in annotated figure 21 below, where the silicon oxynitride (SiON) “transition layer” 12B1 (*first dielectric layer* that *includes oxygen-rich nitride*) is shaded in darker red and the silicon nitride “bulk layer” 12B2 (*second dielectric layer* that *includes oxygen-lean nitride*) is shaded in lighter red.

FIG. 21



Ex. 1006 (Fujiwara), Fig. 21; *see also id.*, Fig. 2, [0212], [0215], [0218].

198. A POSITA would have understood that "transition layer (SiON) film" 12B1 is *first dielectric layer* that *includes oxygen-rich nitride*, and that nitride "bulk layer" 12B2 is a *second dielectric layer* that *includes oxygen-lean nitride*, relative to each other.

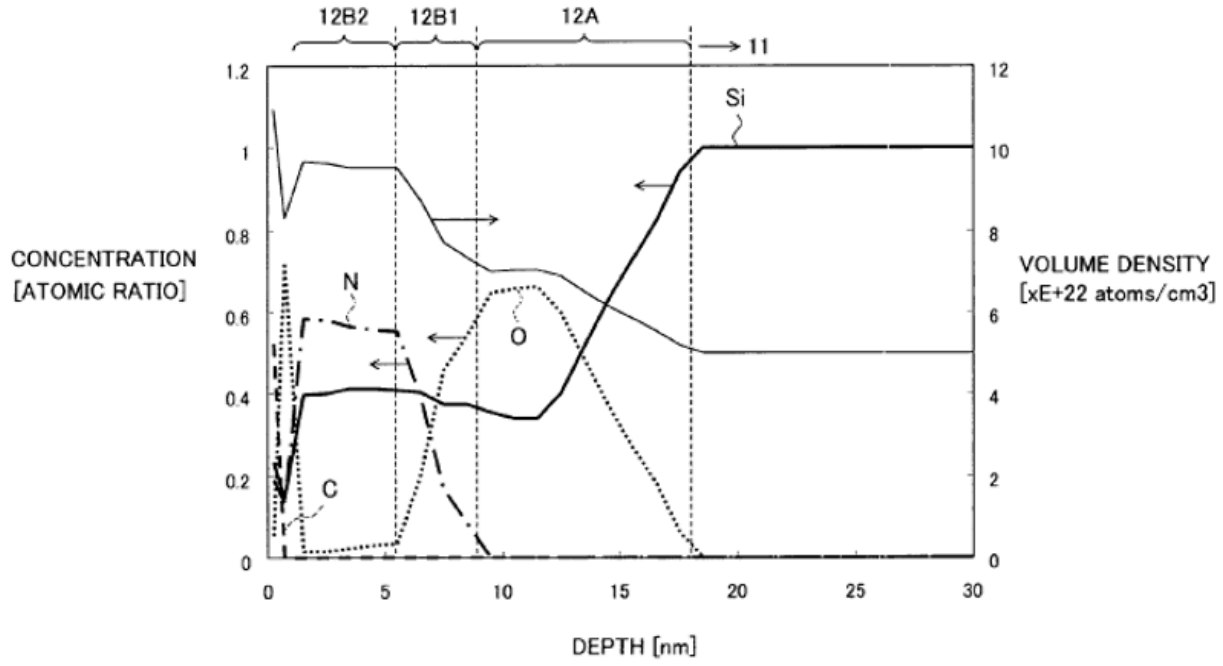
199. Indeed, Fujiwara characterizes the upper (oxygen-lean) nitride layer (12B2) as the "main structure of the charge storage layer." Ex. 1006 (Fujiwara), [0215]; *see also id.*, [0199]. The lower (oxygen-rich) nitride layer (12B1) is a silicon oxynitride transition layer chosen because it is "low in the charge trap and high in the data retention characteristic." *Id.*, [0205]; *see also id.*, [0201], [0210].

A POSITA would have understood "high in the data retention characteristic" to mean promoting charge retention and preventing leakage.

200. These teachings mirror those of the '240 patent, which states that the upper, oxygen-lean nitride is designed to trap charges, while the lower, oxygen-rich nitride is substantially trap-free and designed to reduce charge loss. *See* Ex. 1001 ('240 patent), 6:4-10 ("bottom, trap free oxynitride layer 210B"); 8:26-26 ("lower, substantially trap free oxynitride layer 318B"); *see also id.*, 10:13-15 ("It has been found that an oxygen-rich, first nitride layer 422a decreases the charge loss rate after programming and after erase."); 13:45-57 (the oxygen-rich layer is designed "to reduce the number of charge traps therein"). These properties of oxygen-rich and oxygen-lean nitride layers were also widely known by POSITAs prior to July 2012. *See* Part III.C.4-6.

201. Beyond the foregoing, Fujiwara also explicitly teaches that the "transition layer (SiON) film" 12B1 is a *first dielectric layer* that *includes oxygen-rich nitride* and the nitride "bulk layer" 12B2 is a *second dielectric layer* that *includes oxygen-lean nitride*) based on the disclosed atomic composition profiles of those layers depicted in figure 22:

FIG. 22



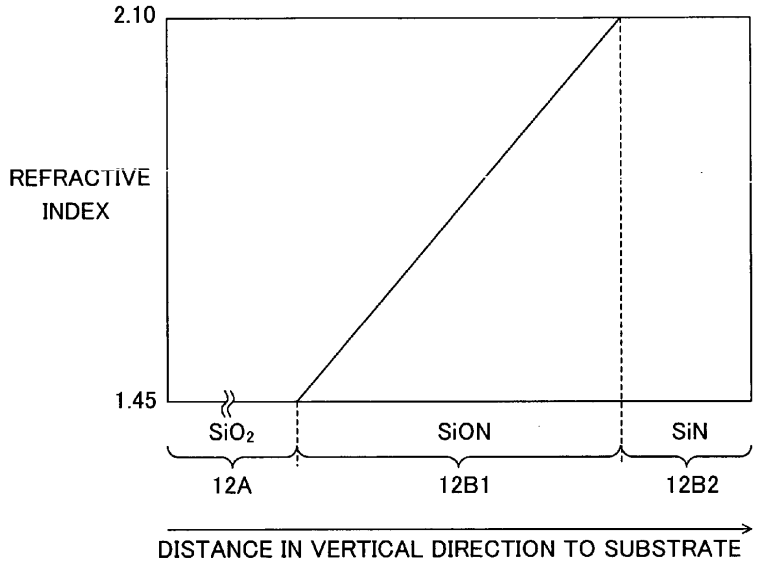
Ex. 1006 (Fujiwara), Fig. 22, [0200]. [7]

202. As reflected above, layer 12B1 (SiON transition layer) is a *first dielectric layer* that *includes oxygen-rich nitride* because its nitride peaks at approximately 50 atomic % oxygen in its interior. Layer 12B2 (Si_3N_4 bulk layer) in figure 22, by contrast, is a *second dielectric layer* that *includes oxygen-lean nitride* because its nitride contains less than approximately 5 atomic % oxygen throughout, and in its interior. With respect to layer 12B1, the oxygen

[7] At the left of the graph of figure 22, the oxygen concentration increases. A POSITA would understand that this occurs as the MONOS stack transitions to the top oxide insulating layer. This is also reflected by the brackets at the top of the chart that show where the bulk nitride layer (12B2) ends/transitions.

concentration varies across its depth, with oxygen concentrations exceeding about 15% for the vast majority of the layer. While the oxygen concentration drops below 15% as a transition is made from layer 12B1 to 12B2, a POSITA would have recognized this as a common variation during CVD or oxidation processes when one layer (e.g., a SiON layer) transitions to another layer (e.g., a SiN layer). Having an oxygen concentration lower than 15% at the transition from layer 12B1 to layer 12B2 would not change a POSITA's understanding that layer 12B1 is a *first dielectric layer* (SiON film) that *includes oxygen-rich nitride*. When assessing whether a nitride layer is a *first dielectric layer* that *includes oxygen-rich nitride*, a POSITA would evaluate the composition across the full layer (e.g., the entire SiON film), not at an isolated interface. In Fujiwara, a vast majority of layer 12B1 (by depth) contains more than 15% oxygen, with portions exceeding 50%. A POSITA would not have required each boundary segment to exceed 15% oxygen, given the well-recognized nature of graded SiON transition films. The foregoing conclusions are reinforced by Fujiwara figure 23, which shows the refractive index of 12B1 grading up to about 2.10, which a POSITA would have understood to represent about 60–67 atomic % O. A POSITA would have recognized refractive index as a standard optical proxy for oxygen incorporation in SiON films. Thus, figure 23 independently confirms the same conclusion as figure 22: 12B1 is an *oxygen-rich* first nitride layer.

FIG. 23



Ex. 1006 (Fujiwara), Fig. 23.

203. In view of the above, Fujiwara teaches that layer 12B1 includes an *oxygen-rich nitride* at least because the percentage of oxygen in layer 12B1 exceeds 15%. *See* Part VII.B (construction of oxygen-rich and oxygen-lean). Similarly, Fujiwara teaches that layer 12B2 includes an *oxygen-lean nitride* at least because the percentage of oxygen is less than 5%. *See id.*

204. It is my opinion that a POSITA would have been motivated to further modify the combination of Lee '255 and Lee '961 to apply the teachings of Fujiwara to optimize the oxygen concentrations of the nitride layers of the multi-layer charge-trapping region.

205. It would have been obvious for a POSITA to consult the teachings of Fujiwara in seeking to improve the memory transistor configuration of Lee '255

and Lee ’961 because Fujiwara is also directed to improving the configuration of SONOS-type charge trapping memory transistors such as those taught in Lee ’255 and Lee ’961. Ex. 1006 (Fujiwara), Fig. 1 (teaching a SONOS stack), [0010]-[0013] (teaching that SONOS retention characteristics need improvement). Fujiwara’s teaching of optimizing oxygen concentrations in nitride layers to improve charge retention is complementary to the combination of Lee ’961 and Lee ’255, which also has the goal of improving data retention. Ex. 1003, ¶297; compare Ex. 1005 (Lee ’961), [0008], [0010] with Ex. 1006 (Fujiwara), [0197], [0205].

206. A POSITA would have been motivated to apply Fujiwara’s layer composition teachings to the Lee ’255 / Lee ’961 charge trapping region to obtain the benefit expressly taught in Fujiwara—to improve the retention characteristic of the charge storage layer of the resultant stack. Ex. 1006 (Fujiwara), [0197] (stating that the oxygen-rich/oxygen-lean embodiment “further improve[s] the charge retention characteristics”). A POSITA would have understood that this combination of Fujiwara with Lee ’255 and Lee ’961 amounts to applying the teachings of Fujiwara for their intended purpose to improve similar devices in the same way.

207. Further, the benefit of using an oxygen-rich bottom nitride layer and an oxygen-lean top nitride layer in a SONOS memory transistor would have been

predictable to a POSITA prior to July 2012. In addition to Fujiwara, many other prior art references show that it was a routine design choice to use an oxygen-rich first nitride layer and an oxygen-lean second nitride layer to obtain improved charge retention characteristics in both SONNOS and SONONOS configurations. *See, e.g.*, Ex. 1012 (Heo), [0058]-[0068] (teaching that using a bottom oxidized nitride layer with a top nitride layer improves "the data retention properties and/or durability of the non-volatile memory device"); Ex. 1017 (Lai '676), [0015], [0068]-[0077] (teaching that an NON charge trapping region with an upper silicon nitride layer 16, middle oxide layer 15, and lower silicon oxynitride layer 14 improves retention); Ex. 1011 (Levy), [0025]-[0026] (using an oxygen-rich bottom nitride layer "decrease[s] the charge loss rate after programming and after erase"); Ex. 1013 (Ganguly), Fig. 3, [0048]-[0050] (teaching first nitride layer is up to 50% oxygen and engineered to have a lower charge trap density in order to promote charge retention in the second nitride layer); and Ex. 1021 (Higuchi) [0007], [0133]-[0134], [0141]-[0142] (teaching that an NON charge trapping region with an upper silicon nitride layer 203, middle oxide layer 202d, and lower silicon oxynitride layer 203c improves retention). Accordingly, applying the teachings of Fujiwara to the Lee '255/Lee '961 stack would have amounted to combining prior art elements according to known methods to obtain predictable results.

208. A POSITA also would have expected success in applying Fujiwara's teachings concerning optimized oxygen concentrations to the multi-layer charge-trapping region of the Lee '255 / Lee '961 framework because the underlying materials, equipment, and process knobs were mainstream. Even without Fujiwara, Lee '255 and Lee '961 already provide a multi-layer charge trap; Fujiwara merely teaches adjusting the compositions of the layers. Indeed, Lee '961's intermediate oxide layer already suggests a natural location for Fujiwara's oxygen-rich transition film, further confirming the compatibility of the two disclosures. Adjusting oxygen content in nitride films was routine using standard LPCVD/PECVD knobs (e.g., gas flows, anneals, or pressure settings), so implementing Fujiwara's oxygen-rich/lean layering would have been a straightforward process adjustment, not new chemistry. Fujiwara further points out that the transition film remains amorphous, avoiding lattice-mismatch penalties, and that both layers tolerate subsequent high-κ caps and metal gates up to about 750 °C —a thermal window already assumed in Lee '255 and Lee '961. Because the retention improvement scales smoothly with the oxygen gradient, a POSITA would reasonably predict that implementing Fujiwara's teaching of oxygen-rich and oxygen-lean nitride layers could be achieved with routine process-tuning and would deliver the same data-retention benefits without introducing new reliability risks.

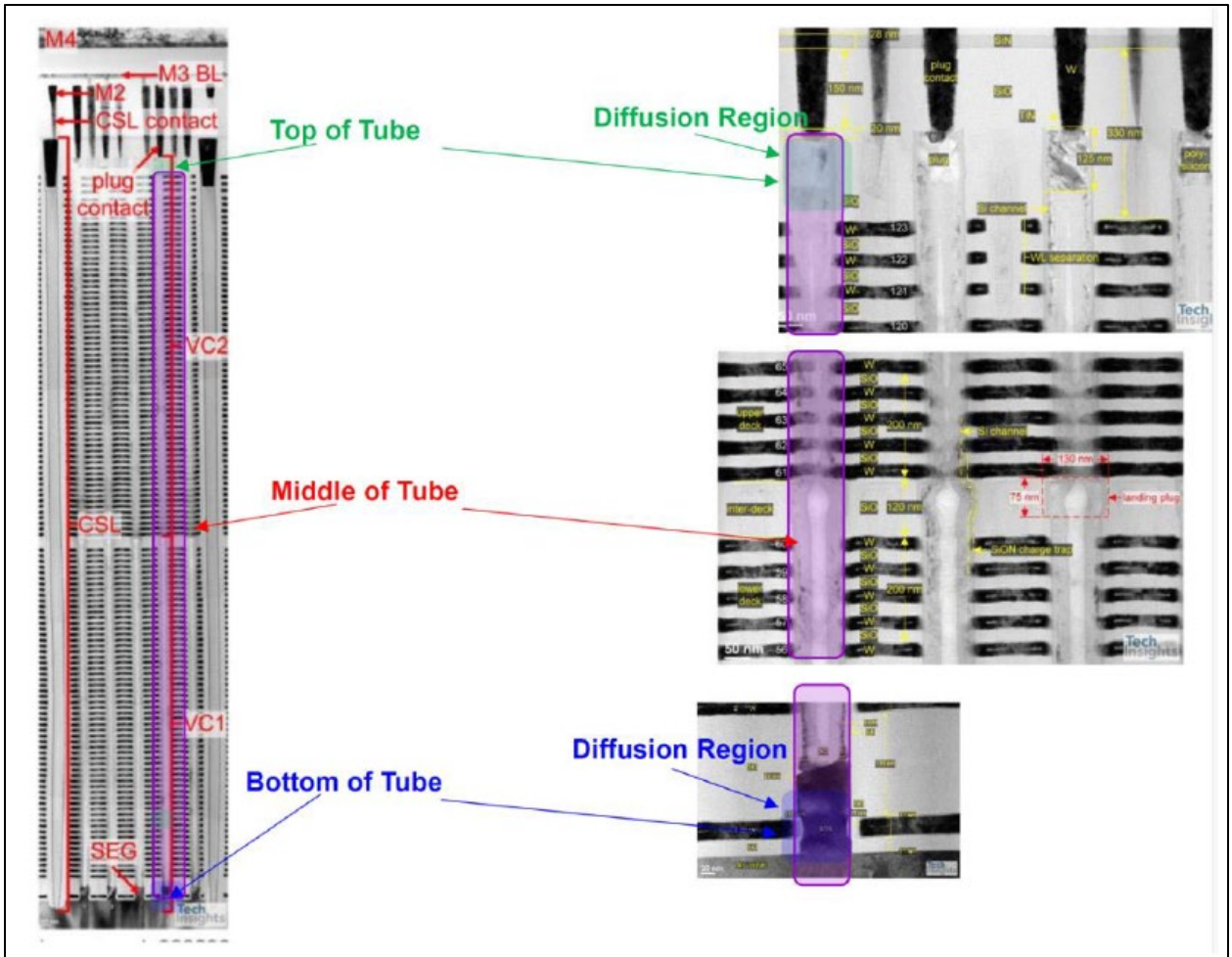
2. Dependent Claims 3-7, 9, and 11

3.	**The memory device of claim 1, wherein the channel, first and second diffusion regions are disposed above a semiconductor material structure.**
4.	**The memory device of claim 1, wherein the channel, first and second diffusion regions are suspended above a semiconductor material structure.**

209. I understand that claims 3 and 4 both depend from claim 1 and therefore have all of the requirements of claim 1. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claim 1.

210. Claim 3 requires that the two diffusion regions and the channel *are disposed above* the substrate. Claim 4 requires that the two diffusion regions and the channel *are suspended above* the substrate.

211. I understand that, in the parallel district court litigation, Patent Owner has taken the position that a vertical NAND structure satisfies the limitations of claims 3 and 4. In particular, Patent Owner has provided the following identification of a channel and first and second diffusion regions in a device accused of infringement:

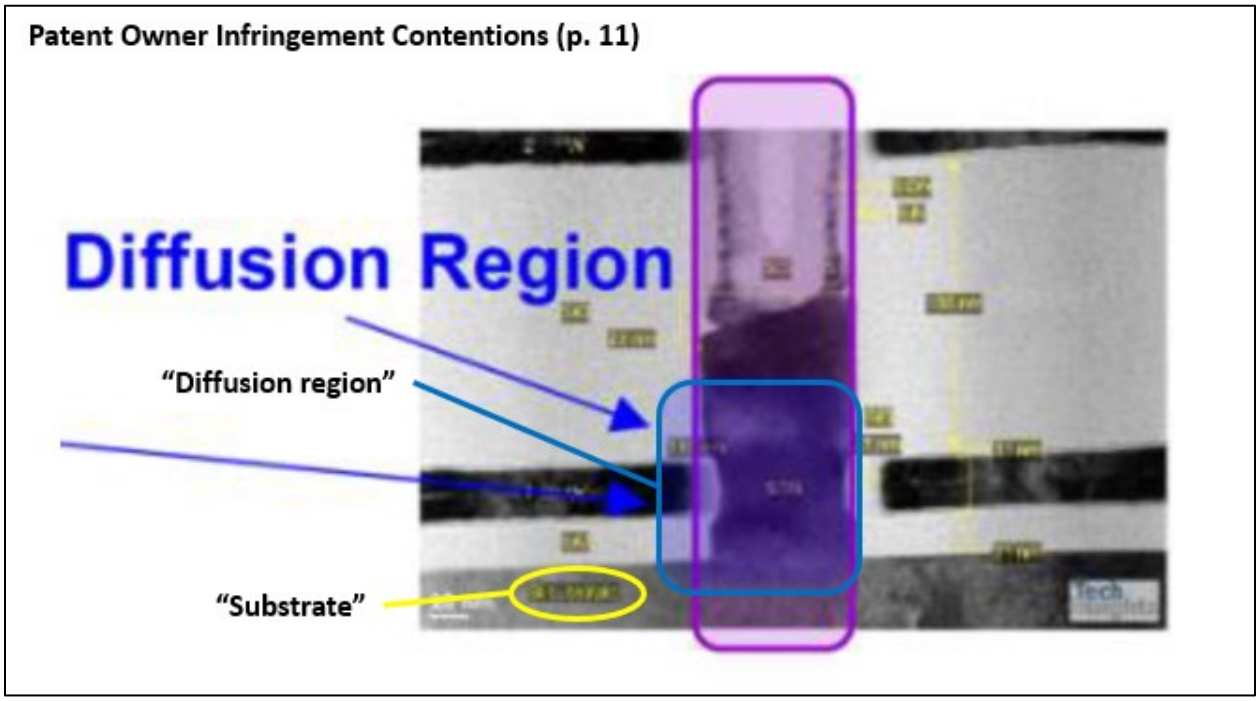


The vertical tubes contain a silicon channel that electrically connect the first and second diffusion regions[15]:

Ex. 1054 (Infringement Contentions), 000011; *see also id.*, [000019, 000021] (asserting that this configuration satisfies claims 3 and 4).

212. I have increased the magnification on a portion of Patent Owner's image and provided annotations to make clearer the arrangement that Patent Owner alleges to show a channel and diffusion regions that are *disposed/suspended above* the substrate. In particular, I have circled Patent Owner's identification of the

"substrate" (yellow) and drawn a border around Patent Owner's identification of the lower "diffusion region" (blue):

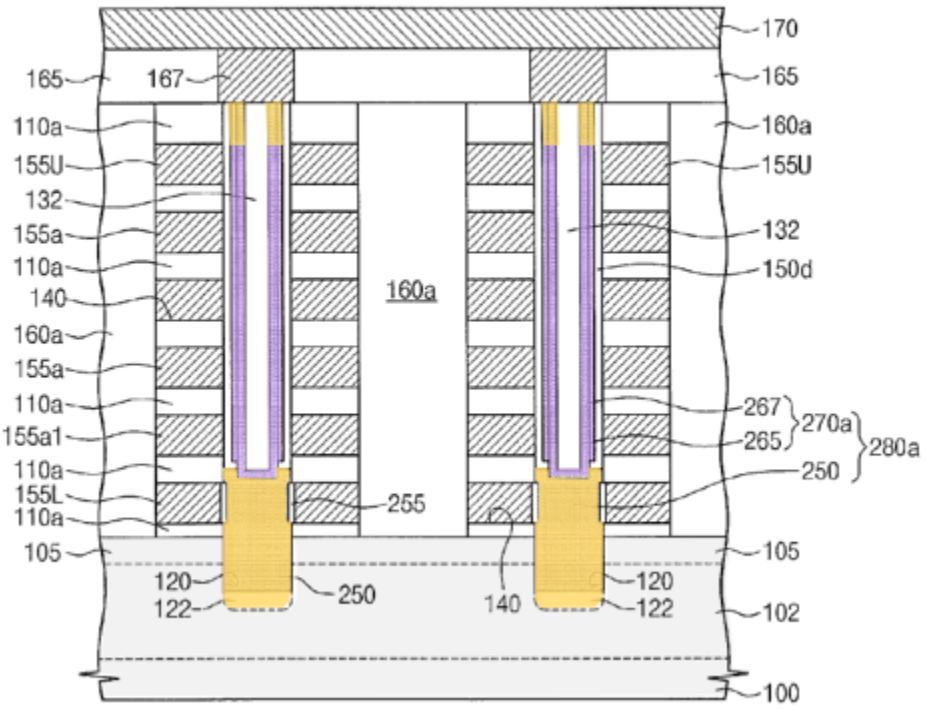


Ex. 1054 (Infringement Contentions), 000011 (annotated).

213. Under Patent Owner's interpretation of claims 3 and 4, Lee '255 teaches a channel and diffusion regions that are *disposed/suspended above* a substrate. In particular, figures 11 and 12A-12F of Lee '255 teach the use of doped lower active pattern 250 using the same dopant as high concentration region 122 (the *first diffusion region* for the reasons discussion in limitation [1b]). Ex. 1004 (Lee '255), [0113], [0114], [0133]. A POSITA would have understood that, because they are doped with the same dopant, doped lower active pattern 250 and high concentration region 122 together (or pattern 250 alone) form a *first diffusion region* for the reasons discussed in limitation [1b]. As shown in the annotated

version of figure 12E below, this *first diffusion region* (the combined structure of high concentration region 122 and doped lower active pattern 250) extends above the substrate 100, which Lee '255 expressly describes as a semiconductor substrate. Ex. 1004 (Lee '255), [0108].

Fig. 12E



Ex. 1004 (Lee '255), Fig. 12E; see also Figs. 11 and 12A-12F, [0113], [0114].

214. Further, in this embodiment, both the vertical active patterns 130/130a (the *channel* for the reasons set forth in limitation [1b]) and the drain (the *second diffusion region* for the reasons set forth in limitation [1b]) are also arranged above the substrate 100 (*semiconductor material structure*).

215. Based on Patent Owner's claim interpretation, Lee '255 teaches that the channel and the first and second diffusion regions are *disposed above a semiconductor material structure* (claim 3) because Lee '255 (like the structure Patent Owner accuses of infringement) has at least a portion of the channel region (purple) and the diffusion regions (gold) arranged above the top surface of a substrate (light gray). Further, under Patent Owner's claim interpretation, this same arrangement also teaches the channel and the first and second diffusion regions are *suspended above a semiconductor material structure* (claim 4). *See* Ex. 1054 (Infringement Contentions),[000011, 000019, 000021]. Based on the Patent Owner's claim interpretation, Lee '255 also teaches that the channel and the diffusion regions are suspended above a substrate because each of those features are arranged above the top surface of substrate 100 and are laterally supported (*suspended*) by the alternating gate 155 and dielectric 110 layers.

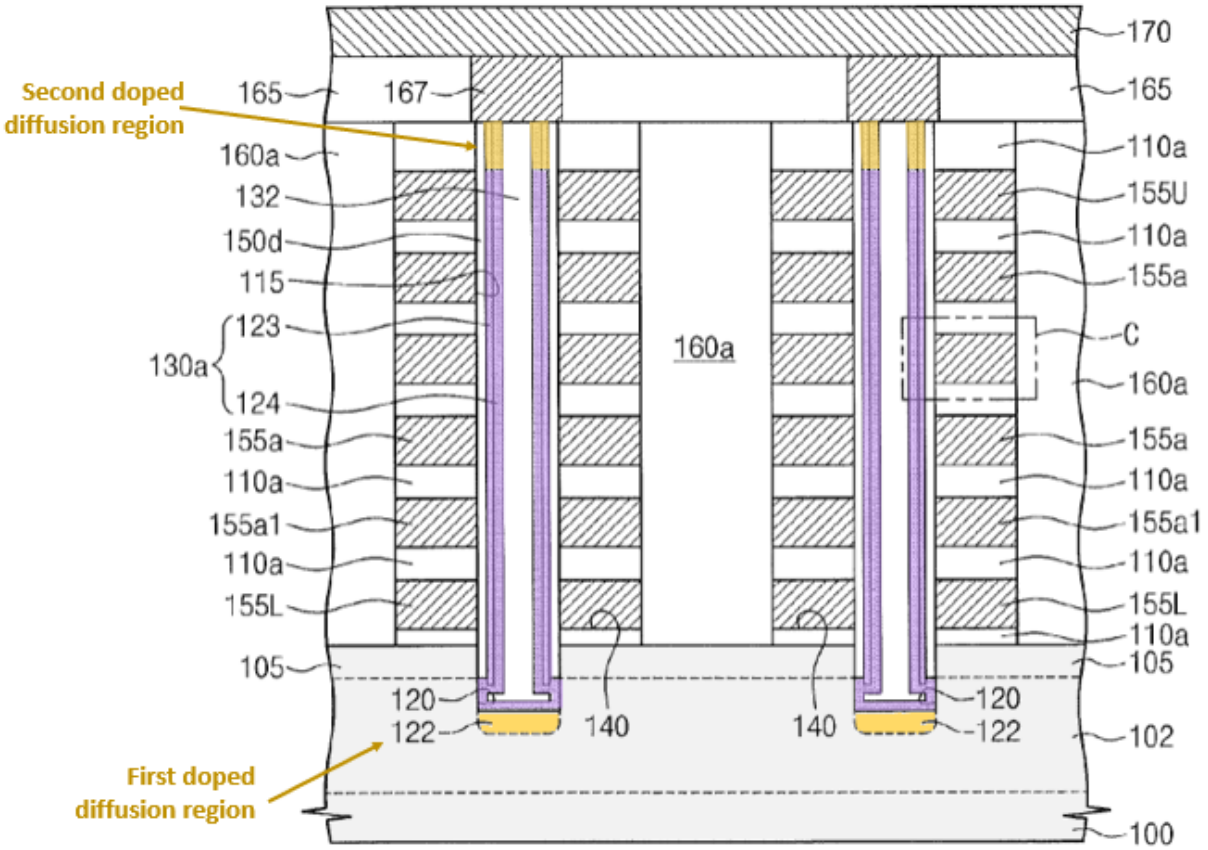
216. Finally, a POSITA would have considered it obvious to employ doped lower active patterns 250 in, for example, the figure 4A embodiment discussed in detail as to claim 1, because Lee '255 teaches that it is an alternative configuration within its inventive concept and provides improved reliability. Ex. 1004 (Lee '255), [0113], [0118]. A POSITA would have recognized that substituting the doped lower active pattern 250 into other Lee '255 embodiments was a routine design choice, as both configurations perform the same function of forming a

diffusion region, with Lee '255's express teaching that the figure 12E structure improves reliability.

5.	**The memory device of claim 1, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure.**

217. I understand that claim 5 depends from claim 1 and therefore has all of the requirements of claim 1. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claim 1.

218. It is my opinion that Lee '255 teaches the additional limitations of claim 5 because it teaches that vertical active pattern 130/130a (the *channel* for the reasons set forth in limitation [1c]) is *vertical and oriented substantially perpendicular to a semiconductor material structure* because it extends vertically from and perpendicular to the plane of substrate 100 (the *semiconductor material structure* for the reasons set forth in the claim construction section above, see Part VII.D), as shown in annotated figure 4A below.



Ex. 1004 (Lee ’255), Fig. 4A; *see also id.*, [0052].

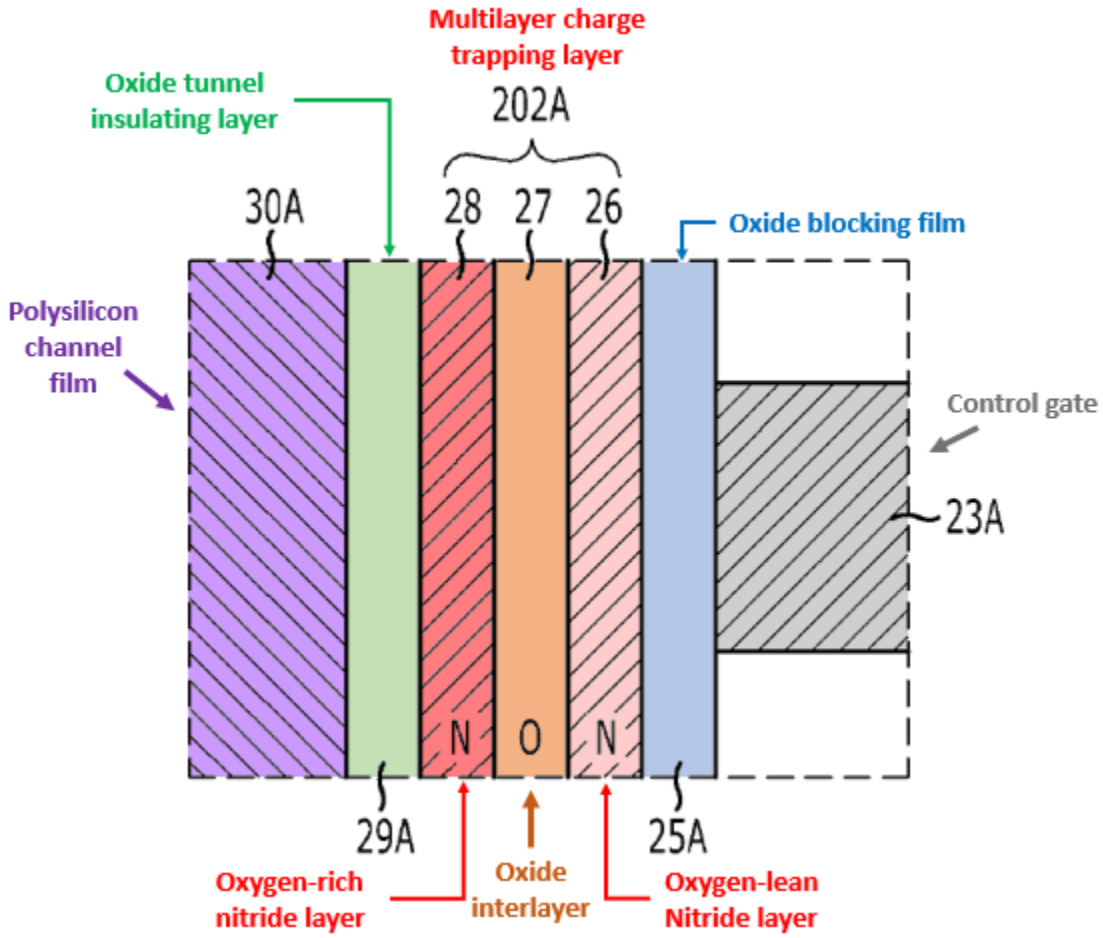
[6pre].	**The memory device of claim 1,**

219. I understand that claim 6 depends on claim 1 and therefore has all of the requirements of claim 1. As I have explained above, it is my opinion that the combination of Lee ’255, Lee ’961, and Fujiwara teaches each and every limitation of claim 1.

220. It is my opinion that the combination of Lee ’255, Lee ’961, and Fujiwara teaches limitation [6pre] for at least the reasons discussed for claim 1, above, and the additional limitations of claim 6 for the reasons set forth below.

[6a]	**wherein the first dielectric layer is disposed abutting the tunnel dielectric layer and substantially trap free, and**

221. It is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches limitation [6a] because, as set forth in limitations [1e]-[1i], the combined teachings of these references will result in, as set forth in limitation [1i], the configuration below:



Ex. 1005 (Lee '961), Fig. 2b, [0020].

222. As reflected in the foregoing configuration, the combination of Lee '255, Lee '961, and Fujiwara teaches a *first dielectric layer* (nitride trap layer

28) adjacent (*disposed abutting*) tunnel dielectric layer 141 (*the tunnel dielectric layer* for the reasons set forth in limitation [1e]).

223. Further, in the foregoing combination of Lee '255, Lee '961, and Fujiwara, Fujiwara also teaches that the *first dielectric layer* (nitride trap layer 28 in the above annotated figure 2b) is *substantially trap free* because it specifically teaches that its lower (oxygen-rich) nitride layer (12B1) is "low in the charge trap and high in the data retention characteristic" (Ex. 1006 (Fujiwara), [0205], [0201], [0210]). A POSITA would have understood "low in the charge trap" to be *substantially trap free* in the context of the '240 patent for several reasons. First the '240 patent does not specify just how "substantial" the *substantially trap free* requirement is or provide any related measurement guideline. Thus, a POSITA would have understood "low in the charge trap" and *substantially trap free* to have overlapping scope (or to provide the latter in view of the teaching of the former). Second, Fujiwara teaches that the "main structure of the charge storage layer" (Ex. 1006 (Fujiwara), [0215], [0199]) is provided by the upper nitride film 12B2, which a POSITA would understand to mean that film 12B1 has lesser trapping functionality, and thus to be substantially trap-free as compared to nitride film 12B2. Third, as set forth above in limitation [1i], the relative oxygen concentrations and described functionality of: (i) Fujiwara's SiON nitride layer 12B1 and the '240 patent's first dielectric layer (318B, 422a, 616a, 716a, 810a);

and (ii) Fujiwara's SiN nitride layer 12B2 and the '240 patent's second dielectric layer (318A, 422b, 616b, 716b, 810b) are similar. Thus, a POSITA would have recognized that Fujiwara's SiON nitride layer 12B1 would be *substantially trap free* like the comparable layers of the '240 patent.

[6b]	**wherein the second dielectric layer is disposed abutting the blocking dielectric layer.**

224. It is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches limitation [6b] because, as reflected in the configuration shown in limitation [6a], the combination of Lee '255, Lee '961, and Fujiwara teaches *the second dielectric layer* (nitride trap layer 26) is adjacent (*disposed abutting*) blocking dielectric layer 143 (*a blocking dielectric layer* for the reasons set forth in limitation [1g]).

7.	**The memory device of claim 1, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO).**

225. I understand that claim 7 depends from claim 1 and therefore has all of the requirements of claim 1. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claim 1.

226. I understand that Patent Owner has taken the position that a blocking dielectric layer comprising aluminum oxide satisfies the requirement of wherein the blocking dielectric layer comprises high K high temperature oxide (HTO):

7. The memory device of claim 1, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO).	In the '240 Accused Instrumentalities the blocking dielectric layer comprises high K high temperature oxide (HTO). For example, the blocking dielectric layer ("BlOx") comprises aluminum oxide, a high K high temperature oxide.

Ex. 1054 (Infringement Contentions), 000022.

227. Based on Patent Owner's interpretation of claim 7, Lee '255 also teaches *the blocking dielectric layer comprises high K dielectric* because Lee '255 teaches a "high-k dielectric layer in the blocking dielectric layer" that is comprised of "aluminum-oxide":

> The blocking dielectric layer 143 may include a high-k dielectric layer having a dielectric constant higher than that of the tunnel dielectric layer 141. For example, **the high-k dielectric layer in the blocking dielectric layer 143 may include metal-oxide such as aluminum-oxide** or hafnium-oxide.

Ex. 1004 (Lee '255), [0057] (emphasis added).

9.	**The memory device of claim 1, wherein the gate structure includes a high work function gate electrode.**
11.	**The memory device of claim 9, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.**

228. I understand that claim 9 depends from claim 1 and therefore has all of the requirements of claim 1 and that claim 11 depends from claim 9 and therefore has all the requirements of claims 1 and 9. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claim 1.

229. It is my opinion that Lee '255 teaches the additional limitations of claims 9 and 11 because it teaches gates 155a "include a conductive material" such as doped silicon, tantalum, or tantalum nitride. Ex. 1004 (Lee '255), [0062]. In the context of the SONONOS configuration taught by the combination of Lee '255, Lee '961, and Fujiwara described above, a POSITA would have understood that doped silicon and tantalum nitride are *high work function* materials[8] and would have considered it obvious that the doped silicon would be *P+ doped polysilicon*. *See, e.g.*, Ex. 1001 (the '240 patent), 7:27-38 (doped polysilicon used for high work function gate electrodes); Ex. 1012 (Heo), [0046] (P-type silicon, tantalum (Ta), and tantalum nitride (TaN) are examples of materials for high work function gate electrodes); Ex. 1017 (Lai '676), [0067], [0072] (p+ polysilicon and tantalum nitride are high work function materials); Ex. 1041 (Zheng), 5:52-62 (P+ polysilicon is "particularly well suited" for use in high work function gate

[8] As I explained in the claim construction section, above (see Part VII.B.), a POSITA would have understood—based on the examples of *high work function gate electrodes* provided in the '240 patent and the recitation of claim 11—that polysilicon doped with p-type impurities is an example of a *high work function* gate material. *See* Ex. 1001 ('240 patent), 7:27-38; *see also* Ex. 1041 (Zheng) 5:36-37 ("For each memory device 12, one of the word lines 14 functions as a gate electrode."); *id*., 5:60-62 ("Materials that are particularly well suited for the word lines 14 include P+ polysilicon (having a work function of about 5.1 eV to about 5.2 eV."); Ex. 1012 (Heo), [0046]; Ex. 1021 (Lai '676), [0067], [0072].

electrodes); id., 6:32-59 (tantalum and tantalum nitride used for high work function gate electrodes).

230. To the extent patent owner argues that the gate materials taught in Lee '255 do not teach the limitations of claims 9 and/or 11, a POSITA would have found it obvious to use a *high work function gate electrode* that *comprises a P+ doped polysilicon* based on the teachings of Lee '961. In particular, Lee '961 teaches "[t]he control gate electrode (23A) includes a polysilicon film, particularly **a doped polysilicon film doped with** N-type impurities or **P-type impurities**." Ex. 1005 (Lee '961), [0018].

231. A POSITA would have been motivated to apply the high work function gate electrode of Lee '961 to the memory device of Lee '255, and expected success in doing so, because the use of such material would have amounted to (i) combining prior art elements according to known methods to yield predictable results; and (ii) use of known techniques to improve a similar device in the same way. As I explained in Part III.C.7, the use of high work function gate electrodes in SONOS-type memory devices was well-established and the benefits of such a design choice were widely recognized. *See, e.g.*, Ex. 1029 (Kim Article), 000005, Fig. 7 ("The erase speed of p^+ polysilicon gate memory is much faster than that of n^+ polysilicon gate memory."); Ex. 1030 (Jeon), Fig. 1, [0009] ("The control gate 14 includes either N^+ polysilicon with a work function of 4.1 eV or p^+

polysilicon with a work function of 5.1 eV."); Ex. 1016 (Lue '189), [0084] (in preferred embodiments, high work function gates can be formed of metals, metal nitrides, or P^+ polysilicon), [0086] ("High work function gate materials suppress gate electron injection into the trapping layer. . . . [T]he memory cells according to high work function gate material embodiments of the present invention are particularly suitable for use in NAND applications where elevated threshold voltages in the erased/reset state can be undesirable."); Ex. 1012 (Heo), [0064] (teaching the use of a high work function gate electrode to improve the efficiency and ease of operation of the flash memory); Ex. 1031 (Shih), [0071] ("In some embodiments, the gate comprises a material having a work function greater than the intrinsic work function of n-type silicon. . . for example, greater than about 5 eV. Representative gate materials include p-type poly TiN, Pt, and other high work function metals and materials."); Ex. 1041 (Zheng), 1:14-18 (high work function gate electrode enhances data retention).

B. Ground 2: Obviousness over Lee '255, Lee '961, Fujiwara, and Hwang

232. It is my opinion that claims 12-18 of the '240 patent are rendered obvious based on the teachings of Lee '255, Lee '961, Fujiwara, and Hwang.

233. Hwang, like Lee '255, Lee '961, and Fujiwara, relates to SONOS charge trapping-type nonvolatile memory devices. Ex. 1048 (Hwang), [0003] ("The present disclosure herein relates to semiconductor devices and, more

particularly, to three dimensional semiconductor memory devices") and [0046]-[0048] (describing the SONOS structure). Hwang, like Lee '255 and Lee '961, teaches a "three dimensional semiconductor memory device" (Hwang (Ex. 1048), [0007]) with a vertical channel 530 (*Id*., [0112]) surrounded by a charge trapping stack 525 (*Id*., [0047], [0112].) passing through an alternating stack of insulating (505) and gate (510) patterns (*Id*., [0112]).

234. A POSITA would also have understood that the memory devices of Lee '255 and Lee '961 would have been connected to MOS logic transistors in the peripheral regions of their respective devices to control their operation. Hwang expressly teaches such device electrical connections to MOS logic transistors in its peripheral circuit region 20, along with a specific "step structure" approach, that it states provides simplified fabrication and improved reliability and integration. Ex. 1048 (Hwang), [0112]-[0113], [0116], [0158].

235. It is my opinion that the combination of Lee '255, Lee '961, Fujiwara, and Hwang teaches each and every element limitation of claims 12-18 of the '240 patent for the reasons discussed in detail below. Further, it is my opinion that a POSITA would have been motivated to further modify the combination of Lee '255, Lee '961, and Fujiwara in view of Hwang's electrical connection teachings to provide an improved charge-trapping nonvolatile memory device. A POSITA also would have expected success in applying the teachings of Hwang to

further modify the combination of Lee '255, Lee '961, and Fujiwara. I have provided further details of my motivation to combine and expectation of success analysis in connection with specific claim limitations below.

236. As I have already explained above, the combination of Lee '255, Lee '961, and Fujiwara differs from the prior art the Examiner considered during prosecution of the '240 patent. That analysis also applies to the further combination of Lee '255, Lee '961, and Fujiwara with Hwang.

1. Independent Claim 12

[12pre]	**A semiconductor device, comprising: a memory device including,**

237. I understand that a preamble does not always limit the claim. *See* Appendix 4. To the extent Patent Owner argues this preamble is limiting, it is my opinion that Lee '255 teaches both *a semiconductor device* and that the semiconductor device is a *memory device* because Lee '255 teaches "a three-dimensional (3D) semiconductor memory device and a method of fabricating the same." *See, e.g.*, Ex. 1004 (Lee ' 255), ¶[0002]; *see also, e.g., id.*, Abstract, Figs. 1A-5B, [0074] (teaching "3D semiconductor memory device").

[12a]	**a gate structure**

238. This limitation is the same as [1a], and is obvious for the same reasons.

[12b]	**including a first high work function gate electrode,**

239. This limitation is similar to claim 9, and is obvious for the same reasons.

[12c]	**a channel positioned between and electrically connecting a first diffusion region and a second diffusion region,**

240. This limitation is the same as limitation [1c], and is obvious for the same reasons.

[12d]	**wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and**

241. This limitation is identical to claim 5, and is obvious for the same reasons.

[12e]	**a tunnel dielectric layer,**

242. This limitation is the same as limitation [1e], and is obvious for the same reasons.

[12f]	**a multi-layer charge trapping layer, and**

243. This limitation is the same as limitation [1f], and is obvious for the same reasons.

[12g]	**a blocking dielectric layer disposed between the gate structure and the channel,**

244. This limitation is the same as limitation [1g], and is obvious for the same reasons.

[12h]	**wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,**

245. This limitation is the same as the first portion of limitation [1h], and is obvious for the same reasons.

[12i]	**wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride; and**

246. This limitation is the same as limitation [1i], and is obvious for the same reasons.

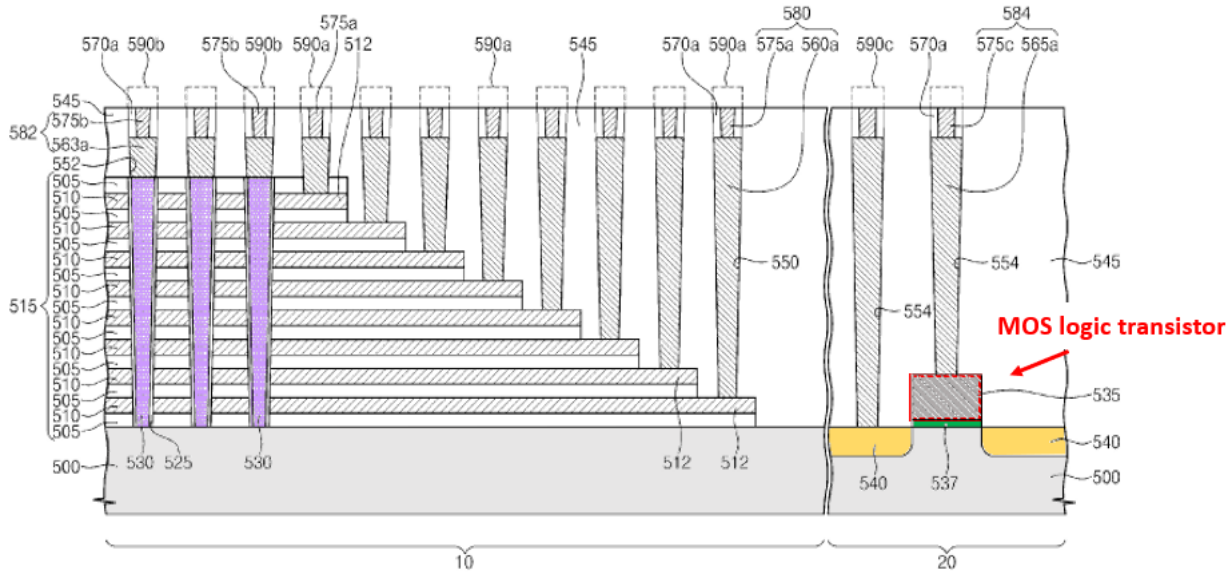
[12j]	**a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.**

247. As set forth above, it is my opinion that a POSITA would have understood that the memory transistors of Lee ’255 would have been designed to work in conjunction with a MOS logic transistor.

248. Hwang teaches an example of such a peripheral MOS transistor that a POSITA would have utilized with Lee ’255. Specifically, Hwang teaches that, in 3D memory configurations like Lee ’255’s, MOS logic transistors can be provided in peripheral circuit region 20. Hwang (Ex. 1048), [0112]-[0113]. Hwang

illustrates an example of a peripheral MOS logic transistor in Fig. 6, reproduced below in annotated form.

Fig. 6



Hwang (Ex. 1048), Fig. 6, [0112].

249. Hwang teaches that its peripheral MOS logic transistor includes peripheral gate 535 (gray with red border), peripheral gate dielectric layer 537 (green), and peripheral source/drain regions 540 (gold). *Id*., [0113]. A POSITA would also have understood there to be a channel in substrate 500 between the peripheral source/drain regions 540 for the MOS logic transistor to function. *See* Part III.C generally. Hwang further teaches that "[t]he peripheral gate dielectric layer 537 may include an oxide layer, a nitride layer, an oxynitride layer, and/or a high-k dielectric layer." *Id*. The foregoing teaches *a metal oxide semiconductor (MOS) logic device* (MOS logic transistor including peripheral gate 535, peripheral

gate dielectric layer 537, peripheral source/drain regions 540, and channel) *including a gate oxide layer* (peripheral gate dielectric layer 537 that can be made of oxide). *See, e.g.,* Ex. 1007 (Lukasiak), [000003-000004], Fig. 4 (discussing history of MOSFET designs).

250. Hwang further teaches *a second high work function gate electrode disposed thereon* because it teaches that:

> the peripheral gate 535 may include at least one of a doped semiconductor layer (e.g., a **doped silicon layer**), a conductive metal nitride layer (e.g., a titanium nitride layer or a **tantalum nitride layer**), a metal layer (e.g., a tungsten layer or an aluminum layer), a transition metal layer (e.g., a titanium layer or a tantalum layer), and a metal-semiconductor compound layer (e.g., a metal silicide layer).

Ex. 1048 (Hwang), Fig. 6 (showing gate 535 disposed on gate dielectric layer 537), [0113].

251. In the context of the SONONOS configuration taught by the combination of Lee '255, Lee '961, Fujiwara, and Hwang described above, a POSITA would have understood that doped silicon and tantalum nitride are *high work function* materials, or would have considered it obvious to utilize *high work function* materials for the gate electrodes (both for the memory and logic

transistors),[9] for at least the reasons set forth in claim 9, Ground 1. *See* claim 9, *supra* (explaining that tantalum nitride and doped silicon are high work function materials).

252. It is my opinion that a POSITA would have been motivated to modify the combination of Lee '255, Lee '961, and Fujiwara to apply Hwang's teachings of a peripheral MOS logic transistor to optimize the electrical interconnections of the combined device.

253. As an initial matter, it would have been obvious for a POSITA to consult the teachings of Hwang in seeking to implement and improve the memory transistor configuration of Lee '255, Lee '961, and Fujiwara because Hwang is also directed to implementing and improving the configuration of SONOS-type charge trapping memory devices such as those taught in Lee '255, Lee '961, and Fujiwara. Ex. 1048 (Hwang), [0007] (teaching a 3D memory device like Lee '251 and Lee '961), [0047], [0112] (teaching a SONOS-type trap configuration like Lee '255, Lee '961, and Fujiwara), and [0158] (teaching its configuration provides an improved 3D memory device).

[9] Hwang teaches that gate layers 535 (for the MOS logic transistor) and 512 (for the memory transistors) are intended to have the same such *high work function* material composition. *Compare* Ex. 1048 (Hwang), [0046] *with Id*., [0113].

254. A POSITA would have been motivated to apply Hwang's electrical connection and peripheral MOS transistor teachings to the Lee '255 / Lee '961 / Fujiwara 3D memory device teachings discussed in Ground 1 to provide an electrical connection and control system, which is not expressly described in that combination, and obtain the benefit expressly taught in Hwang—simplified fabrication, improved reliability, and enhanced integration. Ex. 1048 (Hwang), [0158] (stating that, by using its "step structure," a "fabrication method may be simplified to improve the throughput of the three dimensional semiconductor memory device. Further, a high reliable and highly integrated three dimensional semiconductor memory device may be realized"). A POSITA would have recognized that Hwang teaches the same vertical-string 3D arrays of memory cell transistors individually defined by gate layers 510, with select gates at the lowermost and uppermost levels (Ex. 1048 (Hwang '744), [0060])—a configuration consistent with Lee '255. Although Lee '255 does not detail its peripheral regions, as that is not its focus, a POSITA would have expected standard peripheral MOS transistors to be present to provide array control, as such circuits were conventional and essential for functional memory operation. *See, e.g.*, Ex. 1057 (Hung) at 2:47-52, 9:36-51, and FIG. 4 (peripheral circuits include MOS transistors for input/output logic); Ex. 1058 (Maejima) [0010], [0061], and [0064] (3D memory arrays include peripheral MOS drivers arranged similarly to Hwang;

Ex. 1059 (Hyundai) at FIGS. 2A-3I and 5:12-15 ("fabrication of flash memory cells, together with peripheral CMOS circuitry"); Ex. 1060 (Lee '690) at [0020]-[0021] (control logic in memory devices); Ex. 1026 (Tanaka), FIG. 7 (arrangement of peripheral circuits analogous to Hwang); Ex. 1052 (Hagemeyer), FIG. 1L (cited by Examiner for its MOS logic teachings during prosecution). Hwang therefore makes explicit what Lee '255 leaves implicit by depicting the peripheral MOS logic transistor and describing its structure in detail. Incorporating Hwang's explicit teaching into Lee '255 would therefore have been a routine design choice for a POSITA, providing improved clarity and reliability of the connection scheme without introducing new materials, new processes, or unconventional circuitry. Accordingly, employing Hwang's peripheral logic and connection strategies in the Lee '255 / Lee '961 / Fujiwara combination would have predictably proper operation while yielding the same fabrication and reliability benefits Hwang describes. A POSITA would have understood that this combination amounts to applying the teachings of Hwang for their intended purpose to improve similar devices in the same way.

255. Further, the benefit of using the peripheral logic device teachings of Hwang in a 3D memory device would have been predictable to a POSITA prior to July 2012. As mentioned above, both Hwang and Lee '255 employ the same vertical-string memory architecture with stacked gate layers and select gates at the

top and bottom (Ex. 1048 (Hwang), [0060]), and such configurations were standard across contemporaneous 3D NAND designs. *See, e.g.*, Ex. 1034 (Lee '247), Fig. 1; Ex. 1035 (Lee '086), Fig. 1; Ex. 1036 (Kim '064), Fig. 1, Ex. 1032 (Yang '696), Fig. 1; Ex. 1033 (Jang), Fig. 1; Ex. 1026 (Tanaka), Fig. 4; and Ex. 1028 (Kim '759), Fig. 6. A POSITA would thus have recognized the compatibility of Hwang's structural and electrical configuration with Lee '255, and would have understood that Hwang's peripheral MOS and interconnect features were interchangeable, well known, and commonly used in similar 3D memory designs. *See, e.g.*, Ex. 1058 (Maejima) [0010], [0061], and [0064] (three-dimensional memory arrays include peripheral MOS drivers arranged similarly to Hwang); Ex. 1026 (Tanaka), FIG. 7 (arrangement of peripheral circuits analogous to Hwang). Therefore, a POSITA would have understood that the structural and electrical features of Lee '255 and Hwang were common and interchangeable, making it obvious to adopt Hwang's connection scheme in Ex. 1004 (Lee '255) to ensure proper device control. Accordingly, applying the teachings of Hwang to the Lee '255/Lee '961/Fujiwara combination would have amounted to combining prior art elements according to known methods to obtain predictable results.

256. A POSITA also would have expected success in applying Hwang's electrical connection teachings to the 3D memory framework of the Lee '255 (Ex. 1004) / Lee '961 (Ex. 1005) / Fujiwara (Ex. 1006) because the underlying device

architectures were the same. Hwang's use of vertical NAND strings was entirely consistent with these references, which each disclose vertical word-line memory cell strings implemented with conventional ONO/ONNO charge-traps. Incorporating Hwang's explicit connection details into this framework would not have required new materials, fabrication steps, or circuit innovations, but only the application of a familiar connection strategy that was already well understood in 3D NAND technology by 2012.

2. Dependent Claims 13-15

[13pre].	**The semiconductor device of claim 12,**

257. This limitation is the same as limitation [6pre], and is obvious for the same reasons.

[13a]	**wherein the first dielectric layer of the multi-layer charge trapping layer is disposed abutting the tunnel dielectric layer and substantially trap free, and**

258. This limitation is similar to limitation [6a], and is obvious for the same reasons.

[13b]	**wherein the second dielectric layer is disposed abutting the blocking dielectric layer.**

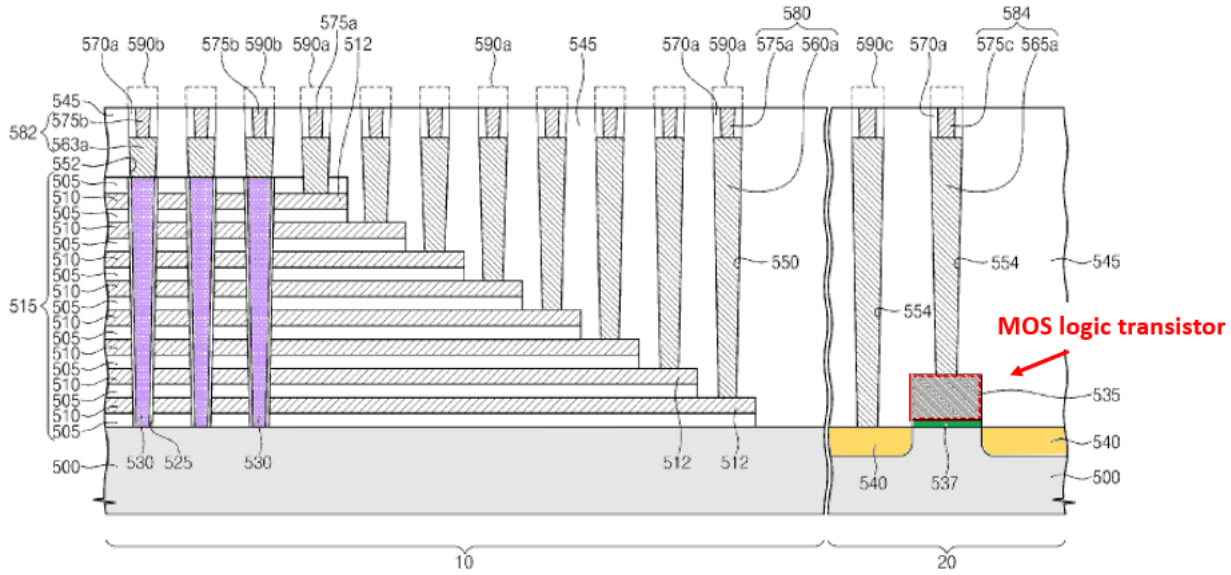
259. This limitation is the same as limitation [6b], and is obvious for the same reasons.

14.	**The semiconductor device of claim 12, wherein the MOS logic device is formed at least partially within a semiconductor material structure.**

260. I understand that claim 14 depends from claim 12 and therefore has all of the requirements of claim 12. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, Fujiwara, and Hwang teaches each and every limitation of claim 12.

261. It is my opinion that Hwang teaches the additional limitations of claim 14 because it teaches a MOS transistor made up of peripheral gate 535, peripheral gate dielectric layer 537, source/drain regions 540, and the channel between source/drain regions 240 (*the MOS logic device* as set forth in claim 12) arranged at least partially within (e.g., at least source/drain regions 540 and the channel therebetween are below the top surface of) substrate 100 (*the semiconductor material structure* as set forth in claim 5). This arrangement is shown in annotated Fig. 6, below:

Fig. 6



Ex. 1048 (Hwang), Fig. 6, [0113].

262. A POSITA would have understood that the positioning of the *MOS logic device* of Hwang vis-à-vis its substrate 500 mirrors the positioning of MOS logic transistor 302 and substrate 306 in figure 3 of the ’240 patent (as shown in the annotated version of figure 3 below), which is the only embodiment of the ’240 patent that sets forth that arrangement. A POSITA also would have been motivated to look to Hwang for this teaching because Hwang, like Lee ’255 and Lee ’961, is directed to 3D NAND SONOS-type architectures (with Lee ’961 specifically teaching a SONONOS variant), and its integration of select MOS devices vis-à-vis the substrate is entirely conventional in NAND design.

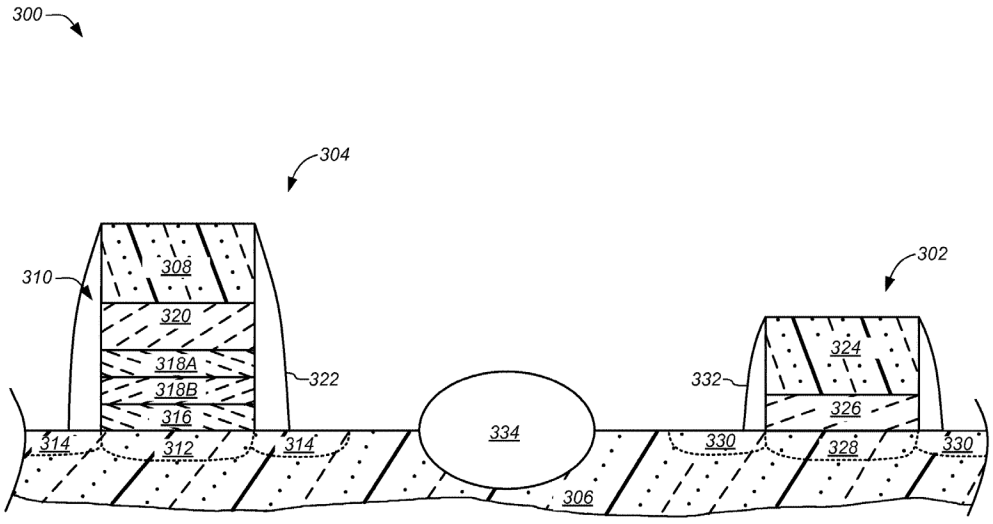


FIG. 3

Ex. 1001 (’240 patent), Fig. 3, 8:10-40.

15.	**The semiconductor device of claim 14, wherein the channel is vertical and oriented substantially orthogonal to the semiconductor material structure.**

263. I understand that claim 15 depends from claim 14, which depends from claim 12 and therefore that claim 15 has all of the requirements of claims 12 and 14. As I have explained above, it is my opinion that the combination of Lee ’255, Lee ’961, Fujiwara, and Hwang teaches each and every limitation of claims 12 and 14.

264. This claim is almost identical to limitation [12d], differing only in that it recites the channel is “oriented substantially orthogonal to the semiconductor material structure” instead of limitation [12d]’s “oriented substantially perpendicular to a semiconductor material structure.” But a POSITA would have

understood "orthogonal" and "perpendicular" to have similar meanings, and thus would have considered claim 15 obvious for the same reasons as limitation [12d]. *See, e.g.*, Ex. 1049 (American Heritage Excerpts) (defining "orthogonal" as "[r]elating to or composed of right angles" and "perpendicular" as "[b]eing at right angles to the horizontal; vertical"); Ex. 1055 (Merriam-Webster Excerpts); Ex. 1056 (New Oxford Excerpts).

3. Independent Claim 16

[16pre]	**A semiconductor device, comprising: a memory device including,**

265. This limitation is the same as limitation [12pre], and is obvious for the same reasons.

[16a]	**a gate structure**

266. This limitation is the same as limitation [12a], and is obvious for the same reasons.

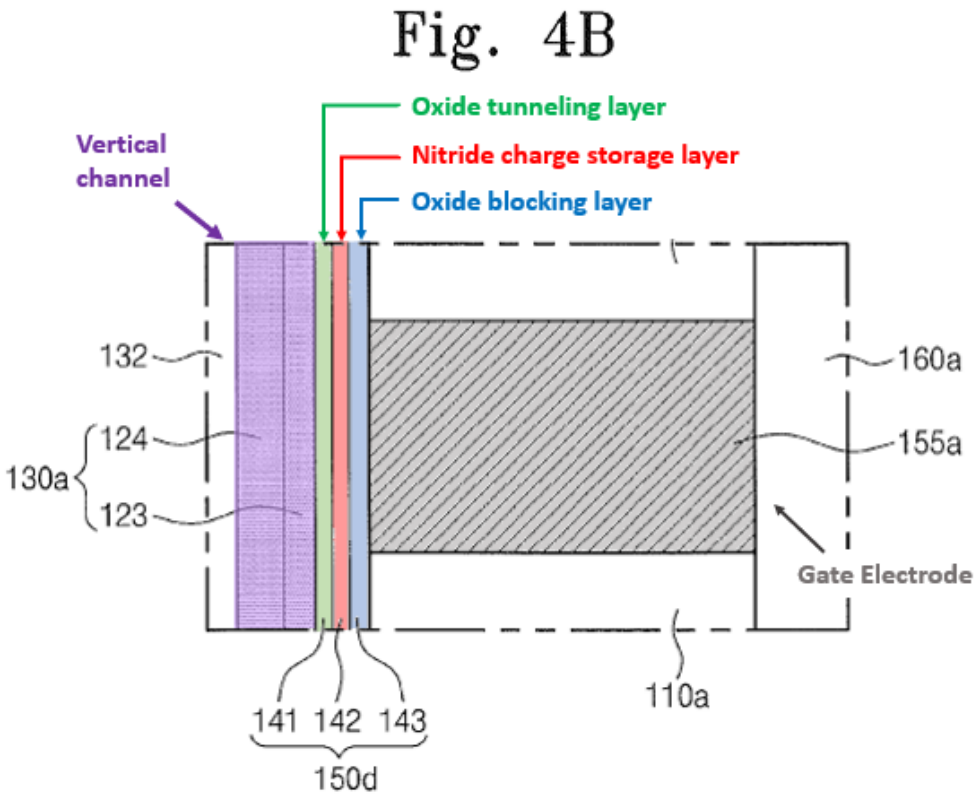
[16b]	**including a first high work function gate electrode,**

267. This limitation is the same as limitation [12b], and is obvious for the same reasons.

[16c]	**a blocking dielectric layer disposed abutting the gate structure,**

268. This limitation is similar to limitation [1g], but recites the blocking layer is "disposed abutting the gate structure" rather than [1g]'s recitation that it is

"disposed between the gate structure and the channel." Limitation [16c] is obvious for the same reasons as [1g], and because Lee '255 teaches, as shown in annotated figure 4B below, that the blocking dielectric layer 143 (*blocking dielectric layer*), shaded in blue, is adjacent (*disposed abutting*) gate electrode 155a (*gate structure*), shaded in gray.



Ex. 1004 (Lee '255), Fig. 4B.

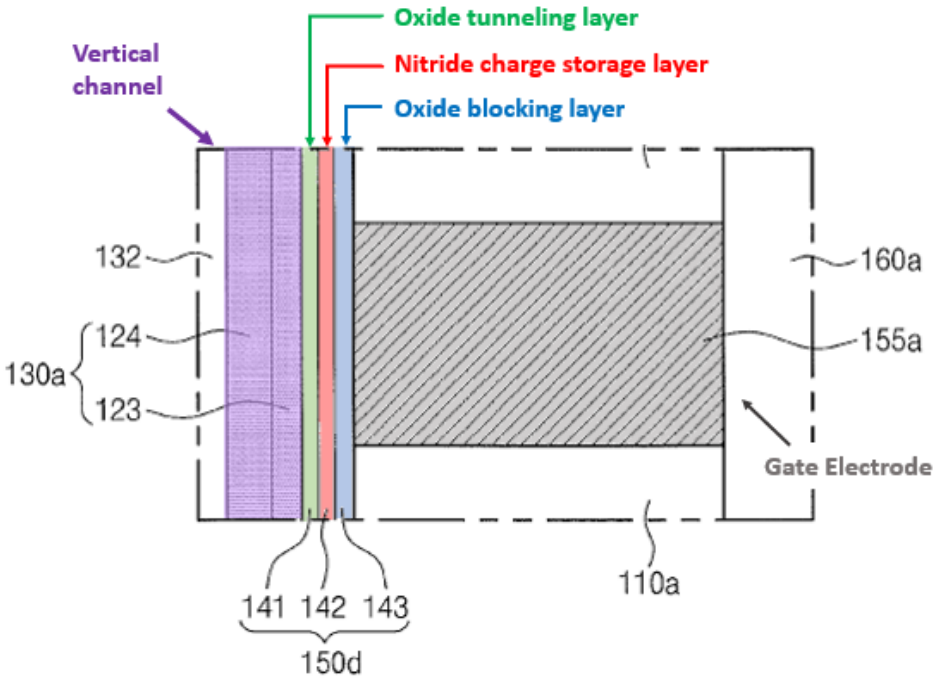
269. As set forth in [1g], Lee '961 teaches the same arrangement of its blocking oxide layer 25A adjacent gate 23A (Ex. 1005 (Lee '961), Fig. 2b), reinforcing the teachings of Lee '255 in the combination of Lee '255, Lee '961, and Fujiwara.

[16d]	**a multi-layer charge trapping layer disposed abutting the blocking dielectric layer,**

270. This limitation recites "a multi-layer charge trapping layer" like limitation [1f], but additionally recites that it is "disposed abutting the blocking dielectric layer." Limitation [16d] is obvious for the same reasons as [1f], and because both Lee '255 and Lee '961 teach arranging their respective charge trapping layers adjacent to their blocking dielectric layers.

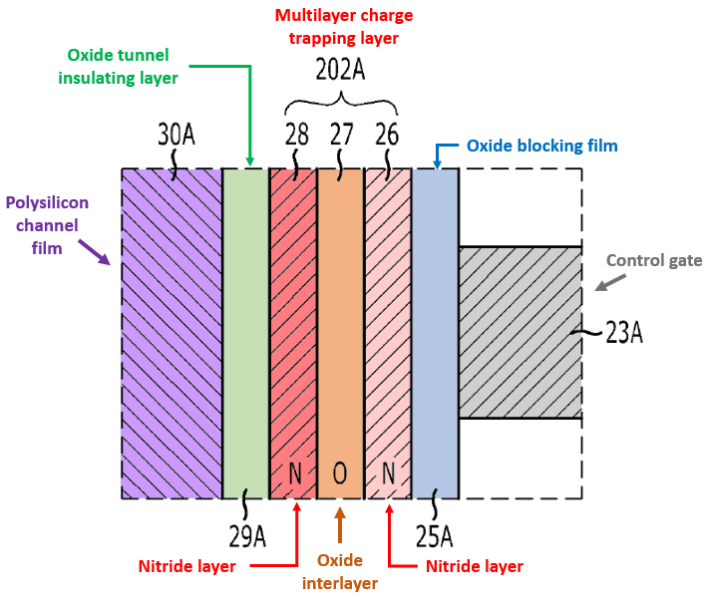
271. First, Lee '255 teaches, as shown in annotated figure 4B below, that its charge storage layer 142 (*charge trapping layer*), shaded in red, is adjacent (*disposed abutting*) blocking dielectric layer 143 (*blocking dielectric layer*), shaded in blue.

Fig. 4B



Ex. 1004 (Lee ’255), Fig. 4B.

272. Second, Lee ’961 teaches, as shown in annotated figure 2b below, that its multilayered charge trap layer 202A (*a multi-layer charge trapping layer*) shaded in dark red, orange, and light red, is adjacent (*disposed abutting*) blocking dielectric layer 25A (*blocking dielectric layer*), shaded in blue.



Ex. 1005 (Lee ’961), Fig. 2b.

273. As I explained in connection with limitation [1f], a POSITA would have been motivated to modify the charge storage layer 142 of Lee ’255 based on Lee ’961’s teachings of a multilayer charge storage layer 202A, resulting in a multilayer charge storage region in Lee ’255, modeled on region 202A of Lee ’961. A POSITA would have understood that the position of the modified charge trapping region in Lee ’255 would have remained the same—i.e., it would be

formed adjacent blocking dielectric layer (blue), as is shown in figure 2b of Lee '961.

[16e]	**wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,**

274. This limitation is the same as the first portion of limitation [1h], and is obvious for the same reasons.

[16f]	**wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride,**

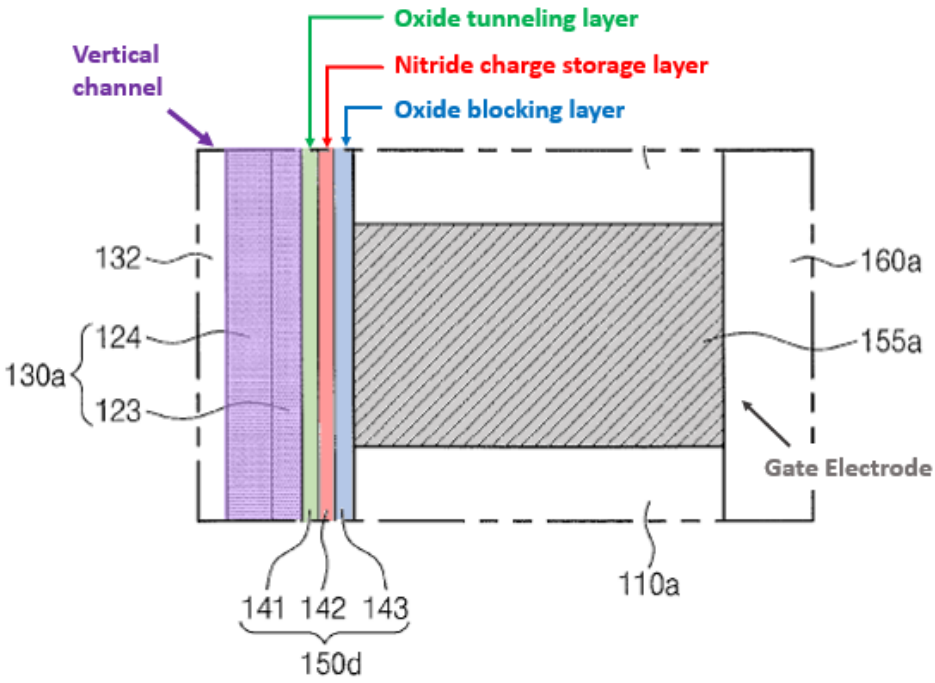
275. This limitation is the same as limitation [1i], and is obvious for the same reasons.

[16g]	**a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer, and**

276. This limitation recites "a tunnel dielectric layer" like limitation [1e], but additionally recites that it is "disposed abutting the multi-layer charge trapping layer." Limitation [16g] is obvious for the same reasons as [1e], and because the combination of Lee '255 and Lee '961 teaches arranging a *multi-layer charge trapping layer* (Lee '961's multilayered charge trap layer 202A) abutting *a tunnel dielectric layer* (Lee '255's tunnel dielectric layer 141, Lee '961's tunnel insulating layer 29A)

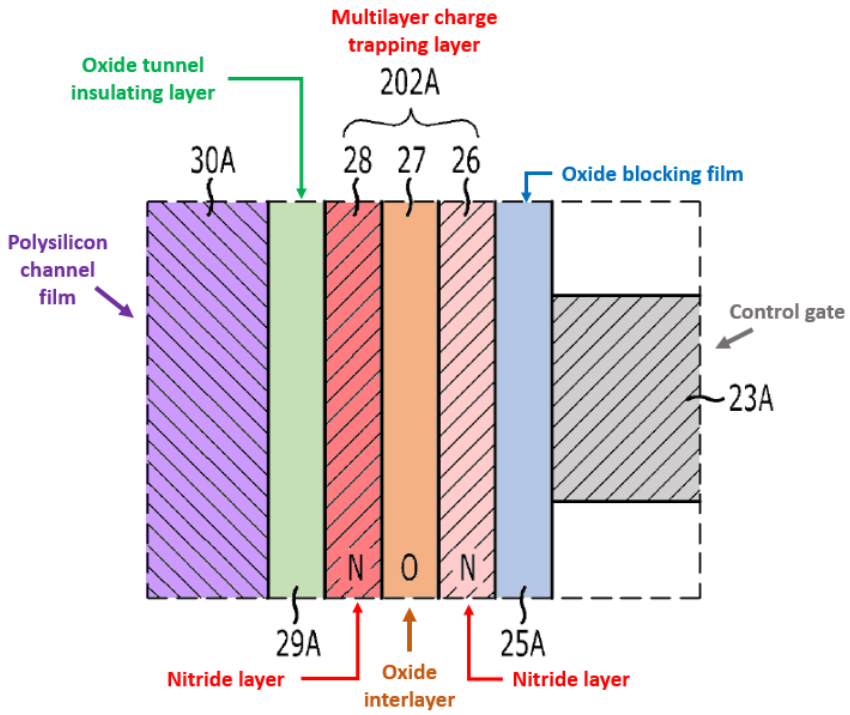
277. First, Lee ’255 teaches, as shown in annotated figure 4B below, that its tunnel dielectric layer 141 (*tunnel dielectric layer*), shaded in green, is adjacent (*disposed abutting*) charge storage layer 142 (*charge trapping layer*), shaded in red.

Fig. 4B



Ex. 1004 (Lee ’255), Fig. 4B.

278. Second, Lee ’961 teaches, as shown in annotated figure 2b below, that its tunnel insulating layer 29A (*a tunnel dielectric layer*), shaded green, is adjacent (*disposed abutting*) multilayered charge trap layer 202A (*a multi-layer charge trapping layer*) shaded in dark red, orange, and light red.



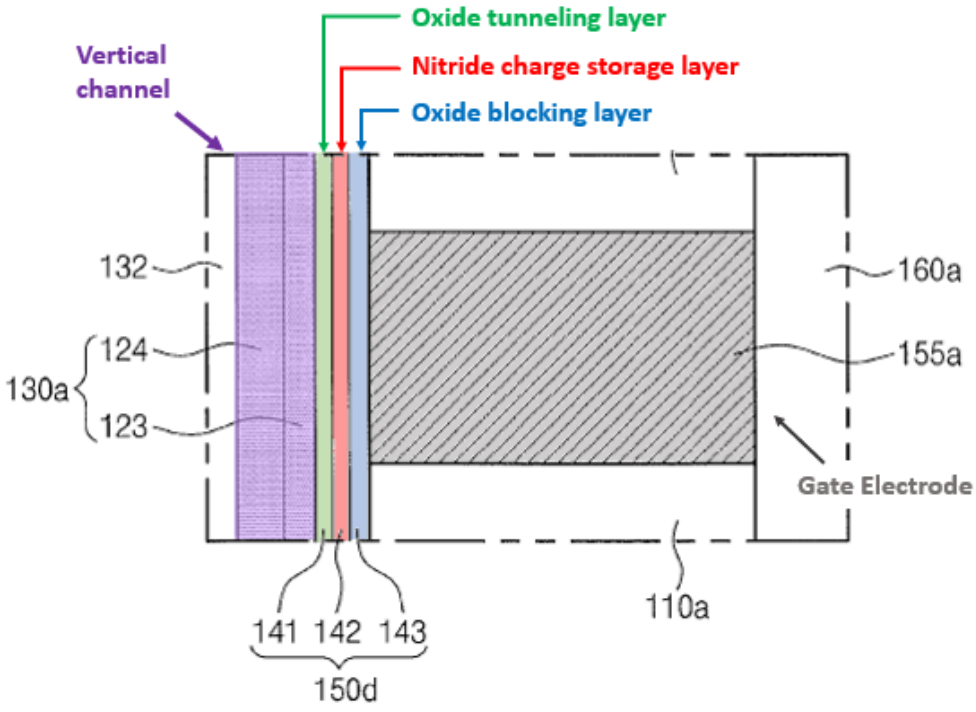
Ex. 1005 (Lee '961), Fig. 2b.

279. As I explained in connection with limitation [1f], a POSITA would have been motivated to modify the charge storage layer 142 of Lee '255 based on Lee '961's teachings of a multilayer charge storage layer 202A, resulting in a multilayer charge storage region in Lee '255, modeled on region 202A of Lee '961. A POSITA would have understood that the position of the modified charge trapping region in Lee '255 would have remained the same—i.e., it would be formed adjacent tunnel dielectric layer (green), as is shown in figure 2b of Lee '961.

[16h]	**a channel disposed abutting the tunnel dielectric layer, wherein the channel is positioned between and electrically connecting a first diffusion region and a second diffusion region,**

280. This limitation is similar to limitation [1c], but additionally recites that the channel is "disposed abutting the tunnel dielectric layer." Limitation [16h] is obvious for the same reasons as [1c], and because Lee '255 teaches, as shown in annotated figure 4B below, that *channel* (vertical active patterns 130/130a), shaded in purple, is adjacent (*disposed abutting*), its tunnel dielectric layer 141 (*tunnel dielectric layer*), shaded in green.

Fig. 4B



Ex. 1004 (Lee '255), Fig. 4B.

281. As set forth in [1c], Lee '961 teaches the same arrangement of its channel 30A adjacent its tunnel insulating layer 29A (Ex. 1005 (Lee '961), Fig. 2b), reinforcing the teachings of Lee '255 in the combination of Lee '255, Lee '961, and Fujiwara.

[16i]	**wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and**

282. This limitation is the same as claim 5, and is obvious for the same reasons.

[16j]	**a metal oxide semiconductor (MOS) logic device including a gate oxide layer and a second high work function gate electrode disposed thereon.**

283. This limitation is the same as limitation [12j], and is obvious for the same reasons.

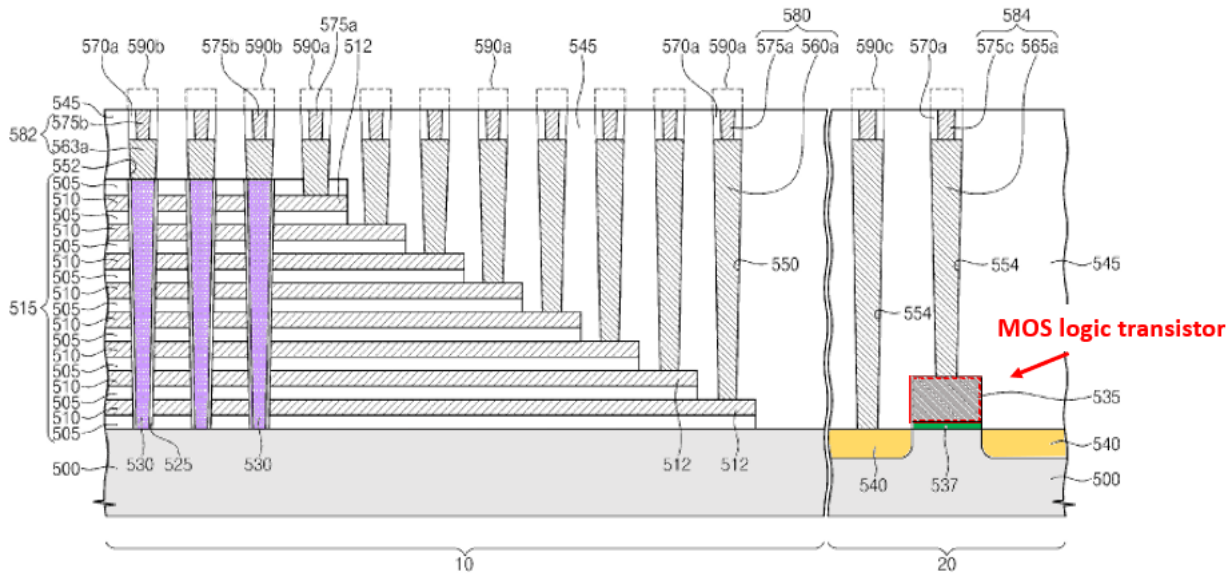
4. Dependent Claims 17, 18

17.	**The semiconductor device of claim 16, wherein the MOS logic device is formed at least partially on the semiconductor material structure.**

284. I understand that claim 17 depends from claim 16 and therefore has all of the requirements of claim 16. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, Fujiwara, and Hwang teaches each and every limitation of claim 16.

285. It is my opinion that Hwang teaches the additional limitations of claim 17 because it teaches a MOS transistor made up of peripheral gate 535, peripheral gate dielectric layer 537, source/drain regions 540, and the channel between source/drain regions 240 (*the MOS logic device* as set forth in claim 12) that is arranged at least partially on (e.g., peripheral gate 535 and peripheral gate dielectric layer 537 are above the top surface of) substrate 500 (*the semiconductor material structure* as set forth in claim 5). This arrangement is shown in annotated figure 6, below:

Fig. 6



Hwang (Ex. 1048), Fig. 6, [0113].

286. A POSITA would have understood that the positioning of the *MOS logic device* of Hwang vis-à-vis its substrate 500 mirrors the positioning of MOS logic transistor 302 and substrate 306 in figure 3 of the '240 patent (as shown in

the annotated version of figure 3 below), which is the only embodiment of the ’240 patent that sets forth that arrangement. A POSITA also would have been motivated to look to Hwang for this teaching because Hwang, like Lee ’255 and Lee ’961, is directed to 3D NAND SONOS-type architectures (with Lee ’961 specifically teaching a SONONOS variant), and its integration of select MOS devices vis-à-vis the substrate is entirely consistent with conventional NAND design.

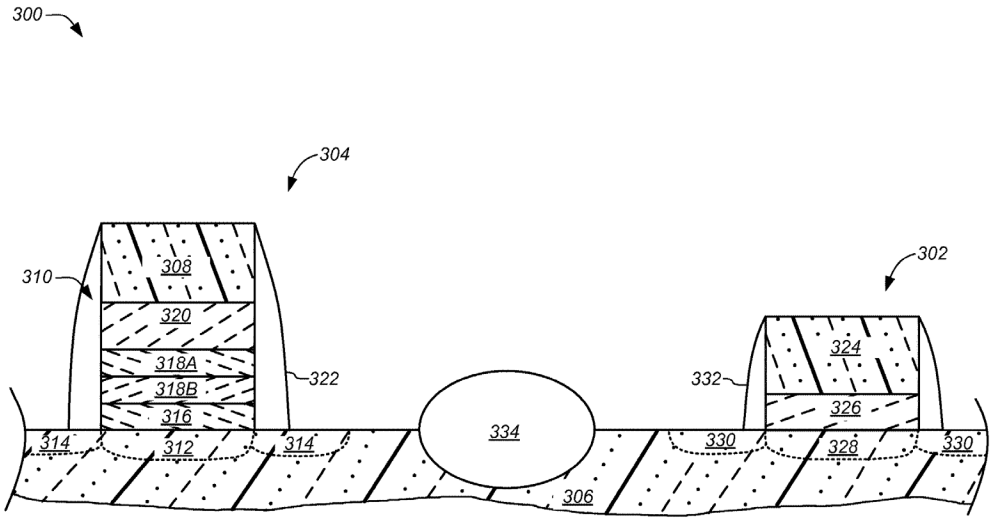


FIG. 3

Ex. 1001 (’240 patent), Fig. 3, 8:10-40.

18.	**The semiconductor device of claim 16, wherein the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first and second dielectric layers, and wherein the anti-tunneling layer includes an oxide layer.**

287. I understand that claim 18 depends from claim 16 and therefore has all of the requirements of claim 16. As I have explained above, it is my opinion that the combination of Lee '255, Lee '961, and Fujiwara teaches each and every limitation of claim 16.

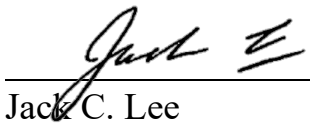
288. This limitation is the same as the second portion of limitation [1h] and is obvious for the same reasons.

X. CONCLUSION

289. I declare that all statements made herein are true to the best of my knowledge, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on October 13, 2025

By:



Jack C. Lee

APPENDIX 1: CURRICULUM VITAE OF JACK C. LEE

Jack C. Lee
Professor Emeritus
Electrical and Computer Engineering Department
The University of Texas at Austin

Current Status
Professor Emeritus
Department of Electrical and Computer Engineering
The University of Texas at Austin

Research / teaching experience and expertise:

- Integrated circuits manufacturing
- Photovoltaic/solar cell technologies
- Alternative channel devices
- Dielectric and passivation processes
- Display technologies
- Semiconductor memory devices

Education

9/84 – 8/88	Ph.D., Electrical Engineering, University of California at Berkeley
9/80 – 12/81	M.S., Electrical Engineering, University of California at Los Angeles
9/76 – 6/80	B.S., Electrical Engineering (with highest honors), University of California at Los Angeles

Professional Career

9/23 – present	Professor Emeritus Department of Electrical and Computer Engineering The University of Texas at Austin
9/00 – 8/23	Cullen Trust for Higher Education Endowed Professorship in Engineering #4 Department of Electrical and Computer Engineering The University of Texas at Austin
9/96 – 8/23	Professor, Department of Electrical and Computer Engineering The University of Texas at Austin
9/92 – 8/96	Associate Professor, Department of Electrical and Computer Engineering The University of Texas at Austin
9/88 – 8/92	Assistant Professor, Department of Electrical and Computer Engineering The University of Texas at Austin
1/88 – 6/88	Lecturer, Electrical Engineering and Computer Science Department University of California at Berkeley
6/79 – 8/84	Member of Technical Staff, High-Speed Bipolar Device Program TRW Microelectronics Center, Redondo Beach, CA

Honors and Awards

IEEE Electron Devices Society Distinguished Lecturer, 2004 - 2016.

Fellow, The Institute of Electrical and Electronic Engineers (IEEE), 2002 "For contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices"

Gordon Lepley IV Endowed Memorial Teaching Award, ECE Department, The University of Texas at Austin, 2004

Cullen Trust For Higher Education Endowed Professorship in Engineering, 2000-present
Dean's Fellow, College of Engineering, The University of Texas at Austin, 1999, 2003
Lockheed Fort-Worth Division Award for Excellence in Engineering Teaching, College of Engineering, The University of Texas at Austin, 1996
Award of Excellence, Halliburton Foundation, 1993
Departmental Teaching Award, College of Engineering, The University of Texas at Austin, 1993
SRC Inventor Recognition Award, Semiconductor Research Corporation, 1991
Hughes Aircraft Company Endowed Faculty Fellowship in Engineering, The University of Texas at Austin, 1991- 2000
Outstanding Engineering Teaching by an Assistant Professor, College of Engineering, The University of Texas at Austin, 1991
Best Paper Award, SEMATECH Centers of Excellence Coordination Meeting, 1990.
Dow Outstanding Young Faculty Award, American Society for Engineering Education, 1990
Engineering Research Initiation Award, Engineering Foundation of the United Engineering Trustees, 1989
Best Paper Award, IEEE International Reliability Physics Symposium, 1988

Litigation Experience as Testifying Experts
The following is a list of cases in which I have provided expert testimony, including through a declaration, report or testimony at deposition or trial since 2016

- Marlin Semiconductor Limited v. TSMC
  April 2025 –
  (Representing defendant, TSMC)

- Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Mfg. Co. Ltd
  October 2024 –
  (Representing defendant, TSMC)

- Yangtze Memory Technologies v. Micron
  January 2024 –
  (Representing defendant, Micron)

- BeSang v. Micron
  March 2023 –
  (Representing defendant, Micron)

- The Trustees of Purdue University v. Wolfspeed, Inc.
  February 2022 – March 2025
  (Representing defendant, Wolfspeed)

- GlobalFoundries - IPR
  March 2021 –
  (Representing petitioner and filed an IPR declaration)

- HD Silicon Solutions LLC v. Microchip Technology Inc.
  January 2021 – February 2025
  (Representing defendant, Microchip Technology Inc.)

- Longitude Licensing Limited vs Western Digital
  March 2023 – January 2024
  (Representing defendant, Western Digital)

- Impinj, Inc. v. NXP USA, Inc.
  September 2019 – July 2023
  (Representing defendant, NXP USA, Inc.)

- Monterey Research, LLC v. Qualcomm Inc.
  February 2020 – May 2022
  (Representing defendant, Qualcomm)

- Bell Semiconductor, LLC v. Texas Instruments Incorporated
  July 2020 – March 2021
  (Representing defendant, Texas Instruments)

- Greenthread LLC v. Samsung
  February 2020 – July 2020
  (Representing plaintiff, Greenthread LLC)

- MLC Intellectual Property LLC vs. Micron Technology, Inc.,
  June 2016 – January 2021
  (Representing plaintiff, MLC Intellectual Property LLC)

- Hanwha v. LONGi Solar Technology
  April 2019 – June 2020
  (Representing defendant LONGi Solar Technology)

- Vista Peak Ventures, LLC v. Innolux Corp.
  January 2019 – March 2019
  (Representing IPR Petitioner, Innolux Corp.)

- Home Semiconductor Corp. v. Samsung
  August 2018 – June 2020
  (Representing plaintiff, Home Semiconductor Corp.)

- Mariner IC Inc. v. Asustek Computer Inc.
  May 2018 – August 2019
  (Representing plaintiff, Mariner IC Inc.)

- Godo Kaisha IP Bridge 1 v. OmniVision Technologies, Inc.

January 2018 – December 2018
(Representing defendant, OmniVision Technologies, Inc.)

- Macronix v. Toshiba
  May 2017 – February 2018
  (Representing defendant, Toshiba)

- University of Illinois v. Micron Technology
  September 2009 – November 2017
  (Representing plaintiff, Univ. of Illinois)

- Silicon Genesis v. Soitec
  October 2016 – March 2017
  (Representing plaintiff, Silicon Genesis)

Non-Litigation Consulting

- Applied Materials, Inc.
  Teaching short courses on semiconductor physics, devices, design/layout, and fabrication technologies (2-3 courses per year).

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Publications
Jack C. Lee
Refereed Journal Publications

1. J. Lee, K. Mayaram and C. Hu, "A Theoretical Study of Gate/Drain Offset in LDD MOSFET's," IEEE Electron Device Letters, vol. EDL-7, no. 3, p. 152 - 154, March 1986.

2. J. Lee, I-C Chen and C. Hu, "Comparison Between CVD and Thermal Oxide Dielectric Integrity," IEEE Electron Device Letters, vol. EDL-7, no. 9, p. 506 - 509, September 1986.

3. K. Mayaram, J. Lee and C. Hu, "A Model for the Electric Field in Lightly Doped Drain Structures," IEEE Transactions on Electron Devices, vol. ED-34, no.7, p. 1509 - 1518, July 1987.

4. J. Lee and C. Hu, "Polarity Asymmetry of Oxides Grown on Polycrystalline Silicon," IEEE Transactions on Electron Devices, vol. ED-35, no. 7, p. 1063 - 1070, July 1988.

5. J. Lee, C. Hegarty and C. Hu, "Electrical Characteristics of MOSFET's Using Low-Pressure Chemical Vapor Deposited Oxide," IEEE Electron Device Letters, vol. EDL-9, no. 7, p. 324 - 327, July 1988.

6. J. Lee, I-C Chen and C. Hu, "Modeling and Characterization of Gate Oxide Reliability," Special Issue of IEEE Transactions on Electron Devices on Reliability, Vol. ED-35, no. 12, p. 2268 - 2278, December 1988.

7. H. Hwang, W. Ting, D. L. Kwong, J. Lee, L. Buhrow and R. Bowling, "Electrical Characteristics of Reoxidized-nitrided CVD Oxide," Applied Physics Letters, 55(8), p. 755 - 756, 21 August, 1989.

8. R. Moazzami, J. Lee and C. Hu, "Temperature Acceleration of Time-Dependent Dielectric Breakdown," Special issue of IEEE Transactions on Electron Devices on Vacuum Microelectronic Devices, vol. ED-36, no. 11, p. 2462 - 2465, November 1989.

9. H. Hwang, W. Ting, D.L. Kwong, J. Lee, L. Buhrow and R.A. Bowling, "Effects of Dynamic Stressing on Nitrided and Reoxidized-Nitrided Chemical Vapor Deposited Gate Oxides," IEEE Electron Device Letters, vol. EDL-10, no. 12, p. 568 - 570, December 1989.

10. J. Lin, S. Banerjee, J. Lee, and C. Teng, "Soft Breakdown in Titanium-Silicided Shallow Source/Drain Junction," IEEE Electron Device Letters, vol. EDL-11, no. 5, p. 191 - 193, May 1990.

11. K. Park, S. Batra, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain, and G. Lux, "Anomalous Capacitance-Voltage Behavior Due to Dopant Segregation and

Carrier Trapping in Arsenic-Implanted Polysilicon and Polycide Gates," Applied Physics Letters, vol. 56, no. 23, p.2325 - 2327, June 4, 1990.

12. J. Lin, S. Banerjee, J. Lee, and C. Teng, "Anomalous Current-Voltage Behavior in Titanium-Silicided Source/Drain Junctions," Journal of Applied Physics, vol. 68, no. 3, p. 1082 - 1087, August 1, 1990.

13. H. Hwang, W. Ting, B. Maiti, D.L. Kwong and J. Lee, "Electrical Characteristics of Ultrathin Gate Dielectrics Prepared by Rapid Thermal Oxidation of Si in N_2O," Applied Physics Letters, vol. 57, no. 10, p. 1010 - 1011, Sept. 3, 1990.

14. S. Batra, K. Park, J. Lin, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain and G. Lux "Effects of Dopant Redistribution, Segregation and Carrier Trapping in As-Implanted MOS Gates," IEEE Transactions on Electron Devices, vol. 37, no. 11, p. 2322 - 2330, October, 1990.

15. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "The Impact of Trench Isolation on Latch-up Immunity in Bulk, Non-epitaxial CMOS," IEEE Electron Device Letters, vol. EDL-12, no. 2, p. 77 - 79, February, 1991.

16. W. Ting, H. Hwang, J. Lee and D. L. Kwong, "Composition and Growth Kinetics of Ultrathin SiO_2 Films Formed by Oxidizing Si Substrate in N_2O," Applied Physics Letters, vol. 57, p. 2808 - 2810, 1990.

17. W. Ting, P.C. Li, G. Q. Lo, J. Lee and D.L. Kwong, "Metal-Oxide Semiconductor Characteristics of Rapid Thermal Processed Chemical Vapor Deposited SiO_2 Gate Dielectrics," Solid State Electronics, vol. 34, no. 4, p 385 - 388, 1991.

18. W. Ting, H. Hwang, J. Lee and D.L. Kwong, "Growth Kinetics of Ultrathin SiO_2 Films Prepared by Rapid Thermal Oxidation of Si Substrates in N_2O," Journal of Applied Physics, vol. 70, no. 2, p. 1072 - 1074, July 15, 1991.

19. J. Lin, K. Park, S. Batra, S. Banerjee, J. Lee and G. Lux, "Enhancement of Boron Diffusion Through Gate Oxides in MOS Devices During Rapid Thermal Silicidation," Applied Physics Letters, vol. 58, no. 19, p. 2123 - 2125, May 1991.

20. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "A Physical Model for Boron Penetration Through Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," Applied Physics Letters, vol. 59, no. 13, p. 1581 - 1582, September 23, 1991.

21. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "Improved Reliability Characteristics of Submicron nMOSFET's with Oxynitride Gate Dielectrics Prepared by Rapid Thermal Oxidation in N_2O," IEEE Electron Device Letters, vol. 12, no.9, p.495-497, September 1991.

22. J. Carrano, C. Sudhama, V. Chikarmane, J. Lee, A. Tasch, W. Shepherd and N. Abt, "Electrical and Reliability Properties of PZT Thin Films for ULSI DRAM Applications," IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, vol. 38, no. 6, p. 690 - 703, November 1991.

23. V. Chikarmane, C. Sudhama, J. Kim, J. Lee, A. Tasch and S. Novak, "Comparative Study of The Perovskite Phase Microstructure Evolution and Electrial Properties of PZT Thin Film Capacitors Annealed in Oxygen and Nitrogen Ambients," Applied Physics Letters, vol. 59, no. 22, p. 2850 - 2852, Nov. 25, 1991.

24. M. Hao and J. Lee, "Electrical Characteristics of Oxynitrides Grown on Textured Single-Crystal Silicon," Applied Physics Letters, vol. 60, no. 4, p. 445 - 447, January 27, 1992 .

25. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "Parametric Study of Latchup-Immunity of Deep Trench-Isolated, Bulk, Non-epitaxial CMOS," IEEE Trans. Elec. Dev., vol. 39, no. 4, p. 921 - 931, April 1992.

26. V. Chikarmane, J. Kim, C. Sudhama, J. Lee and A. Tasch, "Annealing of Lead Zirconate Titanate (65/35) Thin Films for Storage Dielectric Applications: Phase Transformations and Electrical Characteristics," Journal of Electronic Materials, vol. 21, no. 5, p. 503 - 512, May 1992.

27. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "Effects of Post-Deposition Annealing Ambient on the Electrical Characteristics and Phase Transformation Kinetics of Sputtered Lead Zirconate titanate (65/35) Thin Film Capacitors," Journal of Vacuum Science and Technology, vol. 10, no. 4, p. 1562 - 1568, July 1992.

28. V.K. Mathews, R. L. Maddox, P.C. Fazan, J. Rosato, H. Hwang and J. Lee, "Degradation of Junction Leakage in Devices Subjected to Gate Oxidation in Nitrous Oxide," IEEE Electron Device Letters, vol. 13, no. 12, p. 648 - 650, Dec. 1992.

29. B. Maiti, M. Hao, I. Lee and J. Lee,"Improved Ultrathin Oxynitride Formed by Thermal Nitridation and Low Pressure Chemical Vapor Deposition Process," Applied Physics Letters, vol. 61, p. 1790 - 1792, 1992.

30. B. Maiti and J. Lee, "Low-Pressure Chemical Vapor Deposited Silicon-Rich Oxides for Non-volatile Memory Applications," IEEE Electron Device Letters, vol. 13, no. 12, p. 624 - 626, Dec. 1992.

31. H. Hwang, M. Y. Hao, J. Lee, V. Mathews, P. Fazan and C. Dennison, "Furnace N_2O Oxidation Process for Submicron MOSFET Device Applications," Solid-State Electronics, vol. 36, p. 749 - 751, 1993.

32. H. Hwang, J. Lee, P. Fazan and C. Dennison, "Hot-Carrier Reliability Characteristics of Narrow Width MOSFETs," Solid-State Electronics, Vol. 36, No. 4, p. 665 - 666, 1993.

33. B. Maiti and J. Lee, "A New Low-Thermal Budget Process for Ultrathin Oxynitride Dielectrics," Journal of Electronic Materials, 1992.

34. J. Lin, W. Chen, S. Banerjee and J. Lee, "Cobalt Disilicide as a Dopant Diffusion Source for Polysilicon Gates in MOS Devices," Journal of Electronic Materials, vol. 22, p. 667 - 673, 1993.

35. W. Chen, J. Lin, S. Banerjee and J. Lee, "Thermal Stability and Dopant Drive-Out Characteristics of $CoSi_2$ Polycide Gates," Journal of Applied Physics, vol. 73, p. 4712 - 4714, May 1993.

36. J. Lee, V. Chikarmane, C. Sudhama, and J. Kim, "Sputtered PZT Thin Films for Memory Applications," Journal of Integrated Ferroelectrics, vol. 3, 1993.

37. C. Sudhama, J. Kim, J. Lee, W. Shepherd and E. Meyer, "The Effects of Lanthanum Doping on the Electrical Properties of Sol-Gel Derived Ferroelectric Lead Zirconate Titanate (PZT) for ULSI DRAM Applications," Journal of Vacuum Science and Technology, p. 1302 - 1309, July / Aug 1993.

38. M. Y. Hao, H. Hwang and J. Lee, "Silicon-Implanted SiO2 for Non-volatile Memory Applications," Solid-State Electronics, vol. 36, p. 1321 - 1324, 1993.

39. M. Y. Hao, H. Hwang and J. Lee, "Memory Effects of Silicon-Implanted Oxides for EEPROM Applications," Applied Physics Letters, vol. 62, No. 13, p. 1530 - 1532, March 1993.

40. S. Batra, K. Picone, K. Park, S. Bhattacharya, S. Banerjee, J. Lee, M. Manning and C. Dennison, "Study of Lateral Non-Uniformity as a Function of Junction Depth in Ultra-Shallow Junctions and Its Effects on Leakage Behavior in As-Deposited Polycrystalline Si and Amorphous Si Diodes," Solid-State Electronics vol. 36, no. 7, p. 955 - 960, 1993.

41. J. Lee, C. Sudhama, J. Kim and R. Khamankar, (Invited Paper) "High Dielectric Constant Ferroelectric Thin Films for DRAM Applications", Extended Abstracts of International Conf. on Solid State Devices and Materials, p. 850 - 852, 1993.

42. W. M. Chen, S. K. Banerjee, and J. C. Lee," Degradation mechanism and improvement of thermal stability of $CoSi_2$/polycrystalline Si layers," Applied Physics Letters, vol. 64, no. 12, p. 1505 - 1507, 1994.

43. W. M. Chen, J. Lin, S. K. Banerjee, and J. C. Lee," Simultaneous Shallow-Junction Formation and Gate Doping p-channel Metal-Semiconductor-Oxide Field-Effect

Transistor Process Using Cobalt Silicide as a Diffusion/Doping Source," Applied Physics Letters, vol. 64, no. 3, p. 345 - 347, 1994.

44. M. Y. Hao, B. Maiti, and J. Lee," Novel Process for Reliable Ultrathin Tunnel Dielectrics," Appl. Phys. Lett., vol.. 64, p. 2102 - 2104, April 1994.

45. B. Jiang, C. Sudhama, R. Khamankar, J. Kim and J. Lee, "Effects of Nonlinear Storage Capacitor on DRAM READ/WRITE," IEEE Electron Device Letters, vol. 15, no. 4, p.126 - 128, April 1994.

46. J. Kim, C. Sudhama, R. Khamankar, B. Jiang, J. Lee, P. Maniar, R. Moazzami, R. Jones and C. J. Mogab, "La Doped PZT Thin Films for Gigabit DRAM Technology," 1994 Symposium on VLSI Tech. Digest, p. 151 - 152, 1994.

47. M. Y. Hao, K. Lai, W. M. Chen, and J. Lee, " Surface Cleaning Effect on Dielectric Integrity for Ultrathin Oxynitrides Grown in N_2O," Applied Physics Letters, vol. 65, no. 9, p. 1133 - 1135, August 1994.

48. K. Lai, M. Y. Hao, C. Y. Hu, W. M. Chen, and J. Lee, " Effects of Surface Preparation on the Electrical and Reliability Properties of Ultrathin Thermal Oxide," IEEE Electron Device Letters, vol. ED-15, no. 11, p. 446 - 448, November, 1994.

49. M. Y. Hao, W. M. Chen, K. Lai, M. Gardner, J. Fulford, and J. Lee, "Correlation of Dielectric Breakdown with Hole Transport for Ultrathin Thermal Oxides and N_2O Oxynitrides," Applied Physics Letters, vol. 66, no. 9, p. 1126 - 1128, February 27, 1995.

50. R. Khamankar, J. Kim, C. Sudhama, B. Jiang, and J. Lee, "Effects of Electrical Stress Parameters on Polarization Loss in Ferroelectric PZT Thin Film Capacitors," Electron Device Letter, p. 130 - 132, April 1995.

51. J. Lee, B. Jiang, R. Khamankar, and J. Kim, "Nonlinearity of Ferroelectric Capacitors on DRAM R/W Operations," Integrated Ferroelectrics, p. 319 - 328, 1995.

52. W. M. Chen, M. Y. Hao, K. Lai, M. Gardner, J. Fulford, and J. Lee, " 'Turn-around' Effects of Stress-Induced Leakage Current of Ultrathin N_2O-Annealed Oxides," Applied Physics Letters, vol. 67, No. 5, p. 1 - 3, July 1995.

53. Kafai Lai, Wei-Ming Chen, Ming-Yin Hao, Mark Gardner, Jim Fulford, Jack C. Lee, "'Turn-around' effects of stress-induced leakage current of ultrathin N_2O-annealed oxides", Applied Physics Letters, vol. 67, no. 5, p. 673-5, Jul. 31, 1995.

54. Kafai Lai, Kiran Kumar, Anthony I. Chou, and Jack C. Lee, "Plasma damage and photo-annealing effects of thin gate oxides and oxynitrides during O_2 plasma exposure", IEEE Elec. Dev. Lett., vol. 17, no. 3, p. 82, Mar. 1996.

55. Anthony I. Chou, Kafai Lai, Kiran Kumar, Mark Gardner, Jim Fulford, and Jack C. Lee, "Optimization of gate dopant concentration and microstructure for improved electrical and reliability characteristics of ultrathin oxides and N_2O-oxynitrides", Applied Physics Letters, vol. 69, no. 7, p. 934, Aug. 12, 1996.

56 C. Lin, A. Chou, K. Kumar, P. Chowdhury, and J. C. Lee, "Effect of BF_2 implantation on ultra-thin gate oxide reliability" Appl. Phys. Lett., vol. 69, no. 11, p1591, Sep. 1996.

57. C. Lin, A. Chou, K. Kumar, P. Chowdhury, and J. C. Lee, "Reliability of gate oxide grown on nitrogen-implanted Si substrate" Appl. Phys. Lett. Vol. 69, No. 24, 9 Dec. 1996.

58. K. Kumar, A. Chou, C. Lin, P. Choudhury, and J. C. Lee, "Optimization of sub 3 nm gate dielectrics grown by rapid thermal oxidation in a nitric oxide ambient", Appl. Phys. Lett. 70 (3), 20 January 1997.

59. Prasenjit Chowdhury, Anthony I. Chou, Kiran Kumar, Chuan Lin and Jack C. Lee, "Improvement of Ultra-Thin Gate Oxide and Oxynitirde Integrity Using Fluorine Implantation Techniques," Applied Physics Letters 70 (1), January 6, 1997.

60. A. Chou, K. Lai, K. Kumar, P. Chowdhury and J. Lee, "Modeling of Stress-Induced Leakage Current in Ultra-Thin Oxide with the Trap Assisted Tunneling Mechanism," Applied Physics Lettes, vol. 70, no. 25, Pg. 3407, June 23, 1997.

61. Byoung Hun Lee, Yongjoo Jeon,Keith Zawadzki, Wen-Jie Qi and Jack C. Lee, "Effect of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon", Appl. Phys. Lett. Vol. 74, p. 3143, 1999.

62. Tung-Sheng Chen, Venkatasubramani Balu, Shylaja Katakam, Jian-Hung Lee and Jack C. Lee, “Effects of Ir Electrodes on BST Thin Film Capacitors for High-Density Memory Application” IEEE Transactions on Electron Devices vol. 46, no. 12, p. 2304, Dec. 1999.

63. Jian-Hung Lee, Razak Mohammedali, Venkatasubramani Balu, Jeong Hee Han, Sundar Gopalan, Chun-Hui Wong and Jack C. Lee “The Niobium Doping Effects on Resistance Degradation of Strontium Titanate Thin Film Capacitors”, Applied Physics Letters, vol. 75, no. 10, p. 1455, September 6, 1999.

64. Sundar Gopalan, Chun-Hui Wong, Venkatasubramani Balu, Jian-Hung Lee, Jeong Hee Han, Razak Mohammedali, and Jack C. Lee, “Effects of Nb Doping on the Microstructure and Electrical Properties of Strontium Titanates Thin Films for Semiconductor Memory Applications”, Applied Physics Letters, vol. 75, no. 14, p. 2123, October 4, 1999.

65. T. Ngai, W. Qi, R. Sharma, J. Fretwell, X. Chen, J. Lee and S. Banerjee, "Electrical Properties of ZrO_2 Gate Dielectric on SiGe," Applied Physics Letters, vol. 76, no. 4, p. 502, January 24, 2000.

66. Laegu Kang, Byoung Hun Lee, Wen-Jie Qi, Yongjoo Jeon, Renee Nieh, Sundar Gopalan, Katsunori Onishi, and Jack C. Lee," Electrical Characteristics of Highly Reliable Ultra-Thin Hafnium Oxide Gate Dielectric," IEEE Electron Dev. Lett., vol. 21, 4, p.181, 2000.

67. Byoung Hun Lee, Laegu Kang, Renee Nieh, Wen-Jie Qi, and Jack C. Lee, "Thermal stability and electrical characteristics of Hafnium oxide gate dielectric reoxidized with rapid thermal annealing", Appl. Phys. Lett., 76, p.1926, 2000.

68. A. Lucas, S. Gopalan, J. Lee, S. Kaushal, R. Niino and Y. Tada, "Ultrathin Gate Oxynitrides Grown Using Fast Ramp Vertical Furnace for Sub-130 Nanometer Technology," Electrochemical and Solid-State Letters, vol. 3, no. 8, p. 389-391, August 2000.

69. Wen-Jie Qi, Renee Nieh, Easwar Dharmarajan, Byoung Hun Lee, Yongjoo Jeon, Laegu Kang, Katsunori Onishi, and Jack C. Lee, "Ultrathin zirconium silicate film with good thermal stability for alternative gate dielectric applications", Appl. Phys. Lett., vol. 77, no.11, p. 1704-1706, Sept. 2000.

70. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, Aaron Lucas, and Jack C. Lee, "Electrical and reliability characteristics of ZrO_2 deposited directly on Si for gate dielectric application", Appl. Phys. Lett., vol. 77, no. 20, p.3269, 2000.

71. T. Ngai, W.J. Qi, R. Sharma, J.L. Fretwell, X. Chen, J.C. Lee, and S.K. Banerjee, "Transconductance Improvement in Surface-Channel SiGe pMOSFETs using ZrO_2 Gate Dielectric," Applied Physics Letters, May 14, 2001.

72. P.D. Kirsch, C. S. Kang, J. Lozano, J. C. Lee, J. G. Eckerdt, "Electrical and spectroscopic comparison of HfO2/Si interfaces on nitrided and un-nitrided Si (100)," Journal of Applied Physics, Volume 91, Number 7, pp. 1 – 11, 1 April 2002.

73. H. Cho, C. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, S. Krishnan and Jack Lee, "Structural and Electrical Properties of HfO_2 with Top Nitrogen Incorporated Layer," IEEE Electron Device Letters, vol. 23, no. 5, p. 249, May 2002.

74. S. Gopalan, K. Onishi, R. Nieh, C. Kang, R. Choi, J. Cho, S. Krishnan, and J. Lee, "Electrical and Physical Characteristics of Ultrathin Hafnium Silicate Films with Polycrystalline Silicon and TaN Gates," Applied Physics Letters, vol. 80, no. 23, p. 4416, June 10, 2002.

75. R. Nieh, R. Choi, S. Gopalan, K. Onishi, C. Kang, H. Cho, S. Krishnan and J. Lee, "Evaluation of Silicon Surface Nitridation Effects on Ultra-thin ZrO2 Gate Dielectrics," Applied Physics Letters, vol. 81, no. 9, p. 1663, August 26, 2002.

76. Chang Seok Kang, Hag-Ju Cho, Katsunori Onishi, Renee Nieh, Rino Choi, Sundar Gopalan, Sid Krishnan, Jeong H. Han, and Jack C. Lee, "Bonding states and electrical properties of ultrathin HfOxNy gate dielectrics", Appl. Phys. Lett. 81, p2593, September 30, 2002.

77. Chang Seok Kang, Katsunori Onishi, Laegu Kang, and Jack C. Lee, "Effects of Hf contamination on the properties of silicon oxide metal--oxide--semiconductor devices", Appl. Phys. Lett. 81, p5018, December 23, 2002.

78. Y. Kim, K. Onishi, C. Kang, H. Cho, R. Nieh, S. Gopalan, R. Choi, J. Han, S. Krishnan, and J. Lee, "Area Dependence of TDDB Characteristics for HfO_2 Gate Dielectrics," IEEE Electron Devices Letters, vol. 23, no. 10, p. 594, October 2002.

79. Y. Fan, R. Nieh, J. Lee, G. Lucovsky, G. Brown, F. Register and S. Banerjee, "Voltage and Temperature Dependent Gate Capacitance and Current Model: Application to ZrO2 n-channel MOS Capacitor," IEEE Tran. Electron Devices, vol. 49, no. 11, p. 1969, November 2002.

80. S. Mudanai, F. Li, S. Samavedam, R. Tobin, C. Kang, R. Nieh, L. Register, J. Lee, and S. Banerjee, "Interfacial Defect States in HfO2 and ZrO2 nMOS Capacitor," IEEE Electron Devices Letters, vol. 23, no. 12, p. 728, December 2002.

81. Y.H. Kim, K. Onishi, C. Kang, H. Cho, R. Choi, S. Krishnan, M. Akbar and J. Lee, "Thickness Dependence of Weibull Slopes of HfO_2 Gate Dielectrics," IEEE Electron Devices Letters, vol. 24, no. 1, p. 40, January 2003.

82. Z. Shi, D. Onsongo, K. Onishi, J. Lee, and S. Banerjee, "Mobility Enhancement in Surface Channel SiGe PMOSFETs With HfO_2 Gate Dielectrics," IEEE Electron Device Letter, vol. 24, no. 1, p. 34, January 2003.

83. K. Onishi, C. Kang, R. Choi, H. Cho, S. Gopalan, R. Nieh, S. Krishnan and J. Lee, "Improvement of Surface Carrier Mobility of HfO_2 MOSFET's by High-Temperature Forming Gas Annealing," IEEE Trans. On Electron Devices, vol. 50, no. 2, p. 384 – 390, February 2003.

84. R. Nieh, C. Kang, H. Cho, K. Onishi, R. Choi, S. Krishnan, J. Han, Y. Kim, A. Shahriar and J. Lee, "Electrical Characterization and Material Evaluation of Nitrogen Incorporated ZrO_2 (ZrO_xN_y) Gate Dielectric in TaN-gated NMOSFET's with High Temperature Forming Gas Annealing," IEEE Trans. On Electron Devices, vol. 50, no. 2, p. 333 – 340, February 2003.

85. Rino Choi, Katsunori Onishi, Chang Seok Kang, Hag-Ju Cho, Y.H. Kim, Siddharth Krishnan, M. S. Akbar and Jack C. Lee, " Effects of Deuterium Anneal on MOSFETs with HfO_2 Gate Dielectrics," IEEE Electron Device Letter, vol. 24, no. 3, p. 144, March 2003.

86. Katsunori Onishi, Chang Seok Kang, Rino Choi, Hag-Ju Cho, Young Hee Kim, Siddharth Krishnan, Mohammad Akbar, and Jack C. Lee, "Performance of polysilicon gate HfO_2 MOSFET's on (100) and (111) silicon substrates," IEEE Electron Device Letter, vol. 24, no. 4, p. 254, April 2003.

87. M.S. Akbar, S. Gopalan, H.-J. Cho, K. Onishi, R. Choi, C.S. Kang, Y.H. Kim, J. Han, S. Krishnan, and J. C. Lee, "High Performance TaN/HfSiON/Si MOSCAP and MOSFET Prepared by Low Thermal Budget NH_3 Post-Deposition Anneal," Applied Physics Letters, vol. 82, no.11, pp.1757, March 17 2003

88. K. Onishi, R. Choi, C. Kang, H. Cho, Y. Kim, R. Nieh, J. Han, S. Krishnan, M. Akbar, and J. Lee, "Bias-temperature Instabilities of Polysilicon Gate HfO_2 MOSFET's." IEEE Trans. On Electron Devices, vol. 50, no. 6, p. 1517, June 2003.

89. Chang Seok Kang, H.-J. Cho, R. Choi, K. Onishi, Y.H. Kim, M. S. Akbar, and J. C. Lee, "Characterization of resistivity and work function of sputtered-TaN film for gate electrode applications", Journal of Vacuum Science and Technology, vol. 21, issue #5, p. 2026, September/October 2003.

90. Y. H. Kim, and J. C. Lee, "Reliability Characteristics of high-k dielectrics" invited paper in the Microelectronics Reliability Journal, Volume 44, Issue 2, Pages 183-193, Feb. 2004.

91. Chang Seok Kang, Hag-Ju Cho, Rino Choi, Young-Hee Kim, Chang Yong Kang, Se Jong Rhee, Changhwan Choi, Mohammad Shahariar Akbar, and Jack C. Lee "The Electrical and Material Characterization of Hafnium Oxynitride Gate Dielectrics with TaN-Gate Electrode" IEEE Transactions on Electron Devices, Vol. 51, No. 2, P220-227, FEBRUARY 2004.

92. C.Y. Kang, Hag-Ju Cho, Rino Choi, Chang Seok Kang, Young Hee Kim, Se Jong Rhee, Chang Hwan Choi, Shahriar M. Akbar, and Jack C. Lee, "Effects of dielectric structure of HfO2 on carrier generation rate in Si substrate and channel mobility", App Phy. Lett., vol 84, 12, pp. 2148-2150, 2004.

93. R. Jha, J. Gurganos, Y. H. Kim, R. Choi, J. Lee and V. Misra, "A Capacitance Based Methodology for Extracting Workfunction of Metal Electrodes on High-K Dielectrics," IEEE Electron Device Letters, vol. 25, no. 6, p. 420, June 2004.

94. Rino Choi, Chang Seok Kang, Hag-Ju Cho, Young-Hee Kim, Mohammad S. Akbar, and Jack C. Lee "Effects of high temperature forming gas anneal on the characteristics

of MOSFET with HfO_2 gate stacks," Applied Physics Letter, Vol. 84, Issue 24, p4839-4841, June 14, 2004.

95. S. J. Rhee, C. Y. Kang, C. S. Kang, R. Choi, C. Choi, M. Akbar and J. Lee, ""Effect of Varying Interfacial Oxide and High-k Layer Thicknesses for HfO_2 Metal Oxide Semiconductor Field Effect Transistor" Applied Physics Letter, Vol. 85, p1286, 2004.

96. C.M. Osburn, S.A. Campbell, E. Eisenbraun, E. Garfunkel, T. Gustafson, A. Kingon, D.-L. Kwong, J. Lee, G. Lucovsky, T.P. Ma, J.P. Maria, V. Misra, G. Parsons, D. Schlom, and S. Stemmer, "Materials and Processes for High k Gate Stack", Semiconductor Fabtech Magazine, 2004.

97. Se Jong Rhee, Chang Yong Kang, Chang Seok Kang, Chang Hwan Choi, Rino Choi, Mohammad S. Akbar, and Jack C. Lee, "Threshold Voltage Instability Characteristics under Positive Dynamic Stress in Ultra Thin HfO_2 Metal Oxide Semiconductor Field Effect Transistors," Applied Physics Letters, vol. 85, no. 15, p. 3184, October 2004.

98. M. S Akbar, H. -J. Cho, R. Choi, C. S. Kang, C.Y. Kang, C. H. Choi, S. J. Rhee, Y. H. Kim and Jack C. Lee "Optimized NH_3 Annealing Process for High Quality HfSiON Gate Oxide", in IEEE Electron Device Letters, vol. 25 (7), pp. 465-467, 2004.

99. Akbar, M.S.; Moumen, N.; Barnett, J.; Lee, B.-H.; Lee, J.C, "Mobility Improvement after HCI Post-Deposition Cleaning of High-k Dielectric A Potential Issue in Wet Etching of Dual Metal Gate Process Technology," IEEE Electron Devices Letters, vol. 26, no. 3, p. 163, March 2005.

100. Rino Choi, Se Jong Rhee, Jack C. Lee, Byoung Hun Lee, Gennadi Bersuker, "Charge trapping and detrapping characteristics in high-k gate dielectric under static and dynamic stress," Electron Dev. Lett. vol 26 (3), p197, 2005.

101. M. S. Akbar, Naim Moumen, Joel Barnett, Johnny Sim and Jack C. Lee, "Effect of NH_3 surface nitridation temperature on mobility of ultrathin atomic layer deposited HfO_2", Appl. Phys. Lett. 86 (2005).

102. C. H. Choi, C.S. Kang, C.Y. Kang, S.J. Rhee, M.S. Akbar, S.A. Krishnan, M. Zhang, and Jack C. Lee, "Positive Bias Temperature Instability Effects of Hf-Based nMOFETs with Various Nitrogen and Silicon Profiles", IEEE Electron Device Letter (EDL), Vol., 26, No.1, p32, 2005.

103. Akbar, M.S.; Choi, C.H.; Rhee, S.J.; Krishnan, S.A.; Kang, C.Y.; Zhang, M.H.; Lee, T.; Ok, I.J.; Zhu, F.; Kim, H.-S.; Lee, J.C., "Electrical Performance and Reliability Improvement by Using Compositionally Varying Bi-Layer Structure of PVD HfSixOy Dielectric," IEEE Electron Devices Letters, vol. 26, no. 3, p. 166, March 2005.

104. Chang Yong Kang, Pat Lysaght, Rino Choi, Byoung Hun Lee, Chang Seok Kang, Se Jong Rhee, Chang Hwan Choi, Shahriar M. Akbar and Jack C.

Lee, “Nickel-Silicide Phase Effects on Flatband Voltage Shift and Equivalent Oxide Thickness Decrease of Hafnium Silicon Oxynitride Metal Silicon Oxide Capacitors,” Applied Physics Letter, vol. 86, article no. 222906, 2005.

105. Chang Yong Kang, Se Jong Rhee, Chang Hwan Choi, Chang Seok Kang, Rino Choi, Mohammad S. Akbar, Manhong Zang, Siddarth A. Krishnan and Jack C. Lee, “Effects of Nitrogen-Incorporated Interface Layer on the Transient Characteristics of Hafnium Oxide n-Metal Oxide Semiconductor Field Effect Transistors,” Applied Physics Letter, vol. 86, article no. 1236506, 2005.

106. Chang Yong Kang, Se Jong Rhee, Chang Hwan Choi, Shariar M. Abkar, Manhong Zhang, Taekhwi Lee, Injo Ok and Jack C. Lee, “Effects of Tantalum Penetration through Hafnium Oxide Layer on Carrier Generation Rate in Silicon Substrate and Carrier Mobility Degradation,” Applied Physics Letter, vol. 86, article no. 012901, 2005.

107. Changhwan Choi, Chang Yong Kang, Se Jong Rhee, Mohammad Shahariar Abkar, Siddarth A. Krishna, Manhong Zhang, Hyungseob Kim, Tackhwi Lee, Feng Zhu, Injo Ok, and Jack C. Lee, "Aggressively Scaled Ultra-Thin Undoped HfO2 Gate Dielectric (EOT < 0.7nm) with TaN Gate Electrode Using Engineered Interface Layer", IEEE Electron Device Letter (EDL), Vol., 26, No.7, p454, 2005.

108. Changhwan Choi, C.S. Kang, C.Y. Kang, S.J.Rhee, M.S. Akbar, S.A. Krishnan, M. Zhang, and Jack C. Lee, "Positive Bias Temperature Instability Effects of Hf-Based nMOFETs with Various Nitrogen and Silicon Profiles", IEEE Electron Device Letter (EDL), Vol., 26, No.1, p32, 2005.

109. Mohammad S. Akbar, Naim Moumen, Joel Barnett, Byoung Hun Lee, and Jack C. Lee, “Improvement in Bias Instabilities of MOCVD Hf-silicate by dilute HCl (500:1) Post-Deposition Rinsing and its effect after High Pressure H_2 Anneal”, in Appl. Phys. Lett. 87, 252903 (2005).

110. Chang Yong Kang, Pat Lysaght, Rino Choi, Byoung Hun Lee, Se Jong Rhee, Chang Hwan Choi, M. S. Akbar, and Jack C. Lee, "Nickel-silicide phase effects on flatband voltage shift and equivalent oxide thickness decrease of hafnium silicon oxynitride metal-silicon-oxide capacitors", Appl. Phys. Lett. 86, 222906 (2005).

111. M. S. Akbar, Naim Moumen, Jeff Peterson, Joel Barnett, Muhammad Hussain and Jack C Lee, “Effect of Precursor Pulse Time on Charge Trapping and Mobility of ALD HfO_2”, Electrochemical Society, 2005.

112. M. H. Zhang, S. J. Rhee, C. Y. Kang, C. H. Choi, M. S. Akbar, S. A. Krishnan, T. Lee, I. J. Ok, F. Zhu, H. S. Kim, and Jack C. Lee, “Improved electrical and material characteristics of HfTaO gate dielectrics with high crystallization temperature,” Applied Physics Letters, 87, 232901 (2005).

113. Se Jong Rhee, Chang Yong Kang, Chang Hwan Choi, Manhong Zhang, and Jack C. Lee, “Material and electrical analysis of hafnium titania bilayer dielectric metal-oxide-semiconductor field-effect transistors,” J. Vac. Sci. Technol. B 23, 2561 (2005).

114. Yanxia Lin, Mehmet C. Öztürk, Bei Chen, Se Jong Rhee, Jack C. Lee, and Veena Misra, ”Impact of Ge on integration of HfO_2 and metal gate electrodes on strained Si channels,” Appl. Phys. Lett. 87, 071903 (2005).

115. (Invited Paper) Se Jong Rhee and Jack C. Lee “Threshold voltage instability characteristics of HfO2 dielectrics n-MOSFETs” IEEE Microelectronic Reliability, 45, p1051-1060, 2005.

116. Feng Zhu, Se Jong Rhee, Chang Yong Kang, Chang Hwan Choi, Akbar, M.S., Krishnan, S.A., Manhong Zhang, Hyoung-Sub Kim, Tackwhi Lee, Ok, I., and J.C. Lee, "Improving channel carrier mobility and immunity to charge trapping of high-k NMOSFET by using stacked Y2O3/HfO2 gate dielectric" Volume 26, Issue 12, Dec. 2005.

117. S. J. Rhee, F. Zhu, H. S. Kim, C. H. Choi, C. Y. Kang, M. Zhang, T. Lee, I. Ok, S. Krishnan, and J. C. Lee, “Hafnium Titanate bilayer structure multimetal dielectric nMOSCAPs”, IEEE Electron Device Letters, vol. 27, issue. 4, p. 225, April 2006.

118. S. J. Rhee, F. Zhu, H. S. Kim, C. Y. Kang, C. H. Choi, M. Zhang, T. Lee, I. Ok, S. Krishnan, and J. C. Lee, “Systematic analysis of silicon oxynitride interfacial layer and its effects on electrical characteristics of high-*k* HfO_2 transistor,” Appl. Physics Letters, 88, 153515, 2006.

119. M. S. Akbar, Naim Moumen, Jeff Peterson, Joel Barnett, Muhammad Hussain and Jack C Lee, “Optimization of Precursor Time in Improving Bulk Trapping Properties of ALD HfO_2 Gate Stacks” Applied Physics Letter, vol. 88, article no. 082901, March 2006.

120. Siddarth A. Krishnan, Manuel Quevedo, Rusty Harris, Paul D. Kirsch, Rino Choi, Byoung Hun Lee, Gennadi Bersuker and Jack C. Lee, “NBTI Dependence on Dielectric Thickness and Nitrogen concentration in Ultra-scaled HfSiON Dielectric/ ALD-TiN Gate Stacks”, JJAP, Vol. 45, No. 4B, 2006.

121. M. S. Akbar, C. H. Choi, S. J. Rhee, S. Krishnan, C. Kang, M. H. Zhang, T. Lee, I. J. Ok, F. Zhu, H. –S. Kim, and Jack C. Lee, “Investigation of Transient Relaxation under Static and Dynamic Stress in Hf-based Gate Oxides”, IEEE Transaction in Electron Device Letters, vol. 53, no. 5, p. 1200-1207, May 2006.

122. C. Y. Kang, R. Choi, S. C. Song, C. D. Young, G. Bersuker, B. H. Lee and J. C. Lee, "Transient Bi-Carrier Response in High-k Dielectrics and its Impact on Transient Charge Effects in High-k Complementary Metal Oxide Semiconductor Devices" Applied Phys. Lett. 88, 162905 (2006).

123. M. H. Zhang, F. Zhu, T. Lee, H. S. Kim, I. J. Ok, G. Thareja, L.Yu, and Jack C. Lee "Fluorine passivation in poly-Si/TaN/HfO_2 through ion implantation", Applied Physics Letters, 89 (142909) 2006.

124. Injo Ok, Hyoung-sub Kim, Manhong Zhang, Chang-Yong Kang, Se Jong Rhee, Changhwan Choi, Siddarth A. Krishnan, Tackhwi Lee, Feng Zhu, Gaurav Thareja, and Jack C. Lee, "Metal Gate – HfO2 MOS Structures on GaAs Substrate with and without Si interlayer", IEEE Electron Device Letters, 27(3), pp. 145-147, March 2006.

125. Hyoung-sub Kim, Injo Ok, Manhong Zhang, Changhwan Choi, Tackhwi Lee, Feng Zhu, Gaurav Thareja, L. Yu and Jack C. Lee, "Ultrathin HfO2 (EOT= 1.1nm) MOS capacitors on n-GaAs substrate with germanium passivation," Applied Physics Letters, 88, p. 252906, 2006.

126. M. H. Zhang, I. J.Ok , H. S. Kim, F. Zhu, T. Lee, G. Thareja, L. Yu, and Jack C. Lee, "Electrical characteristics of sputter deposited Hf $_{1-x}Si_xO$/Si/GaAs gate stacks," Applied Physics Letters 89, p. 042902, 2006.

127. Feng Zhu, Chang Yong Kang, Se Jong Rhee, Chang Hwan Choi, Siddarth A. Krishnan, Manhong Zhang, Hyoung-Sub Kim, Taekhwi Lee, Injo Ok, Gaurav Thareja, and Jack C. Lee, "Mechanism of improved channel carrier mobility for stacked Y2O3 /HfO2 gate dielectric", Applied Physics Letters, 89, 257642, 2006.

128. Tackhwi Lee, Se Jong Rhee, Chang Yong Kang, Feng Zhu, Hyoung-sub Kim, Changhwan Choi, Injo Ok, Manhong Zhang, Siddarth Krishnan, Gaurav Thareja, and Jack C. Lee "Structural Advantage for the EOT Scaling and Improved Electron Channel Mobility by Incorporating Dysprosium Oxide (Dy2O3) Into HfO2 n-MOSFETs" IEEE Electron Device Letters, Vol. 27, No. 8, P.640-643, August 2006.

129. Hyoung-Sub Kim, Injo Ok, Manhong Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tasi, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, "Depletion-mode GaAs metal-oxide-semiconductor field-effect transistor with HfO_2 dielectric and germanium interfacial passivation layer," *Appl. Phys. Lett.*, Vol. 89, pp. 222904, 2006.

130. Hyoung-Sub Kim, Injo Ok, Manhong Zhang, Tackhwi Lee, Feng Zhu, Lu Yu and Jack C. Lee, "Metal gate-HfO_2 metal-oxide-semiconductor capacitors on n-GaAs substrate with silicon/germanium interfacial passivation layers," *Appl. Phys. Lett*., Vol. 89, pp. 222903, 2006.

131. G. Thareja, H. Wen, R. Harris, P. Majhi, B. Lee, and Jack Lee, "NMOS Compatible Workfunction of TaN Metal Gate with Gadolinium Oxide Buffer Layer on Hf-Based Dielectrics," IEEE Electron Devices Letters, vol. 27, no. 10, p. 802, October 2006.

132. M. S. Akbar and J. Lee, “A Novel Approach in Separating the Roles of Electrons and Holes in Degradation of Hf-based MOSFET Devices by Using Stress-Anneal Technique,” IEEE Electron Devices Letters, vol. 28, no. 2, February 2007.

133. J. Lee (Invited Paper) "MOSCAP's and MOSFET's on III-V Channel Materials with Si, Ge and SiGe Interface Passivation Layer", Electrochemical Society Transactions, Volume 6, "Silicon Nitride, Silicon Dioxide, and Emerging Dielectrics 9", April 2007.

134. M. S. Akbar, C. H. Choi, S. J. Rhee, S. Krishnan, C. Kang, M. H. Zhang, T. Lee, I. J. Ok, F. Zhu, H. –S. Kim, and Jack C. Lee, “A Novel Approach in Separating the roles of Electrons and Holes in causing Degradation in Hf-based MOSFET Devices by using Stress-Anneal Technique”, in IEEE Electron Device Letter, vol. 28 (2), pp.132-134, 2007.

135. Feng Zhu, S. Koveshnikov, I. Ok, H.S. Kim, V. Tokranov, M. Yakimov, S. Oktyabrsky, M. Zhang, T. Lee, G. Thareja, L. Yu, W. Tsai and J. C. Lee, “Depletion-mode GaAs metal-oxide-semiconductor field-effect transistor with amorphous silicon interface passivation layer and thin HfO2 gate oxide,” Applied Physics Letters, 91, 043507 (2007).

136. Hyoung-Sub Kim, Injo Ok, Manhong Zhang, F. Zhu, S. Park, J. Yum, Han Zhao, and Jack C. Lee, “Gate oxide scaling down in HfO_2-GaAs metal-oxide-semiconductor capacitor using germanium interfacial passivation layer,” *Appl. Phys. Lett*., Vol. 91, pp. 042904, 2007.

137. M. H. Zhang, M. Oye, B. Cobb, F. Zhu, H. S. Kim, I. J. Ok, J. Hurst, S. Lewis, A. Holmes, J. C. Lee, S. Koveshnikov, W. Tsai, M. Yakimov, V. Torkanov, S. Oktyabrsky, “Importance of controlling oxygen incorporation into HfO_2/Si/n-GaAs gate stacks” *J. Appl. Phys*. . 101, 034103 (2007).

138. Sachin Joshi, Cristiano Krug, Dawei Heh, Hoon Joo Na, Harlan R Harris, Jung Woo Oh, Paul D. Kirsch, Prashant Majhi, Byoung Hun Lee, Hsing-Huang Tseng, Raj Jammy, Jack C. Lee and Sanjay K. Banerjee, “Improved Ge Surface Passivation with Ultrathin SiO_X Enabling High Mobility Surface Channel PMOSFETs Featuring a HfSiO/WN gate stack,” Electron Devices Letters, vol. 28, p. 308, April 2007.

139. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao and Jack C. Lee, “Temperature Effects of Si Interface Passivation Layer Deposition on High-k III-V Metal–Oxide–Semiconductor Characteristics.” Applied physics letters, 91, 2007.

140. Han Zhao, Hyoung-Sub Kim, Feng Zhu, Manhong Zhang, Injo OK, Sung Il Park, Jung Hwan Yum and Jack C Lee, “Metal-oxide-semiconductor capacitors on GaAs with germanium nitride passivation layer”, Applied Physics Letters, 91, 172101, (2007)

141. Sung Il Park, InJo Ok, Hyoung-sub Kim, Feng Zhu, Manhong Zhang, Jung Hwan Yum, Zhao Han, and Jack C. Lee, “Optimization of electrical characteristics of TiO2-

incorporated HfO2 n-type doped gallium arsenide metal oxide semiconductor capacitor with silicon interface passivation layer", in Applied Physics Letters 91, 081908(2007).

142. Feng Zhu, S. Koveshnikov, I. Ok, H.S. Kim, M. Zhang, T. Lee, G. Thareja, L. Yu, V. Tokranov, M. Yakimov, and S. Oktyabrsky, W. Tsai and J. C. Lee, "Depletion-mode GaAs N-MOSFETs with amorphous silicon interface passivation layer and thin HfO_2 gate oxide," Applied Physics Letters, 91, 043507 (2007)

143. M. H. Zhang, F. Zhu, H. S. Kim, I. J. Ok and Jack C. Lee, "Fluorine passivation in gate stacks of poly-Si/TaN/HfO_2 (and HfSiON/HfO_2)/Si through gate ion implantation", IEEE Electron Device Letters, 28, 195 (2007).

144. Hyoung-Sub Kim, Injo Ok, Manhong Zhang, F. Zhu, S. Park, J. Yum, Han Zhao, and Jack C. Lee, "Gate oxide scaling down in HfO_2-GaAs metal-oxide-semiconductor capacitor using germanium interfacial passivation layer," Appl. Phys. Lett., Vol. 91, pp. 042904, (2007).

145. Han Zhao, Hyoung-Sub Kim, Feng Zhu, Manhong Zhang, Injo OK, Sung Il Park, Jung Hwan Yum, and Jack C. Lee, "Metal-oxide-semiconductor capacitors on GaAs with germanium nitride passivation layer", Applied Physics Letters, 91, 172101 (2007)
146. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J. Oh, P. Majhi, and Jack C. Lee, "Flatband voltage instability characteristics of HfO_2-based GaAs metal-oxide-semiconductor capacitors with a thin Ge layer," Appl. Phys. Lett., Vol. 92, pp. 102904, (2008).

147. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J. Oh, P. Majhi, and Jack C. Lee, "Inversion-type enhancement-mode HfO_2-based GaAs metal-oxide-semiconductor field effect transistors with a thin Ge layer," Appl. Phys. Lett., Vol. 92, pp. 032907, (2008).

148. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, N. Goel and W. Tsai, C. K. Gaspe, M.B. Santos, and Jack C. Lee, "Metal gate: HfO_2 metal-oxide-semiconductor structures on high-indium-content InGaAs substrate using physical vapor deposition." Appl. Phys. Lett. 92, 112904 (2008).

149. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, and Jack C. Lee, "Influence of the substrate orientation on the electrical and material properties of GaAs metal-oxide-semiconductor (MOS) Capacitors and self-aligned transistors using HfO_2 and silicon interface passivation layer (IPL)" Appl. Phys. Lett. 92, 1 (2008)

150. InJo Ok , H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, N. Goel and W. Tsai, C.K. Gaspe, M.B. Santos, and Jack C. Lee, "Self-aligned n-channel metal-oxide-semiconductor field effect transistor on high-indium-

content $In_{0.53}Ga_{0.47}As$ and InP using physical vapor deposition HfO_2 and silicon interface passivation Layer." Appl. Phys. Lett. 92, 202903 (2008)

151. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao and Jack C. Lee, "Self-aligned n- channel GaAs metal–oxide–semiconductor field-effect transistors (MOSFETs) Using HfO_2 and silicon interface passivation layer: post metal annealing optimization." Microelectronics Engineering (2008).

152. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, P. Majhi, N. Goel, W. Tsai, C. K. Gaspe, M. B. Santos, and Jack C. Lee, "A study of Metal-Oxide-Semiconductor Capacitors on GaAs, In0.53Ga0.47As, InAs, and InSb Substrates using a Germanium Interfacial Passivation Layer," Appl. Phys. Lett., (2008).

153. K. T. Lee, C. Y. Kang, B. S. Ju, R. Choi, K. S. Min, O. S. Yoo, B. H. Lee, R. Jammy, J.C. Lee, H. D. Lee, Y.H. Jeong, "Effects of In Situ O2 Plasma Treatment on off-State Leakage and Reliability in Metal-Gate/High- k Dielectric MOSFETs", IEEE Electron Device Letters, vol. 29, pp. 565, Jun. 2008.

154. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, P. Majhi, and Jack C. Lee, "HfO_2-based InP n-channel metal-oxide-semiconductor field-effect transistors and metal-oxide-semiconductor capacitors using a germanium interfacial passivation layer," Appl. Phys. Lett., 93, 102906 (2008)

155. Han Zhao, Davood Shahrjerdi, Feng Zhu, Manhong Zhang, Hyoung-Sub Kim, Injo OK, Jung Hwan Yum, Sung Il Park, Sanjay K. Banerjee, and Jack C. Lee, "Gate-first inversion-type InP metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al_2O_3 gate dielectric", Applied Physics Letters, 92, 233508 (2008)

156. Han Zhao, Davood Shahrjerdi, Feng Zhu, Hyoung-Sub Kim, Injo OK, Manghong Zhang, Jung Hwan Yum, Sanjay K. Banerjee, and Jack C. Lee, "Inversion-type indium phosphide metal-oxide-semiconductor field-effect transistors with equivalent oxide thickness of 12 Å using stacked $HfAlO_x/HfO_2$ gate dielectric", Applied Physics Letters, 92, 253506 (2008)

157. Han Zhao, Davood Shahrjerdi, Feng Zhu, Hyoung-Sub Kim, Injo OK, Manhong Zhang, Jung Hwan Yum, Sanjay K. Banerjee and Jack C Lee, "Inversion-type InP MOSFETs with EOT of 21 Å using atomic layer deposited Al_2O_3 gate dielectric", Electrochemical and solid-state letters, 11, H233, (2008)

158. Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Niti Goel, Jack C Lee, "Effect of channel doping concentration and thickness on device performance for $In_{0.53}Ga_{0.47}As$ MOS transistors with atomic-layer-deposited Al_2O_3 dielectrics", Applied Physics Letters, 94, 093505 (2009)

159. Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Yanzhen Wang, Niti Goel, Jack C Lee, "High performance $In_{0.7}Ga_{0.3}As$ metal-oxide-semiconductor transistors with mobility > 4400 cm^2/Vs using InP barrier layer", Applied Physics Letters, 94, 193502 (2009)

160. Han Zhao, Jung Hwan Yum, Yen-Ting Chen, and Jack C Lee, "$In_{0.53}Ga_{0.47}As$ n-MOSFETs with ALD Al_2O_3, HfO_2 and $LaAlO_3$ gate dielectrics", Journal of Vacuum Science and Technology B, 27, 2024, (2009)

161. Feng Zhu, Han Zhao, I. Ok, H.S. Kim, M. Zhang, S. Park, J. Yum, Niti Goel, C.K. Gaspe, M.B. Santos, W. Tsai and Jack C. Lee, "Effects of anneal and silicon interface passivation layer thickness on device characteristics of $In_{0.53}Ga_{0.47}As$ n-MOSFETs with HfO_2 gate oxide", Electrochemical and Solid-State Letters, 12, H131 (2009)

162. Feng Zhu, Han Zhao, I. Ok, H.S. Kim, J. Yum, Niti Goel, C.K. Gaspe, M.B. Santos, W. Tsai, and Jack C. Lee, "A high performance $In_{0.53}Ga_{0.47}As$ Metal-Oxide-Semiconductor Field Effect Transistor with silicon interface passivation layer", Applied Physics Letters, 94, 013511 (2009)

163. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, and Jack C. Lee, "Metal-oxide-semiconductor field-effect-transistors on indium phosphide using HfO_2 and silicon passivation layer with equivalent oxide thickness of 18Å", APPLIED PHYSICS LETTERS 94, 213505, May 2009

164. Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, Jack Lee, "High Performance InGaAs MOSFETs with High Mobility using InP Barrier Layer", Electrochemical Society Transactions, Vol. 25, Issue #7, p. 397-404 (2009)

165. H Zhao, J. Lee, et al, "Effects of gate-first and gate-last process on interface quality of $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors using atomic-layer-deposited Al_2O_3 and HfO_2 oxides", Applied Physics Letters, 95, 253501 (2009)

166. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee "Improved electrical characteristics of TaN/Al2O3 / In0.53Ga0.47As metal-oxide-semiconductor field-effect transistors by fluorine incorporation", APPLIED PHYSICS LETTERS 95, 013501 (2009)

167. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Effects of fluorine incorporation on the electrical properties of atomic-layer-deposited Al2O3 gate dielectric on InP substrate", Journal of The Electrochemical Society, 157 (3) G71-G75 January (2010)

168. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Fluorinated HfO2 gate dielectric engineering on In0.53Ga0.47As metal-oxide-semiconductor field-effect-transistors, APPLIED PHYSICS LETTERS 96, 103506, March (2010)

169. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Effects of fluorine incorporation into HfO2 gate dielectrics on InP and In0.53Ga0.47As metal-oxide-semiconductor field-effect-transistors," APPLIED PHYSICS LETTERS 96, 253502 (2010).

170. H Zhao, J. Lee, et al, "Effects of barrier layers on device performance of high mobility $In_{0.7}Ga_{0.3}As$ quantum-well metal-oxide-semiconductor field-effect-transistors", Applied Physics Letters, 96, 102101 (2010).

171. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, "Scaling Properties of $In_{0.7}Ga_{0.3}As$ buried-channel MOSFETs with atomic layer deposited gate dielectric", Electronics Letters, vol. 46, no. 25 (2010).

172. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, "Investigation of surface channel InGaAs MOSFETs with Al2O3 and ZrO2 ALD Gate Dielectric", Electrochemical Society Transactions 33 (3), 479 (2010).

173. C. Choi, J. Lee, "Scaling equivalent oxide thickness with flat band voltage (V_{FB}) modulation using *in situ* Ti and Hf interposed in a metal/high-*k* gate stack," Journal of Applied Physics, vol. 108, no. 1, 2010.

174. M.S. Park, K. T. Lee, C. Y. Kang, G. B. Choi, H.C. Sagong, C. W. Sohn, B. G. Min, J. Oh, P. Majhi, H. Tseng, J. Lee, J. S. Lee, R. Jammy, Y. H. Jeong, "The Effect of a Si Capping Layer on RF Characteristics of High-k/Metal Gate SiGe Channel pMOSFETs," IEEE Electron Device Letters, vol. 31, no. 10, p. 1104-1106, Oct. 2010.

175. Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Fei Xue, and Jack C Lee, "$In_{0.7}Ga_{0.3}As$ tunneling field-effect-transistors with a I_{on} of 50 mA/mm and a subthreshold swing of 86 mV/dec using HfO_2 gate oxide", Electron Device Letters, 31, 1392, (2010).

176. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee ,"InAs inserted InGaAs buried channel metal-oxide-semiconductor field-effect-transistors with atomic-layer-deposited gate dielectric ", Appl. Phys. Lett. 98, 082106 (2011).

177. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack C. Lee, "Effect of indium concentration on InGaAs channel metal-oxide-semiconductor field-effect transistors with atomic layer deposited gate dielectric", J. Vac. Sci. Technol. B 29, 040601 (2011).

178. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "ZrO2-based InP MOSFETs (EOT=1.2nm) Using Various Interfacial Dielectric Layers" Electrochemical Society Transactions 35(3), 375, May (2011).

179. Y. Wang, Y. Chen, H. Zhao, F. Xue, F. Zhou, and J. Lee, "Impact of SF_6 plasma treatment on performance of TaN-HfO_2-InP metal-oxide-semiconductor field-effect transistor ", Applied Physics Letters, 98, 043506, (2011).

180. Y. Wang, Y. Chen, H. Zhao, F. Xue, F. Zhou, and J. Lee, "Improved electrical properties of HfO_2-based gate dielectrics on InP substrate using Al_2O_3/HfO_2 and SF_6 plasma treatment", Electrochemical Solid-state Letters, 14, H291 (2011).

181. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack C. Lee, "High-k InGaAs metal-oxide-semiconductor field-effect-transistors with various barrier layer materials" Appl. Phys. Lett. Vol. 99, issue 3, p. 033507 - 033507-3, July 2011.

182. Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Fei Xue, and Jack C. Lee, "Improving the on-current of $In_{0.7}Ga_{0.3}As$ tunneling field-effect-transistors by p^{++}/n^{+} tunneling junction", Applied physics letters, 98, 093501, (2011).

183. Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Fei Xue, and Jack C. Lee, "InGaAs tunneling field-effect-transistors with atomic-layer-deposited gate oxides", IEEE Transactions on Electron Devices, vol. 58, no. 9, p. 2990-2995, Sept. 2011.

184. H. C. Sagong, C. Y. Kang, C. W. Sohn, K. Jeon, D. Choi, C-K Baek, J-S Lee, J. Lee and Y. Jeong, "Comprehensive Study of Quasi-Ballistic Transport in High-K/Metal Gate nMOSFETs," IEEE Electron Device Letters, vol. 31, no. 11, p. 1424, Nov. 2011.

185. Y. Chen, Y. Wang, F. Xue, F. Zhou, J. Lee, "Application of Post-HfO_2 Fluorine Plasma Treatment for Improvement of $In_{0.53}Ga_{0.47}As$ MOSFET Performance," IEEE Electron Device Letters, vol. 31, no. 11, p. 1531, Nov. 2011.

186. J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, G. Bersuker, M. Downer, C. W. Bielawski, J. C. Lee and S. K. Banerjee, "Atomic layer deposited beryllium oxide: Effective passivation layer for III-V metal/oxide/semiconductor devices," Journal of Applied Physics, vol. 109, 064101 (2011).

187. J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, J. C. Lee and S. K. Banerjee, "Inversion Type InP Metal Oxide Semiconductor Field Effect Transistor Using Novel Atomic Layer Deposited BeO Gate Dielectric," Applied Physics Letters, 99, 033502 (2011).

188. J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, J. C. Lee and S. K. Banerjee, "Comparison of Self Cleaning Effect and Electrical Characteristics between Atomic Layer Deposited BeO and Al_2O_3 as an Interface Passivation Layer on GaAs MOS Devices," Journal of Vacuum Science and Technology, vol. 29, issue 6, p. 061501-6, Nov. 2011.

189. Yum J. H.; Akyol T.; Lei M.; Ferrer, D. A. Hudnall, Todd. W., Downer, M, Bielawski, C. W. Bersuker, G. Lee, J. C.; Banerjee, S. K., "A study of highly crystalline novel beryllium oxide film using atomic layer deposition ," Journal of Crystal Growth, vol. 334, issue 1, p. 126-133, Nov. 2011.

190. Jung Hwan Yum, Gennadi Bersuker, Tarik Akyol, D. A. Ferrer, Ming Lei, Keun Woo Park, Todd W. Hudnall, Mike C. Downer, Christopher W. Bielawski, Edward T. Yu, Jimmy Price, Jack C. Lee and Sanjay K. Banerjee*, "Epitaxial ALD BeO: Efficient Oxygen Diffusion Barrier for EOT Scaling and Reliability Improvement*," IEEE Transaction on Electron Devices, vol. 58, issue 12, p. 4384-4392, Dec. 2011.

191. Yanzhen Wang, Yen-Ting Chen, Fei Xue, Fei Zhou, and Jack C. Lee, "HfO_2 dielectrics engineering using low power SF_6 plasma on InP and $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors", Applied Physics Letters, 100, 243508 (2012).

192. Yanzhen Wang, Yen-Ting Chen, Fei Xue, Fei Zhou, and Jack C. Lee, "Effects of SF_6 plasma treatment on electrical characteristics of TaN-Al_2O_3-InP metal-oxide-semiconductor field-effect transistor", Applied Physics Letters, 101, 063505 (2012).

193. Yanzhen Wang, Yen-Ting Chen, Fei Xue, Fei Zhou, Yao-Feng Chang, and Jack C. Lee, "MOSFETs on InP substrate with $LaAlO_3/HfO_2$ bilayer of different $LaAlO_3$ thickness and single $La_XAl_{1-X}O$ layer with different La doping level", Electrochemical Society Transactions, 50 (2012).

194. Yanzhen Wang, Burt Fowler, Yen-Ting Chen, Fei Xue, Fei Zhou, Yao-Feng Chang, and Jack C. Lee, "Effect of hydrogen/deuterium incorporation on electroforming voltage of SiO_x resistive random access memory", Applied Physics Letters, 101, 183505 (2012).

195. Yanzhen Wang, Yen-Ting Chen, Fei Xue, Fei Zhou, Yao-Feng Chang, Burt Fowler, and Jack C. Lee, "Memory switching properties of e-beam evaporated SiO_x on N++ Si substrate" Applied Physics Letters, 100, 083502 (2012).

196. Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Physical and Electrical Analysis of Post-HfO2 Fluorine Plasma Treatment for Improvement of In0.53Ga0.47As MOSFETs Performance", IEEE Trans. Electron Devices Vol. 59, No., 139, 2012.

197. Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Optimization of Fluorine Plasma Treatment for Interface Improvement on HfO2/In0.53Ga0.47As MOSFETs", Special Issue (Organo-Fluorine Chemical Science) of Appl. Sci. Vol. 2(1), 233, 2012 (Invited).

198. L. Morassi, G. Verzellesi, H. Zhao, J.C. Lee, D. Veksler, G. Bersuker, "Errors Limiting Split-CV Mobility Extraction Accuracy in Buried-Channel InGaAs MOSFETs", IEEE Transactions on Electron Devices, vol. 59(4), pp. 1068-1075, Apr. 2012.

199. M. Hanna, H. Zhao and J. Lee, “Poole Frenkel current and Schottky emission in SiN gate dielectric in AlGaN/GaN metal insulator semiconductor heterostructure field effect transistors,” Appl. Phys. Lett. 101, 153504 (2012).

200. L. Morassi, G. Verzellesi, H. Zhao, J.C. Lee, D. Veksler, G. Bersuker, “Engineering barrier and buffer layers in InGaAs quantum-well MOSFETs”, IEEE Transactions on Electron Devices, vol. 59, no. 12, p. 3651-3654, 2012.

201. Yao-Feng Chang, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, Burt Fowler, and Jack C. Lee, “Study of polarity effect in SiOx-based resistive switching memory”, Appl. Phys. Lett., 101, 052111 (2012).

202. Yao-Feng Chang, Pai-Yu Chen, Burt Fowler, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, and Jack C. Lee, “Understanding the resistive switching characteristics and mechanism in active SiOx-based resistive switching memory”, J. Appl. Phys., 112, 123702 (2012).

203. Fei Xue, Aiting Jiang, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, “Channel Thickness Dependence of InGaAs Quantum-Well Field-Effect Transistors with High-κ Gate Dielectrics,” *IEEE Electron Device Lett*., Vol. 33, No. 9, 1255 (2012).

204. Fei Xue, Aiting Jiang, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, “Sub-50nm In0.7Ga0.3As MOSFETs with various barrier layer materials”, *IEEE Electron Device Lett*. Vol. 33, No. 1, 32 (2012).

205. Fei Xue, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Yao-Feng Chang, Burt Fowler and Jack Lee, “ The Effect of Plasma Treatment on Reducing Electroforming Voltage of Silicon Oxide RRAM”, Electrochemical Society Transactions, vol. 45, No. 6,245 (2012).

206. Yen-Ting Chen, Burt Fowler, Yanzhen Wang, Fei Xue, Fei Zhou, Yao-Feng Chang, Pai-Yu Chen, and Jack C. Lee, “Tristate Operation in Resistive Switching of SiO2 Thin Films,” IEEE Electron Devices Letters, VOL. 33, NO. 12, p. 1702, December 2012.

207. Yen-Ting Chen, Burt Fowler, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Random process of filamentary growth and localized switching mechanism in resistive switching of SiOx thin films", ECS Journal of Solid State Science and Technology 1 (3) P1-P4 (2012).

208. Chang-Woo Sohn, Chang Yong Kang, Myung-Dong Ko, , Do-Young Choi, Hyun Chul Sagong, Eui-Young Jeong, Chan-Hoon Park, Sang-Hyun Lee, Ye-Ram Kim, Chang-Ki Baek, Jeong-Soo Lee, Jack C. Lee, and Yoon-Ha Jeong, “Analytical Model of S/D Series Resistance in Trigate FinFETs with Polygonal Epitaxy”, IEEE Transactions on Electron Devices, vol. 60, issue 4, p.1302-1309, April 2013.

209. Yen-Ting Chen, Burt Fowler, Yao-Feng Chang, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Reduced electroforming voltage and enhanced programming stability in resistive switching of SiO_2 thin film", ECS Solid State Letters, 2(5) N18, 2013.

210. Yao-Feng Chang, P. Y. Chen, Fei Zhou, Fei Xue, Burt Fowler, Edward T. Yu, and Jack C. Lee, "Investigation of edge- and bulk-related resistive switching behaviors and backward-scan effects in SiO_x-based resistive switching memory", Appl. Phys. Lett., 103, 193508 (2013).

211. Yao-Feng Chang, Li Ji, Zhuo-Jie Wu, Fei Zhou, Yanzhen Wang, Fei Xue, Burt Fowler, Edward T. Yu, Paul S. Ho, and Jack C. Lee, "Oxygen-induced bi-modal failure phenomenon in SiOx-based resistive switching memory", Appl. Phys. Lett., 103, 033521 (2013).

212. Li Ji, Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Tsung-Ming Tsai, Kuan-Chang Chang, Min-Chen Chen, Ting-Chang Chang, Simon M. Sze, Edward T. Yu and Jack C. Lee, "Integrated One Diode–One Resistor Architecture in Nanopillar SiOx Resistive Switching Memory by Nanosphere Lithography", Nano Lett., 14 p. 813, (2014).

213. Fei Xue*,* Aiting Jiang, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Yao-Feng Chang and Jack Lee, "Non-planar InGaAs Gate-Wrapped-Around Field-Effective-Transistors," IEEE Transactions on Electron Devices, vol. 61, issue 7, p. 2332, July 2014.

214. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Intrinsic SiOx-based unipolar resistive switching memory Part I: Oxide stoichiometry effects on reversible switching and program window optimization" J. Appl. Phys. 116, 043708 (2014).

215. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Intrinsic SiOx-based unipolar resistive switching memory Part II: Thermal effects on charge transport and characterization of multilevel programing" J. Appl. Phys. 116, 043709 (2014).

216. (Highlighted as News & Views in the same issue) Li Ji, Martin D. McDaniel, Shijun Wang, Agham B. Posadas, Xiaohan Li, Haiyu Huang, Jack C. Lee, Alexander A. Demkov, John G. Ekerdt, Allen J. Bard and Edward T. Yu, "A Silicon-based photocathode for water reduction with an expitaxial SrTiO3 protection layer and a nanostructured catalyst", Nature Nanotechnology, Vol 10, (2015), p 84-90.

217. Fei Zhou, Yao-Feng Chang, Yanzhen Wang, Ying-Chen Chen, Fei Xue, Burt Fowler, and Jack C. Lee, "Discussion on device structures and SU-8 encapsulation for SiO_x random access memory operation in air", *Appl. Phys. Lett.*, 105, 163506 (2014).

218. Fei Zhou, Yao-Feng Chang, Kwangsub Byun, Burt Fowler, and Jack C. Lee, "Characterization of external resistance effect and performance optimization in unipolar-type SiO_x-based resistive switching memory", *Appl. Phys. Lett.*, 105, 133501 (2014).

219. Burt W. Fowler, Yao-Feng Chang, Fei Zhou, Yanzhen Wang, Pai-Yu Chen, Fei Xue, Yen-Ting Chen, Brad Bringhurst, Scott Pozder, and Jack C. Lee, "Recent Progress on Understanding Electroforming and Resistive Switching in Silicon Dioxide Resistive Memory Devices" RSC advances 5, 21215 (2015).

220. Fei Zhou, Yao-Feng Chang, Kwangsub Byun, Burt Fowler, Jack C. Lee, "Stabilization of Multiple Resistance Levels by Current-Sweep in SiO_x-based Resistive Switching Memory" *Appl. Phys. Lett.*, 106, 063508 (2015).

221. Yao-Feng Chang, Burt Fowler, Fei Zhou, and Jack C. Lee, "The Intrinsic Unipolar SiOx-based Resistive Switching Memory: Characterization, Mechanism and Applications" ECS Transactions 69 (5), 149-164 (2015).

222. Fei Zhou, Lauren Guckert, Yao-Feng Chang, Earl Swartzlander, and Jack C. Lee, "Bidirectional Voltage Biased Implication Operations Using SiOx Based Unipolar Memristors" Applied Physics Letters, 107 (18), 183501 (2015).

223. Fei Zhou, Yao-Feng Chang, Ying-Chen Chen, Xiaohan Wu, Ye Zhang, Burt Fowler and Jack C. Lee, "A Study of Interfacial Resistive Switching Mechanism by Proton Exchange Reactions on SiOx layer" Physical Chemistry Chemical Physics, 18, 700 - 703 (2016).

224. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou and Jack C. Lee, "Study of self-compliance behaviors and internal filament characteristics in intrinsic SiOx-based resistive switching memory," Applied Physics Letters, 2016.

225. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Simon M. Sze, and Jack C. Lee, "A Synaptic Device Built in One Diode-One Resistor (1D-1R) Architecture with Intrinsic SiOx-based Resistive Switching Memory", Nano Devices and Sensors, ISBN: 978-1-5015-0153-1, (2016).

226. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Xiaohan Wu, Yen-Ting Chen, Yanzhen Wang, Fei Xue, and Jack C. Lee, "Resistive Switching Characteristics and Mechanisms in Silicon Oxide Memory Devices", Nano Devices and Sensors, ISBN: 978-1-5015-0153-1, (2016).

227. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Chih-Hung Pan, Ting-Chang Chang and Jack C. Lee, "Demonstration of Synaptic Behaviors and Resistive Switching Characterizations by Proton Exchange Reactions in Silicon Oxide" Scientific Reports, 6, 21268 (2016). (doi: 10.1038/srep21268)

228. Yao-Feng Chang,Burt Fowler, Ying-Chen Chen and Jack C. Lee, “Proton exchange reactions in SiO x-based resistive switching memory: Review and insights from impedance spectroscopy” Progress in Solid State Chemistry, 1-11 (2016).

229. Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, Meiqi Guo, Fei Zhou, Burt Fowler, and Jack C. Lee, "Characterization of SiOx/HfOx bilayer Resistive-Switching Memory Devices" ECS Transaction *72(2): 25-33; doi:10.1149/07202.0025ecst* (2016).

230. Y.F. Chang, B. Fowler, F. Zhou, Y.C. Chen, J.C. Lee, “Study of self-compliance behaviors and internal filament characteristics in intrinsic SiOx-based resistive switching memory,” *Applied Physics Letters*, 108, 033504 (2016).

231. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Simon M. Sze, and Jack C. Lee, "A Synaptic Device Built in One Diode-One Resistor (1D-1R) Architecture with Intrinsic SiO_x-based Resistive Switching Memory", Physical Sciences Reviews (2016).

232. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Xiaohan Wu, Yen-Ting Chen, Yanzhen Wang, Fei Xue, and Jack C. Lee, "Resistive Switching Characteristics and Mechanisms in Silicon Oxide Memory Devices", Physical Sciences Reviews, DOI: 10.1515/psr-2016-0011, 2016.

233. Li Ji, Hsien-Yi Hsu, Xiaohan Li, Kai Huang, Ye Zhang, Jack C. Lee, Allen J. Bard and Edward T. Yu, “Localized dielectric breakdown and antireflection coating in metal–oxide–semiconductor photoelectrodes,” Nature Materials, 07 November 2016/ DOI 10.1038/nmat4801.

234. Y.-C. Chen, Y. F. Chang, CY Lin, X Wu, G Xu, B Fowler, TC Chang, JC Lee, “Built-in Nonlinear Characteristics of Low Power Operating One-Resistor Selector-Less RRAM By Stacking Engineering”, ECS Transactions 80 (10), 923-931 (2017).

235. Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, Fei Zhou, Meiqi Guo, Chih-Yang Lin, Cheng-Chih Hsieh, Burt Fowler, Ting-Chang Chang, and Jack C. Lee, “Dynamic Conductance Characteristics in HfOx-based Resistive Random-Access Memory,” Royal Society of Chemistry Advances, vol. 7, issue 21 (2017).

236. Yao-Feng Chang, Fei Zhou, Burt W. Fowler, Ying-Chen Chen, Cheng-Chih Hsieh, Lauren Guckert, Earl E. Swartzlander, Jack C. Lee, "Memcomputing (Memristor + Computing) in Intrinsic SiOx-Based Resistive Switching Memory: Arithmetic Operations for Logic Applications," IEEE Transactions on Electron Devices, 64 (7), 2977-2983 (2017).

237. Meiqi Guo, Ying-Chen Chen, Chih-Yang Lin, Yao-Feng Chang, Burt Fowler, Q. Q. Li, Jack C. Lee, Y. G. Zhao, “Unidirectional Threshold Resistive Switching in Au/NiO/Nb: $SrTiO_3$ Devices,” Applied Physics Letters, vol. 110, issue 23, no. 233504, June 2017.

238. (Front Cover) Li Ji, Hsien-Yi Hsu, Xiaohan Li, Kai Huang, Ye Zhang, Jack C. Lee, Allen J. Bard and Edward T. Yu, "Localized dielectric breakdown and antireflection coating in metal-oxide-semiconductor photoelectrodes," Nature Materials, 1 (2017) p127.

239. Ruijing Ge, Xiaohan Wu, Myungsoo Kim, Jianping Shi, Sushant Sonde, Li Tao, Yanfeng Zhang, Jack C. Lee, and Deji Akinwande, "Atomristor: Nonvolatile Resistance Switching in Atomic Sheets of Transition Metal Dichalcogenides," Nano Letters, 18 (1) p. 434-441, 2018.

240. Li Ji, Hsien-Yi Hsu, Jack C. Lee, Allen J. Bard, Edward T. Yu, "High performance photodetectors based on solution-processed epitaxial grown hybrid halide perovskites," Nano Letters, 18(2) p. 994-1000, 2018.

241. Y.-C. Chen, Y.-F. Chang, J. Lee, "Selector-Less Graphite Memristor: Intrinsic Nonlinear Behavior with Gap Design Method for Array Applications", Electrochemical Society Transactions, 85 (1), 11-19 (2018).

242. Ying-Chen Chen, Chih-Yang Lin, Hui-Chun Huang, Sungjun Kim, Burt Fowler, Yao-Feng Chang, Xiaohan Wu, Gaobo Xu, Ting-Chang Chang, and Jack C. Lee. "Internal Filament Modulation in Low-dielectric Gap Design for Built-in Selector-less Resistive Switching Memory Application." *Journal of Physics D: Applied Physics*, vol. 51, Issue 5, Feb. 2018.

243. Myungsoo Kim, Ruijing Ge, Xiaohan Wu, Xing Lan, Jesse Tice, Jack C. Lee and Deji Akinwande, "Zero-static power RF Switches Based on MoS2 Atomristors," Nature Communications, June 2018.

244. Ying-Chen Chen, Yao-Feng Chang, Hui-Chun Huang and Jack Lee, "Effects of ambient sensing on SiOx-based resistive switching and resilience modulation by stacking engineering," Electronic Materials and Processing of Electrochemical Society Journal of Solid-State Science and Technology, July 2018.

245. Ying-Chen Chen, Szu-Tung Hu, Chih-Yang Lin, Burt Fowler, Hui-Chun Huang, Chao-Cheng Lin, Sungjun Kim,Yao-Feng Chang, and Jack C. Lee, "Graphite-based Selectorless RRAM: Improvable Intrinsic Nonlinearity for Array Applications", *Nanoscale* 2018.

246. Yao-Feng Chang, Burt W Fowler, Ying-Chen Chen, Zhi-Yang Lin, Gaobo Xu, Huichun Huang, Jia Chen, Sungjun Kim, Yi Li and Jack C. Lee "Beyond SiOx: An Active Electronics Resurgence and Biomimetic Reactive Oxygen Species Production and Regulation from Mitochondrion," Journal of Materials Chemistry C (2018).

247. Ruijing Ge, Xiaohan Wu, Myungsoo Kim, Jianping Shi, Sushant Sonde, Li Tao, Yanfeng Zhang, Jack C Lee, Deji Akinwande "Atomristor: nonvolatile resistance

switching in atomic sheets of transition metal dichalcogenides", Nano letters 18 (1), 434-441. 2018.

248. Ying-Chen Chen, Chao-Cheng Lin, Sungjun Kim, and Jack C. Lee, "Selectorless Oxide-based Resistive Switching Memory with Nonuniform Dielectric for Low Power Crossbar Array Applications" Electrochemical Society ECS Transactions, 2019.

249. Ying-Chen Chen, Hui-Chun Huang, Chih-Yang Lin, Szu-Tung Hu, Yao-Feng Chang and Jack C. Lee "Selectorless Resistive Switching Memory: Non-uniform Dielectric Architecture and Seasoning Effect Determination for Low Power Array Applications" *AIP Advances* (2019) (Featured on cover)

250. Ying-Chen Chen, Chao-Cheng Lin, Szu-Tung Hu, Chih-Yang Lin, Burt Fowler, and Jack Lee "A Novel Resistive Switching Identification Method through Relaxation Characteristics for Sneak-path-constrained Selectorless RRAM application", *Scientific Reports* (2019).

251. Xiaohan Wu, Ruijing Ge, Po-An Chen, Harry Chou, Zhepeng Zhang, Yanfeng Zhang, Sanjay Banerjee, Meng-Hsueh Chiang, Jack C. Lee, Deji Akinwande "Thinnest Nonvolatile Memory Based on Monolayer h-BN", Advanced Materials 31 (15), 1806790. 2019.

252. Myungsoo Kim, Emiliano Pallecchi, Ruijing Ge, Xiaohan Wu, Guillaume Ducournau, Jack C. Lee, Henri Happy, Deji Akinwande, "Analogue switches made from boron nitride monolayers for application in 5G and terahertz communication systems", Nature Electronics vol. 3, p. 479-485 (2020).

253. X. Wu, R. Ge, Y. Huang, D. Akinwande, and J. C. Lee, "Resistance state evolution under constant electric stress on a MoS_2 non-volatile resistive switching device," *The Royal Society of Chemistry (RSC) Advances,* vol. 10, no. 69, pp. 42249-42255, 2020.

254. Hyojong Cho, Ji-Ho Ryu, Chandreswar Mahata, Muhammad Ismail, Ying-Chen Chen, Yao-Feng Chang, Seongjae Cho, Alexey N Mikhaylov, Jack C Lee, Sungjun Kim, "Bipolar resistive switching with unidirectional selector function in nitride/oxide heterostructures" Applied Physics Letters vol. 53 (43) p. 435102 (1-6), 2020.

255. Mostafa Rahimi Azghadi, Ying-Chen Chen, Jason K. Eshraghian, Jia Chen, Chih-Yang Lin, Amirali Amirsoleimani, Adnan Mehonic, Anthony J Kenyon, Burt Fowler, Jack C. Lee, Yao-Feng Chang, "CMOS and Memristive Hardware for Neuromorphic Computing" Advanced Intelligent Systems, p. 1900189: 1-24 (2020).

256. Ying-Chen Chen, Chih-Yang Lin, Hyojong Cho, Sungjun Kim, Burt Fowler, and Jack C. Lee, "Current-Sweep Operation on Nonlinear Selectorless RRAM for Multilevel Cell Applications" Journal of Electronic Materials, vol. 49, no. 6, p. 3499-

3503 (2020).

257. Yang, Hanjie; Wang, Yang; Zou, Xingli; Bai, Rongxu; Han, Sheng; Wu, Zecheng; Han, Qi; Zhang, Yu; Zhu, Hao; Chen, Lin; Lu, Xionggang; Sun, Qing-Qing; Lee, Jack; Yu, Edward; Akinwande, Deji; Ji, Li, "Growth mechanisms and morphology engineering of atomic layer deposited WS2" accepted to ACS Applied Materials & Interfaces, August 2021.

258. Ying-Chen Chen, Jack Lee, Chih-Yang Lin, "Dual-functional Hybrid Selectorless RRAM and Selection Device for Memory Array Application" *IEEE Transactions on Electron Device*, volume 68, issue 9, p. 4363-4367, Sept. 2021.

259. Hanjie Yang, Yang Wang, Xingli Zou, Rong-Xu Bai, Sheng Han, Zecheng Wu, Qi Han, Yu Zhang, Hao Zhu, Lin Chen, Xionggang Lu, Qingqing Sun, Jack C. Lee, Edward T. Yu, Deji Akinwande, and Li Ji, "Growth Mechanisms and Morphology Engineering of Atomic Layer-Deposited WS_2", ACS Appl. Mater. Interfaces, (2021).

260. Ruijing Ge, Xiaohan Wu, Liangbo Liang, Yuqian Gu, Emmanuel Okogbue, Harry Chou, Jianping Shi, Yanfeng Zhang, Sanjay K. Banerjee, Yeonwoong Jung, Jack C. Lee, Deji Akinwande "A library of atomically thin 2D nanomaterials with resistive switching characteristics" *Advanced Materials*. 2021.

261. Ying-Chen Chen, Chao-Cheng Lin, Yao-Feng Chang, Yao-Feng Chang, "Post-Moore Memory Technology: Sneak Path Current (SPC) Phenomena on RRAM Crossbar Array and Solutions", Micromachines 12 (1), 50 (2021).

262. Y. Huang, X. Wu, Y. Gu, R. Ge, D. Akinwande, and J. C. Lee, "On the stochastic nature of conductive points formation and their effects on reliability of MoS2 RRAM: experimental characterization and Monte Carlo simulation," *Microelectronics Reliability*, 126, 114274, 2021.

263. Y. Gu, M. I. Serna, S. Mohan, A. Londoño-Calderon, T. Ahmed, Y. Huang, J. Lee, S. Walia, M. T. Pettes, K. M. Liechti, and D. Akinwande, "Sulfurization Engineering of One-step Low-temperature MoS2 and WS2 Thin Films for Memristor Device Applications" *Advanced Electronic Material*, 8(2): 2100515, 2021.

264. Hanjie Yang, Yang Wang, Xingli Zou, Rong-Xu Bai, Sheng Han, Zecheng Wu, Qi Han, Yu Zhang, Hao Zhu, Lin Chen, Xionggang Lu, Qingqing Sun, Jack C. Lee, Edward T. Yu, Deji Akinwande, and Li Ji, "Wafer-scale synthesis of WS_2 films with in-situ controllable p-type doping by atomic layer deposition", Research, Volume 2021, Article ID 9862483, Dec. 2021.

265. Zecheng Wu, Yu Zhang, Shiqiang Lu, Rongxu Bai, Na Gao, Kai Huang, Shen Hu, Qingqing Sun, David Wei Zhang, Jack C. Lee, Edward T. Yu, and Li Ji, "Amorphous semi-insulating Al-doped In_2O_3 growth by atomic layer deposition for thin-film transistors," Journal of Vacuum Science & Technology A, Volume 40, Issue 4,

042402, May 12, 2022.

266. Xiaohan Wu, Yuqian Gu, Ruijing Ge, Martha I. Serna, Yifu Huang, Jack C. Lee, and Deji Akinwande, "Electron irradiation-induced defects for reliability improvement in monolayer MoS2-based conductive-point memory devices". *npj 2D Materials and Applications*, *6*(1), 1-12, 2022.

267. Alam, Md Hasibul; Chowdhury, Sayema; Roy, Anupam; Wu, Xiaohan; Ge, Ruijing; Rodder, Michael; Chen, Jun; Lu, Yang; Stern, Chen; Houben, Lothar; Chrostowski, Robert; Burlison, Scott; Yang, Sung Jin; Serna, Martha; Dodabalapur, Ananth; Mangolini, Filippo; Naveh, Doron; Lee, Jack C.; Banerjee, Sanjay; Warner, Jamie; Akinwande, Deji "Wafer-Scalable Single Layer Amorphous Molybdenum Trioxide", *ACS Nano* 2022, 16, 3, 3756–3767, February 21, 2022.

268. Y.-C. Chen, S. Sarkar, J. G. Gibbs, Y. Huang, J. C. Lee, C.-C. Lin, C.-H. Lin. "Nano Helical-Shaped Dual-Functional Resistive Memory for Low-Power Crossbar Array Application". *ACS Applied Engineering Materials*, 1, 1, 252–257, 2022.

269. Y. Huang, R. Hopkins, D. Janosky, Y.-C. Chen, Y.-F. Chang and J. C. Lee. "Effect of Temperature on Analog Memristor in Neuromorphic Computing". *IEEE Transactions on Electron Devices*, 69 (11), 6102-6105, 2022.

270. Ying-Chen Chen, Yifu Huang, Sumant Sarkar, John Gibbs, Jack C. Lee, "Direct-Grown Helical-Shaped Tungsten-Oxide-Based Devices with Reconfigurable Selectivity for Memory Applications" *J. Low Power Electron. Appl.* 12(4), 55 (2022)

271. Y. Huang, Y. Gu, X. Wu, R. Ge, Y.-F. Chang, Y.-C. Chen, D. Akinwande, J. Lee. "Understand the Resistive Switching and Reliability Mechanisms of 2D TMD Material: Defect Engineering, Finite Element Analysis and Monte Carlo Modeling". *Bulletin of the American Physical Society*, 2023.

272. Y. Huang, Y. Gu, Y.-F. Chang, Y.-C. Chen, D. Akinwande, J. C. Lee. "Understanding the Resistive Switching Mechanism of 2D RRAM: Monte Carlo Modeling and a Proposed Application for Reliability Research". *IEEE Transactions on Electron Devices*, 1-6, 1557-9646, 2023.

273. Y.-C. Chen, Y. Huang, J. C. Lee, J. B. Stouffer. "Self-Selective Dielectric-Fuse Effect with Ambient Factors in Oxide-Based Memory". *ECS Journal of Solid-State Science and Technology*, 12(6): 065003, 2023.

274. Y. Huang, Y. Gu, S. Mohan, A. Dolocan, N. D. Ignacio, S. Kutagulla, K. Matthews, A. Londono-Calderon, Y.-F. Chang, Y.-C. Chen, J. H. Warner, M. T. Pettes, J. C. Lee, D. Akinwande. "Reliability improvement and effective switching layer model of thin-film MoS2 memristors". *Advanced Functional Materials*, 34 (15), 2214250 (2024).

275. Seonjeong Leea, Yifu Huangb, Yao-Feng Chang, Seungjae Baik, Jack C. Lee, and Minsuk Koo, “Enhancing simulation feasibility for multi-layer 2D MoS2 RRAM devices: reliability performance learnings from passive network model”, RSC Physical Chemistry Chemical Physics, Accepted, 2024.

Refereed Conference Publications

1. S. Holland, I-C Chen, J. Lee, Y. Fong, K.K. Young, and C. Hu, "Time-Dependent Breakdown of Thin Oxides," Electrochemical Society Meeting, vol. 86-2, p. 599 - 600, Fall 1986.

2. Y. Fong, I-C Chen, S. Holland, J. Lee and C. Hu, "Dynamic Stressing of Thin Oxides," IEEE International Electron Devices Meeting Technical Digest, p. 664 - 667, December 1986.

3. K. Mayaram, J. Lee, T.Y. Chan and C. Hu, "An Analytical Perspective of LDD MOSFETs," 1986 Symposium on VLSI Technology, no. VI-1, p. 61 - 62, May 1986.

4. J. Lee, I-C Chen, S. Holland, Y. Fong and C. Hu, "Oxide Defect Density, Failure Rate and Screen Yield," 1986 Symposium on VLSI Technology, no. VI-5, p. 69 - 70, May 1986.

5. I-C Chen, J. Lee and C. Hu, "Accelerated Testing of Silicon Dioxide Wearout," 1987 Symposium on VLSI Technology, no. IV-2, p. 23 - 24, May 1987.

6. J. Lee, I-C Chen and C. Hu, "Statistical Modeling of Silicon Dioxide Reliability," IEEE International Reliability Physics Symposium, 26th annual proceeding, p. 131 - 138, April 1988 [Best Paper Award].

7. J. Lee and C. Hu, "Low-Pressure Chemical Vapor Deposited Oxide Process for MOS Device Application," 1988 Symposium on VLSI Technology, no. V-8, p. 49 - 50, May 1988.

8. C. Hu, P. Ko, P. Lee, J. Lee, N. Cheung and B. Liew, "IC Reliability Prediction," SRC Technical Program Conference, Extended Abstract, p. 240, October 1988.

9. R. Moazzami, J. Lee, I-C Chen and C. Hu, "Projecting the Minimum Acceptable Oxide Thickness for Time-Dependent Dielectric Breakdown," IEEE International Electron Devices Meeting Technical Digest, p. 710 - 713, December 1988.

10. J. Carrano, C. Sudhama, J. Lee, A. Tasch and W. Miller, "Electrical and Reliability Characteristics of Lead-Zirconate-Titanate (PZT) Ferroelectric Thin Films for DRAM Application," IEEE International Electron Devices Meeting Technical Digest, p. 255 - 258, December 1989.

11. J. Carrano, C. Sudhama, J. Lee and A. Tasch, "Electrical and Reliability Properties of PZT Thin Films for ULSI DRAM Applications," SEMATECH Centers of Excellence Coordination Meeting, March 20-22, 1990 (Best Paper Award).

12. J. Lin, K. Park, S. Batra, S. Yoganathan, J. Lee, S. Banerjee, S. Sun, J. Yeargain, G. Lux, "Effects of Arsenic Segregation and Electron Trapping on the Capacitance-Voltage Behavior of Polysilicon and Polycide Gates," Materials Research Society Proceeding, vol. 182, p. 195 - 200, April 1990.

13. C. Sudhama, J. Carrano, L. Parker, V. Chikarmane, J. Lee, A. Tasch, W. Miller, N. Abt and W. Shepherd, "Scaling Properties in the Electrical and Reliability Characteristics of Lead-Zirconate-Titanate (PZT) Ferroelectric Thin Film Capacitors," Proc. of the Spring Meeting of the Materials Research Society, vol. 200, p. 331 - 336, April 1990.

14. H. Hwang, W. Ting, D.L. Kwong and J. Lee, "High Quality Ultrathin Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," Solid State Devices Meeting, p. 1155 - 1156, August 1990.

15. H. Hwang, W. Ting, B. Maiti, D. L. Kwong and J. Lee, "Electrical Characteristics of Ultrathin Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," SRC Technical Program Conference, Extended Abstract, p. 91 - 94, October 1990.

16. V. Chikarmane, C. Sudhama, J. Carrano, J. Lee and A. Tasch, " Material Characterization of Sol-Gel Derived PZT Films for ULSI DRAM Applications," Proc. of SRC Technical Program Conference, p. 139 - 142, October 1990.

17. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "Electrical Characteristics of Ultrathin Oxynitride Gate Dielectric Prepared by Rapid Thermal Oxidation of Si in N_2O," Electrochemical Society Meeting, Extended Abstract # 312, October 1990.

18. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "Electrical and Reliability Characteristics of Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," IEEE International Electron Devices Meeting Technical Digest, p. 421 - 424, December 1990.

19. S. Bhattacharya, S. Banerjee, J. Lee, A. Tasch and A. Chatterjee, "Deign Issues for Achieving Latchup-Free, Deep Trench-Isolated, Bulk, Non-Epitaxial, Submicron CMOS," IEEE International Electron Devices Meeting Technical Digest, p. 185 - 188, December 1990.

20. V. Chikarmane, C. Sudhama, J. Lee, and A. Tasch, "The Effects of Pb Compensation and Thermal Processing on the Characteristics of DC-Magnetron Sputtered Lead Zirconate Titanate Thin Films," Proc. of the Spring Meeting of the Materials Research Society, Vol. 230, p. 297 - 300, April 1991.

21. H. Hwang, W. Ting, D. L. Kwong and J. Lee, "Ultrathin Oxynitride Gate Dielectric Prepared by Rapid Thermal Oxidation in N_2O for ULSI Applications," Proc. of the Spring Meeting of the Materials Research Society, p. 379 - 384, April 1991.

22. J. Lin, K. Park, S. Batra, S. Banerjee, J. Lee and G. Lux, "Effects of $TiSi_2$ Formation on Boron Penetration Through Gate Oxides in MOS Devices Under Rapid Thermal Processing," Proc. of the Spring Meeting of the Materials Research Society, p. 152 - 155, April 1991.

23. H. Hwang, W. Ting, D. L. Kwong, and J. Lee, "Excellent Reliability Characteristics of Submicron MOSFETs with Oxynitride Gate Dielectric Prepared by Rapid Thermal Oxidation in N_2O," SPIE Optical Engineering Conference, May 8-10, 1991.

24. C. Sudhama, V. Chikarmane, J. Kim, J. Lee and A. Tasch, "Measurement Techniques for Characterization of Ferroelectric Thin Films for Memory Applications," SPIE Optical Engineering Conference, May 8-10, 1991.

25. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "The Effects of Pb Compensation and Thermal Processing on the Phase Content and Electrical Characteristics of DC-Magnetron Sputtered PZT Thin Films," SPIE Optical Engineering Conference, May 8-10, 1991.

26. J. Lin, K. Park, S. Batra, S. Banerjee, J. Lee and G. Lux, "Effects of $TiSi_2$ Formation on Boron Penetration through Gate Oxides in MOS Devices," SPIE Optical Engineering Conference, May 8-10, 1991.

27. B. Maiti and J. Lee, "Stacked Thermal/LPCVD Oxide for Ultra-thin Gate Dielectric Application," SPIE Optical Engineering Conference, May 8-10, 1991.

28. B. Maiti and J. Lee, "The Effects of Post-Deposition Annealing on Dielectric Integrity of Thin Chemical Vapor Deposited Oxides," SPIE Optical Engineering Conference, May 8-10, 1991.

29. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "The Effects of Deposition Temperature and Annealing on the Material and Electrical Characteristics of DC-Magnetron Sputtered PZT Thin Films Capacitors," Electronic Materials Conference, Technical Program Abstract, p. 2 - 7, June, 1991.

30. K. Picone, S. Batra, K. Park, M. Lobo, S. Bhattacharya, J. Lee and S. Banerjee, "Leakage Characteristics and Lateral Uniformity of Ultra-Shallow Junctions Formed Using Polysilicon and Amorphous Silicon Diffusion Source," Electronic Materials Conference, June, 1991

31. H. Hwang, W. Ting, D. L. Kwong, J. Lee, "Electrical and Reliability Characteristics of Submicron nMOSFET's with Oxynitride Gate Dielectrics Prepared by Rapid Thermal Oxidation in N_2O," Device Research Conference, p. IVB-6 - IVB-7, June, 1991.

32. C. Sudhama, V. Chikarmane, J. Kim, J. Lee and A. Tasch, "Electrically Induced Improvement in the Properties of Thin Ferroelectric Films for NVRAM and DRAM Cells," Proceedings of the 10th Annual Symposium on Electronic Materials, Processing and Characterization Conference, June 3-4, 1991.

33. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "Electrical Characteristics and Structure Property Relationships in DC-Magnetron Sputtered PZT Thin Film Capacitors Annealed in Oxygen and Nitrogen Ambient for ULSI DRAM Applications, " 10th Annual Symposium on Electronic Materials Processing and Characterization, June 1991.

34. C. Maziar and J. Lee, "Team Teaching a Multi-Section Introductory Electronics Course," Proceedings of the 1991 Frontiers in Education Conference, p.709 West Lafayette, IN, September 21-24, 1991.

35. V. Chikarmane, J. Kim, C. Sudhama, J. Lee and A. Tasch, "Growth and Electrical Characterization of $Pb(Zr_XTi_{1-X})O_3$ Thin Films for Memory Applications," 3rd Annual New Mexico Symposium on Ceramics and Advanced Materials, October 24, 1991.

36. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "Effects of Post-deposition Annealing Ambient on the Electrical Characteristics and Phase-Transformation Kinetics of Sputtered Lead Zirconate Titanate (65/35)Thin Film Capacitors," American Vacuum Society 38th Annual Symposium, Seattle, WA, November, 1991.

37. C. Sudhama, J. Kim, V. Chikarmane, J. Lee and A. Tasch, "The Effects of La Doping on the Electrical Properties of Sol-Gel Derived Ferroelectric Lead-Zirconate-Titanate (PZT) for ULSI DRAM Application," American Vacuum Society 38th Annual Symposium, Seattle, WA, November 1991.

38. V. Chikarmane, C. Sudhama, J. Kim, J. Lee and A. Tasch, "The Role of the PZT-Pt Interface in the Anomalous Phase Transformation Kinetics in Sputtered Thin Film Capacitors at sub-200nm Thicknesses," Proceeding of the Fall Meeting of the Materials Research Society, Vol. 243, p. 367 - 372, December 1991.

39. C. Sudhama, J. Kim, V. Chikarmane, J. Lee and A. Tasch, "Polarity and Area Dependence of Reliability Characteristics of Sputtered and Sol-Gel Derived Thin PLZT Films for DRAM Applications," Proceeding of the Fall Meeting of the Materials Research Society, Vol. 243, p. 147 - 152, December 1991.

40. V. Chikarmane, J. Kim, C. Sudhama, J. Lee and A. Tasch, "The Dependence of Device Electrical Properties on the Zr/Ti Ratio in Reactively Sputtered Ferroelectric $Pb(Zr_XTi_{1-X})O_3$ Thin FIlms for Memory Applications," Minerals, Metals and Materials Society (TMS) Annual Meeting, San Diego, CA, March 1992.

41. J. Lee, V. Chikarmane, C. Sudhama, J. Kim and A. Tasch, "Sputtered PZT Thin Films for Memory Applications," 4th International Symposium on Integrated Ferroelectrics, Monterey, CA, March 1992, Invited Paper.

42. W. Chen, J. Lin, S. Banerjee and J. Lee, "Thermal Stability of Cobalt Disilicide for Self-Aligned Silicide Applications," Spring Meeting of Materials Research Society, Mat. Res. Soc. Symp. Proc., vol. 260, p.163 - 167, April 1992.

43. J. Lin, W. Chen, S. Banerjee and J. Lee, "Study of SITOX (SIlicidation Through OXide) Process and its Application to Advanced CMOS Devices," Spring Meeting of Materials Research Society, Mat. Res. Soc. Symp. Proc., vol. 260, p.623 - 628, April 1992.

44. M. Hao, J. Lee, I.C. Chen and C. Teng, "Reliability of Submicron MOSFET's with Deposited Gate Oxides Under F-N Injection and Hot-Carrier Stress," Spring Meeting of Materials Research Society, Mat. Res. Soc. Symp. Proc., vol. 265, p. 237 - 242, Sept. 1992.

45. H. Hwang and J. Lee, "Excellent Boron Diffusion Barrier Characteristics of Oxynitride Gate Dielectric Prepared by Rapid Thermal Processing in N_2O," Spring Meeting of Materials Research Society, April 1992.

46. B. Maiti and J. Lee, "Electrical and Reliability Characteristics of Silicon-Rich Oxide for Non-volatile Memory Applications," Spring Meeting of Materials Research Society, vol. 265, p. 255 - 260, April 1992.

47. J. Kim, V. Chikarmane, C. Sudhama, J. Lee and A. Tasch, "The Impact of Device Asymmetry on the Fatigue-Endurance of Ferroelectric PZT for Memory Applications," Spring Meeting of Materials Research Society, vol. 265, p. 313 - 318, April 1992.

48. B. Maiti and J. Lee, "Highly-Reliable Stacked Thermal/LPCVD Oxides for Ultrathin Gate Dielectric Applications," Spring Meeting of Materials Research Society, vol. 265, p. 261 - 266, April 1992.

49. C. Sudhama, J. Kim, V. Chikarmane, R. Khamankar, J. Lee and A. Tasch, "Optimization of Pb Compensation with Thickness-Scaling of Thin Sputtered PZT Films in the 200nm Range for Memory Applications," Electronic Materials Conference, June 1992.

50. J. Lin, W. Chen, S. Banerjee and J. Lee, "Cobalt Disilicide as a Dopant Source for Polysilicon Gates in MOS Devices," Electronic Materials Conference, June 1992, Journal of Electronic Materials, vol. 22, No. 6, p. 667 - 673, 1993.

51. B. Maiti and J. Lee, "A New Low-Thermal Budget Process for Ultrathin Oxynitride Dielectric," Electronic Materials Conference, June 1992.

52. J. Kim, V. Chikarmane, C. Sudhama, R. Khamankur and J. Lee, "The Enhancement of Lifetime of Sputtered Lead Zirconate Titanate Thin Film Capacitors Under A.C. Stressing," Electronic Materials Conference, June 1992.

53. V. Chikarmane, C. Sudhama, J. Kim, R. Khamankar and J. Lee, "Sputtered ZPT Thin Films with Low-Thermal Budget for I.C. Applications," Electronic Materials Conference, June 1992.

54. B. Maiti, M.Y. Hao and J. Lee, "Incorporation of Nitrogen into Oxynitride Dielectrics through Thermal Nitridation of Silicon," Spring Meeting of Materials Research Society, vol. 309, p.3 - 8, 1993.

55. W. Chen, J. Lin, S. Banerjee and J. Lee, "The Impact of Pre-Silicidation Heat Treatment and Dopant Effects on the Thermal Stability of $CoSi_2$ Polycide during Rapid Thermal Annealing," Materials Research Society Symposia Proceeding, vol. 303, p. 81 - 86, 1993.

56. W. Chen J. Lin, S. Banerjee and J. Lee, "Using $CoSi_2$/Polysilicon Polycide Structure as a Gate Diffusion Source in Rapid Thermal Processing," Materials Research Society Symposia Proceeding, vol. 303, p. 271 - 276, 1993.

57. J. Lin, W. Chen, S. Banerjee and J. Lee, "Enhanced Boron Diffusion in Silicon Using $CoSi_2$ Diffusion Source and Rapid Thermal Processing," Materials Research Society Symposia Proceeding, vol. 303, p. 265 - 270, 1993.

58. J. Kim, C. Sudhama, R. Khamankar and J. Lee, "Ultra-Thin (65nm) Sputtered PZT Films for ULSI DRAMs," Materials Research Society Symposium Proceedings, vol. 310, p.473 - 478, 1993.

59. J. Kim, R. Khamankar, C. Sudhama, J. Lee, S. Summerfelt and B. Gnade, "Investigation of Electrode Materials for Metal-Ferroelectrics-Pt Capacitors for DRAM Applications," 184th Meeting of Electrochemical Society Meeting, Extended Abstracts, vol. 93-2, p. 269 - 270, Oct. 1993.

60. W. M. Chen, J. C. Lee, and M. R. Frost, " Silicided p-n junction fabricated by silicidation through silicon buffer layer and dopant drive-out process ," Mat. Res. Soc. Symp. Proc., vol. 320, p. 47 - 51, 1993.

61. J. Lee, C. Sudhama, J. Kim and R. Khamankar, "High Dielectric Constant Ferroelectric Thin Films for DRAM Applications," International Conference on Solid State Devices and Materials, Chiba, Japan, 1993(Invited Paper).

62. C. Sudhama, R. Khamankar, J. Kim, J. C. Lee, P. D. Maniar, R. Moazzami, R. E. Jones and C. J. Mogab, "Novel Methods for the Reliability Testing of Ferroelectric DRAM Storage Capacitors," 32nd Annual IEEE International Reliability Physics Proceedings, p. 238 - 242, 1994.

63. J. Kim, C. Sudhama, R. Khamankar, B. Jiang, J. Lee, P. Maniar, R. Moazzami, R. Jones and C. J. Mogab, "La Doped PZT Thin Films for Gigabit DRAM Technology," 1994 Symposium on VLSI Tech. Digest, Honolulu, June 1994 and published in VLSI Tech. Digest, p. 151 - 152, 1994.

64. R. Khamankar, J. Kim, C. Sudhama and J. Lee, "Effect of Deposition Temperature on Material and Electrical Properties of PZT Thin Films for DRAM Applications," International Symposium on Integrated Ferroelectrics, 1994, published in Integrated Ferroelectrics, 1994.

65. K. Lai, M. Y. Hao, W. M. Chen, and J. Lee, "Surface Cleaning Effects on Reliability for Devices with Ultrathin Oxides or Oxynitrides," Proceedings of SPIE Conference on Microelectronics Manufacturing '94, vol. 2334, p. 137-143, Oct. 1994.

66. R. Khamankar, J. Kim, B. Jiang, and J. Lee, "Effects ac Stress on Charge and Voltage Decay Rates of PZT Thin Film Capacitors for DRAM Applications," Material Research Symposium Fall Meeting, Boston, MA, Nov. 1994.

67. B. Jiang, J. Kim, R. Khamankar, I. Lee, and J. Lee, "Effects of Electron-beam Irradiation on PZT/PLZT Thin Film Capacitors," Material Research Symposium Fall Meeting, Boston, MA, Nov. 1994.

68. J. Kim, B. Jiang, R. Khamankar, I. Lee, J. Lee, P. Maniar, R. Moazzami, and R. Jones, "Effects of Microstructure on the Electrical Characteristics of Sol-Gel Derived PZT Thin Films," Material Research Symposium Fall Meeting, Boston, MA, Nov. 1994

69. R. Khamankar, J. Kim, B. Jiang, J. Lee, P. Maniar, R. Moazzami, R. Jones, "Impact of Process Damages on Performance of High Dielectric Constant PLZT Capacitor for ULSI DRAM Applications," IEEE International Electron Devices Meeting Technical Digest, p. 337 - 339, Dec. 1994.

70. M. Y. Hao, K. Lai, W. M. Chen and J. Lee, "Reliability Characteristics and Surface Preparation Technique for Ultra-thin (33 Å - 87 Å) Oxides and Oxynitrides," IEEE International Electron Devices Meeting Technical Digest, p. 601 - 603, Dec. 1994.

71. W. M. Chen, J. Lin and J. Lee, "A Novel $CoSi_2$ Thin Film Process with Improved Thickness Scalability and Thermal Stability," IEEE International Electron Devices Meeting Technical Digest, p. 691 - 695, Dec. 1994.

72. K. Lai, A. Chou, K. Kumar, P. Chowdhury, M. Hao, W. Chen, M. Gardner, J. Fulford and J. Lee, "Breakdown Mechanisms and Stress-Induced Leakage Current in Ultra-thin Oxides and N_2O Oxynitrides," Eleventh Biennial University/ Government / Industry Microelectronics Symposium, May 1995.

73. C. Sudhama, J. Kim, V. Chikarmane, R. Khamankar, J. Lee and A. Tasch, "Optimization of Pb Compensation with Thickness-Scaling of Thin Sputtered PZT Films in the 200nm Range for Memory Applications," Journal of Electronic Materials.

74. R. Khamankar, B. Jiang, R. Tsu, W. Hsu, J. Nulman, S. Summerfelt, M. Anthony and J. Lee, "A Novel Low-Temperature Process for High Dielectric Constant BST Thin Films for ULSI DRAM Applications," presented at the 1995 Symposium on VLSI Technology, Kyoto, Japan, May 1995 and published in VLSI Techn. Digest, p. 127 - 128, 1995.

75. Jack C. Lee, Anthony Chou, Kafai Lai and Kiran Kumar, "N_2O-Based tunnel oxides", Proceedings of SPIE Conference on Microelectronics Manufacturing '95, vol. 2636, p. 182.

76. Kafai Lai, Anthony Chou, Kiran Kumar, Mark Gardner, Jim Fulford, and Jack C. Lee, "Effects of gate doping species, concentration, and microstructure on the electrical and reliability characteristics of ultrathin oxides and N_2O-oxynitrides", Proceedings of 1995 International Semiconductor Device Research Symposium, Dec. 1995.

77. Kafai Lai, Kiran Kumar, Anthony I. Chou, and Jack C. Lee, "Effects of oxide exposure, photoresist and dopant activation on the plasma damage immunity of ultrathin oxides and oxynitrides", Tech. Dig. IEEE Int. Elec. Dev. Mtg. Tech. Dig., p. 319, 1995.

78. T. Chen, V. Balu, B. Jiang, S. Kuah and J. Lee, "Stability of Reaactive DC-Sputtered Ir and IrO_2 Thin Films in Various Ambients,"presented at the Int. Symp. on Integrated Ferroelectrics, March 18-20, Tempe, AZ, 1996 and published in ISIF Extended Abstract, p. 48C, 1996.

79. B. Jiang and J. Lee, "Modeling Ferroelectric Capacitor Switching Using Parallel-Element Model," presented at the Int. Symp. on Integrated Ferroelectrics, March 18-20, Tempe, AZ, 1996 and published in ISIF Extended Abstract, p. 49C, 1996.

80. V. Balu, T. Chen, B. Jiang, S. Kuah and J. Lee, P. Chu, R. Joens, P. Zurcher, D. Taylor and S. Gillespie, "Electrode Materials for Ferroelectic Capacitors: Properties of Reactive DC Sputtered IrO_2 Thin Films," 1996 Materials Research Society Spring Meeting, San Francisco, CA, April 8-12, 1996; abstract no. T4.3, 1996 MRS Abstract Proceeding, p. 337, 1996 and published in MRS Symposium Proceedings, Ferroelectric thin films V, p.169, 1996.

81. B. Jiang, V. Balu, T. Chen, S. Kuah, and J. Lee, "Polarization Relaation in PZT/PLZT Thin Film Capacitors, " 1996 Materials Research Society Spring Meeting, San Francisco, CA, April 8-12, 1996; abstract no. T6.3, 1996 MRS Abstract Proceeding, p. 340, 1996.

82. B. Jiang, V. Balu, T. Chen, Jack Lee, P. Chu, R. Jones, P. Zurcher, D. Taylor, M. Kottke, and S. Gillespie, "A New Electrode Technology for High-Density Nonvolatile

Ferroelectric (SrBi2Ta2O9) Memories," presented at the 1996 Symposium on VLSI Technology, Honolulu, June 1996 and published in VLSI Techn. Digest, p. 26-27, 1996.

83. C. Lin, A. Chou, K. Kumar, P. Chowdhury, and J. C. Lee, "Leakage current, reliability characteristics and boron penetration of ultra-thin (32-36Å) O2-oxide and N2O/NO-Oxynitrides, Tech. Dig. IEEE Int. Elec. Dev. Mtg. Tech. Dig., 1996, p-331.

84. C. Lin, A. Chou, B. Doyle, H. R. Soleimani, and J. C. Lee, "Effect of nitrogen implant on gate oxide reliability," 27th IEEE Semiconductor Interface Specialists Conference, San Diego, CA, 1996.

85. Tung-Sheng Chen, Venkatasubramani Balu, Bo Jiang, Shao-Hong Kuah, and Jack Lee, "Stability of reactive DC-sputtered Ir and IrO_2 thin films in various ambients," International Symposium on Integrated Ferroelectrics (ISIF), 1996.

86. Tung-Sheng Chen, Daniel Hadad, Venkatasubramani Balu, Bo Jiang, Shao-Hong Kuah, Paul McIntyre, Scott Summerfelt, Mark Anthony, and Jack Lee, "Ir-electroded BST thin film capacitors for 1 giga-bit DRAM application," Tech. Dig. IEEE Int. Elec. Dev. Mtg. (IEDM), p. 679, 1996.

87. Shaohong Kuah, Venkatasubramani Balu, Tung-Sheng Chen, Bo Jiang, Daniel Hadad, Bruce White, Robert Jones, Peter Zurcher, Bradley Melnick, Sherry Gillespie and Jack C. Lee, "Interaction of Ir and IrO_2 Thin Films with Polysilicon, W and WSi_X". The 9th International Symposium on Integrated Ferroelectrics (ISIF), p. 150C, Mar 2-5, 1997.

88. Daniel Hadad, Tung-Sheng Chen, Venkatasubramani Balu, Bo Jiang, ShaoHong Kuah, Paul McIntyre, Scott Summerfelt, Mark Anthony and Jack C. Lee, "The Effects ofForming Gas Anneal on the Electrical Characteristics of Ir-Electroded BST Thin Film Capacitors" The 9th International Symposium on Integrated Ferroelectrics (ISIF), p. 152C, Mar 2-5, 1997.

89. A. Chou, C. Lin, K. Kumar, P. Chowdhury, M. Garder, M. Gilmer, J. Fulford, and J. C. Lee, "The effects of nitrogen implant into gate electrode on the characteristics of dual-gate MOSFETS with ultra-thin oxide and oxynitrides," International Reliability Physics Symposium, 1997.

90. Bo Jiang, P. Zurcher, R. Jones, S. Gillespie, and J. Lee, "Computationally Efficient Ferroelectric Capacitor Model for Circuit Simulation," presented at the 1997 Symposium on VLSI Technology, Kyoto, Japan, June 1997 and published in VLSI Tech. Digest, p. 141-142, 1997.

91. Chou, Chan Lin, Keith Zawadzki, Yongjoo Jeon, Aaron Lucas and Jack Lee, "Enhanced oxidation rate of oxynitrides during RTP in N_2O," the 28th IEEE Semiconductor Interface Specialists Conference, Charleston, SC, 1997.

92. Venkatasubramani Balu, Tung-Sheng Chen, Shylaja Katakam, Jian-Hung Lee, Bruce White, Sufi Zafar, Bo Jiang, Peter Zurcher, Robert E. Jones and Jack C. Lee, "Dielectric Dispersion in Barium Strontium Titanate Thin Film capacitors with Ir electrodes", Presented at the 10th International Symposium on Integrated Ferroelectrics, March 1-4, 1998, Published in the Integrated Ferroelectrics.

93. Tung-Sheng Chen, Venkatasubramani Balu, Shylaja Katakam, Jian-Hung Lee, B. White, S. Zafar, B. Jiang, P. Zurcher, R. Jones and Jack C. Lee, "Study of $SrTiO_3$ Thin Films on Ir Bottom Electrodes for Ultra-large scale Integrated DRAM application" Presented at the 10th International Symposium on Integrated Ferroelectrics, Mar 1-4, 1998, Published in the Integrated Ferroelectrics.

94. Tung-Sheng Chen, Venkatasubramani Balu, Shylaja Katakam, Jian-Hung Lee, Jeong Hee Han, Robert E. Jones, Sherry Gillespie and Jack C. Lee, "Dynamic Stressing Effects on Reliability of Strontium Titanate Thin Film Capacitors for High-density Memory Applications" 1998 Symposium on VLSI Technology Digest of Technical Papers, p. 54, (1998).

95. Keith Zawadzki, Wen Jie Qi, Yongjoo Jeon, Byoung Hun Lee, Aaron Lucas, Renee Nieh, and Jack Lee, "Sputtered BST Thin Films for Alternative High K Gate Dielectrics", Proceedings of American Vacuum Society Symposium, Austin, 1998.

96. Byoung Hun Lee, Yongjoo Jeon, Keith Zawadzki, Wen-Jie Qi, Renee Nieh, Aaron Lucas and Jack Lee, "Leakage characteristics of TiO2 films", Proceedings of American Vacuum Society Symposium, Austin, 1998.

97. Yongjoo Jeon, Keith Zawadzki, Byoung Hun Lee, Venkatsubramani Balu, and Jack Lee, "Alternative Gate Dielectric with BST/TiO2(Barrier Layer) Stacked Structure", Abstracts of MRS Symposium on Rapid thermal and Integrated Processing, San Fransisco, April 10, p.370, 1998.

98. Byoung Hun Lee, Yongjoo Jeon, Aaron Lucas, Mark Gilmer, Mark Gardner, Jim Fair and Jack C. Lee, "Comparative study of TiO_2 and Ta_2O_5 on JVD nitride as an alternative gate dielectrics", 29th IEEE Semiconductor Interface Specialists Conference, December 1998.

99. Jian-Hung Lee, Venkatasubramani Balu, Tung-Sheng Chen, Jeong Hee Hanand Jack C. Lee, "N2O Processed Ferroelectric Thin Films", MRS Symposium Proceedings, Ferroelectric thin films VII, 1998.

100. Yongjoo Jeon, Byoung Hun Lee, Keith Zawadzki, Wen-Jie Qi, Aaron Lucas, Renee Nieh and Jack Lee, "Effect of Barrier layer on the Electrical and Reliability Characteristics of High-k gate dielectric films", IEEE Tech. Dig. Of International Electron Devices Meeting, p. 707, December 1998.

101. Jeong Hee Han, Venkatasubramani Balu, Jian-Hung Lee, Razak Mohammedali, Sundar Gopalan, Chun-Hui Wong and Jack C. Lee, "Effect of N_2O on RF-magnetron sputtered $SrTiO_3$ films for ULSI DRAM applcation," Presented at the 11th International Symposium on Integrated Ferroelectrics, March 1999.

102. Renee Nieh, Wen-Jie Qi, Yongjoo Jeon, Byoung Hun Lee, Aaron Lucas and Jack C. Lee," Nitrogen implantation to suppress growth of interfacial oxide in MOCVD BST and sputtered BST films", Proceedings of MRS spring meeting,1999.

103. J. Lee, "ZrO_2 Thin Films for Gate Dielectric Applications" an Invited Talk to be presented at the Taiwan Future Development Conference, Hsin-Chu, Taiwan, June 24, 1999.

104. J. Lee, "ZrO_2 and Zr-Silicate Ultra-thin Gate Dielectrics" an Invited Talk to be presented at the SEMATECH Gate Stacked Workshop, Austin TX, July 22, 1999.

105. J. Lee, "High-K Gate Dielectrics" an Invited Talk to be presented at the SPIE's 1999 Symposium and Education Program on Microelectronic Manufacturing, Santa Clara, CA September 22, 1999.

106. J. Lee, "High-K Films for Gate Dielectric" an Invited Talk to be presented at the First International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology, Tokyo, Japan, October 22-23, 1999.

107. B. Lee, L. Kang, W. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. Lee, "Ultrathin Hafnium oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application," IEEE Tech. Dig. Of International Electron Devices Meeting, p. 133, December 1999.

108. W. Qi, R. Nieh, B. Lee, L. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banerjee, and J. Lee, "MOSCAP and MOSFET Characteristics Using ZrO_2 Gate Dielectric Deposited Directly on Si", IEEE Tech. Dig. Of International Electron Devices Meeting, p. 145, December 1999.

109. L. Kang, B. Lee, W. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. Lee, "Highly Reliable Thin Hafnium Oxide Gate Dielectric," presented at the Materials Research Symposium, Fall 1999.

110. B. Lee, L. Kang, W. Qi, R. Nieh, Y. Jeon, and J. Lee, "Electrical Characteristics of Ultra-Thin Hafnium Oxide Gate Dielectric", Proceedings of the 30th IEEE Semiconductor Interface Specialists Conference, December 1999.

111. W. Qi, R. Nieh, B. Lee, L. Kang, Y. Jeon and J. Lee, "Study on ZrO_2 Deposited Directly on Si as an Alternative Gate Dielectric Material", Proceedings of Materials Research Symposium, vol. 606, 2000.

112. W. Qi, K. Zawadzki, R. Nieh, Y. Jeon, B. Lee, A. Lucas, L. Kang, and J. Lee, "A study on Hysteresis Effect of Barrium Strontium Titanate Thin Films for Alternative Gate Dielectric Application," Proceedings of Materials Research Symposium, vol. 606, 2000.

113. W. Qi, R. Nieh, B. Lee, L. Kang, Y. Jeon, K. Onishi, S. Gopalan, and J. Lee, "Temperature Effect on the Reliability of ZrO_2 Gate Dielectric Deposited Directly on Silicon," IEEE International Reliability Physics Symposium, p. 72, April 2000.

114. Wen-Jie Qi, Byoung Hun Lee, Renee Nieh, Laegu Kang, Yongjoo Jeon, Katsu Onishi, and Jack C. Lee, "High-k gate dielectrics", Proc. SPIE Vol. 3881, p. 24-32, Microelectronic Device Technology III, 2000.

115. Laegu Kang, Yongjoo Jeon, Katsunori Onishi, Byoung Hun Lee, Wen-Jie Qi, Renee Nieh, Sundar Gopalan, and Jack C. Lee, "Single-layer Thin HfO_2 Gate Dielectric with n+-Polysilicon Gate," Symposium on VLSI Technology, pp. 44, 2000.

116. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Katsunori Onishi, Laegu Kang, Yongjoo Jeon, Jack C. Lee, Vidya Kaushik, Bich-Yen Neuyen, Lata Prabhu, Kurt Eigenbeiser, and Jeff Finder,"Performance of MOSFETs with ultra-thin ZrO_2 and Zr silicate gate dielectrics," Symposium on VLSI Technology, pp. 40, 2000.

117. Y. –Y. Fan, S. Mudani, W. Qi, J. C. Lee, A. F. Tasch, L. F. Register, and S. K. Banerjee, "Modeling high k gate current from p-type Si inversion layers", Proceedings of 58th Device Research Conference, p.63, 2000.

118. T. Ngai, W. J. Qi, X. Chen, R. Sharma, J. L. Fretwell, J. C. Lee, S. K. Banerjee, "SiGe and Si PMOSFET's characteristics with ZrO_2 gate dielectric", Proceedings of 58th Device Research Conference, p.21, 2000.

119. J.M. Leng, S.Li, J.L. Opsal, B.H. Lee, and J.C. Lee, "Interface between c-Si and the High-k dielectric HfO2: Characterization by rotating compensator spectroscopic ellipsometry (RCSE)", Proceedings of the First International Conference on Microelectronics and Interfaces, 2000.

120. Renee Nieh, Wen-Jie Qi, Byoung Hun Lee, Laegu kang, Yongjoo Jeon, Katsunori Onishi, and Jack C. Lee, "Processing effect and electrical characteristics of ZrO2 formed by RTP oxidation of Zr", ECS spring meeting, Ontario, 2000.

121. J. Lee, "ZrO_2 and HfO_2 Gate Dielectrics," an Invited Talk at PASSS Symposium, Portland OR August 18, 2000.

122. J. Lee, "Ultra-thin High-K Gate Dielectrics," an Invited Talk at IBM Yorktown Research Center Seminar Series, NY September 28, 2000.

123. J. Lee, “Reliability Issues of ZrO2 and HfO2 for Gate Dielectrics Applications,” an Invited Talk at the SRC Topic Research Conference, Stanford CA October 30-Nov. 1, 2000.

124. Laegu Kang, Katsunori Onishi, Yongjoo Jeon, Byoung Hun Lee, Changseok Kang, Wen-Jie Qi, Renee Nieh, Sundar Gopalan, Rino Choi, and Jack C. Lee, “MOSFET Devices with Polysilicon on Single-Layer HfO_2 High-K Dielectrics,” International Electron Devices Meeting, IEDM Technical Digest, p. 35, 2000.

125. Byoung Hun Lee,Rino Choi, Laegu Kang, Sundar Gopalan, Renee Nieh, Katsunori Onishi, Yongjoo Jeon, Wen-Jie Qi, Changseok Kang, and Jack C Lee, "Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8-12Å)", International Electron Devices Meeting, IEDM Technical Digest, p. 39, 2000.

126. J. Lee, “Scaling of Gate Dielectrics and the Impact of High-K Dielectrics,” an Invited Talk at The ULIS'2001 Workshop (2nd European Workshop on Ultimate Integration of Silicon) Grenoble, France January 18-19, 2001.

127. J. Lee, “High-Dielectric Gate Dielectrics” an Invited Talk at the 6th Workshop on Formation, Characterization and Reliability of Ultrathin Silicon Oxide, held at Atagawa, Sizuoka, Japan, p. 55, January 26-27, 2001.

128. J. Lee, “Alternative Gate Dielectrics for Future CMOS Devices” an Invited Talk at the Cypress Semiconductor Workshop, San Jose, CA March 7, 2001.

129. J. Lee, “Future Gate Dielectrics Materials” an Invited Talk in the "Rapid Thermal and Other Short-Time Processing Technologies” Session at the 199th Electrochemical Society (ECS) Meeting, Washington D.C., March 25-30, 2001.

130. J. Lee, “High-K Gate Dielectric Devices” (keynote speaker) 2001 Symposium on Nano Device Technology, Hsinchu, Taiwan, April 23-25, 2001.

131. R. Choi, C. Kang, B. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J. Lee, “High-Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation,” Tech. Dig. of Symposium on VLSI Technology (Highlight Session), p. 15, June 2001.

132. K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Gopalan, Y. Jeon, C. Kang, B. Lee, R. Nieh, and J. Lee, “Dopant Penetration Effects on Polysilicon Gate HfO_2 MOSFETs,” Tech. Dig. of Symposium on VLSI Technology, p. 131, June 2001.

133. T. Ngai, K. Onishi, R. Choi, C. Kang, J. Fretwell, X. Chen, J. Chen, J. Lee and S. Banerjee, “Electrical Properties of HfO_2 Gate Dielectric on SiGe,” Electronic Materials Conference, June 2001.

134. J. Lee, "High-K Gate Dielectrics: ZrO_2 and HfO_2" an Invited Talk presented at the Distinguished Lectures Series of the Electron Devices Society, Kansai Chapter, Kyoto, Japan, June 15, 2001.

135. Easwar Dharmarajan, Wen-Jie Qi, Renee Nieh, Laegu Kang, Katsunori Onishi, and Jack C. Lee, "Ultra-Thin Zirconium Silicate Films With Good Physical and Electrical Properties for Gate Dielectric Applications," MRS fall meeting 2000.

136. Renee Nieh, Katsunori Onishi, Rino Choi, Hag-Ju Cho, Chang Seok Kang, Sundar Gopalan, Siddarth Krishna, and Jack C. Lee, "Performance Effects of Two Nitrogen Incorporation Techniques on TaN/HfO_2 and poly/HfO_2 MOSCAP and MOSFET Devices" 1st International Workshop on Gate Insulator (IWGI) Tokyo, p. 70, Japan, November 1-2, 2001.

137. S. Gopalan, E. Dharmarajan, K. Onishi, R. Nieh, C. S. Kang, R. Choi, H-J. Cho and J. C. Lee, "Ultra-thin Hafnium Silicate films with TaN and Polysilicon gates for gate dielectric application", IEEE Semiconductor Interface Specialist Conference (SISC) Proceedings, p. 11, November 2001.

138. H. Cho, C. Kang, K. Onishi, S. Gopalan, R. Nieh, E. Dharmarajan, and J. Lee, "Novel Nitrogen Profile Engineering for Improved TaN/ HfO_2/Si MOSFET Performance" International Electron Devices Meeting (IEDM Technical Digest), p. 655, 2001.

139. K. Onishi, C. Kang, R. Choi, H. Cho, S. Gopalan, R. Nieh, E. Dharmarajan, and J. Lee, "Reliability Characteristics, including NBTI, of Polysilicon Gate MOSFET's," International Electron Devices Meeting (IEDM Technical Digest), p. 659, 2001.

140. J. Lee, "High-K Gate Dielectrics (HfO_2 and ZrO_2), Semicon Korea Technical Program Digest, p. 155, February 2002.

141. C.M. Osburn, S.K. Han, I. Kim, S. Campbell, E. Garfunkel, T. Gustafson, J. Hauser, T.-J. King, A. Kingon, D.-L. Kwong, S.J. Lee, C.H. Lee, J. Lee, C.S. Kang, K. Onishi, R. Choi, G. Lucovsky, J.G. Hong, T.P. Ma, W. Zhu, Z. Luo, J.P. Maria, D. Wicaksana, V. Misra, J.J. Lee, Y.S. Suh, G. Parsons, D. Niu, and S. Stemmer, "Integration Issues with High k Gate Stacks" an invited to VLSI Symposium of The Electrochemical Society Meeting, Spring 2002.

142. C. Kang, H. Cho, K. Onishi, R. Choi, R. Nieh, S. Gopalan, S. Krishnan, and J. Lee, "Improved Thermal Stability and Device Perfromance of Ultra-thin (EOT < 10 Å) Gate Dielectric MOSFET's by Using Hafnium Oxynitride (HfO_xN_y)," 2002 Symposium on VLSI Technology, p. 146, June 2002.

142. R. Nieh, S. Krishnan, H. Cho, C. Kang, S. Gopalan, K. Onishi, R. Choi, and J. Lee, "Comparison between ultra-thin ZrO_2 and ZrO_xN_y gate dielectrics in TaN or poly-gated NMOSCAP and NMOSFET devices," 2002 Symposium on VLSI Technology, p. 186, June 2002.

143. K. Onishi, C. Kang, R. Choi, H. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J. Lee, "Effects of High-Temperature Forming Gas Anneal on HfO_2 MOSFET Performance," The 2002 Symposium on VLSI Technology, p. 22, June 2002.

144. Q. Lu, H. Takeuchi, X. Meng, T. King, C. Hu, K. Onihi, H. Cho, and J. Lee, "Improved Performance of Ultra-thin HfO_2 CMOSFETs Using Poly-SiGe Gate," 2002 Symposium on VLSI Technology, p. 86, June 2002.

145. K. Onishi, C. Kang, R. Choi, H. Cho, S. Gopalan, R. Nieh, S. Krishnan and J. Lee, "Charging Effects on Reliability of HfO_2 Devices with Polysilicon Gate Electrode," Proceeding of International Reliability Physics Symposium, pp. 419-420, 2002.

146. Q. Lu, H. Takeuchi, R. Lin, T. King, C. Hu, K. Onishi, R. Choi, C. Kang and J. Lee, "Hot Carrier Reliability of n-MOSFET with Ultra-thin HfO_2 Gate Dielectric and Poly-Si Gate," 2002 International Reliability Physics Symposium Proceedings, p429 (2002).

147. R. Choi, K. Onishi, C. S. Kang, R. Nieh, S. Gopalan, H.-J. Cho, S. Krishnan, and J. C. Lee, "High Quality MOSFETs Fabrication with HfO_2 Gate Dielectric and TaN Gate Electrode", 60th Device Research Conference at the University of California, Santa Barbara, June 24-26, 2002, p. 193.

148. S. Gopalan, R. Choi, K. Onishi, R. Nieh, C. Kang, H. Cho, S. Krishnan, and J. Lee, "Impact of NH_3 Pre-treatment on the Electrical and Reliability Characteristics of Ultra-thin Hafnium Silicate Films Prepared by Re-oxidation Method," 60th Device Research Conference at the University of California, Santa Barbara, June 24-26, 2002, p. 195.

149. K. Onishi, R. Choi, C. Kang, H. Cho, Y. Kim, R. Nieh, J. Han, S. Krishnan, A. Shahriar and J. Lee, "Charge Trapping and Interfacial Degradation of Polysilicon Gate HfO_2 NMOSFET's," Gate Stack Engineering Working Group Symposium, October 16-18, 2002.

150. J. Lee, "Nitrogen Incorporation and High-Temperature Forming Gas Anneal for High-K Gate Dielectrics," an Invited Paper in 202nd Meeting of the Electrochemical Society, p. 171, October 20-25, 2002.

151. J. Lee, "Effects of Interface States and Charge Trapping on Performance of High-K Dielectric Devices," an Invited Paper in the 33rd IEEE Semiconductor Interface Specialists Conference, December 5-7, 2002.

152. C. Kang, H. Cho, K. Onishi, R. Choi, Y. Kim, R. Nieh, J. Han, S. Krishnan and J. Lee, "Nitrogen Concentration Effects and Performance Improvement of MOSFETs Using Thermally Stable HfO_xN_y Gate Dielectrics," International Electron Devices Meeting (IEDM), p. 865, December 2002.

153. Y. Kim, K. Onishi, C. Kang, R. Choi, H. Cho, R. Nieh, J. Han, S. Krishnan and J. Lee, "Hard and Soft-Breakdown Characteristics of Ultra-Thin HfO_2 Under Dynamic and Constant Voltage Stress," International Electron Devices Meeting (IEDM), p. 629, December 2002.

155. R. Choi, K. Onishi, C. Kang, S. Gopalan, R. Nieh, Y. Kim, J. Han, S. Krishnan, H. Cho, A. Shahriar, and J. Lee ""Fabrication of High Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs Using Deuterium Anneal," International Electron Devices Meeting (IEDM), p. 613, December 2002.

156. Y. H. Kim, K. Onishi, C. S. Kang, R. Choi, H. -J. Cho, S. Krishnan, M. Akbar, and J. C. Lee, "Dynamic Reliability Characteristics of Ultra-Thin HfO_2," Highlight Session of 2003 International Reliability Physics Symposium, p. 46, March 2003.

157. H. Cho, C. Kang, M. Akbar, K. Onishi, Y. Kim, R. Choi, and J. Lee, "Application of Top HfSiON Layer for Improved Poly-Gated HfO_2 PMOSFET Performance," the 61st Device Research Conference (section II.B), p. 37, June 23-25, 2003.

158. Y. H. Kim, K. Onishi, C. S. Kang, R. Choi, H. -J. Cho, M. S. Akbar, and J. C. Lee, "Polarity Dependence of the Reliability Characteristics of HfO_2 with Poly-Si Gate Electrode", the 61st Device Research Conference proceeding (DRC), p.57, 2003.

159. Y. H. Kim, K. Onishi, C. S. Kang, R. Choi, H. -J. Cho, and J. C. Lee, "The Effects of Forming Gas Anneal Temperature and Dielectrics Leakage Current on TDDB Properties of HfO_2 Devices" Electrochemical Society Proceeding (ECS), October 2003.

160. H.-J. Cho, C.Y. Kang, C.S. Kang, Y.H. Kim, R. Choi, A. Shahriar, C.H. Choi, S.J. Rhee and J. C. Lee, "Effects of NH_3 Annealing on High-k HfSiON/HfO_2 Gate Stack Dielectrics," Electrochemical Society Proceeding (ECS), October 2003.

161. C.S. Kang, H.-J. Cho, Y.H. Kim, R. Choi, A. Shahriar, C.Y. Kang, C.H. Choi, S.J. Rhee and J. C. Lee, "Characterization of resistivity and work function of sputtered-TaN film for gate electrode applications," Electrochemical Society Proceeding (ECS), October 2003.

162. Jack C. Lee, "Hf-based Dielectrics and Reliability" Invited Paper presented at the SRC Topical Research Conference, October 2003.

163. J. Lee, "Hf-based High-K Dielectrics" Invited Paper presented at the International Workshop on Gate Insulator, Tokyo, Japan, Nov. 2003.

164. Y. H. Kim, R. Choi, R. Jha, J.H. Lee, V. Misra and J. C. Lee, "Interface Tunneling Mechanism of HfO_2 /Dual Metal Gate Stack with Varying Interface Layer Thickness and Different Bias Polarities", 34th IEEE Semiconductor Interface Specialists Conference, p. 45, December 2003.

165. J. Lee, “High-K Dielectrics and MOSFET Characteristics”, Invited Paper at IEEE International Electron Devices Meeting, Section 4, no. 4, p. 95, December 2003.

166. H. Cho and J. Lee, “The Effects of Nitrogen in HfO_2 for Improved MOSFET Performance” presented at the 2003 International Semiconductor Device Research Symposium, Washington D.C. December 2003.

167. C.M. Osburn, S.A. Campbell, E. Eisenbraun, E. Garfunkel, T. Gustafson, A. Kingon, D.-L. Kwong, J. Lee, G. Lucovsky, T.P. Ma, J.P. Maria, V. Misra, G. Parsons, D. Schlom, and S. Stemmer, “Materials and Processes for High k Gate Stack”, International Forum on Semiconductor Technology, Paris, February 2004.

168. Y. H. Kim, R. Choi, R. Jha, J.H. Lee, V. Misra and J. C. Lee. “Effects of Gate Electrodes and Barrier Heights on the Breakdown Characteristics and Weibull Slopes of HfO_2 MOS Devices” 2004 International Reliability Physics Symposium, p. 595, 2004.

169. C. Y. Kang, H. -J. Cho, C. S. Kang, R. Choi, Y. H. Kim, S. J. Rhee, C. H. Choi, A. Shahriar and J. C. Lee, “Effects of Thin SiN Interface Layer on Transient I-V Characteristics and Stress Induced Degradation of High-k Dielectrics,” 2004 International Reliability Physics Symposium, p. 587, 2004.

170. Se Jong Rhee, Young Hee Kim, Chang Yong Kang, Chang Seok Kang, Hag-Ju Cho, Rino Choi, Chang Hwan Choi, Mohammad S. Akbar, and Jack C. Lee, "Dynamic Positive Bias Temperature Instability Characteristics of Ultra-Thin HfO_2 NMOSFET," 2004 International Reliability Physics Symposium, p. 269, 2004.

171. C. S. Kang, C. Choi, C. Y. Kang, S. J. Rhee, Y. H. Kim, S. Akbar, J. Lee, “Advantage and Concerns of Si and N Incorporation”, Sematech Gate Stack Workshop Digest, Sect. 1, p. 1, March 2004.

172. R. Choi, B. Lee, G. Brown, P. Zeitzoff, J. H. Sim, and J. C. Lee, “Polarity Dependence of Dielectrics Wearout Properties for Hf-based High-K Dielectrics,” Sematech Gate Stack Workshop Digest, Sect. 1, p. 4, March 2004.

173. C. Choi, C.S. Kang, C. Y. Kang, R. Choi, Y. Kim, S. J. Rhee, M. Akbar and J. Lee, “The Effects of Nitrogen and Silicon Profile on High-K MOSFET Performance and Bias Temperature Instability,” 2004 Symposium on VLSI Technology, p. 214, June 2004.

174. Y. Kim, R. Choi, R. Jha, J. H. Lee, V. Misra and J. Lee, “Effects of Barrier Height and the Nature of Bi-Layer Structure on the Reliability of High-K Dielectrics with Dual Metal Gate (Ru & Ru-Ta alloy) Technology,” 2004 Symposium on VLSI Technology, p. 138, June 2004.

175. Rino Choi, B. H. Lee, G. Brown, P. Zeitzoff, J. H. Sim, and J. C.Lee, "Polarity dependence of FN Stress induced degradation on NMOSFETs with Polysilicon Gate and HfSiON Gate Dielectrics," to be presented at the 11th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2004), p. 21, 2004.

176. Rino Choi, Byoung Hun Lee, K. Matthews, J. H. Sim, G. Bersuker, L. Larson and Jack C. Lee, "Relaxation of FN stress induced Vth shift at NMOSFETs with HfSiON Gate Dielectric and TiN Gate Electrode," 62nd annual Device Research Conference (2004 DRC), p. 14, 2004.

177. Se Jong Rhee, Chang Yong Kang, Young Hee Kim, Chang Seok Kang, Hag-Ju Cho, Rino Choi, Chang Hwan Choi, Mohammad S. Akbar, and Jack C. Lee, "Threshold Voltage Instability of Ultra-Thin HfO_2 NMOSFETs : Characteristics of Polarity Dependences," 62nd annual Device Research Conference (2004 DRC), p. 101, 2004.

178. Y. H. Kim, R. Choi, R. Jha, J.H. Lee, V. Misra, and J. C. Lee, "Reliability of High-K Dielectrics and Its Dependence on Gate Electrode and Interfacial / High-K Bi-Layer Structure" to be published at the 15th European Symposium on Reliability of Electronic Devices, Failure Physics and Analysis, October 2004.

179. C. Y. Kang, R. Choi, J. H. Sim, C. Young, B. H. Lee, G. Bersuker, and Jack C. Lee, "Charge Trapping Effects in HfSiON Dielectrics on the Ring Oscillator Circuit and the Single Stage Inverter Operation," Technical Digest of International Electron Devices Meeting (IEDM), p. 485, December 2004.

180. Se Jong Rhee, Chang Seok Kang, Chang Hwan Choi, Chang Yong Kang, Siddarth Krishnan, Manhong Zhang, Mohammad S. Akbar and Jack C. Lee, "Improved Electrical and Material Characteristics of Hafnium Titanate Multi-metal Oxide n-MOSFETs with Ultra-Thin-EOT (~8Å) Gate Dielectric Application" Technical Digest of International Electron Devices Meeting (IEDM), p. 837, December 2004.

181. Se Jong Rhee, Chang Seok Kang, Chang Yong Kang, Chang Hwan Choi, Manhong Zhang, Siddarth Krishnan, Mohammad S. Akbar and Jack C. Lee "Charge Compensation Effect in Hafnium Titanate Multi-metal Oxide n-MOSFETs," IEEE Semiconductor Interface Specialists Conference, p. 50-51, 2004.

182. C. Choi, C. Y. Kang, S. Rhee, M. Akbar, S. Krishnan, M. Zhang and J. Lee, "A Suppression of Interfacial Oxide Formation by Oxygen-Scavenging Technique to Reduce EOT to < 0.7nm of "Undoped" HfO_2 / Si Gate Stacks" IEEE Semiconductor Interface Specialists Conference, 2004.

183. C. Y. Kang, R. Choi, B. H. Lee, G. Bersuker, and Jack C. Lee, "A Study of Charge Trapping Dynamics in HfSiON Dielectrics Using the Single Stage Inverter Circuit" IEEE Semiconductor Interface Specialists Conference, December 2004.

184. Invited Paper -Jack C. Lee , *C.* Kang, S. Rhee, C. Choi, S. Krishnan, I. Ok, M. Akbar, H. Kim, F. Zhu, M. Zhang, T. Lee, "Hafnium-based High-K Dielectrics" VLSI Technology (VLSI-TSA-Tech), 2005 IEEE VLSI-TSA International Symposium on Page(s):122 – 125, April 2005.

185. Invited Paper - Jack C. Lee, S. Rhee, C. Kang, C. Choi, S. Krishnan, I. Ok, M. Akbar, H. Kim, F. Zhu, M. Zhang, T. Lee, "Process Effects and Characterization of Hf-Based Dielectrics, "Electrochemical Society 207th meeting, May 2005.

186. M. S. Akbar, Naim Moumen, Joel Barnett, Byoung-Hun Lee, and Jack C. Lee, "Effects of High-k Post Deposition Cleaning in Improving CMOS Bias Instabilities and Mobility. A Potential Issue in Reliability of Dual Metal Gate Technology", IEEE International Reliability Physics Symposium, pp. 640, 2005.

187. C. Y. Kang, S. J. Rhee, C. H. Choi, M. S. Akbar, H. -S. Kim, M. Zhang, T. Lee, I. Ok, F. Zhu, and J. C. Lee, "Effects of Optimized Nitrogen Tailoring in High-k dielectrics on Impurity Penetration and Stress Induced Device Degradation", IEEE International Reliability Physics Symposium, p. 628, 2005.

188. Siddarth Krishnan, Jeff J. Peterson, Chadwin D. Young, George Brown, Rino Choi, Rusty Harris, Jang Hoan Sim, Peter Zeitzoff, Paul Kirsch, Jim Gutt, Hong Jyh Li, Ken Matthews, Jack C. Lee, Byoung Hun Lee, and Gennadi Bersuker "Dominant SILC mechanisms in HfO_2/TiN Gate nMOS and pMOS transistors", and, Proceedings of 43rd Annual IEEE International Reliability Physics Symposium, Page(s): 642 – 643, 2005.

189. Changhwan Choi, Chang Yong Kang, Se Jong Rhee, Mohammad Shahariar Abkar, Siddarth A. Krishna, Manhong Zhang, Hyungseob Kim, Tackhwi Lee, Feng Zhu, Injo Ok, Sergei Koveshnikov and Jack C. Lee, "Fabrication of TaN-gated Ultra-Thin MOSFETs (EOT <1.0nm) with HfO2 using a Novel Oxygen Scavenging Process for Sub 65nm Application" Symposium on VLSI Technology, Kyoto, Japan, p. 226, 2005.

190. J. Lee, "High-K Dielectrics – processes and reliability," IEEE Solid-State Circuits Society Fort Collins, Aug. 5, 2005.

191. M. S. Akbar, Naim Moumen, Jeff Peterson, Joel Barnett, Muhammad Hussain and Jack C Lee, "Effect of Precursor Pulse Time on Charge Trapping and Mobility of ALD HfO_2", 207th Electrochemical Society (ECS) Meeting, pp. 161, 2005.

192. Se Jong Rhee, Hyoung-Sub Kim, Chang Yong Kang, Chang Hwan Choi, Manhong Zhang, Feng Zhu, Tackhwi Lee, Injo Ok, Mohammad S. Akbar, Siddarth A. Krishnan, and Jack C. Lee, "Optimization and Reliability Characteristics of TiO_2/HfO_2 Multi-metal Dielectric MOSFETs" Symposium on VLSI Technology, Kyoto, Japan, p. 168, 2005.

193. Se Jong Rhee, Hyoung-Sub Kim, Chang Yong Kang, Chang Hwan Choi, M. S. Akbar, Manhong Zhang, Tackwhi Lee, Injo Ok, Feng Zhu, Siddarth A. Krishnan, and Jack C. Lee, "Structural Optimization and Electrical Characteristics of Ultra-thin Gadolinium (Gd_2O_3) Incorporated HfO_2 n-MOSFETs," 63rd annual Device Research Conference (2005 DRC), p. 219, 2005.

194. Siddarth A. Krishnan, M.A. Quevedo-Lopez, Rino Choi, Paul Kirsch, Chadwin Young, Rusty Harris, Jeff J. Peterson, Hong-Jyh Li, Byoung Hun Lee and Jack C. Lee "Charge Trapping Dependence on the Physical Structure of Ultra-thin ALD-HfSiON/TiN Gate Stacks", International Integrated Reliability Workshop (IIRW) proceedings, p. 89, October 2005.

195. Siddarth A. Krishnan, Manuel Quevedo, Rusty Harris, Paul D. Kirsch, Rino Choi, Byoung Hun Lee, Gennadi Bersuker, Jeff Peterson, Hong-Jyh Li, Chadwin Young and Jack C. Lee, "NBTI Dependence on Dielectric Thickness in Ultra-scaled HfSiO Dielectric/ALD-TiN Gate Stacks", Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, p. 23, 2005.

196. J. Lee, "Future of High-K Dielectrics" (Invited Talk) Electron Device Society Mini-Colloquium at UCF, p. 31, February 23-25, 2006.

197. Chang Yong Kang, Jack Lee, "Carrier Recombination in High-k Dielectrics and its Impact on Transient Charge Effects in High-k Devices", Advanced Gate Stack Engineering Working Group Biannual Meeting, March 2006.

198. Feng Zhu, C.Y Kang, S.J. Rhee, C.H. Choi, S.A. Krishnan, M. Zhang, H.S. Kim, T. Lee, I. Ok, G. Thareja, and J.C. Lee, "Improving carrier mobility and reliability characteristics of high-k NMOSFET by using stacked Y2O3/HfO2 gate dielectric", Proceedings of IEEE International Reliability Physics Symposium, p659, 2006.

199. C. Y. Kang, R. Choi, S. C. Song, C. D. Young, G. Bersuker, B. H. Lee, and J. C. Lee, "Carrier Recombination in High-k Dielectrics and its Impact on Transient Charge Effects in High-k Devices", Proceedings of IEEE International Reliability Physics Symposium, p. 657, 2006.

200. J. Lee, (Invited Talk) "High-K Gate Dielectrics," Symposium on VLSI Technology Short Course Series, Honolulu, HI, June 12-15, 2006.

201. InJo Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, G. Thareja, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee "Depletion-Mode MOSFET on n-GaAs substrate with HfO2 and Silicon Interface Passivation", IEEE Device Research Conference, pp. 45-46, 2006.

202. Feng Zhu, S. Koveshnikov, I. Ok, H.S. Kim,V. Tokranov, M. Yakimov, S. Oktyabrsky, W. Tsai and J. C. Lee, "Enhancement and Depletion-mode GaAs N-MOSFETs with

stacked HfO2/Y2O3 gate dielectric", Digest of Device Research Conference, p. 83, 2006.

203. H.S. Kim, I. Ok, M. Zhang, T. Lee, F. Zhu, G. Tharaja, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, "Germanium passivation for high-k dielectric III-V MOSFETs and temperature dependence of dielectric leakage current," IEEE Device Research Conference, p. 87, 2006.

204. Tackhwi Lee; Se Jong Rhee; Chang Yong Kang; Feng Zhu; Manhong Zhang; Hyoung-sub Kim; Changhwan Choi; Injo Ok; Sergei Koveshnikov; Hokyung Park; Lee, J.C., "Improved MOSFET characteristics by Incorporating Laminated Dysprosium (Dy2O3) Dielectric into HfO2 Gate Stack," IEEE Device Research Conference, Page(s): 69 – 70, June 2006.

205. H. Park, H. C. Wen, M. Chang, M. Jo, R. Choi, B. H. Lee, S.C. Song, C. Y. Kang, T. Lee, G. Brown, J. C. Lee and H. Hwang, "Thermal stability of metal electrodes and its impact on gate dielectric characteristics," Solid State Devices Meeting, 2006.

206. Keynote Speech – Jack C. Lee, "MOS and MOSFET Structures on III-V Substrate with Interface Passivation Layer", 3rd Annual International Symposium on Advanced Gate Stack Technology, September 2006.

207. Invited Paper - C.M. Osburn, S.A. Campbell, A. Demkov, E. Eisenbraun, E. Garfunkel, T. Gustafsson, A.I. Kingon, J. Lee, D.J. Lichtenwalner, G. Lucovsky, T.P. Ma, J.P. Maria, V. Misra, R.J. Nemanich, G.N. Parsons, D.G. Schlom, S. Stemmer, R.M. Wallace, and J. Whitten, "Materials and Processes for High k Gate Stacks: Results from the FEP Transition Center,", Electrochemical Society Transactions, 3(3), 389, October 2006.

208. Michael M. Oye, Davood Shahrjerdi, Jeffrey B. Hurst, Shannon D. Lewis, Sagnik Dey, David Q. Kelly, Sachin Joshi, Injo Ok, Terry J. Mattord, Jack C. Lee, Archie L. Holmes Jr., and Sanjay K. Banerjee, "Molecular-beam Epitaxy Growth of Ge and GaAs on Silicon substrates for High-k III-V MOSFET applications," the 24th North American Conference on Molecular Beam Epitaxy, October 2006.

209. G. Thareja, J. Lee, A. V. Y. Thean, V. Vartanian, B. Y. Nguyen, "NBTI Reliability of Strained SOI MOSFETs," 32nd International Symposium for Testing and Failure Analysis, November 2006.

210. InJo Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee "Self-Aligned n- and p-channel GaAs MOSFETs on Undoped and P-type Substrates Using HfO_2 and Silicon Interface Passivation Layer", IEEE International Electron Devices Meeting, p. 829, 2006.

211. InJo Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, and Jack C. Lee "Metal Gate HfO2 MOS Structures on GaAs Substrate with SiGe Interface Passivation Layer", IEEE Semiconductor Interface Specialists Conference, 2006.

212. Feng Zhu, S. Koveshnikov, I. Ok, H.S. Kim, M. Zhang, V. Tokranov, M. Yakimov, S. Oktyabrsky, W. Tsai and J. C. Lee, "Investigation of charge trapping properties of high-κ on GaAs with silicon interface passivation layer", IEEE Semiconductor Interface Specialists Conference 2006.

213. M. H. Zhang, F. Zhu , I. J.Ok , H. S. Kim, L.Yu, M. Oye, J.Hurst, B. Cobb, S. Lewis, A. Holmes and Jack C. Lee, "Criticality of controlling oxygen incorporation into HfO_2/Si/GaAs gate stacks" IEEE Semiconductor Interface Specialists Conference 2006.

214. H.-S. Kim, I. Ok, M. Zhang, F. Zhu, L. Yu, T. Lee, and Jack C. Lee, "The Effects of Germanium Interfacial Passivation Layer Thickness on Electrical Characteristics of HfO_2 MOSCAP on GaAs Substrate" IEEE Semiconductor Interface Specialists Conference, p. 28, 2006.

215. H. J. Na, C. Krug, S. Joshi, D. Heh, R. D. Kirsh, R. Choi, B. H. Lee, R. Jammy, S. Banerjee, and J. Lee, "Improved Passivation and Characterization of Ge/HfSiO Interface Enabling Surface Channel Ge pFETs," IEEE Semiconductor Interface Specialists Conference, session 8, no. 3, 2006.

216. Invited Paper -- Jack C. Lee, "III-V Channel High-K MOSFETs" Technical Digest of SEMI Technology Symposium (STS) Korea, p. 285, January 31, 2007.

217. S. Joshi, C. Krug, D. Heh, H. Na, H. Harris, J. Oh, P. Kirsch, P. Majhi, B. Lee, H. Tseng, R. Jammy, J. Kee and S. Banerjee, "Improved Ge Surface Passivation with Ultrathin SiOx Enabling High Mobility Surface Channel PMOSFETs Featuring a HfSiO/WN Gate Stack," 37th Conference on the Physics and Chemistry of Semiconductor Interfaces, February 2007.

218. S. Koveshnikov, S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Moore, W. Tsai, F. Zhu, J.C. Lee, "Metal-Oxide-Semiconductor Field Effect Transistors with InGaAs and GaAs/InGaAs Channels and High-k Gate Dielectric," Materials Research Society Symposium, San Francisco, April 2007.

219. J. Lee (Invited talk) "MOSCAP's and MOSFET's on III-V Channel Materials with Si, Ge and SiGe Interface Passivation Layer", Electrochemical Society Meeting, May 7, 2007.

220. J. Lee (Invited Talk) " III-V Channel Materials with Si, Ge and SiGe Interface Passivation Layer", Ohio State University Distinguished Lecture Series, May 24, 2007.

221. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee "Metal Gate – HfO_2 MOS Structures on InGaAs Substrate with Varying Si Interface Passivation Layers and PDA Conditions", Conference on the Physics and Chemistry of Semiconductor Interfaces, 2007

222. Feng Zhu, Injo Ok, Hyoung-sub Kim, Manhong Zhang, Sung Il Park, Jung Hwan Yum and Jack C. Lee, "Investigation of the passivation mechanism of ultra-thin silicon interface layer for III-V MOS devices," Conference on the Physics and Chemistry of Semiconductor Interfaces (PCSI) (2007).

223. S. Oktyabrsky, S. Koveshnikov, V. Tokranov, M. Yakimov, R. Kambhampati, H. Bakhru, F. Zhu, J. Lee, and W. Tsai, "InGaAs and GaAs/InGaAs Channel Enhancement Mode n-MOSFETs With HfO2 Gate Oxide and a-Si Interface Passivation Layer," Device Research Conference, June 19, 2007.

224. Hyoung-Sub Kim, Injo Ok, Feng Zhu, M. Zhang, S. Park, J. Yum, H. Zhao, and Jack C. Lee, "n- and p-channel TaN/HfO_2 MOSFETs on GaAs substrate using a germanium interfacial passivation layer," *The 65th annual Device Research Conf.*, pp. 99, 2007.

225. Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, "HfO_2-based Metal-Oxide-Semiconductor Capacitors on n-InGaAs Substrate with a Thin Germanium Passivation Layer," *The International Conference on Compound Semiconductor Manufacturing Technology*, pp. 69, 2007.

226. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee "Hydrogen Incorporation of Metal Gate HfO_2 MOS Structures on $In_{0.2}Ga_{0.8}As$ Substrate with Si Interface Passivation Layer", International Conference on Compound Semiconductor Manufacturing Technology, 2007.

227. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and Jack C. Lee, "Metal Gate HfO2 MOS Structures on InGaAs Substrate with Varying Si Interface Passivation Layer and PDA Condition," J. Vac. Sci. Technol. B 25, Jul/Aug 2007.

228. Injo Ok, Hyung-sub Kim, Manhong Zhang, Feng Zhu, Sung-il Park, Junghwan Yum, Han Zhao and Jack C. Lee, "Post Metal Annealing Optimization of Self-Aligned n-channel GaAs MOSFETs Using HfO2 and Silicon Interface Passivation Layer," International Symposium on Advanced Gate Stack Technology, September 2007.

229. InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Domingo Garcia, Prashant Majhi, and Jack C. Lee, "Influence of the substrate orientation on the electrical and material properties of GaAs MOSFETs Using HfO2 and Silicon Interface

Passivation Layer," Semiconductor Interface Specialists Conference (SISC), December 2007.

230. Manhong Zhang, I. Ok, H. Kim, F. Zhu, and J. Lee, "Mechanism of V_{fb} shift in SiO2 and Hf-based gate dielectric stacks by capping Gd2O3," Semiconductor Interface Specialists Conference (SISC), December 2007.

231. Tackhwi Lee, Jack C. Lee and Sanjay K. Banerjee, "Characterization of Dysprosium oxide (Dy_2O_3) incorporated HfO_2 gate oxide devices" Semiconductor Interface Specialists Conference (SISC), December 2007.

232. InJo Ok, H. Kim, M. Zhang, F. Zhu, H. Zhao, S. Park, J. Yum, Domingo Garcia, Prashant Majhi, N. Goel and W. Tsai, C.K. Gaspe, M.B. Santos, and Jack C. Lee, "Self-Aligned n-channel MOSFET on InP and In0.53Ga0.47As Using Physical Vapor Deposition HfO2 and Silicon Interface Passivation Layer." IEEE Device Research Conference, June 2008.

233. Manhong Zhang, Feng Zhu, In-Jo Ok, Hyoung- Kim, Han Zhao, Jack C. Lee "Mechanism of flatband voltage shift capping Me_2O_3 (Me=Gd, Y, Dy)", IEEE Device Research Conference June 2008.

234. Feng Zhu, Injo Ok, Hyoung-sub Kim, Manhong Zhang, Sung Il Park, Jung Hwan Yum, Han Zhao and Jack C. Lee, "Can GaAs MOS device match with its silicon counterpart in interface quality by using silicon interface passivation layer and HfO_2 gate oxide?" Electronic Materials Conference (EMC) (2008).

235. Jack Lee (Invited Paper), "$In_{0.53}Ga_{0.47}As$ n-MOSFETs with Si interface passivation layer and HfO_2 gate oxide" 5th International Symposium on Advanced Gate Stack Technology, Sep. 2008.

236. Feng Zhu, H. Zhao, I. Ok, H.S. Kim, M. Zhang, S. Park, J. Yum, S. Koveshnikov, V. Tokranov, M. Yakimov, S. Oktyabrsky, W. Tsai and Jack C. Lee, "Charge trapping and wearout characteristics of self-aligned enhancement-mode GaAs n-MOSFET with Si interface passivation layer and HfO_2 gate oxide", Compound Semiconductor IC Symposium (CSICS) 2008.

237. Feng Zhu, Han Zhao, H.S. Kim, I. Ok, J. Yum and Jack C. Lee, "The effects of silicon interface passivation layer thickness on device characteristics of InP enhancement-mode nMOSFETs with HfO_2 gate oxide", IEEE SISC Semiconductor Interface Specialists Conference 2008

238. Feng Zhu, Han Zhao, H.S. Kim, I. Ok, J. Yum and Jack C. Lee, "A high performance enhancement-mode $In_{0.53}Ga_{0.47}As$ nMOSFET with directly sputtered HfO_2 gate oxide", IEEE SISC Semiconductor Interface Specialists Conference 2008

239. H. Zhao, D. Shahrjerdi, F. Zhu, H.S. Kim, J. Yum, S. Banerjee and J. C. Lee "Atomic-layer-deposited Al_2O_3 gate dielectrics on InP using sulfur passivation", 50th Electronic Materials Conference, (2008)

240. H. Zhao, D. Shahrjerdi, F. Zhu, H.S. Kim, J. Yum, S. Banerjee and J. C. Lee "ALD Al_2O_3 based MOSFETs on undoped and p-type $In_{0.53}Ga_{0.47}As$ substrates", 39th IEEE Semiconductor Interface Specialists Conference, (2008)

241. H. Zhao, Y. Chen, J. Yum, Y. Wang, N. Goel, S. Koveshnikov, W. Tsai, and J. C. Lee, "HfO_2-Based $In_{0.53}Ga_{0.47}As$ MOSFETs (EOT≈10Å) Using Various Interfacial Dielectric Layers", IEEE Device Research Conference, (2009)

242. Han Zhao, Jung Hwan Yum, Yen-Ting Chen, and Jack C Lee "$In_{0.53}Ga_{0.47}As$ n-MOSFETs with ALD Al_2O_3, HfO_2 and $LaAlO_3$ gate dielectrics", 36th Conference on the Physics and Chemistry of Semiconductor Interfaces, (2009)

243. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "$In_{0.53}Ga_{0.47}As$ MOSFETs with CF4 plasma treatment and Al_2O_3 gate oxide", International Symposium on Advanced Gate Stack Technology (ISAGST), August 2009

244. Yen-Ting Chen, Han Zhao, Jung Hwan Yum, Yanzhen Wang, and Jack C. Lee, "Atomic-layer-deposited HfO_2 gate dielectrics on InP using silicon interface passivation layer" Electronic Materials Conference (EMC) 2009

245. Han Zhao, Yen-Ting Chen, Jung Hwan Yum, and Jack C Lee "Channel Doping Concentration and Thickness Dependence of Device Performance for $In_{0.53}Ga_{0.47}As$ n-MOSFETs with ALD Al_2O_3 dielectrics", 2009 Materials Research Society Spring Meeting

246. Han Zhao, and Jack C Lee, "Self-aligned $In_{0.53}Ga_{0.47}As$ MOSFETs with Atomic Layer Deposited Al_2O_3, ZrO_2, and Stacked Al_2O_3/ZrO_2 Gate Dielectrics", 2009 International Conference on IC Design and Technology

247. J. Lee (Invited Paper) "High-K III-V MOSFETs" 1st International Symposium on Integrated Ferroelectrics and Functionalities ($ISIF^2$), in Colorado Springs, CO, September 27-30, 2009

248. J. Lee, H. Zhao, Y. Chen, J. Yum, F. Xue, F. Zhou and Y. Wang, (Invited Paper) "High Performance InGaAs MOSFETs with High Mobility using InP Barrier Layer" 216th Electrochemical Society Meeting (E10 - ULSI Process Integration) in Vienna, Austria, October 2009.

249. J. Huang, N. Goel, H. Zhao, C. Y. Kang, K.S. Min, G. Bersuker, S. Oktyabrsky, S. Koveshnikov, Jack C. Lee, P. Majhi, W. Tsai, P. D. Kirsch, H. H. Tseng and R. Jammy, "InGaAs MOSFET Performance and Reliability Improvement by Simultaneous

Reduction of Oxide and Interface Charge in ALD (La)AlO_x/ZrO_2 Gate Stack", IEEE International Electron Devices Meeting IEDM 13.5, 2009

250. K.S. Min, C.Y. Kang, C. Park, C.S. Park, B. J. Park, J. B. Park, M. M. Hussain, Jack C. Lee, B. H. Lee, P. Kirsch, H-H, Tseng, R. Jammy, and G. Y. Yeom, "A Novel Damage-Free High-k Etch Technique Using Neutral Beam Assisted Atomic Layer Etching (NBALE) for sub-32nm Technology Node Low Power Metal Gate/High-K Dielectric CMOSFETs" IEEE International Electron Devices Meeting IEDM 17.4, 2009.

251. Han Zhao, Ning Kong, Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, Sanjay K. Banerjee and Jack C. Lee, "Effects of InP barrier layer thicknesses and different ALD oxides on device performance of $In_{0.7}Ga_{0.3}As$ MOSFETs", IEEE Device Research Conference, (2010).

252. H. Zhao, N. Goel, J. Huang, Y. Chen, J. Yum, Y. Wang, F. Zhou, F. Xue, and J. Lee, "Factors Enhancing $In_{0.7}Ga_{0.3}As$ MOSFETs and Tunneling FETs Device performance" IEEE Device Research Conference, (2010).

253. (Invited Paper) Jack Lee, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Xue, Fei Zhou, "Investigation of III-V n-MOSFETs with ALD high-k gate oxides", 4th International Workshop on High-k dielectrics on High Carrier Mobility Channel Materials, (2010)

254. Y. Wang, H. Zhao, Y. Chen, F. Xue, F. Zhou, and J. Lee, "Atomic-Layer-Deposition HfO2Based InP n-Channel MOSFETs Using Different Thicknesses of Al2O3 as Interfacial Passivation Layer", Electrochemical Society (ECS) Transactions, Vol. 33, 487, Oct. 2010.

255. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou and Jack C. Lee, "Investigation of surface channel InGaAs MOSFETs with Al_2O_3 and ZrO_2 ALD Gate Dielectric", Electrochemical Society Transactions. 33(3), 487, (Oct. 2010)

256. [Best Student Paper Award] F. Xue, H. Zhao, Y. Chen, Y. Wang, F. Zhou and J. Lee, "InAs and $In_{0.7}Ga_{0.3}As$ buried channel MOSFETs with ALD gate dielectrics" 41th IEEE Semiconductor Interface Specialists Conference, (Dec. 2010)

257. F. Xue, H. Zhao, Y. Chen, Y. Wang, F. Zhou and J. Lee "Investigation of ALD Al_2O_3 and ZrO_2 Gate Dielectric InGaAs Surface Channel MOSFETs with Large EOT Range" 2010 Materials Research Society Fall Meeting, Nov. 2010.

258. (Invited paper) J. C. Lee, H. Zhao, Y. Chen, Y. Wang, F. Xue, and F. Zhou, "Buried-channel $In_{0.7}Ga_{0.3}As$ MOSFETs and vertical $In_{0.7}Ga_{0.3}As$ tunneling FETs for beyond CMOS applications," Electrochemical Society (ECS) Transactions, Vol. 33, Oct. 2010.

259. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "Improved Electrical Performance of Fluorinated HfO2 dielectrics on In0.53Ga0.47As MOSFETs" Materials Research Society (MRS) November 2010.

260. Y. Wang, Y. Chen, H. Zhao, F. Xue, F. Zhou, and J. Lee, "Improved Electrical Characteristics of ALD HfO2, Al2O3 Based n-Channel MOSFETs on InP Substrate with Postgate SF_6 Plasma Treatment ", IEEE Semiconductor Interface Specialists Conference, Dec. 2010.

261. (Invited Keynote Speaker) Jack C Lee, "High-K Dielectrics / High-Mobility Channel MOSFETs," SEMINATEC Workshop, Campinas, Brazil, March 24-25, 2011.

262. Yen-Ting Chen, Han Zhao, Yanzhen Wang, Fei Xue, Fei Zhou, and Jack C. Lee, "ZrO2-based InP MOSFETs (EOT = 1.2nm) Using Various Interfacial Dielectric Layers", the Electrochemical Society (ECS) the 219th meeting May 2011.

263. J. Huang, N. Goel, P. Lysaght, D. Veksler, P. Nagaiah[a], S. Oktyabrsky, , J. Price, H. Zhao, Y.T. Chen, J. C. Lee, J. C. Woicik, P. Majhi, P. D. Kirsch, and R. Jammy, "Detailed High-k/$In_{0.53}Ga_{0.47}As$ Interface Understanding to Enable Improved $In_{0.53}Ga_{0.47}As$ Gate Stack Quality" 2011 VLSI-TSA Symposium, June 2011.

264. Luca Morassi, Giovanni Verzellesi, Paolo Pavan, Dmitry Veksler, Injo Ok, Han Zhao, Jack C. Lee and Gennadi Bersuker, "Experimental/numerical investigation of buried-channel InGaA MOS-HEMTs with Al_2O_3 gate dielectric," IPRM 2011 --- 23th International Conference on Indium Phosphide and Related Materials, Berlin, Germany, May 2011.

265. L. Morassi, G. Verzellesi, P. Pavan, D. Veksler, I. Ok, H. Zhao, J.C. Lee, G. Bersuker, "Experimental/numerical investigation of buried-channel InGaAs MOS-HEMTs with Al_2O_3 gate dielectric", Proc. of the 23th International Conference on Indium Phosphide and Related Materials (IPRM 2011), Berlin (Germany), May 2011, pp. 103-105.

266. L. Morassi, G. Verzellesi, L. Larcher, H. Zhao, J.C. Lee, "Errors affecting split-CV mobility measurements in InGaAs MOS-HEMTs", Proc. of the 23th International Conference on Indium Phosphide and Related Materials (IPRM 2011), Berlin (Germany), May 2011, pp. 327-329.

267. T. Akyol, J. H. Yum, D. A. Ferrer, M. Lei, M. Downer, C. W. Bielawski, T. W. Hudnall, G. Bersuker, J. Lee and S. Banerjee, "Introduction of ALD Beryllium Oxide Gate Dielectric for III-V MOS Devices," Device Research Conference, Santa Barbara, 2011.

268. Hao Tang, Patrice Rannou, Ryan A. Mesch, Lei Zhu, Edward T. Yu, Jack C. Lee, and C. Grant Willson, "Mobility Enhancement in Mesophases of Liquid Crystalline Organic Semiconductors," Organic Microelectronics & Optoelectronics Workshop VII in San Francisco, July 18-20, 2011.

269. Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack Lee, "In0.7Ga0.3As tunneling field-effect-transistors with LaAlO3 and ZrO2 high-k dielectrics", Electrochemical Society meeting (2011).

270. (Invited Paper) Jack C. Lee, F. Xue, Y. Chen, Y. Wang, and F. Zhou, "High-K Dielectrics / High-Mobility Channel MOSFETs" Electrochemical Society meeting (2011).

271. Y. Wang, H. Zhao, Y. Chen, F. Xue, F. Zhou, and J. Lee, "SF_6 plasma treated high k dielectrics engineering on InP metal-oxide-semiconductor field-effect-transistors", 220th ECS Meeting, October 2011, Boston, MA.

272. J. H. Yum, T. Akyol, M. Lei, D. A. Ferrer, Todd. W. Hudnall, M. Downer, C. W. Bielawski, G. Bersuker, J. C. Lee and S. K. Banerjee, "ALD Beryllium Oxide as a High-k Gate Dielectric for III-V MOS Devices," Session A-44, the 2011 Atomic Layer Deposition Conference.

273. J. Yum, "ALD Beryllium Oxide: Novel Barrier Layer for High Performance Gate Stacks on Si and High Mobility Substrates," IEEE International Electron Devices Meeting Technical Digest, p. 638-641, 2011.

274. F. Xue, Y. Chen, Y. Wang, F. Zhou, B. Fowler, and J. Lee, "The Effect of Plasma Treatment on Reducing Electroforming Voltage of Silicon Oxide RRAM", 221st ECS Meeting in Seattle, Washington (May 6 -10, 2012).

275. Y. T. Chen, J. Huang, J. Price, P. Lysaght, D. Veksler, C. Weiland, J. C. Woicik, G. Bersuker, R. Hill, J. Oh, N. Goel, P. D. Kirsch, R. Jammy, and J. C. Lee, "III-V Gate Stack Interface Improvement to Enable High Mobility 11nm node CMOS", International Symposium on VLSI Technology, Systems and Applications, Hsin-Chu, R.O.C., 2012.

276. Yao-Feng Chang, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, Burt Fowler, and Jack C. Lee, "Study of SiOx-based Complementary Resistive Switching Memristor", Device Research Conference, June 18-20 (2012).

277. Y. Wang, Y. Chen, F. Xue, F. Zhou, and J. Lee, "MOSFETs on InP substrate with $LaAlO_3/HfO_2$ bilayer of different $LaAlO_3$ thickness and single $La_XAl_{1-X}O$ layer with different La doping level", 222th ECS meeting (Honolulu HI, Oct. 2012).

278. (Invited talk) Jack Lee, Fei Xue, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Yao-Feng Chang and Jack Lee, "Excellent Device performance of III-V Channel Field-Effect-Transistors with High-k Gate Dielectrics," Technical Digest of World Congress of Nano-Science and Technologies, Qingdao, China September 2012.

279. Mina J. Hanna, Han Zhao, and Jack C. Lee, "Hysteresis-like effect in AlGaN/GaN MISFETs with SiN gate dielectric," International workshop on nitride semiconductors, Sapporo, Japan, Oct. 2012.

280. X. Sun, N. Xu, F. Xue, A. Alian, F. Andrieu, B.Y. Nguyen, T. Poiroux, O. Faynot, J. Lee, S.Cui and T. P .Ma, "AC Transconductance: A Novel Method to Characterize Oxide Traps in Advanced FETs without a Body Contact" IEEE International Electron Devices Meeting (IEDM), p.19.4.1-19.4.4, Dec. 2012.

281. Fei Xue, Aiting Jiang, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, Yaofeng Chang and Jack Lee, "Excellent Device performance of 3D $In_{0.53}Ga_{0.47}As$ Gate-Wrap-Around Field-Effect-Transistors with High-k Gate Dielectrics," IEEE International Electron Devices Meeting (IEDM), p.27.5.1-27.5.4, Dec. 2012.

282. Yao-Feng Chang, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, Pai-Yu Chen, Burt Fowler, and Jack C. Lee, "Study of device architecture and multilevel characteristics in SiOx-based resistive switching memory", IEEE Semiconductor Interface Specialists Conference, December 6-8 (2012).

283. Yao-Feng Chang, Pai-Yu Chen, Burt Fowler, Yen-Ting Chen, Fei Xue, Yanzhen Wang, Fei Zhou, and Jack C. Lee, "Study of ambient effect in active SiOx-based resistive switching memory", International Symposium on VLSI Technology, Systems and Applications, April 22-24 (2013).

284. Yao-Feng Chang, Ying-Chen Chen, Ji Li, Fei Xue, Yanzhen Wang, Fei Zhou, Burt Fowler and Jack C. Lee, "Comprehensive Trap-Level Study in SiOx-based Resistive Switching Memory", Device Research Conference, June 23-26 (2013).

285. Yao-Feng Chang, Li Ji, Pai-Yu Chen, Fei Zhou, Fei Xue, Burt Fowler, Edward T. Yu, Jack C. Lee, "Study of SiO_x-Based Resistive Switching Memory by Nano-Sphere Lithography", IEEE Semiconductor Interface Specialists Conference, December 5-7 (2013).

286. Li Ji, Yao-Feng Chang, Ying-Chen Chen, Fei Zhou, Tsung-Ming Tsai, Kuan-Chang Chang, Min-Chen Chen, Ting-Chang Chang, Burt Fowler, Jack C. Lee, Edward T. Yu, "Optimization of High Density One Diode - One Resistor Architecture in Nano-Pillar SiO_x-Based Resistive Switching Memory by Nano-Sphere Lithography", *Materials Research Society Spring Meeting*, April 21-25 (2014).

287. Yao-Feng Chang, Li Ji, Ying-Chen Chen, Fei Zhou, Tsung-Ming Tsai, Kuan-Chang Chang, Min-Chen Chen, Ting-Chang Chang, Burt Fowler, Edward T. Yu and Jack C. Lee, "High-density nano-pillar SiOx-based resistive switching memory using nano-sphere lithography to fabricate a one diode - one resistor (1D-1R) architecture", IEEE International Symposium on VLSI Technology, Systems and Applications, April 28-30 (2014).

288. (Invited Paper) Fei Zhou, Fei Xue, Yao-Feng Chang and Jack Lee, “III-V Gate-Wrap-Around Field-Effect-Transistors with High-k Gate Dielectrics,” Device Research Conference, June 22-25, 2014.

289. Yao-Feng Chang, B. Fowler, Y. Chen, L. Ji, F. Zhou and Jack Lee, “The Voltage-Triggered SET Mechanism and Self-Compliance Characteristics in Intrinsic Unipolar SiO_x-Based Resistive Switching Memory,” Device Research Conference, June 22-25, 2014.

290. Fei Zhou, Yao-Feng Chang, Burt Fowler, and Jack C. Lee, "Characteristics of PECVD SiO_xN_{1-x} for Resistive Memory Application" International Conference on Metallurgical Coatings & Thin Films, April 28 - May 2 (ICMCTF 2014).

291. Fei Zhou, Yao-Feng Chang, Burt Fowler, and Jack C. Lee, "Discussion on Backward Voltage Sweep Set Effect in SiO_x Resistive Memory" 32nd International Conference on the Physics of Semiconductors (ICPS 2014), August 10-15.

292. Yao-Feng Chang, Burt Fowler, Li Ji, Ying-Chen Chen, Fei Zhou, Edward T. Yu, and Jack C. Lee, "Comprehensive Study of Intrinsic Unipolar SiO_x-Based RRAM Characteristics and Self-Compliance Characteristics in High-Density Nano Pillar-Type 1D-1R Architecture" 32nd International Conference on the Physics of Semiconductors (ICPS 2014), August 10-15.

293. Li Ji, Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Tsung-Ming Tsai, Kuan-Chang Chang, Min-Chen Chen, Ting-Chang Chang, Simon M. Sze, Edward T. Yu, and Jack C. Lee, “Resistive Switching of SiO_X with One Diode-One Resistor Nanopillar Architecture Fabricated via Nanosphere Lithography”, IEEE Device Research Conference, June 22-25 (2014).

294. Li Ji, Martin D. McDaniel, Li Tao, Xiaohan Li, Agham B. Posadas, Yao-Feng Chang, Alexander A. Demkov, John G. Ekerdt, Deji Akinwande, Rodney S. Ruoff, Jack C. Lee and Edward T. Yu, “Atomic Scale Engineering of Metal-Oxide-Semiconductor Photoelectrodes for Energy Harvesting Application Integrated with Graphene and Epitaxy SrTiO3,” 2014 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, December 15^{th}-17^{th}, 2014.

295. Yao-Feng Chang, Burt Fowler, Fei Zhou, Kwangsub Byun, Jack C. Lee, "Study of SiOx-Based Resistive Switching Memory (ReRAM) in Integrated One Diode – One Resistor (1D-1R) Architecture" IEEE Semiconductor Interface Specialists Conference (SISC), December 10-13 (2014).

296. (Invited Talk) J. Lee, “Advantages and Challenges of FinFET Devices and Technologies,” Northern California Chapter American Vacuum Society Conference, Sept. 25, 2014.

297. K. Byun, F. Zhou, B. Fowler, Y.F. Chang, and J.C. Lee "Electrical characteristics of Si nanocrystal filament in unipolar SiO_x based RRAM," 45th IEEE Semiconductor Interface Specialists Conference (SISC), Dec. 2014.

298. Yao-Feng Chang, Burt Fowler, Fei Zhou, Kwangsub Byun, Jack C. Lee, "Study of SiOx-Based Resistive Switching Memory (ReRAM) in Integrated One Diode – One Resistor (1D-1R) Architecture" 45th IEEE Semiconductor Interface Specialists Conference (SISC), December 10-13 (2014).

299. Yao-Feng Chang, Burt Fowler, Fei Zhou, Kwangsub Byun, Jack C. Lee, "Understanding Electroforming and Resistive Switching in Silicon Dioxide Resistive Memory Devices" American Physical Society (APS) March Meeting 2015.

300. Yao-Feng Chang, Burt Fowler, Fei Zhou, Kwangsub Byun, and Jack C. Lee, "Comprehensive study of intrinsic unipolar SiO_x-based ReRAM characteristics and resistive switching mechanism in TiW/SiO_x/TiW structure" International Symposium on VLSI Technology, Systems and Applications (2015 VLSI-TSA) April 2015.

301. [Best Student Papers Award] Yao-Feng Chang, Burt Fowler, Fei Zhou, Jack C. Lee, "Study of SiOx-Based Resistive Switching Memory (ReRAM) in Integrated One Diode – One Resistor (1D-1R) Architecture," 4th International Symposium on Next-Generation Electronics (IEEE ISNE 2015) at National Taiwan University of Science and Technology in Taipei, Taiwan from May 4-6, 2015.

302. (Invited Talk) Yao-Feng Chang, Burt Fowler, Fei Zhou, and Jack C. Lee, "The Intrinsic Unipolar SiOx-based Resistive Switching Memory: Characterization, Mechanism and Applications" ECS Fall Meeting (2015).

303. (Invited Talk) Yao-Feng Chang, "Intrinsic Unipolar SiOx-Based Resistive Switching Memory: Characterization, Mechanism and Applications" International Symposium on Next-Generation Electronics, Taipei, Taiwan, May 4 - 6 (2015).

304. Kwangsub Byun, Ying Wang, Bruce Adams, Jack Lee, "Laser Curing and Ink-Jet Processes for Fabricating SiOx RRAM Structures," 43rd International Conference on the Physics and Chemistry of Surfaces & Interfaces (PCSI-43), 2016.

305. (Best Paper Award Finalist) Ying-Chen Chen, Yao-Feng Chang, Burt Fowler, Fei Zhou, Xiaohan Wu, Cheng-Chih Hsieh, Heng-Lu Chang, Chih-Hung Pan, Min-Chen Chen, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, and Jack C. Lee, "Comprehensive Study of Intrinsic Unipolar SiOx-Based ReRAM Characteristics in AC Frequency Response and Low Voltage (< 2V) Operation" International Symposium on VLSI Technology, Systems and Applications (VLSI- TSA) 2016.

306. Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, MeiqiGuo, Fei Zhou, Burt Fowler, Jack C Lee, "Characterization of SiOx/HfOx bilayer Resistive-Switching Memory Devices," *Electrochemical Society (ECS) Meeting*, 2016.

307. Meiqi Guo, Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, Burt Fowler, Yonggang Zhao and Jack C. Lee, "Characteristics of Electrically Driven Metal-Insulator-Transition (E-MIT) in Nb-doped SrTiO3 and HfO2-based Selector Devices," Device Research Conference (DRC) (2016).

308. Fei Zhou, Ying-Chen Chen, Xiaohan Wu, MeiqiGuo, Burt Fowler, Jack Lee "The Role of Oxygen Deficiency in SiO_x Based Resistive Memory," *International Conference on Metallurgical Coatings and Thin Films (ICMCTF)*, 2016.

309. (Invited) Ying-Chen Chen, Xiaohan Wu, MeiqiGuo, Fei Zhou, Yao-Feng Chang, Burt Fowler, Chih-Hung Pan, Ting-Chang Chang, Jack C Lee, "Memcomputing (Memristor+ Computing) in Intrinsic SiOx-Based Resistive Switching Memory", 230th Meeting of The Electrochemical Society (2016).

310. Ying-Chen Chen, Xiaohan Wu, Meiqi Guo, Fei Zhou, Yao-Feng Chang**, Burt Fowler, Chih-Hung Pan, Ting-Chang Chang, and Jack C. Lee, "Memcomputing (Memristor + Computing) in Intrinsic SiO_x-Based Resistive Switching Memory" PRiME 2016 (Invited Talk).

311. (Best Student Paper Award) Chih-Yang Lin, Ying-Chen Chen, Meiqi Guo, Chih-Hung Pan, Fu-Yuan Jin, Cheng Chih Hsieh, Xiaohan Wu, Min-Chen Chen, Yao-Feng Chang, Fei Zhou, Burt Fowler, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Yonggang Zhao, Simon M. Sze, Sanjay Banerjee, Jack C. Lee, "A Universal Model for Interface-type Threshold Switching Phenomena by Comprehensive Study of Vanadium Oxide-Based Selector", International Symposium on VLSI Technology, Systems and Applications (2017 VLSI-TSA), Hsinchu, Taiwan, April 24-27, (2017).

312. Sungjun Kim, Yao-Feng Chang*, Ying-Chen Chen, Byung-Gook Park, and Jack C. Lee, "Resistive Switching Characteristics and Mechanisms in Silicon Oxide and Silicon Nitride Memristors", China RRAM International Workshop (2017).

313. Y.-C. Chen, YF Chang, CY Lin, X Wu, G Xu, B Fowler, TC Chang, JC Lee, "Built-in Nonlinear Characteristics of Low Power Operating One-Resistor Selector-Less RRAM By Stacking Engineering", 232nd Meeting of The Electrochemical Society (2017).

314. Jia Chen, Sungjun Kim, Ying-Chen Chen, Min-Hwi Kim, Yi Li, Xiang-Shui Miao, Yao-Feng Chang, Byung-Gook Park, Jack C. Lee, "Synaptic Properties Considering Temperature Effect in HfOx-Based Memristor – Demonstration of Homo-thermal Synaptic Behaviors", International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) (2018).

315. Ying-Chen Chen, Xiaohan Wu, Yao-Feng Chang, Jack C Lee, "Nonlinearity Enhancement by Positive Pulse Stress in Multilevel Cell Selectorless RRAM Applications", 76th Device Research Conference (DRC). 2018.

316. Y.-C. Chen, C.-Y. Lin, Y.-F. Chang, T.-C. Chang, J. Lee, "Selector-Less Graphite Memristor: Intrinsic Nonlinear Behavior with Gap Design Method for Array Applications," 233rd Meeting of The Electrochemical Society (2018).

317. Ruijing Ge, Xiaohan Wu, Myungsoo Kim, Po-An Chen, Jianping Shi, Junho Choi, Xiaoqin Li, Yanfeng Zhang, Meng-Hsueh Chiang, Jack C. Lee and Deji Akinwande, "Atomristors: Memory Effect in Atomically-thin Sheets and Record Solid-state RF Switches," IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, December 1-5, 2018.

318. Ying-Chen Chen, Chih-Yang Lin, Yao-Feng Chang and Jack C. Lee, "Energy Efficient Nonlinear Selectorless RRAM by Current Sweep Operation for Crossbar Array Applications," IEEE Semiconductor Interface Specialists Conference (SISC), San Diego CA, December 5-8, 2018.

319. Ying-Chen Chen, Szu-Tung Hu, Chao-Cheng Lin, Jack C. Lee, "Resistive Switching Early Failure and Gap Identification in Bilayer Selectorless RRAM Applications" 77th Device Research Conference (DRC), 2019.

320. Y.C. Chen, C.Y. Lin, H.C. Huang and J. C. Lee "Energy Efficient Operation Schemes of Nonlinear Selectorless RRAM for Crossbar Array Applications" 61st Electronic Materials Conference (EMC), 2019.

321. Ying-Chen Chen, Chao-Cheng Lin, Sungjun Kim, Yao-Feng Chang, Jack Lee, "Non-Uniform Dielectric Selectorless Resistive Switching Memory and Reliability Determination for Low Power Array Applications" 235th Meeting of The Electrochemical Society, 2019.

322. Xiaohan Wu, Ruijing Ge, Po-An Chen, Meng-Hsueh Chiang, Deji Akinwande, Jack C. Lee, "Non-Volatile Resistance Switching Phenomenon in Monolayer h-BN", 236th Electrochemical Society ECS Meeting, 2019. (Invited talk)

323. Myungsoo Kim, Emiliano Pallecchi, Ruijing Ge, Xiaohan Wu, Vanessa Avramovic, Etienne Okada, Jack C. Lee, Henri Happy, and Deji Akinwande, "Non-volatile RF and mm-wave Switches based on monolayer hBN" International Electron Devices Meeting (IEDM) Dec. 2019.

324. Saban Hus, Ruijing Ge, Xiaohan Wu, Yuqian Gu, Jack C Lee, An-Ping Li, Deji Akinwande, "Atomic Level Investigation of Resistance Switching in 2D Memory Devices", 235th Electrochemical Society ECS Meeting. 2019.

325. Xiaohan Wu, Ruijing Ge, Deji Akinwande and Jack C. Lee, "Non-volatile resistance switching behavior in monolayer two-dimensional materials", Electronic Materials Conference EMC 2020.

326. Y. Huang, X. Wu, R. Ge, D. Akinwande, J. C. Lee, "Modeling of temperature distribution in 2D MoS2-based non-volatile resistance switching devices," *51st IEEE Semiconductor Interface Specialists Conference (SISC)*, 2020.

327. Xiaohan Wu, Ruijing Ge, Deji Akinwande and Jack C. Lee, "Understanding of Multiple Resistance States by Current-sweep Measurement and Compliance Current Modulation in 2D MoS2-based Non-volatile Resistance Switching Devices", Device Research Conference DRC 2020.

328. Xiaohan Wu, Ruijing Ge, Myungsoo Kim, Deji Akinwande and Jack C. Lee, "Atomristors: Non-volatile Resistance Switching in 2D monolayers", Proceedings of the 2020 Pan Pac Microelectronics Symposium.

329. Xiaohan Wu, Ruijing Ge, Deji Akinwande and Jack C. Lee, "Non-volatile Resistance Switching in Monolayer 2D Atomic Sheets", Electronic Materials Science Nov. 5-7, 2020.

330. Xiaohan Wu, Ruijing Ge, Myungsoo Kim, Deji Akinwande and Jack C. Lee, "The Applications of 2D Monolayer-based Atomristors in Non-volatile Memory, RF switches and Neuromorphic Computing", MRS Spring/Fall Meeting, Nov. 27-Dec. 5, 2020.

331. Xiaohan Wu, Ruijing Ge, Myungsoo Kim, Deji Akinwande and Jack C. Lee, "Atomristors: Non-volatile Resistance Switching Behavior in 2D Monolayers and the Applications in Memory, RF Switch and Neuromorphic Computing", TechConnect World Innovation Conference, June 12-14, 2021.

332. Yao-Feng Chang, Ilya Karpov, Reed Hopkins, David Janosky, Jacob Medeiros, Benjamin Sherrill, Jiahan Zhang, Yifu Huang, Tanmoy Pramanik, Albert Chen, Tony Acosta, Abdullah Guler, James A O'Donnell, Pedro A Quintero, Nathan Strutt, Oleg Golonzka, Chris Connor, Jack C Lee, Jeffrey Hicks, "A Comprehensive Study of Enhanced Characteristics with Localized Transition in Interface-type Vanadium-based Devices" International Reliability Physics Symposium (IRPS), March 21- March 24, (2021).

333. Xiaohan Wu, Ruijing Ge, Yuqian Gu, Saban M. Hus, Jack C. Lee and Deji Akinwande "A Library of Atomristors: Non-Volatile Resistive Switching Phenomenon in 2D Atomic Sheets", Device Research Conference *2021*. (Invited talk)

334. Xiaohan Wu, Ruijing Ge, Yuqian Gu, Emmanuel Okogbue, Jianping Shi, Abhay Shivayogimath, Peter Bøggild, Timothy J. Booth, Yanfeng Zhang, Yeonwoong Jung, Jack C. Lee and Deji Akinwande "Universal Non-Volatile Resistive Switching Behavior in 2D Metal Dichalcogenides Featuring Unique Conductive-Point Random Access Memory Effect", Electron Devices Technology and Manufacturing Conference (EDTM) 2021.

335. Xiaohan Wu, Ruijing Ge, Myungsoo Kim, Deji Akinwande and Jack C. Lee "Atomristors: Non-volatile Resistance Switching Behavior in 2D Monolayers", *TechConnect World Innovation Conference 2021*.

336. Xiaohan Wu, Ruijing Ge, Deji Akinwande and Jack C. Lee "Toward Universal 2D Memory: Conductive-Point Resistive Switching in Non-Metallic Atomic Layers", *Electronic Materials Conference June 23-25, 2021*.

337. Y. Huang, X. Wu, Y. Gu, R. Ge, J. Zhang, Y. F. Chang, D. Akinwande, and J. C. Lee, "Monte Carlo and Circuit-Level Simulation of 2D Memristors for Neuromorphic Computing", *2021 IEEE 16th Nanotechnology Materials and Devices Conference (NMDC)*, 1-5, 2021.

338. Y. Huang, Y. Gu, X. Wu, R. Ge, Y.-F. Chang, X. Wang, J. Zhang, D. Akinwande and J. C. Lee, "ReSe2-based RRAM and Circuit-level Model for Neuromorphic Computing", *Frontiers in Nanotechnology*, 89, 2021.

339. Y. Huang, X. Wu, Y. Gu, R. Ge, J. Zhang, Y.-F. Chang, D. Akinwande and J. C. Lee. "2D ReSe2 RRAM and Analog Model for Neuromorphic Computing". *52nd IEEE Semiconductor Interface Specialists Conference (SISC)*, 2021.

340. Y. Huang, Y. Gu, Y.-F. Chang, D. Akinwande, J. C. Lee. "Understand the Resistive Switching Mechanism of 2D RRAM by Monte Carlo Modeling". *53rd IEEE Semiconductor Interface Specialists Conference (SISC)*, 2022.

PATENTS ISSUED

1. B. Doyle and J. Lee, "Method for Forming a High Dielectric Constant Insulator in the Fabrication of an Integrated Circuit, " (issued April 6, 1999, US 5,891,798)
2. M. Gardner, M. Gilmer, J. Fulford and J. Lee, "Semiconductor Device Having a Tri-Layer Gate Insulating Dielectric," (issued May 2000, US 6,057,584)
3. M. Gardner, J. Fulford and J. Lee, "Semiconductor Having a PMOS Device Having Source/Drain Region Formed using a Heavy Atom P-type Implant and Method of Manufacturing Thereof," (issued January 11, 2000, US 6,013,546).
4. M. Gardner, J. Fulford and J. Lee, "Semiconductor Device with Asymmetric PMOS Source/Drain Implant and Method of Manufacture Thereof" (issued Nov. 14, 2000, US 6,146,934)
5. B. Doyle and J. Lee, "Method for Forming a High Dielectric Constant Insulator in the Fabrication of an Integrated Circuit" (issued Oct. 2001, US6,306,742)
6. Jack Lee and Han Zhao, "Tunnel Field Effect Transistor (TFET) with Lateral Oxidation," (issued Mar. 26, 2016, US 9,293,591).
7. Jack Lee and Han Zhao, "Tunnel Field Effect Transistor (TFET) with Lateral Oxidation," (issued Dec. 26, 2017, US 9,853,135).
8. Jack C. Lee and Fei Xue, "Three-Dimensional Gate-Wrap-Around Field Effect Transistor" (issued June 2, 2015, US 9,048,330)

9. Jack C. Lee and Fei Xue, “Vertical III-V Nanowire Field-Effect Transistor Using Nanosphere Lithography,” (issued Dec. 8, 2015, US 9,209,271).
10. Deji Akinwande, Xiaohan Wu, Ruijing Ge and Jack C. Lee, Non-volatile Resistance Switching in Monolayer Atomic Sheets. *Serial No. 62/548,295, Aug. 2017*

Book / Book Chapters

1. Xiaohan Wu, Ruijing Ge, Deji Akinwande, Jack C. Lee “Memristors based on 2D monolayer materials”, Memristors. Published by Intech 2021.

2. Ruijing Ge, Xiaohan Wu, Myungsoo Kim, Jack C. Lee and Deji Akinwande, “2D Materials based Non-volatile Resistive Memories and RF Switches”, *Emerging 2D Materials and Devices for the Internet of Things: Information, Sensing and Energy Applications*, 1st Edition. ISBN: 978-012-81-8386-1, Published by Elsevier, June 2020.

3. Cheng Chih Hsieh, Yao-Feng Chang, Ying-Chen Chen, Chih-Yang Lin, Meiqi Guo, Fei Zhou, Burt Fowler, Ting-Chang Chang, Sanjay Banerjee, Jack C. Lee, “Memristor and Memristive Neural Networks: Review of Recently Progress on Memcomputing (Memristor + Computing) Applications in Intrinsic SiOx-Based Resistive Switching Memory”, ISBN: 978-953-51-5481-5, InTech (2018).

4. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Simon M. Sze, and Jack C. Lee, "A Synaptic Device Built in One Diode-One Resistor (1D-1R) Architecture with Intrinsic SiOx-based Resistive Switching Memory", Nano Devices and Sensors, Published by De Gruyter publisher, March (2016).

5. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Kuan-Chang Chang, Tsung-Ming Tsai, Ting-Chang Chang, Simon M. Sze, and Jack C. Lee, "A Synaptic Device Built in One Diode-One Resistor (1D-1R) Architecture with Intrinsic SiOx-based Resistive Switching Memory", *Nano Devices and Sensors*, p. 91-112, ISBN: 978-1-5015-0153-1, Published by De Gruyter, (March 2016).

6. Yao-Feng Chang, Burt Fowler, Ying-Chen Chen, Fei Zhou, Xiaohan Wu, Yen-Ting Chen, Yanzhen Wang, Fei Xue, and Jack C. Lee, “Resistive Switching Characteristics and Mechanisms in Silicon Oxide Memory Devices,” *Nano Devices and Sensors*, p. 73-90, ISBN: 978-1-5015-0153-1, Published by De Gruyter publisher, (March 2016).

7. Y. H. Kim and J. Lee, “Hf-Based High-K Dielectrics, Process Development, Performance Characterization and Reliability,” ISBN: 9781598290042, Morgan and Claypool Publishers (Jan. 2006).

8. K. Onishi and J. Lee, “High-*k* Transistor Characteristics” in the book entitled, “High k Gate Dielectrics” (Ed. Michel Houssa), ISBN:0-7503-0906-7, published by IOP Publishing Ltd (2004).

APPENDIX 2: MATERIALS CONSIDERED IN THE PREPARATION OF THIS DECLARATION

Exhibit No.	Description
1001	U.S. Patent No. 9,929,240 to Polishchuk et al. ("the '240 patent")
1002	Prosecution file history for the '240 patent, U.S. Patent Application No. 15/335,180 ("Pros. Hist.")
1004	U.S. Patent Application Publication No. 2012/0068255 to Changhyun Lee, et al. ("Lee '255")
1005	Korean Patent Publication No. 2011-0118961 to Gi Hong Lee et al. and Certified English Translation of Korean Patent Publication No. 2011-0118961 to Gi Hong Lee et al. ("Lee '961")
1006	U.S. Patent Application Publication No. 2006/0065919A1 to Ichiro Fujiwara ("Fujiwara")
1007	L. Lukasiak and A. Jakubowski, History of Semiconductors, Journal of Telecommunications and Information Technology, Vol. 3 (2010) ("Lukasiak")
1008	U.S. Patent No. 4,203,158 to Dov Frohman-Bentchkowsky, et al. ("Frohman-Bentchkowsky")
1009	U.S. Patent Application Publication No. 2006/0255399 to Ju-Hyung Kim, et al. ("Kim '399")
1010	U.S. Patent Application Publication No. 2003/0122204 to Kazumasa Nomoto, et al. ("Nomoto")
1011	U.S. Patent Application Publication No. 2009/0179253 to Levy, et al. ("Levy")
1012	U.S. Patent Application Publication No. 2011/0045647 to Jin-Hwa Heo, et al. ("Heo")
1013	U.S. Patent Application Publication No. 2011/0281429 to Udayan Ganguly, et al. ("Ganguly")
1014	US 2006/0113586 to Wang ("Wang '586")
1015	U.S. Patent No. 6,897,533 to Jean Yee-Mei Yang, et al. ("Yang '533")
1016	U.S. Patent Application Publication No. 2006/0198189 to Hang-

Exhibit No.	Description
	Ting Lue, et al. ("Lue '189")
1017	U.S. Patent Application Publication No. 2009/0059676 to Shen Chih Lai, et al. ("Lai '676")
1018	Erh-Kun Lai, et al., *A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory*, Proceedings of the 2006 International Electron Devices Meeting (IEEE Dec. 2006) ("Lai Article")
1019	U.S. Patent Application Publication No. 2005/0006696A1 to Mitsuhiro Noguchi, et al. ("Noguchi")
1020	Antonio Arreghini, et al., *Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells*, IEEE Transactions on Electron Devices, Vol. 55, No. 5 (May 2008) ("Arreghini")
1021	U.S. Patent Application Publication No. 2010/0157680A1 to Masaaki Higuchi, et al. ("Higuchi")
1022	U.S. Patent Application Publication No. 2008/0128790 to Jin-Hyo Jung ("Jung")
1023	U.S. Patent Application Publication No. 2003/0198106 to Jeong-Hyuk Choi ("Choi").
1024	U.S. Patent Application Publication No. 2009/0026460 to Tien-Fan Ou, et al. ("Ou")
1025	Falong Zhou, et al., *VDNROM: A Novel Four-Bits-Per-Cell Vertical Channel Dual-Nitride-Trapping-Layer ROM for High Density Flash Memory Applications*, Proceeding of 2006 European Solid-State Device Research Conference (IEEE Sept. 2006) ("VDNROM")
1026	H. Tanaka, et al., *Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory*, 2007 IEEE Symposium on VLSI Technology (June 2007) ("Tanaka")
1027	Toshiba Press Release, Toshiba Develops New NAND Flash Technology (June 12, 2007) ("Toshiba PR")
1028	U.S. Patent Application Publication No. 2010/0178759A1 to JinGyun Kim, et al. ("Kim '759")

Exhibit No.	Description
1029	Moon Kyung Kim, et al., *A Comparison of N+ Type and P+ Type Polysilicon Gate in High Speed Non-Volatile Memories*, Material Research Society Symposium Proceedings, Vol. 997 (MRS 2007) ("Kim Article")
1030	U.S. Patent Application Publication No. 2006/0118858 to Sang-hun Jeon ("Jeon")
1031	U.S. Patent Application Publication No. 2005/0237809 to Yen-Hao Shih, et al. ("Shih")
1032	U.S. Patent Application Publication No. 2012/0276696 to Jun-Kyu Yang, et al. ("Yang '696")
1033	U.S. Patent Application Publication No. 2013/0270625 to Byong-hyun Jang, et al. ("Jang")
1034	U.S. Patent Application Publication No. 2012/0068247 to Changhyun Lee, et al. ("Lee '247")
1035	U.S. Patent Application Publication No. 2012/0299086 to Jaegoo Lee ("Lee '086")
1036	U.S. Patent Application Publication No. 2011/0316064 to Jung Ho Kim, et al. ("Kim '064")
1037	U.S. Provisional Application No. 60/940,160 ("'160 Provisional App.")
1038	Prosecution file history for the '434 patent (U.S. Application No. 12/152,518) ("'434 Pros. Hist.)
1039	Prosecution file history for the '374 patent (U.S. Application No. 13/288,919) ("'374 Pros. Hist.")
1040	Prosecution file history for the '537 patent (U.S. Application No. 13/539,466) ("'537 Pros. Hist.")
1041	U.S. Patent No. 6,912,163 to Wei Zheng, et al. ("Zheng")
1042	S.M. Sze and K. Ng, *Physics of Semiconductor Devices* (3rd Ed. Wiley-Interscience 2007) ("Sze")
1043	U.S. Patent Application Publication No. 2010/0019312 to Katsuyuki Sekine, et al. ("Sekine")
1045	Declaration of June Munford

Exhibit No.	Description
1046	IEEE Declaration of Gordon MacPherson
1048	U.S. Patent Application Publication No. 2012/0061744 to Sung-Min Hwang et al ("Hwang")
1049	Excerpts from The American Heritage Dictionary of the English Language (5th Ed. 2011) (American Heritage Excerpts)
1050	US 2008/0272424 to Kim et al. ("Kim '424")
1051	US 2007/0029625 to Lue et al. ("Lue '625")
1052	US 2006/0008959 to Hagemeyer et al., ("Hagemeyer")
1053	Prosecution file history for the '336 patent (U.S. Application No. 15/864,832) ("'336 Pros. Hist.")
1054	Infringement Contentions from *SanDisk Corp. v. IPValue Management, Inc., et al.*, No. 25-cv-02389 (N.D. Cal.) (Infringement Contentions)
1055	Excerpts from Merriam-Webster's Collegiate Dictionary (11th Ed. 2003) (Merriam-Webster Excerpts)
1056	Excerpts from New Oxford American Dictionary (3rd Ed. 2010) (New Oxford Excerpts)
1057	US 5,998,826 to Hung et al. ("Hung")
1058	US 2009/0268522 to Maejima ("Maejima")
1059	EP 0 810 667 A2 by Hyundai ("Hyundai")
1060	US 2003/0135690 to Lee et al. ("Lee '690")

APPENDIX 3: CHALLENGED CLAIMS

[1pre]. A memory device, comprising:

[1a] a gate structure;

[1b] a channel positioned between and electrically connecting a first diffusion region and a second diffusion region; and

[1c] a tunnel dielectric layer,

[1d] a multi-layer charge trapping layer, and

[1e] a blocking dielectric layer disposed between the gate structure and the channel,

[1f] wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer and an anti-tunneling layer disposed between the first and second dielectric layers, wherein the anti-tunneling layer includes an oxide layer, and

[1g] wherein the first dielectric layer includes oxygen-rich nitride, and the second dielectric layer includes oxygen-lean nitride.

3. The memory device of claim 1, wherein the channel, first and second diffusion regions are disposed above a semiconductor material structure.

4. The memory device of claim 1, wherein the channel, first and second diffusion regions are suspended above a semiconductor material structure.

5. The memory device of claim 1, wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure.

[6pre]. The memory device of claim 1,

[6a] wherein the first dielectric layer is disposed abutting the tunnel dielectric layer and substantially trap free, and

[6b] wherein the second dielectric layer is disposed abutting the blocking dielectric layer.

7. The memory device of claim 1, wherein the blocking dielectric layer comprises high K high temperature oxide (HTO).

9. The memory device of claim 1, wherein the gate structure includes a high work function gate electrode.

11. The memory device of claim 9, wherein the high work function gate electrode comprises a P+ doped polysilicon layer.

[12pre]. A semiconductor device, comprising:

a memory device including,

[12a] a gate structure

[12b] including a first high work function gate electrode,

[12c] a channel positioned between and electrically connecting a first diffusion region and a second diffusion region,

[12d] wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure, and

[12e] a tunnel dielectric layer,

[12f] a multi-layer charge trapping layer, and

[12g] a blocking dielectric layer disposed between the gate structure and the channel,

[12h] wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,

[12i] wherein the first dielectric layer includes oxygen-rich nitride and the second dielectric layer includes oxygen-lean nitride; and

[12j] a metal oxide semiconductor (MOS) logic device including a gate oxide layer, and a second high work function gate electrode disposed thereon.

[13pre]. The semiconductor device of claim 12,

[13a] wherein the first dielectric layer of the multi-layer charge trapping layer is disposed abutting the tunnel dielectric layer and substantially trap free, and

[13b] wherein the second dielectric layer is disposed abutting the blocking dielectric layer.

14. The semiconductor device of claim 12, wherein the MOS logic device is formed at least partially within a semiconductor material structure.

15. The semiconductor device of claim 14, wherein the channel is vertical and oriented substantially orthogonal to the semiconductor material structure.

[16pre]. A semiconductor device, comprising:

a memory device including,

[16a] a gate structure

[16b] including a first high work function gate electrode,

[16c] a blocking dielectric layer disposed abutting the gate structure,

[16d] a multi-layer charge trapping layer disposed abutting the blocking dielectric layer,

[16e] wherein the multi-layer charge trapping layer comprises a first dielectric layer disposed abutting a second dielectric layer,

[16f] wherein the first dielectric layer includes oxygen-rich nitride, and the second dielectric layer includes oxygen-lean nitride,

[16g] a tunnel dielectric layer disposed abutting the multi-layer charge trapping layer, and

[16h] a channel disposed abutting the tunnel dielectric layer, wherein the channel is positioned between and electrically connecting a first diffusion region and a second diffusion region,

[16i] wherein the channel is vertical and oriented substantially perpendicular to a semiconductor material structure; and

[16j] a metal oxide semiconductor (MOS) logic device including a gate oxide layer, and a second high work function gate electrode disposed thereon.

17. The semiconductor device of claim 16, wherein the MOS logic device is formed at least partially on the semiconductor material structure.

18. The semiconductor device of claim 16, wherein the multi-layer charge trapping layer further comprises an anti-tunneling layer disposed between the first

and second dielectric layers, and wherein the anti-tunneling layer includes an oxide layer.

APPENDIX 4: UNDERSTANDING OF THE LAW

I have applied the following legal principles provided to me by counsel in arriving at the opinions shown in this report.

Legal Standard for Prior Art

I am not an attorney. I have been informed by attorneys of the relevant legal principles and have applied them to arrive at the opinions shown in this declaration.

I understand that the Petition in an *inter partes* review proceeding may challenge the validity of one or more patent claims and request the cancellation of those claims based on the grounds available under 35 U.S.C. § 102 and 35 U.S.C. § 103 using prior art that consists of patents and printed publications.

Anticipation and Prior Art

I understand that § 102 specifies when a challenged claim is invalid for lacking novelty over the prior art, and that this concept is also known as "anticipation." I understand that a prior art reference anticipates a challenged claim, and thus renders it invalid by anticipation, if all elements of the challenged claim are disclosed in the prior art reference. I understand the disclosure in the prior art reference can be either explicit or inherent, meaning it is necessarily present or implied. I understand that the prior art reference does not have to use the same words as the challenged claim, but all of the requirements of the claim

must be disclosed so that a person of ordinary skill in the art could make and use the claimed subject-matter.

In addition, I understand that § 102 also defines what is available for use as a prior art reference to a challenged claim.

Under § 102(a), a challenged claim is anticipated if it was patented or described in a printed publication in the United States or a foreign country before the challenged claim's date of invention.

Under § 102(b), a challenged claim is anticipated if it was patented or described in a printed publication in the United States or a foreign country more than one year prior to the challenged patent's filing date.

Under § 102(e), a challenged claim is anticipated if it was described in a published patent application that was filed by another in the United States before the challenged claim's date of invention or was described in a patent granted to another that was filed in the United States before the challenged claim's date of invention.

I understand that a challenged claim's date of invention is presumed to be the challenged patent's filing date. I also understand that the patent owner may establish an earlier invention date and "swear behind" prior art defined by § 102(a) or § 102(e) by proving (with corroborated evidence) the actual date on which the

named inventors conceived of the subject matter of the challenged claim and proving that the inventors were diligent in reducing the subject matter to practice.

I understand that the filing date of a patent is generally the filing date of the application filed in the United States that issued as the patent. However, I understand that a patent may be granted an earlier effective filing date if the patent owner properly claimed priority to an earlier patent application.

I understand that when a challenged claim covers several structures, either generically or as alternatives, the claim is deemed anticipated if any of the structures within the scope of the claim is found in the prior art reference.

I understand that when a challenged claim requires selection of an element from a list of alternatives, the prior art teaches the element if one of the alternatives is taught by the prior art.

Legal Standard for Obviousness

I understand that even if a challenged claim is not anticipated, it is still invalid if the differences between the claimed subject matter and the prior art are such that the claimed subject matter would have been obvious to a person of ordinary skill in the pertinent art at the time the alleged invention.

I understand that obviousness must be determined with respect to the challenged claim as a whole.

I understand that one cannot rely on hindsight in deciding whether a claim is obvious.

I also understand that an obviousness analysis includes the consideration of factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the challenged claim, (3) the level of ordinary skill in the pertinent art, and (4) "secondary" or "objective" evidence of non-obviousness.

Secondary or objective evidence of non-obviousness includes evidence of: (1) a long felt but unmet need in the prior art that was satisfied by the claimed invention; (2) commercial success or the lack of commercial success of the claimed invention; (3) unexpected results achieved by the claimed invention; (4) praise of the claimed invention by others skilled in the art; (5) taking of licenses under the patent by others; (6) deliberate copying of the claimed invention; and (7) contemporaneous and independent invention by others. However, I understand that there must be a relationship between any secondary evidence of non-obviousness and the claimed invention.

I understand that a challenged claim can be invalid for obviousness over a combination of prior art references if a reason existed (at the time of the alleged invention) that would have prompted a person of ordinary skill in the art to combine elements of the prior art in the manner required by the challenged claim. I understand that this requirement is also referred to as a "motivation to combine,"

"suggestion to combine," or "reason to combine," and that there are several rationales that meet this requirement.

I understand that the prior art references themselves may provide a motivation to combine, but other times simple common sense can link two or more prior art references. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may come from market forces.

I understand obviousness to include, for instance, scenarios where known techniques are simply applied to other devices, systems, or processes to improve them in an expected or known way. I also understand that practical and common-sense considerations should be applied in a proper obviousness analysis. For instance, familiar items may have obvious uses beyond their primary purposes.

I understand that the combination of familiar elements according to known methods is obvious when it yields predictable results. For instance, obviousness bars patentability of a predictable variation of a technique even if the technique originated in another field of endeavor. This is because design incentives and other market forces can prompt variations of it, and predictable variations are not the product of innovation, but rather ordinary skill and common sense.

I understand that a particular combination may be obvious if it was obvious to try the combination. For example, when there is a design need or market

pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. This would result in something obvious because the result is the product not of innovation but of ordinary skill and common sense. However, I understand that it may not be obvious to try a combination when it involves unpredictable technologies.

It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

It is my understanding that the Manual of Patent Examining Procedure §2143 sets forth the following as exemplary rationales that support a conclusion of obviousness:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

- Choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

A person of ordinary skill in the art looking to overcome a problem will often use the teachings of multiple publications together like pieces of a puzzle, even though the prior art does not necessarily fit perfectly together. Therefore, I understand that references for obviousness need not fit perfectly together like puzzle pieces. Instead, I understand that obviousness analysis takes into account inferences, creative steps, common sense, and practical logic and applications that a person of ordinary skill in the art would employ under the circumstances.

I understand that a claim can be obvious in light of a single reference, if the elements of the challenged claim that are not explicitly or inherently disclosed in the reference can be supplied by the common sense of one of skill in the art.

I understand that obviousness also bars the patentability of applying known or obvious design choices to the prior art. One cannot patent merely substituting one prior art element for another if the substitution can be made with predictable

results. Likewise, combining prior art techniques that are interoperable with respect to one another is generally obvious and not patentable.

In order for a claim to be found invalid based upon a modification or combination of the prior art, there must be reasonable expectation that a person of ordinary skill would have successfully modified or combined the prior art to arrive at the claimed arrangement. This does not mean that it must be certain that a person of ordinary skill would have been successful – the law only requires that the person of ordinary skill in the art would have perceived a reasonable expectation of success in modifying or combining the prior art to arrive at the claimed invention.

In sum, my understanding is that obviousness invalidates claims that merely recite combinations of, or obvious variations of, prior art teachings using understanding and knowledge of one of skill in the art at the time and motivated by the general problem facing the inventor at the time. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of or attempting obvious variations on prior art references in the claimed manner.

Legal Standard for Claiming the Benefit of the Filing Date of an Earlier-Filed Patent Application

I understand that an invention described in a patent may claim the benefit of, or priority to, a prior application filed in the United States or in a foreign country. I understand that, to claim the benefit of an earlier-filed application, the later-filed

application must contain a specific reference to the earlier-filed application. In addition, I understand that the later-filed application must be an application for a patent for an invention which is also disclosed in the prior application. I understand that the disclosure in the prior application and the later-filed application must be sufficient to comply with the written description and enablement requirements of 35 U.S.C. § 112(a), which provides for two requirements: (1) a written description, which must allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed; and (2) enablement, meaning that the patent must teach an ordinary artisan to make and use the invention without undue experimentation. I understand that a patent cannot claim priority to earlier applications if the later patent includes new matter not present in those earlier disclosures. For example, I understand that a claim in a continuation-in-part application is entitled only to the filing date of the continuation-in-part application when the claim recites a feature which was not disclosed or adequately supported by a proper disclosure under 35 U.S.C. 112 in the earlier-filed parent application.

Legal Standard for Claim Construction

I understand that before any invalidity analysis can be properly performed, the scope and meaning of the challenged claims must be determined by claim construction.

I understand that a patent may include two types of claims, independent claims, and dependent claims. I understand that an independent claim stands alone and includes only the limitations it recites. I understand that a dependent claim depends from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to the limitations recited in the claim (or claims) from which it depends.

In comparing the challenged claims to the prior art, I have carefully considered the patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

I understand that to determine how a person of ordinary skill would have understood a claim term, one should look to sources available at the time of the alleged invention that show what a person of skill in the art would have understood disputed claim language to mean. It is my understanding that this may include what is called "intrinsic" evidence as well as "extrinsic" evidence.

I understand that, in construing a claim term, one should primarily rely on intrinsic patent evidence, which includes the words of the claims themselves, the remainder of the patent specification, and the prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient. I understand that extrinsic evidence may include

principles, concepts, terms, and other resources available to those of skill in the art at the time of the invention.

I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else or something more specific. I understand that to determine whether a term has special meaning, the claims, the patent specification, and the prosecution history are particularly important, and may show that the inventor gave a term a particular definition or intentionally disclaimed, disavowed, or surrendered claim scope.

I understand that the claims of a patent define the scope of the rights conferred by the patent. I understand that because the claims point out and distinctly claim the subject matter which the inventors regard as their invention, claim construction analysis must begin with and is focused on the claim language itself. I understand that the context of the term within the claim as well as other claims of the patent can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, how a term is used in one claim can often inform the meaning of the same term in other claims. Differences among claims or claim terms can also be a useful guide in understanding the meaning of particular claim terms.

I understand that a claim term should be construed not only in the context of the particular claim in which the disputed term appears, but in the context of the

entire patent, including the entire specification. I understand that because the specification is a primary basis for construing the claims, a correct construction must align with the specification.

I understand that the prosecution history of the patent as well as art incorporated by reference or otherwise cited during the prosecution history are also highly relevant in construing claim terms. For instance, art cited by or incorporated by reference may indicate how the inventor and others of skill in the art at the time of the invention understood certain terms and concepts. Additionally, the prosecution history may show that the inventors disclaimed or disavowed claim scope, or further explained the meaning of a claim term.

With regard to extrinsic evidence, I understand that all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical dictionaries may indicate how one of skill in the art used or understood the claim terms. However, I understand that extrinsic evidence is considered to be less reliable than intrinsic evidence, and for that reason is generally given less weight than intrinsic evidence.

I understand that in general, a term or phrase found in the introductory words or preamble of the claim, should be construed as a limitation if it recites essential structure or steps, or is necessary to give meaning to the claim. For

instance, I understand preamble language may limit claim scope: (i) if dependence on a preamble phrase for antecedent basis indicates a reliance on both the preamble and claim body to define the claimed invention; (ii) if reference to the preamble is necessary to understand limitations or terms in the claim body; or (iii) if the preamble recites additional structure or steps that the specification identifies as important.

On the other hand, I understand that a preamble term or phrase is not limiting where a challenged claim defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. I understand that to make this determination, one should review the entire patent to gain an understanding of what the inventors claim they invented and intended to encompass in the claims.

I understand that 35 U.S.C. § 112 ¶ 6 created an exception to the general rule of claim construction called a "means plus function" limitation. These types of terms and limitations should be interpreted to cover only the corresponding structure described in the specification, and equivalents thereof. I also understand that a limitation is presumed to be a means plus function limitation if (a) the claim limitation uses the phrase "means for;" (b) the "means for" is modified by functional language; and (c) the phrase "means for" is not modified by sufficient structure for achieving the specified function.

I understand that a structure is considered structurally equivalent to the corresponding structure identified in the specification only if the differences between them are insubstantial. For instance, if the structure performs the same function in substantially the same way to achieve substantially the same result. I further understand that a structural equivalent must have been available at the time of the issuance of the claim.