IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

RADIAN MEMORY SYSTEMS LLC,, Plaintiff, v. SAMSUNG ELECTRONICS, CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC., Defendants.	Case Nos. 2:24-cv-01073-JRG JURY TRIAL DEMANDED

SAMSUNG'S P.R. 3-3 AND 3-4 INVALIDITY CONTENTIONS

I. INTRODUCTION

Defendants Samsung Electronics, Co., Ltd. and Samsung Electronics America, Inc. (collectively, "Samsung") provide these Invalidity Contentions to Radian Memory Systems LLC ("Radian") for the following patents (collectively, "Asserted Patents") and claims (collectively, "Asserted Claims"), which were identified as asserted in Radian's Preliminary Infringement Contentions served on April 9, 2025 ("Infringement Contentions"):

U.S. Patent No.	Asserted Claims
11,544,183 ("'183 Patent")	1, 2, 6, 8, 9, 11-14, and 17-19.
11,709,772 ("'772 Patent")	1-6, 8, 11-13, 15-20, 22, and 25-30.
11,681,614 ("'614 Patent)	1-7, 9-18, 20-25, and 27-30.
11,740,801 ("'801 Patent")	1-4, 6, 9-16, and 21-24.
11,347,656 ("'656 Patent")	1-2, 4-9, 12-15, 19-21, and 23.
11,347,657 ("'657 Patent")	1-4, 8-15, and 18-22.
11,307,995 ("'995 Patent")	1-11, 13-15, 20-21, 27, and 29-30.

II. RESERVATIONS AND EXPLANATIONS

These Invalidity Contentions and accompanying document productions are subject to further revision as follows. Nothing in these contentions constitutes an admission concerning the priority date, conception date, or date of reduction to practice of the Asserted Claims. Samsung

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reserves the right to modify or supplement these Invalidity Contentions, including in response to any positions taken or information disclosed regarding the priority date, conception date, or date of reduction to practice of the Asserted Claims.

This disclosure is directed to invalidity issues only and does not address other defenses or grounds, including but not limited to: claim construction, non-infringement, patent misuse, inequitable conduct, estoppel, waiver, acquiescence, patent exhaustion, unfair competition, unclean hands, express or implied license, or non-statutory defenses of any sort. Samsung reserves all rights with respect to such issues, including but not limited to their position that the Asserted Claims are to be construed in a particular manner and are not infringed.

For prior art patents and prior art publications identified in these Invalidity Contentions, Samsung reserves the right to rely on the public use, offer for sale, sale, and/or actual products embodying the methods and systems described therein uncovered during discovery. Samsung also reserves the right to rely on any related patents and patent applications, foreign patent counterparts and foreign patent applications of U.S. patents identified in these Invalidity Contentions, and U.S. counterparts of foreign patents and foreign patent applications identified in these Invalidity Contentions.

Samsung also contends that the Asserted Patents are invalid under 35 U.S.C. §§ 102 and/or 103. Samsung has applied post-AIA 35 U.S.C. §§ 102 and/or 103 in these contentions because the Asserted Patents were filed after the AIA went into effect and Radian has not established an earlier priority date. However, to the extent that any of the Asserted Patents are deemed to be pre-AIA, Samsung's invalidity contentions apply equally under 35 U.S.C. §§ 102(a), (b), (e), and/or (g), and/or § 103.

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Samsung also reserves the right to rely on any system, public knowledge or use embodying or otherwise incorporating any of the prior art disclosed herein alone or in combination. Samsung further reserves the right to rely on any other documents or references describing any such system, knowledge, or use. Samsung also reserves the right to rely on physical exemplars of these prior art systems (and will make the same available for inspection).

Samsung's Invalidity Contentions are based in part on Samsung's present understanding of the Asserted Claims and Radian's apparent interpretation of these claims as reflected in its Infringement Contentions. By including prior art that anticipates or renders obvious claims based on Radian's apparent or explicit claim interpretations, Samsung is not agreeing that Radian's claim interpretations are correct. Any invalidity analysis depends on claim construction, which is a question of law reserved for the Court. Samsung reserves the right to amend, supplement, or materially modify its Invalidity Contentions in response to any claim construction positions that Radian may take in this case or any claim construction the Court may adopt in this case. Samsung also reserves the right to assert that a claim is indefinite, not enabled, or fails to meet the written description requirement, in response to any additional claim construction positions Radian may take in this case or any further claim construction the Court may adopt in this case.

Samsung contends that Radian appears to be pursuing overly broad constructions of the Asserted Claims in an effort to piece together an infringement claim where none exists and to accuse products that do not practice the claims as properly construed. At the same time, Radian's Infringement Contentions are in many respects too general and vague to discern exactly how Radian contends the accused instrumentalities practice each element of the Asserted Claims. These Invalidity Contentions are not intended to be, and are not, an admission that the Asserted Claims are infringed by any of Samsung's products or technology, that any particular feature or

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aspect of the accused instrumentalities practices any element of the Asserted Claims, or that any of Radian's proposed constructions are supportable or proper. To the extent that any of the prior art references disclose the same functionality or feature of any of the accused instrumentalities, Samsung reserves the right to argue that said feature or functionality does not practice the Asserted Claims, and to argue, in the alternative, that if said feature or functionality is found to practice the Asserted Claims, then the prior art reference demonstrates that that feature or functionality is not novel, is obvious, or is not patentable.

The accompanying invalidity claim charts provide examples of prior art that discloses, either expressly or inherently, every limitation of certain claims and/or teachings, suggestions and motivations through which a POSITA at the time of the alleged invention would have considered the limitations obvious in view of the state of the art at the time, the differences between the claimed invention and the state of the art, and the foreseeability from a technical perspective and/or marketing and/or natural and expected evolution of the art. Where Samsung cites to a particular figure in a reference, the citation should be understood to encompass the caption and description of the figure and any text relating to the figure. Conversely, where Samsung cites to particular text referring to a figure, the citation should be understood to include the figure as well. As discovery progresses and the scope and focus of the liability issues become clearer, Samsung may rely on uncited portions of the prior art.

Samsung reserves the right to revise its contentions concerning the invalidity of the Asserted Claims, which may change depending on discovery taken in the case, the Court's construction of the Asserted Claims, any findings as to the priority date of the Asserted Claims, and/or positions that Radian or expert witness(es) may take concerning claim construction, infringement, and/or invalidity issues.

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Samsung may rely on Radian's or any inventor's admissions concerning the scope of prior art relevant to the Asserted Patents; the patent prosecution histories for the Asserted Patents; any deposition testimony of the named inventors on the Asserted Patents; and the papers filed and any evidence submitted by Radian in connection with this litigation.

Prior art not included in this disclosure, whether known or not known to Samsung, may become relevant. In particular, Samsung is currently unaware of the extent, if any, to which Radian will contend that limitations of the Asserted Patents are not disclosed in the prior art identified by Samsung. To the extent such an issue arises, Samsung reserves the right to identify other references that would render obvious the allegedly missing limitation(s) of the disclosed device or method. Further, because Samsung has not yet completed its search for or analysis of relevant prior art, Samsung reserves the right to revise, amend, and/or supplement the information provided herein, including identifying, charting, and relying on additional references, should Samsung's further search and analysis yield additional information or references, consistent with the Federal Rules of Civil Procedure. Radian also has a duty to produce to Samsung all relevant documents from other proceedings involving the patents related to the Asserted Patents or their subject matter, including but not limited to all prior art invalidity contentions and expert reports on invalidity among other relevant items.

Additionally, because third-party discovery is not yet begun, Samsung reserves the right to present additional items of prior art under 35 U.S.C. §§ 102 and/or 103, to the extent that such discovery or investigation yields information forming the basis for such invalidity. For example, Samsung plans to issue subpoenas to (and has received and expects to receive, voluntarily or subject to subpoenas, information from) third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed below and/or additional prior

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art. These third parties include, without limitation, the authors, inventors, vendors, or assignees of the references listed in these disclosures.

Samsung further reserve the right to modify or add additional contentions in the event that Radian provides amended infringement contentions and to the extent the Court orders or allows Radian to amend its infringement contentions.

Pursuant to the Scheduling Order, and in light of Radian's Infringement Contentions and accompanying claim chart, Samsung lists in these Invalidity Contentions the prior art now known to it that it contends anticipates or renders obvious the Asserted Claims. Although Samsung has identified at least one disclosure of a limitation for each prior art reference, each and every disclosure of the same limitation in the same reference is not necessarily identified. In an effort to focus the issues, Samsung's citations are only to representative portions of an identified reference, even where a reference may contain additional support for a particular claim limitation. POSITAs generally read an item of prior art as a whole and in the context of other publications and literature. Thus, to understand and interpret any specific statement or disclosure within a prior art reference, such persons would rely on other information within the reference, along with other publications and their general scientific knowledge. Samsung may rely on uncited portions of the prior art references and on other publications and expert testimony to provide context, and as aids to understanding and interpreting the portions that are cited.

Samsung incorporates in these Invalidity Contentions, in full, all prior art references cited in the Asserted Patents and their prosecution histories.

Subject to Samsung's reservation of rights, Samsung identifies each item of prior art that anticipates and/or renders obvious the Asserted Claims. The patents/applications, publications,

and systems identified are also relevant to show the state of the art and reasons and motivations for making improvements, additions, and combinations.

III. PRIORITY DATE OF THE ASSERTED PATENTS AND CLAIMS

Radian asserts the following priority dates for the Asserted Claims of the Asserted Patents:

- "'183 Patent is entitled to a priority date of January 28, 2013"
- "'772 Patent is entitled to a priority date of October 7, 2013"
- "'614 Patent is entitled to a priority date of October 7, 2013"
- "'801 Patent is entitled to a priority date of October 13, 2014"
- "'657 Patent are entitled to a priority date of October 13, 2014: claims 1–4, 8, 10–15, 18; and the following asserted claims of the '657 Patent are entitled to a priority date of July 31, 2015: claims 9, 19–22."
- "[C]laim 20 of the '656 Patent is entitled to a priority date of July 31, 2015, and that each of the other asserted claims of the '656 Patent is entitled to a priority date of October 13, 2014"
- "[C]laims 27 and 29 of the '995 Patent are entitled to a priority date of July 31, 2015, and that each of the other asserted claims of the '995 Patent is entitled to a priority date of October 13, 2014"

(Infringement Contentions, pgs. 5-7).

It is Radian's burden to show entitlement to its asserted priority date, and Samsung asserts that Radian has failed to meet that burden. *See Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327 (Fed. Cir. 2008); *see also, In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1376 (Fed. Cir. 2016) ("[A] patentee bears the burden of establishing that its claimed invention is entitled to an earlier priority date than an asserted prior art reference."). For example, Radian has failed to show that Asserted Claims in continuation patents are supported by the parent applications to which they all ultimately claim priority. Indeed, Samsung's Interrogatory No. 9 required Radian to identify, among other things, the priority date to which each Asserted Claim is allegedly entitled, as well as Radian's "basis for asserting such earlier priority date, including by identifying the

supporting disclosure in each earlier application upon which you are asserting priority on an element-by-element basis in each Asserted Claim." Radian has yet to meaningfully answer this Interrogatory, and has not provided the basis for asserting an earlier priority date of the alleged supporting disclosure in each earlier application upon which you are asserting priority on an element-by-element basis in each Asserted Claim. Samsung reserves the right to supplement, modify, or otherwise respond should Radian be allowed to identify the basis for contending that the Asserted Patents are entitled to a priority date earlier than the filing date.

Further, Samsung contends that the Asserted Patents are not entitled to a priority date earlier than the filing date. For instance, the applications to which the Asserted Patents claim priority lack written description support for at least the limitations identified in Section VII.B.

Samsung has focused on prior art that predates the priority dates Radian claims in its Infringement Contentions. Samsung reserves the right to amend these Invalidity Contentions with additional prior art and/or with additional charts of the art if Radian alleges earlier or later priority dates.

In addition, Radian has not identified a date of conception or reduction to practice for the '183 Patent. Radian has objected to Samsung's Interrogatory No. 10 – which seeks information regarding conception and reduction to practice – as "premature." Radian provides a conclusory assertion "that Andrey V. Kuzmin, Mike Jadon, and Richard M. Mathews conceived of the claimed inventions of the '183 Patent between late 2011 and early 2012" and that "[t]o the extent Kuzmin, Jadon, and Mathews did not actually reduce the inventions to practice prior to January 28, 2013, they constructively did so by January 28, 2013, by filing U.S. Provisional Application No. 61/757,464." However, Radian does not identify the basis for this assertion or the specific information or portions of documents that corroborate any alleged conception or reduction to

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practice dates. Moreover, the applications to which the Asserted Patents claim priority do not demonstrate constructive reduction to practice at least because they lack written description support for at least the limitations identified in Section VII.B. Samsung therefore also reserves its right to amend its Invalidity Contentions if Radian is permitted to allege earlier dates of conception for the '183 Patent, or if Radian does not meet its burden to prove the priority dates it asserts.

IV. PRIOR ART REFERENCES

Samsung identifies the NVMe Zoned Namespaces (ZNS) specification and products implementing the ZNS specification that were on-sale and/or were prior inventions that anticipate or renders obvious the asserted claims of the Asserted Patents under Radian's allegations. *See Peters v. Active Manufacturing Co.*, 129 U.S. 530, 537 (1889); *Evans Cooling Systems, Inc. v. General Motors Corp.*, 125 F.3d 1448, 1450 (Fed. Cir. 1997); *Vanmoor v. Wal-Mart Stores*, 201 F.3d 1363, 1365 (Fed. Cir. 2000). Radian has not met its burden to show that the Asserted Patents are entitled to a priority date earlier than their filing date. For instance, Revision 1.1 of the ZNS specification, which is dated May 18, 2021, predates the filing date of the '772, '614, '801, '656, '657, and '995 Patents. Moreover, earlier drafts and presentations of the ZNS specification existed as early as 2020, and these drafts predate the filing date of the '183 Patent.[1] Radian has also admitted to selling or offering for sale products that are in "compliance with the Zone Namespaces (ZNS) specification from NVM Express industry standards organization" more than one year before the filing date of the earliest Asserted Patent. Radian has alleged that Samsung's Accused Products infringe the Asserted Patents because they are compliant with the ZNS specification. While Samsung disputes Radian's allegation, to the extent they are credited the Asserted Patents

[1] *See, e.g.,* https://blog.westerndigital.com/nvme-spec-ratification-zns-ssd/ (article describing NVM Express 1.4 Ratified TP as available for download in June 2020); https://lwn.net/Articles/823154/ (same); https://blocksandfiles.com/2020/06/26/storage-salade-nicoise-with-teradata-in-the-cloud-wd-zoned-ssds-and-more/ (same).

are invalid because "that which infringes if later would anticipate if earlier." *Peters*, 129 U.S. at 537.

Samsung identifies the following prior art now known to Samsung that anticipates and/or renders obvious the Asserted Claims under 35 U.S.C. §§ 102 and 103. At this time, Samsung contends that the prior art references described below render obvious one or more of the Asserted Claims. These prior art references also provide a description of the level of skill in the art and provide background information showing the knowledge of a person of skill in the art. Samsung reserves the right to rely on these references for those purposes.

Samsung additionally incorporates by reference all prior art references cited on the face of the Asserted Patents, each related patent, and each foreign counterpart. Samsung further incorporates by reference all prior art references identified in the file histories of the same. Samsung reserves the right to rely upon foreign counterparts of the U.S. Patents identified in these Invalidity Contentions; U.S. counterparts of foreign patents and foreign patent applications identified in these Invalidity Contentions; U.S. and foreign patents and patent applications corresponding to articles and publications identified in these Invalidity Contentions; and any systems, products, or prior inventions related to any references identified in these Invalidity Contentions.

In these Invalidity Contentions, including the exhibits, any citation to a printed publication or other reference describing a prior art system should also be construed to include a reference to the prior art system itself.

A subset of the Asserted Patents has asserted claims with limitations that are substantially similar to limitations of other asserted claims of that Asserted Patent. A subset of the Asserted Patents also has asserted claims with limitations that are substantially similar to limitations of

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asserted claims on other Asserted Patents. For example, many of the asserted claims recite a "controller" for flash memory organized into subdivisions or zones, where the control includes logic to receive and complete certain commands direct to the subdivisions or zones, and logic to generate and track certain metadata for the subdivisions or zones, etc. Samsung reserves the right to rely on references and obviousness arguments charted for a limitation of one asserted claim when invalidating another asserted claim with a similar limitation.

Similarly, these Invalidity Contentions, including the exhibits, may contain citations to certain embodiments disclosed in a prior art reference but not to all embodiments disclosed in that reference. Samsung reserves the right to rely on variant embodiments in cited prior art references even if those variant embodiments are not otherwise specifically cited.

A. Prior Art Patent Publications

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
2004/0083335	October 14, 2003	April 29, 2004	USA
2004/0093457	November 12, 2002	May 13, 2004	USA
2004/0250043	June 9, 2003	January 3, 2006	USA
2005/0144360	December 30, 2003	June 30, 2005	USA
2005/0144367	December 16, 2004	June 30, 2005	USA
2005/0235098	February 2, 2005	October 20, 2005	USA
2007/0233941	April 3, 2007	October 4, 2007	USA
2007/0183198	March 28, 2006	August 9, 2007	USA
2007/0245070	April 17, 2007	October 18, 2007	USA
2007/0260845	April 24, 2007	November 8, 2007	USA
2008/0052446	February 9, 2007	February 28, 2008	USA
2008/0189485	August 3, 2007	August 7, 2008	USA
2008/0279005	May 11, 2007	November 13, 2008	USA
2008/0288712	April 25, 2007	November 20, 2008	USA
2009/0157964	December 11, 2008	June 18, 2009	USA
2009/0172257	April 8, 2008	July 2, 2009	USA
2009/0172267	December 24, 2008	July 2, 2009	USA
2009/0172308	April 8, 2008	July 2, 2009	USA
2009/0182975	January 11, 2008	July 16, 2009	USA

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
2009/0271562	April 25, 2008	October 29, 2009	USA
2009/0327804	May 12, 2009	December 31, 2009	USA
2010/0023677	March 2, 2009	January 28, 2010	USA
2010/0042798	August 13, 2008	February 18, 2010	USA
2010/0049908	December 30, 2003	February 25, 2010	USA
2010/0082917	December 29, 2008	April 1, 2010	USA
2010/0131699	November 26, 2008	May 27, 2010	USA
2010/0153616	December 16, 2008	June 17, 2010	USA
2010/0161886	November 6, 2009	June 24, 2010	USA
2010/0169553	September 24, 2009	July 1, 2010	USA
2010/0228928	March 2, 2009	September 9, 2010	USA
2010/0228940	March 4, 2009	September 9, 2010	USA
2010/0241793	March 26, 2009	September 23, 2010	USA
2011/0022778	May 6, 2009	January 27, 2011	USA
2011/0107016	October 29, 2009	May 5, 2011	USA
2011/0153911	December 18, 2009	June 23, 2011	USA
2011/0161560	December 31, 2009	June 30, 2011	USA
2011/0161565	February 22, 2010	June 30, 2011	USA
2011/0161784	December 30, 2009	June 30, 2011	USA
2011/0191531	April 18, 2011	August 4, 2011	USA
2011/0225346	March 10, 2010	September 15, 2011	USA
2011/0264884	March 23, 2011	October 27, 2011	USA
2011/0271032	July 27, 2010	November 3, 2011	USA
2011/0302477	June 3, 2010	December 8, 2011	USA
2011/0314204	March 21, 2011	December 22, 2011	USA
2012/0303931	March 4, 2009	November 29, 2012	USA
2012/0054419	July 11, 2011	March 1, 2012	USA
2012/0072807	November 28, 2011	March 22, 2012	USA
2012/0096217	October 15, 2010	April 19, 2012	USA
2012/0166715	December 22, 2011	June 28, 2012	USA
2012/0191906	April 5, 2012	July 26, 2012	USA
2012/0221784	November 23, 2010	August 30, 2012	USA
2012/0246393	March 15, 2012	September 27, 2012	USA
2012/0254636	February 22, 2012	October 4, 2012	USA
2012/0284587	July 2, 2012	November 8, 2012	USA
2012/0290779	July 27, 2012	November 15, 2012	USA
2012/0311232	May 31, 2011	December 6, 2012	USA

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
2012/0311244	June 8, 2012	December 6, 2012	USA
2012/0311245	August 9, 2012	December 6, 2012	USA
2013/0007511	June 20, 2011	January 3, 2013	USA
2013/0021846	April 25, 2012	January 24, 2013	USA
2013/0024608	July 18, 2012	January 24, 2013	USA
2013/0036253	August 3, 2011	February 7, 2013	USA
2013/0054881	August 31, 2011	February 28, 2013	USA
2013/0073787	September 16, 2011	March 21, 2013	USA
2013/0145085	December 28, 2012	June 6, 2013	USA
2013/0159601	December 20, 2011	June 20, 2013	USA
2013/0166822	December 23, 2011	June 27, 2013	USA
2013/0166825	September 14, 2012	June 27, 2013	USA
2013/0173841	February 25, 2013	July 4, 2013	USA
2013/0179624	January 9, 2012	July 11, 2013	USA
2013/0205102	October 10, 2012	August 8, 2013	USA
2013/0227246	September 11, 2012	August 29, 2013	USA
2013/0275650	December 14, 2011	October 17, 2013	USA
2013/0304872	July 11, 2013	November 14, 2013	USA
2014/0032817	July 27, 2012	January 30, 2014	USA
2014/0047159	August 10, 2012	February 13, 2014	USA
2014/0068216	March 8, 2012	March 6, 2014	USA
2014/0156966	November 30, 2012	June 5, 2014	USA
2014/0164674	February 18, 2013	June 12, 2014	USA
2014/0207997	January 21, 2013	July 24, 2014	USA
2021/0182166	December 12, 2019	June 17, 2021	USA
2022/0100390	December 25, 2019	March 31, 2022	USA
9,423,970	December 30, 2013	August 23, 2016	USA
8,244,960	January 5, 2009	August 14, 2012	USA
5,404,485	March 8, 1993	April 4, 1995	USA
6,578,127	October 1, 1998	June 10, 2003	USA
6,983,355	June 9, 2003	January 3, 2006	USA
7,139,864	December 30, 2003	November 21, 2006	USA
7,409,489	August 3, 2005	August 5, 2008	USA
7,552,272	October 10, 2006	June 23, 2009	USA
7,647,470	August 19, 2005	January 12, 2010	USA
7,739,444	December 26, 2006	June 15, 2010	USA
7,913,032	April 25, 2007	March 22, 2011	USA

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
7,917,686	December 26, 2006	March 29, 2011	USA
7,984,233	May 5, 2010	July 19, 2011	USA
8,095,765	March 4, 2009	January 10, 2012	USA
8,156,303	October 18, 2010	April 10, 2012	USA
8,166,233	July 24, 2009	April 24, 2012	USA
8,214,583	May 7, 2010	July 3, 2012	USA
8,244,960	January 5, 2009	August 14, 2012	USA
8,301,826	October 30, 2009	October 30, 2012	USA
8,301,861	April 29, 2010	October 30, 2012	USA
8,386,700	December 27, 2007	February 26, 2013	USA
2011/0225347	March 10, 2010	May 7, 2013	USA
8,621,137	April 8, 2008	July 2, 2009	USA
8,751,731	August 6, 2012	June 10, 2014	USA
8,745,309	August 3, 2007	August 7, 2008	USA
8,838,876	October 13, 2008	September 16, 2014	USA
8,898,373	June 29, 2011	November 25, 2014	USA
9,134,918	December 31, 2009	September 15, 2015	USA
9,141,526	September 14, 2011	September 22, 2015	USA
9,239,781	February 7, 2012	January 19, 2016	USA
9,323,662	March 11, 2013	April 26, 2016	USA
9,558,112	May 8, 2012	January 31, 2017	USA
9,652,376	February 14, 2013	May 16, 2017	USA
9,671,962	November 30, 2012	June 6, 2017	USA
9,996,274	September 23, 2011	July 20, 2017	USA
2374134	January 4, 2010	April 23, 2014	Europe
2005/018490	June 26, 2003	January 20, 2005	Japan
2005/038655	July 17, 2003	February 10, 2005	Japan
2005/209184	December 27, 2004	August 4, 2005	Japan
2005107600	September 26, 2003	April 21, 2005	Japan
2007-249469	March 15, 2006	September 27, 2007	Japan
2008/158908	December 25, 2006	July 10, 2008	Japan
2008/176606	January 19, 2007	July 31, 2008	Japan
2010-0058678	October 2, 2008	June 3, 2010	Korea
4173410	June 26, 2003	October 29, 2008	Japan
10-0868674	October 30, 2006	November 13, 2008	Korea
10-0914646	August 31, 2002	August 28, 2009	Korea
10-0932096	July 15, 2009	December 16, 2009	Korea

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
10-1107288	December 17, 2003	January 20, 2012	Korea
10-1146059	July 31, 2007	May 14, 2012	Korea
10-1155542	October 11, 2010	June 18, 2012	Korea
10-1185617	April 4, 2006	September 24, 2012	Korea
10-1438716	August 8, 2012	September 11, 2014	Korea
10-1464199	December 19, 2007	November 21, 2014	Korea
10-2004-0085422	March 31, 2003	October 8, 2004	Korea
10-2008-0025999	September 19, 2006	March 24, 2008	Korea
10-2008-0031787	April 4, 2008	October 8, 2009	Korea
10-2009-0106221	April 4, 2008	October 8, 2009	Korea
10-2010-0034743	January 8, 2010	April 1, 2010	Korea
10-2010-0037860	October 2, 2008	April 12, 2010	Korea
10-2010-0098848	October 11, 2010	April 19, 2012	Korea
10-2010-0139149	November 24, 2010	December 31, 2010	Korea
10-2011-0046880	October 29, 2009	December 23, 2011	Korea
10-2011-0069049	April 4, 2011	December 8, 2016	Korea
10-2012-0045421	October 29, 2010	June 16, 2017	Korea
10-2014-0035916	May 11, 2012	March 24, 2014	Korea
10-2014-0038110	September 20, 2012	March 28, 2014	Korea
2007/0066539	December 22, 2005	June 27, 2007	Korea
2008/082996	December 19, 2007	July 10, 2008	WO
2013/022915	August 8, 2012	February 14, 2013	WO
5,568,423	April 14, 1995	October 22, 1996	USA
5,652,857	January 29, 1996	July 29, 1997	USA
5,860,082	March 28, 1996	January 12, 1999	USA
5,933,840	May 19, 1997	August 3, 1999	USA
5,963,977	October 9, 1997	October 5, 1999	USA
6,134,631	October 31, 1996	October 17, 2000	USA
6,381,668	March 21, 1997	April 30, 2002	USA
6,892,287	July 31, 2002	May 10, 2005	USA
7,012,835	October 3, 2003	March 14, 2006	USA
7,096,378	August 29, 2002	August 22, 2006	USA
7,120,729	October 14, 2003	October 10, 2006	USA
7,339,823	October 10, 2006	March 4, 2008	USA
7,404,031	September 7, 1989	July 23, 1991	USA
7,406,563	February 8, 2005	July 29, 2008	USA
7,519,869	December 8, 2005	April 14, 2009	USA

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
7,552,272	October 10, 2006	June 23, 2009	USA
7,555,628	August 15, 2006	June 30, 2009	USA
7,581,078	September 10, 2007	August 25, 2009	USA
7,610,437	August 2, 2006	October 27, 2009	USA
7,631,138	December 30, 2003	December 8, 2009	USA
7,702,846	March 9, 2006	April 20, 2010	USA
7,702,948	July 13, 2004	April 20, 2010	USA
7,710,777	December 14, 2007	May 4. 2010	USA
7,747,813	September 7, 2007	June 29, 2010	USA
7,752,381	May 24, 2005	July 6, 2010	USA
7,801,561	September 28, 2006	September 21, 2010	USA
7,809,900	September 7, 2007	October 5, 2010	USA
7,818,489	November 15, 2007	October 19, 2010	USA
7,836,244	November 1, 2007	November 16, 2010	USA
7,861,122	January 27, 2006	December 28, 2010	USA
7,877,540	December 13, 2005	January 25, 2011	USA
7,904,619	September 7, 2007	March 8, 2011	USA
7,941,692	December 31, 2007	May 10, 2011	USA
7,962,688	September 2, 2009	June 14, 2011	USA
7,970,983	October 14, 2007	June 28, 2011	USA
7,984,233	May 5, 2010	July 19, 2011	USA
7,991,944	February 6, 2008	August 2, 2011	USA
8,000,144	March 26, 2010	August 16, 2011	USA
8,001,318	October 28, 2008	August 16, 2011	USA
8,024,545	October 20, 2008	September 20, 2011	USA
8,046,524	September 28, 2007	October 25, 2011	USA
8,055,833	December 15, 2006	November 8, 2011	USA
8,065,471	September 2, 2009	November 22, 2011	USA
8,065,473	June 10, 2010	November 22, 2011	USA
8,068,365	December 8, 2008	November 29, 2011	USA
8,069,284	May 15, 2009	November 29, 2011	USA
8,072,463	October 4, 2006	December 6, 2011	USA
8,074,022	September 28, 2007	December 6, 2011	USA
8,082,389	December 30, 2009	December 20, 2011	USA
8,086,790	March 3, 2011	December 27, 2011	USA
8,099,570	February 22, 2008	January 17, 2012	USA
8,099,581	June 30, 2009	January 17, 2012	USA

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
8,099,632	September 28, 2007	January 17, 2012	USA
8,285,918	December 11, 2009	October 9, 2012	USA
8,341,339	June 14, 2010	December 25, 2012	USA
8,347,042	May 28, 2009	January 1, 2013	USA
8,402,249	October 12, 2010	March 19, 2013	USA
8,539,197	June 29, 2010	September 17, 2013	USA
8,572,331	October 30, 2008	October 29, 2013	USA
8,601,202	August 26, 2009	December 3, 2013	USA
8,626,989	February 2, 2011	January 7, 2014	USA
8,645,634	January 16, 2009	February 4, 2014	USA
8,886,899	September 20, 2010	November 11, 2014	USA
8,898,410	February 20, 2013	November 25, 2014	USA
9,063,844	August 30, 2012	June 23, 2015	USA
9,134,918	December 31, 2009	September 15, 2015	USA
9,171,585	November 26, 2013	October 27, 2015	USA
9,176,864	May 10, 2012	November 3, 2015	USA
9,229,854	October 7, 2013	January 5, 2016	USA
9,335,939	July 11, 2012	May 10, 2016	USA
9,348,749	March 14, 2014	May 24, 2016	USA
9,378,149	August 29, 2014	June 28, 2016	USA
9,383,926	May 27, 2014	July 5, 2016	USA
9,400,749	January 28, 2016	July 26, 2016	USA
9,432,298	December 10, 2012	August 30, 2016	USA
9,489,296	October 17, 2012	November 8, 2016	USA
9,519,578	November 25, 2015	December 13, 2016	USA
9,542,118	October 12, 2015	January 10, 2017	USA
9,569,320	December 27, 2012	February 14, 2017	USA
9,588,904	February 25, 2016	March 7, 2017	USA
9,652,376	February 14, 2013	May 16, 2017	USA
9,696,917	June 30, 2014	July 4, 2017	USA
9,710,377	November 8, 2016	July 18, 2017	USA
9,727,454	August 22, 2014	August 8, 2017	USA
9,740,439	December 23, 2011	August 22, 2017	USA
9,785,572	March 18, 2016	October 10, 2017	USA
9,846,541	March 12, 2015	December 19, 2017	USA
10,063,379	June 16, 2017	August 28, 2018	USA
10,445,229	June 13, 2017	October 15, 2019	USA

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
10,552,058	July 15, 2016	February 4, 2020	USA
10,552,085	July 15, 2016	February 4, 2020	USA
10,642,505	September 8, 2015	May 5, 2020	USA
10,642,748	August 29, 2017	May 5, 2020	USA
10,838,853	June 16, 2017	November 17, 2020	USA
10,884,915	June 16, 2017	January 5, 2021	USA
10,915,458	February 3, 2020	February 9, 2021	USA
10,956,082	December 4, 2019	March 23, 2021	USA
10,977,188	February 3, 2020	April 13, 2021	USA
10,983,907	March 28, 2020	April 20, 2021	USA
10,996,863	March 27, 2020	May 4, 2021	USA
11,003,586	February 5, 2020	May 11, 2021	USA
11,023,315	October 3, 2019	June 1, 2021	USA
11,023,386	February 5, 2020	June 1, 2021	USA
11,023,387	February 5, 2020	June 1, 2021	USA
11,048,643	March 3, 2020	June 29, 2021	USA
11,074,175	April 6, 2020	July 27, 2021	USA
11,080,181	March 24, 2021	August 3, 2021	USA
11,086,789	March 25, 2021	August 10, 2021	USA
11,100,006	April 6, 2020	August 24, 2021	USA
11,118,457	October 21, 2019	September 14, 2021	USA
11,130,169	February 6, 2020	September 28, 2021	USA
11,163,492	February 13, 2020	November 2, 2021	USA
11,175,984	December 9, 2019	November 16, 2021	USA
11,188,457	September 13, 2019	November 30, 2021	USA
11,216,365	March 28, 2020	January 4, 2022	USA
11,221,959	March 3, 2020	January 11, 2022	USA
11,221,960	March 3, 2020	January 11, 2022	USA
11,221,961	March 27, 2020	January 11, 2022	USA
11,226,903	March 3, 2020	January 18, 2022	USA
11,269,781	February 19, 2020	March 8, 2022	USA
11,275,695	February 19, 2020	March 15, 2022	USA
11,307,995	October 20, 2021	April 19, 2022	USA
11,314,636	January 24, 2020	April 26, 2022	USA
11,321,237	February 3, 2020	May 3, 2022	USA
11,334,479	February 5, 2020	May 17, 2022	USA
11,347,638	August 19, 2020	May 31, 2022	USA

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
11,347,639	August 28, 2020	May 31, 2022	USA
11,354,234	August 28, 2020	June 7, 2022	USA
11,354,235	August 28, 2020	June 7, 2022	USA
11,416,413	December 27, 2021	August 16, 2022	USA
11,449,436	December 27, 2021	September 20, 2022	USA
11,487,656	December 28, 2021	November 1, 2022	USA
11,487,657	December 28, 2021	November 1, 2022	USA
11,537,528	December 27, 2021	December 27, 2022	USA
11,537,529	September 1, 2022	December 27, 2022	USA
11,544,200	September 1, 2022	January 3, 2023	USA
2003/0028733	June 13, 2002	February 6, 2003	USA
2003/0037071	August 3, 2001	February 20, 2003	USA
2003/0065866	October 1, 2001	April 3, 2003	USA
2003/0165076	September 27, 2002	September 4, 2003	USA
2003/0188032	March 29, 2002	October 2, 2003	USA
2004/0083335	October 14, 2003	April 29, 2004	USA
2005/0073844	January 24, 2003	April 7, 2005	USA
2005/0073884	October 3, 2003	April 7, 2005	USA
2005/0141313	August 13, 2004	June 30, 2005	USA
2005/0144413	December 30, 2003	June 30, 2005	USA
2005/0160227	January 21, 2004	July 21, 2005	USA
2005/0195635	March 8, 2004	September 8, 2005	USA
2006/0004957	March 16, 2005	January 5, 2006	USA
2006/0022171	January 21, 2005	February 2, 2006	USA
2006/0106972	November 15, 2004	May 18, 2006	USA
2006/0184719	February 16, 2005	August 17, 2006	USA
2006/0221713	March 31, 2005	January 17, 2012	USA
2007/0019481	April 20, 2006	January 25, 2007	USA
2007/0033325	October 25, 2005	February 8, 2006	USA
2007/0046681	August 16, 2006	March 1, 2007	USA
2007/0058431	December 29, 2005	March 15, 2007	USA
2007/0091497	December 8, 2005	April 26, 2007	USA
2007/0136555	December 13, 2005	June 14, 2007	USA
2007/0143569	December 19, 2005	June 21, 2007	USA
2007/0168321	April 27, 2005	July 19, 2007	USA
2007/0233939	March 29, 2007	October 4, 2007	USA
2007/0258162	April 10, 2007	November 8, 2007	USA

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2007/0260811	May 8, 2006	November 8, 2007	USA
2007/0260841	May 2, 2006	November 8, 2007	USA
2007/0276283	May 15, 2006	November 29, 2007	USA
2007/0283428	September 7, 2006	December 6, 2007	USA
2007/0294496	June 27, 2006	December 20, 2007	USA
2008/0005502	September 6, 2007	January 3, 2008	USA
2008/0034153	October 11, 2007	February 7, 2008	USA
2008/0082596	September 29, 2006	April 3, 2008	USA
2008/0126685	September 7, 2007	May 29, 2008	USA
2008/0126690	February 5, 2007	May 29, 2008	USA
2008/0126719	September 7, 2007	May 29, 2008	USA
2008/0126720	September 7, 2007	May 29, 2008	USA
2008/0126724	September 7, 2007	May 29, 2008	USA
2008/0147964	October 4, 2007	June 19, 2008	USA
2008/0155204	December 21, 2006	June 26, 2008	USA
2008/0189485	August 3, 2007	August 7, 2008	USA
2008/0201517	December 20, 2005	August 21, 2008	USA
2008/0209114	April 11, 2008	August 28, 2008	USA
2008/0219057	March 7, 2007	September 11, 2008	USA
2008/0250202	June 13, 2008	October 9, 2008	USA
2008/0256287	February 4, 2008	October 16, 2008	USA
2008/0320476	June 24, 2008	December 25, 2008	USA
2009/0036163	August 2, 2007	February 5, 2009	USA
2009/0044190	September 28, 2007	February 12, 2009	USA
2009/0046533	July 26, 2005	February 19, 2009	USA
2009/0083478	September 24, 2008	March 26, 2009	USA
2009/0089482	September 28, 2007	April 2, 2009	USA
2009/0089490	September 26, 2008	April 2, 2009	USA
2009/0119529	February 11, 2008	May 7, 2009	USA
2009/0138671	November 28, 2007	May 28, 2009	USA
2009/0144497	May 18, 2007	June 4, 2009	USA
2009/0172219	December 30, 2007	July 2, 2009	USA
2009/0172246	December 26, 2007	July 2, 2009	USA
2009/0172250	December 28, 2007	July 2, 2009	USA
2009/0172257	April 8, 2008	July 2, 2009	USA
2009/0172286	December 31, 2007	July 2, 2009	USA
2009/0172499	April 8, 2008	July 2, 2009	USA

Prior Art	Effective Filing Date	Publication / Issue Date	Country of Origin
2009/0182964	January 1, 2008	July 16, 2009	USA
2009/0198946	April 22, 2008	August 6, 2009	USA
2009/0210616	February 11, 2009	August 20, 2009	USA
2009/0210636	February 11, 2009	August 20, 2009	USA
2009/0216992	February 26, 2008	August 27, 2009	USA
2009/0240903	March 20, 2008	September 24, 2009	USA
2009/0254689	February 11, 2009	October 8, 2009	USA
2009/0254705	April 7, 2008	October 8, 2009	USA
2009/0271562	April 25, 2008	October 29, 2009	USA
2009/0292839	May 15, 2009	November 26, 2009	USA
2009/0300015	June 2, 2008	December 3, 2009	USA
2009/0327602	June 30, 2008	December 31, 2009	USA
2010/0011085	August 28, 2008	January 14, 2010	USA
2010/0011186	June 30, 2009	January 14, 2010	USA
2010/0023566	September 22, 2008	January 28, 2010	USA
2010/0026773	July 31, 2008	February 4, 2010	USA
2010/0030946	October 9, 2008	February 4, 2010	USA
2010/0042655	August 18, 2008	February 18, 2010	USA
2010/0077136	November 6, 2007	March 25, 2010	USA
2010/0083050	March 13, 2008	April 1, 2010	USA
2010/0106695	October 24, 2008	April 29, 2010	USA
2010/0106734	October 24, 2008	April 29, 2010	USA
2010/0115172	October 28, 2009	May 6, 2010	USA
2010/0161882	August 20, 2009	June 24, 2010	USA
2010/0162012	March 2, 2010	June 24, 2010	USA
2010/0182838	March 26, 2010	July 22, 2010	USA
2010/0191779	January 27, 2009	July 29, 2010	USA
2010/0211737	February 23, 2010	August 19, 2010	USA
2010/0241866	March 28, 2008	September 23, 2010	USA
2010/0250837	May 28, 2008	September 30, 2010	USA
2010/0262761	August 7, 2009	October 14, 2010	USA
2010/0262762	August 7, 2009	October 14, 2010	USA
2010/0262765	April 7, 2010	October 14, 2010	USA
2010/0262773	August 7, 2009	October 14, 2010	USA
2010/0281230	April 29, 2009	November 4, 2010	USA
2010/0287217	April 7, 2010	November 11, 2010	USA
2010/0287327	February 15, 2010	November 11, 2010	USA

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2010/0287332	April 30, 2010	November 11, 2010	USA
2010/0312976	June 3, 2009	December 9, 2010	USA
2010/0325351	June 9, 2010	December 23, 2010	USA
2010/0329011	February 5, 2010	December 30, 2010	USA
2011/0022784	February 10, 2009	January 27, 2011	USA
2011/0033548	August 3, 2010	February 10, 2011	USA
2011/0035536	March 26, 2010	February 10, 2011	USA
2011/0040927	December 21, 2009	February 17, 2011	USA
2011/0041039	August 11, 2009	February 17, 2011	USA
2011/0055445	March 15, 2010	March 3, 2011	USA
2011/0066792	February 4, 2009	March 17, 2011	USA
2011/0066789	September 16, 2009	March 17, 2011	USA
2011/0082967	October 5, 2010	April 7, 2011	USA
2011/0125956	June 24, 2010	May 26, 2011	USA
2011/0126045	October 8, 2010	May 26, 2011	USA
2011/0153817	December 21, 2010	June 23, 2011	USA
2011/0153911	December 18, 2009	June 23, 2011	USA
2011/0153917	February 9, 2010	June 23, 2011	USA
2011/0161560	December 31, 2009	June 30, 2011	USA
2011/0161784	December 30, 2009	June 30, 2011	USA
2011/0167199	July 26, 2010	July 7, 2011	USA
2011/0197014	March 29, 2010	August 11, 2011	USA
2011/0197023	March 18, 2009	August 11, 2011	USA
2011/0217977	March 1, 2011	September 8, 2011	USA
2011/0231623	March 17, 2010	September 22, 2011	USA
2011/0231730	August 19, 2010	September 22, 2011	USA
2011/0238892	December 30, 2010	September 29, 2011	USA
2011/0238943	March 29, 2010	September 29, 2011	USA
2011/0255339	June 29, 2011	October 20, 2011	USA
2011/0258388	June 29, 2011	October 20, 2011	USA
2011/0264843	April 22, 2010	October 27, 2011	USA
2011/0276756	May 6, 2010	November 10, 2011	USA
2011/0283043	July 13, 2011	November 17, 2011	USA
2011/0283046	April 12, 2010	November 17, 2011	USA
2011/0289255	May 23, 2011	November 24, 2011	USA
2011/0296089	November 30, 2009	December 1, 2011	USA
2011/0296094	August 11, 2011	December 1, 2011	USA

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2011/0296133	May 13, 2011	December 1, 2011	USA
2011/0314209	June 18, 2010	December 22, 2011	USA
2012/0030669	July 28, 2010	February 2, 2012	USA
2012/0033519	December 30, 2008	February 9, 2012	USA
2012/0054419	July 11, 2011	March 1, 2012	USA
2012/0059972	October 18, 2010	March 8, 2012	USA
2012/0060060	March 7, 2011	March 8, 2012	USA
2012/0066441	November 21, 2011	March 15, 2012	USA
2012/0072645	March 16, 2011	March 22, 2012	USA
2012/0079174	September 28, 2011	March 29, 2012	USA
2012/0131270	February 1, 2012	May 24, 2012	USA
2012/0131381	August 5, 2010	May 24, 2012	USA
2012/0155492	December 21, 2010	June 21, 2012	USA
2012/0159039	December 2, 2011	June 21, 2012	USA
2012/0166911	December 7, 2011	June 28, 2012	USA
2012/0191921	October 4, 2010	July 26, 2012	USA
2012/0198128	February 2, 2011	August 2, 2012	USA
2012/0198129	February 2, 2011	August 2, 2012	USA
2012/0204079	November 22, 2011	August 9, 2012	USA
2012/0221781	May 7, 2012	August 30, 2012	USA
2012/0260150	December 16, 2010	October 11, 2012	USA
2012/0303875	May 7, 2012	October 29, 2012	USA
2013/0007343	June 28, 2011	January 3, 2013	USA
2013/0013852	September 23, 2011	January 10, 2013	USA
2013/0019057	July 11, 2012	January 17, 2013	USA
2013/0019062	July 11, 2012	January 17, 2013	USA
2013/0024460	June 22, 2012	January 24, 2013	USA
2013/0073793	March 20, 2012	March 21, 2013	USA
2013/0073816	September 14, 2012	March 21, 2013	USA
2013/0073895	November 13, 2012	March 21, 2013	USA
2013/0097236	October 17, 2011	April 18, 2013	USA
2013/0111295	October 31, 2011	May 2, 2013	USA
2013/0111298	October 31, 2011	May 2, 2013	USA
2013/0122781	April 6, 2011	May 16, 2013	USA
2013/0124793	January 7, 2013	May 16, 2013	USA
2013/0124807	November 13, 2012	May 16, 2013	USA
2013/0138868	November 30, 2013	May 30, 2013	USA

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2013/0145111	February 4, 2013	June 6, 2013	USA
2013/0166824	September 13, 2012	June 27, 2013	USA
2013/0166825	September 14, 2012	June 27, 2013	USA
2013/0242425	March 16, 2013	September 19, 2013	USA
2013/0275682	September 30, 2011	October 17, 2013	USA
2013/0282055	June 14, 2013	October 24, 2013	USA
2013/0282955	April 19, 2012	October 24, 2013	USA
2013/0290619	April 30, 2012	October 31, 2013	USA
2013/0297852	May 2, 2012	November 7, 2013	USA
2013/0297880	June 29, 2013	November 7, 2013	USA
2013/0326117	June 4, 2012	December 5, 2013	USA
2013/0332656	September 14, 2012	December 12, 2013	USA
2013/0339580	April 9, 2013	December 19, 2013	USA
2014/0040550	September 30, 2011	February 6, 2014	USA
2014/0047210	August 9, 2013	February 13, 2014	USA
2014/0075097	December 27, 2012	March 13, 2014	USA
2014/0101371	October 10, 2012	April 10, 2014	USA
2014/0122781	October 30, 2013	May 1, 2014	USA
2014/0189207	March 14, 2013	July 3, 2014	USA
2014/0189209	March 14, 2013	July 3, 2014	USA
2014/0195720	January 9, 2013	July 10, 2014	USA
2014/0195725	January 8, 2014	July 10, 2014	USA
2014/0208003	October 16, 2013	July 24, 2014	USA
2014/0208004	October 23, 2013	July 24, 2014	USA
2014/0208062	January 17, 2014	July 24, 2014	USA
2014/0215129	February 14, 2013	July 31, 2014	USA
2014/0237168	April 25, 2014	August 21, 2014	USA
2014/0297949	March 25, 2014	October 2, 2014	USA
2014/0317346	April 22, 2013	October 23, 2014	USA
2015/0046670	August 4, 2014	February 12, 2015	USA
2015/0067297	April 14, 2014	March 5, 2015	USA
2015/0113203	December 20, 2013	April 23, 2015	USA
2015/0134930	November 9, 2013	May 14, 2015	USA
2015/0149789	November 5, 2014	May 28, 2015	USA
2015/0193148	March 24, 2015	July 9, 2015	USA
2015/0212938	November 11, 2014	July 30, 2015	USA
2015/0261456	March 13, 2014	September 17, 2015	USA

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2015/0263978	March 14, 2014	September 17, 2015	USA
2015/0309734	July 6, 2015	October 29, 2015	USA
2015/0324264	May 6, 2014	November 12, 2015	USA
2015/0339187	May 21, 2014	November 26, 2015	USA
2015/0347041	July 3, 2014	December 3, 2015	USA
2015/0347291	May 26, 2015	December 3, 2015	USA
2015/0347296	July 3, 2014	December 3, 2015	USA
2015/0355965	August 20, 2015	December 10, 2015	USA
2015/0363120	June 25, 2013	December 17, 2015	USA
2015/0364218	January 14, 2015	December 17, 2015	USA
2015/0378613	May 17, 2013	December 31, 2015	USA
2015/0378886	April 6, 2015	December 31, 2015	USA
2016/0011818	September 10, 2015	January 14, 2016	USA
2016/0018998	January 14, 2015	January 21, 2016	USA
2016/0019159	October 10, 2013	January 21, 2016	USA
2016/0026564	October 1, 2015	January 28, 2016	USA
2016/0062698	August 19, 2015	March 3, 2016	USA
2016/0070496	November 16, 2015	March 10, 2016	USA
2016/0092116	September 26, 2014	March 31, 2016	USA
2016/0147669	November 21, 2014	May 26, 2016	USA
2016/0162186	December 9, 2014	June 9, 2016	USA
2016/0179664	December 23, 2014	June 23, 2016	USA
2016/0202910	January 13, 2016	July 14, 2016	USA
2016/0342509	May 22, 2015	November 24, 2016	USA
2016/0357462	April 12, 2016	December 8, 2016	USA
2016/0364179	August 25, 2016	December 15, 2016	USA
2017/0031699	July 29, 2015	February 2, 2017	USA
2017/0060680	December 26, 2015	March 2, 2017	USA
2017/0075620	April 24, 2014	March 16, 2017	USA
2017/0109078	October 14, 2015	April 20, 2017	USA
2017/0139838	November 13, 2015	May 18, 2017	USA
2017/0192901	September 29, 2016	July 6, 2017	USA
2017/0199703	January 13, 2016	July 13, 2017	USA
2017/0220287	April 12, 2017	August 3, 2017	USA
2017/0364445	June 15, 2017	December 21, 2017	USA
2018/0203761	January 17, 2018	July 19, 2018	USA
2018/0210787	May 2, 2017	July 26, 2018	USA

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2019/0042150	November 1, 2017	February 7, 2019	USA
2020/0368491	May 26, 2020	November 26, 2020	USA
2020/0409559	June 27, 2019	December 31, 2020	USA
10/552,085	July 15, 2016	February 4, 2020	USA
13/767,723	February 14, 2013	May 16, 2017	USA
14/047,193	October 7, 2013	January 5, 2016	USA
14/466,167	August 22, 2014	August 8, 2017	USA
14/848,273	September 8, 2015	May 5, 2020	USA
14/880,529	October 12, 2015	January 10, 2017	USA
14/951,708	November 25, 2015	December 13, 2016	USA
15/009,275	January 28, 2016	July 26, 2016	USA
15/053,372	February 25, 2016	March 7, 2017	USA
15/074,778	March 18, 2016	October 10, 2017	USA
15/211,927	July 15, 2016	February 4, 2020	USA
15/211,939	July 15, 2016	February 4, 2020	USA
15/346,641	November 8, 2016	July 18, 2017	USA
15/621,888	June 13, 2017	October 15, 2019	USA
15/625,931	June 16, 2017	November 17, 2020	USA
15/625,946	June 16, 2017	August 28, 2018	USA
15/690,006	August 29, 2017	May 5, 2020	USA
16/570,922	September 13, 2019	November 30, 2021	USA
16/591,735	October 3, 2019	June 1, 2021	USA
16/702,736	December 4, 2019	March 23, 2021	USA
16/707,934	December 9, 2019	November 16, 2021	USA
16/751,925	January 24, 2020	April 26, 2022	USA
16/779,918	February 3, 2020	February 9, 2021	USA
16/783,083	February 5, 2020	May 17, 2022	USA
16/833,547	March 28, 2020	January 4, 2022	USA
17/952,230	September 24, 2022	September 19, 2023	USA
17/952,964	September 26, 2022	April 9, 2024	USA
17/563,467	December 28, 2021	November 1, 2022	USA
17/563,481	December 28, 2021	November 1, 2022	USA
17/571,394	January 7, 2022	July 18, 2023	USA
17/877,881	July 29, 2022	July 25, 2023	USA
17/931,516	September 12, 2022	September 5, 2023	USA
JP2011/123863	May 21, 2010	June 23, 2011	Japan
JP2011/203916	March 25, 2010	October 13, 2011	Japan

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WO2005055043	November 22, 2004	June 16, 2005	PCT
WO2008057557	November 6, 2007	May 15, 2008	PCT
WO2009084724	December 25, 2008	July 9, 2009	PCT
WO2009100149	February 4, 2009	August 13, 2009	PCT
WO2010027983	September 1, 2009	March 11, 2010	PCT
WO2011044154	October 5, 2010	April 14, 2011	PCT
WO2011055407	November 4, 2009	May 12, 2011	PCT

B. Prior Art Non-Patent Publications

Prior Art	Author	Pub. Date	Publisher
Performance Impact and Interplay of SSD Parallelism through Advanced Commands, Allocation Strategy and Data Granularity	Yang Hu, et al.	2011-06-04	ICS '11, Proceedings of the international conference on Supercomputing
Exploring and Exploiting the Multilevel Parallelism Inside SSDs for Improved Performance and Endurance	Yang Hu, et al.	02-28-2013	IEEE
NVM Express 1.0b	-	2011-07-12	NVMe Express
NVM Express 1.0e	-	2013-01-23	NVMe Express
Zoned Namespace Command Set Specification	-	2021-05-18	NVMe Express
Zoned Namespace Command Set Specification Technical Proposal			
An NVM Express Tutorial	Marks, K.	August 13-15, 2013	Flash Memory Summit 2013
Bridging the Information Gap in Storage Protocol Stacks	Denehy, T., et al.	June 10-15, 2002	USENIX Association
Making Garbage Collection Wear Conscious for Flash SSD	Tjioe, J., et al.	June 30, 2012	IEEE

Prior Art	Author	Pub. Date	Publisher
NAND Flash Memory		February 27, 2009	
NVM express 1.1		October 11, 2012	NVM Express
Nvm EXPRESS Revision 1.1b		July 2, 2014	NVM Express, Inc.
Survey of Address Translation Technologies for Flash Memories		January 01, 2014	ACM Computing Surveys (CSUR), Volum e 46, Issue 3 Article No.: 36, Pages 1 – 39
Zoned Namespace Command Set Specification Technical Proposal			
Small Computer System Interface (SCSI) Primary Commands - 4 (SPC-4) Revision 16		July 29, 2008	T10 / International Committee for Information Technology Standards (INCITS)
Small Computer System Interface (SCSI) Block Commands – 3 (SBC-3) Revision 0		September 9, 2005	T10 / International Committee for Information Technology Standards (INCITS)
Small Computer System Interface (SCSI) Block Commands – 4 (SBC-4) Revision 3		August 27, 2014	T10 / International Committee for Information Technology Standards (INCITS)
Small Computer System Interface (SCSI) Zoned Block Commands (ZBC) Revision 1		May 8, 2014	T10 / International Committee for

Prior Art	Author	Pub. Date	Publisher
			Information Technology Standards (INCITS)
"Hybrid Memory Cube" specification.	Altera Corporation	January 2013	Hybrid Memory Cube Consortium
Removing The Costs Of Indirection in Flash - based SSDs with Nameless Writes	Andrea C. Arpaci-Dusseau, Remzi H. Arpaci-Dusseau, Vijayan Prabhakaran	June 22, 2010	Usenix, The Advanced Computing Systems Association
What's the Difference Between SATA and NVMe	Bob Pierce	May 31, 2012	Electronic Design
Detecting Solid-State Disk Geometry for Write Pattern Optimization	Chun-Chieh Kuo, Jen-Wei Hsieh, Li-Pin Chang	September 29, 2011	17th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications
An efficient FTL design for multi-chipped solid-state drives	Yuan-Hao Chang	September 30, 2010	The Sixteenth IEEE International Conference on Embedded and Real-Time Computing Systems and Applications
Anatomy of a solid state drive	Michael Cornwell	October 17, 2012	Association for Computing Machinery
Optimizing NAND Flash Performance	Ryan Fisher	August 2008	Flash Memory Summit

Prior Art	Author	Pub. Date	Publisher
High Performance Solid State Storage Under Linux	Eric Seppanen, Matthew T. O'Keefe, David J. Lilja	April 10, 2010	Institute of Electrical and Electronics Engineers
Principles of Operation for Shingled Disk Devices	Garth Gibson, Greg Ganger	April 2011	Parallel Data Laboratory Carnegie Mellon University
High-Speed NAND Flash: Design Considerations to Maximize Performance	Robert Pierce	August 11, 2009	Flash Memory Summit
Achieving page-mapping FTL performance at blockmapping FTL cost by hiding address translation	Yang Hu, Hong Jiang, Dan Feng, Lei Tian, Shuping Zhang, Jingning Liu	June 28, 2010	Institute of Electrical and Electronics Engineers
A Novel I/O Scheduler for SSD with Improved Performance and Lifetime	Hua Wang, Ping Huang, Shuang He, Ke Zhou, Chunhua Li, and Xubin He	May 6-10, 2013	2013 IEEE 29th Symposium
Flash-aware RAID techniques for dependable and high-performance flash memory SSD	Soojun Im and Dongkun Shin	October 14, 2010	Institute of Electrical and Electronics Engineers
PCI - SIG SR - IOV Primer - An Introduction to SR - IOV Technology	Intel Corp.	January 2011	Intel Corp.
A methodology for extracting performance parameters in solid state disks (SSDs)	Jae-Hong Kim, Dawoon Jung, Jin-Soo Kim, Jaehyuk Huh	December 28, 2009	Institute of Electrical and Electronics Engineers
JEDEC Standard, JESD229		December 2011	JEDEC Solid State Technology Association
Hybrid Aggregates: Combining SSDs and HDDs in a single storage pool	John D. Strunk	December 15, 2012	Association for Computing Machinery

Prior Art	Author	Pub. Date	Publisher
High level modeling and performance evaluation of address mapping in NAND flash memory	Walid Lafi, Didier Lattard and Ahmed Jerraya	February 17, 2010	Institute of Electrical and Electronics Engineers
Hybrid Solid State Disks: Combining Heterogeneous NAND Flash in Large SSDs	Li-Pin Chang	April 8, 2008	Institute of Electrical and Electronics Engineers
Tracking Back References in a Write-Anywhere File System Feb. 23 , 2010 .	Peter Macko, Margo Seltzer, Keith A. Smith	February 23, 2010	Usenix, The Advanced Computing Systems Association
NAND Flash Memory in Embedded Systems," http://web.archive.org/web/20101001 0107 l 6/http://www.design-reuse.com/articles/24503/nandflash-memory-embedded-systems.htrnl.	Michal Jedrak	October 1, 2010	
NAND 201: An Update on the Continued Evolution of NAND Flash	Jim Cooke	September 6, 2011	Micron
NVM Express, V. 1.2.1 , 217 pages	NVM Express	June 3, 2016	NVM Express
NVM Express, Command Set Specification, Version 1.0b, published at http://www.nvmexpress.org/resources/ by the NVM Express Work Group	NVM Express	January 6, 2022	NVM Express
Defragmentation Mechanisms for Copy-On-Write File-systems	Ohad Rodeh	April 23, 2010	IBM
Open NAND Flash Interface (ONFI) Specification, version 2.0		February 27, 2008	Open NAND Flash Interface
Open NAND Flash Interface (ONFI), Specification, version 3.1		September 19, 2012	Open NAND Flash Interface
SDF: Software-Defined Flash for Web-Scale Internet Storage Systems	Jian Ouyang, Shiding Lin, Song Jiang, Zhenyu Hou, Yong Wang,	March 2014	Association for Computing Machinery

Prior Art	Author	Pub. Date	Publisher
	Yuanzheng Wang		
Flash-aware RAID techniques for dependable and high-performance flash memory SSD	Soojun Im and Dongkun Shin	January 2011	Institute of Electrical and Electronics Engineers
Silicon FarEast, System on a chip (SOC), http://web/archive.org/web/20050901 23 1 724/http://www.sillconfareast.com		September 1, 2006	
Spansion SLC NAND Flash Memory for Embedded, data sheet, S34ML01G1, S34ML02G1, S34ML04G1 , Sep. 6 , 2012			
FIOS: A Fair, Efficient Flash I / O Scheduler	Stan Park and Kai Shen	February 23, 2012	Usenix, The Advanced Computing Systems Association
Memory space mapping using virtual addressing to multiple sized memory units	RD Tennison	August 1, 1975	IP.com
An Efficient Design and Implementation of LSM-Tree based Key-Value Store on Open-Channel SSD	Peng Wang, Guangyu Sun, Song Jiang, Jian Ouyang, Shiding Lin, Jason Cong, Chen Zhang	April 14, 2014	Association for Computing Machinery
"Asynchronous," http://web. archive.org/web/200104110325 1 4/http://www.webopedia.com/TERM /a/asynchronous.html	Webopedia	April 11, 2001	Webopedia
Expect More Mixed Cores, Less Power, and Faster Storage	William Wong	December 19, 2011	Penton Media
Beyond Block I/O: Rethinking Traditional Storage Primitives	Xiangyong Ouyang, David Nellans, Robert Wipfel, David Flynn,	August 20, 2011	Institute of Electrical and Electronics Engineers

Prior Art	Author	Pub. Date	Publisher
	Dhabalesware K. Panda		
De-indirection for Flash - based SSDs with Nameless Writes	Yiying Zhang, Leo Prasath Arulraj, Andrea C. Arpaci-Dusseau, Remzi H. Arpaci-Dusseau	February 7, 2012	Usenix, The Advanced Computing Systems Association
Performance Impact and Interplay of SSD Parallelism through Advanced Commands, Allocation Strategy and Data Granularity	Yang Hu, Hong Jiang, Dan Feng, Lei Tan, Hao Luo, Shuping Zhang	June 4, 2011	ICS '11: Proceedings of the international conference on Supercomputing
Exploring and Exploiting the Multilevel Parallelism Inside SSDs for Improved Performance and Endurance	Yang Hu, Hong Jiang, Dan Feng, Lei Tan, Hao Luo, Chao Ren	February 28, 2013	IEEE

Samsung additionally identifies and relies on patent or publication references that describe or are otherwise related to the prior art systems identified below, including any patents or publications cited in the claim charts for these systems or elsewhere in these Invalidity Contentions, including Sections V and VI, below. Samsung's investigation into prior art patent and publication references is ongoing, and Samsung reserves the right to identify and rely on additional patent or publication references that are identified through further investigation or discovery. Samsung reserves the right to supplement as further prior art is identified through investigation or discovery.

C. Prior Art Systems And Products

Samsung also contends that the Asserted Claims are invalid based on public knowledge and uses and/or offers for sale or sales of products and services that are prior art under 35 U.S.C.

§ 102(a) and/or (b); and/or prior inventions made in the United States by other inventors who had not abandoned, suppressed, or concealed them under 35 U.S.C. § 102(g), and that anticipate or render obvious under 35 U.S.C. § 103 the Asserted Claims.

Prior Art	Date of Public Use, Sale, Offer, or Availability	Offering Entity
PM1731a	2020-11	Samsung
BM1733a	2021-10	Samsung
RMS-200	2017-03-08	Radian
RMS-250	2017-03-08	Radian
RMS-300	2019-08	Radian
RMS-325	2019-11-24	Radian
RMS-350	2019-06-24	Radian
RMS-360	2020-08	Radian
RMS-375	2019-11-24	Radian
Google developed host-based FTL SSD, termed "SmartFTL SSD"[2]	2010	Google
HGST Memory Products, e.g., SMR Drives	2014	HGST (WD)
Sandforce/Seagate Memory Products	2013	Sandforce/Seagate
Baidu Memory Products, e.g., Software-Defined Flash SSDs	2013	Baidu
PureStorage Memory Products, e.g., directFlash SSDs	2009	PureStorage
NetApp Memory Products[3]	2010	NetApp (formerly SolidFire)
Toshiba Memory Products, SMR SSD	2018	Toshiba
Microsoft Azure Memory Products, e.g., Project Denali	2018	Microsoft
CNEX Labs Memory Products, e.g., OpenChannel SSDs	2018	CNEX Labs
Kioxia Memory Products, e.g., HK3R series	2013	Kioxia
SK-Hynix Memory Products, e.g., MLC NAND Flash drive	2013	SK-Hynix
Marvell Memory Products, e.g., DragonFly™ NVDRIVE	2013	MARVELL
Solidigm Memory Products, Intel SSDs	2012	Solidigm

[2] https://146a55aca6f00848c565-a7635525d40ac1c70300198708936b4e.ssl.cf1.rackcdn.com/images/c867f55eaa86f735dc82d649bd18077e9388f07f.pdf

[3] https://www.netapp.com/media/23262-tradeoffs-west10.pdf

Samsung has begun to take discovery of third parties, but the process of identifying and engaging with entities that may have prior art from twenty or more years ago is ongoing. Samsung reserves the right to conduct such discovery and supplement these Invalidity Contentions to include any prior art systems and products that render the asserted claims invalid, if necessary. Samsung may use documentation and publications, physical samples, executable software, or source code as evidence of the relevant functionality of these prior art products or services. Samsung will make available for inspection any physical samples of products, systems, or software listed above, and/or any source code therefor, that it has in its possession or that becomes available during discovery.

V. BACKGROUND: STATE OF THE ART AT TIME OF ALLEGED INVENTION

A. All Asserted Patents

1. Admitted Prior Art

Prior to the earliest priority date of the Asserted Patents, a POSITA understood that "[S]olid-state drives (SSDs) [may] utilize NAND flash memory," "characterized by being partitioned into storage areas called erase units (EU)." '183 Patent, 1:30-47, '657 Patent, 4:36-49. Memory management may be carried out using a "flash memory controller." *Id.*, 1:47-51.

The underlying functions or tasks may be managed by a flash memory controller using a flash translation layer (FTL), which keeps records of logical-to-physical translations, wear count, bad blocks and so forth using RAM that is built-in to the flash memory controller." *Id.*, 60-64.

One such function is maintenance, where, e.g., "wear leveling" is used "to help mitigate wear caused by accumulated writes to particular locations of flash memory," based on tracked metadata. *Id.,* 2:5-20.

Another such function is bad block management. "[M]emory cells in flash memory lose their ability to retain data reliably, portions of physical storage can be marked as 'bad;' some flash

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30 memory controllers therefore also track 'bad blocks' and use the FTL to remap valid memory so as to avoid these bad blocks." *Id.*, 2:27-37. The controller may "detect when a host attempts to write data to an already-programmed location" and "remaps" or substitutes the "bad block" with a "free EU." *Id.*

Prior to the earliest priority date of the Asserted Patents, it was also known that a memory system should perform garbage collection. '614 patent, 36:45-67. "To reclaim released space, memory controllers are periodically forced to run a garbage collection task, where they locate and consolidate partially used erase blocks to reclaim space."

Prior to the earliest priority date of the Asserted Patents, it was also known that a memory system can be organized into a multi-plane architecture and can utilize multi-plane commands. '614 patent, 1:59-2:33, 53:59-54:7.

2. Groupings of Blocks As Unit Of Memory.

Prior to the earliest priority date of the Asserted Claims, there was a known need to increase the latency and efficiency of flash memory through systems which employed units of memory comprised of multiple blocks.

For example, Seagate released Shingled Magnetic Recording (SMR) drives in 2013, which incorporate large erase granularities and sequential writes and are based on a shared software stack in Linux (as between SMR and ZNS).

For example, U.S. Patent Application No. 2012/0096217 ("Son") described systems organized by "superblocks" which are "a grouping of … blocks," where write and erasure commands were directed at superblocks using a "superblock address." *Id.*, ¶¶[0029], [0038].

For example, U.S. Patent 9,239,781 ("Ellis-781") described systems sub-divided into superblocks where each superblock is a group of erase blocks. *Id.*, 6:43-65. Ellis-781 described the operational benefits of using superblocks, such as those efficiencies related to superblock-level

metadata: "[o]ne of the effects is amount of metadata that is stored in each of the erase blocks 408 is minimized or reduced" and "[a]nother of the effects is fewer blocks are managed as well as reduction in time to initialize these data structure." *Id.*, 7:46-52.

For example, U.S. Pat. No. 7,739,444 ("Sinclair-444") taught systems organized into "metablocks," where "four blocks" "from each plane [are] logically linked together to form a metablock." *Id.*, 9:52-57, 7:2-4.

As another example, JP2005018490A ("Terasaki-490"), JP2008158908A ("Takeshi") and JP2008176606A ("Takeo") taught systems organized into physical and logical "zones," where the physical and logical zones are comprised of multiple blocks, which are in turn comprised of pages. Terasaki-490, ¶¶41-43, Fig. 4; Takeshi, ¶¶33, 39-41, Figs. 2, 4, Takeo, ¶¶22, 41-42, Fig. 3. A logical block may be comprised of less blocks than a physical zone, to account for blocks that may go bad over the lifetime of the memory. *Id.*

U.S. Pub. No. 2005/0144367 ("Sinclair-367") also discloses zones, where a flash memory's "physical memory cells are also grouped into two or more zones." *Id.*, ¶[0011]. A zone has a "specified range of logical block addresses mapped" to it. *Id.*, ¶[0011].

Numerous other examples of flash memory systems that organize memory into a grouping of blocks comprised of pages are disclosed in the charts attached to these Invalidity Contentions and are incorporated by reference herein.

3. Shared Host And Controller Memory Management.

Prior to the earliest priority date of the Asserted Claims, there was a known need for memory systems which employed shared memory management to solve for known issues relating to conventional systems which relied on memory management functionality carried out entirely by the controller.

There are numerous examples of the need for, and development of, SSDs which implemented various degrees host and controller memory management functionality.

For example, Google developed host-based FTL SSD, termed "SmartFTL SSD.[4]

For example, PureStorage developed several "directFlash" host-FTL SSD products.

For example, Samsung's U.S. Pat. Pub. 2008/0189485A1 ("Jung"), which issued as U.S. Patent No. 8,745,309, describes "method[s] of cooperative memory management where "at least one of several memory management functions [is] performed by the host." Jung, Abstract. Jung teaches the shortcomings of memory management carried out exclusively by the controller: "Unfortunately, the resources of flash controllers are generally smaller than those of hosts. Thus, a resulting execution speed of such FTL functions performed in the controller is typically slow. In some cases, the FTL functions cannot be performed at all, such as where the controller becomes overloaded." *Id.*, ¶[0005]. Jung describes various examples regarding how certain functions may be shared between the host and controller through the use of a "host FTL." *Id.*, Fig. 7. ¶¶[0038]-[0039]. To facilitate the host's memory management responsibilities, Jung teaches that the controller "loads meta information, such as an erase count, garbage collection data and a mapping table" to the host. *Id.*, ¶[0038].

For example, Son described the "shortcomings of conventional systems," and describes the benefits of shared memory management where the host "incorporates both file system information and information related to the underlying physical solid-state storage media into its operations." *Id.*, ¶[0014]. Shared memory management "may achieve various advantages … such as enhanced

[4] chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/https://146a55aca6f00848c565-a7635525d40ac1c70300198708936b4e.ssl.cf1.rackcdn.com/images/c867f55eaa86f735dc82d649bd18077e9388f07f.pdf

I/O performance, simplified SSD firmware, and extended SSD lifespan." *Id.* Systems therefore "mov[ed] solid-state management functions above the firmware level." *Id.*, ¶¶[0012]-[0014].

For example, U.S. Pub. No. 2011/0271032 ("Yamada-032") discloses that "data maintenance" operations "require[] a certain amount of power consumption" and that "conventional techniques fail to consider the device conditions" when maintenance is performed. Yamada, ¶[0010]. Yamada thus teaches that to "solve this problem" it moves certain management operations to the host, such as wear leveling. Yamada, ¶¶[0011], [0030].

For example, U.S. Pub. No. 2014/0047159 ("Ahwal") discloses a "system controller 318" and a "host 300" including a "media management layer ('MML') 104 for controlling the array of flash storage modules 106" where "[f]unctions from the flash management of the system controller 318 may be shifted to the host 300" and "the MML 104 may take over certain operations, such that the flash management 326 only handles low level operations." Ahwal, ¶[0022]. The shifted "host operations 402 may include operations that may have been previously performed by on the flash memory device itself" including, for example, mapping, wear leveling, data ordering, pre-fetch, garbage collection, block management, and data buffering. Ahwal, ¶[0024], Fig. 4.

Numerous other examples of flash memory systems that share host and controller management are disclosed in the charts attached to these Invalidity Contentions and are incorporated by reference herein.

4. Multi-Plane Design And Commands

Prior to the earliest priority date of the Asserted Claims, there was a known need for memory systems which employed multi-plane designs and utilized multi-plane commands in order to improve parallel operations and memory performance.

For example, U.S. Pat. No. 8,386,700 ("Olbrich-700") taught dividing the flash memory into "SuperBlocks," comprised of erase units in each zone are on two or more different planes.

Id., 16:12-16. Olbrich-700 further teaches that each Superblock includes SuperPages, where each SuperPage includes a "starting address," *i.e.,* "a zone start logical block address" ("ZSLBA") and "15 consecutive LBAs," "a range of logical block addresses" ("LBAs"). *Id.*, 72:33-38. "[E]ach SuperPage consists of four flash Pages, each of which is stored on a different Flash Die" (across different planes). *Id.*, 6:23-29. Olbrich-700 utilizes a common page address in which the pages of a SuperPage have the "same address location." *Id.*, 15:60-67. U.S. Pat. No. 8,621,137 ("Olbrich-137") teaches the same or substantially similar limitations.

For example, U.S. Pat. Pub. No. 2010/0049908A1 ("Gonzalez-908") taught that "blocks may be linked together as metablocks; that is, each logically addressable metablock is defined to include one physical block from each plane." *Id.*, ¶[0010]. Each metablock includes a "common logical address" and is comprised of a "range of consecutive [logical] addresses." *Id.*, ¶¶[0010], [0018], [0044], [0057].

For example, Yang Hu et al., Performance Impact and Interplay of SSD Parallelism through Advanced Commands, Allocation Strategy and Data Granularity ("Hu") discloses that "SSD manufacturers have provided advanced commands, such as… multi-plane." Hu, §1.3 ("SSD manufacturers have provided advanced commands, such as… multi-plane…"), §2.2 ("Multi-plane command activates multiple read, program or erase operations in all planes of the same die"), Fig. 4. Hu explains that a "multi-plane command" where the "blocks executing a multi-plane" command have the "same … page addresses" had already been implemented by SSD manufacturers (Hu, §2.2) and that such techniques "improve the performance of SSD by handling read, write and erase operations more efficiently" (Hu, §1.3, "Advanced commands"). Hu also confirms that at the time "parallelism" was "regarded as a key to achieving the peak performance" of an SSD (Hu, §1.4, "SSD parallelism").

For example, Yamada-032 describes the host "control[ling] the maintenance to be performed." *Id.*, ¶[0029]. "This improves the data retention properties of the nonvolatile memory" because the host "can … determine an address for which maintenance is to be performed … by managing the write history of predetermined addresses of the nonvolatile memory." *Id.*, ¶[0029]. Additionally, the host can "receive the status of nonvolatile memory … and enable[] data maintenance … without … maintenance to be performed together with normal processing of the system." *Id.*, ¶[0036].

Numerous other examples of flash memory systems that utilize multi-plane commands are disclosed in the charts attached to these Invalidity Contentions and are incorporated by reference herein.

5. NVMe Ratifies And Releases ZNS Specification.

Prior to the filing of all Asserted Claims, on June 4, 2020, the NVMe ratified the ZNS Technical Proposal ("Zoned Namespace Command Set Specification"). Therein, the specification defined a "zone" as "[a] contiguous range of logical block addresses that is managed as a single unit," *id.*, § 1.5.6, and a "Zoned Namespace" as a set of "zones," *id.*, § 1.5.9, where the "set of zones that are contiguous non-overlapping logical block addresses," *id.*, § 2.1.

The Zoned Namespace Command Set Specification describes zone-level metadata, including, *e.g.*: (i) "Zone State," where a zone may be classified as, *inter alia*, empty, open, closed, full; (ii) a zone "write pointer" identifying "the next writeable logical block address in that zone;" a "Zone Start Logical Block Address (ZSLBA) attribute defines the lowest logical block address for that zone;" (iii) "Zone Capacity attribute defines the writable capacity of that zone;" and (iv) "Reset Zone Recommended attribute indicates that the controller recommends that the host resets that zone." *Id.*, § 2.2.

The Zoned Namespace Command Set Specification describes host commands such as "Identify Namespace Data Structure," which commands the controller to provide information about the Zoned Namespaces. *Id.*, § 3.1.2. It further describes host commands to retrieve "Zone Descriptor Data Structure," which commands the controller to provide information about the Zones. § 4.4.2.3.

The Zoned Namespace Command Set Specification describes additional features including "host management requirements." *Id.*, Annex A.

Prior to the filing of all Asserted Claims (except for those contained in the '183 Patent), on May 18, 2021, the NVMe ratified the Zoned Namespace Command Set Specification 1.1.

B. Tracking Metadata For Groups Of Blocks

Prior to the earliest priority date of the Asserted Patents, there were various means to track metadata, such as page utilization, for groupings of blocks.

For example, Son taught tracking "a wear count [], a valid page count [], an invalid page count [], … a next page indicator [], … [and] a last modification time[.]" *Id.*, ¶[0039]. Ellis-781 taught tracking "valid-page count," defined as the "number of pages that are valid in each of the super blocks 502," *Id.*, 11:58-12:2; 12:37-41, Claims 1 and 5, as well as "erase count," which is "defined as a numerical value indicating a number of times … the super blocks 502 are programmed or erased," *id.*, 11:63-67, 13:14-24, claim 1. Sinclair-444 taught tracking "[t]he number of pages" and "the number of pages of unprogrammed capacity" for each metablock. *Id.*, 26:5-17.

Prior to the earliest priority date of the Asserted Patents, there were various means by which a controller would share metadata with the host in order for the host to conduct memory management functions and operations. For example, Yamada teaches the benefit of share host and controller memory management functions with respect to maintenance activities. Such shared

management responsibility enabled (i) data maintenance to be performed in accordance with the status of the nonvolatile memory system, without requiring the data maintenance to be performed together with normal processing of the system;" "maintenance to be performed with a sufficiently long processing time allocated to the maintenance, and improves the data retention properties;" and (iii) "system management status, such as the battery level, to be controlled in a manner that the maintenance will be completed in a reliable manner." *Id.* ¶[0036]. Yamada describes systems including a controller with a "maintenance request unit," and the access device (host) includes a "maintenance command unit," where memory management is shared and requests for copying data originate from the controller and are commanded by the host. *Id.*, ¶[0012]. U.S. Pat. Pub. 2012/0284587 ("Yu") taught functionality where the host is able to query the controller for metadata through "Self-Monitoring, Analysis and Reporting Technology" ("S.M.A.R.T) commands. *Id.*, ¶[0095], [0213]. The S.M.A.R.T. functionality is a discrete example of shared responsible between the host and controller to "monitor and control error correction, wear, bad block, and other flash memory management." *Id*.

C. Defective Block Or Bad Block Management And Remapping

Prior to the earliest priority date of the Asserted Patents, flash memory was known to become defective over a long period of time. There are various means for detecting and replacing the defective flash blocks or erase units, called bad blocks (*i.e.*, "bad block management"), including remapping logical addresses to new flash blocks.

For example, U.S. Pat. No. 7,984,233 ("Sinclair-233") taught that "[i]n typical memory system[s], a few extra blocks of storage capacity are provided than are necessary to store the amount of data within the address space … ." *Id.*, 10:31-65. "One or more of these extra blocks may be provided as redundant blocks for substitution for other blocks that may become defective during the lifetime of the memory." *Id.*, 10:31-65.

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For example, Sinclair-367 taught that "logical block addresses are regularly re-mapped to different physical block addresses in order to even out the usage (wear) of all the erase blocks." *Id.*, ¶¶[0107]-[0108]. And this remapping applies with "identification of any defective cells within the erase block," where "the logical address of the data that is mapped into this physical block and the address of-any substitute erase block in case the primary erase block is defective." *Id.*, ¶¶[0107]-[0108].

For example, U.S. Pat. No. 8,301,861 ("Reiter") disclosed keeping track of a "bad block indicator" for each flash block and "updat[ing] the corresponding mapping data structures" based on block type, such as a bad block. *Id.*, 6:47-62, 9:26-51.

For example, U.S. Pat. No. 8,095,765 ("Asnaashari"), which was published as U.S. Publication No. 2012/0303931, discussed determining "one or more … blocks … are … defective" and "assigning a respective replacement block." *Id.*, Abstract.

D. Memory Addressing And Bitfields

Prior to the earliest priority date of the Asserted Patents, there were various means to address memory, including addresses split into various bitfields where each bitfield is a sub-address for a sub-component of memory (*e.g.*, namespace, block device, zone, block, page, sector). And extracting those bitfields to find the storage location at the address is done with various means such as integer division, modulo operations, bit shifting, bit masking, and otherwise accessing only bits associated with the bitfield.

For example, U.S. Pat. No. 5,404,485 ("Ban") taught extracting a logical unit address from the complete logical address. "The logical unit number is the high order binary digits of the logical address and may be derived from the logical address by a bit shift operation." *Id.*, 4:67-5:12.

For example, Reiter taught about a storage device receiving a logical sector number (*i.e.*, logical address) "correspond[ing] to a logical block number (LBN) … and a logical page number (LPN) … ." *Id.*, 9:5-25. The storage device "derives LBN … by dividing LSN … by a number of sectors per block of flash media," and "derives LPN … by dividing LSN … by a number of sectors per page of flash media …" *Id.*, 9:5-25.

For example, U.S. Pub. No. 2009/0271562 ("Sinclair-562") discussed "a sample LBA address format." *Id.*, ¶[0157]. The "address format … is shown as 32 bits in length" with the "least significant bits … relating to the LBA address in a metapage," "the next bits in the address may be treated as representing the bank identifier," the "next bits may be treated as the page in the megablock," and the "final bits may be interpreted as the megablock identifier." *Id.*, ¶[0157]. "[T]he controller may strip off the bits of the bank identifier … ." *Id.*, ¶[0157].

E. Memory Data Management And Maintenance Operations

Prior to the earliest priority date of the Asserted Patents, there are various disclosures of copying data from one flash block to another, such as for maintenance operations like garbage collection.

For example, Sinclair-367 taught that "[c]opying [of data from a partially full metablock to a smaller metablock] may also be done as part of a garbage collection routine." *Id.*, ¶[0132].

For example, Sinclair-562 taught that "[w]hen a short run of addresses from the host is updated in isolation, the full logical block of addresses containing the run must retain its long-term mapping to a single block. This necessitates a garbage collection operation within the logical-to-physical memory management system, in which all data not updated by the host within the logical block is relocated to consolidate it with the updated data." *Id.*, ¶[0004].

For example, U.S. Pub. No. 2011/0314204 ("Ootsuka") taught "[w]hen the blocks in such a porous state increase, substantially usable blocks decrease and a storage area of the flash

memory cannot be effectively used. Therefore, the flash memory needs to be organized by performing, for example, compaction of collecting valid latest date and rewriting the data in a different block." *Id.*, ¶[0032].

VI. ANTICIPATION AND OBVIOUSNESS (35 U.S.C. §§ 102 AND 103)

The Asserted Claims are anticipated by and/or rendered obvious in view of one or more items of prior art identified in these Contentions, alone and/or in combination. Based on its investigation to date, Samsung has provided in the lists above the prior art presently known to Samsung that anticipates and/or renders obvious the Asserted Claims under at least Radian's and/or apparent application of those claims. The prior art identified in these Contentions discloses (*i.e.*, anticipates and/or renders obvious) the elements of the Asserted Claims either explicitly or inherently.

Prior art patents or publications included in these Contentions may be related (such as a divisional, continuation, continuation-in-part, parent, or child) to earlier or later-filed patents or publications, may have counterparts filed in other jurisdictions, or may incorporate (or be incorporated by) other patents or publications by reference. The listed patents or publications are intended to be representative of these other patents or publications to the extent they exist. Samsung accordingly reserves the right to modify, amend, or supplement these Contentions with these related patents or publications, as well as other prior art references, upon further investigation. Additionally, any reference in these Contentions, including the appendices and/or exhibits thereto, to a specific subsection or subsections of 35 U.S.C. § 102, is merely exemplary, and Samsung expressly reserves the right to rely on additional or other sections of 35 U.S.C. § 102, as appropriate.

To the extent that a primary reference is deemed, by itself, not to anticipate or render obvious a claim for failing to teach one or more limitations, the claim would nonetheless have been

obvious to a POSITA at the time of the invention by the combination of the primary reference with one or more other primary references and/or the knowledge of someone skilled in the art.

To the extent any limitation is deemed not to be exactly met by an item of prior art listed above and in the appended Exhibits, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid for obviousness under 35 U.S.C. § 103.

Additional prior art, including material referenced herein or produced in conjunction with these Invalidity Contentions, that has not been charted is nonetheless relevant to the obviousness of the Asserted Patents, including without limitation as evidence of the state of the art at the alleged time of invention, defining the relevant POSITA, and demonstrating how a POSITA would understand the charted prior art. This includes prior art identified in Sections IV and V of these cover pleadings and in the accompanying exhibits.

Moreover, Exhibits A-Obviousness, B-Obviousness, C-Obviousness, D-Obviousness, E-Obviousness, F-Obviousness, and G-Obviousness list secondary prior art references and identify, on limitation-by-limitation bases, exemplary disclosures where each secondary reference teaches the limitations of the asserted claims. To the extent that a primary reference is deemed, by itself, not to anticipate or render obvious a claim for failing to teach one or more limitations, the claim would nonetheless have been obvious to a POSITA at the time of the invention by the additional combination of the primary reference with one or more of the references listed as disclosing those alleged missing limitations in Exhibits A-Obviousness, B-Obviousness, C-Obviousness, D-Obviousness, E-Obviousness, F-Obviousness, and G-Obviousness. To the extent that an element

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of an Asserted Claim is not shown in a chart, the Asserted Claims would have been obvious based on a combination of one or more other prior art references, as set forth below and in Appendices A-F.

As such, a POSITA would have been motivated to combine any reference set forth in at least the following charts:

- Exhibits A-1 through Exhibits A-7 for the asserted claims of the '183 Patent;
- Exhibits B-1 through Exhibits B-15 for the asserted claims of the '772 Patent;
- Exhibits C-1 through Exhibits C-6 for the asserted claims of the '614 Patent;
- Exhibits D-1 through Exhibits D-5 for the asserted claims of the '801 Patent;
- Exhibits E-1 through Exhibits E-4 for the asserted claims of the '656 Patent;
- Exhibits F-1 through Exhibits F-5 for the asserted claims of the '657 Patent;
- Exhibits G-1 through Exhibits G-4 for the asserted claims of the '995 Patent.

Such combinations would be achieved, for example, by merely combining the disclosures described in the respective claim charts for each reference.

These charts, however, are exemplary. The claimed features are similarly described and suggested in other places (including in all of the documents cited during prosecution of each piece of prior art), and also were present when prior-art systems practicing the described prior art were used before the application that ultimately led to the Asserted Patents. Where patents or other printed materials are disclosed, Samsung reserves the right to also rely on those materials as descriptions of systems, devices, or methods referenced therein, publicly used, and/or on sale or known in the United States. Further, Samsung reserves the right to rely on other evidence of the prior art beyond merely the exemplary references cited in the charts attached as Exhibits.

Samsung's assertion that the combinations above render the asserted claims obvious under 35 U.S.C. § 103 is not, and is not intended to be, an admission or suggestion that each reference does not independently anticipate the Asserted Claims under 35 U.S.C. § 102. *See Connell v. Sears, Roebuck & Co*., 722 F.2d 1542, 1548 (Fed. Cir. 1983) ("'[A]nticipation is the epitome of obviousness.'") (quoting *In re Fracalossi*, 681 F.2d 792, 794 (CCPA 1982)). Further, the fact that certain secondary references are listed solely in Exhibits A-Obviousness, B-Obviousness, C-Obviousness, D-Obviousness, E-Obviousness is not intended to be an admission or suggestion that each individual reference cited therein does not also independently anticipate and/or render obvious the Asserted Claims under 35 U.S.C. §§ 102 and 103. Samsung expressly reserves the right to rely on any secondary reference cited in Exhibits A-Obviousness, B-Obviousness, C-Obviousness, D-Obviousness, E-Obviousness, F-Obviousness and G-Obviousness, as if it were set forth as a primary reference in Section IV.A, supra. Finally, the inclusion of the exemplary combinations in the attached Exhibits and Appendices does not exclude other combinations of prior art disclosed in this or previous sections.

A. Exemplary Combinations

Exemplary combinations of prior art references that render the Asserted Claims invalid as obvious under 35 U.S.C. § 103 are described in:

- Exhibits A-1 through Exhibits A-7 for the asserted claims of the '183 Patent;
- Exhibits B-1 through Exhibits B-15 for the asserted claims of the '772 Patent;
- Exhibits C-1 through Exhibits C-6 for the asserted claims of the '614 Patent;
- Exhibits D-1 through Exhibits D-5 for the asserted claims of the '801 patent;
- Exhibits E-1 through Exhibits E-4 for the asserted claims of the '656 patent;
- Exhibits F-1 through Exhibits F-5 for the asserted claims of the '657 Patent;
- Exhibits G-1 through Exhibits G-4 for the asserted claims of the '995 Patent.

Moreover, each prior art reference or system may be combined with (1) information known to persons skilled in the art at the time of the alleged invention; (2) any other anticipatory prior art references or systems; and (3) any of the additional prior art identified above or in the prosecution of the Asserted Patents and related applications.

Below are examples of prior art references and/or systems that would have been combined by one of ordinary skill in the art at the time of the alleged invention. These combinations are merely examples.

1. '183 Patent

The Asserted Claims of the '183 Patent are rendered obvious by:

- U.S. Patent Publication No. 2013/0205102 ("Ellis-102") in combination with one or more of the references identified in Exhibits A2-A7;
- Sinclair-444 in combination with one or more of the references identified in Exhibits A1, A3-A7;
- Son in combination with one or more of the references identified in Exhibits A1, A2, A4-A7;
- Terasaki-490 in combination with one or more of the references identified in Exhibits A1-A6.
- Ellis-102 and Son together or in combination with one or more of the references identified in Exhibits A2, A4-A7;
- Ellis-102, Son and Yamada together or in combination with one or more of the references identified in Exhibits A2, A5-A7;
- Terasaki-490, Son and Yamada in combination with one or more of the references identified in Exhibits A1, A2, A5, A6.
- Sinclair-444 and Son together or in combination with one or more of the references identified in Exhibits A1, A4-A7;
- Sinclair-444, Son, Yu and Jung together or in combination with one or more of the references identified in Exhibits A1, A4, A7;

2. ’772 Patent

The Asserted Claims of the ‘772 Patent are rendered obvious by:

- Olbrich-700 in combination with one or more of the references identified in Exhibits B2-B15;
- U.S. Publication No. 2010/0049908 (“Gonzalez-908”) in combination with one or more of the references identified in Exhibits B1, B2, B4-B15;
- Yamada in combination with one or more of the references identified in Exhibits B1-B5, B7-B15;
- Olbrich-700, Yamada and NVMe 1.0b together or in combination with one or more of the references identified in Exhibits B2-B5, B7-B-9, B11-B15;
- Gonzalez-908, U.S. Publication No. 2011/0302477 (“Goss-477”) and NVMe 1.0b together or in combination with one or more of the references identified in Exhibits B1, B2, B4-B9, B11-B14;
- Gonzalez-908, Goss-477, NVMe 1.0b, and Ban together or in combination with one or more of the references identified in Exhibits B1, B2, B4-B9, B12-B14;
- Gonzalez-908, Goss-477, NVMe 1.0b, and Sprouse together or in combination with one or more of the references identified in B1, B2, B4-B9, B11, B12, B14;
- Gonzalez-908, Goss-477, NVMe 1.0b, and Cornwell together or in combination with one or more of the references identified in Exhibits B1, B2, B4-B8, B11-B14;

3. ’614 Patent

The Asserted Claims of the ‘614 Patent are rendered obvious by:

- Ellis-102 in combination with one or more of the references identified in Exhibits C2-C6;
- Son in combination with one or more of the references identified in Exhibits C1, C3-C6;
- International Publication No. WO 2008/082996 (“Sinclair-996”) in combination with one or more of the references identified in Exhibits C1-C2, C4-C6;
- Takeo in combination with one or more of the references identified in Exhibits C1-C3, C5-C6;

- Terasaki-490 in combination with one or more of the references identified in Exhibits C1-C4, C6;

- Asnaashari in combination with one or more of the references identified in Exhibits C1-C5;

- Ellis-102, Son, and Olbrich-137 in combination with one or more of the references identified in Exhibits C3-C6;

- Ellis-102, Son, Olbrich-137, and Yamada in combination with one or more of the references identified in Exhibits C3-C6;

- Takeo, Son, Sinclair-996 in combination with one or more of the references identified in Exhibits C1-C6;

- Takeo, Son, Sinclair-996, and Olbrich-137 in combination with one or more of the references identified in Exhibits C1, C5-C6;

- Takeo, Son, Sinclair-996, Olbrich-137, and Yu in combination with one or more of the references identified in Exhibits C1, C5-C6;

- Takeo, Son, Sinclair-996, Olbrich-137, Ellis-102 and Yamada in combination with one or more of the references identified in Exhibits C1, C5-C6.

- Asnaashari, Son, Olbrich-137, in combination with one or more of the references identified in Exhibits C1-C5;

- Asnaashari, Son, Olbrich-137, Ellis-102 and Yamada in combination with one or more of the references identified in Exhibits C1-C5.

4. ’801 Patent

The Asserted Claims of the ’801 patent are rendered obvious by:

- Sinclair-562 in combination with one or more of the references identified in Exhibits D2-D5;

- Olbrich-137 in combination with one or more of the references identified in Exhibits D1-D5;

- Terasaki-490 in combination with one or more of the references identified in Exhibits D1-D3, D5;

- Yamada in combination with one or more of the references identified in Exhibits D1-D3, D5;

- Ahwal in combination with one or more of the references identified in Exhibits D1-D2, D4-D5;

- Sinclair-562 and Yamada in combination with one or more of the references identified in Exhibits D3-D5;

- Sinclair-562, Yamada, and Ahwal in combination with one or more of the references identified in Exhibits D4-D5;

- Sinclair-562, Yamada, and Olbrich-137 in combination with one or more of the references identified in Exhibits D3-D5;

- Sinclair-562, Yamada, and Sinclair-996 in combination with one or more of the references identified in Exhibits D3-D5;

- Terasaki-490 and Yamada in combination with one or more of the references identified in Exhibits D1-D2, D3-D5;

- Terasaki-490, Yamada, and Ahwal in combination with one or more of the references identified in Exhibits D1, D5;

5. ’656 Patent

The Asserted Claims of the ’656 patent are rendered obvious by:

- Ban in combination with one or more of the references identified in Exhibits E2-E4;

- Reiter in combination with one or more of the references identified in Exhibits E1, E3-E4;

- ZBC in combination with one or more of the references identified in Exhibits E1-E3;

- Ban and Sinclair-562 together or in combination with one or more references identified in Exhibits E2-E4;

- Ban, Sinclair-562, and Asnaashari together or in combination with one or more references identified in Exhibits E2-E4;

- Ban, Sinclair-562, and Sinclair-367 together or in combination with one or more references identified in Exhibits E2, E4;

- Ban, Sinclair-562, and ZBC together or in combination with one or more references identified in Exhibits E1, E3;

- Ban, Sinclair-562, ZBC, and Sinclair-367 together or in combination with one or more references identified in Exhibits E2;
- Ban, Sinclair-562, ZBC, and Asnaashari together or in combination with one or more references identified in Exhibits E2, E3;
- Ban, ZBC, and Sinclair-367 together or in combination with one or more of the references identified in Exhibits E2;
- Ban, ZBC, Sinclair-367, and Yamada together or in combination with one or more of the references identified in Exhibits E2;
- Ban, ZBC, and Asnaashari together or in combination with one or more references identified in Exhibits E2-E3;
- Ban, ZBC, Asnaashari, and Yamada together or in combination with one or more references identified in Exhibits E2-E3;
- Reiter and Sinclair-562 together or in combination with one or more references identified in Exhibits E1, E3-E4;
- Reiter, Sinclair-562, and Asnaashari together or in combination with one or more references identified in Exhibits E1, E3-E4;
- Reiter, Sinclair-562, and Sinclair-367 together or in combination with one or more references identified in Exhibits E1, E4;
- Reiter, Sinclair-562, and ZBC together or in combination with one or more references identified in Exhibits E1, E3;
- Reiter, Sinclair-562, ZBC, and Sinclair-367 together or in combination with one or more references identified in Exhibits E1;
- Reiter, Sinclair-562, ZBC, and Asnaashari together or in combination with one or more references identified in Exhibits E1, E3;
- Reiter and ZBC together or in combination with one or more of the references identified in Exhibits E1, E3;
- Reiter, ZBC, and Sinclair-367 together or in combination with one or more of the references identified in Exhibits E1; and
- Reiter, ZBC, Sinclair-367, and Yamada together or in combination with one or more of the references identified in Exhibits E1;
- Reiter, ZBC, and Asnaashari together or in combination with one or more of the references identified in Exhibits E1, E3; and

- Reiter, ZBC, Asnaashari, and Yamada together or in combination with one or more of the references identified in Exhibits E1, E3;

6. ’657 Patent

The Asserted Claims of the ‘657 Patent are rendered obvious by:

- Ban in combination with one or more of the references identified in Exhibits F2-F5;
- Reiter in combination with one or more of the references identified in Exhibits F1, F1, F3-F5;
- Sinclair-233 in combination with one or more of the references identified in Exhibits F1-F2, F4-F5;
- ZBC in combination with one or more of the references identified in Exhibits F1-F4;
- Ban and Sinclair-562 together or in combination with one or more references identified in Exhibits F2-F5;
- Ban, Sinclair-562, and Asnaashari together or in combination with one or more references identified in Exhibits F2-F5;
- Ban, Sinclair-562, and Sinclair-367 together or in combination with one or more references identified in Exhibits F2-F3, F5;
- Ban, Sinclair-562, and ZBC together or in combination with one or more references identified in Exhibits F2-F4;
- Ban, Sinclair-562, ZBC, and Sinclair-367 together or in combination with one or more references identified in Exhibits F2-F3;
- Ban, Sinclair-562, ZBC, and Asnaashari together or in combination with one or more references identified in Exhibits F2-F4;
- Ban and ZBC together or in combination with one or more of the references identified in Exhibits F2-F4;
- Ban, ZBC, and Sinclair-367 together or in combination with one or more of the references identified in Exhibits F2-F3;
- Ban, ZBC, Sinclair-367, and Yamada together or in combination with one or more of the references identified in Exhibits F2-F3;

- Ban, ZBC, and Asnaashari together or in combination with one or more of the references identified in Exhibits F2-F4;

- Ban, ZBC, Asnaashari, and Yamada together or in combination with one or more of the references identified in Exhibits F2-F4;

- Reiter and Sinclair-562 together or in combination with one or more references identified in Exhibits F1, F3-F5;

- Reiter, Sinclair-562, and Asnaashari together or in combination with one or more references identified in Exhibits F1, F3-F5;

- Reiter, Sinclair-562, and Sinclair-367 together or in combination with one or more references identified in Exhibits F1, F3, F5;

- Reiter, Sinclair-562, and ZBC together or in combination with one or more references identified in Exhibits F1, F3-F4;

- Reiter, Sinclair-562, ZBC, and Sinclair-367 together or in combination with one or more references identified in Exhibits F1, F3;

- Reiter, Sinclair-562, ZBC, and Asnaashari together or in combination with one or more references identified in Exhibits F1, F3-F4;

- Reiter and ZBC together or in combination with one or more of the references identified in Exhibits F1, F3-F4;

- Reiter, ZBC, and Sinclair-367 together or in combination with one or more of the references identified in Exhibits F1, F3; and

- Reiter, ZBC, Sinclair-367, and Yamada together or in combination with one or more of the references identified in Exhibits F1, F3.

- Reiter, ZBC, and Asnaashari together or in combination with one or more of the references identified in Exhibits F1, F3; and

- Reiter, ZBC, Asnaashari, and Yamada together or in combination with one or more of the references identified in Exhibits F1, F3.

7. ’995 Patent

The Asserted Claims of the ’995 Patent are rendered obvious by:

- Ban in combination with one or more of the references identified in Exhibits G2-G4;

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- Reiter in combination with one or more of the references identified in Exhibits G1, G3-G4;
- ZBC in combination with one or more of the references identified in Exhibits G1-G3;
- Ban and Sinclair-562 together or in combination with one or more references identified in Exhibits G2-G4;
- Ban, Sinclair-562, and Asnaashari together or in combination with one or more references identified in Exhibits G2-G4;
- Ban, Sinclair-562, and Illiadis together or in combination with one or more references identified in Exhibits G2, G4;
- Ban, Sinclair-562, and Sinclair-367 together or in combination with one or more references identified in Exhibits G2, G4;
- Ban, Sinclair-562, and ZBC together or in combination with one or more references identified in Exhibits G1, G3;
- Ban, Sinclair-562, ZBC, and Sinclair-367 together or in combination with one or more references identified in Exhibits G2;
- Ban, Sinclair-562, ZBC, and Asnaashari together or in combination with one or more references identified in Exhibits G2, G3;
- Ban, Sinclair-562, ZBC, and Illiadis together or in combination with one or more references identified in Exhibits G2;
- Ban, ZBC, and Sinclair-367 together or in combination with one or more of the references identified in Exhibits G2;
- Ban, ZBC, Sinclair-367, and Yamada together or in combination with one or more of the references identified in Exhibits G2;
- Ban, ZBC, and Asnaashari together or in combination with one or more of the references identified in Exhibits G2-G3;
- Ban, ZBC, Asnaashari, and Yamada together or in combination with one or more of the references identified in Exhibits G2-G3;
- Ban, ZBC, and U.S. Patent No. 9,141,526 ("Illiadis") together or in combination with one or more of the references identified in Exhibits G2-G3;
- Ban, ZBC, Illiadis, and Yamada together or in combination with one or more of the references identified in Exhibits G2-G3;

- Reiter and Sinclair-562 together or in combination with one or more references identified in Exhibits G1, G3-G4;
- Reiter, Sinclair-562, and Asnaashari together or in combination with one or more references identified in Exhibits G1, G3-G4;
- Reiter, Sinclair-562, and Illiadis together or in combination with one or more references identified in Exhibits G1, G3-G4;
- Reiter, Sinclair-562, and Sinclair-367 together or in combination with one or more references identified in Exhibits G1, G4;
- Reiter, Sinclair-562, and ZBC together or in combination with one or more references identified in Exhibits G1, G3;
- Reiter, Sinclair-562, ZBC, and Sinclair-367 together or in combination with one or more references identified in Exhibits G1;
- Reiter, Sinclair-562, ZBC, and Asnaashari together or in combination with one or more references identified in Exhibits G1, G3;
- Reiter, Sinclair-562, ZBC, and Illiadis together or in combination with one or more references identified in Exhibits G1, G3;
- Reiter, ZBC, and Sinclair-367 together or in combination with one or more of the references identified in Exhibits G1; and
- Reiter, ZBC, Sinclair-367, and Yamada together or in combination with one or more of the references identified in Exhibits G1.
- Reiter, ZBC, and Asnaashari together or in combination with one or more of the references identified in Exhibits G1-G2; and
- Reiter, ZBC, Asnaashari, and Yamada together or in combination with one or more of the references identified in Exhibits G1-G2.
- Reiter, ZBC, and Illiadis together or in combination with one or more of the references identified in Exhibits G1-G2; and
- Reiter, ZBC, Illiadis, and Yamada together or in combination with one or more of the references identified in Exhibits G1-G2.

B. Motivation To Combine

Samsung intends to present expert evidence demonstrating the motivation to combine of one of ordinary skill in the art. Such facts and evidence is expert testimony and will be presented

in the experts' reports according to the schedule of the Court. Samsung incorporates by reference its forthcoming expert reports and any testimony of its experts presented according to the Court's schedule. The motivation to combine or modify the above items of prior art are present, for example, in the references themselves, the Asserted Patents, references cited on the face of the Asserted Patents, the knowledge, skill, or creativity of one of ordinary skill in the art, the prior art as a whole, and/or the nature of the problems allegedly addressed by the Asserted Patents. The law requires no showing of a specific motivation to combine or modify prior art references disclosed herein and in the Invalidity Charts, as each combination or modification of art would have no unexpected results and at most would simply represent a known alternative to one of skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1739-40 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases, a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id*. at 1742. Thus, to a person of ordinary skill in the art, the Asserted Claims represent solutions that would have been obvious to try, with predictable results.

Nevertheless, should additional evidence of motivation to combine or modify be required to render the Asserted Claims obvious, Samsung contends that there was a motivation to combine the references identified above. That motivation was provided in the nature of the problem allegedly solved by the Asserted Patents, the teachings of the cited prior art itself, and/or the knowledge of a person of ordinary skill in the art. For example, the combinations identified above would have been combined or modified using: known methods to yield predictable results; common sense; known techniques in the same way; a simple substitution of one known, equivalent

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element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining or modifying the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. In addition, the combination of the prior art references would have been obvious because the combination represents known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine or modify the prior art references above includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge, skill, or creativity that would have been possessed by a person having ordinary skill in the art. Samsung may rely on uncited portions of the prior art references cited and produced, other publications and testimony, and the testimony of experts to establish that a person of ordinary skill in the art would have been motivated to modify or combine certain of the cited references so as to render the claims obvious.

For example, where multiple publications describe the same system, describe devices that are intended to be used together, or are from the same author, publisher, or manufacturer, one of ordinary skill would be motivated and find it obvious to read those publications together and combine their disclosure. As another example, where a product was available in another country, the availability of such a product would motivate a person of ordinary skill to arrive at the same or similar product in the United States. As yet another example, where the prior art identifies the

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desirability of or plans for future enhancements of a system, a person of ordinary would be motivated to incorporate such enhancements even if the original developer or author was unable to complete those enhancements.

1. Motivation To Combine – '183 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references in the A-Obviousness chart as they all discuss methods and systems for the improvement and optimization of NAND Flash SSD memory management. Moreover, these references are analogous because they all discuss various means of memory management relying on the generation and tracking of metadata where that metadata is updated over time and that metadata is used for activities to prolong the useful life of the memory. A POSITA would have been motivated to combine any of the references in A-1 to A-7 in A-Obviousness, because the references all disclose techniques for improving the lifetime, data retention, and performance of solid state disk drives (SSDs) and therefore all relate to the same technological field.

Memory management systems in SSDs typically rely on and combine ideas from different references to iteratively achieve the superior functionality—and reflect discrete implementable improvements in the field of memory management—based on known techniques in the art. Accordingly, a POSITA would be motivated to combine the above-identified contributions, and variations thereof, to incorporate various forms of metadata and the utility of said metadata, e.g., the use of maintenance metadata for maintenance activities, in order to increase efficiency and memory system longevity. These combinations would also have been a combination of prior art elements according to known methods and obvious to try given that there were a finite number of identified, predictable solutions in the prior art. Moreover, these combinations would have been the result of applying known techniques to a known method – that was ready for improvement – to yield predictable results.

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A person of ordinary skill in the art would have been motivated to combine any of memory systems and methods disclosed in Exs. A3-A6 with primary references such as Ex. A1, Ellis-102, Ex. A2, Sinclair-444, and Ex. A7, Terasaki-490. Ellis-102, Sinclair-444, and Terasaki-490 describe systems organized by groupings of blocks termed Superblocks, Metablocks, or zone where metadata is maintained for those groupings of blocks and used to monitor memory. Ellis-102, Sinclair-444 and Terasaki-490 propose solutions to address the unique challenges of SSDs, in particular, the inefficiencies introduced by the varying write and erase unit size causing garbage collection overheads and reducing the performance and endurance of SSDs due to additional data copies. A POSITA would naturally look to techniques that (i) cut the number of meta data bookkeeping structures and (ii) keep file data contiguous. Ellis-102 already teaches the first—merging many erase blocks into larger super-blocks so the controller tracks far fewer units and can recycle them in RAID-aligned stripes. Sinclair teaches the second—mapping each host file to contiguous logical blocks sized to the underlying erase geometry to curb fragmentation. Because these patents address the same design pressure (metadata overhead and additional data copies to perform garbage collection) in the same field (NAND-flash controllers), combining Sinclair-444's logical-block/file mapping with Ellis-102's physical super-block architecture would have been a routine optimization, yielding the predictable benefit of still fewer metadata pages and even smoother recycling across the larger super-blocks.

Ellis-102 and Sinclair-444 also both describe systems where the controller and host may share memory management responsibility, *i.e.*, Ellis-102 describes that the host may assume tasks described for the controller and Sinclair describes the need to share information (typically reserved for the controller) with the host in order to ensure efficient allocation of data. It would be obvious to a POSITA to combine these two primary references with the systems and methods disclosed in

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Exs. A3-A7, as they teach additional types of useful metadata along with the uses and benefits of that metadata, and teach additional discrete implementations of host and controller shared memory management functions.

Similar to Ellis-102 and Sinclair-444, Terasaki-490 similarly teaches a physical zone architecture in order to optimize memory management. It further teaches the use of a Zone Management Table, maintaining and collecting zone-level metadata concerning the status of each zone, *i.e.*, the data stored within and physical mapping information. This status information is provided to and exchanged with the host via the host interface facilitating shared memory management by the host based on the metadata provided. As with Ellis-102 and Sinclair-444, Terasaki-490 represents a primary reference comprising the requisite architectural scaffolding to practice the Asserted Claims. Further, in light of the suite of metadata maintained at the zone-level in Terasaki-490, the inclusion of additional forms of metadata described in, e.g., Son, or the discrete shared management responsibilities in, e.g., Yamada, could be implemented by a POSA using common techniques and would be obvious to try.

A POSITA could implement the additional types of metadata with a reasonable expectation of success. Ellis-102, Sinclair-444, and Terasaki-490 already describe systems with the infrastructure to generate, track and store metadata, and a POSITA would need only incorporate additional types of metadata into that pre-existing structure—adding additional useful metadata represents routine work that is well-understood and predictable. Given the utility of the metadata described in the art, its inclusion would be obvious to try. Indeed, the references acknowledge the flexibility and tailor-ability of system metadata. And, a POSITA could implement the additional discrete types of shared host and controller memory management with a reasonable expectation of success. Ellis-102, Sinclair-444 and Terasaki-490 already describe flexible controller and host

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responsibilities, and the incorporation of discrete aspects of shared responsibility merely requires the transposing of certain data and logic from the firmware of the controller to the software of the host. In light of the benefits of such discrete implementations described in the art, it would be obvious to incorporate these teachings, and the relocation of functions from the controller to the host represents routine work that is well-understood and predictable combinations. Crucially, host participation can reduce garbage-collection (GC) overhead by leveraging application-level knowledge: the host can schedule GC when the workload is idle, and it can guide the controller to group "hot" (frequently updated) data together and "cold" (rarely updated) data together within the same super-blocks, thereby lowering write-amplification and extending flash lifetime. In addition, market pressure from hyperscale operators such as Google was already driving the industry toward host-aware SSD designs. Google, for example, publicly sought APIs that let the host "control timing over background tasks" to tame tail-latency and eventually introduced its custom-designed Titanium Local SSD for cloud workloads—evidence that longevity and performance concerns were spurring hyperscalers to build their own SSD solutions.

For example, a POSITA would have been motivated to combine Ellis-102 and Son. Son and Ellis both concern the optimization of NAND Flash SSD memory management. Both Ellis-102 and Son address the same problem—simplifying systems, improving efficiency and performance, and prolonging life-span—through the use of larger units of memory, superblocks.

Specifically, a POSITA would have been motivated to incorporate Son's teaching regarding (i) additional forms of superblock metadata and (ii) the sharing of superblock metadata with a host for purposes of memory management, to the system described in Ellis-102. First, Ellis-102 teaches that "metadata can include … [any] NAND statistics that [are] collected as a consequence of normal operatives," and "any additional information … that can aid in retrieval,

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organization, health of, and current condition or state of the memory devices." Ellis-102, 10:21-32, 12:26-29. Son teaches the benefits of such metadata including for, i.e., write operations and maintenance. *E.g.*, Son, ¶¶[0078]-[0080]. A POSITA would have had a reasonable expectation of success in combining Son and Ellis-102 as it merely represents adding the additional variants of superblock metadata describing in Son, in e.g., the Superblock table relating to page utilization, to the set of superblock metadata already described in Ellis. Second, in light of variable host and controller responsibility described in Ellis and Son, a POSITA would be motivated to combine Son's host functionality with the system described in Ellis. Ellis teaches the memory management responsibility may be shared between the controller and the host. Ellis-102, 4:58-65, 20:40-44. A POSITA would therefore consider Son's teaching regarding the shortcomings of SSDs which do not share responsibility between the host and controller, and teaches the benefits of "incorporating both file system [(host)] and physical storage information [(controller)]" and "moving solid-state management functions above the firmware level." Son, ¶¶[0012]-[0014]. A POSITA would have had a reasonable expectation in moving (above the firmware) certain responsibility from SSD controller to host-side software. This exercise, moving functionality in device firmware to the host-side software is common, straightforward and routine. Indeed, such translocation for cooperative memory management had been well-described in the art. For example, Jung describes "method[s] of cooperative memory management where "at least one of several memory management functions [is] performed by the host." Jung, Abstract.

For the same and similar reasons, a POSITA would have been motivated to combine the teachings of Son with the system in Sinclair-444, as Sinclair-444 similar teaches the maintenance of categories of metablock metadata and shared memory management responsibility between the host and controller, as well as Terasaki-490 for the reasons set out above.

For further example, a POSITA would have been motivated to combine the teachings of Yamada with Ellis-102 or Terasaki-490. Like Ellis-102 (and Son), Yamada involve similar techniques to solve the same problem, i.e., collecting, storing and using metadata for maintenance activities to improve the efficiency, performance and "integrity of data" in NAND flash memory systems. *E.g.*, Yamada, ¶¶[0005]-[0011], [0207]-[0211], [0029].

Specifically, a POSITA would be motivated to incorporate Yamada's teaching regarding host-initiated maintenance/copy commands. Yamada teaches a variety of benefits for systems with host-initiated maintenance/copy commands based on metadata received from the controller, e.g., "enabl[ing] data maintenance to be performed in accordance with the status of the nonvolatile memory system, without requiring the data maintenance to be performed together with normal processing of the system," "enable[ing] the maintenance to be performed with a sufficiently long processing time allocated to the maintenance, and improves the data retention properties," and "enabl[ing] the system management status, such as the battery level, to be controlled in a manner that the maintenance will be completed in a reliable manner." Yamada, ¶[0036]. In light of the teaching in Ellis-102 that memory management responsibility may be shared between the controller and the host (or the teaching in Terasaki-490 of the need to transmit zone status metadata with the host) and the benefits described in Yamada, a POSITA would be motivated to incorporate Yamada's teaching regarding host-initiated copy/maintenance commands which are carried out by the controller and are based on metadata collected by the controller. Incorporating this teaching from Yamada would have been readily accomplished as it is merely a discrete embodiment of the shared controller and host responsibility already contemplated by Ellis-102 and Terasaki-490. A POSITA would have had a reasonable expectation of success in incorporating this host command

functionality—moving the copy command responsibility from SSD controller firmware to host-side software would have been straightforward and routine.

For the same and similar reasons—i.e., primary references contemplating shared host and controller memory management responsibility and secondary references teaching the benefits of discrete implementations of the same—a POSITA would have been motivated to combine the teachings of Yu and Jung with the system in Sinclair.

2. Motivation To Combine – '772 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references in the B-Obviousness chart as they all discuss methods and systems for the improvement and optimization of NAND Flash SSD memory management. Moreover, these references are analogous because they all discuss various means of memory management relying on the generation and tracking of metadata where that metadata is updated over time and that metadata is used for activities to prolong the useful life of the memory. A POSITA would have been motivated to combine any of the references in B-1 to B-15 in A-Obviousness, because the references all disclose techniques for improving the lifetime, data retention, and performance of solid state disk drives (SSDs) and therefore all relate to the same technological field.

Memory management systems in SSDs typically rely on and combine ideas from different references to iteratively achieve the superior functionality—and reflect discrete implementable improvements in the field of memory management—based on known techniques in the art. Accordingly, a POSITA would be motivated to combine the above-identified contributions, and variations thereof, to incorporate various forms of metadata and the utility of said metadata, e.g., the use of maintenance metadata for maintenance activities, in order to increase efficiency and memory system longevity. These combinations would also have been a combination of prior art elements according to known methods and obvious to try given that there were a finite number of

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identified, predictable solutions in the prior art. Moreover, these combinations would have been the result of applying known techniques to a known method—that was ready for improvement—to yield predictable results.

A person of ordinary skill in the art would have been motivated to combine any of memory systems and methods disclosed in Exs. B2, B4-B15 with primary references such as Ex. B1, Olbrich-700 (8,386,700) and Ex. B3, Gonzalez-908 (2010/0049908A1). Olbrich-700 and Gonzalez-908 both describe systems organized by groupings of blocks termed Superblocks or Metablocks, where metadata is maintained for those groupings of blocks and used to monitor memory. Faced with excessive metadata traffic—the need to read-modify-write per-block mapping pages every time data is moved—and the write-amplification that occurs when many small blocks are garbage-collected separately, a POSITA would have been motivated to integrate the adaptive (sub-) Metablock sizing of Gonzalez-908 with the SuperBlock-based garbage-collection scheme of Olbrich-700. Olbrich-700 already aggregates multiple physical blocks into a SuperBlock and tracks them with a single metadata table, so the controller can erase the whole unit once an 'invalid-page' threshold is met, reducing bookkeeping I/O and GC passes. Gonzalez-908 confronts the same fragmentation problem and likewise bundles blocks into Metablocks, but goes further—shrinking or expanding the group to match host write size so that only the right-sized unit is later copied or erased, thereby reducing copy-on-write traffic and erase cycles . Because both references pursue the identical goal—minimizing metadata overhead and write-amplification by treating several physical blocks as one logical erase unit—combining Gonzalez-908's host-adaptive grouping with Olbrich-700's proven SuperBlock metadata and GC method would have been an obvious, predictable optimization well within ordinary skill. Olbrich-700 and Gonzalez-908 both describe various techniques and methods for identifying data in need of

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maintenance and the execution of such maintenance. Confronted with the need to align SSD maintenance operations with host, respectively application, activity, a POSITA would have been motivated to marry Gonzalez-908's host-driven maintenance scheduling with Olbrich-700's unit-level health counters. Olbrich-700 already stores, for every erase unit, a compact table that holds an invalid-page counter, a time-stamp of last close, and an erase-cycle count; the controller consults those fields to decide when and which units to garbage-collect or wear-level, thereby minimizing background traffic. Gonzalez-908 tackles the same upkeep problem from the opposite direction, logging host-usage statistics (sector-count histograms, data-consolidation events, access-mode bits) so the firmware can reformat regions or defer work until traffic subsides, again reducing maintenance overhead and write-amplification.

Once one table of counters already exists, extending it to hold the other set of fields is routine firmware bookkeeping; the controller merely increments a few additional counters on the same metadata write, and the host (or a cloud orchestration layer) can interpret both health and usage telemetry in one read. The NVMe spec even expects such evolution: since version 1.3 it defines host- and controller-initiated telemetry log pages and expressly reserves vendor-specific admin commands and log pages so designers can surface new maintenance and debug data without changing hardware (nvmexpress.org). Industry practice shows a clear trend toward collecting ever-richer SSD telemetry for cross-layer optimization, so combining Olbrich-700's health counters with Gonzalez-908's usage statistics into a single maintenance framework would have been an obvious, predictable enhancement squarely within ordinary skill. It would be obvious to a POSITA to combine these two primary references with the systems and methods disclosed in Exs. B2, B4-B15, as they teach additional types of useful metadata along with the uses and benefits of that metadata for maintenance activities.

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A POSITA could implement the additional types of metadata with a reasonable expectation of success. Olbrich-700 and Gonzalez-908 already describe systems with the infrastructure to generate, track and store metadata, and a POSITA would need only incorporate additional types of metadata into that pre-existing structure—adding additional useful metadata represents routine work that is well-understood and predictable. Given the maintenance specific utility of the metadata described in the art, its inclusion would be obvious to try. Indeed, the references acknowledge the flexibility and tailor-ability of system metadata. And, in light of the teaching in Exs. B2, B4-B15 regarding the shortcomings of systems which rely solely on the controller for maintenance, and the benefits of maintenance responsibilities shared between the host and the controller, it would be obvious to a POSITA incorporate the discrete implementations of shared host and memory management taught therein. A POSITA could implement the additional discrete types of shared host and controller memory management with a reasonable expectation of success because the incorporation of discrete aspects of shared responsibility merely requires the transposing of certain data and logic from the firmware of the controller to the software of the host. Such relocation of functions from the controller to the host represents routine work that is well-understood and predictable combinations.

For example, a POSITA would have been motivated to combine the teachings of Yamada with Olbrich-700. Yamada involve similar techniques to solve the same problem, i.e., collecting, storing and using metadata for maintenance activities to improve the efficiency, performance and "integrity of data" in NAND flash memory systems. *E.g.*, Yamada, ¶¶[0005]-[0011], [0207]-[0211], [0029]. For the same and similar reasons set out with respect to the '183 Patent, a POSITA would be motivated to incorporate Yamada's teaching regarding host-initiated maintenance/copy commands. A POSITA would have had a reasonable expectation of success in incorporating this

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host command functionality—moving the copy command responsibility from SSD controller firmware to host-side software would have been straightforward and routine.

For the same and similar reasons, a POSITA would have been motivated to combine the teachings of Yamada with the system in Gonzalez-908, as Gonzalez-908 teaches that memory management responsibilities may be distributed between the host and controller, i.e., including "direct control by the host system." Gonzalez-908, ¶[0037]. Yamada represents one implementation of direct control from the host with respect to memory maintenance.

For the same and similar reasons, a POSITA would have been motivated to combine the teachings of U.S. Patent Publication No. 2011/0035536 ("Shim") and U.S. Patent No. 2011/0066789 ("Wakrat") with the systems in Gonzalez-908 or Olbrich-700. Shim and Wakrat both describe discrete implementations of shared memory management with a host system. By way of illustrative example, Shim and Wakrat describe methods and systems with certain memory management functions delegated to the host, such as wear-leveling, where this functionality is enabled due to controller sharing certain metadata with the host. Both Shim and Wakrat provide additional alternative means (to Yamada), where the controller enables host maintenance functionality. The variety of means to accomplish this same functionality is further evidence that such a combination would be obvious to try and would have a reasonable expectation of success.

3. Motivation To Combine – '614 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references in the C-Obviousness chart as they all discuss methods and systems for the improvement and optimization of NAND Flash SSD memory management. Moreover, these references are analogous because they all discuss various means of memory management relying on the generation and tracking of metadata where that metadata is updated over time and that metadata is used for activities to prolong the useful life of the memory. A POSITA would have

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been motivated to combine any of the references in C-1 to C-6 and in C-Obviousness, because the references all disclose techniques for improving the operation and management of flash memory and therefore all relate to the same technological field. A POSITA would have also been motivated to combine these references because they cite to one another and/or to references involving similar subject matters and problems

Memory management systems in SSDs typically rely on and combine ideas from different references to iteratively achieve the superior functionality—and reflect discrete implementable improvements in the field of memory management—based on known techniques in the art. Accordingly, a POSITA would be motivated to combine the contributions in any of the references in C-1 to C-6 and in C-Obviousness, and variations thereof, to incorporate various forms of metadata and the utility of said metadata, e.g., the use of maintenance metadata for maintenance activities, in order to increase efficiency and memory system longevity. These combinations would also have been a combination of prior art elements according to known methods and obvious to try given that there were a finite number of identified, predictable solutions in the prior art. Moreover, these combinations would have been the result of applying known techniques to a known method – that was ready for improvement – to yield predictable results.

To the extent any reference fails to disclose a management command, it would have been obvious in view of the references in C-1 to C-6 and in C-Obviousness. A POSITA would have understood that management operations are essential for flash memory to maintain data integrity and ensure consistent performance over time. Management operations such as wear leveling, bad block management, and garbage collection help prevent premature degradation of memory cells. Without these operations, flash memory would suffer from reduced lifespan, increased error rates, and slower read/write speeds. For instance, a POSITA would be motivated to implement

management commands related to wear leveling to extend the lifespan of the device by distributing write and erase cycles evenly across all memory cells. Since flash memory has a limited number of program/erase (P/E) cycles, frequently rewriting to the same physical locations can cause those cells to wear out prematurely. Wear leveling algorithms monitor usage patterns and help ensure that the memory ages at a similar rate. Similarly, a POSITA would understand that a storage device may be improved by implementing garbage collection to consolidate valid data from partially used blocks into new blocks, then erases the old blocks to free up space. This process is crucial for maintaining write performance and maximizing the storage efficiency of flash memory devices. And because flash memory can include bad blocks from the factor or that are developed over time due to wear and repeated program/erase cycles, a POSITA would have been motivated to improve a storage device by implementing bad block detection and management. As a final example, refreshing data is an important maintenance operation in flash memory because it helps preserve data integrity over time, especially in cells that are infrequently accessed. Flash memory cells can lose charge gradually due to leakage, which may lead to data retention errors if the data is not periodically rewritten or "refreshed," such that a POSITA would have been motivated to refresh blocks or data that have not been written to in a long time.

To the extent any reference fails to disclose that the management command is sent from a host, it would have been obvious in view of the references in C-1 to C-6 and in C-Obviousness. A POSITA would have understood that host-issued management operation can account for host information and conditions and can help reduce the load on the memory controller. The prior art also includes express teachings, suggestions and motivations to modify a storage device so that a management command is sent by a host to the storage device.

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For instance, Son explains that an SSD can include a "controller and firmware" for performing "data management operations," such as "wear leveling"—and other operations, such as "address remapping," "garbage collection," etc. Son, ¶[0013]. Son states that "the inventors have discovered that the failure of conventional SSDs to incorporate file system information" (from the host) "into their operational logic often results in inefficiencies." *Id*. Son also discloses that moving some or all of the management operations to the host helps "relieve the SSD controller and firmware of these responsibilities." *Id*., ¶[0063]. Thus, Son discloses that Ellis-102 can be improved by configuring an "SDD module" of a host to perform management operations to "help improve the performance of the SSD array." *Id*., ¶¶[0017], [0021].

As yet a further example, Jung teaches that an SSD may be improved by sharing the management functions between the host and controller. Jung discloses a system for "cooperative memory management," and teaches that in some SSDs "all FTL functions" (e.g., "wear-leveling") are performed in the flash controller, and that the "resources of the flash controller are generally smaller than those of hosts" such that it can lead to problems with "execution speed" and the controller becoming "overloaded." Jung, ¶¶[0003]-[0005]. Thus, Jung discloses that these system can be improved by implementing "some or all of the software modules for executing the FTL functions" in the host, such that the "host issues at least one command to the memory card device" to perform management operations. Jung, ¶¶[0041], [0007] ("a host in signal communication with the memory card device, wherein the host assumes at least one memory management function for the memory card device.").

As a further example, Yamada discloses that "data maintenance" operations "require[] a certain amount of power consumption" and that "conventional techniques fail to consider the device conditions" when maintenance is performed. Yamada, ¶[0010]. Yamada teaches that to

"solve this problem" it moves certain management operations to the host, such as wear leveling. *Id*., ¶¶[0011], [0030]. Thus, Son, Jung, and Yamada all provide an express teaching, suggestion, and motivation for modifying a device like Ellis-102 so that one or more management commands for the superblocks are issued by the host.

To the extent any reference fails to disclose bad block detection as a result of issuing an erase command, it would have been obvious in view of the references in C-1 to C-6 and in C-Obviousness. The prior art recognizes the importance of bad block detection, and a POSITA would have recognized that erasure performance can help identify bad blocks, such that integrating bad block detection with erasure improves efficiency and accuracy. *See, e.g.*, U.S. Patent 9,423,970 at 6:31-7:18. For instance, a POSITA would have understood that detecting bad block during erasure is desirable because where a "block needs more than predetermined number of erase cycles applied to fully erase the block," it is an indication that the block has failed and should be marked bad. *Id*.

To the extent any reference fails to disclose returning to the host zone information in response to a host query, it would have been obvious in view of the references in C-1 to C-6 and in C-Obviousness. The prior art provides express teachings, suggestions and motivations to make this modification so that the host system may utilize the information to optimize storage and issue management commands. For instance, a POSITA would understand the need to return information about the zones so they may be evaluated and optimized when choosing where to write data and as part of management operations. Son, ¶¶[0047]-[0048], [0064], [0090], Figs. 6-7; Sinclair-996, ¶¶[0099]-[0100]; Takeo, Abstract ("problem" to be solved is the need to "efficiently transfer internal information within a flash memory system," such as information about "zones," "to the host system side in response to a request from the host system side"). By the time of the '614

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Patent, it was understood that information about the zones could be returned in many ways, such as by defining a vendor specific host query command. *See* Sinclair-996, ¶[0101] ("There are many ways in which these parameters may be read by the host. One example is to define a vendor specific command that is issued by the host 211 to the memory device 207"), Son, ¶¶[0046]-[0047]; Takeo, ¶¶[0045]-[0046].

To the extent any reference fails to disclose multi-plane write that concurrently to two or more erase units and use a common page address, it would have been obvious in view of the references in C-1 to C-6 and in C-Obviousness. Multi-plane command were well-known in the art by the time of the '614 Patent. Hu, §1.3 ("SSD manufacturers have provided advanced commands, such as… multi-plane…"), §2.2 ("Multi-plane command activates multiple read, program or erase operations in all planes of the same die"), Fig. 4. And the prior art includes express teachings, suggestions and motivations to implement multi-plane commands using a common page address to improve performance of the storage device and allow for "parallel" operations. Ellis-102, 5:32-52; Olbrich-137, 2:41-43, Sinclair-996, ¶¶62-65, 76. Indeed, the prior art explains that "multi-plane command" where the "blocks executing a multi-plane" command have the "same … page addresses" had already been implemented by SSD manufacturers (Hu, §2.2) and that such techniques "improve the performance of SSD by handling read, write and erase operations more efficiently" (Hu, §1.3, "Advanced commands"). The prior art also confirms that at the time "parallelism" was "regarded as a key to achieving the peak performance" of an SSD (Hu, §1.4, "SSD parallelism").

To the extent any reference fails to disclose a storage controller that tracks when a metadata threshold is exceeded (e.g., amount of time since the zone was written to or the erasure count) and then recommends that the host send a management command in response, it would have been

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obvious in view of the references in C-1 to C-6 and in C-Obviousness. As mentioned above, a POSITA would have understood the importance of performing maintenance operations in an SSD. Tracking the amount of time since the zone was written to or the erasure count are basic metadata that a POSITA would have understood should be evaluated when determining when to refresh data or perform wear leveling. The prior art also discloses the benefits of sharing management responsibility between a controller and host such that the host is responsible or scheduling and issuing maintenance commands at optimal times. A POSITA would also understand that a vendor may not want to expose performance characteristics to the host. Because different memory devices may have different characteristics such that the optimal threshold for triggering a maintenance command may differ across devices, a POSITA would have found it obvious for the memory controller to determine whether a threshold has been exceeded internally and then simply notify the host so as to avoid having to expose these characteristics to the host device or expose the hose to the complexities associated with different thresholds for different devices.

4. Motivation To Combine – '801 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references in the D-Obviousness chart as they all discuss methods and systems for the improvement and optimization of NAND Flash SSD memory management. Moreover, these references are analogous because they all discuss various means of memory management relying on the generation and tracking of metadata where that metadata is updated over time and that metadata is used for activities to prolong the useful life of the memory. A POSITA would have been motivated to combine any of the references in D-1 to D-5 and in D-Obviousness, because the references all disclose techniques for improving the operation and management of flash memory and therefore all relate to the same technological field. A POSITA would have also been motivated

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to combine these references because they cite to one another and/or to references involving similar subject matters and problems.

Memory management systems in SSDs typically rely on and combine ideas from different references to iteratively achieve the superior functionality—and reflect discrete implementable improvements in the field of memory management—based on known techniques in the art. Accordingly, a POSITA would be motivated to combine the contributions in any of the references in D-1 to D-5 and in D-Obviousness, and variations thereof, to incorporate various forms of metadata and the utility of said metadata, e.g., the use of maintenance metadata for maintenance activities, in order to increase efficiency and memory system longevity. These combinations would also have been a combination of prior art elements according to known methods and obvious to try given that there were a finite number of identified, predictable solutions in the prior art. Moreover, these combinations would have been the result of applying known techniques to a known method – that was ready for improvement – to yield predictable results.

To the extent any reference fails to disclose a maintenance request, it would have been obvious in view of the references in D-1 to D-5 and in D-Obviousness. A POSITA would have understood that maintenance requests are essential for flash memory to maintain data integrity and ensure consistent performance over time. Maintenance operations such as wear leveling, bad block management, and garbage collection help prevent premature degradation of memory cells. Without these operations, flash memory would suffer from reduced lifespan, increased error rates, and slower read/write speeds. For instance, a POSITA would be motivated to implement maintenance request related to wear leveling to extend the lifespan of the device by distributing write and erase cycles evenly across all memory cells. Since flash memory has a limited number of program/erase (P/E) cycles, frequently rewriting to the same physical locations can cause those

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cells to wear out prematurely. Wear leveling algorithms monitor usage patterns and help ensure that the memory ages at a similar rate. Similarly, a POSITA would understand that a storage device may be improved by implementing garbage collection to consolidate valid data from partially used blocks into new blocks, then erases the old blocks to free up space. This process is crucial for maintaining write performance and maximizing the storage efficiency of flash memory devices. And because flash memory can include bad blocks from the factor or that are developed over time due to wear and repeated program/erase cycles, a POSITA would have been motivated to improve a storage device by implementing bad block detection and management. As a final example, refreshing data is an important maintenance operation in flash memory because it helps preserve data integrity over time, especially in cells that are infrequently accessed. Flash memory cells can lose charge gradually due to leakage or the program state of flash memory cells can be changed due to interference between memory cells, which may lead to data retention errors if the data is not periodically rewritten or "refreshed," such that a POSITA would have been motivated to refresh blocks or data that have not been written to in a long time.

To the extent any reference fails to disclose that the maintenance request is sent from a host, it would have been obvious in view of the references in D-1 to D-5 and in D-Obviousness. A POSITA would have understood that host-issued maintenance operation can account for host information and conditions and can help reduce the load on the memory controller. The prior art also includes express teachings, suggestions and motivations to modify a storage device so that a maintenance request s sent by a host to the storage device.

For instance, Sinclair-562 explains that when its storage address re-mapping detects a need for more white blocks in the bank, a flush operation needs to be initiated to move valid data from a pink block so that pink blocks become white blocks available for writing data. Sinclair-562,

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¶[0065]. A block information table (BIT) containing lists of block addresses for white, pink and other types of DLBA address blocks is maintained to assist in this maintenance, and its flush maintenance operation is performed when initiated by a host activity or when a host "flush cache" command occurs, or may also be interleaved in response to host commands. *Id.*, ¶¶[0082], [0112].

As a further example, Yamada discloses that "data maintenance" operations "require[] a certain amount of power consumption" and that "conventional techniques fail to consider the device conditions" when maintenance is performed. Yamada, ¶[0010]. Yamada teaches that to "solve this problem" it moves certain management operations to the host, such as wear leveling. Yamada, ¶¶[0011], [0030].

As a further example, Ahwal explains that its system controller may shift certain operations to the host media management layer (MML) including mapping, wear leveling, data ordering, pre-fetch, garbage collection, block management, and data buffering. Ahwal, ¶[0024], Fig. 4. As one example, Ahwal explains that "Block management 414 is another exemplary host operation 402 that may be part of the MML 104 at the host 102 [and] may include the localized management of blocks. For example, block management may include maintenance of a bad block list, as well as keeping track of free blocks and used blocks. Block management may further include the control and usage of SLC and MLC blocks." *Id.*, ¶[0030]. Thus, Ahwal and Yamada both provide an express teaching, suggestion, and motivation for modifying a device like Sinclair-562 so that one or more maintenance request for the megablocks are issued by the host.

Moreover, such cooperation of memory maintenance between a controller and a host was known in the art at the time, and other references also teach that a storage system may be improved by having the host issue management requests. For instance, Jung discloses a system for "cooperative memory management" and teaches that moving some or all management functions

to the host can increase "execution speed" and avoid the controller becoming "overloaded." Jung, ¶¶[0003]-[0005], [0007], [0041]. Similarly, Son explains that a storage device that performs "management operations," such as "address remapping" or "garbage collection," can be improved by having the host issue the management command so that it may "incorporate file system information" and "relieve the SSD controller and firmware of these responsibilities." Son, ¶¶[0013], [0063]. Thus, Son discloses that a device like Sinclair-996 can be improved by configuring a host to issue management request, thereby "improv[ing] the performance of the SSD array." Son, ¶¶[0017], [0021]. Thus, *Sinclair, Yamada, Jung, and Son* all provide an express teaching, suggestion, and motivation for modifying a device like Sinclair-562 so that a maintenance request, such as a flush operation, is issued by the host.

A POSITA would also have had a reasonable expectation of success in combining Sinclair-562 and Yamada because it represents a straightforward implementation of issuing maintenance requests, such as Sinclair's flush operation, from a host device. Indeed, Sinclair-562 already teaches and suggests that that its disclosures encompass performing maintenance operations on the host or the memory controller. *See* Sinclair-562, Fig. 11 (address remapping on the memory controller), Fig. 12 (moved to the host).

To the extent any reference fails to disclose returning to the host information in response to a host query, it would have been obvious in view of the references in D-1 to D-5 and in D-Obviousness. The prior art provides express teachings, suggestions and motivations to make this modification so that the host system may utilize the information to optimize storage and issue maintenance request. For instance, a POSITA would understand the need to return information about the zones so they may be evaluated and optimized when choosing where to write data and as part of maintenance operations, manage obsolete data, or update its management table such as

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the block information table (BIT). Sinclair-562, ¶¶58-78, 84; Ahwal ¶30 (media management layer (MML) and block management). By the time of the '801 patent, it was understood that information about the zones could be returned in many ways, such as by shifting management to the host. *See* Ahwal ¶30.

To the extent any reference fails to disclose the additional types of metadata, it would have been obvious in view of the references in D-1 to D-5 and in D-Obviousness, as they teach additional types of useful metadata along with the uses and benefits of that metadata for maintenance activities and a POSITA could implement the additional types of metadata with a reasonable expectation of success. For example, Olbrich-137 already describes systems with the infrastructure to generate, track and store metadata, and a POSITA would need only incorporate additional types of metadata into that pre-existing structure—adding additional useful metadata represents routine work that is well-understood and predictable. Given the maintenance specific utility of the metadata described in the art, its inclusion would be obvious to try. Indeed, the references acknowledge the flexibility and tailor-ability of system metadata. And, in light of the teaching in Exs. D1-D5 regarding the shortcomings of systems which rely solely on the controller for maintenance, and the benefits of maintenance responsibilities shared between the host and the controller, it would be obvious to a POSITA incorporate the discrete implementations of shared host and memory management taught therein. A POSITA could implement the additional discrete types of shared host and controller memory management with a reasonable expectation of success because the incorporation of discrete aspects of shared responsibility merely requires the transposing of certain data and logic from the firmware of the controller to the software of the host. Such relocation of functions from the controller to the host represents routine work that is well-understood and predictable combinations.

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For example, a POSITA would have been motivated to combine the teachings of Yamada with Olbrich-137. Yamada involve similar techniques to solve the same problem, *i.e.*, collecting, storing and using metadata for maintenance activities to improve the efficiency, performance and "integrity of data" in NAND flash memory systems. *E.g.*, Yamada, ¶¶[0005]-[0011], [0207]-[0211], [0029]. For the same and similar reasons set out with respect to the '801 Patent, a POSITA would be motivated to incorporate Yamada's teaching regarding host-initiated maintenance/copy commands. A POSITA would have had a reasonable expectation of success in incorporating this host command functionality—moving the copy command responsibility from SSD controller firmware to host-side software would have been straightforward and routine.

5. Motivation To Combine – '656 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references in the E-Obviousness chart as they all discuss methods and systems for the improvement and optimization of address translation and memory management for NAND Flash SSDs. Moreover, these references are analogous because they all discuss various means of logical-to-physical address translation, primarily two-step address translation or address translation with intermediate addresses. Further, the references tackle the same management problems of bad block management and garbage collection. A POSITA would have been motivated to combine any of the references in E1 to E4 in E-Obviousness, because the references all disclose techniques for address translation and memory management of a NAND Flash SSD and therefore all relate to the same technological field.

Address translation, bad block management, and garbage collection systems for flash memory typically rely on and combine ideas from different references to iteratively achieve the superior functionality based on known techniques in the art. Accordingly, a POSITA would be motivated to combine the above-identified contributions, and variations thereof, to incorporate

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various forms of logical-to-physical address translation, bad block management, and garbage collection to not only improve address translation speed and memory cost, memory system longevity, and memory capacity, respectively. These combinations would also have been a combination of prior art elements according to known methods and obvious to try given that there were a finite number of identified, predictable solutions in the prior art. Moreover, these combinations would have been the result of applying known techniques to a known method – that was ready for improvement – to yield predictable results.

For example, a person of ordinary skill in the art would have been motivated to combine any of memory systems and methods disclosed in Exs. E1-E3 with Ex. E4, ZBC. ZBC describes an up-and-coming SCSI standard. SCSI is a common standard used for all hardware storage devices. For the sake of interoperability, the systems and methods for storage devices described in the other references would be expected to accept commands from a SCSI standard. Ensuring interoperability of NAND Flash SSDs with common storage device command sets is an explicit motivation for some of the references. *See* Ban, 1:52-62, 3:52-4:10; Reiter, 7:9-18. Moreover, flash-memory-specific command sets, such as NVMe, have provided references for translating SCSI commands to the flash-memory-specific command set. *See* "NVM Express: SCSI Translation Reference" Rev. 1.3 (Sep. 23, 2014), https://www.nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_3_20140923_Gold.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.2 (Mar. 17, 2014), https://nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_2_03172014.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.0b (Jun. 2013), https://www.nvmexpress.org/wp-content/uploads/2013/06/NVM-Express-SCSI-Translation-Reference-1.0b.pdf. It would be obvious to a POSITA to combine a SCSI standard ZBC with the

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flash storage systems and methods disclosed in Exs. E1-E3, because SCSI is a common command specification for storage devices. And interoperability with such standards is expected of flash memory systems.

A POSITA could implement flash memory systems and methods to accept commands from SCSI standards with a reasonable expectation of success. A POSITA would understand that flash memory can be abstracted out to a block device or otherwise fit the mold of a SCSI storage device. Some of the flash memory specifics can be managed internally, while providing an interface to accept block-device or SCSI commands. This is not unlike abstracting out the particulars of a hard disk drive to provide a block-device or SCSI interface. As previously stated, a block-device or SCSI interface is expected of flash memory, where some of the flash memory references explicitly refer to acceptance of basic storage device command sets, including SCSI standards. *See* Ban, 1:52-62, 3:52-4:10; Reiter, 7:9-18. Also as previously stated, NVMe provides a reference to translate SCSI commands to work under the NVMe standards. *See* "NVM Express: SCSI Translation Reference" Rev. 1.3 (Sep. 23, 2014), https://www.nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_3_20140923_Gold.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.2 (Mar. 17, 2014), https://nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_2_03172014.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.0b (Jun. 2013), https://www.nvmexpress.org/wp-content/uploads/2013/06/NVM-Express-SCSI-Translation-Reference-1.0b.pdf.

As another example, a person of ordinary skill in the art would have been motivated to combine any of memory management systems and methods disclosed in Exs. E3-E4 with Ex. E1 Ban (U.S. Pat. No. 5,404,485) and/or Ex. E2 Reiter (U.S. Pat. No. 8,301,861). Ban and Reiter

both describe flash memory storage devices. A POSITA would understand that all flash memory storage devices have unique problems with bad blocks and garbage collection. Compared to other memory systems, flash memory experiences worse wear and tear as cells are re-written over and over again. The memory cells become unreliable and cause the flash blocks to be defective (i.e., bad blocks). For instance, this problem is expressed in Reiter, which uses a "bad block indicator" to track bad blocks. Reiter, 9:26-51. Similarly, compared to other memory systems, flash memory experiences worse fragmentation and more stale data, requiring more sophisticated garbage collection, because memory cells cannot be re-written freely. For instance, a group of memory cells, called a flash block, must be erased prior to re-writing any single memory cell in the flash block. Because re-writing to a completely new block is less costly, stale data tends to stick around longer and pile up. A POSITA would be motivated to combine these two primary flash-memory references with the bad block management systems found in other references to improve resiliency and increase the lifespan of the storage device. Additionally, a POSITA would be motivated to combine these two primary flash-memory references with more sophisticated garbage collection systems found in other references to reduce delay from these operations and reduce fragmentation and stale data.

A POSITA could implement other bad-block-management and garbage collection systems with a reasonable expectation of success. Ban and Reiter at most mention the need for these systems, or at most referring to these systems at a high level. Given the modularity of these systems, Ban and Reiter provide room for incorporation of other bad-block-management and garbage collection systems. And given the commonality of bad-block, fragmentation, and stale-data problems and importance of sophisticated maintenance for flash memory, inclusion or testing

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of various solutions would be obvious to try. In light of the need for such implementations described in the art, it would be obvious and well-understood to incorporate these teachings.

6. Motivation To Combine – '657 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references in the E-Obviousness chart as they all discuss methods and systems for the improvement and optimization of address translation and memory management for NAND Flash SSDs. Moreover, these references are analogous because they all discuss various means of logical-to-physical address translation, primarily two-step address translation or address translation with intermediate addresses. Further, the references tackle the same management problems of bad block management and garbage collection. A POSITA would have been motivated to combine any of the references in Exs. F1-F5 and in F-Obviousness, because the references all disclose techniques for address translation and memory management of a NAND Flash SSD and therefore all relate to the same technological field.

Address translation, bad block management, and garbage collection systems for flash memory typically rely on and combine ideas from different references to iteratively achieve the superior functionality based on known techniques in the art. Accordingly, a POSITA would be motivated to combine the above-identified contributions, and variations thereof, to incorporate various forms of logical-to-physical address translation, bad block management, and garbage collection to not only improve address translation speed and memory cost, memory system longevity, and memory capacity, respectively. These combinations would also have been a combination of prior art elements according to known methods and obvious to try given that there were a finite number of identified, predictable solutions in the prior art. Moreover, these combinations would have been the result of applying known techniques to a known method—that was ready for improvement—to yield predictable results.

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For example, a person of ordinary skill in the art would have been motivated to combine any of memory systems and methods disclosed in Exs. F1-F4 with Ex. F5, ZBC. ZBC describes an up-and-coming SCSI standard. SCSI is a common standard used for all hardware storage devices. For the sake of interoperability, the systems and methods for storage devices described in the other references would be expected to accept commands from a SCSI standard. Ensuring interoperability of NAND Flash SSDs with common storage device command sets is an explicit motivation for some of the references. *See* Ban, 1:52-62, 3:52-4:10; Reiter, 7:9-18. Moreover, flash-memory-specific command sets, such as NVMe, have provided references for translating SCSI commands to the flash-memory-specific command set. *See* "NVM Express: SCSI Translation Reference" Rev. 1.3 (Sep. 23, 2014), https://www.nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_3_20140923_Gold.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.2 (Mar. 17, 2014), https://nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_2_03172014.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.0b (Jun. 2013), https://www.nvmexpress.org/wp-content/uploads/2013/06/NVM-Express-SCSI-Translation-Reference-1.0b.pdf. It would be obvious to a POSITA to combine a SCSI standard ZBC with the flash storage systems and methods disclosed in Exs. F1-F4, because SCSI is a common command specification for storage devices. And interoperability with such standards is expected of flash memory systems.

A POSITA could implement flash memory systems and methods to accept commands from SCSI standards with a reasonable expectation of success. A POSITA would understand that flash memory can be abstracted out to a block device or otherwise fit the mold of a SCSI storage device. Some of the flash memory specifics can be managed internally, while providing an interface to

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accept block-device or SCSI commands. This is not unlike abstracting out the particulars of a hard disk drive to provide a block-device or SCSI interface. As previously stated, a block-device or SCSI interface is expected of flash memory, where some of the flash memory references explicitly refer to acceptance of basic storage device command sets, including SCSI standards. *See* Ban, 1:52-62, 3:52-4:10; Reiter, 7:9-18. Also as previously stated, NVMe provides a reference to translate SCSI commands to work under the NVMe standards. *See* "NVM Express: SCSI Translation Reference" Rev. 1.3 (Sep. 23, 2014), https://www.nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_3_20140923_Gold.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.2 (Mar. 17, 2014), https://nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_2_03172014.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.0b (Jun. 2013), https://www.nvmexpress.org/wp-content/uploads/2013/06/NVM-Express-SCSI-Translation-Reference-1.0b.pdf.

As another example, a person of ordinary skill in the art would have been motivated to combine any of memory management systems and methods disclosed in Exs. F3-F5 with Ex. F1 Ban (U.S. Pat. No. 5,404,485) and Ex. F2 Reiter (U.S. Pat. No. 8,301,861). Ban and Reiter both describe flash memory storage devices. A POSITA would understand that all flash memory storage devices have unique problems with bad blocks and garbage collection. Compared to other memory systems, flash memory experiences worse wear and tear as cells are re-written over and over again. The memory cells become unreliable and cause the flash blocks to be defective (*i.e.*, bad blocks). For instance, this problem is expressed in Reiter, which uses a "bad block indicator" to track bad blocks. Reiter, 9:26-51. Similarly, compared to other memory systems, flash memory experiences worse fragmentation and more stale data, requiring more sophisticated garbage

collection, because memory cells cannot be re-written freely. For instance, a group of memory cells, called a flash block, must be erased prior to re-writing any single memory cell in the flash block. Because re-writing to a completely new block is less costly, stale data tends to stick around longer and pile up. A POSITA would be motivated to combine these two primary flash-memory references with the bad block management systems found in other references to improve resiliency and increase the lifespan of the storage device. Additionally, a POSITA would be motivated to combine these two primary flash-memory references with more sophisticated garbage collection systems found in other references to reduce delay from these operations and reduce fragmentation and stale data.

A POSITA could implement other bad-block-management and garbage collection systems with a reasonable expectation of success. Ban and Reiter at most mention the need for these systems, or at most referring to these systems at a high level. Given the modularity of these systems, Ban and Reiter provide room for incorporation of other bad-block-management and garbage collection systems. And given the commonality of bad-block, fragmentation, and stale-data problems and importance of sophisticated maintenance for flash memory, inclusion or testing of various solutions would be obvious to try. In light of the need for such implementations described in the art, it would be obvious and well-understood to incorporate these teachings.

7. Motivation To Combine – '995 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references in the E-Obviousness chart as they all discuss methods and systems for the improvement and optimization of address translation and memory management for NAND Flash SSDs. Moreover, these references are analogous because they all discuss various means of logical-to-physical address translation, primarily two-step address translation or address translation with intermediate addresses. Further, the references tackle the same management problems of bad

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block management and garbage collection. A POSITA would have been motivated to combine any of the references in G1 to G4 and in G-Obviousness, because the references all disclose techniques for address translation and memory management of a NAND Flash SSD and therefore all relate to the same technological field.

Address translation, bad block management, and garbage collection systems for flash memory typically rely on and combine ideas from different references to iteratively achieve the superior functionality based on known techniques in the art. Accordingly, a POSITA would be motivated to combine the above-identified contributions, and variations thereof, to incorporate various forms of logical-to-physical address translation, bad block management, and garbage collection to not only improve address translation speed and memory cost, memory system longevity, and memory capacity, respectively. These combinations would also have been a combination of prior art elements according to known methods and obvious to try given that there were a finite number of identified, predictable solutions in the prior art. Moreover, these combinations would have been the result of applying known techniques to a known method—that was ready for improvement—to yield predictable results.

For example, a person of ordinary skill in the art would have been motivated to combine any of memory systems and methods disclosed in Exs. G1-G3 with Ex. G4, ZBC. ZBC describes an up-and-coming SCSI standard. SCSI is a common standard used for all hardware storage devices. For the sake of interoperability, the systems and methods for storage devices described in the other references would be expected to accept commands from a SCSI standard. Ensuring interoperability of NAND Flash SSDs with common storage device command sets is an explicit motivation for some of the references. *See* Ban, 1:52-62, 3:52-4:10; Reiter, 7:9-18. Moreover, flash-memory-specific command sets, such as NVMe, have provided references for translating

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SCSI commands to the flash-memory-specific command set. *See* "NVM Express: SCSI Translation Reference" Rev. 1.3 (Sep. 23, 2014), https://www.nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_3_20140923_Gold.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.2 (Mar. 17, 2014), https://nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_2_03172014.pdf; "NVM Express: SCSI Translation Reference" Rev. 1.0b (Jun. 2013), https://www.nvmexpress.org/wp-content/uploads/2013/06/NVM-Express-SCSI-Translation-Reference-1.0b.pdf. It would be obvious to a POSITA to combine a SCSI standard ZBC with the flash storage systems and methods disclosed in Exs. G1-G3, because SCSI is a common command specification for storage devices. And interoperability with such standards is expected of flash memory systems.

A POSITA could implement flash memory systems and methods to accept commands from SCSI standards with a reasonable expectation of success. A POSITA would understand that flash memory can be abstracted out to a block device or otherwise fit the mold of a SCSI storage device. Some of the flash memory specifics can be managed internally, while providing an interface to accept block-device or SCSI commands. This is not unlike abstracting out the particulars of a hard disk drive to provide a block-device or SCSI interface. As previously stated, a block-device or SCSI interface is expected of flash memory, where some of the flash memory references explicitly refer to acceptance of basic storage device command sets, including SCSI standards. *See* Ban, 1:52-62, 3:52-4:10; Reiter, 7:9-18. Also as previously stated, NVMe provides a reference to translate SCSI commands to work under the NVMe standards. *See* "NVM Express: SCSI Translation Reference" Rev. 1.3 (Sep. 23, 2014), https://www.nvmexpress.org/wp-content/uploads/NVM_Express_-_SCSI_Translation_Reference-1_3_20140923_Gold.pdf;

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As another example, a person of ordinary skill in the art would have been motivated to combine any of memory management systems and methods disclosed in Exs. G3-G4 with Ex. G1 Ban (U.S. Pat. No. 5,404,485) and Ex. G2 Reiter (U.S. Pat. No. 8,301,861). Ban and Reiter both describe flash memory storage devices. A POSITA would understand that all flash memory storage devices have unique problems with bad blocks and garbage collection. Compared to other memory systems, flash memory experiences worse wear and tear as cells are re-written over and over again. The memory cells become unreliable and cause the flash blocks to be defective (*i.e.*, bad blocks). For instance, this problem is expressed in Reiter, which uses a "bad block indicator" to track bad blocks. Reiter, 9:26-51. Similarly, compared to other memory systems, flash memory experiences worse fragmentation and more stale data, requiring more sophisticated garbage collection, because memory cells cannot be re-written freely. For instance, a group of memory cells, called a flash block, must be erased prior to re-writing any single memory cell in the flash block. Because re-writing to a completely new block is less costly, stale data tends to stick around longer and pile up. A POSITA would be motivated to combine these two primary flash-memory references with the bad block management systems found in other references to improve resiliency and increase the lifespan of the storage device. Additionally, a POSITA would be motivated to combine these two primary flash-memory references with more sophisticated garbage collection

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systems found in other references to reduce delay from these operations and reduce fragmentation and stale data.

A POSITA could implement other bad-block-management and garbage collection systems with a reasonable expectation of success. Ban and Reiter at most mention the need for these systems, or at most referring to these systems at a high level. Given the modularity of these systems, Ban and Reiter provide room for incorporation of other bad-block-management and garbage collection systems. And given the commonality of bad-block, fragmentation, and stale-data problems and importance of sophisticated maintenance for flash memory, inclusion or testing of various solutions would be obvious to try. In light of the need for such implementations described in the art, it would be obvious and well-understood to incorporate these teachings.

C. No Secondary Considerations Or Objective Indicia Of Non-Obviousness

Objective indicia of non-obviousness include: (1) commercial success, (2) copying, (3) industry praise, (4) skepticism, (5) long-felt but unsolved need, and (6) failure of others. *See*, *e.g.*, *Transocean Offshore Deepwater Drilling, Inc. v. Maersk Drilling U.S., Inc.*, 699 F.3d 1340, 1349–56 (Fed. Cir. 2012). Samsung is not aware of any evidence that would tend to establish any secondary considerations of non-obviousness. This lack of evidence further renders the Asserted Claims obvious. Proving any such secondary considerations is Radian's burden. *See*, *e.g.*, *ZUP, LLC v. Nach Mfg., Inc.*, 896 F.3d 1365, 1373 (Fed. Cir. 2018) ("[A] patentee bears the burden of production with respect to evidence of secondary considerations of nonobviousness."). Accordingly, Samsung reserves all rights regarding its full contention in this respect until after Radian completes its final and binding disclosure of any such evidence and contentions. In the meantime, Samsung note the complete lack of any such evidence in the record.

Radian has disclosed no evidence of, and Samsung knows of no viable evidence to suggest:

The alleged invention's commercial success. The industry has moved away from and did not fully adopt products alleged to practice the Asserted Claims, i.e., incorporate the NVMe ZNS Standard. Nor has Radian presented evidence of commercial success via a licensing program.

To the extent Radian asserts that Samsung's products practice the Asserted Patents, Samsung denies that assertion and incorporates its responses to date and any future contentions, expert reports, and testimony. Further, Samsung knows of no nexus between any commercial success and the Asserted Claims. *See, e.g.*, *Windsurfing Int'l Inc. v. AMF*, 782 F.2d 995 (Fed. Cir. 1986) (considerations such as intervening, non-covered technological innovations, popularity of accessories, and advertising expense are all relevant to the nexus determination).

If any commercial success is due to any of the concepts discussed in the Asserted Patents, those concepts are also present in the prior art, as described above, and thus do not support any commercial success that is relevant to the question of obviousness. *See Tokai Corp. v. Easton Enters, Inc.*, 632 F.3d 1358, 1369–70 (Fed. Cir. 2011) ("If commercial success is due to an element in the prior art, no nexus exists."); *In re Huai-Hung Kao*, 639 F.3d 1057, 1068 (Fed. Cir. 2011) ("Where the offered secondary consideration actually results from something other than what is both claimed and novel in the claim, there is no nexus to the merits of the claimed invention."); *Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1312 (Fed. Cir. 2006) ("[I]f the feature that creates the commercial success was known in the prior art, the success is not pertinent.").

Long felt but unresolved needs. Radian has presented no evidence of any long felt and unresolved need. To the contrary, multiple solutions to the alleged problems pre-dated the Asserted Claims. Further to the contrary, to the extent Radian claims that the Asserted Claims are practiced by products that are complaint with the NVMe ZNS Standard, given that this standard was not widely adopted by the industry no long felt but unresolved need was met.

Industry praise. There is also no evidence of industry praise for the alleged invention of the Asserted Claims. To the extent any praise is related to any functionality that allegedly practices the Asserted Claims, that praise is not due to any novel features of the Asserted Patents, but instead only to features present in the prior art, which is not a sufficient nexus to be relevant to the question of industry praise for purposes of obviousness. *See Muniauction, Inc. v. Thomson Corp.*, 532 F.3d 1318, 1328 (Fed. Cir. 2008). Praise of Samsung's mobile phones and features is not praise of the Asserted Patents.

Unexpected results. No evidence of any such unexpected results is known. As discussed above, the concepts contained in the Asserted Claims were already combined in the same manner as in those claims. These prior art systems, as described in the above-referenced exhibits, disclosed the same combination of elements, and the same result of that combination, that is recited in the claims. Thus, there were no unexpected results that arose from combining the well-known elements in the Asserted Claims.

The failure of others. No evidence of any such failure is known, and no such failure is associated with a problem that was first solved by the Asserted Claims.

Skepticism by experts. No experts or person of skill expressed skepticism about implementing the alleged inventions.

Teaching away by others. No evidence of any such teaching is known.

Recognition of a problem. As discussed above, the industry recognized the problem and had already discussed multiple approaches that implemented the Asserted Claims to solve that problem.

Copying of the alleged invention by competitors. No evidence of any such copying is known. *See Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1366 (Fed. Cir. 2001) (allegedly copied feature must be an embodiment of the patented claims).

VII. INVALIDITY UNDER 35 U.S.C. § 112

Pursuant to the Order Governing Proceedings, Samsung identifies below grounds of invalidity under 35 U.S.C. § 112.

A. Legal Background Regarding The Indefiniteness, Enablement, And Written Description Requirements

Section 112, ¶ 2 includes a definiteness requirement: "[T]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2. "[A] patent is invalid for indefiniteness if its claims, read in light of the patent's specification and prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014).

The definiteness requirement requires that the claim set forth what the applicant regards as the invention, and do so with sufficient particularity and definiteness. *Allen Eng'g Corp. v. Bartell Indus.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002). Where it would be apparent to one of skill in the art, based on the patent specification, that the "invention" set forth in a claim is not what the patent applicant regarded as the invention, the claim is invalid. *Id.*

35 U.S.C. § 112 further includes an enablement requirement: "The specification shall contain a written description . . . of the manner and process of making and using [the invention] in such full, clear, concise and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same." 35 U.S.C. § 112, ¶ 1. To satisfy the enablement requirement, the disclosure "must teach those skilled in the art how

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to make and use the full scope of the claimed invention without 'undue experimentation.'" *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1366 (Fed. Cir. 1997); *MagSil Corp. v. Hitachi Glob. Storage Techs., Inc.*, 687 F.3d 1377, 1381 (Fed. Cir. 2012); *Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 999 (Fed. Cir. 2008). If a specification teaches away from a substantial portion of the claim or does not enable the full scope of the claim, there is no enablement. *AK Steel Corp. v. Sollac*, 344 F.3d 1234 (Fed. Cir. 2003); *see also MagSil Corp.*, 687 F.3d at 1383-84 (Fed. Cir. 2012).

35 U.S.C. § 112 further includes a written description requirement: "The specification shall contain a written description of the invention . . . ." 35 U.S.C. § 112, ¶ 1. "To satisfy the written description requirement, a patent applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention." *ICU Medical Inc. v. Alaris Medical Systems, Inc.*, 558 F.3d 1368, 1377 (Fed. Cir. 2009) (internal quotation marks and citations omitted); *see also Synthes USA, LLC v. Spinal Kinetics, Inc.*, 734 F.3d 1332, 1340 (Fed. Cir. 2013). "The test [for written description support] requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed." *Ariad Pharmaceuticals, Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc).

The specification must describe the claimed invention in sufficient detail so that a POSITA can recognize what is claimed. "The appearance of mere indistinct words in a specification or a claim, even an original claim, does not necessarily satisfy that requirement." *University of Rochester v. G.D. Searle & Co.*, 358 F.3d 916, 923 (Fed. Cir. 2004) (internal quotation marks and citations omitted).

B. Invalidity Grounds Under 35 U.S.C. § 112

Based on Radian's Infringement Contentions, and subject to the reservations set out above, Samsung identifies grounds upon which it contends that the Asserted Claims are invalid for failure to meet the requirements of 35 U.S.C. § 112. Although its investigation continues, Samsung believes that the Asserted Claims identified below are invalid for failure to comply with 35 U.S.C. § 112 for at least the following reasons: (1) the common specification of the Asserted Patents lacks a written description of the alleged inventions of the Asserted Claims in full, clear, concise, and exact terms as required by 35 U.S.C. § 112; and/or (2) the specifications of the Asserted Patents do not enable the Asserted Claims as required by 35 U.S.C. § 112; (3) one or more of the Asserted Claims fail to specify the scope of the claimed inventions with reasonable particularity as required under 35 U.S.C. § 112. Samsung specifically reserves the right to amend and/or supplement these Invalidity Contentions based on a failure to comply with the requirements of 35 U.S.C. § 112, including, for example, based on supplementation or amendments to Radian's deficient Infringement Contentions.

The Asserted Claims fail to meet the written description requirement because the alleged inventions claimed therein are not sufficiently described in the specifications of the Asserted Patents. Specifically, the Asserted Claims fail to meet the written description requirement for at least the terms identified below because, based on those terms, the specifications of the Asserted Patents do not adequately convey to those skilled in the art that the inventors had possession of the claimed subject matter as of the filing date. The Asserted Claims additionally fail to meet the enablement requirement because the specifications of the Asserted Patents do not describe the manner and process of making and using the alleged inventions in the Asserted Claims to enable a person of skill in the art to make and use the full scope of the alleged invention without undue experimentation. Specifically, the Asserted Claims fail to meet the enablement requirement for at

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least the terms identified below because the specifications of the Asserted Patents do not describe the manner and process of making and using the alleged invention in the Asserted Claims. Based on Samsung's present understanding of the Asserted Claims and Radian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112 because the precise scope of at least the phrases listed below (or terms contained therein) cannot be determined with reasonable certainty by a POSITA when reading the claims in light of the specification and prosecution history.

The Asserted Claims fail the requirements of 35 U.S.C. § 112 in view of at least the following claim terms and phrases:

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
'183 Patent		
All claims	"subdivisions, each of the subdivisions corresponding to a respective group of erase blocks"	Lack of Written Description; Lack of Enablement; Indefinite
All claims	"logic to"	Lack of Written Description; Indefinite
All claims	"page utilization of the specific one of the subdivisions"	Lack of Written Description; Lack of Enablement; Indefinite
All claims	"the write request accompanied by an address that designates a specific one of the subdivisions"	Lack of Written Description; Lack of Enablement; Indefinite
All claims	"the erasure request accompanied by the address corresponding to the specific one of the subdivisions, to responsively control erasure of each unerased erase block in the group	Lack of Written Description; Lack of Enablement; Indefinite

[5] Includes unlisted claims that depend from listed claims.

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
	respective to the specific one of the subdivisions"	
All claims	"designates a specific one of the subdivisions"	Lack of Written Description; Lack of Enablement; Indefinite
Claims 2, 14	"wherein the host interface is also to receive a data copy request from the host, wherein the memory controller is to responsively retrieve data from a source location in the flash memory, the source location associated with the specific one of the subdivisions,"	Lack of Written Description; Lack of Enablement; Indefinite
Claims 9, 19	"to assign a write destination in the flash memory, in which data accompanying the write request is to be stored, the write destination corresponding to the specific one of the subdivisions,"	Lack of Written Description; Lack of Enablement; Indefinite
Claim 12	"represents a remaining space of the specific one of the subdivisions that is available for writing without first erasing the specific one of the subdivisions"	Lack of Written Description; Lack of Enablement; Indefinite
'772 Patent		
All claims	"divide the flash memory into zones; wherein the zones are non-overlapping subdivisions of the flash memory, each zone comprises two or more erase units, the erase units in at least one zone are on two or more different planes"	Lack of Written Description; Lack of Enablement; Indefinite
All claims	"each zone is associated with a zone start logical block address and a range of logical block addresses"	Lack of Written Description; Lack of Enablement; Indefinite

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
All claims	“using a common page address for the respective erase units on the different planes”	Lack of Written Description; Lack of Enablement; Indefinite
All claims	“metadata based on accessing and maintenance of erase units in the specified zone”	Lack of Written Description; Lack of Enablement; Indefinite
All claims	“make a notification available to the host that recommends performing maintenance on the specified zone, wherein the recommendation is associated with the zone start logical block address of the specified zone”	Lack of Written Description; Lack of Enablement; Indefinite
All claims	“logic” terms, including “logic coupled to,” “logic operates,” “logic further operates”	Lack of Written Description; Indefinite
Claim 5	"identify the zone start logical block address associated with the specified zone for which maintenance is recommended"	Lack of Written Description; Lack of Enablement; Indefinite
Claim 6	"transmit to the host (a) information representing a list of host accessible zones including a zone start logical block address for each listed zone, and (b) a host accessible capacity for each listed zone"	Lack of Written Description; Lack of Enablement; Indefinite
Claim 7	"the logic operates to generate an address offset from the write command which corresponds to a location within a sequential range of locations that corresponds to the integer number of erase units"	Lack of Written Description; Lack of Enablement; Indefinite
Claim 8	"each read command directed to the SSD is accompanied by a logical read address, each logical read address has	Lack of Written Description; Lack of Enablement; Indefinite

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
	a first address portion which identifies one of the zones according to a value of the first portion, and a second address portion which identifies a physical memory location in the SSD in a manner that depends on the first address portion"	
Claim 9	"transmit, to the host, information identifying the number of zones and sizes of the zones"	Lack of Written Description; Lack of Enablement; Indefinite
Claim 17	"a maintenance command from the host directed to the zone start logical block address of the specified zone"	Lack of Written Description; Lack of Enablement; Indefinite
Claim 22	"in response to a write command from the host to the zone start logical block address of the specified zone: assign a logical block address within the range of logical block addresses of the specified zone, transfer data from the host to the specified zone at the assigned logical block address, and return the assigned logical block address to the host"	Lack of Written Description; Lack of Enablement; Indefinite
Claim 28	"transmit to the host the zone start logical block address and a state of the specified zone"	Lack of Written Description; Lack of Enablement; Indefinite
'614 Patent		
All claims	"zone"	Lack of Written Description; Lack of Enablement; Indefinite
All claims	"common page address"	Lack of Written Description; Lack of Enablement; Indefinite

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Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
All claims	"flash memory divided into zones, each zone of the zones being a subdivision comprising a set of erase units"	Lack of Written Description; Lack of Enablement; Indefinite
All claims	"logical operable to" / "the logic"	
Claims 1-20	"wherein each zone: is associated with a logical address range, has a zone size for which the storage device is operable to receive a management command from a host that results in the storage device performing an erasure of one or more erase units of the set of erase units, is in a full state when there are no host accessible pages available for writing, and is in an empty state when all host accessible pages are available for writing" (Claims 1-9) / "wherein each zone: is associated with a logical address range, has a zone size associated with a management command from a host, transitions to a full state in response to no longer having host accessible pages available for writing, and in response to the storage device receiving the management command associated therewith, transitions to an empty state such that all host accessible pages are available for writing" (Claims 10-20)	Lack of Written Description; Lack of Enablement; Indefinite
Claims 1-20	"return information about the zones in response to a query command from the host, the information about the zones comprising a list of the zones accessible by the host, a zone state, the zone size, logical addresses associated with respective zones, and information representing an extent to which the respective zones include	Lack of Written Description; Lack of Enablement; Indefinite

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
	host accessible pages available for writing" (Claims 1-9) / "return information about zones stored by the storage device in response to a query command from the host, the information about the zones comprising: a list of the zones accessible by the host, a respective logical address associated with a zone of the zones stored, the zone size, information indicating, for respective zones in which there are no host accessible pages available for writing the respective zone, that the respective zones are in the full state, and information representing, for respective zones, an extent to which the respective zones include host accessible pages available for writing" (Claims 10-20)	
Claims 1-20	"has a zone size for which the storage device operable to receive a management command from a host" (Claims 1-9) / "has a zone size associated with a management command from a host" (Claims 10-20)	Lack of Written Description; Lack of Enablement; Indefinite
Claim 2	"after writing data to the set of erase units of the specified zone using the multi-plane write command, the storage device is operable to update a state of the specified zone to the full state"	Lack of Written Description; Lack of Enablement; Indefinite
Claim 4	"the zone size is a minimum memory size associated with the management command"	Lack of Written Description; Lack of Enablement; Indefinite
Claims 21-30	"zones are each associated with a respective logical address range"	Lack of Written Description; Lack of Enablement; Indefinite

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
Claims 21-30	"storage arranged to retain information about the zones, the information about the zones comprising zone size, a logical address associated with a zone of the zones, and information representing an extent to which the zone of the zones comprises host accessible pages available for writing; and logic operable to cause the storage device to output the information about the zones in response to a query command from a host"	Lack of Written Description; Lack of Enablement; Indefinite
Claims 23-25	"the state of the zone is a full state when the zone has no host accessible pages available for writing the zone" (Claim 23) / the state of the zone is updated to the full state in response to the zone having no host accessible pages available for writing the zone after writing to the set of erase units of the zone of the zones using the common page address (Claim 24) / The storage device of claim 22, wherein the state of the zone is an empty state when all host accessible pages of the zone are available for writing. (Claim 25)	Lack of Written Description; Lack of Enablement; Indefinite
'801 Patent		
All claims	information	Lack of Written Description; Lack of Enablement; Indefinite
All claims	memory controller	Lack of Written Description; Lack of Enablement; Indefinite
All claims	circuitry	Lack of Written Description; Lack of Enablement; Indefinite

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
All claims	logic	Lack of Written Description; Indefinite
All claims	map non-overlapping ranges of logical addresses to respective subdivisions of physical storage in the NAND flash memory, each of the respective subdivisions comprising erase blocks	Lack of Written Description; Lack of Enablement; Indefinite
All claims	update information, for the specific one of the respective subdivisions, representing an extent to which the erase blocks of the specific one of the respective subdivisions are full,	Lack of Written Description; Lack of Enablement; Indefinite
All claims	store information, responsive to detection of the condition, wherein the information is accessible to the host and indicates that the condition was detected;	Lack of Written Description; Lack of Enablement; Indefinite
Claim 1	a next available storage location within the specific one of the respective subdivisions	Lack of Written Description; Lack of Enablement; Indefinite
Claim 1	store a value representing a size of the NAND flash memory that is to be physically erased in fulfilling a maintenance request issued by the host	Lack of Written Description; Lack of Enablement; Indefinite
Claims 2-3	the metadata comprises information representing an age-since-write of data stored in the specific one of the respective subdivisions and the memory controller also comprises logic to, responsive to the identification of the condition, control copying of data associated with an age-since-write greater than a threshold to a new physical storage location in the NAND flash memory.	Lack of Written Description; Lack of Enablement; Indefinite

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
Claims 4, 6	the information that indicates that the condition was detected is sent to the host responsive to the query and is to provide to the host with at least one address associated with the specific one of the respective subdivisions.	Lack of Written Description; Lack of Enablement; Indefinite
Claim 9	the metadata is a function of data error in the data being characterized; and	Lack of Written Description; Lack of Enablement; Indefinite
Claim 12	the metadata comprises information representing an age-since-write of data stored in the specific one of the respective subdivisions; and	Lack of Written Description; Lack of Enablement; Indefinite
Claim 14	and to transmit information to the host that identifies that a storage location in the specific one of the respective subdivisions has experienced the failure condition.	Lack of Written Description; Lack of Enablement; Indefinite
Claim 15	transmit to the host a notification of a write failure and logical address information identifying the given one of the respective subdivisions corresponding to the one of the erase blocks for which the failure condition has been detected.	Lack of Written Description; Lack of Enablement; Indefinite
Claims 21-22	the NAND flash memory comprises physical planes, wherein the specific one of the respective subdivisions comprises erase blocks that are in respective ones of the physical planes; and	Lack of Written Description; Lack of Enablement; Indefinite

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
'656 Patent		
All claims	"identify an addressed segment within the addressed block device from the second address portion"	Lack of Written Description; Lack of Enablement
All claims	"identify an addressed storage location within the addressed segment from the third address portion"	Lack of Written Description; Lack of Enablement
All claims	"wherein the circuitry is to use a division operation to identify a logical erase unit within the addressed segment"	Lack of Written Description; Lack of Enablement
Claim 6	"the storage device further comprises circuitry to transmit information to a host dependent on said tracked metadata"	Lack of Written Description; Lack of Enablement
Claim 7	"the storage device is to assign an address value in association with fulfillment of each of the write requests, in order to identify a physical storage location in which associated write data has been stored, and comprises circuitry to transmit information representing each assigned address value to the host"	Lack of Written Description; Lack of Enablement
Claim 7	"for one of the incoming data access requests which is directed to data which has been written into the flash memory pursuant to one of the write requests, the addressed storage location identified from the third portion is dependent on the assigned address value which was transmitted to the host in association with the one of the write requests"	Lack of Written Description; Lack of Enablement

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
'657 Patent		
All claims	"use a first division operation on the second address portion, to identify an addressed segment within the addressed block device, wherein the addressed segment corresponds to a subset of the erase units of the flash memory"	Lack of Written Description; Lack of Enablement
All claims	"for each of the data write requests, identify from the first division operation a third address portion, and use a second division operation on the third address portion to identify an address value to select one of the erase units from the subset which corresponds to the addressed segment and to identify a storage location within the selected one of the erase units"	Lack of Written Description; Lack of Enablement
All claims	"wherein said circuitry is also to execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests"	Lack of Written Description; Lack of Enablement
Claim 14	"responsive to detection of a condition that a specific one of the values representing time since data was programmed has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations	Lack of Written Description; Lack of Enablement

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
	associated with the specific one of the values"	
Claim 15	"responsive to the query, compare the metadata to at least one threshold, to identify specific metadata, and transmit information to the host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata"	Lack of Written Description; Lack of Enablement
'995 Patent		
All claims	"identify an addressed segment within the addressed block device from the second address portion"	Lack of Written Description; Lack of Enablement
All claims	"identify an addressed storage location within the addressed segment from the third address portion"	Lack of Written Description; Lack of Enablement
All claims	"wherein the circuitry is to use a division operation on at least one of the incoming address information or information derived therefrom, to identify a logical erase unit within the addressed segment"	Lack of Written Description; Lack of Enablement
Claim 6	"the storage device further comprises circuitry to compare the metadata to at least one threshold and, responsive to detection that specific metadata has satisfied the at least one threshold, to transmit information to a host wherein such transmitted information conveys address information for data stored at a physical storage location associated with the specific metadata"	Lack of Written Description; Lack of Enablement

Asserted Claims[5]	Claim Term	Invalidity Based on 35 U.S.C. § 112
Claim 6	"the copy of data by the storage device from the first one of the physical erase units to the second one of the physical erase units is dependent on the transmitted information"	Lack of Written Description; Lack of Enablement
Claim 15	"the storage device further comprises circuitry to selectively transmit to the host information which is dependent upon the second metadata"	Lack of Written Description; Lack of Enablement
Claim 21	"the storage device further comprises circuitry to compare the metadata to at least one threshold and, responsive to detection that specific metadata has satisfied the at least one threshold, to transmit information to a host wherein such transmitted information conveys address information for data stored in a physical storage location associated with the specific metadata prior to the copy of the data to the second one of the physical erase units"	Lack of Written Description; Lack of Enablement

Samsung reserves the right to modify, amend, or supplement its contentions relating to 35 U.S.C. § 112 as the case progresses, including in view of any claim construction orders entered by the Court in this matter.

VIII. INVALIDITY UNDER 35 U.S.C. § 101

The Asserted Claims are also invalid under 35 U.S.C. § 101. The named inventors of the Asserted Patents did not invent the claimed subject matter. Instead, the named inventors, and the individuals associated with filing and prosecuting the Asserted Patents failed to identify the proper named inventors while attempting to draft claims purportedly covering ZNS.

35 U.S.C. § 101 states that "[w]hoever invents … may obtain a patent … ." The named inventors of the Asserted Patents are not the inventors of the Asserted Patents, and the named inventors failed to identify the proper inventors while attempting to obtain claims that they now allege cover ZNS. The Asserted Patents were filed after the ZNS technical proposal or publication of the ZNS on May 18, 2021 and the earlier ZNS draft publications and presentations from 2020.[6] On information and belief, Radian was aware of ZNS and ZNS specification (including drafts) prior to filing one or more of the Asserted Patents and attempted to draft the Asserted Claims to track ZNS, and not the specifications of the Asserted Patents, despite knowing that the written description lacked support for such claims. For instance, while discovery is still in its early stages, Radian has conceded that "Radian and its prosecution counsel were aware of and possessed" the "NVM Express Command Set Specification 1.0 was first published on May 18, 2021" when prosecuting the Asserted Patents. *See* Radian's Response to Samsung's Interrogatory No. 11. While Samsung disputes that the Asserted Patents cover the ZNS specification or ZNS products, to the extent the allegations in Radian's Infringement Contentions are credited the named inventors of the Asserted Patents include those at NVMe responsible for the ZNS specification.

IX. DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS

With these Invalidity Contentions and Subject Matter Eligibility Contentions, Samsung produces the documents required under Local Patent Rule 3-4 and the Standing Order Regarding Subject Matter Eligibility Contentions Applicable to All Patent Infringement Cases Assigned to Chief District Judge Rodney Gilstrap, as ordered on 25 July, 2019.

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[6] *See, e.g.,* https://blog.westerndigital.com/nvme-spec-ratification-zns-ssd/ (article describing NVM Express 1.4 Ratified TP as available for download in June 2020); https://lwn.net/Articles/823154/ (same); https://blocksandfiles.com/2020/06/26/storage-salade-nicoise-with-teradata-in-the-cloud-wd-zoned-ssds-and-more/ (same).

Dated: June 18, 2025 *<u>/s/ Kevin Hardy</u>*

Melissa R. Smith
Texas State Bar No. 24001351
melissa@gillamsmithlaw.com
GILLAM & SMITH, LLP
303 South Washington Avenue
Marshall, Texas 75670
Phone: (903) 934-8450
Fax: (903) 934-9257

Sean Pak
California Bar No. 219032 (admitted *pro hac vice)*
seanpak@quinnemanuel.com
QUINN EMANUEL URQUHART & SULLIVAN, LLP
50 California Street, 22nd Floor
San Francisco, CA 94111
Tel: 415-875-6600
Fax: 415-875-6700

Kevin Hardy
D.C. Bar No. 473941 (admitted in E.D. Tex.)
kevinhardy@quinnemanuel.com
QUINN EMANUEL URQUHART & SULLIVAN, LLP
1300 I Street, N.W., Suite 900
Washington, DC 20005
Tel: 202.538.8000
Fax: 202.538.8100

Lance Yang
California Bar No. 260705 (admitted in E.D. Tex.)
lanceyang@quinnemanuel.com
Arian Koochesfahani
California Bar No. 344642 (admitted *pro hac vice*)
ariankoochesfahani@quinnemanuel.com
QUINN EMANUEL URQUHART & SULLIVAN, LLP
865 South Figueroa Street, 10th Floor
Los Angeles, CA 90017
Tel: (213) 443-3000
Fax: (213) 443-3100

Counsel for Defendants Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.

CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and Local Rule CV-5, I hereby certify that, on June 18, 2025, all counsel of record who have appeared in this case are being served with a copy of the foregoing via email.

Dated: June 18, 2025 *<u>/s/ Joseph LeRoy</u>*
Joseph LeRoy

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