

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

RADIAN MEMORY SYSTEMS, LLC,
Patent Owner.

Case IPR2025-01289
Patent 11,681,614

EXHIBIT 2020

DECLARATION OF DR. MARK JONES

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I. INTRODUCTION

1. My name is Mark Jones. I have been retained as an expert witness to provide my independent opinion in regard to the matters at issue in *inter partes* review of U.S. Patent No. 11,681,614 (“the ’614 patent”) in IPR2025-001289. I have been retained by Radian Memory Systems, LLC (“Radian” or “Patent Owner”), the Patent Owner in this proceeding. Petitioner is Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (“Samsung” or “Petitioner”).

2. I am being compensated \$750 per hour for my time spent working in connection with this case. My compensation is in no way related to the outcome of this litigation. If called as a witness, I would testify as to the statements and opinions contained in this report.

3. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

II. QUALIFICATIONS

4. I graduated summa cum laude from Clemson University in 1986 with a B.S. in Computer Science and a minor in Computer Engineering, while holding a National Merit Scholarship and the R. F. Poole Scholarship. I graduated from Duke University in 1990 with a Ph.D. in Computer Science, while holding the Von Neumann Fellowship.

5. Upon graduation, I joined the Department of Energy at its Argonne National Laboratory facility. While at the Department of Energy, I received the IEEE Gordon Bell Prize.

6. In 1994, I joined the Computer Science faculty at the University of Tennessee. While at the University of Tennessee, I received a CAREER Award from the National Science Foundation.

7. In 1997, I joined the Electrical and Computer Engineering faculty at Virginia Tech. I was cited multiple times on the College of Engineering's Dean's List for teaching.

8. In 2021, I became a Professor Emeritus of Electrical and Computer Engineering at Virginia Tech.

9. During my academic career, my teaching included courses on computer architecture and computer organization. These classes frequently covered topics specific to storage systems and more specifically to flash storage systems—including, for example, the division of responsibility for storage management between software and hardware on a host system and software and hardware on an embedded controller. My research has also at times involved the integration of flash storage into various computer architectures.

10. In addition to the activities, education, and professional experience listed above, I have been involved in research projects that contribute to my expertise

relating to this report. While at Virginia Tech, for example, I was a primary or co-investigator on government and industrial research grants and contracts in excess of five million dollars.

11. A detailed record of my professional qualifications is set forth in the attached Exhibit A, which is my *curriculum vitae*, including a list of publications, awards, research grants, and professional activities. My *curriculum vitae* also lists the matters in which I have served as an expert.

III. BASES OF OPINION

12. In the course of conducting my analysis and forming my opinions, I have reviewed materials including those listed below:

- i. The Petition filed by Petitioner in IPR2025-01289,
- ii. U.S. Patent No. 11,681,614 (“’614 Patent”) (Ex. 1001);
- iii. The prosecution history of the ’614 Patent (Ex. 1002);
- iv. The Declaration of Dr. Heiner Litz in IPR2025-01289 (Ex. 1003) (the “Litz Declaration” or “Litz-Decl.”);
- v. U.S. Patent No. 9,239,781 (“Ellis”) (Ex. 1004);
- vi. U.S. Pub. No. 2012/0096217 (“Son”) (Ex. 1005)¹;

¹ Although the Petition refers to Sinclair and Son as Exhibits “1005” and “1006,” respectively, *see, e.g.*, Pet., vi, Petitioner marked and submitted these

- vii. International Publication No. WO 2008/082996 (“Sinclair”) (Ex. 1006);
- viii. U.S. Pub. No. 2008/0189485 (“Jung”) (Ex. 1007);
- ix. Yang Hu et al., Performance Impact and Interplay of SSD Parallelism through Advanced Commands, Allocation Strategy and Data Granularity (2011) (Ex. 1008);
- x. U.S. Pub. No. 2012/0303931 (“Asnaashari”) (Ex. 1009);
- xi. U.S. Patent 8,621,137 (“Olbrich”) (Ex. 1010);
- xii. Radian ’614 Infringement Contentions (Ex. 1011);
- xiii. Certified Translation of JP2008176606A (“Takeo”) (Ex. 1012);
- xiv. JP2008176606A (Ex. 1013);
- xv. Hu et al., Exploring and Exploiting Multilevel Parallelism Inside SSDs for Improved Performance and Endurance (2013) (Ex. 1014);
- xvi. U.S. Pat. Pub. No. 2011/0271032A1 (“Yamada”) (Ex. 1015);
- xvii. U.S. Pat. Pub. 2012/0284587 (“Yu”) (Ex. 1016);
- xviii. U.S. Patent No. 9,423,970 (“Darragh”) (Ex. 1017);

documents to the Board as Exhibits 1006 and 1005, respectively. I will use the numbering of the exhibits as marked and submitted to the Board with additional parentheticals in citations to avoid confusion.

xix. The exhibits and other documents cited herein.

IV. APPLICABLE LEGAL STANDARDS

A. Level Of Ordinary Skill In The Art

13. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan,” or by the acronyms “POSA,” “POSITA” or “PHOSITA,” as of the time of the invention. I understand that the ’614 patent issued on June 20, 2023, and that it claims priority to Provisional Application No. 61/757,464, which was filed on January 28, 2013.

14. I have been told that the person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. I am instructed that “relevant” means relevant to the challenged claims of the ’614 patent.

15. I understand that factual indicators of the level of ordinary skill in the art include the various prior art approaches employed, the types of problems encountered in the art, the rapidity with which innovations are made, the sophistication of the technology involved, and the educational background of those actively working in the field. I understand that, in assessing the level of skill of a person of ordinary skill in the art, one should consider the type of problems encountered in the art, the prior solutions to those problems found in the prior art

references, the rapidity with which innovations are made, the sophistication of the technology, the level of education of active workers in the field, and my own experience working with those of skill in the art at the time of the invention.

16. In this case, Dr. Litz has asserted in his declaration that a person of ordinary skill in the art as of the time of the '614 patent would have had “at least a Bachelor of Science degree in electrical engineering, or an equivalent field, and at least three years of experience with SSDs or other flash memory devices” and that “[m]ore education can supplement practical experience and vice versa.” Pet., 4-5; Ex. 1003 [Litz-Decl.] ¶ 28.

17. For the purposes of this declaration, I accept Dr. Litz’s proposed qualifications of a POSITA. I reserve the right to revisit the issue of the level of knowledge of the POSITA should the Petition be instituted.

18. As further discussed below, my opinions as stated in this declaration are valid even if the Board adopts a somewhat higher or somewhat lower level of ordinary skill in the art than proposed. For example, as will be discussed throughout my report, even a person with the level of knowledge or experience described by Dr. Litz or adopted by the Board as described above would not have a reasonable expectation of success in implementing certain aspects of the proposed combination as of the priority date of the '614 patent.

19. In this report, the absence of an expressed opinion about any section or paragraph of the Petition or Dr. Litz's declaration, does not indicate my agreement with the section or paragraph.

B. My Understanding Of Legal Standards

20. When considering the '614 patent and stating my opinions, I rely on the following legal standards as described to me by the attorneys for Radian.

21. I understand that a patent claim is unpatentable if the claimed invention was anticipated by a prior art reference or would have been obvious to a person of ordinary skill in the art at the time of the purported invention.

22. I understand that anticipation requires that every limitation of the claim at issue be disclosed, either expressly or under principles of inherency, in a single prior art reference.

23. I understand that inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. Instead, it must be proven that the claim limitation not expressly found in the reference necessarily follows from what is found there.

24. I understand that an obviousness analysis involves comparing a claim to the prior art to determine whether the claimed invention would have been obvious to a person of ordinary skill in the art at the time of the invention in view of the prior art and in light of the general knowledge in the art as a whole. I also understand that

obviousness is ultimately a legal conclusion based on underlying facts of four general types, all of which must be considered: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) any objective indicia of non-obviousness.

25. I also understand that obviousness may be established under certain circumstances by combining or modifying the teachings of the prior art. Specific teachings, suggestions, or motivations to combine any first prior art reference with a second prior art reference can be explicit or implicit, but must have existed before the date of purported invention. I understand that prior art references themselves may be one source of a specific teaching or suggestion to combine features of the prior art, but that such suggestions or motivations to combine art may come from the knowledge that a person of ordinary skill in the art would have had.

26. I understand that a reference may be relied upon for all that it teaches, including uses beyond its primary purpose, but also including teachings that lead away from the invention. I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, although the mere disclosure of alternative designs does not teach away.

27. I further understand that whether there is a reasonable expectation of success in combining references in a particular way is also relevant to the analysis.

28. I understand that it is improper to use hindsight to combine references or elements of references to reconstruct the invention using the claims as a guide. My analysis of the prior art is made from the perspective of a person of ordinary skill in the art at the time of the invention.

29. I am not offering any legal opinions in this declaration nor am I qualified to do so. I only consider such legal standards in framing my opinions and conclusions as well as placing assertions made by Petitioner in the Petition into the proper context. Additionally, from a subject matter perspective, I understand that the petitioner always has the burden of persuasion regarding a challenge of patentability of an invention under an inter partes review.

V. CLAIMS AND GROUNDS AT ISSUE

30. I understand that Petitioner has challenged the claims of the '614 patent as follows (Pet., 1):

- Claims 1-2, 4-8 based on obviousness over Ellis and Son (Ground 1);
- Claims 3, 10-14, 16-19, 21-29 based on obviousness over Ellis, Son, and Olbrich (Ground 2);
- Claims 9, 15, 20, 30 based on obviousness over Ellis, Son, Olbrich, and Yamada (Ground 3);
- Claims 1-2, 4-8 based on obviousness over Takeo, Son, and Sinclair (Ground 4);

- Claims 3, 10-14, 16-19, 21-29 based on obviousness over Takeo, Son, Sinclair, and Olbrich (Ground 5);
- Claims 9, 15, 20, 30 based on obviousness over Takeo, Son, Sinclair, Olbrich, Yamada (Ground 6).

VI. OPINIONS

A. **Petitioner Does Not Show A Motivation To Combine Ellis With Son (And Other References).**

31. I have reviewed Petitioner's Grounds 1-3, which rely upon the combination of Ellis and Son. Pet. 5-51.

32. I understand that all of Petitioner's Ellis grounds rely upon Petitioner's combination of Ellis and Son ("Ground 1") against independent claim 1. *See, e.g.*, Pet. 33-41 (Petitioner's Ground 2 referring to Petitioner's Ground 1 for all aspects of independent claims), 43-51 (Petitioner's Ground 3 addressing dependent claims only), 29-31 (Petitioner's Ground 1 relying upon its arguments as to claim 1 for all other claims challenged by this ground, which depend from claim 1). Accordingly, I have focused my analysis of Petitioner's Grounds 1-3 on Petitioner's Ground 1 argument against claim 1. I reserve the right to supplement my opinions if the Petition is instituted.

1. Petitioner Modifies Ellis Without Explanation.

33. Petitioner first begins combining Ellis with Son in connection with the limitation of claim 1 that recites a storage device “operable to receive a management command *from a host.*” Pet. 11. Petitioner identifies “wear leveling and garbage collection commands” within Ellis as alleged “management commands” in the sense of claim 1. Pet., 11. Petitioner notes that in Ellis, a flash translation layer (“FTL”) within Ellis’s memory controller “performs maintenance operations on ‘the superblocks,’ such as ‘wear leveling,’” Pet., 11. I agree with Petitioner that Ellis discloses a component within Ellis’s memory controller as responsible for operations like garbage collection and wear leveling in Ellis’s system.

34. Petitioner then says, however, that “Ellis states that *either* ‘the memory controller *[or] the host system...* can operate any of the modules and functions of the memory controller.” Pet., 11 (citing Ex. 1004 [Ellis] 4:58-65).

35. With this argument, Petitioner is proposing to modify Ellis. The disclosure in Ellis that Petitioner cites reads more fully as follows:

The functional units in the memory controller 104 can work individually and independently of the other functional units. For illustrative purposes, the memory controller 104 is described by operation of the memory controller 104 with the host system 108 and the memory array 106. It is understood that the memory controller 104,

the host system 108, and the memory array 106 can operate any of the modules and functions of the memory controller 104.

Ex. 1004 [Ellis] 4:58-65.

36. This generic statement is not specific to Ellis. The same disclosure appears, verbatim or near verbatim, in at least ten unrelated patent applications filed by the same entity that filed Ellis, including patents that list different sets of named inventors.² A POSITA would recognize this type of statement as the kind of language that is commonly used in patent applications to indicate that a patent disclosure is not necessarily limited to the specifics of the examples that it discusses. This statement does not suggest that the wear leveling and garbage collection that Ellis locates within its controller in the systems that are expressly discussed in Ellis could advantageously be moved to the host in the way proposed by Petitioner. Indeed, this disclosure, which is not specific to wear leveling or garbage collection,

² See, e.g., Ex. 2021 [U.S. Patent No. 8,949,689] 4:32-39; Ex. 2022 [U.S. Patent No. 9,021,231] 4:60-67; Ex. 2023 [U.S. Patent No. 9,098,399] 4:66-5:6; Ex. 2024 [U.S. Patent No. 9,123,445] 4:43-49; Ex. 2025 [U.S. Patent No. 9,170,941] 9:29-37; Ex. 2026 [U.S. Patent No. 9,183,137] 4:58-65; Ex. 2027 [U.S. Patent No. 9,244,519] 6:41-49; Ex. 2028 [U.S. Patent No. 9,543,025] 6:3-10; Ex. 2029 [U.S. Patent No. 9,671,962] 4:58-65; Ex. 2030 [U.S. Patent No. 10,546,648] 4:49-56.

does not generally suggest that any particular modification of the systems expressly disclosed in Ellis would be desirable.

37. Because this paragraph is the only paragraph in Ellis that Petitioner offers for its argument that Ellis discloses host-based garbage collection and wear leveling, in my opinion, Petitioner has not shown how a POSITA would be motivated by Ellis to locate the specific functions identified by Petitioner in Ellis's host, let alone that a POSITA would be motivated to do so with a reasonable expectation of success.

2. Petitioner Does Not Explain, Let Alone Motivate, How Son's "SSD Module" Is Involved In The Combined System.

38. Petitioner also suggests that the claimed "management command from a host" and "query command from [a] host," if not disclosed in Ellis, could be taught by Son (or more specifically, that disclosures within Son concerning the operation of Son's "SSD module" show how claimed "command[s]" might come "from a host" in Petitioner's combination of Ellis and Son. *See, e.g.*, Pet. 17–24 (Petitioner's Ground 1 analysis of a "query command" limitation repeatedly discussing Son's SSD module), 35 (incorporating this analysis into a challenge to independent claim 10), 39 (same, for independent claim 21). But I do not see where Petitioner identifies exactly how Ellis would be modified by Son.

39. Petitioner pairs disclosures about Son’s SSD module with statements like “[a] POSITA would be motivated to combine Son’s teachings of a host query for returning information about superblocks [zones] with Ellis’s storage device,” or the statement that “Son discloses the benefits of returning the information about zones to the host so that the host may utilize the information to issue management commands.” *See, e.g.,* Pet., 24-25. But such statements fail to identify how much (if any) of “Ellis’s storage device” remains in its combination, or how much of Son’s SSD module is present in the modified Ellis “host” of its combination, as I discuss further below.

a) *Petitioner Does Not Explain How Son’s SSD Module Is Involved In Any “management command from a host.”*

40. Claim 1 recites a storage device “operable to receive a **management command from a host.**” Petitioner identifies Ellis’s “memory system” (102 in Ellis’s Figure 1) with the claimed “storage device,” Pet. 8, Ellis’s “host system” (108 in Ellis’s Figure 1) with the claimed “host,” *see, e.g.,* Pet., 11-12, and offers wear leveling commands as examples of the claimed “management commands.” *See id.*

41. As discussed above, Ellis’s controller performs flash maintenance, not its host—as Petitioner elsewhere appears to acknowledge, *see* Pet., 11, and Petitioner’s citation of a generic disclosure about modules being “operat[ed]” by

either the controller or host does not provide a rationale for moving this functionality to the host in a modified system.

42. As an alternative attempt to show the claimed “management commands” in its combination, Petitioner points to Son’s SSD module performing “maintenance operations including garbage collection and wear leveling” for flash memory present in Son’s SSD array (145 in Son’s Figure 1). *See* Pet., 12-13. Implicitly, when Son’s SSD module initiates these operations, it does so by sending instructions to Son’s controller, which directly accesses Son’s SSD array. Petitioner suggests that the controller’s receipt of such commands from Son’s SSD module would teach the claimed “storage device operable to receive a management command from a host.” *See* Pet., 13. Petitioner further argues that Son allegedly teaches that “Ellis can be improved by configuring an ‘SSD module’ of a host to perform management operations,” Pet., 14, and that Son allegedly motivates “modifying Ellis’s device so that one or more management commands for the superblocks are issued by the host.” Pet., 15.

43. Petitioner presumably frames its proposed modification of Ellis in terms of where alleged “management commands” come from, Pet., 15, because claim 1 recites “a management command from a host.” But to frame Petitioner’s modification in these terms is to understate the technical implications of what Petitioner proposes to change in Ellis.

44. Ellis’s memory controller performs both wear leveling and garbage collection without being commanded to do so by its host, and Ellis maintains all metadata needed to carry out these operations out within its controller—as Petitioner elsewhere appears to recognize. *See, e.g.,* Pet., 11 (Petitioner observing that “Ellis discloses that *the memory controller* 104 [of Ellis’s Figure 1] can include a flash translation layer (FTL),” and that “[t]he FTL performs maintenance operations . . . such as wear leveling”) (internal quotations omitted).

45. When Petitioner proposes “modifying Ellis’s device so that one or more management commands for the superblocks are issued by the host,” Pet., 15, Petitioner does not identify the *basis* on which Ellis’s modified host would issue such commands. In particular, Petitioner does not specify whether the host in its combined system would perform wear leveling on the same bases as Ellis’s controller, using the same inputs that Ellis’s controller would use, or on the same bases as Son’s SSD module, using the same inputs that Son’s SSD module would use, or some other possibility. And Petitioner does not identify where any relevant inputs would be stored in its combination. A POSITA would understand that these are fundamental architectural choices that need to be made as part of the design of a system; they are not incidental details that a POSITA could simply fill in from Petitioner’s high-level description of where what it identifies as “management commands” in the combined system ultimately come from.

46. When Petitioner speaks of “moving . . . management *operations* to the host,” Pet. 14 (emphasis added), Petitioner does not say how this “moving” would be reflected in changes to how Ellis or Son store, update, and access relevant *inputs* to those operations. This language does not, for example, identify what data structures are used for “management operations” in the combined system—whether it is Ellis’s controller-resident data structures (used by Ellis for what Petitioner identifies as “management operations”), the tables managed by Son’s host-side SSD module (used by Son for what Petitioner identifies as “management operations”), or some unexplained hybrid of the two.

47. A POSITA would understand that modifying where *commands* to perform wear leveling and garbage collection operations come from in Ellis, from controller to host, would likely also involve shifting at least some aspects of the underlying *tasks* of wear leveling and garbage collection, from controller to host. Such a shift would likely involve, at a minimum, modifying Ellis so that its host system has access to whatever flash maintenance information the combined system uses to decide when to initiate wear leveling and garbage collection, and perhaps also other information.

48. Petitioner does not identify what information this would be, except vaguely and by implication, for example, by citation to Ellis (as an unmodified system) and to Son (as an unmodified system). As one example, Son offers “whether

one or more superblocks have a wear count above a predetermined threshold value” (Ex. 1005 [Son] [0079]) as a threshold for deciding whether to initiate wear leveling, and “whether the number of free superblocks in the SSD falls below a predetermined threshold” (Ex. 1005 [Son] [0064]) as a threshold for deciding whether to initiate garbage collection. But Petitioner does not argue that Ellis’s host system has access to these inputs in the unmodified form of Ellis. Similarly, Ellis discloses data such as “a number of times or cycles the memory devices ... associated with ... super blocks ... are programmed or erased” and “a valid-page count, but expressly locates this information inside “metadata pages” managed by a “block control module” within Ellis’s controller, not Ellis’s host system. Ex. 1004 [Ellis] 4:66-5:3 (“The memory controller . . . can include a block control module”), 11:58-67 (locating program/erase cycle counts and valid page counts in metadata pages “managed by the block control module”). And Petitioner does not say whether the host of the combined system would somehow be given access to these inputs as they are stored on Ellis’s controller (let alone how that would be done), or whether the host in the combined system would rely on other information in some other way.

49. Indeed and more generally, Petitioner fails to specify whether the “host” in its Ellis/Son combination would somehow itself maintain inputs relevant to wear leveling and garbage collection, or whether the “host” of the combined system would obtain that information in some way from Ellis’s controller (or a

modified version of Ellis's controller). Taken individually, Ellis and Son each offer different approaches to handling this issue, and Petitioner does not reconcile these differences.

50. In Ellis, inputs relevant to wear leveling and garbage collection are maintained and updated only at Ellis's controller, while in Son, a host-side "SSD module" maintains and updates this information. Petitioner's description of its combination is thus consistent with at least two architectures.

51. As one possibility, Ellis's controller could continue to track and update metadata related to wear leveling and garbage collection, as a POSITA would understand that it does in the unmodified form of Ellis. But in this case, the basis on which the modified host would issue commands for those operations is not clear. Petitioner does not, for example, identify how the host would be able to access the information it would use to issue commands relating to wear leveling or garbage collection.

52. Another possibility is that the memory controller in the combined system is effectively relieved of any responsibility for wear leveling and garbage collection in the combination. Son expressly envisions this possibility. *See, e.g.,* Ex. 1005 [Son], [0063] ("The SSD module performs various SSD maintenance operations including garbage collection and wear leveling, which can relieve the SSD controller and firmware of these responsibilities."). In this type of combination

of Ellis and Son, the “host” of the combination might more closely resemble Son’s “SSD module,” in that it would not only issue *commands* that initiate wear leveling and garbage collection, but also track and update the *inputs* used to decide when those operations take place.

53. Son expressly envisions the use of its “SSD module” with memory controllers that are not tasked with wear leveling and garbage collection, by disclosing, for example, that “[i]n some embodiments, the controller and firmware are configured differently from many conventional systems in that *they do not perform onboard garbage collection or wear-leveling*, but rely upon the SSD module to manage such operation,” Ex. 1005 [Son] [0017], and by containing a claim directed to a system where “the controller and firmware *do not include garbage collection logic or wear leveling logic*.” *Id.*, cl. 4; *see also id.* [0063] (“The SSD module performs various SSD maintenance operations including garbage collection and wear leveling, which can relieve the SSD controller and firmware of these responsibilities.”) These disclosures about “some embodiments,” of course, do not rule out the use of Son’s SSD module with controllers (like the controller in Ellis) that *do* include garbage collection and wear leveling logic.

54. In the hypothetical case of a combination in which Son’s “SSD module” entirely takes over garbage collection and wear leveling, however, it is unclear exactly what aspects of Ellis’s unmodified host system and Ellis’s unmodified

controller (if any) would remain in the combination, or why they would be retained in the combination.

55. For at least these reasons, in my opinion, Petitioner and Dr. Litz do not show how a POSITA would have been motivated to combine Ellis and Son in the way proposed by Petitioner.

b) *Petitioner Does Not Explain How Son's SSD Module Is Involved In Any "query command from the host."*

56. Petitioner also discusses aspects of the alleged motivation to combine Ellis and Son in connection with the claimed "logic to return information about the zones in response to a query command from the host"—a limitation that is present (in different wordings) in all challenged claims. *See, e.g.*, Ex. 1001 ['614] 64:61-62 (independent claim 1), 65:58-61 (independent claim 9), 67:15-18 (independent claim 21). Petitioner directly analyzes this limitation only in connection with claim 1, dealing with its appearance in other claims by reference only. *See, e.g.*, Pet., 35, 39.

57. Petitioner identifies the claimed "logic to return information about the zones" within Ellis's "memory system 102," Pet., 8 (identifying the "storage device" of claim 1 that comprises the claimed logic as Ellis's memory system), and argues that interactions between Son's "SSD module" with Son's "management tables" would teach this limitation. *See generally* Pet., 17-21.

58. Petitioner argues by analogy, in which the claimed “query command from a host” is analogized to interactions between Son’s “SSD module” and data stored in various structures. Petitioner describes various instances of Son’s SSD module accessing the contents of “management tables” as depicted (for example) in Son’s Figures 3A-3D, *see, e.g.*, Pet., 17-18 (citing Son’s Figure 3C), 20, 21-22 (citing Son’s Figure 3C), 23 (citing Son’s Figures 3B, 3D) and “management data structures” as depicted (for example) in Son’s Figure 4. Pet. 18-19.

59. Petitioner does not argue that these data structures in Son exist in Ellis’s memory system, and Petitioner never states that they would exist in Petitioner’s combination of Ellis and Son. Petitioner’s argument is presumably that because Son’s SSD module accesses these data structures in Son, a POSITA would have been motivated to task the host in Petitioner’s combination with querying some component of Ellis’s “memory system” for similar information, such that this component would “return” information from these structures “in response to a query command from the host,” as the claim recites. *See, e.g.*, Pet., 24 (arguing that “A POSITA would be motivated to combine Son’s teachings of a host query for returning information about superblocks [zones] with Ellis’s storage device”).

60. I do not agree that these disclosures in Son show why a POSITA would be motivated to modify Ellis in the way proposed by Petitioner. Indeed, Petitioner’s selective quotation from Son appears to be driven by the claim language itself, and

a desire to find something more analogous to “logic to return information about the zones in response to a query command from the host” than what can be found in unmodified Ellis. Petitioner does not, for example, identify any particular defect in Ellis that would be remedied by its proposed modification, or suggest any that particular benefit could be obtained by modifying Ellis in the way that it proposes. Petitioner does not even identify what structures in the modified system would play the role of the “management tables” in Son in Petitioner’s own analogy.

61. For at least these reasons, it is not clear how Petitioner is proposing to modify Ellis, and in my opinion, Petitioner and Dr. Litz have not shown why a POSITA would be motivated to make whatever modification they are proposing, let alone be able to do so with a reasonable expectation of success.

B. Petitioner Does Not Show That Ellis And Son Teach A Storage Device “operable to receive a management command from a host” (Ground 1, All Challenged Claims; Ground 2, All Challenged Claims Except 21-27 And 29; Ground 3, All Challenged Claims Except Claim 30).

62. Claim 1 recites a storage device “operable to receive a management command from a host that results in the storage device performing an erasure of one or more erase units.” Petitioner identifies Ellis’s “memory system” (102 in Ellis’s Figure 1) with the claimed “storage device,” Pet. 8, Ellis’s “host system” (108 in Ellis’s Figure 1) with the claimed “host,” *see, e.g.*, Pet., 11-12, and wear leveling commands as the claimed “management commands.” *See id.*

1. Ellis Does Not Teach The Claimed Management Command “from a host.”

63. Petitioner argues that “would have been obvious to *modify* Ellis’s storage system” as to teach a storage device “operable to receive a management command from a host that results in the storage device performing an erasure of one or more erase units.” Pet., 12. As Petitioner “modify” language suggests, Ellis’s unmodified system does not teach this limitation.

64. Petitioner acknowledges that in Ellis, a “flash translation layer (FTL)” within Ellis’s “*memory controller 104*”—that is, *not* Ellis’s “host system”—performs operations such as “wear leveling.” Pet., 11. Petitioner identifies these operations in Ellis with the claimed “management commands,” but only argues that Ellis teaches that these operations could come “*from a host*” from a generic disclosure in Ellis. Pet. 11 (citing Ex. 1004 [Ellis] 4:58-65). Ellis states:

[t]he functional units in the memory controller 104 can work individually and independently of the other functional units. For illustrative purposes, the memory controller 104 is described by operation of the memory controller 104 with the host system 108 and the memory array 106. It is understood that the memory controller 104, the host system 108, and the memory array 106 can operate any of the modules and functions of the memory controller 104.

Ex. 1004 [Ellis] 4:58-65.

65. In suggesting that this passage teaches what Petitioner identifies as “management commands” being sent by Ellis’s host, Petitioner ignores details of how Ellis’s system actually functions—*i.e.*, where the things that Petitioner would identify as “management commands” originate in unmodified Ellis, and how metadata relevant to flash maintenance is stored and updated in Ellis.

66. In Ellis, commands that initiate garbage collection and wear leveling originate in Ellis’s **controller**, and do not come from Ellis’s “host system.” A POSITA would certainly recognize that the flash memory system disclosed in Ellis performs garbage collection and wear leveling operations—as Petitioner’s expert recognizes. *See, e.g.*, Ex. 1003 [Litz-Decl.] ¶ 33 (describing garbage collection in section entitled “Technology Background and State of the Art” as a feature of managing solid-state drives); 35 (in the same section, describing wear leveling as “essential” in flash management)). Ellis expressly discloses, for example, that its controller keeps track of numbers of valid pages, program/erase cycles, and the like—inputs that a POSITA would understand to be important to garbage collection or wear leveling operations (again, as Petitioner’s expert would appear to generally acknowledge in the context of flash management; *see* Ex. 1003 [Litz-Decl.] ¶¶ 33-34 (describing the general role of “valid blocks” in garbage collection), 35 (discussing P/E cycles in the context of wear leveling)).

67. Although Ellis does not employ the term “garbage collection,” Ellis expressly describes its “memory access module” (which resides within Ellis’s controller, Ex. 1004 [Ellis] 4:67-5:3) as performing “recycle operations” for reasons “including freeing space and wear leveling,” Ex. 1004 [Ellis] 16:4-13), and a POSITA would recognize that garbage collection involves “freeing space.” Because Ellis never discloses any role for its host system in performing such operations (or in accessing or updating any of the relevant inputs), a POSITA would understand that flash garbage collection and wear leveling operations in Ellis are performed exclusively by Ellis’s controller, without involvement of Ellis’s host.

68. Accordingly, in my opinion, Ellis does not disclose or teach the claimed management command “from a host.”

2. Petitioner Does Not Show That Son Teaches The Claimed Management Command “from a host” In Its Combination.

69. Petitioner argues that Son teaches the claimed management command “from a host” in combination with Ellis. Petitioner cites various disclosures of Son’s “SSD module” initiating “maintenance operations including garbage collection and wear leveling” for flash memory present in Son’s SSD array (145 in Son’s Figure 1). *See* Pet., 12-13. Implicitly, when Son’s SSD module performs these operations in Son, it does so by sending instructions to the controller that manages Son’s SSD array—and according to Petitioner, the controller’s receipt of such commands from

Son's SSD module would teach the claimed "storage device operable to receive a management command from a host" in some modification of Ellis. *See* Pet., 13; *see also id.*, 14 (arguing that Son teaches that "Ellis can be improved by configuring an 'SDD module' of a host to perform management operations"), 15 (arguing that Son allegedly motivates "modifying Ellis's device so that one or more management commands for the superblocks are issued by the host").

70. As I have already discussed in connection with Petitioner's alleged motivation to combine, however, this argument never identifies how Ellis would be modified. Petitioner does not indicate, for example, which inputs relevant to alleged "management operations" in the individual references would be present in the combined system, or where they would be stored.

71. Accordingly, for at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that Ellis's combinations with Son teach the claimed management command "from a host."

C. Petitioner Does Not Show That Ellis And Son Teach Logic Operable To Return "information about the zones in response to a query command from the host" (Grounds 1-3, All Challenged Claims).

72. Claim 1 recites a storage device with logic to "return information about the zones in response to a query command from the host." In my opinion, Petitioner

does not show that this limitation is present in its combinations involving Ellis and Son.

73. Petitioner analogizes Ellis’s memory controller with the claimed “storage device,” but never argues that Ellis alone teaches this limitation. *See, e.g.,* Pet., 17 (arguing only “[t]o the extent Ellis does not expressly disclose returning the information recited in this limitation”). Petitioner argues that Son teaches this limitation, analogizing “information about ... superblocks” within Son’s “management tables,” to the claimed “information about the zones,” *see, e.g.,* Pet., 17, and analogizing Son’s “memory controller” to the claimed logic operable to return that information. *See* Pet., 18-24.

74. Petitioner’s argument that Son teaches the claimed “return[ing] information . . . in response to a query command from the host” in its combination misunderstands Son.

75. Petitioner repeatedly speaks of Son’s SSD module obtaining information from Son’s “management tables” as a result of “querying” Son’s memory controller, or as the result of Son’s memory controller “returning” such information “in response to a query.” *See, e.g.,* Pet., 18. Son does not use the term “querying” in connection with the processes that Petitioner is discussing, and Petitioner’s repeated use of the claim term “querying” does not itself establish that any such “querying” is taught by Son.

76. Petitioner repeatedly relies upon citation to Son's paragraph 47 in attempting to characterize Son's SSD module as "querying" Son's memory controller for information. *See, e.g.,* Pet., 18 (arguing that Son's SSD module retrieves information from a data structure in step 410 of Son's Figure 4 "by 'querying the controller'" in Son) (purportedly quoting Ex. 1006 [Son] [0047]), 22 (partially quoting "querying" language in Son's paragraph 47 again), 22 (citing Son's paragraph 47 as support for an argument that "Son discloses" its memory controller as "return[ing]" certain information "in response to a query from the SSD module in the host"), 24 (same). This paragraph does not disclose that Son's SSD module obtains the information that Petitioner is pointing to by "querying" its memory controller.

77. Son's paragraph 47 discusses Son's SSD module selecting a "superblock" during a write operation (at step 415 of Son's Figure 4), and reads in full as follows.

At block 415, the SSD module selects a superblock and PLBA to store the source data in order to fulfill the requested operation. When selecting the superblock, the SSD module may evaluate any combination of several factors including, as non-exhaustive examples: the volume of source data to be written, the number of free, valid and/or invalid pages in each candidate superblock, the state of each candidate superblock, the data type of the source data, the data type of data

already stored in each candidate superblock, the wear count and/or last modification time of each candidate superblock, the superblock associated with a previously-stored PLBA, the physical configuration or layout of the solid-state memory in the SSD. Other examples of factors include other recent, in-progress, or pending I/O requests received before, during, or after the current write request was received. In the case of a rewrite, the SSD module may also evaluate the previously-stored PLBA. The SSD module may determine some or all of these various factors *by accessing and analyzing the various management data structures described previously* and/or *by querying the file system or the controller*.

Ex. 1005 [Son] [0047].

78. The “various management data structures described previously” that Son refers to here are the tables described in Son’s Figures 3A-3D. *See, e.g.*, Ex. 1005 [Son] [0037]-[0043]. Petitioner identifies material within these “management data structures” as providing alleged examples of the claimed “information.” *See, e.g.*, Pet., 17 (citing Figures 3A-3D), 18 (reproducing Son’s Figure 3C), 18-19 (arguing that “retriev[ing] information from the management data structures” as in Son’s Figure 4 teaches this limitation).

79. A POSITA would understand that when Son speaks of “accessing and analyzing the various management data structures described previously *and/or* by querying the file system or the controller,” it is describing *alternative* ways in which

Son's SSD module may obtain information. In particular, a POSITA would understand that when Son speaks of its SSD module accessing and analyzing the contents of tables in its Figures 3A-3D, this occurs *without* querying Son's controller for that information.

80. Indeed, a POSITA would recognize that the ability of Son's SSD module to access and analyze information without querying its controller is an essential feature of Son's system. Son repeatedly says, for example, that one object of its design is to "mov[e] solid-state management functions above the firmware level." *See, e.g.*, Ex. 1005 [Son], Abstract, [0014]. Son also says, for example, that its system "may achieve various advantages over conventional systems" by allowing the use of "simplified SSD firmware." *See id.* A POSITA would understand this reference to "simplified" firmware to include firmware that might support basic read and write functionality but not any specialized "querying" commands for flash status information.

81. Petitioner also analogizes the garbage collection described in Son's Figure 6 with the claimed "query command from a host." Pet., 19. Partially quoting from Son's paragraph 65, Petitioner states:

Similarly, Figure 6 shows a garbage collection process that involves "identifying source superblocks and target superblocks" at step 603. [Son], Fig. 6. Son discloses that in the identify step the SSD

module evaluates “information obtained from the controller,” such as “information shown in the superblock table, other management data structures, or information obtained from the controller.” [Son], [0065].

Pet., 19.

82. I do not agree with Petitioner’s implied argument—that the “information shown in the superblock table” or the “other management data structures” referenced in Son’s paragraph 65 are examples of what Son refers to when it refers to “information obtained from the controller.” A POSITA would instead understand looking to “information shown in the superblock table” and “other management data structures” the garbage collection process of Figure 6 to be *alternatives* to what Son refers to as consulting “information obtained from the controller.”

83. Son’s paragraph 65 states:

At block 603, the SSD module identifies a source superblock and target superblocks. The SSD module may consider various combinations of factors to select the source and target superblocks, including the following such factors, as nonexhaustive examples: free page count, valid page count, invalid page count, last modification time, wear count, the data type of data stored in a superblock (e.g., metadata versus user versus raw), or any other information about superblocks (or their constituent pages, including page status or DIF header information), such as the other information shown in the superblock

table, other management data structures, *or* information obtained from the controller or file system.

Ex. 1005 [Son] [0065].

84. A POSITA would recognize this disclosure for what it is: generic, boilerplate language signaling that nothing in Son’s design strictly limits its SSD module to considering data from only one source when deciding what superblocks are to be the source or target of garbage collection. Paragraph 65 does not identify any of the information that it enumerates (or any examples that Petitioner identifies in connection with this limitation) as being obtained by querying Son’s controller. Indeed, here Son suggests that the SSD module’s use of the “superblock table” or “other management data structures” are *alternatives* to using “information obtained from the controller or file system.”

85. Elsewhere, Son makes clear that the SSD module itself maintains its “management data structures” (e.g., its page status table, mapping table, superblock table, page detail array), and a POSITA would understand that Son’s SSD module may access the information that is kept in these tables without “querying” Son’s memory controller for that purpose. *See, e.g.*, Ex. 1005 [Son], Figs. 3A-3D; [0033]-[0043].

86. For at least these reasons, in my opinion, Petitioner and Dr. Litz do not show how the proposed combination of Ellis and Son teaches a storage device

“return[ing] information about the zones in response to a query command from the host.”

D. Petitioner Does Not Show A Motivation To Combine Takeo With Son And Sinclair (And Other References).

87. All of Petitioner’s Takeo grounds rely upon Petitioner’s combination of Takeo, Son, and Sinclair (“Ground 4”) against independent claim 1. *See, e.g.*, 72-81 (Petitioner’s Ground 5 referring to Petitioner’s Ground 4 analysis of claim 1 for all aspects of independent claims), Pet. 82-85 (Petitioner’s Ground 6 discussing dependent claims only), 68-72 (all of Petitioner’s Ground 4 arguments incorporating Petitioner’s Ground 4 arguments for claim 1). Accordingly, I have focused my analysis of Petitioner’s Grounds 4-6 on Petitioner’s Ground 1 argument against claim 1. I reserve the right to supplement my opinions if the Petition is instituted.

88. In my opinion, Petitioner and Dr. Litz have not shown that a POSITA would have been motivated to make its proposed modification of Takeo.

1. Petitioner's Takeo Combinations Are Not Specified (Grounds 4-6, All Challenged Claims).

- a) *Petitioner Does Not Explain How Its Takeo Combinations Receive A "management command from a host."*³

89. Petitioner discusses aspects of its Takeo combinations when discussing the limitation of claim 1 that recites a storage device "operable to receive a management command from a host that results in the storage device performing an erasure of one or more erase units of the set of erase units." Ex. 1001 ['614] 64:53-55 (claim 1). All of Petitioner's obviousness arguments involving Takeo incorporate its Ground 4 argument as to claim 1,⁴ *see, e.g.*, Pet., 73-74, 79-80, and Petitioner admits that "Takeo does not expressly discuss management commands." Pet., 58.

90. Petitioner first attempts to implicitly address Takeo's failure to disclose any "management commands" by stating that "Son discloses the claimed

³ This argument addresses Ground 4, all challenged claims; Ground 5, all challenged claims Except 21-27 And 29, Ground 6, all challenged claims except claim 30.

⁴ While independent claims 1 and 10 contain similarly worded versions of this limitation, independent claim 21 and its dependent claims (with the exception of claim 28) do not. Petitioner does not, however, separately articulate any combinations as to the claims that do not contain this limitation.

management command”—an assertion that Petitioner supports with reference to arguments involving *Ellis* and Son. *See, e.g.*, Pet., 58. As I have discussed above, in my opinion, Petitioner and Dr. Litz did not show how its combination of *Ellis* and Son would actually issue what Petitioner identifies as “management commands.” And Petitioner does not identify any similarities between *Ellis* and Takeo that would cause any hypothetical implementation of the claimed “management commands” in *Ellis* and Son to motivate “management commands” in Petitioner’s proposed combination of Takeo and Son. I

91. Petitioner argues that “[a] POSITA would understand that a flash memory system should perform management operations such as wear leveling and garbage collection” and that “[b]ecause Takeo is silent regarding these management operations, a POSITA would look to references like Son that describe these operations.” Pet., 58. I do not agree with Petitioner’s conclusion.

92. Takeo does not use the express terms “wear leveling” or “garbage collection,” but Takeo is not agnostic as to which component of its system performs these operations: that component is Takeo’s memory controller—not its Takeo’s host. (I will return to this point below in discussing Petitioner’s argument that its combination teaches this limitation.) When Petitioner states that a POSITA would “look to references like Son that describe these operations” as Petitioner proposes, Pet., 58, therefore, this is using a secondary reference to *modify* Takeo, and not

simply (for example) to supply the details of an implementation of an embodiment of unmodified Takeo.

93. In specifically looking to Son, moreover, Petitioner looks past other references that do not locate wear leveling or garbage collection functionality at a host (let alone Son's host).

94. As one example, Petitioner's Ellis grounds cite a combination of Ellis and Son for alleged teachings of this limitation, and Petitioner acknowledges that Ellis locates this functionality at Ellis's controller. *See, e.g.,* Pet., 11 (arguing that Ellis discloses a "memory controller" that "may issue wear leveling and garbage collection commands").

95. As another example, Petitioner's Takeo combinations all involve Sinclair in combination with Son and Takeo, and Sinclair states that it is common to locate similar functionalities in a memory controller, *see, e.g.,* Ex. 1006 [Sinclair] [0083] (referring to "data consolidation and garbage collection" as "operations [that] are normally scheduled by the memory system controller to take place in the background as much as possible," and noting that "the need to perform these operations can cause the controller to have to give the host a busy status signal until such an operation is completed"). Sinclair also expressly employs a controller that can "automatically" perform similar operations. *See, e.g., id.* [00155] (addressing a situation where "the memory controller manages the physical memory in way that

automatically consolidates data from partially written blocks in order to reclaim new erased block capacity”).

96. Petitioner does not explain why any alleged silence of Takeo on wear leveling or garbage collection would, all by itself, lead a POSITA to combine Takeo with Son in the way proposed by Petitioner, when references like Sinclair or Ellis (for example) might suggest alternative approaches.

97. Even we were to assume that a POSITA would be motivated to look to Son for teachings about wear leveling and garbage collection, Petitioner does not connect what Son allegedly teaches about wear leveling and garbage collection with its proposed modification of Takeo. Petitioner states:

And as discussed above (see Ground 1, Limitation 1[a.ii]), the prior art includes express teachings, suggestions and motivations for combining Son’s disclosure of host-issued management operations to Takeo’s storage device, including that it would allow the system to incorporate device conditions in its management logic, improve execution speed, and avoid the controller becoming overloaded.

Pet., 59.

98. Petitioner’s “Ground 1” is one of Petitioner’s Ellis grounds, and does not address “combining Son’s disclosure of host-issued management operations to Takeo’s storage device.” This reference to Ellis does not identify what the “host” in the Takeo/Son combination would be.

99. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that Son would motivate a POSITA to combine Takeo with other references as proposed by Petitioner.

b) *Petitioner Does Not Explain Why A POSITA Would Modify Takeo To Return Its Alleged “information about [] zones” (Grounds 4-6, All Challenged Claims).*

100. Every challenged claim recites logic operable to return “information about [] zones ... in response to a query command from [a] host,” where the claimed “information” comprises, among other things, a “zone size,” and “logical addresses associated with respective zones” (or a “logical address associated with a zone of the zones”). *See, e.g.*, Ex. 1001 [’614] 64:60-67 (claim 1), 65:60-66:5 (independent claim 10), 67:15-22 (independent claim 21). All of Petitioner’s arguments regarding these limitations and Takeo refer back to the arguments made in Petitioner’s Ground 4 against this limitation as it appears in independent claim 1. *See, e.g.*, Pet., 74, 79 (incorporating Petitioner’s arguments for “limitation 1[b.i]”).

101. Petitioner identifies what it regards as a “zone size” and “logical addresses associated with respective zones” in Takeo, but admits that Takeo does not disclose returning a “zone size” or “logical addresses associated with respective zones” in response to a query command from a host. *See, e.g.*, Pet., 65-66. Petitioner offers two arguments that the POSITA would be motivated to modify Takeo as to satisfy this limitation. I do not agree with either argument.

102. First, Petitioner argues that “Son renders obvious returning the claimed information about the zones in response to a query command from the host for the reasons discussed in connection with Ground 1, Limitation 1[b.i],” Pet., 62. Petitioner’s “Ground 1” is an Ellis combination, not a Takeo combination. Petitioner’s Takeo Ground 4 elsewhere exclusively relies upon Takeo alone, *see, e.g.*, Pet., 55-57 (Petitioner’s limitations [1pre], [1a], [1a.i]), 62 (limitations [1a.iv] and [1b]), 68 (limitations [1b.iii] and [1c]), and expressly rely upon Takeo and Sinclair for another limitation, *see, e.g.*, Pet. 66-67 (limitation [1b.ii]). Accordingly, it is not clear how Petitioner proposes to transfer its arguments about the combination of Ellis and Son to any combination of Takeo, Son, and Sinclair.

103. Petitioner’s second argument pairs various disclosures in Takeo with disclosures in Sinclair. *See generally* Pet., 62-66. Petitioner contends that “Sinclair teaches that if the host ‘know[s] the physical characteristics of the memory with which it is operating’ ... it can avoid having files scattered across metablocks.” Pet., 66.

104. Sinclair’s “metablocks” are not Takeo’s “zones,” so the problem of having “files scattered across metablocks” does not exist in Takeo’s system. And Petitioner’s rationale for combining the systems rests upon an analogy between Sinclair’s metablocks and Takeo’s zones that does not make technological sense.

105. In more detail, claim 1 recites “[a] storage device comprising ... logic operable to[] return information about the zones in response to a query command from the host, the information about the zones comprising . . . a zone state, . . . [and] logical addresses associated with respective zones” Ex. 1001 [’614] 64:60-65. Petitioner identifies Takeo’s flash memory system (labeled 1 in Takeo’s Figure 1) as the claimed “storage device,” Pet. 55, Takeo’s host system (labeled 4 in Takeo’s Figure 1) as the claimed “host,” and Takeo’s physical zones with the claimed “zones,” Pet., 56 (citing Ex. 1012 [Takeo] ¶ 41). Petitioner states that the number of bytes in a block of one of Takeo’s physical zones determines the claimed “zone size.” Pet., 58.

106. With these identifications, Petitioner admits that Takeo does not disclose returning the claimed “zone size” or “logical addresses associated with respective zones” in response to a query from what Petitioner identifies as Takeo’s “host.” *See* Pet., 65. Petitioner argues by analogy that Sinclair teaches this limitation.

107. Petitioner states that Sinclair’s memory system exposes “the ‘number of pages per metablock’ and the ‘size of a physical page,’” as well as “the lowest logical address that is mapped to a first page of a physical metablock,” to Sinclair’s host. *See* Pet., 65. Analogizing Sinclair’s “metablocks” to Takeo’s “zones,” Petitioner argues that “[a] POSITA would have been motivated to modify Takeo to

return this information as part of Takeo's vendor internal information acquisition command," Pet., 66, purportedly because:

Sinclair discloses that when writing data files they may become "scattered among a larger number of metablocks when file boundaries are not known." [Sinclair], ¶ 86. Sinclair teaches that if the host "know[s] the physical characteristics of the memory with which it is operating" (e.g., the zone size and logical addressing information discussed above) it can avoid having files scattered across metablocks.

Pet., 66.

108. The differences Sinclair's metablocks to Takeo's "zones" make Petitioner's analogy an unnatural one, and Petitioner's analogy does not support Petitioner's proposed modification of Takeo.

109. Sinclair's "metablocks" are not the same as Takeo's "zones." Both Sinclair's "metablocks" and Takeo's "zones" are groups of individually erasable units of flash memory (Sinclair calls its units "blocks," *see, e.g.*, Ex. 1006 [Sinclair], [0062], while Takeo calls these units "erasure units," "block units," or "blocks," *see, e.g.*, Ex. 1012 [Takeo] ¶ 3). But these groups are managed differently in the two systems.

110. Sinclair discloses that the units of flash within its "metablocks" are written and erased together. Ex. 1006 [Sinclair] [0062]; *see also id.* (noting that while a "block" represents "the smallest number of memory cells that are physically

erasable together[,] [f]or increased parallelism . . . the blocks are operated in larger metablock units”). Petitioner’s reading of Sinclair expressly relies on aspect of Sinclair’s “metablocks.” Pet., 53 (stating that “‘metablocks’ . . . comprise a group of blocks across multiple planes that may be operated together (e.g., *written and erased together*)”).

111. A POSITA would understand that the units of flash that make up Takeo’s “zones,” by contrast, are not written and erased together; in particular, the fundamental unit of erasing flash memory in Takeo is a block. In the main example discussed in Takeo, there are hundreds of blocks in each of Takeo’s “zones.”

112. Takeo nowhere indicates that all blocks within a Takeo “zone” must be written to or erased as a group. Takeo expressly discloses storing information relating to block-level write operations *within individual blocks*, on the basis of *individual blocks*, clearly indicating to the POSITA that Takeo’s write operations are not limited to writing entire Takeo “zones” at a time. Ex. 1012 [Takeo] ¶ 43 (“logical address information corresponding to the data that has been written will be written to the redundant region of *the physical block where the data was written*”). A POSITA would recognize from this and other disclosures in Takeo that in Takeo’s system, blocks may be written to or erased individually.

113. A simple but plain indication to the POSITA that Takeo’s “zones” are not written to or erased as groups is the fact that Takeo’s central example is a system

with exactly eight “zones.” *See, e.g.*, Ex. 1012 [Takeo], Figure 4 (listing counts for “PZN #0” through “PZN #7”). A POSITA would not understand *any* system with only eight collectively erasable divisions of flash memory as a practical system, let alone a system appropriate for illustrating aspects of a technical disclosure like Takeo’s patent publication.

114. Managing flash on the basis of only eight units that are written and erased together is not a plausible operating model: every time such a device needed free space, it would be forced to evacuate whatever valid data still resides in a targeted zone and then erase 12.5% of the entire medium—just to continue an ordinary write that might involve far less data than 12.5% of the entire medium. The practical effect would be severe and immediate: latency would spike during each reclamation cycle, and such a device would frequently end up moving and rewriting far more data than the host actually needed to write. The cumulative effect of this method of management would accelerate wear on the flash, and any practical system would not be designed so that small host writes do not trigger enormous volumes of internal writes. Of course, Takeo is not designed that way, because Takeo’s “zones” are not written and erased together, like Sinclair’s “metablocks.” Takeo’s “zones” are more roughly analogous to higher-level administrative partitions—functionally analogous to separate volumes or drives—than a fundamental unit of writing to or reclaiming flash memory.

115. Because Takeo’s “zones” are different from Sinclair’s “metablocks,” the analogy that Petitioner uses in an attempt to motivate sending what Petitioner identifies as Takeo’s “zone size” and “logical addresses associated with respective zones” to Takeo’s host breaks down.

116. The fact that the blocks within Sinclair’s “metablocks” are all written and erased together underlies what Petitioner offers as an alleged motivation for modifying Takeo—Sinclair’s concern for “scattering” a file across multiple metablocks, which in Sinclair is addressed by host-visible metablock size information. *See* Pet. 66 (suggesting that a host with a “query command from the host” that returns a “zone size” can “avoid having files scattered across metablocks”).

117. In more detail, if a single file is spread across many of Sinclair’s metablocks, it may occur that these metablocks each hold a small amount of valid data (in the form of their respective portions of that single file) and a lot of reclaimable space. Compacting this space at the metablock level (as may happen during garbage collection) requires copying the valid portions out of each metablock and erasing each entire metablock—work that scales with the number of affected metablocks. *See, e.g.,* Ex. 1006 [Sinclair], [0081]-[0082]. Again, this is because Sinclair teaches that the units of flash within a “metablock” are erased together. As described by Petitioner, Sinclair’s system does not regain storage capacity by erasing

smaller groups of individually erasable units of flash memory (*e.g.*, individual blocks within Sinclair’s “metablocks”).

118. When Sinclair describes its host attempting to place files across smaller numbers of Sinclair’s “metablocks,” this is an attempt to mitigate what would otherwise be the increased costs of performing data compaction and garbage collection operations on the basis of its metablocks. *See, e.g.*, Ex. 1006 [Sinclair], [0006], [0067], [0078]-[0080]. This problem is not present in Takeo.

119. A POSITA would understand that compaction and garbage collection in Takeo do not implicate writing to or erasing entire Takeo “zones” at once. A POSITA would instead understand that when Takeo’s memory controller performs data compaction and garbage collection, it can write to and erase individual blocks within Takeo “zones.” What Petitioner identifies as a “zone size” in Takeo is thus not relevant to flash maintenance in Takeo in way that Sinclair’s metablock size is relevant to flash maintenance in Sinclair.

120. The quantitative difference between a “metablock” in Sinclair and a Takeo “zone” is well illustrated by an example in Takeo in which there are 1024 physical blocks (used for storing 1000 logical blocks)) in every “zone.” *See, e.g.*, Ex. 1012 [Takeo] ¶ 42. For purposes of comparison with Petitioner’s analogy to Sinclair, Sinclair’s Figure 4 offers an example in which “four blocks ... are shown to form one metablock” in Sinclair. Ex. 1006 [Sinclair] [0062]; Pet. 53 (citing this

example). If one were to use Petitioner’s analogy to “metablocks” to re-“zone” Takeo’s system of 8000 logical blocks to a system whose Takeo “zones” have only four blocks each (like Sinclair’s exemplary “metablocks”), the resulting system would employ thousands of “zones,” not eight of them. Even then, considerations applicable to “metablocks” in Sinclair would not directly apply to Takeo “zones,” for example, because in this hypothetical embodiment of Takeo system, the four blocks within a Takeo “zones” in this hypothetical would not necessarily be written and erased as a group, as “metablocks” are in Sinclair.

121. Other features of Sinclair also undercut the analogy that Petitioner draws between “zones” and “metablocks” in Sinclair.

122. As one example, Sinclair expressly contemplates systems that make use of metablocks of variable size—that is, metablocks that can have different numbers of blocks to match different kinds of workloads. *See* Ex. 1006 [Sinclair] ¶ 84. A modification of Takeo consistent with this aspect of Sinclair would not necessarily adopt the single, fixed “metablock size” that Petitioner relies on in supposedly motivating Takeo’s host returning a “zone size.”

123. As another example, Sinclair discloses an alternative interface that “eliminate[s] use of the logical address space,” i.e., a file-object interface that does not traffic in host-visible logical block addresses at all. *Id.* ¶ 87. A modification of

Takeo aligned with this aspect of Sinclair might not involve returning what “logical addresses associated with respective zones” at all.

124. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that a POSITA would be motivated to combine Takeo with Son and Sinclair in the way proposed by Petitioner.

E. Petitioner Does Not Show That Its Takeo Combinations Teach A “storage device . . . operable to receive a management command from a host” (Ground 4, All Challenged Claims; Ground 5, All Challenged Claims Except 21-27 and 29; Ground 6, All Challenged Claims Except Claim 30).

125. Claim 1 recites a storage device . . . operable to receive a management command from a host that results in the storage device performing an erasure of one or more erase units of the set of erase units.” In my opinion, Petitioner and Dr. Litz have not shown this limitation to be present in Petitioner’s Takeo combinations.

126. Petitioner admits that “Takeo does not expressly discuss management commands” and relies on Son for this limitation. Pet., 58. According to Petitioner, upon “[a]pplying Son’s teaching to Takeo, the flash memory system of Takeo would receive a management command from the host system that results in the erasure of erase units in a zone.” Pet., 58.

127. Petitioner does not expressly identify any specific “management command” in its combination of Takeo and Son and Sinclair. Petitioner’s statements that “[a] POSITA would understand that a flash memory system should perform

management operations such as wear leveling and garbage collection,” and that “Son . . . describe[s] these operations,” Pet., 58, are implicit argument that a “management command” in Petitioner’s proposed combination would relate to wear leveling or garbage collection in a modified version of Takeo.

128. Petitioner argues that “a POSITA would look to references like Son that describe” wear leveling and garbage collection because “Takeo is silent regarding these management operations.” Pet., 58.

129. Although Takeo does not use the terms “garbage collection” or “wear leveling,” a POSITA would readily understand that Takeo’s system necessarily performs garbage collection and wear leveling. As of Takeo’s 2007 filing date, these background maintenance operations were well-recognized as essential to the operation of NAND flash memory, which has limited program/erase cycles and cannot be overwritten in place—as Petitioner elsewhere appears to recognize when it says that “A POSITA would understand that a flash memory system should perform management operations such as wear leveling and garbage collection.” Pet., 58.

130. A POSITA would also understand that in Takeo’s system, it is Takeo’s controller that is tasked with wear leveling and garbage collection. Takeo’s controller is designed to interoperate with hosts that may not even be aware that they are using flash storage rather than magnetic storage. *See, e.g.*, Ex. 1012 [Takeo] ¶ 4

(noting that “memory systems using NAND flash memory are increasingly used in applications that replace the conventional magnetic disk devices” and “[f]or this reason, the interface of memory systems using NAND flash memory typically uses AT Attachment (ATA), which is used in magnetic disk devices”), Abstract (describing Takeo as providing a way “[t]o efficiently transfer internal information within a flash memory system that is connected to an ATA interface to the host system side”), [0005] (describing how host access works “even in the case of a flash memory system in which a peripheral device uses flash memory as a storage medium”), [0007] (describing the host’s use of an “ATA interface”). A POSITA would understand that such a controller could not rely on the host to direct any flash-specific housekeeping such as garbage collection and wear leveling, and that such a controller would not rely on host input for that purpose.

131. Takeo does not disclose its host as sending anything other than standard input/output commands (that is, commands to read and write data), and “vendor-specific” commands, which in Takeo are exclusively described in terms of the host requesting that status information be reported back to Takeo’s host.

132. Takeo does not disclose its host sending any commands to its controller to initiate garbage collection or wear leveling. Takeo presents its controller as receiving commands from its host via an interface that includes support for host reads, host writes, and a vendor-specific query path—the “internal-information

acquisition command”—which Takeo uses for the host to request, and the controller to report, state information. *See generally* Ex. 1012 [Takeo], Fig. 1 (depicting an ATA host/device architecture), Fig. 4 (depicting per-zone state information as can be reported back to Takeo’s host), Figs. 5-6 (flowcharts for computing/buffering and returning information via the ATA data path).

133. Because Petitioner apparently regards Son as providing details of wear leveling and garbage collection as it might already occur in an embodiment of Takeo, Petitioner does not address the fact that Petitioner’s combination with Son would actually modify this aspect of Takeo, and for at least this reason, in my opinion, Petitioner and Dr. Litz do not show how its Takeo combination teaches the claimed “storage device . . . operable to receive a management command from a host.”

F. Petitioner Does Not Show That Its Takeo Combinations Teach Logic Operable To Write To Erase Units “using a common page address” (Grounds 5-6, All Challenged Claims).

134. Dependent claim 3 and independent claims 10 and 21 (from which all other claims challenged in Grounds 5-6 depend) each recite logic to write “two or more erase units of the set of erase units of the specified zone using a common page address” (claim 3), or to write a “set of erase units of a specified zone using a common page address” (claim 10), or to write a “set of erase units of the zone of the zones using a common page address” (claim 11). *See, e.g.*, Ex. 1001 [’614] 65:17-20, 66:6-7, 67:17-19. Petitioner addresses all limitations identically, with reference

to its Ground 5 argument for dependent claim 3. *See, e.g.,* Pet., 72, 75,⁵ 80. Petitioner does not argue that this limitation is disclosed or taught by Takeo. *See id.*

135. In arguing that its combinations teach the claimed write “using a common page address,” Petitioner first argues as follows:

Sinclair renders obvious the logic is operable to write the data to the two or more erase units of the set of erase units of the specified zone. *See* Ground 4, Limitation 1[b.ii].

Pet. 73.

136. Here Petitioner’s “the logic” is a reference back to Takeo’s memory controller, which Petitioner identified in claim 1 as the “logic” of claim 1 to which 3’s “logic ... operable to write” refers back. *See* Pet., 62. Petitioner’s citation to “Ground 4, Limitation 1[b.ii]” is to the following:

Sinclair discloses that erase blocks that span multiple planes may be grouped together into a metablock [zone] and that data may be written to the set of erase blocks [sets of erase units] of a specified metablock [specified zone] using a multi-plane write command such

⁵ This reference (“See Ground 4, Claim 3”) contains a typographical error.

As Ground 4 has no such challenge, Petitioner likely means to refer to Ground 5, Claim 3.

that the data is written concurrently to two or more erase blocks of the set of erase blocks. *See* Ground 1, Limitation 1[b.ii].

Pet., 66-67.

137. Following that citation to its source, one finds mostly arguments about Ellis (because Petitioner's Ground 1 is an Ellis ground). Pet., 25-26. Petitioner also states:

To the extent Ellis does not explicitly disclose the use of a multi-plane command, it was at least obvious in view of the general knowledge of a POSITA. EX1003, ¶109. Multi-plane commands were well-known in the art. EX1014, §1.3 (“SSD manufacturers have provided advanced commands, such as... multiplane...”), §2.2 (“Multi-plane command activates multiple read, program or erase operations in all planes of the same die”), Fig. 4. The prior art includes express teachings, suggestions and motivations *to utilize a multi-plane command with Ellis’s storage device* by disclosing that the commands permit “parallel” operations and that “parallelism has been regarded as a key to achieving the peak performance.” EX1004, 5:32-52; EX1010, 2:41-43; EX1014, §1.4.

Pet., 26.

138. Although Petitioner cites this material for the proposition that “*Sinclair discloses* that erase blocks that span multiple planes may be grouped together into a metablock [zone] and that data may be written to the set of erase blocks [sets of erase units] of a specified metablock [specified zone] using a multi-plane write command

such that the data is written concurrently to two or more erase blocks of the set of erase blocks,” Pet., 66-67, I do not see how Sinclair discloses this limitation, or how the above argument shows how Sinclair would teach this limitation.

139. Petitioner argues that “[m]ulti-plane commands were well-known in the art,” Pet., 26 (citing Ex. 1007), quotes Ellis to the effect that “parallelism has been regarded as a key to achieving the peak performance.” I do not see how these statements show that Petitioner’s Takeo combination teaches a multi-plane write “using a common page address.” A POSITA would generally recognize, for example, that it is possible for a flash storage system to perform a multi-plane write while using a common page address, and that it is also possible for a flash storage system to perform a multi-plane write without using a common page address. There is nothing inherent in the general concept of a multi-plane write, or a general desire to leverage unspecified benefits of “parallelism,” that mandates the use of a common page address.

140. Petitioner separately argues that Olbrich teaches this aspect of its Takeo combinations. Pet., 72-73. Petitioner argues:

As discussed above, Olbrich discloses a multi-plane write command that uses a common page address to concurrently write to pages of a superblock that are on different planes. *See* Ground 2, Claim 3. Olbrich’s superblocks and super pages are similar to Sinclair’s metablocks and metapages.

Pet., 73.

141. Petitioner states that Olbrich’s “superblocks and super pages” are analogous to Sinclair’s “metablocks and metapages” but does not explain this analogy. *See, e.g.*, Pet., 32-33 (describing Olbrich in isolation, without comparing it to Sinclair). Claim 3 also depends upon claim 1, and Petitioner’s argument for claim 3 incorporates and depends upon its argument claim 1. *See* Pet., 72. In analyzing claim 1, Petitioner identifies the claimed “zones” (which include the “specified zone” of claim 3’s recitation of writing data to “erase units ... of the specified zone using a common page address”) with Takeo “zones,” not Takeo “superblocks.” *See* Pet., 56 (identifying the claimed “zones” with Takeo’s “zones”), 62 (same), 64 (identifying the claimed “specified zone” with a “zone” in Takeo). Petitioner’s statement about Olbrich and Sinclair does not provide or explain any analogy between Olbrich’s “superblocks and super pages” and Takeo zones.

142. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that Petitioner’s Takeo combinations teach the “using a common page address” aspect of claim 1.

VII. CONCLUSION

143. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject

to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required, I will appear for cross-examination within the United States during the time allotted.

144. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Respectfully submitted,

Dated: October 20, 2025



Dr. Mark Jones

Exhibit A

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**PROFESSIONAL
EXPERIENCE**

Professor Emeritus of Electrical and Computer Engineering, Virginia Tech,
2021-present

Professor, Department of Electrical and Computer Engineering, Virginia Tech,
8/97-2021

Chief Technology Advisor, *Ocean Tomo, LLC*, August 2013 to December 2013.

Professor, Department of Computer Science, University of Tennessee, 8/93-7/97

Assistant Computer Scientist, Mathematics and Computer Science Division,
Argonne National Laboratory, Chicago, IL, 6/90 to 7/93.

EDUCATION

Ph.D., Duke University, Computer Science, May 1990.

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Virginia Bioinformatics Faculty Fellow
1st prize and Honorable Mention at AOL-CIT Research Day
Virginia Tech College of Engineering Dean's List for Teaching
NSF CAREER Award
University of Tennessee Science Alliance Award
Atanasoff Best Paper Award
Gordon Bell Prize
Von Neumann Fellowship
R. F. Poole Scholarship
National Merit Scholar

**EXPERT
TESTIMONY**

Blackboard v. Desire2Learn
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving Internet-based educational
software employing role-based access control
Testified: Jury trial (infringement and validity), injunction hearing,
contempt hearing, and deposition (4 times)

TechRadium v. Blackboard
United States District Court for the Eastern District of Virginia

United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving network-based emergency notification systems
Testified: Preliminary injunction hearing and deposition

Computer Associates v. Digex
Circuit Court for Prince George's County Maryland
Overview: Contract dispute involving enterprise management systems
Testified: Jury trial and deposition

Computer Associates v. Retired Persons Services
United States District Court for the Eastern District of Virginia
Overview: Contract dispute involving enterprise management systems
Testified: Deposition

DVSI v. University of Phoenix and Walden University
United States District Court for the Eastern District of Virginia
Overview: Patent infringement case involving network-based educational software employing digital rights management
Testified: Deposition (3 days)

VirnetX v. Microsoft
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving VPN software in Microsoft Windows and Microsoft's Unified Communications software
Testified: Jury trial (infringement and validity) and deposition (3 days)

TechRadium v. Twitter
United States District Court for the Southern District of Texas
Overview: Patent infringement case involving network-based notification systems
Testimony: Deposition

Bedrock Computer Tech v. Softlayer et al
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving data structures in the Linux operating system's network stack
Testimony: Jury trial v. Google (infringement and validity), Jury trial v. Yahoo (infringement and validity) and deposition (3 days)

CEATS v. Continental Airlines et al
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving Web-based interactive seat maps
Testimony: Jury trial (infringement and validity) and deposition (2 days)

VirnetX v. Cisco et al
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving secure communications, VPNs, and Voice-over-IP
Testimony: Jury trial v. Apple (infringement and validity), Jury trial v. Cisco (validity), and deposition (3 days), 2nd jury trial v. Apple (infringement), 3rd jury trial v. Apple (infringement), 4th jury trial v. Apple (infringement), 5th jury trial v. Apple

Summit6 v. Research In Motion et al
United States District Court for the Northern District of Texas

Overview: Patent infringement case involving network-based photo uploading tools on smartphones and web browsers

Testimony: Jury trial v. Samsung (infringement and validity) and deposition (3 days)

Ericsson v. Samsung

International Trade Commission

Overview: Patent infringement case involving Java technology and touchscreen technology on smartphones

Testimony: Deposition

AT Engine Controls LTD. v. Goodrich Corp and Goodrich Pump & Engine Control Systems, Inc.

United States District Court for the District of Connecticut

Overview: Trade secret case involving an embedded computing system design for helicopter engine control

Testimony: Deposition

SmartFlash LLC. v. Apple, et. al.

SmartFlash LLC. v. Samsung, et. al.

United States District Court for the Eastern District of Texas

Overview: Patent infringement case involving digital rights management and content distribution

Testimony: Jury trial v. Apple (infringement and validity) and deposition (4 days)

Unwired Planet v. Apple

United States District Court for the Northern District of California

Overview: Patent infringement case involving several technologies related to mobile devices

Testimony: Deposition (3 days); technology tutorial presentation to the Court

Facebook v. Rembrandt Social Media

Patent Trial and Appeal Board

Overview: Validity of a patent in the area of a web-based diary system

Testimony: Deposition

Motorola Mobility v. Intellectual Ventures

Patent Trial and Appeal Board

Overview: Validity of a patent in the area transmitting and browsing preformatted information

Testimony: Deposition

Summit6 v. Apple et al

United States District Court for the Northern District of Texas

Overview: Patent infringement case involving network-based photo uploading tools on smartphones and web browsers

Testimony: Deposition

EMC v. Pure Storage et al

United States District Court for the District of Delaware

Overview: Patent infringement case involving memory systems

Testimony: Deposition and jury trial (infringement and validity)

Parallel Networks v. IBM

United States District Court for the District of Delaware

Overview: Patent infringement case involving web servers and load balancing

Testimony: Deposition (2 days)

Parallel Networks v. Microsoft

United States District Court for the District of Delaware

Overview: Patent infringement case involving web servers and load balancing

Testimony: Deposition (2 days) and jury trial (infringement and validity)

Microsoft and IBM v. Parallel Networks

Patent Trial and Appeal Board

Overview: Validity of a patent related to web servers and load balancing

Testimony: Deposition

adidas v. Under Armour

United States District Court for the District of Delaware

Overview: Patent infringement case involving fitness tracking

Testimony: Deposition

BMC Software v. ServiceNow

United States District Court for the Eastern District of Texas

Overview: Patent infringement case involving enterprise management software

Testimony: Deposition

Ericsson v. TCL

United States District Court for the Eastern District of Texas

Overview: Patent infringement case involving Java technology and security on smartphones

Testimony: Deposition (3 days) and jury trial (infringement)

REM v. Square

United States District Court for the Eastern District of Missouri

Overview: Intellectual property case involving credit card readers for smartphones

Testimony: Deposition

AARC v. Chrysler et al

United States District Court for the District of Columbia

Overview: Intellectual property case involving car infotainment systems

Testimony: Deposition

Spex Technologies v. Apricorn

United States District Court for the Central District of California

Overview: Patent infringement case involving secure memory devices

Testimony: Deposition, Jury trial

United States Conference of Mayors v. Great-West Life Annuity Insurance Co.

United States District Court for the District of Columbia

Overview: Contract dispute

Testimony: Deposition and jury trial

Tecsec, Inc. v. Adobe Systems Inc. and Oracle (listed as IBM, et.al.).

United States District Court for the Eastern District of Virginia

Overview: Patent infringement case involving secure object technology

Testimony: Adobe: Deposition and jury trial (infringement and validity); Oracle (deposition)

Egenera, Inc. v. Cisco Systems, Inc.

United States District Court for the District of Massachusetts

Overview: Patent infringement case involving an architecture for a processing platform

Testimony: Deposition, bench trial, and jury trial

Unified Patents v. Sound View Innovations

Patent Trial and Appeal Board

Overview: Validity of a patent related to concurrency control

Testimony: Deposition

Hulu v. Sound View Innovations

Patent Trial and Appeal Board

Overview: Validity of a patent related to concurrency control

Testimony: Deposition

Grace and Potter. v. Apple Inc.

United States District Court for the Northern District of California

Overview: Class action case involving FaceTime

Testimony: Deposition

HTC v. Ericsson

United States District Court for the Eastern District of Texas

Overview: Patent licensing related to cellular standards

Testimony: Deposition

Windy City.Innovations v. FaceBook, Inc..

United States District Court for the Northern District of California

Overview: Patent infringement case involving an architecture for a messaging platform

Testimony: Deposition

Hulu v. Sound View Innovations

Patent Trial and Appeal Board

Overview: Validity of a patent related to real time systems

Testimony: Deposition

Citrix Systems, Inc. v. Avi Networks, Inc..

United States District Court for the District of Delaware

Overview: Patent infringement case involving network devices

Testimony: Deposition

Rovi v. Comcast

International Trade Commission

Overview: Patent infringement case set top boxes

Testimony: Deposition, Trial

Seven Networks v. Apple

United States District Court for the Eastern District of Texas

Overview: Patents related to mobile device push-based communication

Testimony: Deposition

Match Group, LLC v. Bumble Trading Inc.

United States District Court for the Western District of Texas

Overview: Patents related to online dating apps

Testimony: Deposition

SAS Institute Inc. v. World Programming Limited, et. al.
United States District Court for the Eastern District of Texas
Overview: Copyright and patents related to statistical software
Testimony: Deposition, Bench trial

Allscripts Healthcare, LLC v. Decision Resources Group,
United States District Court for the District of Massachusetts
Overview: Contract dispute
Testimony: Deposition, jury trial

Clear Imaging v. Samsung
United States District Court for the Eastern District of Texas
Overview: Patents related to image processing
Testimony: Deposition

Nokia v. Lenovo
International Trade Commission
Overview: Patents related to video encoding
Testimony: Deposition

Dish Network v. Sound View Innovations
Patent Trial and Appeal Board
Overview: Validity of a patent related to scheduling for QoS
Testimony: Deposition

Dish Network v. Sound View Innovations
Patent Trial and Appeal Board
Overview: Validity of a patent related real-time multimedia applications
Testimony: Deposition

RFCyber v. Samsung
United States District Court for the Eastern District of Texas
Overview: Patents related to secure payment systems
Testimony: Deposition

RightQuestion LLC v. Samsung
United States District Court for the Eastern District of Texas
Overview: Patents related to hardware-based authentication
Testimony: Deposition

Daedalus Blue, LLC v. MicroStrategy Inc.
United States District Court for the Eastern District of Virginia, Norfolk
Division
Overview: Patent infringement case involving business intelligence software
Testimony: Deposition

Seven Networks v. Motorola Mobility LLC,
United States District Court for the Eastern District of Texas
Overview: Patents related to mobile device communication methods
Testimony: Deposition

HID Global Corp. v. Vector Flow Inc. and Ajay Jain, Vikrant Ghai, and
Shailendra Sharma
United States District Court for the District of Delaware
Overview: Patents related to security monitoring

Testimony: Deposition and Trial

YouToo Technologies, LLC, v. Twitter, Inc.

United States District Court for the Northern District of Texas Dallas Division

Overview: Patents related to video

Testimony: Deposition (2 days) and jury trial

Constellation Designs, LLC v. LG Electronics, Inc., LG Electronics USA, Inc.,
and LG Electronics Alabama, Inc.

U.S. District Court, Eastern District of Texas, Marshall Division

Overview: Patents related to digital communication systems

Testimony: Deposition and Trial

Ryan Hardin, et al. v. Samsung Electronics Co., LTD., et al.

U.S. District Court, Eastern District of Texas, Marshall Division.

Overview: Patents related to geofencing

Testimony: Deposition

Xerox, ACS Transport Solutions, Conduent and New Jersey Transit v.

Bytemark, Inc.

Patent Trial and Appeal Board

Overview: Validity of a patent related to mobile ticketing

Testimony: Deposition

Motista LLC v. Ernst and Young LLP

Arbitration Proceedings

Overview: Matters related to trade secrets

Testimony: Hearing

Inovalon v. Komodo Health

Arbitration Proceedings

Overview: Matters related to trade secrets and breach of contract

Testimony: Hearing

Alacritech, Inc. v. Dell Inc. et al

U.S. District Court, Eastern District of Texas, Marshall Division

Overview: Patents related to network interface devices

Testimony: Deposition

RFCyber v. Apple

United States District Court for the Western District of Texas

Overview: Patents related to secure payment systems

Testimony: Deposition

K. Mizra LLC v. Hewlett Packard Enterprise Co and Aruba Networks LLC

U.S. District Court, Eastern District of Texas, Marshall Division

Overview: Patents related to network security

Testimony: Deposition

Carbyne v. Apple

United States District Court for the Western District of Texas

Overview: Patents related to hardware-based authentication

Testimony: Deposition

Radian Memory Systems LLC, v. Samsung Electronics Co., LTD., et al.

U.S. District Court, Eastern District of Texas, Marshall Division.

Overview: Patents related to flash memory controllers

Testimony: Deposition

Leo Riot, et al. v. Apex Trader Funding Inc., et al.

United States District Court for the Western District of Texas, Austin Division.

Overview: Matters related to trade secrets, copyrights, and breach of contract

Testimony: Deposition

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NSF, "SCH: INT: Collaborative Research: Smart Wearable Systems to Support and Measure Movement in Children With and Without Mobility Impairments," \$326,658, 10/1/17-9/30/21.

NASA, "Integrated Sensors for the Evaluation of Structural Integrity of Inflatable Habitats," with NanoSonic, \$35,000, 9/1/2016-8/31/17.

NSF, "SHB: Small: Collaborative Research: Electronic textiles for ambulatory health monitoring," \$306,083, 7/1/2011-6/30/2014.

DARPA, "RECE," With BBN, \$30,000, 4/16/09-10/16/09.

NSF, "Investigating a Novel Embedded Processor Architecture for Electronic Textiles in Wearable and Pervasive Computing," \$220,000, 12/1/08-11/30/10.

NSF, "Fundamental Algorithms to Enable the Simulation of Multi-Scale Biological Systems," \$200,000, 9/1/07-8/31/10.

AFRL, "Phase II: Amorphous Soft-Core Processor for Hardware Anti-Tamper," ~\$230,000, 11/1/06-10/31/08.

Intel, "E-Textile Rug for Gait Analysis, People Tracking and Emergency Directions," \$15,000, 6/1/06-12/31/06.

Carilion, "Quantitative Measurement and Modeling of Early Events in Influenza Pathogenesis," \$20,000, 7/1/05-6/30/06.

AFRL, "Phase I: Wearable Computer for Enhanced Situation Awareness," \$30,000, 5/1/06-1/1/07.

AFRL, "Phase I: Amorphous Soft-Core Processor for Hardware Anti-Tamper," \$35,000, 1/1/06-11/1/06.

MDA, "Phase I: Secure Software Platform for Real-Time Software Anti-Tamper," \$29,994, 6/1/06-11/1/06.

National Science Foundation (NSF), "CRI", (e-textiles equipment), ~\$80,000, 8/05-7/07.

Harris Corporation, "Exploiting the Reconfigurability of a Software-Defined Radio Platform," \$161,070, 9/1/05-6/30/06.

DARPA, "Phase I: Technology for Trusted Circuits," \$31,000, 3/1/05-9/15/05.

Harris Corporation, "Partial Reconfiguration Support for the Harris Programmable Modem Platform," \$73,448, 12/01/04-6/30/05.

NSF, "Phase I: An Electronic Textile System for Gait Analysis", \$33,000, 1/1/2005-6/30/2005.

Office of Naval Research (ONR). "AWINN." \$452,300, 12/20/04-7/31/06.

Office of Secretary of Defense, "Phase II: Reconfigurable Processor Technology for Software Protection," SBIR Subcontract with Luna Innovations, \$237,581, 6/04-5/06.

NSF, REU Supplement to ITR: Tailor-Made: Design of e-Textile Architectures for Wearable Computing, NSF, \$12,000, 6/1/2005 – 8/31/2005.

Office of Secretary of Defense, "Phase I: Reconfigurable Processor Technology for Software Protection," SBIR Subcontract with Luna Innovations, \$33,000, 8/03-2/04.

National Science Foundation (NSF), "ITR: Tailor-Made: Design of e-Textile Architectures for Wearable Computing", \$399,000, 8/02-8/06.

NSF, REU Supplement to above grant, \$10,000.

NSF, REU Supplement to above grant, \$6,000.

NSF, "A Toolbox of Scalable Algorithms and Software for Advanced Scientific Computing Applications", \$300,000, 4/03-4/06.

Defense Advanced Research Projects Agency (DARPA). Computational Fabrics, \$217,000, 3/01-12/02. Subcontract from ISI/University of Southern California.

Office of Naval Research (ONR). Secure Configurable Radio. \$751,000, 4/00-4/04.

NSF, SUCCEED, \$33,000, 9/1/01-8/31/02.

National Science Foundation (NSF). Parallel unstructured mesh algorithms, Amount: \$145,023, 10/99-9/02.

DARPA, Development of algorithms and software for the control of distributed, dynamic sensor networks, Amount \$411,625, 6/99-6/02.

DARPA, Subcontract with USC/ISI. Development of algorithms and runtime software for systems of configurable computers, Amount \$160,000, 10/00-10/01.

Department of Energy, Development of algorithms and software for massively parallel architectures, Amount: \$145,000, 12/98-11/01.

DARPA, Development of Java-based tools and applications for fast, flexible run-time reconfiguration of configurable computing devices, Amount: \$345,574, 9/99-9/01.

DARPA, Development of an application programming interface, algorithms, and applications for run-time reconfiguration on novel adaptive computing architectures, Amount: \$250,000, 6/99-6/01.

Lockheed-Martin/Sanders, A Wireless Link for Remote Telemetry of Compact Airborne System, \$125,000, 5/00-4/01.

DARPA, Development of algorithms and runtime software for systems of configurable computers, Amount \$169,792, 11/99-10/00.

National Security Agency (NSA), Software for the translation of JBits FPGA programs to EDIF programs, Amount \$75,000, 9/99-7/00.

DARPA, Construction of an API & applications for the control of distributed systems of configurable computing nodes, Amount \$162,886, 9/98-10/99.

NSF, Career Award: Parallel algorithms and software for unstructured mesh computations, Amount: \$125,881, 7/96-7/99.

Air Force Research Laboratory, Research and development of an Internet-based, interactive, decision making program, Amount: \$97,425, 11/97-5/99.

NSF, Equipment funding for a 16-node cluster of configurable computers, Amount: \$85,000, 12/97-12/98.

NSF, Scientific applications in a distributed computing environment, Amount: \$318,807, 7/95-7/98.

NSF, Equipment funding for an ATM-based cluster of workstations, Amount, \$100,000, 1/96-12/96.

NSF, Workshop organized at Argonne National Laboratory, Amount, \$10,000, 1996.

PATENTS

Inventor, United States Patent No. 8,473,754, Hardware-Facilitated Secure Software Execution Environment.

SOFTWARE

SLAAC/ACS API (4/99): Software for the control of complex systems of configurable computing nodes and high-speed networks. This code has been distributed to the ACS community. Developed in Configurable Computing Laboratory with Peter Athanas.

BlockSolve (4/93 & 1/96): Software for solving large sparse linear systems on distributed memory architectures. This code has been distributed via netlib and ANL ftp and has been accessed by several hundred people as of 4/4/99. Developed at Argonne National Laboratory with Paul Plassmann.

LANZ (10/90): Software for solving the generalized eigenproblem on shared memory architectures. This code has been distributed via netlib and NASA and has been accessed by over 10,000 people as of 4/4/99. Developed at Duke University and Argonne National Laboratory with Merrell Patrick.

TEACHING

Computer Programming

RESPONSIBILITIES

ECE 5574, *Advanced Software Development for CAE*
ECE 4574, *Large-Scale Software Development for Engineering Systems*
ECE 3574, *Applied Software Design*
ECE 2574, *Data Structures*
ECE 1574, *Engineering Problem Solving with C++*
Computer Simulation and Modeling
CS 371, *Numerical Analysis*
CS 594, *Computational Modeling*
Computer Network, Architecture, and Organization
ECE 2504, *Introduction to Computer Engineering*
CS 594, *Internetworking with TCP/IP*
ECE 4504, *Computer Organization*
ECE 4534, *Design of Embedded Systems*
ECE 5504 (formerly ECE 5515), *Computer and Network Architectures*
ECE Special Studies: *Configurable Computing*, E-Textiles
ECE 5984, *Java-Based Configurable Computing*
ECE 6504, *Applications of Parallel and Distributed Computing*, TV course.
CS 530, *Computer Systems Organization*
CEO of DISC, a student-run virtual corporation, for Fall 1998 and Spring 1999.
