Docket No.: 085393-0935

REQUEST FORM FOR CONTINUATION APPLICATION UNDER 35 USC 111(a)

Prior Application: **International Application No. PCT/JP2011/006167**
Art Unit: **(Unassigned)**
Examiner: **(Unassigned)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a Request for filing a continuation application, entitled **SEMICONDUCTOR DEVICE**, under 35 U.S.C. 111(a) of pending prior International Application No. **PCT/JP2011/006167**, filed on **November 4, 2011**, by the following named inventors:

INVENTOR	RESIDENCE	CITIZENSHIP	POST OFFICE ADDRESS
Yoshihiro SATO	Toyama, Japan	Japanese	c/o Panasonic Corporation 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501
Hideyuki ARAI	Toyama, Japan	Japanese	c/o Panasonic Corporation 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501
Takayuki YAMADA	Toyama, Japan	Japanese	c/o Panasonic Corporation 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501

1. ☒ I hereby verify, to the best of my knowledge, that the enclosed copy of this prior application is a true copy of the above-identified prior application, including the oath or declaration as originally filed.

2. ☐ Preliminary Amendment is enclosed.

3. ☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.

4. ☐ Cancel claims

TSMC-1002
U.S. Patent 8,884,373

5. ☐ Applicant is entitled to claim Small Entity status.

6. The filing fee is calculated on the basis of the claims existing in the prior application as amended above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	16	-20	0	$60.00	$0.00
Independent Claims	1	-3	0	$250.00	$0.00
Multiple Dependent Claim(s)					$0.00
Sheets of specification and drawing ($310.00 for each 50 sheets in excess of 100)					$0.00
Basic Filing Fee					$390.00
Patent Search Fee					$620.00
Patent Examination Fee					$250.00
Total of Above Calculations					$1,250.00
Less ½ for Small Entity					$0.00
Assignment & Recording Fee					$0.00
Total Fee					**$1,260.00**

1. ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees or credit any overpayment to Deposit Account No. 500417.

2. ☐ Amend the specification by inserting before the first line the sentence:

3. ☒ Priority of Japanese Application No. **2011-068131** filed **March 25, 2011,** in Japan and International Application No. **PCT/JP2011/006167** filed **November 4, 2011** designating the U.S. is claimed under 35 USC 119, 120 and/or 365.

4. ☒ The prior application is assigned of record to:

PANASONIC CORPORATION
Osaka, Japan

5. ☒ The power of attorney in the prior application is to:

MAEDA PATENT OFFICE
Osaka, Japan

6. ☒ Also enclosed:

- Executed Declaration and Power of Attorney
- Front Page of International Publication
- PCT Request
- International Search Report
- PCT/IB/301,304
- PCT/ISA/237

7. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until

8. ☒ Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

	McDERMOTT WILL & EMERY LLP
	500 North Capitol Street NW
	Washington, D. C. 20001

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

500 North Capitol Street NW
Washington, DC 20001
(202) 756-8000 MEF:sym
Facsimile: (202) 756-8087
Date: October 31, 2012

Docket No.: 085393-0935
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Yoshihiro SATO et al.	Customer Number: 53080
Application No.: Not Yet Assigned	Confirmation No.: N/A
Filed: October 31, 2012	Art Unit: N/A
For: SEMICONDUCTOR DEVICE	Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

A summary/abstract translation of the non-English language references is enclosed.

Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 CFR 1.98(a)(2).

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0417, under Order No. 085393-0935.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

500 North Capitol Street, N.W
Washington, DC 20001
Phone: (202) 756-8372 MEF:sm
Facsimile: (202) 756-8087
Date: October 31, 2012

PTO/SB/08b (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	Not Yet Assigned
Filing Date	October 31, 2012
First Named Inventor	Yoshihiro SATO
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	085393-0935

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A1*	US-2003/0107090-A1	06-12-2003	Kumeno	Corresponds to JP 2003-179056-A
	A2*	US-2008/0036010-A1	02-14-2008	Tamaki et al.	Corresponds to JP 2008-042092-A

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	B1	JP-2010-067912-A	03-25-2010	Panasonic Corp	English Abstract	
	B2	JP-6-275788-A	09-30-1994	Ricoh Kk	English Abstract	
	B3	JP-8-017934-A	01-19-1996	Ricoh Kk	English Abstract	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		International Search Report issued in International Application No. PCT/JP2011/006167 oissued on January 24, 2011.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/006167

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/8234(2006.01)i, *H01L21/28*(2006.01)i, *H01L21/76*(2006.01)i, *H01L21/8238*(2006.01)i, *H01L21/8244*(2006.01)i, *H01L27/088*(2006.01)i, *H01L27/092*(2006.01)i, *H01L27/10*(2006.01)i, *H01L27/11*(2006.01)i,
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L21/8234, H01L21/28, H01L21/76, H01L21/8238, H01L21/8244, H01L27/088, H01L27/092, H01L27/10, H01L27/11, H01L29/423, H01L29/49

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2012
Kokai Jitsuyo Shinan Koho	1971-2012	Toroku Jitsuyo Shinan Koho	1994-2012

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	JP 2008-042092 A (Matsushita Electric Industrial Co., Ltd.), 21 February 2008 (21.02.2008), paragraphs [0074] to [0123]; fig. 1 to 5 & US 2008/0036010 A1	1-4,16 5-7,15
A	JP 2003-179056 A (Fujitsu Ltd.), 27 June 2003 (27.06.2003), entire text; all drawings & US 2003/0107090 A1 & EP 1320130 A2 & DE 60220762 D	1-7,15,16
A	JP 2010-067912 A (Panasonic Corp.), 25 March 2010 (25.03.2010), paragraphs [0035] to [0065]; fig. 1 to 3 (Family: none)	1-7,15,16

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 January, 2012 (13.01.12)	24 January, 2012 (24.01.12)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 2009)

Continuation of A. CLASSIFICATION OF SUBJECT MATTER
(International Patent Classification (IPC))

H01L29/423(2006.01)i, *H01L29/49*(2006.01)i

(According to International Patent Classification (IPC) or to both national classification and IPC)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/006167

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See extra sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1-7, 15 and 16

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Continuation of Box No.III of continuation of first sheet(2)

There must be a special technical feature that links a group of inventions in claims so as to form a single general inventive concept to have the group of inventions satisfy the requirement of unity of invention. The group of inventions in claims 1-20 is linked by the feature in claim 1.

This feature, however, has been disclosed in prior art document JP 2008-042092 A (Matsushita Electric Industrial Co., Ltd.), 21 February 2008 (21.02.2008), paragraphs [0074]-[0123] and fig. 1-5. Therefore, it cannot be a special technical feature.

Consequently, there is no special technical feature among the group of inventions in claims 1-20 so as to link the inventions to form a single general inventive concept. Therefore, it is clear that the group of inventions in claims 1-20 does not satisfy the requirement of unity of invention.

Next, the number of groups of inventions, namely, the number of inventions, so linked as to form the general inventive concept in claims in this international application is examined.

The inventions in claims 1-4 not having a special technical feature are classified as the inventions of the invention group 1.

Invention group 1: The inventions in claims 1-5, and the inventions having the special technical feature stated below among the inventions in claims 6, 7, 15 and 16
"The first conductivity type impurity concentration of the first first conductivity type silicon film on a portion positioned on a first active region is higher than the first conductivity type impurity concentration of a second first conductivity type silicon film on a portion positioned on the third active region."

Invention group 2: The invention in claim 8

Invention group 3: The inventions having the special technical feature stated below among the inventions in claims 9-13
"The first conductivity type impurity concentration of the first first conductivity type silicon film on a portion positioned on an element isolating region is higher than the first conductivity type impurity concentration of a second first conductivity type silicon film on a portion positioned on the third active region."

Invention group 4: The invention in claim 14

Invention group 5: The inventions in claims 17-20

The invention that can be classified as an invention of a plurality of the above-mentioned invention groups is classified as an invention of the first one of such invention groups.

Consequently, there are five invention groups classified as [1-7, 15, 16], [8], [9-13], [14], [17-20] in the claims of this international application.

(12) 特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2012 年 10 月 4 日(04.10.2012)

WIPO | PCT

(10) 国際公開番号
WO 2012/131818 A1

(51) 国際特許分類:
H01L 21/8234 (2006.01) *H01L 27/092* (2006.01)
H01L 21/28 (2006.01) *H01L 27/10* (2006.01)
H01L 21/76 (2006.01) *H01L 27/11* (2006.01)
H01L 21/8238 (2006.01) *H01L 29/423* (2006.01)
H01L 21/8244 (2006.01) *H01L 29/49* (2006.01)
H01L 27/088 (2006.01)

(21) 国際出願番号: PCT/JP2011/006167

(22) 国際出願日: 2011 年 11 月 4 日(04.11.2011)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

(30) 優先権データ:
特願 2011-068131 2011 年 3 月 25 日(25.03.2011) JP

(71) 出願人 (米国を除く全ての指定国について): パナソニック株式会社 (PANASONIC CORPORATION) [JP/JP]; 〒5718501 大阪府門真市大字門真１００６番地 Osaka (JP).

(72) 発明者; および

(75) 発明者/出願人 (米国についてのみ): 佐藤 好弘 (SATO, Yoshihiro). 新井 秀幸 (ARAI, Hideyuki). 山田 隆順 (YAMADA, Takayuki).

(74) 代理人: 前田 弘, 外 (MAEDA, Hiroshi et al.); 〒5410053 大阪府大阪市中央区本町２丁目５番７号 大阪丸紅ビル Osaka (JP).

(81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

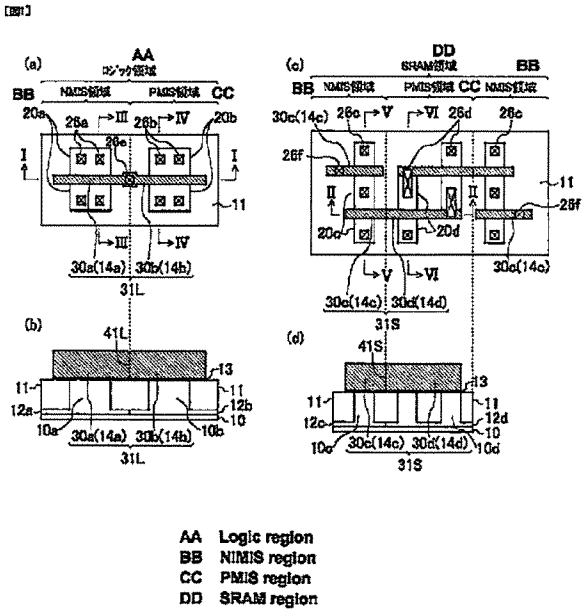
(84) 指定国 (表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類:

— 国際調査報告 (条約第 21 条(3))

(54) Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME

(54) 発明の名称 : 半導体装置及びその製造方法



(57) Abstract: A dual gate electrode (31L) has: a gate electrode (30b), which includes a first conductivity-type silicon film (14b) formed on an active region (10b); and a gate electrode (30a), which includes a second conductivity-type silicon film (14a) formed on an active region (10a). A dual gate electrode (31S) has: a gate electrode (30d), which includes a first conductivity-type silicon film (14d) formed on an active region (10d); and a gate electrode (30c), which includes a second conductivity-type silicon film (14c) formed on an active region (10c). The concentration of a first conductivity-type impurity in at least a part of the first conductivity-type silicon film (14b) is higher than the concentration of the first conductivity-type impurity in a part of the first conductivity-type silicon film (14d), said part being positioned on the active region (10d).

(57) 要約: デュアルゲート電極（３１Ｌ）は、活性領域（１０ｂ）上に形成された第１導電型シリコン膜（１４ｂ）を含むゲート電極（３０ｂ）と、活性領域（１０ａ）上に形成された第２導電型シリコン膜（１４ａ）を含むゲート電極（３０ａ）とを有する。デュアルゲート電極（３１Ｓ）は、活性領域（１０ｄ）上に形成された第１導電型シリコン膜（１４ｄ）を含むゲート電極（３０ｄ）と、活性領域（１０ｃ）上に形成された第２導電型シリコン膜（１４ｃ）を含むゲート電極（３０ｃ）とを有する。第１導電型シリコン膜（１４ｂ）の少なくとも一部分における第１導電型不純物濃度は、活性領域（１０ｄ）上に位置する部分の第１導電型シリコン膜（１４ｄ）の第１導電型不純物濃度よりも高い。

WO 2012/131818 A1

特許協力条約に基づく国際出願願書

紙面による写し (注意　電子データが原本となります)

0	受理官庁記入欄	
0-1	国際出願番号	
0-2	国際出願日	
0-3	(受付印)	

0-4	様式 PCT/RO/101 この特許協力条約に基づく国際出願願書は、	
0-4-1	右記によって作成された。	PCT-SAFE Version 3.51.049.225 MT/FOP 20110401/0.20.5.19
0-5	申立て 出願人は、この国際出願が特許協力条約に従って処理されることを請求する。	
0-6	出願人によって指定された受理官庁	日本国特許庁 (RO/JP)
0-7	出願人又は代理人の書類記号	P615651P0
I	発明の名称	半導体装置及びその製造方法
II	出願人	
II-1	この欄に記載した者は	出願人である (applicant only)
II-2	右の指定国についての出願人である。	米国を除く全ての指定国 (all designated States except US)
II-4ja	名称	パナソニック株式会社
II-4en	Name:	PANASONIC CORPORATION
II-5ja	あて名	5718501 日本国 大阪府門真市大字門真１００６番地
II-5en	Address:	1006, Oaza Kadoma, Kadoma-shi, Osaka 5718501 Japan
II-6	国籍(国名)	日本国 JP
II-7	住所(国名)	日本国 JP
II-8	電話番号	06-6908-1473
II-9	ファクシミリ番号	06-6909-0053
III-1	その他の出願人又は発明者	
III-1-1	この欄に記載した者は	出願人及び発明者である (applicant and inventor)
III-1-2	右の指定国についての出願人である。	米国のみ (US only)
III-1-4ja	氏名(姓名)	佐藤　好弘
III-1-4en	Name (LAST, First):	SATO, Yoshihiro
III-1-5ja	あて名	
III-1-5en	Address:	
III-1-6	国籍(国名)	
III-1-7	住所(国名)	

特許協力条約に基づく国際出願願書

紙面による写し (注意　電子データが原本となります)

III-2	その他の出願人又は発明者	
III-2-1	この欄に記載した者は	出願人及び発明者である (applicant and inventor)
III-2-2	右の指定国についての出願人である。	米国のみ (US only)
III-2-4ja	氏名(姓名)	新井　秀幸
III-2-4en	Name (LAST, First):	ARAI, Hideyuki
III-2-5ja	あて名	
III-2-5en	Address:	
III-2-6	国籍(国名)	
III-2-7	住所(国名)	
III-3	その他の出願人又は発明者	
III-3-1	この欄に記載した者は	出願人及び発明者である (applicant and inventor)
III-3-2	右の指定国についての出願人である。	米国のみ (US only)
III-3-4ja	氏名(姓名)	山田　隆順
III-3-4en	Name (LAST, First):	YAMADA, Takayuki
III-3-5ja	あて名	
III-3-5en	Address:	
III-3-6	国籍(国名)	
III-3-7	住所(国名)	
IV-1	代理人又は共通の代表者、通知のあて名 下記の者は国際機関において右記のごとく出願人のために行動する。	代理人 (agent)
IV-1-1ja	氏名(姓名)	前田　弘
IV-1-1en	Name (LAST, First):	MAEDA, Hiroshi
IV-1-2ja	あて名	5410053 日本国 大阪府大阪市中央区本町２丁目５番７号　大阪丸紅ビル
IV-1-2en	Address:	Osaka-Marubeni Bldg.,5-7,Hommachi 2-chome, Chuo-ku, Osaka-shi, Osaka 5410053 Japan
IV-1-3	電話番号	06-6125-2255
IV-1-4	ファクシミリ番号	06-6125-2288
IV-1-6	代理人登録番号	100077931
IV-2	その他の代理人	筆頭代理人と同じあて名を有する代理人 (additional agent(s) with the same address as first named agent)
IV-2-1ja	氏名	原田　智雄(100117710); 前田　亮(100143409); 間脇　八蔵(100157093)
IV-2-1en	Name(s)	HARADA, Tomoo(100117710); MAEDA, Ryo(100143409); MAWAKI, Hachizo(100157093)
V	国の指定	
V-1	この願書を用いてされた国際出願は、規則4.9(a)に基づき、国際出願の時点で拘束される全てのPCT締約国を指定し、取得しうるあらゆる種類の保護を求め、及び該当する場合には広域と国内特許の両方を求める国際出願となる。	

特許協力条約に基づく国際出願願書

紙面による写し (注意　電子データが原本となります)

VI-1	**先の国内出願に基づく優先権主張**		
VI-1-1	出願日	2011年 03月 25日 (25.03.2011)	
VI-1-2	出願番号	2011-068131	
VI-1-3	国名	日本国 JP	
VI-2	**優先権証明書送付の請求**		
	上記の先の出願のうち、右記の番号のものについては、出願書類の認証謄本を作成し国際事務局へ送付することを、受理官庁に対して請求している。	VI-1	
VI-3	**引用による補充：**		
	条約第11条(1)(iii)(d)若しくは(e)に規定する国際出願の要素の全部、又は規則20.5(a)に規定する明細書、請求の範囲若しくは図面の一部がこの国際出願には含まれていないが、受理官庁が条約第11条(1)(iii)に規定する要素の1つ以上を最初に受領した日において優先権を主張する先の出願にそれが完全に含まれている場合には、規則20.6に基づく確認の手続を条件として、その要素又は部分を規則20.6の規定によりこの国際出願に引用して補充することを請求する。		
VII-1	**特定された国際調査機関(ISA)**	日本国特許庁 (ISA/JP)	
VIII	**申立て**	申立て数	
VIII-1	発明者の特定に関する申立て	-	
VIII-2	出願し及び特許を与えられる国際出願日における出願人の資格に関する申立て	-	
VIII-3	先の出願の優先権を主張する国際出願日における出願人の資格に関する申立て	-	
VIII-4	発明者である旨の申立て(米国を指定国とする場合)	-	
VIII-5	不利にならない開示又は新規性喪失の例外に関する申立て	-	
IX	**照合欄**	用紙の枚数	添付された電子データ
IX-1	願書(申立てを含む)	4	✓
IX-2	明細書	44	✓
IX-3	請求の範囲	6	✓
IX-4	要約	1	✓
IX-5	図面	16	✓
IX-7	合計	71	
	添付書類	添付	添付された電子データ
IX-8	手数料計算用紙	-	✓
IX-18	PCT-SAFE 電子出願	-	-
IX-20	**要約とともに提示する図の番号**	1	
IX-21	**国際出願の使用言語名**	日本語	
X-1	**出願人、代理人又は代表者の記名押印**	(PKCS7 デジタル署名)	
X-1-1	氏名(姓名)	前田弘	
X-1-2	署名者の氏名		
X-1-3	権限(署名者が法人の場合)		

特許協力条約に基づく国際出願願書

紙面による写し (注意　電子データが原本となります)

受理官庁記入欄

10-1	国際出願として提出された書類の実際の受理の日	
10-2	図面	
10-2-1	受理された	
10-2-2	不足図面がある	
10-3	国際出願として提出された書類を補完する書類又は図面であってその後期間内に提出されたものの実際の受理の日(訂正日)	
10-4	特許協力条約第11条(2)に基づくあ要な補完の期間内の受理の日	
10-5	出願人により特定された国際調査機関	ISA/JP
10-6	調査手数料未払いにつき、国際調査機関に調査用写しを送付していない	

国際事務局記入欄

11-1	記録原本の受理の日	

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF RECEIPT OF RECORD COPY

(PCT Rule 24.2(a))

To:

MAEDA, Hiroshi
Osaka-Marubeni Bldg.
5-7, Hommachi 2-chome
Chuo-ku, Osaka-shi
Osaka 5410053
JAPON

Date of mailing *(day/month/year)*	IMPORTANT NOTIFICATION
21 December 2011 (21.12.2011)	
Applicant's or agent's file reference Inte P615651P0 M11-401C71-7	International application No. PCT/JP2011/006167

The applicant is hereby **notified** that the International Bureau has received the record copy of the international application as detailed below.

RECEIVED
JAN. 20. 2012
MAEDA & PARTNERS

Name(s) of the applicant(s) and State(s) for which they are applicants:

PANASONIC CORPORATION (for all designated States except US)
SATO, Yoshihiro et al (for US)

International filing date: 04 November 2011 (04.11.2011)
Priority date(s) claimed: 25 March 2011 (25.03.2011)
Date of receipt of the record copy by the International Bureau: 16 November 2011 (16.11.2011)
List of designated Offices:

AP: BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW
EA: AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
EP: AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR
OA: BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG
National: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW

ATTENTION: The applicant should carefully check the data appearing in this Notification. In case of any discrepancy between these data and the indications in the international application, the applicant should immediately inform the International Bureau. **In addition, the applicant's attention is drawn to:**

- time limits for entry into the national phase (see www.wipo.int/pct/en/texts/time_limits.htmland *PCT Applicant's Guide*, National Phase, especially Chapters 3 and 4)
- requirements regarding priority documents (if applicable) (see *PCT Applicant's Guide*, International Phase, paragraph 5.070)

A copy of this notification is being sent to the receiving Office and to the International Searching Authority.

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Chevallay-Worley Madeleine
Facsimile No. +41 22 338 70 10	e-mail pt08.pct@wipo.int Telephone No. +41 22 338 74 08

Form PCT/IB/301 (July 2010) I/FHQGFC6ZU2T4L0

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING SUBMISSION, OBTENTION OR TRANSMITTAL OF PRIORITY DOCUMENT

(PCT Administrative Instructions, Section 411)

To:

MAEDA, Hiroshi
Osaka-Marubeni Bldg.
5-7, Hommachi 2-chome
Chuo-ku, Osaka-shi
Osaka 5410053
JAPON

Date of mailing *(day/month/year)* 22 December 2011 (22.12.2011)	
Applicant's or agent's file reference P615651P0 M11-401671-2.	**IMPORTANT NOTIFICATION**
International application No. PCT/JP2011/006167	International filing date *(day/month/year)* 04 November 2011 (04.11.2011)
International publication date *(day/month/year)* **Not yet published**	Priority date *(day/month/year)* 25 March 2011 (25.03.2011)
Applicant PANASONIC CORPORATION et al	

The applicant is hereby notified of the date of receipt (or of obtaining by the International Bureau) of the priority document(s) relating to all earlier application(s) whose priority is claimed. Unless otherwise indicated by the letters "NR", in the right-hand column or by an asterisk appearing next to the date of receipt, **the priority document concerned was submitted or transmitted to or obtained by the International Bureau in compliance with Rule 17.1(a), (b) or (b-*bis*)**. This Form replaces any previously issued notification concerning submission, transmittal or obtaining of priority documents.

Priority date	Priority application No.	Country or regional Office or PCT receiving Office	Date of receipt of priority document
25 March 2011 (25.03.2011)	2011-068131	JP	14 December 2011 (14.12.2011)

The letters "NR" denote a priority document which, on the date of mailing of this Form, had not yet been received or obtained by the International Bureau in compliance with Rule 17.1(a), (b) or (b-*bis*). Where the applicant has failed to either submit, request to prepare and transmit or obtain and transmit, or to request the International Bureau to obtain the priority document within the applicable time limit under that Rule, the attention of the applicant is directed to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

An asterisk "*" next to a date of receipt, denotes a priority document submitted or transmitted to or obtained by the International Bureau but not in compliance with Rule 17.1(a), (b) or (b-*bis*) (the priority document was received after the time limit prescribed in Rule 17.1(a); the request to prepare and transmit the priority document was submitted to the receiving Office after the applicable time limit under Rule 17.1(b) or the request to the receiving Office or the International Bureau to obtain the priority document was made after the applicable time limit under Rule 17.1(b-*bis*)). Even though the priority document was not furnished in compliance with Rule 17.1(a), (b) or (b-*bis*), the International Bureau will nevertheless transmit a copy of the document to the designated Offices, for their consideration. In case such a copy is not accepted by the designated Office as the priority document, Rule 17.1(c) provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

RECEIVED
JAN. 20. 2012
MAEDA & PARTNERS

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 70 10

Authorized officer
Masashi Honda
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Telephone No. +41 22 338 74 08

特許協力条約

前田
'12.1.25
特許

発信人　日本国特許庁（国際調査機関）

代理人
　前田　弘

様

あて名
〒541-0053
日本国大阪府大阪市中央区本町２丁目５番７号　大阪丸紅ビル

PCT
国際調査機関の見解書
（法施行規則第40条の2）
〔PCT規則43の2.1〕

発送日 （日.月.年）	24. 01. 2012
出願人又は代理人 の書類記号　P615651P0	今後の手続きについては、下記２を参照すること。

国際出願番号	国際出願日	優先日
PCT／JP2011／006167	（日.月.年）　04. 11. 2011	（日.月.年）　25. 03. 2011

国際特許分類（IPC）Int.Cl. 補充欄参照

出願人（氏名又は名称）
パナソニック株式会社

１．この見解書は次の内容を含む。

- [x] 第Ⅰ欄　見解の基礎
- [ ] 第Ⅱ欄　優先権
- [ ] 第Ⅲ欄　新規性、進歩性又は産業上の利用可能性についての見解の不作成
- [x] 第Ⅳ欄　発明の単一性の欠如
- [x] 第Ⅴ欄　PCT規則43の2.1(a)(i)に規定する新規性、進歩性又は産業上の利用可能性についての見解、それを裏付けるための文献及び説明
- [ ] 第Ⅵ欄　ある種の引用文献
- [ ] 第Ⅶ欄　国際出願の不備
- [ ] 第Ⅷ欄　国際出願に対する意見

２．今後の手続き
国際予備審査の請求がされた場合は、出願人がこの国際調査機関とは異なる国際予備審査機関を選択し、かつ、その国際予備審査機関がPCT規則66.1の2(b)の規定に基づいて国際調査機関の見解書を国際予備審査機関の見解書とみなさない旨を国際事務局に通知していた場合を除いて、この見解書は国際予備審査機関の最初の見解書とみなされる。

この見解書が上記のように国際予備審査機関の見解書とみなされる場合、様式PCT／ISA／220を送付した日から3月又は優先日から22月のうちいずれか遅く満了する期限が経過するまでに、出願人は国際予備審査機関に、適当な場合は補正書とともに、答弁書を提出することができる。

さらなる選択肢は、様式PCT／ISA／220を参照すること。

３．さらなる詳細は、様式PCT／ISA／220の備考を参照すること。

見解書を作成した日 13. 01. 2012	
名称及びあて先 日本国特許庁（ISA／JP） 郵便番号100－8915 東京都千代田区霞が関三丁目4番3号	特許庁審査官（権限のある職員）　4L　4429 松本　陶子 電話番号　03－3581－1101　内線　3498

様式PCT／ISA／237（表紙）（2009年7月）

国際調査機関の見解書

国際出願番号 PCT／JP2011／006167

第Ⅰ欄 見解の基礎

1．言語に関し、この見解書は以下のものに基づき作成した。

☑ 出願時の言語による国際出願

☐ 出願時の言語から国際調査のための言語である＿＿＿＿＿＿語に翻訳された、この国際出願の翻訳文（ＰＣＴ規則12.3(a)及び23.1(b)）

2．☐ この見解書は、ＰＣＴ規則 91 の規定により国際調査機関が認めた又は国際調査機関に通知された明らかな誤りの訂正を考慮して作成した（ＰＣＴ規則 43 の 2.1(b)）。

3．この国際出願で開示されたヌクレオチド又はアミノ酸配列に関して、提出された以下の配列表に基づき見解書を作成した。

a．提出手段 ☐ 紙形式

☐ 電子形式

b．提出時期 ☐ 出願時の国際出願に含まれていたもの

☐ この国際出願と共に電子形式により提出されたもの

☐ 出願後に、調査のために、この国際調査機関に提出されたもの

4．☐ さらに、複数の版の配列表又は配列表の写しを提出した場合、出願後に提出した配列の写し若しくは追加して提出した配列の写しが、出願時に提出した配列と同一である旨又は出願時の開示を超える事項を含まない旨の陳述書の提出があった。

5．補足意見：

国際調査機関の見解書

国際出願番号 PCT／JP2011／006167

第Ⅳ欄 発明の単一性の欠如

1．☑ 追加手数料の納付命令書（様式PCT／ISA／206）に対して、出願人は、規定期間内に、

☐ 追加手数料を納付した。

☐ 追加手数料及び、該当する場合には、異議申立手数料の納付と共に、異議を申し立てた。

☐ 追加手数料の納付と共に異議を申し立てたが、規定の異議申立手数料を支払わなかった。

☑ 追加手数料を納付しなかった。

2．☐ 国際調査機関は、発明の単一性の要件を満たしていないと判断したが、追加手数料の納付を出願人に求めないこととした。

3．国際調査機関は、PCT規則13.1、13.2及び13.3に規定する発明の単一性を次のように判断する。

☐ 満足する。

☑ 以下の理由により満足しない。

請求項に記載されている一群の発明が単一性の要件を満たすためには、その一群の発明を単一の一般的発明概念を形成するように連関させるための、特別な技術的特徴の存在が必要であるところ、請求項 1-20 に記載されている一群の発明は、請求項1に記載された事項で連関していると認められる。

しかしながら、この事項は先行技術文献 JP 2008-042092 A（松下電器産業株式会社）2008.02.21, 【0074】-【0123】, 図 1-5 に記載されているため、特別な技術的特徴とはなり得ない。

そうすると、請求項 1-20 に記載されている一群の発明の間には、単一の一般的発明概念を形成するように連関させるための、特別な技術的特徴は存しないこととなる。そのため、請求項1-20に記載されている一群の発明が発明の単一性の要件を満たしていないことは明らかである。

次に、この国際出願の請求項に記載されている、一般的発明概念を形成するように連関している発明の群の数、すなわち、発明の数につき検討すると、この国際出願の請求項には、[1-7, 15, 16]、[8]、[9-13]、[14]、[17-20]に区分される5個の発明が記載されていると認められる。

4． したがって、国際出願の次の部分について、この見解書を作成した。

☐ すべての部分

☑ 請求項 1-7, 15, 16 に関する部分

様式PCT／ISA／237（第Ⅳ欄）（2009年7月）

国際調査機関の見解書

国際出願番号 PCT／JP2011／006167

第Ⅴ欄 新規性、進歩性又は産業上の利用可能性についてのＰＣＴ規則43の2.1(a)(i)に定める見解、それを裏付ける文献及び説明

1. 見解

新規性（N）	請求項	5-7,15	有
	請求項	1-4,16	無
進歩性（ＩＳ）	請求項	5-7,15	有
	請求項	1-4,16	無
産業上の利用可能性（ＩＡ）	請求項	1-7,15,16	有
	請求項		無

2. 文献及び説明

文献１：JP 2008-042092 A（松下電器産業株式会社）2008.02.21,
【0074】-【0123】，図1-5

・請求項 1-4,16
請求項1-4,16に係る発明は、国際調査報告で引用された文献１の【0074】-【0123】，図1-5に記載されているので、新規性、進歩性を有さない。

・請求項 5-7,15
請求項5-7,15に係る発明は、国際調査報告で引用されたいずれの文献にも記載されておらず、当業者にとって自明なものでもない。

様式ＰＣＴ／ＩＳＡ／２３７（第Ⅴ欄）（２００９年７月）

補充欄

いずれかの欄の大きさが足りない場合

第　　欄の続き

H01L21/8234(2006.01)i, H01L21/28(2006.01)i, H01L21/76(2006.01)i,
H01L21/8238(2006.01)i, H01L21/8244(2006.01)i, H01L27/088(2006.01)i,
H01L27/092(2006.01)i, H01L27/10(2006.01)i, H01L27/11(2006.01)i,
H01L29/423(2006.01)i, H01L29/49(2006.01)i

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	085393-0935
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yoshihiro		SATO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Toyama	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Panasonic Corporation		
Address 2	1006, Oaza Kadoma		
City	Kadoma-shi, Osaka	**State/Province**	
Postal Code	571-8501	**Country** i	JP

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hideyuki		ARAI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Toyama	Country of Residence i	JP

Mailing Address of Inventor:

Address 1	c/o Panasonic Corporation		
Address 2	1006, Oaza Kadoma		
City	Kadoma-shi, Osaka	**State/Province**	
Postal Code	571-8501	**Country** i	JP

Inventor 3 Remove

Legal Name

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	085393-0935
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Takayuki		YAMADA	

Residence Information (Select One) ◯ US Residency ◉ Non US Residency ◯ Active US Military Service

City	Toyama	Country of Residence i	JP

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City	Kadoma-shi, Osaka	**State/Province**	
Postal Code	571-8501	**Country** i	JP

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

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Customer Number	53080		
Email Address	washington_ip_docket@mwe.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE		
Attorney Docket Number	085393-0935	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	16	**Suggested Figure for Publication (if any)**	1

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

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Representative Information:

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	085393-0935
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

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Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	PCT/JP2011/006167	2011-11-04

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Remove

Application Number	Country i	Filing Date (YYYY-MM-DD)	Priority Claimed
2011-068131	JP	2011-03-25	◉ Yes ○ No

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Authorization to Permit Access:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	085393-0935
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE	

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In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

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Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

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◉	Assignee	○	Legal Representative under 35 U.S.C. 117
○	Person to whom the inventor is obligated to assign.	○	Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :	

If the Assignee is an Organization check here. ☒

Organization Name	Panasonic Corporation

Mailing Address Information:

Address 1	1006, Oaza Kadoma		
Address 2			
City	Kadoma-shi, Osaka	**State/Province**	
Country [i]	JP	Postal Code	571-8501
Phone Number		Fax Number	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	085393-0935
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Signature	/michael e. fogarty/			Date (YYYY-MM-DD)	2012-10-31
First Name	Michael	Last Name	Fogarty	Registration Number	36139

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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PATENT ABSTRACTS OF JAPAN

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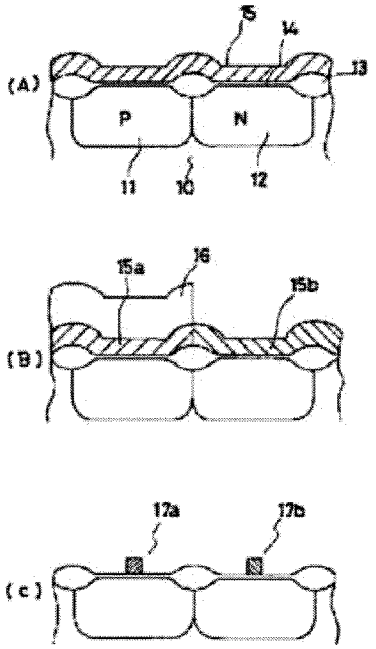
(51)Int.Cl. H01L 27/092
H01L 21/265

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(22)Date of filing : 22.03.1993

(71)Applicant : RICOH CO LTD
(72)Inventor : ISHIDA MAMORU

(54) MANUFACTURE OF DUAL GATE CMOS SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To suppress the diffusion of boron by lowering process temperature and also, prevent the partial cavity growth or resistance increase of a p-type polysilicon gate electrode when manufacturing a dual gate CMOS type semiconductor device.
CONSTITUTION: An n-type conductive polysilicon film 15, where n-type impurities exist uniformly within a film, is formed on the gate oxide film 14 on a silicon substrate 10, and it is changed into a p-type polysilicon film by implanting ions of boron into the polysilicon film 15 in a PMOSFET type region. Gate electrodes 17a and 17b are formed by patterning the polysilicon films 15a and 15b. Then, for both MOSFETs, impurities are implanted into a board with gate electrodes as masks. The temperature of activation of implanted impurities is set rather low at 800-900° C.



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審査請求　未請求　請求項の数３　ＦＤ　（全　６　頁）

(21)出願番号　特願平5－88124

(22)出願日　平成５年(1993)３月22日

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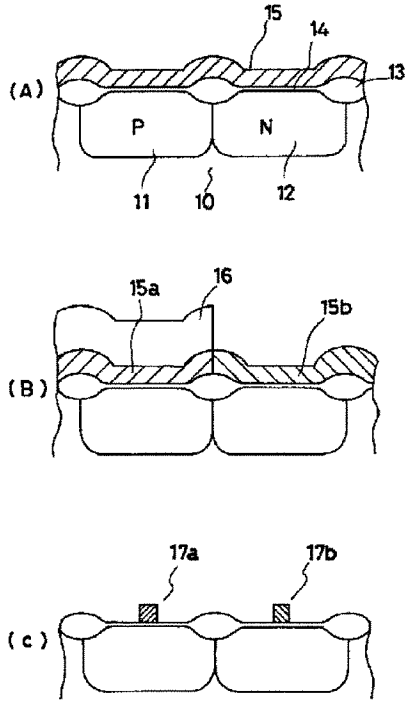
(74)代理人　弁理士　野口　繁雄

(54)【発明の名称】　デュアルゲートＣＭＯＳ型半導体装置の製造方法

(57)【要約】

【目的】　デュアルゲートＣＭＯＳ型半導体装置を製造する際に、プロセス温度を下げてボロンの拡散を抑えるとともに、Ｎ型ポリシリコンゲート電極の部分空乏化や高抵抗化を防ぐ。

【構成】　シリコン基板１０上のゲート酸化膜１４上に膜内にＮ型不純物が均一に存在したＮ型導電性ポリシリコン膜１５を形成し、ＰＭＯＳＦＥＴ形成領域のポリシリコン膜１５にボロンをイオン注入してＰ型ポリシリコン膜１５ｂに変える。ポリシリコン膜１５ａ，１５ｂをパターン化してゲート電極１７ａ，１７ｂを形成する。その後、両ＭＯＳＦＥＴ用にゲート電極をマスクとしてセルフアラインで不純物を基板に導入する。導入不純物の活性化温度は８００～９００℃と低めに設定する。



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【特許請求の範囲】

【請求項1】　以下の工程（A）から（D）を含むデュアルゲートCMOS型半導体装置の製造方法。

（A）シリコン基板上にゲート酸化膜を介してN型導電性ポリシリコン膜を形成する工程、

（B）NチャネルMOS型素子形成領域をレジストで被い、PチャネルMOS型素子形成領域のポリシリコン膜にP型不純物を導入してそのPチャネルMOS型素子形成領域のポリシリコン膜をP型導電性に変える工程、

（C）前記ポリシリコン膜をパターン化してNチャネル型MOS素子形成領域とPチャネル型MOS素子形成領域とにそれぞれゲート電極を形成する工程、

（D）NチャネルMOS型素子形成領域とPチャネル型MOS素子形成領域の基板に少なくともソース領域とドレイン領域を形成するために、それぞれの導電型の不純物を導入する工程。

【請求項2】　以下の工程（A）から（E）を含むデュアルゲートCMOS型半導体装置の製造方法。

（A）シリコン基板上にゲート酸化膜を介してゲート電極として必要な濃度よりも低濃度のN型導電性ポリシリコン膜を形成する工程、

（B）PチャネルMOS型素子形成領域をレジストで被い、NチャネルMOS型素子形成領域のポリシリコン膜にN型不純物を導入してそのNチャネルMOS型素子形成領域のポリシリコン膜をゲート電極として必要な濃度のN型導電性にする工程、

（C）NチャネルMOS型素子形成領域をレジストで被い、PチャネルMOS型素子形成領域のポリシリコン膜にP型不純物を導入してそのPチャネルMOS型素子形成領域のポリシリコン膜をゲート電極として必要な濃度のP型導電性に変える工程、

（D）前記ポリシリコン膜をパターン化してNチャネル型MOS素子形成領域とPチャネル型MOS素子形成領域とにそれぞれゲート電極を形成する工程、

（E）NチャネルMOS型素子形成領域とPチャネル型MOS素子形成領域の基板に少なくともソース領域とドレイン領域を形成するために、それぞれの導電型の不純物を導入する工程。

【請求項3】　以下の工程（A）から（D）を含むデュアルゲートCMOS型半導体装置の製造方法。

（A）シリコン基板上にゲート酸化膜を介してゲート電極として必要な濃度よりも低濃度のN型導電性ポリシリコン膜を形成する工程、

（B）前記ポリシリコン膜をパターン化してNチャネル型MOS素子形成領域とPチャネル型MOS素子形成領域とにそれぞれゲート電極を形成する工程、

（C）NチャネルMOS型素子のソース領域とドレイン領域を形成するための基板へのN型不純物の注入と同時に、NチャネルMOS型素子のゲート電極にもN型不純物を注入してそのNチャネル型MOS素子のゲート電極をゲート電極として必要な濃度のN型導電性にする工程、

2

（D）PチャネルMOS型素子のソース領域とドレイン領域を形成するための基板へのP型不純物の注入と同時に、PチャネルMOS型素子のゲート電極にもP型不純物を注入してそのPチャネルMOS型素子のゲート電極をゲート電極として必要な濃度のP型導電性に変える工程、

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明はMOS型半導体装置の製造方法に関し、特にPチャネル型MOS（以下、PMOSという）素子にはP型導電性のポリシリコンゲート電極を備え、NチャネルMOS（以下、NMOSという）素子にはN型導電性のポリシリコンゲート電極を備えたデュアルゲート型CMOS半導体装置であって、例えばサブミクロン以下のような微細パターンを有するCMOS型半導体装置の製造方法に関するものである。

【0002】

【従来の技術】一般に、半導体集積回路装置（以下、LSIという）プロセスは、微細化が進むほどその工程数が増加する傾向にある。また、MOS型LSIのプロセスでは、微細化が進むほど短チャネル効果やホットキャリア効果など種々の問題が生じる。

【0003】同一基板にNMOSFETとPMOSFETを形成したCMOSデバイスでは、ポリシリコンゲート電極としてはN^+ポリシリコンゲート電極が広く用いられている。これは、ポリシリコン膜上にリンガラスを堆積し、熱処理によってリンをポリシリコン膜に拡散させて低抵抗化を図ったポリシリコンゲート電極である。そのようなCMOSデバイスでは、NMOSFET側を表面チャネル型、PMOSFET側を埋込みチャネル型にしている場合が多い。

【0004】しかし、微細化が進みサブミクロン以下やハーフミクロン以下のプロセスになると、埋込み型構造では短チャネル効果を抑制することが困難になるため、PMOSFET側も表面型に移行せざるを得ない状況になっている。その場合、PMOSFET側用に新たにP^+ポリシリコンゲート電極（アクセプタ注入によるポリシリコンゲート電極の低抵抗化）や、N^+ポリシリコンゲート電極とP^+ポリシリコンゲート電極とを接続するためのサリサイド構造の採用が必要になるなど、工程数は増加する一方である。

【0005】また、P^+ポリシリコンゲート電極の採用に当り、ゲート電極の低抵抗化は不純物注入による手法を用いなければならないが、注入時又はその注入不純物の活性化時において、ゲート電極に注入された不純物がゲート酸化膜を突き抜けて基板チャネル部分へ侵入してしまう恐れが生じる。チャネル部分に不純物が侵入すると、しきい値電圧がシフトしたり、耐圧劣化などの諸問

題が生じ、所望のＭＯＳＦＥＴ特性が得られなくなる。

【０００６】

【発明が解決しようとする課題】Ｐ型ポリシリコンゲート電極用に導入されるボロンはゲート酸化膜中の拡散係数が大きく、ＭＯＳＦＥＴのチャネル濃度を変化させ、しきい値電圧を変化させてしまう。その問題を解決するためには、プロセス温度を下げてボロンの拡散を抑制する方法が有効である。しかし、プロセス温度を下げると、Ｎ型ポリシリコンゲートに導入される砒素やリンの拡散はボロン以上に抑えられ、Ｎ型ポリシリコンゲート電極を部分空乏化したり高抵抗化させる問題が生じる。その結果、ＮＭＯＳＦＥＴのしきい値電圧を変化させたり、ＣＭＯＳデバイスの高速動作の障害になる。

【０００７】プロセス温度を下げることに伴う問題は、特にＮＭＯＳＦＥＴのゲート電極をマスクとしてソース領域とドレイン領域をセルフアラインで形成する工程で、ゲート電極への不純物導入と基板への不純物導入を同時に行なおうとするプロセスでより重要となる。なぜならば、ソース領域とドレイン領域にはより浅い不純物濃度プロファイルの実現が望まれ、ゲート電極への導入とは要求が相反するためである。本発明はプロセス温度を低温化してボロンの拡散を抑えるとともに、Ｎ型ポリシリコンゲート電極の部分空乏化や高抵抗化を防ぐことのできるデュアルゲートＣＭＯＳ型半導体装置の製造方法を提供することを目的とするものである。

【０００８】

【課題を解決するための手段】本発明は、以下の工程（Ａ）から（Ｄ）を含んでいる。（Ａ）シリコン基板上にゲート酸化膜を介してＮ型導電性ポリシリコン膜を形成する工程、（Ｂ）ＮチャネルＭＯＳ型素子形成領域をレジストで被い、ＰチャネルＭＯＳ型素子形成領域のポリシリコン膜にＰ型不純物を導入してそのＰチャネルＭＯＳ型素子形成領域のポリシリコン膜をＰ型導電性に変える工程、（Ｃ）前記ポリシリコン膜をパターン化してＮチャネル型ＭＯＳ素子形成領域とＰチャネル型ＭＯＳ素子形成領域とにそれぞれゲート電極を形成する工程、（Ｄ）Ｎチャネル型ＭＯＳ素子形成領域とＰチャネル型ＭＯＳ素子形成領域の基板に少なくともソース領域とドレイン領域を形成するために、それぞれの導電型の不純物を導入する工程。

【０００９】好ましい態様では、上記の工程（Ａ）で形成されるＮ型導電性ポリシリコン膜のＮ型不純物濃度をゲート電極として必要な濃度よりも低濃度にしておき、上記工程（Ｂ）でＰチャネルＭＯＳ型素子形成領域のポリシリコン膜をＰ型導電性に変える際のＰ型不純物の注入量が少なくてすむようにする。ＮチャネルＭＯＳ型素子形成領域ではポリシリコン膜にさらにＮ型不純物を注入してゲート電極として必要な濃度まで高める。

【００１０】他の好ましい態様では、上記の工程（Ａ）で形成されるＮ型導電性ポリシリコン膜のＮ型不純物濃度をゲート電極として必要な濃度よりも低濃度にしておき、ポリシリコン膜をパターン化してゲート電極パターンを形成した後、ソース領域とドレイン領域を形成するための基板への不純物注入と同時にゲート電極にも不純物を注入してゲート電極を低抵抗化する。

【００１１】

【実施例】図１は第１の実施例を表わす。

（Ａ）シリコン基板１０にＰウエル１１、Ｎウエル１２、フィールド酸化膜１３及びゲート酸化膜１４を形成する。ゲート酸化膜１４上にＮ型導電性ポリシリコン膜１５を形成する。ポリシリコン膜１５はリン又は砒素を反応ガスに添加したＣＶＤ法によって形成することができる。Ｎ型導電性ポリシリコン膜１５を形成する他の方法は、不純物が導入されていないポリシリコン膜をＣＶＤ法によって堆積し、リン又は砒素をイオン注入した後、十分活性化させる方法である。ポリシリコン膜１５は膜内にＮ型不純物が均一に存在している。このときのＮ型不純物量はＮ型ポリシリコンゲート電極の空乏化を防ぐのに必要な濃度であるとともに、後の工程でＰ型不純物を導入することによってＰ型導電性に変えることのできる程度の濃度である。したがって、ポリシリコン膜１５中のＮ型不純物濃度はプロセス条件の選択によって最適範囲は変化するが、1×10^{19}～2×10^{20}／cm^3の範囲が適当である。Ｎ型ポリシリコン膜１５の一例は、ジシランとホスフィンを反応ガスとするＬＰＣＶＤ法で成膜したリンドープポリシリコン膜であり、膜厚は約３５００Åである。

【００１２】（Ｂ）ＮＭＯＳＦＥＴ形成領域をフォトレジスト膜１６によって被い、ＰＭＯＳＦＥＴ形成領域のポリシリコン膜１５にボロンをイオン注入する。このときのボロン注入量はポリシリコン膜１５中の不純物量の少なくとも２倍、望ましくは４倍程度に設定する。この結果、ポリシリコン膜１５はフォトレジスト膜１６で被われている領域のＮ型ポリシリコン膜１５ａと、Ｐ型に変化したＰ型ポリシリコン膜１５ｂとに分かれる。

【００１３】（Ｃ）フォトレジスト膜１６を除去した後、再びフォトレジスト膜を形成し、写真製版とエッチングによってポリシリコン膜１５ａ，１５ｂにパターン化を施してゲート電極１７ａと１７ｂを形成する。その後、既知のプロセスにより、ＮＭＯＳＦＥＴ用にはゲート電極１７ａをマスクとしてセルフアラインでＮ型不純物の砒素又はリンを基板に導入し、ＰＭＯＳＦＥＴ用にはゲート電極１７ｂをマスクとしてセルフアラインでＰ型不純物のボロンを基板に導入する。

【００１４】ゲート電極１７ａ，１７ｂに導入された不純物は、工程（Ｃ）でパターン化される前に熱処理を行なって活性化してもよく、パターン化後に活性化してもよい。また、ソース領域・ドレイン領域に導入された不純物の活性化と同時に行なってもよい。活性化温度は８００～９００℃、望ましくは８００～８５０℃である。

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【0015】図2は第2の実施例を表わす。

（A）図1と同様にポリシリコン膜25を形成する。この場合、ポリシリコン膜25の不純物濃度は少なくとも1×10^{19}、望ましくは5×10^{19}／cm^3とする。この場合も不純物はポリシリコン膜25の膜内に均一に存在している。

（B）既知の写真製版とエッチングによりポリシリコン膜25をパターン化してゲート電極27を形成する。

【0016】（C）PMOSFET形成領域をフォトレジスト膜26で被い、NMOSFET形成領域にN型不純物をイオン注入する。これによりNMOSFETのゲート電極27aとソース・ドレイン領域28に同時に不純物が導入されて、ゲート電極27aの低抵抗化とソース・ドレイン領域28の形成が同時になされる。フォトレジスト膜26を除去した後、活性化を行なう。ソース・ドレイン領域28には浅い不純物導入領域が形成され、一方ゲート電極27aに導入された不純物は通常のゲート電極の膜厚であればその表面付近にのみ偏在してしまうが、ポリシリコン膜25が当初からN型導電性であるためNMOSFETのしきい値電圧変動やCMOSデバイスの動作速度上の問題は生じない。

【0017】（D）上記の工程（C）とは逆に、NMOSFET形成領域をフォトレジスト膜29によって被い、P型不純物をイオン注入してPMOSFETのゲート電極27bの低抵抗化とソース・ドレイン領域30の形成を同時に行なう。フォトレジスト膜29を除去した後、活性化を行なう。このとき、P型不純物の注入量はゲート電極27bを当初のN型導電性からP型導電性へと極性を判定させなければならないため、ポリシリコン膜25のN型不純物量の少なくとも2倍、望ましくは4倍に設定する。P型不純物のボロンはポリシリコン膜中での拡散が速いので、ゲート電極27bは均一にP型導電性を示すようになる。しかし、活性化温度が高すぎるとMOSFETのチャネル濃度変化の問題が発生するので、活性化温度は800～900℃、望ましくは800～850℃以下とする。

【0018】図3は図2のプロセスを用いて作成したデュアルゲート構造のCMOSを表わしている。図3のCMOSデバイスを製造するために、図2に従いPウエル11、Nウエル12、フィールド酸化膜13及びゲート酸化膜14を形成した後、N型ポリシリコン膜25を形成する。ポリシリコン膜25はジシランとホスフィンを反応ガスとするLPCVD法で成膜した膜厚3500Å、膜中リン濃度5×10^{19}／cm^3のリンドープポリシリコン膜である。そのポリシリコン膜25をパターン化してゲート電極27を形成する。

【0019】次に、フォトレジスト膜をマスクとしてNMOSFETのゲート電極27a及びソース・ドレイン領域28並びにNウエル12の基板コンタクト領域36に砒素をイオン注入する。注入エネルギーは30Ke

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V、ドーズ量は1×10^{15}／cm^2である。この後900℃で30分間の活性化を行なう。次に、フォトレジスト膜を形成しなおし、そのフォトレジスト膜をマスクとしてPMOSFETのゲート電極27b及びソース・ドレイン領域30並びにPウエル11の基板コンタクト領域37にBF_2をイオン注入する。注入エネルギーは20KeV、ドーズ量は3×10^{15}／cm^2である。この後850℃で30分間の活性化を行なう。

【0020】次に、既知のプロセスにより、チタンシリサイド38をサリサイドセルフアラインプロセスにより両MOSFETのゲート電極、ソース領域、ドレイン領域及び基板コンタクト上に形成する。次に、層間絶縁膜39を形成した後、コンタクトホールを開口し、メタル電極40を形成する。

【0021】比較例として、不純物を導入しないノンドープポリシリコン膜を用い、図3を参照して説明したプロセスと同じプロセスによってCMOSデバイスを形成した。比較例のプロセスは従来のプロセスである。図3の実施例と比較例のしきい値電圧を比較した結果を図4に示す。PMOSFETでは実施例と比較例の差はない。しかし、NMOSFETの場合は比較例の方が大きな値になっており、比較例のN型ポリシリコンゲート電極は部分空乏化していることが予想される。

【0022】そこで、ゲート面積の大きなNMOSFETを用いて1MHzの周波数で高周波CV測定を行なった。実施例の場合は計算値と一致する酸化膜容量が検出された。それに対し、比較例の場合は計算値の半分程度の酸化膜容量しか検出されなかった。このことから比較例のポリシリコンゲート電極は部分空乏化しており、そのため高周波に対する応答が悪くなっていると考えられる。

【0023】

【発明の効果】本発明により製造したデュアルゲートCMOSデバイスはプロセス温度が低く抑えられているため、P型ポリシリコンゲート電極中のボロンの拡散によるMOSFETのチャネル濃度が変化してしきい値電圧が変化する問題は発生しない。また、N型ポリシリコンゲート電極には予め均一に不純物を存在させてあるため、プロセス温度が低いことによる拡散不足の問題も発生しない。

【図面の簡単な説明】

【図1】第1の実施例を示す工程断面図である。

【図2】第2の実施例を示す工程断面図である。

【図3】図2の工程により製造したCMOSデバイスを示す断面図である。

【図4】実施例と従来例を比較するしきい値電圧の図である。

【符号の説明】

10　シリコン基板

11　Pウエル

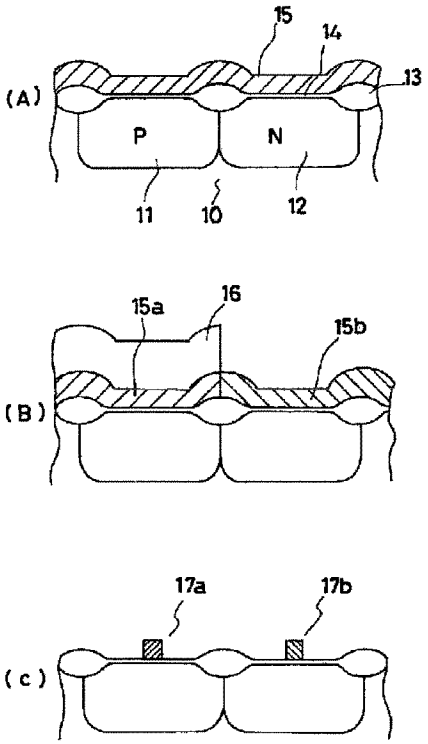
7

12　　Nウエル
14　　ゲート酸化膜
15，15a，25　　N型ポリシリコン膜
15b　　P型に変わったポリシリコン膜

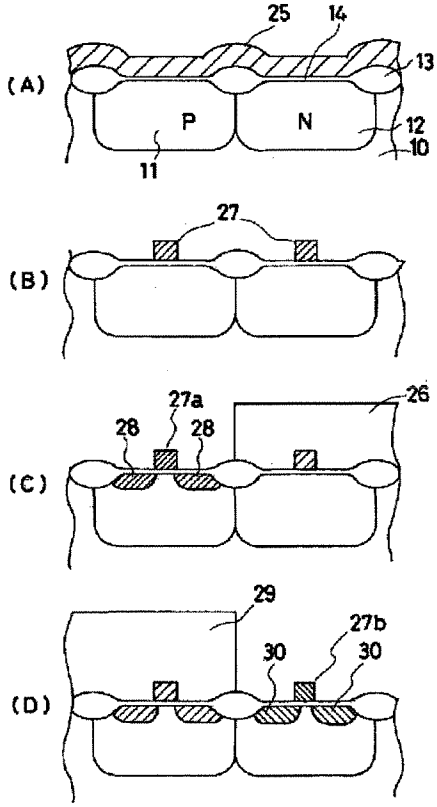
8

＊17a，27a　　N型ポリシリコンゲート電極
17b，27b　　P型ポリシリコンゲート電極
28，30　　ソース・ドレイン領域
＊

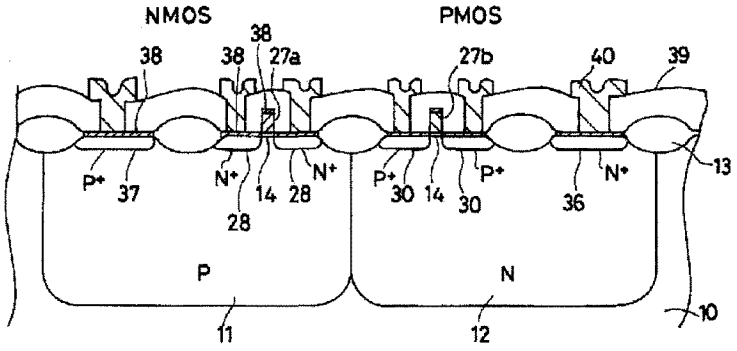
【図1】



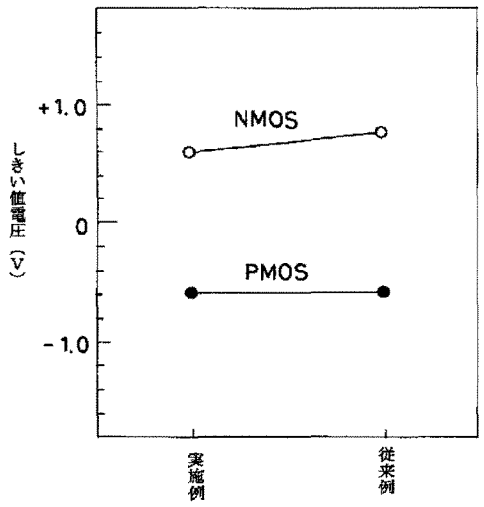
【図2】



【図3】



【図４】



PATENT ABSTRACTS OF JAPAN

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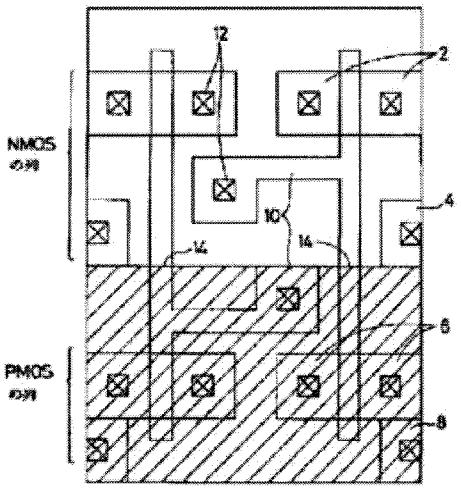
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(54) DUAL GATE CMOS SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To restrain change of element characteristics which is caused by mutual diffusion of impurities of gate electrodes.
CONSTITUTION: An SRAM is formed of the source.drain region 2 of an NMOSFET, the substrate contact region 4 of the NMOSFET, the source.drain region 6 of a PMOSFET, the substrate contact region 8 of the PMOSFET, and a polysilicon gate 10. Before a gate polysilicon film is patterned, ions are implanted in the gate electrode 10 by using a mask having the same pattern as a well forming mask. P-type impurities are implanted in the hatched part. N-type impurities are implanted in the part except the hatched part.



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審査請求　未請求　請求項の数７　ＦＤ　（全　６　頁）

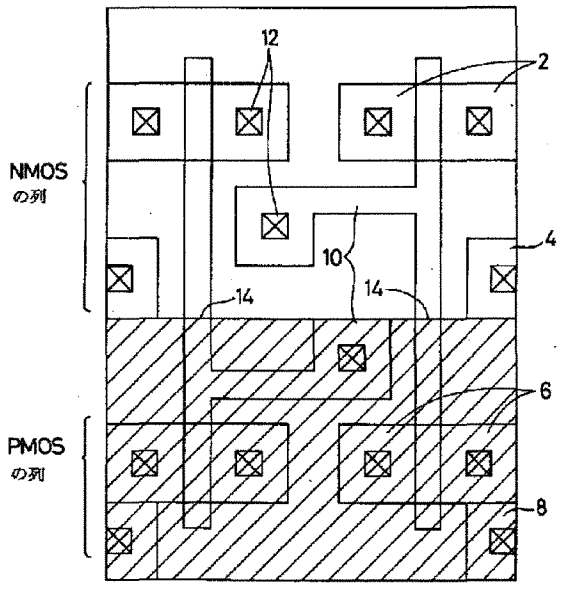
(21)出願番号　特願平6－173513

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(54)【発明の名称】　デュアルゲートＣＭＯＳ半導体装置とその製造方法

(57)【要約】
【目的】　ゲート電極の不純物の相互拡散による素子特性の変動を抑える。
【構成】　ＮＭＯＳＦＥＴのソース・ドレイン領域２、ＮＭＯＳＦＥＴの基板コンタクト領域４、ＰＭＯＳＦＥＴのソース・ドレイン領域６、ＰＭＯＳＦＥＴの基板コンタクト領域８、ポリシリコンゲート電極１０によりＳＲＡＭが形成されている。ゲート電極１０のためのイオン注入はゲートポリシリコン膜をパターン化する前に、ウエル形成マスクと同一パターンのマスクを用いて行なわれ、斜線の施された領域にはＰ型不純物が注入され、斜線部以外の領域にはＮ型不純物が注入されている。



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【特許請求の範囲】

【請求項1】　Nチャネル型MOSFETのゲート電極としてN型ポリシリコンが用いられ、Pチャネル型MOSFETのゲート電極としてP型ポリシリコンが用いられているCMOS半導体装置において、

前記ポリシリコンゲート電極のN型とP型の境界がウエルの分離位置に対応した位置にのみ設けられていることを特徴とするデュアルゲートCMOS半導体装置。

【請求項2】　前記ポリシリコンゲート電極上には高融点金属シリサイド層が形成されている請求項1に記載のデュアルゲートCMOS半導体装置。

【請求項3】　半導体基板上にゲート絶縁膜を介してポリシリコン膜を形成した後、そのポリシリコン膜をゲート電極形状にパターン化する前又はパターン化後に、次の（A）から（D）のいずれかのマスクに該当するマスクを用いてそのポリシリコン膜にイオン注入を施してN型領域とP型領域を形成する工程を含むことを特徴とするデュアルゲートCMOS半導体装置の製造方法。

（A）ウエル形成マスク

（B）ウエル形成マスクのパターン寸法を変えたマスク

（C）ウエル形成マスクのパターンを反転させ、又はさらにその寸法を変えたマスク

（D）ウエル形成マスクを基準にしてそれと同一寸法でもしくはパターン寸法を変えて作成された他のイオン注入マスク、又は前記他のイオン注入マスクのパターンを反転させたマスク。

【請求項4】　前記ポリシリコン膜にN型領域とP型領域を形成するイオン注入工程は、そのポリシリコン膜のゲート電極へのパターン化前である請求項3に記載のデュアルゲートCMOS半導体装置の製造方法。

【請求項5】　前記ポリシリコン膜にN型領域とP型領域を形成するイオン注入を施した後、ソース・ドレイン領域形成のためのイオン注入工程までの間にそのポリシリコン膜上に高融点金属シリサイド膜を形成し、さらにその上にソース・ドレイン形成のためのイオン注入工程でのイオンがゲート電極に注入されるのを阻止するキャップ材を形成する請求項4に記載のデュアルゲートCMOS半導体装置の製造方法。

【請求項6】　ソース・ドレイン形成のためのイオン注入後、前記キャップ材の全て又は一部を除去する請求項5に記載のデュアルゲートCMOS半導体装置の製造方法。

【請求項7】　前記キャップ材がSiO_2膜であり、その膜厚はソース・ドレイン形成のためのイオン注入工程での不純物飛程以上であり、かつ、そのキャップ材の除去にはフッ酸を含むエッチング液を用いる請求項6に記載のデュアルゲートCMOS半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明はNチャネル型MOSFET（以下NMOSFETという）のゲート電極としてN型ポリシリコンが用いられ、Pチャネル型MOSFET（以下PMOSFETという）のゲート電極としてP型ポリシリコンが用いられているデュアルゲートCMOS半導体装置とその製造方法に関するものである。

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【0002】

【従来の技術】一般に、半導体集積回路装置プロセスは、微細化が進むほどその工程数が増加する傾向にある。また、MOS半導体装置のプロセスでは、微細化が進むほど短チャネル効果やホットキャリア効果など種々の問題が生じる。

【0003】同一基板にNMOSFETとPMOSFETを形成したMOS半導体装置では、ポリシリコンゲート電極としてはN^+ポリシリコンゲート電極が広く用いられている。これは、ポリシリコン膜上にリンガラスを堆積し、熱処理によってリンをポリシリコン膜に拡散させて低抵抗化を図ったシリコンゲート電極である。そのようなCMOS半導体装置では、Nチャネル側を表面チャネル型、Pチャネル側を埋込みチャネル型にしている場合が多い。

【0004】しかし、サブハーフミクロン以下やクウォータミクロン以下と称されるような微細な半導体装置のプロセスでは、埋込み型構造では短チャネル効果を抑制することが困難になるため、Pチャネル型も表面型に移行せざるを得ない状況になっている。その結果として、NMOSFETのゲート電極をN型とし、PMOSFETのゲート電極をP型としたデュアルゲートCMOS半導体装置が用いられるようになってきている。

【0005】デュアルゲートCMOS半導体装置では、N型のポリシリコンゲート電極とP型のポリシリコンゲート電極とを接続するために、ポリシリコンゲート電極上に高融点金属シリサイド層が形成される。その場合、ポリシリコンゲート電極のN型領域とP型領域の境界ではその中の不純物が高融点金属シリサイド層又はポリシリコンゲート電極介して相互に拡散し、その結果、ゲート電極の仕事関数が変化してFETのしきい値電圧が変動する。この相互拡散は、ポリシリコンだけでなく、高融点金属シリサイド中での不純物の拡散速度が非常に大きいことが原因になっている。

【0006】ゲート電極用のポリシリコン膜にN型領域とP型領域を形成する方法として、従来はソース・ドレイン領域と基板コンタクト領域へのN型不純物注入マスクとP型不純物注入マスクの寸法を変化させたものをマスクに用いて、ゲート電極用のポリシリコン膜にイオン注入している。

【0007】SRAMのゲート電極にN型領域とP型領域を形成するためのイオン注入を行なう例を図1に示す。2はNMOSFETのソース・ドレイン領域、4はNMOSFETの基板コンタクト領域、6はPMOSFETのソース・ドレイン領域、8はPMOSFETの基

板コンタクト領域であり、１０はポリシリコンゲート電極、１２はコンタクトホールである。斜線の施された領域はソース・ドレイン及び基板コンタクトのためのＰ型不純物注入マスクをフィールドに対してオーバーサイズしたマスクを用いて形成されたゲート電極用ポリシリコン膜へのＰ型不純物注入領域、斜線部以外の領域はＮ型不純物注入領域である。

【０００８】

【発明が解決しようとする課題】このような、ソース・ドレインと基板コンタクトへの不純物注入用のマスクを基準にして作成したマスクを用いてゲート電極のポリシリコン膜のＮ型領域とＰ型領域を形成すると、次のような問題が発生する。

（１）ゲート電極のＮ型領域とＰ型領域の境界１４がフィールドに近い位置に設定され、相互拡散の問題がいっそう顕著になる。

（２）ゲート電極には境界１６のように、より多くのＮ型とＰ型の境界ができる。

これらの問題は、例えばＳＲＡＭのように高密度に素子がレイアウトされるＬＳＩでより大きな問題であり、微細化及び高集積化に対する阻害要因になっている。

【０００９】本発明はゲート電極でのＮ型とＰ型の境界をフィールドに近づけないようにするとともに、その数を増やさないようにすることにより、ゲート電極の不純物の相互拡散による素子特性の変動を抑えたデュアルゲートＣＭＯＳ半導体装置を提供することを目的とするものである。本発明はまたそのような半導体装置を製造する方法を提供することを目的とするものである。

【００１０】

【課題を解決するための手段】ポリシリコンゲート電極でのＮ型とＰ型の境界をフィールドに近づけないようにするとともに、その数を増やさないようにするために、本発明ではポリシリコンゲート電極のＮ型とＰ型の境界がウエルの分離位置に対応した位置にのみ設けられているようにする。そして、ポリシリコンゲート電極上には高融点金属シリサイド層が形成されていることが好ましい。

【００１１】ポリシリコンゲート電極でのＮ型とＰ型の境界をこのように定めるために、本発明の製造方法では、半導体基板上にゲート絶縁膜を介してポリシリコン膜を形成した後、そのポリシリコン膜をゲート電極形状にパターン化する前又はパターン化後に、次の（Ａ）から（Ｄ）のいずれかのマスクに該当するマスクを用いてそのポリシリコン膜にイオン注入を施してＮ型領域とＰ型領域を形成する。

（Ａ）ウエル形成マスク

（Ｂ）ウエル形成マスクのパターン寸法を変えたマスク

（Ｃ）ウエル形成マスクのパターンを反転させ、又はさらにその寸法を変えたマスク

（Ｄ）ウエル形成マスクを基準にしてそれと同一寸法でもしくはパターン寸法を変えて作成された他のイオン注入マスク、又は前記他のイオン注入マスクのパターンを反転させたマスク。

【００１２】すでにパターン化されたポリシリコンゲート電極に対し、本発明のマスクを用いて例えばＰ型不純物をイオン注入する場合には、ゲート電極だけでなくＰＭＯＳＦＥＴのソース・ドレインと逆導電型であるＰＭＯＳＦＥＴの基板にも不純物が注入されるため、注入条件、活性化条件、逆導電型基板領域の形成条件など全てを考慮しなければならず、条件範囲が大幅に狭くなる。そのため、ゲートポリシリコンへのイオン注入は、ポリシリコン膜をゲート電極形状にパターン化する前に行なうことによって不必要な領域への注入を阻止できる。

【００１３】また、後工程で行なわれるソース・ドレイン及び基板コンタクト領域へのイオン注入の条件によっては、ゲート電極に新たにＮ型不純物とＰ型不純物が注入されて境界が発生するおそれがある。これを防止するために、ゲート電極へのイオン注入後にゲート電極上にキャップ材を形成し、後工程でのゲート電極への不純物導入を阻止するのが効果的である。キャップ材の膜厚は少なくとも後工程での注入不純物飛程以上が必要であり、注入不純物の大部分がキャップ材にのみ注入されるようにする。キャップ材としてSiO_2膜厚を用いる場合は、少なくとも５０ｎｍの膜厚が必要である。キャップ材としてはSiO_2に限らずシリコン窒化膜やポリシリコン膜を用いることもできる。

【００１４】キャップ材を形成したときは、後工程のイオン注入が終わった後、そのキャップ材を除去することによって後工程でキャップ材に注入された不純物を取り除き、ゲート電極へその不純物が拡散するのを未然に防ぐことができる。キャップ材としてSiO_2を使用した場合にはフッ酸（ＨＦ）を含むエッチング液で除去すれば、シリコンに対して高選択比でエッチング除去できる。

【００１５】

【実施例】図２は本発明をＳＲＡＭのゲート電極形成に適用した一実施例を表わす。図１と同一部分には同一の符号を用いる。２はＮＭＯＳＦＥＴのソース・ドレイン領域、４はＮＭＯＳＦＥＴの基板コンタクト領域、６はＰＭＯＳＦＥＴのソース・ドレイン領域、８はＰＭＯＳＦＥＴの基板コンタクト領域であり、１０はポリシリコンゲート電極、１２はコンタクトホールである。

【００１６】ゲート電極１０のためのイオン注入はゲートポリシリコン膜をパターン化する前に、ウエル形成マスクと同一パターンのマスクを用いて行なわれ、斜線の施された領域にはＰ型不純物が注入され、斜線部以外の領域にはＮ型不純物が注入されている。

【００１７】図２の不純物注入領域を図１のものと比較すると、ゲート電極のＮ型とＰ型の境界１４がＮＭＯＳＦＥＴからもＰＭＯＳＦＥＴからも離れた位置に形成さ

れている点で異なっている。また、ゲート電極でのN型とP型の境界１６がなく、図１のものよりも境界の数が少なくなり、抵抗値が低くなっていることも分かる。

【００１８】図３は本発明の製造方法を用いて形成されるＣＭＯＳ半導体装置の一例を模式的に示したものである。シリコン基板２０にPウエル２２とNウエル２４が互いに隣接して形成されている。Pウエル２２にはＬＤＤ（Lightly Doped Drain）構造のＮＭＯＳＦＥＴが形成されている。すなわち、高濃度N型不純物領域によるソース・ドレイン２６のチャネル側には低濃度のN型不純物領域２８が形成され、チャネル領域上にはゲート酸化膜３０を介してN型ポリシリコンゲート電極３２が形成されている。３４は絶縁物のサイドウォールである。

【００１９】Nウエル２４にはシングルドレイン構造のＰＭＯＳＦＥＴが形成されており、３８はP型不純物拡散領域のソース・ドレインであり、チャネル領域上にはゲート酸化膜３０を介してP型ポリシリコンゲート電極４０が形成されている。N型ポリシリコンゲート電極３２とP型ポリシリコンゲート電極４０はフィールド酸化膜４２上の境界１４でつながっており、ポリシリコンゲート電極３２，４０上にはタングステンシリサイドのような高融点金属シリサイド層４４が形成されている。境界１４はウエル２２と２４の境界上にのみ形成されている。

【００２０】境界１４又は高融点金属シリサイド層４４を通って、P型ポリシリコンゲート電極４０のボロンがN型ポリシリコンゲート電極３２中へ拡散し、又はN型ポリシリコンゲート電極３２中の砒素がP型ポリシリコンゲート電極４０中へ拡散する相互拡散が起こっても、ポリシリコンゲート電極の境界１４がいずれのＭＯＳＦＥＴからも離れているため、相互拡散した不純物がＭＯＳＦＥＴのしきい値電圧を変化させるおそれが少ない。

【００２１】図４と図５により本発明の製造方法の一実施例を説明する。

（Ａ）シリコン基板２０の表面にPウエル２２及びNウエル２４を形成した後、ＬＯＣＯＳ（選択酸化）法によるフィールド酸化膜４２を形成する。その後、基板上にゲート酸化膜３０を熱酸化法によって成長させた後、ＬＰ－ＣＶＤ法により不純物が導入されていないポリシリコン膜５０を約２００ｎｍの厚さに堆積させる。ポリシリコン膜５０の全面にボロンイオンを１０ＫｅＶで、4×10^{15}／cm^2程度注入する。その後、ポリシリコン膜５０上にウエル形成時のマスクを用いてNウエル２４上をレジスト５２で被い、Pウエル２２上のポリシリコン膜５０のみに砒素イオンを３０ＫｅＶで6×10^{15}／cm^2程度注入する。これにより、Nウエル２４上のポリシリコン膜５０はP型ポリシリコン、それ以外の領域のポリシリコン膜５０はN型ポリシリコンとなる。

【００２２】（Ｂ）ポリシリコン膜５０上にスパッタリング法によりタングステンシリサイド（ＷＳｉｘ）膜４４を約７０ｎｍの厚さに全面に堆積する。さらに、そのタングステンシリサイド膜４４上にキャップ材として常圧ＣＶＤ法によってＮＳＧ（不純物が導入されていないシリコン酸化膜）５４を約５０ｎｍの厚さに堆積させる。

【００２３】（Ｃ）フォトリソグラフィーとドライエッチングによってＮＳＧ膜５４、ＷＳｉｘ膜４４及びポリシリコン膜５０をパターン化して積層ゲート電極５６，５８を形成する。Pウエル２２上ではＮＭＯＳＦＥＴ形成領域に開口を有するレジストパターンを形成し、それをマスクとしてＬＤＤ構造のN^-領域を形成するために、リン又は砒素のN型不純物を３５ＫｅＶで2×10^{13}／cm^2程度注入する。

【００２４】レジストを除去した後、全面にＨＴＯ膜（高温酸化膜）を形成し、エッチバックを施してゲート電極側面にサイドウォール３４を形成する。ＮＭＯＳＦＥＴのソース・ドレイン領域とＰＭＯＳＦＥＴの基板コンタクト領域にN^+領域を形成するために、砒素イオンを４０ＫｅＶで6×10^{15}／cm^2程度注入する。これにより、Pウエル２２のＮＭＯＳＦＥＴ形成領域には、N^-領域２８とN^+領域２６をもつソース・ドレインを有するＬＤＤ構造のＭＯＳＦＥＴが形成され、Nウエル２４には基板コンタクト領域６０が形成される。次に、そのレジストを除去し、今度はＰＭＯＳＦＥＴ形成領域とPウエル２２における基板コンタクト領域に開口をもつレジストパターンを形成し、それをマスクとしてBF_2イオンを３０ＫｅＶで3×10^{15}／cm^2程度注入する。これにより、NウエルにはＰＭＯＳＦＥＴのソース・ドレイン領域３８が形成され、Pウエル２２には基板コンタクト領域６２が形成される。

【００２５】（Ｅ）ゲート電極上に形成されていたキャップ材のＮＳＧ膜５４をＨＦを含む溶液によってエッチングして除去する。これにより、ゲート電極上層のＮＳＧ膜５４に注入されていた不純物が同時に取り除かれ、ゲート電極への新たな不純物導入が阻止される。

【００２６】（Ｆ）ＰＳＧ膜やＢＰＳＧ膜などの層間絶縁膜６４を堆積した後、８５０℃でリフローさせて表面を平坦化する。この熱処理で、ポリシリコン膜５０、N^-領域２８、N^+領域２６，６０、P^+領域３８，６２に注入されていた不純物が活性化される。層間絶縁膜６４にコンタクトホールを開けた後、アルミニウム又はアルミニウム合金によるメタル配線６６を形成する。

【００２７】ゲート電極用のポリシリコン膜をN型とP型に分けるために、実施例では初めに全面にP型不純物を注入し、その後N型とすべき領域にN型不純物を注入しているので、リソグラフィ工程が１回ですむ。しかし、N型とP型にそれぞれリソグラフィ工程でマスクを形成してイオン注入を行なうようにしてもよい。

【００２８】ポリシリコン膜をN型とP型に分けるためのイオン注入のためのマスクは、実施例ではウエル形成

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マスクを用いているが、ウエル形成マスクのパターン寸法を変えたマスク、ウエル形成マスクのパターンを反転させ、もしくはさらにその寸法を変えたマスク、ウエル形成マスクを基準にしてそれと同一寸法でもしくはパターン寸法を変えて作成された他のイオン注入マスク又はさらにその他のイオン注入マスクのパターンを反転させたマスクなどを使用してもよい。

【００２９】実施例では高融点金属シリサイド膜としてタングステンシリサイド膜４４を例示しているが、他の高融点金属シリサイド膜、例えばモリブデンシリサイド膜、タンタルシリサイド膜、チタンシリサイド膜などを用いてもよい。ＭＯＳＦＥＴの構造としてNチャネル型ではＬＤＤ構造とし、Ｐチャネル型ではシングルドレイン構造としているが、本発明ではＭＯＳＦＥＴの構造はこれらに限定されるものではない。

【００３０】

【発明の効果】本発明のデュアルゲートＣＭＯＳ半導体装置では、ゲート電極のＮ型とＰ型の境界がフィールドから離れた位置に形成されるので、不純物の相互拡散による素子特性の変動を抑えることができ、また微細化及び高集積化に適したＣＭＯＳ半導体装置とすることができる。本発明の製造方法では、ゲートポリシリコンへのイオン注入をポリシリコン膜をゲート電極形状にパターン化する前に行なうことによって不必要な領域への注入を阻止できる。また、ゲート電極へのイオン注入後にゲート電極上にキャップ材を形成することにより、後工程＊

8

＊で行なわれるソース・ドレイン及び基板コンタクト領域へのイオン注入工程でのゲート電極への不純物導入を阻止することができる。そして、そのキャップ材は、後工程のイオン注入が終わった後に除去することによって、後工程でキャップ材に注入された不純物がゲート電極へ拡散するのを未然に防ぐことができる。

【図面の簡単な説明】

【図１】従来の半導体装置におけるゲート電極のＰ型領域とＮ型領域を形成するための不純物注入領域を示す平面図である。

【図２】一実施例におけるゲート電極のＰ型領域とＮ型領域を形成するための不純物注入領域を示す平面図である。

【図３】一実施例における主要部の斜視断面図である。

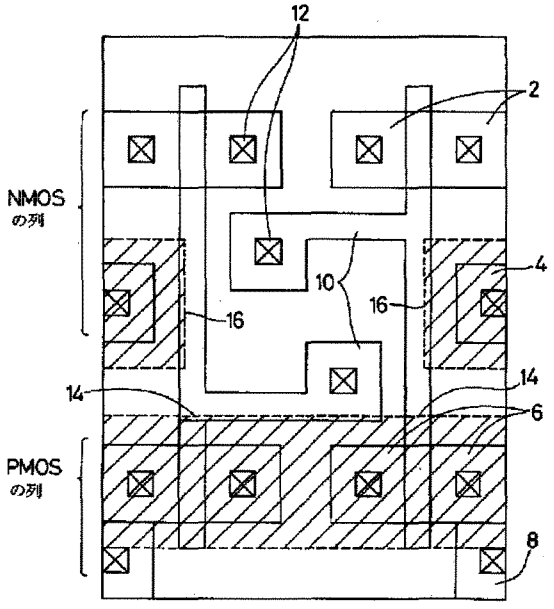
【図４】一実施例の製造方法の前半部を示す工程断面図である。

【図５】同実施例の製造方法の後半部を示す工程断面図である。

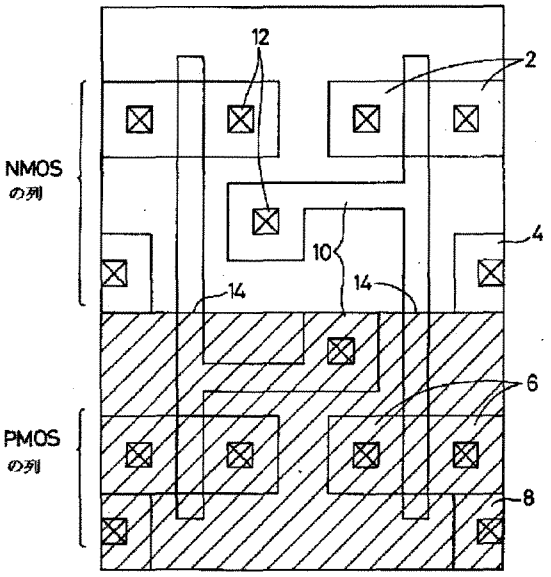
【符号の説明】

１０	ゲート電極
１４	ゲート電極のＰ型とＮ型の境界
３２	Ｎ型ポリシリコンゲート電極
４０	Ｐ型ポリシリコンゲート電極
４４	タングステンシリサイド膜
５０	ポリシリコン膜
５４	キャップ材のSiO_2膜

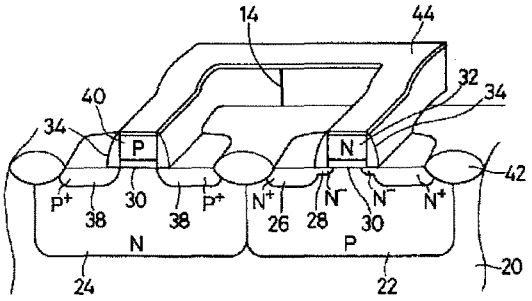
【図１】



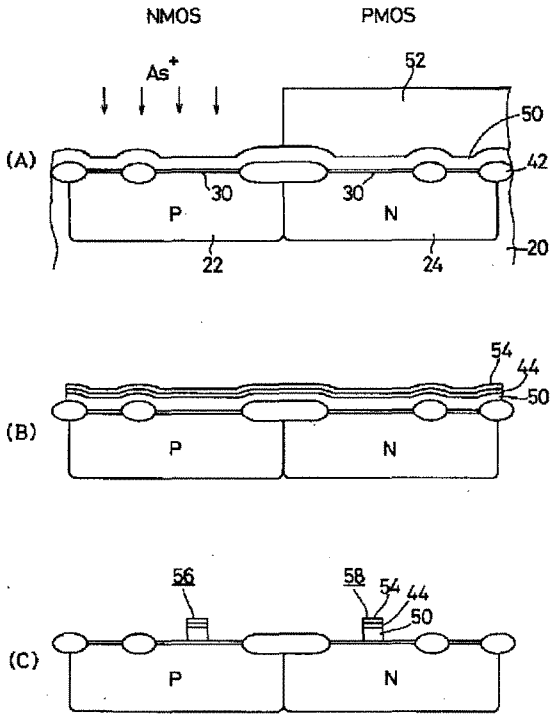
【図２】



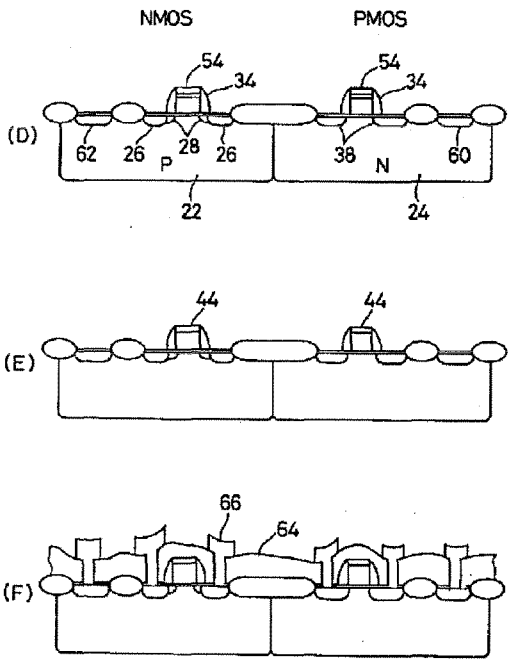
【図3】


14
44
40
32
34
34
P
N
42
P+
30
38
38
P+
N+
26
28
N-
30
N-
N+
N
P
24
22
20

【図4】


NMOS
PMOS
As+
52
(A)
50
42
30
30
P
N
22
24
20
54
44
50
(B)
P
N
56
58
54
44
50
(C)
P
N

【図5】


NMOS
PMOS
54
34
54
34
(D)
62
26
P
28
26
38
N
60
22
24
44
44
(E)
66
64
(F)

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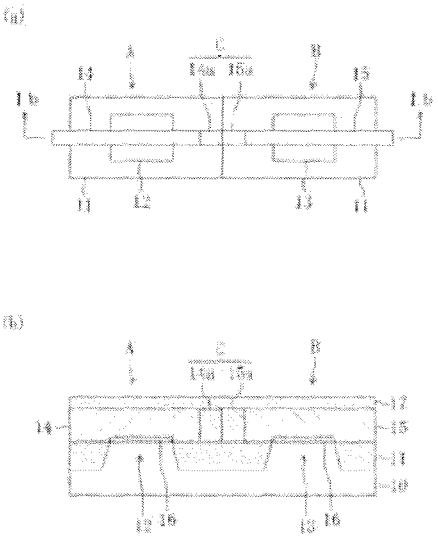
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(72)Inventor : SHIMOMURA MEGUMI
FUJINAGA KIYOO

(54) SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent increase of resistance of wiring by preventing disconnection of a metal silicide film in a PN junction boundary region without inhibiting miniaturization of an element and high integration.
SOLUTION: The semiconductor device includes a gate electrode formed on a semiconductor substrate 10 and formed of silicon having conductivity, and an a nickel silicide film 17 formed on the gate electrode. The gate electrode includes at least a first gate electrode 14 exhibiting N-type conductivity, a second gate electrode 15 exhibiting P-type conductivity, and a third gate electrode 14a formed between the first gate electrode 14 and the second gate electrode 15. The third gate electrode 14a is connected to the first gate electrode 14, and the concentration of impurities of the third gate electrode 14a is lower than the concentration of N-type impurities of the first gate electrode 14.



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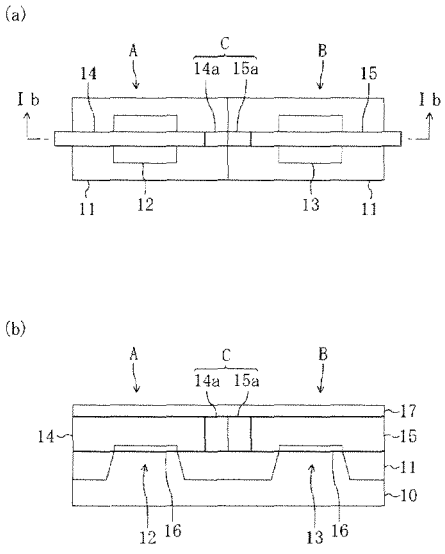
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最終頁に続く

(54)【発明の名称】半導体装置及びその製造方法

(57)【要約】
【課題】素子の微細化及び高集積化を妨げることなく、ＰＮ接合境界領域における金属シリサイド膜の断線を防止して、配線の高抵抗化を回避できるようにする。
【解決手段】半導体装置は、半導体基板１０の上に形成され、導電性を有するシリコンからなるゲート電極と、該ゲート電極の上に形成されたニッケルシリサイド膜１７とを有している。ゲート電極は、少なくとも、Ｎ型の導電性を示す第１のゲート電極１４と、Ｐ型の導電性を示す第２のゲート電極１５と、第１のゲート電極１４及び第２のゲート電極１５の間に形成された第３のゲート電極１４ａとを有している。第３のゲート電極１４ａは第１のゲート電極１４と接続されると共に、第３のゲート電極１４ａの不純物の濃度は、第１のゲート電極１４のＮ型不純物の濃度よりも低い。
【選択図】　図１



【特許請求の範囲】
【請求項１】
半導体基板の上に形成され、導電性を有するシリコンからなる配線と、
前記配線の上に形成された金属シリサイド膜とを備え、
前記配線は、Ｎ型の導電性を示す第１領域と、Ｐ型の導電性を示す第２領域と、前記第１領域と前記第２領域との間に形成された第３領域とを有し、
前記第３領域は前記第１領域及び前記第２領域とに接続されると共に、前記第３領域の不純物の濃度は、前記第１領域のＮ型不純物の濃度及び前記第２領域のＰ型不純物の濃度よりも低いことを特徴とする半導体装置。
【請求項２】
前記第１領域は、Ｎチャネル型トランジスタのゲート電極であり、
前記第２領域は、Ｐチャネル型トランジスタのゲート電極であることを特徴とする請求項１に記載の半導体装置。
【請求項３】
前記第３領域は、前記第１領域と接続され且つＮ型の導電性を示す第４領域と、前記第２領域と接続され且つＰ型の導電性を示す第５領域とからなることを特徴とする請求項１又は２に記載の半導体装置。
【請求項４】
前記第３領域における前記第１領域と前記第２領域とを接続する方向の長さは、マスク合わせ工程における重ね合わせ寸法以上であることを特徴とする請求項１～３のうちのいずれか１項に記載の半導体装置。
【請求項５】
前記金属シリサイド膜は、ニッケルシリサイド、チタンシリサイド又はコバルトシリサイドからなることを特徴とする請求項１～４のうちのいずれか１項に記載の半導体装置。
【請求項６】
半導体基板の上にシリコンからなる配線形成膜を形成する工程（ａ）と、
前記配線形成膜の第１領域を開口する第１マスク膜を用いて、前記配線形成膜の前記第１領域に第１導電型の不純物を導入する工程（ｂ）と、
前記配線形成膜における前記第１領域と隣接する第２領域を開口する第２マスク膜を用いて、前記配線形成膜の前記第２領域に第２導電型の不純物を導入する工程（ｃ）と、
前記配線形成膜の前記第２領域と、前記配線形成膜の前記第１領域における前記第２領域との境界部と接する一部の領域である第３領域を覆うと共に、前記第１領域の残部を開口する第３マスク膜を用いて、前記配線形成膜における前記第１領域の残部に第１導電型の不純物を導入する工程（ｄ）と、
前記配線形成膜に対して熱処理を行うことにより、前記第１領域、第２領域及び第３領域に導入された各不純物を活性化する工程（ｅ）と、
前記配線形成膜の上に金属シリサイド膜を形成する工程（ｆ）とを備えていることを特徴とする半導体装置の製造方法。
【請求項７】
前記第１領域は、Ｎチャネル型トランジスタのゲート電極であり、
前記第２領域は、Ｐチャネル型トランジスタのゲート電極であることを特徴とする請求項６に記載の半導体装置の製造方法。
【請求項８】
前記第３領域における前記第２領域との境界部から前記第１領域側への長さは、マスク合わせ工程における重ね合わせ寸法以上であることを特徴とする請求項６又は７に記載の半導体装置の製造方法。
【請求項９】
前記工程（ｄ）と前記工程（ｅ）との間に、
前記配線形成膜の前記第１領域と、前記配線形成膜の前記第２領域における前記第１領域との境界部と接する一部の領域である第４領域を覆うと共に、前記第２領域の残部を開

口する第４マスク膜を用いて、前記配線形成膜における前記第２領域の残部に第２導電型の不純物を導入する工程（ｇ）をさらに備え、

前記工程（ｅ）において、前記配線形成膜の前記第４領域に導入された不純物をも活性化することを特徴とする請求項６又は７に記載の半導体装置の製造方法。

【請求項１０】

前記第３領域における前記第２領域との境界部から前記第１領域側への長さ、及び前記第４領域における前記第１領域との境界部から前記第２領域側への長さは、いずれもマスク合わせ工程における重ね合わせ寸法以上であることを特徴とする請求項９に記載の半導体装置の製造方法。

【請求項１１】

前記金属シリサイド膜は、ニッケルシリサイド、チタンシリサイド又はコバルトシリサイドであることを特徴とする請求項６～１０のうちのいずれか１項に記載の半導体装置の製造方法。

【発明の詳細な説明】

【技術分野】

【０００１】

本発明は、半導体装置及びその製造方法に関し、特に上部に金属シリサイド膜を備えた配線を有する半導体装置及びその製造方法に関する。

【背景技術】

【０００２】

近年、半導体集積回路装置の高集積化、高機能化及び高速化に伴って、ＣＭＯＳ（Complementary Metal Oxide Semiconductor）プロセスにおいて、Ｎチャネル型ＭＯＳトランジスタのゲート電極にはＮ型不純物を注入したシリコン電極を用い、Ｐチャネル型ＭＯＳトランジスタのゲート電極にはＰ型不純物を注入したシリコン電極を用いるデュアルゲート構造が採用されている。

【０００３】

このようなデュアルゲート構造を有する半導体装置において、シリコンからなるゲート電極におけるＮチャネル領域とＰチャネル領域とが互いに接続する境界領域では、Ｎチャネル領域とＰチャネル領域との不純物濃度の影響により抵抗値が上昇することにより、回路の動作速度が遅延するなどの集積回路の性能が阻害されるという問題がある。

【０００４】

この問題を解決すべく、従来は、ゲート電極の上部を金属シリサイド化することにより、ゲート電極の抵抗を小さくする方法が提案され、多くの改良がなされている（例えば、特許文献１を参照。）。

【０００５】

（第１の従来例）

図４（ａ）～図４（ｆ）は第１の従来例に係るゲート電極の上部を金属シリサイド化してゲート電極の抵抗を下げる半導体装置の製造方法の工程順の断面構成を示している。ここでは、ゲート幅方向の断面であって、金属シリサイド膜が形成されたデュアルゲート構造を有する半導体装置の製造方法を示している。

【０００６】

まず、図４（ａ）に示すように、シリコンからなる半導体基板１００の上部に形成した活性領域を取り囲み、且つＮチャネル型ＭＯＳトランジスタ領域ＡとＰチャネル型ＭＯＳトランジスタ領域Ｂとを分離する素子分離領域１０１を形成する。その後、半導体基板１００の上にゲート絶縁膜１０２と多結晶シリコン膜１０３とを順次形成する。

【０００７】

次に、図４（ｂ）に示すように、多結晶シリコン膜１０３の上に、Ｐチャネル型ＭＯＳトランジスタ領域Ｂを覆い、且つＮチャネル型ＭＯＳトランジスタ領域Ａを開口する開口パターンを有する第１のレジスト膜１０４を形成し、形成した第１のレジスト膜１０４をマスクとして、多結晶シリコン膜１０３のＮチャネル型ＭＯＳトランジスタ領域ＡにＮ型

不純物であるリン（P^+）イオンをイオン注入する。その後、第１のレジスト膜１０４を除去する。

【０００８】

次に、図４（ｃ）に示すように、多結晶シリコン膜１０３の上に、Ｎチャネル型ＭＯＳトランジスタ領域Ａを覆い、且つＰチャネル型ＭＯＳトランジスタ領域Ｂを開口する開口パターンを有する第２のレジスト膜１０５を形成し、形成した第２のレジスト膜１０５をマスクとして、多結晶シリコン膜１０３のＰチャネル型ＭＯＳトランジスタ領域ＢにＰ型不純物であるボロン（B^+）イオンをイオン注入する。その後、第２のレジスト膜１０５を除去する。

【０００９】

次に、図４（ｄ）に示すように、半導体基板１００に対して熱処理を行って、多結晶シリコン膜１０３に注入された各不純物イオンを活性化することにより、多結晶シリコン膜１０３からＮ型多結晶シリコン領域１０３ａとＰ型多結晶シリコン領域１０３ｂとを形成する。このとき、多結晶シリコン膜１０３におけるリンイオンとボロンイオンとが拡散して、多結晶シリコン膜１０３におけるＮチャネル型ＭＯＳトランジスタ領域ＡとＰチャネル型ＭＯＳトランジスタ領域Ｂとの境界部にＰＮ接合境界領域Ｃが形成される。

【００１０】

次に、図４（ｅ）に示すように、多結晶シリコン膜１０３の上に、Ｎ型多結晶シリコン領域１０３ａとＰ型多結晶シリコン領域１０３ｂとに跨るように金属膜１１２を堆積する。

【００１１】

次に、図４（ｆ）に示すように、公知のサリサイド形成技術により、Ｎ型多結晶シリコン領域１０３ａとＰ型多結晶シリコン領域１０３ｂとに跨る金属シリサイド膜１１２Ａを形成する。

【００１２】

しかしながら、前記の第１の従来例に係る製造方法では、金属シリサイド膜１１２Ａの配線幅が小さくなると、金属シリサイド膜１１２が凝集してしまい、金属シリサイド膜１１２に断線が生じやすくなる。特にデュアルゲート構造では、多結晶シリコン膜１０３のＰＮ接合境界領域Ｃをシリサイド化した金属シリサイド膜１１２Ａに、不純物濃度が影響してシリサイド化反応が遅くなり、金属シリサイド膜１１２Ａの膜厚が薄くなる結果、抵抗上昇や断線が生じやすい。

【００１３】

このように、ＰＮ接合境界領域Ｃにおいて金属シリサイド膜１１２Ａに断線が発生すると、多結晶シリコン膜１０３のＰＮ接合に逆バイアスが印加された場合に抵抗上昇が生じ、ゲート電極が極めて高抵抗になるという問題がある。

【００１４】

そこで、このような金属シリサイド膜の断線によるゲート電極の高抵抗化を回避するために、図５に示す他の構成が提案されている（例えば、特許文献２を参照。）。

【００１５】

（第２の従来例）

図５は第２の従来例に係るＮチャネル型ＭＯＳトランジスタ領域とＰチャネル型トランジスタ領域とを有するデュアルゲートトランジスタの平面構成を示している。

【００１６】

図５に示すように、Ｐチャネル型トランジスタ領域１の上に配されたＰ型ゲート電極４と、Ｎチャネル型ＭＯＳトランジスタ領域３の上に配されたＮ型ゲート電極５との境界部に、不純物を注入しないノンドープ領域８を設けることにより、シリサイド形成時の不純物濃度による影響を回避して金属シリサイド膜の薄膜化を防止している。

【特許文献１】特開昭５９－２１３１５６号公報

【特許文献２】特開平１０－０１２７４５号公報

【発明の開示】

【発明が解決しようとする課題】
【００１７】
しかしながら、前記の第２の従来例に係る製造方法は、ＰＮ接合境界領域にノンドープ領域を設けてはいるものの、熱処理時のノンドープ領域への不純物拡散が大きいため、熱処理後には実質的にノンドープ領域が非常に小さくなっているか又は消失するおそれがある。
【００１８】
このため、熱処理後においてもノンドープ領域を確保するには、ノンドープ領域を大きく設定する必要があり、素子の微細化及び高集積化を妨げるという問題がある。
【００１９】
本発明は、前記従来の問題に鑑み、素子の微細化及び高集積化を妨げることなく、ＰＮ接合境界領域における金属シリサイド膜の断線を防止して、配線の高抵抗化を回避できるようにすることを目的とする。
【課題を解決するための手段】
【００２０】
前記の目的を達成するため、本発明は、半導体装置及びその製造方法を、デュアルゲート構造におけるＮチャネル型トランジスタ領域とＰチャネル型ＭＯＳトランジスタ領域との境界部に、不純物が低濃度にドープされた領域を設ける構成とする。
【００２１】
具体的に、本発明に係る半導体装置は、半導体基板の上に形成され、導電性を有するシリコンからなる配線と、配線の上に形成された金属シリサイド膜とを備え、配線は、Ｎ型の導電性を示す第１領域と、Ｐ型の導電性を示す第２領域と、第１領域と第２領域との間に形成された第３領域とを有し、第３領域は第１領域及び第２領域とに接続されると共に、第３領域の不純物の濃度は、第１領域のＮ型不純物の濃度及び第２領域のＰ型不純物の濃度よりも低いことを特徴とする。
【００２２】
本発明の半導体装置によると、第１領域と第２領域との接続部、すなわちＰＮ接合境界領域である第３領域の不純物の濃度が、第１領域のＮ型不純物の濃度及び第２領域のＰ型不純物の濃度よりも低いため、金属シリサイド膜の薄膜化を抑制することができる。このため、金属シリサイド膜の断線を防止することができるので、配線の高抵抗化を回避することができる。
【００２３】
本発明の半導体装置において、第１領域は、Ｎチャネル型トランジスタのゲート電極であり、第２領域は、Ｐチャネル型トランジスタのゲート電極であることが好ましい。
【００２４】
本発明の半導体装置において、第３領域は、第１領域と接続され且つＮ型の導電性を示す第４領域と、第２領域と接続され且つＰ型の導電性を示す第５領域とからなることが好ましい。
【００２５】
本発明の半導体装置において、第３領域における第１領域と第２領域とを接続する方向の長さは、マスク合わせ工程における重ね合わせ寸法以上であることが好ましい。
【００２６】
本発明の半導体装置において、金属シリサイド膜は、ニッケルシリサイド、チタンシリサイド又はコバルトシリサイドからなることが好ましい。
【００２７】
本発明に係る半導体装置の製造方法は、半導体基板の上にシリコンからなる配線形成膜を形成する工程（ａ）と、配線形成膜の第１領域を開口する第１マスク膜を用いて、配線形成膜の第１領域に第１導電型の不純物を導入する工程（ｂ）と、配線形成膜における第１領域と隣接する第２領域を開口する第２マスク膜を用いて、配線形成膜の第２領域に第２導電型の不純物を導入する工程（ｃ）と、配線形成膜の第２領域と、配線形成膜の第１

領域における第２領域との境界部と接する一部の領域である第３領域を覆うと共に、第１領域の残部を開口する第３マスク膜を用いて、配線形成膜における第１領域の残部に第１導電型の不純物を導入する工程（ｄ）と、配線形成膜に対して熱処理を行うことにより、第１領域、第２領域及び第３領域に導入された各不純物を活性化する工程（ｅ）と、配線形成膜の上に金属シリサイド膜を形成する工程（ｆ）とを備えていることを特徴とする。

【００２８】

本発明の半導体装置の製造方法によると、シリコンからなる配線形成膜における第１領域の一部の領域である第３の領域の不純物濃度は、工程（ｄ）においてマスクされているため、第１の領域の不純物濃度よりも低くなる。このため、金属シリサイド膜の薄膜化を抑制することができるので、金属シリサイド膜の断線を防止することができるようになり、その結果、配線の高抵抗化を回避することができる。

【００２９】

本発明の半導体装置の製造方法において、第１領域は、Ｎチャネル型トランジスタのゲート電極であり、第２領域は、Ｐチャネル型トランジスタのゲート電極であることが好ましい。

【００３０】

本発明の半導体装置の製造方法において、第３領域における第２領域との境界部から第１領域側への長さは、マスク合わせ工程における重ね合わせ寸法以上であることが好ましい。

【００３１】

本発明の半導体装置の製造方法は、工程（ｄ）と工程（ｅ）との間に、配線形成膜の第１領域と、配線形成膜の第２領域における第１領域との境界部と接する一部の領域である第４領域を覆うと共に、第２領域の残部を開口する第４マスク膜を用いて、配線形成膜における第２領域の残部に第２導電型の不純物を導入する工程（ｇ）をさらに備え、工程（ｅ）において、配線形成膜の第４領域に導入された不純物をも活性化することが好ましい。

【００３２】

本発明の半導体装置の製造方法において、第３領域における第２領域との境界部から第１領域側への長さ、及び第４領域における第１領域との境界部から第２領域側への長さは、いずれもマスク合わせ工程における重ね合わせ寸法以上であることが好ましい。

【００３３】

本発明の半導体装置の製造方法において、金属シリサイド膜は、ニッケルシリサイド、チタンシリサイド又はコバルトシリサイドであることが好ましい。

【発明の効果】

【００３４】

本発明に係る半導体装置及びその製造方法によると、金属シリサイド膜の薄膜化を抑制することができ、金属シリサイド膜の断線を防止することができるので、配線の高抵抗化を回避することができる。

【発明を実施するための最良の形態】

【００３５】

（一実施形態）

本発明の一実施形態について図面を参照しながら説明する。

【００３６】

図１（ａ）は本発明の一実施形態に係る半導体装置の平面構成を示し、図１（ｂ）は図１（ａ）のＩｂ－Ｉｂ線における断面構成を示している。

【００３７】

図１（ａ）に示すように、本実施形態に係る半導体装置は、ＮチャネルＭＯＳトランジスタ領域ＡとＰチャネル型トランジスタ領域Ｂとを有するデュアルゲートトランジスタである。なお、図１（ａ）においては、説明のため、ゲート電極の上部に設けられた金属シリサイド膜を省略している。

【００３８】
図１（ａ）及び図１（ｂ）に示すように、Ｎチャネル型ＭＯＳトランジスタ領域Ａには、シリコンからなる半導体基板１０の上部に形成された素子分離領域１１によってその周囲を囲まれ、Ｎ型不純物拡散層からなるソースドレイン領域として機能するＮ型活性領域１２と、該Ｎ型活性領域１２及び素子分離領域１１の上に跨って形成され、Ｎ型不純物を含む多結晶シリコンからなる第１のゲート電極１４とが配置されている。
【００３９】
同様に、Ｐチャネル型ＭＯＳトランジスタ領域Ｂは、素子分離領域１１によってその周囲を囲まれ、Ｐ型不純物拡散層からなるソースドレイン領域として機能するＰ型活性領域１３と、該Ｐ型活性領域１３及び素子分離領域１１の上に跨って形成され、Ｐ型不純物を含む多結晶シリコンからなる第２のゲート電極１５とが配置されている。
【００４０】
半導体基板１０の主面上におけるＮ型活性領域１２と第１のゲート電極１４との間及びＰ型活性領域１３と第２のゲート電極１５との間には、例えば酸化シリコンからなるゲート絶縁膜１６がそれぞれ形成されている。
【００４１】
Ｎチャネル型ＭＯＳトランジスタ領域ＡとＰチャネル型ＭＯＳトランジスタ領域Ｂとに跨るデュアルゲートにおける第１のゲート電極１４と第２のゲート電極１５との間には、Ｎ型不純物を含む多結晶シリコンからなり、第１のゲート電極１４と隣接する第３のゲート電極１４ａと、Ｐ型不純物を含む多結晶シリコンからなり、第２のゲート電極１５と隣接する第４のゲート電極１５ａとが形成されており、第３のゲート電極１４ａと第４のゲート電極１５ａとがＰＮ接合境界領域Ｃを形成するように互いに接している。
【００４２】
本実施形態の特徴として、第３のゲート電極１４ａのＮ型不純物の濃度は、第１のゲート電極１４のＮ型不純物の濃度よりも低濃度であり、且つ、第４のゲート電極１５ａのＰ型不純物の濃度は第２のゲート電極１５のＰ型不純物の濃度よりも低濃度である。
【００４３】
また、図１（ｂ）に示すように、第１のゲート電極１４、第２のゲート１５、第３のゲート電極１４ａ及び第４のゲート電極１５ａの上部には、例えばニッケルシリサイド膜１７が形成されている。
【００４４】
以下、前記のように構成された本実施形態に係る半導体装置の製造方法について図面を参照しながら説明する。
【００４５】
図２（ａ）～図２（ｄ）及び図３（ａ）～図３（ｄ）は本実施形態に係る半導体装置の製造方法の工程順の断面構成を示している。
【００４６】
まず、図２（ａ）に示すように、シリコンからなる半導体基板１０の上部に、Ｎ型活性領域１２及びＰ型活性領域１３をそれぞれ囲むと共に、ＮチャネルトランジスタＡとＰチャネル型トランジスタ領域Ｂとを分離するシャロウトレンチアイソレーション（ＳＴＩ）からなる素子分離領域１１を形成する。その後、例えば熱酸化法により、半導体基板１０の主面上に厚さが２ｎｍの酸化シリコンからなるゲート絶縁膜１６を形成する。続いて、化学的気相堆積（ＣＶＤ）法により、半導体基板１０の上にゲート絶縁膜１６及び素子分離領域１１を含む全面にわたって、厚さが２００ｎｍの多結晶シリコン膜２０を形成する。
【００４７】
次に、図２（ｂ）に示すように、リソグラフィ法により、多結晶シリコン膜２０の上に、Ｎチャネル型トランジスタ領域Ａに開口部を持つ第１のレジスト膜２１を形成し、形成した第１のレジスト膜２１をマスクとして、多結晶シリコン膜２０のＮチャネル型トランジスタ領域Ａに、Ｎ型不純物であるリン（P^+）イオンを注入エネルギーが２０ｋｅＶで

、ドーズ量が５×１０^{15}／ｃｍ^{2}の注入条件でイオン注入する。その後、第１のレジスト膜２１を除去する。

【００４８】

次に、図２（ｃ）に示すように、リソグラフィ法により、多結晶シリコン膜２０の上に、Ｐチャネル型トランジスタ領域Ｂに開口部を持つ第２のレジスト膜２２を形成し、形成した第２のレジスト膜２２をマスクとして、多結晶シリコン膜２０のＰチャネル型トランジスタ領域Ｂに、Ｐ型不純物であるボロン（Ｂ$^{+}$）イオンを注入エネルギーが２ｋｅＶで、ドーズ量が２×１０^{15}／ｃｍ^{2}の注入条件でイオン注入する。続いて、第２のレジスト膜２２を除去した後、リソグラフィ法及びドライエッチング法により、多結晶シリコン膜２０を、図１（ａ）に示すようなゲート電極形状にパターニングする。

【００４９】

次に、図２（ｄ）に示すように、多結晶シリコン膜２０の上に、第１のレジスト膜２１よりもＮチャネル型トランジスタ領域Ａの上の開口幅を、該Ｎチャネル型トランジスタ領域Ａ側に１０ｎｍ程度小さくすることにより、Ｐチャネル型トランジスタ領域Ｂ及び該Ｐチャネル型トランジスタ領域ＢとＮチャネル型トランジスタ領域Ａとの境界部であるＰＮ接合境界領域Ｃを覆う第３のレジスト膜２３を形成する。続いて、形成した第３のレジスト膜２３をマスクとして、多結晶シリコン膜２０のＮチャネル型トランジスタ領域Ａに、リン（Ｐ$^{+}$）イオンを注入エネルギーが２０ｋｅＶで、ドーズ量が１×１０^{15}／ｃｍ^{2}の注入条件でイオン注入する。その後、第３のレジスト膜２３を除去する。

【００５０】

次に、図３（ａ）に示すように、多結晶シリコン膜２０の上に、第２のレジスト膜２２よりもＰチャネル型トランジスタ領域Ｂの上の開口幅を、該Ｐチャネル型トランジスタ領域Ｂ側に１０ｎｍ程度小さくすることにより、Ｎチャネル型トランジスタ領域Ａ及びＰＮ接合境界領域Ｃを覆う第４のレジスト膜２４を形成する。続いて、形成した第４のレジスト膜２４をマスクとして、多結晶シリコン膜２０のＰチャネル型トランジスタ領域Ｂに、ボロン（Ｂ$^{+}$）イオンを注入エネルギーが２ｋｅＶで、ドーズ量が１×１０^{15}／ｃｍ^{2}の注入条件でイオン注入する。その後、第４のレジスト膜２４を除去する。

【００５１】

次に、図３（ｂ）に示すように、半導体基板１０に熱処理を行って、多結晶シリコン膜２０に注入された各不純物を活性化する。この熱処理によって、多結晶シリコン膜２０に注入されたリンイオンとボロンイオンとが拡散して、多結晶シリコン膜２０のＮチャネル型トランジスタ領域Ａには、Ｎ型多結晶シリコン領域からなる第１のゲート電極１４が形成され、多結晶シリコン膜２０のＰチャネル型トランジスタ領域Ｂには、Ｐ型多結晶シリコン領域からなる第２のゲート電極１５が形成される。また、多結晶シリコン膜２０のＰＮ接合境界領域ＣにおけるＮチャネル型トランジスタ領域Ａ側には、第１のゲート電極１４よりもＮ型不純物の濃度が低い第３のゲート電極１４ａが形成され、ＰＮ接合境界領域ＣにおけるＰチャネル型トランジスタ領域Ｂ側には、第２のゲート電極１５よりもＰ型不純物の濃度が低い第４のゲート電極１５ａが形成される。

【００５２】

次に、図３（ｃ）に示すように、真空蒸着法又はスパッタ法により、各ゲート電極１４、１４ａ、１５及び１５ａの上の全面に、金属膜として、例えば厚さが１０ｎｍのニッケル（Ｎｉ）膜１７Ａを堆積する。このとき、ニッケル膜１７Ａの上に窒化チタン（ＴｉＮ）膜を堆積してもよい。

【００５３】

次に、図３（ｄ）に示すように、半導体基板１０に対して、温度が４３０℃で、３０秒間の第１の短時間熱処理（急速熱処理）を施して、各ゲート電極１４、１５等を構成するシリコンとその上に堆積したニッケルとを反応させることにより、各ゲート電極１４、１４ａ、１５及び１５ａの上部にニッケルシリサイド（ＮｉＳｉ）膜１７を形成する。続いて、硫酸（H_2SO_4）と過酸化水素水（H_2O_2）との混合液等の溶液を用いて、未反応のニッケル膜１７Ａを選択的に除去する。その後、半導体基板１０に温度が８５０℃で

、６０秒間の第２の短時間熱処理を行う。

【００５４】

以上により、本実施形態に係るデュアルゲート構造を有する半導体装置を得ることができる。

【００５５】

なお、本実施形態においては、Ｎチャネル型トランジスタ領域ＡとＰチャネル型トランジスタ領域ＢとのＰＮ接合境界領域Ｃにおいて、Ｎチャネル型トランジスタ領域Ａの第１のゲート電極１４と接する第３のゲート電極１４ａのＮ型不純物の濃度を第１のゲート電極１４の濃度よりも低くすると共に、Ｐチャネル型トランジスタ領域Ｂの第２のゲート電極１５と接する第４のゲート電極１５ａのＰ型不純物の濃度を第２のゲート電極１５の濃度よりも低くしている。しかしながら、本発明は、第３のゲート電極１４ａの不純物濃度のみを第１のゲート電極１４の不純物濃度よりも低くしてもよく、逆に、第４のゲート電極１４ａの不純物濃度のみを第２のゲート電極１５の不純物濃度よりも低くしてもよい。

【００５６】

また、本実施形態においては、Ｎ型不純物であるリンイオンを注入した後、Ｐ型不純物であるボロンイオンを注入しているが、これとは逆に、ボロンイオンを注入した後にリンイオンを注入してもよい。また、リンイオンとボロンイオンとを交互に２回ずつ注入するのではなく、リンイオンとボロンイオンのうち、いずれか一方のイオンを連続して注入した後に、他方のイオンを連続して注入してもよい。

【００５７】

また、ＰＮ接合境界領域Ｃを覆う第３のレジスト膜２３及び第４のレジスト膜２４におけるＰＮ接合境界領域Ｃを覆う部分の寸法は、１０ｎｍとしたが、マスク合わせ工程における重ね合わせ精度以上であることが望ましい。

【００５８】

なお、上記の実施形態において、ＰＮ接合境界領域Ｃにおける不純物濃度が、リンイオンなら$6\times10^{15}/cm^2$以上、ボロンイオンなら$3\times10^{15}/cm^2$以上であると、シリサイド化の反応速度が遅くなる。特に、高融点金属にニッケルを使用した場合に反応が遅くなる。

【００５９】

以上説明したように、本実施形態に係る半導体装置は、図３（ｂ）に示したように、Ｎチャネル型トランジスタ領域ＡとＰチャネル型トランジスタ領域ＢとのＰＮ接合境界領域Ｃの不純物濃度は、他の領域よりも低く形成される。

【００６０】

より具体的には、ＰＮ接合境界領域Ｃにおける、第３のゲート電極１４ａのＮ型不純物の濃度が第１のゲート電極１４のＮ型不純物の濃度よりも低く、且つ第４のゲート電極１５ａのＰ型不純物の濃度が第２のゲート電極１５のＰ型不純物の濃度よりも低い構成であるため、ＰＮ接合境界領域Ｃの上に形成されるニッケルシリサイド膜１７の膜厚が薄くなることを防止できるので、ＰＮ接合境界領域Ｃにおけるニッケルシリサイド膜１７の断線を防止することができる。

【００６１】

従って、第２の従来例のようなＰＮ接合境界領域に不純物を全く注入しないノンドープ領域を形成することにより、ニッケルシリサイド膜のＰＮ接合境界領域での断線を防止する手法と比べて、トランジスタの占有面積を増大させることなく、集積回路不良を防止することができる。

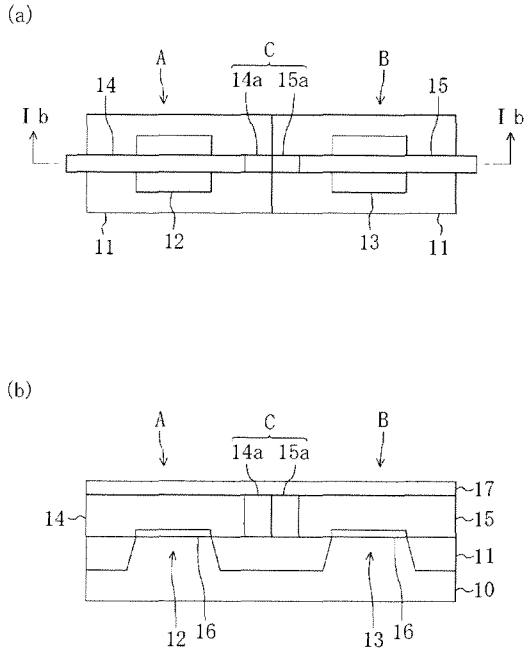
【００６２】

なお、本実施形態においては、半導体装置としてＮチャネル型ＭＯＳトランジスタ領域ＡとＰチャネル型トランジスタ領域Ｂとを有するデュアルゲートトランジスタを説明したが、この構成に限定されず、例えば、半導体基板上に形成され、Ｎ型シリコン膜とＰ型シリコン膜とが接続したシリコン膜からなる配線であっても、同様の効果を得ることができる。

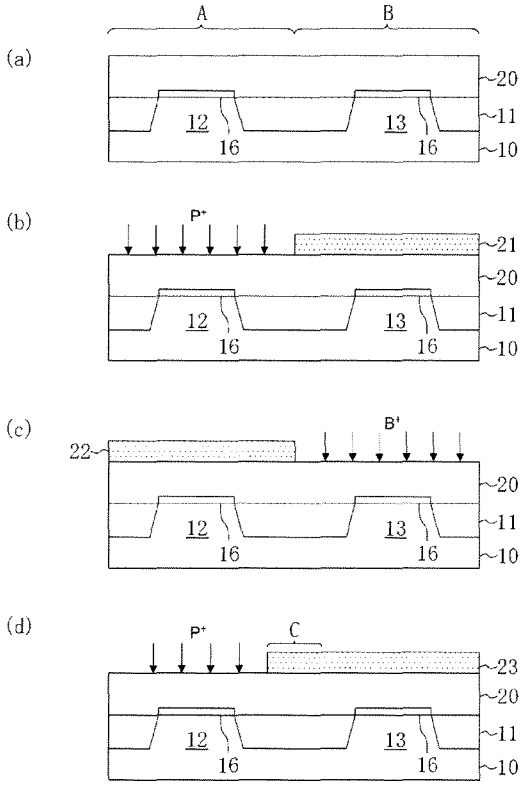
【００６３】
また、ＰＮ接合境界領域Ｃにおける金属シリサイド膜の断線は、配線長には依存しないが、配線幅は狭くなる程発生しやすい。具体的には、配線幅が６０ｎｍ以下では発生しやすく、従って、配線幅が６０ｎｍ以下の場合により大きい効果を得ることができる。
【００６４】
また、本実施形態においては、金属シリサイド膜としてニッケルシリサイドを用いたが、チタン（Ｔｉ）又はコバルト（Ｃｏ）等のシリサイドを形成可能な高融点金属を用いても構わない。
【００６５】
また、前述したように、ＰＮ接合境界領域Ｃの長さ方向（ゲート幅方向）の寸法、すなわち第３のゲート電極１４ａ及び第４のゲート電極１５ａのゲート幅方向の寸法は、マスク合わせ工程における重ね合わせ精度以上であることが望ましい。また、通常、第３のゲート電極１４ａ及び第４のゲート電極１５ａのドーズ量は2×10^{15}／cm^2程度であることが望ましい。
【産業上の利用可能性】
【００６６】
本発明に係る半導体装置及びその製造方法は、素子の微細化及び高集積化を妨げることなく、ＰＮ接合境界領域における金属シリサイド膜の断線を防止し、配線の高抵抗化を回避でき、特に金属シリサイド膜を備えたデュアルゲート構造の半導体装置及びその製造方法等に有用である。
【図面の簡単な説明】
【００６７】
【図１】（ａ）及び（ｂ）は本発明の一実施形態に係る半導体装置を模式的に示し、（ａ）は平面図であり、（ｂ）は（ａ）のＩｂ－Ｉｂ線における断面図である。
【図２】（ａ）～（ｄ）は本発明の一実施形態に係る半導体装置の製造方法を模式的に示す工程順の断面図である。
【図３】（ａ）～（ｄ）は本発明の一実施形態に係る半導体装置の製造方法を模式的に示す工程順の断面図である。
【図４】（ａ）～（ｆ）は第１の従来例に係る半導体装置の製造方法を模式的に示す工程順の断面図である。
【図５】第２の従来例に係る半導体装置を示す平面図である。
【符号の説明】
【００６８】
Ａ　Ｎチャネル型ＭＯＳトランジスタ領域
Ｂ　Ｐチャネル型ＭＯＳトランジスタ領域
Ｃ　ＰＮ接合境界領域
１０　半導体基板
１１　素子分離領域
１２　Ｎ型活性領域
１３　Ｐ型活性領域
１４　第１のゲート電極
１５　第２のゲート電極
１４ａ　第３のゲート電極
１５ａ　第４のゲート電極
１６　ゲート絶縁膜
１７　ニッケルシリサイド膜
１７Ａ　ニッケル膜
２０　多結晶シリコン膜
２１　第１のレジスト膜
２２　第２のレジスト膜

２３　　第３のレジスト膜
２４　　第４のレジスト膜

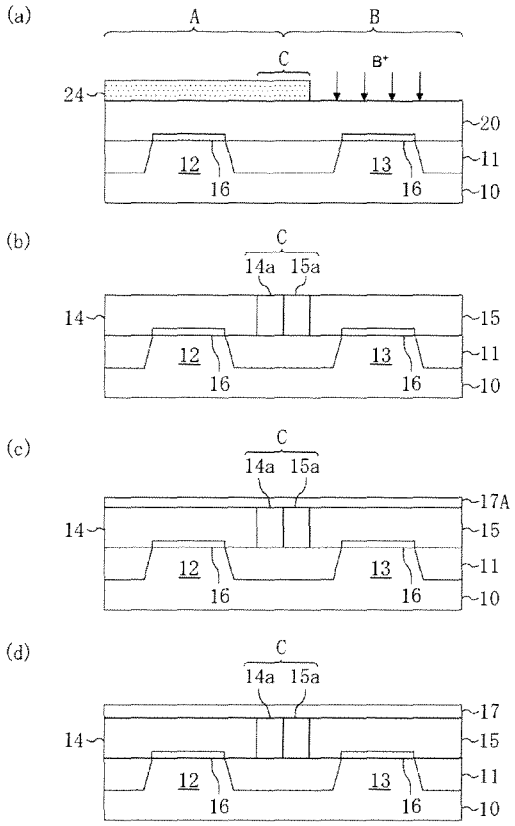
【図１】



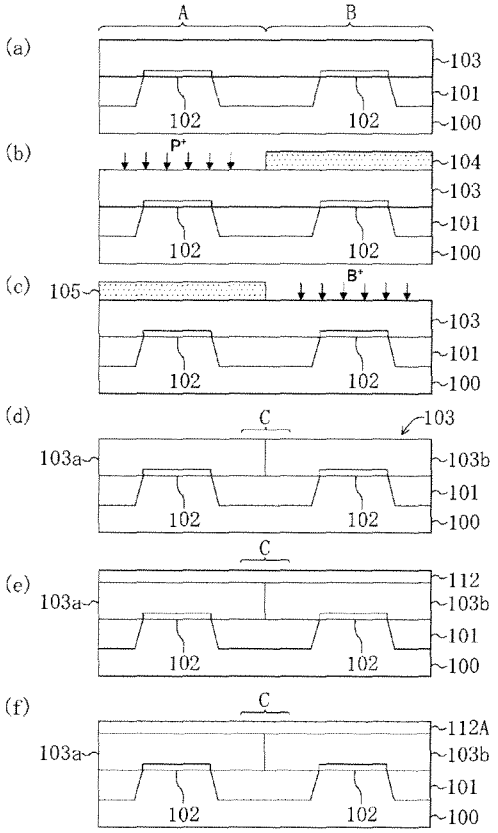
【図２】



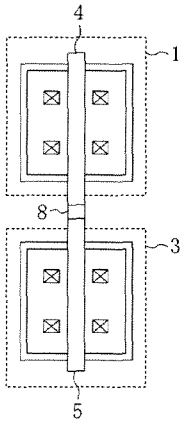
【図３】


(a)
A
B
C
B+
24
20
12
13
16
16
11
10
(b)
C
14a 15a
14
15
12
13
16
16
11
10
(c)
C
14a 15a
17A
14
15
12
13
16
16
11
10
(d)
C
14a 15a
17
14
15
12
13
16
16
11
10

【図４】


A
B
(a)
103
101
102
102
100
(b)
P+
104
103
101
102
102
100
(c)
105
B+
103
101
102
102
100
(d)
C
103
103a
103b
101
102
102
100
(e)
C
112
103a
103b
101
102
102
100
(f)
C
112A
103a
103b
101
102
102
100

【図５】


4
1
8
3
5

フロントページの続き

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DD55 DD56 DD78 DD84 FF14 GG10 HH20
5F033 HH04 HH25 HH27 LL04 MM07 PP06 QQ59 QQ65 QQ70 QQ73
VV06 XX00 XX08
5F048 AA07 AC03 BA01 BB06 BB07 BB08 BB12 BE03 BF04 BF05
BF06 BF19 BG13

SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation of PCT International Application PCT/JP2011/006167 filed on November 4, 2011, which claims priority to Japanese Patent Application No. 2011-068131 filed on March 25, 2011. The disclosures of these applications including the specifications, the drawings, and the claims are hereby incorporated by reference in their entirety.

BACKGROUND

The present disclosure relates to semiconductor devices and methods for fabricating semiconductor devices, and more particularly to a semiconductor device having a complementary metal insulator semiconductor (CMIS) dual-gate structure and a method for fabricating such a semiconductor device.

The integration degree of semiconductor integrated circuits have been increased by miniaturizing CMIS devices with dual-gate structures. A CMIS device with a dual-gate structure generally refers to a device including a polysilicon film doped with an n-type impurity as a gate electrode of an n-channel metal insulator semiconductor field effect transistor (hereinafter referred to as an NMISFET) and also including a polysilicon film doped with a p-type impurity as a gate electrode of a p-channel MISFET (hereinafter referred to as a PMISFET) (see, for example, Japanese Patent Publication No. H06-275788). In a CMIS device with a dual-gate structure, a metal silicide layer is formed on a polysilicon gate electrode in order to connect an n-type polysilicon gate electrode and a p-type polysilicon gate electrode. In this structure, in the boundary between an n-type region and a p-type region in each of the polysilicon gate electrode, impurities in these regions are diffused from one region to the other through the metal silicide layer or the polysilicon film, resulting in a change in

work function of the gate electrode, and thus, a variation in threshold voltage of each of the FETs.

As a conventional method for forming an n-type region and a p-type region in a polysilicon film for gate electrodes, ions of impurities are implanted into the polysilicon film for gate electrodes using a mask designed such that the boundary between the n-type region and the p-type region is located on an isolation between well regions (see, for example, Japanese Patent Publication No. H08-17934).

A conventional semiconductor device in which an n-type region and a p-type region are formed by implanting ions into gate electrodes of a transistor for a logic circuit and a transistor for a static random access memory (SRAM) circuit will be described with reference to the drawings.

FIG. 15A is a plan view illustrating a logic area of a conventional semiconductor device. FIG. 15B is a cross-sectional view taken along the line B-B (along the gate width) in FIG. 15A. FIG. 15C is a plan view illustrating an SRAM area of the conventional semiconductor device. FIG. 15D is a cross-sectional view taken along the line D-D (along the gate width) in FIG. 15C. In FIGS. 15A-15D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. 15B and 15D.

As illustrated in FIGS. 15A-15D, each of the logic area and the SRAM area of the conventional semiconductor device has an NMIS region and a PMIS region. In the NMIS region in the logic area, a p-well region 102a is provided on a semiconductor substrate 100 and an active region 100a is surrounded by an isolation region 101. In the PMIS region in the logic area, an n-well region 102b is provided on the semiconductor substrate 100 and an active region 100b is surrounded by the isolation region 101. In the NMIS region in the SRAM area, a p-well region 102c is provided on the semiconductor substrate 100, and an

active region 100c is surrounded by the isolation region 101. In the PMIS region in the SRAM area, an n-well region 102d is provided on the semiconductor substrate 100, and an active region 100d is surrounded by the isolation region 101.

On the active region 100a, a gate electrode 111a including an n-type polysilicon film 104a is formed with a gate insulating film 103 interposed therebetween. On the active region 100b, a gate electrode 111b including a p-type polysilicon film 104b is formed with the gate insulating film 103 interposed therebetween. The gate electrode 111a and the gate electrode 111b are connected to each other at a PN boundary 113L between the active region 100a and the active region 100b on the isolation region 101, thereby forming a dual-gate electrode 112L. N-type source/drain regions 105a are defined at both sides of the gate electrode 111a in the active region 100a. P-type source/drain regions 105b are defined at both sides of the gate electrode 111b in the active region 100b. A contact 108 is formed to be connected to the dual-gate electrode 112L, the n-type source/drain regions 105a, and the p-type source/drain regions 105b.

On the active region 100c, a gate electrode 111c including an n-type polysilicon film 104c is formed with the gate insulating film 103 interposed therebetween. On the active region 100d, a gate electrode 111d including a p-type polysilicon film 104d is formed with gate insulating film 103 interposed therebetween. The gate electrode 111c and the gate electrode 111d are connected to each other at a PN boundary 113S between the active region 100c and the active region 100d on the isolation region 101, thereby forming a dual-gate electrode 112S. N-type source/drain regions 105c are defined at both sides of the gate electrode 111c in the active region 100c. P-type source/drain regions 105d are defined at both sides of the gate electrode 111d in the active region 100d. A contact 108 is formed to be connected to the dual-gate electrode 112S, the n-type source/drain regions 105c, and the p-type source/drain regions 105d.

FIGS. 16A and 16B are views schematically illustrating formation of a p-type region and an n-type region by implanting ions of impurities into a polysilicon film (before gate patterning) to be dual-gate electrodes 112L and 112S. In FIGS. 16A and 16B, components already shown in FIGS. 15A-15D are denoted by the same reference characters.

As illustrated in FIGS. 16A and 16B, in gate injection for the PMIS regions, ions of a p-type impurity are implanted into the polysilicon film 104 using a mask pattern 151 covering the NMIS region in each of the logic area and the SRAM area, thereby forming p-type polysilicon films 104b and 104d. That is, the p-type polysilicon films 104b and 104d have substantially the same concentration of the p-type impurity. In gate injection for the NMIS regions, ions of an n-type impurity are implanted into the polysilicon film 104 using a mask pattern 152 covering the PMIS region of each of the logic area and the SRAM area, thereby forming n-type polysilicon films 104a and 104c. That is, the n-type polysilicon films 104a and 104c have substantially the same concentration of the n-type impurity. For simplicity, not resist patterns actually employed in ion implantation but mask patterns on photomasks for forming the resist patterns are schematically shown as the mask patterns 151 and 152. The mask patterns 151 and 152 are designed such that the PN boundaries formed in the polysilicon film 104 are located between the active region 100a and the active region 100b and between the active region 100c and the active region 100d, respectively, on the isolation region 101.

Although not shown, in ion implantation for forming source/drain regions in each of the PMIS region and the NMIS region, mask patterns similar to the mask patterns 151 and 152 shown in FIGS. 16A and 16B are used.

In the gate injection illustrated in FIGS. 16A and 16B, the PN boundary formed in the polysilicon film 104 is located on a portion of the isolation region between the active regions. Thus, it is possible to reduce degradation of characteristics of FETs due to mutual

diffusion of impurities between the n-type region and the p-type region in the polysilicon gate electrode.

SUMMARY

However, as the gate length decreases with miniaturization of devices, there arises the following problem in addition to the problem of mutual diffusion in the polysilicon film. Specifically, the difference in the etching speed of the polysilicon film between different types of ions serving as dopants relatively increases, thereby causing a variation in final gate length, and as a result, a variation in the threshold voltages of transistors arises. To solve the problem, especially in devices such as SRAMs which need to have their cell sizes reduced, it is necessary to reduce a variation in gate dimensions occurring near a PN boundary.

In addition, as in the conventional method described above, even if the PN boundary in the polysilicon gate electrode is located on a portion of the isolation region between the active regions, a small width of the isolation region especially in a device such as an SRAM makes the influence of mutual diffusion of impurities between the n-type region and the p-type region in the polysilicon gate electrode nonnegligible. Consequently, a variation occurs in the work functions of the gate electrodes to deteriorate transistor characteristics such as a variation in threshold voltage. As a result, failures in circuit operation often occurs.

It is therefore an object of the present disclosure to reduce a variation in transistor characteristics due to a variation in gate dimensions near a PN boundary and mutual diffusion of impurities in a semiconductor device with a CMIS dual-gate structure.

To achieve the object, a semiconductor device in an aspect of the present disclosure includes: a first dual-gate electrode; and a second dual-gate electrode, wherein the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a

second active region and having a first silicon film of a second conductivity type, the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type, the first active region and the second active region are isolated from each other with an isolation region interposed therebetween, the first gate electrode and the second gate electrode are connected to each other on the isolation region, and at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

In the semiconductor device, an isolation width between the first active region and the second active region may be larger than that between the third active region and the fourth active region.

In the semiconductor device, at least a portion of the first silicon film of the second conductivity type may have a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on each of the first active region and the isolation region may have a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

a portion of the first silicon film of the second conductivity type located on the second active

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the second active region may have a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the second active region may have a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the isolation region may have a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the isolation region may have a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the second active region may have a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the second active region may have a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

In the semiconductor device, a portion of the first silicon film of the second conductivity type located on the isolation region may have a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on the first active region may have a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region, and a portion of the first silicon film of the second conductivity type located on the second active region may have a

second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

In the semiconductor device, the first gate electrode may be a gate electrode of a first PMIS transistor, the second gate electrode may be a gate electrode of a first NMIS transistor, the third gate electrode may be a gate electrode of a second PMIS transistor, and the fourth gate electrode may be a gate electrode of a second NMIS transistor.

In the semiconductor device, each of the first gate electrode and the second gate electrode may be a gate electrode of a transistor for a logic circuit, and each of the third gate electrode and the fourth gate electrode may be a gate electrode of a transistor for an SRAM circuit.

A method for fabricating a semiconductor device in an aspect of the present disclosure is a method for forming a semiconductor device including a first dual-gate electrode including a first gate electrode located on a first active region and a second gate electrode located on a second active region and a second dual-gate electrode including a third gate electrode located on a third active region and a fourth gate electrode located on a fourth active region. The method for fabricating a semiconductor device includes the steps of: (a) forming a silicon film on the first active region, the second active region, the third active region, and the fourth active region; (b) introducing an impurity of a first conductivity type into the silicon film with portions of the silicon film located on the second active region, the third active region, and the fourth active region being covered with a first mask pattern; (c) introducing an impurity of a second conductivity type with a portion of the silicon film located on the first active region being covered with a second mask pattern; and (d) patterning the silicon film after steps (b) and (c), thereby forming the first gate electrode, the second gate electrode, the third gate electrode, and the fourth gate electrode including the silicon film on the first active region, the second active region, the third active region, and the fourth active

region, respectively. In the method for fabricating a semiconductor device, step (b) and step (c) may be performed in any order.

In the method for fabricating a semiconductor device, the first mask pattern may expose a portion of the silicon film located on the first active region, and the second mask pattern may expose portions of the silicon film located on the second active region, the third active region, and the fourth active region.

In the method for fabricating a semiconductor device, the first active region and the second active region are electrically isolated from each other by an isolation region. In step (a), the silicon film may also be formed on the isolation region, the first mask pattern may cover a portion of the silicon film located on the first active region and expose a portion of the silicon film located on the isolation region, and the second mask pattern may cover a portion of the silicon film located on the second active region and expose portions of the silicon film located on the isolation region, the third active region, and the fourth active region. The first mask pattern and the second mask pattern do not need to expose a portion of the silicon film located on the isolation region. In other words, the first mask pattern and the second mask pattern may cover a portion of the silicon film located on the isolation region.

In the method for fabricating a semiconductor device, the first active region and the second active region may be electrically isolated from each other by an isolation region. In step (a), the silicon film may also be formed on the isolation region, the first mask pattern may cover a portion of the silicon film located on the first active region and expose a portion of the silicon film located on the isolation region, and the second mask pattern may cover portions of the silicon film located on the second active region, the third active region, and the fourth active region and expose a portion of the silicon film located on the isolation region.

In the method for fabricating a semiconductor device, the second mask pattern may cover portions of the silicon film located on the third active region and the fourth active

region.

According to the present disclosure described above, it is possible to reduce a variation in transistor characteristics due to a variation in gate dimensions near a PN boundary and mutual diffusion of impurities in a semiconductor device with a CMIS dual-gate structure. Thus, the present disclosure is useful for semiconductor devices with CMIS dual-gate structures and methods for fabricating such semiconductor devices.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a plan view illustrating a logic area of a semiconductor device according to a first embodiment, FIG. 1B is a cross-sectional view taken along the line I-I in FIG. 1A, FIG. 1C is a plan view illustrating an SRAM area of the semiconductor device of the first embodiment, and FIG. 1D is a cross-sectional view taken along the line II-II in FIG. 1C.

FIGS. 2A-2F are cross-sectional views showing a process step of a method for fabricating a semiconductor device according to the first embodiment.

FIGS. 3A-3F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. 4A-4F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. 5A-5F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. 6A-6F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. 7A-7F are cross-sectional views showing a process step of the method for fabricating a semiconductor device of the first embodiment.

FIGS. 8A-8F are cross-sectional views showing a process step of the method for

fabricating a semiconductor device of the first embodiment.

FIG. 9A is a plan view illustrating a logic area of a semiconductor device according to a second embodiment, FIG. 9B is a cross-sectional view taken along the line I-I in FIG. 9A, FIG. 9C is a plan view illustrating an SRAM area of the semiconductor device of the second embodiment, and FIG. 9D is a cross-sectional view taken along the line II-II in FIG. 9C.

FIGS. 10A-10F are cross-sectional views showing a process step of a method for fabricating a semiconductor device according to the second embodiment.

FIG. 11A is a plan view illustrating a logic area of a semiconductor device according to a third embodiment, FIG. 11B is a cross-sectional view taken along the line I-I in FIG. 11A, FIG. 11C is a plan view illustrating an SRAM area of the semiconductor device of the third embodiment, and FIG. 11D is a cross-sectional view taken along the line II-II in FIG. 11C.

FIGS. 12A-12F are cross-sectional views showing a process step of a method for fabricating a semiconductor device according to the third embodiment.

FIG. 13A is a plan view illustrating a logic area of a semiconductor device according to a fourth embodiment, FIG. 13B is a cross-sectional view taken along the line I-I in FIG. 13A, FIG. 13C is a plan view illustrating an SRAM area of the semiconductor device of the fourth embodiment, and FIG. 13D is a cross-sectional view taken along the line II-II in FIG. 13C.

FIGS. 14A-14F are cross-sectional views showing a process step of a method for fabricating a semiconductor device according to the fourth embodiment.

FIG. 15A is a plan view illustrating a logic area of a conventional semiconductor device, FIG. 15B is a cross-sectional view taken along the line B-B in FIG. 15A, FIG. 15C is a plan view illustrating an SRAM area of the conventional semiconductor device, and FIG.

15D is a cross-sectional view taken along the line D-D in FIG. 15C.

FIGS. 16A and 16B are views schematically illustrating formation of p-type regions and n-type regions by implanting ions of an impurity into a polysilicon film (before gate patterning) to be a dual-gate electrode in a conventional method for fabricating a semiconductor device.

DETAILED DESCRIPTION

(FIRST EMBODIMENT)

A semiconductor device according to a first embodiment of the present disclosure will be described with reference to the drawings.

FIG. 1A is a plan view illustrating a logic area of a semiconductor device according to the first embodiment. FIG. 1B is a cross-sectional view taken along the line I-I (along the gate width) in FIG. 1A. FIG. 1C is a plan view illustrating an SRAM area of the semiconductor device of the first embodiment. FIG. 1D is a cross-sectional view taken along the line II-II (along the gate width) in FIG. 1C. In FIGS. 1A-1D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. 1B and 1D.

As illustrated in FIGS. 1A-1D, the semiconductor device of this embodiment includes an area where a logic circuit is to be formed (hereinafter referred to as a logic area) and an area where an SRAM circuit is to be formed (hereinafter referred to as an SRAM area). Each of the logic area and the SRAM area includes a region where an NMISFET is to be formed (hereinafter referred to as an NMIS region) and a region where a PMISFET is to be formed (hereinafter referred to as a PMIS region). In the NMIS region in the logic area, a p-well region 12a is provided on a semiconductor substrate 10, and an active region 10a is surrounded by an isolation region 11. In the PMIS region in the logic area, an n-well region 12b is provided on the semiconductor substrate 10, and an active region 10b is surrounded by

the isolation region 11. In the NMIS region in the SRAM area, a p-well region 12c is provided on the semiconductor substrate 10, and an active region 10c is surrounded by the isolation region 11. In the PMIS region in the SRAM area, an n-well region 12d is provided on the semiconductor substrate 10, and an active region 10d is surrounded by the isolation region 11.

On the active region 10a, a gate electrode 30a including an n-type silicon film 14a is formed with a gate insulating film 13 interposed therebetween. On the active region 10b, a gate electrode 30b including a p-type silicon film 14b is formed with the gate insulating film 13 interposed therebetween. The gate electrode 30a and the gate electrode 30b are connected to each other at a PN boundary 41L between the active region 10a and the active region 10b on the isolation region 11, thereby forming a dual-gate electrode 31L. N-type source/drain regions 20a are defined at both sides of the gate electrode 30a in the active region 10a. P-type source/drain regions 20b are defined at both sides of the gate electrode 30b in the active region 10b. Contacts 26a and 26b are formed to be connected to the n-type source/drain regions 20a and the p-type source/drain regions 20b, and a contact 26e is formed to be connected to the dual-gate electrode 31L.

On the active region 10c, a gate electrode 30c including an n-type silicon film 14c is formed with the gate insulating film 13 interposed therebetween. On the active region 10d, a gate electrode 30d including a p-type silicon film 14d is formed with the gate insulating film 13 interposed therebetween. The gate electrode 30c and the gate electrode 30d are connected to each other at a PN boundary 41S between the active region 10c and the active region 10d on the isolation region 11, thereby forming a dual-gate electrode 31S. N-type source/drain regions 20c are defined at both sides of the gate electrode 30c in the active region 10c. P-type source/drain regions 20d are defined at both sides of the gate electrode 30d in the active region 10d. Contacts 26c and 26d are formed to be connected to the n-type

source/drain regions 20c and the p-type source/drain regions 20d, and a contact 26f is formed to be connected to the gate electrode 30c.

A feature of this embodiment is that the p-type impurity concentration in the entire p-type silicon film 14b is higher than that in the entire p-type silicon film 14d.

The n-type impurity concentration of the n-type silicon film 14a is substantially equal to that of the n-type silicon film 14c. The width of the isolation region 11 (specifically a portion of the isolation region 11 between the active region 10a and the active region 10b) in the logic area is, for example, about 70 nm or more, whereas the width of the isolation region 11 (specifically a portion of the isolation region 11 between the active region 10c and the active region 10d) in the SRAM area is, for example, about 30-60 nm.

A method for fabricating a semiconductor device according to the first embodiment will be described hereinafter with reference to the drawings.

FIGS. 2A-2F, 3A-3F, 4A-4F, 5A-5F, 6A-6F, 7A-7F, and 8A-8F are cross-sectional views illustrating process steps of a method for fabricating a semiconductor device according to the first embodiment. FIGS. 2A, 3A, 4A, 5A, 6A, 7A, and 8A illustrate cross-sectional structures taken along the line III-III (along the gate length) in FIG. 1A in respective process steps. FIGS. 2B, 3B, 4B, 5B, 6B, 7B, and 8B illustrate cross-sectional structures taken along the line IV-IV (along the gate length) in FIG. 1A in the respective process steps. FIGS. 2C, 3C, 4C, 5C, 6C, 7C, and 8C illustrate cross-sectional structures taken along the line V-V (along the gate length) in FIG. 1C in the respective process steps. FIGS. 2D, 2D, 3D, 4D, 5D, 6D, 7D, and 8D illustrate cross-sectional structures taken along the line VI-VI (along the gate length) in FIG. 1C in the respective process steps. FIGS. 2E, 3E, 4E, 5E, 6E, 7E, and 8E illustrate cross-sectional structures taken along the line I-I (along the gate width) in FIG. 1A in the respective process steps. FIGS. 2F, 3F, 4F, 5F, 6F, 7F, and 8F illustrate cross-sectional structures taken along the line II-II (along the gate width) in FIG. 1C in the

respective process steps.

First, as illustrated in FIGS. 2A-2F, an isolation region 11 formed by filling a trench with an insulating film is selectively formed in an upper portion of a semiconductor substrate 10 of, for example, p-type silicon by a method such as shallow trench isolation (STI). Accordingly, in the NMIS region in the logic area, an active region 10a is formed in a portion of the semiconductor substrate 10 surrounded by the isolation region 11. In the PMIS region in the logic area, an active region 10b is formed in a portion of the semiconductor substrate 10 surrounded by the isolation region 11. In the NMIS region in the SRAM area, an active region 10c is formed in a portion of the semiconductor substrate 10 surrounded by the isolation region 11. In the PMIS region in the SRAM area, an active region 10d is formed in a portion of the semiconductor substrate 10 surrounded by the isolation region 11. Thereafter, a p-type impurity such as boron (B) is implanted into each of the NMIS regions of the semiconductor substrate 10 by, for example, lithography and ion implantation. Subsequently, an n-type impurity such as phosphorus (P) is implanted into each of the PMIS regions of the semiconductor substrate 10 by, for example, lithography and ion implantation. Then, the semiconductor substrate 10 is subjected to heat treatment at 850°C for 30 seconds, for example, thereby forming a p-well region 12a on the semiconductor substrate 10 in the NMIS region in the logic area, an n-well region 12b on the semiconductor substrate 10 in the PMIS region in the logic area, a p-well region 12c on the semiconductor substrate 10 in the NMIS region in the SRAM area, and an n-well region 12d on the semiconductor substrate 10 in the PMIS region in the SRAM area.

Next, as illustrated in FIGS. 3A-3F, the surface of the semiconductor substrate 10 is cleaned with diluted hydrogen fluoride, and then a gate insulating film 13 of a silicon dioxide film with a thickness of, for example, about 2 nm is formed by in-situ steam generation (ISSG) oxidation on the active regions 10a, 10b, 10c, and 10d. Thereafter, the

semiconductor substrate 10 is subjected to, for example, a nitrogen plasma process, thereby nitriding the surface of the gate insulating film 13 to form a nitrided layer (not shown). Then, annealing is performed, thereby removing nitrogen atoms with weak bonds from the nitrided layer. Subsequently, a silicon film 14 of, for example, polysilicon with a thickness of about 100 nm is deposited by, for example, chemical vapor deposition (CVD) over the gate insulating film 13.

Then, as illustrated in FIGS. 3A-3F, with a mask pattern 51A covering the entire NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the entire PMIS region in the logic area, ions of a p-type impurity such as boron (B) are implanted into the silicon film 14 at a dose of 4×10^{15} cm^{-2}, thereby forming a p-type silicon film 14P. Thereafter, with a mask pattern 52A covering the entire PMIS region in the logic area and exposing the entire NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area), ions of an n-type impurity such as phosphorus (P) are implanted into the silicon film 14 at a dose of 3×10^{15} cm^{-2}, thereby forming an n-type silicon film 14N. That is, as a feature of this embodiment, ions of the n-type impurity are implanted in the gate injection for the PMIS region in the SRAM area.

Formation of the p-type silicon film 14P and formation of the n-type silicon film 14N may be performed in any order. In FIGS. 3A-3F, not resist patterns formed on the semiconductor substrate 10 by photolithography but mask patterns on photomasks for forming these resist patterns are schematically shown as the mask patterns 51A and 52A for simplicity. The mask patterns 51A and 52A are designed such that the PN boundary 41L between the p-type silicon film 14P and the n-type silicon film 14N is located on a portion of the isolation region 11 between the active region 10a and the active region 10b.

After formation of the p-type silicon film 14P and the n-type silicon film 14N, the

semiconductor substrate 10 is subjected to heat treatment at 850°C for 30 seconds, for example, thereby uniformizing a profile (specifically a profile vertical to the principal surface of the substrate, hereinafter referred to as a vertical profile) of an impurity implanted in the form of ions into each of the p-type silicon film 14P and the n-type silicon film 14N.

Thereafter, a resist pattern (not shown) having a gate shape is formed by photolithography on the silicon film 14, and then using the resist pattern as a mask, the silicon film 14 is patterned by dry etching. In this manner, as illustrated in FIGS. 4A-4F, a gate electrode 30a including an n-type silicon film 14a is formed on the active region 10a with a gate insulating film 13a interposed therebetween, a gate electrode 30b including a p-type silicon film 14b is formed on the active region 10b with a gate insulating film 13b interposed therebetween, a gate electrode 30c including an n-type silicon film 14c is formed on the active region 10c with a gate insulating film 13c interposed therebetween, and a gate electrode 30d including an n -type silicon film 14d' is formed on the active region 10d with a gate insulating film 13d interposed therebetween. The gate electrode 30a and the gate electrode 30b are connected to each other at the PN boundary 41L between the active region 10a and the active region 10b on the isolation region 11, thereby forming a dual-gate electrode 31L. The gate electrode 30c and the gate electrode 30d are connected to each other on a portion of the isolation region 11 between the active region 10c and the active region 10d, thereby forming a dual-gate electrode 31S. At the end of the process step shown in FIGS. 4A-4F, no PN boundary is formed in the dual-gate electrode 31S.

Subsequently, an insulating film for offset spacers of, for example, a silicon dioxide film with a thickness of 8 nm is deposited by, for example, CVD over the entire surface of the semiconductor substrate 10, and then the insulating film for offset spacers is subjected to anisotropic etching. In this manner, as illustrated in FIGS. 5A-5F, offset spacers 15a are formed on side surfaces of the gate insulating film 13a and the gate electrode 30a, offset

spacers 15b are formed on side surfaces of the gate insulating film 13b and the gate electrode 30b, offset spacers 15c are formed on side surfaces of the gate insulating film 13c and the gate electrode 30c, and offset spacers 15d are formed on side surfaces of the gate insulating film 13d and the gate electrode 30d.

Then, a resist pattern (not shown) exposing each NMIS region and covering each PMIS region is formed on the semiconductor substrate 10, and then, using the resist pattern and the gate electrodes 30a and 30c as masks, ions of an n-type impurity such as arsenic (As) are implanted. With this process, as illustrated in FIGS. 5A-5D, n-type source/drain regions (e.g., lightly doped drain (LDD) regions or extension regions) 16a and 16c having relatively shallow junction depths are defined in a self-aligned manner in portions of the active region 10a below the sides of the gate electrode 30a and in portions of the active region 10c below the sides of the gate electrode 30c. Subsequently, a resist pattern (not shown) covering each NMIS region and exposing each PMIS region is formed on the semiconductor substrate 10, and using the resist pattern and the gate electrodes 30b and 30d as masks, ions of a p-type impurity such as BF_2 are implanted. With this process, as illustrated in FIGS. 5A-5D, p-type source/drain regions (e.g., LDD regions or extension regions) 16b and 16d having relatively shallow junction depths are defined in a self-aligned manner in portions of the active region 10b below the sides of the gate electrode 30b and portions of the active region 10d below the sides of the gate electrode 30d.

Formation of the n-type source/drain regions 16a and 16c and formation of the p-type source/drain regions 16b and 16d may be performed in any order.

Then, a first insulating film of, for example, a silicon dioxide film with a thickness of about 10 nm and a second insulating film of, for example, a silicon nitride film with a thickness of about 30 nm are deposited in this order by, for example, CVD over the entire surface of the semiconductor substrate 10, and then the first insulating film and the second

insulating film are subjected to anisotropic etching. In this manner, as illustrated in FIGS. 6A-6F, sidewall spacers 19a are formed on side surfaces of the gate electrode 30a with the offset spacers 15a interposed therebetween, sidewall spacers 19b are formed on side surfaces of the gate electrode 30b with the offset spacers 15b interposed therebetween, sidewall spacers 19c are formed on side surfaces of the gate electrode 30c with the offset spacers 15c interposed therebetween, and sidewall spacers 19d are formed on side surfaces of the gate electrode 30d with the offset spacers 15d interposed therebetween. Each of the sidewall spacers 19a includes an inner sidewall 17a having an L shape in cross section and made of the first insulating film and an outer sidewall 18a located on the inner sidewall 17a and made of the second insulating film. Each of the sidewall spacers 19b includes an inner sidewall 17b having having an L shape in cross section and made of the first insulating film and an outer sidewall 18b located on the inner sidewall 17b and made of the second insulating film. Each of the sidewall spacers 19c includes an inner sidewall 17c having an L shape in cross section and made of the first insulating film and an outer sidewall 18c located on the inner sidewall 17c and made of the second insulating film. Each of the sidewall spacers 19d includes an inner sidewall 17d having an L shape in cross section and made of the first insulating film and an outer sidewall 18d located on the inner sidewall 17d and made of the second insulating film.

Subsequently, as illustrated in FIGS. 6A-6F, using a mask pattern 53 covering the entire NMIS region in the logic area and the entire NMIS region in the SRAM area, the gate electrode 30b, the offset spacers 15b, and the sidewall spacers 19b in the active region 10b, and the gate electrode 30d, the offset spacers 15d, and the sidewall spacers 19d in the active region 10d as mask, ions of a p-type impurity such as boron (B) are implanted into the active region 10b and the active region 10d at a dose of 5×10^{15} cm^{-2}. In this manner, p-type source/drain regions 20b having a junction depth deeper than that of the shallow p-type

source/drain regions 16b and connected to the p-type source/drain regions 16b are defined in a self-aligned manner below the outer sides of the sidewall spacers 19b in the active region 10b, and p-type source/drain regions 20d having a junction depth deeper than that of the shallow p-type source/drain regions 16d and connected to the p-type source/drain regions 16d are defined in a self-aligned manner below the outer sides of the sidewall spacers 19d in the active region 10d. In this process step, the p-type impurity is also implanted into the p-type silicon film 14b forming the gate electrode 30b and the n-type silicon film 14d' forming the gate electrode 30d, thereby increasing the p-type impurity concentration of the p-type silicon film 14b and changing the n-type silicon film 14d' into the p-type silicon film 14d. In this manner, a PN boundary 41S between the n-type silicon film 14c (the gate electrode 30c) and the p-type silicon film n 14d (the gate electrode 30d) is formed in the dual-gate electrode 31S. At this time, the p-type impurity concentration of the p-type silicon film 14b is higher than that of the p-type silicon film 14d.

Thereafter, as illustrated in FIGS. 6A-6F, using a mask pattern 54 covering the entire PMIS region in the logic area and the entire PMIS region in the SRAM area, the gate electrode 30a, the offset spacers 15a, and the sidewall spacers 19a in the active region 10a, and the gate electrode 30c, the offset spacers 15c, and the sidewall spacers 19c in the active region 10c as masks, ions of an n-type impurity such as arsenic (As) are implanted into the active region 10a and the active region 10c at a dose of 4×10^{15} to 5×10^{15} cm^{-2}. In this manner, n-type source/drain regions 20a having a junction depth deeper than that of the shallow n-type source/drain regions 16a and connected to the n-type source/drain regions 16a are defined in a self-aligned manner below the outer sides of the sidewall spacers 19a in the active region 10a, and n-type source/drain regions 20c having a junction depth deeper than that of the shallow n-type source/drain regions 16c and connected to the n-type source/drain regions 16c are defined in a self-aligned manner below the outer sides of the sidewall spacers

19c in the active region 10c.

Formation of the p-type source/drain regions 20b and 20d and formation of the n-type source/drain regions 20a and 20c may be performed in any order. In FIGS. 6A-6F, not resist patterns formed by photolithography on the semiconductor substrate 10 but mask patterns on photomasks for forming the resist patterns are schematically shown as the mask patterns 53 and 54 for simplicity. The mask patterns 53 and 54 are designed such that the location (i.e., on a portion of the isolation region 11 between the active region 10a and the active region 10b) of the PN boundary 41L between the p-type silicon film 14a (the gate electrode 30a) and the n-type silicon film 14b (the gate electrode 30b) is not changed and that the PN boundary 41S between the p-type silicon film 14c (the gate electrode 30c) and the n-type silicon film 14d (the gate electrode 30d) is located on a portion of the isolation region 11 between the active region 10c and the active region 10d.

After formation of the n-type source/drain regions 20a and 20c and the p-type source/drain regions 20b and 20d, the semiconductor substrate 10 is subjected to heat treatment, thereby activating the impurities implanted into the n-type source/drain regions 20a and 20c and the p-type source/drain regions 20b and 20d.

Then, natural oxide films (not shown) on the surfaces of the deep n-type source/drain regions 20a and 20c and the deep p-type source/drain regions 20b and 20d are removed, and then a metal film (not shown) of, for example, nickel with a thickness of about 10 nm is deposited by, for example, sputtering over the entire surface of the semiconductor substrate 10. Thereafter, first rapid thermal annealing (RTA) is performed on the semiconductor substrate 10 at, for example, 320°C in, for example, a nitrogen atmosphere, thereby causing silicon (Si) in surface portions of the deep n-type source/drain regions 20a and 20c and the deep p-type source/drain regions 20b and 20d and nickel (Ni) in the metal film to react with each other. In this manner, as illustrated in FIGS. 7A-7F, metal silicide

layers 21a-21d of nickel silicide are formed on the deep n-type source/drain regions 20a and 20c and the deep p-type source/drain regions 20b and 20d. In this process step, Si in surface portions of the n-type silicon films 14a and 14c constituting the gate electrode 30a and 30c and the p-type silicon films 14b and 14d constituting the gate electrodes 30b and 30d also reacts with Ni in the metal film, thereby forming metal silicide layers 22a-22d of nickel silicide on the gate electrodes 30a-30d. Subsequently, the semiconductor substrate 10 is immersed in an etchant of a mixed solution of, for example, sulfuric acid and a hydrogen peroxide solution, thereby removing unreacted portions of the metal film remaining on, for example, the isolation region 11, the offset spacers 15a-15d, and the sidewall spacers 19a-19d. Then, second RTA is performed at a temperature (e.g., 550°C) higher than that in the first RTA, thereby stabilizing the silicide content in each of the metal silicide layers 21a-21d and the metal silicide layers 22a-22d.

Thereafter, as illustrated in FIGS. 8A-8F, an insulating film 23 of, for example, a silicon nitride film a thickness of about 20 nm is deposited by, for example, plasma CVD over the entire surface of the semiconductor substrate 10. Then, an interlayer insulating film 24 of, for example, a silicon dioxide film is deposited by, for example, CVD over the insulating film 23. Subsequently, the surface of the interlayer insulating film 24 is planarized by, for example, chemical mechanical polishing (CMP). Then, as in a method for fabricating a semiconductor device with a general MIS transistor, a resist film (not shown) having a contact hole pattern is formed on the interlayer insulating film 24, and using the resist film as a mask, contact holes 25a-25d are formed by dry etching in the insulating film 23 and the interlayer insulating film 24 such that the contact holes 25a-25d reach the upper surfaces of the metal silicide layers 21a-21d, respectively. In this process step, a two-step etching process in which etching is temporarily stopped when the insulating film 23 is exposed is employed, thereby reducing the amount of overetching of the metal silicide layers 21a-21d. Thereafter,

a barrier metal film (not shown) as a stack of, for example, a titanium film and a titanium nitride film is formed by, for example, sputtering or CVD on each of the bottoms and side surfaces of the contact holes 25a-25d. Subsequently, a tungsten film, for example, is deposited by CVD over the interlayer insulating film 24 to fill the contact holes 25a-25d, and then portions of the tungsten film located outside the contact holes 25a-25d are removed by, for example, CMP. In this manner, contacts 26a-26d in each of which the tungsten film is buried with the barrier metal film interposed between the contact hole and the tungsten film are formed in the contact holes 25a-25d. Thereafter, metal interconnects (not shown) electrically connected to the contacts 26a-26d are formed on the interlayer insulating film 24.

In the foregoing manner, the semiconductor device of this embodiment, i.e., the semiconductor device including: an NMISFET located in the logic area and including the gate electrode 30a having the n-type silicon film 14a; a PMISFET located in the logic area and including the gate electrode 30b having the p-type silicon film 14b; an NMISFET located in the SRAM area and including the gate electrode 30c having the n-type silicon film 14c; and a PMISFET located in the SRAM area and including the gate electrode 30d having the p-type silicon film 14d, can be fabricated.

In this embodiment, in forming the gate electrodes 30a-30d by dry-etching the silicon film 14, substantially only the n-type impurity is present in portions of the silicon film 14 constituting the gate electrodes 30c and 30d in the SRAM area susceptible to the influence of mutual diffusion of the impurities because of a small width of the isolation region 11 (specifically a portion of the isolation region 11 between the active region 10c and the active region 10d). Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film 14 caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode 30c of the NMISFET and the gate electrode 30d of the PMISFET, thereby reducing variations in

transistor characteristics due to variations in gate length. In addition, in dry-etching the silicon film 14, it is necessary to uniformize the vertical profile of an impurity implanted into the silicon film 14 beforehand by annealing. However, in this embodiment, since substantially only an n-type impurity is present in a portion of the silicon film 14 located in the SRAM area at the time when the silicon film 14 is etched, the influence of mutual diffusion (specifically diffusion in the direction parallel to the principal surface of the substrate) of the impurities due to the annealing is substantially negligible. As a result, variations in transistor characteristics can be further reduced.

In this embodiment, in an a portion of the silicon film 14 constituting the gate electrode 30d of the PMIS region in the SRAM area, the n-type impurity is implanted in the gate injection, whereas the p-type impurity is implanted in source/drain implantation. Accordingly, to form the PMISFET in the SRAM area as a surface channel type, the n-type impurity concentration in the gate injection is preferably lower than the p-type impurity concentration in the source/drain implantation. In this case, as a feature of this embodiment, the p-type impurity concentration of the p-type silicon film 14b constituting the gate electrode 30b in the PMIS region in the logic area is higher than that of the p-type silicon film 14d in constituting the gate electrode 30d in the PMIS region in the SRAM area.

In this embodiment, gate injection of the n-type impurity is performed on the NMIS region and the PMIS region in the SRAM area, and then source/drain implantation of the p-type impurity is performed, thereby reversing the conductivity type of a portion of the silicon film 14 constituting the gate electrode 30d in the PMIS region in the SRAM area to the p-type. Alternatively, the conductivity type of a portion of the silicon film 14 constituting the gate electrode 30c in the NMIS region in the SRAM area may be reversed to the n-type by performing gate injection of the p-type impurity on the NMIS region and the PMIS region in the SRAM area and then performing source/drain implantation of the n-type impurity.

(SECOND EMBODIMENT)

A semiconductor device according to a second embodiment of the present disclosure will be described hereinafter with reference to the drawings.

FIG. 9A is a plan view illustrating a logic area of the semiconductor device of the second embodiment. FIG. 9B is a cross-sectional view taken along the line I-I (along the gate width) in FIG. 9A. FIG. 9C is a plan view illustrating an SRAM area of the semiconductor device of the second embodiment. FIG. 9D is a cross-sectional view taken along the line II-II (along the gate width) in FIG. 9C. In FIGS. 9A-9D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. 9B and 9D. In FIGS. 9A-9D, components already shown in FIGS. 1A-1D for the first embodiment are denoted by the same reference characters, and descriptions thereof will not be repeated and only different characteristics will be described hereinafter.

The second embodiment is different from the first embodiment in the following aspects. As illustrated in FIGS. 9A and 9B, a dual-gate electrode 31L in a logic area includes: a gate electrode 30a located in an NMIS region and including an n-type silicon film 14a1 provided on an active region 10a and a portion of an isolation region 11 near the active region 10a and an n-type silicon film 14a2 provided on portions of the isolation region 11 at both ends of the n-type silicon film 14a1; and a gate electrode 30b located on a PMIS region and including a p-type silicon film 14b1 provided on an active region 10b and a portion of the isolation region 11 near the active region 10b and a p-type silicon film 14b2 provided on portions of the isolation region 11 at both ends of the p-type silicon film 14b1.

The configuration of the SRAM area illustrated in FIGS. 9C and 9D including the structure of a dual-gate electrode 31S is the same as that in the SRAM area of the first embodiment illustrated in FIGS. 1C and 1D. Specifically, in the same manner as in the first

embodiment, the dual-gate electrode 31S includes a gate electrode 30c located on an NMIS region and including an n-type silicon film 14c and a gate electrode 30d located on a PMIS region and including a p-type silicon film 14d.

A feature of this embodiment is that the p-type silicon film 14b1 has a p-type impurity concentration lower than that of the p-type silicon film 14b2. In addition, each of the p-type silicon film 14b1 and the p-type silicon film 14b2 has a p-type impurity concentration higher than that of the p-type silicon film 14d. The n-type silicon film 14a1 has an n-type impurity concentration lower than that of each of the n-type silicon film 14a2 and the n-type silicon film 14c. The n-type silicon film 14a2 has an n-type impurity concentration substantially equal to that of the n-type silicon film 14c.

A method for fabricating a semiconductor device according to the second embodiment will be described hereinafter with reference to the drawings. The method for fabricating a semiconductor device of this embodiment is different from that of the first embodiment only in the location of gate injection in the logic area (see FIGS. 10A-10F).

FIGS. 10A-10F are cross-sectional views illustrating a process step of the method for fabricating a semiconductor device of the second embodiment. FIG. 10A illustrates a cross-sectional structure in the process step taken along the line III-III (along the gate length) in FIG. 9A. FIG. 10B illustrates a cross-sectional structure in the process step taken along the line IV-IV (along the gate length) in FIG. 9A. FIG. 10C illustrates a cross-sectional structure in the process step taken along the line V-V (along the gate length) in FIG. 9C. FIG. 10D illustrates a cross-sectional structure in the process step taken along the line VI-VI (along the gate length) in FIG. 9C. FIG. 10E illustrates a cross-sectional structure in the process step taken along the line I-I (along the gate width) in FIG. 9A. FIG. 10F illustrates a cross-sectional structure in the process step taken along the line II-II (along the gate width) in FIG. 9C.

In this embodiment, first, the same process step as that of the first embodiment illustrated in FIGS. 2A-2F is performed. Thereafter, as illustrated in FIGS. 10A-10F, the surface of a semiconductor substrate 10 is cleaned with, for example, diluted hydrogen fluoride, and then a gate insulating film 13 of, for example, a silicon dioxide film with a thickness of about 2 nm is deposited by, for example, ISSG oxidation on the active regions 10a, 10b, 10c, and 10d. Subsequently, the semiconductor substrate 10 is subjected to, for example, a nitrogen plasma process, thereby nitriding the surface of the gate insulating film 13 to form a nitrided layer (not shown). Then, annealing is performed, thereby removing nitrogen atoms with weak bonds from the nitrided layer. Subsequently, a silicon film 14 of, for example, polysilicon with a thickness of about 100 nm is deposited by, for example, CVD over the gate insulating film 13.

Then, as illustrated in FIGS. 10A-10F, with a mask pattern 51B covering the entire NMIS region and the active region 10b in the PMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the isolation region 11 in the PMIS region in the logic area, ions of a p-type impurity such as boron (B) are implanted into the silicon film 14 at a dose of 4×10^{15} cm^{-2}, thereby forming a p-type silicon film 14P on a portion of the isolation region 11 in the PMIS region in the logic area. In this process step, the length (e.g., about 50 nm) of a portion of the isolation region 11 covered with the mask pattern 51B near the active region 10b in the PMIS region in the logic area is determined in consideration of the influence of mutual diffusion of the impurities. Thereafter, with a mask pattern 52B covering the entire PMIS region and the active region 10a in the NMIS region in the logic area and exposing the isolation region 11 in the NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area), ions of an n-type impurity such as phosphorus (P) are implanted into the silicon film 14 at a dose of 3×10^{15} cm^{-2},

thereby forming an n-type silicon film 14N on a portion of the isolation region 11 located in the NMIS region in the logic area and the entire SRAM area. In this process step, the length (e.g., about 50 nm) of a portion of the isolation region 11 covered with the mask pattern 51B near the active region 10a in the NMIS region in the logic area is determined in consideration of the influence of mutual diffusion of the impurities. That is, in this embodiment, ions of the n-type impurity are implanted in gate injection for the PMIS region in the SRAM area in the same manner as in the first embodiment.

Formation of the p-type silicon film 14P and formation of the n-type silicon film 14N may be performed in any order. In FIGS. 10A-10F, not resist patterns formed on the semiconductor substrate 10 by photolithography but mask patterns on photomasks for forming these resist patterns are schematically shown as the mask patterns 51B and 52B for simplicity. The mask patterns 51B and 52B are designed such that a PN boundary 41L between the p-type silicon film 14P and the n-type silicon film 14N is located on a portion of the isolation region 11 between the active region 10a and the active region 10b.

After formation of the p-type silicon film 14P and the n-type silicon film 14N, the semiconductor substrate 10 is subjected to heat treatment at 850°C for 30 seconds, for example, thereby uniformizing a vertical profile of an impurity implanted as ions into each of the p-type silicon film 14P and the n-type silicon film 14N.

Thereafter, process steps similar to the process step (gate patterning) illustrated in FIGS. 4A-4F, the process step (formation of offset spacers and shallow source/drain regions) illustrated in FIGS. 5A-5F, the process step (formation of sidewall spacers and deep source/drain regions) illustrated in FIGS. 6A-6F, the process step (formation of a silicide layer) illustrated in FIGS. 7A-7F, and the process step (formation of an interlayer insulating film and a contact silicide layer) illustrated in FIGS. 8A-8F of the first embodiment are performed in order.

In the foregoing manner, the semiconductor device of this embodiment, i.e., the semiconductor device including: an NMISFET located in the logic area and including the gate electrode 30a having the n-type silicon films 14a1 and 14a2; a PMISFET located in the logic area and including the gate electrode 30b having the p-type silicon films 14b1 and 14b2; an NMISFET located in the SRAM area and including the gate electrode 30c having the n-type silicon film 14c; and a PMISFET located in the SRAM area and including the gate electrode 30d having the p-type silicon film 14d, can be fabricated.

In this embodiment, in forming the gate electrodes 30a-30d by dry-etching the silicon film 14, substantially only the n-type impurity is present in portions of the silicon film 14 constituting the gate electrodes 30c and 30d in the SRAM area susceptible to the influence of mutual diffusion of the impurities because of a small width of the isolation region 11 (specifically a portion of the isolation region 11 between the active region 10c and the active region 10d). Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film 14 caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode 30c of the NMISFET and the gate electrode 30d of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length. In addition, in dry-etching the silicon film 14, it is necessary to uniformize the vertical profile of an impurity implanted into the silicon film 14. However, in this embodiment, since substantially only the n-type impurity is present in a portion of the silicon film 14 located in the SRAM area at the time when the silicon film 14 is etched in the same manner as in the first embodiment, the influence of mutual diffusion (specifically diffusion in the direction parallel to the principal surface of the substrate) of the impurities due to the annealing is substantially negligible. As a result, variations in transistor characteristics can be further reduced.

In this embodiment, in forming the gate electrodes 30a-30d by dry-etching the

silicon film 14, substantially no impurities are implanted into portions of the silicon film 14 at least on the active regions 10a and 10b in the logic area. Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film 14 caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode 30a of the NMISFET and the gate electrode 30b of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length.

In addition, in this embodiment, in a portion of the silicon film 14 constituting the gate electrode 30d in the PMIS region in the SRAM area, the n-type impurity is implanted in the gate injection, whereas the p-type impurity is implanted in source/drain implantation. Accordingly, to form the PMISFET in the SRAM area as a surface channel type, the n-type impurity concentration in the gate injection is preferably lower than the p-type impurity concentration in the source/drain implantation, as in the first embodiment. In this case, as a feature of this embodiment, the p-type impurity concentration of each of the p-type silicon films 14b1 and 14b2 constituting the gate electrode 30b in the PMIS region in the logic area is higher than that of the p-type silicon film 14d in constituting the gate electrode 30d in the PMIS region in the SRAM area.

Further, in this embodiment, the n-type silicon film 14a1 on the active region 10a formed in the logic area has an n-type impurity concentration lower than that of the n-type silicon film 14a2 on a portion of the isolation region 11 formed in the logic area, and the p-type silicon film 14b1 on the active region 10b formed in the logic area has a p-type impurity concentration lower than that of the p-type silicon film 14b2 on a portion of the isolation region 11 formed in the logic area. Accordingly, although the gate electrodes 30a and 30b on the active regions 10a and 10b formed in the logic area have high resistances, metal silicide layers 22a and 22b are formed on the gate electrodes 30a and 30b, and the gate

electrodes 30a and 30b (i.e., gate lines) on portions of the isolation region 11 formed in the logic area have high impurity concentrations similar to those in the first embodiment. In this manner, a delay of the circuit speed due to increase in resistance of the gate electrodes 30a and 30b on the active regions 10a and 10b can be reduced. Since no impurities are implanted into portions of the silicon film 14 constituting the gate electrodes 30a and 30b on the active regions 10a and 10b in gate injection in this embodiment, an impurity in an amount necessary for preventing formation of depletion in the final structure needs to be implanted in source/drain implantation. In a case where a delay of the circuit speed due to an increase in resistance of the gate electrodes 30a and 30b on the active regions 10a and 10b has a small influence, an impurity does not need to be implanted into portions the silicon film 14 constituting the gate electrodes 30a and 30b on portions of the isolation region 11 formed in the logic area in gate injection.

In this embodiment, gate injection of the n-type impurity is performed on the NMIS region and the PMIS region in the SRAM area, and then source/drain implantation of the p-type impurity is performed, thereby reversing the conductivity type of a portion of the silicon film 14 constituting the gate electrode 30d in the PMIS region in the SRAM area to the p-type. Alternatively, the conductivity type of a portion of the silicon film 14 constituting the gate electrode 30c in the NMIS region in the SRAM area may be reversed to the n-type by performing gate injection of an p-type impurity on the NMIS region and the PMIS region in the SRAM area and then performing source/drain implantation of an n-type impurity.

(THIRD EMBODIMENT)

A semiconductor device according to a third embodiment of the present disclosure will be described hereinafter with reference to the drawings.

FIG. 11A is a plan view illustrating a logic area of the semiconductor device of the third embodiment. FIG. 11B is a cross-sectional view taken along the line I-I (along the

gate width) in FIG. 11A. FIG. 11C is a plan view illustrating an SRAM area of the semiconductor device of the third embodiment. FIG. 11D is a cross-sectional view taken along the line II-II (along the gate width) in FIG. 11C. In FIGS. 11A-11D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. 11B and 11D. In FIGS. 11A-11D, components already shown in FIGS. 1A-1D for the first embodiment are denoted by the same reference characters, and descriptions thereof will not be repeated and only different characteristics will be described hereinafter.

The third embodiment is different from the first embodiment in the following aspects. As illustrated in FIGS. 11A and 11B, in the same manner as in the second embodiment illustrated in FIGS. 9A and 9B, a dual-gate electrode 31L includes: a gate electrode 30a located in an NMIS region and including an n-type silicon film 14a1 provided on an active region 10a and a portion of the isolation region 11 near the active region 10a and an n-type silicon film 14a2 provided on portions of the isolation region 11 at both ends of the n-type silicon film 14a1; and a gate electrode 30b located on a PMIS region and including a p-type silicon film 14b1 provided on an active region 10b and a portion of the isolation region 11 near the active region 10b and a p-type silicon film 14b2 provided on portions of the isolation region 11 at both ends of the p-type silicon film 14b1.

The configuration of an SRAM area illustrated in FIGS. 11C and 11D including the structure of a dual-gate electrode 31S is basically the same as that in the SRAM area of the first embodiment illustrated in FIGS. 1C and 1D. Specifically, in the same manner as in the first embodiment, the dual-gate electrode 31S includes a gate electrode 30c located in an NMIS region and including an n-type silicon film 14c and a gate electrode 30d located in a PMIS region and including a p-type silicon film 14d. However, in this embodiment, the n-type impurity concentration of the n-type silicon film 14c and the p-type impurity

concentration of the p-type silicon film 14d are lower than those in the first embodiment.

A feature of this embodiment is that the p-type silicon film 14b2 has a p-type impurity concentration higher than that of the p-type silicon film 14d and that the p-type silicon film 14b1 has a p-type impurity concentration substantially equal to that of the p-type silicon film 14d. Specifically, the p-type silicon film 14b1 has a p-type impurity concentration lower than that of the p-type silicon film 14b2. The n-type silicon film 14a1 has an n-type impurity concentration substantially equal to that of the n-type silicon film 14c. The n-type silicon film 14a1 has an n-type impurity concentration lower than that of the n-type silicon film 14a2. Specifically, the n-type silicon film 14a2 has an n-type impurity concentration lower than that of the n-type silicon film 14c.

A method for fabricating a semiconductor device according to the third embodiment will be described hereinafter with reference to the drawings. The method for fabricating a semiconductor device of this embodiment is different from that of the first embodiment only in the location of gate injection in each of the logic area and the SRAM area (see FIGS. 12A-12F).

FIGS. 12A-12F are cross-sectional views illustrating a process step of the method for fabricating a semiconductor device of the third embodiment. FIG. 12A illustrates a cross-sectional structure in the process step taken along the line III-III (along the gate length) in FIG. 11A. FIG. 12B illustrates a cross-sectional structure in the process step taken along the line IV-IV (along the gate length) in FIG. 11A. FIG. 12C illustrates a cross-sectional structure in the process step taken along the line V-V (along the gate length) in FIG. 11C. FIG. 12D illustrates a cross-sectional structure in the process step taken along the line VI-VI (along the gate length) in FIG. 11C. FIG. 12E illustrates a cross-sectional structure in the process step taken along the line I-I (along the gate width) in FIG. 11A. FIG. 12F illustrates a cross-sectional structure in the process step taken along the line II-II (along the gate width)

in FIG. 11C.

In this embodiment, first, the same process step as that of the first embodiment illustrated in FIGS. 2A-2F is performed. Thereafter, as illustrated in FIGS. 12A-12F, the surface of a semiconductor substrate 10 is cleaned with, for example, diluted hydrogen fluoride, and then a gate insulating film 13 of, for example, a silicon dioxide film with a thickness of about 2 nm is deposited by, for example, ISSG oxidation on the active regions 10a, 10b, 10c, and 10d. Subsequently, the semiconductor substrate 10 is subjected to, for example, a nitrogen plasma process, thereby nitriding the surface of the gate insulating film 13 to form a nitrided layer (not shown). Then, annealing is performed, thereby removing nitrogen atoms with weak bonds from the nitrided layer. Subsequently, a silicon film 14 of, for example, polysilicon with a thickness of about 100 nm is deposited by, for example, CVD over the gate insulating film 13.

Then, as illustrated in FIGS. 12A-12F, with a mask pattern 51C covering the entire NMIS region and the active region 10b in the PMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the isolation region 11 in the PMIS region in the logic area, ions of a p-type impurity such as boron (B) are implanted into the silicon film 14 at a dose of 4×10^{15} cm^{-2}, thereby forming a p-type silicon film 14P on a portion of the isolation region 11 in the PMIS region in the logic area. In this process step, the length (e.g., about 50 nm) of a portion of the isolation region 11 covered with the mask pattern 51C near the active region 10b in the PMIS region in the logic area is determined in consideration of the influence of mutual diffusion of the impurities. Thereafter, with a mask pattern 52C covering the entire PMIS region and the active region 10a in the NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the isolation region 11 in the NMIS region in the logic area, ions of an n-type impurity such

as phosphorus (P) are implanted into the silicon film 14 at a dose of 3×10^{15} cm^{-2}, thereby forming an n-type silicon film 14N on a portion of the isolation region 11 located in the NMIS region in the logic area. In this process step, the length (e.g., about 50 nm) of a portion of the isolation region 11 covered with the mask pattern 52C near the active region 10a in the NMIS region in the logic area is determined in consideration of the influence of mutual diffusion of the impurities. That is, in this embodiment, no gate injection is performed on any of the NMIS region and PMIS region in the SRAM area, unlike the first and second embodiments.

Formation of the p-type silicon film 14P and formation of the n-type silicon film 14N may be performed in any order. In FIGS. 12A-12F, not resist patterns formed on the semiconductor substrate 10 by photolithography but mask patterns on photomasks for forming these resist patterns are schematically shown as the mask patterns 51C and 52C for simplicity. The mask patterns 51C and 52C are designed such that a PN boundary 41L between the p-type silicon film 14P and the n-type silicon film 14N is located on a portion of the isolation region 11 between the active region 10a and the active region 10b.

After formation of the p-type silicon film 14P and the n-type silicon film 14N, the semiconductor substrate 10 is subjected to heat treatment at, for example, 850°C for 30 seconds, thereby uniformizing a vertical profile of an impurity implanted as ions into each of the p-type silicon film 14P and the n-type silicon film 14N.

Thereafter, process steps similar to the process step (gate patterning) illustrated in FIGS. 4A-4F and the process step (formation of offset spacers and shallow source/drain regions) illustrated in FIGS. 5A-5F, the process step (formation of sidewall spacers and deep source/drain regions) illustrated in FIGS. 6A-6F, the process step (formation of a silicide layer) illustrated in FIGS. 7A-7F, and the process step (formation of an interlayer insulating film and a contact silicide layer) illustrated in FIGS. 8A-8F of the first embodiment are

performed in order.

In the foregoing manner, the semiconductor device of this embodiment, i.e., the semiconductor device including: an NMISFET located in the logic area and including the gate electrode 30a having the n-type silicon films 14a1 and 14a2; a PMISFET located in the logic area and including the gate electrode 30b having the p-type silicon films 14b1 and 14b2; an NMISFET located in the SRAM area and including the gate electrode 30c having the n-type silicon film 14c; and a PMISFET located in the SRAM area and including the gate electrode 30d having the p-type silicon film 14d, can be fabricated.

In this embodiment, in forming the gate electrodes 30a-30d by dry-etching the silicon film 14, no impurities are implanted into portions of the silicon film 14 constituting the gate electrodes 30c and 30d in the SRAM area susceptible to the influence of mutual diffusion of the impurities because of a small width of the isolation region 11 (specifically a portion of the isolation region 11 between the active region 10c and the active region 10d). Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film 14 caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode 30c of the NMISFET and the gate electrode 30d of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length. In addition, in dry-etching the silicon film 14, it is necessary to uniformize the vertical profile of an impurity implanted into the silicon film 14 beforehand by annealing. However, in this embodiment, since substantially no impurities are implanted into a portion of the silicon film 14 located in the SRAM area at the time when the silicon film 14 is etched, the influence of mutual diffusion (specifically diffusion in the direction parallel to the principal surface of the substrate) of the impurities due to the annealing is substantially negligible. As a result, variations in transistor characteristics can be further reduced.

In this embodiment, in forming the gate electrodes 30a-30d by dry-etching the silicon film 14, substantially no impurities are implanted into portions of the silicon film 14 at least on the active regions 10a and 10b in the logic area. Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film 14 caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode 30a of the NMISFET and the gate electrode 30b of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length.

In addition, in this embodiment, the n-type silicon film 14a1 on the active region 10a formed in the logic area has an n-type impurity concentration lower than that of the n-type silicon film 14a2 on a portion of the isolation region 11 formed in the logic area, and the p-type silicon film 14b1 on the active region 10b formed in the logic area has a p-type impurity concentration lower than that of the p-type silicon film 14b2 on a portion of the isolation region 11 formed in the logic area. Accordingly, although the gate electrodes 30a and 30b on the active regions 10a and 10b formed in the logic area have high resistances, metal silicide layers 22a and 22b are formed on the gate electrodes 30a and 30b, and the gate electrodes 30a and 30b (i.e., gate lines) on portions of the isolation region 11 formed in the logic area have high impurity concentrations similar to those in the first embodiment. In this manner, a delay of the circuit speed due to increase in resistance of the gate electrodes 30a and 30b on the active regions 10a and 10b can be reduced. Since no impurities are implanted into the silicon film 14 constituting the gate electrodes 30a and 30b on the active regions 10a and 10b in gate injection in this embodiment, an impurity in an amount necessary for preventing formation of depletion in the final structure needs to be implanted in source/drain implantation. In a case where a delay of the circuit speed due to an increase in resistance of the gate electrodes 30a and 30b on the active regions 10a and 10b has a small

influence, an impurity does not need to be implanted into portions of the silicon film 14 constituting the gate electrodes 30a and 30b on portions of the isolation region 11 formed in the logic area in gate injection.

Further, in this embodiment, no impurities are implanted into portions of the silicon film 14 constituting the gate electrodes 30c and 30d in the SRAM area in gate injection, i.e., impurities are implanted into portions of the silicon film 14 constituting the gate electrodes 30c and 30d only in source/drain implantation. Thus, the gate electrodes 30c and 30d have resistances higher than those of the gate electrodes 30a and 30b in the logic area. However, since transistors for SRAM circuits do not need to operate at high speed, unlike transistors for logic circuits, the influence of, for example, a delay of the circuit speed due to increase in resistance of the gate electrodes 30c and 30d is small.

(FOURTH EMBODIMENT)

A semiconductor device according to a fourth embodiment of the present disclosure will be described hereinafter with reference to the drawings.

FIG. 13A is a plan view illustrating a logic area of the semiconductor device of the fourth embodiment. FIG. 13B is a cross-sectional view taken along the line I-I (along the gate width) in FIG. 13A. FIG. 13C is a plan view illustrating an SRAM area of the semiconductor device of the fourth embodiment. FIG. 13D is a cross-sectional view taken along the line II-II (along the gate width) in FIG. 13C. In FIGS. 13A-13D, sidewall spacers, a silicide layer, and an interlayer film, for example, are not shown for simplicity, and contacts are not shown in FIGS. 13B and 13D. In FIGS. 13A-13D, components already shown in FIGS. 1A-1D for the first embodiment are denoted by the same reference characters, and descriptions thereof will not be repeated and only different characteristics will be described hereinafter.

The configuration of the logic area illustrated in FIGS. 13A and 13B including the

structure of a dual-gate electrode 31L is the same as that of the logic area of the first embodiment illustrated in FIGS. 1A and 1B. Specifically, in the same manner as in the first embodiment, the dual-gate electrode 31L includes a gate electrode 30a located in an NMIS region and including an n-type silicon film 14a and a gate electrode 30b located in a PMIS region and including a p-type silicon film 14b.

On the other hand, the configuration of the SRAM area illustrated in FIGS. 13C and 13D including the structure of a dual-gate electrode 31S is basically the same as that in the SRAM area of the first embodiment illustrated in FIGS. 1C and 1D. Specifically, in the same manner as in the first embodiment, the dual-gate electrode 31S includes a gate electrode 30c located on an NMIS region and including an n-type silicon film 14c and a gate electrode 30d located on a PMIS region and including a p-type silicon film 14d. However, in this embodiment, the n-type impurity concentration of the n-type silicon film 14c and the p-type impurity concentration of the p-type silicon film 14d are lower than those in the first embodiment.

A feature of this embodiment is that the p-type silicon film 14b has a p-type impurity concentration higher than that of the p-type silicon film 14d and that the n-type silicon film 14a has an n-type impurity concentration higher than that of the n-type silicon film 14c.

A method for fabricating a semiconductor device according to the fourth embodiment will be described hereinafter with reference to the drawings. The method for fabricating a semiconductor device of this embodiment is different from that of the first embodiment only in the location of gate injection in the SRAM area (see FIGS. 14A-14F).

FIGS. 14A-14F are cross-sectional views illustrating a process step of the method for fabricating a semiconductor device of the fourth embodiment. FIG. 14A illustrates a cross-sectional structure in the process step taken along the line III-III (along the gate length)

in FIG. 13A. FIG. 14B illustrates a cross-sectional structure in the process step taken along the line IV-IV (along the gate length) in FIG. 13A. FIG. 14C illustrates a cross-sectional structure in the process step taken along the line V-V (along the gate length) in FIG. 13C. FIG. 14D illustrates a cross-sectional structure in the process step taken along the line VI-VI (along the gate length) in FIG. 13C. FIG. 14E illustrates a cross-sectional structure in the process step taken along the line I-I (along the gate width) in FIG. 13A. FIG. 14F illustrates a cross-sectional structure in the process step taken along the line II-II (along the gate width) in FIG. 13C.

In this embodiment, first, the same process step as that of the first embodiment illustrated in FIGS. 2A-2F is performed. Thereafter, as illustrated in FIGS. 14A-14F, the surface of a semiconductor substrate 10 is cleaned with, for example, diluted hydrogen fluoride, and then a gate insulating film 13 of, for example, a silicon dioxide film with a thickness of about 2 nm is deposited by, for example, ISSG oxidation on the active regions 10a, 10b, 10c, and 10d. Subsequently, the semiconductor substrate 10 is subjected to, for example, a nitrogen plasma process, thereby nitriding the surface of the gate insulating film 13 to form a nitrided layer (not shown). Then, annealing is performed, thereby removing nitrogen atoms with weak bonds from the nitrided layer. Subsequently, a silicon film 14 of, for example, polysilicon with a thickness of about 100 nm is deposited by, for example, CVD over the gate insulating film 13.

Then, as illustrated in FIGS. 14A-14F, with a mask pattern 51D covering the entire NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the entire PMIS region in the logic area, ions of a p-type impurity such as boron (B) are implanted into the silicon film 14 at a dose of 4×10^{15} cm^{-2}, thereby forming a p-type silicon film 14P in the entire PMIS region in the logic area. Thereafter, with a mask pattern 52D covering the entire PMIS region in the logic area

and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and exposing the entire NMIS region in the logic area, ions of an n-type impurity such as phosphorus (P) are implanted into the silicon film 14 at a dose of 3×10^{15} cm^{-2}, thereby forming an n-type silicon film 14N in the entire NMIS region in the logic area. That is, in this embodiment, no gate injection is performed on any of the NMIS region and the PMIS region in SRAM area, as in the third embodiment.

Formation of the p-type silicon film 14P and formation of the n-type silicon film 14N may be performed in any order. In FIGS. 14A-14F, not resist patterns formed on the semiconductor substrate 10 by photolithography but mask patterns on photomasks for forming these resist patterns are schematically shown as the mask patterns 51D and 52D for simplicity. The mask patterns 51D and 52D are designed such that a PN boundary 41L between the p-type silicon film 14P and the n-type silicon film 14N is located on a portion of the isolation region 11 between the active region 10a and the active region 10b.

After formation of the p-type silicon film 14P and the n-type silicon film 14N, the semiconductor substrate 10 is subjected to heat treatment at, for example, 850°C for 30 seconds, thereby uniformizing a vertical profile of an impurity implanted in the form of ions into each of the p-type silicon film 14P and the n-type silicon film 14N.

Thereafter, process steps similar to the process step (gate patterning) illustrated in FIGS. 4A-4F, the process step (formation of offset spacers and shallow source/drain regions) illustrated in FIGS. 5A-5F, the process step (formation of sidewall spacers and deep source/drain regions) illustrated in FIGS. 6A-6F, the process step (formation of a silicide layer) illustrated in FIGS. 7A-7F, and the process step (formation of an interlayer insulating film and a contact silicide layer) illustrated in FIGS. 8A-8F of the first embodiment are performed in order.

In the foregoing manner, the semiconductor device of this embodiment, i.e., the

semiconductor device including: an NMISFET located in the logic area and including the gate electrode 30a having the n-type silicon film 14a; a PMISFET located in the logic area and including the gate electrode 30b having the p-type silicon film 14b; an NMISFET located in the SRAM area and including the gate electrode 30c having the n-type silicon film 14c; and a PMISFET located in the SRAM area and including the gate electrode 30d having the p-type silicon film 14d, can be fabricated.

In this embodiment, in forming the gate electrodes 30a-30d by dry-etching the silicon film 14, no impurities are implanted into portions of the silicon film 14 constituting the gate electrodes 30c and 30d in the SRAM area susceptible to the influence of mutual diffusion of the impurities because of a small width of the isolation region 11 (specifically a portion of the isolation region 11 between the active region 10c and the active region 10d). Accordingly, it is possible to avoid occurrence of difference in the etching speed of the silicon film 14 caused by difference between ion species of the implanted impurities. Thus, no difference occurs in gate dimensions between the gate electrode 30c of the NMISFET and the gate electrode 30d of the PMISFET, thereby reducing variations in transistor characteristics due to variations in gate length. In addition, in dry-etching the silicon film 14, it is necessary to uniformize the vertical profile of an impurity implanted into the silicon film 14 beforehand by annealing. However, in this embodiment, since no impurities are implanted into a portion of the silicon film 14 located in the SRAM area at the time when the silicon film 14 is etched, the influence of mutual diffusion (specifically diffusion in the direction parallel to the principal surface of the substrate) of the impurities due to the annealing is substantially negligible. As a result, variations in transistor characteristics can be further reduced.

In this embodiment, no impurities are implanted into portions of the silicon film 14 constituting the gate electrodes 30c and 30d in the SRAM area in gate injection, i.e., impurities are implanted into portions of the silicon film 14 constituting the gate electrodes

30c and 30d only in source/drain implantation. Thus, the gate electrodes 30c and 30d have resistances higher than those of the gate electrodes 30a and 30b in the logic area. However, since transistors for SRAM circuits do not need to operate at high speed, unlike transistors for logic circuits, the influence of, for example, a delay of the circuit speed due to increase in resistance of the gate electrodes 30c and 30d is small.

In the first through fourth embodiments, a silicon oxynitride film is used as a gate insulating film and a polysilicon electrode is used as a gate electrode, as examples. However, the present disclosure is not limited to these embodiments. Alternatively, the gate insulating film material may be a high-k material (e.g., an insulating material having a relative dielectric constant of 8 or more) typified by metal oxide such as alumina (Al_2O_3), hafnium oxide (HfO_2), or hafnium silicate ($HfSiO_x$), and the gate electrode structure may be a metal-inserted poly-silicon stack (MIPS) structure including a metal film of, for example, titanium nitride (TiN) or tantalum nitride (TaN) between the gate insulating film and the polysilicon film in addition to the polysilicon film. In such a case, advantages similar to those of the foregoing embodiments can be obtained. In the MIPS structure, the threshold voltage of a transistor is adjusted mainly by using the work function. This adjustment is determined by a combination of a high-k gate insulating film material and a metal film material. Specifically, the adjustment of the threshold voltage between the NMISFET and the PMISFET may be performed either by changing metal film materials while using the same high-k gate insulating film material or by changing high-k gate insulating film materials while using the same metal film material. Since formation of depletion in the gate electrode is reduced in the MIPS structure, the impurity concentration in the polysilicon film only needs to be set in consideration of gate resistance (resistance of a bulk region, resistance of a silicide/polysilicon interface, resistance of a polysilicon/metal interface). When each of the interface resistances has a sufficiently low resistance, gate resistance is low in a MIPS

structure using a metal film.

In the first and second embodiments, to form the PMISFET in the SRAM area as a surface channel type, the n-type impurity concentration in gate injection is preferably lower than the p-type impurity concentration in source/drain implantation. However, in the case of employing an MIPS structure, in view of reducing the resistance of the silicon film and the interface resistances mentioned above, the n-type impurity concentration in gate injection may be higher than the p-type impurity concentration in source/drain implantation. Alternatively, no source/drain implantation may be performed on the silicon films constituting the gate electrodes in the SRAM area. In other words, only gate injection of an n-type impurity may be performed on the silicon films constituting the gate electrodes in the SRAM area. This process changes all the silicon films constituting the gate electrodes of the CMISFETs in the SRAM area into n-type silicon films. In this case, only gate injection of an n-type impurity may be performed on the silicon films constituting the gate electrodes in the logic area, without performing source/drain implantation. This process also changes all the silicon films constituting the gate electrodes of the CMISFET in the logic area into n-type silicon films.

In the third and fourth embodiments, no gate injection is performed on the silicon films constituting the gate electrodes in the SRAM area. However, in the case of employing an MIPS structure, gate injection does not need to be performed on the silicon films constituting the gate electrodes in the SRAM area and the logic area. In other words, only source/drain implantation may be performed on the silicon films constituting the gate electrodes in the SRAM area and the logic area.

The first through fourth embodiments are directed to semiconductor device including logic circuits and SRAM circuits. However, the present disclosure is not limited to these embodiments. For example, in the case of including input/output circuits instead of

the logic circuits, the dual-gate electrodes for logic circuits of the above embodiments are applicable. Specifically, the two types of dual-gate electrodes described in each of the above embodiments can be selectively used depending on the width of the isolation region between a pair of active regions where CMISFETs are to be formed. Specifically, the dual-gate electrodes for logic circuits described in the above embodiments may be used for CMISFETs with a relatively wide isolation region, whereas the dual-gate electrodes for SRAM circuits described in the above embodiments may be used for CMISFETs with a relatively narrow isolation region.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a first dual-gate electrode; and

a second dual-gate electrode, wherein

the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,

the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,

the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,

the first gate electrode and the second gate electrode are connected to each other on the isolation region, and

at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

2. The semiconductor device of claim 1, wherein

an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.

3. The semiconductor device of claim 1, wherein

at least a portion of the first silicon film of the second conductivity type has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

4. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

5. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

6. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

7. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

8. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region.

9. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

10. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region.

11. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

12. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the second conductivity type located on the

second active region has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

13. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

14. The semiconductor device of claim 1, wherein

a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region, and

a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

15. The semiconductor device of claim 1, wherein

the first gate electrode is a gate electrode of a first PMIS transistor,

the second gate electrode is a gate electrode of a first NMIS transistor,

the third gate electrode is a gate electrode of a second PMIS transistor, and

the fourth gate electrode is a gate electrode of a second NMIS transistor.

16. The semiconductor device of claim 1, wherein

each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and

each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit.

ABSTRACT

A first dual-gate electrode includes a gate electrode located on a first active region and having a first silicon film of a first conductivity type and a gate electrode located on a second active region and having a first silicon film of a second conductivity type. A second dual-gate electrode includes a gate electrode located on a third active region and having a second silicon film of the first conductivity type and a gate electrode located on a fourth active region and having a second silicon film of the second conductivity type. At least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

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Application Number	Not Yet Assigned
Filing Date	October 31, 2012
First Named Inventor	Yoshihiro SATO
Title	SEMICONDUCTOR DEVICE
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	085393-0935

SIGNATURE of Applicant or Patent Practitioner

Signature		Date	October 31, 2012
Name	Michael E. Fogarty	Telephone	(202) 756-8372
Registration Number	36,139		

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SIGNATURE of Applicant for Patent

Signature		Date	Sep. 11, 2012
Name	HIROKI NAITO	Telephone	
Title and Company	**Director, Authorized Signing Officer for Applicant, Panasonic Corporation**		

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Title of Invention	**SEMICONDUCTOR DEVICE**

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☒ The attached application, or

☐ United States application or PCT international application number _____

filed on _____.

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LEGAL NAME OF INVENTOR

Inventor: **Yoshihiro SATO** Date (Optional) : Sep. 27, 2012

Signature: Yoshihiro Sato

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LEGAL NAME OF INVENTOR

Inventor: Hideyuki ARAI Date (Optional) : September 24, 2012

Signature: HideyukiArai

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I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Takayuki YAMADA Date (Optional): September 27, 2012

Signature: Takayuki Yamada

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FIG.1A

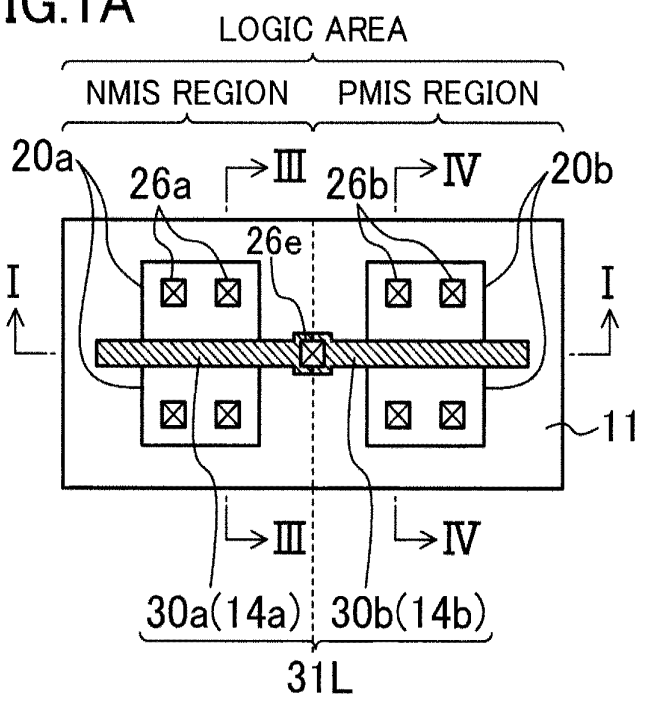


FIG.1B

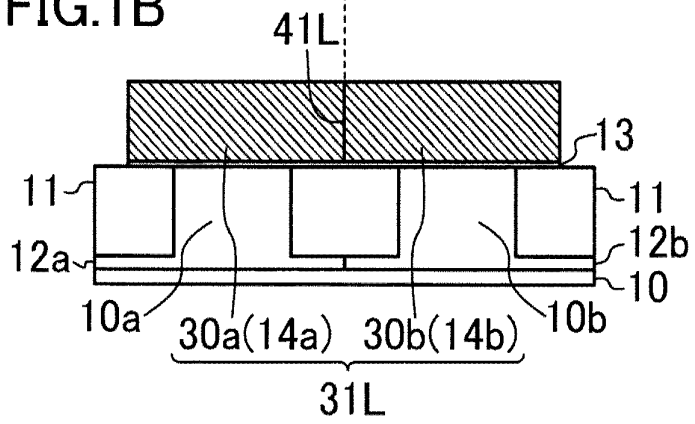


FIG.1C

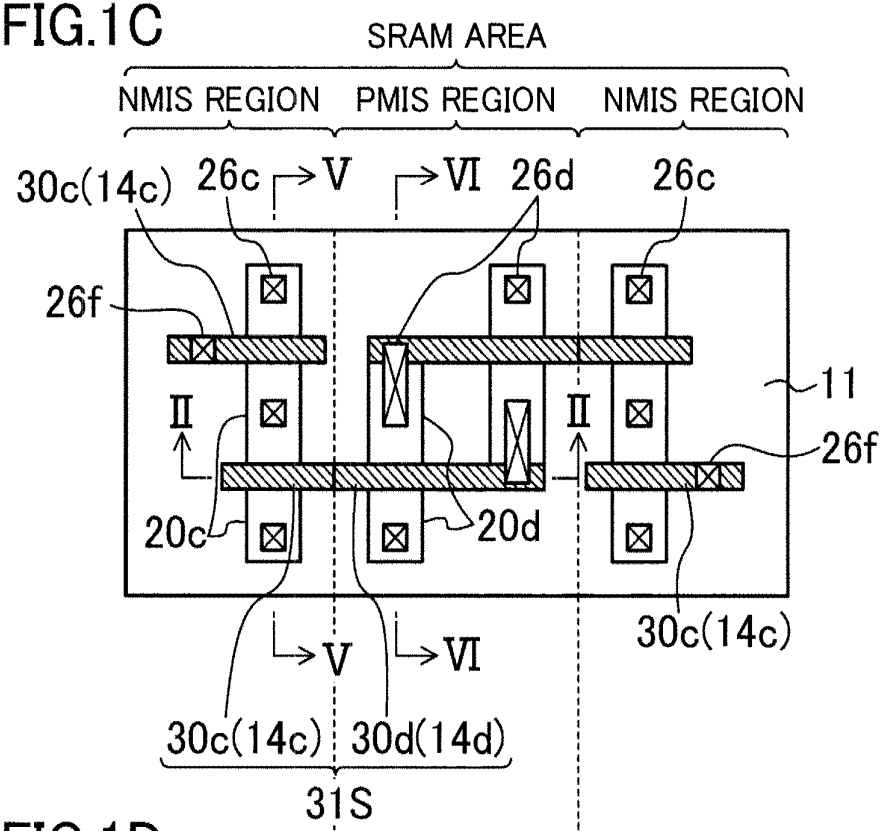
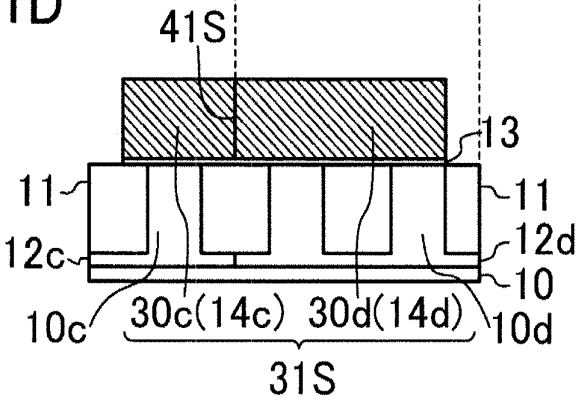


FIG.1D



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FIG.2A

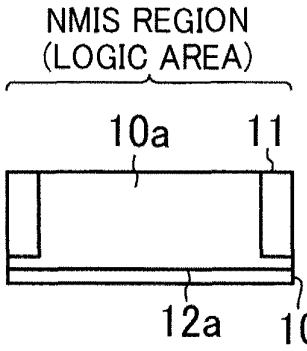


FIG.2B

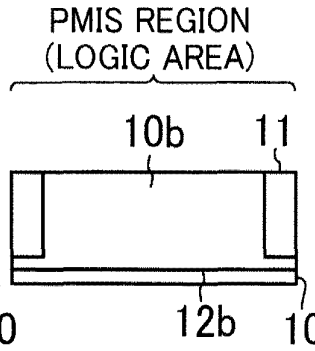


FIG.2C

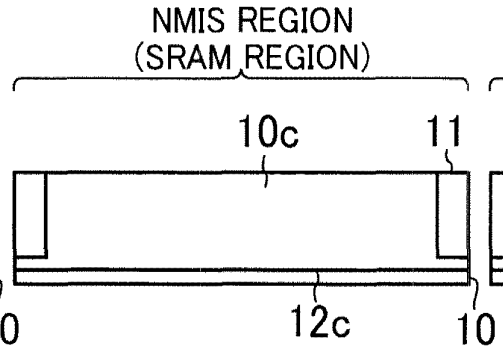


FIG.2D

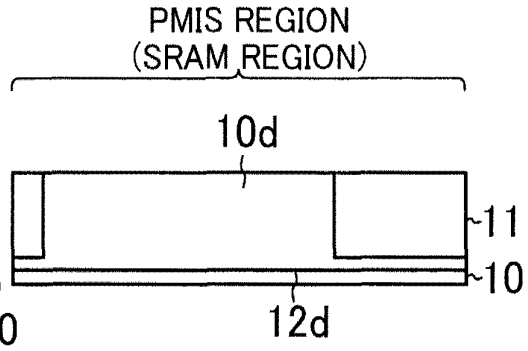


FIG.2E

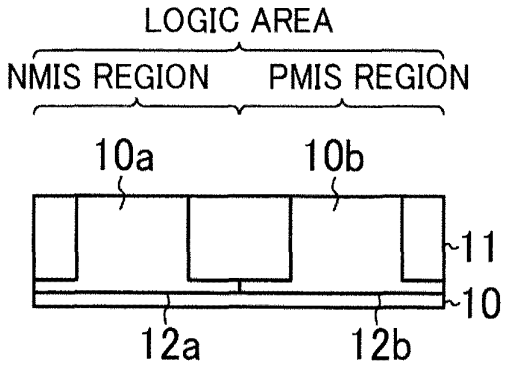
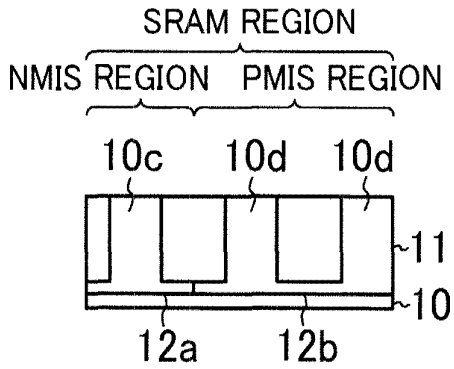
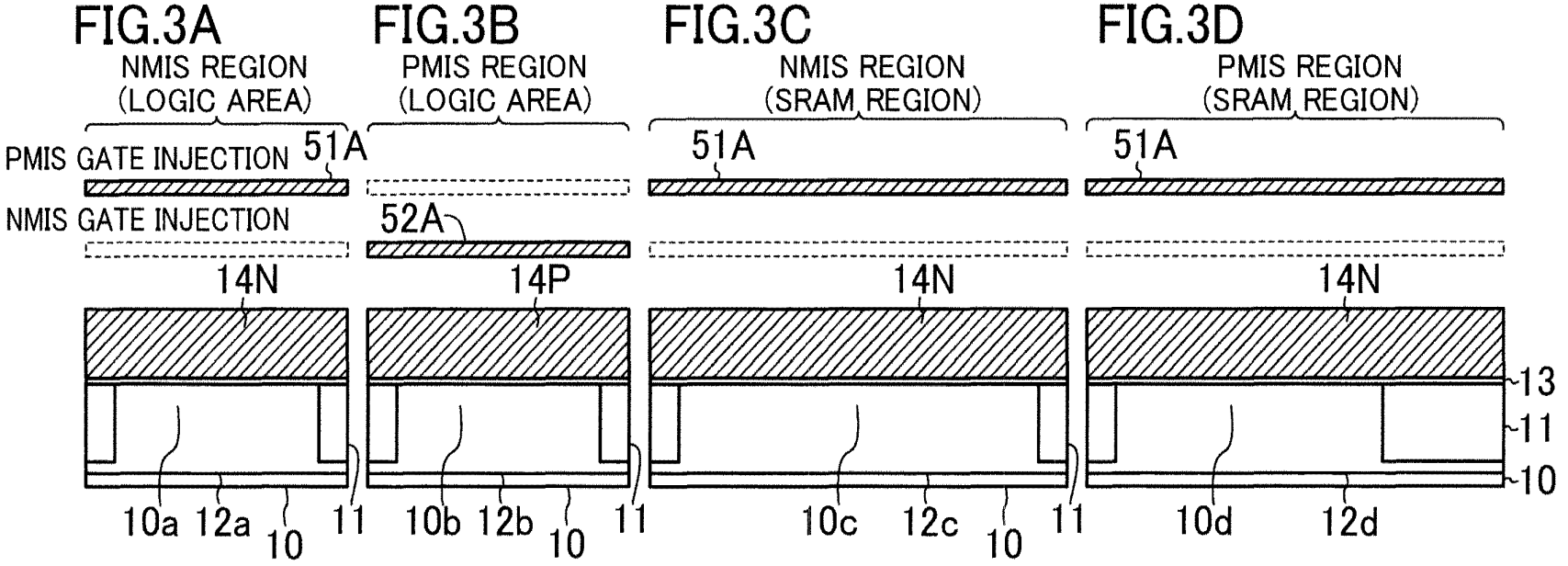


FIG.2F




FIG.3A
NMIS REGION
(LOGIC AREA)
PMIS GATE INJECTION
51A
NMIS GATE INJECTION
14N
10a
12a
10
11
FIG.3B
PMIS REGION
(LOGIC AREA)
52A
14P
10b
12b
10
11
FIG.3C
NMIS REGION
(SRAM REGION)
51A
14N
10c
12c
10
11
FIG.3D
PMIS REGION
(SRAM REGION)
51A
14N
10d
12d
13
11
10

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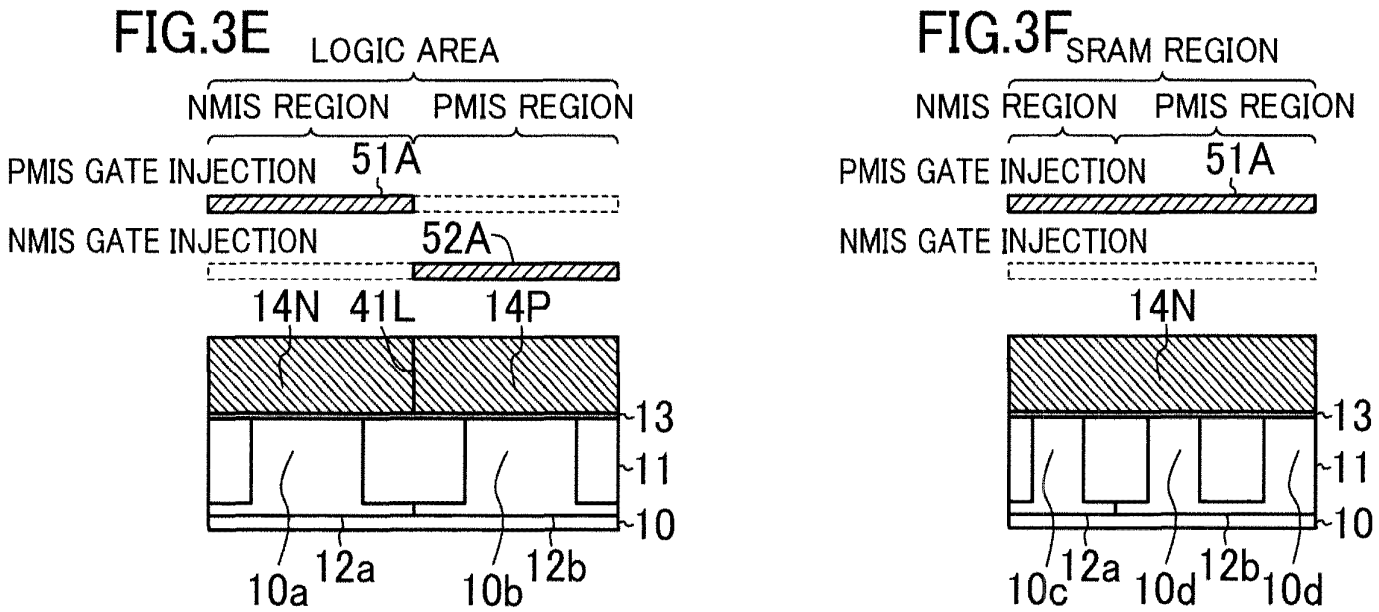

FIG.3E
LOGIC AREA
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
51A
NMIS GATE INJECTION
52A
14N
41L
14P
13
11
10
10a
12a
10b
12b
FIG.3F
SRAM REGION
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
51A
NMIS GATE INJECTION
14N
13
11
10
10c
12a
10d
12b
10d

FIG.4A

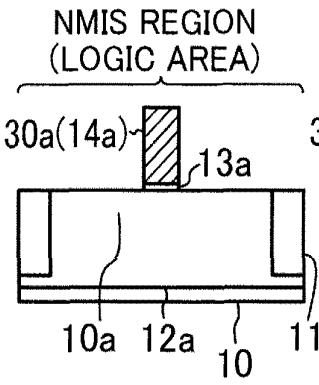


FIG.4B

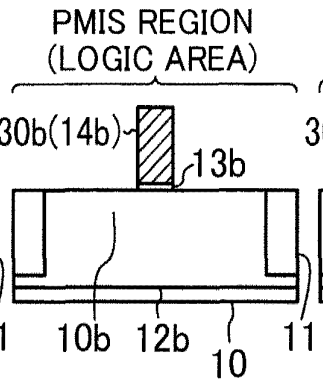


FIG.4C

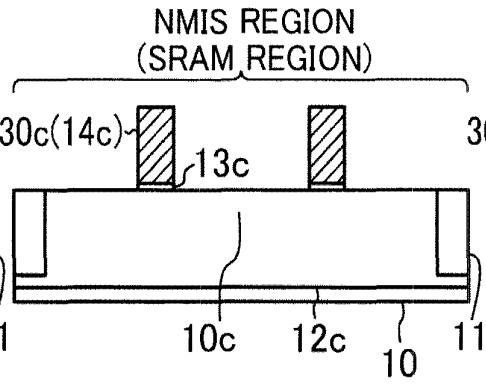


FIG.4D

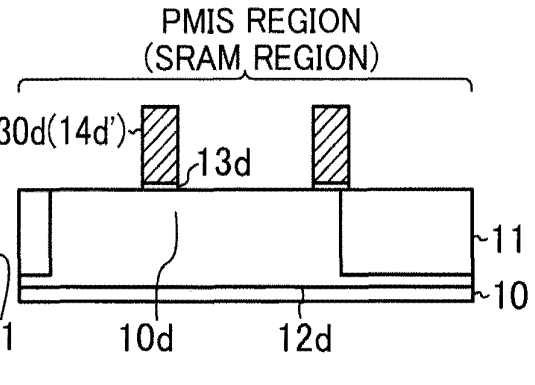


FIG.4E

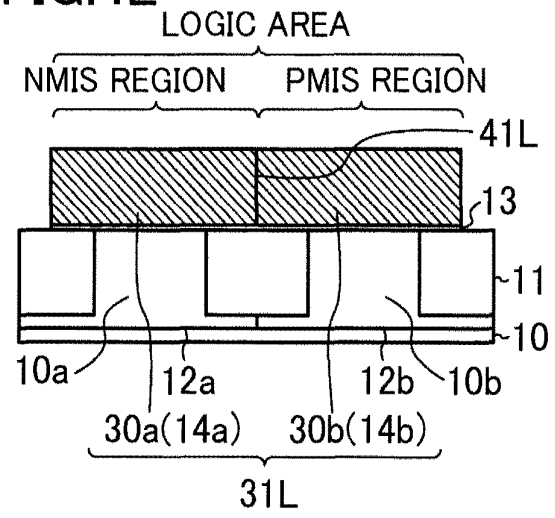


FIG.4F

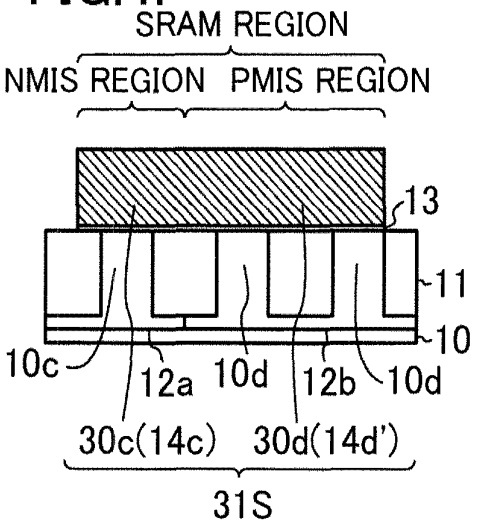


FIG.5A

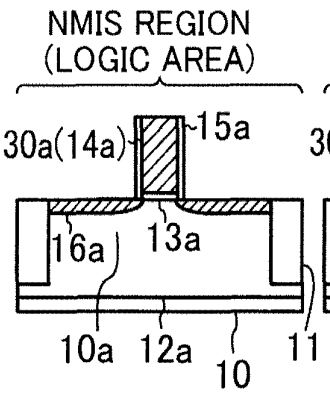


FIG.5B

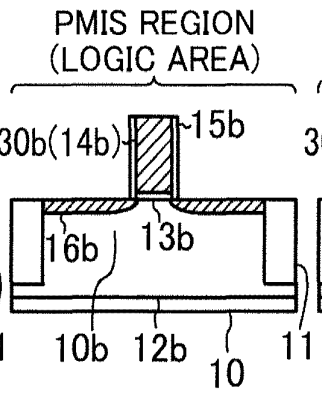


FIG.5C

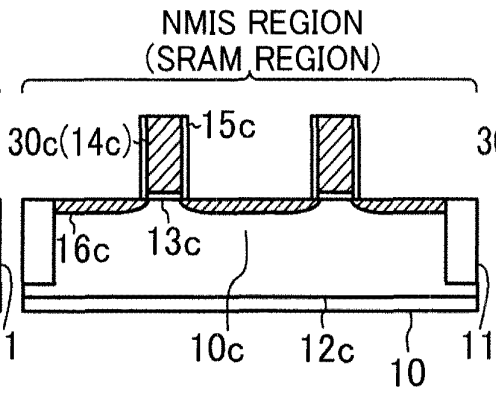
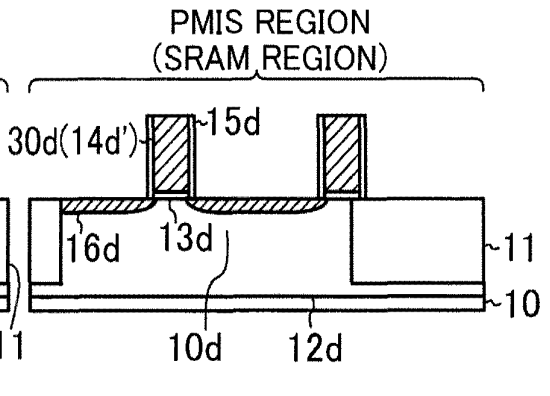


FIG.5D



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FIG.5E

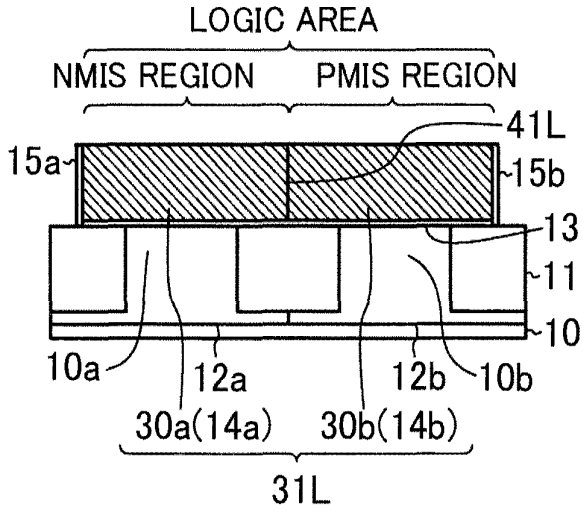
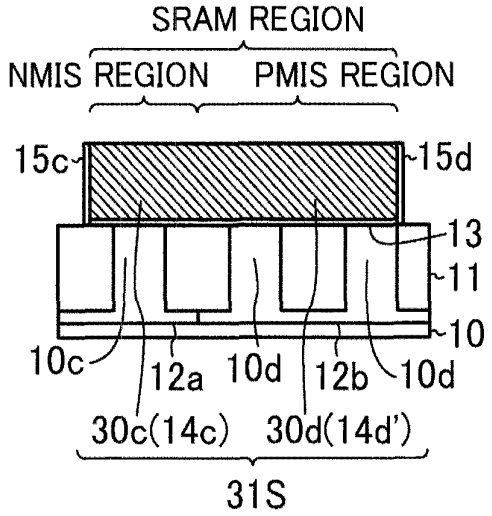
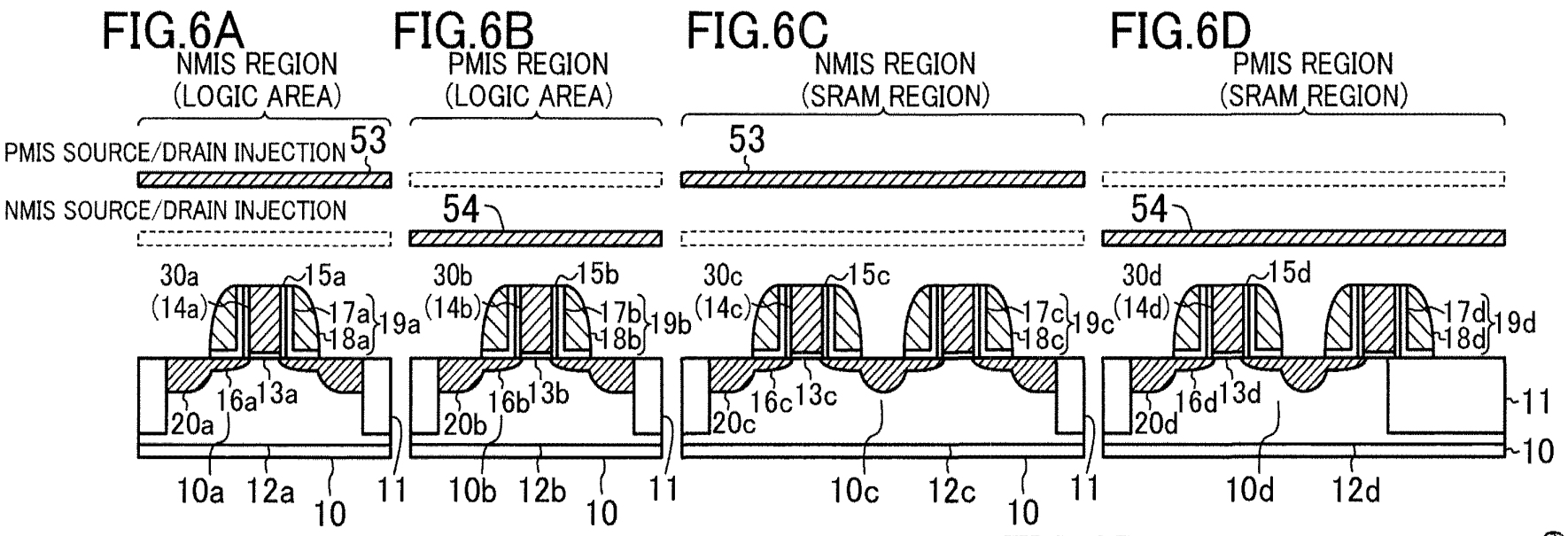
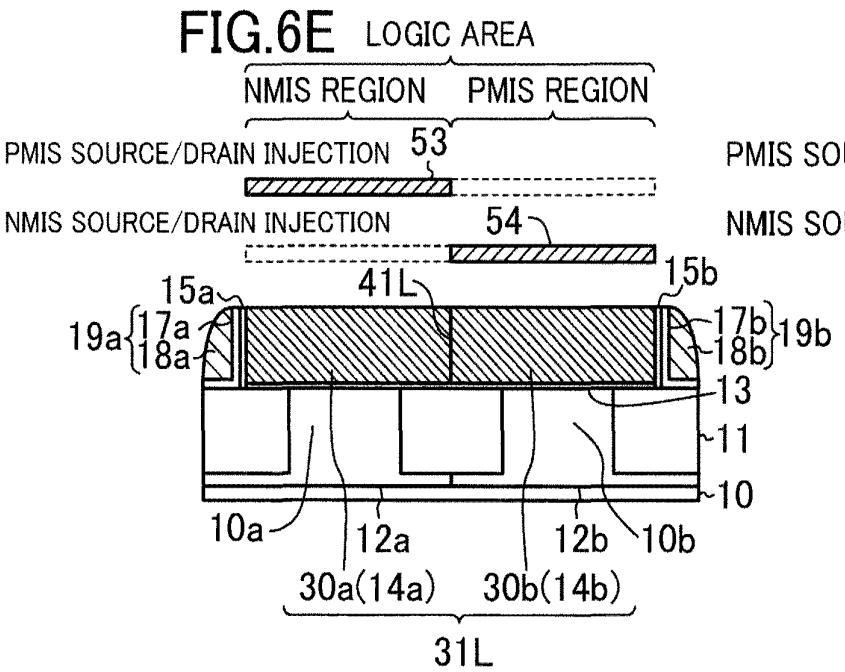
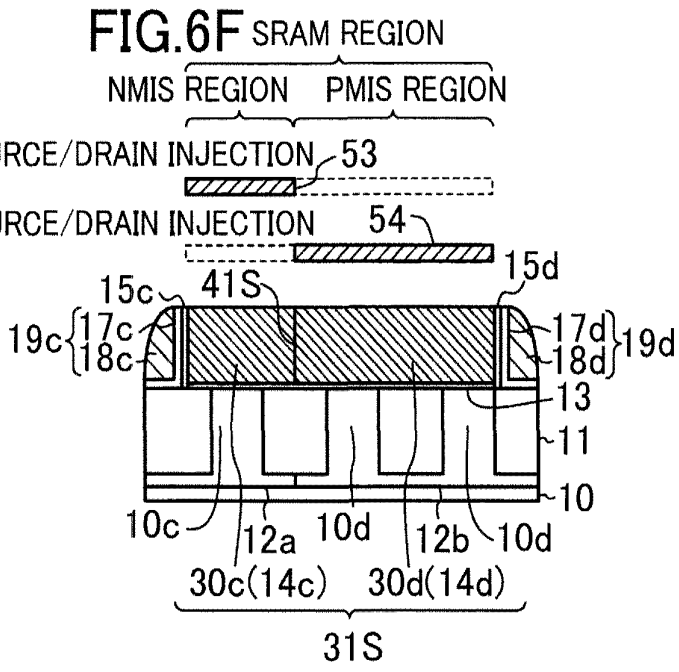


FIG.5F




FIG.6A
NMIS REGION
(LOGIC AREA)
PMIS SOURCE/DRAIN INJECTION
53
NMIS SOURCE/DRAIN INJECTION
30a
(14a)
15a
17a
18a
19a
16a
13a
20a
10a
12a
10
11
FIG.6B
PMIS REGION
(LOGIC AREA)
54
30b
(14b)
15b
17b
18b
19b
16b
13b
20b
10b
12b
10
11
FIG.6C
NMIS REGION
(SRAM REGION)
53
54
30c
(14c)
15c
17c
18c
19c
16c
13c
20c
10c
12c
10
11
FIG.6D
PMIS REGION
(SRAM REGION)
54
30d
(14d)
15d
17d
18d
19d
16d
13d
20d
10d
12d
11
10


FIG.6E LOGIC AREA
NMIS REGION
PMIS REGION
PMIS SOURCE/DRAIN INJECTION
53
NMIS SOURCE/DRAIN INJECTION
54
15a
41L
15b
19a
17a
18a
17b
18b
19b
13
11
10
10a
12a
12b
10b
30a(14a)
30b(14b)
31L


FIG.6F SRAM REGION
NMIS REGION
PMIS REGION
PMIS SOURCE/DRAIN INJECTION
53
NMIS SOURCE/DRAIN INJECTION
54
15c
41S
15d
19c
17c
18c
17d
18d
19d
13
11
10
10c
12a
10d
12b
10d
30c(14c)
30d(14d)
31S

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FIG.7A

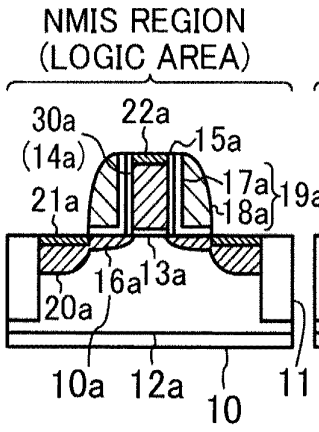


FIG.7B

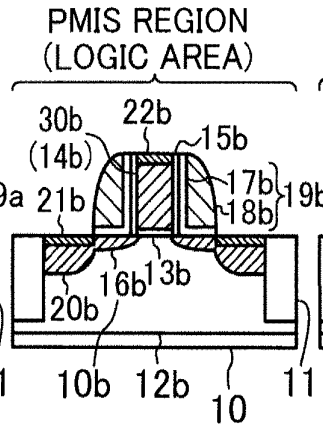


FIG.7C

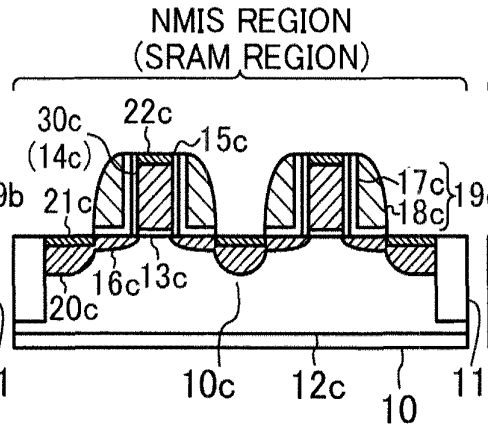


FIG.7D

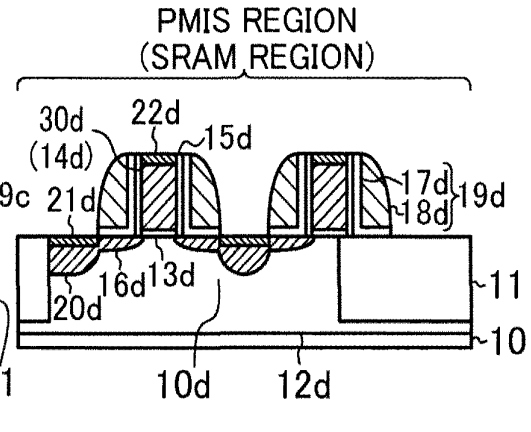


FIG.7E

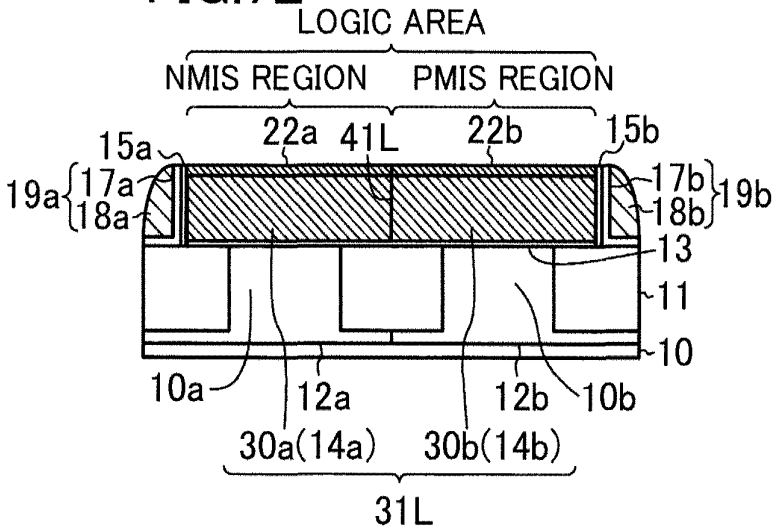
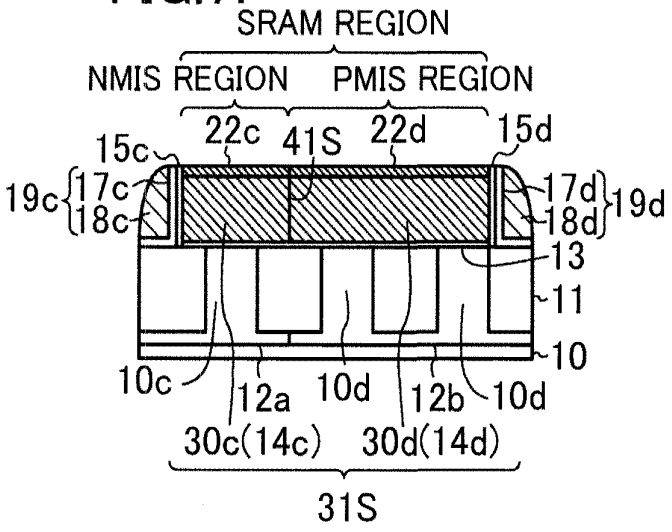


FIG.7F



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FIG.8A

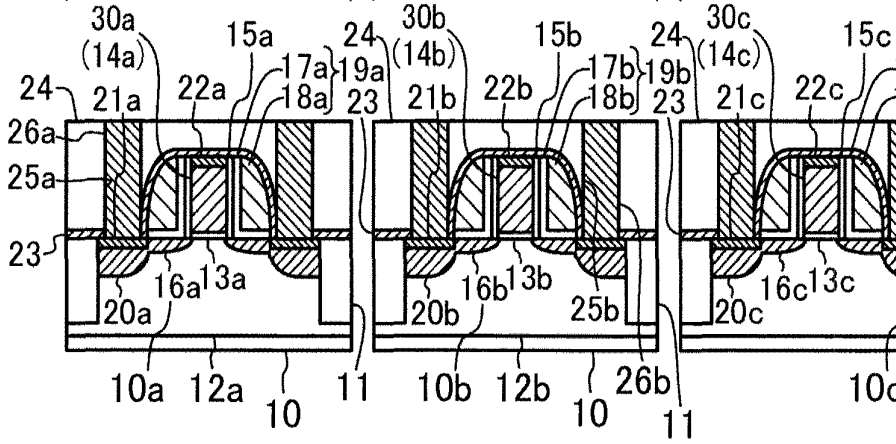


FIG.8B

FIG.8C

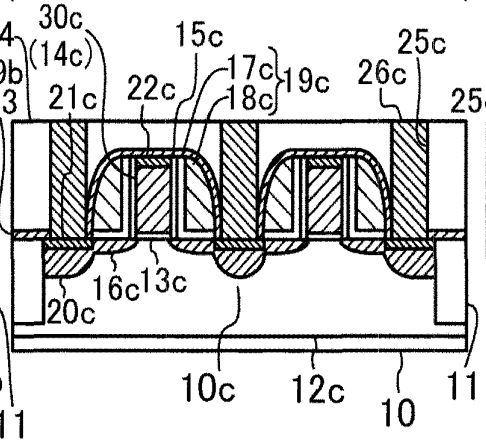


FIG.8D

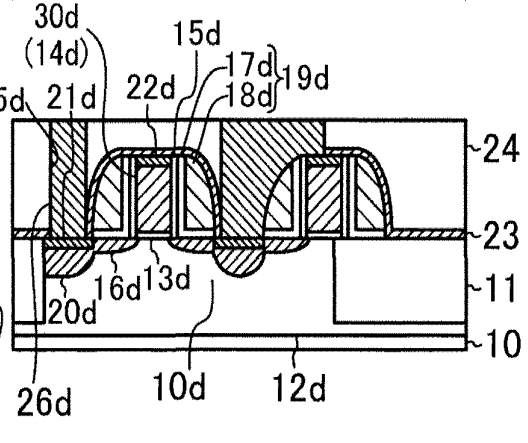


FIG.8E

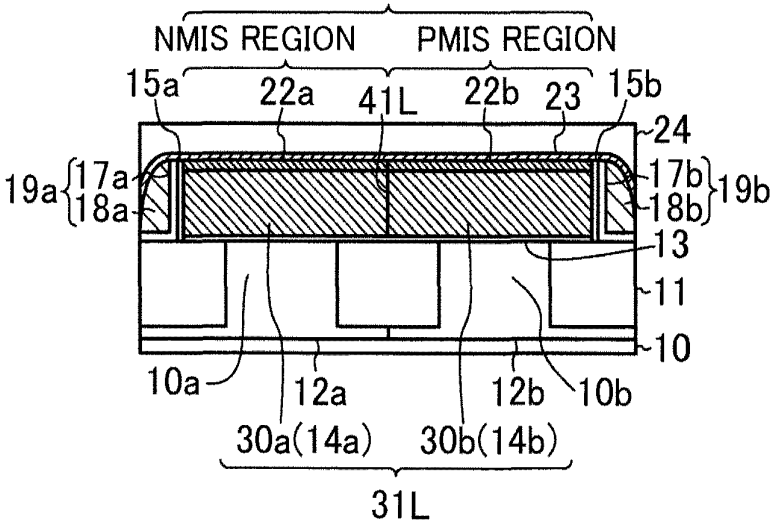
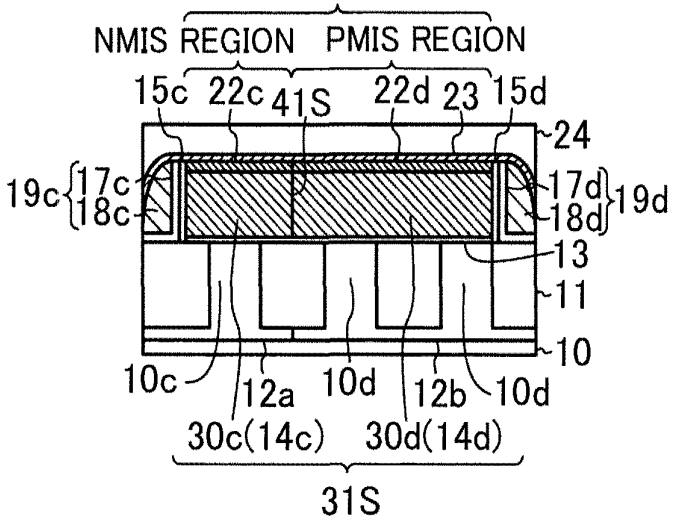


FIG.8F



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FIG.9A

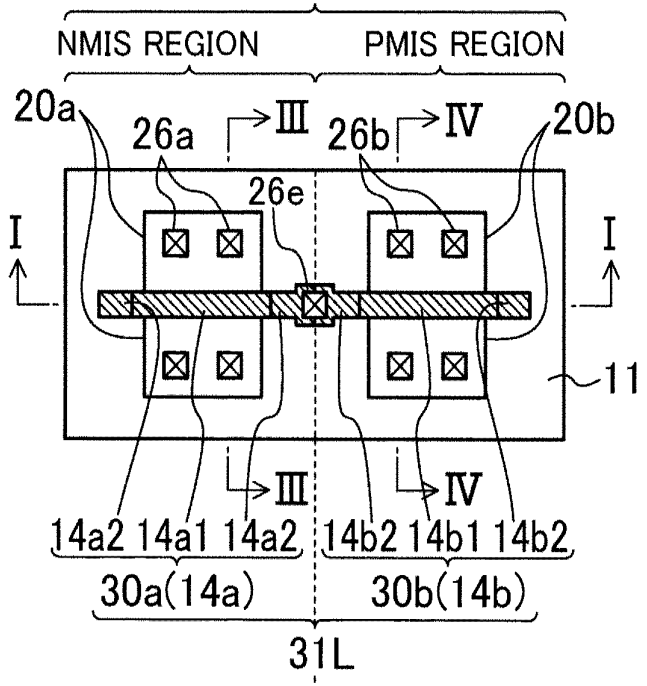


FIG.9B

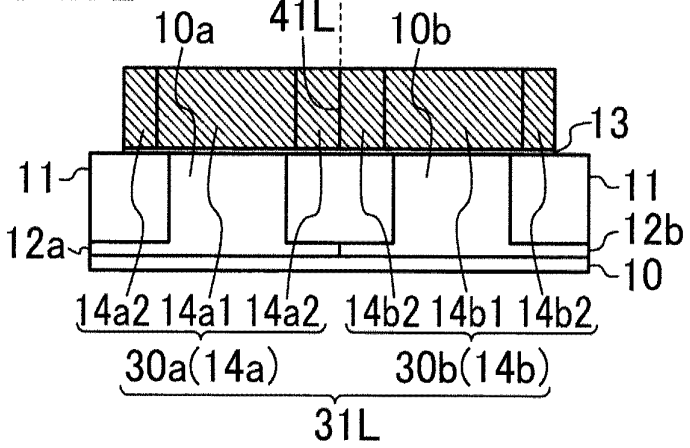


FIG.9C

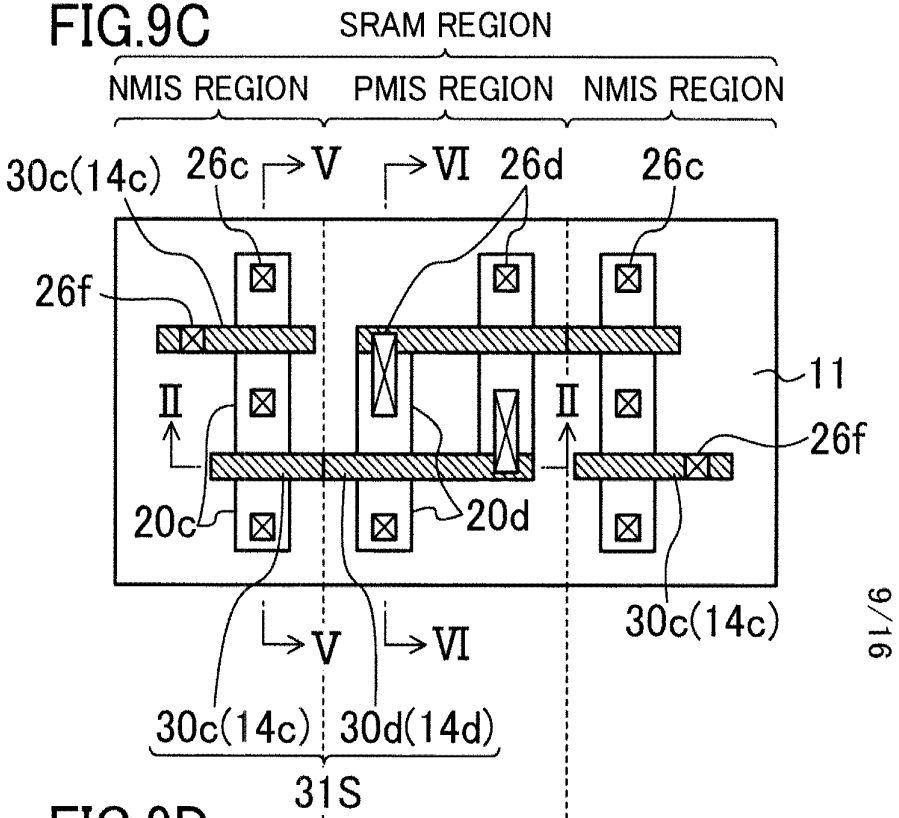
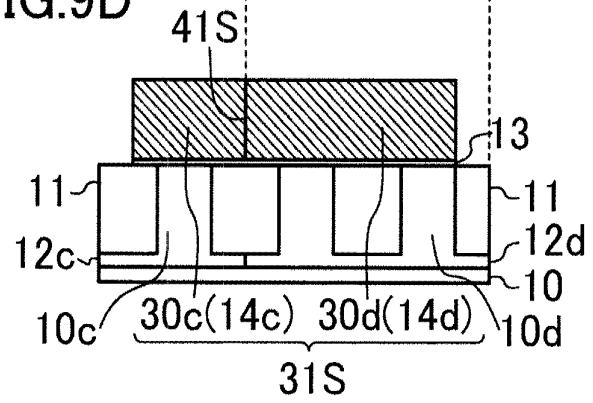


FIG.9D



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FIG.10A

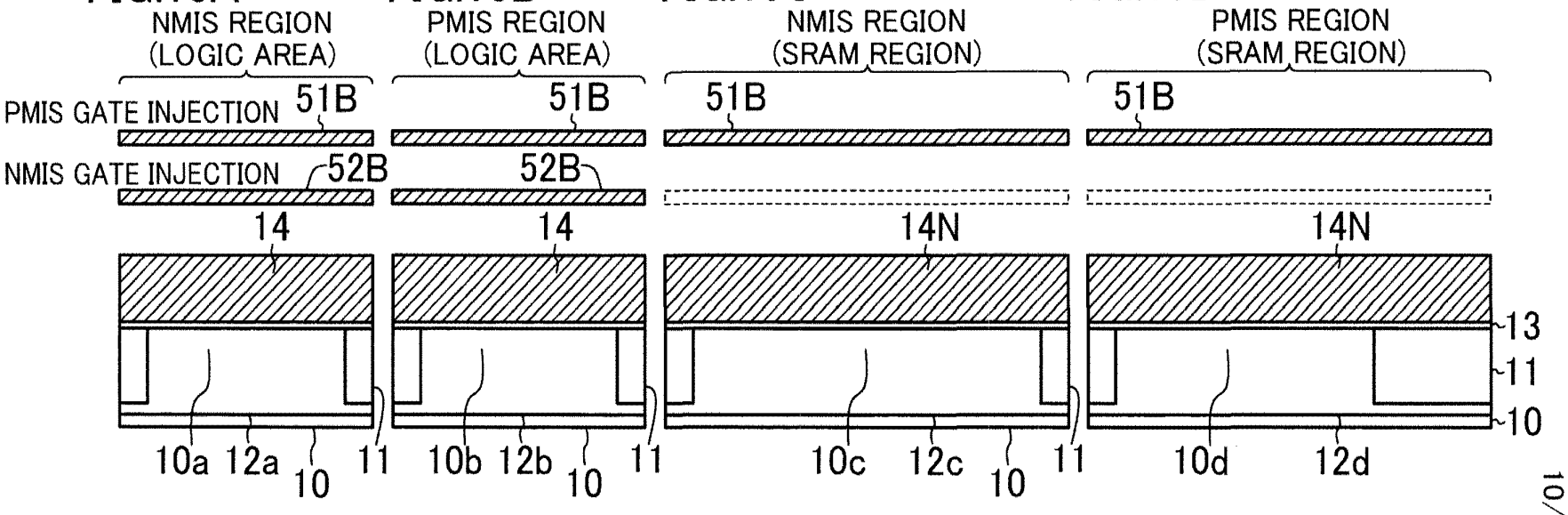


FIG.10B

FIG.10C

FIG.10D

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FIG.10E

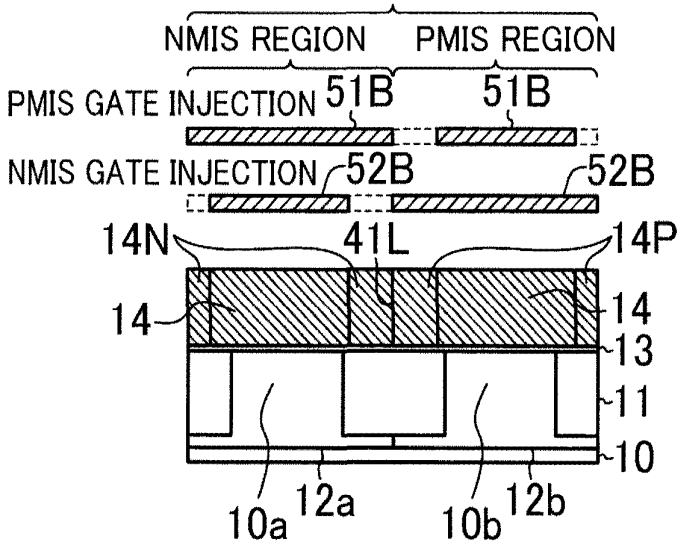


FIG.10F

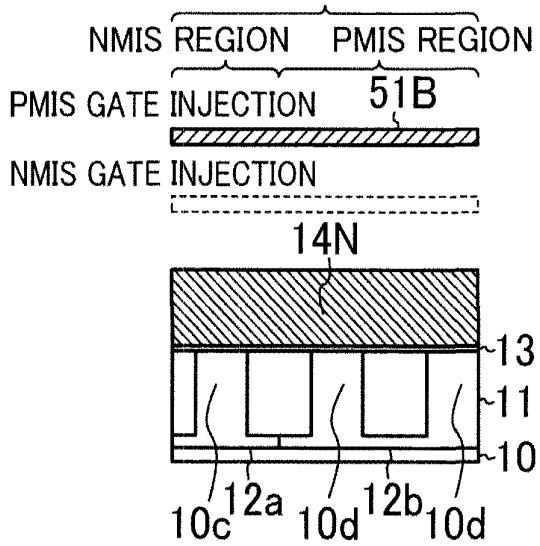


FIG.11A

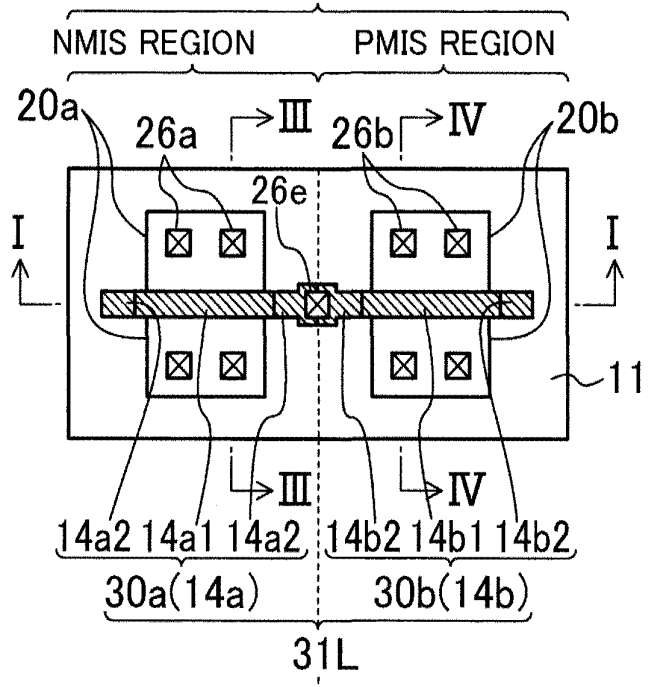


FIG.11B

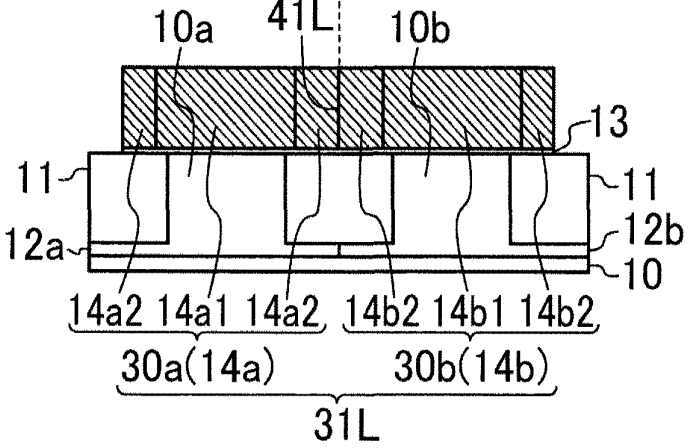


FIG.11C

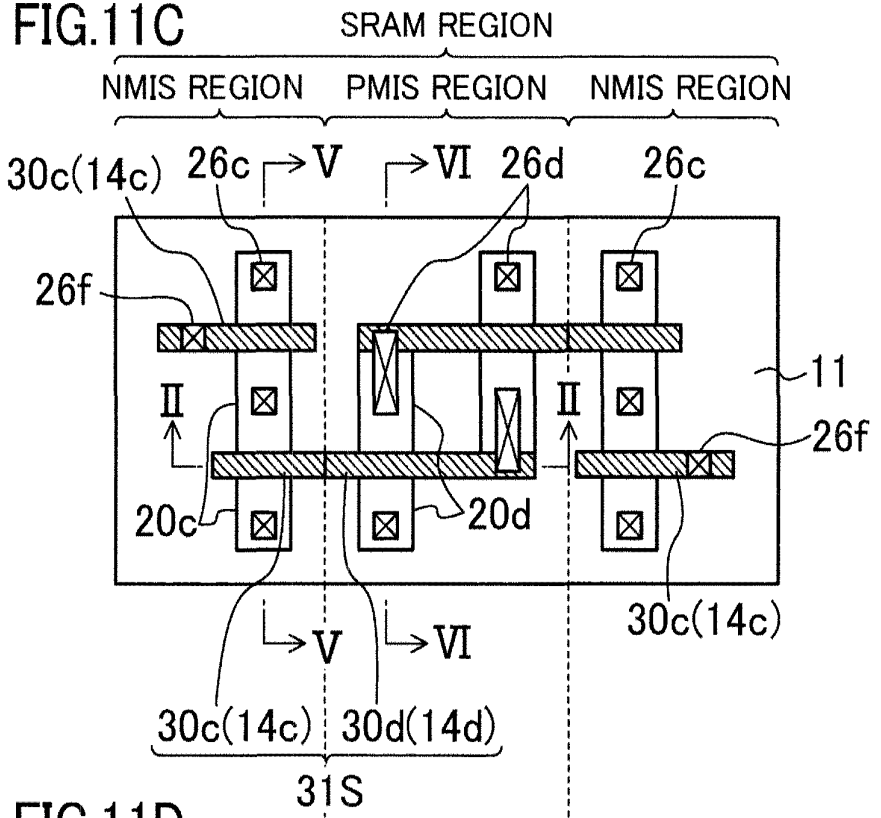
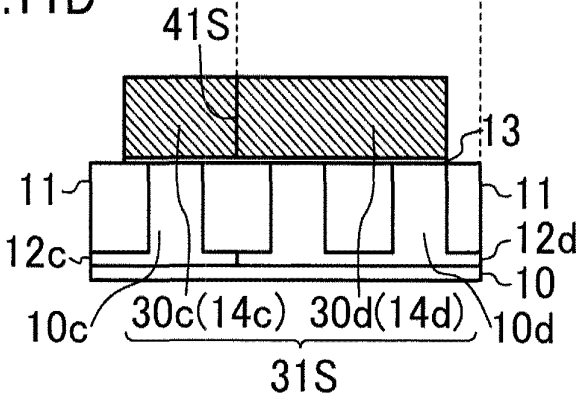


FIG.11D



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FIG.12A

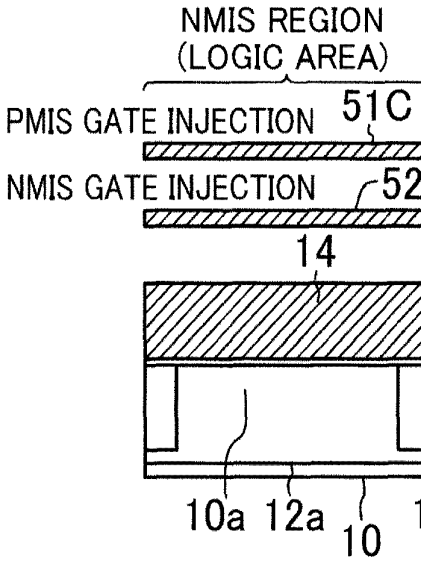


FIG.12B

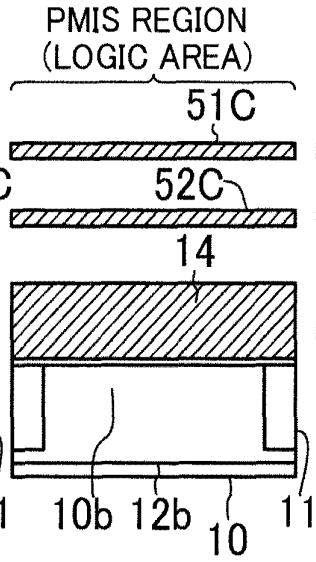


FIG.12C

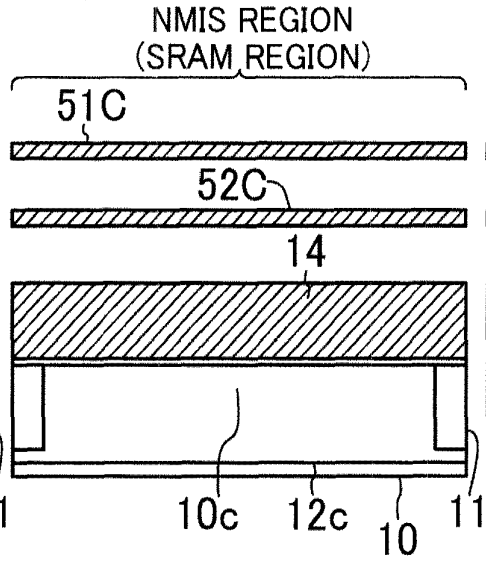
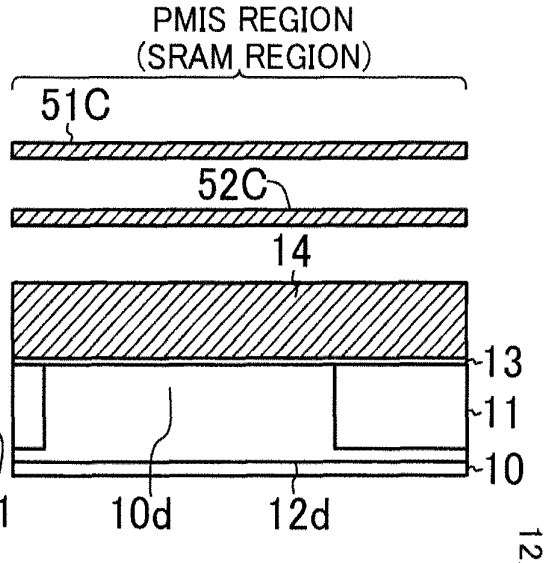


FIG.12D



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FIG.12E LOGIC AREA

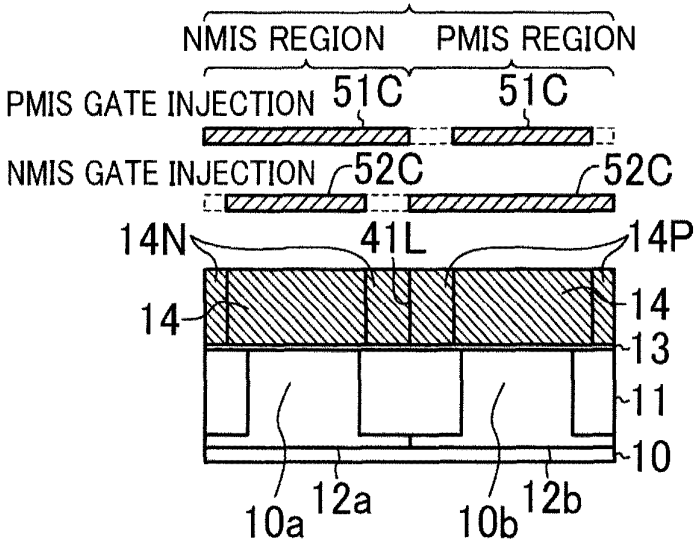


FIG.12F SRAM REGION

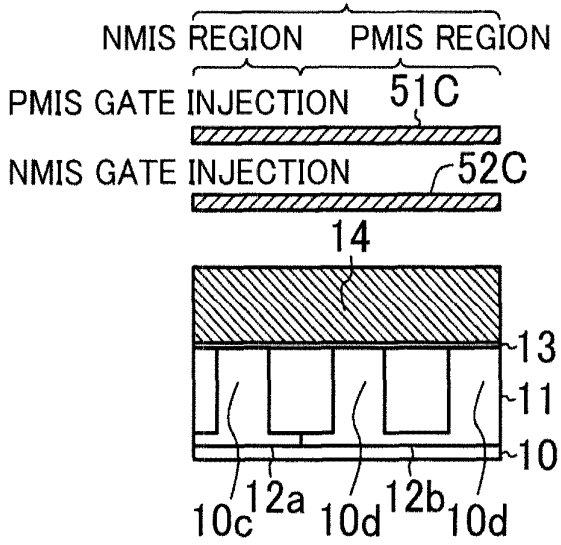


FIG.13A

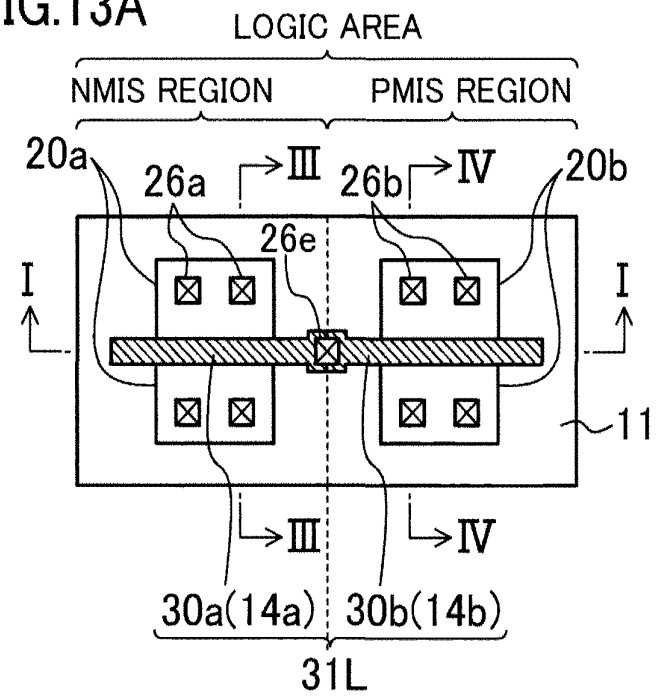


FIG.13B

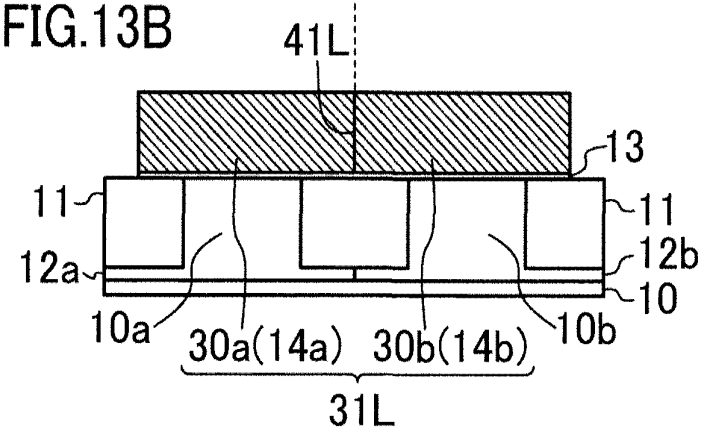


FIG.13C

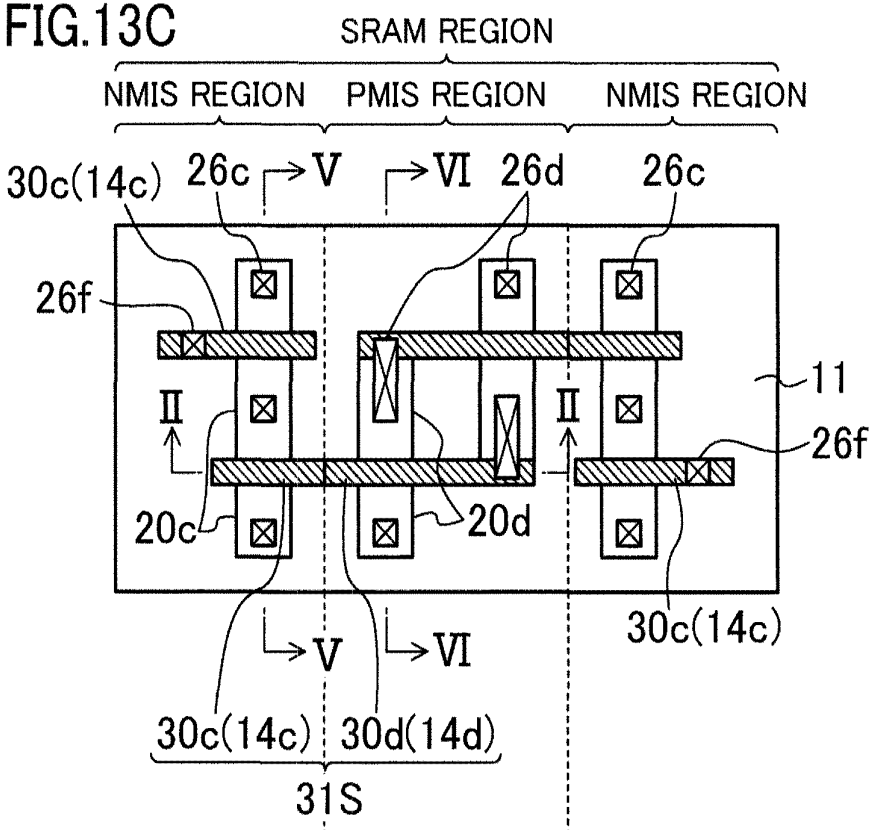
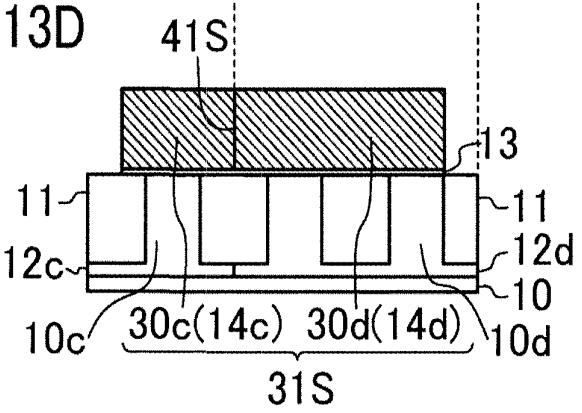
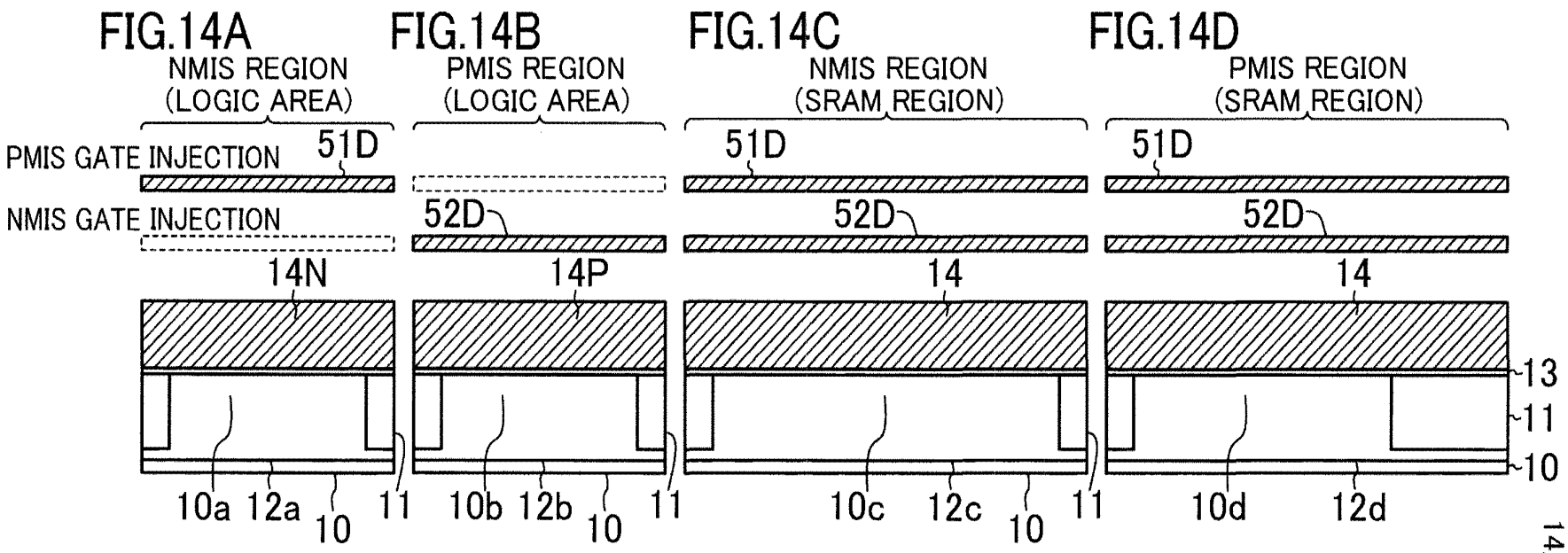
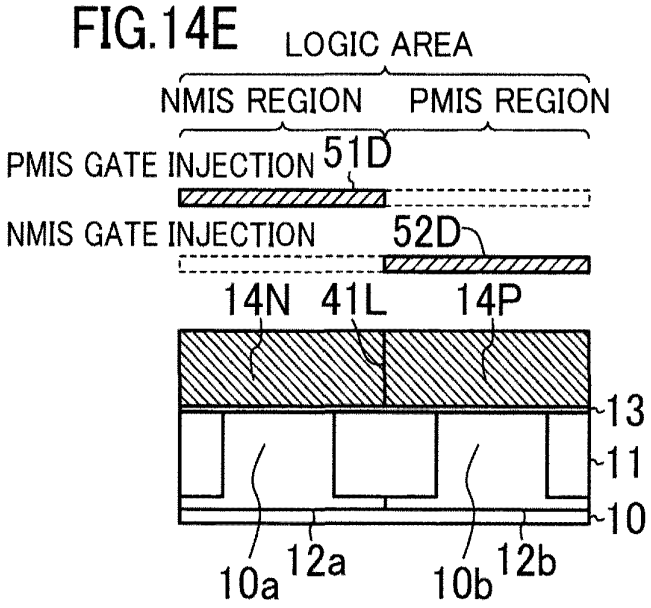


FIG.13D



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FIG.14A
NMIS REGION
(LOGIC AREA)
PMIS GATE INJECTION
51D
NMIS GATE INJECTION
14N
10a
12a
10
11
FIG.14B
PMIS REGION
(LOGIC AREA)
52D
14P
10b
12b
10
11
FIG.14C
NMIS REGION
(SRAM REGION)
51D
52D
14
10c
12c
10
11
FIG.14D
PMIS REGION
(SRAM REGION)
51D
52D
14
10d
12d
13
11
10


FIG.14E
LOGIC AREA
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
51D
NMIS GATE INJECTION
52D
14N
41L
14P
13
11
10
10a
12a
10b
12b

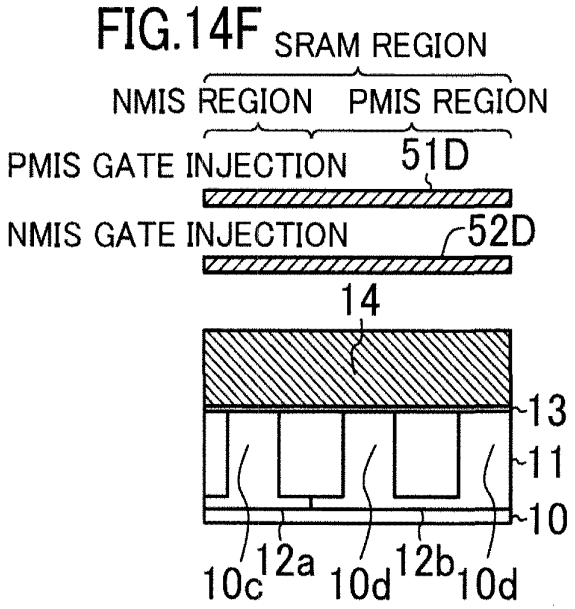

FIG.14F
SRAM REGION
NMIS REGION
PMIS REGION
PMIS GATE INJECTION
51D
NMIS GATE INJECTION
52D
14
13
11
10
10c
12a
10d
12b
10d

FIG.15A
PRIOR ART

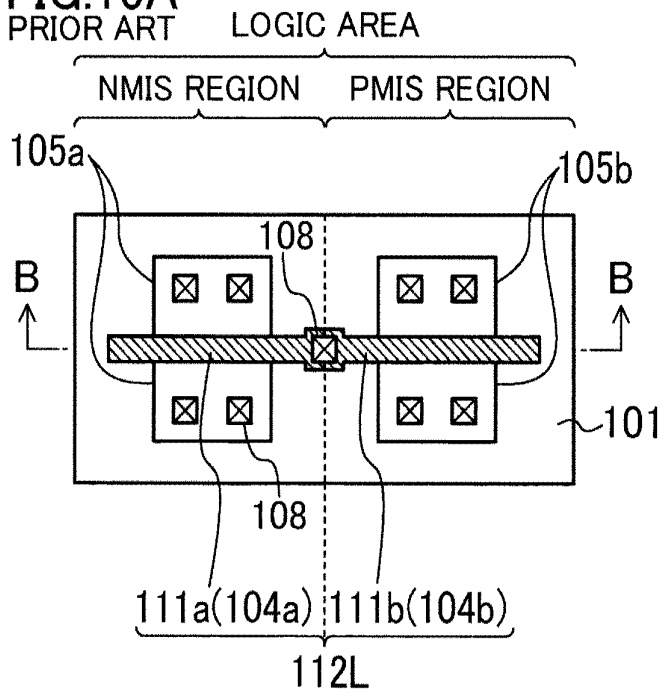


FIG.15B
PRIOR ART

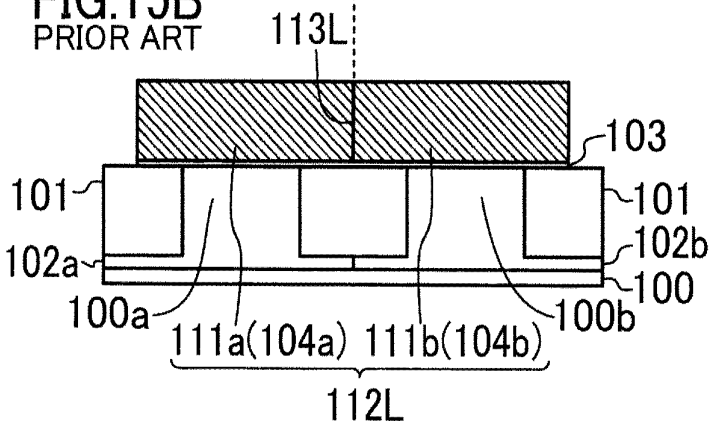


FIG.15C
PRIOR ART

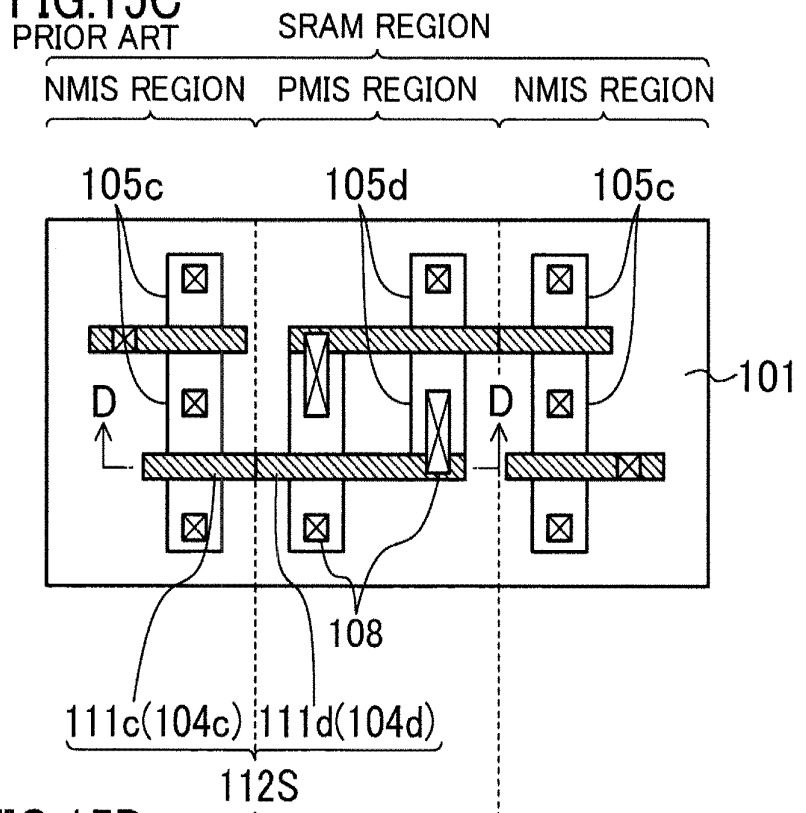
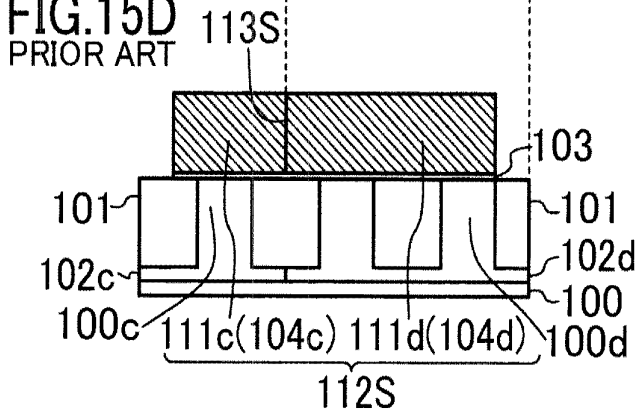


FIG.15D
PRIOR ART



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FIG.16A
PRIOR ART

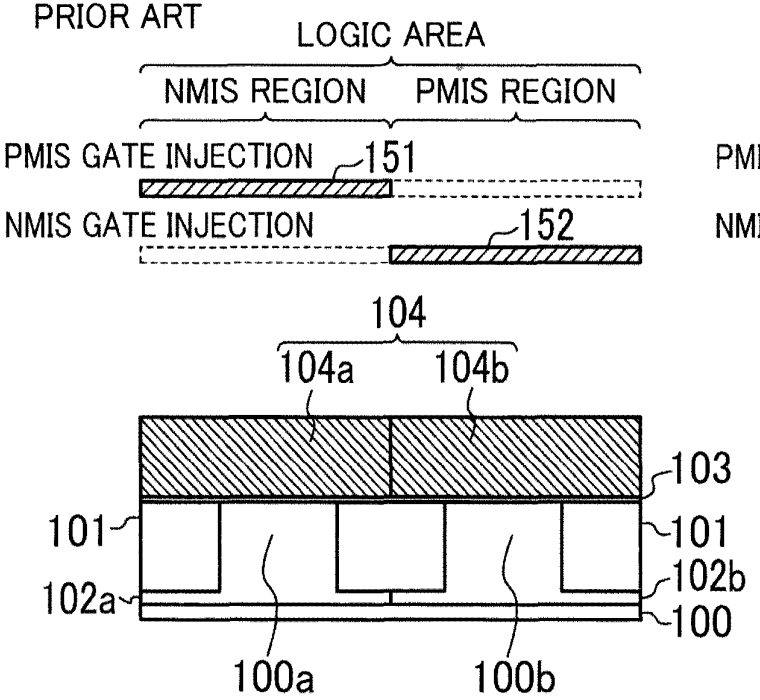
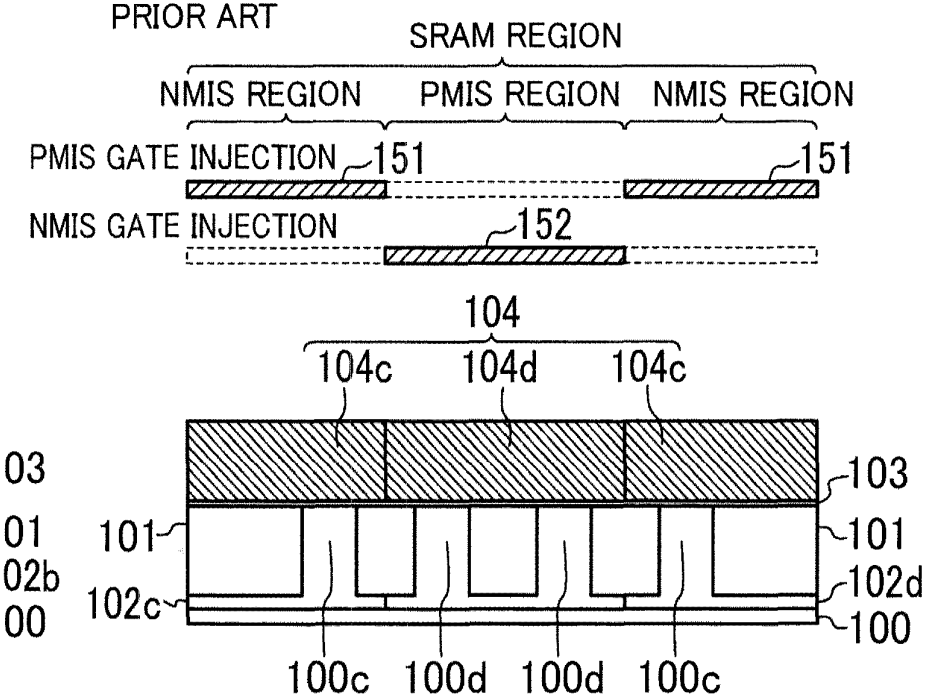


FIG.16B
PRIOR ART



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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Filer:	Michael E. Fogarty/Shante Morgan
Attorney Docket Number:	085393-0935

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	390	390
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1260**

Electronic Acknowledgement Receipt

EFS ID:	14118407
Application Number:	13665376
International Application Number:	
Confirmation Number:	4442
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Customer Number:	53080
Filer:	Michael E. Fogarty/Shante Morgan
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0935
Receipt Date:	31-OCT-2012
Filing Date:	
Time Stamp:	17:10:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1260
RAM confirmation Number	4712
Deposit Account	500417
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P615651-01_TRN_085393-0935.PDF	866568 c31e02ca2272d517232a3a36ace573cc8472be77	yes	22

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal of New Application	1	3
Transmittal Letter	4	5
Information Disclosure Statement (IDS) Form (SB08)	6	6
Non Patent Literature	7	10
Miscellaneous Incoming Letter	11	22

Warnings:					
Information:					
2	Application Data Sheet	ADS_085393-0935.pdf	1882351 7b0e6037ccda2d345c6de1567356df4f643da8a1	no	6
Warnings:					
Information:					
3	Foreign Reference	JP6-275788.PDF	257161 b2d6d5d3665ea5ebd672713b6c651a8f6668d59d	no	7
Warnings:					
Information:					
4	Foreign Reference	JP8-017934.PDF	300523 aff0be490b64ec24ce0b280d3dee79d067182e01	no	7
Warnings:					
Information:					
5	Foreign Reference	JP2010-067912.PDF	445781 d7a3720af2489e4cba7aa6cda7eaeccb1b152dbd	no	14
Warnings:					
Information:					
6		P615651-01_SPEC_085393-0935.PDF	546256 fe84372f4cc099cf04fa41af67f9dd99d4282138	yes	52

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	46	
	Claims		47	51	
	Abstract		52	52	
Warnings:					
Information:					
7		P615651-01_POA_DEC_085393-0935.PDF	313829 310ee82b9edad6a3745c8ab43b50d2bdc16c9372	yes	5
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Power of Attorney		1	2	
	Oath or Declaration filed		3	5	
Warnings:					
Information:					
8	Drawings-only black and white line drawings	P615651-01_DRW_085393-0935.PDF	495937 3c341b5931ac690b833b28831fe923aed0c6f242	no	16
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	32815 46bb6cf2cd6aa5797ad37db7c65756bd223d9497	no	2
Warnings:					
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			Total Files Size (in bytes):	5141221	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/665,376	10/31/2012	2811	1260	085393-0935	16	1

CONFIRMATION NO. 4442

53080
MCDERMOTT WILL & EMERY LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

FILING RECEIPT



Date Mailed: 11/27/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Yoshihiro SATO, Toyama, JAPAN;
Hideyuki ARAI, Toyama, JAPAN;
Takayuki YAMADA, Toyama, JAPAN;

Applicant(s)

Panasonic Corporation, Osaka, JAPAN

Assignment For Published Patent Application

PANASONIC CORPORATION, Osaka, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 53080

Domestic Priority data as claimed by applicant

This application is a CON of PCT/JP2011/006167 11/04/2011

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
JAPAN 2011-068131 03/25/2011

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 11/20/2012
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/665,376**

Projected Publication Date: 03/07/2013

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICE

Preliminary Class

257

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/665,376

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	390
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	16 minus 20 =	*			OR	x 62 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1260

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935

CONFIRMATION NO. 4442

53080
MCDERMOTT WILL & EMERY LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

POA ACCEPTANCE LETTER

OC000000057721303

Date Mailed: 11/27/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/31/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hngo/

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

出　願　年　月　日
Date of Application:　２０１１年　３月２５日

出　願　番　号
Application Number:　特願２０１１－０６８１３１

パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is　ＪＰ２０１１－０６８１３１

出　願　人
Applicant(s):　パナソニック株式会社

２０１２年１２月２０日

特許庁長官
Commissioner,
Japan Patent Office　深野弘行

【書類名】　特許願
【整理番号】　P60603801
【あて先】　特許庁長官　殿
【国際特許分類】　H01L 27/092
【発明者】
　【住所又は居所】　大阪府門真市大字門真１００６番地　パナソニック株式会社内
　【氏名】　佐藤　好弘
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【書類名】明細書
【発明の名称】半導体装置及びその製造方法
【技術分野】
【０００１】
本発明は、半導体装置及びその製造方法に関し、特に、ＣＭＩＳ（Complementary Metal Insulator Semiconductor ）デュアルゲート構造を有する半導体装置及びその製造方法に関する。
【背景技術】
【０００２】
半導体集積回路の高集積化は、デュアルゲート構造を有するＣＭＩＳデバイスの微細化によって実現されてきた。デュアルゲート構造のＣＭＩＳデバイスとは、一般的には、ＮチャネルＭＩＳＦＥＴ（Metal Insulator Semiconductor Field Effect Transistor ）（以下、ＮＭＩＳＦＥＴと称する）のゲート電極としてＮ型不純物がドープされたポリシリコン膜を用い、且つＰチャネルＭＩＳＦＥＴ（以下、ＰＭＩＳＦＥＴと称する）のゲート電極としてＰ型不純物がドープされたポリシリコン膜を用いたデバイスを意味する（例えば特許文献１参照）。デュアルゲート構造のＣＭＩＳデバイスでは、Ｎ型のポリシリコンゲート電極とＰ型のポリシリコンゲート電極とを接続する為に、ポリシリコンゲート電極上に金属シリサイド層が形成される。その場合、ポリシリコンゲート電極におけるＮ型領域とＰ型領域との境界では各領域中の不純物が金属シリサイド層又はポリシリコン膜を通じて相互拡散し、その結果、各ゲート電極の仕事関数が変化して各ＦＥＴの閾値電圧が変動する。
【０００３】
ゲート電極用のポリシリコン膜にＮ型領域及びＰ型領域を形成する方法として、従来、Ｎ型領域とＰ型領域との境界がウェル領域同士の間の分離上に位置するように設定されたマスクを用いて、ゲート電極用のポリシリコン膜に不純物のイオン注入を行っている（例えば特許文献２参照）。
【０００４】
ロジック（Ｌｏｇｉｃ）回路用トランジスタ及びＳＲＡＭ（static random access memory ）回路用トランジスタのそれぞれのゲート電極にイオン注入を用いてＮ型領域及びＰ型領域を形成した従来の半導体装置について、図面を参照しながら説明する。
【０００５】
図１５（ａ）は、従来の半導体装置におけるロジック領域の平面図であり、図１５（ｂ）は、図１５（ａ）におけるＢ－Ｂ線（ゲート幅方向）の断面図である。また、図１５（ｃ）は、従来の半導体装置におけるＳＲＡＭ領域の平面図であり、図１５（ｄ）は、図１５（ｃ）におけるＤ－Ｄ線（ゲート幅方向）の断面図である。尚、説明を簡単にするために、図１５（ａ）～（ｄ）においてサイドウォールスペーサ、シリサイド層及び層間膜等の図示を省略していると共に、図１５（ｂ）及び（ｄ）においてコンタクトの図示を省略している。
【０００６】
図１５（ａ）～（ｄ）に示すように、従来の半導体装置におけるロジック領域及びＳＲＡＭ領域はそれぞれ、ＮＭＩＳ領域及びＰＭＩＳ領域を有している。ロジック領域のＮＭＩＳ領域においては、半導体基板１００上にＰ型ウェル領域１０２ａが設けられていると共に素子分離領域１０１に囲まれるように活性領域１００ａが設けられている。ロジック領域のＰＭＩＳ領域においては、半導体基板１００上にＮ型ウェル領域１０２ｂが設けられていると共に素子分離領域１０１に囲まれるように活性領域１００ｂが設けられている。ＳＲＡＭ領域のＮＭＩＳ領域においては、半導体基板１００上にＰ型ウェル領域１０２ｃが設けられていると共に素子分離領域１０１に囲まれるように活性領域１００ｃが設けられている。ＳＲＡＭ領域のＰＭＩＳ領域においては、半導体基板１００上にＮ型ウェル領域１０２ｄが設けられていると共に素子分離領域１０１に囲まれるように活性領域１００ｄが設けられている。

【０００７】
活性領域１００ａ上にはゲート絶縁膜１０３を介してＮ型ポリシリコン膜１０４ａを有するゲート電極１１１ａが形成されている。活性領域１００ｂ上にはゲート絶縁膜１０３を介してＰ型ポリシリコン膜１０４ｂを有するゲート電極１１１ｂが形成されている。ゲート電極１１１ａとゲート電極１１１ｂとは、活性領域１００ａと活性領域１００ｂとの間の素子分離領域１０１上に位置するＰＮ境界１１３Ｌで互いに接続されており、これにより、デュアルゲート電極１１２Ｌが構成されている。活性領域１００ａにおけるゲート電極１１１ａの両側にはＮ型ソース／ドレイン領域１０５ａが設けられていると共に、活性領域１００ｂにおけるゲート電極１１１ｂの両側にはＰ型ソース／ドレイン領域１０５ｂが設けられている。デュアルゲート電極１１２Ｌ、Ｎ型ソース／ドレイン領域１０５ａ及びＰ型ソース／ドレイン領域１０５ｂのそれぞれと接続するようにコンタクト１０８が形成されている。
【０００８】
活性領域１００ｃ上にはゲート絶縁膜１０３を介してＮ型ポリシリコン膜１０４ｃを有するゲート電極１１１ｃが形成されている。活性領域１００ｄ上にはゲート絶縁膜１０３を介してＰ型ポリシリコン膜１０４ｄを有するゲート電極１１１ｄが形成されている。ゲート電極１１１ｃとゲート電極１１１ｄとは、活性領域１００ｃと活性領域１００ｄとの間の素子分離領域１０１上に位置するＰＮ境界１１３Ｓで互いに接続されており、これにより、デュアルゲート電極１１２Ｓが構成されている。活性領域１００ｃにおけるゲート電極１１１ｃの両側にはＮ型ソース／ドレイン領域１０５ｃが設けられていると共に、活性領域１００ｄにおけるゲート電極１１１ｄの両側にはＰ型ソース／ドレイン領域１０５ｄが設けられている。デュアルゲート電極１１２Ｓ、Ｎ型ソース／ドレイン領域１０５ｃ及びＰ型ソース／ドレイン領域１０５ｄのそれぞれと接続するようにコンタクト１０８が形成されている。
【０００９】
図１６（ａ）及び（ｂ）は、デュアルゲート電極１１２Ｌ及び１１２Ｓとなるポリシリコン膜（ゲートパターニング前）に不純物をイオン注入することによってＰ型領域及びＮ型領域を形成する様子を模式的に示す図である。尚、図１６（ａ）及び（ｂ）において、図１５（ａ）～（ｄ）と同じ構成要素には同じ符号を付している。
【００１０】
図１６（ａ）及び（ｂ）に示すように、ＰＭＩＳ領域のゲート注入の際には、ロジック領域及びＳＲＡＭ領域のそれぞれのＮＭＩＳ領域を覆うマスクパターン１５１を用いてポリシリコン膜１０４にＰ型不純物をイオン注入することによってＰ型ポリシリコン膜１０４ｂ及び１０４ｄを形成する。すなわち、Ｐ型ポリシリコン膜１０４ｂ及び１０４ｄのそれぞれにおけるＰ型不純物濃度は実質的に同じである。また、ＮＭＩＳ領域のゲート注入の際には、ロジック領域及びＳＲＡＭ領域のそれぞれのＰＭＩＳ領域を覆うマスクパターン１５２を用いてポリシリコン膜１０４にＮ型不純物をイオン注入することによってＮ型ポリシリコン膜１０４ａ及び１０４ｃを形成する。すなわち、Ｎ型ポリシリコン膜１０４ａ及び１０４ｃのそれぞれにおけるＮ型不純物濃度は実質的に同じである。尚、説明を分かりやすくするために、マスクパターン１５１及び１５２として、イオン注入に実際に用いられるレジストパターンではなく、当該レジストパターンを形成するためのフォトマスク上のマスクパターンを模式的に示している。また、マスクパターン１５１及び１５２は、ポリシリコン膜１０４中に形成されるＰＮ境界が、活性領域１００ａと活性領域１００ｂとの間の素子分離領域１０１上、及び活性領域１００ｃと活性領域１００ｄとの間の素子分離領域１０１上にそれぞれ位置するように設定されている。
【００１１】
尚、図示はしていないが、ＰＭＩＳ領域及びＮＭＩＳ領域のそれぞれにおいてソース／ドレイン領域を形成するためのイオン注入においても、図１６（ａ）及び（ｂ）に示すマスクパターン１５１及び１５２と同様のマスクパターンを用いる。
【００１２】

図１６（ａ）及び（ｂ）に示すゲート注入によると、ポリシリコン膜１０４に形成されるＰＮ境界が活性領域同士の間の素子分離領域上に位置するため、ポリシリコンゲート電極におけるＮ型領域とＰ型領域との間の不純物の相互拡散に起因する各ＦＥＴの特性劣化を抑制することができる。

【先行技術文献】

【特許文献】

【００１３】

【特許文献１】特開平６－２７５７８８号公報

【特許文献２】特開平８－１７９３４号公報

【発明の概要】

【発明が解決しようとする課題】

【００１４】

しかしながら、素子の微細化に伴ってゲート長が短くなると、ポリシリコン膜中での相互拡散の問題とは別に、注入不純物であるイオン種の違いに起因するポリシリコン膜のエッチング速度の差が相対的に大きくなり、その結果、ゲート長の仕上がり寸法が変動してトランジスタの閾値電圧が変動するという問題が顕在化してくる。従って、特にセルサイズの縮小を要求されるＳＲＡＭ等においてはＰＮ境界近傍で発生するゲート寸法の変動を抑制する必要がある。

【００１５】

また、前述の従来技術のように、ポリシリコンゲート電極中のＰＮ境界を活性領域同士の間の素子分離領域上に位置させたとしても、素子の微細化が進むにつれて、特にＳＲＡＭ等においては素子分離領域の幅が狭くなるので、ポリシリコンゲート電極におけるＮ型領域とＰ型領域との間の不純物の相互拡散の影響が無視できなくなる。その結果、各ゲート電極の仕事関数が変化するため、閾値電圧の変動等のトランジスタ特性の劣化が起こるので、回路動作不良が発生し易くなるという問題が生じてしまう。

【００１６】

前記に鑑み、本発明は、ＣＭＩＳデュアルゲート構造を有する半導体装置において、ＰＮ境界近傍でのゲート寸法変動や不純物の相互拡散に起因する素子特性の変動を抑制できるようにすることを目的とする。

【課題を解決するための手段】

【００１７】

前記の目的を達成するために、本発明に係る半導体装置は、第１のデュアルゲート電極と第２のデュアルゲート電極とを備えた半導体装置であって、前記第１のデュアルゲート電極は、第１の活性領域上に形成された第１の第１導電型シリコン膜を含む第１のゲート電極と、第２の活性領域上に形成された第１の第２導電型シリコン膜を含む第２のゲート電極とを有し、前記第２のデュアルゲート電極は、第３の活性領域上に形成された第２の第１導電型シリコン膜を含む第３のゲート電極と、第４の活性領域上に形成された第２の第２導電型シリコン膜を含む第４のゲート電極とを有し、前記第１の活性領域と前記第２の活性領域とは素子分離領域を挟んで分離されており、前記第１のゲート電極と前記第２のゲート電極とは前記素子分離領域上で接続しており、前記第１の第１導電型シリコン膜の少なくとも一部分における第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度よりも高い。

【００１８】

本発明に係る半導体装置において、前記第１の活性領域と前記第２の活性領域との間の分離幅は、前記第３の活性領域と前記第４の活性領域との間の分離幅よりも大きくてもよい。

【００１９】

本発明に係る半導体装置において、前記第１の第２導電型シリコン膜の少なくとも一部分における第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度と実質的に同じであってもよい。

【００２０】
本発明に係る半導体装置において、前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度よりも高くてもよい。
【００２１】
本発明に係る半導体装置において、前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度よりも低くてもよい。
【００２２】
本発明に係る半導体装置において、前記第１の活性領域及び前記素子分離領域のそれぞれの上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記第３の活性領域の上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度よりも高くてもよい。
【００２３】
本発明に係る半導体装置において、前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度よりも低くてもよい。
【００２４】
本発明に係る半導体装置において、前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度よりも低くてもよい。
【００２５】
本発明に係る半導体装置において、前記素子分離領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度と実質的に同じであってもよい。
【００２６】
本発明に係る半導体装置において、前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度と実質的に同じであってもよい。
【００２７】
本発明に係る半導体装置において、前記素子分離領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度よりも高くてもよい。
【００２８】
本発明に係る半導体装置において、前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度と実質的に同じであってもよい。
【００２９】
本発明に係る半導体装置において、前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度よりも低くてもよい。
【００３０】
本発明に係る半導体装置において、前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度と実質的に同じであってもよい。
【００３１】

本発明に係る半導体装置において、前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度よりも低くてもよい。

【００３２】

本発明に係る半導体装置において、前記素子分離領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度よりも高くてもよい。

【００３３】

本発明に係る半導体装置において、前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度よりも高く、前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度よりも高くてもよい。

【００３４】

本発明に係る半導体装置において、前記第１のゲート電極は、第１のＰＭＩＳトランジスタのゲート電極であり、前記第２のゲート電極は、第１のＮＭＩＳトランジスタのゲート電極であり、前記第３のゲート電極は、第２のＰＭＩＳトランジスタのゲート電極であり、前記第４のゲート電極は、第２のＮＭＩＳトランジスタのゲート電極であってもよい。

【００３５】

本発明に係る半導体装置において、前記第１のゲート電極及び前記第２のゲート電極はそれぞれ、ロジック回路用トランジスタのゲート電極であり、前記第３のゲート電極及び前記第４のゲート電極はそれぞれ、ＳＲＡＭ回路用トランジスタのゲート電極であってもよい。

【００３６】

また、本発明に係る半導体装置の製造方法は、第１の活性領域上に形成された第１のゲート電極及び第２の活性領域上に形成された第２のゲート電極を有する第１のデュアルゲート電極と、第３の活性領域上に形成された第３のゲート電極及び第４の活性領域上に形成された第４のゲート電極を有する第２のデュアルゲート電極とを備えた半導体装置の製造方法であって、前記第１の活性領域、前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上にシリコン膜を形成する工程（ａ）と、前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に位置する部分の前記シリコン膜を第１のマスクパターンによって覆いながら、前記シリコン膜に第１導電型不純物を導入する工程（ｂ）と、前記第１の活性領域上に位置する部分の前記シリコン膜を第２のマスクパターンによって覆いながら、前記シリコン膜に第２導電型不純物を導入する工程（ｃ）と、前記工程（ｂ）及び前記工程（ｃ）よりも後に、前記シリコン膜をパターニングし、それにより、前記第１の活性領域、前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に、前記シリコン膜をそれぞれ含む前記第１のゲート電極、前記第２のゲート電極、前記第３のゲート電極及び前記第４のゲート電極を形成する工程（ｄ）とを備えている。尚、本発明に係る半導体装置の製造方法において、前記工程（ｂ）及び前記工程（ｃ）のいずれを先に実施してもよい。

【００３７】

本発明に係る半導体装置の製造方法において、前記第１のマスクパターンは、前記第１の活性領域上に位置する部分の前記シリコン膜上に開口を有し、前記第２のマスクパターンは、前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に位置する部分の前記シリコン膜上に開口を有していてもよい。

【００３８】

本発明に係る半導体装置の製造方法において、前記第１の活性領域と前記第２の活性領域とは素子分離領域によって電気的に分離されており、前記工程（ａ）において、前記シ

リコン膜は前記素子分離領域上にも形成され、前記第１のマスクパターンは、前記第１の活性領域上に位置する部分の前記シリコン膜を覆うと共に前記素子分離領域上に位置する部分の前記シリコン膜上に開口を有し、前記第２のマスクパターンは、前記第２の活性領域上に位置する部分の前記シリコン膜を覆うと共に前記素子分離領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に位置する部分の前記シリコン膜上に開口を有していてもよい。ここで、前記第１のマスクパターン及び前記第２のマスクパターンは、前記素子分離領域上に位置する部分の前記シリコン膜上に開口を有していなくてもよい。言い換えると、前記第１のマスクパターン及び前記第２のマスクパターンは、前記素子分離領域上に位置する部分の前記シリコン膜を覆っていてもよい。

【００３９】

本発明に係る半導体装置の製造方法において、前記第１の活性領域と前記第２の活性領域とは素子分離領域によって電気的に分離されており、前記工程（ａ）において、前記シリコン膜は前記素子分離領域上にも形成され、前記第１のマスクパターンは、前記第１の活性領域上に位置する部分の前記シリコン膜を覆うと共に前記素子分離領域上に位置する部分の前記シリコン膜上に開口を有し、前記第２のマスクパターンは、前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に位置する部分の前記シリコン膜を覆うと共に前記素子分離領域上に位置する部分の前記シリコン膜上に開口を有していてもよい。

【００４０】

本発明に係る半導体装置の製造方法において、前記第２のマスクパターンは、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に位置する部分の前記シリコン膜を覆っていてもよい。

【発明の効果】

【００４１】

本発明によると、ＣＭＩＳデュアルゲート構造を有する半導体装置において、ＰＮ境界近傍でのゲート寸法変動や不純物の相互拡散に起因する素子特性の変動を抑制することができる。

【図面の簡単な説明】

【００４２】

【図１】図１（ａ）は、第１の実施形態に係る半導体装置におけるロジック領域の平面図であり、図１（ｂ）は、図１（ａ）におけるＩ－Ｉ線の断面図であり、図１（ｃ）は、第１の実施形態に係る半導体装置におけるＳＲＡＭ領域の平面図であり、図１（ｄ）は、図１（ｃ）におけるII－II線の断面図である。

【図２】図２（ａ）～（ｆ）は、第１の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。

【図３】図３（ａ）～（ｆ）は、第１の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。

【図４】図４（ａ）～（ｆ）は、第１の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。

【図５】図５（ａ）～（ｆ）は、第１の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。

【図６】図６（ａ）～（ｆ）は、第１の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。

【図７】図７（ａ）～（ｆ）は、第１の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。

【図８】図８（ａ）～（ｆ）は、第１の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。

【図９】図９（ａ）は、第２の実施形態に係る半導体装置におけるロジック領域の平面図であり、図９（ｂ）は、図９（ａ）におけるＩ－Ｉ線の断面図であり、図９（ｃ）は、第２の実施形態に係る半導体装置におけるＳＲＡＭ領域の平面図であり、図９

（ｄ）は、図９（ｃ）におけるII－II線の断面図である。
【図１０】図１０（ａ）～（ｆ）は、第２の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。
【図１１】図１１（ａ）は、第３の実施形態に係る半導体装置におけるロジック領域の平面図であり、図１１（ｂ）は、図１１（ａ）におけるＩ－Ｉ線の断面図であり、図１１（ｃ）は、第３の実施形態に係る半導体装置におけるＳＲＡＭ領域の平面図であり、図１１（ｄ）は、図１１（ｃ）におけるII－II線の断面図である。
【図１２】図１２（ａ）～（ｆ）は、第３の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。
【図１３】図１３（ａ）は、第４の実施形態に係る半導体装置におけるロジック領域の平面図であり、図１３（ｂ）は、図１３（ａ）におけるＩ－Ｉ線の断面図であり、図１３（ｃ）は、第４の実施形態に係る半導体装置におけるＳＲＡＭ領域の平面図であり、図１３（ｄ）は、図１３（ｃ）におけるII－II線の断面図である。
【図１４】図１４（ａ）～（ｆ）は、第４の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。
【図１５】図１５（ａ）は、従来の半導体装置におけるロジック領域の平面図であり、図１５（ｂ）は、図１５（ａ）におけるＢ－Ｂ線の断面図であり、図１５（ｃ）は、従来の半導体装置におけるＳＲＡＭ領域の平面図であり、図１５（ｄ）は、図１５（ｃ）におけるＤ－Ｄ線の断面図である。
【図１６】図１６（ａ）及び（ｂ）は、従来の半導体装置の製造方法においてデュアルゲート電極となるポリシリコン膜（ゲートパターニング前）に不純物をイオン注入することによってＰ型領域及びＮ型領域を形成する様子を模式的に示す図である。

【発明を実施するための形態】

【００４３】

（第１の実施形態）

以下、本発明の第１の実施形態に係る半導体装置について、図面を参照しながら説明する。

【００４４】

図１（ａ）は、第１の実施形態に係る半導体装置におけるロジック領域の平面図であり、図１（ｂ）は、図１（ａ）におけるＩ－Ｉ線（ゲート幅方向）の断面図である。また、図１（ｃ）は、第１の実施形態に係る半導体装置におけるＳＲＡＭ領域の平面図であり、図１（ｄ）は、図１（ｃ）におけるII－II線（ゲート幅方向）の断面図である。尚、説明を簡単にするために、図１（ａ）～（ｄ）においてサイドウォールスペーサ、シリサイド層及び層間膜等の図示を省略していると共に、図１（ｂ）及び（ｄ）においてコンタクトの図示を省略している。

【００４５】

図１（ａ）～（ｄ）に示すように、本実施形態の半導体装置は、ロジック回路が形成される領域（以下、ロジック領域と称する）及びＳＲＡＭ回路が形成される領域（以下、ＳＲＡＭ領域と称する）を有しており、ロジック領域及びＳＲＡＭ領域はそれぞれ、ＮＭＩＳＦＥＴが形成される領域（以下、ＮＭＩＳ領域と称する）及びＰＭＩＳＦＥＴが形成される領域（以下、ＰＭＩＳ領域と称する）を有している。ロジック領域のＮＭＩＳ領域においては、半導体基板１０上にＰ型ウェル領域１２ａが設けられていると共に素子分離領域１１に囲まれるように活性領域１０ａが設けられている。ロジック領域のＰＭＩＳ領域においては、半導体基板１０上にＮ型ウェル領域１２ｂが設けられていると共に素子分離領域１１に囲まれるように活性領域１０ｂが設けられている。ＳＲＡＭ領域のＮＭＩＳ領域においては、半導体基板１０上にＰ型ウェル領域１２ｃが設けられていると共に素子分離領域１１に囲まれるように活性領域１０ｃが設けられている。ＳＲＡＭ領域のＰＭＩＳ領域においては、半導体基板１０上にＮ型ウェル領域１２ｄが設けられていると共に素子分離領域１１に囲まれるように活性領域１０ｄが設けられている。

【００４６】

活性領域１０ａ上にはゲート絶縁膜１３を介してＮ型シリコン膜１４ａを有するゲート電極３０ａが形成されている。活性領域１０ｂ上にはゲート絶縁膜１３を介してＰ型シリコン膜１４ｂを有するゲート電極３０ｂが形成されている。ゲート電極３０ａとゲート電極３０ｂとは、活性領域１０ａと活性領域１０ｂとの間の素子分離領域１１上に位置するＰＮ境界４１Ｌで互いに接続されており、これにより、デュアルゲート電極３１Ｌが構成されている。活性領域１０ａにおけるゲート電極３０ａの両側にはＮ型ソース／ドレイン領域２０ａが設けられていると共に、活性領域１０ｂにおけるゲート電極３０ｂの両側にはＰ型ソース／ドレイン領域２０ｂが設けられている。Ｎ型ソース／ドレイン領域２０ａ及びＰ型ソース／ドレイン領域２０ｂのそれぞれと接続するようにコンタクト２６ａ及び２６ｂが形成されていると共に、デュアルゲート電極３１Ｌと接続するようにコンタクト２６ｅが形成されている。

【００４７】

活性領域１０ｃ上にはゲート絶縁膜１３を介してＮ型シリコン膜１４ｃを有するゲート電極３０ｃが形成されている。活性領域１０ｄ上にはゲート絶縁膜１３を介してＰ型シリコン膜１４ｄを有するゲート電極３０ｄが形成されている。ゲート電極３０ｃとゲート電極３０ｄとは、活性領域１０ｃと活性領域１０ｄとの間の素子分離領域１１上に位置するＰＮ境界４１Ｓで互いに接続されており、これにより、デュアルゲート電極３１Ｓが構成されている。活性領域１０ｃにおけるゲート電極３０ｃの両側にはＮ型ソース／ドレイン領域２０ｃが設けられていると共に、活性領域１０ｄにおけるゲート電極３０ｄの両側にはＰ型ソース／ドレイン領域２０ｄが設けられている。Ｎ型ソース／ドレイン領域２０ｃ及びＰ型ソース／ドレイン領域２０ｄのそれぞれと接続するようにコンタクト２６ｃ及び２６ｄが形成されていると共に、ゲート電極３０ｃと接続するようにコンタクト２６ｆが形成されている。

【００４８】

本実施形態の特徴として、Ｐ型シリコン膜１４ｂ全体のＰ型不純物濃度は、Ｐ型シリコン膜１４ｄ全体のＰ型不純物濃度よりも高い。

【００４９】

尚、Ｎ型シリコン膜１４ａのＮ型不純物濃度は、Ｎ型シリコン膜１４ｃのＮ型不純物濃度と実質的に同じである。また、ロジック領域の素子分離領域１１（具体的には活性領域１０ａと活性領域１０ｂとの間の素子分離領域１１）の幅が例えば７０ｎｍ程度以上であるのに対して、ＳＲＡＭ領域の素子分離領域１１（具体的には活性領域１０ｃと活性領域１０ｄとの間の素子分離領域１１）の幅は例えば３０～６０ｎｍ程度である。

【００５０】

以下、本発明の第１の実施形態に係る半導体装置の製造方法について、図面を参照しながら説明する。

【００５１】

図２（ａ）～（ｆ）、図３（ａ）～（ｆ）、図４（ａ）～（ｆ）、図５（ａ）～（ｆ）、図６（ａ）～（ｆ）、図７（ａ）～（ｆ）及び図８（ａ）～（ｆ）は、第１の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。尚、図２（ａ）、図３（ａ）、図４（ａ）、図５（ａ）、図６（ａ）、図７（ａ）及び図８（ａ）は、図１（ａ）におけるIII－III線（ゲート長方向）の断面構成を各工程毎に示したものであり、図２（ｂ）、図３（ｂ）、図４（ｂ）、図５（ｂ）、図６（ｂ）、図７（ｂ）及び図８（ｂ）は、図１（ａ）におけるIV－IV線（ゲート長方向）の断面構成を各工程毎に示したものであり、図２（ｃ）、図３（ｃ）、図４（ｃ）、図５（ｃ）、図６（ｃ）、図７（ｃ）及び図８（ｃ）は、図１（ｃ）におけるＶ－Ｖ線（ゲート長方向）の断面構成を各工程毎に示したものであり、図２（ｄ）、図３（ｄ）、図４（ｄ）、図５（ｄ）、図６（ｄ）、図７（ｄ）及び図８（ｄ）は、図１（ｃ）におけるVI－VI線（ゲート長方向）の断面構成を各工程毎に示したものである。また、図２（ｅ）、図３（ｅ）、図４（ｅ）、図５（ｅ）、図６（ｅ）、図７（ｅ）及び図８（ｅ）は、図１（ａ）におけるＩ－Ｉ線（ゲート幅方向）の断面構成を各工程毎に示したものであり、図２（ｆ）、図３（ｆ）、図４（ｆ）、図５（ｆ

）、図６（ｆ）、図７（ｆ）及び図８（ｆ）は、図１（ｃ）におけるII－II線（ゲート幅方向）の断面構成を各工程毎に示したものである。

【００５２】

まず、図２（ａ）～（ｆ）に示すように、例えば埋め込み素子分離（Shallow Trench Isolation（ＳＴＩ））法により、例えばｐ型シリコンからなる半導体基板１０の上部に、トレンチ内に絶縁膜が埋め込まれてなる素子分離領域１１を選択的に形成する。これにより、ロジック領域のＮＭＩＳ領域においては、素子分離領域１１に囲まれた半導体基板１０からなる活性領域１０ａが形成され、ロジック領域のＰＭＩＳ領域においては、素子分離領域１１に囲まれた半導体基板１０からなる活性領域１０ｂが形成され、ＳＲＡＭ領域のＮＭＩＳ領域においては、素子分離領域１１に囲まれた半導体基板１０からなる活性領域１０ｃが形成され、ＳＲＡＭ領域のＰＭＩＳ領域においては、素子分離領域１１に囲まれた半導体基板１０からなる活性領域１０ｄが形成される。その後、例えばリソグラフィ法及びイオン注入法により、半導体基板１０における各ＮＭＩＳ領域に、例えばＢ（ホウ素）等のＰ型不純物を注入する。続いて、例えばリソグラフィ法及びイオン注入法により、半導体基板１０における各ＰＭＩＳ領域に、例えばＰ（リン）等のＮ型不純物を注入する。その後、半導体基板１０に対して、例えば８５０℃、３０秒間の熱処理を施すことにより、ロジック領域のＮＭＩＳ領域においては、半導体基板１０上にＰ型ウェル領域１２ａを形成し、ロジック領域のＰＭＩＳ領域においては、半導体基板１０上にＮ型ウェル領域１２ｂを形成し、ＳＲＡＭ領域のＮＭＩＳ領域においては、半導体基板１０上にＰ型ウェル領域１２ｃを形成し、ＳＲＡＭ領域のＰＭＩＳ領域においては、半導体基板１０上にＮ型ウェル領域１２ｄを形成する。

【００５３】

次に、図３（ａ）～（ｆ）に示すように、例えば希釈フッ酸処理により、半導体基板１０の表面を洗浄した後、例えばＩＳＳＧ（In-Situ Steam Generation）酸化法により、活性領域１０ａ、１０ｂ、１０ｃ及び１０ｄのそれぞれの上に、例えば厚さ２ｎｍ程度のシリコン酸化膜からなるゲート絶縁膜１３を形成する。その後、半導体基板１０に対して、例えば窒素プラズマ処理を行うことにより、ゲート絶縁膜１３の表面を窒化して窒化層（図示省略）を形成する。その後、アニール処理を実施することにより、前記窒化層から、結合の弱い窒素を除去する。続いて、ゲート絶縁膜１３上に、例えばＣＶＤ（chemical vapor deposition ）法により、例えばポリシリコンからなる厚さ１００ｎｍ程度のシリコン膜１４を堆積する。

【００５４】

続いて、図３（ａ）～（ｆ）に示すように、ロジック領域のＮＭＩＳ領域全体及びＳＲＡＭ領域全体（ＮＭＩＳ領域全体及びＰＭＩＳ領域全体）を覆い且つロジック領域のＰＭＩＳ領域全体上に開口を有するマスクパターン５１Ａを用いて、シリコン膜１４に例えばＢ（ホウ素）等のＰ型不純物をドーズ量４×１０^{15}ｃｍ$^{-2}$でイオン注入することによってＰ型シリコン膜１４Ｐを形成する。次に、ロジック領域のＰＭＩＳ領域全体を覆い且つロジック領域のＮＭＩＳ領域全体及びＳＲＡＭ領域全体（ＮＭＩＳ領域全体及びＰＭＩＳ領域全体）のそれぞれの上に開口を有するマスクパターン５２Ａを用いて、シリコン膜１４に例えばＰ（リン）等のＮ型不純物をドーズ量３×１０^{15}ｃｍ$^{-2}$でイオン注入することによってＮ型シリコン膜１４Ｎを形成する。すなわち、本実施形態の特徴として、ＳＲＡＭ領域のＰＭＩＳ領域のゲート注入においてＮ型不純物のイオン注入を行っている。

【００５５】

尚、Ｐ型シリコン膜１４Ｐの形成とＮ型シリコン膜１４Ｎの形成とは、いずれを先に実施してもよい。また、図３（ａ）～（ｆ）においては、説明を分かりやすくするために、マスクパターン５１Ａ及び５２Ａとして、フォトリソグラフィ法により半導体基板１０上に形成されるレジストパターンではなく、当該レジストパターンを形成するためのフォトマスク上のマスクパターンを模式的に示している。また、マスクパターン５１Ａ及び５２Ａは、Ｐ型シリコン膜１４ＰとＮ型シリコン膜１４ＮとのＰＮ境界４１Ｌが、活性領域１０ａと活性領域１０ｂとの間の素子分離領域１１上に位置するように設定されている。

【００５６】
Ｐ型シリコン膜１４Ｐ及びＮ型シリコン膜１４Ｎの形成後、半導体基板１０に対して、例えば８５０℃、３０秒間の熱処理を施すことにより、Ｐ型シリコン膜１４Ｐ及びＮ型シリコン膜１４Ｎのそれぞれにイオン注入された不純物のプロファイル（具体的には基板主面に対して垂直な方向のプロファイル（以下、垂直方向プロファイルと称する））の均一化を行う。
【００５７】
次に、フォトリソグラフィ法により、シリコン膜１４上に、ゲート形状を有するレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとして、ドライエッチング法により、シリコン膜１４をパターニングする。これにより、図４（ａ）～（ｆ）に示すように、活性領域１０ａ上にゲート絶縁膜１３ａを介してＮ型シリコン膜１４ａを含むゲート電極３０ａが形成され、活性領域１０ｂ上にゲート絶縁膜１３ｂを介してＰ型シリコン膜１４ｂを含むゲート電極３０ｂが形成され、活性領域１０ｃ上にゲート絶縁膜１３ｃを介してＮ型シリコン膜１４ｃを含むゲート電極３０ｃが形成され、活性領域１０ｄ上にゲート絶縁膜１３ｄを介してＮ型シリコン膜１４ｄ’を含むゲート電極３０ｄが形成される。ここで、ゲート電極３０ａとゲート電極３０ｂとは、活性領域１０ａと活性領域１０ｂとの間の素子分離領域１１上に位置するＰＮ境界４１Ｌで互いに接続されており、これにより、デュアルゲート電極３１Ｌが構成されている。また、ゲート電極３０ｃとゲート電極３０ｄとは、活性領域１０ｃと活性領域１０ｄとの間の素子分離領域１１上で互いに接続されており、これにより、デュアルゲート電極３１Ｓが構成されている。但し、図４（ａ）～（ｆ）に示す工程の終了時点でデュアルゲート電極３１Ｓ中にＰＮ境界は形成されていない。
【００５８】
次に、例えばＣＶＤ法により、半導体基板１０上の全面に、例えば厚さ８ｎｍのシリコン酸化膜からなるオフセットスペーサ用絶縁膜を堆積した後、当該オフセットスペーサ用絶縁膜に対して異方性エッチングを行う。これにより、図５（ａ）～（ｆ）に示すように、ゲート絶縁膜１３ａ及びゲート電極３０ａの各側面上にオフセットスペーサ１５ａが形成され、ゲート絶縁膜１３ｂ及びゲート電極３０ｂの各側面上にオフセットスペーサ１５ｂが形成され、ゲート絶縁膜１３ｃ及びゲート電極３０ｃの各側面上にオフセットスペーサ１５ｃが形成され、ゲート絶縁膜１３ｄ及びゲート電極３０ｄの各側面上にオフセットスペーサ１５ｄが形成される。
【００５９】
次に、半導体基板１０上に、各ＮＭＩＳ領域上に開口を有し且つ各ＰＭＩＳ領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターン並びにゲート電極３０ａ及び３０ｃをマスクとして、例えばＡｓ（ヒ素）等のｎ型不純物のイオン注入を行うことにより、図５（ａ）～（ｄ）に示すように、活性領域１０ａにおけるゲート電極３０ａの側方下及び活性領域１０ｃにおけるゲート電極３０ｃの側方下に、接合深さが比較的浅いＮ型ソース／ドレイン領域（例えばＬＤＤ（lightly doped drain ）領域又はエクステンション領域）１６ａ及び１６ｃをそれぞれ自己整合的に形成する。続いて、半導体基板１０上に、各ＮＭＩＳ領域を覆い且つ各ＰＭＩＳ領域上に開口を有するレジストパターン（図示省略）を形成した後、当該レジストパターン並びにゲート電極３０ｂ及び３０ｄをマスクとして、例えばBF_2 等のｐ型不純物のイオン注入を行うことにより、図５（ａ）～（ｄ）に示すように、活性領域１０ｂにおけるゲート電極３０ｂの側方下及び活性領域１０ｄにおけるゲート電極３０ｄの側方下に、接合深さが比較的浅いＰ型ソース／ドレイン領域（例えばＬＤＤ領域又はエクステンション領域）１６ｂ及び１６ｄをそれぞれ自己整合的に形成する。
【００６０】
尚、Ｎ型ソース／ドレイン領域１６ａ及び１６ｃの形成とＰ型ソース／ドレイン領域１６ｂ及び１６ｄの形成とは、いずれを先に実施してもよい。
【００６１】

次に、例えばＣＶＤ法により、半導体基板１０上の全面に、例えば厚さ１０ｎｍ程度のシリコン酸化膜からなる第１絶縁膜、及び例えば厚さ３０ｎｍ程度のシリコン窒化膜からなる第２絶縁膜を順次堆積した後、当該第１絶縁膜及び当該第２絶縁膜に対して異方性エッチングを行う。これにより、図６（ａ）～（ｆ）に示すように、ゲート電極３０ａの側面上にオフセットスペーサ１５ａを介してサイドウォールスペーサ１９ａが形成され、ゲート電極３０ｂの側面上にオフセットスペーサ１５ｂを介してサイドウォールスペーサ１９ｂが形成され、ゲート電極３０ｃの側面上にオフセットスペーサ１５ｃを介してサイドウォールスペーサ１９ｃが形成され、ゲート電極３０ｄの側面上にオフセットスペーサ１５ｄを介してサイドウォールスペーサ１９ｄが形成される。ここで、サイドウォールスペーサ１９ａは、Ｌ字状の断面形状を有し且つ前記第１絶縁膜からなる内側サイドウォール１７ａと、内側サイドウォール１７ａ上に形成され且つ前記第２絶縁膜からなる外側サイドウォール１８ａとを有する。また、サイドウォールスペーサ１９ｂは、Ｌ字状の断面形状を有し且つ前記第１絶縁膜からなる内側サイドウォール１７ｂと、内側サイドウォール１７ｂ上に形成され且つ前記第２絶縁膜からなる外側サイドウォール１８ｂとを有する。また、サイドウォールスペーサ１９ｃは、Ｌ字状の断面形状を有し且つ前記第１絶縁膜からなる内側サイドウォール１７ｃと、内側サイドウォール１７ｃ上に形成され且つ前記第２絶縁膜からなる外側サイドウォール１８ｃとを有する。また、サイドウォールスペーサ１９ｄは、Ｌ字状の断面形状を有し且つ前記第１絶縁膜からなる内側サイドウォール１７ｄと、内側サイドウォール１７ｄ上に形成され且つ前記第２絶縁膜からなる外側サイドウォール１８ｄとを有する。

【００６２】

続いて、図６（ａ）～（ｆ）に示すように、ロジック領域のＮＭＩＳ領域全体及びＳＲＡＭ領域のＮＭＩＳ領域全体を覆うマスクパターン５３、活性領域１０ｂにおけるゲート電極３０ｂ、オフセットスペーサ１５ｂ及びサイドウォールスペーサ１９ｂ、並びに活性領域１０ｄにおけるゲート電極３０ｄ、オフセットスペーサ１５ｄ及びサイドウォールスペーサ１９ｄをマスクとして、活性領域１０ｂ及び活性領域１０ｄに例えばＢ（ボロン）等のＰ型不純物をドーズ量５×１０^{15}ｃｍ$^{-2}$でイオン注入する。これにより、活性領域１０ｂにおけるサイドウォールスペーサ１９ｂの外側方下に、浅いＰ型ソース／ドレイン領域１６ｂよりも接合深さが深く且つＰ型ソース／ドレイン領域１６ｂと接続するＰ型ソース／ドレイン領域２０ｂを自己整合的に形成すると共に、活性領域１０ｄにおけるサイドウォールスペーサ１９ｄの外側方下に、浅いＰ型ソース／ドレイン領域１６ｄよりも接合深さが深く且つＰ型ソース／ドレイン領域１６ｄと接続するＰ型ソース／ドレイン領域２０ｄを自己整合的に形成する。このとき、ゲート電極３０ｂを構成するＰ型シリコン膜１４ｂ及びゲート電極３０ｄを構成するＮ型シリコン膜１４ｄ’にも前記Ｐ型不純物が注入される結果、Ｐ型シリコン膜１４ｂのＰ型不純物濃度はより高くなる一方、Ｎ型シリコン膜１４ｄ’はＰ型シリコン膜１４ｄとなる。これにより、デュアルゲート電極３１Ｓ中にＮ型シリコン膜１４ｃ（ゲート電極３０ｃ）とＰ型シリコン膜１４ｄ（ゲート電極３０ｄ）とのＰＮ境界４１Ｓが形成される。ここで、Ｐ型シリコン膜１４ｂのＰ型不純物濃度は、Ｐ型シリコン膜１４ｄのＰ型不純物濃度よりも高くなる。

【００６３】

続いて、図６（ａ）～（ｆ）に示すように、ロジック領域のＰＭＩＳ領域全体及びＳＲＡＭ領域のＰＭＩＳ領域全体を覆うマスクパターン５４、活性領域１０ａにおけるゲート電極３０ａ、オフセットスペーサ１５ａ及びサイドウォールスペーサ１９ａ、並びに活性領域１０ｃにおけるゲート電極３０ｃ、オフセットスペーサ１５ｃ及びサイドウォールスペーサ１９ｃをマスクとして、活性領域１０ａ及び活性領域１０ｃに例えばＡｓ（ヒ素）等のＮ型不純物をドーズ量４×１０^{15}～５×１０^{15}ｃｍ$^{-2}$でイオン注入する。これにより、活性領域１０ａにおけるサイドウォールスペーサ１９ａの外側方下に、浅いＮ型ソース／ドレイン領域１６ａよりも接合深さが深く且つＮ型ソース／ドレイン領域１６ａと接続するＮ型ソース／ドレイン領域２０ａを自己整合的に形成すると共に、活性領域１０ｃにおけるサイドウォールスペーサ１９ｃの外側方下に、浅いＮ型ソース／ドレイン領域１６

ｃよりも接合深さが深く且つＮ型ソース／ドレイン領域１６ｃと接続するＮ型ソース／ドレイン領域２０ｃを自己整合的に形成する。

【００６４】

尚、Ｐ型ソース／ドレイン領域２０ｂ及び２０ｄの形成とＮ型ソース／ドレイン領域２０ａ及び２０ｃの形成とは、いずれを先に実施してもよい。また、図６（ａ）～（ｆ）においては、説明を分かりやすくするために、マスクパターン５３及び５４として、フォトリソグラフィ法により半導体基板１０上に形成されるレジストパターンではなく、当該レジストパターンを形成するためのフォトマスク上のマスクパターンを模式的に示している。また、マスクパターン５３及び５４は、Ｐ型シリコン膜１４ａ（ゲート電極３０ａ）とＮ型シリコン膜１４ｂ（ゲート電極３０ｂ）とのＰＮ境界４１Ｌの位置（活性領域１０ａと活性領域１０ｂとの間の素子分離領域１１上）が変わらないように、且つ、Ｐ型シリコン膜１４ｃ（ゲート電極３０ｃ）とＮ型シリコン膜１４ｄ（ゲート電極３０ｄ）とのＰＮ境界４１Ｓが、活性領域１０ｃと活性領域１０ｄとの間の素子分離領域１１上に位置するように設定されている。

【００６５】

Ｎ型ソース／ドレイン領域２０ａ及び２０ｃ並びにＰ型ソース／ドレイン領域２０ｂ及び２０ｄの形成後、半導体基板１０に対して熱処理を施すことにより、Ｎ型ソース／ドレイン領域２０ａ及び２０ｃ並びにＰ型ソース／ドレイン領域２０ｂ及び２０ｄのそれぞれにイオン注入された不純物を活性化させる。

【００６６】

次に、深いＮ型ソース／ドレイン領域２０ａ及び２０ｃ並びに深いＰ型ソース／ドレイン領域２０ｂ及び２０ｄのそれぞれの表面に形成されている自然酸化膜（図示省略）を除去した後、例えばスパッタ法により、半導体基板１０上の全面に、例えばニッケルからなる厚さ１０ｎｍ程度の金属膜（図示省略）を堆積する。その後、例えば窒素雰囲気中において、半導体基板１０に対して、例えば３２０℃の温度で１回目のＲＴＡ（Rapid Thermal Annealing）処理を行うことにより、深いＮ型ソース／ドレイン領域２０ａ及び２０ｃ並びに深いＰ型ソース／ドレイン領域２０ｂ及び２０ｄのそれぞれの表面部のシリコン（Ｓｉ）と前記金属膜のニッケル（Ｎｉ）とを反応させる。これにより、図７（ａ）～（ｆ）に示すように、深いＮ型ソース／ドレイン領域２０ａ及び２０ｃ並びに深いＰ型ソース／ドレイン領域２０ｂ及び２０ｄのそれぞれの上に、ニッケルシリサイドからなる金属シリサイド層２１ａ～２１ｄが形成される。このとき、ゲート電極３０ａ及び３０ｃを構成するＮ型シリコン膜１４ａ及び１４ｃ並びにゲート電極３０ｂ及び３０ｄを構成するＰ型シリコン膜１４ｂ及び１４ｄのそれぞれの表面部のＳｉと前記金属膜のＮｉとも反応する結果、ゲート電極３０ａ～３０ｄのそれぞれの上に、ニッケルシリサイドからなる金属シリサイド層２２ａ～２２ｄが形成される。その後、例えば硫酸と過酸化水素水との混合液からなるエッチング液中に半導体基板１０を浸漬することにより、素子分離領域１１、オフセットスペーサ１５ａ～１５ｄ及びサイドウォールスペーサ１９ａ～１９ｄ等の上に残存する未反応の前記金属膜を除去した後、１回目のＲＴＡ処理よりも高い温度（例えば５５０℃）で２回目のＲＴＡ処理を行うことにより、金属シリサイド層２１ａ～２１ｄ及び金属シリサイド層２２ａ～２２ｄのそれぞれのシリサイド組成比を安定化させる。

【００６７】

次に、図８（ａ）～（ｆ）に示すように、例えばプラズマＣＶＤ法により、半導体基板１０上の全面に、例えば厚さ２０ｎｍ程度のシリコン窒化膜からなる絶縁膜２３を堆積した後、例えばＣＶＤ法により、絶縁膜２３上に、例えばシリコン酸化膜からなる層間絶縁膜２４を堆積し、その後、例えばＣＭＰ（Chemical Mechanical Polishing）法により、層間絶縁膜２４の表面を平坦化する。次に、通常のＭＩＳトランジスタを有する半導体装置の製造方法と同様に、層間絶縁膜２４上に、コンタクトホールパターンを有するレジスト膜（図示省略）を形成した後、当該レジスト膜をマスクとして、ドライエッチング法により、絶縁膜２３及び層間絶縁膜２４に、金属シリサイド層２１ａ～２１ｄのそれぞれの上面に到達するコンタクトホール２５ａ～２５ｄを形成する。このとき、絶縁膜２３が露

出した時点で一度エッチングを中断する２ステップのエッチング法を用いることにより、金属シリサイド層２１ａ～２１ｄに対するオーバーエッチング量を減らすことができる。その後、例えばスパッタ法又はＣＶＤ法により、コンタクトホール２５ａ～２５ｄの底部及び側壁のそれぞれの上に、例えばチタン膜と窒化チタン膜とが順次堆積されてなるバリアメタル膜（図示省略）を形成する。その後、例えばＣＶＤ法により、層間絶縁膜２４上に、コンタクトホール２５ａ～２５ｄを埋め込むように例えばタングステン膜を堆積した後、例えばＣＭＰ法により、コンタクトホール２５ａ～２５ｄの外に形成されている前記タングステン膜を除去する。このようにして、コンタクトホール２５ａ～２５ｄに、前記バリアメタル膜を介して前記タングステン膜が埋め込まれてなるコンタクト２６ａ～２６ｄを形成する。その後、層間絶縁膜２４上に、コンタクト２６ａ～２６ｄと電気的に接続する金属配線（図示省略）を形成する。

【００６８】

以上のようにして、本実施形態に係る半導体装置、つまり、Ｎ型シリコン膜１４ａを含むゲート電極３０ａを有するロジック領域内のＮＭＩＳＦＥＴと、Ｐ型シリコン膜１４ｂを含むゲート電極３０ｂを有するロジック領域内のＰＭＩＳＦＥＴと、Ｎ型シリコン膜１４ｃを含むゲート電極３０ｃを有するＳＲＡＭ領域内のＮＭＩＳＦＥＴと、Ｐ型シリコン膜１４ｄを含むゲート電極３０ｄを有するＳＲＡＭ領域内のＰＭＩＳＦＥＴとを備えた半導体装置を製造することができる。

【００６９】

本実施形態によると、ドライエッチング法により、シリコン膜１４をエッチングして、ゲート電極３０ａ～３０ｄを形成する際に、素子分離領域１１（具体的には活性領域１０ｃと活性領域１０ｄとの間の素子分離領域１１）の幅が狭くて不純物の相互拡散の影響を受けやすいＳＲＡＭ領域のゲート電極３０ｃ及び３０ｄを構成するシリコン膜１４中には実質的にＮ型不純物のみが存在している。従って、注入不純物であるイオン種の違いに起因してシリコン膜１４のエッチング速度に差が生じる事態を回避できるため、ＮＭＩＳＦＥＴのゲート電極３０ｃとＰＭＩＳＦＥＴのゲート電極３０ｄとの間でゲート寸法差が生じることがないので、ゲート長変動に起因するトランジスタ特性の変動を抑制することができる。また、ドライエッチング法により、シリコン膜１４をエッチングする際には、シリコン膜１４中に注入された不純物の垂直方向プロファイルを予めアニール処理によって均一化しておく必要があるが、本実施形態では、シリコン膜１４をエッチングする時点でＳＲＡＭ領域内のシリコン膜１４中の不純物は実質的にＮ型不純物のみであるため、前記アニール処理に起因する不純物の相互拡散（具体的には基板主面に対して平行な方向への拡散）の影響は実質的に無視できる。従って、トランジスタ特性の変動をより一層抑制することができる。

【００７０】

また、本実施形態では、ＳＲＡＭ領域内のＰＭＩＳ領域のゲート電極３０ｄを構成するシリコン膜１４中には、ゲート注入の際にはＮ型不純物が注入される一方、ソース／ドレイン注入の際にはＰ型不純物が注入される。従って、ＳＲＡＭ領域内のＰＭＩＳＦＥＴを表面チャネル型にするためには、ゲート注入の際のＮ型不純物濃度を、ソース／ドレイン注入の際のＰ型不純物濃度よりも小さく設定しておくことが望ましい。この場合、本実施形態の特徴として、ロジック領域内のＰＭＩＳ領域のゲート電極３０ｂを構成するＰ型シリコン膜１４ｂ中のＰ型不純物濃度は、ＳＲＡＭ領域内のＰＭＩＳ領域のゲート電極３０ｄを構成するＰ型シリコン膜１４ｄ中のＰ型不純物濃度よりも大きくなる。

【００７１】

尚、本実施形態では、ＳＲＡＭ領域内のＮＭＩＳ領域及びＰＭＩＳ領域に対してＮ型不純物のゲート注入を行った後、Ｐ型不純物のソース／ドレイン注入によって、ＳＲＡＭ領域内のＰＭＩＳ領域のゲート電極３０ｄを構成するシリコン膜１４の導電型をＰ型に反転させた。しかし、これに代えて、ＳＲＡＭ領域内のＮＭＩＳ領域及びＰＭＩＳ領域に対してＰ型不純物のゲート注入を行った後、Ｎ型不純物のソース／ドレイン注入によって、ＳＲＡＭ領域内のＮＭＩＳ領域のゲート電極３０ｃを構成するシリコン膜１４の導電型をＮ

型に反転させてもよい。
【００７２】
（第２の実施形態）
以下、本発明の第２の実施形態に係る半導体装置について、図面を参照しながら説明する。
【００７３】
図９（ａ）は、第２の実施形態に係る半導体装置におけるロジック領域の平面図であり、図９（ｂ）は、図９（ａ）におけるＩ－Ｉ線（ゲート幅方向）の断面図である。また、図９（ｃ）は、第２の実施形態に係る半導体装置におけるＳＲＡＭ領域の平面図であり、図９（ｄ）は、図９（ｃ）におけるII－II線（ゲート幅方向）の断面図である。尚、説明を簡単にするために、図９（ａ）～（ｄ）においてサイドウォールスペーサ、シリサイド層及び層間膜等の図示を省略していると共に、図９（ｂ）及び（ｄ）においてコンタクトの図示を省略している。また、図９（ａ）～（ｄ）において、図１（ａ）～（ｄ）に示す第１の実施形態と同じ構成要素には同じ符号を付しており、以下、第１の実施形態と共通する点については適宜説明を省略し、第１の実施形態と相違する点について主として説明する。
【００７４】
本実施形態が第１の実施形態と異なっている点は、図９（ａ）及び（ｂ）に示すように、ロジック領域のデュアルゲート電極３１Ｌが、活性領域１０ａ及びその近傍の素子分離領域１１の上に位置するＮ型シリコン膜１４ａ１とその両側の素子分離領域１１の上に位置するＮ型シリコン膜１４ａ２とを含むＮＭＩＳ領域のゲート電極３０ａと、活性領域１０ｂ及びその近傍の素子分離領域１１の上に位置するＰ型シリコン膜１４ｂ１とその両側の素子分離領域１１の上に位置するＰ型シリコン膜１４ｂ２とを含むＰＭＩＳ領域のゲート電極３０ｂとを有していることである。
【００７５】
尚、図９（ｃ）及び（ｄ）に示すＳＲＡＭ領域の構成は、デュアルゲート電極３１Ｓの構成を含めて、図１（ｃ）及び（ｄ）に示す第１の実施形態のＳＲＡＭ領域の構成と同じである。すなわち、デュアルゲート電極３１Ｓは、第１の実施形態と同様に、Ｎ型シリコン膜１４ｃを含むＮＭＩＳ領域のゲート電極３０ｃと、Ｐ型シリコン膜１４ｄを含むＰＭＩＳ領域のゲート電極３０ｄとを有している。
【００７６】
本実施形態の特徴として、Ｐ型シリコン膜１４ｂ１のＰ型不純物濃度は、Ｐ型シリコン膜１４ｂ２のＰ型不純物濃度よりも低い。また、Ｐ型シリコン膜１４ｂ１及びＰ型シリコン膜１４ｂ２のそれぞれのＰ型不純物濃度は、Ｐ型シリコン膜１４ｄのＰ型不純物濃度よりも高い。また、Ｎ型シリコン膜１４ａ１のＮ型不純物濃度は、Ｎ型シリコン膜１４ａ２及びＮ型シリコン膜１４ｃのそれぞれのＮ型不純物濃度よりも低い。また、Ｎ型シリコン膜１４ａ２のＮ型不純物濃度は、Ｎ型シリコン膜１４ｃのＮ型不純物濃度と実質的に同じである。
【００７７】
以下、本発明の第２の実施形態に係る半導体装置の製造方法について、図面を参照しながら説明する。尚、本実施形態に係る半導体装置の製造方法が第１の実施形態と相違している点は、ロジック領域におけるゲート注入箇所のみである（図１０（ａ）～（ｆ）参照）。
【００７８】
図１０（ａ）～（ｆ）は、第２の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。尚、図１０（ａ）は、図９（ａ）におけるIII－III線（ゲート長方向）の一工程での断面構成を示したものであり、図１０（ｂ）は、図９（ａ）におけるIV－IV線（ゲート長方向）の一工程での断面構成を示したものであり、図１０（ｃ）は、図９（ｃ）におけるＶ－Ｖ線（ゲート長方向）の一工程での断面構成を示したものであり、図１０（ｄ）は、図９（ｃ）におけるVI－VI線（ゲート長方向）の一工程での断面構成を示した

ものである。また、図１０（ｅ）は、図９（ａ）におけるＩ－Ｉ線（ゲート幅方向）の一工程での断面構成を示したものであり、図１０（ｆ）は、図９（ｃ）におけるII－II線（ゲート幅方向）の一工程での断面構成を示したものである。

【００７９】

本実施形態においては、まず、第１の実施形態における図２（ａ）～（ｆ）に示す工程と同様の工程を実施した後、図１０（ａ）～（ｆ）に示すように、例えば希釈フッ酸処理により、半導体基板１０の表面を洗浄し、その後、例えばＩＳＳＧ酸化法により、活性領域１０ａ、１０ｂ、１０ｃ及び１０ｄのそれぞれの上に、例えば厚さ２ｎｍ程度のシリコン酸化膜からなるゲート絶縁膜１３を堆積する。その後、半導体基板１０に対して、例えば窒素プラズマ処理を行うことにより、ゲート絶縁膜１３の表面を窒化して窒化層（図示省略）を形成する。その後、アニール処理を実施することにより、前記窒化層から、結合の弱い窒素を除去する。続いて、ゲート絶縁膜１３上に、例えばＣＶＤ法により、例えばポリシリコンからなる厚さ１００ｎｍ程度のシリコン膜１４を堆積する。

【００８０】

続いて、図１０（ａ）～（ｆ）に示すように、ロジック領域におけるＮＭＩＳ領域全体及びＰＭＩＳ領域のうちの活性領域１０ｂ並びにＳＲＡＭ領域全体（ＮＭＩＳ領域全体及びＰＭＩＳ領域全体）を覆い且つロジック領域におけるＰＭＩＳ領域のうちの素子分離領域１１上に開口を有するマスクパターン５１Ｂを用いて、シリコン膜１４に例えばＢ（ホウ素）等のＰ型不純物をドーズ量４×１０^{15}ｃｍ$^{-2}$でイオン注入する。これにより、ロジック領域のＰＭＩＳ領域のうちの素子分離領域１１上にＰ型シリコン膜１４Ｐが形成される。ここで、マスクパターン５１Ｂは、ロジック領域のＰＭＩＳ領域における活性領域１０ｂ近傍の素子分離領域１１を不純物の相互拡散の影響を考慮した寸法（例えば５０ｎｍ程度）だけ覆っている。次に、ロジック領域におけるＰＭＩＳ領域全体及びＮＭＩＳ領域のうちの活性領域１０ａを覆い且つロジック領域におけるＮＭＩＳ領域のうちの素子分離領域１１及びＳＲＡＭ領域全体（ＮＭＩＳ領域全体及びＰＭＩＳ領域全体）のそれぞれの上に開口を有するマスクパターン５２Ｂを用いて、シリコン膜１４に例えばＰ（リン）等のＮ型不純物をドーズ量３×１０^{15}ｃｍ$^{-2}$でイオン注入する。これにより、ロジック領域のＮＭＩＳ領域のうちの素子分離領域１１上にＮ型シリコン膜１４Ｎが形成されると共に、ＳＲＡＭ領域全体に亘ってＮ型シリコン膜１４Ｎが形成される。ここで、マスクパターン５２Ｂは、ロジック領域のＮＭＩＳ領域における活性領域１０ａ近傍の素子分離領域１１を不純物の相互拡散の影響を考慮した寸法（例えば５０ｎｍ程度）だけ覆っている。すなわち、本実施形態においても、第１の実施形態と同様に、ＳＲＡＭ領域のＰＭＩＳ領域のゲート注入においてＮ型不純物のイオン注入を行っている。

【００８１】

尚、Ｐ型シリコン膜１４Ｐの形成とＮ型シリコン膜１４Ｎの形成とは、いずれを先に実施してもよい。また、図１０（ａ）～（ｆ）においては、説明を分かりやすくするために、マスクパターン５１Ｂ及び５２Ｂとして、フォトリソグラフィ法により半導体基板１０上に形成されるレジストパターンではなく、当該レジストパターンを形成するためのフォトマスク上のマスクパターンを模式的に示している。また、マスクパターン５１Ｂ及び５２Ｂは、Ｐ型シリコン膜１４ＰとＮ型シリコン膜１４ＮとのＰＮ境界４１Ｌが、活性領域１０ａと活性領域１０ｂとの間の素子分離領域１１上に位置するように設定されている。

【００８２】

Ｐ型シリコン膜１４Ｐ及びＮ型シリコン膜１４Ｎの形成後、半導体基板１０に対して、例えば８５０℃、３０秒間の熱処理を施すことにより、Ｐ型シリコン膜１４Ｐ及びＮ型シリコン膜１４Ｎのそれぞれにイオン注入された不純物の垂直方向プロファイルの均一化を行う。

【００８３】

その後、第１の実施形態における図４（ａ）～（ｆ）に示す工程（ゲートパターニング）、図５（ａ）～（ｆ）に示す工程（オフセットスペーサ及び浅いソース／ドレイン領域の形成）、図６（ａ）～（ｆ）に示す工程（サイドウォールスペーサ及び深いソース／ド

レイン領域の形成）、図７（ａ）～（ｆ）に示す工程（シリサイド層の形成）及び図８（ａ）～（ｆ）に示す工程（層間絶縁膜及びコンタクトの形成）のそれぞれと同様の工程を順次実施する。

【００８４】

以上のようにして、本実施形態に係る半導体装置、つまり、Ｎ型シリコン膜１４ａ１及び１４ａ２を含むゲート電極３０ａを有するロジック領域内のＮＭＩＳＦＥＴと、Ｐ型シリコン膜１４ｂ１及び１４ｂ２を含むゲート電極３０ｂを有するロジック領域内のＰＭＩＳＦＥＴと、Ｎ型シリコン膜１４ｃを含むゲート電極３０ｃを有するＳＲＡＭ領域内のＮＭＩＳＦＥＴと、Ｐ型シリコン膜１４ｄを含むゲート電極３０ｄを有するＳＲＡＭ領域内のＰＭＩＳＦＥＴとを備えた半導体装置を製造することができる。

【００８５】

本実施形態によると、ドライエッチング法により、シリコン膜１４をエッチングして、ゲート電極３０ａ～３０ｄを形成する際に、素子分離領域１１（具体的には活性領域１０ｃと活性領域１０ｄとの間の素子分離領域１１）の幅が狭くて不純物の相互拡散の影響を受けやすいＳＲＡＭ領域のゲート電極３０ｃ及び３０ｄを構成するシリコン膜１４中には実質的にＮ型不純物のみが存在している。従って、注入不純物であるイオン種の違いに起因してシリコン膜１４のエッチング速度に差が生じる事態を回避できるため、ＮＭＩＳＦＥＴのゲート電極３０ｃとＰＭＩＳＦＥＴのゲート電極３０ｄとの間でゲート寸法差が生じることがないので、ゲート長変動に起因するトランジスタ特性の変動を抑制することができる。また、ドライエッチング法により、シリコン膜１４をエッチングする際には、シリコン膜１４中に注入された不純物の垂直方向プロファイルを予めアニール処理によって均一化しておく必要があるが、本実施形態では、第１の実施形態と同様に、シリコン膜１４をエッチングする時点でＳＲＡＭ領域内のシリコン膜１４中の不純物は実質的にＮ型不純物のみであるため、前記アニール処理に起因する不純物の相互拡散（具体的には基板主面に対して平行な方向への拡散）の影響は実質的に無視できる。従って、トランジスタ特性の変動をより一層抑制することができる。

【００８６】

また、本実施形態によると、ドライエッチング法により、シリコン膜１４をエッチングして、ゲート電極３０ａ～３０ｄを形成する際に、ロジック領域における少なくとも活性領域１０ａ及び１０ｂ上のシリコン膜１４中には不純物が注入されていない。従って、注入不純物であるイオン種の違いに起因してシリコン膜１４のエッチング速度に差が生じる事態を回避できるため、ＮＭＩＳＦＥＴのゲート電極３０ａとＰＭＩＳＦＥＴのゲート電極３０ｂとの間でゲート寸法差が生じることがないので、ゲート長変動に起因するトランジスタ特性の変動を抑制することができる。

【００８７】

また、本実施形態では、ＳＲＡＭ領域内のＰＭＩＳ領域のゲート電極３０ｄを構成するシリコン膜１４中には、ゲート注入の際にはＮ型不純物が注入される一方、ソース／ドレイン注入の際にはＰ型不純物が注入される。従って、ＳＲＡＭ領域内のＰＭＩＳＦＥＴを表面チャネル型にするためには、第１の実施形態と同様に、ゲート注入の際のＮ型不純物濃度を、ソース／ドレイン注入の際のＰ型不純物濃度よりも小さく設定しておくことが望ましい。この場合、本実施形態の特徴として、ロジック領域内のＰＭＩＳ領域のゲート電極３０ｂを構成するＰ型シリコン膜１４ｂ１及び１４ｂ２中のＰ型不純物濃度は、ＳＲＡＭ領域内のＰＭＩＳ領域のゲート電極３０ｄを構成するＰ型シリコン膜１４ｄ中のＰ型不純物濃度よりも大きくなる。

【００８８】

さらに、本実施形態では、ロジック領域内に形成された活性領域１０ａ上のＮ型シリコン膜１４ａ１のＮ型不純物濃度は、ロジック領域内に形成された素子分離領域１１上のＮ型シリコン膜１４ａ２のＮ型不純物濃度よりも小さいと共に、ロジック領域内に形成された活性領域１０ｂ上のＰ型シリコン膜１４ｂ１のＰ型不純物濃度は、ロジック領域内に形成された素子分離領域１１上のＰ型シリコン膜１４ｂ２のＰ型不純物濃度よりも小さい。

このため、ロジック領域内に形成された活性領域１０ａ及び１０ｂ上のゲート電極３０ａ及び３０ｂの抵抗は高くなるものの、ゲート電極３０ａ及び３０ｂ上には金属シリサイド層２２ａ及び２２ｂが形成されていると共に、ロジック領域内に形成された素子分離領域１１上のゲート電極３０ａ及び３０ｂ（つまりゲート配線）中の不純物濃度は第１の実施形態と同様に高濃度に設定されている。従って、活性領域１０ａ及び１０ｂ上のゲート電極３０ａ及び３０ｂの高抵抗化に起因する回路速度の遅延を抑制することができる。尚、本実施形態では、活性領域１０ａ及び１０ｂ上のゲート電極３０ａ及び３０ｂを構成するシリコン膜１４にはゲート注入時に不純物が導入されないので、当該シリコン膜１４にはソース／ドレイン注入時に、最終的に空乏化が発生しない程度の不純物量を注入しておく必要がある。また、活性領域１０ａ及び１０ｂ上のゲート電極３０ａ及び３０ｂの高抵抗化に起因する回路速度の遅延の影響が小さい場合には、ロジック領域内に形成された素子分離領域１１上のゲート電極３０ａ及び３０ｂを構成するシリコン膜１４にもゲート注入時に不純物を導入しなくてもよい。

【００８９】

尚、本実施形態では、ＳＲＡＭ領域内のＮＭＩＳ領域及びＰＭＩＳ領域に対してＮ型不純物のゲート注入を行った後、Ｐ型不純物のソース／ドレイン注入によって、ＳＲＡＭ領域内のＰＭＩＳ領域のゲート電極３０ｄを構成するシリコン膜１４の導電型をＰ型に反転させた。しかし、これに代えて、ＳＲＡＭ領域内のＮＭＩＳ領域及びＰＭＩＳ領域に対してＰ型不純物のゲート注入を行った後、Ｎ型不純物のソース／ドレイン注入によって、ＳＲＡＭ領域内のＮＭＩＳ領域のゲート電極３０ｃを構成するシリコン膜１４の導電型をＮ型に反転させてもよい。

【００９０】

（第３の実施形態）

以下、本発明の第３の実施形態に係る半導体装置について、図面を参照しながら説明する。

【００９１】

図１１（ａ）は、第３の実施形態に係る半導体装置におけるロジック領域の平面図であり、図１１（ｂ）は、図１１（ａ）におけるＩ－Ｉ線（ゲート幅方向）の断面図である。また、図１１（ｃ）は、第３の実施形態に係る半導体装置におけるＳＲＡＭ領域の平面図であり、図１１（ｄ）は、図１１（ｃ）におけるII－II線（ゲート幅方向）の断面図である。尚、説明を簡単にするために、図１１（ａ）～（ｄ）においてサイドウォールスペーサ、シリサイド層及び層間膜等の図示を省略していると共に、図１１（ｂ）及び（ｄ）においてコンタクトの図示を省略している。また、図１１（ａ）～（ｄ）において、図１（ａ）～（ｄ）に示す第１の実施形態と同じ構成要素には同じ符号を付しており、以下、第１の実施形態と共通する点については適宜説明を省略し、第１の実施形態と相違する点について主として説明する。

【００９２】

本実施形態が第１の実施形態と異なっている点は、図９（ａ）及び（ｂ）に示す第２の実施形態と同様に、図１１（ａ）及び（ｂ）に示すように、ロジック領域のデュアルゲート電極３１Ｌが、活性領域１０ａ及びその近傍の素子分離領域１１の上に位置するＮ型シリコン膜１４ａ１とその両側の素子分離領域１１の上に位置するＮ型シリコン膜１４ａ２とを含むＮＭＩＳ領域のゲート電極３０ａと、活性領域１０ｂ及びその近傍の素子分離領域１１の上に位置するＰ型シリコン膜１４ｂ１とその両側の素子分離領域１１の上に位置するＰ型シリコン膜１４ｂ２とを含むＰＭＩＳ領域のゲート電極３０ｂとを有していることである。

【００９３】

尚、図１１（ｃ）及び（ｄ）に示すＳＲＡＭ領域の構成は、デュアルゲート電極３１Ｓの構成を含めて、図１（ｃ）及び（ｄ）に示す第１の実施形態のＳＲＡＭ領域の構成と基本的に同じである。すなわち、デュアルゲート電極３１Ｓは、第１の実施形態と同様に、Ｎ型シリコン膜１４ｃを含むＮＭＩＳ領域のゲート電極３０ｃと、Ｐ型シリコン膜１４ｄ

を含むＰＭＩＳ領域のゲート電極３０ｄとを有している。但し、本実施形態においては、Ｎ型シリコン膜１４ｃのＮ型不純物濃度及びＰ型シリコン膜１４ｄのＰ型不純物濃度はそれぞれ、第１の実施形態と比較して小さく設定されている。

【００９４】

本実施形態の特徴として、Ｐ型シリコン膜１４ｂ２のＰ型不純物濃度は、Ｐ型シリコン膜１４ｄのＰ型不純物濃度よりも高い。また、Ｐ型シリコン膜１４ｂ１のＰ型不純物濃度は、Ｐ型シリコン膜１４ｄのＰ型不純物濃度と実質的に同じである。すなわち、Ｐ型シリコン膜１４ｂ１のＰ型不純物濃度は、Ｐ型シリコン膜１４ｂ２のＰ型不純物濃度よりも低い。また、Ｎ型シリコン膜１４ａ１のＮ型不純物濃度は、Ｎ型シリコン膜１４ｃのＮ型不純物濃度と実質的に同じである。また、Ｎ型シリコン膜１４ａ１のＮ型不純物濃度は、Ｎ型シリコン膜１４ａ２のＮ型不純物濃度よりも低い。すなわち、Ｎ型シリコン膜１４ａ２のＮ型不純物濃度は、Ｎ型シリコン膜１４ｃのＮ型不純物濃度よりも高い。

【００９５】

以下、本発明の第３の実施形態に係る半導体装置の製造方法について、図面を参照しながら説明する。尚、本実施形態に係る半導体装置の製造方法が第１の実施形態と相違している点は、ロジック領域及びＳＲＡＭ領域のそれぞれにおけるゲート注入箇所のみである（図１２（ａ）～（ｆ）参照）。

【００９６】

図１２（ａ）～（ｆ）は、第３の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。尚、図１２（ａ）は、図１１（ａ）におけるIII－III線（ゲート長方向）の一工程での断面構成を示したものであり、図１２（ｂ）は、図１１（ａ）におけるIV－IV線（ゲート長方向）の一工程での断面構成を示したものであり、図１２（ｃ）は、図１１（ｃ）におけるＶ－Ｖ線（ゲート長方向）の一工程での断面構成を示したものであり、図１２（ｄ）は、図１１（ｃ）におけるVI－VI線（ゲート長方向）の一工程での断面構成を示したものである。また、図１２（ｅ）は、図１１（ａ）におけるＩ－Ｉ線（ゲート幅方向）の一工程での断面構成を示したものであり、図１２（ｆ）は、図１１（ｃ）におけるII－II線（ゲート幅方向）の一工程での断面構成を示したものである。

【００９７】

本実施形態においては、まず、第１の実施形態における図２（ａ）～（ｆ）に示す工程と同様の工程を実施した後、図１２（ａ）～（ｆ）に示すように、例えば希釈フッ酸処理により、半導体基板１０の表面を洗浄し、その後、例えばＩＳＳＧ酸化法により、活性領域１０ａ、１０ｂ、１０ｃ及び１０ｄのそれぞれの上に、例えば厚さ２ｎｍ程度のシリコン酸化膜からなるゲート絶縁膜１３を堆積する。その後、半導体基板１０に対して、例えば窒素プラズマ処理を行うことにより、ゲート絶縁膜１３の表面を窒化して窒化層（図示省略）を形成する。その後、アニール処理を実施することにより、前記窒化層から、結合の弱い窒素を除去する。続いて、ゲート絶縁膜１３上に、例えばＣＶＤ法により、例えばポリシリコンからなる厚さ１００ｎｍ程度のシリコン膜１４を堆積する。

【００９８】

続いて、図１２（ａ）～（ｆ）に示すように、ロジック領域におけるＮＭＩＳ領域全体及びＰＭＩＳ領域のうちの活性領域１０ｂ並びにＳＲＡＭ領域全体（ＮＭＩＳ領域全体及びＰＭＩＳ領域全体）を覆い且つロジック領域におけるＰＭＩＳ領域のうちの素子分離領域１１上に開口を有するマスクパターン５１Ｃを用いて、シリコン膜１４に例えばＢ（ホウ素）等のＰ型不純物をドーズ量$４\times１０^{15}ｃｍ^{-2}$でイオン注入する。これにより、ロジック領域のＰＭＩＳ領域のうちの素子分離領域１１上にＰ型シリコン膜１４Ｐが形成される。ここで、マスクパターン５１Ｃは、ロジック領域のＰＭＩＳ領域における活性領域１０ｂ近傍の素子分離領域１１を不純物の相互拡散の影響を考慮した寸法（例えば５０ｎｍ程度）だけ覆っている。次に、ロジック領域におけるＰＭＩＳ領域全体及びＮＭＩＳ領域のうちの活性領域１０ａ並びにＳＲＡＭ領域全体（ＮＭＩＳ領域全体及びＰＭＩＳ領域全体）を覆い且つロジック領域におけるＮＭＩＳ領域のうちの素子分離領域１１上に開口を有するマスクパターン５２Ｃを用いて、シリコン膜１４に例えばＰ（リン）等のＮ型不純

物をドーズ量３×１０^{15}ｃｍ$^{-2}$でイオン注入する。これにより、ロジック領域のＮＭＩＳ領域のうちの素子分離領域１１上にＮ型シリコン膜１４Ｎが形成される。ここで、マスクパターン５２Ｃは、ロジック領域のＮＭＩＳ領域における活性領域１０ａ近傍の素子分離領域１１を不純物の相互拡散の影響を考慮した寸法（例えば５０ｎｍ程度）だけ覆っている。すなわち、本実施形態においては、第１及び第２の実施形態と異なり、ＳＲＡＭ領域のＮＭＩＳ領域及びＰＭＩＳ領域のいずれにもゲート注入を行っていない。

【００９９】

尚、Ｐ型シリコン膜１４Ｐの形成とＮ型シリコン膜１４Ｎの形成とは、いずれを先に実施してもよい。また、図１２（ａ）～（ｆ）においては、説明を分かりやすくするために、マスクパターン５１Ｃ及び５２Ｃとして、フォトリソグラフィ法により半導体基板１０上に形成されるレジストパターンではなく、当該レジストパターンを形成するためのフォトマスク上のマスクパターンを模式的に示している。また、マスクパターン５１Ｃ及び５２Ｃは、Ｐ型シリコン膜１４ＰとＮ型シリコン膜１４ＮとのＰＮ境界４１Ｌが、活性領域１０ａと活性領域１０ｂとの間の素子分離領域１１上に位置するように設定されている。

【０１００】

Ｐ型シリコン膜１４Ｐ及びＮ型シリコン膜１４Ｎの形成後、半導体基板１０に対して、例えば８５０℃、３０秒間の熱処理を施すことにより、Ｐ型シリコン膜１４Ｐ及びＮ型シリコン膜１４Ｎのそれぞれにイオン注入された不純物の垂直方向プロファイルの均一化を行う。

【０１０１】

その後、第１の実施形態における図４（ａ）～（ｆ）に示す工程（ゲートパターニング）、図５（ａ）～（ｆ）に示す工程（オフセットスペーサ及び浅いソース／ドレイン領域の形成）、図６（ａ）～（ｆ）に示す工程（サイドウォールスペーサ及び深いソース／ドレイン領域の形成）、図７（ａ）～（ｆ）に示す工程（シリサイド層の形成）及び図８（ａ）～（ｆ）に示す工程（層間絶縁膜及びコンタクトの形成）のそれぞれと同様の工程を順次実施する。

【０１０２】

以上のようにして、本実施形態に係る半導体装置、つまり、Ｎ型シリコン膜１４ａ１及び１４ａ２を含むゲート電極３０ａを有するロジック領域内のＮＭＩＳＦＥＴと、Ｐ型シリコン膜１４ｂ１及び１４ｂ２を含むゲート電極３０ｂを有するロジック領域内のＰＭＩＳＦＥＴと、Ｎ型シリコン膜１４ｃを含むゲート電極３０ｃを有するＳＲＡＭ領域内のＮＭＩＳＦＥＴと、Ｐ型シリコン膜１４ｄを含むゲート電極３０ｄを有するＳＲＡＭ領域内のＰＭＩＳＦＥＴとを備えた半導体装置を製造することができる。

【０１０３】

本実施形態によると、ドライエッチング法により、シリコン膜１４をエッチングして、ゲート電極３０ａ～３０ｄを形成する際に、素子分離領域１１（具体的には活性領域１０ｃと活性領域１０ｄとの間の素子分離領域１１）の幅が狭くて不純物の相互拡散の影響を受けやすいＳＲＡＭ領域のゲート電極３０ｃ及び３０ｄを構成するシリコン膜１４中には不純物が注入されていない。従って、注入不純物であるイオン種の違いに起因してシリコン膜１４のエッチング速度に差が生じる事態を回避できるため、ＮＭＩＳＦＥＴのゲート電極３０ｃとＰＭＩＳＦＥＴのゲート電極３０ｄとの間でゲート寸法差が生じることがないので、ゲート長変動に起因するトランジスタ特性の変動を抑制することができる。また、ドライエッチング法により、シリコン膜１４をエッチングする際には、シリコン膜１４中に注入された不純物の垂直方向プロファイルを予めアニール処理によって均一化しておく必要があるが、本実施形態では、シリコン膜１４をエッチングする時点ではＳＲＡＭ領域内のシリコン膜１４中に不純物が注入されていないため、前記アニール処理に起因する不純物の相互拡散（具体的には基板主面に対して平行な方向への拡散）の影響は実質的に無視できる。従って、トランジスタ特性の変動をより一層抑制することができる。

【０１０４】

また、本実施形態によると、ドライエッチング法により、シリコン膜１４をエッチング

して、ゲート電極３０ａ～３０ｄを形成する際に、ロジック領域における少なくとも活性領域１０ａ及び１０ｂ上のシリコン膜１４中には不純物が注入されていない。従って、第２の実施形態と同様に、注入不純物であるイオン種の違いに起因してシリコン膜１４のエッチング速度に差が生じる事態を回避できるため、ＮＭＩＳＦＥＴのゲート電極３０ａとＰＭＩＳＦＥＴのゲート電極３０ｂとの間でゲート寸法差が生じることがないので、ゲート長変動に起因するトランジスタ特性の変動を抑制することができる。

【０１０５】

また、本実施形態では、ロジック領域内に形成された活性領域１０ａ上のＮ型シリコン膜１４ａ１のＮ型不純物濃度は、ロジック領域内に形成された素子分離領域１１上のＮ型シリコン膜１４ａ２のＮ型不純物濃度よりも小さいと共に、ロジック領域内に形成された活性領域１０ｂ上のＰ型シリコン膜１４ｂ１のＰ型不純物濃度は、ロジック領域内に形成された素子分離領域１１上のＰ型シリコン膜１４ｂ２のＰ型不純物濃度よりも小さい。このため、ロジック領域内に形成された活性領域１０ａ及び１０ｂ上のゲート電極３０ａ及び３０ｂの抵抗は高くなるものの、ゲート電極３０ａ及び３０ｂ上には金属シリサイド層２２ａ及び２２ｂが形成されていると共に、ロジック領域内に形成された素子分離領域１１上のゲート電極３０ａ及び３０ｂ（つまりゲート配線）中の不純物濃度は第１の実施形態と同様に高濃度に設定されている。従って、活性領域１０ａ及び１０ｂ上のゲート電極３０ａ及び３０ｂの高抵抗化に起因する回路速度の遅延を抑制することができる。尚、本実施形態では、活性領域１０ａ及び１０ｂ上のゲート電極３０ａ及び３０ｂを構成するシリコン膜１４にはゲート注入時に不純物が導入されないので、当該シリコン膜１４にはソース／ドレイン注入時に、最終的に空乏化が発生しない程度の不純物量を注入しておく必要がある。また、活性領域１０ａ及び１０ｂ上のゲート電極３０ａ及び３０ｂの高抵抗化に起因する回路速度の遅延の影響が小さい場合には、ロジック領域内に形成された素子分離領域１１上のゲート電極３０ａ及び３０ｂを構成するシリコン膜１４にもゲート注入時に不純物を導入しなくてもよい。

【０１０６】

さらに、本実施形態では、ＳＲＡＭ領域内に形成されたゲート電極３０ｃ及び３０ｄを構成するシリコン膜１４にはゲート注入時に不純物が導入されないので、言い換えると、ゲート電極３０ｃ及び３０ｄを構成するシリコン膜１４にはソース／ドレイン注入時のみに不純物が導入されるので、ゲート電極３０ｃ及び３０ｄの抵抗は、ロジック領域内に形成されたゲート電極３０ａ及び３０ｂの抵抗よりも高くなる。しかし、ＳＲＡＭ回路用のトランジスタの動作に対しては、ロジック回路用のトランジスタのように高速動作が要求されないため、ゲート電極３０ｃ及び３０ｄの高抵抗化に起因する回路速度の遅延等の影響は小さい。

【０１０７】

（第４の実施形態）

以下、本発明の第４の実施形態に係る半導体装置について、図面を参照しながら説明する。

【０１０８】

図１３（ａ）は、第４の実施形態に係る半導体装置におけるロジック領域の平面図であり、図１３（ｂ）は、図１３（ａ）におけるＩ－Ｉ線（ゲート幅方向）の断面図である。また、図１３（ｃ）は、第４の実施形態に係る半導体装置におけるＳＲＡＭ領域の平面図であり、図１３（ｄ）は、図１３（ｃ）におけるII－II線（ゲート幅方向）の断面図である。尚、説明を簡単にするために、図１３（ａ）～（ｄ）においてサイドウォールスペーサ、シリサイド層及び層間膜等の図示を省略していると共に、図１３（ｂ）及び（ｄ）においてコンタクトの図示を省略している。また、図１３（ａ）～（ｄ）において、図１（ａ）～（ｄ）に示す第１の実施形態と同じ構成要素には同じ符号を付しており、以下、第１の実施形態と共通する点については適宜説明を省略し、第１の実施形態と相違する点について主として説明する。

【０１０９】

まず、図１３（ａ）及び（ｂ）に示すロジック領域の構成は、デュアルゲート電極３１Ｌの構成を含めて、図１（ａ）及び（ｂ）に示す第１の実施形態のロジック領域の構成と同じである。すなわち、デュアルゲート電極３１Ｌは、第１の実施形態と同様に、Ｎ型シリコン膜１４ａを含むＮＭＩＳ領域のゲート電極３０ａと、Ｐ型シリコン膜１４ｂを含むＰＭＩＳ領域のゲート電極３０ｂとを有している。

【０１１０】

一方、図１３（ｃ）及び（ｄ）に示すＳＲＡＭ領域の構成も、デュアルゲート電極３１Ｓの構成を含めて、図１（ｃ）及び（ｄ）に示す第１の実施形態のＳＲＡＭ領域の構成と基本的に同じである。すなわち、デュアルゲート電極３１Ｓは、第１の実施形態と同様に、Ｎ型シリコン膜１４ｃを含むＮＭＩＳ領域のゲート電極３０ｃと、Ｐ型シリコン膜１４ｄを含むＰＭＩＳ領域のゲート電極３０ｄとを有している。但し、本実施形態においては、Ｎ型シリコン膜１４ｃのＮ型不純物濃度及びＰ型シリコン膜１４ｄのＰ型不純物濃度はそれぞれ、第１の実施形態と比較して小さく設定されている。

【０１１１】

本実施形態の特徴として、Ｐ型シリコン膜１４ｂのＰ型不純物濃度は、Ｐ型シリコン膜１４ｄのＰ型不純物濃度よりも高く、Ｎ型シリコン膜１４ａのＮ型不純物濃度は、Ｎ型シリコン膜１４ｃのＮ型不純物濃度よりも高い。

【０１１２】

以下、本発明の第４の実施形態に係る半導体装置の製造方法について、図面を参照しながら説明する。尚、本実施形態に係る半導体装置の製造方法が第１の実施形態と相違している点は、ＳＲＡＭ領域におけるゲート注入箇所のみである（図１４（ａ）～（ｆ）参照）。

【０１１３】

図１４（ａ）～（ｆ）は、第４の実施形態に係る半導体装置の製造方法の一工程を示す断面図である。尚、図１４（ａ）は、図１３（ａ）におけるIII－III線（ゲート長方向）の一工程での断面構成を示したものであり、図１４（ｂ）は、図１３（ａ）におけるIV－IV線（ゲート長方向）の一工程での断面構成を示したものであり、図１４（ｃ）は、図１３（ｃ）におけるＶ－Ｖ線（ゲート長方向）の一工程での断面構成を示したものであり、図１４（ｄ）は、図１３（ｃ）におけるVI－VI線（ゲート長方向）の一工程での断面構成を示したものである。また、図１４（ｅ）は、図１３（ａ）におけるＩ－Ｉ線（ゲート幅方向）の一工程での断面構成を示したものであり、図１４（ｆ）は、図１３（ｃ）におけるII－II線（ゲート幅方向）の一工程での断面構成を示したものである。

【０１１４】

本実施形態においては、まず、第１の実施形態における図２（ａ）～（ｆ）に示す工程と同様の工程を実施した後、図１４（ａ）～（ｆ）に示すように、例えば希釈フッ酸処理により、半導体基板１０の表面を洗浄し、その後、例えばＩＳＳＧ酸化法により、活性領域１０ａ、１０ｂ、１０ｃ及び１０ｄのそれぞれの上に、例えば厚さ２ｎｍ程度のシリコン酸化膜からなるゲート絶縁膜１３を堆積する。その後、半導体基板１０に対して、例えば窒素プラズマ処理を行うことにより、ゲート絶縁膜１３の表面を窒化して窒化層（図示省略）を形成する。その後、アニール処理を実施することにより、前記窒化層から、結合の弱い窒素を除去する。続いて、ゲート絶縁膜１３上に、例えばＣＶＤ法により、例えばポリシリコンからなる厚さ１００ｎｍ程度のシリコン膜１４を堆積する。

【０１１５】

続いて、図１４（ａ）～（ｆ）に示すように、ロジック領域におけるＮＭＩＳ領域全体及びＳＲＡＭ領域全体（ＮＭＩＳ領域全体及びＰＭＩＳ領域全体）を覆い且つロジック領域におけるＰＭＩＳ領域全体上に開口を有するマスクパターン５１Ｄを用いて、シリコン膜１４に例えばＢ（ホウ素）等のＰ型不純物をドーズ量$4\times10^{15}cm^{-2}$でイオン注入する。これにより、ロジック領域のＰＭＩＳ領域全体にＰ型シリコン膜１４Ｐが形成される。次に、ロジック領域におけるＰＭＩＳ領域全体及びＳＲＡＭ領域全体（ＮＭＩＳ領域全体及びＰＭＩＳ領域全体）を覆い且つロジック領域におけるＮＭＩＳ領域全体上に開口を

有するマスクパターン５２Ｄを用いて、シリコン膜１４に例えばＰ（リン）等のＮ型不純物をドーズ量３×１０^{15}ｃｍ$^{-2}$でイオン注入する。これにより、ロジック領域のＮＭＩＳ領域全体にＮ型シリコン膜１４Ｎが形成される。すなわち、本実施形態においては、第３の実施形態と同様に、ＳＲＡＭ領域のＮＭＩＳ領域及びＰＭＩＳ領域のいずれにもゲート注入を行っていない。

【０１１６】

尚、Ｐ型シリコン膜１４Ｐの形成とＮ型シリコン膜１４Ｎの形成とは、いずれを先に実施してもよい。また、図１４（ａ）～（ｆ）においては、説明を分かりやすくするために、マスクパターン５１Ｄ及び５２Ｄとして、フォトリソグラフィ法により半導体基板１０上に形成されるレジストパターンではなく、当該レジストパターンを形成するためのフォトマスク上のマスクパターンを模式的に示している。また、マスクパターン５１Ｄ及び５２Ｄは、Ｐ型シリコン膜１４ＰとＮ型シリコン膜１４ＮとのＰＮ境界４１Ｌが、活性領域１０ａと活性領域１０ｂとの間の素子分離領域１１上に位置するように設定されている。

【０１１７】

Ｐ型シリコン膜１４Ｐ及びＮ型シリコン膜１４Ｎの形成後、半導体基板１０に対して、例えば８５０℃、３０秒間の熱処理を施すことにより、Ｐ型シリコン膜１４Ｐ及びＮ型シリコン膜１４Ｎのそれぞれにイオン注入された不純物の垂直方向プロファイルの均一化を行う。

【０１１８】

その後、第１の実施形態における図４（ａ）～（ｆ）に示す工程（ゲートパターニング）、図５（ａ）～（ｆ）に示す工程（オフセットスペーサ及び浅いソース／ドレイン領域の形成）、図６（ａ）～（ｆ）に示す工程（サイドウォールスペーサ及び深いソース／ドレイン領域の形成）、図７（ａ）～（ｆ）に示す工程（シリサイド層の形成）及び図８（ａ）～（ｆ）に示す工程（層間絶縁膜及びコンタクトの形成）のそれぞれと同様の工程を順次実施する。

【０１１９】

以上のようにして、本実施形態に係る半導体装置、つまり、Ｎ型シリコン膜１４ａを含むゲート電極３０ａを有するロジック領域内のＮＭＩＳＦＥＴと、Ｐ型シリコン膜１４ｂを含むゲート電極３０ｂを有するロジック領域内のＰＭＩＳＦＥＴと、Ｎ型シリコン膜１４ｃを含むゲート電極３０ｃを有するＳＲＡＭ領域内のＮＭＩＳＦＥＴと、Ｐ型シリコン膜１４ｄを含むゲート電極３０ｄを有するＳＲＡＭ領域内のＰＭＩＳＦＥＴとを備えた半導体装置を製造することができる。

【０１２０】

本実施形態によると、ドライエッチング法により、シリコン膜１４をエッチングして、ゲート電極３０ａ～３０ｄを形成する際に、素子分離領域１１（具体的には活性領域１０ｃと活性領域１０ｄとの間の素子分離領域１１）の幅が狭くて不純物の相互拡散の影響を受けやすいＳＲＡＭ領域のゲート電極３０ｃ及び３０ｄを構成するシリコン膜１４中には不純物が注入されていない。従って、注入不純物であるイオン種の違いに起因してシリコン膜１４のエッチング速度に差が生じる事態を回避できるため、ＮＭＩＳＦＥＴのゲート電極３０ｃとＰＭＩＳＦＥＴのゲート電極３０ｄとの間でゲート寸法差が生じることがないので、ゲート長変動に起因するトランジスタ特性の変動を抑制することができる。また、ドライエッチング法により、シリコン膜１４をエッチングする際には、シリコン膜１４中に注入された不純物の垂直方向プロファイルを予めアニール処理によって均一化しておく必要があるが、本実施形態では、第３の実施形態と同様に、シリコン膜１４をエッチングする時点ではＳＲＡＭ領域内のシリコン膜１４中に不純物が注入されていないため、前記アニール処理に起因する不純物の相互拡散（具体的には基板主面に対して平行な方向への拡散）の影響は実質的に無視できる。従って、トランジスタ特性の変動をより一層抑制することができる。

【０１２１】

また、本実施形態では、ＳＲＡＭ領域内に形成されたゲート電極３０ｃ及び３０ｄを構

成するシリコン膜１４にはゲート注入時に不純物が導入されないので、言い換えると、ゲート電極３０ｃ及び３０ｄを構成するシリコン膜１４にはソース／ドレイン注入時のみに不純物が導入されるので、ゲート電極３０ｃ及び３０ｄの抵抗は、ロジック領域内に形成されたゲート電極３０ａ及び３０ｂの抵抗よりも高くなる。しかし、ＳＲＡＭ回路用のトランジスタの動作に対しては、ロジック回路用のトランジスタのように高速動作が要求されないため、ゲート電極３０ｃ及び３０ｄの高抵抗化に起因する回路速度の遅延等の影響は小さい。

【０１２２】

尚、第１～第４の実施形態では、ゲート絶縁膜としてシリコン酸窒化膜、ゲート電極としてポリシリコン電極を用いた場合について説明したが、本発明はこれに限定されるものではない。例えば、ゲート絶縁膜材料として、アルミナ（Al_2O_3）、ハフニア（HfO_2）又はハフニウムシリケート（$HfSiO_x$）等の金属酸化物に代表される高誘電率材料（例えば比誘電率が８以上の絶縁材料）を用いると共に、ゲート電極構造として、ポリシリコン膜に加えて、ゲート絶縁膜とポリシリコン膜との間に、窒化チタン（ＴｉＮ）又は窒化タンタル（ＴａＮ）等の金属膜を有するＭＩＰＳ（Metal-Inserted Poly-silicon Stack）構造を用いる場合にも、各実施形態と同様の効果を実現することができる。ＭＩＰＳ構造では、主に仕事関数によってトランジスタの閾値電圧の調整が行われる。当該調整は、高誘電率ゲート絶縁膜材料と金属膜材料との組み合わせで決まる。具体的には、ＮＭＩＳＦＥＴとＰＭＩＳＦＥＴとの間での閾値電圧の調整を、高誘電率ゲート絶縁膜材料を同じにして金属膜材料を変えることによって行ってもよいし、又は金属膜材料を同じにして高誘電率ゲート絶縁膜材料を変えることによって行ってもよい。また、ＭＩＰＳ構造では、ゲート電極の空乏化が抑制されるため、ポリシリコン膜中の不純物濃度については、ゲート抵抗（バルク部分の抵抗、シリサイド／ポリシリコン界面の抵抗、ポリシリコン／金属界面の抵抗）を考慮して設定すればよい。尚、各界面抵抗が十分に小さければ、金属膜を用いているＭＩＰＳ構造ではゲート抵抗は小さくなる。

【０１２３】

また、第１及び第２の実施形態では、ＳＲＡＭ領域内のＰＭＩＳＦＥＴを表面チャネル型にするために、ゲート注入の際のＮ型不純物濃度を、ソース／ドレイン注入の際のＰ型不純物濃度よりも小さく設定することが望ましいとしたが、ＭＩＰＳ構造を用いる場合、シリコン膜の抵抗及び前記各界面抵抗を小さくするという観点から、ゲート注入の際のＮ型不純物濃度を、ソース／ドレイン注入の際のＰ型不純物濃度よりも大きく設定してもよい。或いは、ＳＲＡＭ領域内のゲート電極を構成するシリコン膜に対してはソース／ドレイン注入を行わなくてもよい。言い換えると、ＳＲＡＭ領域内のゲート電極を構成する各シリコン膜に対してはＮ型不純物のゲート注入のみを行ってもよい。これにより、ＳＲＡＭ領域内のＣＭＩＳＦＥＴのゲート電極を構成する全てのシリコン膜はＮ型シリコン膜となる。この場合、ロジック領域内のゲート電極を構成する各シリコン膜に対しても、ソース／ドレイン注入を行わず、Ｎ型不純物のゲート注入のみを行ってもよい。これにより、ロジック領域内のＣＭＩＳＦＥＴのゲート電極を構成する全てのシリコン膜もＮ型シリコン膜となる。

【０１２４】

また、第３及び第４の実施形態では、ＳＲＡＭ領域内のゲート電極を構成する各シリコン膜に対して、ゲート注入を行わなかったが、ＭＩＰＳ構造を用いる場合、ＳＲＡＭ領域内及びロジック領域内それぞれのゲート電極を構成する各シリコン膜に対して、ゲート注入を行わなくてもよい。言い換えると、ＳＲＡＭ領域内及びロジック領域内それぞれのゲート電極を構成する各シリコン膜に対して、ソース／ドレイン注入のみを行ってもよい。

【０１２５】

また、第１～第４の実施形態では、ロジック回路及びＳＲＡＭ回路を有する半導体装置について説明したが、本発明はこれに限定されるものではない。例えば、ロジック回路に代えて、入出力回路を有する場合にも、各実施形態のロジック回路用のデュアルゲート電極を適用可能である。すなわち、各実施形態における２種類のデュアルゲート電極は、Ｃ

ＭＩＳＦＥＴが形成される一対の活性領域同士の間の素子分離領域の幅に応じて使い分けることが可能である。具体的には、素子分離領域の幅が相対的に広いＣＭＩＳＦＥＴには、各実施形態のロジック回路用のデュアルゲート電極を適用し、素子分離領域の幅が相対的に狭いＣＭＩＳＦＥＴには、各実施形態のＳＲＡＭ回路用のデュアルゲート電極を適用することが可能である。

【産業上の利用可能性】

【０１２６】

本発明は、ＣＭＩＳデュアルゲート構造を有する半導体装置において、ＰＮ境界近傍でのゲート寸法変動や不純物の相互拡散に起因する素子特性の変動を抑制でき、ＣＭＩＳデュアルゲート構造を有する半導体装置及びその製造方法に好適である。

【符号の説明】

【０１２７】

１０　半導体基板
１０ａ、１０ｂ、１０ｃ、１０ｄ　活性領域
１１　素子分離領域
１２ａ、１２ｃ　Ｐ型ウェル領域
１２ｂ、１２ｄ　Ｎ型ウェル領域
１３、１３ａ、１３ｂ、１３ｃ、１３ｄ　ゲート絶縁膜
１４　シリコン膜
１４ａ、１４ａ１、１４ａ２、１４ｃ、１４ｄ’、１４Ｎ　Ｎ型シリコン膜
１４ｂ、１４ｂ１、１４ｂ２、１４ｄ、１４Ｐ　Ｐ型シリコン膜
１５ａ、１５ｂ、１５ｃ、１５ｄ　オフセットスペーサ
１６ａ、１６ｃ　浅いＮ型ソース／ドレイン領域
１６ｂ、１６ｄ　浅いＰ型ソース／ドレイン領域
１７ａ、１７ｂ、１７ｃ、１７ｄ　内側サイドウォール
１８ａ、１８ｂ、１８ｃ、１８ｄ　外側サイドウォール
１９ａ、１９ｂ、１９ｃ、１９ｄ　サイドウォールスペーサ
２０ａ、２０ｃ　深いＮ型ソース／ドレイン領域
２０ｂ、２０ｄ　深いＰ型ソース／ドレイン領域
２１ａ、２１ｂ、２１ｃ、２１ｄ　金属シリサイド層
２２ａ、２２ｂ、２２ｃ、２２ｄ　金属シリサイド層
２３　絶縁膜
２４　層間絶縁膜
２５ａ、２５ｂ、２５ｃ、２５ｄ　コンタクトホール
２６ａ、２６ｂ、２６ｃ、２６ｄ、２６ｅ、２６ｆ　コンタクト
３０ａ、３０ｂ、３０ｃ、３０ｄ　ゲート電極
３１Ｌ、３１Ｓ　デュアルゲート電極
４１Ｌ、４１Ｓ　ＰＮ境界
５１Ａ、５１Ｂ、５１Ｃ、５１Ｄ　マスクパターン
５２Ａ、５２Ｂ、５２Ｃ、５２Ｄ　マスクパターン
５３、５４　マスクパターン

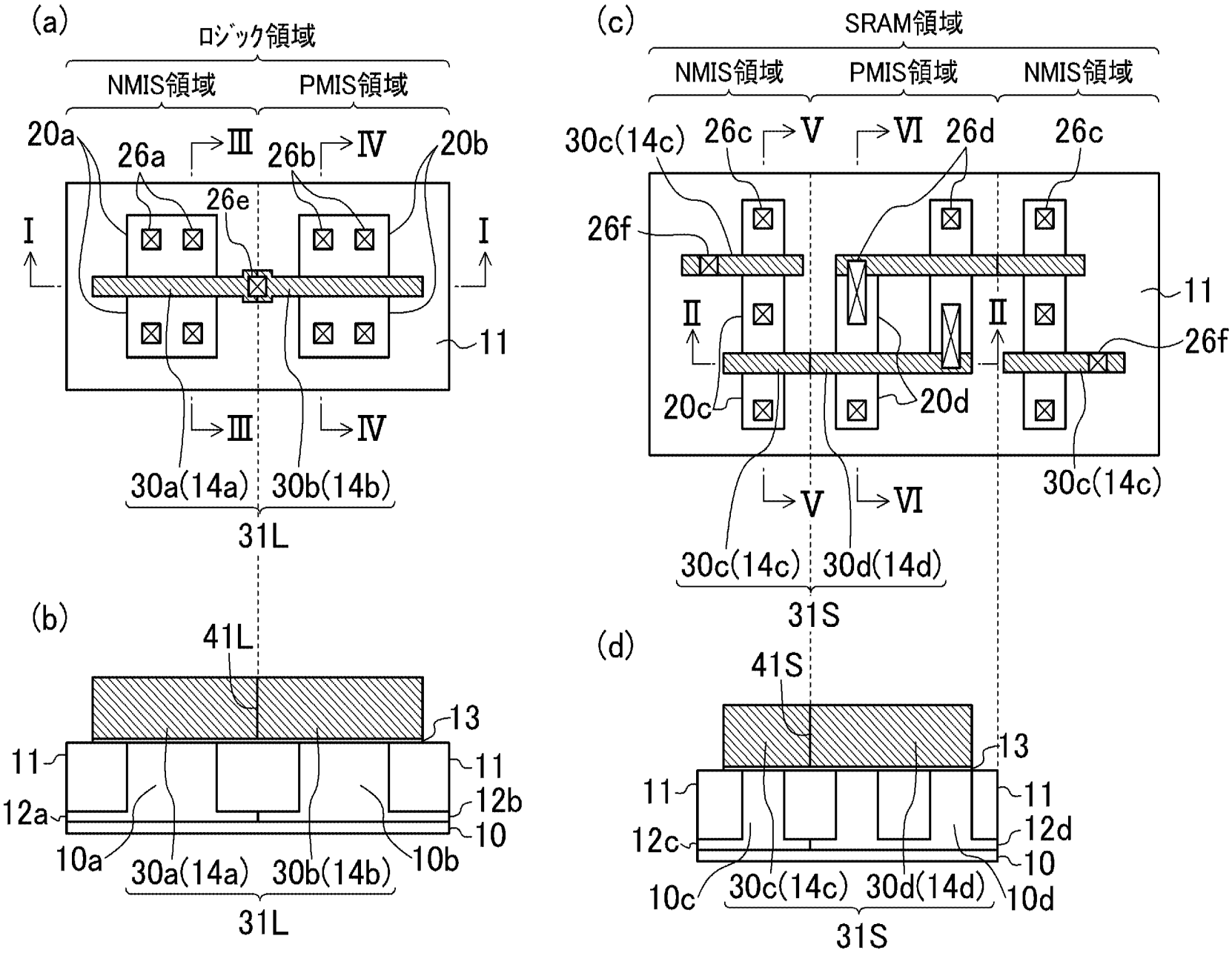
【書類名】特許請求の範囲
【請求項１】
第１のデュアルゲート電極と第２のデュアルゲート電極とを備えた半導体装置であって、
前記第１のデュアルゲート電極は、第１の活性領域上に形成された第１の第１導電型シリコン膜を含む第１のゲート電極と、第２の活性領域上に形成された第１の第２導電型シリコン膜を含む第２のゲート電極とを有し、
前記第２のデュアルゲート電極は、第３の活性領域上に形成された第２の第１導電型シリコン膜を含む第３のゲート電極と、第４の活性領域上に形成された第２の第２導電型シリコン膜を含む第４のゲート電極とを有し、
前記第１の活性領域と前記第２の活性領域とは素子分離領域を挟んで分離されており、
前記第１のゲート電極と前記第２のゲート電極とは前記素子分離領域上で接続しており、
前記第１の第１導電型シリコン膜の少なくとも一部分における第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度よりも高いことを特徴とする半導体装置。
【請求項２】
請求項１に記載の半導体装置において、
前記第１の活性領域と前記第２の活性領域との間の分離幅は、前記第３の活性領域と前記第４の活性領域との間の分離幅よりも大きいことを特徴とする半導体装置。
【請求項３】
請求項１又は２に記載の半導体装置において、
前記第１の第２導電型シリコン膜の少なくとも一部分における第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度と実質的に同じであることを特徴とする半導体装置。
【請求項４】
請求項１～３のいずれか１項に記載の半導体装置において、
前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度よりも高いことを特徴とする半導体装置。
【請求項５】
請求項１～４のいずれか１項に記載の半導体装置において、
前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度よりも低いことを特徴とする半導体装置。
【請求項６】
請求項１～５のいずれか１項に記載の半導体装置において、
前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度よりも低いことを特徴とする半導体装置。
【請求項７】
請求項１～６のいずれか１項に記載の半導体装置において、
前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度よりも低いことを特徴とする半導体装置。
【請求項８】
請求項１～４のいずれか１項に記載の半導体装置において、
前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度と実質的に同じであることを特徴とする半導体装置。

【請求項９】
請求項１～３のいずれか１項に記載の半導体装置において、
前記素子分離領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度よりも高いことを特徴とする半導体装置。
【請求項１０】
請求項１～３、９のいずれか１項に記載の半導体装置において、
前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度と実質的に同じであることを特徴とする半導体装置。
【請求項１１】
請求項１～３、９、１０のいずれか１項に記載の半導体装置において、
前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度よりも低いことを特徴とする半導体装置。
【請求項１２】
請求項１～３、９～１１のいずれか１項に記載の半導体装置において、
前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度と実質的に同じであることを特徴とする半導体装置。
【請求項１３】
請求項１～３、９～１２のいずれか１項に記載の半導体装置において、
前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記素子分離領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度よりも低いことを特徴とする半導体装置。
【請求項１４】
請求項１又は２に記載の半導体装置において、
前記第１の活性領域上に位置する部分の前記第１の第１導電型シリコン膜の第１導電型不純物濃度は、前記第３の活性領域上に位置する部分の前記第２の第１導電型シリコン膜の第１導電型不純物濃度よりも高く、
前記第２の活性領域上に位置する部分の前記第１の第２導電型シリコン膜の第２導電型不純物濃度は、前記第４の活性領域上に位置する部分の前記第２の第２導電型シリコン膜の第２導電型不純物濃度よりも高いことを特徴とする半導体装置。
【請求項１５】
請求項１～１４のいずれか１項に記載の半導体装置において、
前記第１のゲート電極は、第１のＰＭＩＳトランジスタのゲート電極であり、
前記第２のゲート電極は、第１のＮＭＩＳトランジスタのゲート電極であり、
前記第３のゲート電極は、第２のＰＭＩＳトランジスタのゲート電極であり、
前記第４のゲート電極は、第２のＮＭＩＳトランジスタのゲート電極であることを特徴とする半導体装置。
【請求項１６】
請求項１～１５のいずれか１項に記載の半導体装置において、
前記第１のゲート電極及び前記第２のゲート電極はそれぞれ、ロジック回路用トランジスタのゲート電極であり、
前記第３のゲート電極及び前記第４のゲート電極はそれぞれ、ＳＲＡＭ回路用トランジスタのゲート電極であることを特徴とする半導体装置。
【請求項１７】
第１の活性領域上に形成された第１のゲート電極及び第２の活性領域上に形成された第２のゲート電極を有する第１のデュアルゲート電極と、第３の活性領域上に形成された第３のゲート電極及び４の活性領域上に形成された第４のゲート電極とを有する第２のデュ

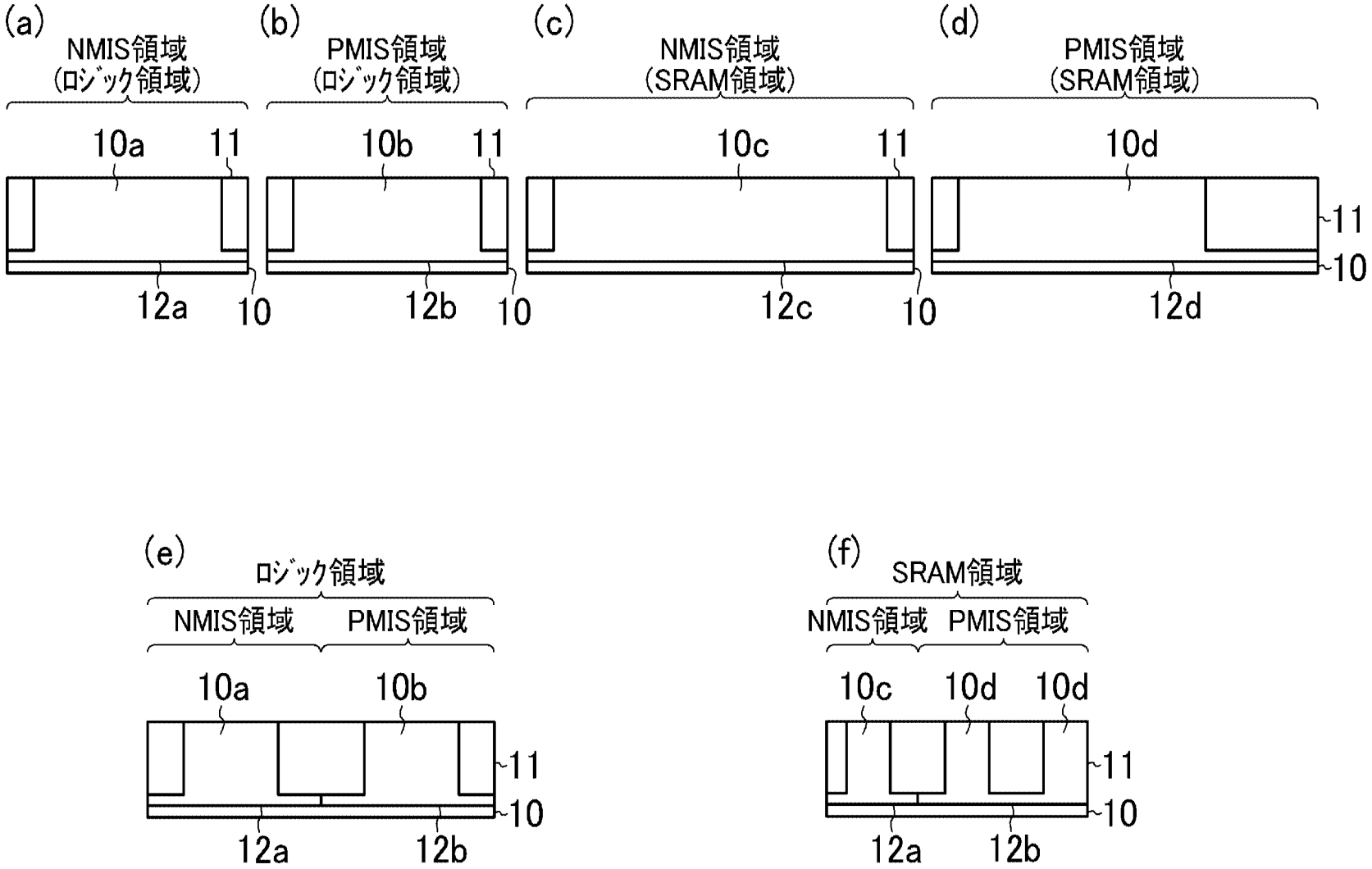
アルゲート電極とを備えた半導体装置の製造方法であって、
前記第１の活性領域、前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上にシリコン膜を形成する工程（ａ）と、
前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に位置する部分の前記シリコン膜を第１のマスクパターンによって覆いながら、前記シリコン膜に第１導電型不純物を導入する工程（ｂ）と、
前記第１の活性領域上に位置する部分の前記シリコン膜を第２のマスクパターンによって覆いながら、前記シリコン膜に第２導電型不純物を導入する工程（ｃ）と、
前記工程（ｂ）及び前記工程（ｃ）よりも後に、前記シリコン膜をパターニングし、それにより、前記第１の活性領域、前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に、前記シリコン膜をそれぞれ含む前記第１のゲート電極、前記第２のゲート電極、前記第３のゲート電極及び前記第４のゲート電極を形成する工程（ｄ）とを備えていることを特徴とする半導体装置の製造方法。
【請求項１８】
請求項１７に記載の半導体装置の製造方法において、
前記第１のマスクパターンは、前記第１の活性領域上に位置する部分の前記シリコン膜上に開口を有し、
前記第２のマスクパターンは、前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に位置する部分の前記シリコン膜上に開口を有することを特徴とする半導体装置の製造方法。
【請求項１９】
請求項１７に記載の半導体装置の製造方法において、
前記第１の活性領域と前記第２の活性領域とは素子分離領域によって電気的に分離されており、
前記工程（ａ）において、前記シリコン膜は前記素子分離領域上にも形成され、
前記第１のマスクパターンは、前記第１の活性領域上に位置する部分の前記シリコン膜を覆うと共に前記素子分離領域上に位置する部分の前記シリコン膜上に開口を有し、
前記第２のマスクパターンは、前記第２の活性領域上に位置する部分の前記シリコン膜を覆うと共に前記素子分離領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に位置する部分の前記シリコン膜上に開口を有することを特徴とする半導体装置の製造方法。
【請求項２０】
請求項１７に記載の半導体装置の製造方法において、
前記第１の活性領域と前記第２の活性領域とは素子分離領域によって電気的に分離されており、
前記工程（ａ）において、前記シリコン膜は前記素子分離領域上にも形成され、
前記第１のマスクパターンは、前記第１の活性領域上に位置する部分の前記シリコン膜を覆うと共に前記素子分離領域上に位置する部分の前記シリコン膜上に開口を有し、
前記第２のマスクパターンは、前記第２の活性領域、前記第３の活性領域及び前記第４の活性領域のそれぞれの上に位置する部分の前記シリコン膜を覆うと共に前記素子分離領域上に位置する部分の前記シリコン膜上に開口を有することを特徴とする半導体装置の製造方法。

【書類名】要約書
【要約】
【課題】ＣＭＩＳデュアルゲート構造を有する半導体装置において、ＰＮ境界近傍でのゲート寸法変動や不純物の相互拡散に起因する素子特性の変動を抑制する。
【解決手段】デュアルゲート電極３１Ｌは、活性領域１０ａ上に形成されたＮ型シリコン膜１４ａを含むゲート電極３０ａと、活性領域１０ｂ上に形成されたＰ型シリコン膜１４ｂを含むゲート電極３０ｂとを有する。デュアルゲート電極３１Ｓは、活性領域１０ｃ上に形成されたＮ型シリコン膜１４ｃを含むゲート電極３０ｃと、活性領域１０ｄ上に形成されたＰ型シリコン膜１４ｄを含むゲート電極３０ｄとを有する。Ｐ型シリコン膜１４ｂの少なくとも一部分におけるＰ型不純物濃度は、活性領域１０ｄ上に位置する部分のＰ型シリコン膜１４ｄのＰ型不純物濃度よりも高い。
【選択図】図１

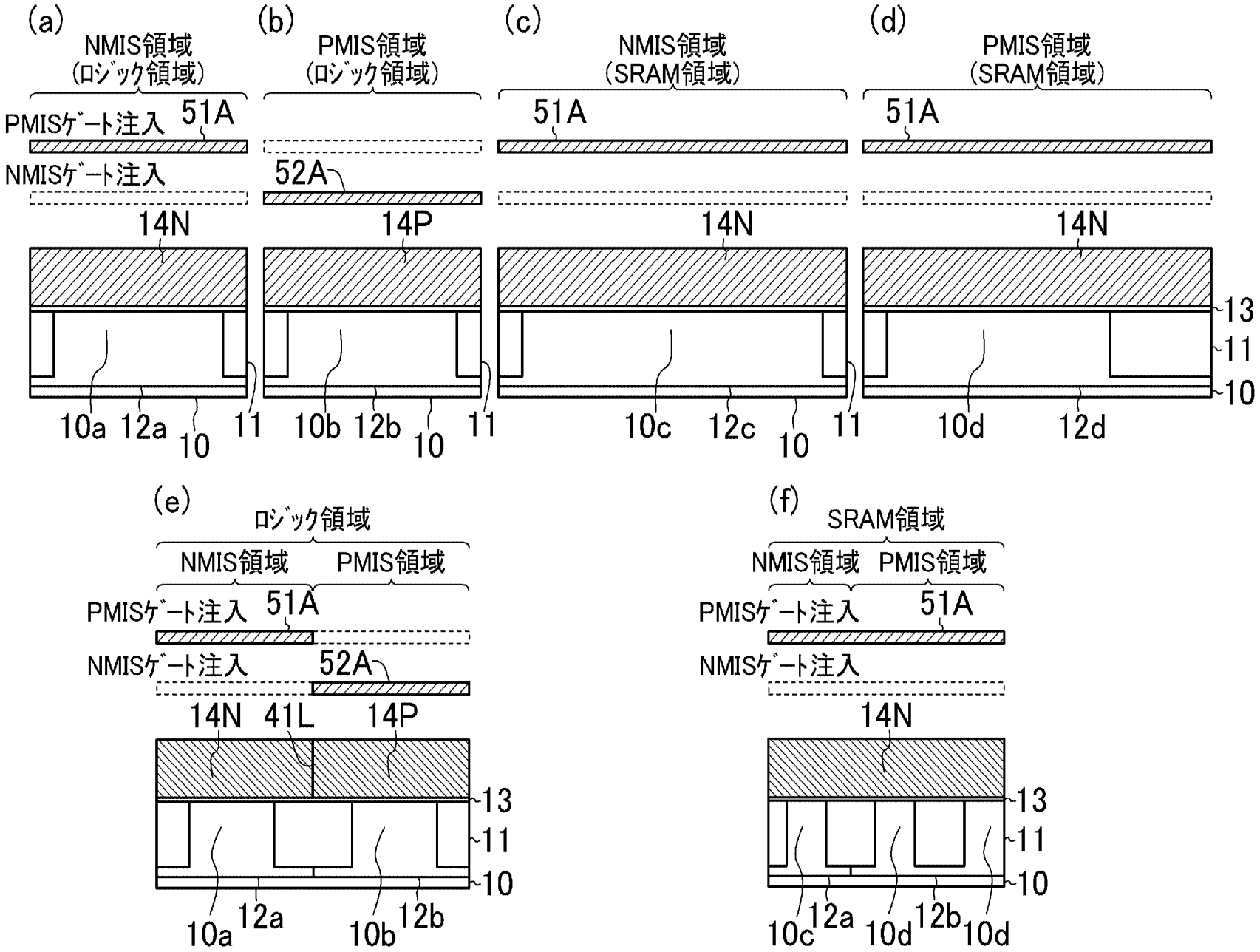
【書類名】図面
【図１】


(a)
ロジック領域
NMIS領域
PMIS領域
20a
26a
Ⅲ
26b
Ⅳ
20b
26e
I
I
11
Ⅲ
Ⅳ
30a(14a)
30b(14b)
31L
(b)
41L
13
11
11
12a
12b
10
10a
30a(14a)
30b(14b)
10b
31L
(c)
SRAM領域
NMIS領域
PMIS領域
NMIS領域
30c(14c)
26c
V
VI
26d
26c
26f
11
Ⅱ
Ⅱ
26f
20c
20d
V
VI
30c(14c)
30c(14c)
30d(14d)
31S
(d)
41S
13
11
11
12c
12d
10
10c
30c(14c)
30d(14d)
10d
31S

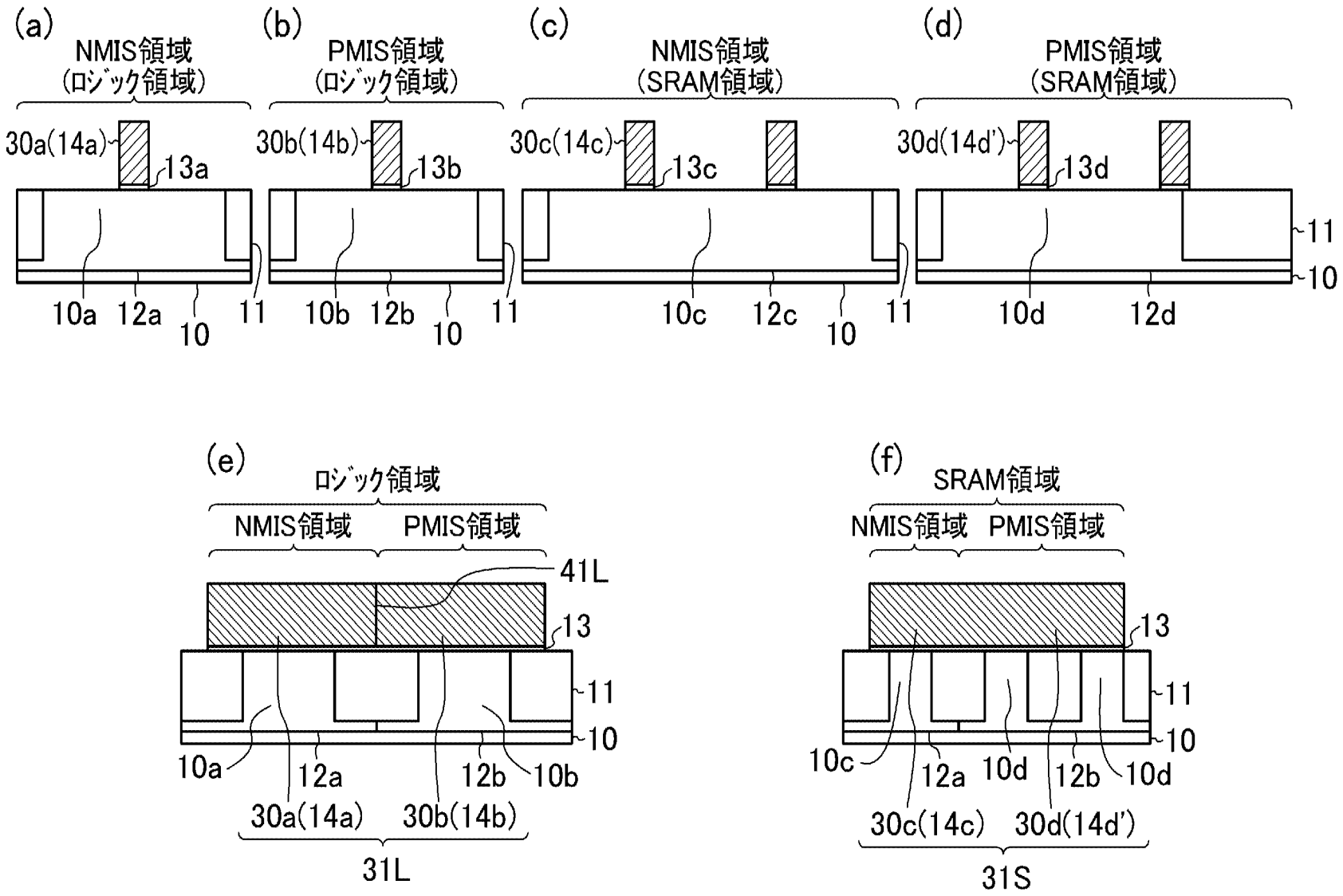
【図２】


(a)
NMIS領域
(ロジック領域)
10a
11
12a
10
(b)
PMIS領域
(ロジック領域)
10b
11
12b
10
(c)
NMIS領域
(SRAM領域)
10c
11
12c
10
(d)
PMIS領域
(SRAM領域)
10d
11
10
12d
(e)
ロジック領域
NMIS領域
PMIS領域
10a
10b
11
10
12a
12b
(f)
SRAM領域
NMIS領域
PMIS領域
10c
10d
10d
11
10
12a
12b

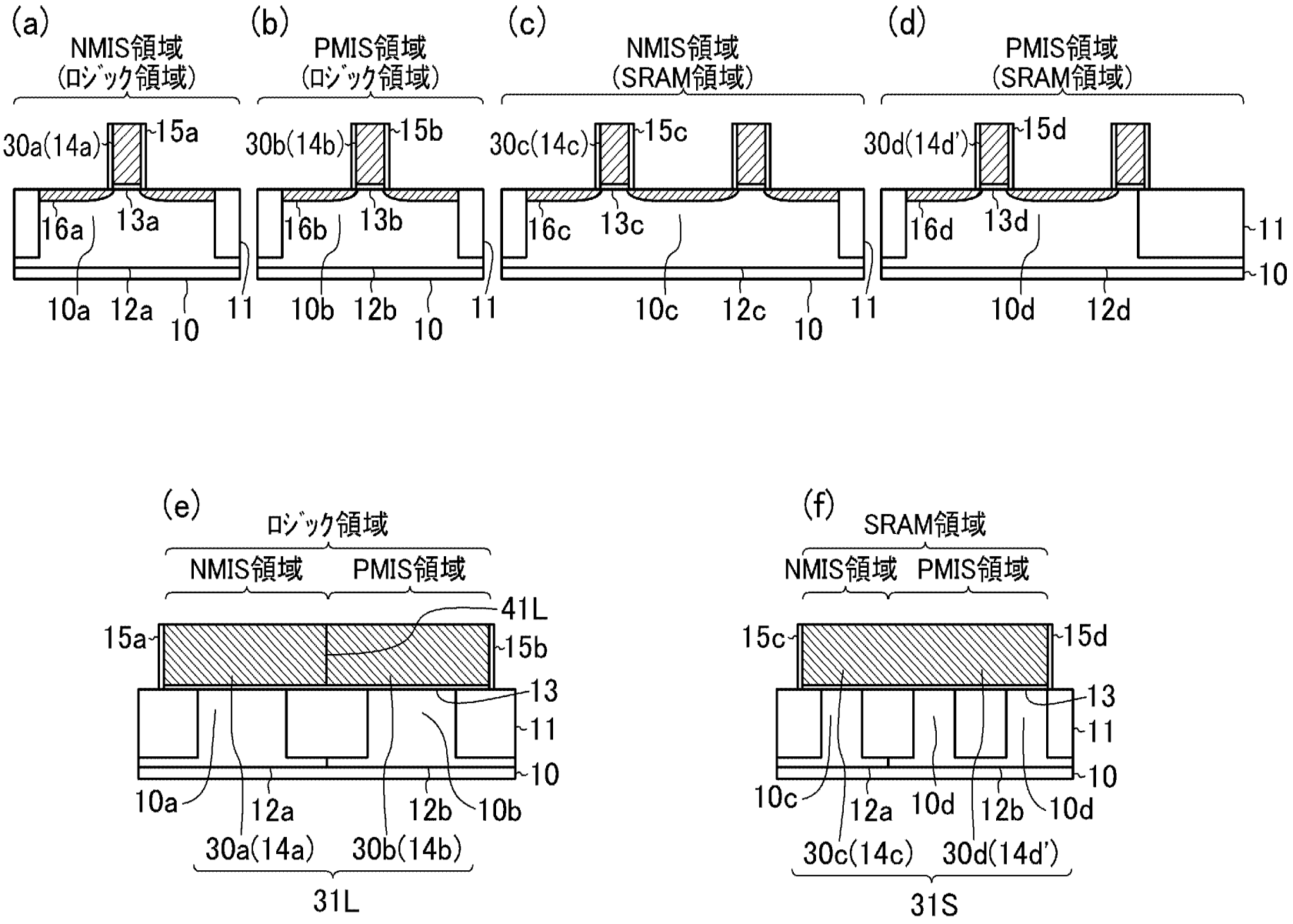
【図３】


(a)
NMIS領域
(ロジック領域)
PMISゲート注入
51A
NMISゲート注入
14N
10a
12a
10
11
(b)
PMIS領域
(ロジック領域)
52A
14P
10b
12b
10
11
(c)
NMIS領域
(SRAM領域)
51A
14N
10c
12c
10
11
(d)
PMIS領域
(SRAM領域)
51A
14N
10d
12d
13
11
10
(e)
ロジック領域
NMIS領域
PMIS領域
PMISゲート注入
51A
NMISゲート注入
52A
14N
41L
14P
10a
12a
10b
12b
13
11
10
(f)
SRAM領域
NMIS領域
PMIS領域
PMISゲート注入
51A
NMISゲート注入
14N
10c
12a
10d
12b
10d
13
11
10

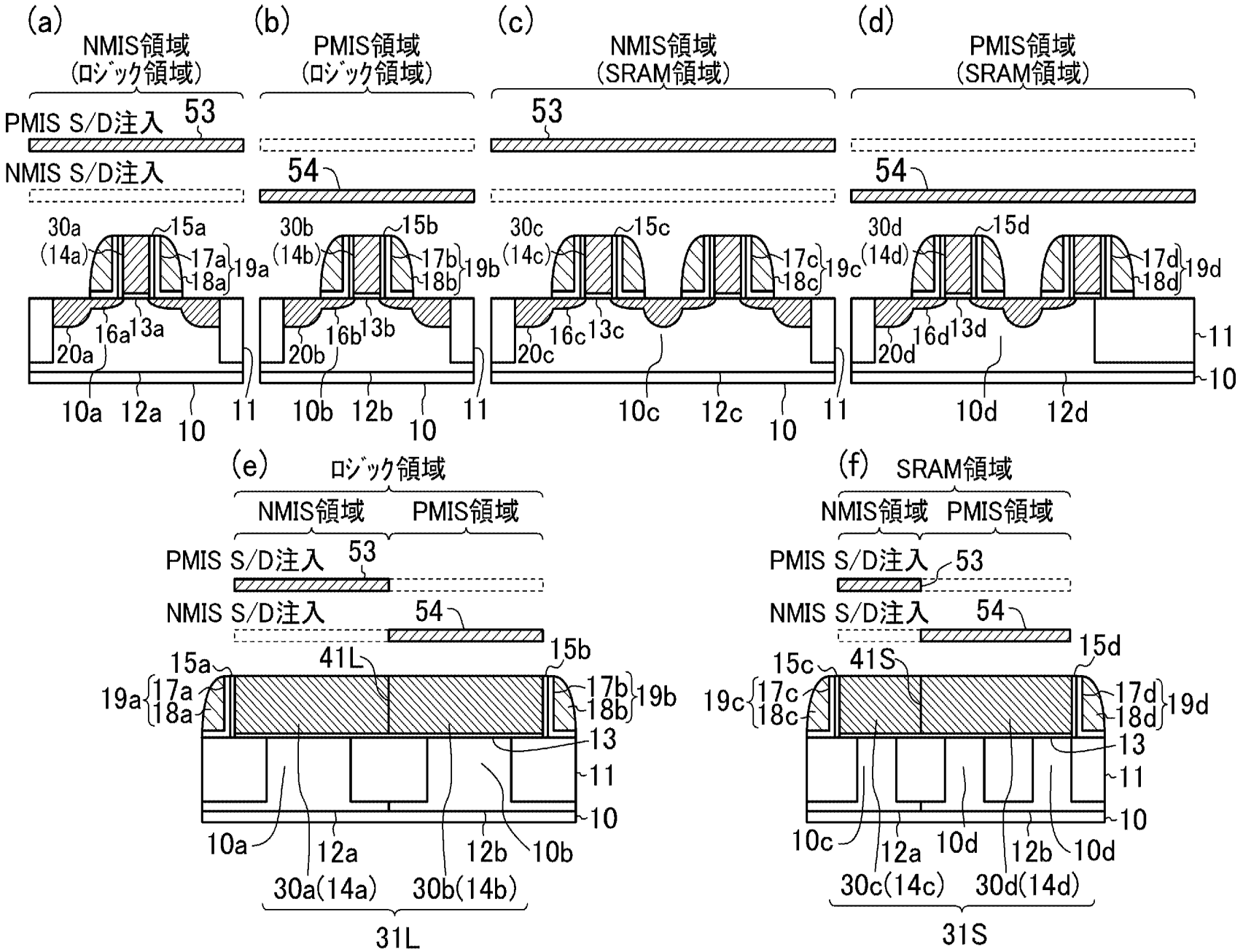
【図４】


(a)
NMIS領域
(ロジック領域)
30a(14a)
13a
10a
12a
10
11
(b)
PMIS領域
(ロジック領域)
30b(14b)
13b
10b
12b
10
11
(c)
NMIS領域
(SRAM領域)
30c(14c)
13c
10c
12c
10
11
(d)
PMIS領域
(SRAM領域)
30d(14d')
13d
10d
12d
11
10
(e)
ロジック領域
NMIS領域
PMIS領域
41L
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10a
12a
12b
10b
30a(14a)
30b(14b)
31L
(f)
SRAM領域
NMIS領域
PMIS領域
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10c
12a
10d
12b
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30c(14c)
30d(14d')
31S

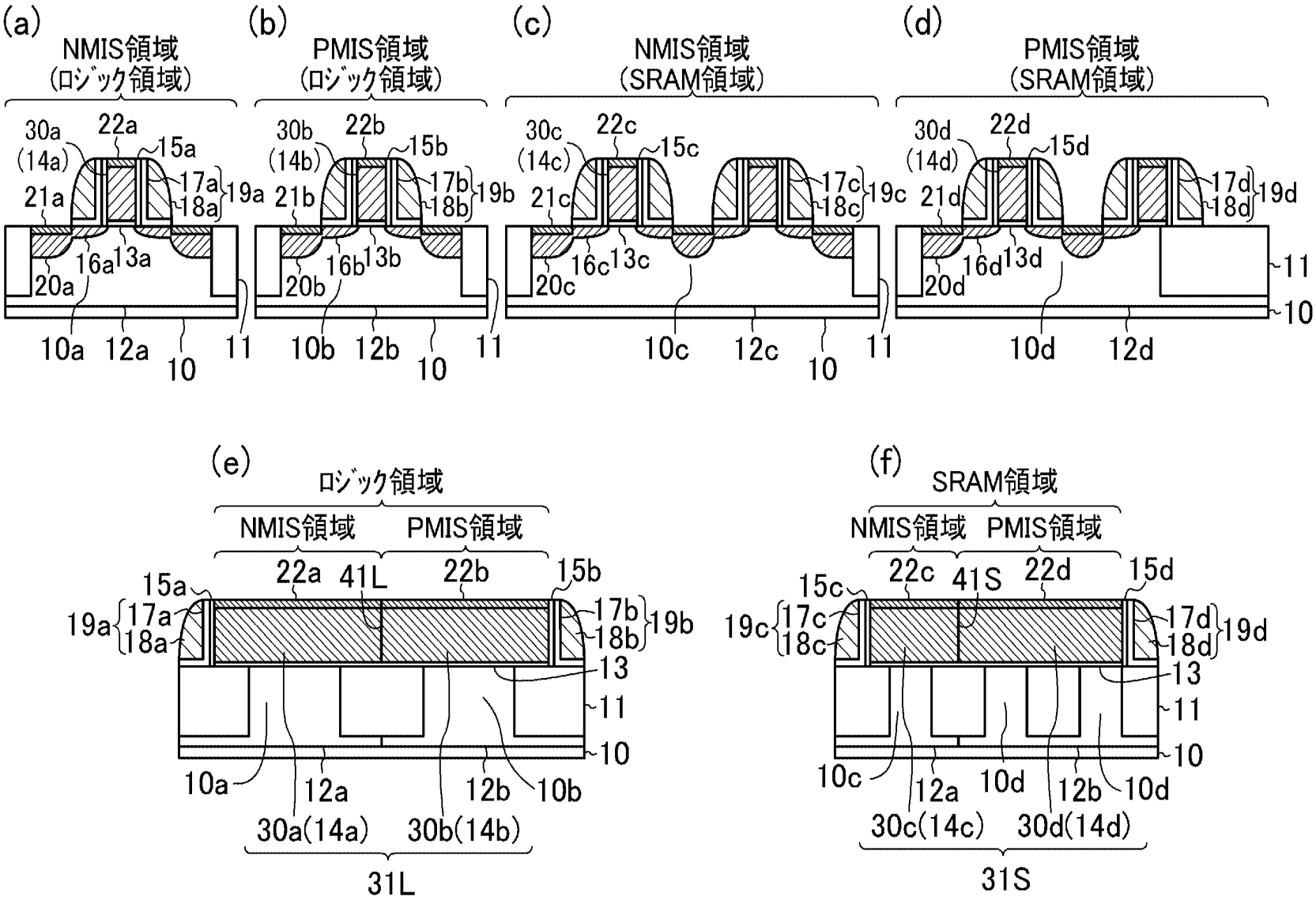
【図5】


(a)
NMIS領域
(ロジック領域)
(b)
PMIS領域
(ロジック領域)
(c)
NMIS領域
(SRAM領域)
(d)
PMIS領域
(SRAM領域)
30a(14a)
15a
30b(14b)
15b
30c(14c)
15c
30d(14d')
15d
16a
13a
16b
13b
16c
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16d
13d
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10a
12a
10
11
10b
12b
10
11
10c
12c
10
11
10d
12d
(e)
ロジック領域
NMIS領域
PMIS領域
41L
15a
15b
13
11
10
10a
12a
12b
10b
30a(14a)
30b(14b)
31L
(f)
SRAM領域
NMIS領域
PMIS領域
15c
15d
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10c
12a
10d
12b
10d
30c(14c)
30d(14d')
31S

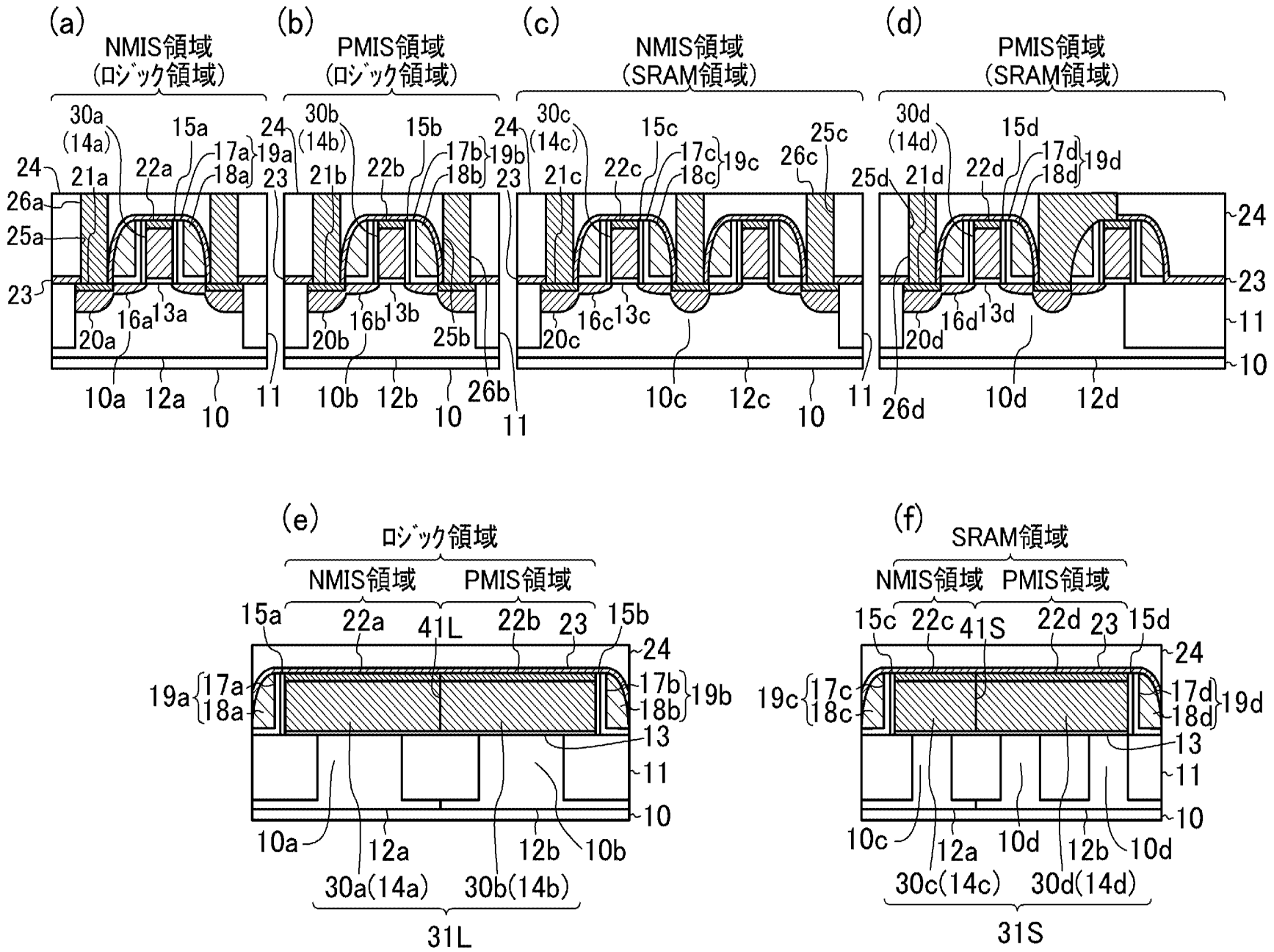
【図6】


(a)
NMIS領域
(ロジック領域)
PMIS S/D注入
53
NMIS S/D注入
30a
(14a)
15a
17a
18a
19a
16a
13a
20a
10a
12a
10
11
(b)
PMIS領域
(ロジック領域)
54
30b
(14b)
15b
17b
18b
19b
16b
13b
20b
10b
12b
10
11
(c)
NMIS領域
(SRAM領域)
53
30c
(14c)
15c
17c
18c
19c
16c
13c
20c
10c
12c
10
11
(d)
PMIS領域
(SRAM領域)
54
30d
(14d)
15d
17d
18d
19d
16d
13d
20d
10d
12d
11
10
(e)
ロジック領域
NMIS領域
PMIS領域
PMIS S/D注入
53
NMIS S/D注入
54
15a
41L
15b
19a
17a
18a
17b
18b
19b
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11
10
10a
12a
12b
10b
30a(14a)
30b(14b)
31L
(f)
SRAM領域
NMIS領域
PMIS領域
PMIS S/D注入
53
NMIS S/D注入
54
15c
41S
15d
19c
17c
18c
17d
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12a
10d
12b
10d
30c(14c)
30d(14d)
31S

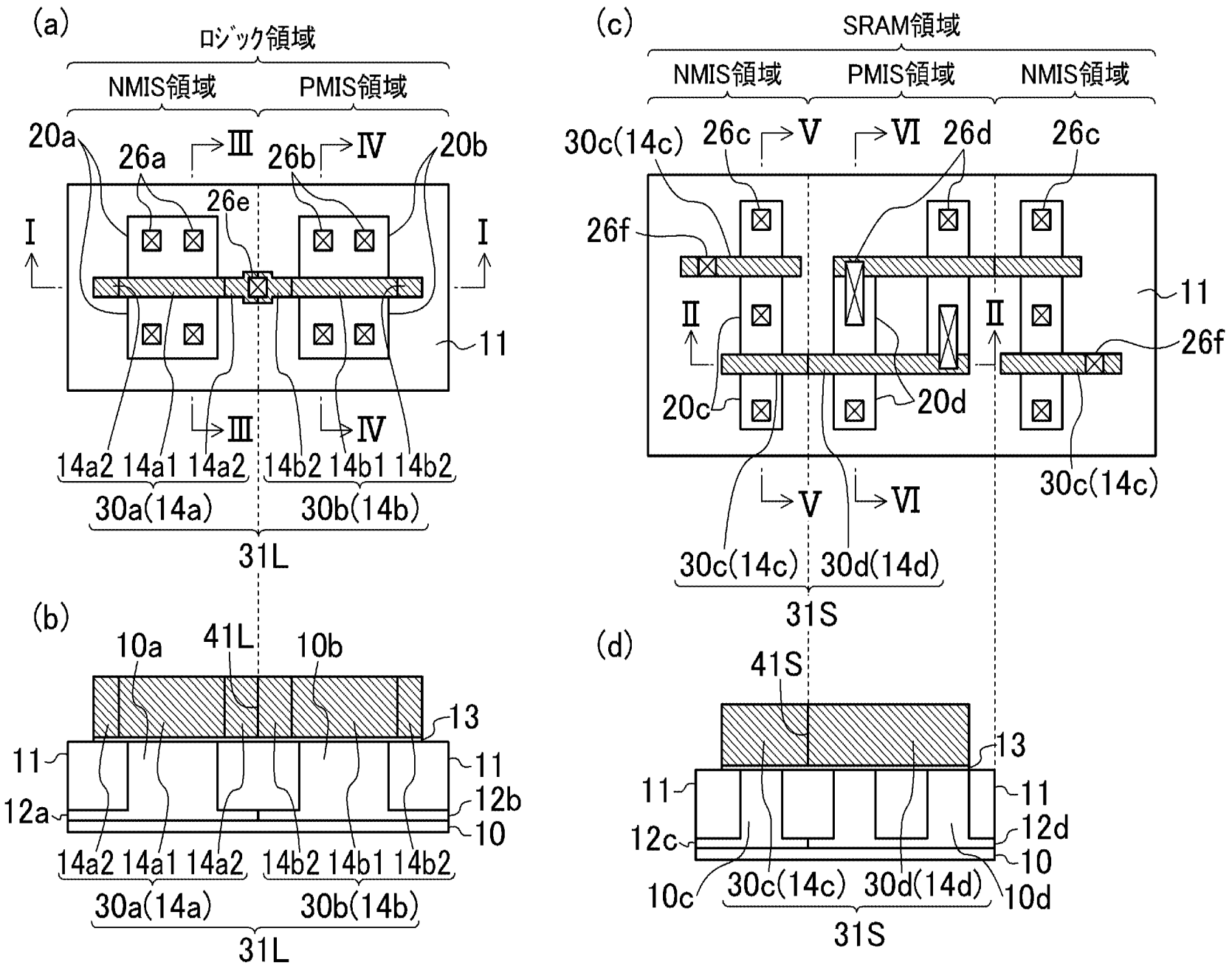
【図７】


(a)
NMIS領域
(ロジック領域)
(b)
PMIS領域
(ロジック領域)
(c)
NMIS領域
(SRAM領域)
(d)
PMIS領域
(SRAM領域)
30a
(14a)
22a
15a
17a
18a
19a
21a
16a
13a
20a
10a
12a
10
11
30b
(14b)
22b
15b
17b
18b
19b
21b
16b
13b
20b
10b
12b
30c
(14c)
22c
15c
17c
18c
19c
21c
16c
13c
20c
10c
12c
30d
(14d)
22d
15d
17d
18d
19d
21d
16d
13d
20d
10d
12d
(e)
ロジック領域
NMIS領域
PMIS領域
22a
41L
22b
15a
15b
17a
18a
17b
18b
19a
19b
13
11
10
10a
12a
12b
10b
30a(14a)
30b(14b)
31L
(f)
SRAM領域
NMIS領域
PMIS領域
22c
41S
22d
15c
15d
17c
18c
17d
18d
19c
19d
13
11
10
10c
12a
10d
12b
10d
30c(14c)
30d(14d)
31S

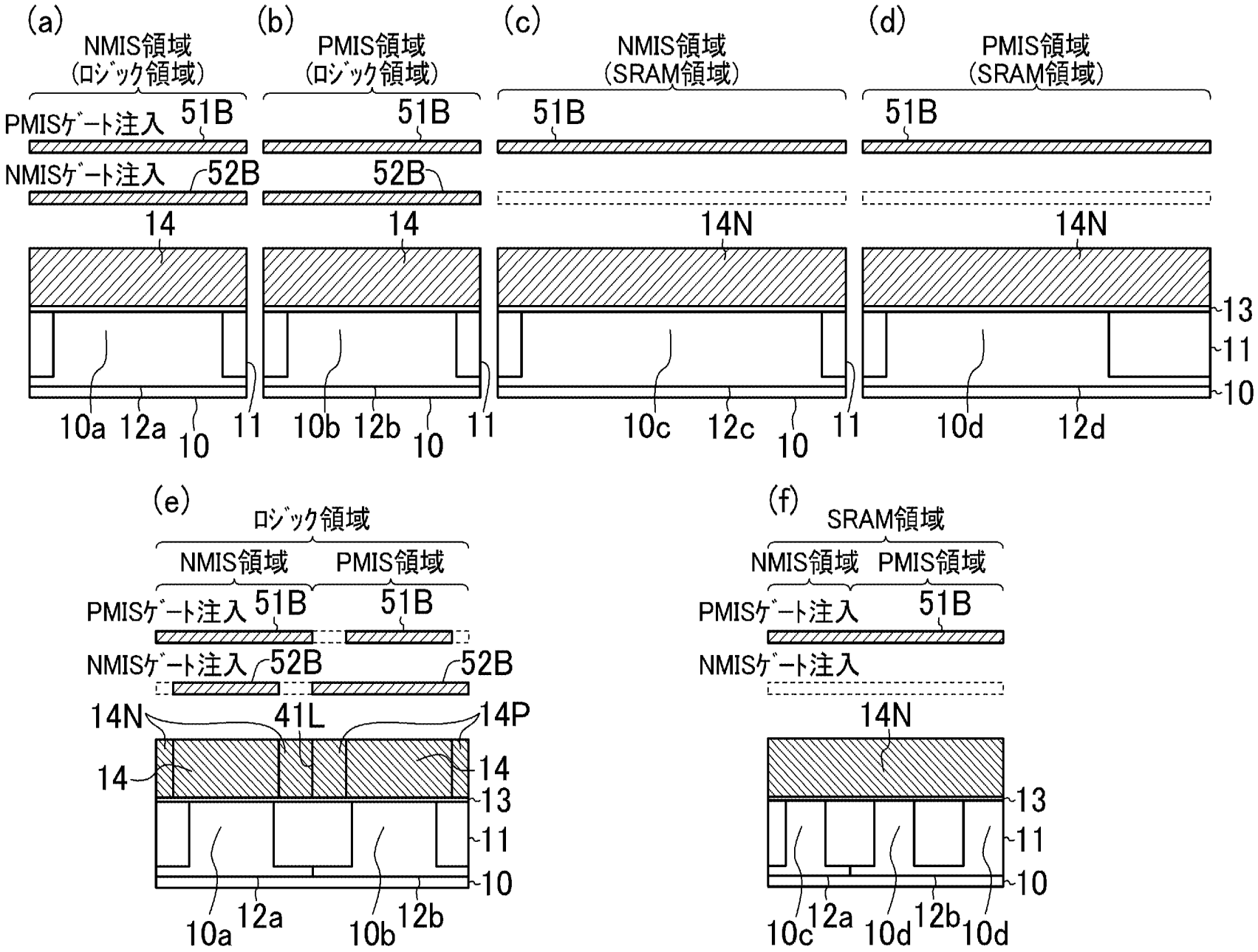
【図８】


(a)
NMIS領域
(ロジック領域)
(b)
PMIS領域
(ロジック領域)
(c)
NMIS領域
(SRAM領域)
(d)
PMIS領域
(SRAM領域)
(e)
ロジック領域
NMIS領域
PMIS領域
(f)
SRAM領域
NMIS領域
PMIS領域
31L
31S

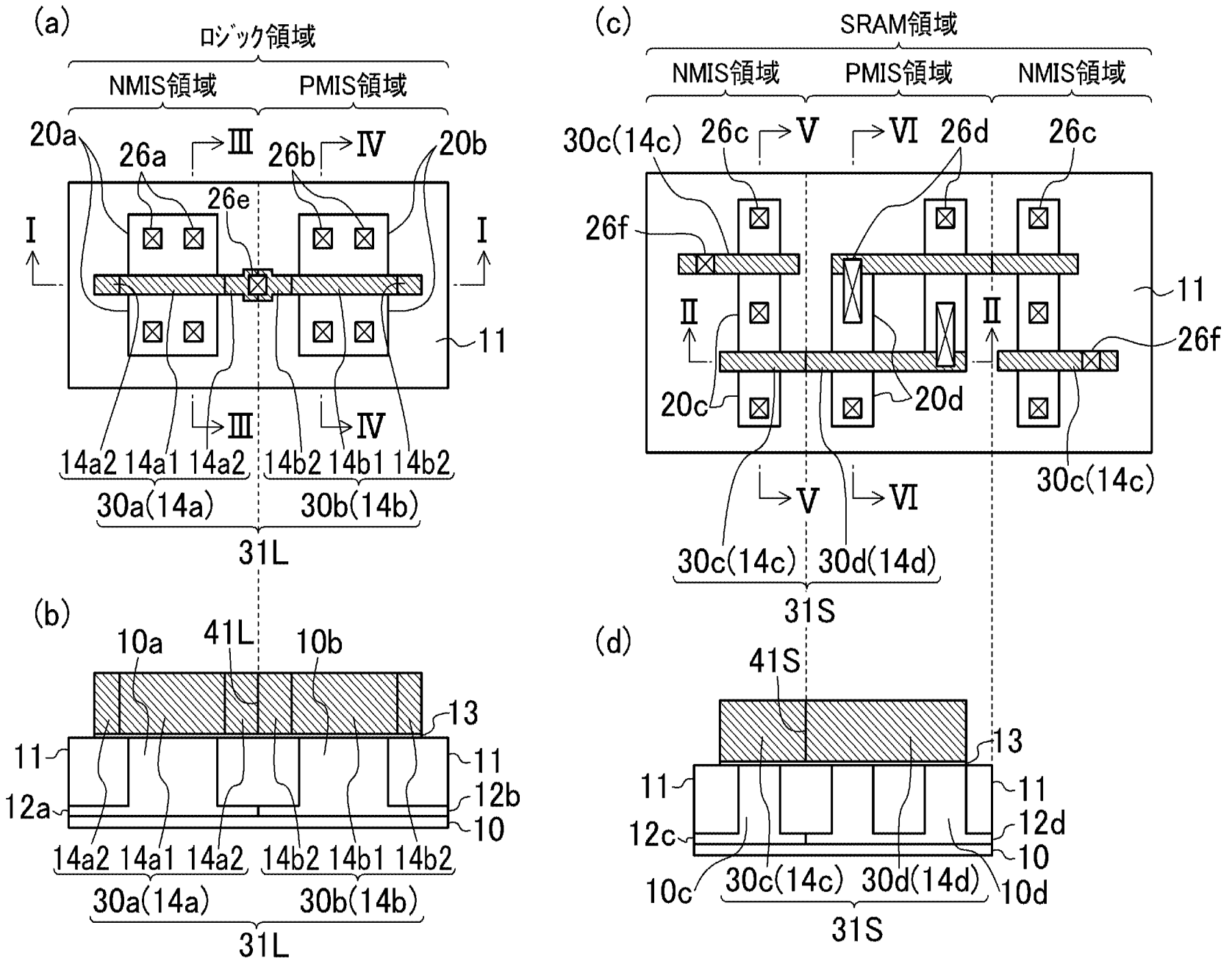
【図９】


(a)
ロジック領域
NMIS領域
PMIS領域
20a
26a
Ⅲ
26b
Ⅳ
20b
26e
I
I
11
Ⅲ
Ⅳ
14a2 14a1 14a2
14b2 14b1 14b2
30a(14a)
30b(14b)
31L
(b)
10a
41L
10b
13
11
11
12a
12b
10
14a2 14a1 14a2
14b2 14b1 14b2
30a(14a)
30b(14b)
31L
(c)
SRAM領域
NMIS領域
PMIS領域
NMIS領域
30c(14c)
26c
V
VI
26d
26c
26f
11
Ⅱ
Ⅱ
26f
20c
20d
30c(14c)
V
VI
30c(14c)
30d(14d)
31S
(d)
41S
13
11
11
12c
12d
10
10c
30c(14c)
30d(14d)
10d
31S

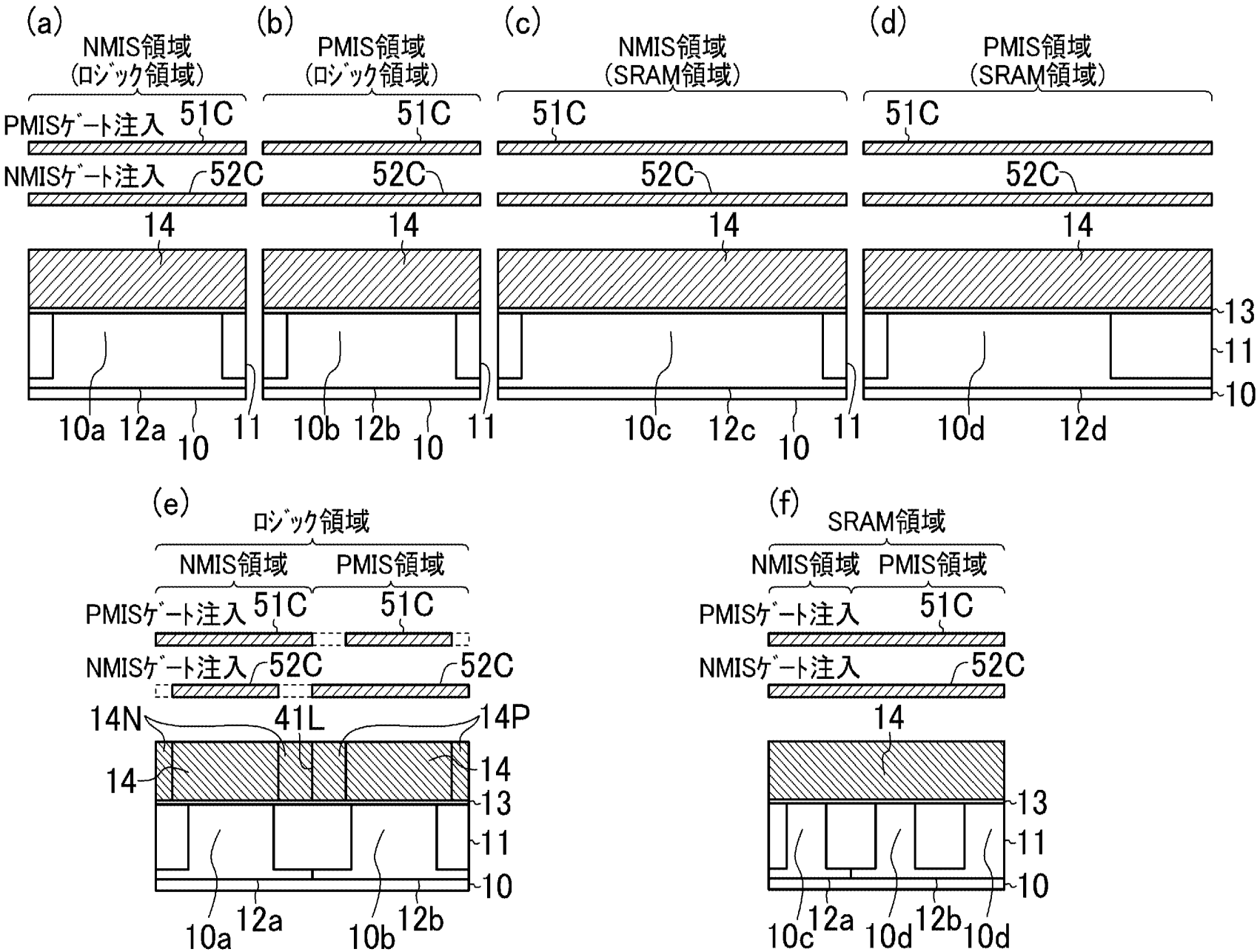
【図１０】


(a)
NMIS領域
(ロジック領域)
PMISゲート注入
51B
NMISゲート注入
52B
14
10a
12a
10
11
(b)
PMIS領域
(ロジック領域)
51B
52B
14
10b
12b
10
11
(c)
NMIS領域
(SRAM領域)
51B
14N
10c
12c
10
11
(d)
PMIS領域
(SRAM領域)
51B
14N
10d
12d
13
11
10
(e)
ロジック領域
NMIS領域
PMIS領域
PMISゲート注入
51B
51B
NMISゲート注入
52B
52B
14N
41L
14P
14
14
13
11
10
10a
12a
10b
12b
(f)
SRAM領域
NMIS領域
PMIS領域
PMISゲート注入
51B
NMISゲート注入
14N
13
11
10
10c
12a
10d
12b
10d

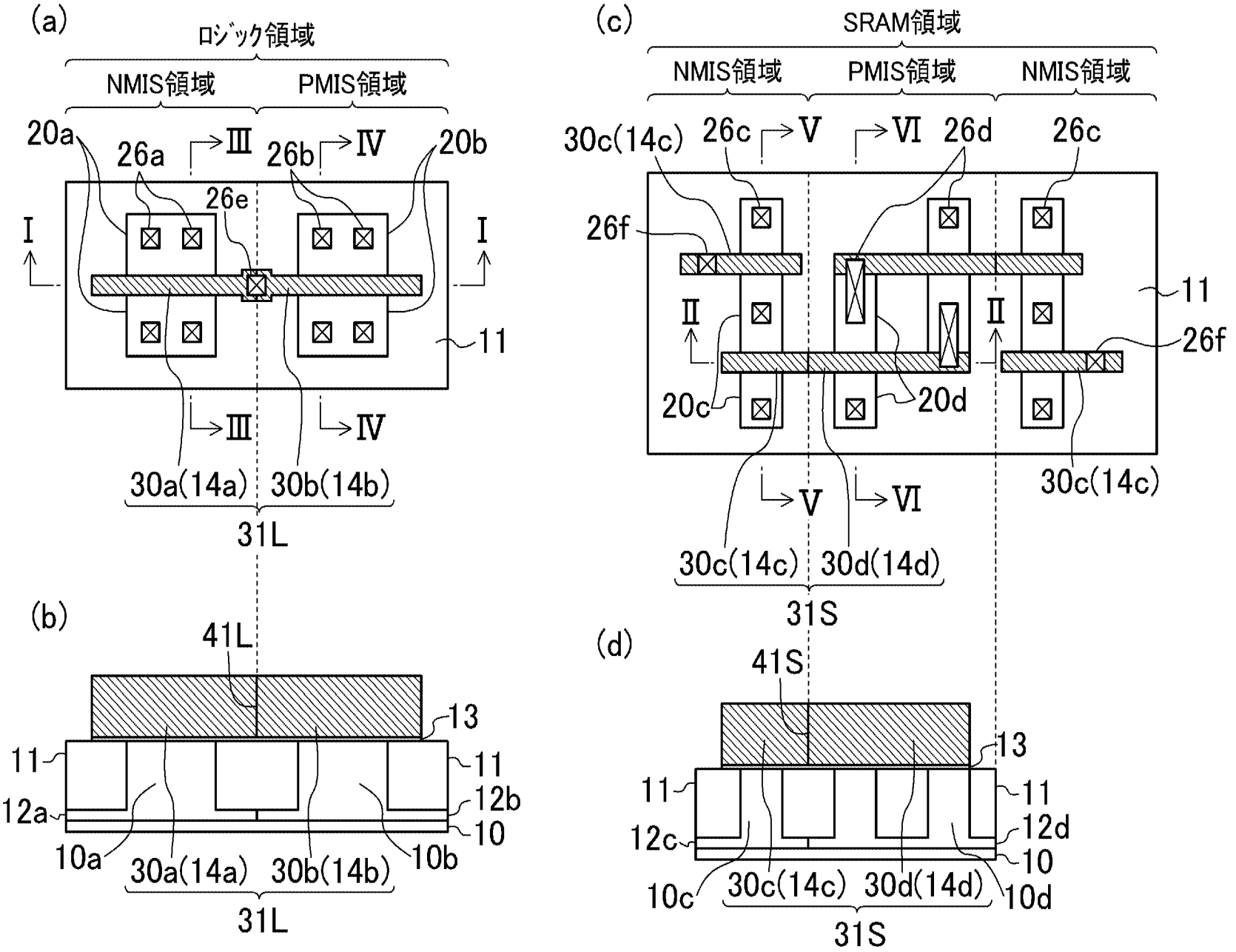
【図１１】


(a)
ロジック領域
NMIS領域
PMIS領域
20a
26a
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26b
Ⅳ
20b
26e
I
I
11
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14a2 14a1 14a2
14b2 14b1 14b2
30a(14a)
30b(14b)
31L
(b)
10a
41L
10b
13
11
11
12a
12b
10
14a2 14a1 14a2
14b2 14b1 14b2
30a(14a)
30b(14b)
31L
(c)
SRAM領域
NMIS領域
PMIS領域
NMIS領域
30c(14c)
26c
V
VI
26d
26c
26f
11
Ⅱ
Ⅱ
26f
20c
20d
30c(14c)
V
VI
30c(14c)
30d(14d)
31S
(d)
41S
13
11
11
12c
12d
10
10c
30c(14c)
30d(14d)
10d
31S

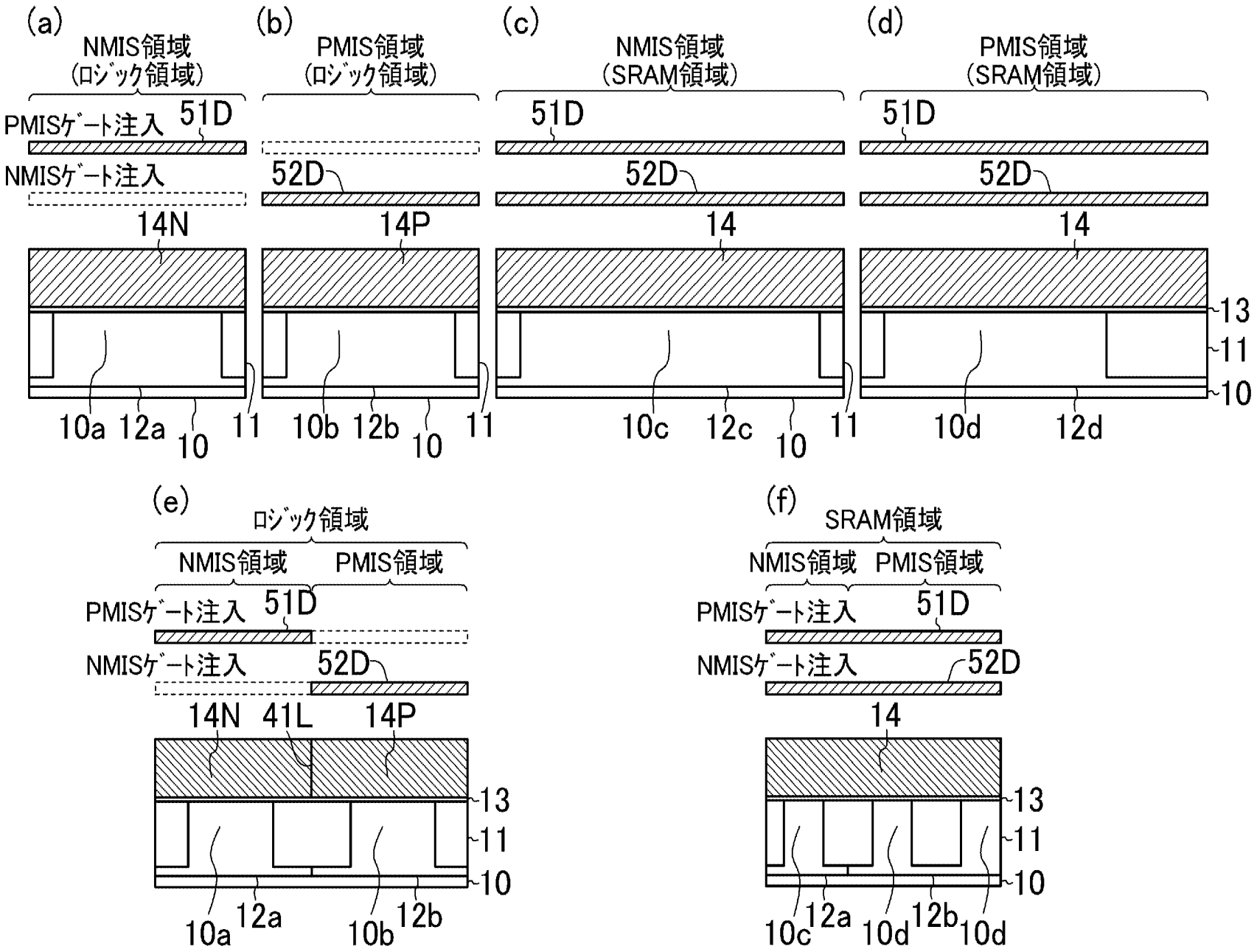
【図１２】


(a)
NMIS領域
(ロジック領域)
PMISゲート注入
51C
NMISゲート注入
52C
14
10a
12a
10
11
(b)
PMIS領域
(ロジック領域)
51C
52C
14
10b
12b
10
11
(c)
NMIS領域
(SRAM領域)
51C
52C
14
10c
12c
10
11
(d)
PMIS領域
(SRAM領域)
51C
52C
14
10d
12d
13
11
10
(e)
ロジック領域
NMIS領域
PMIS領域
PMISゲート注入
51C
51C
NMISゲート注入
52C
52C
14N
41L
14P
14
14
13
11
10
10a
12a
10b
12b
(f)
SRAM領域
NMIS領域
PMIS領域
PMISゲート注入
51C
NMISゲート注入
52C
14
13
11
10
10c
12a
10d
12b
10d

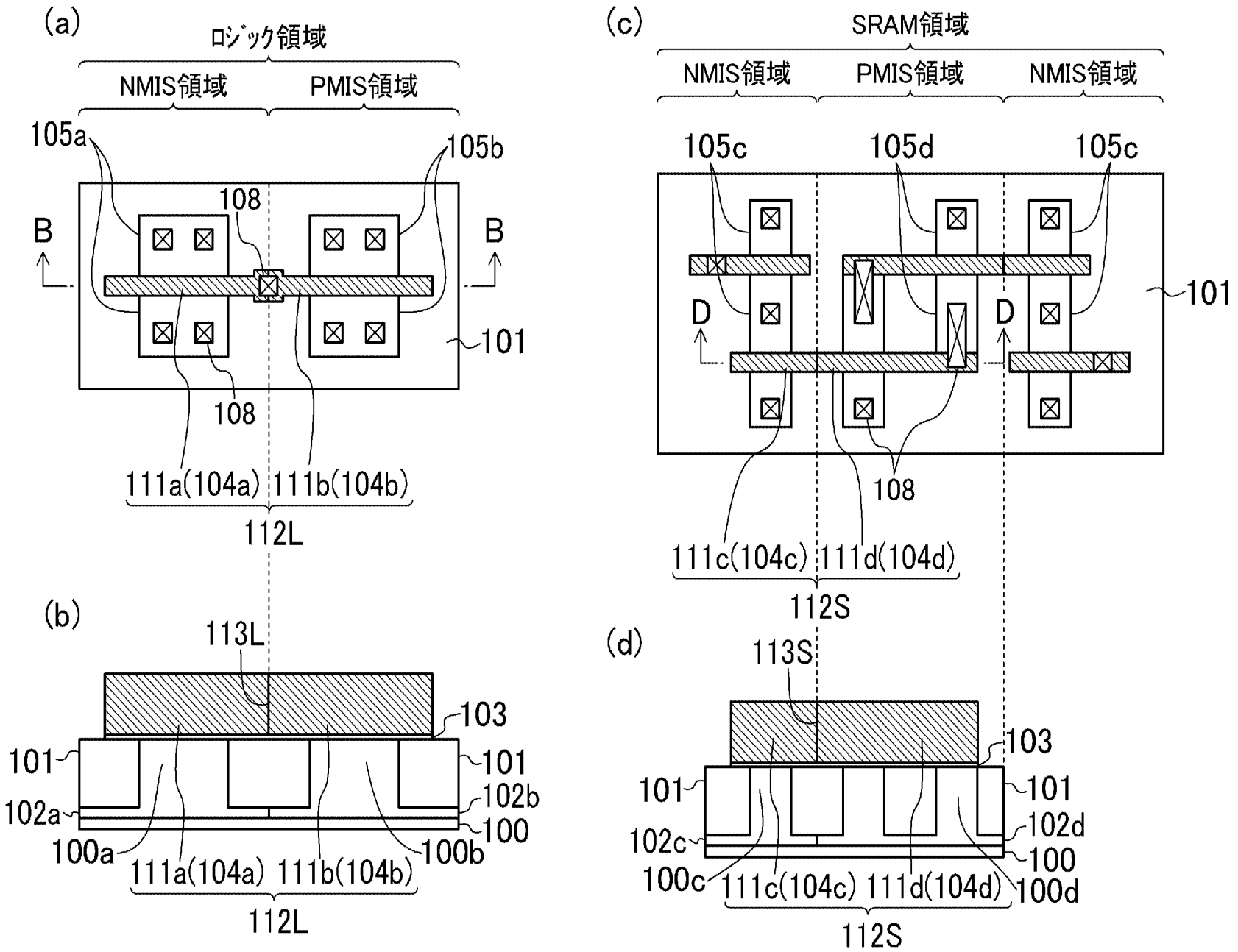
【図１３】


(a)
ロジック領域
NMIS領域
PMIS領域
20a
26a
Ⅲ
26b
Ⅳ
20b
26e
I
I
11
Ⅲ
Ⅳ
30a(14a)
30b(14b)
31L
(b)
41L
13
11
11
12a
12b
10
10a
30a(14a)
30b(14b)
10b
31L
(c)
SRAM領域
NMIS領域
PMIS領域
NMIS領域
30c(14c)
26c
V
Ⅵ
26d
26c
26f
11
Ⅱ
Ⅱ
26f
20c
20d
30c(14c)
V
Ⅵ
30c(14c)
30d(14d)
31S
(d)
41S
13
11
11
12c
12d
10
10c
30c(14c)
30d(14d)
10d
31S

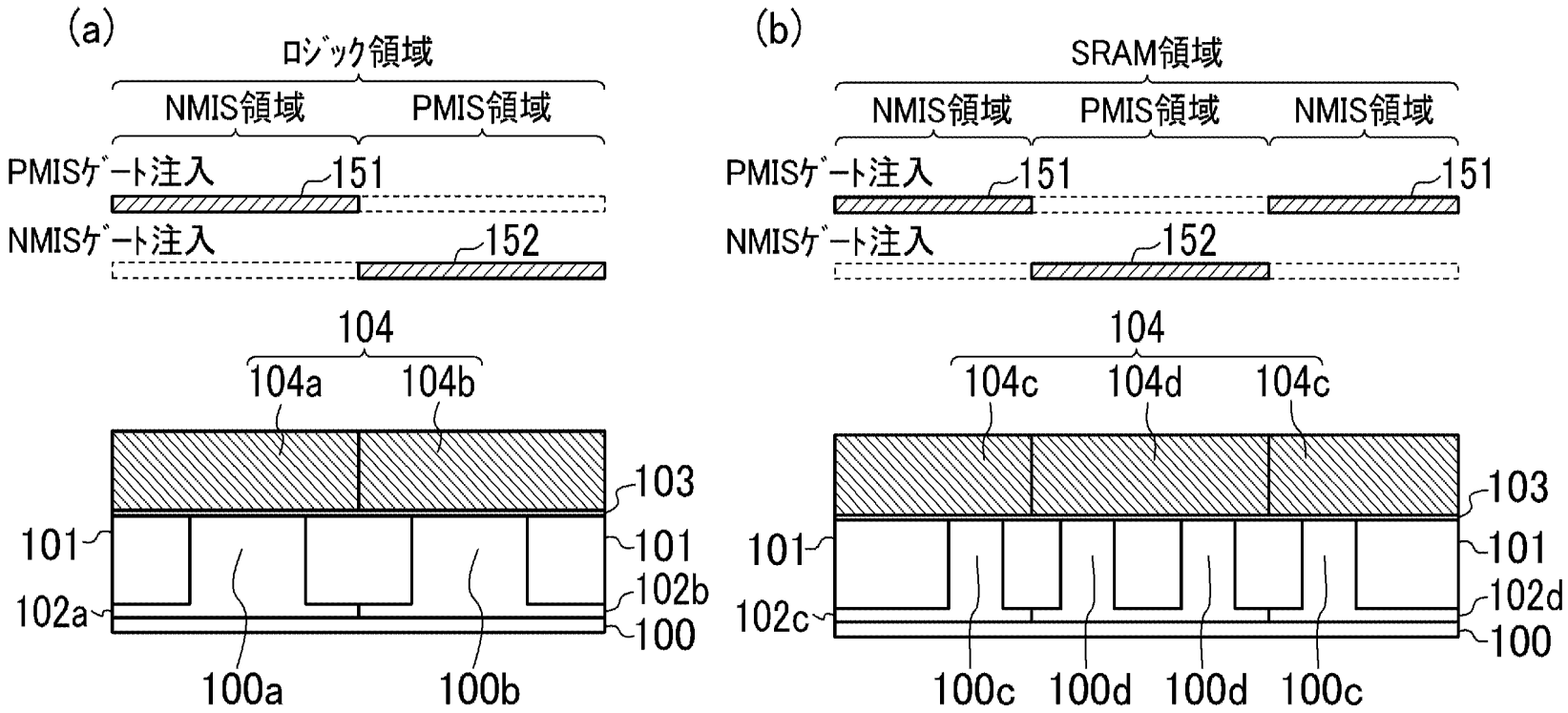
【図１４】


(a)
NMIS領域
(ロジック領域)
PMISゲート注入
51D
NMISゲート注入
14N
(b)
PMIS領域
(ロジック領域)
52D
14P
(c)
NMIS領域
(SRAM領域)
51D
52D
14
(d)
PMIS領域
(SRAM領域)
51D
52D
14
13
11
10
10a
12a
10
11
10b
12b
10
11
10c
12c
10
11
10d
12d
(e)
ロジック領域
NMIS領域
PMIS領域
PMISゲート注入
51D
NMISゲート注入
52D
14N
41L
14P
13
11
10
10a
12a
10b
12b
(f)
SRAM領域
NMIS領域
PMIS領域
PMISゲート注入
51D
NMISゲート注入
52D
14
13
11
10
10c
12a
10d
12b
10d

【図15】


(a)
ロジック領域
NMIS領域
PMIS領域
105a
105b
108
B
B
101
108
111a(104a)
111b(104b)
112L
(b)
113L
103
101
101
102a
102b
100
100a
100b
111a(104a)
111b(104b)
112L
(c)
SRAM領域
NMIS領域
PMIS領域
NMIS領域
105c
105d
105c
D
D
101
108
111c(104c)
111d(104d)
112S
(d)
113S
103
101
101
102c
102d
100
100c
100d
111c(104c)
111d(104d)
112S

【図16】


(a)
ロジック領域
NMIS領域
PMIS領域
PMISゲート注入
151
NMISゲート注入
152
104
104a
104b
103
101
101
102b
102a
100
100a
100b
(b)
SRAM領域
NMIS領域
PMIS領域
NMIS領域
PMISゲート注入
151
151
NMISゲート注入
152
104
104c
104d
104c
103
101
101
102d
102c
100
100c
100d
100d
100c

出願人履歴

０００００５８２１

20081001

名称変更

５０６１７８４４９

大阪府門真市大字門真１００６番地

パナソニック株式会社

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935

CONFIRMATION NO. 4442

53080
MCDERMOTT WILL & EMERY LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

PUBLICATION NOTICE

OC000000059713833

Title:SEMICONDUCTOR DEVICE

Publication No.US-2013-0056832-A1
Publication Date:03/07/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935	4442

53080 7590 10/24/2013

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER	
NGUYEN, LAWRENCE-LIN T	
ART UNIT	PAPER NUMBER
2897	

NOTIFICATION DATE	DELIVERY MODE
10/24/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

Office Action Summary	Application No. 13/665,376	Applicant(s) SATO ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☐ Claim(s) _____ is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-16* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species:

I. Species **I**, as disclosed, is pertaining to the second embodiments, FIGs 9-10.

II. Species **II**, as disclosed, is pertaining to the third embodiment, FIGs 11-12.

III. Species **III**, as disclosed, is pertaining to the fourth embodiments, FIGs 13-14.

FIG.s **1-8** is common to species **I**, **II**, or **III**.

2. The species are independent or distinct, each from the other because of the following reasons:

I. Species **I** in this case, as a feature of this embodiment is that the p-type silicon film 14b1 has a p-type impurity concentration lower than that of the p-type silicon film 14b2. In addition, each of the p-type silicon film 14b1 and the p-type silicon film 14b2 has a p-type impurity concentration higher than that of the p-type silicon film 14d. The n-type silicon film 14a1 has an n-type impurity concentration lower than that of each of the n-type silicon film 14a2 and the n-

type silicon film 14c. The n-type silicon film 14a2 has an n-type impurity concentration substantially equal to that of the n-type silicon film 14c.

II. Species **II** in this case, as a feature of this embodiment is that the p-type silicon film 14b2 has a p-type impurity concentration higher than that of the p-type silicon film 14d and that the p-type silicon film 14b1 has a p-type impurity concentration substantially equal to that of the p-type silicon film 14d. Specifically, the p-type silicon film 14b1 has a p-type impurity concentration lower than that of the p-type silicon film 14b2. The n-type silicon film 14a1 has an n-type impurity concentration substantially equal to that of the n-type silicon film 14c. The n-type silicon film 14a1 has an n-type impurity concentration lower than that of the n-type silicon film 14a2. Specifically, the n-type silicon film 14a2 has an n-type impurity concentration lower than that of the n-type silicon film 14c.

III. Species **III** in this case, as a feature of this embodiment is that the p-type silicon film 14b has a p-type impurity concentration higher than that of the p-type silicon film 14d and that the n-type silicon film 14a has an n-type impurity concentration higher than that of the n-type silicon film 14c.

3. In addition, these species are not obvious variants of each other based on the current record.

4. Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, Figures 1-8 appears to be generic.

5. There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s) apply:

The species or groupings of patentably indistinct species require a different field of search (e.g., searching different classes /subclasses or electronic resources, or employing different search strategies or search queries) and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

6. **Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or a grouping of patentably indistinct species to be examined** even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

7. The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are

added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

8. Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

9. Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

10. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAWRENCE-LINH T. NGUYEN whose telephone number is (571) 272-6267. The examiner can normally be reached on M-F (8AM - 4PM EST).

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on (571) 272-1867. The fax phone number for the organization where this application or proceeding is assigned is (571) 272-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (in USA or CANADA) or (571) 272-1000.

/Lawrence-Linh T Nguyen/
Examiner, Art Unit 2897

/Fernando L. Toledo/
Supervisory Patent Examiner, Art Unit 2897

Docket No.: 085393-0935
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Yoshihiro SATO et al.	:	Customer Number: 53080
Application No.: 13/665,376	:	Confirmation No.: 4442
Filed: October 31, 2012	:	Art Unit: 2897
For: SEMICONDUCTOR DEVICE	:	Examiner: L. T. Nguyen

RESPONSE TO RESTRICTION REQUIREMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

In response to the restriction requirement set forth in the Office Action mailed October 24, 2013, having a shortened statutory period for response set to expire November 24, 2013, wherein the Examiner required restriction between the following distinct Species:

Species I, as disclosed, is pertaining to the second embodiments, FIGs 9-10;
Species II, as disclosed, is pertaining to the third embodiment, FIGs 11-12; and
Species III, as disclosed, is pertaining to the fourth embodiments, FIGs 13-14.

Applicants elect Species I: Figs 9-10, with claims 1-7, 9, 11, 13, 15 and 16 readable thereon, for initial prosecution on the merits. Applicants also reserve the right to file a Divisional Application for the non-elected claims which the Examiner has indicated are patentably distinct.

Applicants believe that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0417, under Order No. 085393-0935.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

/Michael E. Fogarty/

Michael E. Fogarty
Registration No. 36,139

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Date: November 4, 2013

Electronic Acknowledgement Receipt

EFS ID:	17305170
Application Number:	13665376
International Application Number:	
Confirmation Number:	4442
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Customer Number:	53080
Filer:	Michael E. Fogarty/Natherine Ordanza
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0935
Receipt Date:	04-NOV-2013
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Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	085393-0935_Response.pdf	30882 4b0bce0f7073459ce961b7f655b83b57547ef180	no	2

Warnings:	
Information:	

Total Files Size (in bytes):	30882

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935	4442

53080 7590 03/18/2014

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER	
NGUYEN, LAWRENCE-LIN T	
ART UNIT	PAPER NUMBER
2897	

NOTIFICATION DATE	DELIVERY MODE
03/18/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

Office Action Summary	Application No. 13/665,376	Applicant(s) SATO ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/04/2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-16* is/are pending in the application.

5a) Of the above claim(s) *3-4,6,8-10,12 and 14* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,2,5,7,11,13,15 and 16* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☒ Some * c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/31/2013*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Detailed Action

1. The present application is being examined under the pre-AIA first to invent provisions.

2. This non-final Office action is responsive to Applicants' application filed **10/31/2012**. Claims **1-16** are presented for examination and claims **1-16** are rejected for the reasons indicated herein below.

Election/Restrictions

3. Applicant's election without traverse of Group **I**, claims **1-7,9,11,13,15-16** in the reply filed on 11/04/2013 is acknowledged.

4. The chosen claims would be further limited to Species I, as stated in the rejection such that - Species **I**, as disclosed, is pertaining to the second embodiments, FIGs 9-10. Species **I** in this case, as a feature of this embodiment is that:

a. the p-type silicon film **14b1** has a p-type impurity concentration ***lower than*** that of the p-type silicon film **14b2 (Claim 7 & 13)**.

b. In addition, each of the p-type silicon film **14b1** and the p-type silicon film **14b2** has a p-type impurity concentration ***higher than*** that of the p-type silicon film **14d**.

c. The n-type silicon film **14a1** has an n-type impurity concentration ***lower than*** that of each of the n-type silicon film **14a2** and the n-type silicon film **14c**

(Claim 7).

d. The n-type silicon film **14a2** has an n-type impurity concentration ***substantially equal*** to that of the n-type silicon film **14c**.

5. Claims **8,10,12, & 14** are withdrawn,

6. Now claims **1-2,5,7,11,13,15-16** are pending.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*
>
> *The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: (See MPEP Ch. 2141)*
>
> *Determining the scope and contents of the prior art;*
>
> *Ascertaining the differences between the prior art and the claims in issue; Resolving the level of ordinary skill in the pertinent art; and Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness*

8. Claims **1-2,5,7,11,13,15-16** are rejected under 35 U.S.C. 102(b), as being anticipated by **Shimomura** et al., (**JP2010-067912**, hereinafter **Shimomura**) in view of

Tamaki et al., (**US20080036010 A1**, hereinafter **Tamaki**).

9. In reclaim **1**, in FIG. 1-2, Shimomura teaches a semiconductor device, comprising:

e. a first dual-gate electrode(**14 & 15**); and

f. a second dual-gate electrode(**14a & 15a**), wherein

g. the first dual-gate electrode(**14 & 15**) includes a first gate electrode(**14**) located on a first active region(**12**) and a second gate electrode(**15**) located on a second active region(**13**),

h. the second dual-gate electrode(**14a & 15a**) includes a third gate electrode(**14a**) located on a third active region(**12a**) and a fourth gate electrode(**15a**) located on a fourth active region(**13a**),

i. the first active region(**12**) and the second active region(**12**) are isolated from each other with an isolation region(**11**) interposed therebetween,

j. the first gate electrode(**14**) and the second gate electrode(**15**) are connected to each other on the isolation region(**11**), and

k. at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region (This limitation will not be examined since it is pertaining to a forth embodiment,

which is Species III).

10. In reclaim **1**, Shimomura does not explicitly teach a silicon film of a conductivity type to all four regions.

11. But in the same field of endeavor of invention, Tamaki teaches a method and having silicon film(**104**) of a first conductivity type and gate electrode(**111**) located on active region and having silicon film(**105**) of a second conductivity type(**112**).

12. Tamaki is evidence that ordinary workers skilled in the art would find reasons, suggestions or motivations to modify the device of Tamaki with Shimomura. Therefore, at the time the invention was made, it would have been obvious to use the teaching of Tamaki in the device of Shimomura since the use of a SiON film as the gate insulating film for thickness reduction thereof for the purpose of improving the transistor characteristics involves problems on reliability, such as TDDB (Time Dependent Dielectric Breakdown), and the like (*See **§ [0009]***).

13. In reclaim **2**, in FIG. 7, Shimomura in view of Tamaki , Tamaki teaches a semiconductor device of claim 1, wherein an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.

14. In reclaim **5**, in FIG. 3, Shimomura in view of Tamaki , Tamaki teaches a semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity

concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region (*See* ***§ [0047-0050]***).

15. In reclaim **7**, in FIG. 3, Shimomura in view of Tamaki , Tamaki teaches a semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region (*See* ***§ [0047-0050]***).

16. In reclaim **11**, in FIG. 3, Shimomura in view of Tamaki , Tamaki teaches a semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region (*See* ***§ [0047-0050]***).

17. In reclaim **13**, in FIG. 3, Shimomura in view of Tamaki , Tamaki teaches a semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region (*See* ***§ [0047-0050]***).

18. In reclaim **15**, in FIG. 3, Shimomura in view of Tamaki , teaches a semiconductor device of claim 1, wherein the first gate electrode is a gate electrode of a first PMIS transistor, the second gate electrode is a gate electrode of a first NMIS transistor, the third gate electrode is a gate electrode of a second PMIS transistor, and the fourth gate

electrode is a gate electrode of a second NMIS transistor.

19. In reclaim **16**, in FIG. 3, Shimomura in view of Tamaki , Tamaki teaches a semiconductor device of claim 1, wherein each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAWRENCE-LINH T. NGUYEN whose telephone number is (571) 272-6267. The examiner can be reached on M-F (8AM - 4PM EST).

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on (571) 272-1867. The fax phone number for the organization where this application or proceeding is assigned is (571) 272-8300.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (in USA or CANADA) or (571) 272-1000.

/Lawrence-Linh T Nguyen/
Examiner, Art Unit 2897

/Fernando L. Toledo/

Supervisory Patent Examiner, Art Unit 2897

Notice of References Cited	Application/Control No. 13/665,376	Applicant(s)/Patent Under Reexamination SATO ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0036010	02-2008	Tamaki et al.	257/372
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP201067912	03-2010	JAPAN	Shimomura	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	3	"13665376"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 07:48
L3	13	"20080036013"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 08:47
L5	1	("2008/0036013").URPN.	USPAT	OR	ON	2014/02/24 09:13
L6	2	("2004/0180522").URPN.	USPAT	OR	ON	2014/02/24 09:40
L7	19	("20030181005" | "20040104405" | "20040159834" | "20040180522" | "20050199958" | "20060148153" | "20060223255" | "20070108529" | "20070141775" | "20070235817" | "20070257308" | "20080064191" | "6479350" | "6492218" | "6762085" | "7015082" | "7026205" | "7449753").PN. OR ("7678636").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/02/24 09:41
L8	6	"11808620"	US-PGPUB; USPAT; USOCR	OR	ON	2014/02/24 09:46
L10	47	"2010067912" "6275788" "8017934"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 09:51
L11	3363	257/392,903,E27.098.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
L12	213729	SRAM STATIC adj RAM STATIC adj RANDOM adj ACCESS	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2014/02/24 12:45

			JPO; DERWENT; IBM_TDB			
L13	26439	L12 and LOGIC adj CIRCUIT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
L14	855317	("257" "438" "365").CLAS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
L15	293	L11 and L12 and L13 and L14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
L16	0	L15 and (add$3 introduc$3 inplant$3) with ((first second third) adj3 (conductive p- n-) adj impurity)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:47
L17	4	L15 and (add$3 introduc$3 inplant$3) near3 (((first second third) adj3 (conductive p- n-)) adj3 impurity)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:49
L18	5	L15 and (add$3 remov$3high$3 low$3 introduc$3 inplant$3) near3 (((first second third) adj3 (conductive p- n-)) adj3 impurity)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:55
S1	1	"13665376"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 10:45
S2	186	((YOSHIHIRO) near2 (SATO)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/27 10:46
S3	68	((HIDEYUKI) near2 (ARAI)).INV.	US-PGPUB; USPAT;	OR	ON	2013/08/27 10:46

			USOCR			
S4	208	((TAKAYUKI) near2 (YAMADA)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/27 10:46
S5	5	"20030107090" "20080036010"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 10:46
S6	17641	("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:10
S7	5987216	((concerntration n- n-type p- p-type second) adj$3 impurit$3) with (high$3 low$3 less more)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:15
S8	321	((second third four$2) adj active) near3 ((second third four$2) adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:21
S9	2	S6 and S7 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:26
S10	11019	S6 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:37
S11	288	(second multipl$3 third four) adj ("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:39
S12	829	(("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)) adj3 (CMIS NMISFET PMISFET MISFET MOSFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2013/08/27 14:43

			JPO; DERWENT; IBM_TDB			
S13	23	("5877535" | "5977591" | "20020093051" | "6180519" | "6586837" | "20020042173" | "20030173625" | "5837601" | "6191460" | "6489664" | "20010007368" | "20010006832").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:46
S14	103632	panasonic.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:46
S15	84	S14 and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:47
S16	44	("5877535" | "5977591" | "20020093051" | "6180519" | "6586837" | "20020042173" | "20030173625" | "5837601" | "6191460" | "6489664" | "20010007368" | "20010006832" | "5122474" | "6010929" | "20040183141" | "20040256653" | "5936844" | "20060138568" | "7129543" | "20070221960" | "7414292").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 15:50
S17	187024	(sram static adj ram$1 static adj ramdom adj acess adj mem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:19
S18	23874	S17 and logic adj circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:20
S19	1985	S18 and (gate with (impurit$3 concerntration))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:21
S21	206	S19 and dual adj gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/08/27 17:22

			DERWENT; IBM_TDB			
S22	332415	((concerntration n- n-type p- p-type second) adj$3 impurit$3) with (high$3 low$3 less more) and ("257".clas. "438".clas.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:24
S24	715	((second third four$2) adj3 active) near3 ((second third four$2) adj electrode$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:26
S25	2567	transistor$1 near3 (PMIS NMIS MISFET NMISFET PMISFET CMIS) and ("257".clas. "438".clas.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:28
S26	1039	(("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)) near3 (CMIS NMISFET PMISFET MISFET MOSFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:28
S27	33	S25 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:31
S30	206	S21 and dual adj gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:41
S31	24133	S17 and logic adj (circuit area)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:49
S32	21	(US-20130062682-$ or US-20080283928-$ or US-20110008954-$ or US-20110006374-$ or US-20090130833-$ or US-20110086510-$ or US-20060138568-$ or US-20020042173-$ or US-20110198707-$ or US-20060292799-$ or US-20060275969-$ or US-20130193493-$).did.	US-PGPUB; USPAT; DERWENT	OR	ON	2013/09/26 20:24

		or (US-8013395-$ or US-7825482-$ or US-7598574-$ or US-7495298-$ or US-7414292-$ or US-6569742-$ or US-5977591-$).did. or (US-20090138840-$ or JP-2006303448-$).did.				
S33	3200	257/392,903,E27.098.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:10
S34	196695	SRAM STATIC adj RAM STATIC adj RANDOM adj ACCESS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:12
S35	25092	S34 and LOGIC adj CIRCUIT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:12
S36	814721	("257" "438" "365").CLAS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:15

2/24/2014 2:12:14 PM
C:\Users\lnguyen16\Documents\EAST\Workspaces\13665376.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13665376	SATO ET AL.
	Examiner	Art Unit
	LAWRENCE-LINH T NGUYEN	2897

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	392,903,E27.098	02/24/2014	LTN

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/665,376	10/31/2012 RULE	257	2897	085393-0935

APPLICANTS

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Hideyuki ARAI, Toyama, JAPAN;
Takayuki YAMADA, Toyama, JAPAN;
PANASONIC CORPORATION, Osaka, JAPAN

**** CONTINUING DATA ***************************

This application is a CON of PCT/JP2011/006167 11/04/2011

**** FOREIGN APPLICATIONS ***************************

JAPAN 2011-068131 03/25/2011

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11/20/2012

Foreign Priority claimed	☑ Yes ☐ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☑ Yes ☐ No		JAPAN	16	16	1
Verified and Acknowledged	/LAWRENCE-LINH T NGUYEN/ Examiner's Signature	Initials				

ADDRESS

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001
UNITED STATES

TITLE

SEMICONDUCTOR DEVICE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	Not Yet Assigned
Filing Date	October 31, 2012
First Named Inventor	Yoshihiro SATO
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	085393-0935

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A1*	US-2003/0107090-A1	06-12-2003	Kumeno	Corresponds to JP 2003-179056-A
	A2*	US-2008/0036010-A1	02-14-2008	Tamaki et al.	Corresponds to JP 2008-042092-A

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	B1	JP-2010-067912-A	03-25-2010	Panasonic Corp	English Abstract	
	B2	JP-6-275788-A	09-30-1994	Ricoh Kk	English Abstract	
	B3	JP-8-017934-A	01-19-1996	Ricoh Kk	English Abstract	

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		International Search Report issued in International Application No. PCT/JP2011/006167 oissued on January 24, 2011.	

Examiner Signature	/Lawrence-Linh Nguyen/	Date Considered	08/26/2013

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13665376	SATO ET AL.
	Examiner	**Art Unit**
	LAWRENCE-LINH T NGUYEN	2897

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/24/2014								
	1	✓								
	2	✓								
	3	-								
	4	-								
	5	✓								
	6	-								
	7	✓								
	8	-								
	9	-								
	10	-								
	11	✓								
	12	-								
	13	✓								
	14	-								
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PRIOR ART

[Background of the Invention]
[0002]
In a CMOS (Complementary Metal Oxide Semiconductor) process in connection with high integration of recent years and a semiconductor integrated circuit device, advanced features, and improvement in the speed, The dual gate structure using the Si electrode which injected the P type impurity is adopted as the gate electrode of a P channel type MOS transistor by the gate electrode of the N channel type MOS transistor using the Si electrode which injected the N type impurity.
[0003]
In the semiconductor device which has such dual gate structure, the N channel region and P channel region in the gate electrode consisting of silicon in the border area connected mutually, When resistance rises under the influence of the impurity concentration of an N channel region and a P channel region, there is a problem that the performance of the integrated circuit of the working speed of a circuit being delayed is inhibited.
[0004]
That this problem should be solved, by metal-silicide-izing the upper part of a gate electrode, the method of making resistance of a gate electrode small is proposed, and many improvement is made conventionally (see the Patent document 1.).
[0005]
(First conventional example)
Fig.4 (a) - Fig.4 (f) show the section composition of the process order of the manufacturing method of the semiconductor device which metal-silicide-izes the upper part of the gate electrode concerning a first conventional example, and lowers resistance of a gate electrode. Here, it is a section of a gate width direction and the manufacturing method of the semiconductor device which has the dual gate structure in which the metal silicide film was formed is shown.
[0006]
First, as shown in Fig.4 (a), the isolation region 101 which encloses the active region formed in the upper part of the semiconductor substrate 100 consisting of silicon, and separates N channel type MOS transistor region A and P channel type MOS transistor region B is formed. Then, the gate dielectric film 102 and the polycrystalline silicon film 103 are sequentially formed on the semiconductor substrate 100.
[0007]
Next, as shown in Fig.4 (b), P channel type MOS transistor region B is covered on the polycrystalline silicon film 103, And form the first resist film 104 that has an opening pattern which carries out the opening of the N channel type MOS transistor region A, and the formed first resist film 104 is used as a mask, The ion implantation of the phosphorus (P^+) ion which is an N type impurity is carried out to N channel type MOS transistor region A of the polycrystalline silicon film 103. Then, the first resist film 104 is removed.
[0008]
Next, as shown in Fig.4 (c), N channel type MOS transistor region A is covered on the polycrystalline silicon film 103, And form the second resist film 105 which has an opening pattern which carries out the opening of the P channel type MOS transistor region B, and the formed second resist film 105 is used as a mask, The ion implantation of the boron (B^+) ion which is a P type impurity is carried out to P channel type MOS transistor region B of the polycrystalline silicon film 103. Then, the second resist film 105 is removed.
[0009]
Next, as shown in Fig.4 (d), the N type polycrystalline silicon region 103a and the P type polycrystalline silicon region 103b are formed from the polycrystalline silicon film 103 by heat-treating to the semiconductor substrate 100 and activating each impurity ion injected into the polycrystalline silicon film 103. At this time, the phosphorous ion and the boron ion in the polycrystalline silicon film 103 diffuse, and the PN-junction border area C is formed in the boundary part of N channel type MOS transistor region A and P channel type MOS transistor region B in the polycrystalline silicon film 103.
[0010]
Next, on the polycrystalline silicon film 103, as shown in Fig.4 (e), the metal film 112 is deposited so that the N type polycrystalline silicon region 103a and the P type polycrystalline silicon region 103b may be straddled.
[0011]
Next, as shown in Fig.4 (f), the metal silicide film 112A over the N type polycrystalline silicon region 103a and the P type polycrystalline silicon region 103b is formed by the publicly known Salicide formation technology.
[0012]
However, in the manufacturing method concerning the aforementioned first conventional example, if the wiring width of the metal silicide film 112A becomes small, the metal silicide film 112 will condense and it will become easy to produce disconnection in the metal silicide film 112. As a result of impurity concentration's influencing the metal silicide film 112A which especially carried out silicide formation of the PN-junction border area C of the polycrystalline silicon film 103 by dual gate structure, a silicide formation reaction's becoming slow and the thickness of the metal silicide film 112A becoming thin, it is easy to produce a resistance rise and disconnection.
[0013]

Thus, when disconnection occurs in the metal silicide film 112A in the PN-junction border area C, when reverse bias is applied to the PN junction of the polycrystalline silicon film 103, a resistance rise arises, and there is a problem that a gate electrode becomes high resistance extremely.

[0014]

Then, in order to avoid high resistance-ization of the gate electrode by disconnection of such a metal silicide film, other composition shown in Fig.5 is proposed (see the Patent document 2.).

[0015]

(Second conventional example)

Fig.5 shows the plane constitution of the dual gate transistor which has an N channel type MOS transistor region concerning a second conventional example, and a P channel type transistor region.

[0016]

The P type gate electrode 4 which was arranged on the P channel type transistor region 1 as shown in Fig.5, By providing the non-doped region 8 which does not inject an impurity into a boundary part with the N type gate electrode 5 which was arranged on N channel type MOS transistor region 3, the influence by the impurity concentration at the time of silicide formation was avoided, and reduction in thickness of a metal silicide film is prevented.

[Patent document 1] JP,S59-213156,A

[Patent document 2] JP,H10-012745,A

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[0067]
[Drawing 1](a) And (b) shows typically the semiconductor device concerning one embodiment of the present invention, (a) is a plan view, and (b) is a cross sectional view in the Ib-Ib line of (a).
[Drawing 2](a) - (d) is a cross sectional view of process order showing typically the manufacturing method of the semiconductor device concerning one embodiment of the present invention.
[Drawing 3](a) - (d) is a cross sectional view of process order showing typically the manufacturing method of the semiconductor device concerning one embodiment of the present invention.
[Drawing 4](a) - (f) is a cross sectional view of process order showing typically the manufacturing method of the semiconductor device concerning a first conventional example.
[Drawing 5]It is a plan view showing the semiconductor device concerning a second conventional example.

[Translation done.]

* NOTICES *

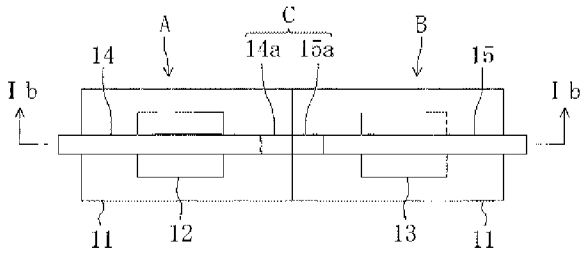
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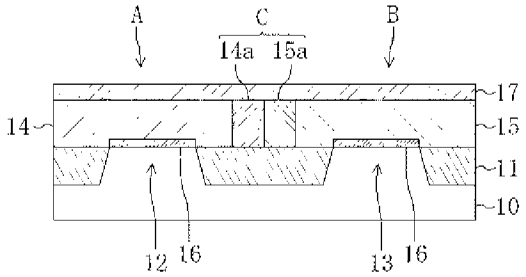
DRAWINGS

[Drawing 1]

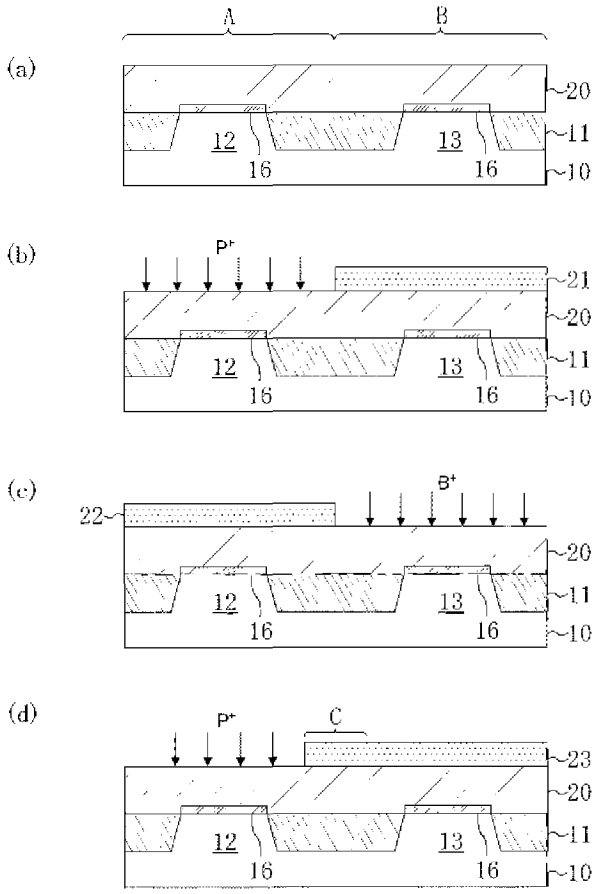
(a)



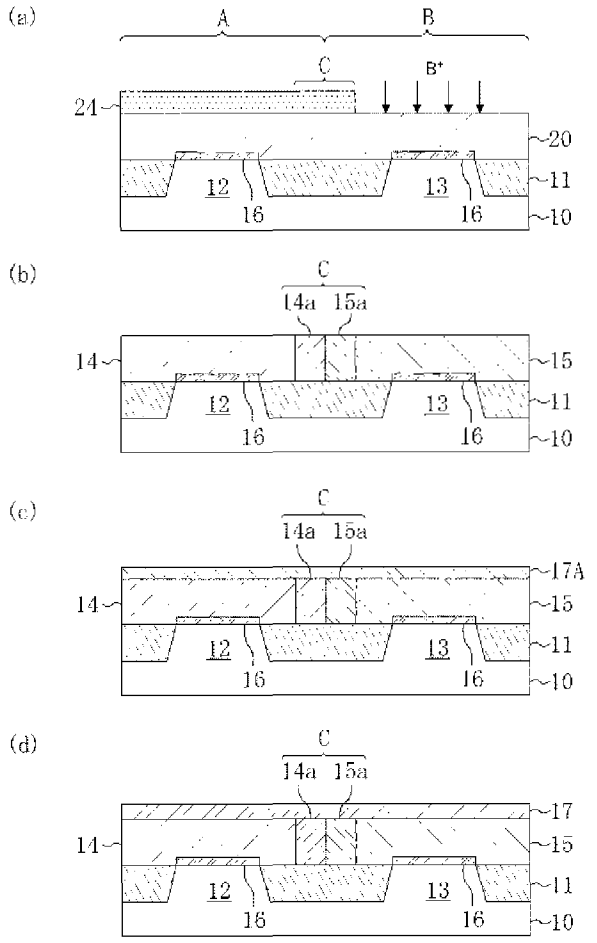
(b)



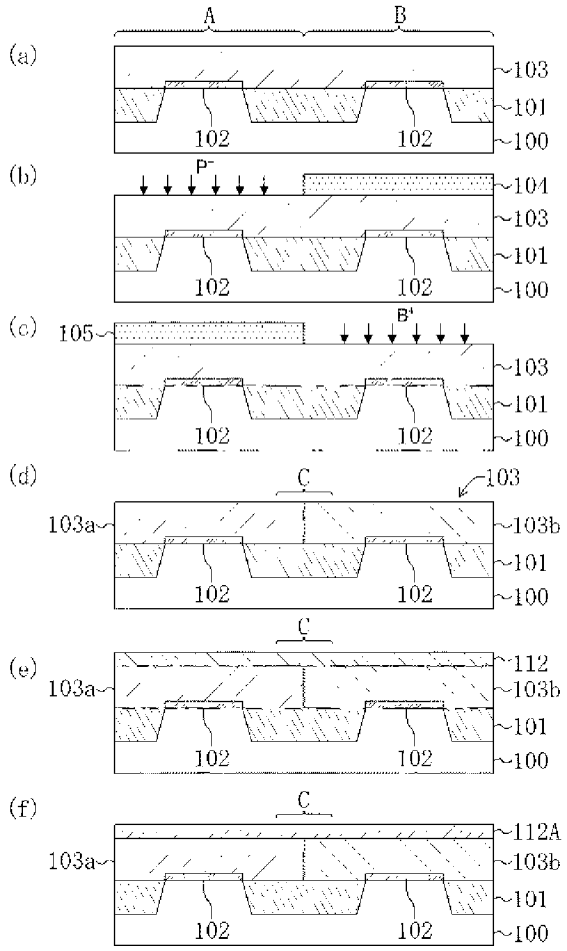
[Drawing 2]


(a)
A
B
20
11
12
13
16
16
10
(b)
P+
21
20
11
12
13
16
16
10
(c)
B+
22
20
11
12
13
16
16
10
(d)
P+
C
23
20
11
12
13
16
16
10

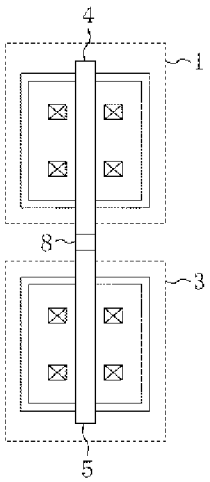
[Drawing 3]


(a)
A
B
C
B+
21
20
11
12
13
16
16
10
(b)
C
14a
15a
14
15
11
12
13
16
16
10
(c)
C
14a
15a
17A
14
15
11
12
13
16
16
10
(d)
C
14a
15a
17
14
15
11
12
13
16
16
10

[Drawing 4]



[Drawing 5]



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention]
[0001]
Especially the present invention relates to a semiconductor device which has the wiring which equipped the upper part with the metal silicide film, and a manufacturing method for the same about a semiconductor device and a manufacturing method for the same.
[Background of the Invention]
[0002]
In a CMOS (Complementary Metal Oxide Semiconductor) process in connection with high integration of recent years and a semiconductor integrated circuit device, advanced features, and improvement in the speed, The dual gate structure using the Si electrode which injected the P type impurity is adopted as the gate electrode of a P channel type MOS transistor by the gate electrode of the N channel type MOS transistor using the Si electrode which injected the N type impurity.
[0003]
In the semiconductor device which has such dual gate structure, the N channel region and P channel region in the gate electrode consisting of silicon in the border area connected mutually, When resistance rises under the influence of the impurity concentration of an N channel region and a P channel region, there is a problem that the performance of the integrated circuit of the working speed of a circuit being delayed is inhibited.
[0004]
That this problem should be solved, by metal-silicide-izing the upper part of a gate electrode, the method of making resistance of a gate electrode small is proposed, and many improvement is made conventionally (see the Patent document 1.).
[0005]
(First conventional example)
Fig.4 (a) - Fig.4 (f) show the section composition of the process order of the manufacturing method of the semiconductor device which metal-silicide-izes the upper part of the gate electrode concerning a first conventional example, and lowers resistance of a gate electrode. Here, it is a section of a gate width direction and the manufacturing method of the semiconductor device which has the dual gate structure in which the metal silicide film was formed is shown.
[0006]
First, as shown in Fig.4 (a), the isolation region 101 which encloses the active region formed in the upper part of the semiconductor substrate 100 consisting of silicon, and separates N channel type MOS transistor region A and P channel type MOS transistor region B is formed. Then, the gate dielectric film 102 and the polycrystalline silicon film 103 are sequentially formed on the semiconductor substrate 100.
[0007]
Next, as shown in Fig.4 (b), P channel type MOS transistor region B is covered on the polycrystalline silicon film 103, And form the first resist film 104 that has an opening pattern which carries out the opening of the N channel type MOS transistor region A, and the formed first resist film 104 is used as a mask, The ion implantation of the phosphorus (P^+) ion which is an N type impurity is carried out to N channel type MOS transistor region A of the polycrystalline silicon film 103. Then, the first resist film 104 is removed.
[0008]
Next, as shown in Fig.4 (c), N channel type MOS transistor region A is covered on the polycrystalline silicon film 103, And form the second resist film 105 which has an opening pattern which carries out the opening of the P channel type MOS transistor region B, and the formed second resist film 105 is used as a mask, The ion implantation of the boron (B^+) ion which is a P type impurity is carried out to P channel type MOS transistor region B of the polycrystalline silicon film 103. Then, the second resist film 105 is removed.
[0009]
Next, as shown in Fig.4 (d), the N type polycrystalline silicon region 103a and the P type polycrystalline silicon region 103b are formed from the polycrystalline silicon film 103 by heat-treating to the semiconductor substrate 100 and activating each impurity ion injected into the polycrystalline silicon film 103. At this time, the phosphorous ion and the boron ion in the polycrystalline silicon film 103 diffuse, and the PN-junction border area C is formed in the boundary part of N channel type MOS transistor region A and P channel type MOS transistor region B in the polycrystalline silicon film 103.
[0010]
Next, on the polycrystalline silicon film 103, as shown in Fig.4 (e), the metal film 112 is deposited so that the N type polycrystalline silicon region 103a and the P type polycrystalline silicon region 103b may be straddled.
[0011]
Next, as shown in Fig.4 (f), the metal silicide film 112A over the N type polycrystalline silicon region 103a and the P type polycrystalline silicon region 103b is formed by the publicly known Salicide formation technology.
[0012]
However, in the manufacturing method concerning the aforementioned first conventional example, if the wiring width of the metal silicide

film 112A becomes small, the metal silicide film 112 will condense and it will become easy to produce disconnection in the metal silicide film 112. As a result of impurity concentration's influencing the metal silicide film 112A which especially carried out silicide formation of the PN-junction border area C of the polycrystalline silicon film 103 by dual gate structure, a silicide formation reaction's becoming slow and the thickness of the metal silicide film 112A becoming thin, it is easy to produce a resistance rise and disconnection.

[0013]

Thus, when disconnection occurs in the metal silicide film 112A in the PN-junction border area C, when reverse bias is applied to the PN junction of the polycrystalline silicon film 103, a resistance rise arises, and there is a problem that a gate electrode becomes high resistance extremely.

[0014]

Then, in order to avoid high resistance-ization of the gate electrode by disconnection of such a metal silicide film, other composition shown in Fig.5 is proposed (see the Patent document 2.).

[0015]

(Second conventional example)

Fig.5 shows the plane constitution of the dual gate transistor which has an N channel type MOS transistor region concerning a second conventional example, and a P channel type transistor region.

[0016]

The P type gate electrode 4 which was arranged on the P channel type transistor region 1 as shown in Fig.5, By providing the non-doped region 8 which does not inject an impurity into a boundary part with the N type gate electrode 5 which was arranged on N channel type MOS transistor region 3, the influence by the impurity concentration at the time of silicide formation was avoided, and reduction in thickness of a metal silicide film is prevented.

[Patent document 1] JP,S59-213156,A

[Patent document 2] JP,H10-012745,A

[Description of the Invention]

[Problem to be solved by the invention]

[0017]

However, although the manufacturing method concerning the aforementioned second conventional example is providing the non-doped region to the PN-junction border area, since the impurity diffusion to the non-doped region at the time of heat treatment is large, after heat treatment, whether the non-doped region's being very small substantially and a possibility of disappearing are.

[0018]

For this reason, in order to secure a non-doped region after heat treatment, it is necessary to set up a non-doped region largely, and there is a problem of barring micronization and high integration of an element.

[0019]

Without barring micronization and high integration of an element in view of the aforementioned conventional problem, the present invention prevents disconnection of the metal silicide film in a PN-junction border area, and an object of the present invention is to enable it to avoid high resistance-ization of wiring.

[Means for solving problem]

[0020]

In order to attain the aforementioned purpose, the present invention is considered as the composition which provides the region where the impurity was doped by the boundary part of the N channel type transistor region and P channel type MOS transistor region in dual gate structure in a semiconductor device and a manufacturing method for the same at low concentration.

[0021]

The semiconductor device concerning the present invention is specifically formed on a semiconductor substrate, have wiring consisting of the silicon which has conductivity, and the metal silicide film formed after wiring, and wiring, Have the 1st region that shows the conductivity of N type, the 2nd region that shows the conductivity of P type, and the 3rd region formed between the 1st region and the 2nd region, and the 3rd region is connected to the 1st region and the 2nd region, and. Concentration of the impurity of the 3rd region is characterized by being lower than the concentration of the N type impurity of the 1st region, and the concentration of the P type impurity of the 2nd region.

[0022]

Since the concentration of the impurity of the 3rd region that is the connection part of the 1st region and the 2nd region, i.e., a PN-junction border area, is lower than the concentration of the N type impurity of the 1st region, and the concentration of the P type impurity of the 2nd region according to the semiconductor device of the present invention, reduction in thickness of a metal silicide film can be inhibited. For this reason, since disconnection of a metal silicide film can be prevented, high resistance-ization of wiring is avoidable.

[0023]

In the semiconductor device of the present invention, the 1st region is a gate electrode of an N channel type transistor, and, as for the 2nd region, it is preferable that it is a gate electrode of a P channel type transistor.

[0024]

As for the 3rd region, in the semiconductor device of the present invention, it is preferable to consist of the 5th region that is connected with the 4th region that is connected with the 1st region and shows the conductivity of N type, and the 2nd region, and shows the conductivity of P type.

[0025]

As for the lay length which connects the 1st region and the 2nd region in the 3rd region, in the semiconductor device of the present invention, it is preferable that it is more than the superposition dimension in a mask alignment process.

[0026]

As for a metal silicide film, in the semiconductor device of the present invention, it is preferable to consist of a nickel silicide, titanium silicides, or a cobalt silicide.

[0027]
The present invention is characterized by a manufacturing method of a semiconductor device comprising the following.
A process of forming a wiring formation film consisting of silicon on a semiconductor substrate (a).
A process (b) of introducing an impurity of the 1st conductivity type into the 1st region of a wiring formation film using the 1st mask layer that carries out the opening of the 1st region of a wiring formation film.
A process (c) of introducing an impurity of the 2nd conductivity type into the 2nd region of a wiring formation film using the 2nd mask layer that carries out the opening of the 1st region in a wiring formation film, and the 2nd adjoining region.
The 3rd region that is some regions which touch the boundary part of the 2nd region of a wiring formation film, and the 2nd region in the 1st region of a wiring formation film with a wrap, Using the 3rd mask layer that carries out the opening of the remainder of the 1st region a process (d) of introducing an impurity of the 1st conductivity type into the remainder of the 1st region in a wiring formation film, and by heat-treating to a wiring formation film, A process (e) of activating each impurity introduced into the 1st region, the 2nd region, and the 3rd region, and a process (f) of forming a metal silicide film on a wiring formation film.

[0028]
According to the manufacturing method of the semiconductor device of the present invention, since the mask of the impurity concentration of the 3rd region that is some regions of the 1st region in the wiring formation film consisting of silicon is carried out in the process (d), it becomes lower than the impurity concentration of a first region. For this reason, since reduction in thickness of a metal silicide film can be inhibited, disconnection of a metal silicide film can be prevented now and, as a result, high resistance-ization of wiring can be avoided.
[0029]
In the manufacturing method of the semiconductor device of the present invention, the 1st region is a gate electrode of an N channel type transistor, and, as for the 2nd region, it is preferable that it is a gate electrode of a P channel type transistor.
[0030]
As for the length from the boundary part with the 2nd region in the 3rd region to the 1st region side, in the manufacturing method of the semiconductor device of the present invention, it is preferable that it is more than the superposition dimension in a mask alignment process.
[0031]
The manufacturing method of the semiconductor device of the present invention the 4th region that is some regions which touch the boundary part of the 1st region of a wiring formation film, and the 1st region in the 2nd region of a wiring formation film between processes (d) (e) with a wrap, It is preferable to have further the process (g) of introducing the impurity of the 2nd conductivity type into the remainder of the 2nd region in a wiring formation film, using the 4th mask layer that carries out the opening of the remainder of the 2nd region, and to also activate the impurity introduced into the 4th region of the wiring formation film in a process (e).
[0032]
As for each of length from the boundary part with the 2nd region in the 3rd region to the 1st region side, and length from the boundary part with the 1st region in the 4th region to the 2nd region side, in the manufacturing method of the semiconductor device of the present invention, it is preferable that it is more than the superposition dimension in a mask alignment process.
[0033]
As for a metal silicide film, in the manufacturing method of the semiconductor device of the present invention, it is preferable that they are a nickel silicide, titanium silicides, or a cobalt silicide.
[Effect of the Invention]
[0034]
Since according to a semiconductor device concerning the present invention, and a manufacturing method for the same reduction in thickness of a metal silicide film can be inhibited and disconnection of a metal silicide film can be prevented, high resistance-ization of wiring is avoidable.
[Best Mode of Carrying Out the Invention]
[0035]
(One embodiment)
It describes referring to Drawings for one embodiment of the present invention.
[0036]
Fig.1 (a) shows the plane constitution of the semiconductor device concerning one embodiment of the present invention, and Fig.1 (b) shows the section composition in the Ib-Ib line of Fig.1 (a).
[0037]
As shown in Fig.1 (a), the semiconductor device concerning this embodiment is a dual gate transistor which has N channel type MOS transistor region A and P channel type transistor region B. In Fig.1 (a), the metal silicide film provided by the upper part of the gate electrode is omitted for a description.
[0038]
As shown in Fig.1 (a) and Fig.1 (b), to N channel type MOS transistor regionA, The N type active region 12 which functions as a source drain area which the circumference is surrounded and consists of an N type impurity diffused layer by the isolation region 11 formed in the upper part of the semiconductor substrate 10 consisting of silicon, It is formed ranging over the this N type active region 12 and isolation region 11 top, and the first gate electrode 14 consisting of the polycrystalline silicon containing an N type impurity is arranged.
[0039]
Similarly P channel type MOS transistor region B, The P type active region 13 which functions as a source drain area which the circumference is surrounded and consists of a P type impurity diffused layer by the isolation region 11, It is formed ranging over the this P type active region 13 and isolation region 11 top, and the second gate electrode 15 consisting of the polycrystalline silicon containing a P type impurity is arranged.
[0040]

Between the N type active region 12 on the main surface of the semiconductor substrate 10, and the first gate electrode 14, and between the P type active region 13 and the second gate electrode 15, the gate dielectric film 16 which consists of silicon oxide, for example is formed, respectively.

[0041]

Between the first gate electrode 14 in the dual gate over N channel type MOS transistor region A and P channel type MOS transistor region B, and the second gate electrode 15, The 3rd gate electrode 14a that consists of polycrystalline silicon containing an N type impurity, and adjoins the first gate electrode 14, It consists of polycrystalline silicon containing a P type impurity, and the second gate electrode 15 and the 4th adjoining gate electrode 15a are formed, and it has touched mutually so that the 3rd gate electrode 14a and 4th gate electrode 15a may form the PN-junction border area C.

[0042]

As characteristics of this embodiment, the concentration of the N type impurity of the 3rd gate electrode 14a is low concentration from the concentration of the N type impurity of the first gate electrode 14, and the concentration of the P type impurity of the 4th gate electrode 15a is low concentration from the concentration of the P type impurity of the second gate electrode 15.

[0043]

As shown in Fig.1 (b), the nickel silicide film 17 is formed in the upper part of the first gate electrode 14, the second gate 15, the 3rd gate electrode 14a, and the 4th gate electrode 15a, for example.

[0044]

It describes referring to Drawings for the manufacturing method of the semiconductor device hereafter applied to this embodiment constituted as mentioned above.

[0045]

Fig.2 (a) – Fig.2 (d) and Fig.3 (a) – Fig.3 (d) show the section composition of the process order of the manufacturing method of the semiconductor device concerning this embodiment.

[0046]

First, as shown in Fig.2 (a), surround the N type active region 12 and the P type active region 13 in the upper part of the semiconductor substrate 10 consisting of silicon, respectively, and. The isolation region 11 which consists of a shallow trench isolation (STI) which separates N channel type transistor region A and P channel type transistor region B is formed. Then, for example, the gate dielectric film 16 consisting of 2-nm-thick silicon oxide is formed on the main surface of the semiconductor substrate 10 by a thermal oxidation method. Then, it crosses on the semiconductor substrate 10 by the chemical gaseous phase depositing (CVD) method all over including the gate dielectric film 16 and the isolation region 11, and the 200-nm-thick polycrystalline silicon film 20 is formed.

[0047]

Next, as shown in Fig.2 (b), form the first resist film 21 that has an opening in N channel type transistor region A on the polycrystalline silicon film 20 by the lithography method, and the formed first resist film 21 is used as a mask, Infused energy carries out by 20keV, and a dose carries out the ion implantation of the phosphorus (P^+) ion which is an N type impurity to N channel type transistor region A of the polycrystalline silicon film 20 by the implanting conditions of $5x10^{15}/cm^2$. Then, the first resist film 21 is removed.

[0048]

Next, as shown in Fig.2 (c), form the second resist film 22 which has an opening in P channel type transistor region B on the polycrystalline silicon film 20 by the lithography method, and the formed second resist film 22 is used as a mask, Infused energy carries out by 2keV, and a dose carries out the ion implantation of the boron (B^+) ion which is a P type impurity to P channel type transistor region B of the polycrystalline silicon film 20 by the implanting conditions of $2x10^{15}/cm^2$. Then, after removing the second resist film 22, the polycrystalline silicon film 20 is patterned after gate electrode form as shown in Fig.1 (a) by the lithography method and the dry etching method.

[0049]

As shown in Fig.2 (d), the aperture width on N channel type transistor region A rather than the first resist film 21 on the polycrystalline silicon film 20 next, by making about 10 nm small at this N channel type transistor region A side, The 3rd resist film 23 of a wrap is formed for the PN-junction border area C which is a boundary part of P channel type transistor region B and this P channel type transistor region B, and N channel type transistor region A. Then, by using the 3rd formed resist film 23 as a mask, infused energy carries out by 20keV, and a dose carries out the ion implantation of the phosphorus (P^+) ion to N channel type transistor region A of the polycrystalline silicon film 20 by the implanting conditions of $1x10^{15}/cm^2$. Then, the 3rd resist film 23 is removed.

[0050]

As shown in Fig.3 (a), the aperture width on P channel type transistor region B rather than the second resist film 22 on the polycrystalline silicon film 20 next, by making about 10 nm small at this P channel type transistor region B side, The 4th resist film 24 of a wrap is formed for N channel type transistor region A and the PN-junction border area C. Then, by using the 4th formed resist film 24 as a mask, infused energy carries out by 2keV, and a dose carries out the ion implantation of the boron (B^+) ion to P channel type transistor region B of the polycrystalline silicon film 20 by the implanting conditions of $1x10^{15}/cm^2$. Then, the 4th resist film 24 is removed.

[0051]

Next, as shown in Fig.3 (b), it heat-treats to the semiconductor substrate 10, and each impurity injected into the polycrystalline silicon film 20 is activated. By this heat treatment, the phosphorous ion and the boron ion which were injected into the polycrystalline silicon film 20 diffuse, and to N channel type transistor region [of the polycrystalline silicon film 20] A, The first gate electrode 14 that consists of an N type polycrystalline silicon region is formed, and the second gate electrode 15 which consists of a P type polycrystalline silicon region is formed in P channel type transistor region [of the polycrystalline silicon film 20] B. To the N channel type transistor region A side in the PN-junction border area C of the polycrystalline silicon film 20, The 3rd gate electrode 14a whose concentration of an N type impurity is lower than the first gate electrode 14 is formed, and the 4th gate electrode 15a whose concentration of a P type impurity is lower than the second gate electrode 15 is formed in the P channel type transistor region B side in the PN-junction border area C.

[0052]

Next, as shown in Fig.3 (c), the 10-nm-thick nickel (nickel)-for example, film 17A is deposited as a metal film by the vacuum deposition method or a sputtering method the whole surface on each gate electrode 14, 14a, 15, and 15a. At this time, a titanium nitride (TiN) film may be deposited on the nickel layer 17A.

[0053]

Next, as shown in Fig.3 (d), temperature to the semiconductor substrate 10 at 430 degrees C, The nickel silicide (NiSi) film 17 is formed in the upper part of each gate electrode 14, 14a, 15, and 15a by performing first short time heat treatment (rapid heat treatment) for 30 seconds, and making the silicon which constitutes each gate electrode 14 and 15, and nickel deposited on it react. Then, the unreacted nickel layer 17A is selectively removed using solutions, such as mixed liquor of sulfuric acid (H_2SO_4) and hydrogen peroxide solution (H_2O_2). Then, temperature performs second short time heat treatment for 60 seconds to the semiconductor substrate 10 at 850 degrees C.

[0054]

The semiconductor device which has the dual gate structure concerning this embodiment by the above can be obtained.

[0055]

On this embodiment and in the PN-junction border area C of N channel type transistor region A and P channel type transistor region B, Make concentration of the N type impurity of the first gate electrode 14 of N channel type transistor region A, and the 3rd touching gate electrode 14a lower than the concentration of the first gate electrode 14, and. Concentration of the P type impurity of the second gate electrode 15 of P channel type transistor region B and the 4th touching gate electrode 15a is made lower than the concentration of the second gate electrode 15. However, the present invention may make only impurity concentration of the 3rd gate electrode 14a lower than the impurity concentration of the first gate electrode 14, and may make only impurity concentration of the 4th gate electrode 14a conversely lower than the impurity concentration of the second gate electrode 15.

[0056]

In this embodiment, after injecting the phosphorous ion which is an N type impurity, the boron ion which is a P type impurity is injected, but contrary to this, phosphorous ion may be injected, after injecting boron ion. After injecting one of ion continuously among phosphorous ion and boron ion rather than injecting phosphorous ion and boron ion 2 times respectively alternately, the ion of the other may be injected continuously.

[0057]

Although the dimension of the wrap portion set the PN-junction border area [in / for the PN-junction border area C / the 3rd resist film 23 of a wrap, and the 4th resist film 24] C to 10 nm, it is desirable that it is beyond the superposition accuracy in a mask alignment process.

[0058]

In the above-mentioned embodiment, if the impurity concentration in the PN-junction border area C is phosphorous ion, in more than $6x10^{15}/cm^2$, the reaction velocity of silicide formation becomes it slow that boron ion is $3x10^{15}$ / more than cm^2. A reaction becomes slow when nickel is especially used for a refractory metal.

[0059]

As are described above, and the semiconductor device concerning this embodiment was shown in Fig.3 (b), the impurity concentration of the PN-junction border area C of N channel type transistor region A and P channel type transistor region B is formed lower than other regions.

[0060]

The concentration of the N type impurity of the 3rd gate electrode 14a in the PN-junction border area C is lower than the concentration of the N type impurity of the first gate electrode 14 more specifically, And since it is the composition whose concentration of the P type impurity of the 4th gate electrode 15a is lower than the concentration of the P type impurity of the second gate electrode 15, Since the thickness of the nickel silicide film 17 formed on the PN-junction border area C can be prevented from becoming thin, disconnection of the nickel silicide film 17 in the PN-junction border area C can be prevented.

[0061]

Therefore, by forming in a PN-junction border area like a second conventional example the non-doped region which does not inject an impurity at all, A poor integrated circuit can be prevented without increasing the occupation area of a transistor compared with the technique of preventing disconnection in the PN-junction border area of a nickel silicide film.

[0062]

Although the dual gate transistor which has N channel type MOS transistor region A and P channel type transistor region B as a semiconductor device was described in this embodiment, It is not limited to this composition, for example, is formed on a semiconductor substrate, and the same effect can be acquired even if it is wiring consisting of the silicone film which the N type silicone film and the P type silicone film connected.

[0063]

Although disconnection of the metal silicide film in the PN-junction border area C is not dependent on a wire length, it is easy to generate it, so that wiring width becomes narrow. Specifically, in 60 nm or less, it is easy to generate wiring width, therefore a large effect can be acquired by the case where wiring width is 60 nm or less.

[0064]

In this embodiment, although the nickel silicide was used as a metal silicide film, the refractory metal which can form silicides, such as titanium (Ti) or cobalt (Co), may be used.

[0065]

As for the dimension of the gate width direction of the dimension 14a of the length direction (gate width direction) of the PN-junction border area C, i.e., the 3rd gate electrode, and the 4th gate electrode 15a, as mentioned above, it is desirable that it is beyond the superposition accuracy in a mask alignment process. As for the dose of the 3rd gate electrode 14a and the 4th gate electrode 15a, it is usually desirable that they are $2x10^{15}$ / cm^2 degree.

[Industrial applicability]

[0066]
A semiconductor device concerning the present invention, and a manufacturing method for the same, It is useful to a semiconductor device of the dual gate structure which prevented disconnection of the metal silicide film in a PN-junction border area, could avoid high resistance-ization of wiring, and was provided especially with the metal silicide film, a manufacturing method for the same, etc., without barring micronization and high integration of an element.
[Brief Description of the Drawings]
[0067]
[Drawing 1](a) And (b) shows typically the semiconductor device concerning one embodiment of the present invention, (a) is a plan view, and (b) is a cross sectional view in the Ib-Ib line of (a).
[Drawing 2](a) - (d) is a cross sectional view of process order showing typically the manufacturing method of the semiconductor device concerning one embodiment of the present invention.
[Drawing 3](a) - (d) is a cross sectional view of process order showing typically the manufacturing method of the semiconductor device concerning one embodiment of the present invention.
[Drawing 4](a) - (f) is a cross sectional view of process order showing typically the manufacturing method of the semiconductor device concerning a first conventional example.
[Drawing 5]It is a plan view showing the semiconductor device concerning a second conventional example.
[Explanations of letters or numerals]
[0068]
A N channel type MOS transistor region
B P channel type MOS transistor region
C PN-junction border area
10 Semiconductor substrate
11 Isolation region
12 N type active region
13 P type active region
14 A first gate electrode
15 A second gate electrode
14a The 3rd gate electrode
15a The 4th gate electrode
16 Gate dielectric film
17 Nickel silicide film
17A Nickel layer
20 Polycrystalline silicon film
21 A first resist film
22 A second resist film
23 The 3rd resist film
24 The 4th resist film

[Translation done.]

* NOTICES *

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damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]
Wiring consisting of silicon which is formed on a semiconductor substrate and has conductivity,
It has a metal silicide film formed after the aforementioned wiring,
The aforementioned wiring has the 1st region that shows the conductivity of N type, the 2nd region that shows the conductivity of P type, and the 3rd region formed between said 1st region and said 2nd region,
A semiconductor device, wherein said 3rd region is connected to said 1st region and said 2nd region and concentration of an impurity of said 3rd region is lower than concentration of an N type impurity of said 1st region, and concentration of a P type impurity of said 2nd region.
[Claim 2]
Said 1st region is a gate electrode of an N channel type transistor,
The semiconductor device according to claim 1, wherein said 2nd region is a gate electrode of a P channel type transistor.
[Claim 3]
The semiconductor device comprising according to claim 1 or 2:
The 4th region that said 3rd region is connected with said 1st region, and shows the conductivity of N type.
The 5th region that is connected with said 2nd region and shows the conductivity of P type.

[Claim 4]
A semiconductor device of a description in any 1 item of the Claims 1-3 which make it pile each other up and are characterized by being [in / in the length of a direction which connects said 1st region in said 3rd region, and said 2nd region / a mask alignment process] more than a dimension.
[Claim 5]
A semiconductor device of a description in any 1 item of the Claims 1-4, wherein the aforementioned metal silicide film consists of a nickel silicide, titanium silicides, or a cobalt silicide.
[Claim 6]
A process (a) of forming a wiring formation film consisting of silicon on a semiconductor substrate,
A process (b) of introducing an impurity of the 1st conductivity type into said 1st region of the aforementioned wiring formation film using the 1st mask layer that carries out the opening of the 1st region of the aforementioned wiring formation film,
A process (c) of introducing an impurity of the 2nd conductivity type into said 2nd region of the aforementioned wiring formation film using the 2nd mask layer that carries out the opening of said 1st region in the aforementioned wiring formation film, and the 2nd adjoining region,
The 3rd region that is some regions which touch a boundary part of said 2nd region of the aforementioned wiring formation film, and said 2nd region in said 1st region of the aforementioned wiring formation film with a wrap, A process (d) of introducing an impurity of the 1st conductivity type into the remainder of said 1st region in the aforementioned wiring formation film using the 3rd mask layer that carries out the opening of the remainder of said 1st region,
A process (e) of activating each impurity introduced into said 1st region, the 2nd region, and the 3rd region by heat-treating to the aforementioned wiring formation film,
A manufacturing method of a semiconductor device provided with a process (f) of forming a metal silicide film on the aforementioned wiring formation film.
[Claim 7]
Said 1st region is a gate electrode of an N channel type transistor,
A manufacturing method of the semiconductor device according to claim 6, wherein said 2nd region is a gate electrode of a P channel type transistor.
[Claim 8]
A manufacturing method of the semiconductor device according to claim 6 or 7 which makes it pile each other up and is characterized by being [in / in length from a boundary part with said 2nd region in said 3rd region to said 1st region side / a mask alignment process] more than a dimension.
[Claim 9]
Between the aforementioned process (d) and the aforementioned processes (e),
The 4th region that is some regions which touch a boundary part of said 1st region of the aforementioned wiring formation film, and said 1st region in said 2nd region of the aforementioned wiring formation film with a wrap, It has further a process (g) of introducing an impurity of the 2nd conductivity type into the remainder of said 2nd region in the aforementioned wiring formation film, using the 4th mask layer that carries out the opening of the remainder of said 2nd region,
A manufacturing method of the semiconductor device according to claim 6 or 7 also activating an impurity introduced into said 4th region

of the aforementioned wiring formation film in the aforementioned process (e).
[Claim 10]
Length from a boundary part with said 2nd region in said 3rd region to said 1st region side, and length from a boundary part with said 1st region in said 4th region to said 2nd region side, A manufacturing method of the semiconductor device according to claim 9 with which you make it pile each other up, and all are characterized by being more than a dimension in a mask alignment process.
[Claim 11]
A manufacturing method of a semiconductor device of a description in any 1 item of the Claims 6-10, wherein the aforementioned metal silicide film is a nickel silicide, titanium silicides, or a cobalt silicide.

[Translation done.]

Docket No.: 085393-0935
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Yoshihiro SATO et al.	:	Customer Number: 53080
Application No.: 13/665,376	:	Confirmation No.: 4442
Filed: October 31, 2012	:	Art Unit: 2897
For: SEMICONDUCTOR DEVICE	:	Examiner: L. T. Nguyen

AMENDMENT UNDER 37 C.F.R. § 1.111

Mail Stop - Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

In response to the Office Action dated March 18, 2014, having a three-month shortened statutory period for response set to expire June 18, 2014, please amend the above-identified application as set forth below.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A semiconductor device, comprising:

a first dual-gate electrode; and

a second dual-gate electrode being separated from the first dual-gate electrode, wherein

the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,

the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,

the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,

the first gate electrode and the second gate electrode are connected to each other on the isolation region, and

at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

2. (Original) The semiconductor device of claim 1, wherein an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.

3. (Withdrawn) The semiconductor device of claim 1, wherein at least a portion of the first

silicon film of the second conductivity type has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

4. (Withdrawn) The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

5. (Original) The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

6. (Withdrawn) The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

7. (Original) The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

8. (Withdrawn) The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first

conductivity type located on the isolation region.

9. (Withdrawn) The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

10. (Withdrawn) The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region.

11. (Cancelled)

12. (Withdrawn) The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

13. (Cancelled)

14. (Withdrawn) The semiconductor device of claim 1, wherein

a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region, and

a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

15. (Original) The semiconductor device of claim 1, wherein

the first gate electrode is a gate electrode of a first PMIS transistor,

the second gate electrode is a gate electrode of a first NMIS transistor,

the third gate electrode is a gate electrode of a second PMIS transistor, and

the fourth gate electrode is a gate electrode of a second NMIS transistor.

16. (Original) The semiconductor device of claim 1, wherein

each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and

each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claim 1 to further clarify the intended subject matter of the present disclosure. Support for the amendment to claim 1 can be found, for example, in paragraphs [0089]-[0090] and Figs. 9A-9D of the published application (USP Pub. No. 2013/0056832). In addition, claims 11 and 13 have been cancelled, without prejudice. No new matter has been added.

Upon allowance of claim 1 it is respectfully requested that claims 3, 4, 6, 8-10, 12 and 14, which are currently withdrawn, be rejoined. As claims 3, 4, 6, 8-10, 12 and 14 are dependent on claim 1, it is clear that claim 1 is generic to claims 3, 4, 6, 8-10, 12 and 14.

Further, it is noted on the Office Action Summary page that "some" of the priority documents have been received. However, it appears from the USPTO PAIR system records that all of the priority documents have been received. Applicants respectfully request that the next paper issued in this application make this indication.

For at least the reasons set forth below, it is respectfully submitted that the pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 103

Claims 1-2, 5, 7, 11, 13, 15 and 16 were rejected under 35 U.S.C. § 103 as being unpatentable over JP 2010-67912 to Shimomura in view of USP Pub. No. 2008/0036010 to Tamaki. For at least the following reasons, it is respectfully submitted that claim 1 is patentable over Shimomura and Tamaki, taken alone or in combination with one another.

First, it is stated in the pending rejection that the limitation of claim 1 reciting "at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region" was not considered because it does not pertain to the elected species. This conclusion is in error, as the foregoing limitation clearly reads on the elected species.

More specifically, the elected species was Species I, which corresponds to Figs. 9 and 10. The following sets forth how the limitation reads on the elected figures. Referring to Figs. 9A-9D and the limitation, "at least a portion (14b1, 14b2) of the first silicon film (14b) of the first conductivity type (P-type) has a first-conductivity-type (P-type) impurity concentration higher than that of a portion (14d) of the second silicon film (14d) of the first conductivity type (P-type) located on the third active region (10d)." This feature is expressly mentioned in paragraph [0091] of the specification, which states "[a] feature of this embodiment is that the p-type silicon film 14b1 has a p-type impurity concentration lower than that of the p-type silicon film 14b2. In addition, each of the p-type silicon film 14b1 and the p-type silicon film 14b2 has a p-type impurity concentration higher than that of the p-type silicon film 14d." (Emphasis added).

It is respectfully submitted that the foregoing explanation makes it clear that the limitation in question clearly reads on the elected species and therefore should have been examined. As this element has not been addressed in the pending rejection, for this reason alone the rejection is in error and should be withdrawn. Furthermore, the next Office Action issued in this application should not be made Final as the foregoing element should have been considered for examination purposes prior to the issuance of the current Office Action.

Turning to the pending rejection, it is noted that claim 1 now recites, *inter alia*, a first dual-

gate electrode; and a second dual-gate electrode ***being separated from the first dual-gate electrode.*** For example, referring to the exemplary embodiment illustrated in Figs. 9A-9D, the device includes a first dual-gate electrode (31L in Figs. 9A-9D) and a second dual-gate electrode (31S in FIGS. 9A-9D), which are independent and separate from each other.

Turning to the cited prior art references, first with regard to Shimomura, Shimomura only discloses one dual-gate electrode, and therefore, at a minimum, fails to disclose or suggest a second dual-gate electrode being separated from the first dual-gate electrode, as recited by claim 1.

More specifically, it is asserted that the first gate electrode 14 and the second gate electrode 15 of Shimomura correspond to the recited first dual-gate electrode, and that the third gate electrode 14a and the fourth gate electrode 14b of Shimomura correspond to the recited second dual-gate electrode.

However, as is shown in Fig. 1 of Shimomura, the third gate electrode 14a and the fourth gate electrode 15a are directly connected to each, and the first gate electrode 14 and the second gate electrode 15 are connected to each other with the third and fourth gate electrodes (14a & 15a) interposed therebetween. In other words, the first through fourth gate electrodes of Shimomura are connected together in a serial manner.

As such, it is clear that the alleged first dual-gate electrode (electrodes 14 and 15 of Shimomura) and the alleged second dual-gate electrode (electrodes 14a and 15a of Shimomura) are neither separated from each other, nor independent of each other. Indeed, the configuration of Shimomura is completely different from that of claim 1. Accordingly, at a minimum, Shimomura does not disclose a first dual-gate electrode and a second dual-gate electrode ***being separated from the first dual-gate electrode***, as recited by claim 1.

Furthermore, it is also asserted in the pending rejection that the third gate electrode 14a allegedly forming part of the second dual-gate electrode (14a & 15a) is located on the third active region 12a and the fourth gate electrode 15a is located on the fourth active region 13a. However, Shimomura does not appear to make any disclosure regarding a "third active region 12a" or a "fourth active region 13a." As shown in Figs. 1A and 1B of Shimomura, the third gate electrode 14a and the fourth gate electrode 15a are provided on an isolation region 11 and are not provided on any of an n-type active region 12 or a p-type active region 13. Thus, it is clear that Shimomura also fails to disclose or suggest a second dual-gate electrode including a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type, as recited by claim 1.

Turning to Tamaki, as this reference also fails to disclose or suggest a device including two dual-gate electrodes that are separated from each other and independent of each other, at a minimum, Tamaki does not cure the foregoing deficiencies of Shimomura, nor is it relied upon doing so.

Accordingly, as each and every element of the claim must be disclosed or suggested by the cited prior art references in order to establish a *prima facie* case of obvious (*see*, M.P.E.P. § 2143.03), and the combination of Shimomura and Tamaki fails to do so for at least the foregoing reasons, it is clear that claim 1 is patentable over the combination of Shimomura and Tamaki.

III. Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,* 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the pending independent claim is patentable for at least the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

IV. Summary

Applicant submits that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

/Michael E. Fogarty/

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

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Washington, DC 20001
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DATE: June 9, 2014
DM_US 52526074-1.085393.0935

Electronic Acknowledgement Receipt

EFS ID:	19247414
Application Number:	13665376
International Application Number:	
Confirmation Number:	4442
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Customer Number:	53080
Filer:	Michael E. Fogarty/Natherine Ordanza
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0935
Receipt Date:	09-JUN-2014
Filing Date:	31-OCT-2012
Time Stamp:	17:58:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		085393-0935_Amendment.pdf	363406 78fcdd5cd8c6c35782ca49297f5b2f48ccd0dbbf	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	10
Warnings:			
Information:			
	Total Files Size (in bytes):	363406	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/665,376	Filing Date 10/31/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT	06/09/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/ANTHONY WILLIAMS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

53080 7590 07/01/2014

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER
NGUYEN, LAWRENCE-LIN T

ART UNIT	PAPER NUMBER
2897	

DATE MAILED: 07/01/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935	4442

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/01/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 07/01/2014
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935	4442

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/01/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, LAWRENCE-LIN T	2897	257-369000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935	4442

53080 7590 07/01/2014

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER	
NGUYEN, LAWRENCE-LIN T	
ART UNIT	PAPER NUMBER
2897	

DATE MAILED: 07/01/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/665,376	Applicant(s) SATO ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *06/03/2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-10, 12, & 14-16*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/31/2012
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LAWRENCE-LINH T NGUYEN/
Examiner, Art Unit 2897

REASONS FOR ALLOWANCE

1. The present application is being examined under the pre-AIA first to invent provisions.

Election/Restrictions

2. Claims **1-10, 12 & 14-16** allowable. The restriction requirement of Method and device and species , as set forth in the Office action mailed on **10/24/2013** , has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Specifically, the restriction requirement of claims **3,4,6,8-10,12, & 14** are withdrawn. Claims **3,4,6,8-10,12, & 14** , directed to Species II no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim.

3. In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See In re Ziegler, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Allowable Subject Matter

4. Applicant's arguments see **Applicant Arguments/Remarks Made in an Amendment**, filed **06/09/2014**, with respect to the 103 Rejection of claims **1-7,9,11,13, & 15-16** have been fully considered and are persuasive.

5. In response to the Applicants' request, claims **1-16** are presented for examination with claims **11 & 13** are **canceled**.

6. This Office action is responsive to Applicants' application filed **06/09/2014**. The independent claim **1** is allowed.

7. The following is an examiner's statement of reasons for allowance:

a. With respect to independent claim **1**, the prior arts of record do not teach or fairly suggest a limitation of " a semiconductor device comprising:

i. *a second dual-gate electrode being separated from the first dual-gate electrode, wherein the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type.*

Thus, it is possible to reduce degradation of characteristics of FETs due to mutual diffusion of impurities between the n-type region and the p-type

region in the polysilicon gate electrode.

ii. Also claims **2-10, 12, 14-16** are depended on claim 1.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Applicant's Remarks

1. Applicant's arguments with respect to claims **1-7,9,11,13, & 15-16** have been considered and are persuasive.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAWRENCE-LINH T. NGUYEN whose telephone number is (571) 272-6267. The examiner can be reached on M-F (8AM - 4PM EST).

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on (571) 272-1867. The fax phone number for the organization where this application or proceeding is assigned is (571) 272-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (in USA or CANADA) or (571) 272-1000.

/**Lawrence-Linh T Nguyen**/

Examiner, Art Unit 2897

/Fernando L. Toledo/

Supervisory Patent Examiner, Art Unit 2897

Notice of References Cited	Application/Control No. 13/665,376	Applicant(s)/Patent Under Reexamination SATO ET AL.	
	Examiner LAWRENCE-LINH T. NGUYEN	Art Unit 2897	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0036010	02-2008	Tamaki et al.	257/372
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	2010-067912	03-2010	JAPAN		H01L21/0238
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		((second third four$2) adj active) near3 ((second third four$2) adj electrode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:21
L19	9428	((sram static adj ram$1 static adj ramdom adj acess adj mem)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/14 21:43
S1	1	"13665376"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 10:45
S2	186	((YOSHIHIRO) near2 (SATO)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/27 10:46
S3	68	((HIDEYUKI) near2 (ARAI)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/27 10:46
S4	208	((TAKAYUKI) near2 (YAMADA)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/27 10:46
S5	5	"20030107090" "20080036010"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 10:46
S6	17641	("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:10
S7	5987216	((concerntration n- n-type p- p-type second) adj$3 impurit$3) with (high$3 low$3 less more)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/08/27 14:15

			IBM_TDB			
S8	321	((second third four$2) adj active) near3 ((second third four$2) adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:21
S9	2	S6 and S7 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:26
S10	11019	S6 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:37
S11	288	(second multipl$3 third four) adj ("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:39
S12	829	(("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)) adj3 (CMIS NMISFET PMISFET MISFET MOSFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:43
S13	23	("5877535" | "5977591" | "20020093051" | "6180519" | "6586837" | "20020042173" | "20030173625" | "5837601" | "6191460" | "6489664" | "20010007368" | "20010006832").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:46
S14	103632	panasonic.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:46
S15	84	S14 and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:47
S16	44	("5877535" | "5977591" | "20020093051" | "6180519" | "6586837" | "20020042173" | "20030173625" | "5837601" |	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2013/08/27 15:50

		"6191460" | "6489664" | "20010007368" | "20010006832" | "5122474" | "6010929" | "20040183141" | "20040256653" | "5936844" | "20060138568" | "7129543" | "20070221960" | "7414292").PN.	EPO; JPO; DERWENT; IBM_TDB			
S17	187024	(sram static adj ram$1 static adj ramdom adj acess adj mem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:19
S18	23874	S17 and logic adj circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:20
S19	1985	S18 and (gate with (impurit$3 concerntration))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:21
S21	206	S19 and dual adj gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:22
S22	332415	((concerntration n- n-type p- p-type second) adj$3 impurit$3) with (high$3 low$3 less more) and ("257".clas. "438".clas.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:24
S24	715	((second third four$2) adj3 active) near3 ((second third four$2) adj electrode$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:26
S25	2567	transistor$1 near3 (PMIS NMIS MISFET NMISFET PMISFET CMIS) and ("257".clas. "438".clas.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:28
S26	1039	(("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)) near3 (CMIS NMISFET PMISFET MISFET MOSFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/08/27 17:28

			DERWENT; IBM_TDB			
S27	33	S25 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:31
S30	206	S21 and dual adj gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:41
S31	24133	S17 and logic adj (circuit area)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:49
S32	21	(US-20130062682-$ or US-20080283928-$ or US-20110008954-$ or US-20110006374-$ or US-20090130833-$ or US-20110086510-$ or US-20060138568-$ or US-20020042173-$ or US-20110198707-$ or US-20060292799-$ or US-20060275969-$ or US-20130193493-$).did. or (US-8013395-$ or US-7825482-$ or US-7598574-$ or US-7495298-$ or US-7414292-$ or US-6569742-$ or US-5977591-$).did. or (US-20090138840-$ or JP-2006303448-$).did.	US-PGPUB; USPAT; DERWENT	OR	ON	2013/09/26 20:24
S33	3200	257/392,903,E27.098.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:10
S34	196695	SRAM STATIC adj RAM STATIC adj RANDOM adj ACCESS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:12
S35	25092	S34 and LOGIC adj CIRCUIT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:12
S36	814721	("257" "438" "365").CLAS.	US-PGPUB; USPAT; USOCR;	OR	ON	2013/10/07 17:15

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S37	3	"13665376"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 07:48
S38	13	"20080036013"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 08:47
S39	1	("2008/0036013").URPN.	USPAT	OR	ON	2014/02/24 09:13
S40	2	("2004/0180522").URPN.	USPAT	OR	ON	2014/02/24 09:40
S41	19	("20030181005" | "20040104405" | "20040159834" | "20040180522" | "20050199958" | "20060148153" | "20060223255" | "20070108529" | "20070141775" | "20070235817" | "20070257308" | "20080064191" | "6479350" | "6492218" | "6762085" | "7015082" | "7026205" | "7449753").PN. OR ("7678636").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/02/24 09:41
S42	6	"11808620"	US-PGPUB; USPAT; USOCR	OR	ON	2014/02/24 09:46
S43	47	"2010067912" "6275788" "8017934"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 09:51
S44	3363	257/392,903,E27.098.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
S45	213729	SRAM STATIC adj RAM STATIC adj RANDOM adj ACCESS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
S46	26439	S45 and LOGIC adj CIRCUIT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/02/24 12:45

			DERWENT; IBM_TDB			
S47	855317	("257" "438" "365").CLAS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
S48	293	S44 and S45 and S46 and S47	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
S49	0	S48 and (add$3 introduc$3 inplant$3) with ((first second third) adj3 (conductive p- n-) adj impurity)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:47
S50	4	S48 and (add$3 introduc$3 inplant$3) near3 (((first second third) adj3 (conductive p- n-)) adj3 impurity)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:49
S51	5	S48 and (add$3 remov$3high$3 low$3 introduc$3 inplant$3) near3 (((first second third) adj3 (conductive p- n-)) adj3 impurity)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:55

6/ 14/ 2014 9:49:17 PM
C:\ Users\ LNguyen16\ Documents\ EAST\ Workspaces\ 13665376.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13665376	SATO ET AL.
	Examiner	**Art Unit**
	LAWRENCE-LINH T NGUYEN	2897

CPC						
Symbol					**Type**	**Version**
H01L		21	/	823842	F	2013-01-01
H01L		21	/	76895	I	2013-01-01
H01L		27	/	1116	I	2013-01-01
H01L		27	/	1104	I	2013-01-01
H01L		27	/	105	I	2013-01-01
H01L		21	/	28518	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
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/LAWRENCE-LINH T NGUYEN/ Examiner.Art Unit 2897	06/13/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	14	
/FERNANDO L TOLEDO/ Supervisory Patent Examiner.Art Unit 2897	06/16/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13665376	SATO ET AL.
	Examiner	**Art Unit**
	LAWRENCE-LINH T NGUYEN	2897

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
257	369	H	0	1	L	27 / 092 (2006.0)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	392	903	E27.098		

/LAWRENCE-LINH T NGUYEN/ Examiner.Art Unit 2897	06/13/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	14	
/FERNANDO L TOLEDO/ Supervisory Patent Examiner.Art Unit 2897	06/16/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13665376	SATO ET AL.
	Examiner	**Art Unit**
	LAWRENCE-LINH T NGUYEN	2897

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
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13	15														
14	16														

/LAWRENCE-LINH T NGUYEN/ Examiner.Art Unit 2897	06/13/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	14	
/FERNANDO L TOLEDO/ Supervisory Patent Examiner.Art Unit 2897	06/16/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13665376	SATO ET AL.
	Examiner	Art Unit
	LAWRENCE-LINH T NGUYEN	2897

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	369,392,903,E27.098	02/24/2014	LTN

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	369,392,903,E27.098	06/13/2014	LTN

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		((second third four$2) adj active) near3 ((second third four$2) adj electrode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:21
L19	9428	((sram static adj ram$1 static adj ramdom adj acess adj mem)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/14 21:43
S1	1	"13665376"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 10:45
S2	186	((YOSHIHIRO) near2 (SATO)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/27 10:46
S3	68	((HIDEYUKI) near2 (ARAI)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/27 10:46
S4	208	((TAKAYUKI) near2 (YAMADA)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2013/08/27 10:46
S5	5	"20030107090" "20080036010"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 10:46
S6	17641	("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:10
S7	5987216	((concerntration n- n-type p- p-type second) adj$3 impurit$3) with (high$3 low$3 less more)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/08/27 14:15

			IBM_TDB			
S8	321	((second third four$2) adj active) near3 ((second third four$2) adj electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:21
S9	2	S6 and S7 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:26
S10	11019	S6 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:37
S11	288	(second multipl$3 third four) adj ("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:39
S12	829	(("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)) adj3 (CMIS NMISFET PMISFET MISFET MOSFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:43
S13	23	("5877535" | "5977591" | "20020093051" | "6180519" | "6586837" | "20020042173" | "20030173625" | "5837601" | "6191460" | "6489664" | "20010007368" | "20010006832").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:46
S14	103632	panasonic.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:46
S15	84	S14 and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 14:47
S16	44	("5877535" | "5977591" | "20020093051" | "6180519" | "6586837" | "20020042173" | "20030173625" | "5837601" |	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2013/08/27 15:50

		"6191460" | "6489664" | "20010007368" | "20010006832" | "5122474" | "6010929" | "20040183141" | "20040256653" | "5936844" | "20060138568" | "7129543" | "20070221960" | "7414292").PN.	EPO; JPO; DERWENT; IBM_TDB			
S17	187024	(sram static adj ram$1 static adj ramdom adj acess adj mem)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:19
S18	23874	S17 and logic adj circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:20
S19	1985	S18 and (gate with (impurit$3 concerntration))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:21
S21	206	S19 and dual adj gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:22
S22	332415	((concerntration n- n-type p- p-type second) adj$3 impurit$3) with (high$3 low$3 less more) and ("257".clas. "438".clas.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:24
S24	715	((second third four$2) adj3 active) near3 ((second third four$2) adj electrode$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:26
S25	2567	transistor$1 near3 (PMIS NMIS MISFET NMISFET PMISFET CMIS) and ("257".clas. "438".clas.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:28
S26	1039	(("dual gate$1" "dual-gate$1" "double layer$1 gate" (dual multiple Bi) adj gate$1)) near3 (CMIS NMISFET PMISFET MISFET MOSFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/08/27 17:28

			DERWENT; IBM_TDB			
S27	33	S25 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:31
S30	206	S21 and dual adj gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:41
S31	24133	S17 and logic adj (circuit area)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/27 17:49
S32	21	(US-20130062682-$ or US-20080283928-$ or US-20110008954-$ or US-20110006374-$ or US-20090130833-$ or US-20110086510-$ or US-20060138568-$ or US-20020042173-$ or US-20110198707-$ or US-20060292799-$ or US-20060275969-$ or US-20130193493-$).did. or (US-8013395-$ or US-7825482-$ or US-7598574-$ or US-7495298-$ or US-7414292-$ or US-6569742-$ or US-5977591-$).did. or (US-20090138840-$ or JP-2006303448-$).did.	US-PGPUB; USPAT; DERWENT	OR	ON	2013/09/26 20:24
S33	3200	257/392,903,E27.098.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:10
S34	196695	SRAM STATIC adj RAM STATIC adj RANDOM adj ACCESS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:12
S35	25092	S34 and LOGIC adj CIRCUIT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/10/07 17:12
S36	814721	("257" "438" "365").CLAS.	US-PGPUB; USPAT; USOCR;	OR	ON	2013/10/07 17:15

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S37	3	"13665376"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 07:48
S38	13	"20080036013"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 08:47
S39	1	("2008/0036013").URPN.	USPAT	OR	ON	2014/02/24 09:13
S40	2	("2004/0180522").URPN.	USPAT	OR	ON	2014/02/24 09:40
S41	19	("20030181005" | "20040104405" | "20040159834" | "20040180522" | "20050199958" | "20060148153" | "20060223255" | "20070108529" | "20070141775" | "20070235817" | "20070257308" | "20080064191" | "6479350" | "6492218" | "6762085" | "7015082" | "7026205" | "7449753").PN. OR ("7678636").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/02/24 09:41
S42	6	"11808620"	US-PGPUB; USPAT; USOCR	OR	ON	2014/02/24 09:46
S43	47	"2010067912" "6275788" "8017934"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 09:51
S44	3363	257/392,903,E27.098.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
S45	213729	SRAM STATIC adj RAM STATIC adj RANDOM adj ACCESS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
S46	26439	S45 and LOGIC adj CIRCUIT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/02/24 12:45

			DERWENT; IBM_TDB			
S47	855317	("257" "438" "365").CLAS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
S48	293	S44 and S45 and S46 and S47	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:45
S49	0	S48 and (add$3 introduc$3 inplant$3) with ((first second third) adj3 (conductive p- n-) adj impurity)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:47
S50	4	S48 and (add$3 introduc$3 inplant$3) near3 (((first second third) adj3 (conductive p- n-)) adj3 impurity)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:49
S51	5	S48 and (add$3 remov$3high$3 low$3 introduc$3 inplant$3) near3 (((first second third) adj3 (conductive p- n-)) adj3 impurity)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/24 12:55

6/ 14/ 2014 9:50:01 PM
C:\ Users\ LNguyen16\ Documents\ EAST\ Workspaces\ 13665376.wsp

PTO/SB/08b (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	Not Yet Assigned
Filing Date	October 31, 2012
First Named Inventor	Yoshihiro SATO
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	085393-0935

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A1*	US-2003/0107090-A1	06-12-2003	Kumeno	Corresponds to JP 2003-179056-A
	A2*	US-2008/0036010-A1	02-14-2008	Tamaki et al.	Corresponds to JP 2008-042092-A

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	B1	JP-2010-067912-A	03-25-2010	Panasonic Corp	English Abstract	
	B2	JP-6-275788-A	09-30-1994	Ricoh Kk	English Abstract	
	B3	JP-8-017934-A	01-19-1996	Ricoh Kk	English Abstract	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		International Search Report issued in International Application No. PCT/JP2011/006167 oissued on January 24, 2011.	

Examiner Signature	/Lawrence-Linh Nguyen/	Date Considered	10/07/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.N./

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13665376	SATO ET AL.
	Examiner	Art Unit
	LAWRENCE-LINH T NGUYEN	2897

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/24/2014	06/14/2014							
	1	✓	=							
	2	✓	=							
	3	-	=							
	4	-	=							
	5	✓	=							
	6	-	=							
	7	✓	=							
	8	-	=							
	9	-	=							
	10	-	=							
	11	✓	-							
	12	-	=							
	13	✓	-							
	14	-	=							
	15	✓	=							
	16	✓	=							

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 07/01/2014
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935	4442

TITLE OF INVENTION: SEMICONDUCTOR DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/01/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, LAWRENCE-LIN T	2897	257-369000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 McDermott Will & Emery LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Panasonic Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Osaka, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-0417 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Ramyar M. Farid/ Date August 6, 2014

Typed or printed name Ramyar M. Farid Registration No. 46,692

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	13665376
Filing Date:	31-Oct-2012
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Filer:	Ramyar Farid/Doris Barnes
Attorney Docket Number:	085393-0935

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt

EFS ID:	19790022
Application Number:	13665376
International Application Number:	
Confirmation Number:	4442
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Customer Number:	53080
Filer:	Ramyar Farid/Doris Barnes
Filer Authorized By:	Ramyar Farid
Attorney Docket Number:	085393-0935
Receipt Date:	06-AUG-2014
Filing Date:	31-OCT-2012
Time Stamp:	17:44:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$960
RAM confirmation Number	4311
Deposit Account	500417
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	P615651-01_FEE_085393-0935.pdf	180029 c2ca72532780b6153c3f13add3ff679215b208e2	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30195 f978c54c1477c0ab885c5637e81c4a6cb6e489e4	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	210224		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935	4442

53080 7590 08/21/2014

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER	
NGUYEN, LAWRENCE-LIN T	
ART UNIT	**PAPER NUMBER**
2897	

NOTIFICATION DATE	DELIVERY MODE
08/21/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 13665376
Applicant : Sato
Filing Date : 10/31/2012
Date Mailed : 08/21/2014

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED.

See attachment(s).

A copy of this notice MUST be returned with the reply. Please address response to "Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

/Shirley Winslow/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 13665376

IDENTIFICATION OF APPLICATION DEFICIENCIES

☐ Applicant must provide legible text for the following item(s).

- ☐ Specification filed , page(s) .
- ☐ Claims filed , claim(s) .
- ☐ Oath/declaration filed .
- ☐ Other: .

☒ Applicant must provide missing information on the following page(s) of the specification by amending the specification to add the missing text. No new matter may be added. p. 7 (line 5) - incomplete sentence

☐ The specification refers to one or more applications by attorney docket number and does not show the U.S. application number(s). Applicant must supply the U.S. application number in place of each attorney docket number.

☐ Applicant must provide an Abstract of the Disclosure.

☐ Applicant has submitted a DECLARATION (37 CFR 1.63) FOR A UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) (e.g., form PTO/SB/01A). The Application Data Sheet, however, is not present with the filed application. Applicant must submit an Application Data Sheet or file a new oath or declaration (e.g., PTO/SB/01) executed by the inventors and containing the information required in 37 CFR 1.63.

☐ Applicant must provide an executed declaration.

☐ Applicant must provide the missing page(s) of the oath/declaration or Application Data Sheet filed

☐ Applicant must provide a declaration signed by inventor(s) .

☐ The oath/declaration filed shows non-initialed and/or non-dated alterations. Applicant must file a new oath/declaration in compliance with 37 CFR 1.67(a).

☐ Applicant(s) in the latest-filed oath/declaration or Application Data Sheet (ADS) did not show the inventor's residence at all, or did not show both a city and state in the U.S. inventor's residence, or did not show both a city and country in the non-U.S. inventor's residence. Applicant must supply an oath/declaration or Application Data Sheet (ADS) that shows each U.S. inventor's city and state of residence and each non-U.S. inventor's city and country of residence.

Docket No.: 085393-0935
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Customer Number: 53080
Yoshihiro SATO et al.	Confirmation Number: 4442
Application No.: 13/665,376	Group Art Unit: 2897
Filed: October 31, 2012	Allowed: July 1, 2014
For: SEMICONDUCTOR DEVICE	Examiner: L. T. Nguyen

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. 1.312

MS Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

INTRODUCTORY COMMENTS

Prior to issuance of the patent, applicant respectfully requests entry on this amendment under 37 C.F.R. 1.312 for the above-captioned patent application.

Amendments to the Specification begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on page 7 at line 1 as follows:

In the semiconductor device, a portion of the first silicon film of the first conductivity type located on each of the first active region and the isolation region may have a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

~~a portion of the first silicon film of the second conductivity type located on the second active~~

REMARKS

In response to the Notice to File Corrected Application Papers issued on August 21, 2014, the specification is being amended on page 7, line 5. No new matter has been introduced.

If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark Office determines that an extension is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 50-0417 referencing docket no. 085393-0935.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0417, under Order No. 085393-0935 from which the undersigned is authorized to draw.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. **53080 as our correspondence address.**

500 North Capitol Street, N.W
Washington, DC 20001
Phone: (202) 756-8372 MEF:mjb
Facsimile: (202) 756-8087
Date: October 6,2014

Electronic Acknowledgement Receipt

EFS ID:	20339988
Application Number:	13665376
International Application Number:	
Confirmation Number:	4442
Title of Invention:	SEMICONDUCTOR DEVICE
First Named Inventor/Applicant Name:	Yoshihiro SATO
Customer Number:	53080
Filer:	Michael E. Fogarty
Filer Authorized By:	
Attorney Docket Number:	085393-0935
Receipt Date:	06-OCT-2014
Filing Date:	31-OCT-2012
Time Stamp:	17:50:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P61565101_F-RES_085393-0935.pdf	236195 2975a1f5f4bed8bdac774f4abc2a4b19e782e2bd	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment after Notice of Allowance (Rule 312)	1	1
	Specification	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	236195	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935	4442

53080 7590 10/14/2014

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER	
NGUYEN, LAWRENCE-LIN T	
ART UNIT	**PAPER NUMBER**
2897	

NOTIFICATION DATE	DELIVERY MODE
10/14/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

Response to Rule 312 Communication	Application No.	Applicant(s)
	13/665,376	
	Examiner	Art Unit

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on *06 October 2014* under 37 CFR 1.312 has been considered, and has been:

a) ☒ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

N.Y. Horne

PUBLISHING DIVISION

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/665,376	11/11/2014	8884373	085393-0935	4442

53080 7590 10/22/2014

McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 5 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yoshihiro SATO, Toyama, JAPAN;
Hideyuki ARAI, Toyama, JAPAN;
Takayuki YAMADA, Toyama, JAPAN;
PANASONIC CORPORATION, Osaka, JAPAN

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: ADVANCED INTEGRATED CIRCUIT PROCESS LLC

Application No./Patent No.: 8884373 Filed/Issue Date: November 11, 2014

Titled: SEMICONDUCTOR DEVICE

ADVANCED INTEGRATED CIRCUIT PROCESS LLC, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: the inventors To: PANASONIC CORPORATION

   The document was recorded in the United States Patent and Trademark Office at

   Reel 031968, Frame 0653, or for which a copy thereof is attached.

2. From: PANASONIC CORPORATION To: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD.

   The document was recorded in the United States Patent and Trademark Office at

   Reel 052755, Frame 0917, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD. To: NUVOTON TECHNOLOGY CORPORATION JAPAN

The document was recorded in the United States Patent and Trademark Office at
Reel 067711, Frame 0965, or for which a copy thereof is attached.

4. From: NUVOTON TECHNOLOGY CORPORATION JAPAN To: ADVANCED INTEGRATED CIRCUIT PROCESS LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 068118, Frame 0314, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Szymon M. Gurda/	December 12, 2024
Signature	Date
Szymon M. Gurda	58451
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
13/665,376	**12/11/2024 11:41:44 PM Z ET**	**085393-0935**

Title of Invention

SEMICONDUCTOR DEVICE

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	8884373
CONFIRMATION #	4442	FILED BY	Yi Lu
PATENT CENTER #	68336260	FILING DATE	10/31/2012
CUSTOMER #	53080	FIRST NAMED INVENTOR	Yoshihiro SATO
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Szymon Gurda

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA.pdf	2	Power of Attorney	1466 KB
aia0096.pdf	3	Assignee showing of ownership per 37 CFR 3.73	119 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA.pdf	34207C3611E6629D65969A7C17C66B6BB5F661DF5FD562FA2 BBEDA0F38C8BA554F7D554764410E6A2A3E7360119AD1F8D CC8D25AA7B9BB5DFB5214543C550473
aia0096.pdf	7116039083E6870D5F7E6DC63C127E4045417EB884BC678D9 E8CDDE358C1F61D209EA9EF20FDF5E1BF8624D21726B6CFB

CF1A48205A5CAD9AFF3F5FA04B6D03E

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/81A (02-15)
Approved for use through 03/31/2021. OMB 0651-0035
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PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Patent Number	8884373
Issue Date	November 11, 2014
First Named Inventor	Yoshihiro SATO
Title	SEMICONDUCTOR DEVICE
Attorney Docket No.	0889-04193

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 27197

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Patent Owner

Signature		Date	November 18, 2024
Name	Szymon Gerda	Telephone	
Title and Company	Authorized Signatory, ADVANCED INTEGRATED CIRCUIT PROCESS LLC		

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935

CONFIRMATION NO. 4442

53080
Rimon PC - Panasonic Corporation
8300 Greensboro Dr.
Suite 500
McLean, VA 22102

POWER OF ATTORNEY NOTICE

OC000000081861587

Date Mailed: 12/13/2024

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/11/2024.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tawashington/

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/665,376	10/31/2012	Yoshihiro SATO	085393-0935

CONFIRMATION NO. 4442

27197
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POA ACCEPTANCE LETTER

OC000000081861621

Date Mailed: 12/13/2024

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/11/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tawashington/