

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner.

IPR2025-01302

U.S. Patent No. 8,884,373

**DECLARATION OF JACK LEE, PH.D. IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF U.S. PATENT 8,884,373**

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent 8,884,373 to Sato et al. (“the ’373 patent”)
1002	File History of U.S. Patent 8,884,373 (“’373 File History”)
1003	Declaration of Dr. Jack Lee in Support of IPR Petition
1004	CV of Dr. Jack Lee
1005	Translated Excerpts from File History of Japanese Patent No. 5857225 to Sato et al. (“JP ’225 patent”) (Japanese counterpart of the ’373 Patent)
1006	U.S. Publication 2008/0036010 to Tamaki, et al. (“Tamaki”)
1007	U.S. Publication 2008/0042218 to Igarashi, et al. (“Igarashi”)
1008	Japanese Patent No. 9181194 to Sumi (“Sumi”)
1009	Certified Translation of Japanese Patent No. 9181194 to Sumi
1010	U.S. Publication 2009/0096031 to Ekbote, et al. (“Ekbote”)
1011	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1012	Weste, “CMOS VLSI Design: A Circuits and Systems Perspective” (Third Edition, 2005) (“Weste”)
1013	Wolf, “Silicon Processing for the VLSI Era, Volume 4 – DeepSubmicron Process Technology” (2002) (“Wolf-4”)
1014	Van Zant, “Microchip Fabrication” (Fifth Edition, 2004) (“Van Zant”)
1015	“International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures” (2007 Edition) (“ITRS”)
1016	U.S. Patent No. 8,355,269 to Zampaglione (“Zampaglione”)

Exhibit	Description
1017	Sze, “Semiconductor Devices: Physics and Technology” (2nd Edition) (2002) (“Sze”)
1018	U.S. Patent 5,208,184 to Bayraktaroglu (“Bayraktaroglu”)

I, Dr. Jack Lee, declare as follows:

1. I have been retained by Taiwan Semiconductor Manufacturing Company Ltd. (“TSMC” or “Petitioner”) as a technical expert witness in connection with the petition for *Inter Partes* Review (“IPR” or “Petition”) of U.S. Patent 8,884,373 to Sato (“the ’373 patent”). To the best of my knowledge, the ’373 patent is currently assigned to Advanced Integrated Circuit Process LLC (“Patent Owner”).

2. Petitioner has asked me to offer opinions regarding the ’373 patent, including (i) the patentability of the claims in view of certain prior art references and the knowledge of a person of ordinary skill in the art (“POSITA”) and (ii) the relationship between the ’373 specification and those claim limitations. This declaration sets forth the opinions I have reached to date.

3. All opinions herein are based on the materials I have reviewed and on my professional judgment. I am over 18 years of age, have personal knowledge of the facts stated, and could competently testify to them if called.

4. I am being compensated for my time at my standard consulting rate and reimbursed for reasonable expenses. My compensation does not depend on the substance of my opinions or the outcome of this proceeding, and I have no financial interest in the ’373 patent or in the result of this IPR.

I. Qualifications

5. I am an expert in the field of semiconductor process technology and semiconductor design with more than 40 years' experience as a researcher, educator, and consultant.

6. The opinions below draw on education, training and experience; a detailed account appears in my curriculum vitae ("CV") (Ex.TSMC-1004).

7. I earned a B.S. with highest honors (1980) and M.S. (1981) in Electrical Engineering, from University of California, Los Angeles, and a Ph.D. in Electrical Engineering (1988) from University of California, Berkeley.

8. From 1979 to 1984, I served as a Member of Technical Staff at the TRW Microelectronics Center, where I worked on high-speed bipolar device/circuit design, fabrication, and testing and was promoted to Engineering Group Leader in 1983.

9. While at UC Berkeley I received several academic honors, including the 1988 IEEE International Reliability Physics Symposium Best Paper Award and a competitive Lectureship with dedicated teaching assistantship.

10. After completing my doctorate, I joined the faculty at The University of Texas at Austin in August 1988. I have taught undergraduate and graduate courses in semiconductor device fabrication and design, supervised more than forty Ph.D. students, and since 2000 have held the Cullen Trust for Higher Education

Endowed Professor in Engineering in the Department of Electrical and Computer Engineering. I became Professor Emeritus level in September 2023.

11. My current research and teaching interests include advanced MOSFETs, memory devices, high-k gate dielectrics and gate electrodes, reliability physics, and modeling, packaging, photovoltaic technologies, and alternative channel materials.

12. I have been invited to present tutorials, short courses and plenary talks various topics including high-k gate stacks in leading conferences such as the Symposium on VLSI Technology and the IEEE International Electron Devices Meeting (IEDM). My research group at UT Austin was among the first to develop hafnium-based high-k for nanoscale MOSFETs, and I have published extensively on HfO₂, HfSiON, hafnium silicate, interfacial engineering, and dielectric reliability.

13. My research has been supported by the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, among others.

14. I have authored more than 600 journal and conference papers, co-authored eight book or book chapters, and am a named inventor on nine U.S. patents. My work has received multiple best-paper and inventor awards.

15. In 2002, I was elected an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices,” and I served as an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

16. I regularly consult for semiconductor companies and consortia, teach industrial short courses, and organized international conferences, including the International Symposium on VLSI Technologies and IEDM.

II. Materials Considered

17. The '373 patent is a continuation of International Application No. PCT/JP2011/006167 (the “'167 PCT application”), which published as WO 2012/131818. In reaching the opinions provided herein, I have considered the '373 patent, its U.S. prosecution history, the prosecution history of foreign patent JP 5857225 B2, which is a national phase entry of the '167 PCT application, and the references cited in my Declaration or Attachment A hereto.

18. I have also relied upon my own education, training, research, knowledge, and personal and professional experience in the field and have also considered the viewpoint of a person of ordinary skill in the art at the time of the '373 patent's priority date. As explained below, I am familiar with the level of skill of a person of ordinary skill in the art regarding the technology at issue as of that time frame.

19. In general, I have been asked to cite to the specification of a patent or patent publication using the following formats: (Patent, Col:Line Number(s)) or (Patent, Paragraph Number(s)). For example, the citation (TSMC-1001, 1:1-10) points to the '373 patent specification at column 1, lines 1-10. Also, for convenience, I have been asked to use italics to denote limitations from the challenged claims. Unless otherwise noted, all emphasis added.

III. Understanding of Relevant Legal Principles

20. I am not a lawyer, and I will not provide any legal opinions. Although I am not a lawyer, I have been advised certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims.

A. Anticipation and Obviousness

21. I understand that the prior art to the '373 patent includes patents and printed publications in the relevant art that (1) were published more than a year before the filing date of the '167 PCT application (November 4, 2011), or (2) otherwise predate the filing date of the '167 PCT application. I further understand that, for purposes of this proceeding in the United States Patent Trial and Appeal Board, only patents and documents that have the legal status of a "printed publication" may be relied on as prior art.

22. I understand that a patent claim is anticipated if a single prior art document describes every element of the claim such that a person of ordinary skill in the art (“POSITA”) could practice the claimed method without undue experimentation.

23. I understand that a patent claim is invalid if it would have been obvious to a person of ordinary skill in the art. I further understand that in analyzing the obviousness of a claim, the following factors may be taken into account: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the art; and (4) any so called “secondary considerations” of non-obviousness, if they are present. I am not aware of any evidence of secondary considerations of non-obviousness relevant to the ’373 patent. I reserve the right to supplement this Declaration if Patent Owner (“PO”) introduces evidence of secondary considerations of non-obviousness.

24. I understand that to prove that prior art or a combination of prior art renders a patent obvious, it is necessary to:

- (1) identify the particular references that, singly or in combination, make the patent obvious;
- (2) specifically identify which elements of the patent claim appear in each of the asserted references; and

(3) explain why a person of ordinary skill in the art would have combined the references, and how they would have done so, to create the inventions claimed in the patent. I further understand that exemplary rationales that may support a conclusion of obviousness include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of known technique(s) to improve similar devices (methods or products) in the same way;
- applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- “obvious to try” – choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a person of ordinary skill in the art; and
- some teaching, suggestion, or motivation in the prior art that would have led a person of ordinary skill in the art to modify the prior art

reference or to combine prior art reference teachings to arrive at the claimed invention.

25. I understand that anticipation or obviousness may be by express disclosure in the prior art. I also understand that a patent claim is invalid if it is anticipated or obvious in view of the prior art, and that a claim can be unpatentable even if all of the requirements of the claim cannot be found in a single prior-art reference. For example, I also understand that if the prior art references does not expressly set forth a particular claim element, the prior art may still anticipate or render obvious a patent claim if that element is “inherent” in its disclosure—that is, if it is necessarily found in the reference. A property is inherent even if a POSITA would not have appreciated that property as of the date of that prior art.

26. I understand that invalidity of a claim requires that the claim be anticipated or obvious from the perspective of a person of ordinary skill in the art at the time the invention was made. To that end, I understand that in considering obviousness, hindsight reasoning derived from the patent-at-issue may not be used.

27. I understand that some claims are independent, and that these claims are complete by themselves. Other claims refer to these independent claims and are “dependent” from those independent claims. The dependent claims include all of the limitations of the claims on which they depend. Moreover, although I understand that preambles are not ordinarily treated as claim limitations, but for

my declaration only, have been asked to complete my analysis as if the preambles were deemed limiting.

B. Claim Construction

28. I understand that “claim construction” is the process of determining a patent claim’s meaning. I understand the claim construction standard used in IPRs seeks to give claim terms their plain and ordinary meaning to a POSITA at the time of the claimed invention in view of the claims, specification, and prosecution history. I also understand that if the patent applicant gave a term a special meaning in the specification or during prosecution, then the special meaning should be used.

29. In my declaration, I apply the above understanding. In my view, no claim terms require explicit construction in this proceeding to resolve patentability of the claims.

C. Level of Ordinary Skill in the Art

30. I understand that certain issues relating to the validity of a patent must be judged from the perspective of a person of ordinary skill in the relevant art, as I discuss below. I have been asked to define the level of a “person of ordinary skill in the art” or “POSITA” at the time the alleged invention as claimed was made (which as discussed above, I have assumed to be November 4, 2011, for the ’373 patent). In deciding the level of ordinary skill, I have considered the following

factors, which I have been informed are relevant to the determination of ordinary skill in the art.

- levels of education and experience of persons working in the field;
- types of problems encountered in the art;
- prior art solutions to these problems;
- rapidity with which innovations are made; and
- sophistication of the technology.

31. In my opinion, a POSITA at the time of the alleged invention of the '373 patent would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing, including planar and 3-dimensional transistors. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.

32. My opinions regarding the level of ordinary skill in the art are based on, among other things, my experience conceiving, patenting, and prototyping novel technology for semiconductor devices and semiconductor fabrication processes. Although my qualifications and experience exceed those of the hypothetical person having ordinary skill in the art, my analysis and opinions regarding the '337 patent have been based on the perspective of a person of ordinary skill in the art as of March 25, 2011.

IV. '373 Patent – Technical Background and Overview

33. The '373 patent, titled “Semiconductor Device,” to Yoshihiro Sato, et al., was filed on October 31, 2012, as a continuation application of International Application No. PCT/P2011/006167 (filed on November 4, 2011), which claims priority to Japanese Application No. 2011-068131 (filed on March 25, 2011). Solely for purposes of this IPR, I have been asked to assume March 25, 2011 as the earliest priority date of the '373 patent.

34. At a high level, the '373 patent relates to metal insulator semiconductor field-effect transistors (MISFETs), and specifically to semiconductor devices that include complementary MISFETs with dual-gate electrodes, where the silicon films of the gate electrodes are have different arrangements of impurity concentrations. (TSMC-1001, Abstract, 3:47-67, 4:5-9, 4:10-14, 4:20-25.) I will discuss this concept, which was known in the art before the priority date of the '373 patent, in greater detail below.

A. Technical Background

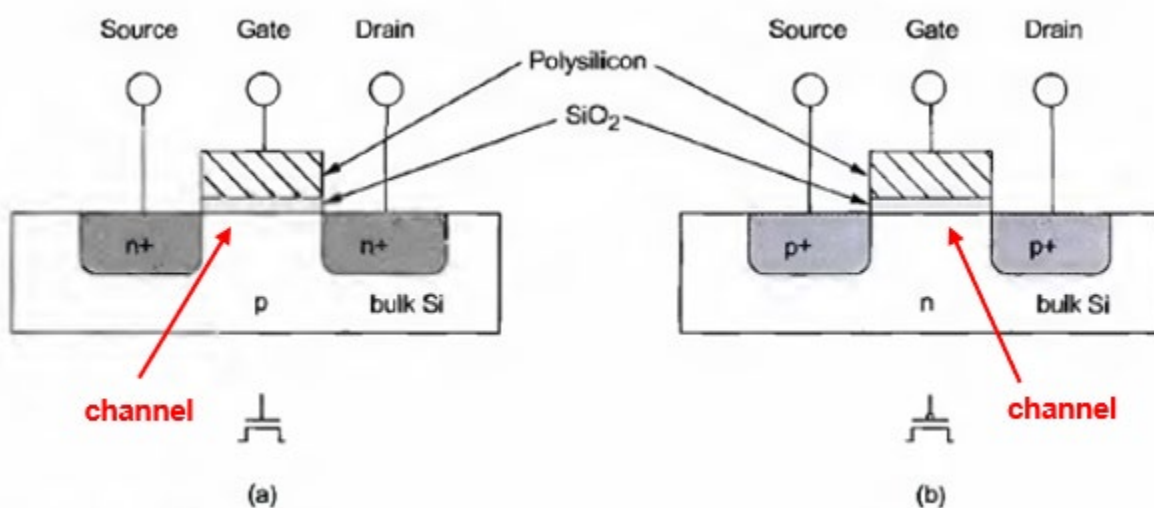
35. A semiconductor device is an electronic component that exploits the properties of semiconductor materials such as silicon, germanium, gallium arsenide, etc. Many types of semiconductor devices exist including, for example, diodes and metal-insulator-semiconductor (MIS) transistors (e.g., field effect transistors (FETs)), to name a few. (*See, e.g.,* Plummer, 33-41.) In this Declaration,

I will focus primarily on FET devices, and more particularly on MISFET devices and complementary MISFET devices which are described in further detail below.

1. MISFET/MOSFET

a. Structure

36. A MOSFET generally includes a stack of the conducting gate, an insulating layer, and “the silicon wafer, also called the *substrate*, *body* or *bulk*.” (Weste, 8 (italics in original).) The substrate can be doped with impurities (e.g., arsenic for n-type or boron for p-type) to influence the electrical behavior of the transistors built on it. A planar nMOS transistor “is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the *source* and *drain*” as illustrated in Figure 1.8(a) from “CMOS VLSI Design: A Circuits and Systems Perspective” by Weste (“Weste”). (*Id.* (italics in original).) The source and drain are physically equivalent and often they are regarded as interchangeable. (*See, e.g., Id.*) A planar pMOS transistor, illustrated below in Weste’s Figure 1.8(b), “is just the opposite, consisting of p-type source and drain regions with an n-type body.” (*Id.*)



Weste, Figure 1.8

37. “In CMOS technology with both flavors of transistors, the substrate is either n-type or p-type” and the “other flavor of transistor must be built in a special well in which dopant atoms have been locally added to form the body of the opposite type.” (Weste, 8.) One of the first steps in most CMOS processes is to define the well regions for the transistors. (Weste, 117.) As shown in the exemplary triple well below, a deep n-well is driven into the p-substrate and shallower n-well and p-well regions are implanted. (*Id.*) After the wells are formed, the doping levels can be adjusted to set the desired threshold voltages for the nMOS and pMOS transistors. (*Id.*) I discuss threshold voltage in further detail in §IV.A.2.

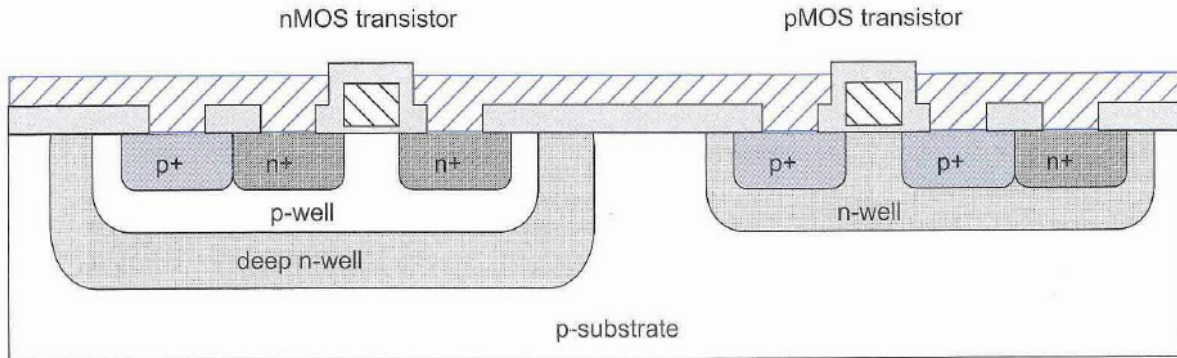
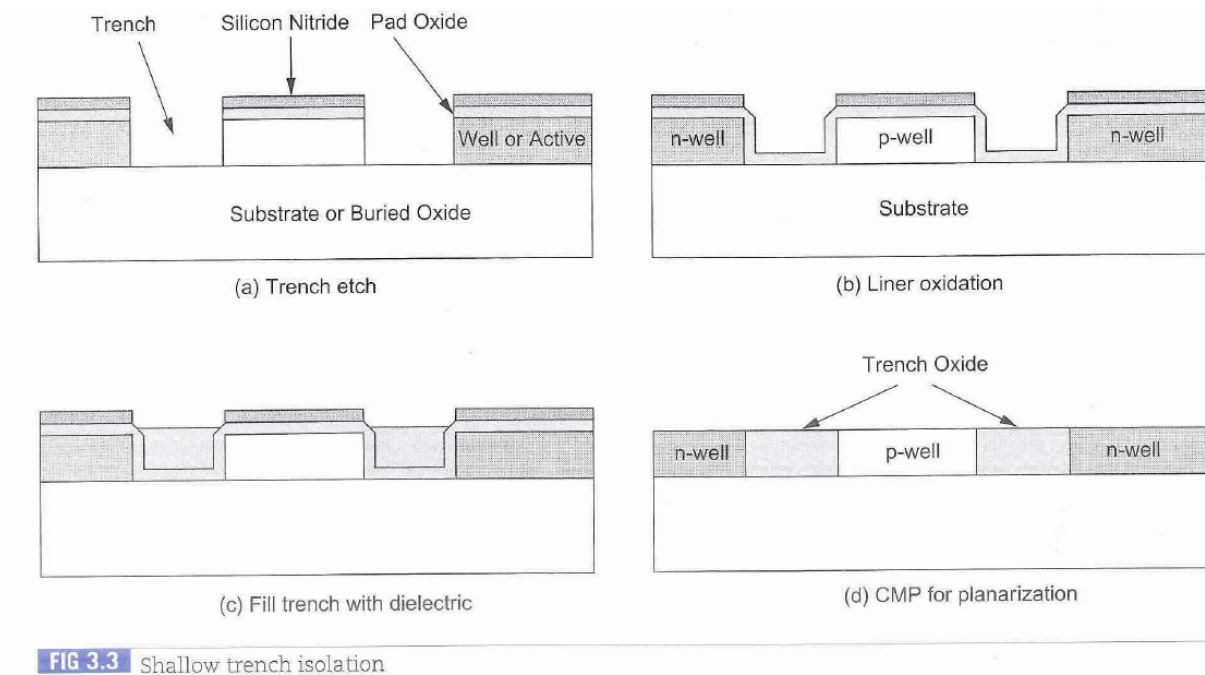


FIG 3.2 Well structure in triple-well process

Weste, Figure 3.2

38. Individual devices “need to be isolated from one another so that they do not have unexpected interactions.” (Weste, 119.) Therefore, one of the early steps in the fabrication process is the creation of structures to isolate the devices. One common technique to achieve isolation is referred to as **shallow trench isolation** (STI). (See, e.g., Weste, 117.) In STI, trenches are etched into the silicon and filled with an insulating material which isolates the active areas of the silicon wafer and prevents electrical interference between adjacent transistors. (Weste, 119.) Figure 3.3 from Weste illustrates STI regions.



Weste, Figure 3.3

(1) Gate Electrode

39. Gates of early transistors were built from metal so the gate stack “was called metal-oxide-semiconductor” (“MOS”). (Weste, 8.) Gates later migrated to polycrystalline silicon (polysilicon or poly), a conductive non-metal material, due to its stability and compatibility with silicon. However, “the name [MOS] stuck.”

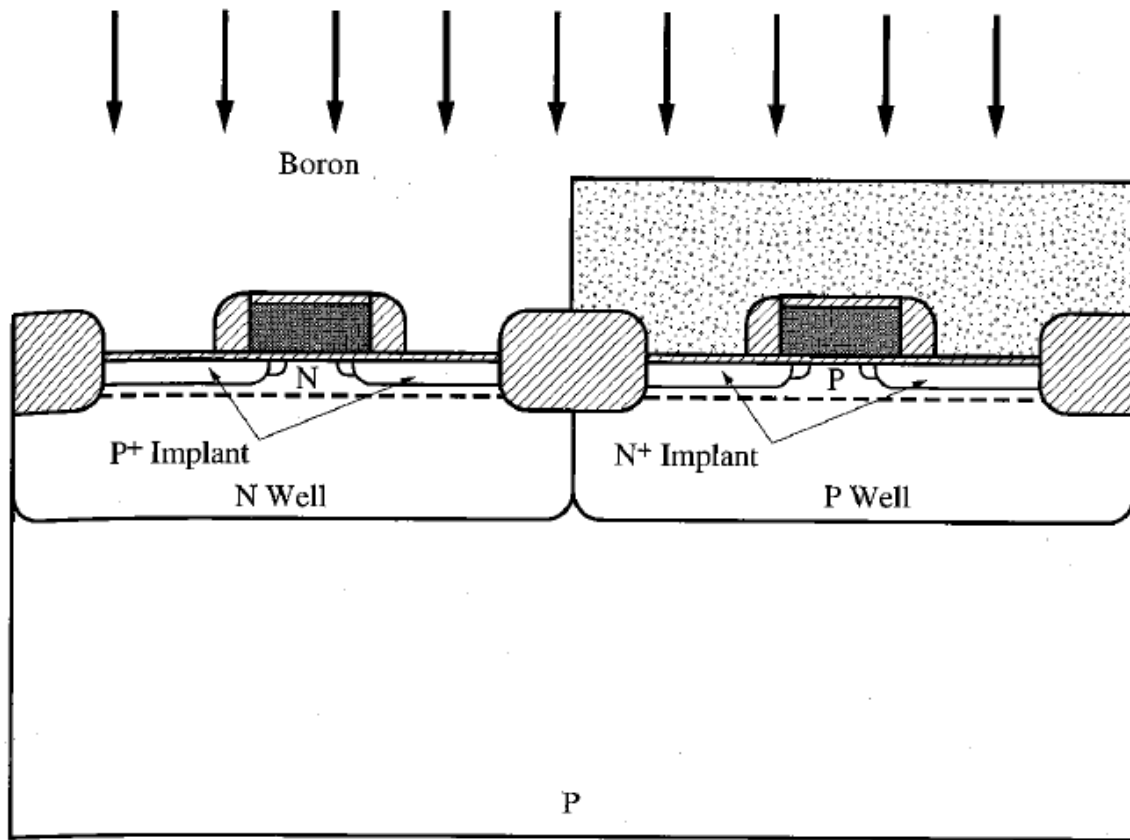
(*Id.*)

(2) Source and Drain

40. The source and drain regions in a transistor are formed by implanting dopants (either n-type or p-type) into the silicon substrate on both sides of the gate electrode. Dopants either contribute extra electrons and become n-type dopants, or they contribute extra holes (i.e., electron vacancies or positively charged carriers)

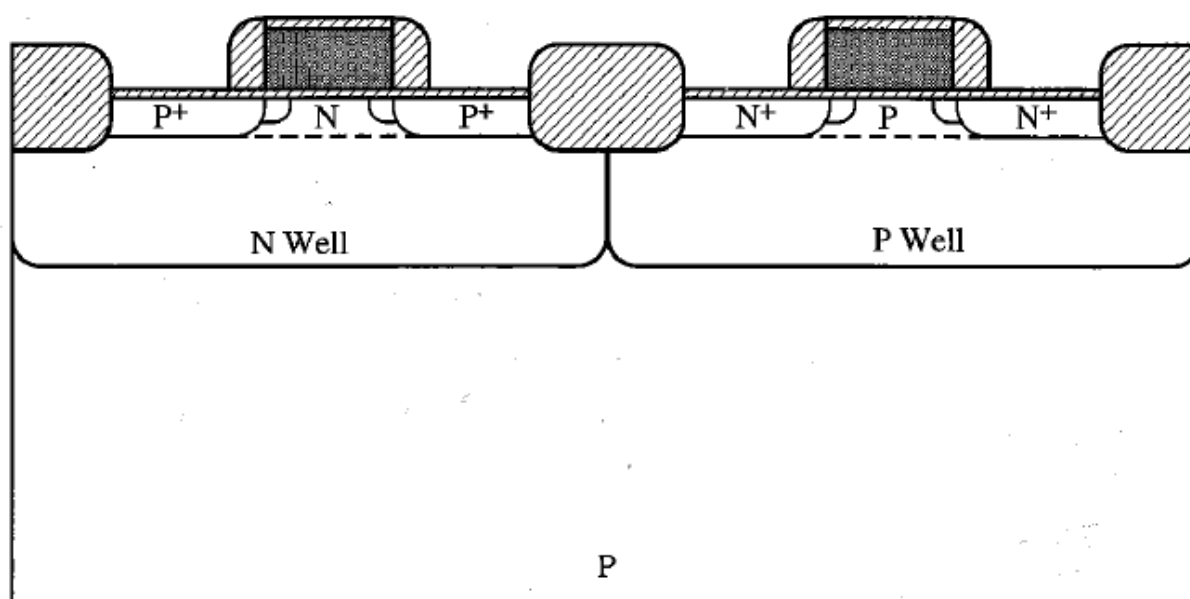
and become p-type dopants. (Plummer, 20.) As a result, to the extent the doping concentration is accurately controlled, the free electron and hole concentrations, and therefore the conductivity of the silicon substrate, can be precisely controlled. (*Id.*) Thus, these regions are heavily doped to improve conductivity and facilitate current flow when the transistor is on. The formation of these regions is critical for defining the transistor's electrical characteristics.

41. The formation of the source/drain regions involves one or more annealing steps necessary to electrically activate the dopants and repair the crystal structure of the body from the ion bombardment. (Plummer, 80-82.) “Silicon VLSI Technology: Fundamentals, Practice and Modeling” by Plummer, et al. (“Plummer”) describes an example of source/drain formation for a CMOS device. As shown in Plummer’s Figure 2-31 below, in a first source/drain implant, photoresist and mask are used to define regions where NMOS source/drain implants are done. (Plummer, 80.) An Arsenic implant then forms the NMOS source and drain regions.



Plummer, Figure 2-32

43. “Because the ion implantation process creates damage, most dopants are not electrically active at the end of the implantation.” (Plummer, 470.) To activate the dopants, the wafers are subjected to a rapid thermal anneal, often called a RTA, typically done at a temperature over 1000°C. (*See, e.g.,* Plummer, 81.) The RTA time can range from one second to a few minutes, with more advanced technologies using the shorter times. (*See, e.g.,* Plummer, 393-394.)



Plummer, Figure 2-33

44. The dopant activation is not the only annealing step performed during the chip manufacturing process and additional annealing steps or thermal process steps at different stages of the integrated circuit fabrication are necessary. For example, formation of a silicide on the gate and source/drain terminals also requires an annealing step to promote the silicidation process and the deposition of dielectric and/or metal layers may occur at elevated temperatures (e.g., at 600 °C or above). (Wolf, 608, 611.) And because thermal processing steps and/or annealing steps can cause thermal diffusion of species between previously formed layers, the transistors are engineered to account for the diffusion of species occurring during these thermal processing and/or annealing steps. (Van Zant, 345.)

b. Operation

45. A MOS transistor is a majority carrier device “in which the current in a conducting channel between the source and drain is controlled by a voltage applied to the gate.” (Weste, 67.) Generally, in a MOSFET, when a voltage is applied to the gate through the gate metal (the gate voltage), a “*field effect* takes place in the surface of the semiconductor” which is “either a buildup of charge or a depletion of charges in the wafer surface under the top plate.” (Van Zant, 525 (italics in original).) “Which event occurs depends on the doping conductivity type in the wafer under the gate and the polarity of the gate voltage.” (*Id.*) This “buildup or depletion of charge creates a channel under the gate that connects the source and drain.” (*Id.*) When the gate voltage is raised above a certain threshold, known as the threshold voltage, an inversion channel forms between the source and the drain, electrically connecting them. Then, with a difference in the drain to source voltage, “current starts to flow as the inverted surface creates an electrically connecting channel.” (*Id.*) “Applying more voltage to the gate increases the size of the channel, allowing more current to flow through the channel.” (*Id.*) In an nMOS transistor, “the majority carriers are electrons” and in a pMOS transistor, “the majority carriers are holes.” (Weste, 67.)

2. Threshold Voltage

46. The threshold voltage is the voltage applied at the gate which brings the onset of inversion (formation of the current-carrying channel)—i.e., the “turn-on” voltage of the transistor. (Van Zant, 526.) “Every MOS transistor is designed to operate at a specific threshold voltage.” (Van Zant, 474.) Because PMOS and NMOS transistors are built on different dopant type bodies and feature different types of dopants for their respective source/drain terminals, one would understand that PMOS and NMOS transistors require different polarity gate voltages. For example, NMOS transistors, which use electrons in a p-type body to form the channel between the source and drain terminals, require a **positive** voltage applied to the gate, and therefore will have a **positive** threshold voltage. Conversely, PMOS transistors, which use holes in an n-type body to form the channel between the source and drain terminals, require a **negative** voltage applied to the gate, and therefore will have a **negative** threshold voltage. (*See, e.g.*, Weste, 74, 293-296, 302, Figure 2.3.)

47. Additionally, consumer devices often have transistors of the same conductivity types but with different threshold voltages to cope with various demands on standby power and operation speed. For example, the International Technology Roadmap for Semiconductors (ITRS) acknowledges that “[i]nnovations in circuit design and architecture for performance management, as

well as utilization of multiple transistors on chip, are needed to design chips with both the desired performance and power dissipation. The multiple transistors have different threshold voltages (V_t), with the low V_t , high leakage devices used mainly in the critical paths, and higher V_t , lower leakage devices used in the rest of the chip.” (ITRS, 3-4.) To this end, the ITRS identifies three types of logic that can be used in chips: high performance (HP) logic, low standby power (LSTP) logic, and low operating power (LOP) logic. (ITRS, 5.) Specifically, “[h]igh-performance [HP] logic refers to chips of high complexity, high performance, and high power dissipation, such as microprocessor unit (MPU) chips for desktop PCs, servers, etc. Low-power logic refers to chips for mobile systems, where the allowable power dissipation and hence the allowable leakage currents are limited by battery life.” (*Id.*) Within the low-power spectrum, there are two major categories, the LOP and the LSTP logic. (*Id.*) The transistors in the HP logic (i.e., the HP transistors) have the highest operating speed, the shortest gate length, the thinnest gate oxide, and the lowest V_{th} among the three (e.g., from the LOP and LSTP transistors). (ITRS, 11, 17, 21.) However, HP transistors suffer from high OFF-leakage current (i.e., current flow through the transistor during the OFF state). “The transistors for LOP chips have somewhat lower performance and considerably lower leakage current, while the transistors for LSTP chips have both the lowest performance and the lowest leakage current of all.” (*Id.*, 5) Thus, LSTP transistors are designed for low

performance and low leakage current, and therefore have thicker gate oxides (i.e., larger EOT) and higher V_{th} ; while LOP transistors are between the HP and LSTP transistors in terms of performance, leakage current, and V_{th} . (ITRS, 11, 17, and 21.) As explained by ITRS:

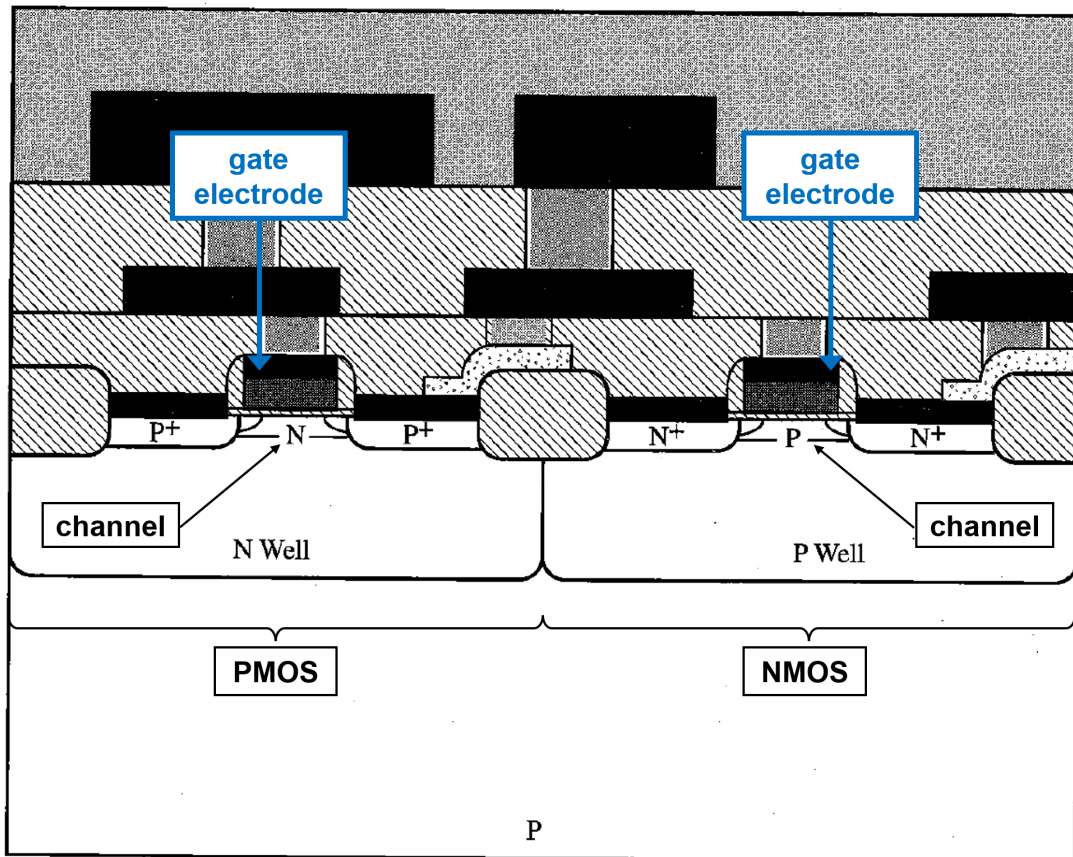
For high-performance chips, the high subthreshold leakage current must be dealt with to keep chip static power dissipation within tolerable limits. One common approach is to fabricate more than one type of transistor on the chip, including the high-performance, low V_t device described above, as well as other MOSFET(s) with higher V_t and sometimes larger EOT to reduce the leakage current. These alternate, lower leakage devices will have lower saturation drive current and hence poorer device performance (i.e., lower MOSFET intrinsic switching frequency, $1/\tau$) than the high-performance devices. The high-performance device is used just in critical paths, and the low leakage devices are used everywhere else. Extensive use of the low leakage devices can significantly reduce the chip static power dissipation without seriously degrading chip performance. ... Hence, a realistic picture of scaled high-performance ICs is that the static power dissipation is controlled by utilizing more than one type of transistor and by utilizing device/design/architectural techniques.

(ITRS, 7.) In other words, as opposed to having different chips for different purposes, modern, scalable, high-performance ICs can be obtained when HP, LOP, and LSTP transistors, as described above, are formed on a single chip to take

advantage of their respective features and to strike a balance between performance and power dissipation.

3. Complementary MOSFETs/MISFETs

48. As discussed above, MISFETs with n-type source/drain regions are referred to as **NMOS**, and MISFETs with p-type source/drain regions are referred to as **PMOS**. (Plummer, 13, Figure 1-11.)



Plummer, Figure 1-11

49. In modern complementary MOS (CMOS) technology, NMOS and PMOS are fabricated and integrated onto the same wafer. (Plummer, 52 (“Modern

CMOS chips integrate millions of active devices (and NMOS and PMOS) side by side in a common silicon substrate.”)) Each NMOS and PMOS transistor is formed over doped wells of opposite conductivity type. “These wells tailor the substrate doping locally to provide optimum device characteristics. The well doping affects device characteristics such as the MOS transistor threshold voltage and the I-V characteristics and PN junction capacitances” (Plummer, 60.) For example, as shown in Figure 1-11 above, PMOS transistors are formed over an n-type well (N-well) and NMOS transistors are formed over a p-type well (P-well). The N and P wells are created in the substrate, which in this case is a p-type substrate, through selective doping (i.e., by selectively masking areas not intended to receive a particular dopant). (*See, e.g.*, Plummer, 60-63.) This arrangement of the CMOS technology enables the creation of high-performance, energy-efficient logic circuits.

4. Complementary MOSFETs/MISFETs With Dual-Gate Electrodes

50. “[D]ual gate structures have become a mainstream in the art in association with increases in accuracy of threshold voltages of n-type MIS transistors and p-type MIS transistors which are accompanied by voltage lowering

in CMIS¹ (Complementary Metal-Insulator-Semiconductor) devices used in large-scale integrated circuits.” (Tamaki, ¶3.)

51. “[A] dual gate structure employs a polysilicon electrode as an n-type gate electrode composing an n-type MIS transistor and a polysilicon electrode as a p-type gate electrode composing a p-type MIS transistor, wherein an n-type impurity is introduced to the n-type gate electrode while a p-type impurity is introduced to the p-type gate electrode.” (Tamaki, ¶4.)

52. Impurities can be deposited on the gate structures using different methods, for example, by “introducing a conductive impurity to an n-type gate electrode or a p-type electrode, the conductive impurity is introduced to a polysilicon film before patterning the polysilicon film.” (Tamaki, ¶5.)

Alternatively, “the conductive impurity is introduced to the n-type gate electrode and the p-type electrode while at the same time being introduced to source/drain regions.” (Tamaki, ¶5; *see also*, Ekbote, ¶4.) “In both cases, thermal treatment is performed after implantation of the conductive impurity for promoting mutual diffusion of an n-type impurity in the n-type gate electrode and a p-type impurity

¹ A “CMIS” (“Complementary Metal-Insulator-Semiconductor”) is also referred to as “CMOS” (“Complementary Metal-**O**xide-Semiconductor”) when the insulator is an oxide.

in the p-type electrode in the integrally-formed n-type and p-type gate electrodes.”
(Tamaki, ¶5.)

a. Logic Circuits With Dual-Gate Electrodes

53. The CMOS inverter is a basic building block used in logic circuits for building logic gates, such as NOR and NAND structures, latches, and flip-flops (Ekbote, ¶5), as well as more complex circuits, such as signal processing circuits, communication circuits, and even, complex microprocessors. (Ekbote, ¶6; *see also*, Ekbote, ¶4 (describing forming a CMOS with dual-gate electrodes where “the gate electrode of the PMOS ... is doped p+, while the gate of the NMOS ... is doped n+,” during their respective source/drain implants.))

b. SRAM Cells With Dual-Gate Electrodes

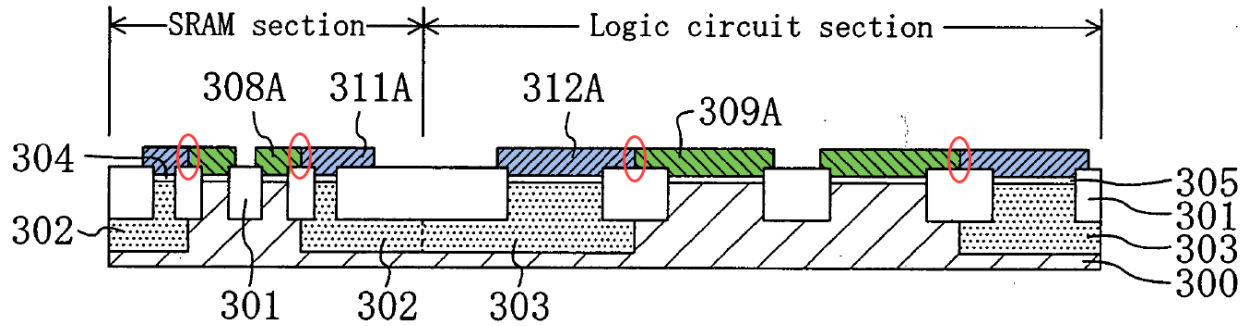
54. Circuit implementations of dual-gate structures are also found in SRAM circuits. Ekbote describes that “[a]nother example of an integrated circuit that includes CMOS inverters is a static ram (SRAM), which generally uses a pair of cross coupled inverters in the bit cells. For example, for integrated circuits that include conventional 5T or 6T SRAM cells, the PMOS load (pull-up) and NMOS driver (pull-down) transistors share a common polysilicon gate.” Ekbote, ¶7.

55. Trends in SRAM design dictate reducing memory cell size to increase the total memory capacity. For example, as Igarashi explains, “[e]specially in recent years, it is in the tendency which also makes bit capacity of SRAM into

large capacity with large-scale-izing of the system mounted in a semiconductor chip. In order to accept the request at the side of such a system, the size of the memory cell which forms SRAM is wanted to be reduced more.” (Igarashi, ¶4.)

56. However, “[i]n order to reduce memory cell size, it is effective to use an MOS transistor with smaller channel width, but by such a pattern with small size, the characteristics variation of a transistor becomes large easily.” (Igarashi, ¶5.) Igarashi explains that “the variation in a transistor increases in inverse proportion to the square root of the product (channel area) of the channel length and channel width of a transistor That is, as a generation progresses like the minimum designed size is 130 nm, 90 nm, 65 nm, that is, as the channel area of the transistor accompanying microfabrication is reduced, the characteristics variation of a transistor will become much more remarkable.” (“Igarashi, ¶7.)

57. The figure below illustrates a conventional semiconductor device with logic circuit and SRAM regions implementing inverters with p-type gate electrodes (shaded blue) and n-type gate electrodes (shaded green). Also annotated in the figure are the pn-boundaries (red ovals) between the p-type gate electrode and the n-type gate electrode.



Tamaki, Figure 7A

5. Voltage Threshold Variations Due to Diffusion Across PN Boundaries

a. Dopant diffusion across PN boundaries

58. At the pn-boundary of a dual-gate electrode in, p-type dopants diffuse into the n^+ polysilicon gate electrode, while n-type dopants diffuse into the p^+ polysilicon gate electrode. (See Igarashi, ¶89 (“the phenomenon in which the P type impurity and N type impurity which were implanted into the gate do mutual diffusion in PN boundary part in the polysilicon gate mentioned above since various heat treatment was applied occurs.”), *see also*, Tamaki, ¶22.)

59. Igarashi explains that this mutual diffusion of gate dopants and the formation of a depletion region at the gate electrode results in threshold voltage variations that are considered undesirable. (Igarashi, ¶90.)

B. Applicant Admitted Prior Art (“AAPA”)

60. As discussed above, semiconductor devices, such as MISFETs and Complementary MISFETs, existed for decades prior to the filing of the ’373

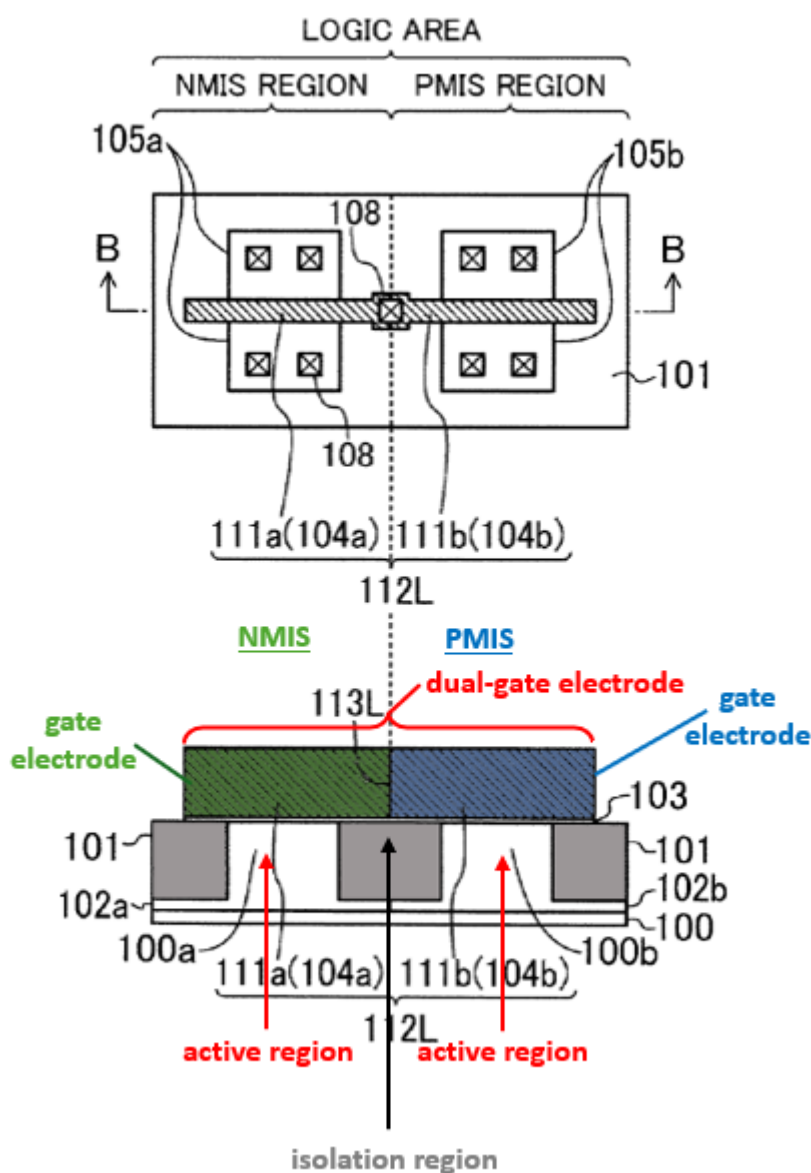
patent. The '373 patent does not purport to invent the limitations of most of its claims, including, for example:

- a first dual-gate electrode that includes (i) a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and (ii) a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,
- a second dual-gate electrode being separated from the first dual-gate electrode that includes (i) a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and (ii) a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,
- where the first active region and the second active region are isolated from each other with an isolation region interposed therebetween, and
- where the first gate electrode and the second gate electrode are connected to each other on the isolation region.

61. Rather, the '373 patent claims are directed to specific arrangements of impurity concentrations for the first conductivity type (which, as I will explain later in relation to the prior art grounds, were also well known). For example, the '373 patent recognized that semiconductor devices such as “[a] CMIS device with a dual-gate structure ... including a polysilicon film doped with an n-type impurity as a gate electrode of an n-channel [MISFET]... and also including a

polysilicon film doped with a p-type impurity as a gate electrode of a p-channel MISFET” already existed prior to its filing in 2012. (TSMC-1001, 1:23-29.)

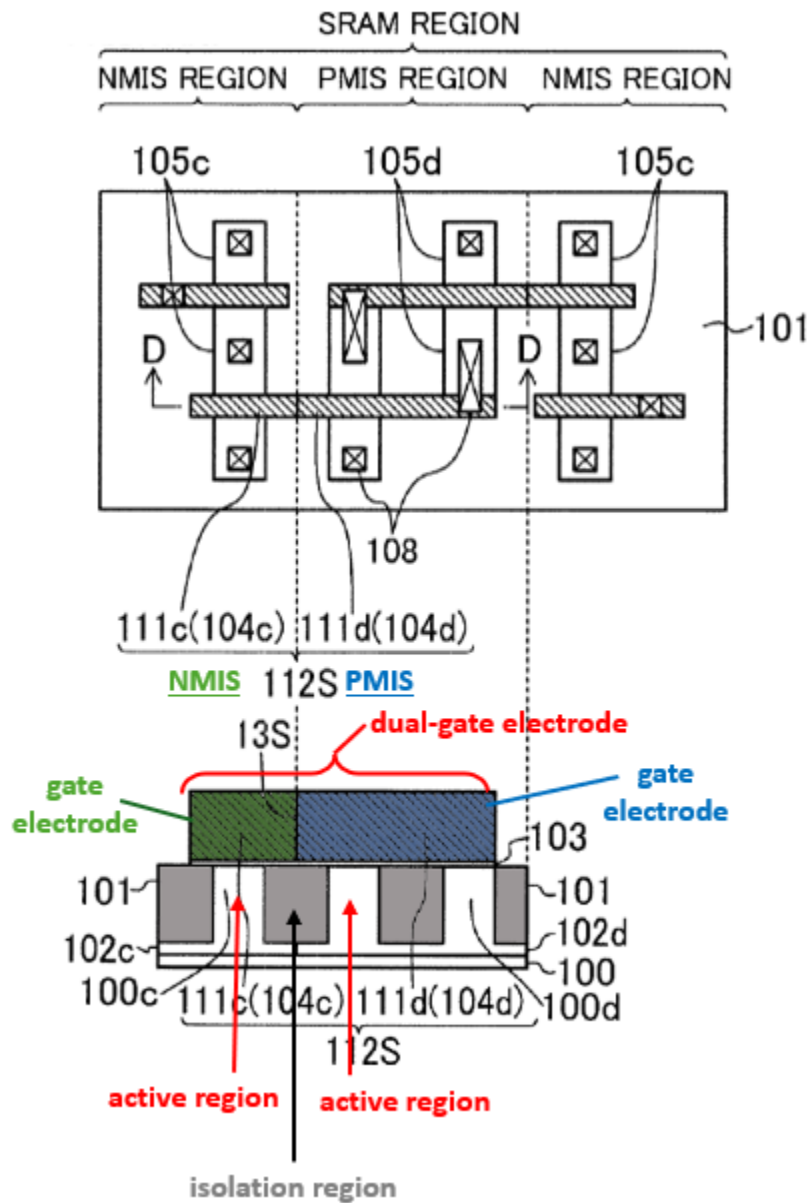
62. The background of the '373 patent describes a “conventional semiconductor device in which an n-type region and a p-type region are formed by implanting ions into gate electrodes of a transistor for a logic circuit and a transistor for a static random-access memory (SRAM) circuit.” (TSMC-1001, 1:48-52.) As shown in Figures 15A and 15B (below), the logic area includes an NMIS region and a PMIS region. Dual-gate electrode 112L in the logic area includes gate electrode 111a with an n-type polysilicon film 104a (green) on active region 100a (NMIS region) and gate electrode 111b with a p-type polysilicon film 104b (blue) on active region 100b (PMIS region). (TSMC-1001, 2:11-16.) Gate electrode 111a and gate electrode 111b “are connected to each other at a PN boundary 113L” between active region 100a and active region 100b on the isolation region 101 (gray). (TSMC-1001, 2:16-20.)



'373 Patent, Figures 15A (top), 15B (bottom): AAPA

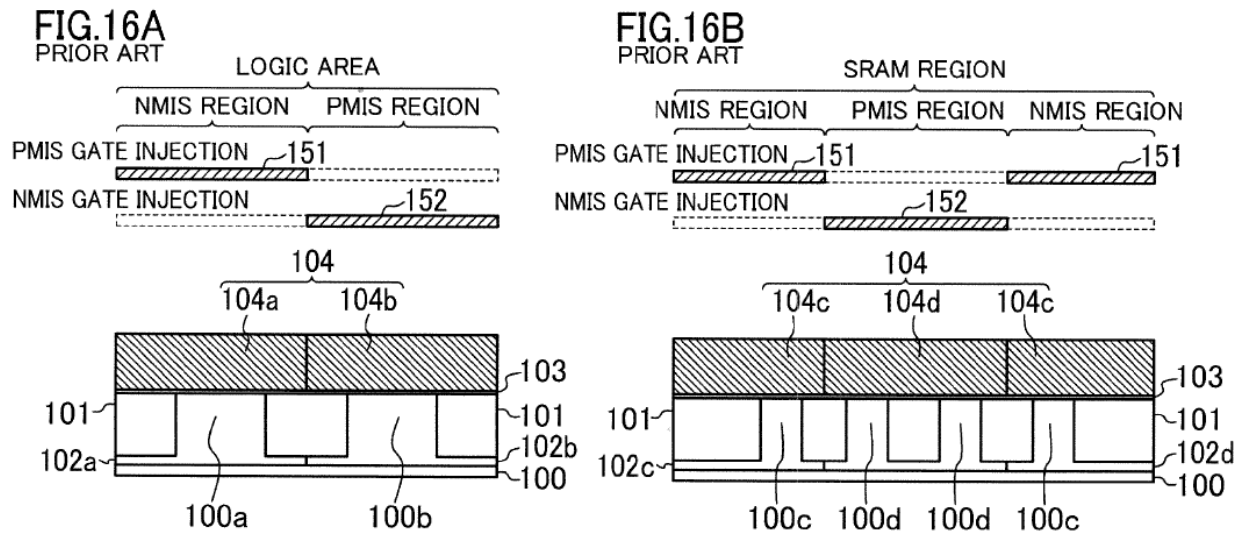
63. As shown in Figures 15C and 15D (below), dual-gate electrode 112S in the SRAM region includes gate electrode 111c with n-type polysilicon film 104c (green) on active region 100c (NMIS region) and gate electrode 111d with p-type polysilicon film 104d (blue) on active region 100d (PMIS region). (TSMC-1001,

2:27-36.) Gate electrode 111c and gate electrode 111d “are connected to each other at a PN boundary [113S]” between active region 100c and active region 100d on the isolation region 101 (gray). (TSMC-1001, 2:32-35.)



'373 Patent, Figures 15C (top), 15D (bottom): AAPA

64. As shown in Figures 16A and 16B (below), in the conventional CMIS dual-gate structure, during the PMIS gate injection, “ions of a p-type impurity are implanted into the polysilicon film 104 using a mask pattern 151 covering the NMIS region in each of the logic area and the SRAM area, thereby forming p- type polysilicon films 104*b* and 104*d*.” (TSMC-1001, 2:50-53.) Consequently, “the p-type polysilicon films 104*b* and 104*d* have substantially the same concentration of the p-type impurity.” (TSMC-1001, 2:54-55.) Similarly, during the NMIS gate injection, “ions of an n-type impurity are implanted into the polysilicon film 104 using a mask pattern 152 covering the PMIS region of each of the logic area and the SRAM area, thereby forming n- type polysilicon films 104*a* and 104*c*.” (TSMC-1001, 2:56-60.) As a result, “the n-type polysilicon films 104*a* and 104*c* have substantially the same concentration of the n-type impurity.” (TSMC-1001, 2:60-62.)



'373 Patent, Figures 16A, 16B: AAPA

C. '373 Patent Overview

65. The '373 patent identifies an alleged problem in prior art "CMIS device[s] with a dual-gate structure [like the admitted CMIS dual-gate structures shown in Figures 16A and 16B], [where] a metal silicide layer is formed on a polysilicon gate electrode in order to connect an n-type polysilicon gate electrode and a p-type polysilicon gate electrode." (TSMC-1001, 1:31-34.) As the '373 patent notes, "[i]n this structure, in the boundary between an n-type region and a p-type region in each of the polysilicon gate electrode, impurities in these regions are diffused from one region to the other through the metal silicide layer or the polysilicon film, **resulting in a change in work function of the gate electrode, and thus, a variation in threshold voltage** of each of the FETs." (TSMC-1001, 1:34-40.) The '373 patent purports to solve this problem by varying the doping,

i.e., impurity concentration, of the gate electrodes of the N-MISFETs and P-MISFETs in the Logic and SRAM areas.

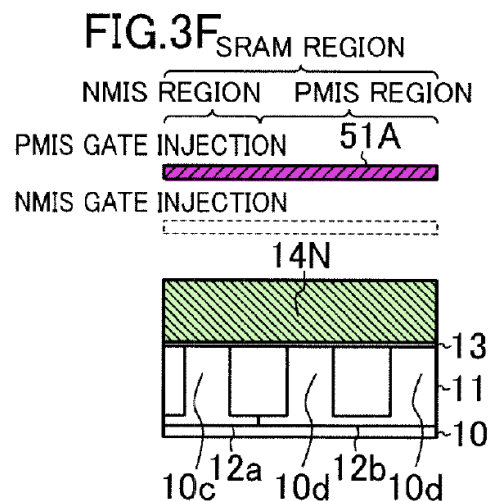
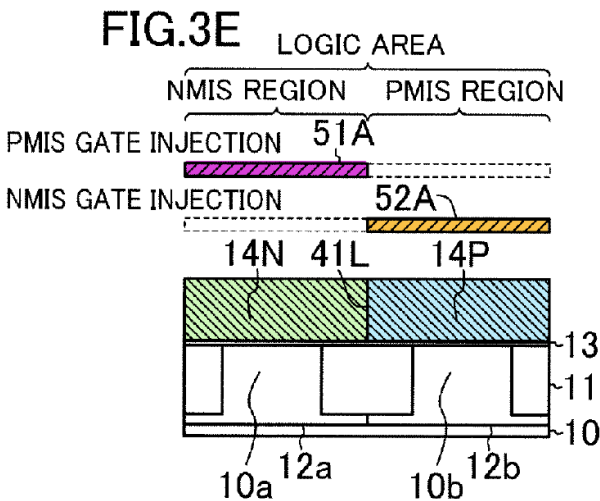
66. Specifically, the '373 patent specification discloses four exemplary embodiments with different arrangements of the impurity concentrations of the gate electrodes of the N-MISFETs and P-MISFETs in the Logic and SRAM areas. The first embodiment is illustrated in Figures 1A-1D through Figures 8A-8F and associated discussion at TSMC-1001, 7:47-14:51. The second embodiment is illustrated in Figures 9A-9D through Figures 10A-10F and associated discussion at TSMC-1001, 14:53-18:35. The third embodiment is illustrated in Figures 11A-11D through Figures 12A-12F and associated discussion at TSMC-1001, 18:37-22:14. The fourth embodiment is illustrated in Figures 13A-13D through Figures 14A-14F and associated discussion at TSMC-1001, 22:16-24:55.

1. First Embodiment

67. I provide below an overview of some of the fabrication steps disclosed in the first embodiment. During fabrication of the N-MISFETs and P-MISFETs of the Logic and SRAM areas, “a silicon film 14 ... is deposited ... over the gate insulating film 13.” (TSMC-1001, 9:55-58, Figures 3A-F.) “Then, as illustrated in [Figures 3E and 3F below], with a mask pattern 51A [purple] covering the entire NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area) and

exposing the entire PMIS region in the logic area, ions of a p-type impurity such as boron (B) are implanted into the silicon film 14 ..., thereby forming a p-type silicon film 14P [light blue].” (TSMC-1001, 9:59-65.)

68. The '373 patent Specification describes that “[t]hereafter, with a mask pattern 52A [orange] covering the entire PMIS region in the logic area and exposing the entire NMIS region in the logic area and the entire SRAM area (i.e., the entire NMIS region and the entire PMIS region in the SRAM area), ions of an n-type impurity such as phosphorus (P) are implanted into the silicon film 14 ..., thereby forming an n-type silicon film 14N [light green].” (TSMC-1001, 9:66-10:5.)



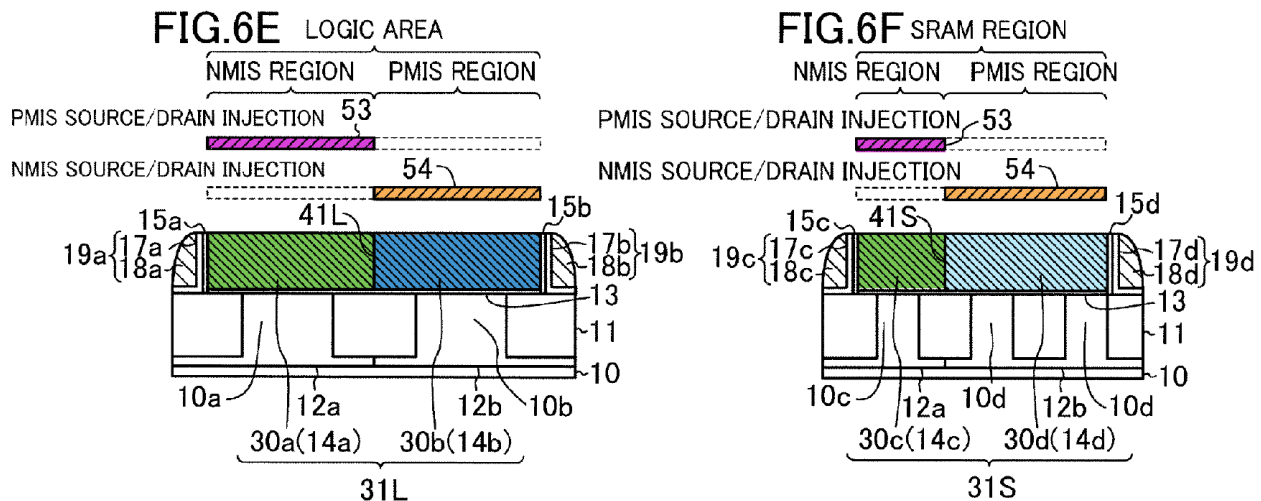
'373 Patent, Figure 3E (left) and Figure 3F (right) (annotated)

69. As can be seen in the figures above and the corresponding disclosure, at this process step “as a feature of this embodiment, ions of the n-type impurity

are implanted in the gate injection for the PMIS region in the SRAM area.”

(TSMC-1001, 10:5-8.)

70. In a subsequent step, “as illustrated in [Figures 6E and 6F below], using a mask pattern 53 [purple] covering the entire NMIS region in the logic area and the entire NMIS region in the SRAM area, the gate electrode 30b ... and the gate electrode 30d ... ions of a p-type impurity such as boron (B) are implanted...” (TSMC-1001, 11:55-62.) Specifically, “[i]n this process step, the p-type impurity is ... implanted into the p-type silicon film 14b forming the gate electrode 30b [dark blue] and the n-type silicon film 14d’ forming the gate electrode 30d [light blue], thereby increasing the p-type impurity concentration of the p-type silicon film 14b and changing the n-type silicon film 14d’ into the p-type silicon film 14d.” (TSMC-1001, 12:6-11.)



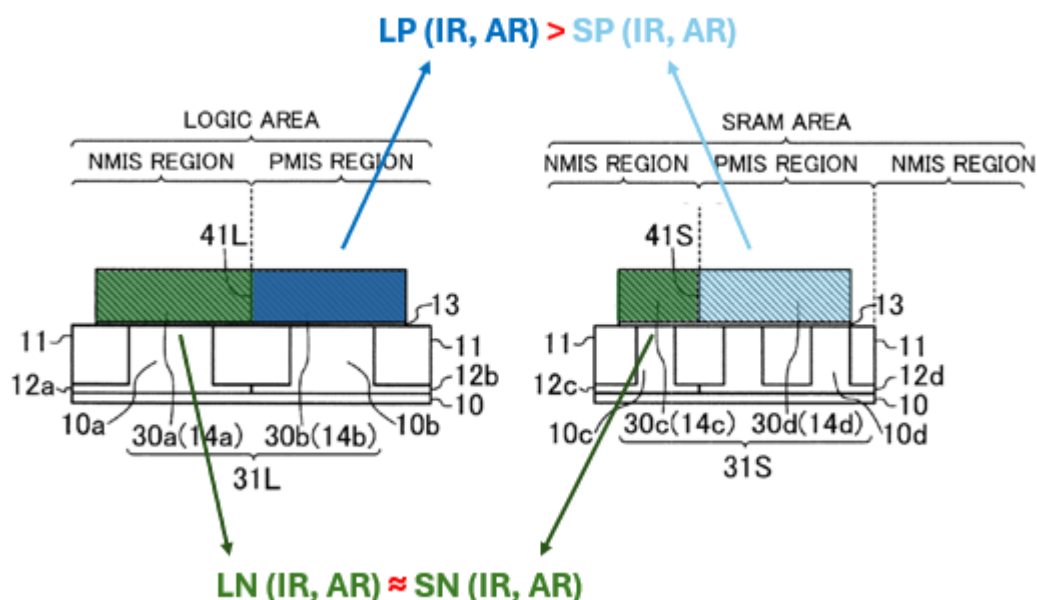
'373 Patent, Figure 6E (left) and Figure 6F (right) (annotated)

71. Therefore, as shown above in Figure 6F, “a PN boundary 41S between the n-type silicon film 14c (the gate electrode 30c [green]) and the p-type silicon film [] 14d (the gate electrode 30d [light blue]) is formed in the dual-gate electrode 31S. At this time, the p-type impurity concentration of the p-type silicon film 14b is higher than that of the p-type silicon film 14d.” (TSMC-1001, 12:12-17.)

72. In a next step, as shown above in Figures 6E and 6F, “using a mask pattern 54 [orange] covering the entire PMIS region in the logic area and the entire PMIS region in the SRAM area, the gate electrode 30a [dark green], ... and the gate electrode 30c [dark green], ions of an n-type impurity such as arsenic (As) are implanted ...” (TSMC-1001, 12:18-25.)

73. In summary, the “p-type impurity concentration in the entire p-type silicon film 14b [dark blue] is higher than that in the entire p-type silicon film 14d [light blue].” (TSMC-1001, 8:47-49.) The “n-type impurity concentration of the n-type silicon film 14a [dark green] is substantially equal to that of the n-type silicon film 14c [dark green].” (TSMC-1001, 8:50-52.) The relationship above can be expressed using the following shorthand notation:

LP (IR, AR) > SP (IR, AR)	LN (IR, AR) $\approx$ SN (IR, AR)
LP: Logic-PMIS gate electrode (IR, AR): IR or AR LP (IR, AR): Portion of logic-PMIS gate electrode over isolation region (IR) or portion over active region (AR) SP: SRAM-PMIS gate electrode SP (IR, AR): Portion of SRAM-PMIS gate electrode over IR or portion over AR	LN: Logic-NMIS gate electrode LN (IR, AR): Portion of logic-NMIS gate electrode over IR or portion over AR SN: SRAM-NMIS gate electrode SN (IR, AR): Portion of SRAM-NMIS gate electrode over IR or portion over AR
> : higher than (impurity concentration) $\approx$: substantially equal to (impurity concentration)	



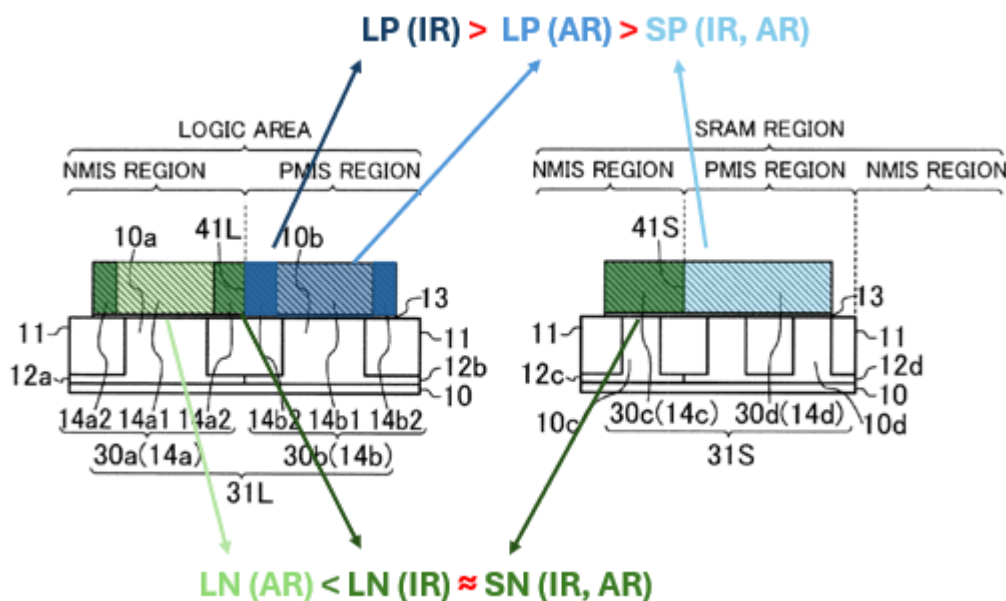
'373 Patent, Figures 1B(left), 1D(right)

2. Second Embodiment

74. In the second embodiment, the “p-type silicon film 14b1 [on active region; blue] has a p-type impurity concentration lower than that of the p-type silicon film 14b2 [on shallow trench isolation (STI); dark blue]” and “each of the p-type silicon film 14b1 and the p-type silicon film 14b2 has a p-type impurity concentration higher than that of the p-type silicon film 14d [light blue].” (TSMC-1001, 15:28-33.)

75. The “n-type silicon film 14a1 [on active region; light green] has an n-type impurity concentration lower than that of each of the n-type silicon film 14a2 [on STI; dark green] and the n-type silicon film 14c” and “n-type silicon film 14a2 has an n-type impurity concentration substantially equal to that of the n-type silicon film 14c.” (TSMC-1001, 15:33-37.) The relationship above can be expressed using the following shorthand notation:

$\begin{aligned} & \text{LP (AR)} < \text{LP (IR)} \\ & + \\ & \text{LP (AR)} > \text{SP (IR, AR)} \\ & \text{LP (IR)} > \text{SP (IR, AR)} \end{aligned}$ that is: $\text{SP (IR, AR)} < \text{LP (AR)} < \text{LP (IR)}$	$\begin{aligned} & \text{LN (AR)} < \text{LN (IR)} \\ & \text{LN (AR)} < \text{SN (IR, AR)} \\ & + \\ & \text{LN (IR)} \approx \text{SN (IR, AR)} \end{aligned}$ that is: $\text{LN (AR)} < \text{LN (IR)} \approx \text{SN (IR, AR)}$
LP (AR): Portion of logic-PMIS gate electrode over AR LP (IR): Portion of logic-PMIS gate electrode over IR SP (IR, AR): Portion of SRAM-PMIS gate electrode over IR or portion over AR	LN(AR): Portion of logic-NMIS gate electrode over AR LN (IR): Portion of logic-NMIS gate electrode over IR SN (IR, AR): Portion of SRAM-NMIS gate electrode over IR or portion over AR
< : lower than (impurity concentration) > : higher than (impurity concentration) ≈ : substantially equal to (impurity concentration)	

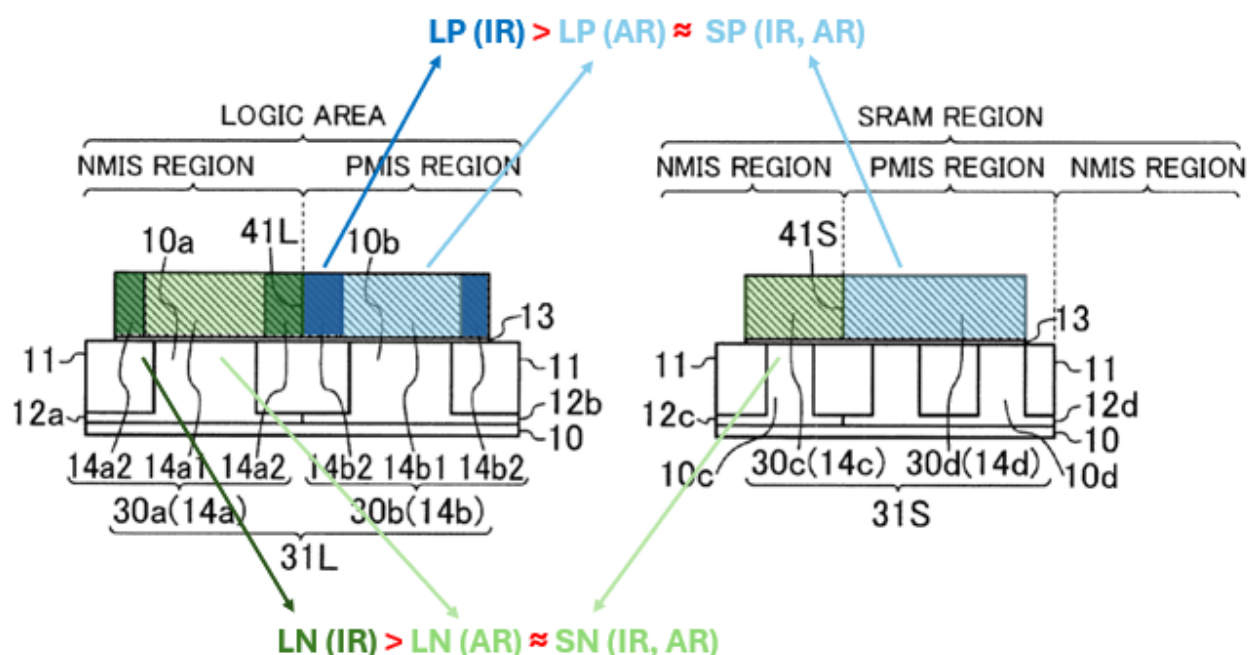


'373 Patent, Figures 9B(left), 9D(right)

3. Third Embodiment

76. In the third embodiment, the “p-type silicon film 14b2 [on STI; dark blue] has a p-type impurity concentration higher than that of the p-type silicon film 14d and that the p-type silicon film 14b1 [on active; light blue] has a p-type impurity concentration substantially equal to that of the p-type silicon film 14d.” (TSMC-1001, 19:16-22.) The “n-type silicon film 14a1 [on active region; light green] has an n-type impurity concentration substantially equal to that of the n-type silicon film 14c” and “n-type silicon film 14a1 has an n-type impurity concentration lower than that of the n-type silicon film 14a2 [on STI; dark green].” (TSMC-1001, 19:22-26.) The relationship above can be expressed using the following shorthand notation:

$\text{LP (IR)} > \text{SP (IR, AR)}$ $+$ $\text{LP (AR)} \approx \text{SP (IR, AR)}$ <u>that is:</u> $\text{LP (IR)} > \text{LP (AR)} \approx \text{SP (IR, AR)}$	$\text{LN (AR)} \approx \text{SN (IR, AR)}$ $+$ $\text{LN (AR)} < \text{LN (IR)}$ <u>that is:</u> $\text{LN (IR)} > \text{LN (AR)} \approx \text{SN (IR, AR)}$
LP (AR): Portion of Logic-PMIS gate electrode over AR LP (IR): Portion of Logic-PMIS gate electrode over IR SP (IR, AR): Portion of SRAM-PMIS gate electrode over IR or portion over AR	LN(AR): Portion of Logic-NMIS gate electrode over AR LN (IR): Portion of Logic-NMIS gate electrode over IR SN (IR, AR): Portion of SRAM-NMIS gate electrode over IR or portion over AR
< : lower than (impurity concentration) > : higher than (impurity concentration) ≈ : substantially equal to (impurity concentration)	

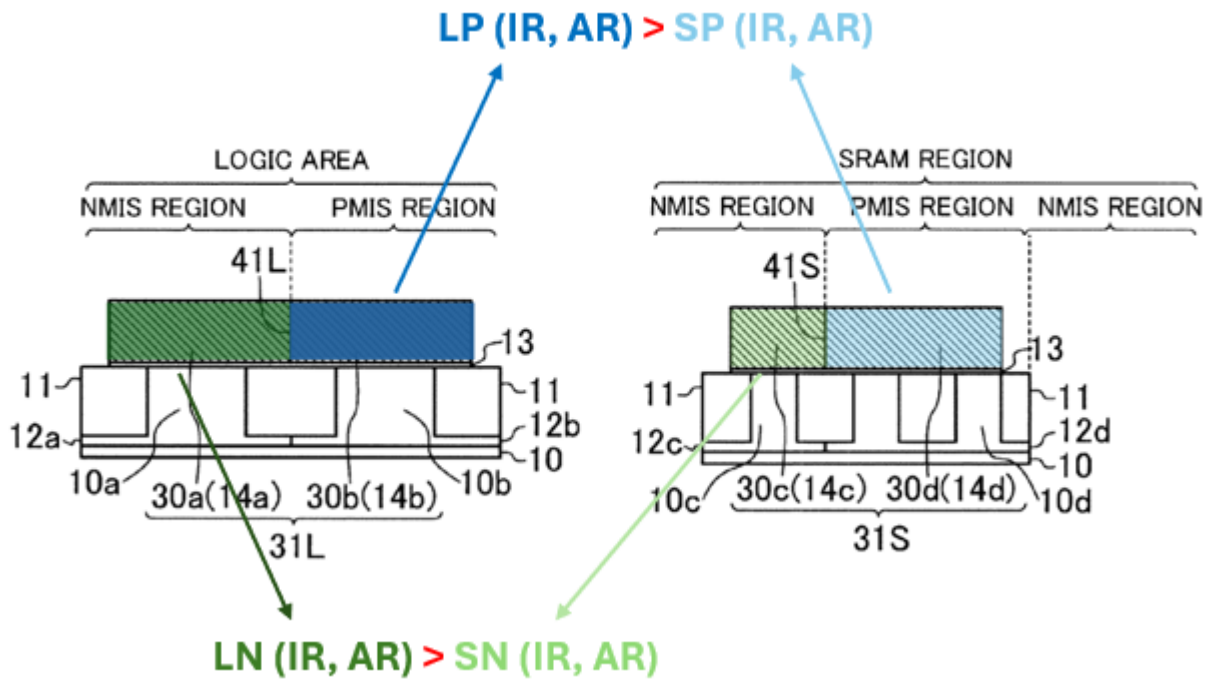


'373 Patent, Figures 11B(left), 11D(right)

4. Fourth Embodiment

77. In the fourth embodiment, the “p-type silicon film 14b [blue] has a p-type impurity concentration higher than that of the p-type silicon film 14d [light blue]” and “the n-type silicon film 14a [green] has an n-type impurity concentration higher than that of the n-type silicon film 14c [light green].” (TSMC-1001, 22:57-61.) The relationship above can be expressed using the following shorthand notation:

LP (IR, AR) > SP (IR, AR)	LN (IR, AR) > SN (IR, AR)
LP (IR, AR): Portion of Logic-PMIS gate electrode over IR or portion over AR SP (IR, AR): Portion of SRAM-PMIS gate electrode over IR or portion over AR	LN (IR, AR): Portion of Logic-NMIS gate electrode over IR or portion over AR SN (IR, AR): Portion of SRAM-NMIS gate electrode over IR or portion over AR
> : higher than (impurity concentration) ≈ : substantially equal to (impurity concentration)	



'373 Patent, Figures 13B(left), 13D(right)

D. '373 Patent Claims

78. Claim 1, the sole independent claim, recites “a *first dual-gate electrode*” and “a *second dual-gate electrode*” but does not limit either to use in a specific type of transistor (e.g., logic or SRAM). Therefore, the independent claim covers the following:

	1	2
“ <i>first dual-gate electrode</i> ”	Logic	SRAM
“ <i>second dual-gate electrode</i> ”	SRAM	Logic

79. The independent claim further recites that the “*first dual-gate electrode*” includes a “*first/third gate electrode*” each having a “*silicon film*” of a “***first conductivity type***” and the “*second dual-gate electrode*” includes a “*second/fourth gate electrode*” each having a “*silicon film*” of a “***second conductivity type***.” However, the claim does not limit “*conductivity type*” to use of a specific type (e.g., n-type or p-type). Therefore, the claim also covers the following:

- A:** first conductivity type = **n-type**
second conductivity type = **p-type**
- B:** first conductivity type = **p-type**
second conductivity type = **n-type**

80. Accordingly, the independent claims encompass at least the following four scenarios²:

Claim Language		Scenarios Covered			
		A-1	A-2	B-1	B-2
<i>first dual-gate electrode</i>	<i>first gate electrode</i>	logic NMOS	SRAM NMOS	logic PMOS	SRAM PMOS
	<i>second gate electrode</i>	logic PMOS	SRAM PMOS	logic NMOS	SRAM NMOS
<i>second dual-gate electrode</i>	<i>third gate electrode</i>	SRAM NMOS	logic NMOS	SRAM PMOS	logic PMOS
	<i>fourth gate electrode</i>	SRAM PMOS	logic PMOS	SRAM NMOS	logic NMOS

81. The '373 patent merely modifies the admitted CMIS dual-gate structure by varying the doping concentrations of the PMIS and NMIS gate electrodes of the logic and SRAM sections.

82. Independent claim 1 recites:

[1P]	1. A semiconductor device, comprising:
[1A]	a first dual-gate electrode; and

² Claim 13 encompasses only Scenarios A-2 and B-2 and claim 14 encompasses only Scenarios A-1 and A-2.

[1B]	a second dual-gate electrode being separated from the first dual-gate electrode, wherein
[1C]	the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,
[1D]	the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,
[1E]	the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,
[1F]	the first gate electrode and the second gate electrode are connected to each other on the isolation region, and
[1G]	at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

83. As shown in the table, with regard to impurity concentration, independent claim 1 recites “*at least a portion of the **first silicon film** of the first conductivity type has a first-conductivity-type impurity concentration **higher than***

*that of a portion of the **second silicon film** of the first conductivity type located on the third active region” [1G].*

84. Dependent claims 3-12 narrow claim 1 by layering on additional impurity concentration requirements. For ease of discussion, I provide in Appendix B illustrations depicting the concentrations recited in these claims using the common CMIS dual-gate structure of each embodiment.

E. Prosecution History

1. U.S. Prosecution of the '373 Patent

85. The filed claims of the '373 patent application were rejected as unpatentable over Japanese Application Publication No. 2010-067912 to Shimomura et al. (“Shimomura”) in view of U.S. Patent Publication No. 2008/0036010 to Tamaki et al. (“Tamaki”). (TSMC-1002, 206-207.) In response, Applicant amended the claims as shown below and argued (1) that the Examiner had incorrectly failed to address the last limitation of claim 1 (TSMC-1002, 244) and (2) that “Shimomura only discloses one dual-gate electrode, and therefore, at a minimum, fails to disclose or suggest a second dual-gate electrode being separated from the first dual-gate electrode, as recited by claim 1.” (TSMC-1002, 245 (emphasis in original).)

1. (Currently amended) A semiconductor device, comprising:

a first dual-gate electrode; and

a second dual-gate electrode being separated from the first dual-gate electrode, wherein

the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,

the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,

the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,

the first gate electrode and the second gate electrode are connected to each other on the isolation region, and

at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

TSMC-1002, 239

86. Applicant mischaracterized both the claim language and Tamaki's teachings, which explicitly teach a first dual-gate electrode that is separated from a second dual-gate electrode. Relying on Applicant's representations, the Examiner overlooked Tamaki's relevant disclosure and subsequently allowed the claims. (TSMC-1002, 257-258.) However, as I will explain later in relation to the prior art grounds, separated dual-gate electrodes were well-known in the art—as also

evidenced by AAPA—as well as silicon films of separated dual-gate electrodes with different impurity concentrations of the same conductivity types.

2. Prosecution of Japanese Counterpart Application

87. I have also reviewed a translated version of the prosecution history for the Japanese patent that is counterpart to the '373 patent. Specifically, Japanese Patent No. 5857225, which was filed as Japanese application No. 2012-530800 (the “JP '800 application”), is a national entry phase of the '167 PCT application, which is the parent of the '373 patent.

88. The JP '800 application was filed with the same claims originally filed with the U.S. application. (*Compare* TSMC-1005, 15-17, *with* TSMC-1002, 103-107.) On April 6, 2015 (after the '373 Patent issued on November 11, 2014), the Japanese Examiner found that, among others, independent claim 1 and dependent claim 2 lacked novelty and inventive step over Japanese Application Publication No. 2008-042092. (TSMC-1005, 9-11.) The Japanese Examiner, however, did not reject claim 3—which depended on claim 2—as lacking novelty and inventive step. In their response, Applicant did not dispute the Examiner’s findings that claims 1 and 2 were unpatentable over Japanese Application Publication No. 2008-042092. Rather, to overcome the novelty and inventive step rejections, Applicant incorporated the limitations of claims 2 and 3 into independent claim 1. (TSMC-1005, 15-17, 20-21, 25-27.)

89. Interestingly, Japanese Application Publication No. 2008-042092 is the Japanese counterpart to US 2008/0036010 to Tamaki, which was used by the US Examiner as a secondary reference to reject the originally filed claims of the '373 Patent.

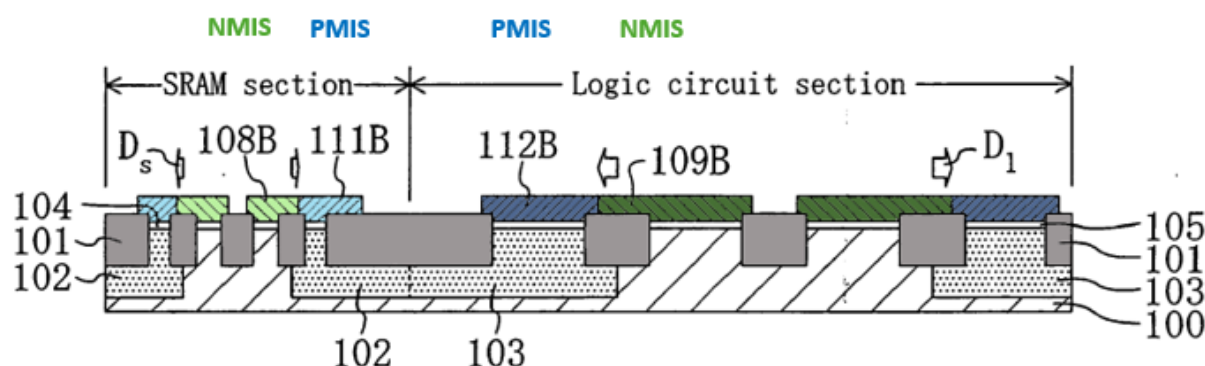
90. In my opinion, the US Examiner did not appreciate the full disclosures of Tamaki, during examination of the '373 Patent. As I explain in Ground 1 below, consistent with the findings of the Japanese Examiner, Tamaki renders claims 1-4, 8-9, and 11-14 obvious.

V. GROUND 1: Tamaki Renders Claims 1-4, 8-9, and 11-14 Obvious.

A. Overview of Tamaki

91. Tamaki “relates to a semiconductor device including a SRAM section and a logic circuit section.” (Tamaki, ¶2.) Specifically, Tamaki discloses two embodiments of a semiconductor device, each embodiment featuring CMIS dual-gate electrode structures in an SRAM section and a logic circuit section of the semiconductor device similar to the conventional structure described in the '373 patent. The primary distinction between the two embodiments lies in the impurity concentrations of the NMIS and PMIS gate electrodes in the SRAM and logic sections, as a result of impurity implantations of different implantation energies and impurity dosages.

92. In the first embodiment illustrated in Figure 3B (below), Tamaki discloses an “n-type impurity implantation ... with respect to the logic circuit section n-type gate electrode formation film 109 [dark green] is performed under the conditions of, for example, **an implantation energy of 10 keV and a dosage of 8×10^{15} atoms/cm²**” (Tamaki, ¶85), a “p-type impurity implantation ... with respect to the logic circuit section p-type gate electrode formation film 112 [dark blue] is performed under the conditions of, for example, **an implantation energy of 5 keV and a dosage of 3×10^{15} atoms/cm²**” (Tamaki, ¶86), an “n-type impurity implantation ... with respect to the SRAM section n-type gate electrode formation film 108 [light green] is performed under the conditions of, for example, **an implantation energy of 10 keV and a dosage of 4×10^{15} at[o]ms/cm²**” (Tamaki, ¶87), and a “p-type impurity implantation ... with respect to the SRAM section p-type gate electrode formation film 111 [light blue] is performed under the conditions of, for example, **an implantation energy of 5 keV and a dosage of 2×10^{15} at[o]ms/cm²**.” (Tamaki, ¶88.)

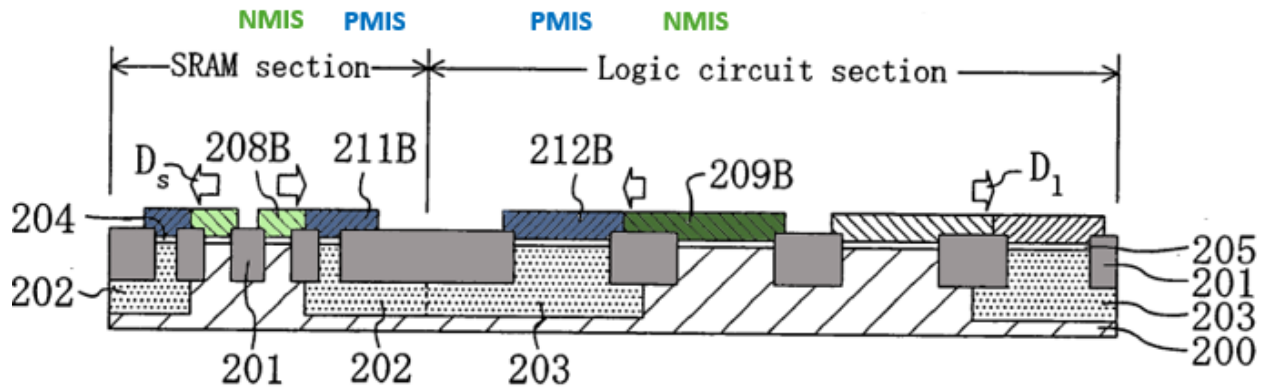


Tamaki, Figure 3B (First Embodiment)

93. In the first embodiment, the n-type dopant implantation is carried out at the same energy (10keV) at the gate electrodes of the SRAM NMIS and the logic NMIS. Because the n-type dopant dosage of the entire gate electrode of the logic NMIS is higher than that of the entire gate electrode of SRAM NMIS (8×10^{15} atoms/cm² v. 4×10^{15} atoms/cm²), the resulting impurity concentration in the gate electrode of the logic NMIS is greater than the resulting impurity concentration in the gate electrode of the SRAM NMIS.

94. Similarly, the p-type dopant implantation is carried out at the same energy (5keV) at the gate electrodes of the SRAM PMIS and the logic PMIS. Because the n-type dopant dosage of the entire gate electrode of the logic PMIS is higher than that of the entire gate electrode of SRAM PMIS (3×10^{15} atoms/cm² v. 2×10^{15} atoms/cm²), the resulting impurity concentration in the gate electrode of the logic PMIS is greater than the resulting impurity concentration in the gate electrode of the SRAM PMIS.

95. In the second embodiment illustrated in Figure 5B (below), Tamaki discloses an “n-type impurity implantation (first n-type impurity implantation) with respect to the SRAM section n-type gate electrode formation film 208 [light green] and the n-type impurity implantation (second n-type impurity implantation) with respect to the logic circuit section n-type gate electrode formation film 209 [dark green] are performed under the conditions of, for example, **an implantation energy of 10 keV and a dosage of 8×10^{15} atoms/cm²**” (Tamaki, ¶118) and a “p-type impurity implantation (third p-type impurity implantation) with respect to the SRAM section p-type gate electrode film 211 [dark blue] and the p-type impurity implantation (fourth p-type impurity implantation) with respect to the logic circuit section p-type gate electrode formation film 212 [dark blue] are performed under the conditions of, for example, **an implantation energy of 5 keV and dosage of 3×10^{15} at[oms]/cm²**” (Tamaki, ¶119) and that “the first n-type impurity is **implanted to only a part of the gate electrode formation film 206 on the n-type MIS formation region in the SRAM** section in the step shown in FIG. 4B so that an undoped SRAM section gate electrode formation film 206 *a* intervenes between the SRAM section p-type gate electrode formation film 211 and the SRAM section n-type gate electrode formation film 208 [light green]...” (Tamaki, ¶120.)



Tamaki, Figure 5B (Second Embodiment)

96. In the second embodiment, the p-type dopant implantation conditions are the same for the entire gate electrode of the logic PMIS and the entire gate electrode of the SRAM PMIS, the resulting impurity concentrations in both gate electrodes are the same. However, for the n-type impurity concentration, Tamaki discloses that the “SRAM section n-type gate electrode 208B has phosphorous concentration lower than the logic circuit section n-type gate electrode 209B” (Tamaki, ¶138.)

97. As I discussed in §IV.E.1, during examination of the '373 Patent, the Examiner rejected the pending claims over the combination of Shimomura and Tamaki. Specifically, the Examiner found that Tamaki discloses a gate electrode having a silicon film of a first conductivity type and a silicon film of a second conductivity type. (*See*, TSMC-1002, 208.)

98. However, the Examiner failed to consider Tamaki in connection with limitation [1G]: “at least a portion of the first silicon film of the first conductivity

type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region,” because, according to the Examiner, “[t]his limitation will not be examined since it is pertaining to a forth [sic] embodiment, which is Species III.” (TSMC-1002, 207-208.)

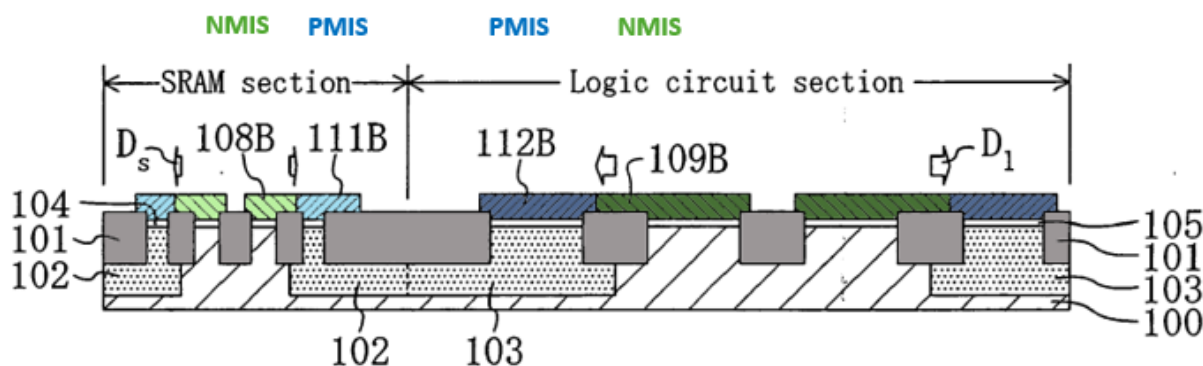
99. But even after the restriction requirement was withdrawn (TSMC-1002, 256), the Examiner did not appear to consider Tamaki in connection with limitation [1G]. Instead, the Examiner relied on Applicant’s Remarks and stated that “Aplicant’s arguments with respect to claims 1-7, 9, 11, 13, & 15-16 have been considered and are persuasive.” (TSMC-1002, 258.) However, Applicant’s sole statement about Tamaki was that “[t]urning to Tamaki, as this reference also fails to disclose or suggest a device **including two dual-gate electrodes that are separated from each other and independent of each other**, at a minimum, Tamaki does not cure the foregoing deficiencies of Shimomura, nor is it relied upon doing so.” (TSMC-1002, 246.) When considering Applicant’s statement, the Examiner further failed to appreciate (i) that Tamaki indeed discloses two dual-gate electrodes that are separated, since a first dual-gate electrode is in the logic section and a second dual-gate electrode is in the SRAM section (*see*, Tamaki, Figures 3A-3B, 5A-5B) and (ii) Applicant’s statement introduced a requirement,

i.e., that the two dual-gate electrodes be “independent,” which is not a claim limitation.

100. But Tamaki discloses and/or at least renders obvious claims 1-4, 8-9, and 11-14, as I discuss below. Specifically, Tamaki’s first embodiment discloses claims 1-2, 4, 8-9, 12, 14 under Scenario A-1 (first conductivity type = **n-type**; second conductivity type = **p-type**), as I discuss in §V.B.3. Tamaki’s first embodiment also discloses claims 1-2, 4, 8-9, 12-14 under Scenario B-1 (first conductivity type = **p-type**; second conductivity type = **n-type**), as I discuss in §V.B.4. Tamaki’s second embodiment discloses claims 1-4, 8-9, 11, and 14 under Scenario A-1 (first conductivity type = **n-type**; second conductivity type = **p-type**), as I discuss in §V.C.

B. Tamaki’s First Embodiment

101. Tamaki’s first embodiment device includes a logic circuit section and SRAM section as shown in Figure 3B (below). The logic section includes p-type gate electrode 112B (dark blue) and n-type gate electrode 109B (dark green). (Tamaki, ¶103.) The SRAM section includes n-type gate electrode 108B (light green) and p-type gate electrode 111B (light blue). (Tamaki, ¶103, Figure 3B (below).)



Tamaki, Figure 3B (First Embodiment)

1. P-type Impurity Concentrations

102. Tamaki discloses that “[t]he p-type impurity implantation (fourth p-type impurity implantation) **with respect to the logic circuit section p-type gate electrode formation film 112** is performed under the conditions of, for example, an implantation energy of **5 keV** and a dosage of **3×10¹⁵ atoms/cm².**” (Tamaki, ¶86.)

103. Tamaki further discloses that the “p-type impurity implantation (third p-type impurity implantation) **with respect to the SRAM section p-type gate electrode formation film 111** is performed under the conditions of, for example, an implantation energy of 5 keV and **a dosage of 2×10^{15} at[oms]/cm².**” (Tamaki, ¶88.)

104. That is, the implantation of the p-type dopants is carried out at the same energy (5keV). However, the p-type dopant dosage of the entire gate electrode of logic PMIS (3×10^{15} atoms/cm²) is higher than that of the entire gate

electrode of SRAM PMIS (2×10^{15} atoms/cm²). For this reason, the resulting p-type impurity concentration in the gate electrode of the logic PMIS would be greater.

2. N-type Impurity Concentrations

105. Tamaki discloses that the “n-type impurity implantation (second n-type impurity implantation) with respect to the logic circuit section n-type gate electrode formation film 109 is performed under the conditions of, for example, an **implantation energy of 10 keV and a dosage of 8×10^{15} atoms/cm².**” (Tamaki, ¶86.)

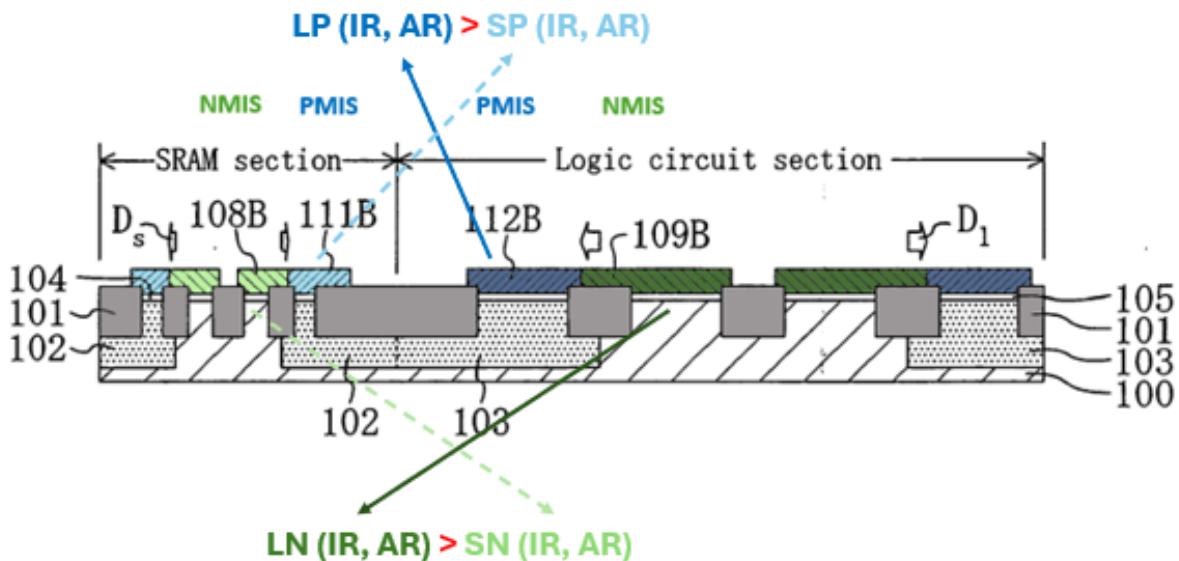
106. Tamaki further discloses that the “n-type impurity implantation (first n-type impurity implantation) with respect to the SRAM section n-type gate electrode formation film 108 is performed under the conditions of, for example, an **implantation energy of 10 keV and a dosage of 4×10^{15} atms/cm² [sic].**” (Tamaki, ¶87.)

107. That is, the implantation of the n-type dopants is carried out at the same energy (10keV). However, the n-type dopant dosage of the entire gate electrode of the logic NMIS (8×10^{15} atoms/cm²) is higher than that of the entire gate electrode of the SRAM NMIS (4×10^{15} atoms/cm²). For this reason, the resulting n-type impurity concentration in the gate electrode of the logic NMIS would be greater.

108. Notably, for both p-type and n-type impurity implantations, each gate electrode over the isolation region and that over the active region in receives the same impurity implantation.

109. Accordingly, under Tamaki's first embodiment, the impurity concentration relationship discussed above, which is illustrated in Figure 3B below, can be expressed as follows:

Tamaki's First Embodiment
$LP(IR, AR) > SP(IR, AR)$
$LN(IR, AR) > SN(IR, AR)$



Tamaki, Figure 3B

3. Scenario A-1

110. As I discussed in §IV.D, the independent claims encompass at least the following four scenarios:

Claim Language		Scenarios Covered			
		A-1	A-2	B-1	B-2
<i>first dual-gate electrode</i>	<i>first gate electrode</i>	logic NMOS	SRAM NMOS	logic PMOS	SRAM PMOS
	<i>second gate electrode</i>	logic PMOS	SRAM PMOS	logic NMOS	SRAM NMOS
<i>second dual-gate electrode</i>	<i>third gate electrode</i>	SRAM NMOS	logic NMOS	SRAM PMOS	logic PMOS
	<i>fourth gate electrode</i>	SRAM PMOS	logic PMOS	SRAM NMOS	logic NMOS

111. Under Scenario A-1 (first conductivity type = **n-type**; second conductivity type = **p-type**), Tamaki's first embodiment renders claims 1-2, 4, 8-9, 12, 14.

a. Independent Claim 1

(1) Preamble [1P]

[1P] <i>A semiconductor device, comprising:</i>

112. Tamaki expressly discloses a “*semiconductor device*”³ that includes an “SRAM section and a logic circuit section.” (Tamaki, ¶¶2, 82 (“semiconductor device manufacturing method in accordance with Embodiment 1”), 104, 115 (“semiconductor device manufacturing method in accordance with Embodiment 2”), Figure 3B (first embodiment), claim 1 (“semiconductor device”).)

(2) “**First Dual-Gate Electrode**” Limitations [1A], [1C], [1E]-[1F]

[1A] *a first dual-gate electrode; and*

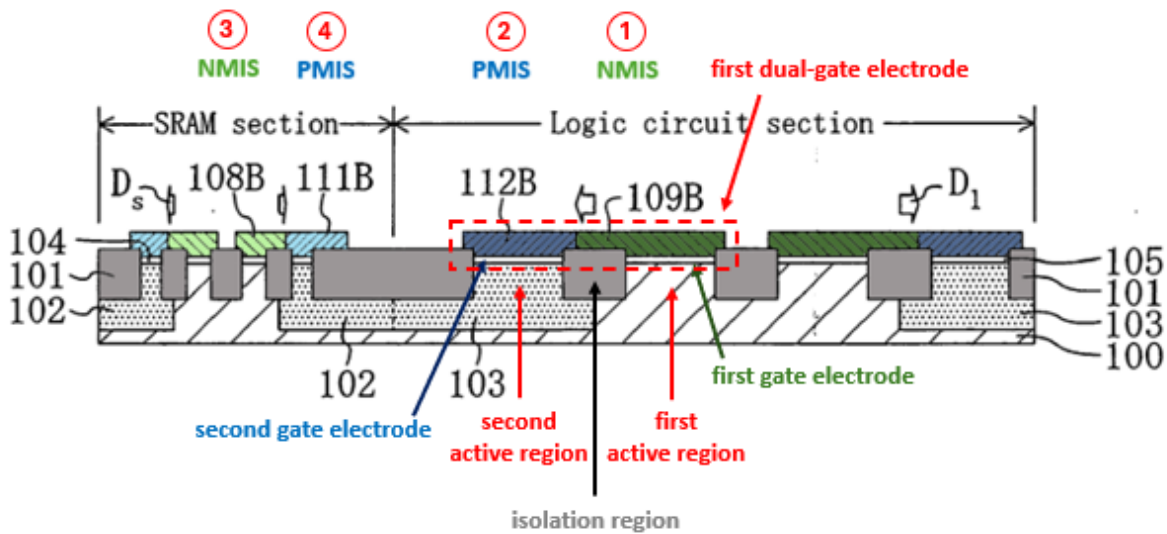
[1C] *the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,*

[1E] *the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,*

[1F] *the first gate electrode and the second gate electrode are connected to each other on the isolation region, and*

113. Tamaki discloses that logic-region n-type gate electrode 109 (“*first gate electrode*”) “is **formed integrally** with” logic p-type gate electrode 112 (“*second gate electrode*”), forming the “*first dual-gate electrode*” [1A]. (Tamaki, ¶¶98, Figure 3B (below), claim 5 reciting that “the second n-type gate electrode is formed integrally with the second p-type gate electrode”).)

³ Claim language indicated by italics throughout.

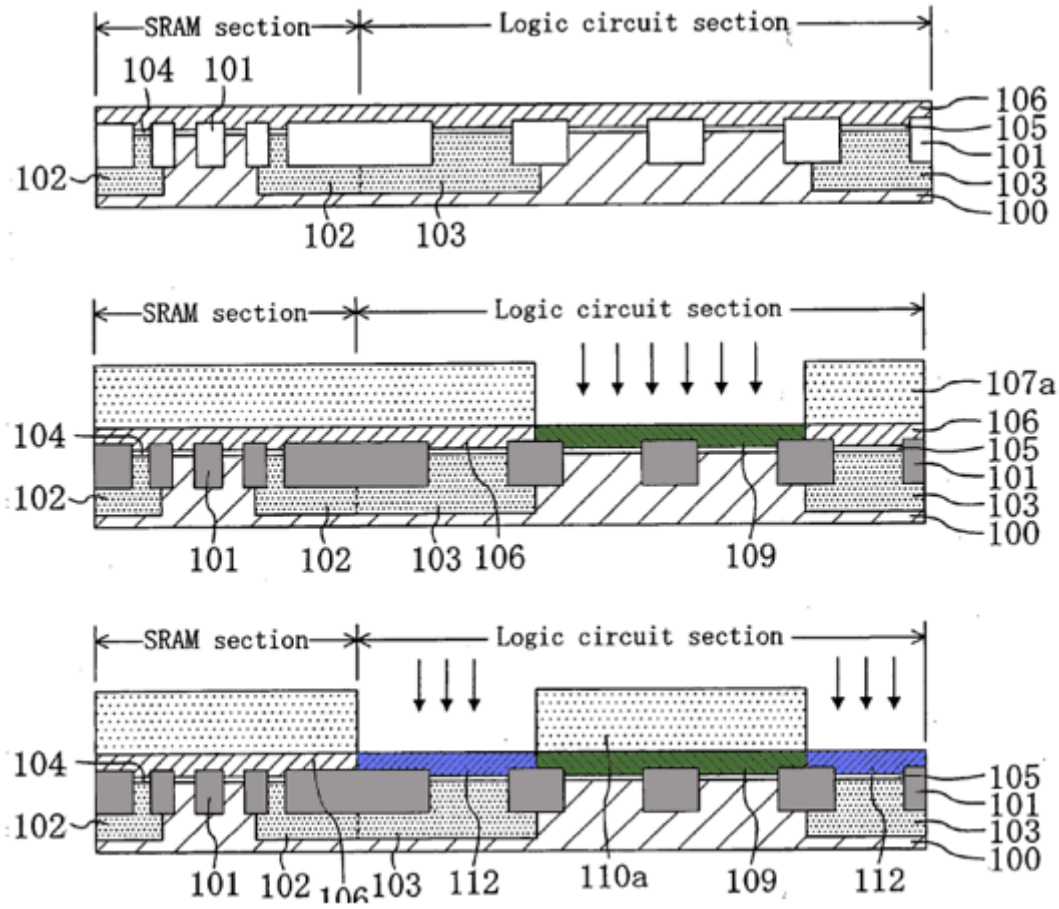


Tamaki, Figure 3B

114. Isolation region 101 separates the n-type and p-type active regions of the logic circuit. (Tamaki, ¶83.) Tamaki defines each “element formation region” as an “*active region*.” (Tamaki, ¶84). Thus, “*the first active region [n-type MIS (NMIS) element formation region] and the second active region [p-type MIS (PMIS) element formation region] are isolated from each other with an isolation region interposed therebetween*” [1E].

115. Tamaki discloses that during formation of the semiconductor device of the first embodiment, “logic circuit section gate insulating film 105 ... is formed in an element formation region (an active region) of the semiconductor substrate 100.” (Tamaki, ¶84.) In Tamaki, as seen in Figure 1A (below-top), gate electrode formation film 106 “**formed of a polysilicon film**” is then formed “on the entirety of the semiconductor substrate.” (Tamaki, ¶84.) Accordingly, the

fabrication sequence: a gate oxide 105 is formed in the logic active region, and a **polysilicon gate-formation film 106** is deposited across the wafer.

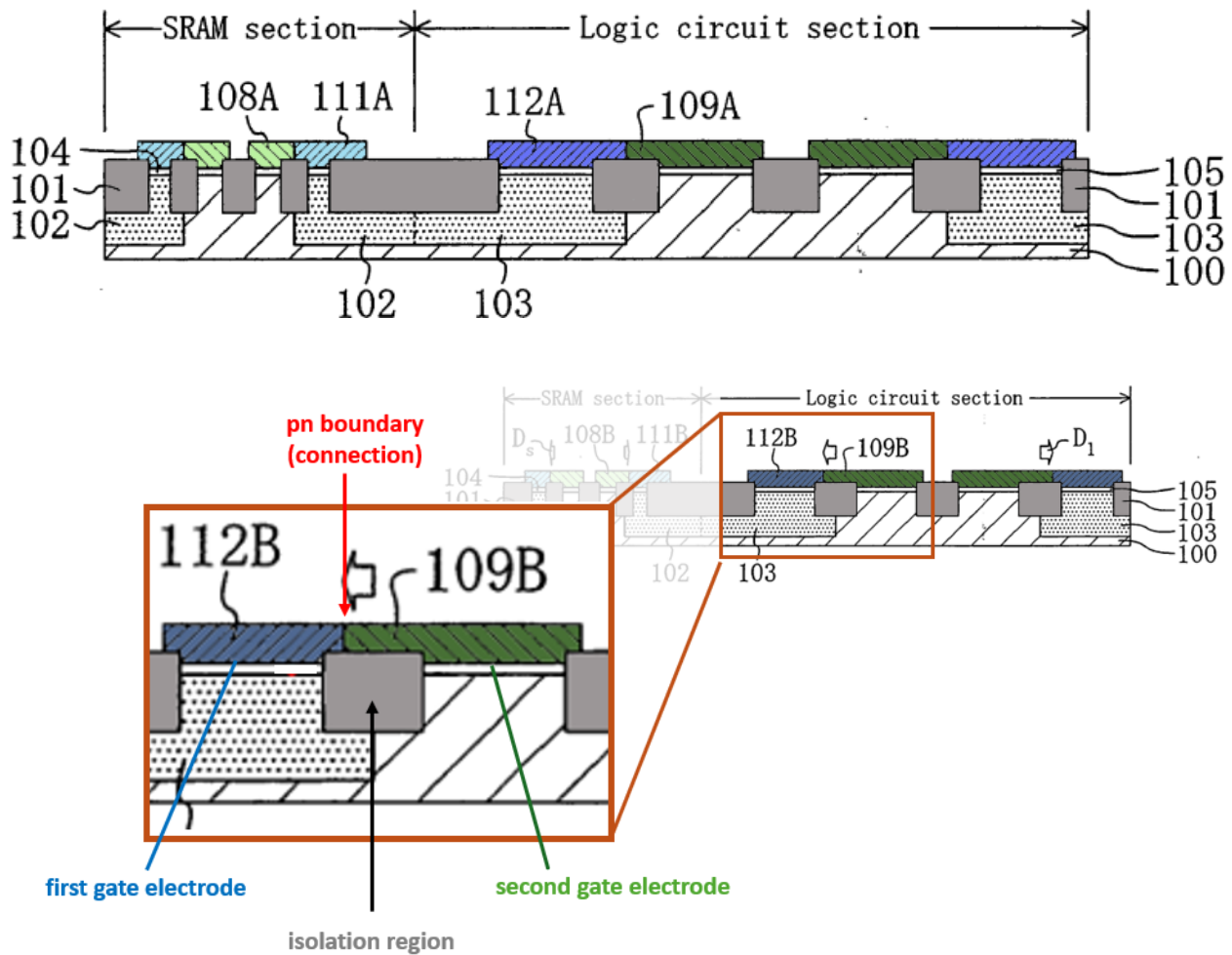


Tamaki, Figures 1A (top), 1B (middle), 1C (bottom)

116. An “n-type” dopant (e.g., phosphorous) is implanted to the gate-formation film 106 over the n-type MIS region, creating “a logic circuit section n-type gate electrode formation film 109.” (Tamaki, ¶85, Figure 1B (above-middle).) A “p-type impurity” (e.g., boron) is subsequently implanted over the p-type MIS region, forming “logic p-type gate electrode formation film 112.” (Tamaki, ¶86,

Figure 1C (above-bottom).) These constitute, respectively, “a first silicon film of a first conductivity type” and “a first silicon film of a second conductivity type.”

117. After patterning, logic n-type gate electrode 109A and logic p-type gate electrode 112A are obtained. (Tamaki, ¶98, Figure 3A (below-top).) In Figure 3B (below-bottom), gate 112B lies on the “first active region” and gate 109B on the “second active region,” satisfying limitation [1C]. Because the two gates share a continuous polysilicon track across isolation region 101, limitation [1F] is also met. (See also, Tamaki, claim 1.) (Tamaki, ¶103.)



Tamaki, Figures 3A (top), 3B (bottom) with enlargement

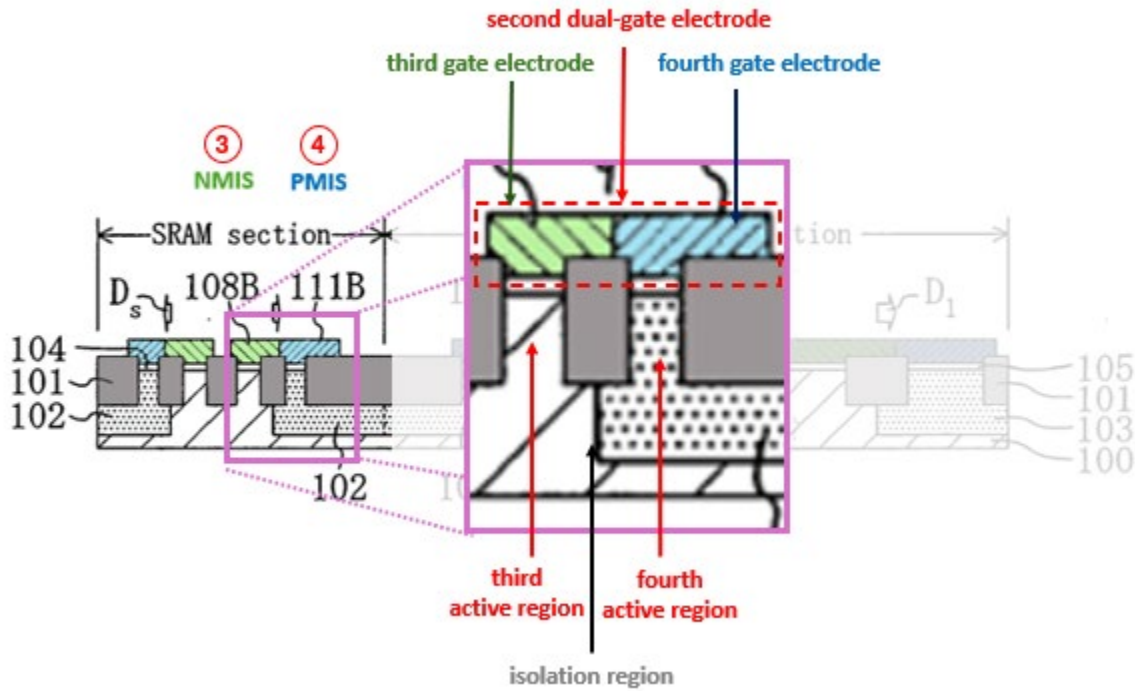
118. As shown in Figure 3B (above-bottom), n-type gate electrode 109B “**is formed integrally**” with the p-type gate electrode. (Tamaki, ¶98, claim 2 reciting that “the first n-type gate electrode is integrally formed with the first p-type gate electrode”.) Tamaki explains “**the pn boundary** between the logic circuit section n-type gate electrode 109B [green] and the logic circuit section p-type gate electrode 112B [blue] **is located at a point on the element isolation region 101**” between the NMOS active region and the PMOS active region. (Tamaki, ¶103.) Tamaki’s first embodiment thus discloses “*the first gate electrode and the second gate electrode are connected to each other on the isolation region.*”

**(3) “Second Dual-Gate Electrode” Limitations
[1B], [1D]**

[1B] *a second dual-gate electrode being separated from the first dual-gate electrode, wherein*

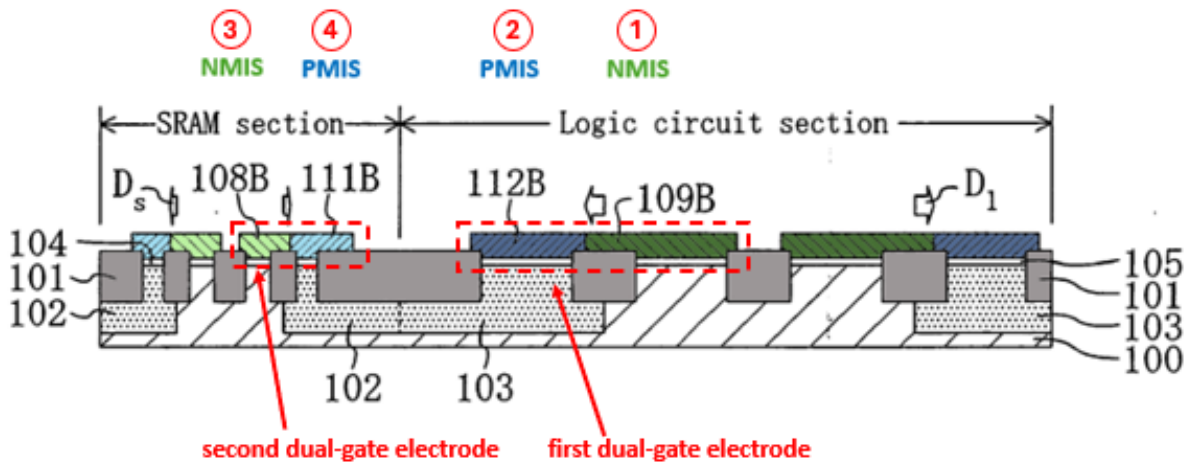
[1D] *the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,*

119. Within the SRAM section, n-type gate electrode 108A (“*third gate electrode*”) “**is formed integrally with**” p-type gate electrode 111A (“*fourth gate electrode*”), forming “*a second dual-gate electrode*” [1B]. (Tamaki, ¶98, Figure 3B, claim 2).



Tamaki, Figure 3B with enlargement

120. Patterning leaves the “*second dual-gate electrode*” physically
“*separated from the first dual-gate electrode,*”satisfying limitation [1B]. (Tamaki
¶98, Figure 3B)



Tamaki, Figure 3B

121. Tamaki details the STI isolation and the n-type/p-type implants that create **silicon films of the respective conductivity types** in the SRAM gates, fulfilling limitation [1D]. Specifically, the SRAM section includes “element isolation region 101, which separates an element formation region of a SRAM section n-type MIS transistor and an element formation region of a SRAM section p-type MIS transistor.” (Tamaki, ¶83.) Each “element formation region” is an “*active region*.” (Tamaki, ¶84 (“an element formation region (an **active region**)”); *see also*, Tamaki, ¶83 (“SRAM section n-type well region 102 is formed in a p-type MIS formation region of the semiconductor substrate 100 in the SRAM section”).)

122. During formation of Tamaki’s first embodiment device, “SRAM section gate insulating film 104 ... is formed in an element formation region (an active region) of the semiconductor substrate 100.” (Tamaki, ¶84.) Gate electrode formation film 106 “**formed of a polysilicon film**” is then formed “on the entirety of the semiconductor substrate.” (Tamaki, ¶84.) An “n-type impurity [“*first conductivity type*”], for example, phosphorous or the like is implanted to the gate electrode formation film 106 on the n-type MIS formation region in the SRAM section.” (Tamaki, ¶87, Figure 2A.) A “p-type impurity [“*second conductivity type*”], for example, boron or the like is implanted to the

gate electrode formation film 106 on the p-type MIS formation region in the SRAM section.” (Tamaki, ¶88, Figure 2B.)

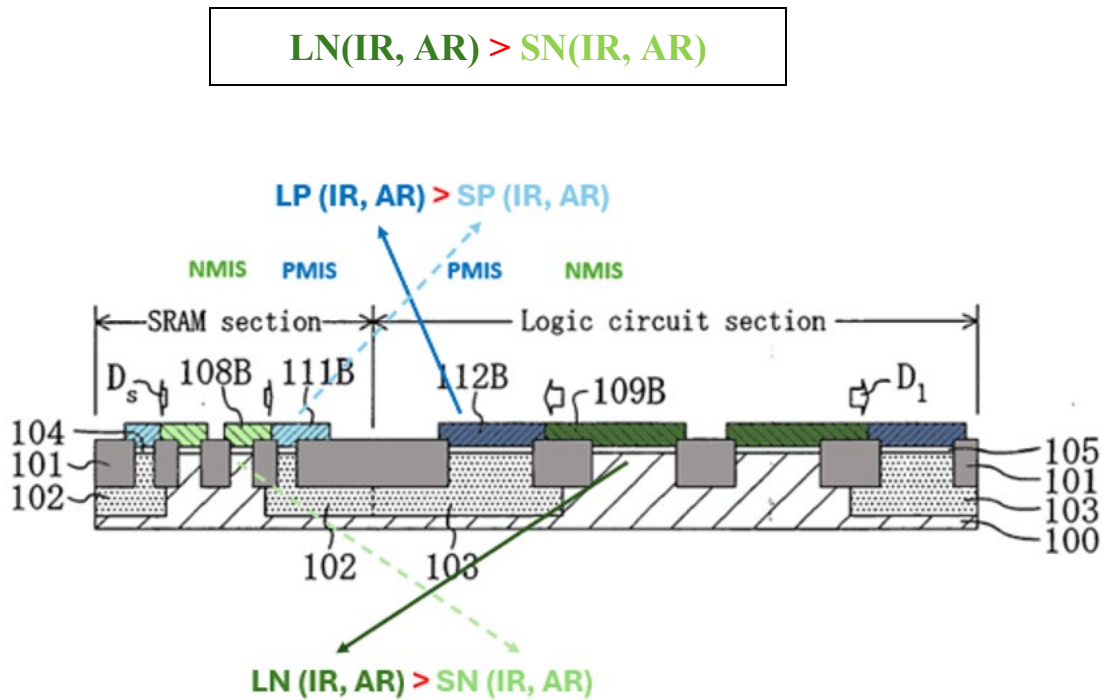
123. Patterning is then performed on “the SRAM section n-type gate electrode formation film 108, and the SRAM section p-type gate electrode formation film 111”, forming SRAM section n-type gate electrode 108B and SRAM section p-type gate electrode 111B. (Tamaki, ¶98.) As shown in Figure 3B (above), n-type gate electrode 108B (“*third gate electrode*”) is “*located on [the] third active region [n-type MIS element formation region]*” and has “*a second silicon film of the first conductivity type [p-type gate electrode formation film]*”. And p-type gate electrode 111B (“*fourth gate electrode*”) is “*located on [the] fourth active region [p-type MIS element formation region]*” and has “*a second silicon film of the second conductivity type [p-type gate electrode formation film]*.”

(4) Impurity Concentration Limitation [1G]

[1G] <i>at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.</i>

124. The impurity concentration relationship of Tamaki’s first embodiment, discussed in §V.B.2, is summarized below:

Tamaki’s First Embodiment
LP(IR, AR) > SP(IR, AR)



Tamaki, Figure 3B

125. Tamaki specifies higher n-type dopant dose for the **logic n-type gate** ($8 \times 10^{15} \text{ cm}^{-2}$) than for the **SRAM n-type gate** ($4 \times 10^{15} \text{ cm}^{-2}$), both implanted at 10 keV. (Tamaki ¶¶ 85, 87.) Consequently, $LN(IR, AR) > SN(IR, AR)$ (see Figure 3B), meeting limitation [1G].

126. Therefore, Tamaki’s first embodiment discloses “at least a portion of the first silicon film of the first conductivity type [$LN(IR, AR)$] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [$SN(IR, AR)$]” under Scenario A-1.

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	LN(IR, AR) > SN(AR)	LN(IR, AR) > SN(IR, AR)
A-2	SN(IR, AR) > LN(AR)	
B-1	LP(IR, AR) > SP(AR)	LP(IR, AR) > SP(IR, AR)
B-2	SP(IR, AR) > LP(AR)	

**(5) First Embodiment Under Scenario A-1
Summary**

<i>“first dual gate electrode”</i>	<i>“a first gate electrode”</i>	Logic-NMIS gate electrode 109
	<i>“a second gate electrode”</i>	Logic-PMIS gate electrode 112
<i>“second dual gate electrode”</i>	<i>“a third gate electrode”</i>	SRAM-NMIS gate electrode 108
	<i>“a fourth gate electrode”</i>	SRAM-PMIS gate electrode 111
impurity concentration relationship relied on		LN (IR, AR) > SN (AR)

127. Accordingly, Tamaki’s first embodiment satisfies every element of independent claim 1 under Scenario A-1.

b. Claim 2

[2] The semiconductor device of claim 1, wherein an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.

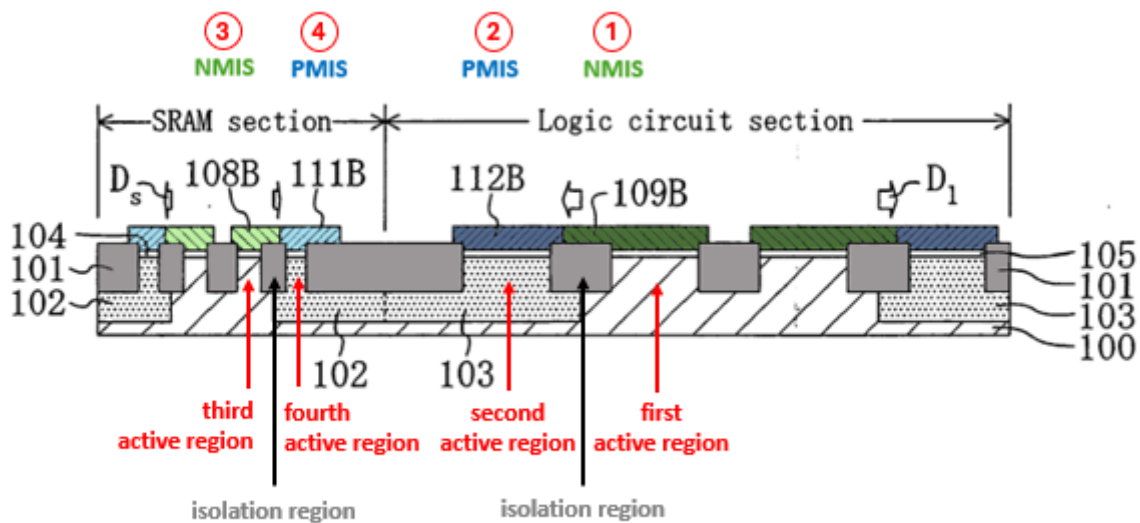
128. Tamaki's first embodiment discloses "*an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region*" under Scenario A-1.

129. In Tamaki's first embodiment, the "width in the gate width direction of an element isolation region 101, which separates an element formation region of a SRAM section n-type MIS transistor [*"third active region"*] and an element formation region of a SRAM section p-type MIS transistor [*"fourth active region"*], is set **smaller** than the width in the gate width direction of an element isolation region 101, which separates an element formation region of a logic circuit section n-type MIS transistor [*"first active region"*] and an element formation region of a logic circuit section p-type MIS transistor [*"second active region"*]." (Tamaki, ¶83, Figure 3A, 3B (below).) In other words, the width of the isolation region 101 located between the SRAM n-type and p-type MIS transistors is smaller than the isolation region width between the corresponding logic transistors.

130. Accordingly, Tamaki's first embodiment expressly teaches this geometry. In particular, element-isolation region 101 separating the logic-region NMIS transistor (*"first active region"*) from the logic-region PMIS (*"second active region"*) is intentionally made *wider* than the corresponding isolation region that separates the SRAM-region NMIS transistor (*"third active region"*) and SRAM-region PMIS transistor (*"fourth active region"*) (Tamaki, ¶83, Figure 3A-3B

(below).) Put differently, the SRAM cell is laid out more densely than the logic inverter, so the STI between its complementary transistors is narrower. That relative spacing difference is exactly what claim 2 requires.

131. A POSITA would expect this result: SRAM arrays chase maximum density, whereas logic blocks tolerate, and often require, larger isolation for noise and layout-routing margins. (Igarashi, ¶4; Tamaki, ¶29; Zampaglione, 3:58-64.)



Tamaki, Figure 3B (Scenario A)

c. Claim 4

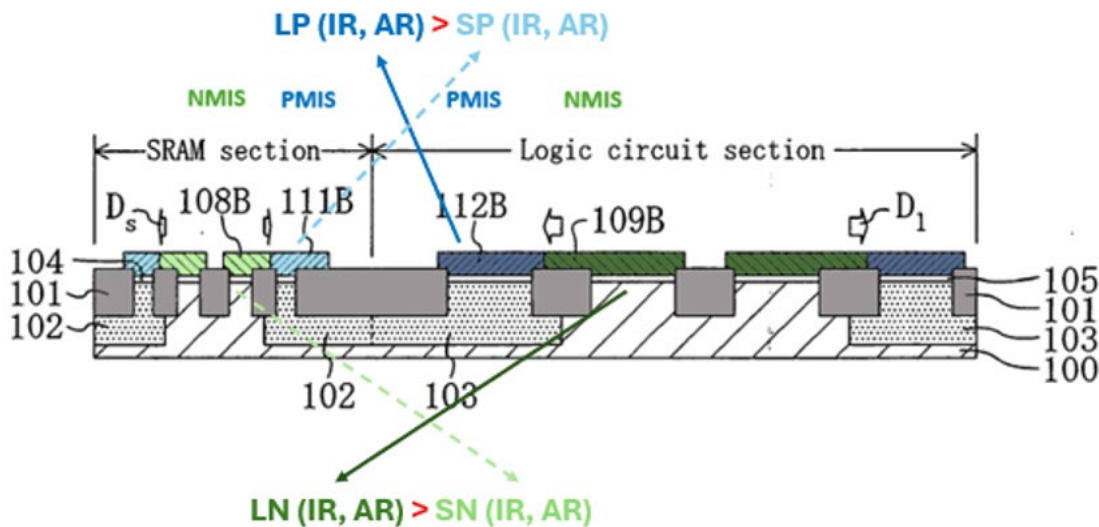
[4] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

132. The following table summarizes the impurity concentration relationship for claim 4 and Tamaki's impurity concentration relationship under the first embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	LN(AR) > SN(AR)	LN(IR, AR) > SN(IR, AR)
A-2	SN(AR) > LN(AR)	
B-1	LP(AR) > SP(AR)	LP(IR, AR) > SP(IR, AR)
B-2	SP(AR) > LP(AR)	

133. As seen in Figure 3B (below), the portion of electrode 109 (dark green) over the active region, **LN(AR)**, which corresponds to the “*the first silicon film of the first conductivity type located on the first active region*” has a higher n-type impurity concentration (“*first-conductivity-type impurity concentration*”) than the portion of electrode 108 (light green) over the active region, **SN(AR)**, (“*the second silicon film of the first conductivity type located on the third active region*”). That is, **LN(AR) > SN(AR)** in Tamaki's first embodiment under scenario A-1. This is because, as explained in §V.B.2, the logic-region n-type gate electrode 109 (**LN(AR)**) receives an n-dopant dose of $8 \times 10^{15} \text{ cm}^{-2}$, whereas the SRAM-region n-type gate electrode 108 (**SN(AR)**) receives only $4 \times 10^{15} \text{ cm}^{-2}$,

under the same energy conditions. Consequently, $LN(AR) > SN(AR)$, exactly as claim 4 demands.



Tamaki, Figure 3B

134. Accordingly, Tamaki's first embodiment discloses "a portion of the first silicon film of the first conductivity type located on the first active region [$LN(AR)$] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [$SN(AR)$]" under scenario A-1.

d. Claim 8

[8] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region.

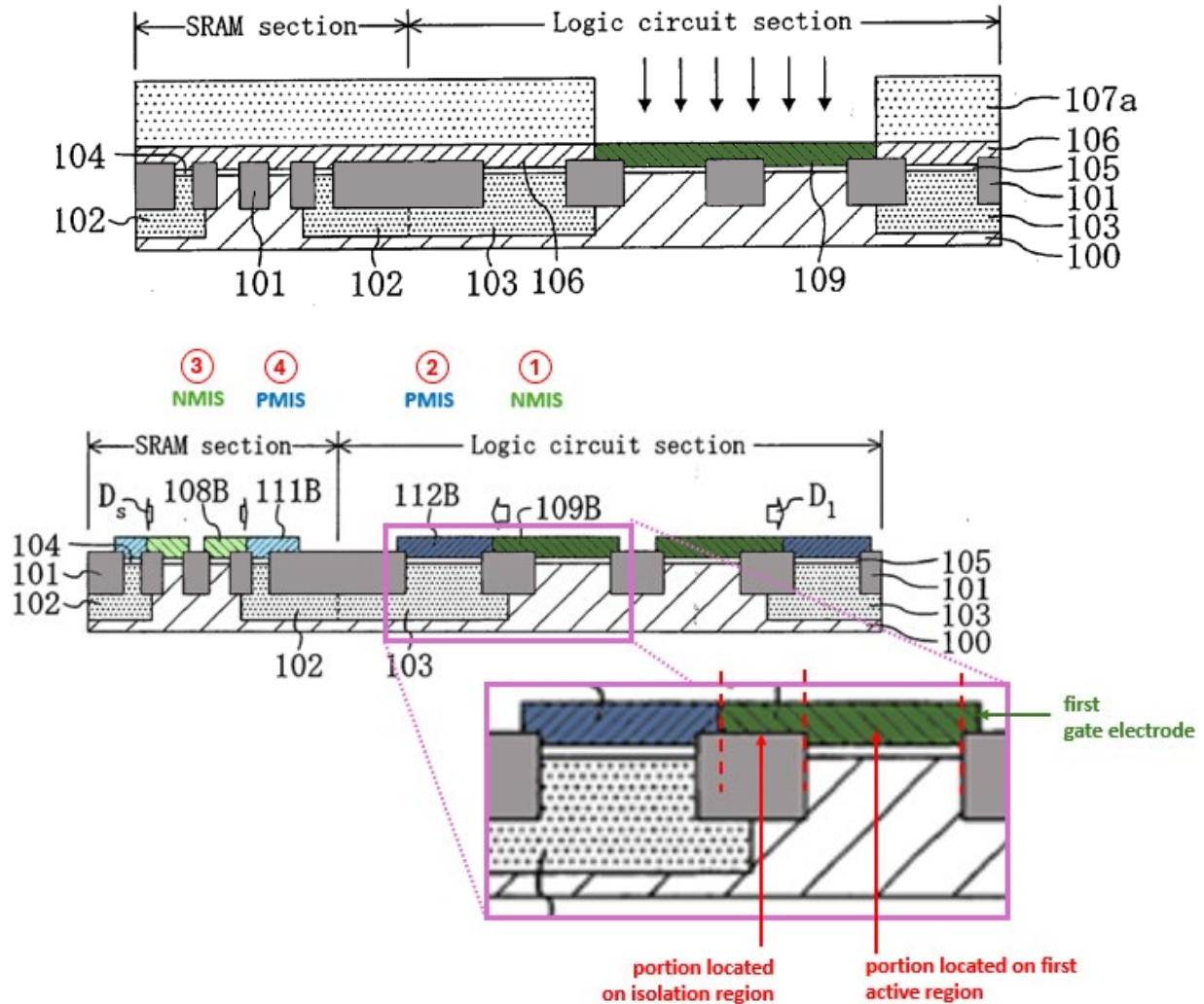
135. The following table summarizes the impurity concentration relationship for claim 8 and Tamaki's impurity concentration relationship under the first embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$\text{LN}(\text{IR}) \approx \text{LN}(\text{AR}) > \text{SN}(\text{AR})$	$\text{LN}(\text{IR}, \text{AR}) > \text{SN}(\text{IR}, \text{AR})$
A-2	$\text{SN}(\text{IR}) \approx \text{SN}(\text{AR}) > \text{LN}(\text{AR})$	
B-1	$\text{LP}(\text{IR}) \approx \text{LP}(\text{AR}) > \text{SP}(\text{AR})$	$\text{LP}(\text{IR}, \text{AR}) > \text{SP}(\text{IR}, \text{AR})$
B-2	$\text{SP}(\text{IR}) \approx \text{SP}(\text{AR}) > \text{LP}(\text{AR})$	

136. As seen in Figure 1B (below-top), the n-type implant into gate-formation film 106 is performed in a single, blanket step across the entire logic-region polysilicon trace. (Tamaki ¶85, implantation at 10 keV and a dosage of 8×10^{15} atoms/cm², Figure 1B (below-top), Figure 3B (below-bottom).) Because the dose and energy are uniform, the segment of gate 109 over the active region and the segment that spans isolation region 101 share essentially the same dopant concentration.

137. That is, the implantation is carried out uniformly across the entire gate electrode film. Therefore, the impurity concentration of the portion of the first gate electrode over the first active region ($\text{LN}(\text{AR})$) is substantially equal to that of the

portion located over the isolation region (**LN(AR)**) or as illustrated with the shorthand notation: **LN(AR) $\approx$ LN(IR)**.



Tamaki, Figures 1B (top), 3B (bottom) with enlargement

138. Thus, Tamaki's first embodiment discloses "a portion of the first silicon film of the first conductivity type located on the first active region [**LN(AR)**] has a first-conductivity-type impurity concentration substantially equal

to that of a portion of the first silicon film of the first conductivity type located on the isolation region [LN(IR)],” under scenario A-1.

139. That is, the relationship $LN(AR) \approx LN(IR)$ in Tamaki’s first embodiment under scenario A-1 satisfies claim 8.

e. Claim 9

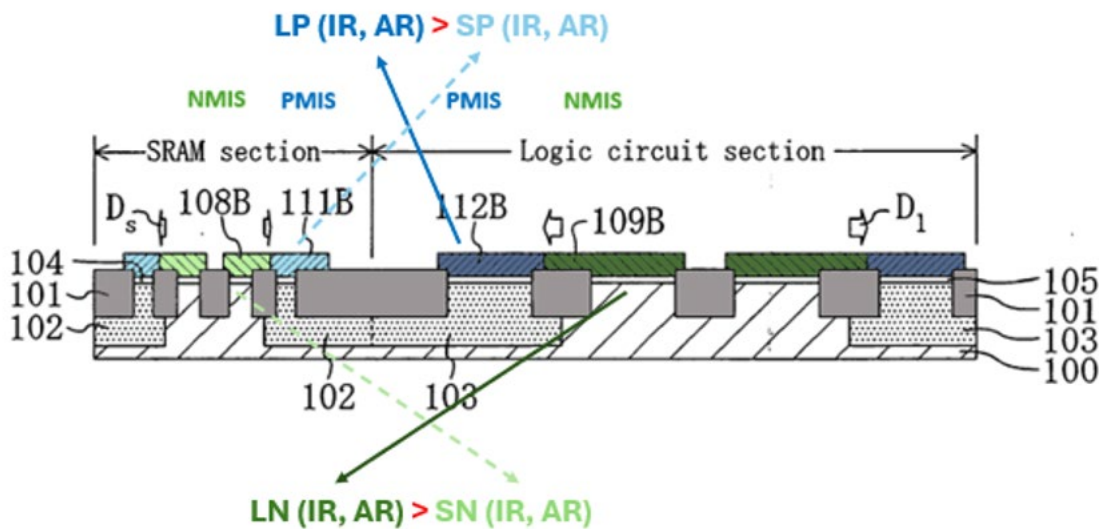
[9] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

140. The following table summarizes the impurity concentration relationship for claim 9 and Tamaki’s impurity concentration relationship under the first embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$LN(IR) > SN(AR)$	$LN(IR, AR) > SN(IR, AR)$
A-2	$SN(IR) > LN(AR)$	
B-1	$LP(IR) > SP(AR)$	$LP(IR, AR) > SP(IR, AR)$
B-2	$SP(IR) > LP(AR)$	

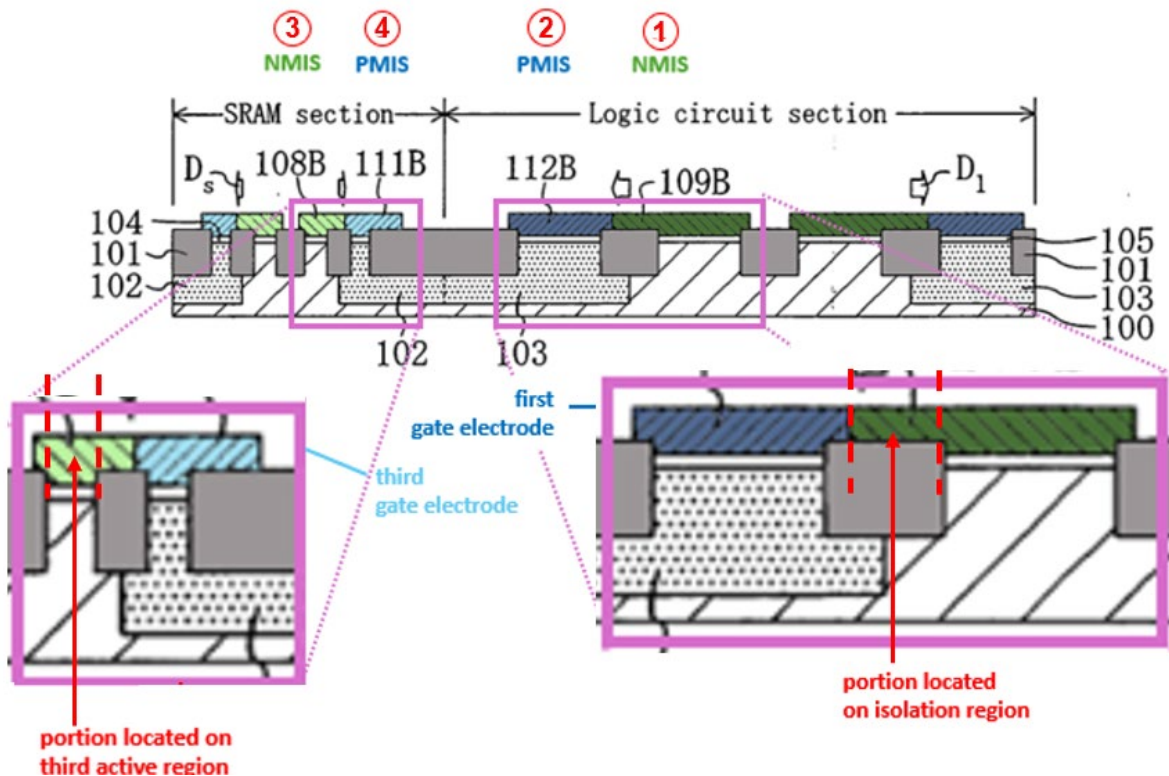
141. As seen below in Figure 3B, the portion of electrode 109 over the isolation region, LN(IR), (“the first silicon film of the first conductivity type located on the isolation region”) has a higher p-type impurity concentration (“first-

conductivity-type impurity concentration”) than the portion of electrode 108 over the active region, **SN(AR)**, (“the second silicon film of the first conductivity type located on the third active region”). That is, **LN(IR) > SN(AR)** in Tamaki’s first embodiment under scenario A-1.



Tamaki, Figure 3B

142. This relationship (**LN(IR) > SN(AR)**) is more clearly illustrated in Figure 3B below with the enlargements that identify the isolation region in the logic NMIS and the active region in the SRAM NMIS. Because the logic-NMIS gate electrode region over STI, designated **LN(IR)**, contains more n-type dopant than the SRAM-NMIS gate electrode region over the active area, **SN(AR)**, the “portion of the first silicon film ... on the isolation region” has a higher first-conductivity-type concentration than the corresponding portion “located on the third active region,” satisfying claim 9.



Tamaki, Figure 3B with enlargements

143. Accordingly, Tamaki discloses “a portion of the first silicon film of the first conductivity type located on the isolation region [LN(IR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SN(AR),” in Tamaki’s first embodiment under scenario A-1.

f. Claim 12

[12P] The semiconductor device of claim 1, wherein

[12A] a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region, and

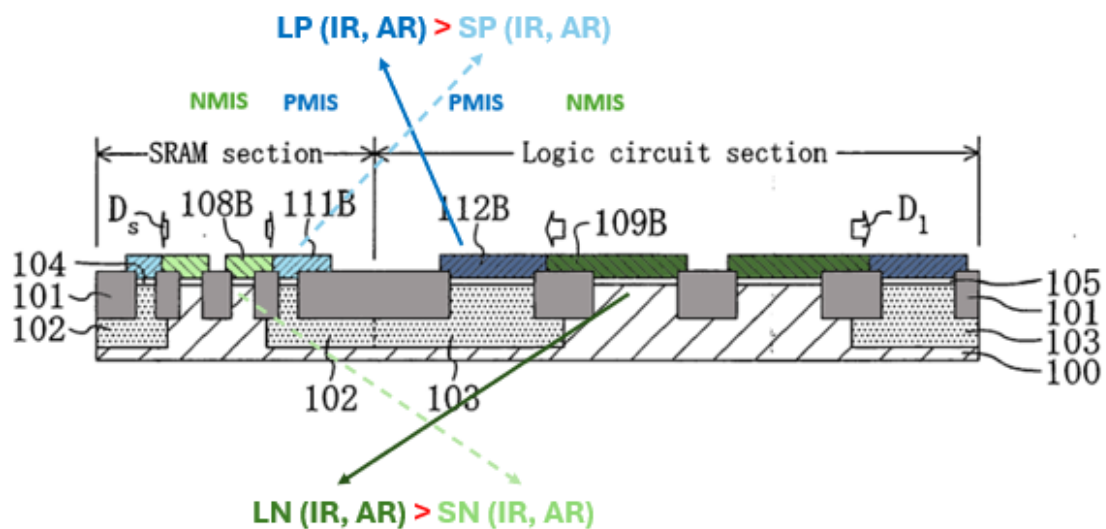
[12B] a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

144. The following table summarizes the impurity concentration relationship for claim 12 and Tamaki's impurity concentration relationship under the first embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$LN(AR) > SN(AR)$ $LP(AR) > SP(AR)$	$LN(IR, AR) > SN(IR, AR)$ $LP(IR, AR) > SP(IR, AR)$
A-2	$SN(AR) > LN(AR)$ $SP(AR) > LP(AR)$	
B-1	$LP(AR) > SP(AR)$ $LN(AR) > SN(AR)$	
B-2	$SP(AR) > LP(AR)$ $SN(AR) > LN(AR)$	

145. As seen in Figure 3B (below), the logic-NMIS region over the active area, $LN(AR)$, is more heavily n-doped than the SRAM-NMIS region $SN(AR)$; thus $LN(AR) > SN(AR)$; and [12B] The logic-PMIS region over the active area, $LP(AR)$, carries a higher p-type concentration than the SRAM-PMIS region $SP(AR)$; thus $LP(AR) > SP(AR)$.

146. Therefore, the portion of electrode 109 over the active region, **LN(AR)**, (“the first silicon film of the first conductivity type located on the first active region”) has a higher p-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 108 over the active region, **SN(AR)**, (“the second silicon film of the first conductivity type located on the third active region”) and the portion of electrode 112 over the active region, **LP(AR)**, (“the first silicon film of the second conductivity type located on the second active region”) has a higher n-type impurity concentration (“second-conductivity-type impurity concentration”) than the portion of electrode 108 over the active region, **SP(AR)**. That is, **LN(AR) > SN(AR)** and **LP(AR) > SP(AR)** in Tamaki’s first embodiment under scenario A-1



Tamaki, Figure 3B

147. Accordingly, Tamaki discloses “*a portion of the first silicon film of the first conductivity type located on the first active region [LN(AR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SN(AR)],*” and “*a portion of the first silicon film of the second conductivity type located on the second active region [LP(AR)] has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region [SP(AR)].*”

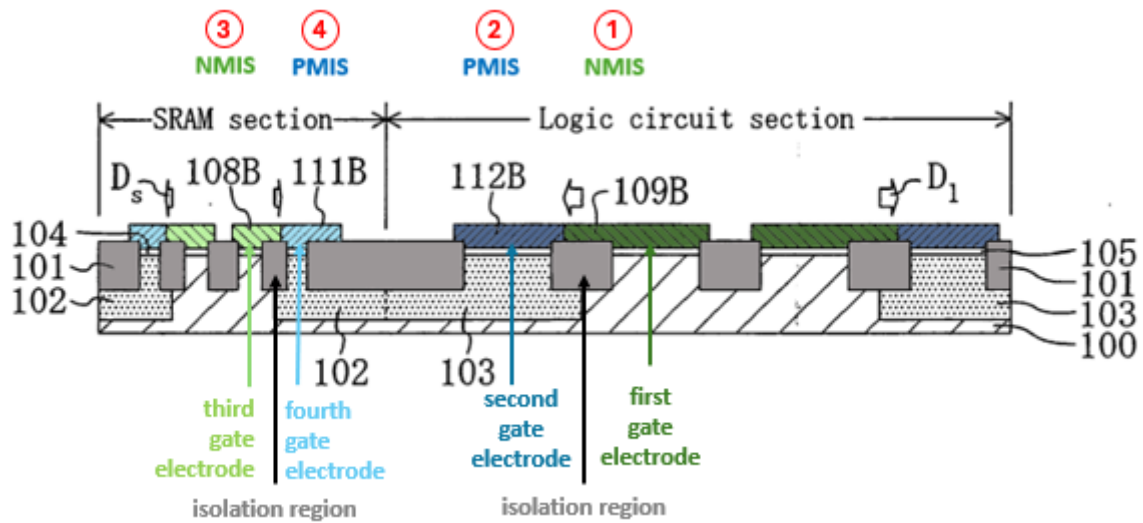
g. Claim 14

[14] The semiconductor device of claim 1, wherein

each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and

each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit.

148. Tamaki’s first embodiment distinguished logic-region transistors from SRAM-region transistors, as shown in Figure 3B (below). The logic circuit section utilizes n-type gate electrode 109B [“*first gate electrode*”] and p-type gate electrode 112B [“*second gate electrode*”], while the SRAM array utilizes n-type gate electrode 108B [“*third gate electrode*”] and p-type gate electrode 111B [“*fourth gate electrode*”].” (Tamaki, ¶98.) Tamaki’s first embodiment discloses claim 14 under Scenario A-1.



Tamaki, Figure 3B

4. Scenario B-1

149. As I discussed in §IV.D, the independent claims encompass at least the following four scenarios:

Claim Language		Scenarios Covered			
		A-1	A-2	B-1	B-2
<i>first dual-gate electrode</i>	<i>first gate electrode</i>	logic NMOS	SRAM NMOS	logic PMOS	SRAM PMOS
	<i>second gate electrode</i>	logic PMOS	SRAM PMOS	logic NMOS	SRAM NMOS
<i>second dual-gate electrode</i>	<i>third gate electrode</i>	SRAM NMOS	logic NMOS	SRAM PMOS	logic PMOS
	<i>fourth gate electrode</i>	SRAM PMOS	logic PMOS	SRAM NMOS	logic NMOS

150. Tamaki's first embodiment renders claims 1-2, 4, 8-9, and 12-14 obvious under Scenario B-1.

a. Independent Claim 1

(1) Preamble [1P]

[1P] *A semiconductor device, comprising:*

151. As discussed in §V.B.3.a.(1), Tamaki's first embodiment clearly describes a "*semiconductor device*" that satisfies the preamble under Scenario B-1.

(2) "First Dual-Gate Electrode" Limitations [1A], [1C], [1E]-[1F]

[1A] *a first dual-gate electrode; and*

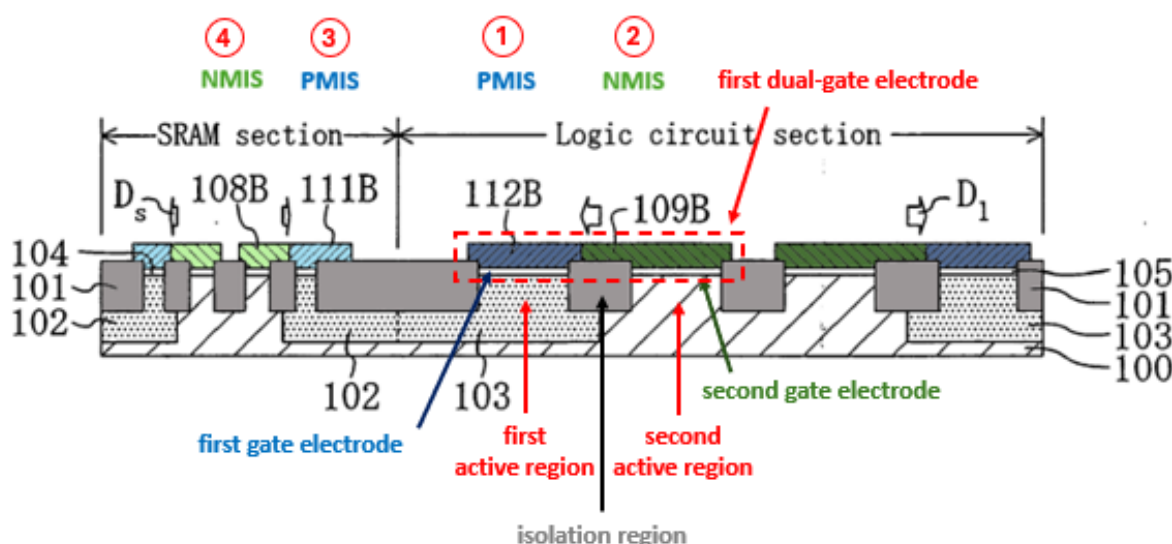
[1C] *the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,*

[1E] *the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,*

[1F] *the first gate electrode and the second gate electrode are connected to each other on the isolation region, and*

152. For the reasons discussed in §V.B.3.a.(2), Tamaki's logic PMIS and NMIS gate electrodes (112 and 109 respectively) are integrally formed and collectively constitute "*a first dual-gate electrode*" [1A]. (See, e.g., Figure 3B, claim 5.) Under Scenario B-1, "*the first dual-gate electrode*" is the logic-PMIS gate electrode 112, which sits on the *first active region* and comprise a *first*

conductivity-type film [p-type]. The second gate electrode is the logic-NMIS gate electrode 109, located on a second active region and made of a second conductivity-type [n-type]” – satisfying limitation [1C].



Tamaki, Figure 3B (Scenario B-1)

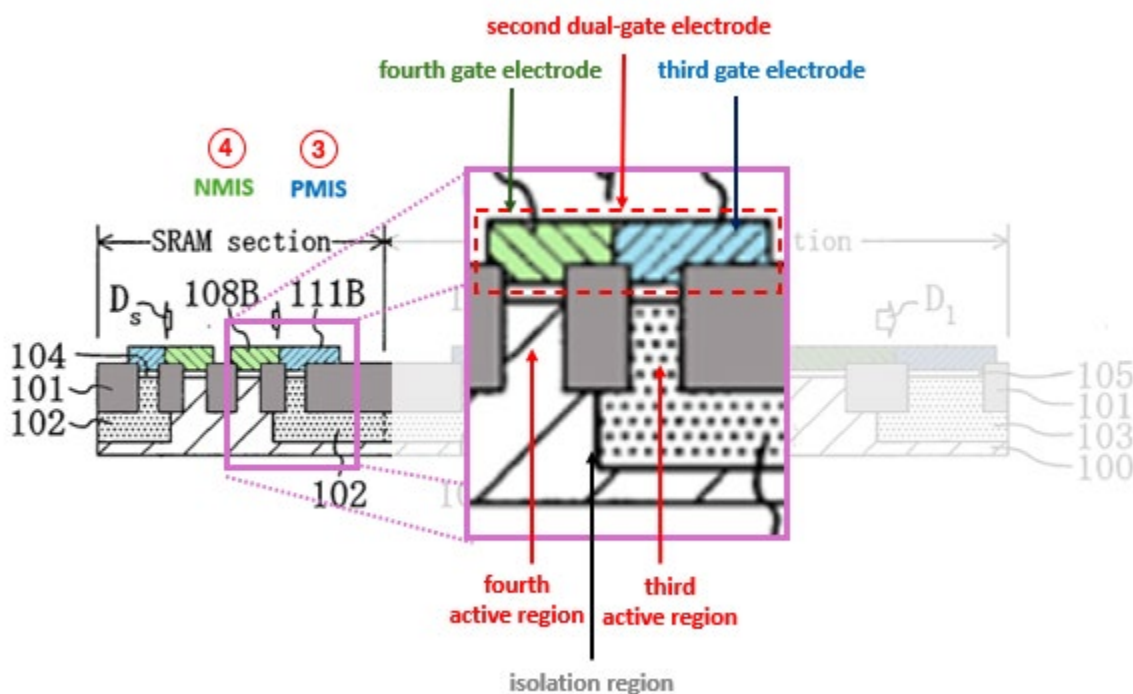
153. Figure 3B also shows that the first and second active region are separated by isolation region 101, and that the logic-PMIS gate electrode 112 and the logic-NMIS gate electrode 109 span this isolation region, confirming the device meets limitation [1E] and [1F].

(3) “Second Dual-Gate Electrode” Limitations [1B], [1D]

[1B] *a second dual-gate electrode being separated from the first dual-gate electrode, wherein*

[1D] the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,

154. As explained in §§V.B.3.a.(3), the SRAM PMIS and NMOS gates (gate electrodes 111 and 108) form a separate and structurally distinct “*second dual-gate electrode*” [1B]. Under Scenario B-1, SRAM PMIS gate 111 is the *third gate electrode* and consists of *the first conductivity type* [**p-type**] over the third active region, while SRAM-NMIS gate 108 is the fourth gate electrode with *the second conductivity type* [**n-type**] over the fourth active region [1D]. This configuration is also shown in Figure 3B.



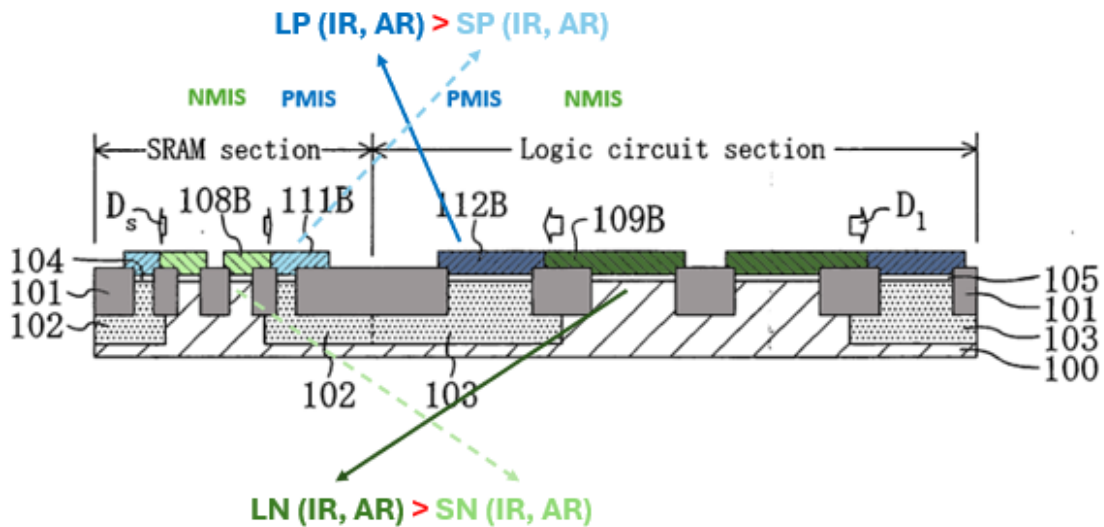
Tamaki, Figure 3B with enlargement

(4) Impurity Concentration Limitation

[1G] at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

155. As discussed in §V.B.2, Tamaki's impurity concentration relationships can be represented as:

Tamaki's First Embodiment
$LP(IR, AR) > SP(IR, AR)$
$LN(IR, AR) > SN(IR, AR)$



Tamaki, Figure 3B

156. Tamaki's first embodiment discloses "at least a portion of the first silicon film of the first conductivity type [$LP(IR, AR)$] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [$SP(IR, AR)$]" under scenario B-1.

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$LN(IR, AR) > SN(AR)$	$LN(IR, AR) > SN(IR, AR)$
A-2	$SN(IR, AR) > LN(AR)$	
B-1	$LP(IR, AR) > SP(AR)$	$LP(IR, AR) > SP(IR, AR)$
B-2	$SP(IR, AR) > LP(AR)$	

(5) First Embodiment Under Scenario B-1
Summary

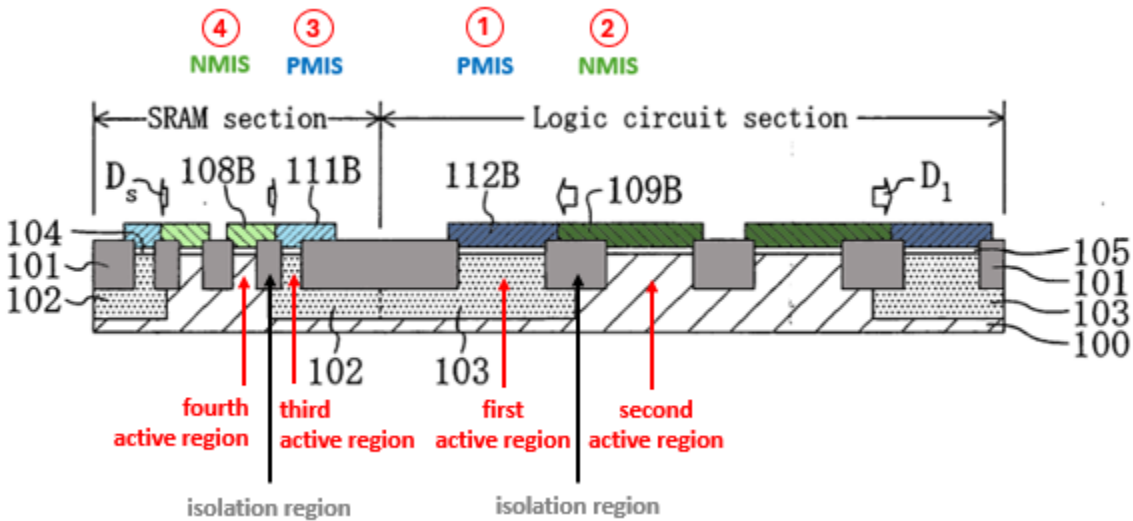
“first dual gate electrode”	“a first gate electrode”	Logic-PMIS gate electrode 112
	“a second gate electrode”	Logic-NMIS gate electrode 109
“second dual gate electrode”	“a third gate electrode”	SRAM-PMIS gate electrode 111
	“a fourth gate electrode”	SRAM-NMIS gate electrode 108
impurity concentration relationship relied on		$LP (IR, AR) > SP (AR)$

b. Claim 2

[2] The semiconductor device of claim 1, wherein an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.

157. As explained in §V.B.3(b), Tamaki’s first embodiment satisfies this claim under Scenario B-1. Specifically, the “*isolation width*” separating the logic-PMIS and NMIS transistors (corresponding to “*first active region and the second active region*”) is **intentionally wider than the width** separating the SRAM-PMIS

and NMIS transistors (corresponding to “*third active region and the fourth active region.*”) (Tamaki, ¶83, Figure 3B below.)



Tamaki, Figure 3B (Scenario B-1)

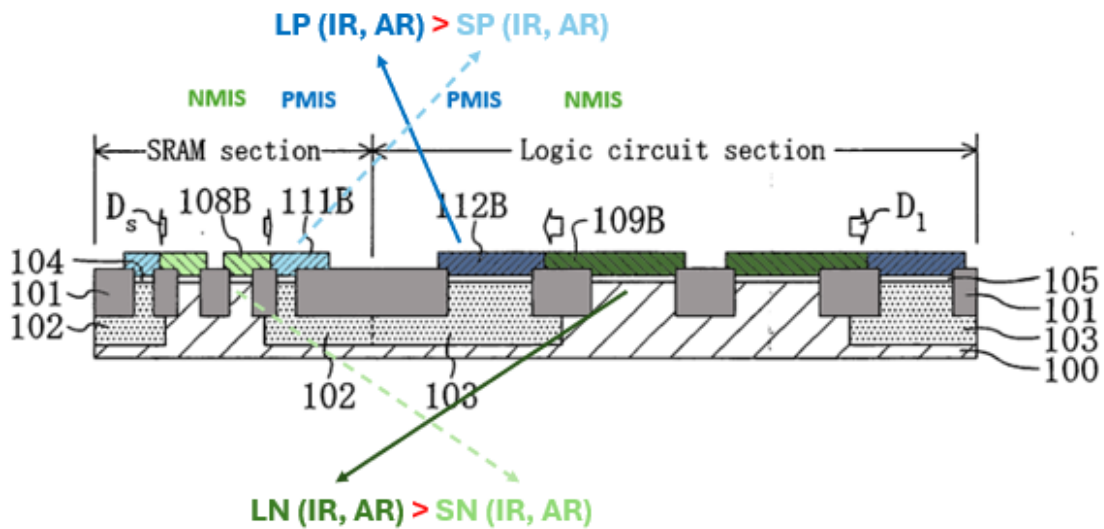
c. Claim 4

[4] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

158. The following table summarizes the impurity concentration relationship for claim 4 and Tamaki's impurity concentration relationship under the first embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	LN(AR) > SN(AR)	LN(IR, AR) > SN(IR, AR)
A-2	SN(AR) > LN(AR)	
B-1	LP(AR) > SP(AR)	LP(IR, AR) > SP(IR, AR)
B-2	SP(AR) > LP(AR)	

159. As seen in Figure 3b (below), the portion of electrode 112 over the active region, **LP(AR)**, (“the first silicon film of the first conductivity type located on the first active region”) has a higher p-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 111 over the active region, **SP(AR)**, (“the second silicon film of the first conductivity type located on the third active region”). That is, **LP(AR) > SP(AR)** in Tamaki’s first embodiment under scenario B-1.



Tamaki, Figure 3B

160. Accordingly, Tamaki's first embodiment discloses "*a portion of the first silicon film of the first conductivity type located on the first active region [LP(AR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SP(AR)]*" under scenario B-1.

d. Claim 8

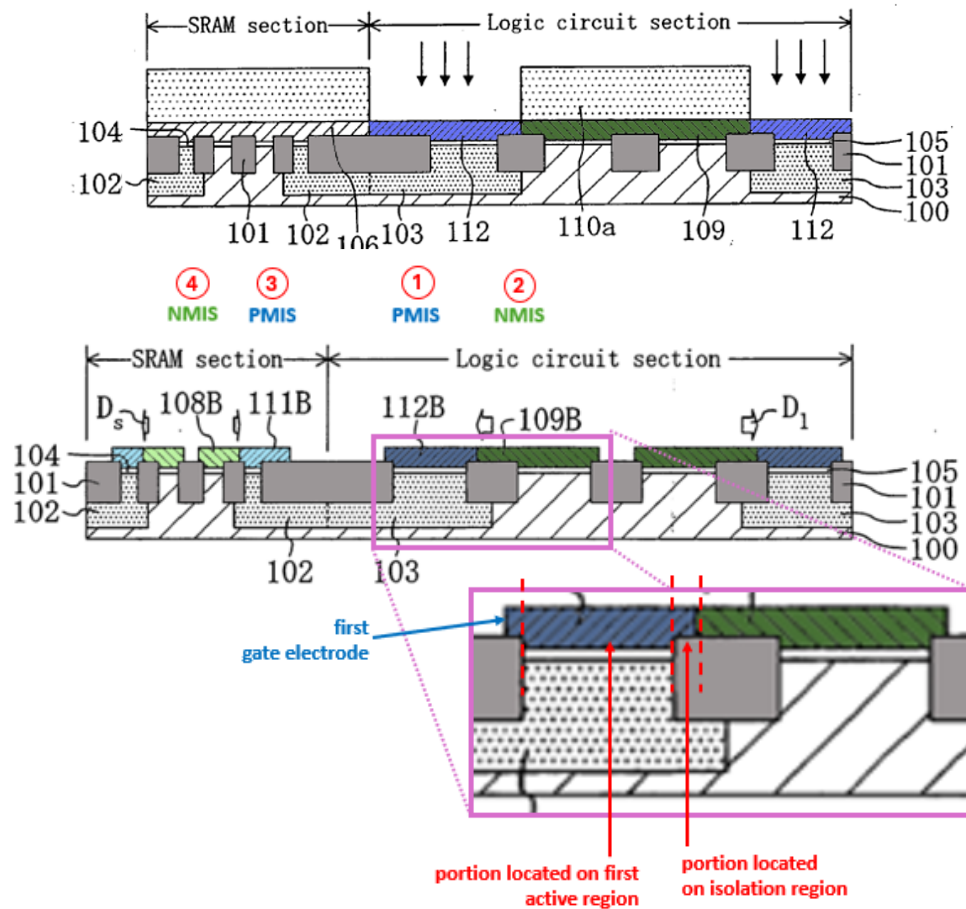
[8] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region.

161. The following table summarizes the impurity concentration relationship for claim 8 and Tamaki's impurity concentration relationship under the first embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$\text{LN}(\text{IR}) \approx \text{LN}(\text{AR}) > \text{SN}(\text{AR})$	$\text{LN}(\text{IR}, \text{AR}) > \text{SN}(\text{IR}, \text{AR})$
A-2	$\text{SN}(\text{IR}) \approx \text{SN}(\text{AR}) > \text{LN}(\text{AR})$	
B-1	$\text{LP}(\text{IR}) \approx \text{LP}(\text{AR}) > \text{SP}(\text{AR})$	$\text{LP}(\text{IR}, \text{AR}) > \text{SP}(\text{IR}, \text{AR})$
B-2	$\text{SP}(\text{IR}) \approx \text{SP}(\text{AR}) > \text{LP}(\text{AR})$	

162. Tamaki teaches that the logic PMOS gate electrode 112 is formed by uniformly implanting boron (p-type) across the polysilicon layer, using an energy of 5 keV and a dosage of 3×10^{15} atoms/cm².” (Tamaki, ¶85, Figures 1C, 3B).

163. That is, the implantation is carried out uniformly across the entire gate electrode film. Therefore, the impurity concentration of the portion of the first gate electrode over the first active region $\text{LP}(\text{AR})$ is substantially equal to that of the portion located over the isolation region $\text{LP}(\text{IR})$, or as illustrated with the shorthand notation: $\text{LP}(\text{AR}) \approx \text{LP}(\text{IR})$.



Tamaki, Figures 1C (top), 3B (bottom) with enlargement

164. Thus, Tamaki's first embodiment discloses "a portion of the first silicon film of the first conductivity type located on the first active region [LP(AR)] has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region [LP(IR)]," under Scenario B-1.

e. Claim 9

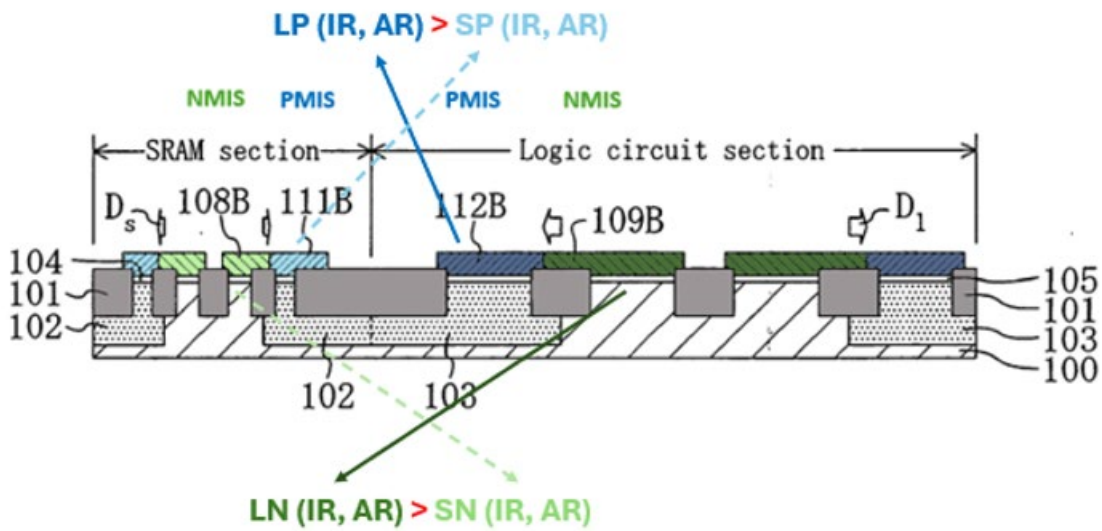
[9] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the

second silicon film of the first conductivity type located on the third active region.

165. The following table summarizes the impurity concentration relationship for claim 9 and Tamaki's impurity concentration relationship under the first embodiment:

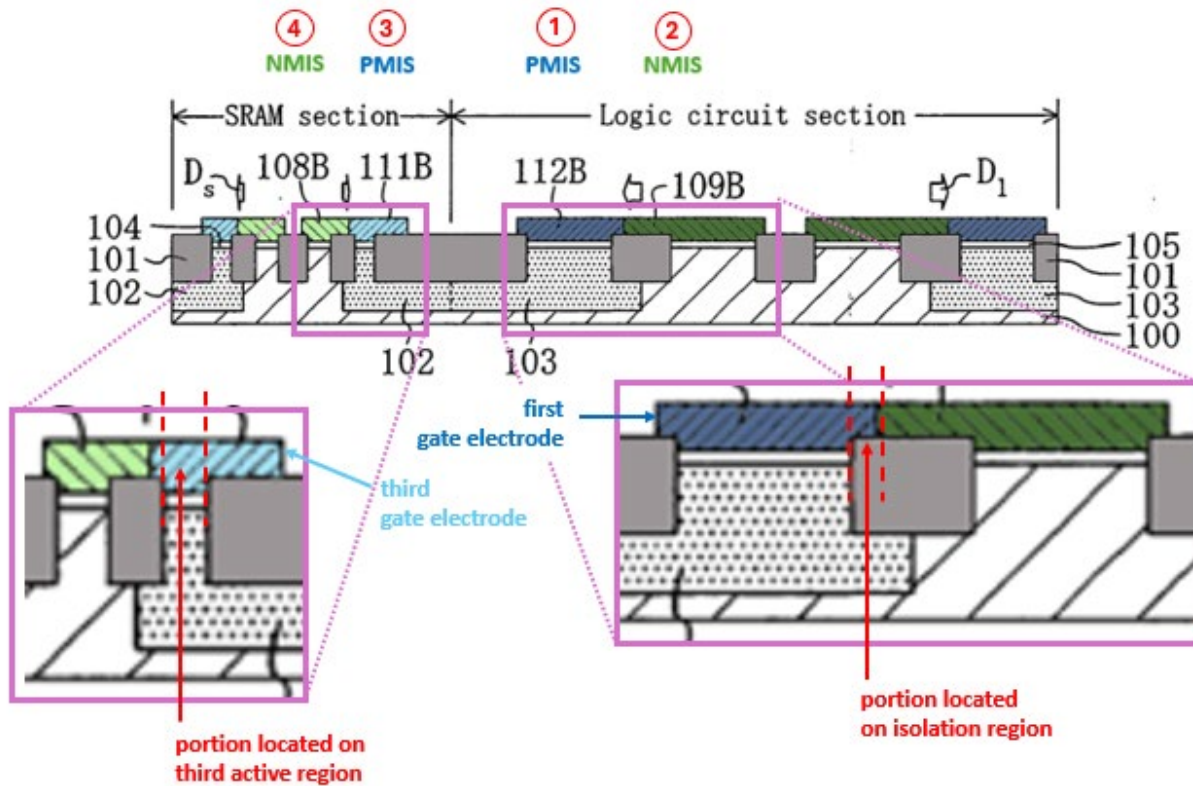
	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	LN(IR) > SN(AR)	LN(IR, AR) > SN(IR, AR)
A-2	SN(IR) > LN(AR)	
B-1	LP(IR) > SP(AR)	LP(IR, AR) > SP(IR, AR)
B-2	SP(IR) > LP(AR)	

166. As seen below in Figure 3B, the portion of electrode 112 over the isolation region, **LP(IR)**, (“*the first silicon film of the first conductivity type located on the isolation region*”) has a higher p-type impurity concentration (“*first-conductivity-type impurity concentration*”) than the portion of electrode 111 over the active region, **SP(AR)**, (“*the second silicon film of the first conductivity type located on the third active region*”). That is, **LP(IR) > SP(AR)** in Tamaki's first embodiment under scenario B-1.



Tamaki, Figure 3B

167. This relationship ($LP(IR) > SP(AR)$) is more clearly illustrated in Figure 3B below with the enlargements that identify the isolation region in the logic PMIS and the active region in the SRAM PMIS.



Tamaki, Figure 3B with enlargements

168. Accordingly, Tamaki discloses “a portion of the first silicon film of the first conductivity type located on the isolation region [LP(IR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SP(AR)],” in Tamaki’s first embodiment under scenario B-1.

f. Claim 12

[12P] The semiconductor device of claim 1, wherein

[12A] a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region, and

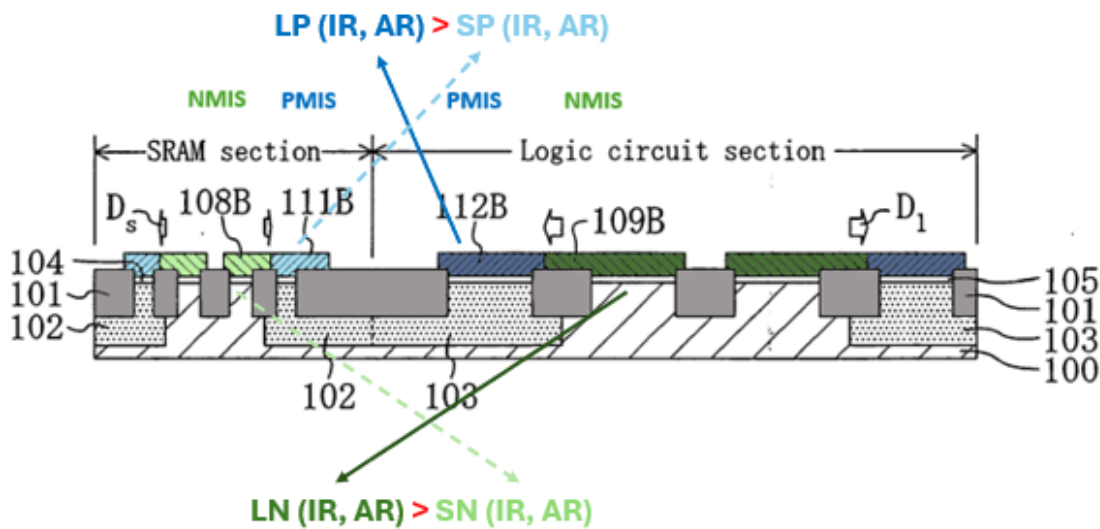
[12B] a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

169. The following table summarizes the impurity concentration relationship for claim 12 and Tamaki's impurity concentration relationship under the first embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$LN(AR) > SN(AR)$ $LP(AR) > SP(AR)$	
A-2	$SN(AR) > LN(AR)$ $SP(AR) > LP(AR)$	
B-1	$LP(AR) > SP(AR)$ $LN(AR) > SN(AR)$	$LP(IR, AR) > SP(IR, AR)$ $LN(IR, AR) > SN(IR, AR)$
B-2	$SP(AR) > LP(AR)$ $SN(AR) > LN(AR)$	

170. As seen in Figure 3B (below), the portion of electrode 112 over the active region, $LP(AR)$, (“the first silicon film of the first conductivity type located on the first active region”) has a higher p-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 111 over the active region, $SP(AR)$, (“the second silicon film of the first conductivity type located on the third active region”) and the portion of electrode 109 over the active

region, **LN(AR)**, (“the first silicon film of the second conductivity type located on the second active region”) has a higher n-type impurity concentration (“second-conductivity-type impurity concentration”) than the portion of electrode 108 over the active region, **SN(AR)**. That is, **LP(AR) > SP(AR)** and **LN(AR) > SN(AR)** in Tamaki’s first embodiment under scenario B-1.



Tamaki, Figure 3B

171. Accordingly, Tamaki discloses “a portion of the first silicon film of the first conductivity type located on the first active region [**LP(AR)**] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [**SP(AR)**],” and “a portion of the first silicon film of the second conductivity type located on the second active region [**LN(AR)**] has a second-conductivity-type

impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region [SN(AR)].”

g. Claims 13-14

[13] The semiconductor device of claim 1, wherein

[13A] the first gate electrode is a gate electrode of a first PMIS transistor,

[13B] the second gate electrode is a gate electrode of a first NMIS transistor,

[13C] the third gate electrode is a gate electrode of a second PMIS transistor, and

[13D] the fourth gate electrode is a gate electrode of a second NMIS transistor.

[14] The semiconductor device of claim 1, wherein

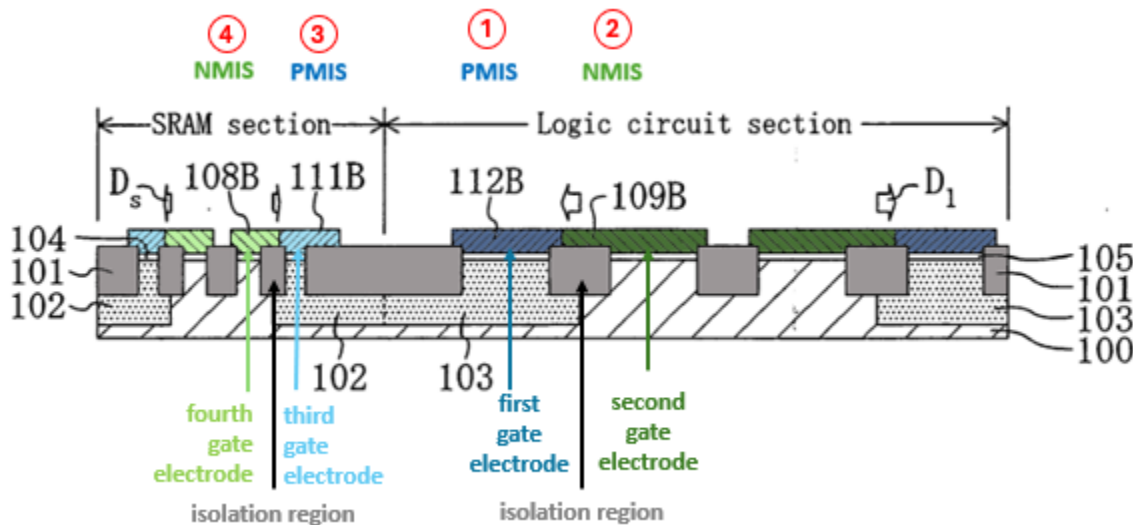
[14A] each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and

[14B] each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit.

172. Tamaki expressly states that logic **PMIS transistor** includes **gate 112B**; logic **NMIS transistor** includes **gate 109B**; SRAM **PMIS transistor** includes **gate electrode 111B**; SRAM **NMIS transistor** includes **gate 108B** (Tamaki, ¶103). Accordingly, the first and second gate electrodes (112B and 109B) correspond to the PMIS and NMIS transistors in the logic circuit section,

respectively, while the third and fourth gate electrodes (111B and 108B) correspond to the PMIS and NMIS transistors in the SRAM section.

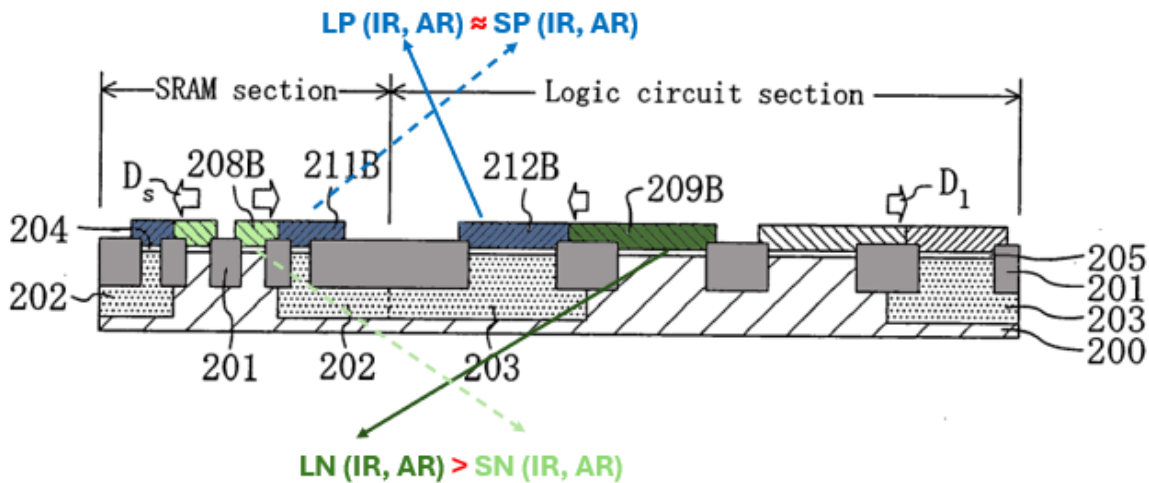
173. Therefore, Tamaki's first embodiment discloses "*the first gate electrode is a gate electrode of a first PMIS transistor, the second gate electrode is a gate electrode of a first NMIS transistor, the third gate electrode is a gate electrode of a second PMIS transistor, and the fourth gate electrode is a gate electrode of a second NMIS transistor*" [13] and "*each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit*" [14] under Scenario B-1.



Tamaki, Figure 3B

C. Tamaki's Second Embodiment Under Scenario A-1

174. Tamaki's second embodiment device includes a logic circuit section and SRAM section as shown in Figure 5B (below). The logic section includes n-type gate electrode 209B (dark green) and p-type gate electrode 212B (blue). (Tamaki, ¶136.) The SRAM section of Tamaki's second embodiment includes n-type gate electrode 208B (light green) and p-type gate electrode 211B (blue). (Tamaki, ¶136, Figure 5B (below).)



Tamaki, Figure 5B

1. P-type Impurity Concentrations

175. Tamaki discloses that “the p-type impurity implantation (third p-type impurity implantation) with respect to the SRAM section p-type gate electrode film 211 and the p-type impurity implantation (fourth p-type impurity implantation) with respect to the logic circuit section p-type gate electrode formation film 212

are performed under the conditions of for example, **an implantation energy of 5 keV and dosage of 3×10^{15} atoms/cm².**” (Tamaki, ¶119.)

176. That is, the implantation conditions (energy and dopant dosage) are the same for the entire gate electrode of the logic PMIS and the entire gate electrode of the SRAM PMIS. Because both PMIS gate electrodes receive the same implant conditions, their resulting boron concentrations are substantially equivalent.

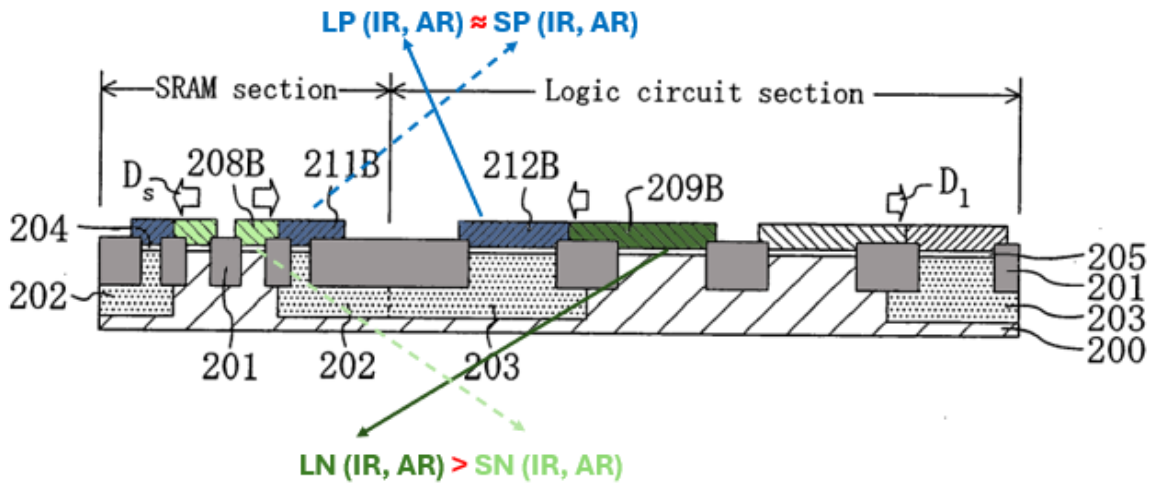
2. N-type Impurity Concentrations

177. Tamaki discloses that the “SRAM section n-type gate electrode 208B has phosphorous concentration **lower than** the logic circuit section n-type gate electrode 209B” (Tamaki, ¶138, Figure 5B.)

178. Importantly, Tamaki confirms that each gate electrode receives uniform doping across both the active and isolation region, i.e., implantation is not selectively masked.

179. The above impurity concentration relationship, illustrated in Figure 3B below, can be expressed as follows:

Tamaki’s Second Embodiment
LP (IR, AR) $\approx$ SP (IR, AR)
LN (IR, AR) $>$ SN (IR, AR)



Tamaki, Figure 5B

180. As I discussed in §IV.D, the independent claims encompass at least the following four scenarios:

Claim Language		Scenarios Covered			
		A-1	A-2	B-1	B-2
<i>first dual-gate electrode</i>	<i>first gate electrode</i>	logic NMOS	SRAM NMOS	logic PMOS	SRAM PMOS
	<i>second gate electrode</i>	logic PMOS	SRAM PMOS	logic NMOS	SRAM NMOS
<i>second dual-gate electrode</i>	<i>third gate electrode</i>	SRAM NMOS	logic NMOS	SRAM PMOS	logic PMOS
	<i>fourth gate electrode</i>	SRAM PMOS	logic PMOS	SRAM NMOS	logic NMOS

181. Tamaki's second embodiment renders claims 1-4, 8-9, 11, and 14 obvious under Scenario A-1.

1. Independent Claim 1

a. Preamble [1P]

[1P] *A semiconductor device, comprising:*

182. Tamaki discloses a “*semiconductor device*” that includes both a logic circuit section and an SRAM section. (Tamaki, ¶¶2, 82, 104, 115, Figure 5B, claim 1.)

b. “First Dual-Gate Electrode” Limitations [1A], [1C], [1E]-[1F]

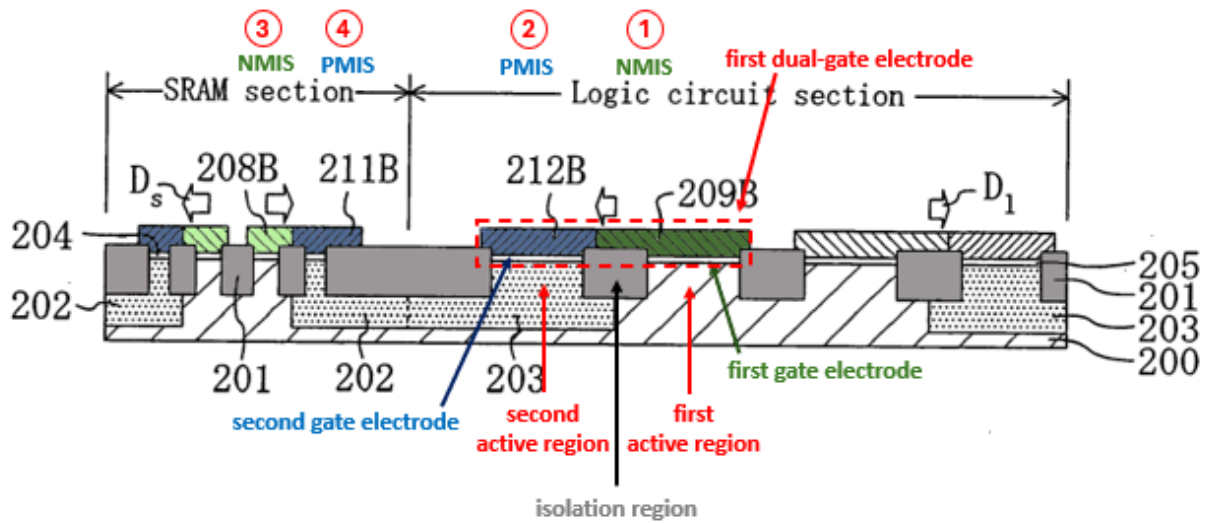
[1A] *a first dual-gate electrode; and*

[1C] *the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,*

[1E] *the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,*

[1F] *the first gate electrode and the second gate electrode are connected to each other on the isolation region, and*

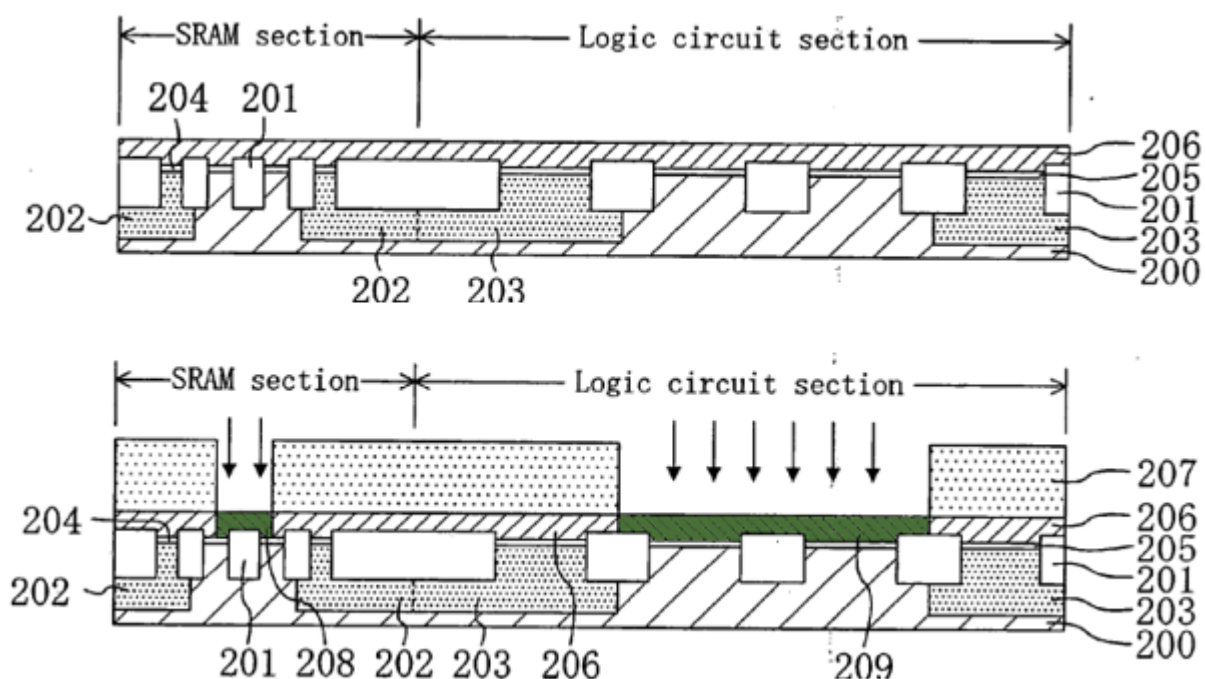
183. Tamaki states that logic NMIS gate electrode 209A is formed integrally with the logic PMIS gate electrode 212A, forming the “*first dual-gate electrode*” [1A]. (See, Tamaki, ¶131, Figure 5B (below), claim 2.)



Tamaki, Figure 5B

184. Isolation region 201, comprised of buried silicon oxide, separates the n-type and p-type active regions in the logic circuit (Tamaki ¶116), satisfying limitation [1E]. Tamaki refers to each “element formation region” as an “active region.” (Tamaki ¶117.)

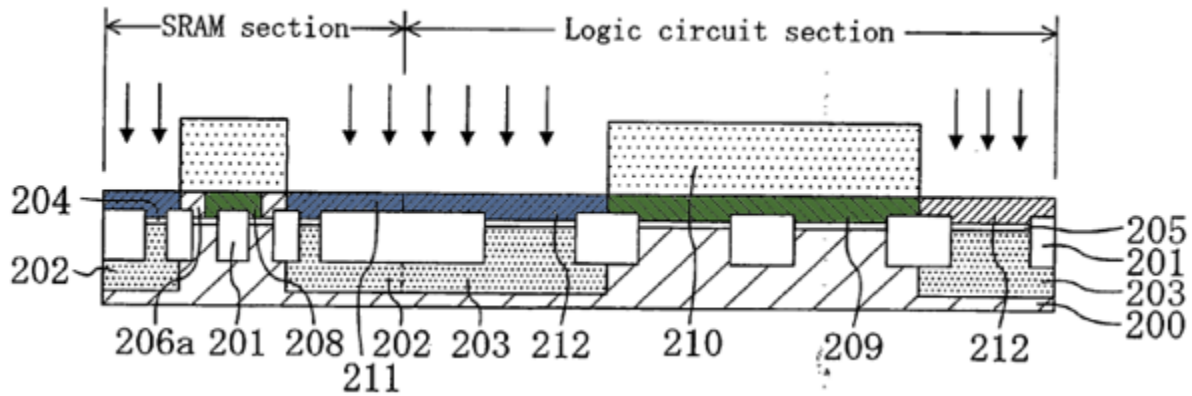
185. Gate insulating film 205 “is formed” over the active regions of the logic section, followed by gate electrode formation film 206 (**polysilicon**) across the substrate. (Tamaki, ¶117, Figure 4A (below-top).)



Tamaki, Figures 4A(top), 4B(bottom)

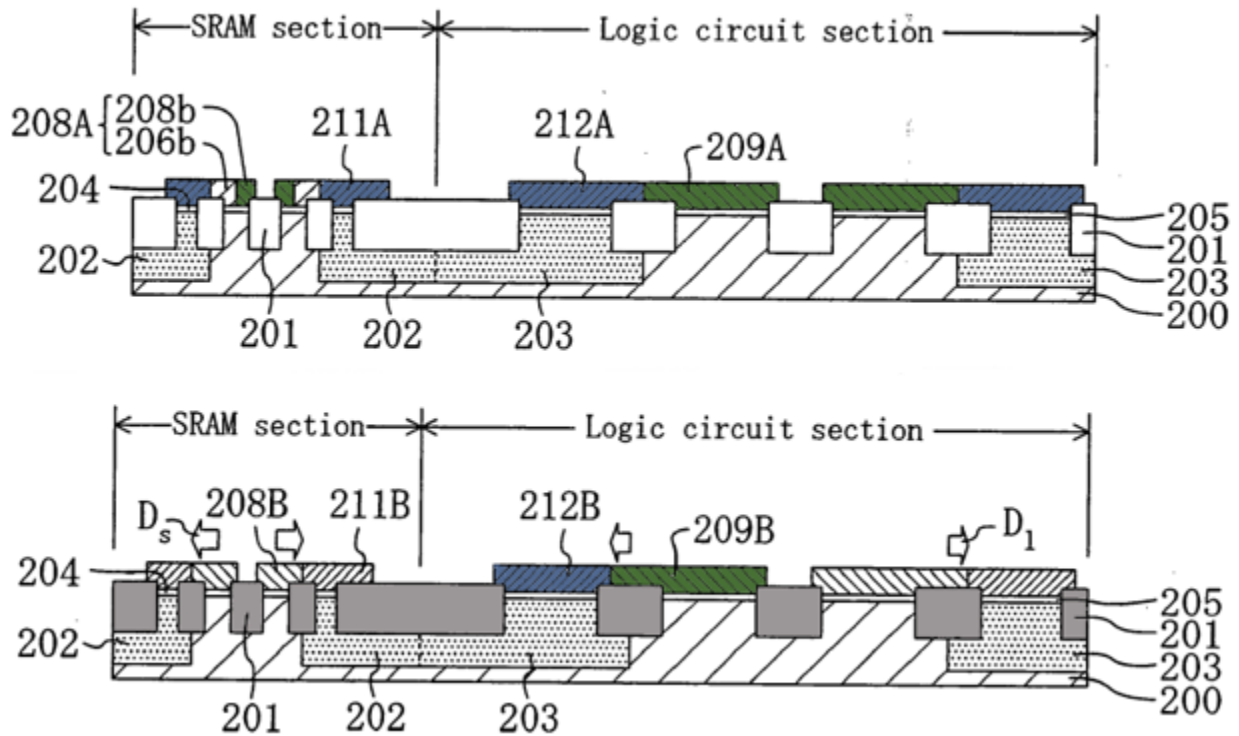
186. An n-type impurity (e.g., phosphorous) is implanted into the gate film 206 over the logic NMIS region, forming gate electrode film 209 -- “a first silicon film of a first conductivity type [**n-type**]. (Tamaki, ¶118, Figure 4B (above-bottom).)

187. A p-type impurity (e.g., boron) is implanted into the gate film 206 over the logic PMIS region forming the gate electrode formation film 212 -- “a first silicon film of a second conductivity type [**p-type**].” (Tamaki, ¶119, Figure 4C (below).)



Tamaki, Figure 4C

188. Patterning the films produces logic NMOS gate 209A and logic PMOS gate 212A. As shown in Figs. 5A and 5B, NMOS gate 209A (209B in Fig. 5B) lies over the first active region, and PMOS gate 212A (212B) lies over the second active region. This satisfies [1C].



Tamaki, Figures 5A (top), 5B (bottom)

189. Tamaki further confirms that **the pn boundary** between the logic NMIS gate 209B [green] and the logic PMIS gate 212B [blue] **is located directly over isolation region 201**. (Tamaki, ¶136.) Hence, “*the first gate electrode and the second gate electrode are connected to each other on the isolation region,*” satisfying [1F].

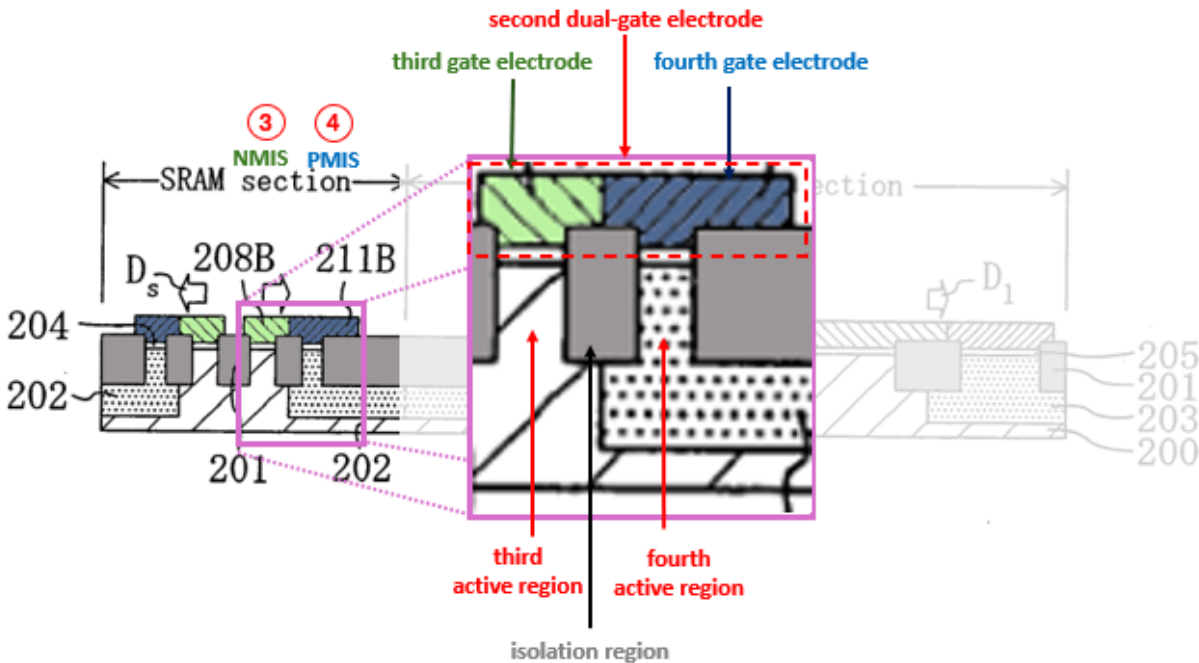
c. “Second Dual-Gate Electrode” Limitations [1B], [1D]

[1B] *a second dual-gate electrode being separated from the first dual-gate electrode, wherein*

[1D] *the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity*

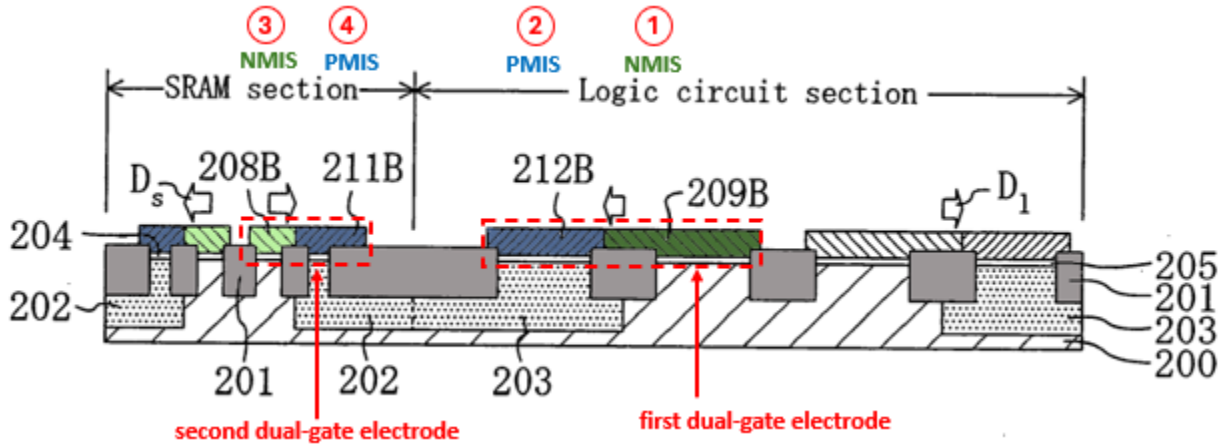
type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,

190. In the SRAM section, Tamaki states that n-type gate electrode 208A (“third gate electrode”) “is **formed integrally** with” p-type gate electrode 211A (“fourth gate electrode”), satisfying limitation [1B]. (Tamaki, ¶131, Figure 5B, claim 2.)



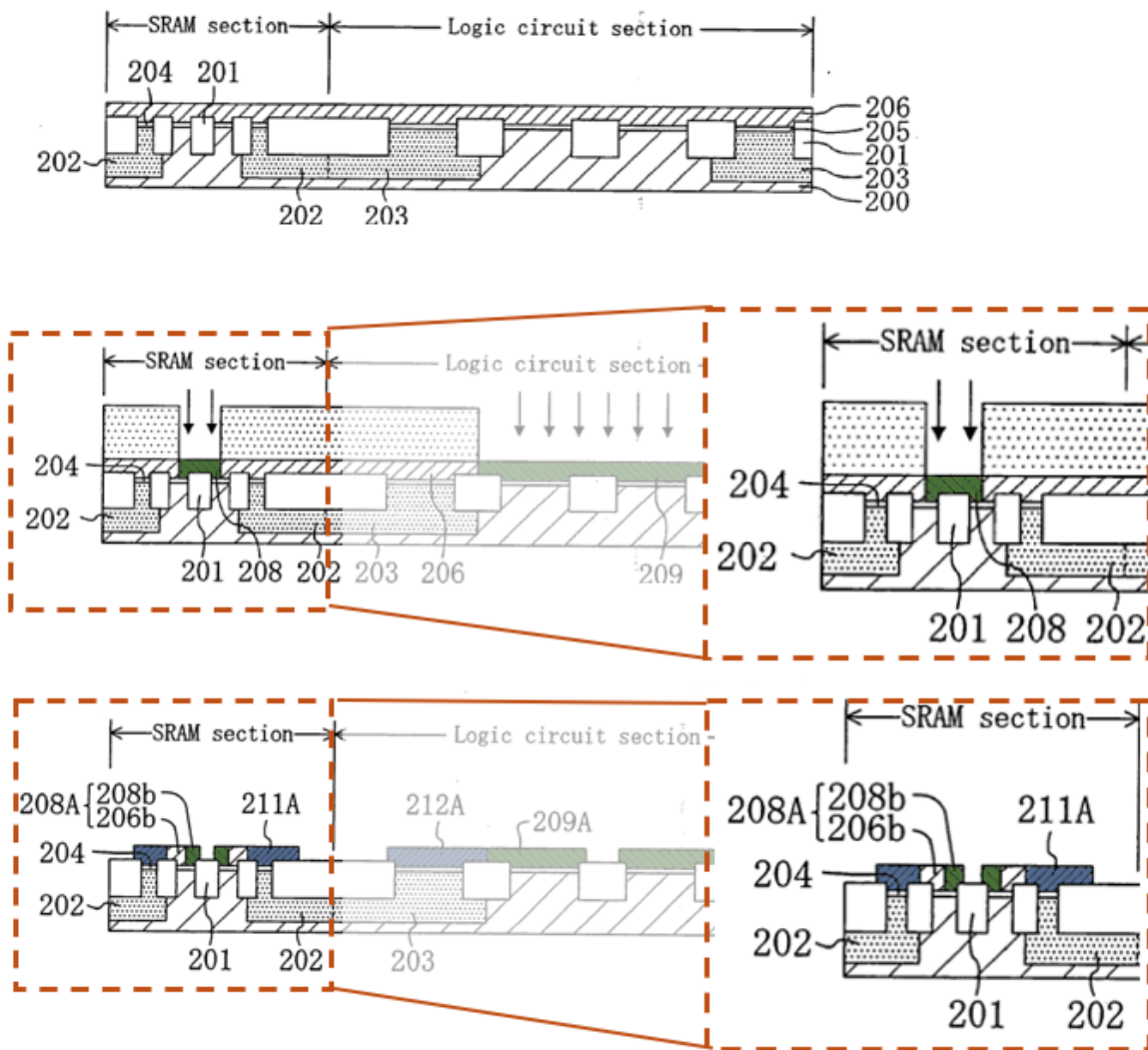
Tamaki, Figure 5B with enlargement

191. As shown in Figure 5B, this dual-gate SRAM structure is physically separated from the logic dual-gate electrode, further satisfying limitation [1B] (See, e.g., Tamaki, ¶¶130-131 (discussing patterning of SRAM and logic gate electrodes.)



192. The SRAM NMOS and PMOS gates sit on distinct active regions separated by isolation region 201 (Tamaki, ¶116), where each element formation region again corresponds to an “*active region*.” (Tamaki, ¶117.)

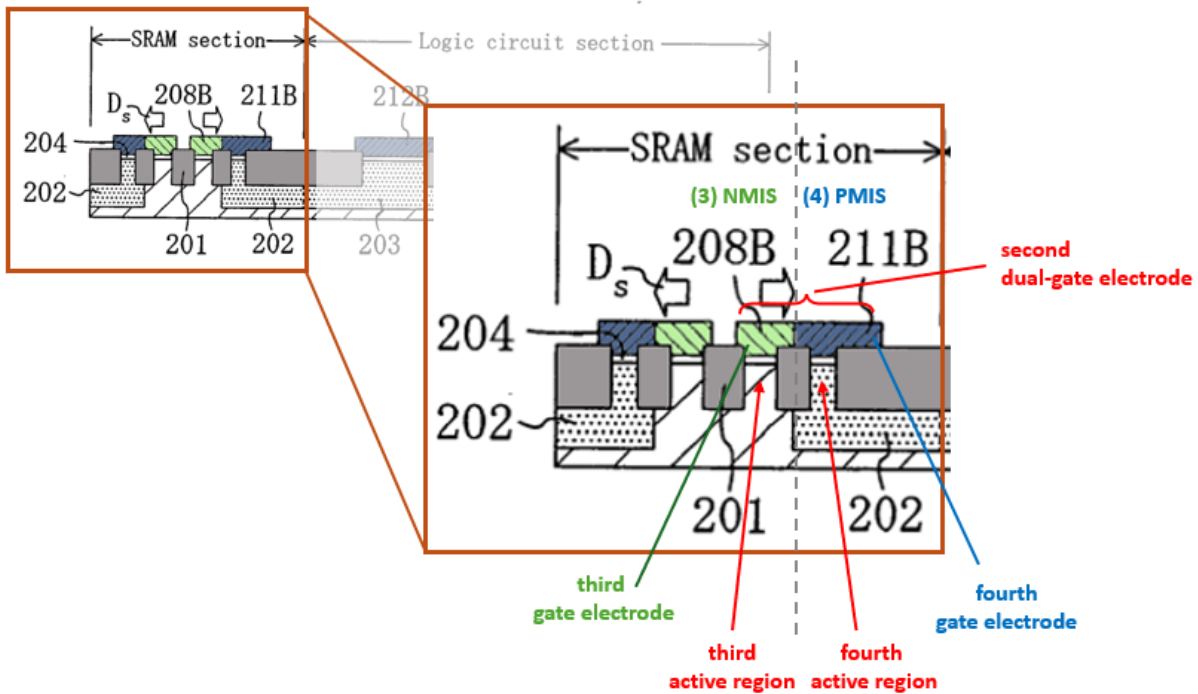
193. Gate insulating film 204 is formed across the SRAM active regions, followed by blanket deposition of gate film 206. The n-type implant is selectively applied to form doped region 208b (Fig. 4B), while part of the gate remains undoped (region 206b). (Tamaki, ¶118, Figure 4B (below-middle), Figure 5A (below-bottom).)



**Tamaki, Figures 4A(top), 4B(middle) with enlargement,
5A(bottom) with enlargement**

194. The p-type implant is applied across the SRAM PMIS region to the (Tamaki, ¶119, Figure 4C, 5A (above-bottom)(shaded blue).), forming gate film 211. After patterning, gate electrode 208A (n-type) and gate electrode 211A (p-type) are created, completing the second dual-gate. Gate electrode 211A “*fourth gate electrode*” (labeled 211B in Figure 5B) lies over “[*the*] *fourth active region*

[p-type MIS element formation region]” and gate 208B over the *third active region*.



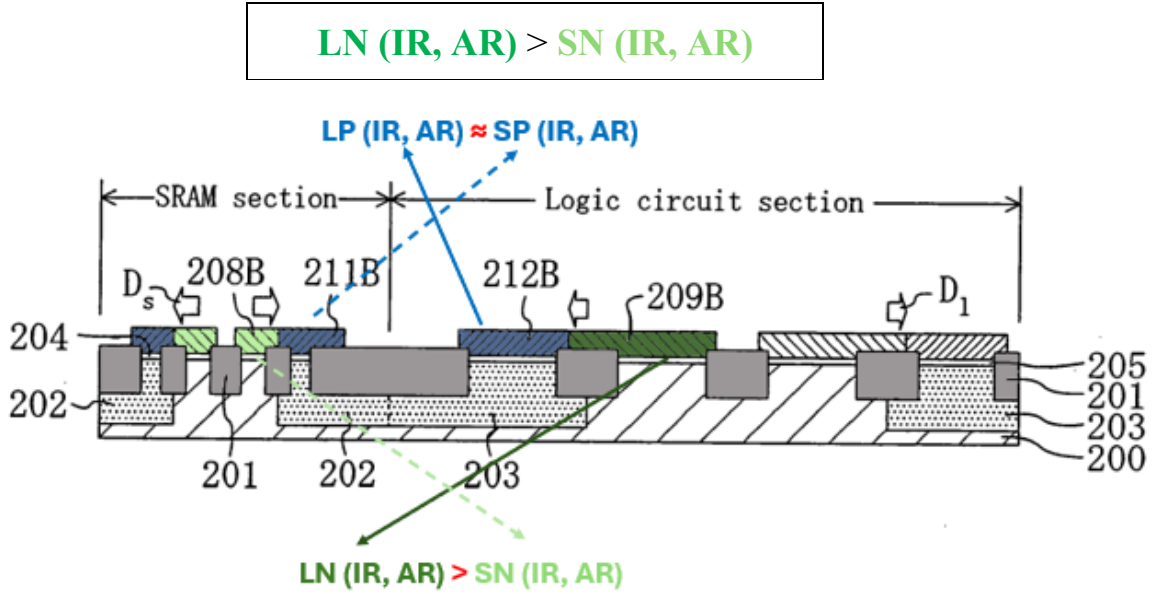
Tamaki, Figure 5B with enlargement

d. Impurity Concentration Limitations [1G]

[1G] at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

195. The impurity concentration relationship of Tamaki’s second embodiment, discussed in §V.C.2, is summarized below:

Tamaki’s Second Embodiment
$LP (IR, AR) \approx SP (IR, AR)$



Tamaki, Figure 5B

196. Tamaki's second embodiment therefore discloses “*at least a portion of the first silicon film of the first conductivity type [LN (IR, AR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SN (AR)]*” under scenario A-1.

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	LN(IR, AR) > SN(AR)	LN(IR, AR) > SN(IR, AR)
A-2	SN(IR, AR) > LN(AR)	
B-1	LP(IR, AR) > SP(AR)	
B-2	SP(IR, AR) > LP(AR)	

e. Second Embodiment Under Scenario A-1 Summary

<i>“first dual gate electrode”</i>	<i>“a first gate electrode”</i>	Logic-NMIS gate electrode 209
	<i>“a second gate electrode”</i>	Logic-PMIS gate electrode 212
<i>“second dual gate electrode”</i>	<i>“a third gate electrode”</i>	SRAM-NMIS gate electrode 208
	<i>“a fourth gate electrode”</i>	SRAM-PMIS gate electrode 211
impurity concentration relationship relied on		LN (IR, AR) > SN (AR)

2. Claim 2

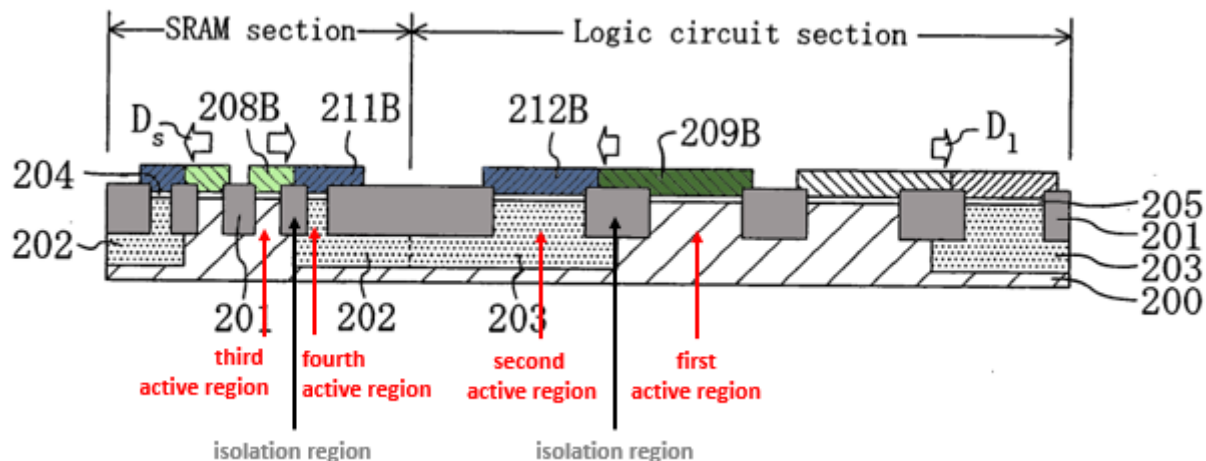
[2] The semiconductor device of claim 1, wherein an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.

197. Tamaki’s second embodiment discloses “an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region” under Scenario A-1.

198. Tamaki’s second embodiment states that the “width in the gate width direction of an element isolation region 201, which separates an element formation region of a SRAM section n-type MIS transistor [*“third active region”*] and an element formation region of a SRAM section p-type MIS transistor [*“fourth active region”*], is **smaller than** the width in the gate width direction of an element isolation region 201, which separates an element formation region of a logic circuit section n-type MIS transistor [*“first active region”*] and an element formation region of a logic circuit section p-type MIS transistor [*“second active region”*].”

(Tamaki, ¶116, Figure 5B (below).) In other words, the STI between the NMIS and PMIS in the SRAM section is narrower than that in the logic section.

199. A POSITA would have expected this distinction: *transistors in the SRAM region are packed more densely than those in the logic region.* (See, e.g., Igarashi, ¶4 (“the size of the memory cell which forms SRAM is wanted to be reduced more.”); Tamaki, ¶29 (“[I]n the SRAM section... is comparatively small in width of the element isolation ...”); Zampaglione, 3:58-64 (“... bit cells provided by the foundries utilize design rules that are tighter than ... random transistors elsewhere...”)).



Tamaki, Figure 5B

3. Claims 3 and 11

[3] The semiconductor device of claim 1, wherein at least a portion of the first silicon film of the second conductivity type has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

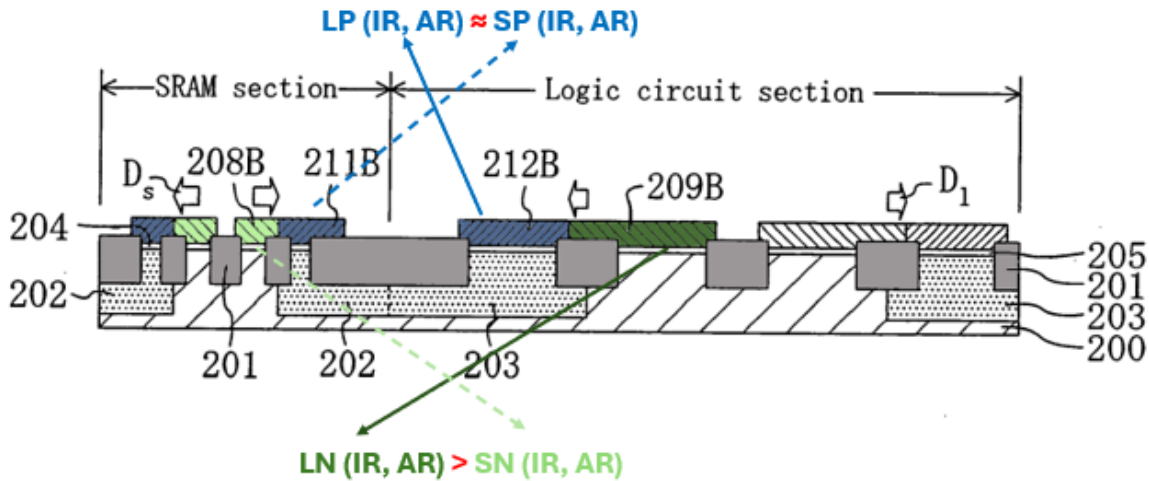
[11] The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

200. The following table summarizes the impurity concentration relationship for claims 3 and 11 and Tamaki's impurity concentration relationship under the second embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$\text{LN}(\text{IR}, \text{AR}) > \text{SN}(\text{AR})$ $\text{LP}(\text{IR}, \text{AR}) \approx \text{SP}(\text{AR})$	$\text{LN}(\text{IR}, \text{AR}) > \text{SN}(\text{IR}, \text{AR})$ $\text{LP}(\text{IR}, \text{AR}) \approx \text{SP}(\text{IR}, \text{AR})$
A-2	$\text{SN}(\text{IR}, \text{AR}) > \text{LN}(\text{AR})$ $\text{SP}(\text{IR}, \text{AR}) \approx \text{LP}(\text{AR})$	
B-1	$\text{LP}(\text{IR}, \text{AR}) > \text{SP}(\text{AR})$ $\text{LN}(\text{IR}, \text{AR}) \approx \text{SN}(\text{AR})$	
B-2	$\text{SP}(\text{IR}, \text{AR}) > \text{LP}(\text{AR})$ $\text{LN}(\text{IR}, \text{AR}) \approx \text{SN}(\text{AR})$	

201. As seen in Figure 5B (below), the portion of electrode 212 over the active region, **LP (AR)** (“at least a portion of the first silicon film of the second conductivity type”) has a substantially equal p-type impurity concentration (“second-conductivity-type impurity concentration”) to the portion of electrode 211 over the active region, **SP (AR)** (“the second silicon film of the second conductivity

type located on the fourth active region”). That is, $LP(AR, IR) \approx SP(AR)$ in Tamaki’s second embodiment under scenario A-1.



Tamaki, Figure 5B

202. Accordingly, Tamaki’s second embodiment discloses claims 3 and 11 under Scenario A-1.

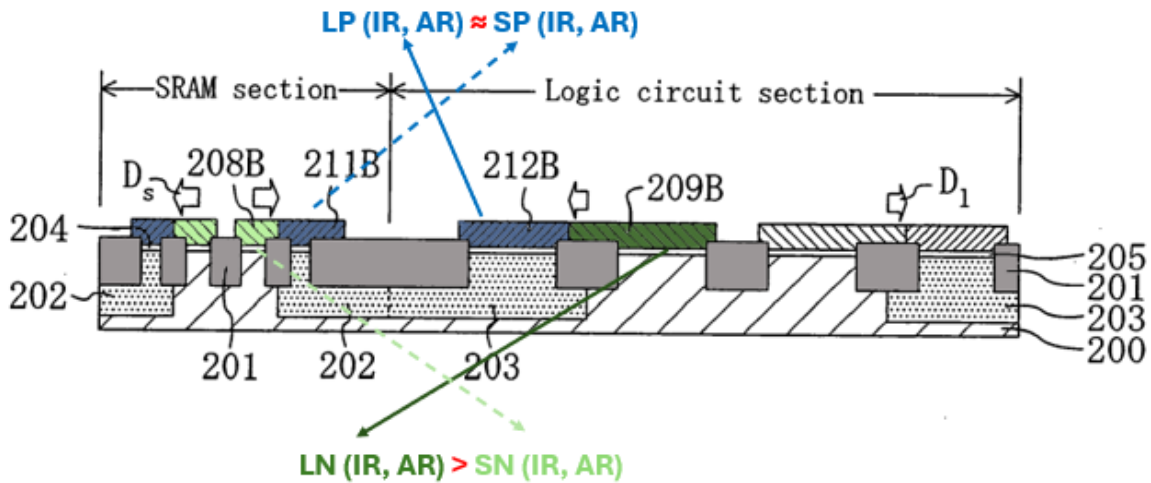
4. Claim 4

[4] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

203. The following table summarizes the impurity concentration relationship for claim 4 and Tamaki’s impurity concentration relationship under the second embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$LN(AR) > SN(AR)$	$LN(IR, AR) > SN(IR, AR)$ $LP(IR, AR) \approx SP(IR, AR)$
A-2	$SN(AR) > LN(AR)$	
B-1	$LP(AR) > SP(AR)$	
B-2	$SP(AR) > LP(AR)$	

204. As seen in Figure 5B, the portion of electrode 209 over the active region, $LN(AR)$, (“the first silicon film of the first conductivity type located on the first active region”) has a higher n-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 208 over the active region, $SN(AR)$, (“the second silicon film of the first conductivity type located on the third active region”). That is, $LN(AR) > SN(AR)$ in Tamaki’s second embodiment under scenario A-1.



Tamaki, Figure 5B

205. Accordingly, Tamaki’s first embodiment discloses “a portion of the first silicon film of the first conductivity type located on the first active region [LN(AR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SN(AR)]” under scenario A-1.

5. Claim 8

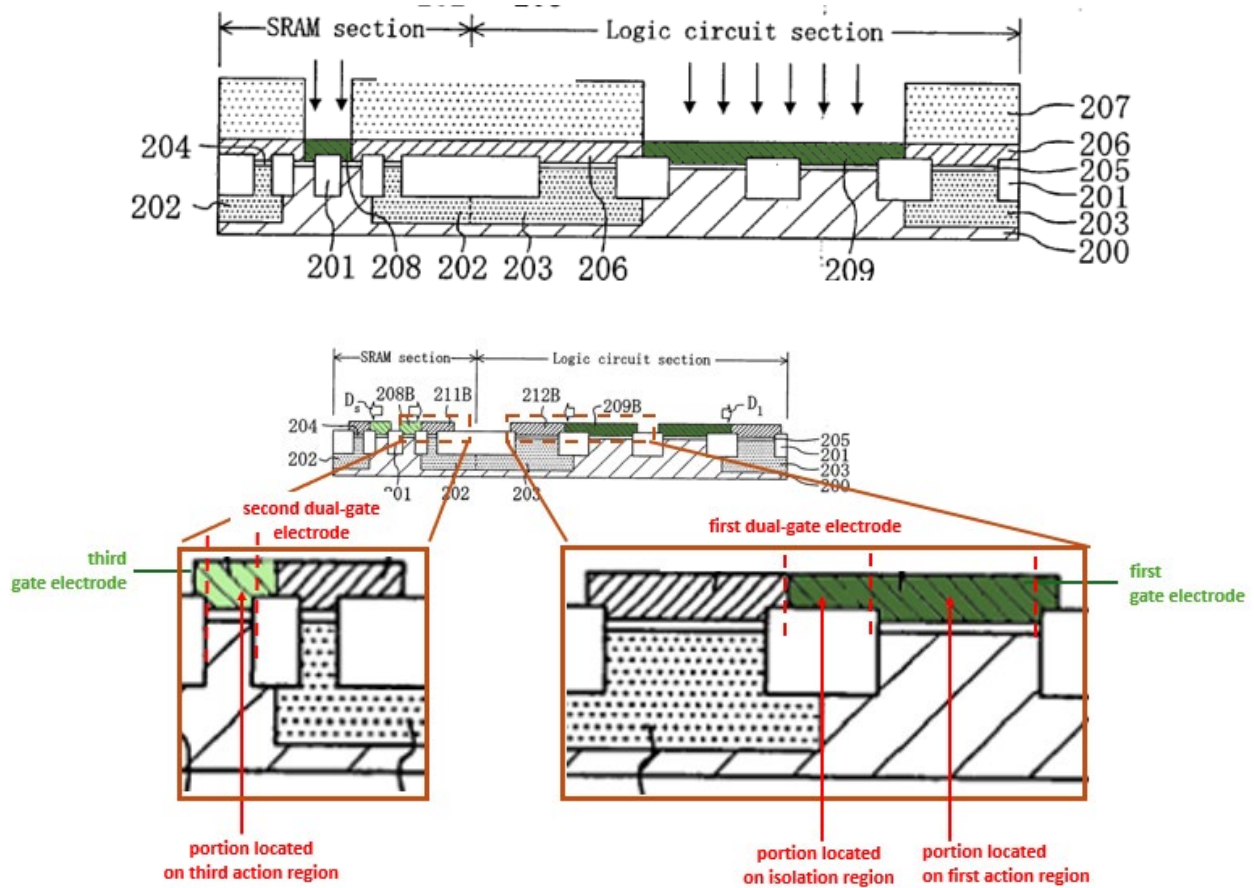
[8] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region.

206. The following table summarizes the impurity concentration relationship for claim 4 and Tamaki’s impurity concentration relationship under the second embodiment:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$\text{LN}(\text{IR}) \approx \text{LN}(\text{AR}) > \text{SN}(\text{AR})$	$\text{LN}(\text{IR}, \text{AR}) > \text{SN}(\text{IR}, \text{AR})$ $\text{LP}(\text{IR}, \text{AR}) \approx \text{SP}(\text{IR}, \text{AR})$
A-2	$\text{SN}(\text{IR}) \approx \text{SN}(\text{AR}) > \text{LN}(\text{AR})$	
B-1	$\text{LP}(\text{IR}) \approx \text{LP}(\text{AR}) > \text{SP}(\text{AR})$	
B-2	$\text{SP}(\text{IR}) \approx \text{SP}(\text{AR}) > \text{LP}(\text{AR})$	

207. As seen in Figure 4B (below-top), in Tamaki’s second embodiment, “an n-type impurity, for example, phosphorous or the like is implanted to ... the gate electrode formation film 206 on the n-type MIS formation region in the logic circuit section.” (See, e.g., Tamaki, ¶118; see also, Tamaki, Figures 4B-5B (below-bottom).) Tamaki explains that the n-type impurity implantation “with respect to the logic circuit section n-type gate electrode formation film 209 [is] performed under the conditions of, for example, an implantation energy of 10 keV and a dosage of 8×10^{15} atoms/cm².” (Tamaki, ¶118.)

208. That is, the implantation is carried out uniformly across the entire gate electrode film in a single process step. Therefore, the impurity concentration of the portion of the first gate electrode over the first active region (**$\text{LN}(\text{AR})$**) is substantially equal to that of the portion located over the isolation region (**$\text{LN}(\text{AR})$**) or as illustrated with the shorthand notation: **$\text{LN}(\text{AR}) \approx \text{LN}(\text{IR})$** .



Tamaki, Figures 4B (top), 5B (bottom) with enlargements

209. Thus, Tamaki's second embodiment discloses “a portion of the first silicon film of the first conductivity type located on the first active region [LN(AR)] has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region [LN(IR)],” under scenario A-1.

6. Claim 9

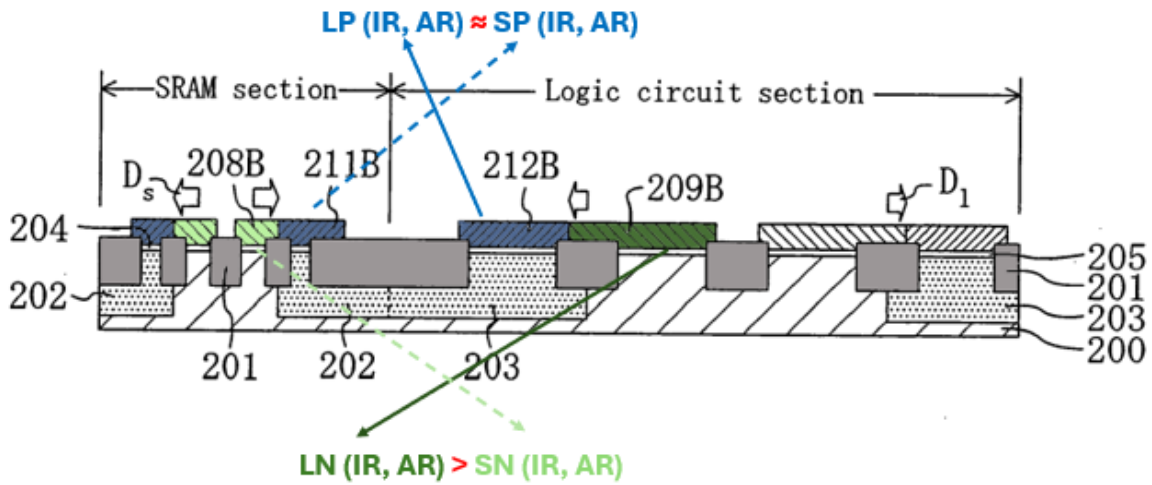
[9] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the

second silicon film of the first conductivity type located on the third active region.

210. The following table summarizes the impurity concentration relationship for claim 9 and Tamaki's impurity concentration relationship under the second embodiment:

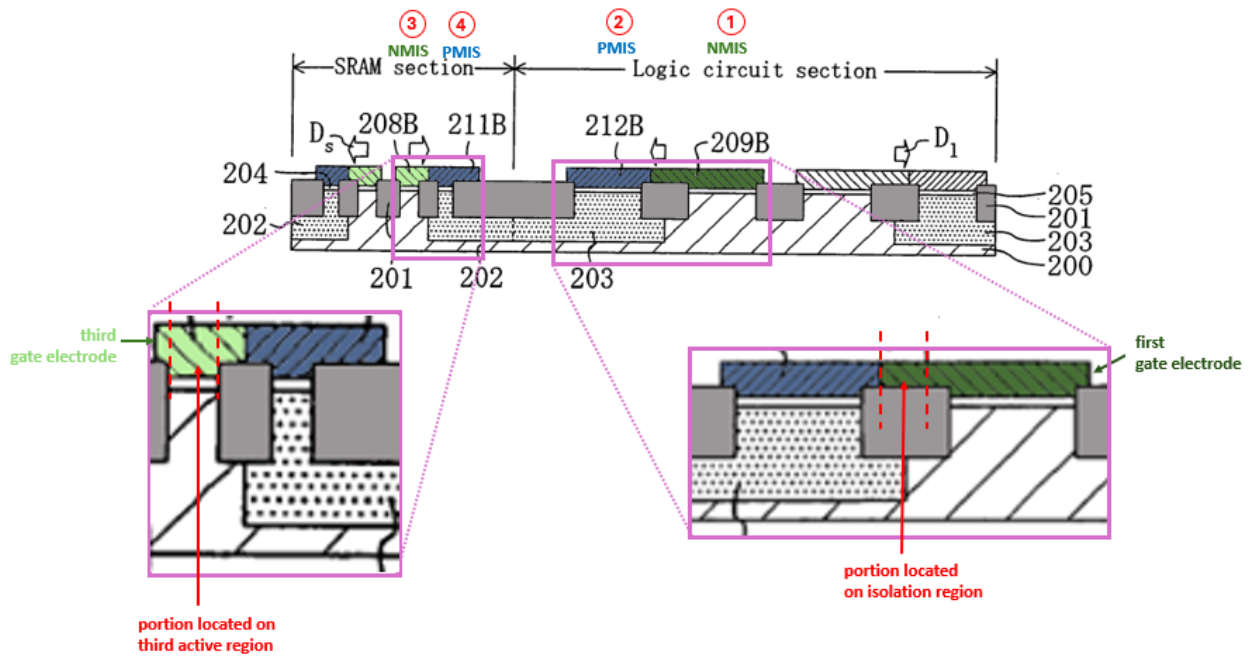
	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	LN(IR) > SN(AR)	LN(IR, AR) > SN(IR, AR)
A-2	SN(IR) > LN(AR)	
B-1	LP(IR) > SP(AR)	LP(IR, AR) > SP(IR, AR)
B-2	SP(IR) > LP(AR)	

211. As seen below in Figure 5B, the portion of electrode 209 over the isolation region, **LN(IR)**, (“the first silicon film of the first conductivity type located on the isolation region”) has a higher n-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 208 over the active region, **SP(AR)**, (“the second silicon film of the first conductivity type located on the third active region”). That is, **LN(IR) > SP(AR)** in Tamaki's second embodiment under scenario A-1.



Tamaki, Figure 5B

212. This relationship ($LN(IR) > SN(AR)$) is more clearly illustrated in Figure 3B below with the enlargements that identify the isolation region in the logic NMIS and the active region in the SRAM NMIS.



Tamaki, Figure 5B with enlargements

213. Accordingly, Tamaki discloses “a portion of the first silicon film of the first conductivity type located on the isolation region [LN(IR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SN(AR),” in Tamaki’s second embodiment under scenario A-1.

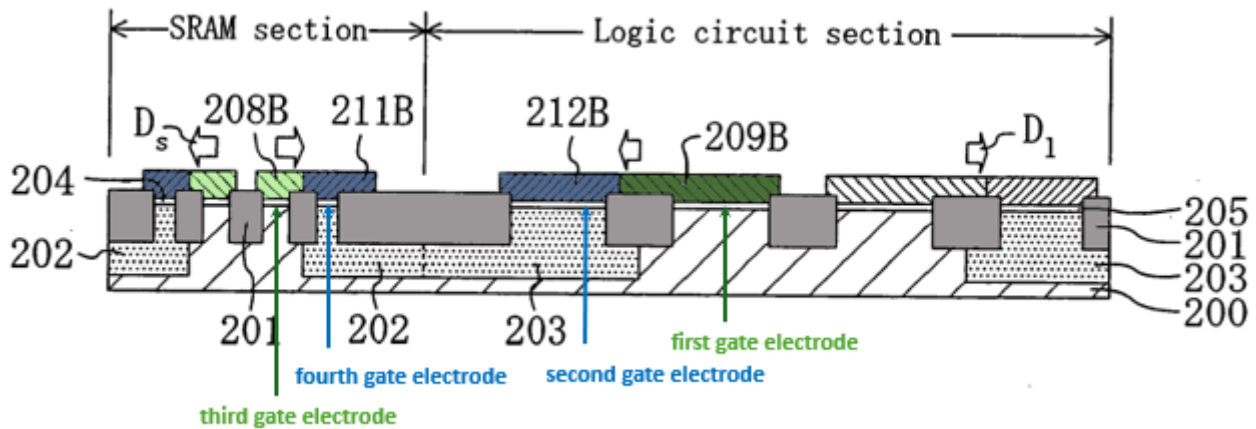
7. Claim 14

[14] The semiconductor device of claim 1, wherein

[14A] each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and

[14b] each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit.

214. Tamaki’s second embodiment device includes an SRAM circuit and a logic circuit, each with corresponding gate electrodes. The SRAM circuit includes n-type gate electrode 208B [*“third gate electrode”*] and p-type gate electrode 211B [*“fourth gate electrode”*], while the logic circuit includes n-type gate electrode 209B [*“first gate electrode”*] and p-type gate electrode 212B [*“second gate electrode”*].” (Tamaki, ¶136.)



Tamaki, Figure 5B

VI. GROUND 2: The Combination of Tamaki and Sumi Renders Claims 5 and 7 Obvious

215. Tamaki does not explicitly disclose a dual-gate electrode having a portion of the silicon film located on an isolation region with a higher impurity concentration than the impurity concentration of a portion of the silicon film located on an active region, as recited in claims 5 and 7. Sumi provides this teaching.

B. The Tamaki and Sumi Combination

1. Mutual Dopant Diffusion in Dual-Gate Structures

216. Tamaki recognized the issues posed by mutual dopant diffusion in its dual-gate electrodes. Specifically, Tamaki noted that due to downstream thermal processing, such as during activation annealing of the source/drain regions, “phosphorous in the SRAM section n-type gate electrode [] and the boron in the SRAM section p-type gateelectrote de [] diffuse mutually in the integrally-formed n-

type and p- type gate electrodes” and “phosphorous in the logic circuit section n-type gate electrode [] and the boron in the logic circuit section p-type gate electrode [] diffuse mutually in the integrally-formed n-type and p- type gate electrodes.” (Tamaki, ¶22.) Consequently, the pn boundary between the n-type gate electrode and the p-type gate electrode “shifts over the element isolation region [] to reach a point on the ... gate insulating film [] located on the ... n-type well region [] [i.e., the active region].” (Tamaki, ¶27.) This shifting of the location of the pn boundary “disables securing of the transistor characteristics” (Tamaki, ¶27) of the p-type MIS transistor, which negatively impacts device performance.

217. To mitigate variations in transistor characteristics caused by dopant diffusion Tamaki reduces both n-type and p-type impurity concentrations (first embodiment). Alternatively, only the n-type concentration is reduced (second embodiment). This effectively reduces the amount of phosphorus dopant available for diffusion because, according to Tamaki, “[t]he diffusion rate of phosphorus is higher than the diffusion rate of boron in general.” (Tamaki, ¶23.)

218. A POSITA would have understood that Tamaki’s approach had limitations, because while Tamaki’s method reduces dopant diffusion, the method does not eliminate it. Further, there is a practical limit to how far dopant concentration can be reduced. For example, reducing dopant concentration can consequently reduce dopant diffusion, but the device performance may be

degraded. That is there is a tradeoff between reducing dopant concentration to avoid dopant diffusion and maintaining device performance. As noted in Tamaki, SRAM regions are particularly vulnerable to mutual dopant diffusion due to narrower isolation regions between the n-type and p-type MIS transistors. With continued device scaling, the width of the isolation region for both SRAM and logic regions continues to decrease. The need for further device scaling combined with the limitations on the amount that gate electrode dopants can be reduced would have led a POSITA to search for alternative approaches to address dopant diffusion for dual-gate structures in both logic and SRAM devices. Sumi discloses an alternative technique that is complementary to Tamaki's approach.

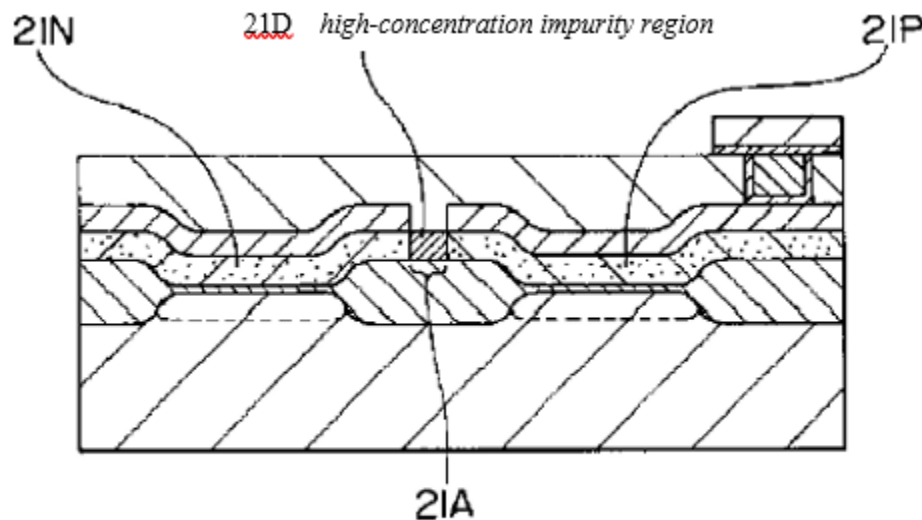
2. Sumi's Technique

219. Similar to Tamaki, Sumi recognizes that mutual dopant diffusion in dual-gate electrode structures is detrimental—not only to the dual-gate electrodes' integration in modern semiconductor devices but also to the overall device performance. (Sumi, ¶11.) Accordingly, Sumi's objective is to “provide a dual gate structure ... that excels in suppressing mutual diffusion of impurities between gate electrodes.” (Sumi, ¶13.)

220. To achieve this objective, Sumi's dual gate structure provides a high-concentration impurity region “in the connection region between the first conductivity type polycrystalline silicon layer and second conductivity type

polycrystalline silicon layer, having a higher impurity concentration than each respective polycrystalline silicon layer.” (Sumi, ¶15, *see also*, Sumi, ¶1.)

Specifically, Sumi’s dual-gate structure includes “connection region 21A between the N-type polycrystalline silicon layer 21N and the P-type polycrystalline silicon layer 21P.” (Sumi, ¶63, Figure 5 (below).) Connection region 21A contains “a higher impurity concentration than that of the N-type and P-type polycrystalline silicon layers 21N and 21P.” (Sumi, ¶63.) As a result of this structure, “it becomes less likely for mutual diffusion of impurities to occur between the N-type and P-type polycrystalline silicon layers 21N and 21P.” (Sumi, ¶64.) That is, Sumi discloses the use of a diffusion barrier between n-type and p-type regions.



An explanatory diagram of the second embodiment related to the dual gate structure of this invention.

Sumi, Figure 5

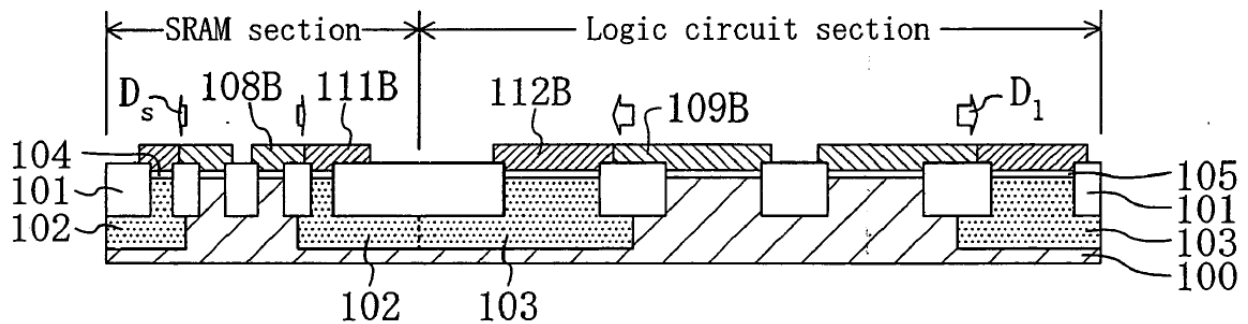
3. Combination of Tamaki and Sumi

221. A POSITA would have been motivated to combine Sumi's teaching regarding use of a high-concentration region to separate n-type and p-type regions in a dual-gate electrode structure with Tamaki's first and second embodiment devices. Specifically, a POSITA would have been motivated to form a high-concentration impurity region – functioning as a diffusion barrier -- like Sumi's region 21D, at the pn junction in Tamaki's dual-gate electrode structures depicted in Figures 3B (first embodiment) and 5B (second embodiment). In particular, Sumi teaches placing this high-concentration region in the connection zone between the adjacent n-type and p-type polycrystalline silicon gate segments, thereby impeding mutual dopant diffusion across the boundary.

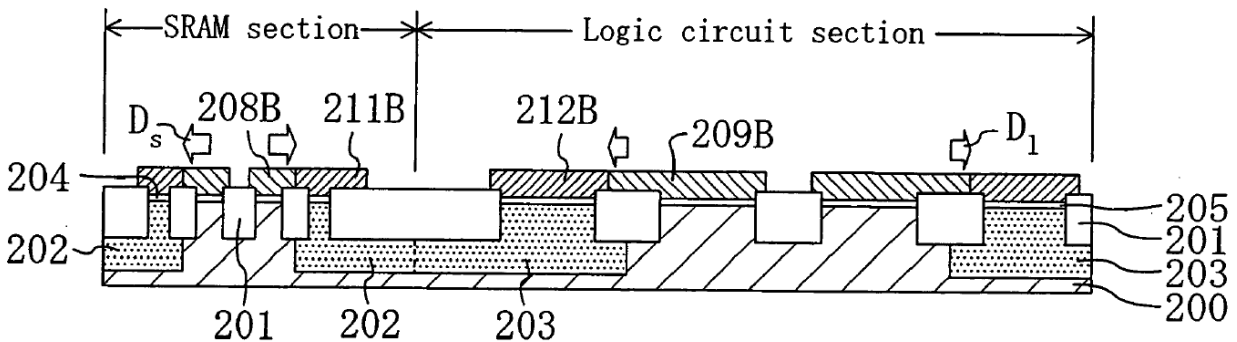
222. This modification would have been especially appealing in Tamaki's logic region, where the pn junction is positioned directly over the shallow trench isolation (STI) region. As Tamaki itself observes, phosphorus and boron diffusion across this junction can shift the pn boundary into the active area, degrading PMIS transistor performance. Sumi's structure directly addresses this problem by stabilizing the junction location and minimizing unwanted dopant encroachment.

223. Moreover, a POSITA would have recognized that Sumi's approach is fully compatible with Tamaki's existing process flows. Both references utilize similar materials (e.g., doped polysilicon gate electrodes), and Sumi's diffusion

barrier region can be introduced with minimal process complexity—e.g., via selective ion implantation in the junction area prior to or during gate formation. Thus, the combination represents a straightforward and predictable enhancement that builds upon Tamaki’s foundational work by incorporating Sumi’s more robust suppression of dopant diffusion.



Tamaki, Figure 3B (first embodiment)



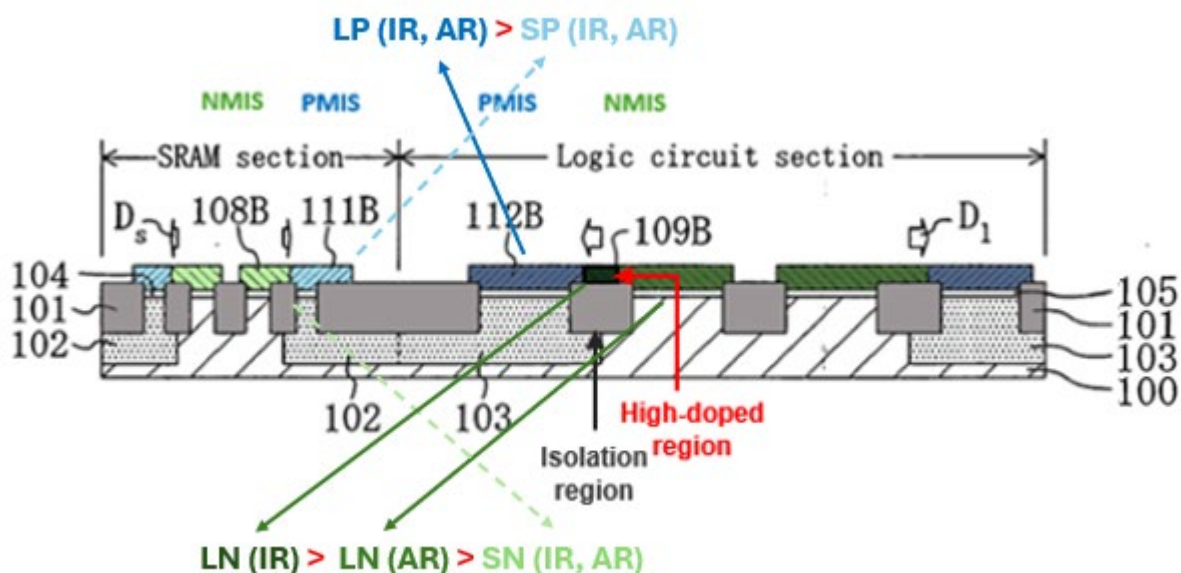
Tamaki, Figure 5B (second embodiment)

224. While Sumi mentions phosphorous as an example impurity for the high concentration region, it does not exclude use of other dopants. (See Sumi, ¶63 (“high-concentration impurity region 21D contains impurities such as phosphorus (P)”).) A POSITA would also recognize that the effectiveness of a diffusion barrier

depends not only on concentration but also on dopant diffusivity. In particular, a region highly doped with a lower-diffusivity dopant—such as arsenic—would serve as a more robust barrier against both boron and phosphorus diffusion. Given that Tamaki uses phosphorus as its n-type gate electrode dopant, a POSITA would have been motivated to select a different dopant for the high concentration region to avoid enhanced self-diffusion. Arsenic, a well-established n-type dopant in silicon, diffuses more slowly than phosphorus and is routinely used in advanced CMOS processes. Both Igarashi and Sumi, for example, utilize arsenic as n-type dopant. (Igarashi, ¶¶105-106, Figure 11D; Sumi, ¶¶10, 21.) Thus, a POSITA would have been motivated to form a high-concentration, arsenic-doped region at the pn boundary over the STI region in Tamaki’s dual-gate structures to more effectively suppress bidirectional dopant diffusion across the junction. This modification would support improved pn boundary stability and enable continued device scaling for both SRAM and logic regions across future technology nodes.

225. The resulting impurity concentration relationship for Tamaki’s first embodiment when combined with Sumi’s high-concentration barrier, illustrated in Figure 3B below, is:

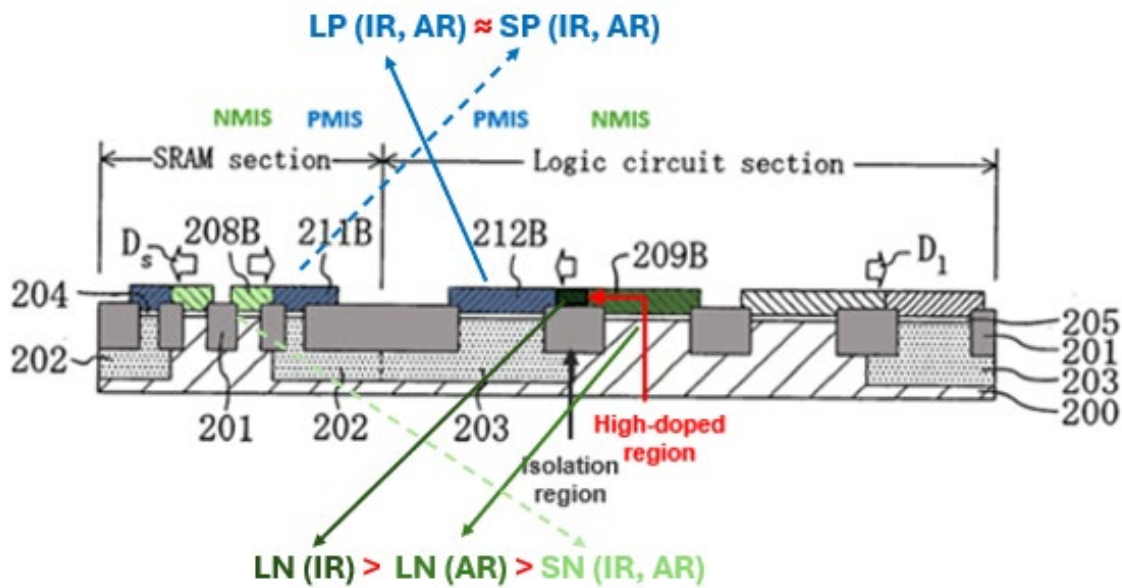
Tamaki’s First Embodiment with Sumi
LP (AR) > SP (IR, AR)
LN(IR) > LN (AR) > SN (IR, AR)



Tamaki Figure 3B (First Embodiment)-Sumi Combination

226. The impurity concentration relationship for Tamaki's first embodiment combined with Sumi, illustrated in Figure 5B below, is

Tamaki's Second Embodiment with Sumi
$LP (IR, AR) \approx SP (IR, AR)$
$LN (IR) > LN (AR) > SN (IR, AR)$



Tamiki Figure 5B (Second Embodiment)-Sumi Combination

4. Motivation to Combine

227. A POSITA would have been motivated to make this combination to overcome limitations of Tamaki's approach discussed in §VI.B.1 and to facilitate further scaling in Tamaki's design, including the chip's logic region. As explained above, Tamaki's reduction in dopant concentration only partially addresses the issue of mutual diffusion and presents tradeoffs with device performance. Sumi directly addresses this issue by proposing a structural barrier against dopant interdiffusion, offering a complementary and more robust solution. A POSITA would have recognized that combining Sumi's dopant-blocking high-concentration region with Tamaki's dual-gate architecture would significantly reduce interdiffusion across the pn junction within the shared gate electrode. By extension, this would improve threshold voltage stability and reduce device variability, both

of which are highly desirable in scaled CMOS design and would further motivate this combination.

228. Moreover, Tamaki and Sumi are in the same field of endeavor as the '373 patent, semiconductor devices. (TSMC-1001, 3:42-46; Tamaki, ¶¶2-4 *and* Sumi, ¶¶11, 13.) They both address challenges specific to dual-gate CMOS structures and focus on performance reliability at the gate level.

229. Additionally, the combination is nothing more than the application of a known technique (Sumi's fabrication of dual-gate electrode devices with a high-doped region) to a known device (Tamaki's dual-gate electrode) ready for improvement for the reasons discussed above, i.e., to minimize dopant diffusion and improve device robustness. A POSITA would have recognized this as an ordinary design enhancement well-supported by industry practices and engineering principles.

230. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable. Sumi's teaching aligns with a POSITA's understanding that dopants diffuse at different rates in silicon (Sze, Figure 4a, 466). It was known that regions doped with low-diffusivity species (like arsenic) could serve as effective barriers to faster-diffusing dopants (like phosphorus or boron). This concept predates the '373 patent and was in routine use in the industry. For instance, Bayraktaroglu discusses "a p-n junction

diffusion barrier ... comprising a first semiconductor layer 28 of p-type conductivity, a second semiconductor layer 32 of n-type conductivity and a third semiconductor layer 30 of p-type conductivity disposed between the first and second layers, the third layer being doped with a relatively low diffusivity dopant in order to **form a diffusion barrier** between the first and the second semiconductor layers.” (Bayraktaroglu, Abstract.) This reinforces the predictability and technical soundness of applying Sumi’s technique to Tamaki’s structure.

231. Furthermore, implementing Sumi’s teachings into Tamaki’s dual-gate electrode structure would have been well within the skill set of a POSITA. The combination requires only standard fabrication techniques, such as the formation of high concentration As-doped regions, that were routine well before the priority date of the ’373 patent. A POSITA would have also recognized the process steps integrating Sumi’s dopant-blocking region are compatible with Tamaki’s process flow, for at least two reasons.

232. First, the high-concentration region in Sumi is formed as a distinct step that utilizes its own photolithography mask for selective ion implantation over the isolation region at the pn junction. (Sumi, ¶¶72-73, Figure 6(2).) Second, Tamaki does not disclose any conflicting masks or process steps targeting this region of the gate electrode structure. Accordingly, inserting Sumi’s step into Tamaki’s flow would not disrupt the overall fabrication sequence. For example, a

POSITA would implement Sumi's step for creating the high-concentration arsenic-doped region prior to phosphorus implantation into the gate electrode formation film 106 of the n-type MIS transistor in the logic section (Tamaki, ¶85; Fig. 1B). This sequencing aligns with Sumi's method, where the high-concentration n-type region is formed before gate doping (Sumi, ¶¶73–75), making the integration both technically feasible and logically consistent.

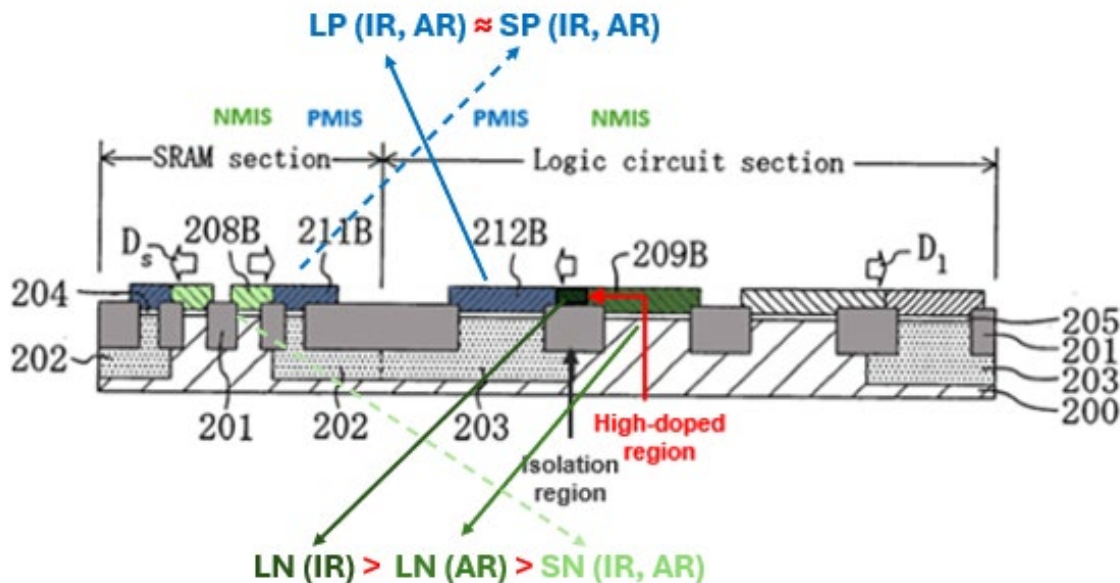
C. Tamaki (Second Embodiment)-Sumi Combination Renders Claim 5 Obvious.

[5] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

233. The following table summarizes the impurity concentration relationship for claim 5 and the impurity concentration relationship of the Tamaki and Sumi device under the second embodiment.

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	LN(IR) > LN(AR) > SN(AR)	LN (IR) > LN (AR) > SN(IR, AR) LP(IR, AR) ≈ SP(IR, AR)
A-2	SN(IR) > SN(AR) > LN(AR)	
B-1	LP(IR) > LP(AR) > SP(AR)	
B-2	SP(IR) > SP(AR) > LP(AR)	

234. As seen in Figure 5B (below), the portion of electrode 209 over the active region, **LN(AR)**, (“portion of the first silicon film of the first conductivity type located on the first active region”) has a lower n-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 209 over the isolation region, **LN(IR)** (“portion of the first silicon film of the first conductivity type located on the isolation region”). That is, **LN(AR) < LN(IR)** in Tamaki’s second embodiment when combined with Sumi under scenario A-1.



Tamiki Figure 5B (Second Embodiment)-Sumi Combination

235. Accordingly, Tamaki’s second embodiment in combination with Sumi discloses “a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower

than that of a portion of the first silicon film of the first conductivity type located on the isolation region” under scenario A-1.

D. Tamaki (First Embodiment)-Sumi Combination Renders Claim 7 Obvious

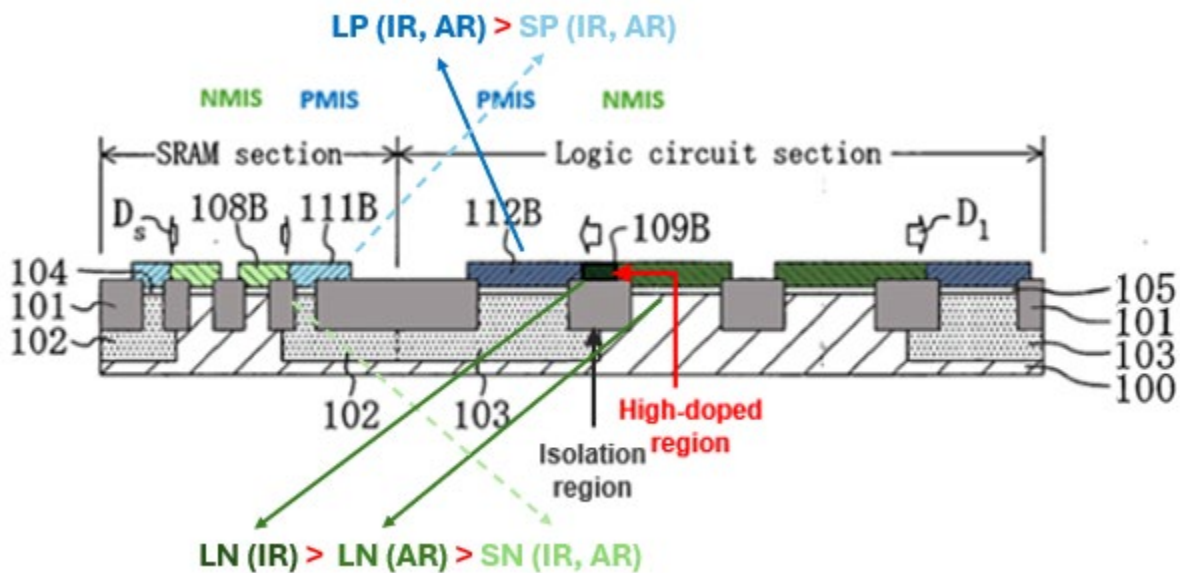
[7] The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

236. The following table summarizes the impurity concentration relationship for claim 7 and the impurity concentration relationship of the Tamaki and Sumi device under the first embodiment.

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$LN(IR, AR) > SN(AR)$ $LP(AR) < LP(IR)$	
A-2	$SN(IR, AR) > LN(AR)$ $SP(AR) < SP(IR)$	
B-1	$LP(IR, AR) > SP(AR)$ $LN(AR) < LN(IR)$	$LP(AR) > SP(IR, AR)$ $LN(IR) > LN(AR) > SN(IR, AR)$
B-2	$SP(IR, AR) > LP(AR)$ $SN(AR) < SN(IR)$	

237. As seen in Figure 3B (below), the portion of electrode 109 over the active region, $LN(AR)$, (“portion of the first silicon film of the second conductivity

type located on the second active region”) has a lower n-type impurity concentration (“second-conductivity-type impurity concentration”) than the portion of electrode 109 over the isolation region, **LN(IR)** (“portion of the first silicon film of the second conductivity type located on the isolation region”). That is, **LN(AR)** < **LN(IR)** in Tamaki’s first embodiment when combined with Sumi under Scenario B-1.



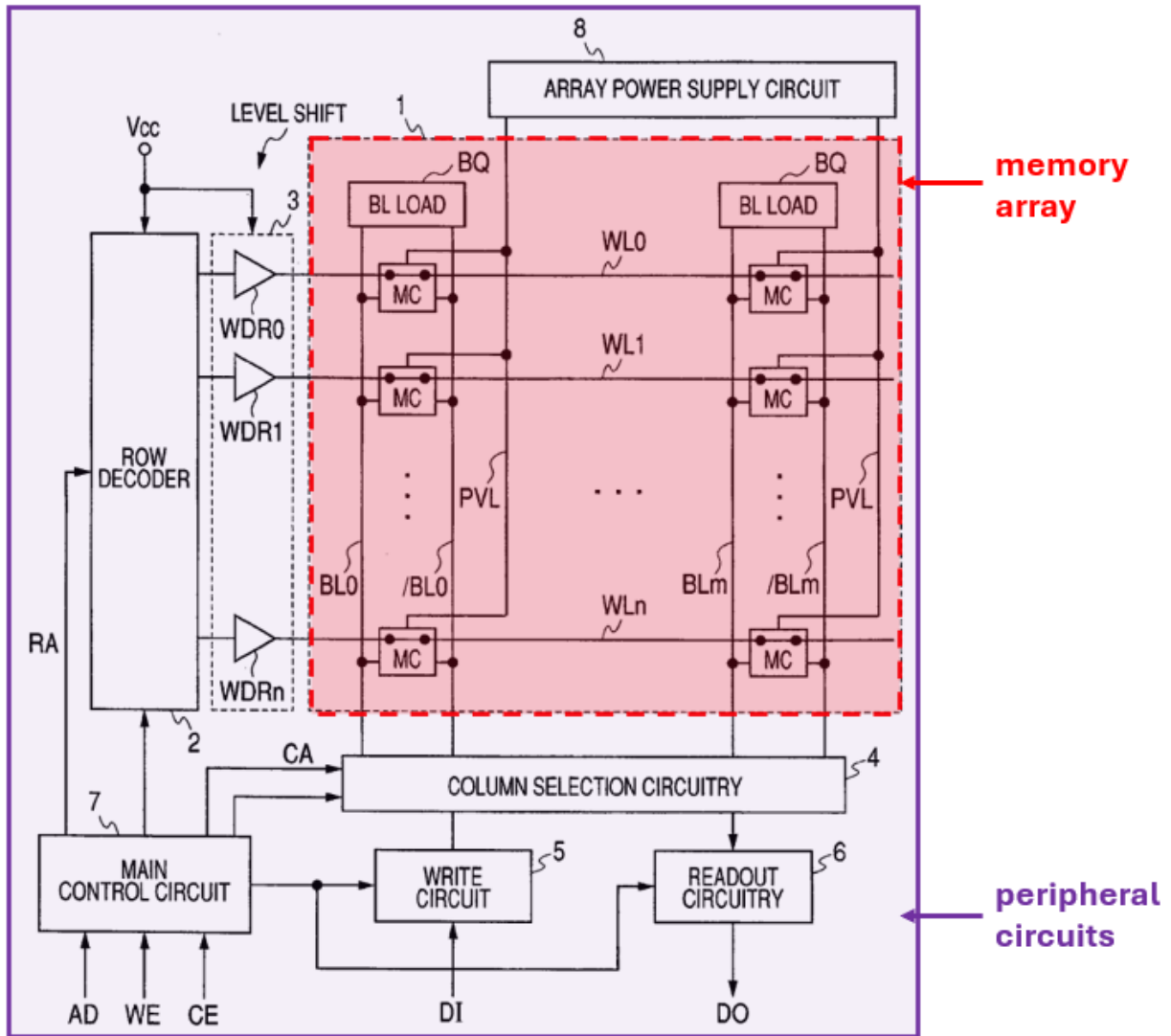
Tamaki Figure 3B (First Embodiment)-Sumi Combination

238. Accordingly, Tamaki’s first embodiment in combination with Sumi discloses “a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region” under Scenario B-1.

VII. GROUND 3: Igarashi Renders Claims 1-4, 6, and 8-14 Obvious.

A. Overview of Igarashi

239. Igarashi describes a “semiconductor memory device” including (1) memory array 1 having a plurality of memory cells (MC) and (2) peripheral circuits such as row decoder 2, word line driver 3, column selection 4, write 5, read 6, control 7, and power supply 8. (Igarashi, Abstract, ¶¶37-48, Figure 1 (below).)

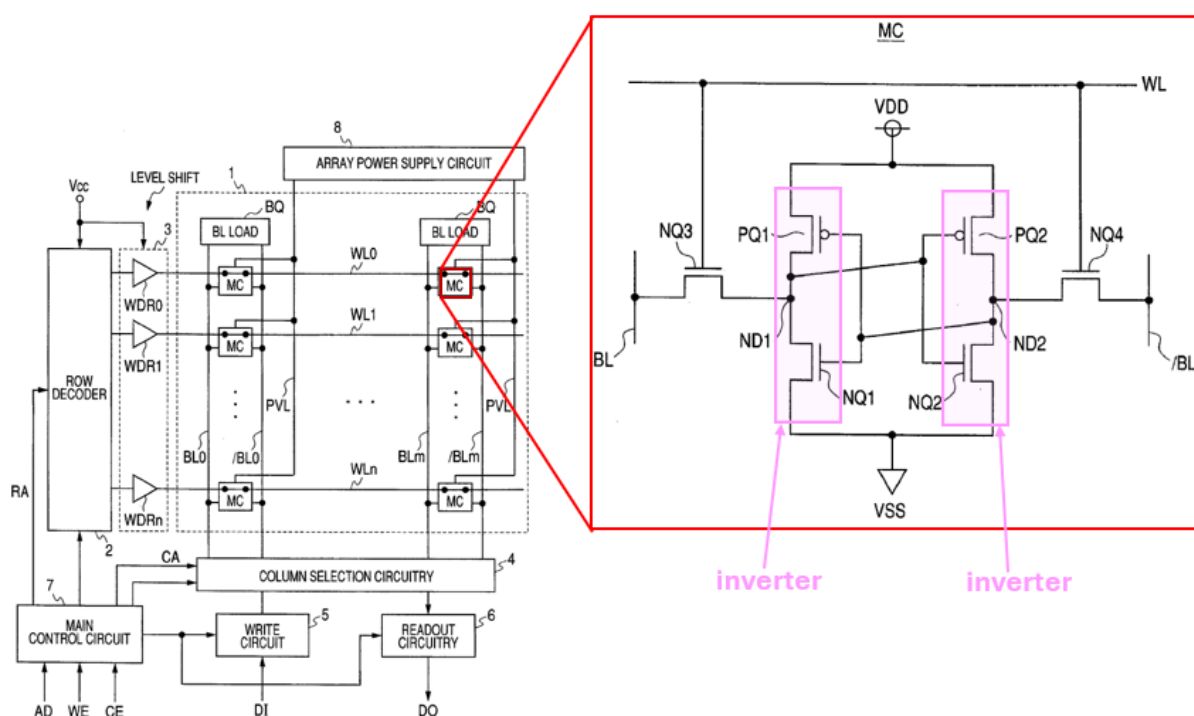


Igarashi, Figure 1

240. I focus my analysis on Igarashi's second embodiment (illustrated in Figures 10, 11A-11E) which renders claims 1-4 and 8-14 obvious under Scenario B (first conductivity type= **p-type**; second conductivity type= **n-type**) and claims 1, 6, and 9-10) obvious under Scenario A (first conductivity type = **n-type**; second conductivity type= **p-type**).

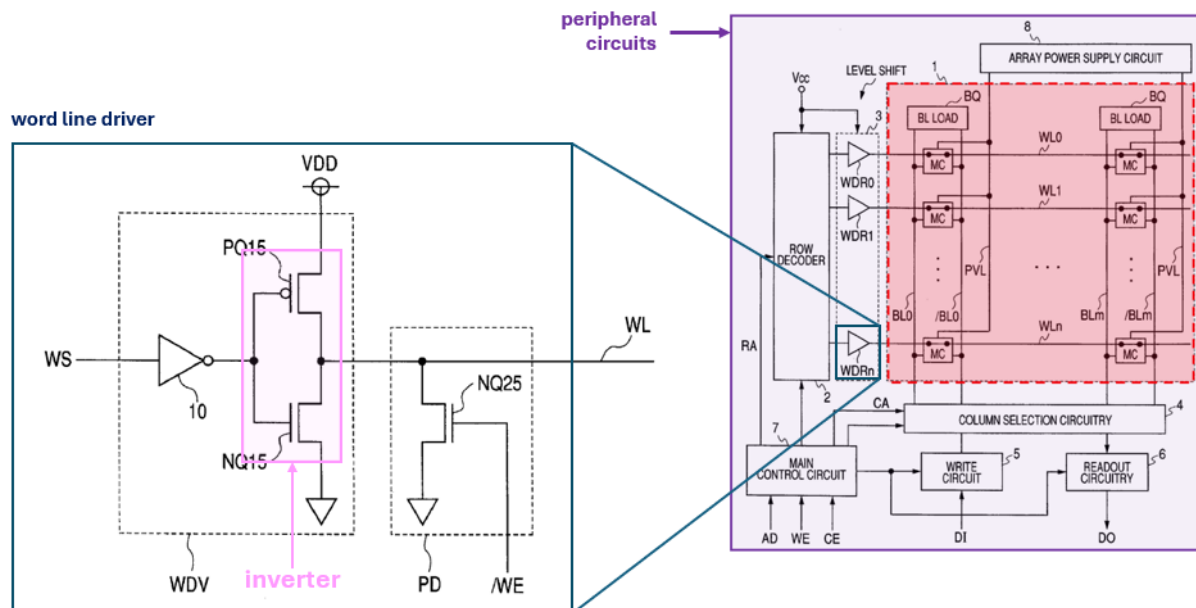
241. Igarashi’s second embodiment is directed to a “semiconductor memory device.” (Igarashi, Abstract.) Specifically, Igarashi “relates to the layout of a CMOS type SRAM memory cell among semiconductor memory devices.” (Igarashi, ¶2.)

242. As I discussed above, Igarashi’s memory device includes an array with multiple SRAM memory cells and peripheral (logic) circuit that controls the SRAM memory cells. Specifically, Figure 1 (below) “illustrates roughly the entire configuration of the semiconductor memory device” (Igarashi, ¶36) and Figure 2 (below) “is a drawing explaining the structure of memory cell MC...” (Igarashi, ¶49.)



Igarashi, Figure 1 (left), Figure 2 (right)

243. Igarashi's peripheral circuit includes, for example, word line driver (WDR) circuit 3 comprising an inverter (pink) in Figure 15 (below) which consists of PMOS transistor (PQ15) and NMOS transistor (NQ15) sharing a common gate electrode. (Igarashi, ¶¶37-48, 134-136.)



Igarashi, Figure 15 (left), Figure 1 (right)

B. Independent Claim 1

1. Preamble [1P]

[1P] A semiconductor device, comprising:

244. Igarashi's second embodiment is a "semiconductor device." For example, Igarashi is entitled "Semiconductor Memory Device" and relates to a "semiconductor memory device." (Igarashi, Abstract.) Igarashi "relates to the

layout of a CMOS type SRAM memory cell among **semiconductor memory devices.**” (Igarashi, ¶2, *see also* Igarashi, Abstract, ¶11 (describing “semiconductor memory device”), claims 3-5 (reciting “semiconductor memory device” comprising “memory array” and “peripheral circuit”); ¶¶, 9-17, 84 (second embodiment).)

2. “First Dual-Gate Electrode” and “Second Dual-Gate Electrode” Limitations [1A]-[1F] and

[1A] *a first dual-gate electrode; and*

[1B] *a second dual-gate electrode being separated from the first dual-gate electrode, wherein*

[1C] *the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,*

[1D] *the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,*

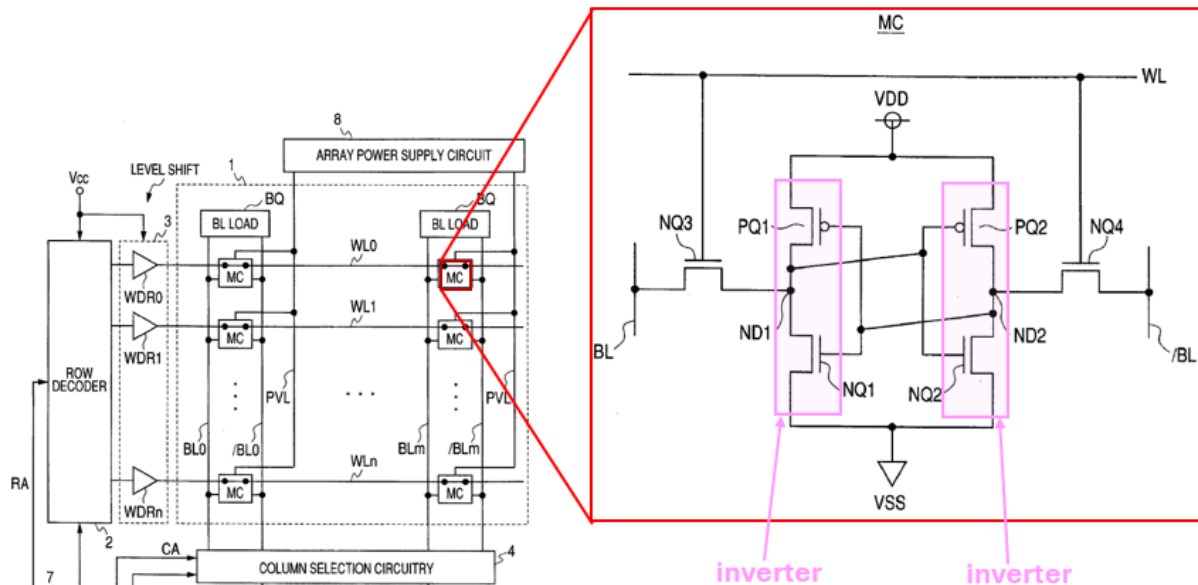
[1E] *the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,*

[1F] *the first gate electrode and the second gate electrode are connected to each other on the isolation region, and*

a. SRAM Memory Cell

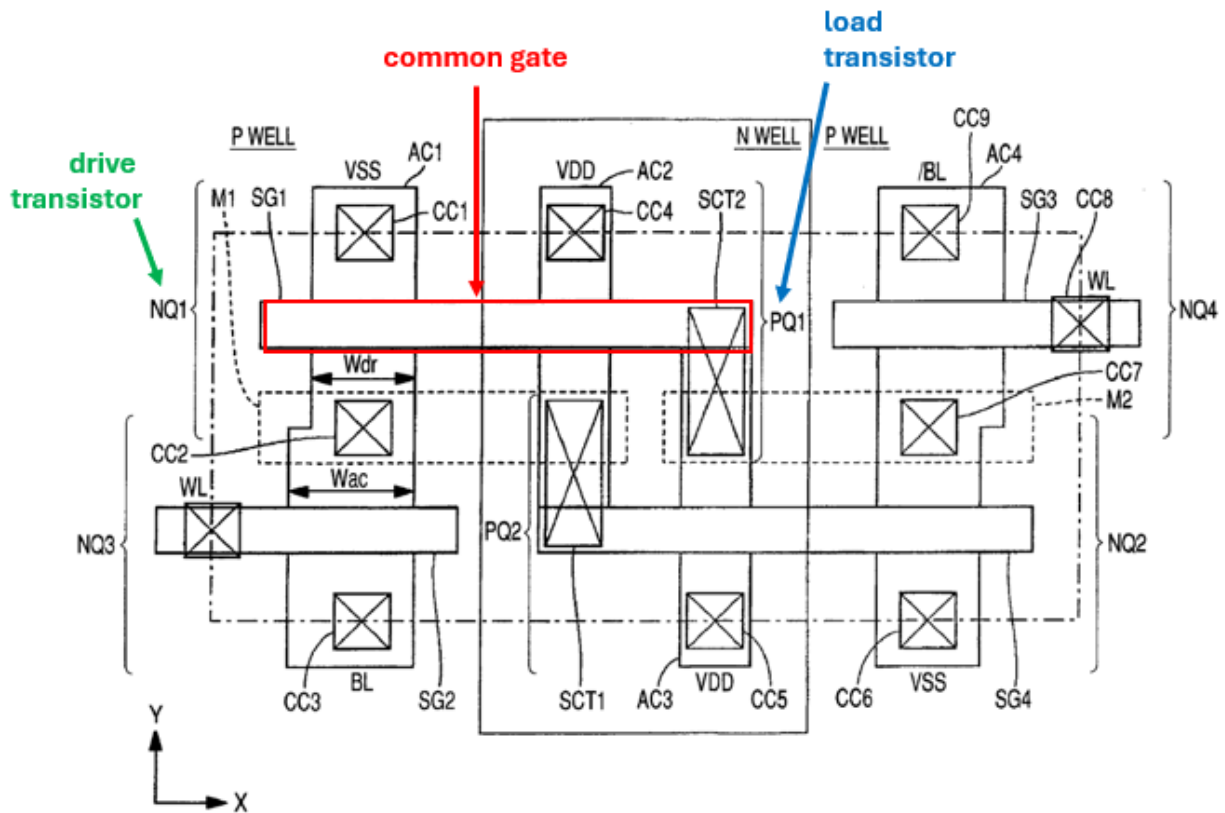
245. Igarashi’s memory array includes multiple SRAM memory cells (MCs). An exemplary 6-Transistor SRAM memory cell (Figure 2 (below-right))

comprises two access transistors (NQ3/NQ4) for enabling read/write operations and a pair of cross-coupled inverters, each having a load PMOS transistor (PQ1/PQ2) and a drive NMOS transistor (NQ1/NQ2). (See, Igarashi, ¶¶49-50, Figure 2 (below); Weste, 715-716.)



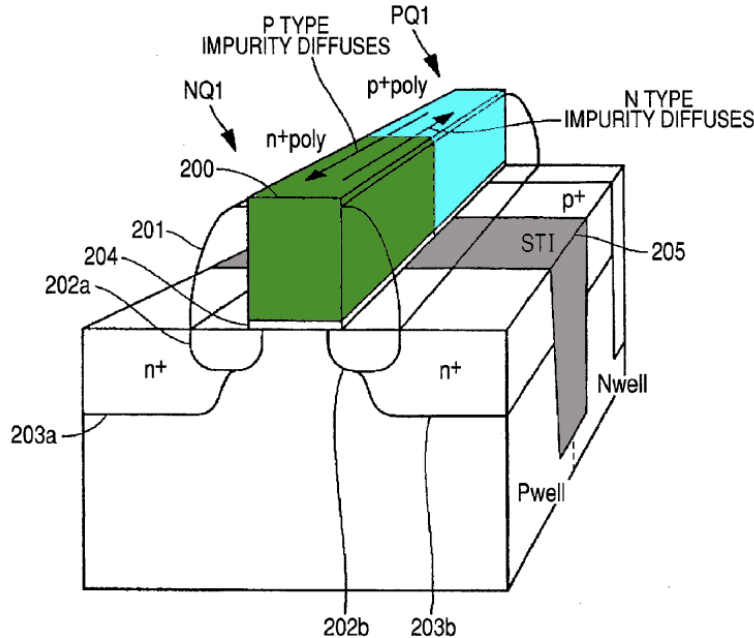
Igarashi, Figure 1 (left), Figure 2 (right)

246. In the layout shown in Figure 3, load transistors (PQ1/PQ2) “are formed in active regions AC2 and AC3” and drive transistors (NQ1/NQ2) are formed “[i]n active regions AC1 and AC4.” (Igarashi, ¶53.) “Polysilicon wiring SG1 forms the common gate of load transistor PQ1 and driver transistor NQ1” and “[p]olysilicon wiring SG4 forms the common gate of load transistor PQ2 and driver transistor NQ2.” (Igarashi, ¶¶57, 60.)



Igarashi, Figure 3

247. Figure 9, reproduced below, illustrates an inverter of an SRAM memory cell having a drive transistor (e.g. NQ1/NQ2) “which shares a polysilicon gate” with a load transistor (e.g., PQ1/PQ2). (Igarashi, ¶¶85.) NMOS driver transistor NQ1 “is formed on” the p-well, and load PMOS transistor PQ1 is formed on the n-well, separated by STI. (Igarashi, ¶¶86-88.) Polysilicon gate 200 includes an “impurity of an N type [] implanted to the region (N+poly) at the side of transistor NQ1” and an “impurity of a P type [] implanted to the region (P+poly) at the side of transistor PQ1.” (Igarashi, ¶¶86.)



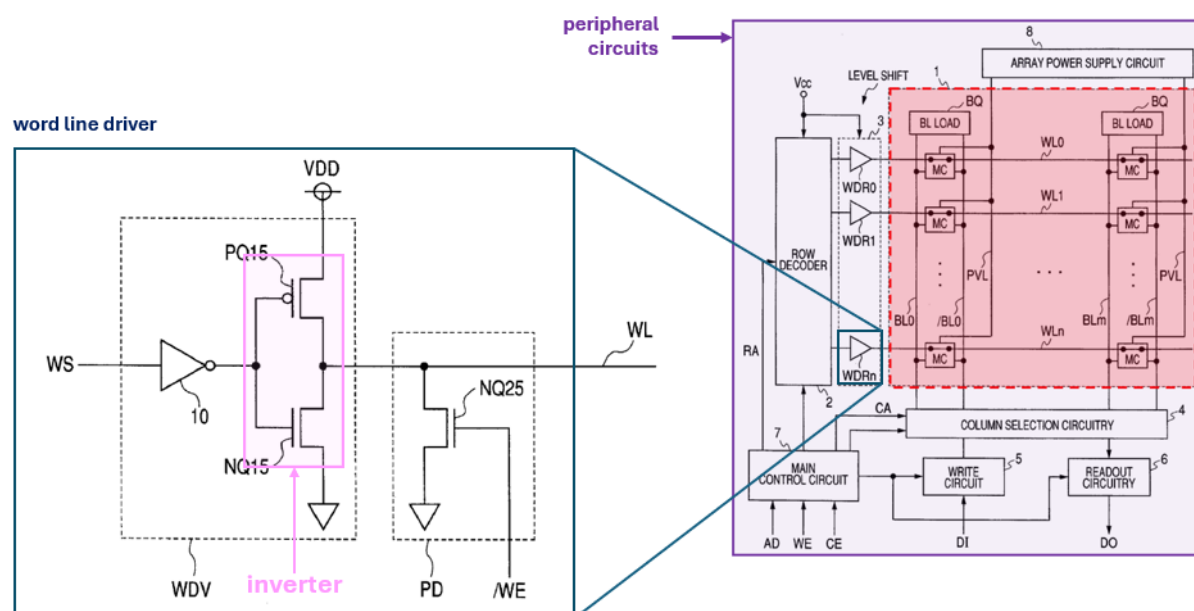
Igarashi, Figure 9

248. Thus, the PMOS transistor of the SRAM memory cell inverter includes a “gate electrode... having a [] silicon film of a [] conductivity type [p-type]” and the NMOS transistor includes a “gate electrode ... having a [] silicon film of a [] conductivity type [n-type]” [1C]. Collectively, these form a “dual-gate electrode” [1A] and “are connected to each other on the isolation region” [1F], as shown in Figure 9 above. (See, e.g., Igarashi, ¶88 (“polysilicon gate 200 is shared also in load transistor PQ1 is shown”).)

b. Peripheral (Logic) Circuit

249. Igarashi's device includes a "P channel MOS transistor [PMOS] and N channel MOS [NMOS] transistor which form [the] peripheral circuit, that is, the circuit for controlling the interior action of a memory array"; i.e., a logic circuit.

(Igarashi, ¶¶96.) The peripheral circuit includes, e.g., word line driver (WDR) circuit 3 comprising an inverter (shaded pink) which consists of PMOS transistor (PQ15) and NMOS transistor (NQ15) sharing a common gate electrode. (Igarashi, ¶¶37-48, 134-136, Figure 15 (below).)



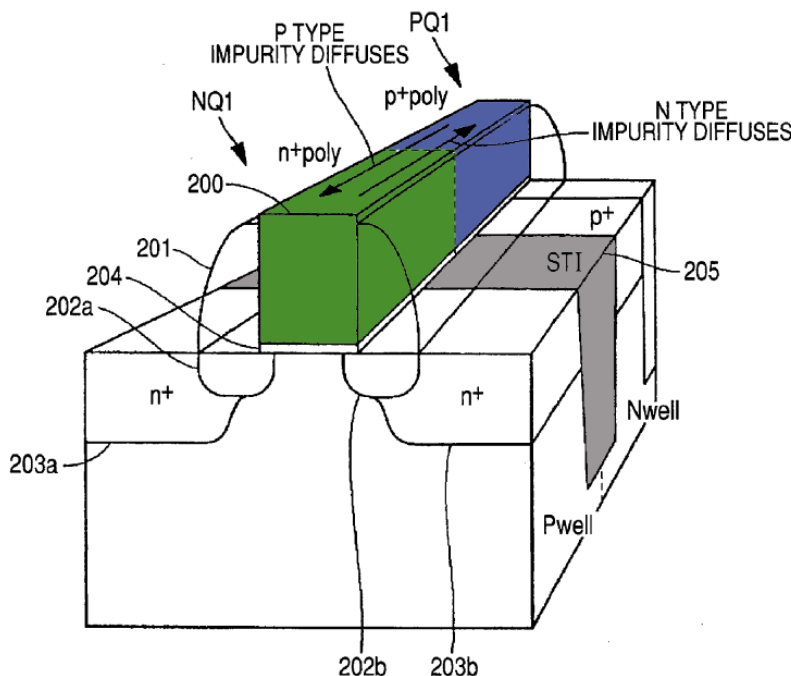
Igarashi, Figure 15 (left), Figure 1 (right)

250. A POSITA would recognize the similarity between the inverter circuits shown in Figure 15 of the WDR circuit and Figure 2 of the MC, and would consider them to be effectively identical dual-gate electrode structures. As discussed above, Igarashi's Figure 9 (reproduced below) illustrates an inverter in which the PMOS and NMOS transistors share a polysilicon gate electrode. (Igarashi, ¶¶85, 88.) Although Igarashi describes Figure 9 with respect to an SRAM memory cell, a POSITA would have understood this shared-gate

configuration (dual-gate electrode) applies not only to inverters in the SRAM region but also to inverters in the peripheral logic circuits or would have been motivated to use such a structure. First, the '373 patent admits that “conventional semiconductor devices” used dual-gate electrodes in the logic section. (TSMC-1001, 1:48-52, 2:16-20, Figures 15A-15B, 16 (“prior art”).) Second, using a unified inverted design approach across memory and logic circuitry promotes process uniformity by limiting design variability and reduces fabrication complexity (e.g., mask layers, etching steps, and material changes), leading to more efficient production and lower costs.

251. Igarashi describes the peripheral region as comprising multiple groups of MOS transistors with different threshold voltages, achieved by varying the impurity quantity implanted into the gate electrode regions. (Igarashi, ¶13.) This confirms the same dual-gate threshold voltage engineering used in the SRAM is also implemented in the peripheral logic circuitry. Figure 1 further supports this by identifying the peripheral region as including logic blocks such as the row decoder, column selection circuitry, word line drivers, and control logic—all of which would be constructed from transistors subject to threshold voltage (V_{th}) control. Further, a POSITA would have understood this shared-gate configuration applies not only to inverters in the SRAM region but also to inverters in the peripheral logic circuits because applying the same inverter design for both the memory

(SRAM) and logic (periphery) reduces the complexity of circuit design and simplifies the manufacturing process.

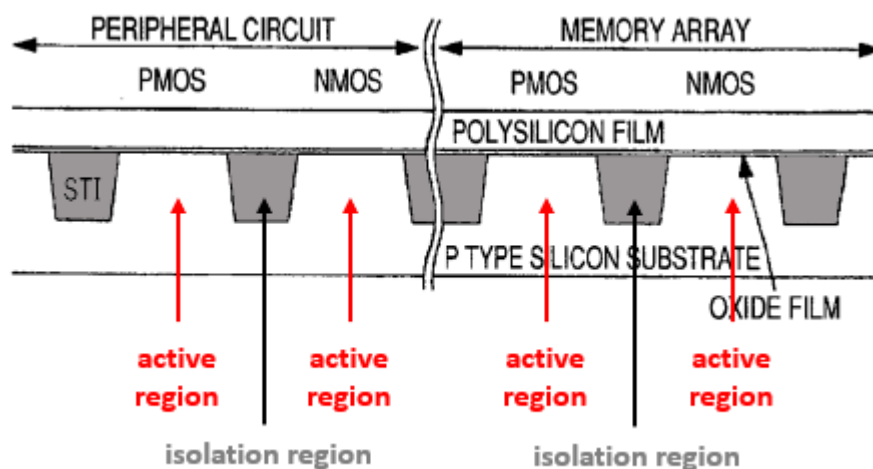


Igarashi, Figure 9

252. Thus, like the SRAM memory cell inverter, the PMOS transistor of the word line driver inverter includes a “*gate electrode... having a [] silicon film of a [] conductivity type [p-type]*” and the NMOS transistor includes a “*gate electrode ... having a [] silicon film of a [] conductivity type [n-type]*” [1C]. Collectively, these form a “*dual-gate electrode*” [1A] and “*are connected to each other on the isolation region*” [1F], as shown in Figure 9 above. (See, e.g., Igarashi, ¶88 (“polysilicon gate 200 is shared also in load transistor PQ1 is shown”).)

c. Transistor Formation

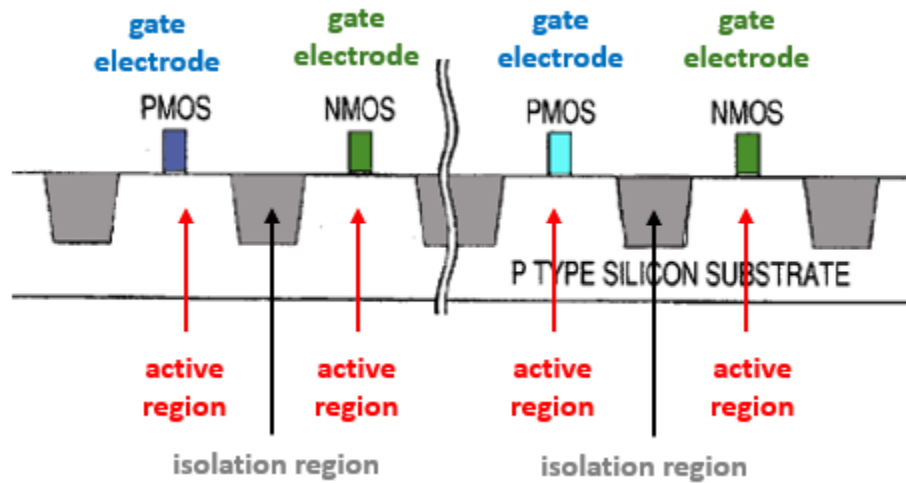
253. The process of forming the transistors of the memory array and peripheral circuit confirm the arrangement of the SRAM and logic transistors. First, “an oxide film is formed on a p type silicon substrate, and the polysilicon film is formed on it.” (Igarashi, ¶99, Figure 11A (below).) That is, the SRAM transistor includes a “*silicon film*” and the logic transistor includes a separate “*silicon film*.” While the n-well and p-well structures are omitted from the drawing for simplicity, Igarashi teaches “the NMOS transistor “is formed on” the p-well, while the PMOS transistor is formed on an n-well.” (Igarashi, ¶¶86, 99.) A POSITA would have understood “*active region(s)*” are in these wells. (See, e.g., Igarashi, ¶52 (describing “active regions ... formed in N well region” and active regions formed “in each of P well region”); see also, TSMC-1001, 1:65-2:4 (describing NMIS/PMIS transistors formed in n-well and p-well); Weste, 117-118; Plummer, 60-63.)



Igarashi, Figure 11A

254. As shown in Figure 11A, an STI region is formed between the PMOS and NMOS active regions. (See, Weste, 119-120; Plummer, 57-60 (describing use of isolation structures); TSMC-1001, 1:65-2:7 (describing AAPA including isolation regions between active regions).) Thus, Igarashi discloses or at least suggests that the “*active region*” of the PMOS transistor and the “*active region*” of the NMOS transistor “*are isolated from each other with an isolation region interposed therebetween*” [1E].

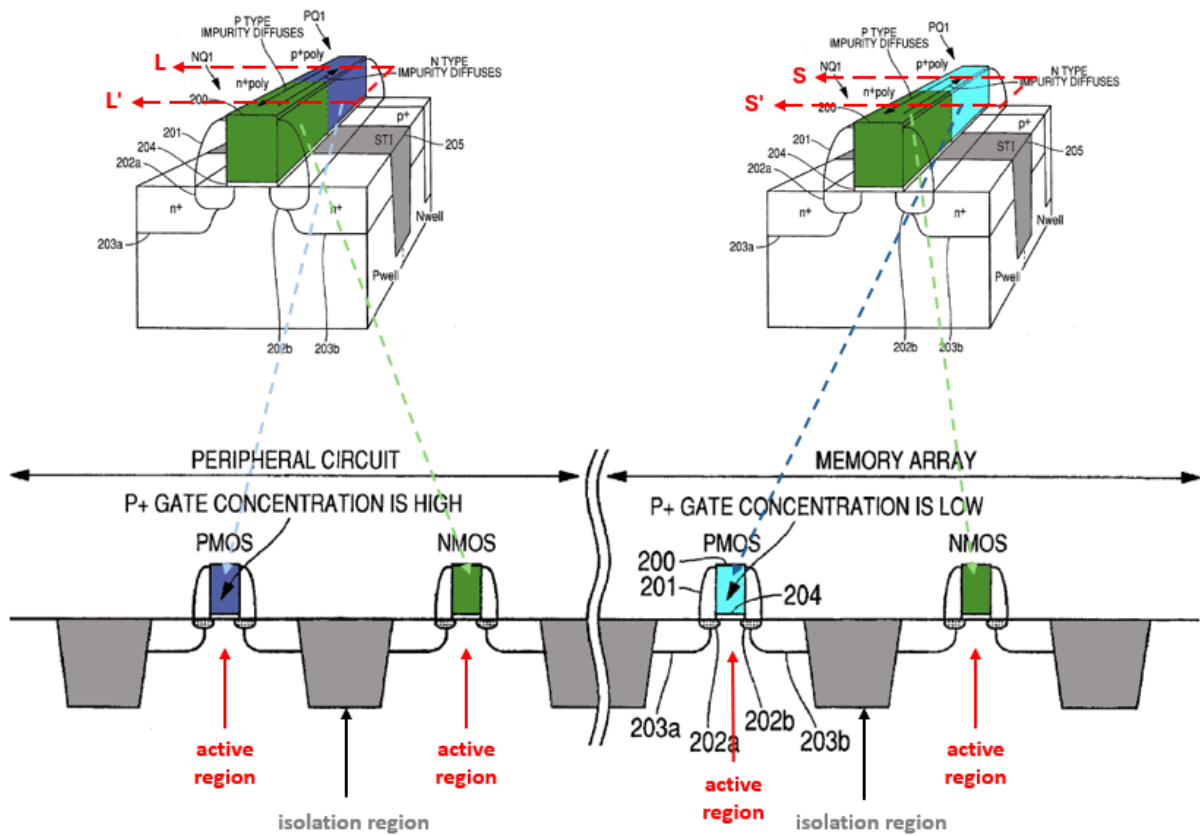
255. Subsequently, the polysilicon gates are formed “by etching.” (TSMC-1007, ¶102, Figure 11D.) As shown, each gate electrode is formed on an “*active region*.”



Igarashi, Figure 11D

256. Igarashi's Figure 10 "is a drawing explaining the impurity concentration implanted into the transistor formed in the memory array and peripheral circuit." (See Igarashi, ¶¶95, 27-28.) Based on this disclosure, a POSITA would have understood the peripheral circuit (left) depicts the inverter of Figure 9 along the L-L' line (left-top) and the memory array (right) depicts the inverter of Figure 9 along the S-S' line.

257. Figure 10 "is a drawing explaining the impurity concentration implanted into the transistor formed in the memory array and peripheral circuit." (See Igarashi, ¶¶95, 27-28.) A POSITA would have understood that the peripheral circuit of Figure 10 depicts the inverter of Figure 9 along the L-L' line (left-top) and the memory array of Figure 10 depicts the inverter of Figure 9 along the S-S' line.



Igarashi, Figure 9 (top-left and top-right), Figure 10 (bottom)

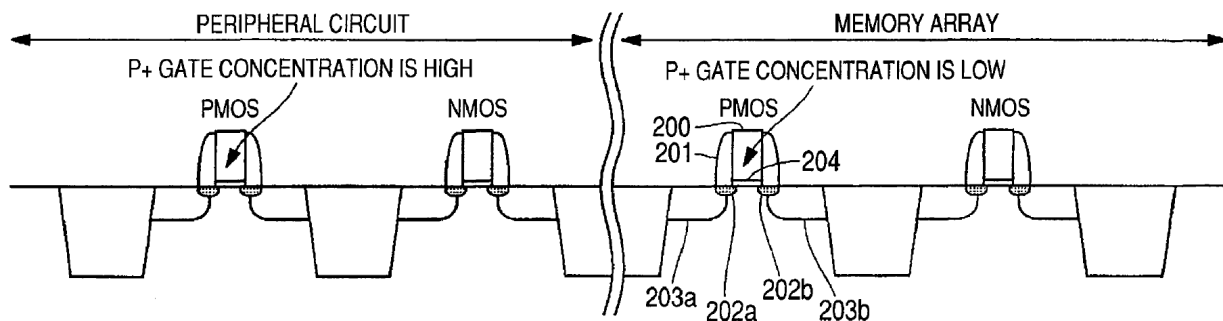
258. Accordingly, Igarashi meets limitations [1A]-[1F] in the manner set forth in the following table for Scenarios A-1, A-2, B-1, and B-2:

		A-1	A-2	B-1	B-2
first dual-gate electrode	first gate electrode on a first active region and having a first silicon film of a first conductivity type	logic NMOS	SRAM NMOS	logic PMOS	SRAM PMOS
	second gate electrode on a second active region and having a first silicon film of a second conductivity type	logic PMOS	SRAM PMOS	logic NMOS	SRAM NMOS

<i>second dual-gate electrode</i>	<i>third gate electrode located on a third active region and having a second silicon film of the first conductivity type</i>	SRAM NMOS	logic NMOS	SRAM PMOS	logic PMOS
	<i>fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type</i>	SRAM PMOS	logic PMOS	SRAM NMOS	logic NMOS

259. Igarashi also discloses the “second dual-gate electrode being separated from the first dual-gate electrode” [1B] under Scenarios A-1, A-2, B-1, and B-2. Figures 10 (below) and 11A-11E show a physical separation between the peripheral circuit and the memory array. Igarashi confirms the structure of the figures teaching that memory array 1 is formed separately from the “peripheral circuits, such as word line drive circuit 3.” (Igarashi, ¶¶37, 48.)

FIG. 10

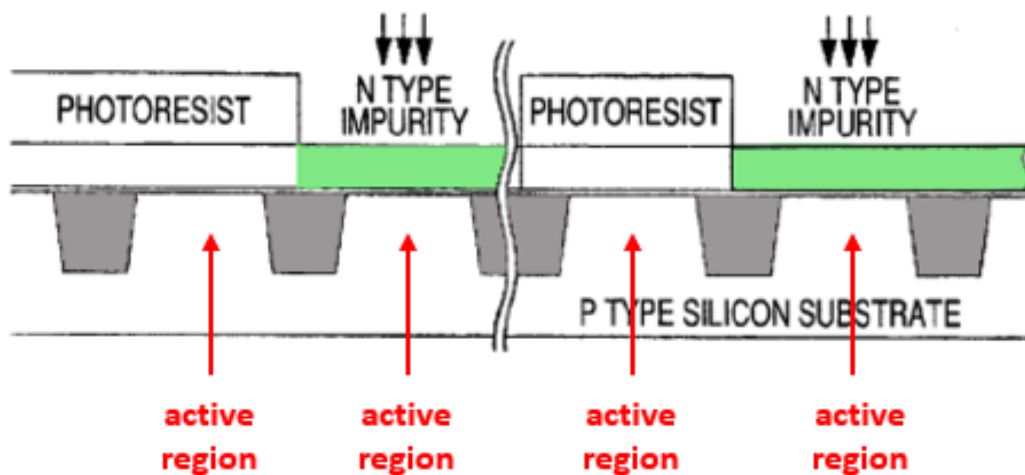


Igarashi, Figure 10

3. Impurity Concentration Limitation [1G]

[1G] at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

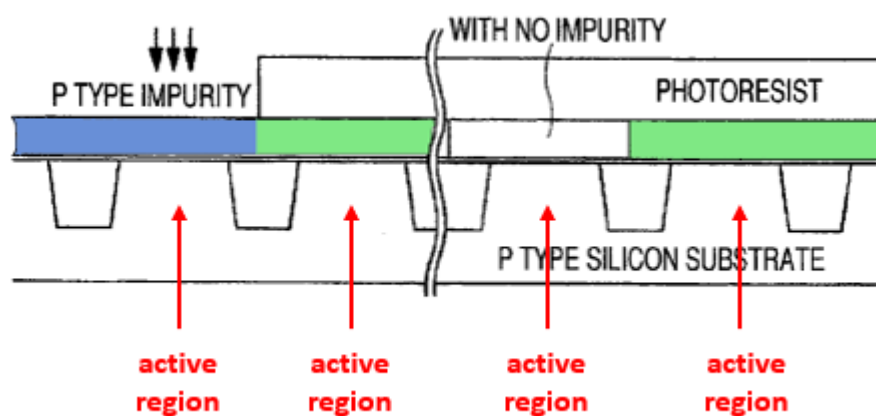
260. Igarashi discloses doping of the polysilicon gate electrodes in both the peripheral (logic) and SRAM circuits. Specifically, during fabrication of the peripheral (logic) circuits, an N-type impurity (e.g., phosphorus) is implanted into the polysilicon gate of the NMOS transistors in both the peripheral and SRAM circuits. (Igarashi, ¶100, Figure 11B.) For example, phosphorus is implanted at a dose of about 4×10^{15} to 6×10^{15} atoms/cm². (Igarashi, ¶100.)



Igarashi, Figure 11B

261. To form the polysilicon gate of the PMOS transistor, a P-type impurity (e.g., boron) is implanted after masking the NMOS region of the

peripheral circuit and the entire SRAM (memory) circuit. (Igarashi, ¶101, Figure 11C.) For example, Boron is implanted at a dose of about 2×10^{15} to 4×10^{15} atoms/cm² in the gate electrode of the peripheral PMOS transistor. (Igarashi, ¶101.) Because “the polysilicon gate of the P channel MOS transistor of a memory array is covered with resist, a P type impurity is not implanted” in the memory PMOS transistor. (Igarashi, ¶101, Figure 11C (below).) Consequently, “it is possible to change the implantation concentration of a P type impurity” of the device such that the implantation concentration in the memory (SRAM) PMOS gate is lower than that in the peripheral (logic) PMOS gate. (Igarashi, ¶¶110-111, Figure 10.)



Igarashi, Figure 11C

262. After lithographic patterning of the gate electrodes (Igarashi, ¶102, Figure 11D), additional source/drain implants are performed. Igarashi masks all regions except the memory PMOS transistor and implants boron or BF_2^+ at 1×10^{14} to 5×10^{14} atoms/cm². (Igarashi, ¶103.) Because the gate electrode is unmasked, this

dopant is also introduced into the gate of the memory PMOS transistor. (Igarashi, ¶103.) Next, Igarashi masks all regions except the peripheral PMOS transistor and implants boron or boron fluoride (B or BF_2^+) at 1×10^{14} to 5×10^{14} atoms/cm² into the unmasked PMOS region—including its gate electrode. (Igarashi, ¶104.)

263. To dope the source/drain of the memory NMOS transistor, arsenic is implanted at 0.5×10^{15} to 1×10^{15} atoms/cm² after masking the rest of the chip. (Igarashi, ¶105.) As the NMOS gate is unmasked, the gate also receives this dopant. Subsequently, arsenic (As) is implanted at 0.5×10^{15} to 1×10^{15} atoms/cm² into the NMOS source/drain region of the peripheral transistor, again affecting the unmasked NMOS gate electrode. (Igarashi, ¶106.)

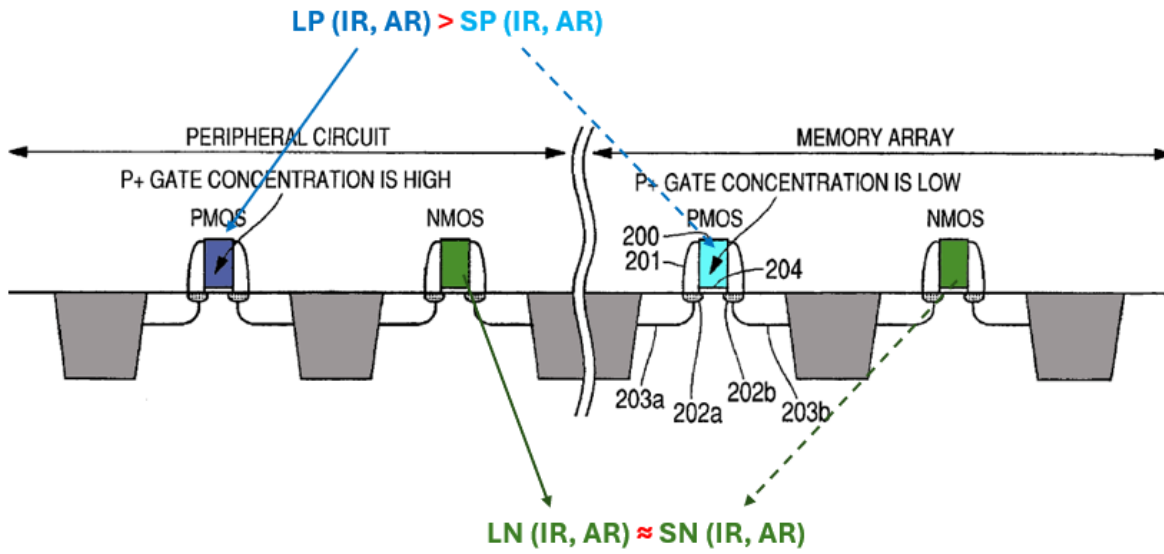
264. Further steps include an additional boron or BF_2^+ implant into the PMOS region (3×10^{15} to 4×10^{15} atoms/cm²) and a final arsenic implant into the NMOS region (1×10^{15} to 4×10^{15} atoms/cm²). (Igarashi, ¶¶108–109.) Because the respective gates are unmasked during these steps, the implanted dopants also affect the gate electrodes.

265. The following table summarizes the exemplary implants discussed above for both the memory and peripheral transistors.

	PMOS-Peripheral	PMOS-Memory
gate electrode implant	$2 \times 10^{15} - 4 \times 10^{15}$ atoms/cm ²	N/A
1 st S/D implant	$1 \times 10^{14} - 5 \times 10^{14}$ atoms/cm ²	$1 \times 10^{14} - 5 \times 10^{14}$ atoms/cm ²
2 nd S/D implant	$3 \times 10^{15} - 4 \times 10^{15}$ atoms/cm ²	$3 \times 10^{15} - 4 \times 10^{15}$ atoms/cm ²
	NMOS-Peripheral	NMOS-Memory
gate electrode implant	$4 \times 10^{15} - 6 \times 10^{15}$ atoms/cm ²	$4 \times 10^{15} - 6 \times 10^{15}$ atoms/cm ²
1 st S/D implant	$0.5 \times 10^{15} - 1 \times 10^{15}$ atoms/cm ²	$0.5 \times 10^{15} - 1 \times 10^{15}$ atoms/cm ²
2 nd S/D implant	$1 \times 10^{15} - 4 \times 10^{15}$ atoms/cm ²	$1 \times 10^{15} - 4 \times 10^{15}$ atoms/cm ²

266. Thus, the impurity concentration relationship disclosed in Igarashi's second embodiment can be expressed as follows:

Igarashi's Second Embodiment
LP(IR, AR) > SP(IR, AR)
LN (IR, AR) $\approx$ SN (IR, AR)
LP: peripheral (logic) PMOS SP: SRAM PMOS LN: peripheral (logic) NMOS SN: SRAM NMOS

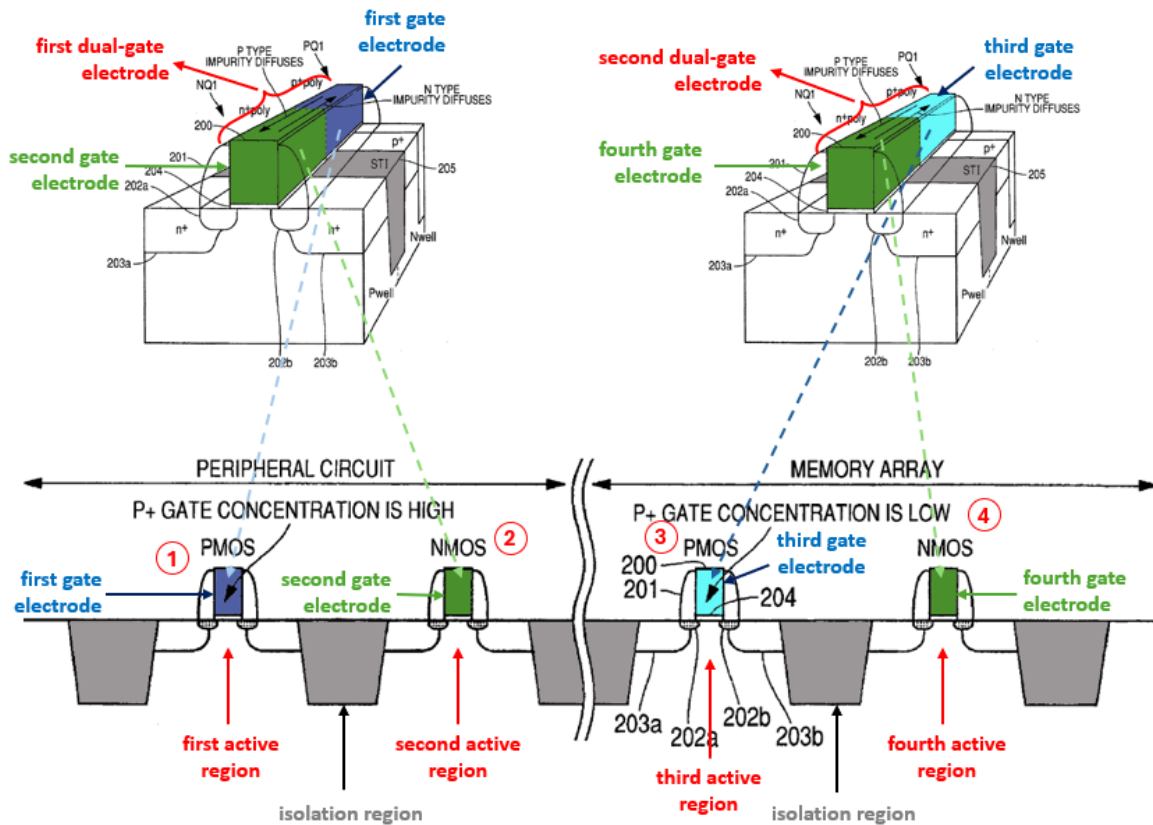


Igarashi, Figure 10

267. Igarashi discloses limitation [1G] under “at least a portion of the first silicon film of the first conductivity type [$LP (IR, AR)$] has a first-conductivity-type impurity concentration” (p-type) higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [$SP (IR, AR)$]” under only scenario B-1.

	Claimed Impurity Concentration Relationship Under Each Scenario	Igarashi Impurity Concentration Relationship
A-1	$LN(IR, AR) > SN(AR)$	
A-2	$SN(IR, AR) > LN(AR)$	
B-1	$LP(IR, AR) > SP(AR)$	$LP(IR, AR) > SP(IR, AR)$
B-2	$SP(IR, AR) > LP(AR)$	

268. In summary, Igarashi renders claim 1 obvious under Scenario B-1 as shown in the illustrations below.



C. Claim 2

[2] The semiconductor device of claim 1, wherein an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.

269. Igarashi renders obvious “an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.”

270. Igarashi's second embodiment explicitly discloses an SRAM memory array containing SRAM memory cells. (Igarashi, ¶¶92, 96.) It also states that the peripheral circuit includes a logic circuit. (Igarashi, ¶96 ("the P channel MOS transistor and N channel MOS transistor which form peripheral circuit, that is, **the circuit for controlling the interior action of a memory array** concretely are shown").) Igarashi acknowledges the trend toward a larger SRAM bit capacities **and system integration**, and notes the resulting demand to **shrink SRAM cell sizes**. (Igarashi, ¶4.)

271. Accordingly, a POSITA would understand that integrating SRAM and logic circuits using Igarashi's dual-gate structure layout demands circuit-specific layout strategies. This is because an SRAM requires high density to increase the memory's capacity and low leakage since most of the memory cells sit idle holding state, while logic circuitry typically demands greater spacing and isolation for signal integrity and noise suppression, especially at high-frequency of operation.

272. Given these distinct requirements, a POSITA would naturally increase isolation widths between peripheral circuit transistors ("*between the first active region and the second active region*") compared to those in the memory array ("*between the third active region and the fourth active region*"), since the SRAM and logic circuitry have competing spatial demands, e.g., high density for high

memory capacity versus spacing in logic circuits for ensuring signal integrity and noise suppression.

273. Thus, Igarashi renders claim 2 obvious.

D. Claims 3 and 11

[3] The semiconductor device of claim 1, wherein at least a portion of the first silicon film of the second conductivity type has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

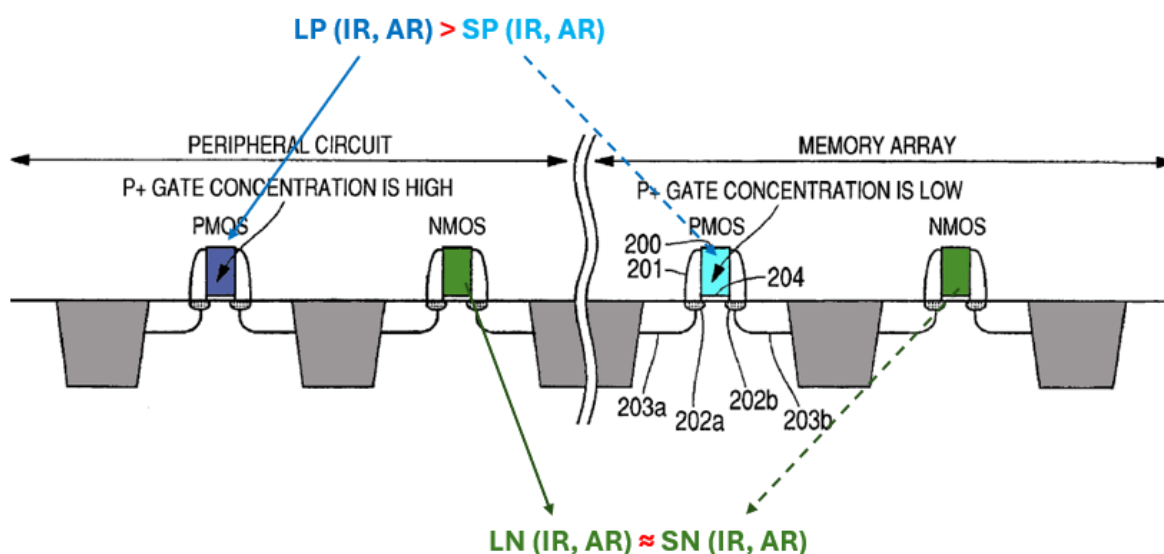
[11] The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

274. The following table summarizes the impurity concentration relationship for claims 3 and 11 and Igarashi's impurity concentration relationship under Igarashi's second embodiment:

	Claimed Impurity Concentration Relationship Under All Scenarios	Igarashi's Impurity Concentration Relationship
A-1	$LN(IR, AR) > SN(AR)$ $LP(IR, AR) \approx SP(AR)$	
A-2	$SN(IR, AR) > LN(AR)$ $SP(IR, AR) \approx LP(AR)$	
B-1	$LP(IR, AR) > SP(AR)$ $LN(IR, AR) \approx SN(AR)$	$LP (IR, AR) > SP (IR, AR)$ $LN (IR, AR) \approx SN (IR, AR)$
B-2	$SP(IR, AR) > LP(AR)$ $LN(IR, AR) \approx SN(AR)$	

275. Igarashi discloses that “in the polysilicon gate of an [NMOS] transistor, in a memory array, the impurity of an N type **is implanted like** the [NMOS] transistor of a peripheral circuit.” (Igarashi, ¶111.) Accordingly, as illustrated in Figure 10 (below), a portion of the electrode of the peripheral circuit NMOS transistor over the active region, **LN (AR)** (“*at least a portion of the first silicon film of the second conductivity type*”) has a substantially equal n-type impurity concentration (“*second-conductivity-type impurity concentration*”) to the portion of electrode 211 over the active region, **SN (IR, AR)** (“*the second silicon film of the second conductivity type located on the fourth active region*”). That is,

$LN(IR, AR) \approx SN(IR, AR)$ in Igarashi's second embodiment under scenario B-1.



Igarashi, Figure 10

276. Accordingly, Igarashi's second embodiment discloses “at least a portion of the first silicon film of the second conductivity type [$LN(AR)$] has a second-conductivity-type impurity concentration [$n\text{-type}$] substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region [$SN(AR)$]” [3] and “a portion of the first silicon film of the second conductivity type located on the second active region [$LN(AR)$] has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region [$SN(AR)$]” under scenario B-1.

E. Claim 4

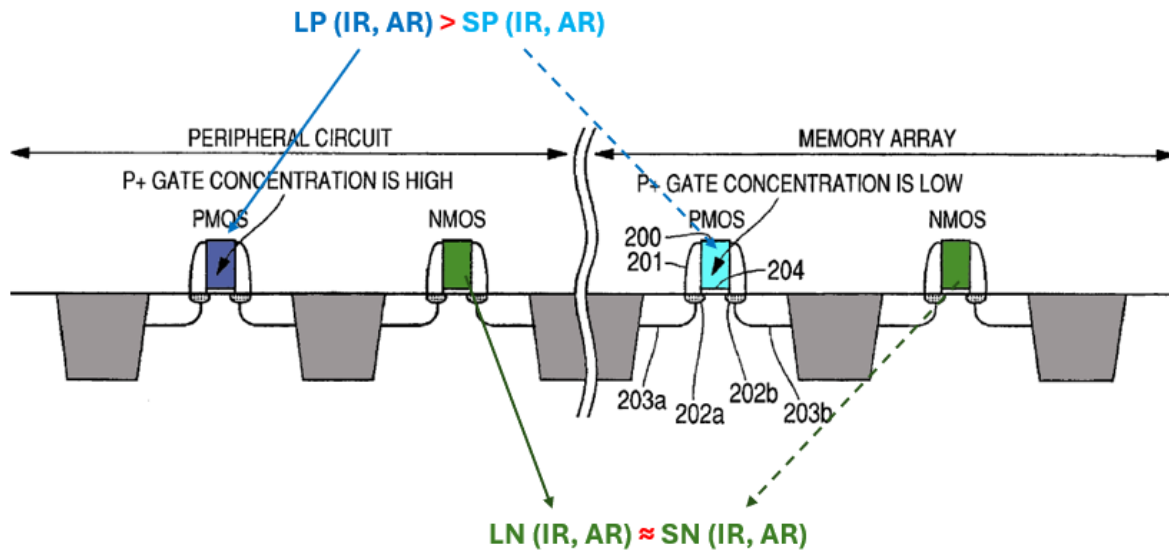
[4] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

277. The following table summarizes the impurity concentration relationship for claim 4 and Igarashi's impurity concentration relationship under Igarashi's second embodiment:

	Claimed Impurity Concentration Relationship	Igarashi Impurity Concentration Relationship
A-1	LN(AR) > SN(AR)	
A-2	SN(AR) > LN(AR)	
B-1	LP(AR) > SP(AR)	LP (IR, AR) > SP (IR, AR) LN (IR, AR) $\approx$ SN (IR, AR)
B-2	SP(AR) > LP(AR)	

278. As illustrated in Figure 10 (below), the portion of the gate electrode over the first active region, **LP(AR)**, (“*the first silicon film of the first conductivity type located on the first active region*”) has a higher p-type impurity concentration (“*first-conductivity-type impurity concentration*”) than the portion of electrode over the third active region, **SP(AR)**, (“*the second silicon film of the first*

conductivity type located on the third active region”). That is, $LP(AR) > SP(AR)$ in Igarashi’s second embodiment under scenario B-1.



Igarashi, Figure 10

279. Accordingly, Igarashi’s second embodiment discloses “a portion of the first silicon film of the first conductivity type located on the first active region [$LP(AR)$] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [$SP(AR)$],” under scenario B-1.

F. Claim 8

[8] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region.

280. As discussed in §VII.B.3, the entire film of the first gate electrode of the PMOS transistor is implanted simultaneously. Therefore, the impurity concentration of the portion of the first gate electrode over the first active region **LP(AR)** is substantially equal to that of the portion located over the isolation region **LP(IR)**, or as illustrated with the shorthand notation: **LP(AR) $\approx$ LP(IR)**.

281. Accordingly, Igarashi discloses “a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region,” under , the portion of the first gate electrode over the first active region has substantially the same impurity concentration as the portion of the first gate electrode over the isolation region. Igarashi discloses claim 8 under Scenario B-1.

G. Claim 9

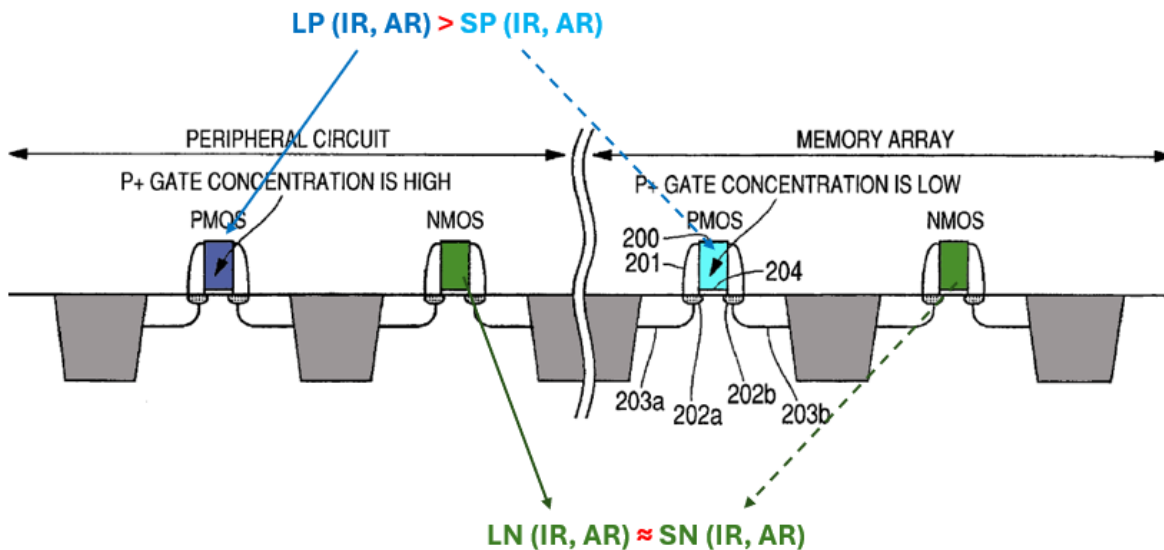
[9] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

282. The following table summarizes the impurity concentration relationship for claim 9 and Igarashi’s impurity concentration relationship under the second embodiment:

	Claimed Impurity Concentration Relationship	Igarashi Impurity Concentration Relationship
A-1	$LN(IR) > SN(AR)$	$LN(IR, AR) > SN(IR, AR)$
A-2	$SN(IR) > LN(AR)$	
B-1	$LP(IR) > SP(AR)$	$LP(IR, AR) > SP(IR, AR)$
B-2	$SP(IR) > LP(AR)$	

283. As illustrated in Figure 10 (below), the portion of logic gate electrode over the isolation region, $LP(IR)$, (“*the first silicon film of the first conductivity type located on the isolation region*”) has a higher p-type impurity concentration (“*first-conductivity-type impurity concentration*”) than the portion of SRAM gate electrode over the active region, $SP(AR)$, (“*the second silicon film of the first conductivity type located on the third active region*”). That is, $LP(IR) > SP(AR)$ in Igarashi’s second embodiment under Scenario B-1.

284.



Igarashi, Figure 10

285. Accordingly, Igarashi's second embodiment discloses "a portion of the first silicon film of the first conductivity type located on the isolation region [LP(IR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SP(AR)]" under Scenario B-1.

H. Claims 13 and 14

[13P] The semiconductor device of claim 1, wherein

[13A] the first gate electrode is a gate electrode of a first PMIS transistor,

[13B] the second gate electrode is a gate electrode of a first NMIS transistor,

[13C] the third gate electrode is a gate electrode of a second PMIS transistor,
and

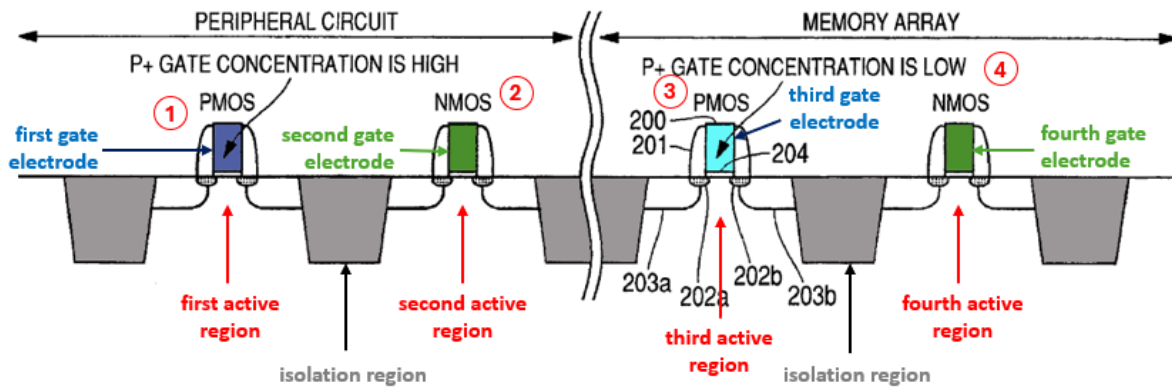
[13D] the fourth gate electrode is a gate electrode of a second NMIS transistor.

[14P] The semiconductor device of claim 1, wherein

[14A] each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and

[14B] each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit.

286. In connection with Figure 10 (below), Igarashi's second embodiment device discloses that "[t]he P channel MOS transistor and N channel MOS transistor of the SRAM memory cell by which accumulation arrangement is done with reference to FIG. 10 here at a memory array, and the P channel MOS transistor and N channel MOS transistor which form peripheral circuit, that is, the circuit for controlling the interior action of a memory array concretely are shown." (Igarashi, ¶96.) Accordingly, Igarashi discloses a structure including both PMOS and NMOS transistors forming the peripheral circuit and both PMOS and NMOS transistors forming the SRAM memory cell. (Igarashi, ¶96.) Igarashi therefore discloses claim 13 under Scenario B-1.



Igarashi, Figure 10

287. Each of the first and second gate electrodes is a gate electrode in the peripheral circuit. (Igarashi, ¶96.) The peripheral circuits include row decoder 2, word line driver circuit 3, column selection circuitry 4, write circuit 5, read-out circuit 6, control circuit 7, and power supply circuit 8. (Igarashi, Figure 1, ¶¶37-48.) A POSITA would have understood this set of circuits constitutes “a logic circuit.” Each of the third and fourth gate electrodes is a gate electrode of a transistor for an SRAM circuit. (Igarashi, ¶96.) Thus, Igarashi discloses or at least renders claim 14 obvious under Scenario B-1.

I. Claims 6 and 12

1. Claim 6

[6] The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

288. Igarashi renders obvious *“a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.”*

289. Specifically, Igarashi describes that the NMOS polysilicon gates in the memory array and the peripheral circuit are doped through **separate and distinct sequential steps** during the source/drain formation. Igarashi first discloses:

A N type impurity with low concentration is implanted to the source/drain region of an N channel MOS transistor, and the first impurity layer is formed. A mask is concretely covered to regions other than an N channel MOS transistor of a memory array.

Implantation of the arsenic (As) of about $0.5\text{E}+15 \sim 1\text{E}+15$ atoms/cm² is done to the first impurity layer that forms the source/drain region of the N channel MOS transistor of a memory array. Implantation of the arsenic (As) of about $0.5\text{E}+15 \sim 1\text{E}+15$ atoms/cm² is done also to the polysilicon gate which forms the gate region of the N channel MOS transistor of a memory array in this case. (Igarashi, ¶105.)

290. At a later step, Igarashi discloses that “a mask is covered to regions other than an N channel MOS transistor of a peripheral circuit. Implantation of the arsenic (As) of about $0.5\text{E}+15 \sim 1\text{E}+15$ atoms/cm² is done to the first impurity layer that forms the source/drain region of the N channel MOS transistor of a

peripheral circuit. Implantation of the arsenic (As) of about $0.5E+15 \sim 1E+15$ atoms/cm² is done also to the polysilicon gate which forms the gate region of the N channel MOS transistor of a peripheral circuit in this case.” (Igarashi, ¶106.)

291. Because these implant steps are **independent**, i.e., decoupled, and each uses dopant **dose ranges** rather than fixed values, a POSITA would have recognized the flexibility disclosed in Igarashi in adjusting dopant levels independently to obtain desired impurity concentrations and, therefore, would thus implement any of **three** disclosed outcomes, based on different design requirements:

- i. Peripheral NMOS gate has a higher impurity concentration than the memory NMOS gate (**LN (IR, AR) > SN (IR, AR)**);
- ii. Both polysilicon gates have equal impurity concentrations (**LN (IR, AR) $\approx$ SN (IR, AR)**); or
- iii. Peripheral NMOS gate has a lower impurity concentration than the memory array NMOS gate (**LN (IR, AR) < SN (IR, AR)**).

292. The impurity concentration relationship disclosed in Igarashi’s second embodiment can be expressed as follows:

Igarashi’s Second Embodiment
LP (IR, AR) > SP (IR, AR)
LN (IR, AR) > $\approx$ < SN (IR, AR)

293. These options are well-defined, predictable and technically straightforward for a POSITA to implement using routine process optimization.

294. The predictable nature of the electrical and performance characteristics resulting from varying impurity concentrations further supports the conclusion that experimentation within this finite set would not require inventive effort, but rather routine optimization.

295. In view of the above, the following table summarizes the impurity concentration relationship for claim 6 and Igarashi's impurity concentration relationship under Igarashi's second embodiment:

	Claimed Impurity Concentration Relationship Under All Scenarios	Igarashi's Impurity Concentration Relationship
A-1	LN(IR, AR) > SN(AR) LP(AR) < SP(AR)	
A-2	SN(IR, AR) > LN(AR) SP(AR) < LP(AR)	
B-1	SP(IR, AR) > LP(AR) SN(AR) < LN(AR)	LP (IR, AR) > SP (IR, AR) LN (IR, AR) > ≈ < SN (IR, AR)
B-2	SP(IR, AR) > LP(AR) LN(IR, AR) ≈ SN(AR)	

296. Accordingly, Igarashi discloses or at least renders obvious “*wherein a portion of the first silicon film of the second conductivity type located on the second active region [LN (AR)] has a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region [SN (AR)]*”.

2. Claim 12

[12P] The semiconductor device of claim 1, wherein

[12A] a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region, and

[12B] a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

297. The following table summarizes the impurity concentration relationship for claim 12 and Igarashi’s impurity concentration relationship under the second embodiment, when considering the different disclosed impurity concentrations discussed in §VII.I:

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$LN(AR) > SN(AR)$ $LP(AR) > SP(AR)$	
A-2	$SN(AR) > LN(AR)$ $SP(AR) > LP(AR)$	
B-1	$LP(AR) > SP(AR)$ $LN(AR) > SN(AR)$	$LP(IR, AR) > SP(IR, AR)$ $LN (IR, AR) > \approx < SN (IR, AR)$
B-2	$SP(AR) > LP(AR)$ $SN(AR) > LN(AR)$	

298. For the reasons discussed in §VII.E, Igarashi discloses the portion of the gate electrode over the first active region, $LP(AR)$, (“*the first silicon film of the first conductivity type located on the first active region*”) has a higher p-type impurity concentration (“*first-conductivity-type impurity concentration*”) than the portion of electrode over the third active region, $SP(AR)$, (“*the second silicon film of the first conductivity type located on the third active region*”). That is, $LP(AR) > SP(AR)$ in Igarashi’s second embodiment under scenario B-1, satisfying limitation [12A].

299. As discussed in §VII.I, $LN (IR, AR) > \approx < SN (IR, AR)$. Thus, a POSITA would have found it obvious to implement a configuration where the peripheral NMOS gate has a higher impurity concentration ($LN (IR, AR) > SN (IR, AR)$), expecting predictable device behavior as a result. The predictable

nature of the electrical and performance characteristics resulting from varying impurity concentrations further supports the conclusion that experimentation within this finite set would not require inventive skill, but rather routine optimization.

300. Thus, Igarashi discloses or at least renders obvious limitation [12B]: *“a portion of the first silicon film of the second conductivity type located on the second active region,”* [LN (AR)] e.g., corresponding to the polysilicon gate of the N channel MOS transistor in the peripheral circuit, *“has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region,”* [SN (AR)] e.g., corresponding to the polysilicon gate of the N channel MOS transistor in the memory array.

301. Accordingly, Igarashi discloses or at least renders obvious “a portion of the first silicon film of the first conductivity type located on the first active region [LP(AR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SP(AR)],” and “a portion of the first silicon film of the second conductivity type located on the second active region [LN(AR)] has a second-conductivity-type impurity concentration higher than that of a portion of

the second silicon film of the second conductivity type located on the fourth active region [SN(AR)].”

VIII. GROUND 4: Combination of Igarashi and Sumi Renders Claims 1-10 and 12-14 Obvious.

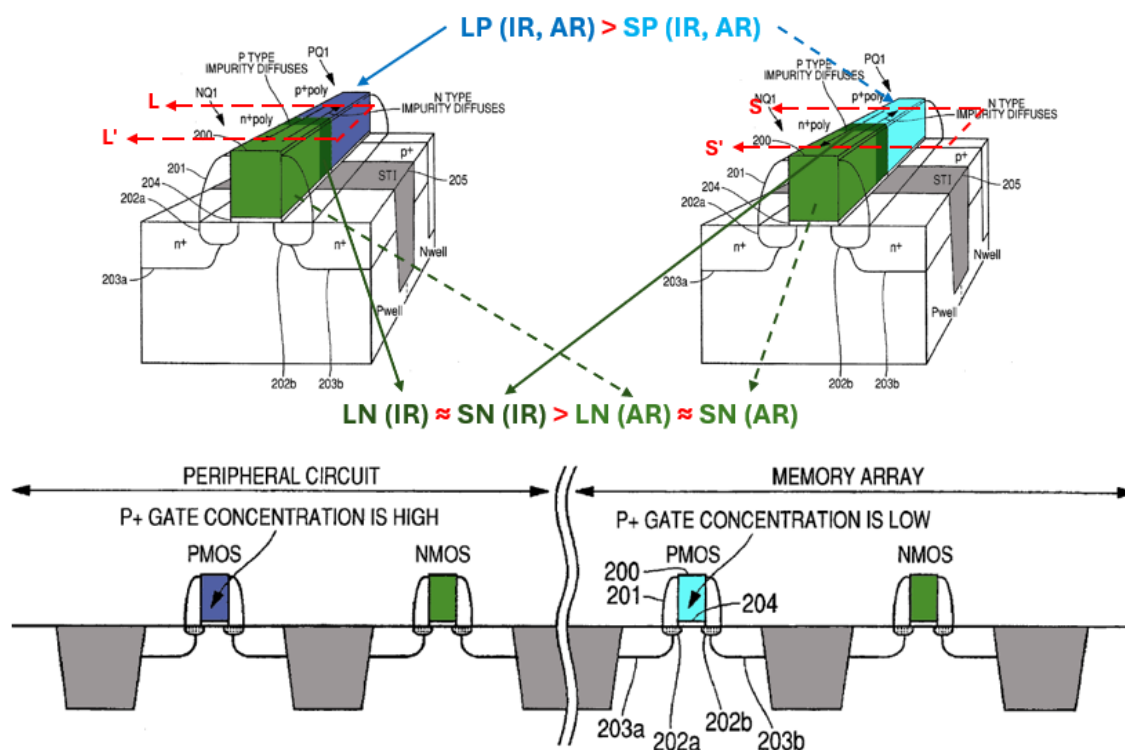
302. As discussed in §VII.B, Igarashi teaches or suggests claim 1 under Scenario B-1. To the extent an argument is made that Igarashi does not disclose limitations [1A] and [1F], it would have been obvious to a POSITA to combine Igarashi with Sumi’s teaching of a logic circuit with a dual-gate electrode, where the gate electrodes are connected to each other on an isolation region.

303. Igarashi does not explicitly disclose a dual-gate electrode having a portion of the silicon film located on an isolation region with a higher impurity concentration than the impurity concentration of a portion of the silicon film location on an active region, as recited in claims 5 and 7. Sumi provides this teaching, as discussed in §VI.B.2.

A. Overview of the Combination

304. A POSITA would have been motivated to combine Sumi’s teaching regarding use of a high-concentration region in dual-gate electrode structure into Igarashi’s dual-gate electrode structure. Specifically, a POSITA would have been motivated to form a high-concentration impurity region (e.g., region 21D) at the pn junction in Igarashi’s dual-gate electrode structure depicted in Figure 9 for both the peripheral (logic) circuit and SRAM circuits—i.e., over a portion of the STI

region, as taught by Sumi, as illustrated in Figure 9 below for both the peripheral (logic) and SRAM inverters.



Igarashi, Figure 9 (left and right-top), Figure 10 (bottom)

305. The impurity concentration relationship for Igarashi's second embodiment combined with Sumi, illustrated in the Figures 9 and 10 above, is

Igarashi's Second Embodiment + Sumi
LP (IR, AR) > SP (IR, AR)
LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)

306. Igarashi and Sumi are in the same field of endeavor as the '373 patent, semiconductor devices. (TSMC-1001, 3:42-46; Igarashi, ¶¶14-17, Sumi, ¶¶11, 13.)

307. A POSITA would have been motivated to make the above combination because both Igarashi and Sumi provide direct motivation to address the same problem. Igarashi observes that SRAM transistors are subject to more aggressively scaling than other transistors on a chip to increase the density of SRAM regions. (Igarashi, ¶¶4–7.) Igarashi further notes the “formation of [a] gate depletion [region due] to gate mutual [dopant] diffusion” leads to undesirable threshold voltage variations in CMOS transistor pairs used in SRAM. (Igarashi, ¶¶89–90.) Specifically, at the pn-junction of a dual-gate electrode in an SRAM transistor pair, p-type dopants diffuse into the n⁺ polysilicon gate electrode, while n-type dopants diffuse into the p⁺ polysilicon gate electrode; resulting in undesirable threshold voltage variations.

308. Similar to Tamaki, Igarashi addresses this variation by reducing the p-type impurity concentration in the polysilicon gate of the SRAM PMOS transistor, relative to the PMOS transistor in the peripheral circuit. (Igarashi, ¶¶92, 97.) Although Igarashi’s approach mitigates mutual dopant diffusion, it does not fully eliminate it. As such, a POSITA would recognize the limitations of Igarashi’s approach and be motivated to seek improvements to further enable SRAM scaling.

309. As discussed in §I.B.2, Sumi provides an explicit structural solution—using a high-concentration diffusion barrier at the junction—to suppress mutual dopant diffusion. Thus, Sumi directly motivates its combination with Igarashi. The

combination would reduce interdiffusion across the dual-gate electrode and minimize transistor variation, particularly in V_{th} , which is crucial for both SRAM and logic stability.

310. Finally, the combination is merely the application of a known technique (Sumi's high-doped pn-junction barrier in dual-gate structures) to a known structure (Igarashi's dual-gate layout in SRAM and logic), which was already recognized as needing improvement.

311. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable and beneficial. The Igarashi–Sumi combination would require only standard fabrication techniques to incorporate Sumi's high-concentration phosphorus-doped region into Igarashi's dual-gate structure. Implementing Sumi's approach in Igarashi's design would have been well within the ordinary skill of a POSITA and based on established semiconductor process integration practices prior to the '373 patent's priority date.

312. A POSITA would have understood the process steps for forming Sumi's high concentration phosphorous-doped region would be compatible with Igarashi's process steps, for at least two reasons. First, forming the high concentration region is an independent step requiring a dedicated photolithography mask for the phosphorous implant step at the pn junction over part of the isolation

structure, as discussed above in connection to Figure 6(2). (Sumi, ¶¶72-73.)

Second, Igarashi does not disclose any conflicting masks or process steps specifically targeting this pn junction, so incorporating Sumi's implant steps would not interfere with Igarashi's process flow.

313. For example, in connection with Figure 11E, Igarashi discloses forming a silicide-blocking oxide on the sidewall of Igarashi's polysilicon gates (Igarashi, ¶107), followed by source/drain formation implants for the P- and N-MOS transistors. (Igarashi, ¶¶108-110.) A POSITA would introduce Sumi's phosphorous-doped region prior to these source/drain implant steps, consistent with Sumi's own sequencing (Sumi, ¶¶73-75) and aligns with Igarashi's gate doping and processing order.

A. Independent Claim 1

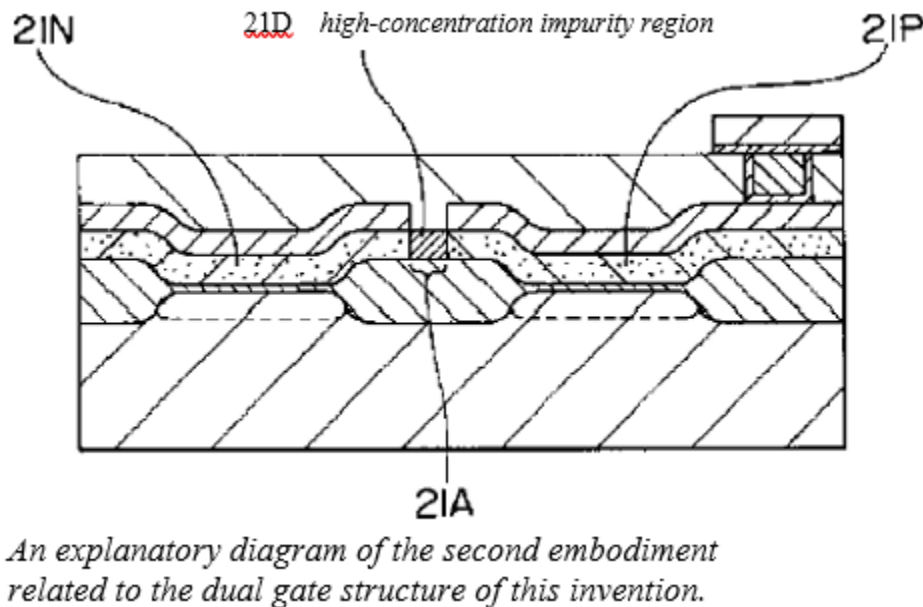
314. As discussed in §VII.B, Igarashi teaches or suggests claim 1. To the extent an argument is made that Igarashi does not disclose limitations [1A] and [1F], it would have been obvious to combine Igarashi with Sumi's teaching of a logic circuit with a dual-gate electrode, where the gate electrodes are connected to each other on an isolation region.

1. Limitations [1A] and [1F]

<i>[1A] a first dual-gate electrode; and</i>
--

[1F] the first gate electrode and the second gate electrode are connected to each other on the isolation region, and

315. Should an argument be made that Igarashi fails to disclose a dual-gate electrode in its logic circuit, Sumi provides those teachings and the combination discloses limitations [1A] and [1F]. Igarashi discloses limitations [1B]-[1E] for the reasons discussed in §VII.B.2. The combination of Igarashi and Sumi discloses limitation [1G] for the further reasons discussed below.



Sumi, Figure 5

316. A POSITA would have been motivated to apply the dual-gate structure of Sumi to Igarashi's logic circuit. First, as discussed in §VII.B.2, Igarashi suggests the use of a dual-gate structure for its peripheral circuits. Moreover, a POSITA would have recognized in standard CMOS/CMIS layout practices, an isolation region is used to electrically isolate adjacent diffusion

regions. However, when a continuous gate electrode spans across two separate active regions physically separated by an isolation structure, the gate electrode necessarily passes over the intervening isolation region. This results in a shared gate electrode that controls two distinct channel regions, one in each active area, thereby forming two transistors that are connected on the isolation region. The connection occurs via the continuous gate, not through diffusion or direct substrate contact, while the isolation structure maintains electrical separation between the underlying source/drain regions. This type of configuration is common in logic circuits and SRAM cells, where compact layouts and shared control of complementary transistors (e.g., PMOS and NMOS) are often required. Accordingly, when two active regions are separated by an isolation structure, a gate electrode spans laterally across both active areas and the intervening isolation structure, and a circuit calls for shared gate control, like an inverter, then the two gate electrodes would be connected on the isolation structure. These configurations are well-understood by circuit designers and layout engineers and are widely used in standard cell libraries and SRAM or logic blocks.

317. Accordingly, the Igarashi-Sumi combination discloses limitations [1A] and [1F].

2. Impurity Concentration Limitation [1G]

[1G] *at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.*

318. As discussed in §VIII.A, the impurity concentration relationship for Igarashi’s second embodiment combined with Sumi is:

Igarashi’s Second Embodiment + Sumi
LP (IR, AR) > SP (IR, AR)
LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)

319. The combination of Igarashi and Sumi therefore also discloses [1G] under Scenarios A-1 and A-2 (first conductivity type = **n-type**; second conductivity type = **p-type**) as well as B-1 (first conductivity type = **p-type**; second conductivity type = **n-type**):

Scenario A-1: “*at least a portion of the first silicon film of the first conductivity type [LN(IR)] has a first-conductivity-type impurity concentration” (n-type) higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SN (AR)]*”

Scenario A-2: “*at least a portion of the first silicon film of the first conductivity type [SN(IR)] has a first-conductivity-type impurity concentration” (n-type) higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [LN (AR)]*”

Scenario B-1: “*at least a portion of the first silicon film of the first conductivity type [LP(IR, AR)] has a first-conductivity-type impurity*

concentration” (**p-type**) higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [**SP(AR)**]”

320. The following table summarizes the impurity concentration relationship for limitation [1G] and Igarashi’s impurity concentration relationship for Igarashi’s second embodiment combined with Sumi:

	Claimed Impurity Concentration Relationship	Igarashi + Sumi Impurity Concentration Relationship
A-1	LN(IR or AR) > SN(AR)	LN (IR) > SN (AR)
A-2	SN(IR or AR) > LN(AR)	SN (IR) > LN (AR)
B-1	LP(IR or AR) > SP(AR)	LP(IR, AR) > SP(IR, AR)
B-2	SP(IR or AR) > LP(AR)	

B. Claims 2-4 and 8, 11-14

321. The Igarashi-Sumi device renders obvious claims 2-4, 8, and 11-14 for the reasons discussed in §§VII.C, VII.D, VII.E, VII.F, VII.I.2, and VII.H under Scenario B-1.

C. Claims 5 and 7

[5] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

[7] The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion

of the first silicon film of the second conductivity type located on the isolation region.

322. Claim 5 differs from claim 7 in that it requires that the impurity concentration of the “*first gate electrode*” be lower at a portion located at the first active region compared to a portion located at the isolation region, while claim 7 requires that the impurity concentration of the “*second gate electrode*” is lower at a portion located at the second active region compared to a portion located at the isolation region.

323. The following table summarizes the impurity concentration relationship for claim 5 and the impurity concentration relationship of the Igarashi and Sumi device under the second embodiment.

	Claimed Impurity Concentration Relationship	Igarashi + Sumi Impurity Concentration Relationship
A-1	LN(IR) > LN(AR) > SN(AR)	LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)
A-2	SN(IR) > SN(AR) > LN(AR)	LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)
B-1	LP(IR) > LP(AR) > SP(AR)	
B-2	SP(IR) > SP(AR) > LP(AR)	

324. The Igarashi and Sumi combination discloses claim 5 under scenario A-1. That is the Igarashi and Sumi combination discloses “*a portion of the first*

silicon film of the first conductivity type located on the first active region

[LN(AR)] has a first-conductivity-type impurity concentration [n-type] lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region [LN(IR)].”

325. The Igarashi-Sumi combination also discloses claim 5 under Scenario A-2. That is the Igarashi and Sumi combination discloses “*a portion of the first silicon film of the first conductivity type located on the first active region [SN(AR)] has a first-conductivity-type impurity concentration [n-type] lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region [SN(IR)].*”

326. The following table summarizes the impurity concentration relationship for claim 7 and the impurity concentration relationship of the Igarashi and Sumi device under the second embodiment.

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	$LN(IR, AR) > SN(AR)$ $LP(AR) < LP(IR)$	
A-2	$SN(IR, AR) > LN(AR)$ $SP(AR) < SP(IR)$	
B-1	$LP(IR, AR) > SP(AR)$ $LN(AR) < LN(IR)$	$LP (IR, AR) > SP (IR, AR)$ $LN (IR) \approx SN (IR) > LN (AR) \approx SN (AR)$
B-2	$SP(IR, AR) > LP(AR)$ $SN(AR) < SN(IR)$	

327. The Igarashi and Sumi combination discloses claim 7 under Scenario B-1. That is, the Igarashi and Sumi combination discloses “a portion of the first silicon film of the second conductivity type located on the second active region [LR(AR)] has a second-conductivity-type impurity concentration [n-type] lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region [LR(IR)].”

D. Claim 6

[6] The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

328. The following table summarizes the impurity concentration relationship for claim 6 and the impurity concentration relationship of the Igarashi and Sumi device under the second embodiment (§VIII.A.2):

	Claimed Impurity Concentration Relationship Under All Scenarios	Igarashi + Sumi Impurity Concentration Relationship
A-1	$\text{LN}(\text{IR}, \text{AR}) > \text{SN}(\text{AR})$ $\text{LP}(\text{AR}) < \text{SP}(\text{AR})$	
A-2	$\text{SN}(\text{IR}, \text{AR}) > \text{LN}(\text{AR})$ $\text{SP}(\text{AR}) < \text{LP}(\text{AR})$	$\text{LN}(\text{IR}) \approx \text{SN}(\text{IR}) > \text{LN}(\text{AR}) \approx \text{SN}(\text{AR})$ $\text{LP}(\text{IR}, \text{AR}) > \text{SP}(\text{IR}, \text{AR})$
B-1	$\text{SP}(\text{IR}, \text{AR}) > \text{LP}(\text{AR})$ $\text{SN}(\text{AR}) < \text{LN}(\text{AR})$	
B-2	$\text{SP}(\text{IR}, \text{AR}) > \text{LP}(\text{AR})$ $\text{LN}(\text{IR}, \text{AR}) \approx \text{SN}(\text{AR})$	

329. The Igarashi and Sumi combination discloses claim 6 under Scenario A-2. That is, the Igarashi and Sumi combination discloses “a portion of the first silicon film of the second conductivity type located on the second active region [$\text{SP}(\text{AR})$] has a second-conductivity-type impurity concentration [p-type] lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region [$\text{LP}(\text{AR})$].”

E. Claim 9

[9] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

330. The following table summarizes the impurity concentration relationship for claim 9 and the impurity concentration relationship of the Igarashi and Sumi device under the second embodiment (§VIII.A.2).

	Claimed Impurity Concentration Relationship	Igarashi + Sumi Impurity Concentration Relationship
A-1	LN(IR) > SN(AR)	$LN(IR) \approx SN(IR) > LN(AR) \approx SN(AR)$ $LP(IR, AR) > SP(IR, AR)$
A-2	SN(IR) > LN(AR)	$LN(IR) \approx SN(IR) > LN(AR) \approx SN(AR)$ $LP(IR, AR) > SP(IR, AR)$
B-1	LP(IR) > SP(AR)	$LP(IR, AR) > SP(IR, AR)$ $LN(IR) \approx SN(IR) > LN(AR) \approx SN(AR)$
B-2	SP(IR) > LP(AR)	

331. The Igarashi and Sumi combination renders claim 9 obvious under Scenario A-1. That is, the Igarashi and Sumi combination renders obvious a “portion of logic NMOS gate electrode over the isolation region, **LN(IR)**, (“the

first silicon film of the first conductivity type located on the isolation region”) has a higher n-type impurity concentration (*“first-conductivity-type impurity concentration”*) than the portion of SRAM NMOS gate electrode over the active region, **SN(AR)**, (*“the second silicon film of the first conductivity type located on the third active region”*). That is, **LN(IR) > SN(AR)** in Igarashi’s second embodiment under Scenario A-1 renders obvious claim 9.

332. The Igarashi and Sumi combination also renders claim 9 obvious under Scenario A-2. That is, the Igarashi and Sumi combination renders obvious a portion of SRAM NMOS gate electrode over the isolation region, **SN(IR)**, (*“the first silicon film of the first conductivity type located on the isolation region”*) has a higher n-type impurity concentration (*“first-conductivity-type impurity concentration”*) than the portion of logic NMOS gate electrode over the active region, **LN(AR)**, (*“the second silicon film of the first conductivity type located on the third active region”*). That is, **SN(IR) > LN(AR)** in Igarashi’s second embodiment under Scenario A-2.

333. Finally, for the same reasons discussed in §VII.G, the Igarashi and Sumi combination renders obvious claim 9 under scenario B-1.

F. Claim 10

[10] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a

portion of the second silicon film of the first conductivity type located on the third active region.

334. The following table summarizes the impurity concentration relationship for claim 10 and the impurity concentration relationship of the Igarashi and Sumi device under the second embodiment (§VIII.A.2):

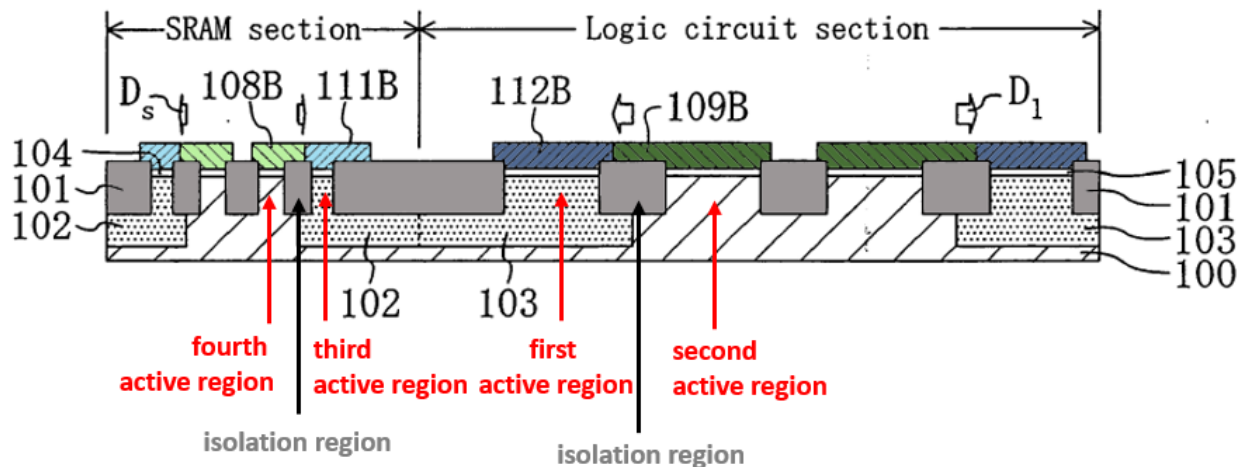
	Claimed Impurity Concentration Relationship Under All Scenarios	Igarashi + Sumi Impurity Concentration Relationship
A-1	LN(AR) > SN(AR)	LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)
A-2	SN(AR) > LN(AR)	LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)
B-1	LP(AR) > SP(AR)	
B-2	SP(AR) > LP(AR)	

335. The Igarashi and Sumi combination renders claim 9 obvious under Scenario A-1. That is, the Igarashi and Sumi combination renders obvious “a portion of the first silicon film of the first conductivity type located on the first active region [LN(AR)] has a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region [SN(AR)]” under Scenario A-1.

336. The Igarashi and Sumi combination also renders claim 9 obvious under Scenario A-2. That is, the Igarashi and Sumi combination renders obvious “a portion of the first silicon film of the first conductivity type located on the first active region [SN (AR)] has a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region [LN(AR)]” under Scenario A-2.

IX. GROUNDS 5-6: The Combination of Igarashi with Tamaki (Ground 5) or the Combination of Igarashi and Sumi with Tamaki (Ground 6) Each Renders Claim 2 Obvious.

337. To the extent Patent Owner argues that Igarashi does not disclose or suggest the limitation of claim 2, Tamaki provides this teaching as discussed in §V.B.3(b). (See, e.g., ¶¶83, 116, Figure 3B (below), Figure 5B.)



Tamaki, Figure 3B

338. Accordingly, the Igarashi and Tamaki (Ground 5) combination and The Igarashi, Sumi, and Tamaki combination (Ground 6) each discloses “*an isolation width between the first active region,*” e.g., below electrode 112A, “*and the second active region,*” e.g., below electrode 109A, *is larger than [an isolation width] between the third active region,*” e.g., below electrode 111A, *and the fourth active region,*” e.g., below electrode 108A, satisfying claim 2.

339. A POSITA would have been motivated to combine Tamaki’s teachings of an isolation region that has a larger width between active regions in a logic circuit compared to the width between active regions in an SRAM circuit with Igarashi’s or Igarashi-Sumi’s dual-gate electrode semiconductor devices in the peripheral circuit area and the memory array area.

340. First, Igarashi, Sumi, and Tamaki are in the same field of endeavor as the ’373 patent, e.g., semiconductor devices. (*Compare* TSMC-1001, 3:42-46, *with* Igarashi, ¶¶14-17 *and* Tamaki, ¶¶3, 147.)

341. Second, Tamaki motivates the combination by teaching transistor layout techniques that directly address the need to control variability, leakage currents, and performance across different functional blocks in an integrated circuit. Specifically, Tamaki discloses forming gate electrodes with different widths and layouts depending on the performance and leakage needs of specific circuit regions, such as logic and memory. (*See, e.g.,* Tamaki, ¶¶82-83, 109-112,

141-144.) Tamaki explains that gate width and layout can be adjusted to manage threshold voltage variation and process-induced fluctuations, which become increasingly problematic as device dimensions shrink. (*See, e.g.*, Tamaki, ¶147.) Igarashi, in turn, describes a semiconductor device structure that includes dual-gate electrodes formed on isolated active regions, with impurity concentrations tailored to provide different threshold voltages. It also emphasizes the need to reduce memory cell sizes and mitigate process variation in high-density SRAM arrays. (*See, e.g.*, Igarashi, ¶¶4-5.)

342. U.S. Patent No. 8,355,269 to Zampaglione (“Zampaglione”) confirms that SRAM bit cells are typically formed using *tighter design rules* than those applied to general-purpose logic transistors on the same chip. Zampaglione discloses that SRAM layouts use reduced feature sizes and spacings compared to the rest of the integrated circuit, which includes logic circuitry. (Zampaglione, 3:58-64.) A POSITA would have understood that this difference in scaling implies that the *isolation width in SRAM regions*—which must support high-density layout—would also be smaller than the isolation widths used in logic circuitry, such as the row decoder, write circuit, readout circuitry, column selection circuitry, main control circuit, and word line drive circuit as depicted in Igarashi’s Figure 1.

343. Moreover, a POSITA would have understood that to implement Igarashi’s dual-gate structure where both SRAM and logic circuits coexist, it

would be necessary to adopt layout strategies that accommodate the differing electrical and spatial requirements of these circuits. Specifically, SRAM circuits prioritize compactness and low leakage, while logic circuits often require stronger isolation to ensure robust signal integrity and prevent noise coupling. Tamaki's guidance directly aligns with these layout challenges by offering a framework to differentiate transistor geometry and spacing based on circuit function. This dichotomy in design priorities would naturally lead a POSITA to consider modifying the isolation widths between active regions depending on their function. Tamaki's guidance directly aligns with these layout challenges by offering a framework to differentiate transistor geometry and spacing based on circuit function. The predictable relationship between isolation spacing and functional performance—especially in terms of leakage, capacitance, and noise margin—would have further reinforced a POSITA's motivation to apply Tamaki's layout teachings to optimize Igarashi's dual-gate structures.

344. Tamaki reinforces this design perspective by teaching that varying the layout and physical dimensions of transistors, such as gate width and spacing, can help optimize performance across different circuit types. (*See, e.g., Tamaki, ¶32.*) Thus, applying Tamaki's teaching to Igarashi's structure, a POSITA would have found it obvious to increase the isolation width between the first and second active

regions (e.g., assigned to logic circuits) while reducing it between the third and fourth active regions (e.g., assigned to SRAM circuits).

345. Moreover, the combination involves only routine design considerations within the capabilities of a POSITA. It would have been obvious to a POSITA at the time to adopt well-known layout differentiation techniques, such as those taught by Tamaki, to further optimize Igarashi's structure for embedded memory applications, particularly where isolation width impacts both device performance and area efficiency.

346. Finally, the combination is nothing more than the application of a known technique (Tamaki's fabrication of dual-gate electrode devices) to a known device (Igarashi's logic circuit and SRAM section) ready for improvement for the reasons discussed above.

347. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable. The Igarashi-Tamaki combination would merely implement standard fabrication techniques to fabricate Tamaki's semiconductor devices in Igarashi's integrated system. Implementing Tamaki's teachings into Igarashi's system would have been well within the skill set of a POSITA because the combination involves standard fabrication techniques and concepts well understood before the earliest priority date of the '373 patent.

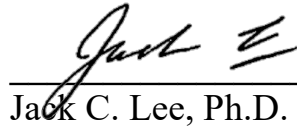
X. Conclusion

348. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 15th day of July, 2025, in Austin, TX.

Respectfully submitted,



Jack C. Lee, Ph.D.