

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner.

IPR2025-01302

U.S. Patent 8,884,373

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT 8,884,373**

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent 8,884,373 to Sato et al. (“the ’373 patent”)
1002	File History of U.S. Patent 8,884,373 (“’373 File History”)
1003	Declaration of Dr. Jack Lee in Support of IPR Petition
1004	CV of Dr. Jack Lee
1005	Translated Excerpts from File History of Japanese Patent No. 5857225 to Sato et al. (“JP ’225 patent”) (Japanese counterpart of the ’373 Patent)
1006	U.S. Publication 2008/0036010 to Tamaki, et al. (“Tamaki”)
1007	U.S. Publication 2008/0042218 to Igarashi, et al. (“Igarashi”)
1008	Japanese Patent No. 9181194 to Sumi (“Sumi”)
1009	Certified Translation of Japanese Patent No. 9181194 to Sumi
1010	U.S. Publication 2009/0096031 to Ekbote, et al. (“Ekbote”)
1011	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1012	Weste, “CMOS VLSI Design: A Circuits and Systems Perspective” (Third Edition, 2005) (“Weste”)
1013	Wolf, “Silicon Processing for the VLSI Era, Volume 4 – DeepSubmicron Process Technology” (2002) (“Wolf-4”)
1014	Van Zant, “Microchip Fabrication” (Fifth Edition, 2004) (“Van Zant”)
1015	“International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures” (2007 Edition) (“ITRS”)
1016	U.S. Patent No. 8,355,269 to Zampaglione (“Zampaglione”)

Exhibit	Description
1017	Sze, “Semiconductor Devices: Physics and Technology” (2nd Edition) (2002) (“Sze”)
1018	U.S. Patent 5,208,184 to Bayraktaroglu (“Bayraktaroglu”)

I. Introduction

Taiwan Semiconductor Manufacturing Company, Limited petitions for *inter partes* review of claims 1-14 of U.S. Patent 8,883,373 (“’373 patent”; TSMC-1001).

II. Grounds for Standing

Petitioner certifies the ’373 patent is available for IPR and it is not barred or estopped from requesting IPR.

III. Identification of Challenge

A. Prior Art

The ’373 patent, filed October 31, 2012, is a continuation of PCT/JP2011/006167 which claims priority to JP2011-068131, filed March 25, 2011. Petitioner does not acquiesce the ’373 patent is entitled to the benefit of the filing date of either application. Regardless, each applied reference was filed or published before March 25, 2011.

1. **U.S. Publication 2008/0036010 to Tamaki et al.** (“Tamaki”; TSMC-1006), published February 14, 2008, is prior art under 35 U.S.C. §102(b).¹

2. **U.S. Publication 2008/0042218 to Igarashi et al.** (“Igarashi”; TSMC-1007), published February 21, 2008, is prior art under 35 U.S.C. §102(b).

¹ Pre-AIA 35 U.S.C. §102 applies.

3. **Japanese Patent 9181194 to Sumi** (“Sumi”; TSMC-1008), published July 11, 1997, is prior art under 35 U.S.C. §102(b).

B. Grounds for Challenge

Ground		Claims	Prior Art
1	103	1-4, 8-9, 11-14	Tamaki
2	103	5, 7	Tamaki+Sumi
3	103	1-4, 6, 8-14	Igarashi
4	103	1-14	Igarashi+Sumi
5	103	2	Igarashi+Tamaki
6	103	2	Igarashi+Sumi+Tamaki

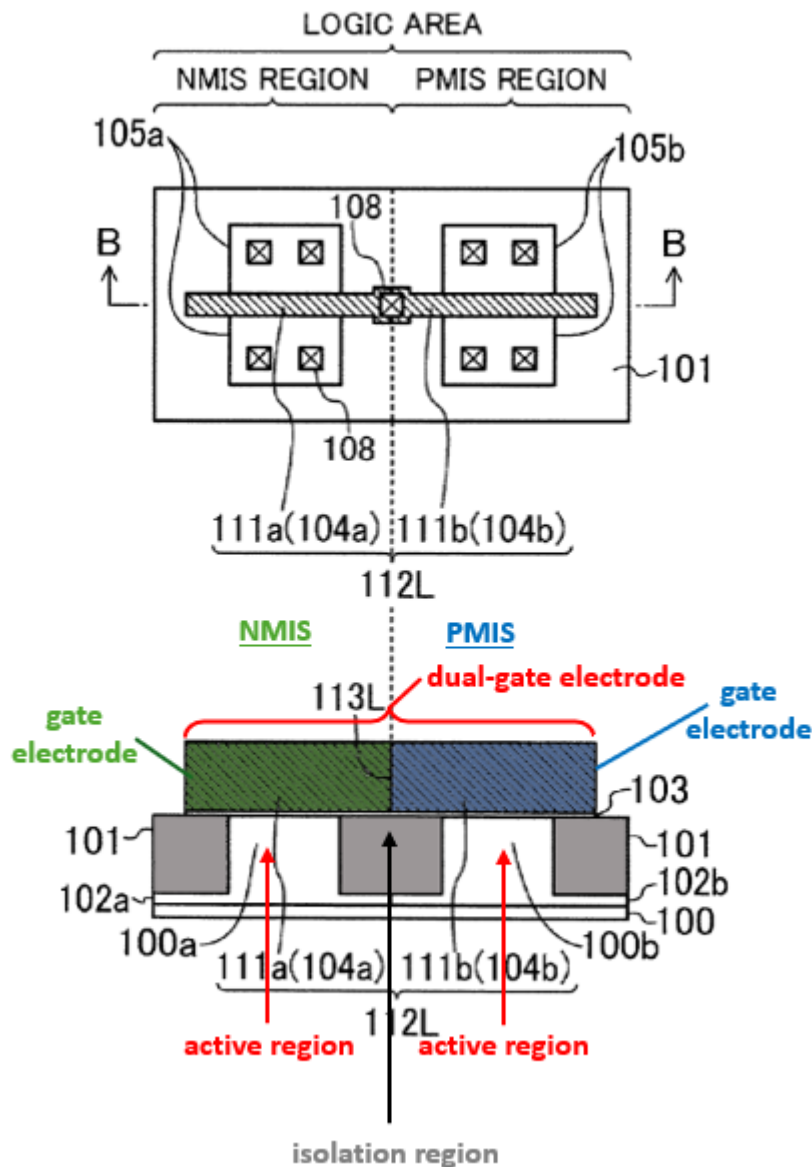
IV. ’373 Patent

The ’373 patent relates “to a semiconductor device having a complementary metal insulator semiconductor (CMIS)² dual-gate structure.” (TSMC-1001, 1:15-20.) The ’373 patent admits such dual-gate CMIS structures were known.

² A “CMIS” (“Complementary Metal-Insulator-Semiconductor”) is also referred to as “CMOS” (“Complementary Metal-**O**xide-Semiconductor”) when the insulator is an oxide. (TSMC-1003, ¶50 n1.)

A. Applicant Admitted Prior Art (“AAPA”)

The '373 patent's background describes a “conventional semiconductor device” having “a transistor for a logic circuit and a transistor for a static random-access memory (SRAM) circuit.” (TSMC-1001, 1:48-52.) The logic circuit comprises dual-gate electrode 112L having gate electrode 111a including n-type polysilicon film 104a (green) on active region 100a and gate electrode 111b including p-type polysilicon film 104b (blue) on active region 100b. (TSMC-1001, 2:11-16, Figures 15A-B (below).) Gate electrode 111a and gate electrode 111b “are connected to each other at a PN boundary 113L” between active region 100a and active region 100b on isolation region 101 (gray). (TSMC-1001, 2:16-20.)



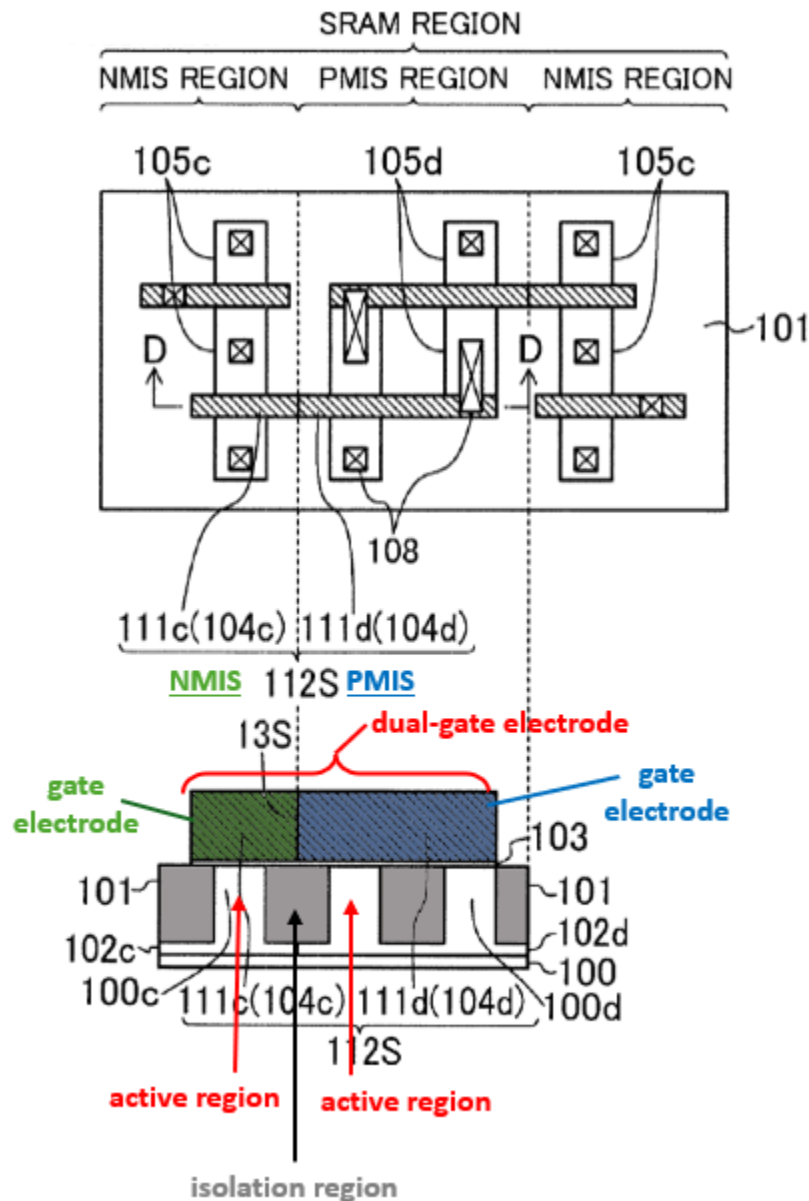
'373 Patent, Figures 15A (top), 15B (bottom): AAPA

The SRAM circuit comprises dual-gate electrode 112S having gate electrode 111c including n-type polysilicon film 104c (green) on active region 100c and gate electrode 111d including p-type polysilicon film 104d (blue) on active region 100d. (TSMC-1001, 2:27-32, Figures 15C-D (below).) Gate electrode 111c and

gate electrode 111d “are connected to each other at a PN boundary 1135 [sic]”

between active region 100c and active region 100d on isolation region 101 (gray).

(TSMC-1001, 2:32-36.)



'373 Patent, Figures 15C (top), 15D (bottom): AAPA

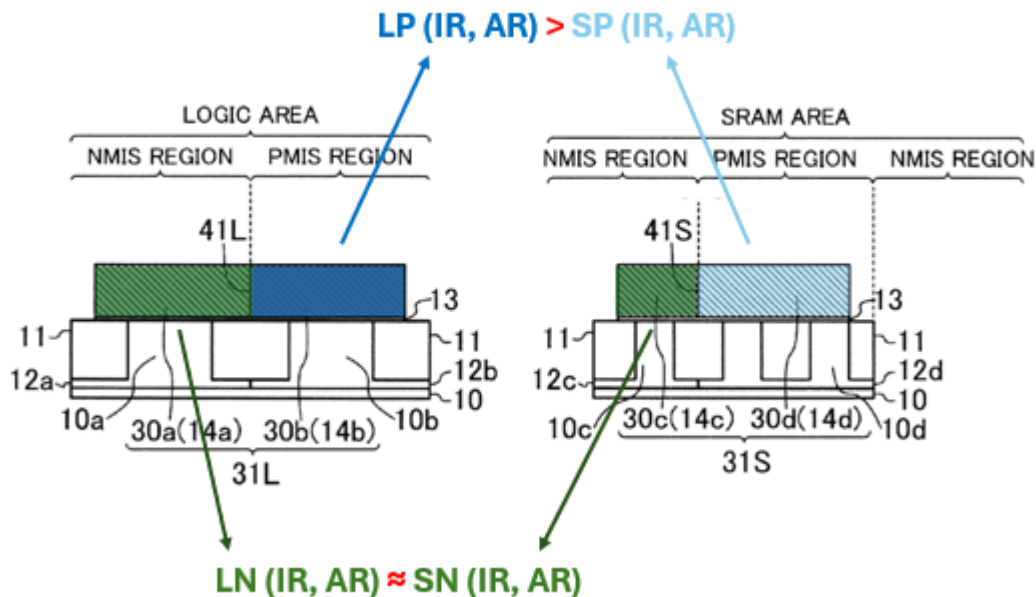
In this conventional CMIS dual-gate structure, “p-type polysilicon films 104b and 104d have substantially the same concentration of the p-type impurity” and “n-type polysilicon films 104a and 104c have substantially the same concentration of the n-type impurity.” (TSMC-1001, 2:53-55, 2:60-62, Figures 16A-B.)

B. '373 Patent

The '373 patent merely modifies this known CMIS dual-gate structure by varying the doping concentrations of the PMIS and NMIS gate electrodes of the logic and SRAM sections. Specifically, the '373 patent presents four exemplary embodiments with different arrangements of impurity concentrations. (TSMC-1001, 7:47-14:51 (first); 14:53-18:35 (second); 18:37-22:14 (third); 22:16-24:57 (fourth).)

First Embodiment: The “p-type impurity concentration in the entire p-type silicon film 14b [dark blue] is higher than that in the entire p-type silicon film 14d [light blue].” (TSMC-1001, 8:47-49.) The “n-type impurity concentration of the n-type silicon film 14a [green] is substantially equal to that of the n-type silicon film 14c [green].” (TSMC-1001, 8:50-52.) The relationship above can be expressed using the following shorthand notation:

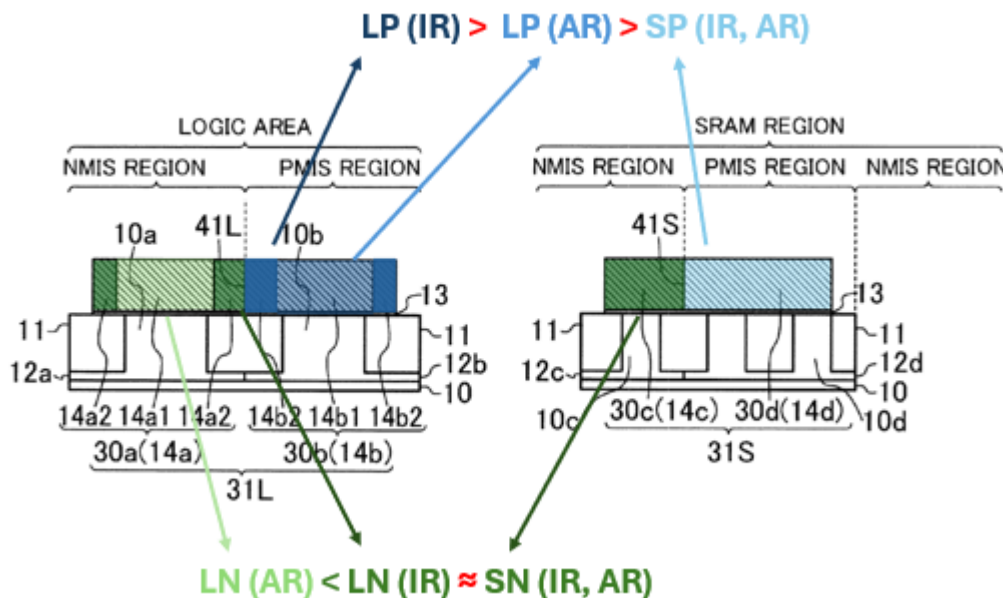
LP (IR, AR) > SP (IR, AR)	LN (IR, AR) $\approx$ SN (IR, AR)
LP: Logic-PMIS gate electrode (IR, AR): Each of IR and AR LP (IR, AR): Portion of logic-PMIS gate electrode over isolation region (IR) or portion over active region (AR) SP: SRAM-PMIS gate electrode SP (IR, AR): Portion of SRAM-PMIS gate electrode over IR or portion over AR	LN: Logic-NMIS gate electrode LN (IR, AR): Portion of ogic-NMIS gate electrode over IR or portion over AR SN: SRAM-NMIS gate electrode SN (IR, AR): Portion of SRAM-NMIS gate electrode over IR or portion over AR
> : higher than (impurity concentration) $\approx$: substantially equal to (impurity concentration)	



'373 Patent, Figures 1B(left), 1D(right)

Second Embodiment: The “p-type silicon film 14b1 [on active region; blue] has a p-type impurity concentration lower than that of the p-type silicon film 14b2 [on shallow trench isolation (STI); dark blue]” and “each of the p-type silicon film 14b1 and the p-type silicon film 14b2 has a p-type impurity concentration higher than that of the p-type silicon film 14d [light blue].” (TSMC-1001, 15:28-33.) The “n-type silicon film 14a1 [on active region; light green] has an n-type impurity concentration lower than that of each of the n-type silicon film 14a2 [on STI; dark green] and the n-type silicon film 14c” and “n-type silicon film 14a2 has an n-type impurity concentration substantially equal to that of the n-type silicon film 14c.” (TSMC-1001, 15:33-37.) The relationship above can be expressed using the following shorthand notation:

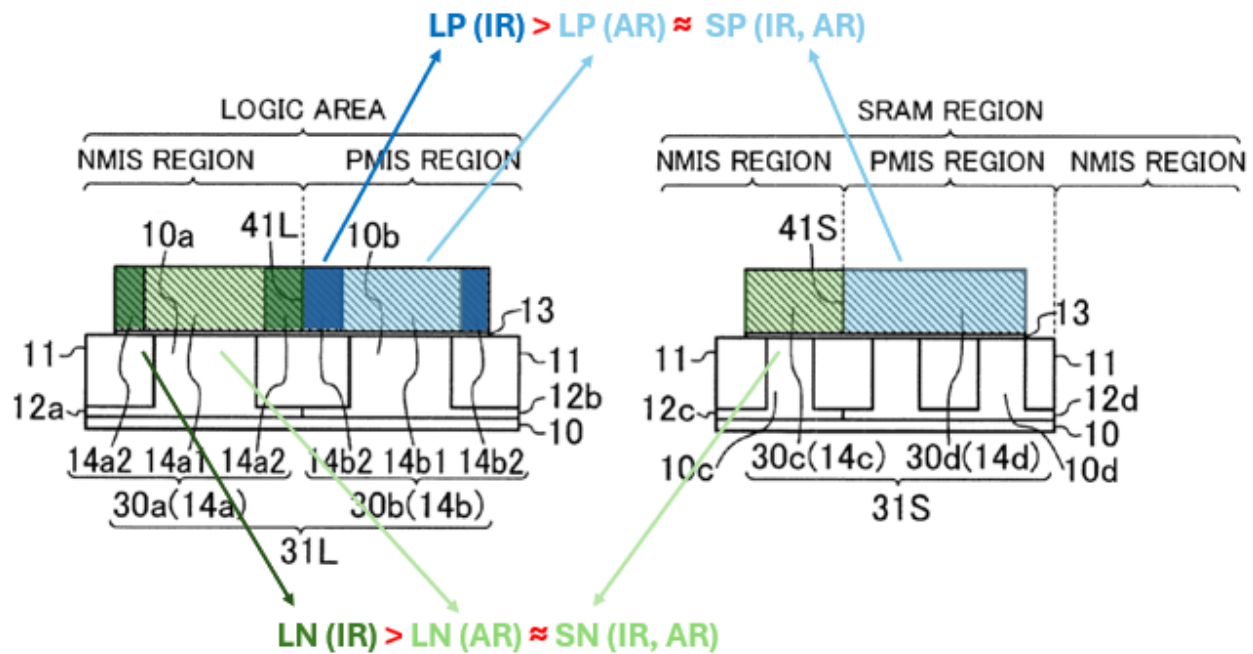
$\begin{aligned} & \text{LP (AR)} < \text{LP (IR)} \\ & + \\ & \text{LP (AR)} > \text{SP (IR, AR)} \\ & \text{LP (IR)} > \text{SP (IR, AR)} \end{aligned}$ that is: $\text{SP (IR, AR)} < \text{LP (AR)} < \text{LP (IR)}$	$\begin{aligned} & \text{LN (AR)} < \text{LN (IR)} \\ & \text{LN (AR)} < \text{SN (IR, AR)} \\ & + \\ & \text{LN (IR)} \approx \text{SN (IR, AR)} \end{aligned}$ that is: $\text{LN (AR)} < \text{LN (IR)} \approx \text{SN (IR, AR)}$
LP (AR): Portion of logic-PMIS gate electrode over AR LP (IR): Portion of logic-PMIS gate electrode over IR SP (IR, AR): Portion of SRAM-PMIS gate electrode over IR or portion over AR	LN(AR): Portion of logic-NMIS gate electrode over AR LN (IR): Portion of logic-NMIS gate electrode over IR SN (IR, AR): Portion of SRAM-NMIS gate electrode over IR or portion over AR
< : lower than (impurity concentration)	



'373 Patent, Figures 9B(left), 9D(right)

Third Embodiment: The “p-type silicon film 14b2 [on STI; dark blue] has a p-type impurity concentration higher than that of the p-type silicon film 14d and that the p-type silicon film 14b1 [on active; light blue] has a p-type impurity concentration substantially equal to that of the p-type silicon film 14d.” (TSMC-1001, 19:16-20.) The “n-type silicon film 14a1 [on active; light green] has an n-type impurity concentration substantially equal to that of the n-type silicon film 14c” and “n-type silicon film 14a1 has an n-type impurity concentration lower than that of the n-type silicon film 14a2 [on STI; dark green].” (TSMC-1001, 19:22-26.) The relationship above can be expressed using the following shorthand notation:

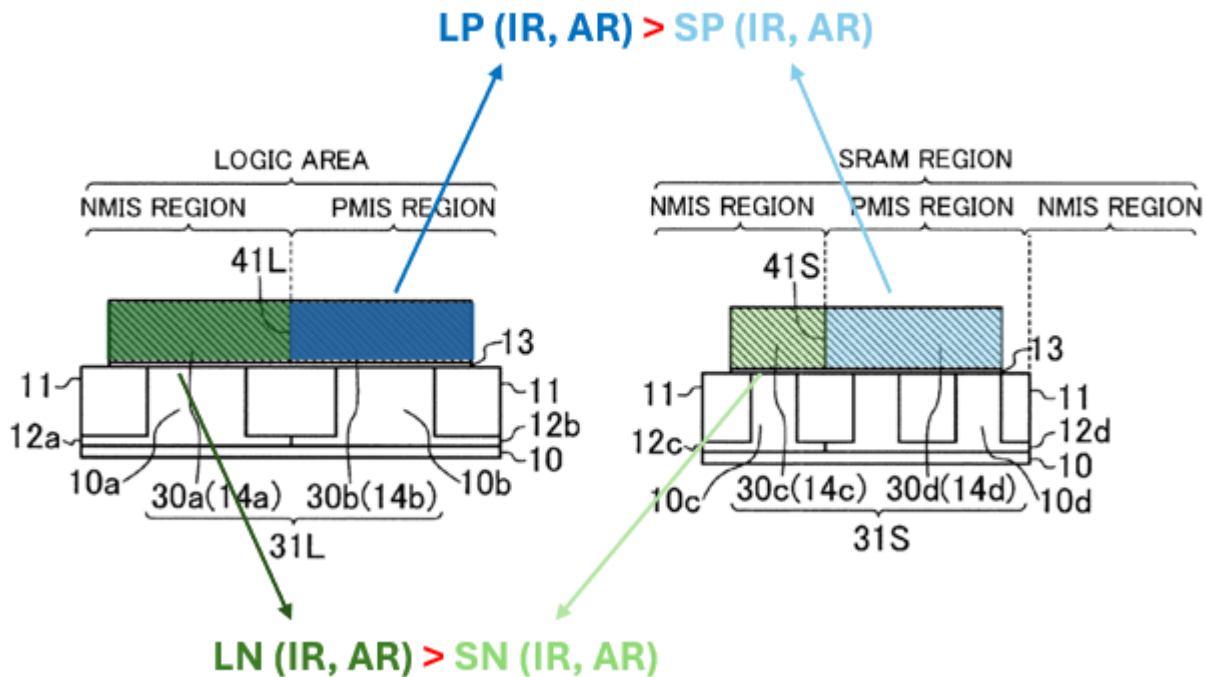
$\begin{array}{c} \text{LP (IR)} > \text{SP (IR, AR)} \\ + \\ \text{LP (AR)} \approx \text{SP (IR, AR)} \end{array}$ <u>that is:</u> $\text{LP (IR)} > \text{LP (AR)} \approx \text{SP (IR, AR)}$	$\begin{array}{c} \text{LN (AR)} \approx \text{SN (IR, AR)} \\ + \\ \text{LN (AR)} < \text{LN (IR)} \end{array}$ <u>that is:</u> $\text{LN (IR)} > \text{LN (AR)} \approx \text{SN (IR, AR)}$
LP (AR): Portion of Logic-PMIS gate electrode over AR LP (IR): Portion of Logic-PMIS gate electrode over IR SP (IR, AR): Portion of SRAM-PMIS gate electrode over IR or portion over AR	LN(AR): Portion of Logic-NMIS gate electrode over AR LN (IR): Portion of Logic-NMIS gate electrode over IR SN (IR, AR): Portion of SRAM-NMIS gate electrode over IR or portion over AR



'373 Patent, Figures 11B(left), 11D(right)

Fourth Embodiment: The “p-type silicon film 14b has a p-type impurity concentration higher than that of the p-type silicon film 14d” and “the n-type silicon film 14a has an n-type impurity concentration higher than that of the n-type silicon film 14c.” (TSMC-1001, 22:57-61.) The relationship above can be expressed using the following shorthand notation:

LP (IR, AR) > SP (IR, AR)	LN (IR, AR) > SN (IR, AR)
LP (IR, AR): Portion of Logic-PMIS gate electrode over isolation region (IR) or portion over (AR) SP (IR, AR): Portion of SRAM-PMIS gate electrode over IR or portion over AR	LN (IR, AR): Portion of Logic-NMIS gate electrode over IR or portion over AR SN (IR, AR): Portion of SRAM-NMIS gate electrode over IR or portion over AR



'373 Patent, Figures 13B(left), 13D(right)

C. Independent Claim 1

The sole independent claim recites “*a first dual-gate electrode*” and “*a second dual-gate electrode*” but does not limit either to use in a specific type of

transistor (e.g., logic or SRAM). Therefore, the independent claim covers the following arrangement:

	1	2
<i>“first dual-gate electrode”</i>	Logic	SRAM
<i>“second dual-gate electrode”</i>	SRAM	Logic

The independent claim further recites the *“dual-gate electrode[s]”* include a *“first/third gate electrode”* each having a *“silicon film”* of a ***“first conductivity type”*** and a *“second/fourth gate electrode”* each having a *“silicon film”* of a ***“second conductivity type.”*** However, the claim does not limit the *“first”* or *“second”* *“conductivity type”* to a specific type (e.g., n-type or p-type). Therefore, the claim also covers the following arrangements:

- A: first conductivity type = **n-type**
second conductivity type = **p-type**
- B: first conductivity type = **p-type**
second conductivity type = **n-type**

Accordingly, independent claim 1 encompasses at least the following four scenarios³:

³ Claim 13 encompasses only Scenarios A-2 and B-2 and claim 14 encompasses only Scenarios A-1 and A-2.

Claim Language		Scenarios Covered by Independent Claim			
		A-1	A-2	B-1	B-2
<i>first dual-gate electrode</i>	<i>first gate electrode</i>	logic NMOS	SRAM NMOS	logic PMOS	SRAM PMOS
	<i>second gate electrode</i>	logic PMOS	SRAM PMOS	logic NMOS	SRAM NMOS
<i>second dual-gate electrode</i>	<i>third gate electrode</i>	SRAM NMOS	logic NMOS	SRAM PMOS	logic PMOS
	<i>fourth gate electrode</i>	SRAM PMOS	logic PMOS	SRAM NMOS	logic NMOS

Limitation [1G] specifies an impurity concentration relationship associated with the gate electrodes. Dependent claims 3-12 narrow claim 1 by adding further impurity concentration relationship requirements. For ease of discussion, the impurity concentration relationships specified in the claims is provided in Appendix B for each scenario.

D. Prosecution History

The filed '373 application claims were rejected as unpatentable over JP-2010-067912 to Shimomura et al. ("Shimomura") and Tamaki. (TSMC-1002, 206-207.) In response, Applicant amended the claims to recite the second dual-gate electrode is separated from the first dual-gate electrode and argued that neither Shimomura nor Tamaki disclosed this added limitation. (TSMC-1002, 245.) Relying on Applicant's representations, the Examiner subsequently allowed the

claims, finding the prior art of record did not teach “a second dual-gate electrode being separated from the first dual gate electrode.” (TSMC-1002, 257-258.)

However, the Applicant mischaracterized both the claim language and Tamaki’s teachings, which explicitly teach a first dual-gate electrode separated from a second dual-gate electrode. (§V.A.) The Examiner subsequently erred in overlooking Tamaki’s relevant disclosure when allowing the claims. Petitioner establishes, when considered properly, Tamaki discloses each limitation of claim 1.

E. Claim Construction

Petitioner does not believe any claim term requires construction to resolve the patentability disputes in this proceeding. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

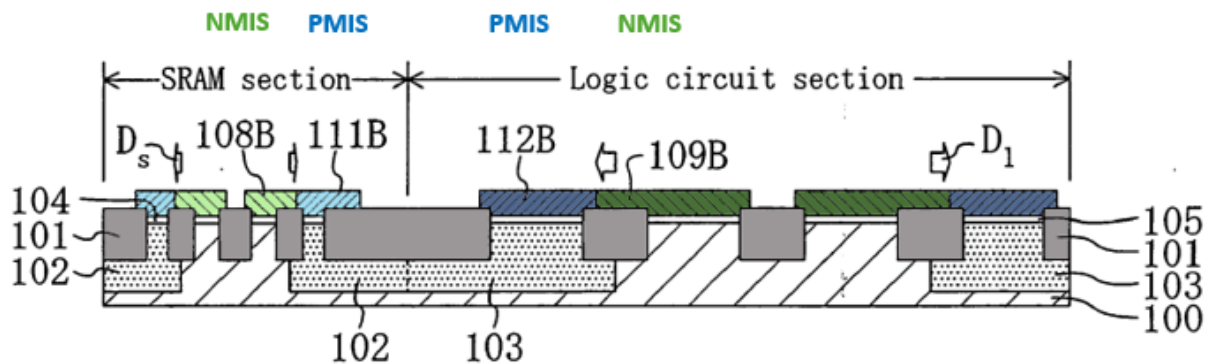
F. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. (TSMC-1003, ¶31.) Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. (*Id.*)

V. GROUND 1: Tamaki Renders Claims 1-4, 8-9, and 11-14⁴ Obvious.

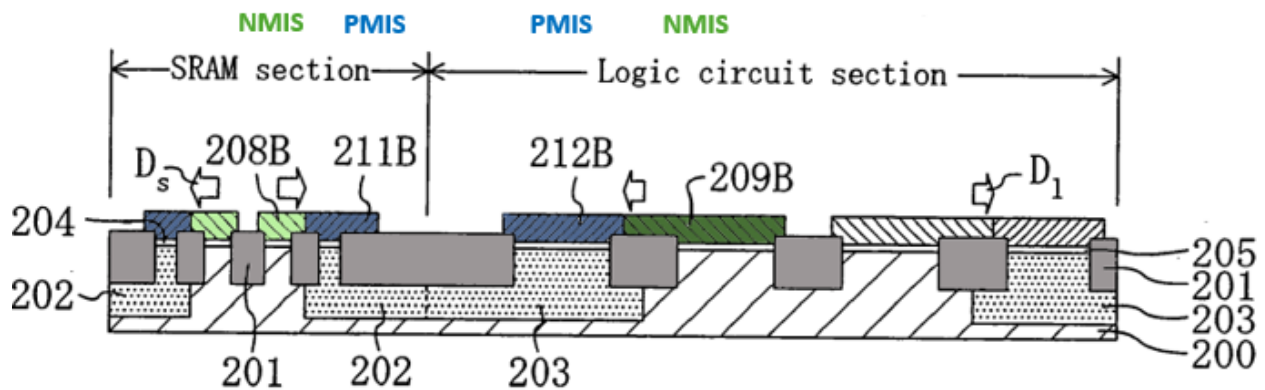
A. Tamaki Overview

Tamaki describes “a semiconductor device including a SRAM section and a logic circuit section.” (TSMC-1006, ¶2.) Tamaki discloses two embodiments, each featuring a CMIS dual-gate electrode structure similar to the conventional structure described in the ’373 patent. (TSMC-1006, Figures 3B (first embodiment), 5B (second embodiment).) The primary distinction between the embodiments is the impurity concentration relationships of the NMIS and PMIS gate electrodes in the SRAM and logic sections. (TSMC-1006, ¶¶86-106 (first embodiment), ¶¶118-135 (second embodiment).)



Tamaki, Figure 3B (First Embodiment)

⁴ Challenged claims listing is provided in Appendix A.



Tamaki, Figure 5B (Second Embodiment)

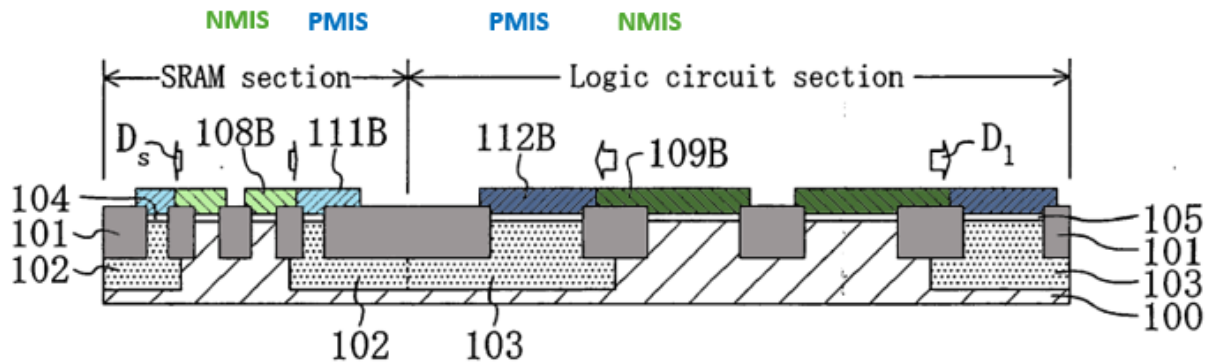
As discussed in §V.B, Tamaki's first embodiment discloses claims 1-2, 4, 8-9, 12-14 under Scenario B-1 (first conductivity type = **p-type**; second conductivity type = **n-type**)⁵. As discussed in §V.C, Tamaki's second embodiment discloses claims 1-4, 8-9, 11, and 14 under Scenario A-1 (first conductivity type = **n-type**; second conductivity type = **p-type**).

B. Tamaki's First Embodiment

The logic section of Tamaki's first embodiment device includes p-type gate electrode 112B (dark blue) and n-type gate electrode 109B (dark green). (TSMC-1006, ¶103.) The SRAM section includes n-type gate electrode 108B (light green)

⁵ Tamaki's first embodiment also discloses claims 1-2, 4, 8-9, 12, 14 under Scenario A-1. (TSMC-1003, ¶¶110-148.) For ease of discussion, the Petition focuses on Scenario B-1.

and p-type gate electrode 111B (light blue). (TSMC-1006, ¶103, Figure 3B (below).)



Tamaki, Figure 3B (First Embodiment)

Tamaki provides the following disclosures regarding the **p-type impurity concentrations** of the logic and SRAM sections:

- The “p-type impurity implantation (fourth p-type impurity implantation) **with respect to the logic circuit section p-type gate electrode formation film 112** is performed under the conditions of, for example, an implantation energy of **5 keV** and a **dosage of 3×10^{15} atoms/cm²**.” (TSMC-1006, ¶86.)
- The “p-type impurity implantation (third p-type impurity implantation) **with respect to the SRAM section p-type gate electrode formation film 111** is performed under the conditions of, for example, an

implantation energy of 5 keV and **a dosage of 2×10^{15} at[oms]/cm².**”
(TSMC-1006, ¶88.)⁶

Because the implantation of the first embodiment is carried out at the same energy (5keV) with the p-type dopant dosage of the entire gate electrode of logic PMIS higher than that of the entire gate electrode of SRAM PMIS, the resulting impurity concentration in the gate electrode of logic PMIS is greater than the gate electrode of the SRAM PMIS. (TSMC-1003, ¶¶101-104.)

Tamaki provides the following disclosures regarding the **n-type impurity concentrations** of the logic and SRAM sections:

- The “n-type impurity implantation (second n-type impurity implantation) with respect to the logic circuit section n-type gate electrode formation film 109 is performed under the conditions of, for example, an **implantation energy of 10 keV and a dosage of 8×10^{15} atoms/cm².**” (TSMC-1006, ¶85.)
- The “n-type impurity implantation (first n-type impurity implantation) with respect to the SRAM section n-type gate electrode formation film 108 is performed under the conditions of, for example, **an implantation energy of 10 keV and a dosage of 4×10^{15} atms/cm² [sic].**” (TSMC-1006, ¶87.)

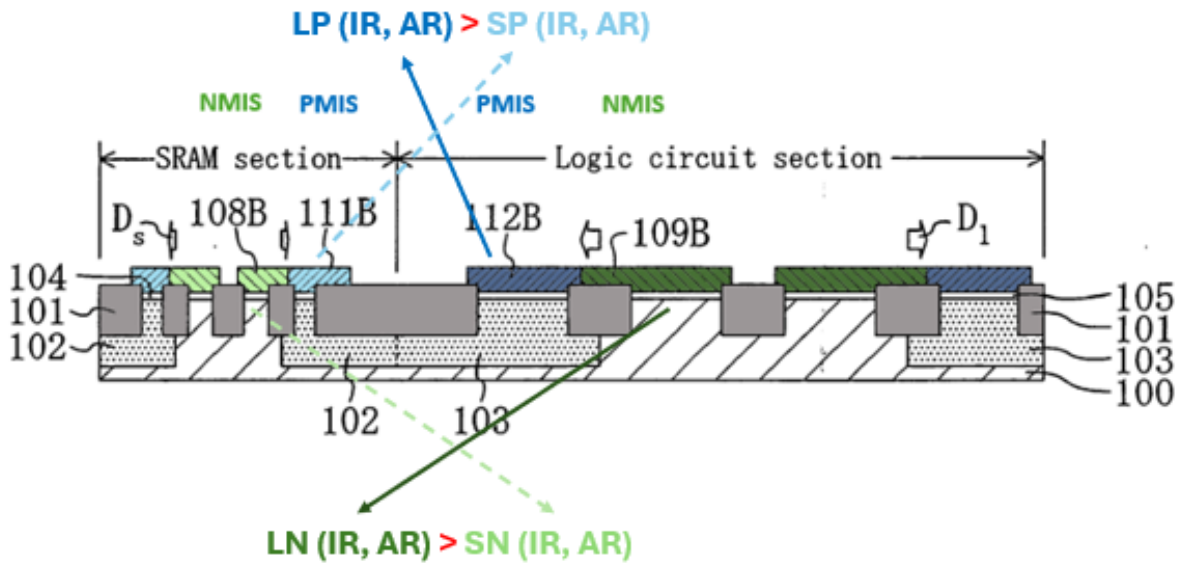
⁶ All emphases added herein unless otherwise stated.

Because the implantation is carried out at the same energy (10keV) with the n-type dopant dosage of the entire gate electrode of logic NMIS higher than that of the entire gate electrode of SRAM NMIS, the resulting impurity concentration in the gate electrode of logic NMIS is greater than the gate electrode of the SRAM PMIS. (TSMC-1003, ¶¶105-107.)

Notably, for both p-type and n-type impurity implantations, the portion of each gate electrode over the isolation region and the portion over the active region receive the same impurity implantation and therefore $LP(IR) \approx LP(AR)$, $SP(IR) \approx SP(AR)$, $LN(IR) \approx LN(AR)$, $SN(IR) \approx SN(AR)$.

The above impurity concentration relationship, illustrated in Figure 3B below:

Tamaki's First Embodiment
$LP(IR, AR) > SP(IR, AR)$
$LN(IR, AR) > SN(IR, AR)$



Tamaki, Figure 3B

1. Independent Claim 1

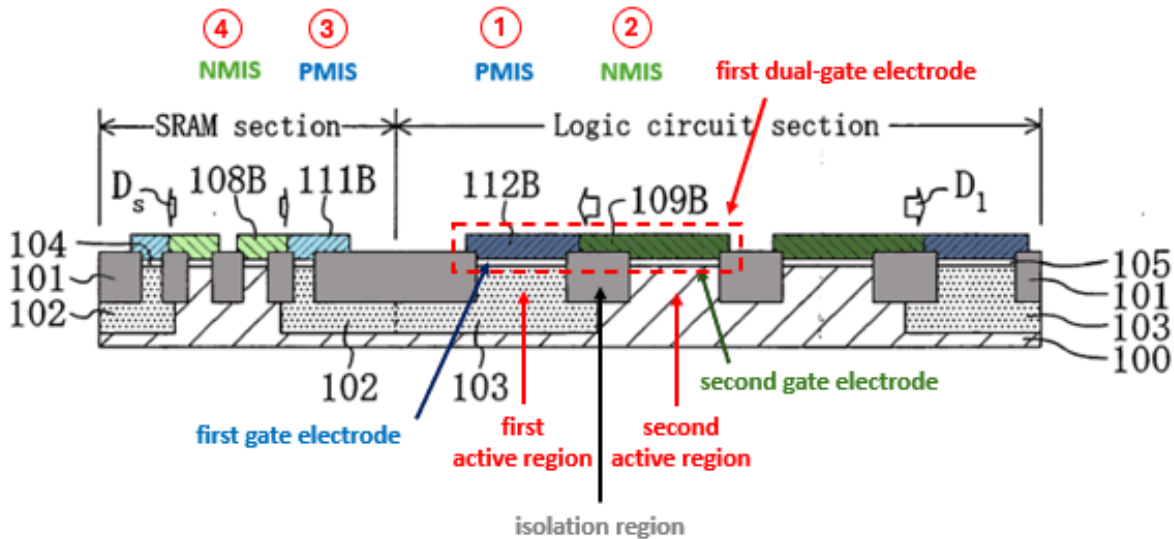
a. Preamble [1P]

Tamaki “relates to a **semiconductor device** including a SRAM section and a logic circuit section.” (TSMC-1006, ¶¶2, 82 (“semiconductor device manufacturing method in accordance with Embodiment 1”), 104, claim 1 (“semiconductor device”).) Thus, Tamaki’s first embodiment discloses a “*semiconductor device*.”

b. “First Dual-Gate Electrode” Limitations [1A]/[1C]/[1E]-[1F]

In Tamaki, logic n-type gate electrode 109 (“*first gate electrode*”) “is **formed integrally** with” logic p-type gate electrode 112 (“*second gate electrode*”).

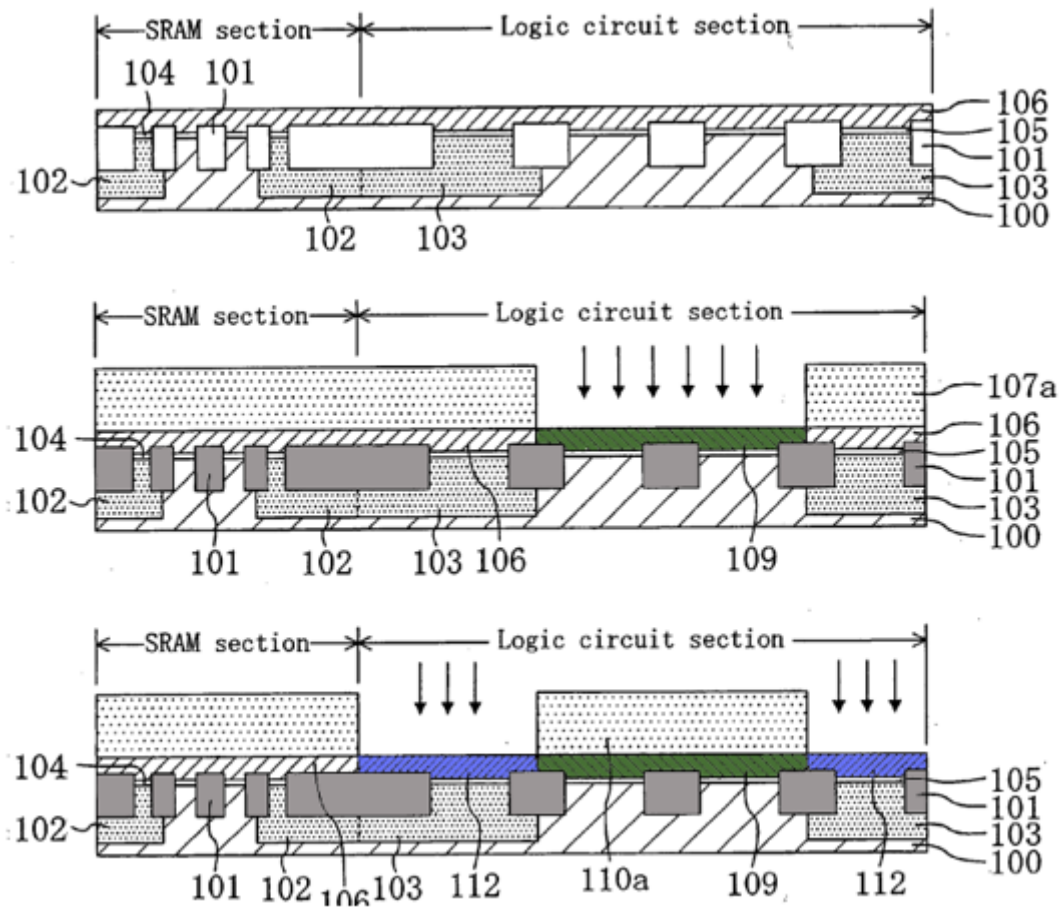
(TSMC-1006, ¶98.) Thus, logic n-type gate electrode and p-type gate electrode are collectively “a first dual-gate electrode” [1A]. (See, e.g., Figure 3B, claim 5.)



Tamaki, Figure 3B

The logic circuit section includes isolation region 101 (gray) which “separates an element formation region of a logic circuit section n-type MIS transistor and an element formation region of a logic circuit section p-type MIS transistor.” (TSMC-1006, ¶83.) Each logic “element formation region” is an “active region.” (TSMC-1006, ¶84 (“element formation region (an active region)”).) Thus, Tamaki’s first embodiment discloses “the first active region [NMIS element formation region] and the second active region [PMIS element formation region] are isolated from each other with an isolation region interposed therebetween” [1E] under Scenario B-1. (TSMC-1003, ¶¶152-153.)

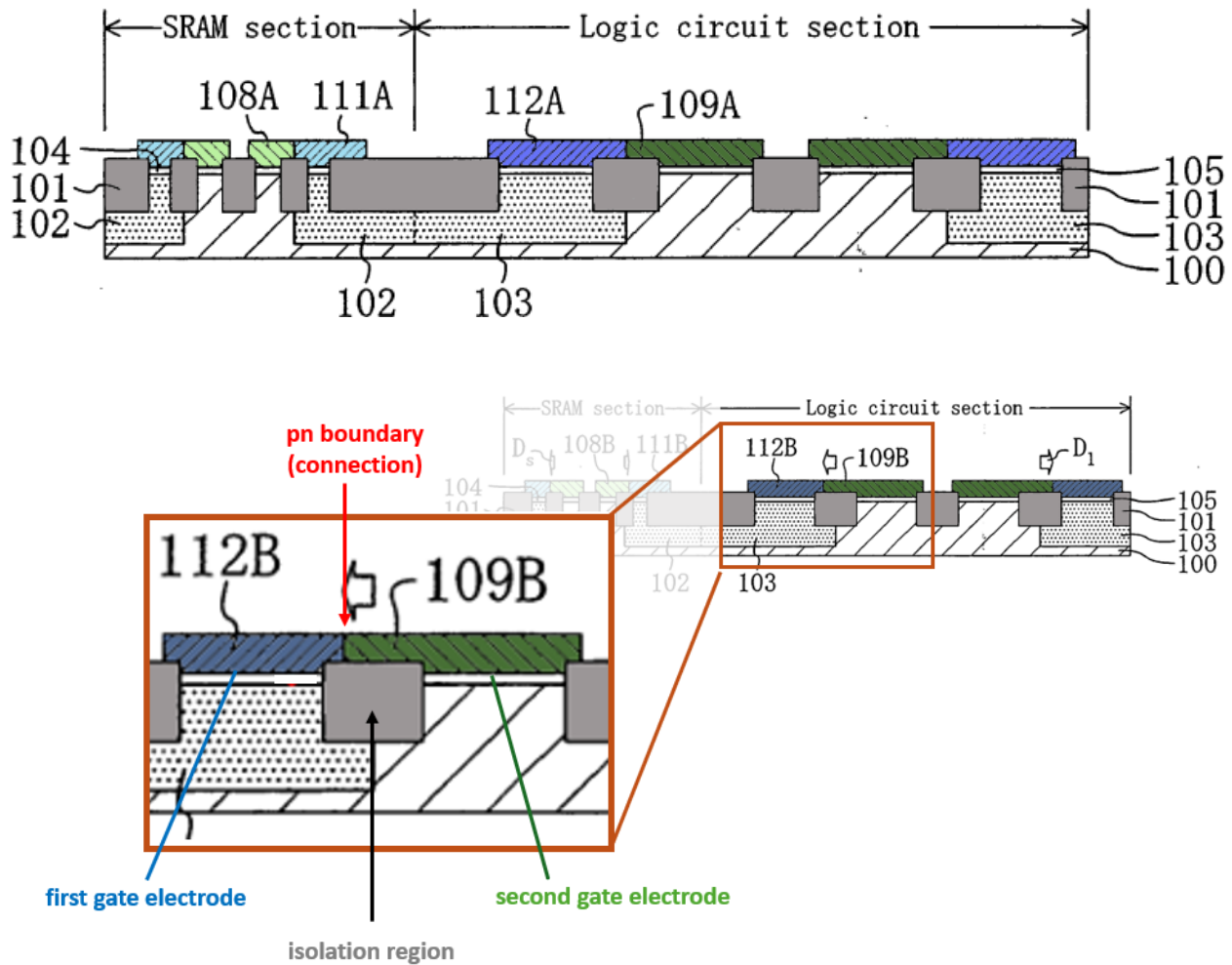
During manufacture of Tamaki's device, after forming SRAM gate insulating film 104 and logic gate insulating film 105, gate electrode formation film 106, "**formed of a polysilicon film**", is formed "on the entirety of the semiconductor substrate." (TSMC-1006, ¶84, Figure 1A (below-top).)



Tamaki, Figures 1A (top), 1B (middle), 1C (bottom)

An "n-type impurity, for example, phosphorous or the like, is implanted to the gate electrode formation film 106 on the n-type MIS formation region in the logic circuit section," forming "a logic circuit section n-type gate electrode

formation film 109.” (TSMC-1006, ¶85, Figure 1B (above-middle).) A “p-type impurity, for example, boron or the like is implanted to the gate electrode formation film 106 on the p-type MIS formation region in the logic circuit section,” forming “logic circuit section p-type gate electrode formation film 112.” (TSMC-1006, ¶86, Figure 1C (above-bottom).) The p-type gate electrode formation film 112 is “*a first silicon film of a first conductivity type*” and the n-type gate electrode formation film 109 is “*a first silicon film of a second conductivity type*.” Patterning is then performed on logic n-type gate electrode formation film 109 and logic p-type gate electrode formation film 112, forming n-type gate electrode 109A and p-type gate electrode 112A. (TSMC-1006, ¶98, Figure 3A (below-top).)



Tamaki, Figures 3A (top), 3B (bottom) with enlargement

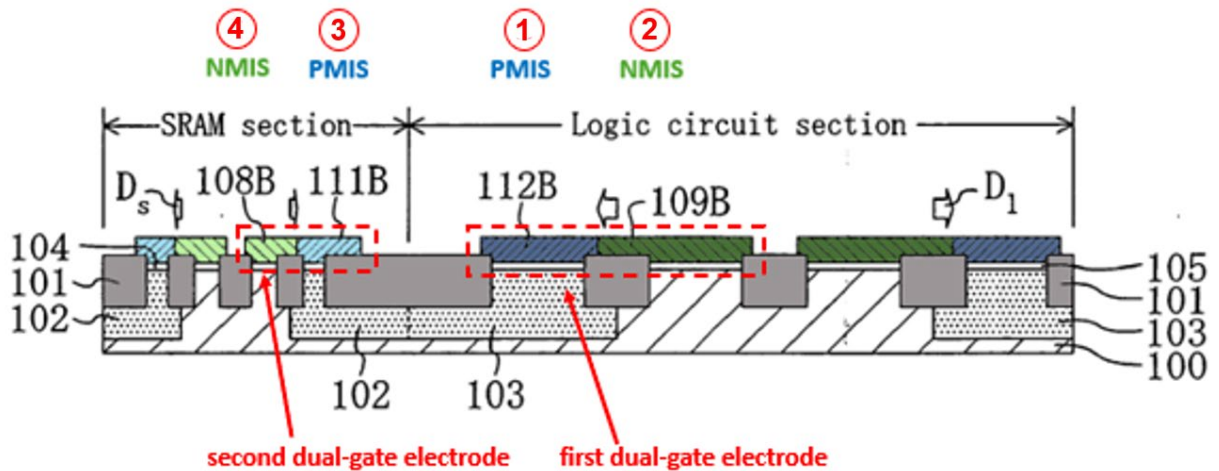
As shown in Figure 3A (above-top) and Figure 3B (above-bottom), p-type gate electrode 112A (labeled 112B in Figure 3B) is “located on [the] first active region” and n-type gate electrode 109A (labeled 109B in Figure 3B) is “located on [the] second active region.” Accordingly, Tamaki’s first embodiment discloses “the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate

electrode located on a second active region and having a first silicon film of a second conductivity type” [1C] under Scenario B-1. (See also, Tamaki, claim 1.)

As shown in the Figure 3B enlargement above, n-type gate electrode 109B “**is formed integrally**” with the p-type gate electrode. (TSMC-1006, ¶98, claim 2.) Tamaki explains “**the pn boundary** between the logic circuit section n-type gate electrode 109B [green] and the logic circuit section p-type gate electrode 112B [blue] **is located at a point on the element isolation region 101**” between the NMIS and PMIS active regions. (TSMC-1006, ¶103.) Tamaki’s first embodiment thus discloses “*the first gate electrode and the second gate electrode are connected to each other on the isolation region*” [1F] under Scenario B-1.

c. “Second Dual-Gate Electrode” Limitations [1B], [1D]

In Tamaki’s first embodiment, SRAM section n-type gate electrode 108A (“*fourth gate electrode*”) “**is formed integrally with**” SRAM section p-type gate electrode 111A (“*third gate electrode*”). (TSMC-1006, ¶98, claim 2 (“the first n-type gate electrode is integrally formed with the first p-type gate electrode”), Figure 3B (below).) Thus, SRAM n-type gate electrode and p-type gate electrode are collectively “*a second dual-gate electrode*” [1B]. And as shown in Figure 3B below, after patterning, the “*second dual-gate electrode*” is “*separated from the first dual-gate electrode*” [1B]. (See, e.g., Tamaki, ¶98 (discussing patterning of SRAM and logic gate electrodes.)

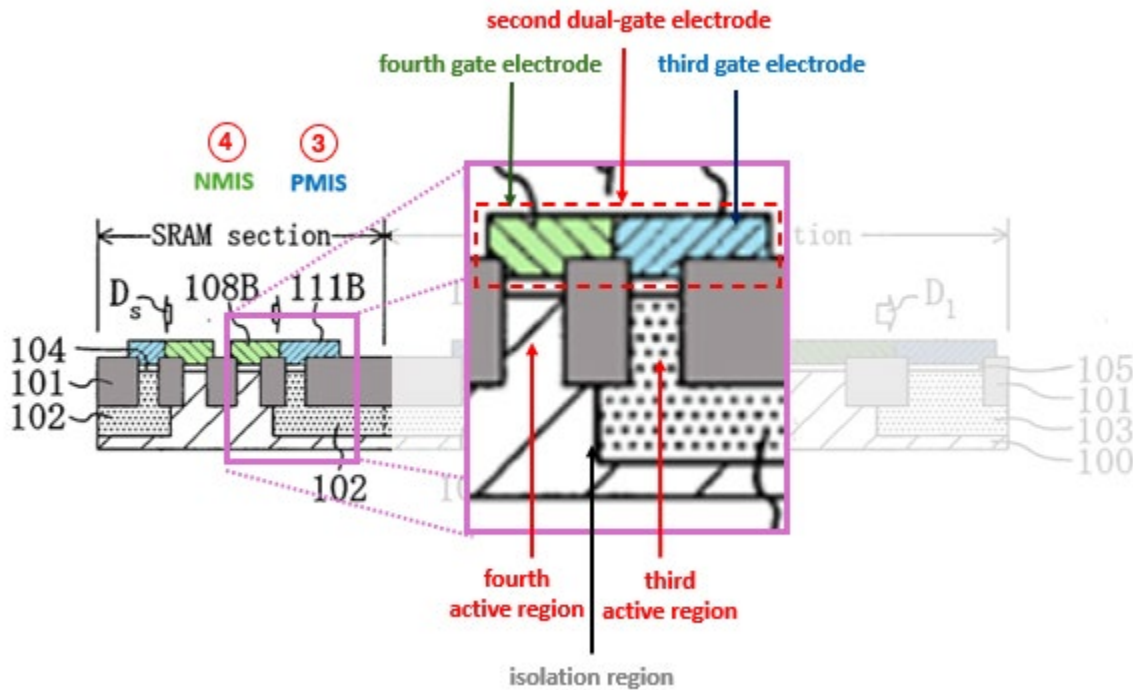


Tamaki, Figure 3B

Like the logic section, the SRAM section includes “element isolation region 101 (gray), which separates an element formation region of a SRAM section n-type MIS transistor and an element formation region of a SRAM section p-type MIS transistor.” (TSMC-1006, ¶83.) Each SRAM “element formation region” is an “*active region*.” (TSMC-1006, ¶84 (“element formation region (an **active region**)”); *see also*, Tamaki, ¶83.)

During manufacture of Tamaki's first embodiment device, gate electrode formation film 106, "**formed of a polysilicon film**," is formed "on the entirety of the semiconductor substrate" after formation of the logic and SRAM gate insulating films. (TSMC-1006, ¶84.) An "n-type impurity [*"second conductivity type"*], for example, phosphorous or the like is implanted to the gate electrode formation film 106 on the n-type MIS formation region in the SRAM section."

(TSMC-1006, ¶87, Figure 2A.) A “p-type impurity [“*first conductivity type*”], for example, boron or the like is implanted to the gate electrode formation film 106 on the p-type MIS formation region in the SRAM section.” (TSMC-1006, ¶88, Figure 2B.)



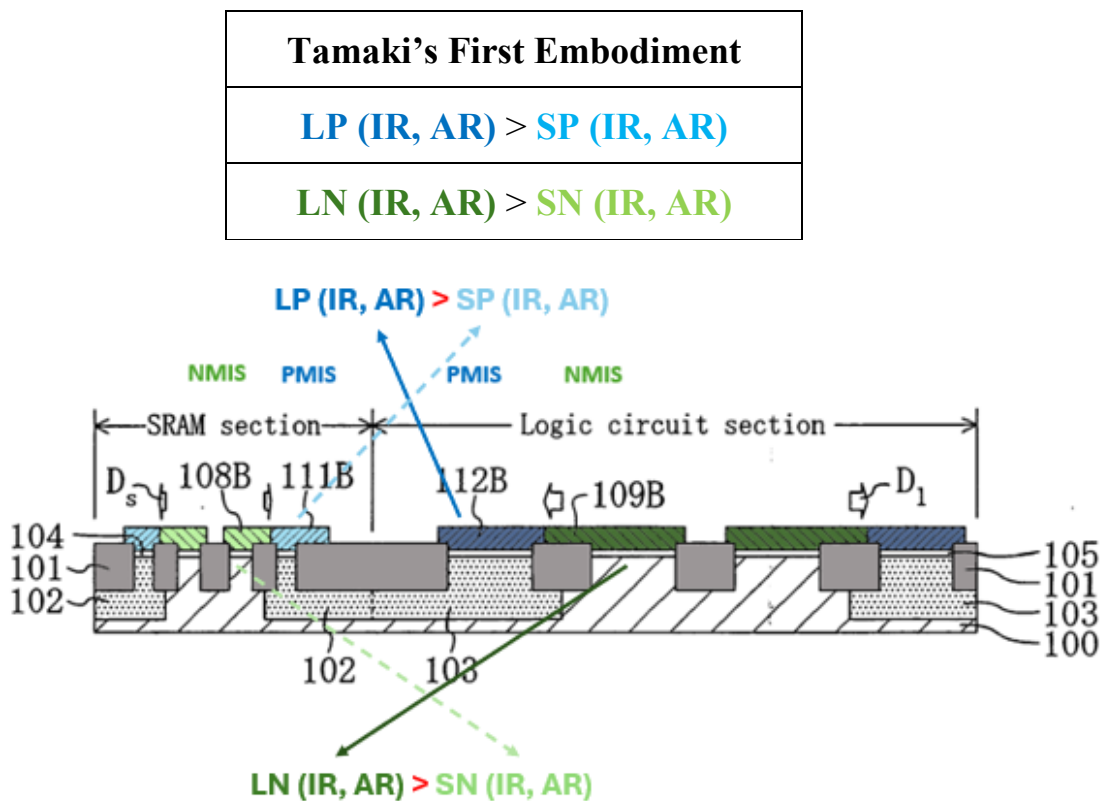
Tamaki, Figure 3B with enlargement

Patterning is then performed on “the SRAM section n-type gate electrode formation film 108, and the SRAM section p-type gate electrode formation film 111,” forming SRAM section n-type gate electrode 108B and SRAM section p-type gate electrode 111B. (TSMC-1006, ¶98.) As shown in Figure 3B (above), n-type gate electrode 108B (“*fourth gate electrode*”) is “located on [the] fourth active region [NMIS element formation region]” and has “a second silicon film of

the second conductivity type [n-type gate electrode formation film]. And p-type gate electrode 111B (“third gate electrode”) is “located on [the] third active region [PMIS element formation region]” and has “a second silicon film of the first conductivity type [p-type gate electrode formation film].”

d. Impurity Concentration Limitation

As discussed in §V.B, Tamaki’s impurity concentration relationship is:



Tamaki, Figure 3B

Tamaki’s first embodiment discloses “at least a portion of the first silicon film of the first conductivity type [$LP(IR, AR)$] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of

the first conductivity type located on the third active region [SP(AR)]” under Scenario B-1. (See §V.B.)

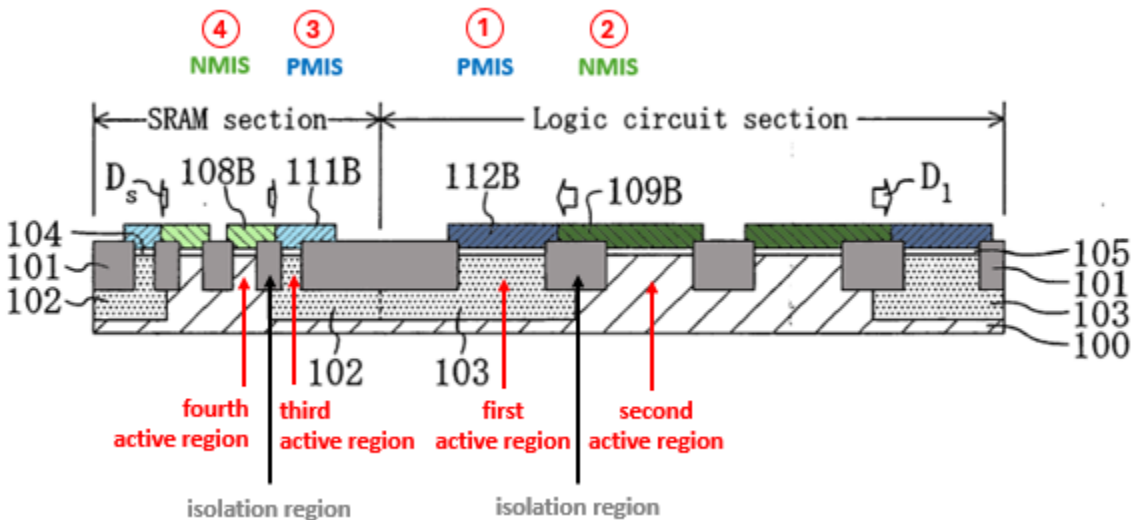
	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	LN(IR, AR) > SN(AR)	LN(IR, AR) > SN(IR, AR)
A-2	SN(IR, AR) > LN(AR)	
B-1	LP(IR, AR) > SP(AR)	LP(IR, AR) > SP(IR, AR)
B-2	SP(IR, AR) > LP(AR)	

2. Claim 2

Tamaki’s first embodiment discloses “*an isolation width between the first active region [logic-PMIS active region] and the second active region [logic-NMIS active region] is larger than that between the third active region [SRAM-PMIS active region] and the fourth active region [SRAM-NMIS active region].*”

In Tamaki’s first embodiment, the “width in the gate width direction of an element isolation region 101, which separates an element formation region of a SRAM section n-type MIS transistor [“*fourth active region*”] and an element formation region of a SRAM section p-type MIS transistor [“*third active region*”], is **set smaller than** the width in the gate width direction of an element isolation region 101, which separates an element formation region of a logic circuit section n-type MIS transistor [“*second active region*”] and an element formation region of

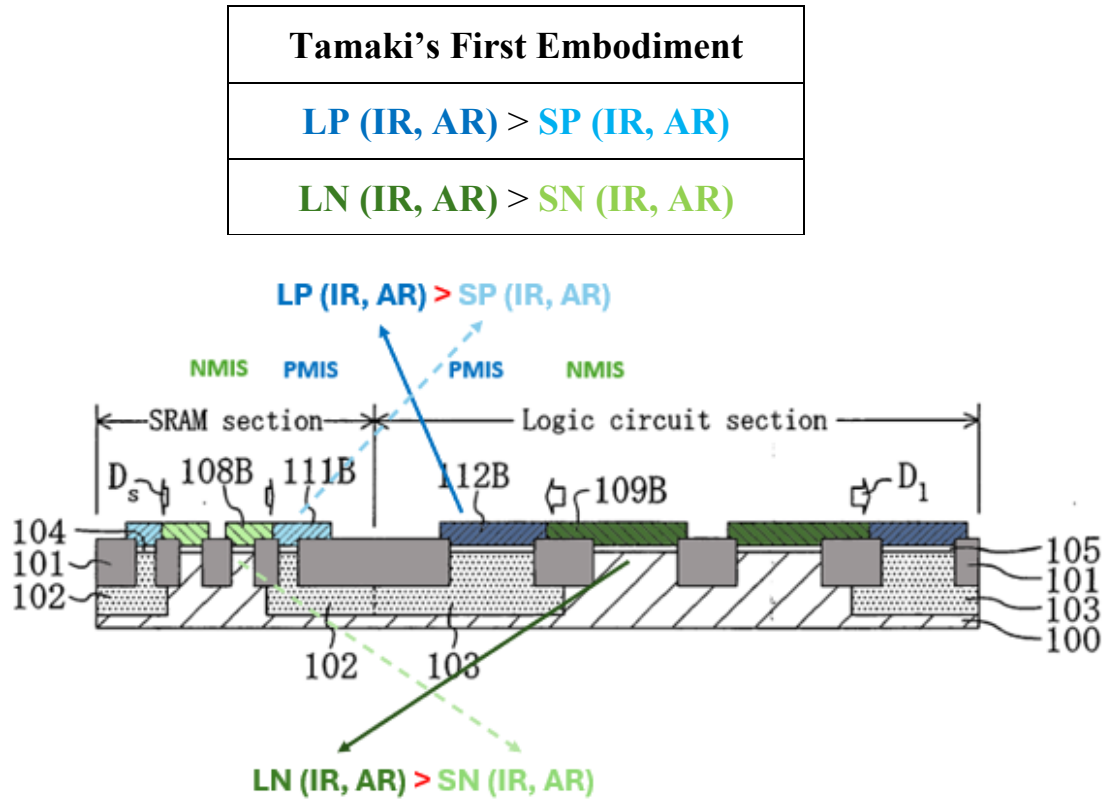
a logic circuit section p-type MIS transistor [*“first active region”*].” (TSMC-1006, ¶83, Figure 3B (below).) In other words, the width of isolation region 101 located between the SRAM NMIS and PMIS transistors, is smaller than that between the logic NMIS and PMIS transistors. Indeed, a POSITA would have known the isolation between transistors in the SRAM area is smaller than that in the logic area because the transistors in the SRAM area are arranged denser than in the logic area. (TSMC-1003, ¶157, TSMC-1006, ¶29; *see also*, TSMC-1007, ¶4; TSMC-1016, 3:58-64; TSMC-1001, Figures 16A-16B (illustrating prior art device having larger isolation region width in logic than SRAM).)



Tamaki, Figure 3B

3. Claim 4

The impurity concentration relationship of Tamaki’s first embodiment, discussed in §V.B, is:



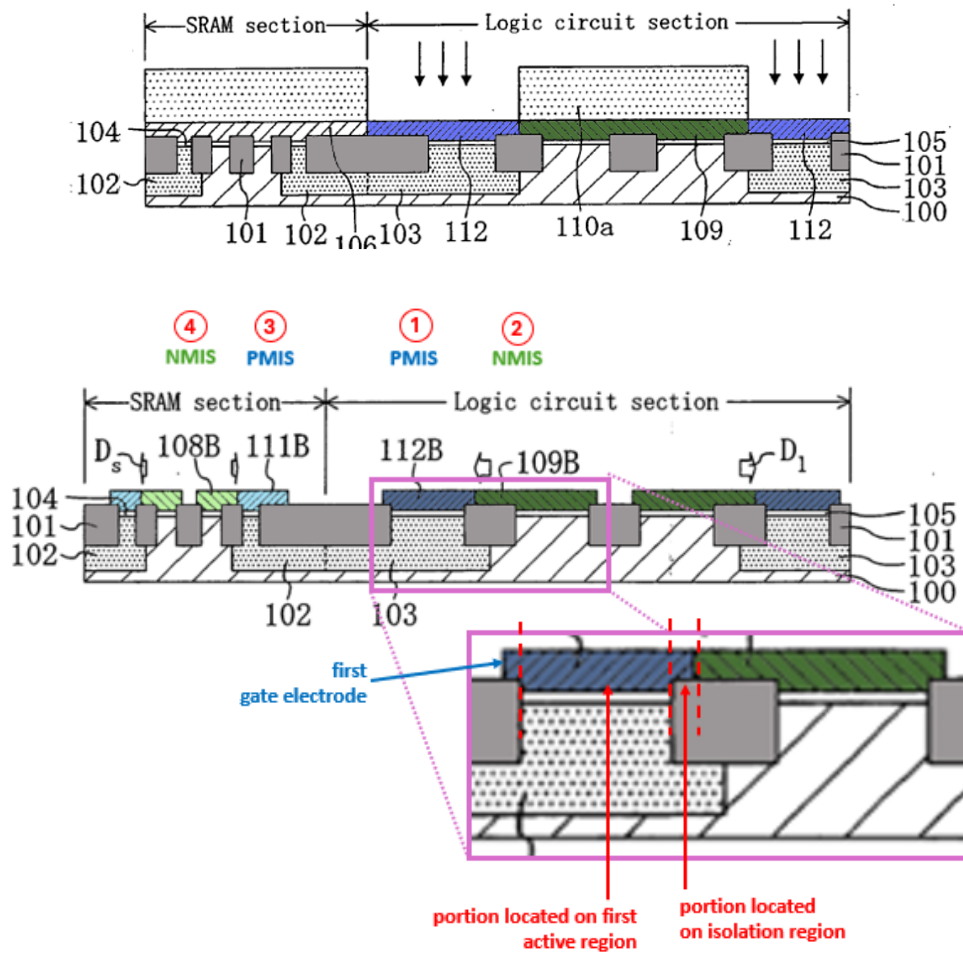
Tamaki, Figure 3B

Accordingly, the portion of electrode 112 over the active region, **LP(AR)**, (“the first silicon film of the first conductivity type located on the first active region”) has a higher p-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 111 over the active region, **SP(AR)**, (“the second silicon film of the first conductivity type located on the third active region”). That is, **LP(AR) > SP(AR)**, satisfying claim 4 under Scenario B-1.

4. Claim 8

In Tamaki’s first embodiment, “a p-type impurity, for example, boron or the like is implanted to the gate electrode formation film 106 on the p-type MIS

formation region in the logic circuit section.” (*See, e.g.*, Tamaki, ¶86, Figure 1C (below-top), Figure 3B (below-bottom).) The p-type impurity implantation “with respect to the logic circuit section p-type gate electrode formation film 112 is performed under the conditions of, for example, an implantation energy of 5 keV and a dosage of 3×10^{15} atoms/cm².” (TSMC-1006, ¶86.) The implantation is carried out uniformly across the entire gate electrode film. Therefore, the impurity concentration of the portion of the first gate electrode over the first active region is substantially equal to that of the portion located over the isolation region. (TSMC-1003, ¶¶161-164.)



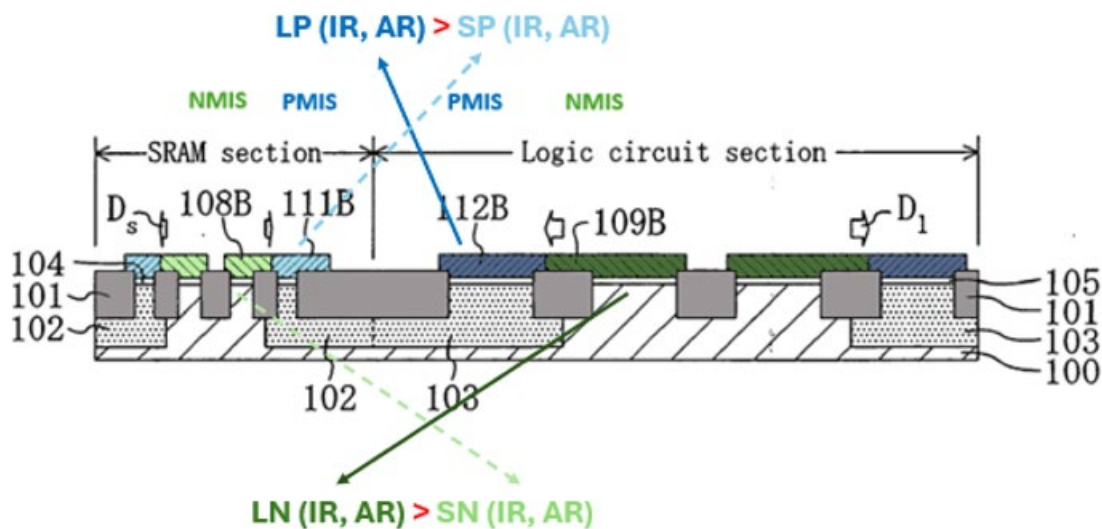
Tamaki, Figures 1C (top), 3B (bottom) with enlargement

Thus, Tamaki's first embodiment discloses "*a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region*" under Scenario B-1.

5. Claim 9

The impurity concentration relationship of Tamaki's first embodiment, discussed in §V.B, is:

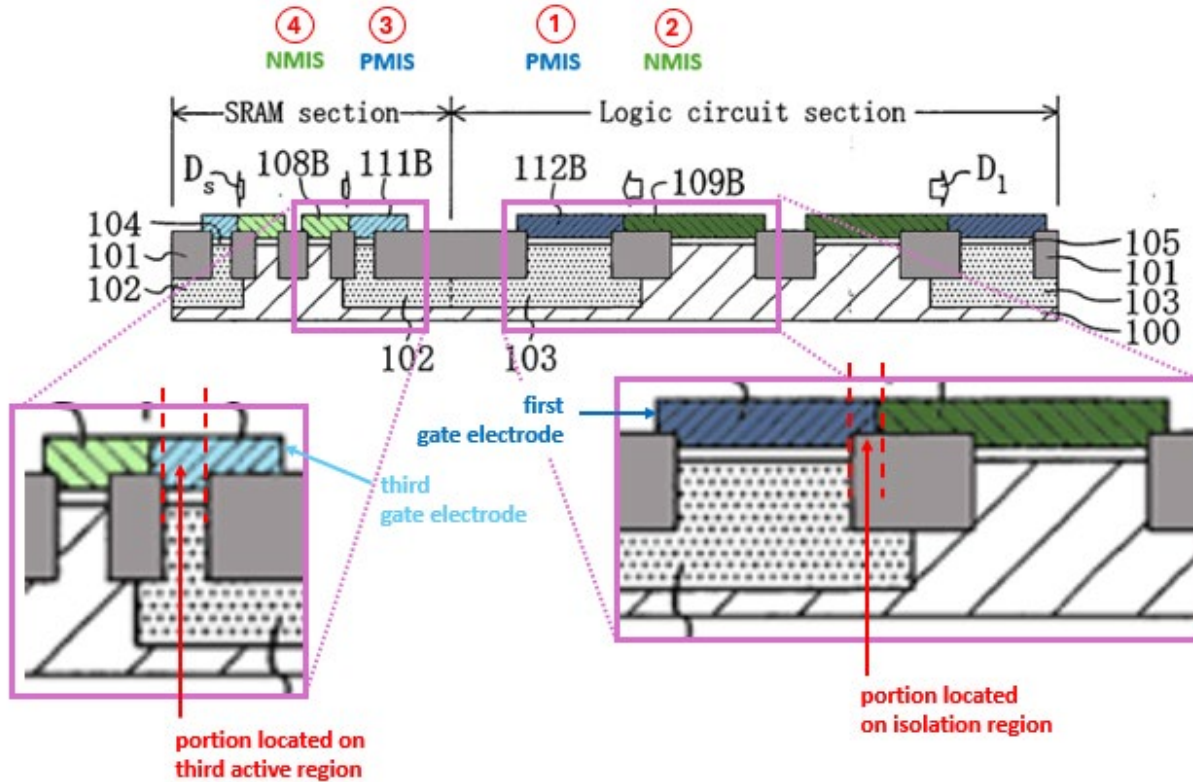
Tamaki's First Embodiment
$LP(IR, AR) > SP(IR, AR)$
$LN(IR, AR) > SN(IR, AR)$



Tamaki, Figure 3B

Accordingly, the portion of electrode 112 over the isolation region, $LP(IR)$, (“the first silicon film of the first conductivity type located on the isolation region”) has a higher p-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 111 over the active region, $SP(AR)$,

(“the second silicon film of the first conductivity type located on the third active region”). That is, $LP(IR) > SP(AR)$, satisfying claim 9 under Scenario B-1.

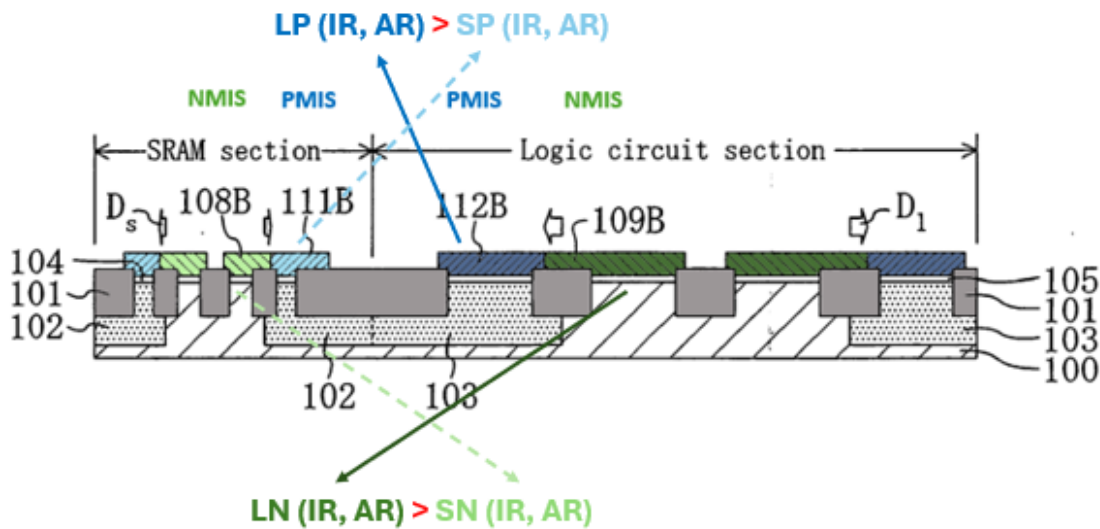


Tamaki, Figure 3B with enlargements

6. Claim 12

The impurity concentration relationship of Tamaki’s first embodiment, discussed in §V.B, is:

Tamaki’s First Embodiment
$LP(IR, AR) > SP(IR, AR)$
$LN(IR, AR) > SN(IR, AR)$



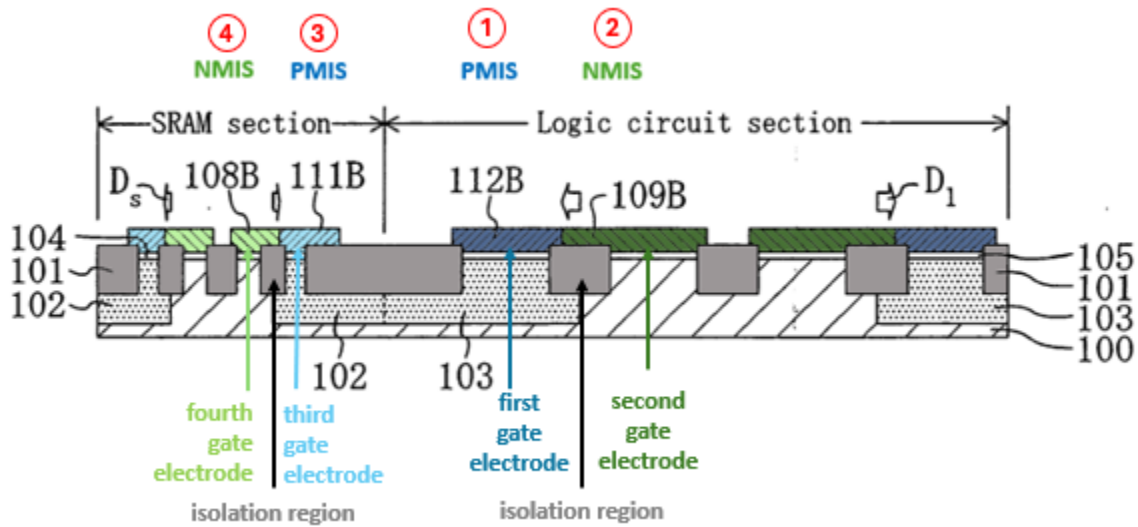
Tamaki, Figure 3B

Accordingly, the portion of electrode 112 over the active region, **LP(AR)**, (“the first silicon film of the first conductivity type located on the first active region”) has a higher p-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 111 over the active region, **SP(AR)**, (“the second silicon film of the first conductivity type located on the third active region”) and the portion of electrode 109 over the active region, **LN(AR)**, (“the first silicon film of the second conductivity type located on the second active region”) has a higher n-type impurity concentration (“second-conductivity-type impurity concentration”) than the portion of electrode 108 over the active region, **SN(AR)**. That is, **LP(AR) > SP(AR)** and **LN(AR) > SN(AR)**, satisfying claim 12 under Scenario B-1.

7. Claims 13-14

Tamaki's logic NMIS transistor includes logic PMIS transistor includes **p-type gate electrode 112B** (“*first gate electrode*”) and logic **n-type gate electrode 109B** (“*second gate electrode*”). (TSMC-1006, ¶103). Similarly, SRAM NMIS transistor includes **p-type gate electrode 111B** (“*third gate electrode*”) and **n-type gate electrode 108B** (“*fourth gate electrode*”). (TSMC-1006, ¶103).

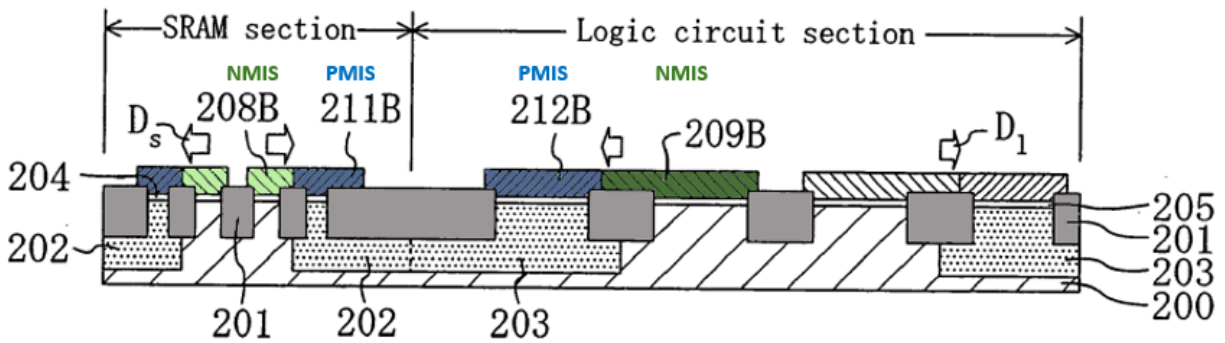
Accordingly, Tamaki's first embodiment discloses “*the first gate electrode is a gate electrode of a first PMIS transistor, the second gate electrode is a gate electrode of a first NMIS transistor, the third gate electrode is a gate electrode of a second PMIS transistor, and the fourth gate electrode is a gate electrode of a second NMIS transistor*” [13] and “*each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit*” [14] under Scenario B-1.



Tamaki, Figure 3B

C. Tamaki's Second Embodiment

Tamaki's second embodiment device has the same structure as the first embodiment device, differing only in the impurity concentration relationship among its gate electrodes. The logic section dual-gate electrode includes n-type electrode 209B (dark green) and p-type electrode 212B (blue). (TSMC-1006, ¶136, Figure 5B (below).) The SRAM section dual-gate electrode includes n-type electrode 208B (light green) and p-type electrode 211B (blue). (TSMC-1006, ¶136.)



Tamaki, Figure 5B

Tamaki provides the following disclosures regarding the **p-type impurity concentrations** of the logic and SRAM sections:

- “the p-type impurity implantation (third p-type impurity implantation) with respect to the SRAM section p-type gate electrode film 211 and the p-type impurity implantation (fourth p-type impurity implantation) with respect to the logic circuit section p-type gate electrode formation film 212 are performed under the conditions of for example, **an implantation energy of 5 keV and dosage of 3×10^{15} at[oms/cm²]**.” (TSMC-1006, ¶119.)

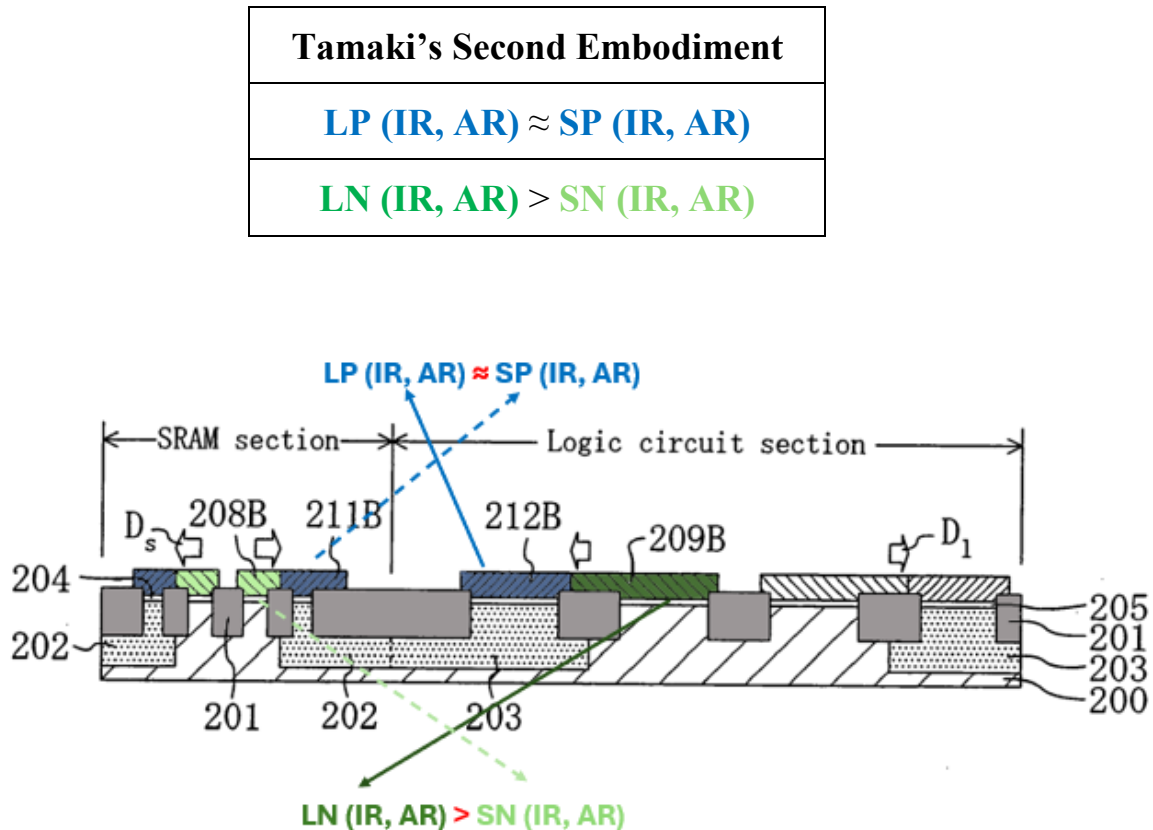
Because the implantation conditions are the same for the entire gate electrode of Logic PMIS and the entire gate electrode of SRAM PMIS, the resulting impurity concentrations in both are the same. (TSMC-1003, ¶¶175-176.)

Tamaki provides the following disclosures regarding the **n-type impurity concentrations** of the logic and SRAM sections:

- “SRAM section n-type gate electrode 208B has phosphorous concentration **lower than** the logic circuit section n-type gate electrode 209B” (TSMC-1006, ¶138, Figure 5B.)

Notably, each gate electrode over the isolation region and that over the active region receives the same impurity implantation.

The above impurity concentration relationship, illustrated in Figure 5B below, is:



Tamaki, Figure 5B

1. Independent Claim 1

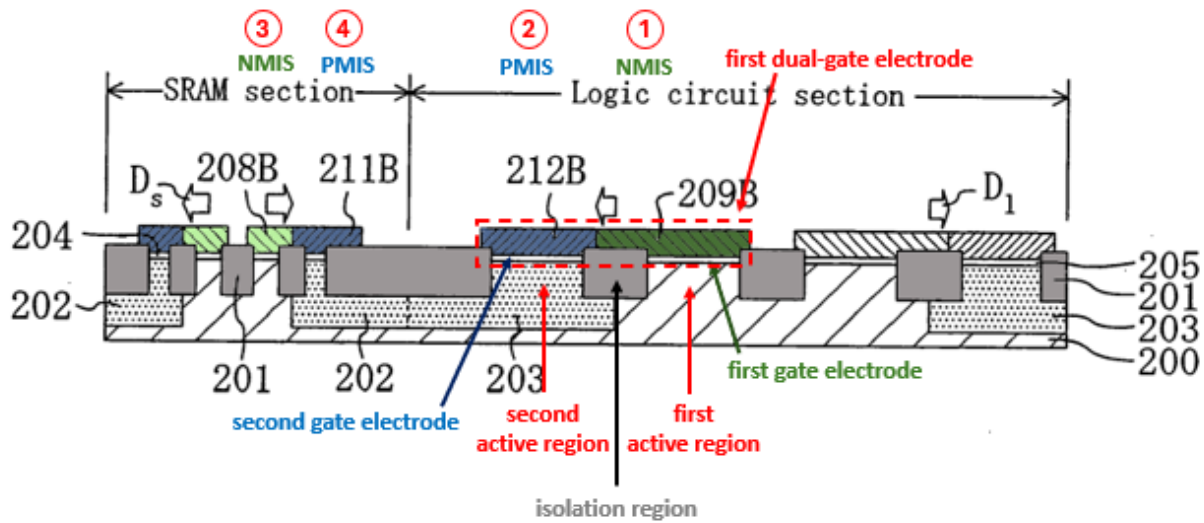
a. Preamble [1P]

For the reasons discussed in §V.B.1.a, Tamaki's second embodiment discloses a "*semiconductor device*" under Scenario A-1. (TSMC-1006, ¶115

(“**semiconductor device** manufacturing method in accordance with Embodiment 2”).)

b. “First Dual-Gate Electrode” Limitations [1A]/[1C]/[1E]-[1F]

For the reasons discussed in §V.B.1.b, logic n-type gate electrode and p-type gate electrode are collectively “*a first dual-gate electrode*” [1A]. (See also, e.g., TSMC-1006, ¶130, Figure 5B (below), claim 2 (“first n-type gate electrode is integrally formed with the first p-type gate electrode”).) And for the reasons discussed in §V.B.1.b, the second embodiment also discloses “*the first dual-gate electrode includes a first gate electrode [logic-NMIS gate electrode] located on a first active region and having a first silicon film of a first conductivity type [n-type] and a second gate electrode [logic-PMIS gate electrode] located on a second active region and having a first silicon film of a second conductivity type [p-type]*” [1C] under Scenario A-1. (See also, TSMC-1006, ¶¶116-131.)



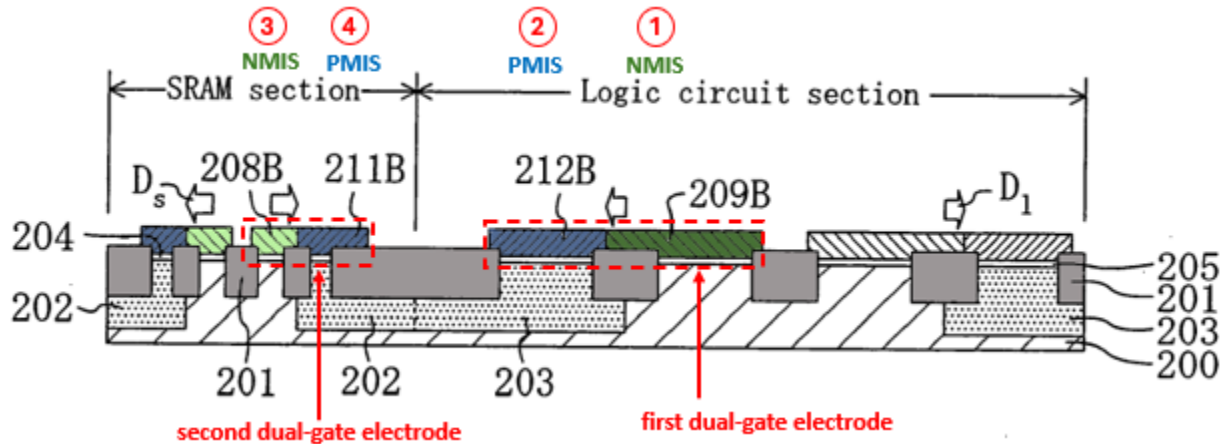
Tamaki, Figure 5B

As shown above and discussed in §V.B.1.b, “the first active region and the second active region are isolated from each other with an isolation region interposed therebetween” [1E] and “the first gate electrode [logic-NMIS gate electrode] and the second gate electrode [logic-PMIS gate electrode] are connected to each other on the isolation region” [1F] under Scenario A-1. (TSMC-1003, ¶¶183-189; see also, TSMC-1006, ¶116.)

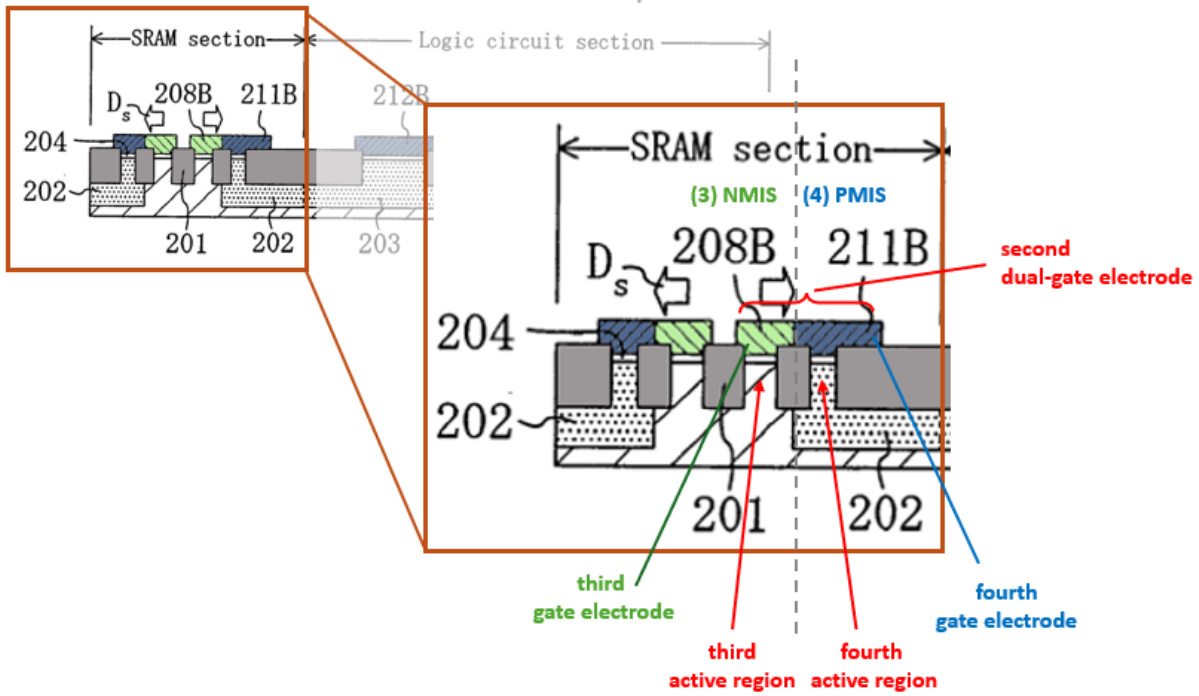
c. “Second Dual-Gate Electrode” Limitations [1B], [1D]

For the reasons discussed in §V.B.1.c, SRAM n-type and p-type gate electrodes are collectively “a second dual-gate electrode” [1B]. (See, e.g., TSMC-1006, ¶116, Figure 5B, claim 2 (“first n-type gate electrode is integrally formed with the first p-type gate electrode”).) As shown in Figure 5B below, after patterning, the “second dual-gate electrode” is “separated from the first dual-gate

electrode.” (See, e.g., TSMC-1006, ¶¶130-131 (discussing patterning of SRAM and logic gate electrodes); §V.B.1.c.)



For the reasons discussed in §V.B.1.c and illustrated in the Figure 5B enlargement below, n-type gate electrode 208 (“third gate electrode”) is “located on [the] third active region [NMIS element formation region]” and has “a second silicon film of the first conductivity type [gate electrode formation film with n-type dopants]” and p-type gate electrode 211 (“fourth gate electrode”) is “located on [the] fourth active region [PMIS element formation region]” and has “a second silicon film of the second conductivity type [p-type gate electrode formation film], satisfying limitation [1D] under Scenario A-1.

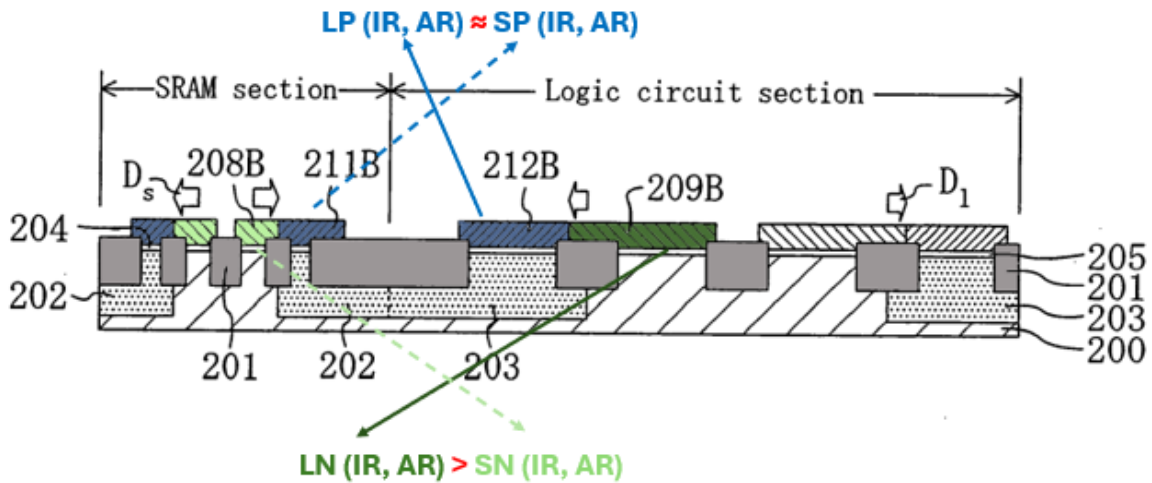


Tamaki, Figure 5B with enlargement

d. Impurity Concentration Limitations [1G]

The impurity concentration relationship of Tamaki's second embodiment, discussed in §V.C, is:

Tamaki's Second Embodiment
$LP(IR, AR) \approx SP(IR, AR)$
$LN(IR, AR) > SN(IR, AR)$



Tamaki, Figure 5B

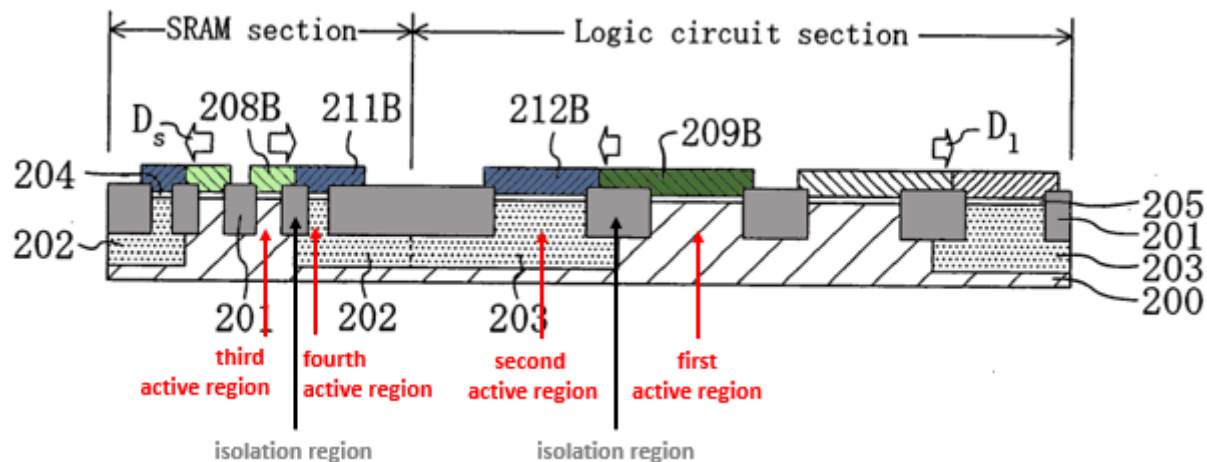
Tamaki's second embodiment therefore discloses “*at least a portion of the first silicon film of the first conductivity type [LN (IR, AR)] has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [SN (AR)]*”, satisfying [1G] under Scenario A-1.

	Claimed Impurity Concentration Relationship	Tamaki Impurity Concentration Relationship
A-1	LN(IR, AR) > SN(AR)	LN(IR, AR) > SN(IR, AR)
A-2	SN(IR, AR) > LN(AR)	
B-1	LP(IR, AR) > SP(AR)	
B-2	SP(IR, AR) > LP(AR)	

2. Claim 2

Tamaki’s second embodiment discloses “*an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region*” under Scenario A-1.

In Tamaki's second embodiment, the width of element isolation region 201, which separates an element formation region of a SRAM NMIS transistor [*"third active region"*] and an element formation region of a SRAM PMIS transistor [*"fourth active region"*], "is **set smaller than** the width" of element isolation region 201, which separates an element formation region of a logic NMIS transistor [*"first active region"*] and an element formation region of a logic PMIS transistor [*"second active region"*]." (TSMC-1006, ¶116, Figure 5B (below).)



Tamaki, Figure 5B

3. Claims 3 and 11

The impurity concentration relationship of Tamaki's second embodiment, discussed in §V.C, is:

Tamaki's Second Embodiment
$LP(IR, AR) \approx SP(IR, AR)$
$LN(IR, AR) > SN(IR, AR)$

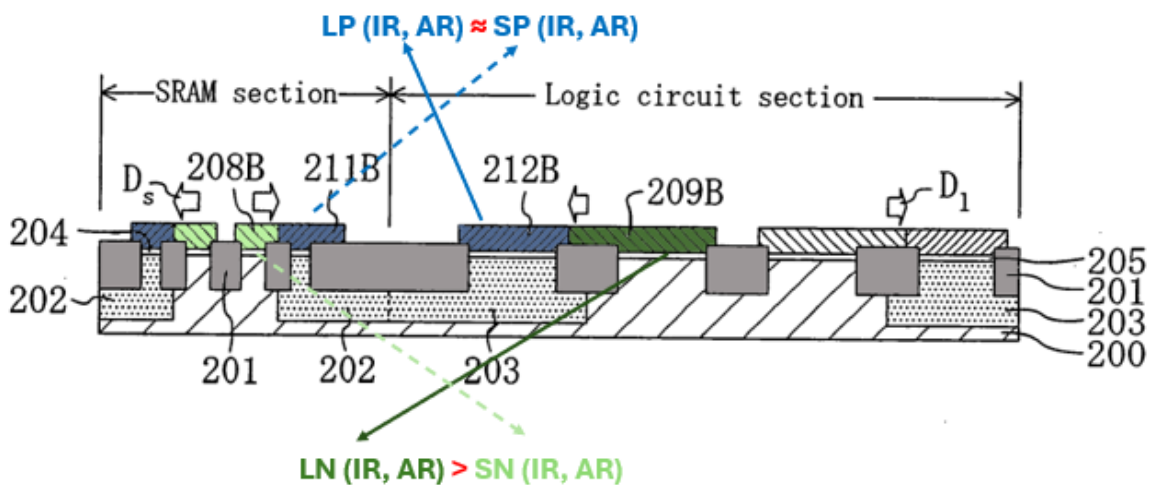
Accordingly, the portion of electrode 212 over the active region, **LP (AR)** (“*at least a portion of the first silicon film of the second conductivity type*”) has a substantially equal p-type impurity concentration (“*second-conductivity-type impurity concentration*”) to the portion of electrode 211 over the active region, **SP (AR)** (“*the second silicon film of the second conductivity type located on the fourth active region*”). That is, $LP(AR, IR) \approx SP(AR)$, satisfying both claims 3 and 11 under Scenario A-1.

4. Claim 4

The impurity concentration relationship of Tamaki's second embodiment, discussed in §V.C, is summarized below:

Tamaki's Second Embodiment
$LP(IR, AR) \approx SP(IR, AR)$
$LN(IR, AR) > SN(IR, AR)$

Accordingly, the portion of electrode 209 over the active region, **LN(AR)**, (“the first silicon film of the first conductivity type located on the first active region”) has a higher n-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 208 over the active region, **SN(AR)**, (“the second silicon film of the first conductivity type located on the third active region”). That is, **LN(AR) > SN(AR)**, satisfying claim 4 under Scenario A-1.

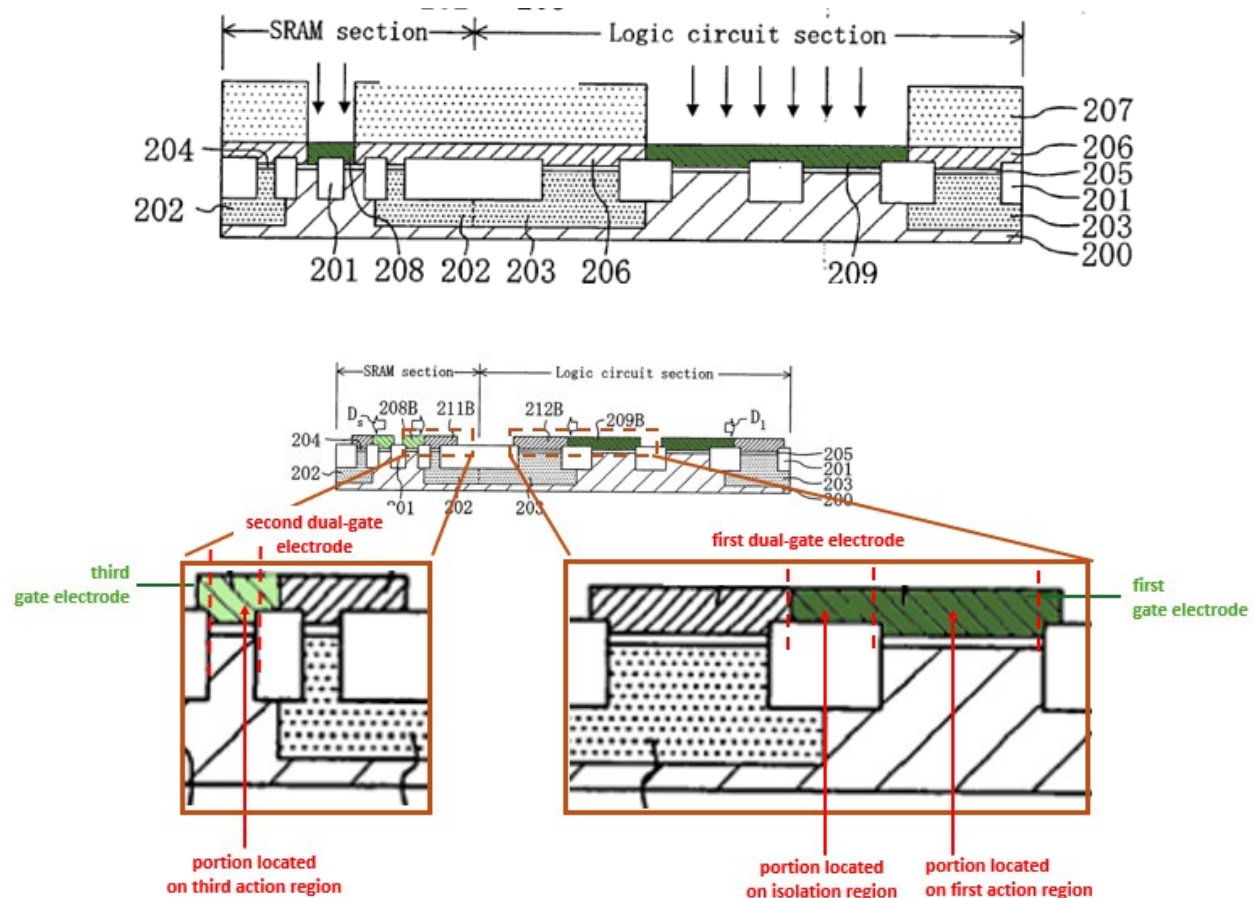


Tamaki, Figure 5B

5. Claim 8

In Tamaki’s second embodiment, an n-type impurity, for example, phosphorous or the like is implanted to “gate electrode formation film 206 on the n-type MIS formation region in the logic circuit section.” (See, e.g., Tamaki, ¶118, Figure 4B (below-top).) The n-type impurity implantation “with respect to the

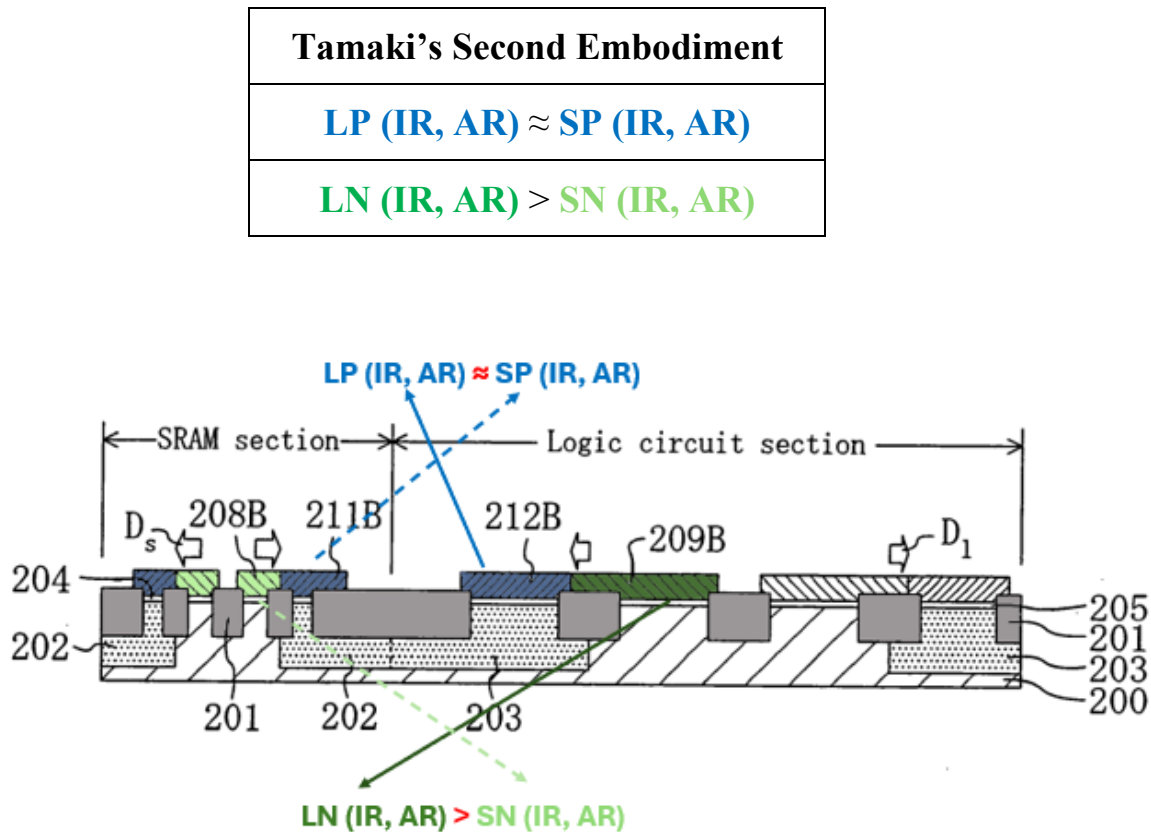
logic circuit section n-type gate electrode formation film 209 [is] performed under the conditions of, for example, an implantation energy of 10 keV and a dosage of 8×10^{15} atoms/cm².” (TSMC-1006, ¶118.) Because the entire gate electrode film is implanted uniformly in a single process step, the portion of the first gate electrode located on the first active region has substantially the same impurity concentration as the portion located over the isolation region. Accordingly, Tamaki’s second embodiment satisfies claim 8 under Scenario A-1.



Tamaki, Figures 4B (top), 5B (bottom) with enlargements

6. Claim 9

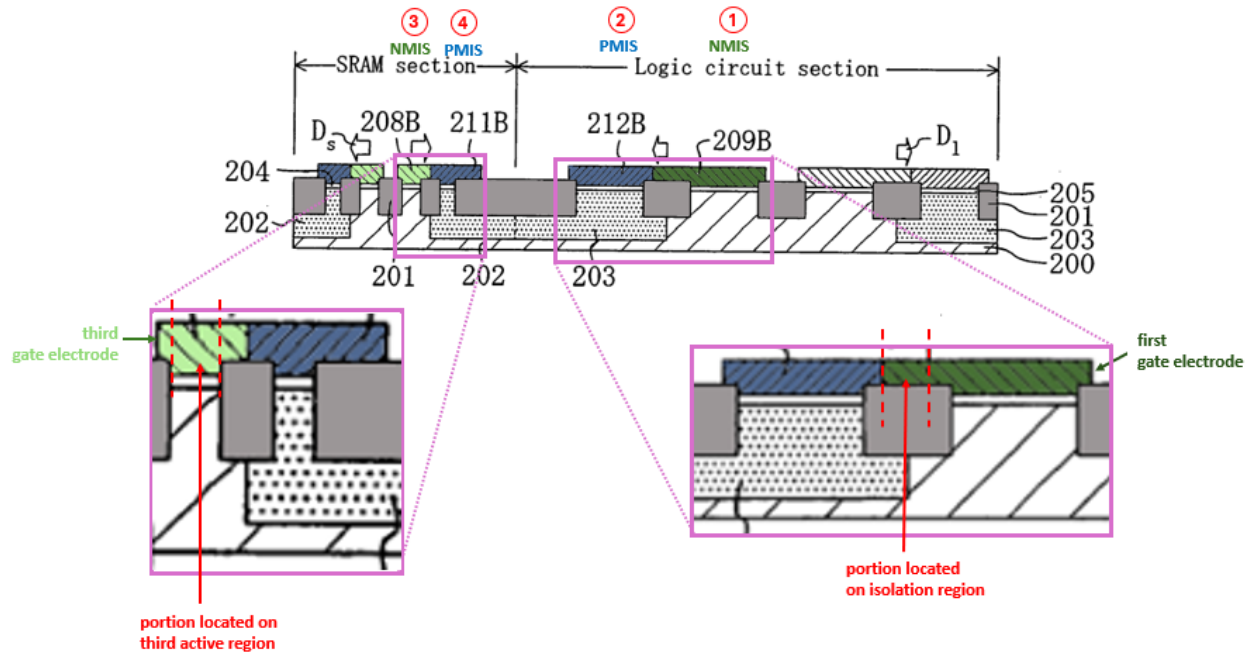
The impurity concentration relationship of Tamaki's second embodiment, discussed in §V.C, is:



Tamaki, Figure 5B

Accordingly, the portion of electrode 209 over the isolation region, $LN(IR)$, (“the first silicon film of the first conductivity type located on the isolation region”) has a higher n-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 208 over the active region, $SP(AR)$,

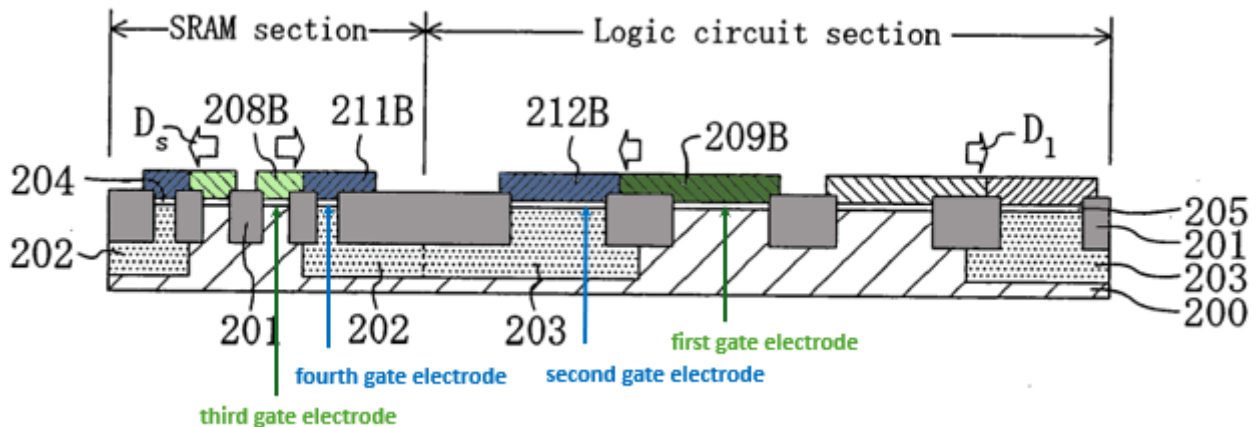
(“the second silicon film of the first conductivity type located on the third active region”). That is, **LN(IR) > SP(AR)**, satisfying claim 9 under Scenario A-1.



Tamaki, Figure 5B with enlargements

7. Claim 14

Tamaki’s second embodiment device includes an SRAM circuit and a logic circuit, each with corresponding gate electrodes. The SRAM circuit includes n-type gate electrode 208B [“*third gate electrode*”] and p-type gate electrode 211B [“*fourth gate electrode*”], while the logic circuit includes n-type gate electrode 209B [“*first gate electrode*”] and p-type gate electrode 212B [“*second gate electrode*”].” (TSMC-1006, ¶136.)



Tamaki, Figure 5B

VI. GROUND 2: Tamaki-Sumi Combination Renders Claims 5 and 7 Obvious

Tamaki does not explicitly disclose a dual-gate electrode having a portion of the silicon film located on an isolation region with a higher impurity concentration than a portion of the silicon film location on an active region (claims 5 and 7).

Sumi provides this teaching.

A. Tamaki-Sumi Combination

1. Mutual Dopant Diffusion in Dual-Gate Structures

Tamaki recognized issues posed by mutual dopant diffusion in dual-gate electrodes. Specifically, Tamaki noted that due to downstream thermal processing, such as during activation annealing of the source/drain, “phosphorous in the SRAM section n-type gate electrode [] and the boron in the SRAM section p-type gate electrode [] diffuse mutually in the integrally-formed n-type and p- type gate

electrodes” and “phosphorous in the logic circuit section n-type gate electrode [] and the boron in the logic circuit section p-type gate electrode [] diffuse mutually in the integrally-formed n-type and p- type gate electrodes.” (TSMC-1006, ¶22.) Consequently, the pn boundary between the n-type and p-type gate electrodes “shifts over the element isolation region [] to reach a point” on the gate insulating film located on the n-type well region (i.e., the active region). (TSMC-1006, ¶27.) This shifting of the pn boundary location “disables securing of the transistor characteristics” of the PMIS transistor, which negatively impacts device performance. (TSMC-1006, ¶26; TSMC-1003, ¶216.)

To mitigate variations in transistor characteristics caused by dopant diffusion Tamaki reduces both n-type and p-type impurity concentrations in the PMIS transistor and NMIS transistor of the SRAM section in Embodiment 1 and only the n-type concentration in Embodiment 2. (*See* §V.A; TSMC-1003, ¶217.) This effectively reduces the amount of phosphorus dopant available for diffusion because, according to Tamaki, “[t]he diffusion rate of phosphorus is higher than the diffusion rate of boron in general.” (TSMC-1006, ¶23.)

A POSITA would have understood Tamaki’s approach had limitations. While Tamaki’s method reduces dopant diffusion, the method does not eliminate it. (TSMC-1003, ¶218.) Further, there is a practical limit to how far dopant concentration can be reduced while maintaining device performance. (TSMC-

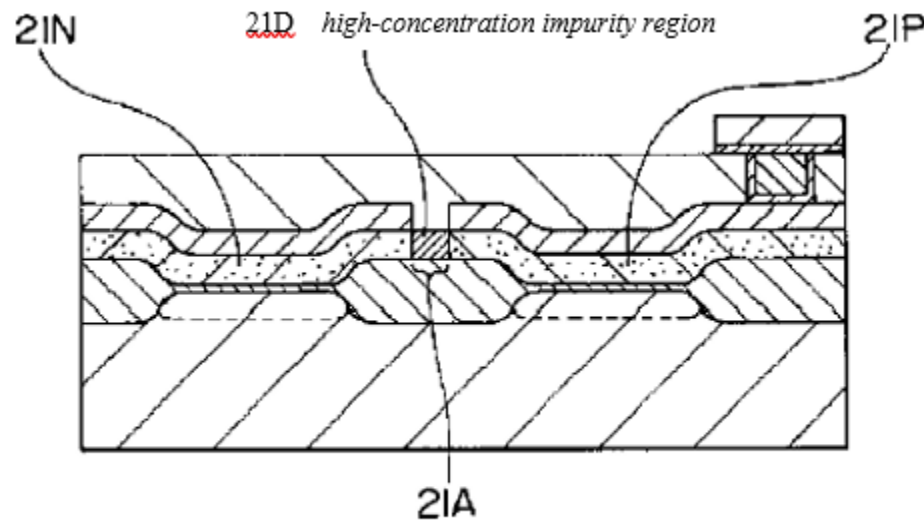
1003, ¶218.) As noted in Tamaki, SRAM regions are particularly vulnerable to mutual dopant diffusion due to narrower isolation between n-type and p-type MIS transistors. With continued device scaling, the width of the isolation region for both SRAM and logic regions continues to become narrower. (TSMC-1003, ¶218.) The need for further device scaling combined with limitations on the amount gate electrode dopants can be reduced would have led a POSITA to search for alternative approaches to address dopant diffusion for dual-gate structures in both logic and SRAM devices, such as disclosed by Sumi. (TSMC-1003, ¶218.)

2. Sumi's Technique

Like Tamaki, Sumi recognizes mutual dopant diffusion in dual-gate electrode structures is detrimental—not only to the dual-gate electrodes' integration in modern semiconductor devices but also to the overall device performance. (TSMC-1009, ¶11.) Accordingly, Sumi's objective is to provide a dual gate structure “that excels in suppressing mutual diffusion of impurities between gate electrodes.” (TSMC-1009, ¶13.)

To achieve this objective, Sumi's dual gate structure provides a high-concentration impurity region “in the connection region between the first conductivity type polycrystalline silicon layer and second conductivity type polycrystalline silicon layer, having a higher impurity concentration than each respective polycrystalline silicon layer.” (TSMC-1009, ¶15, *see also*, Sumi, ¶1.)

Specifically, Sumi's dual-gate structure includes "connection region 21A between the N-type polycrystalline silicon layer 21N and the P-type polycrystalline silicon layer 21P." (TSMC-1009, ¶63, Figure 5 (below).) Connection region 21A contains "a higher impurity concentration than that of the N-type and P-type polycrystalline silicon layers 21N and 21P." (TSMC-1009, ¶63.) As a result of this structure, "it becomes less likely for mutual diffusion of impurities to occur between the N-type and P-type polycrystalline silicon layers 21N and 21P." (TSMC-1009, ¶64.) That is, Sumi discloses use of a diffusion barrier between n-type and p-type regions.



An explanatory diagram of the second embodiment related to the dual gate structure of this invention.

Sumi, Figure 5

3. Combination of Tamaki and Sumi

A POSITA would have been motivated to combine Sumi's teaching regarding use of a high-concentration region to separate n-type and p-type regions

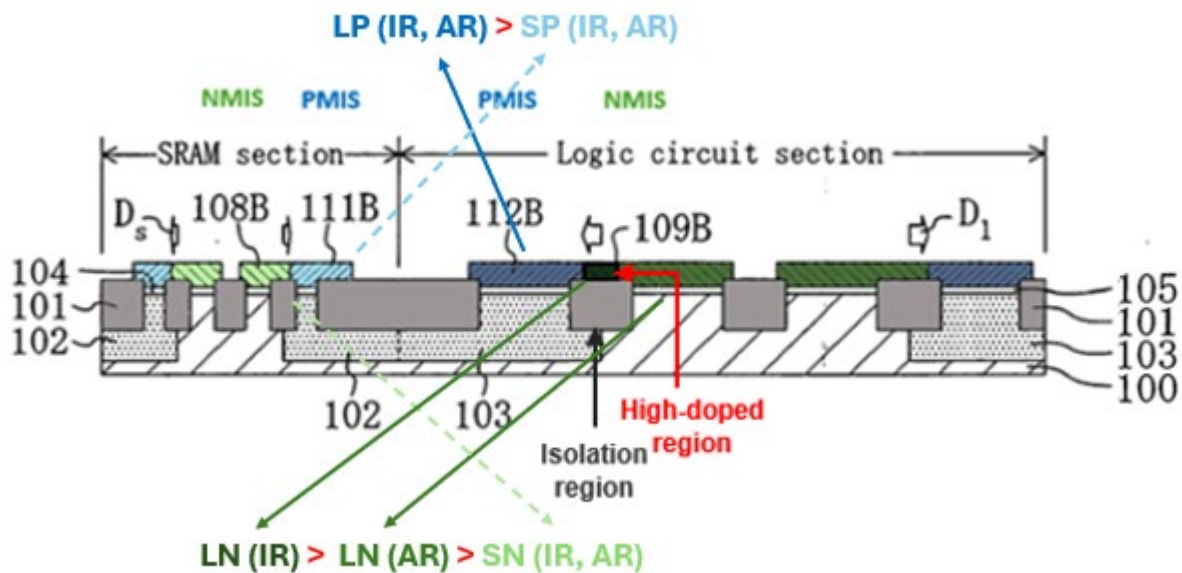
in dual-gate electrode structure with Tamaki's first and second embodiment devices. Specifically, a POSITA would have been motivated to form a high-concentration impurity region to act as a diffusion barrier, like Sumi's region 21D, at the pn junction in Tamaki's dual-gate electrode structures depicted in Figures 3B (first embodiment) and 5B (second embodiment)—i.e., over a portion of the STI region in the logic area, as taught by Sumi.

While Sumi mentions phosphorous as an example impurity for the high concentration region, Sumi does not exclude use of other dopants. (*See* Sumi, ¶63 (“high-concentration impurity region 21D contains impurities such as phosphorus (P)”); TSMC-1003, ¶224.) A POSITA would have also understood a highly doped region would serve as an effective diffusion barrier if it includes a silicon dopant with a lower diffusion rate than both boron and phosphorus—such as arsenic (As). (TSMC-1003, ¶224.) Because Tamaki uses phosphorus as its n-type gate electrode dopant, a POSITA would have been motivated to use a different dopant for the high concentration region, such as arsenic. (TSMC-1003, ¶224.) For example, Sumi uses arsenic as n-type dopant in silicon. (TSMC-1009, ¶¶ 21, 31, 37, 41, 63, 75; *see also*, TSMC-1007, ¶¶105-106 (discloses use of As as n-type dopant).) Additionally, arsenic is an n-type dopant widely used in the semiconductor industry. (TSMC-1003, ¶224.) Therefore, a POSITA would have been motivated to form a high-concentration, arsenic-doped region at the pn boundary of Tamaki's

dual-gate structures over the isolation region to further suppress phosphorus and boron diffusion, enabling continued scaling of both SRAM and logic circuit sections in future technology nodes. (§VI.A.1; TSMC-1003, ¶224.)

The impurity concentration relationship for Tamaki's **first embodiment** combined with Sumi, illustrated in modified Figure 3B below, is:

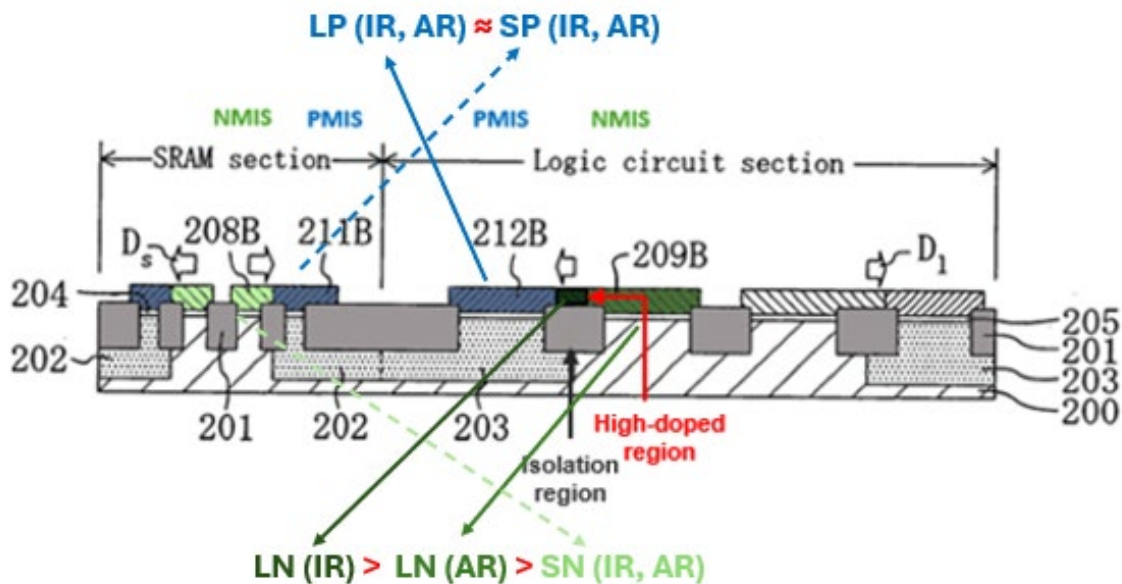
Tamaki's First Embodiment-Sumi
$LP(AR) > SP(IR, AR)$
$LN(IR) > LN(AR) > SN(IR, AR)$



Tamaki Figure 3B (First Embodiment)-Sumi Combination

The impurity concentration relationship for Tamaki's **second embodiment** combined with Sumi, illustrated in modified Figure 5B below, is:

Tamaki's Second Embodiment-Sumi
$LP(AR) \approx SP(AR)$
$LN(IR) > LN(AR) > SN(IR, AR)$



Tamaki Figure 5B (Second Embodiment)-Sumi Combination

4. Motivation to Combine

A POSITA would have been motivated to make this combination to overcome limitations of Tamaki's approach discussed in §VI.A.1 and to facilitate further scaling of Tamaki's design. (TSMC-1003, ¶227.) As discussed in §VI.A.2, Sumi also motivates this combination, stressing the benefits of use of a dopant diffusion barrier. A POSITA would have understood based on the suggestions of

Tamaki and Sumi that the Tamaki (first and second embodiments)-Sumi combination drastically reduces dopant interdiffusion across the dual-gate electrode and, by extension, minimizes variations in transistor characteristics, including threshold voltage variation, which is highly desirable and further motivates the combination. (TSMC-1003, ¶227.)

Moreover, Tamaki and Sumi are in the same field of endeavor as the '373 patent, semiconductor devices. (TSMC-1001, 1:15-20, 3:42-46; TSMC-1006, ¶¶2-4; TSMC-1009, ¶¶11, 13.)

Additionally, the combination is nothing more than the application of a known technique (Sumi's fabrication of dual-gate electrode devices with a high-doped region) to a known device (Tamaki's dual-gate electrode) ready for improvement for the reasons discussed above. (TSMC-1003, ¶229.) *KSR Int'l. Co. v. Teleflex Inc.*, 550 U.S. 398, 416-417.

A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable. (TSMC-1003, ¶230.) Sumi's teaching aligns with a POSITA's understanding that dopants diffuse at different rates in silicon (TSMC-1017, Figure 4a, 456), and that regions with high concentrations of dopants with lower diffusion rates can act as diffusion barriers to dopants with higher diffusion rates. This well-established practice in the industry was well-known before the priority date of the '373 patent. For instance,

Bayraktaroglu (TSMC-1018) discusses a p-n junction diffusion barrier

“comprising a first semiconductor layer 28 of p-type conductivity, a second semiconductor layer 32 of n-type conductivity and a third semiconductor layer 30 of p-type conductivity disposed between the first and second layers, the third layer being doped with a relatively low diffusivity dopant in order to **form a diffusion barrier** between the first and the second semiconductor layers.” (TSMC-1018, Abstract.)

Further, implementing Sumi’s teachings into Tamaki’s dual-gate electrode structure would have been well within the skill set of a POSITA because the combination involves standard fabrication techniques and concepts, such as the formation of high concentration As-doped regions, that were well understood before the ’373 patent. (TSMC-1003, ¶231.) A POSITA would have also understood the process steps for forming a high concentration n-type doped region, like Sumi’s, are compatible with Tamaki’s process flow, for at least two reasons. (TSMC-1003, ¶231.)

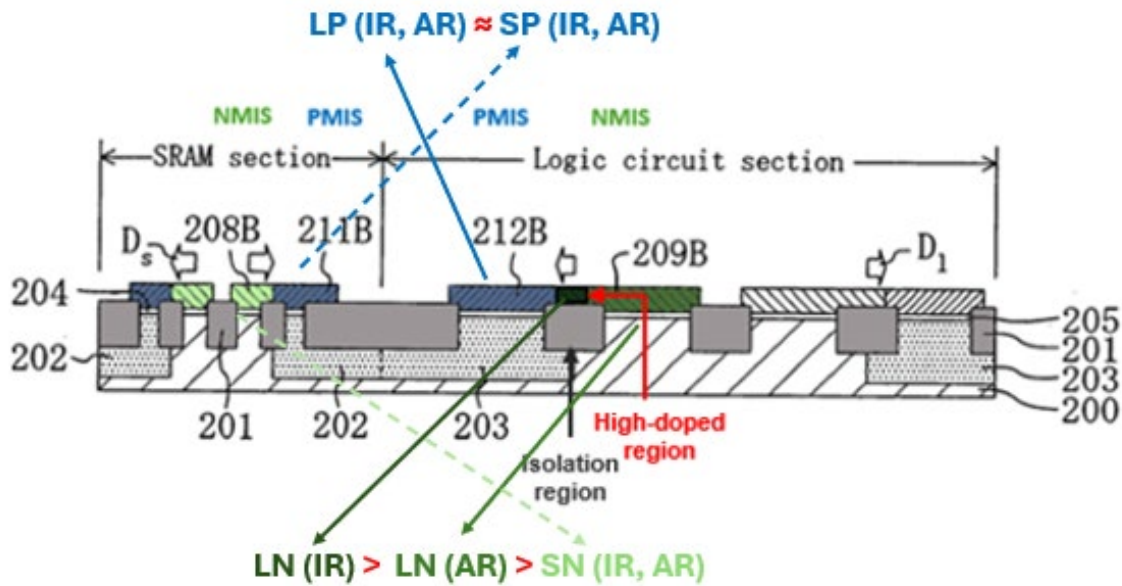
First, forming the high-concentration region is an independent step requiring its own dedicated photolithography mask for the n-type implant step at the pn-junction over a portion of the isolation structure, as discussed above in connection to Figure 6(2). (TSMC-1009, ¶¶72-73.) Second, Tamaki does not disclose any other masks or process steps specifically targeting the pn-junction of the p-type

and n-type electrodes over at least the isolation structure of the logic circuit section, and therefore introducing Sumi's steps for forming the high concentration n-doped region would not interfere with other process steps. (TSMC-1003, ¶232.) For example, a POSITA would incorporate Sumi's steps for forming the high-concentration arsenic-doped region prior to the implantation of phosphorus or similar dopants into the gate electrode formation film 106 of the n-type MIS region in the logic circuit section, as shown in Tamaki's Figure 1B (TSMC-1006, ¶85). This is because, in Sumi's process, the high-concentration n-type region is created before gate electrode doping (TSMC-1009, ¶¶73–75), which is consistent with the dopant flow described in Tamaki. (TSMC-1003, ¶232.)

B. Tamaki (Second Embodiment)-Sumi Combination Renders Claim 5 Obvious.

The impurity concentration relationship of Tamaki's second embodiment combined with Sumi, discussed in §V.C, is summarized below:

Tamaki's Second Embodiment-Sumi
LP (AR) $\approx$ SP (IR, AR)
LN (IR) > LN (AR) > SN (IR, AR)



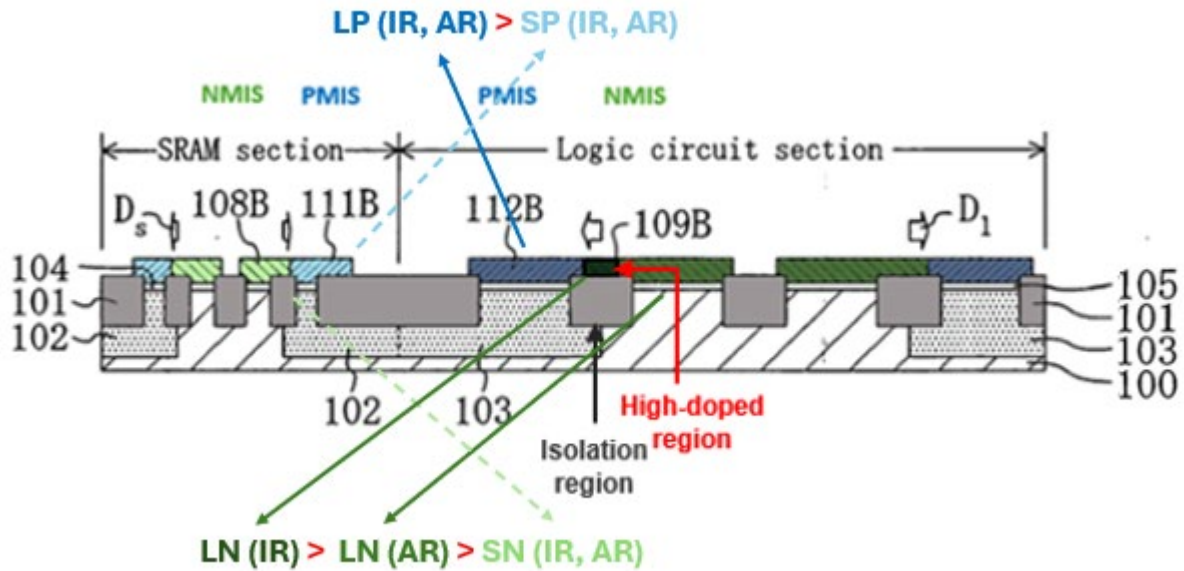
Tamiki Figure 5B (Second Embodiment)-Sumi Combination

Accordingly, the portion of electrode 209 over the active region, $LN(AR)$, (“portion of the first silicon film of the first conductivity type located on the first active region”) has a lower n-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode 209 over the isolation region, $LN(IR)$ (“portion of the first silicon film of the first conductivity type located on the isolation region”). That is, $LN(AR) < LN(IR)$, satisfying claim 5 under Scenario A-1.

C. Tamaki (First Embodiment)-Sumi Combination Renders Claim 7 Obvious

The impurity concentration relationship of Tamaki’s first embodiment combined with Sumi, discussed in §V.B, is summarized below:

Tamaki's First Embodiment-Sumi
LP (AR) > SP (IR, AR)
LN(IR) > LN (AR) > SN (IR, AR)



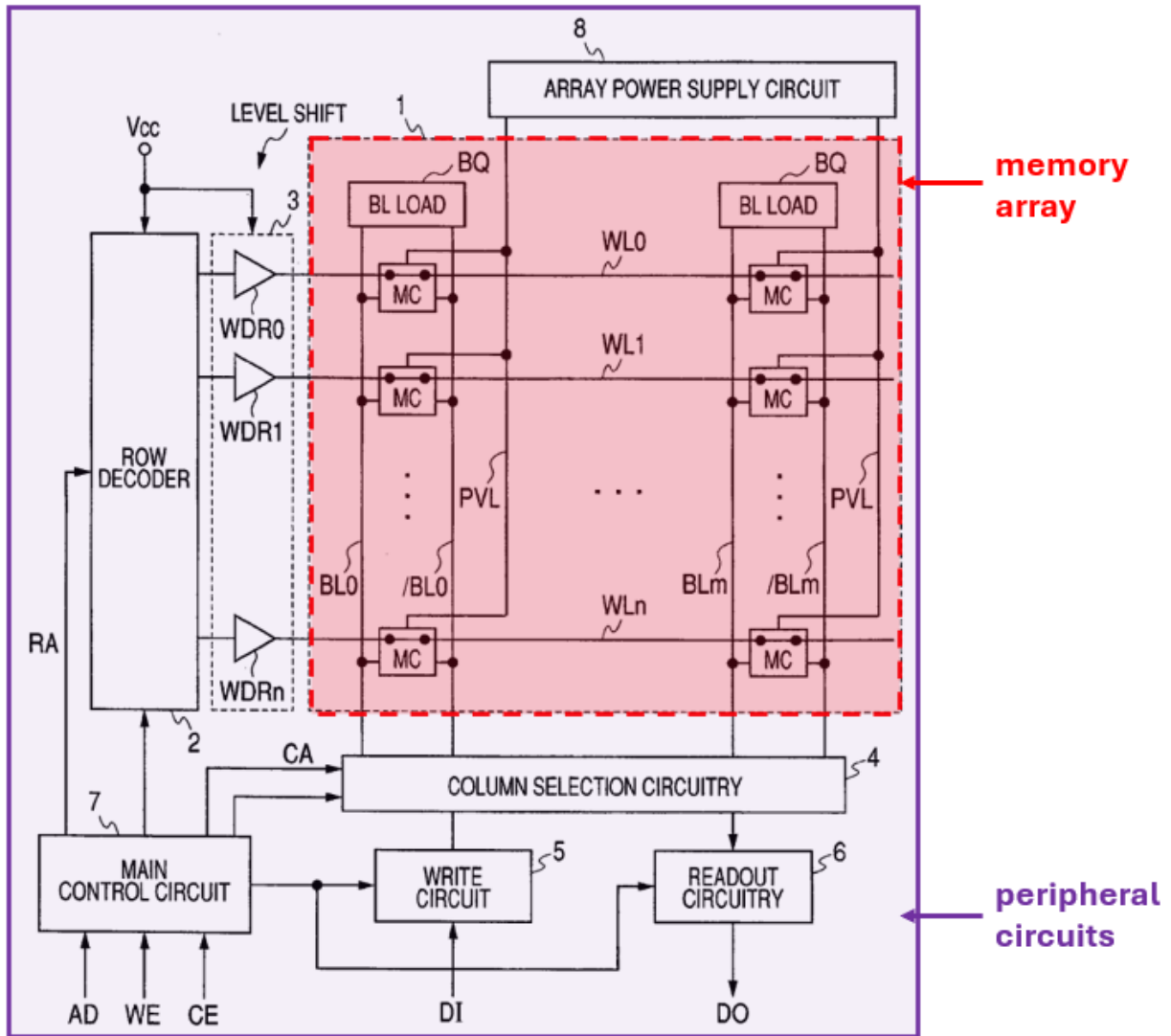
Tamaki Figure 3B (First Embodiment)-Sumi Combination

Accordingly, the portion of electrode 109 over the active region, **LN(AR)**, (“portion of the first silicon film of the second conductivity type located on the second active region”) has a lower n-type impurity concentration (“second-conductivity-type impurity concentration”) than the portion of electrode 109 over the isolation region, **LN(IR)** (“portion of the first silicon film of the second conductivity type located on the isolation region”). That is, **LN(AR) < LN(IR)**, satisfying claim 7 under Scenario B-1.

VII. GROUND 3: Igarashi Renders Claims 1-4, 6, and 8-14 Obvious.

A. Igarashi Overview

Igarashi describes a “semiconductor memory device” including (1) a memory array 1 (red) having memory cells (MC) and (2) peripheral circuits (purple) such as word line driver 3. (TSMC-1007, Abstract, ¶¶37-48, Figure 1 (below).)



Igarashi, Figure 1

This Petition focuses on Igarashi's second embodiment (Figures 10, 11A-11E) which renders claims 1-4 and 8-14 obvious under Scenario B-1 and claims 1, 6, and 9-10 obvious under Scenario A-1.

B. Independent Claim 1

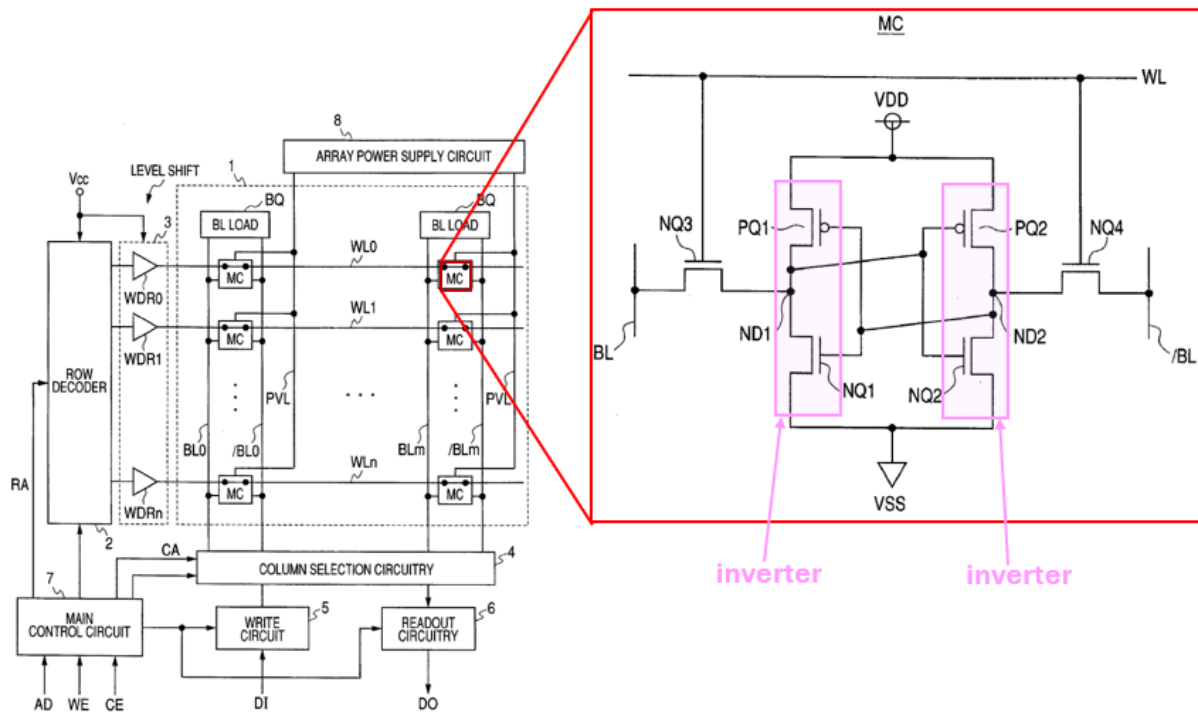
1. Preamble [1P]

Igarashi's second embodiment discloses a "*semiconductor device*." Igarashi relates to "**semiconductor memory devices**." (TSMC-1007, ¶2, *see also* Igarashi, Abstract, ¶11 (describing "semiconductor memory device"), claims 3-5 (reciting "semiconductor memory device" comprising "memory array" and "peripheral circuit").)

2. "First Dual-Gate Electrode"/"Second Dual-Gate Electrode" Limitations [1A]-[1F]

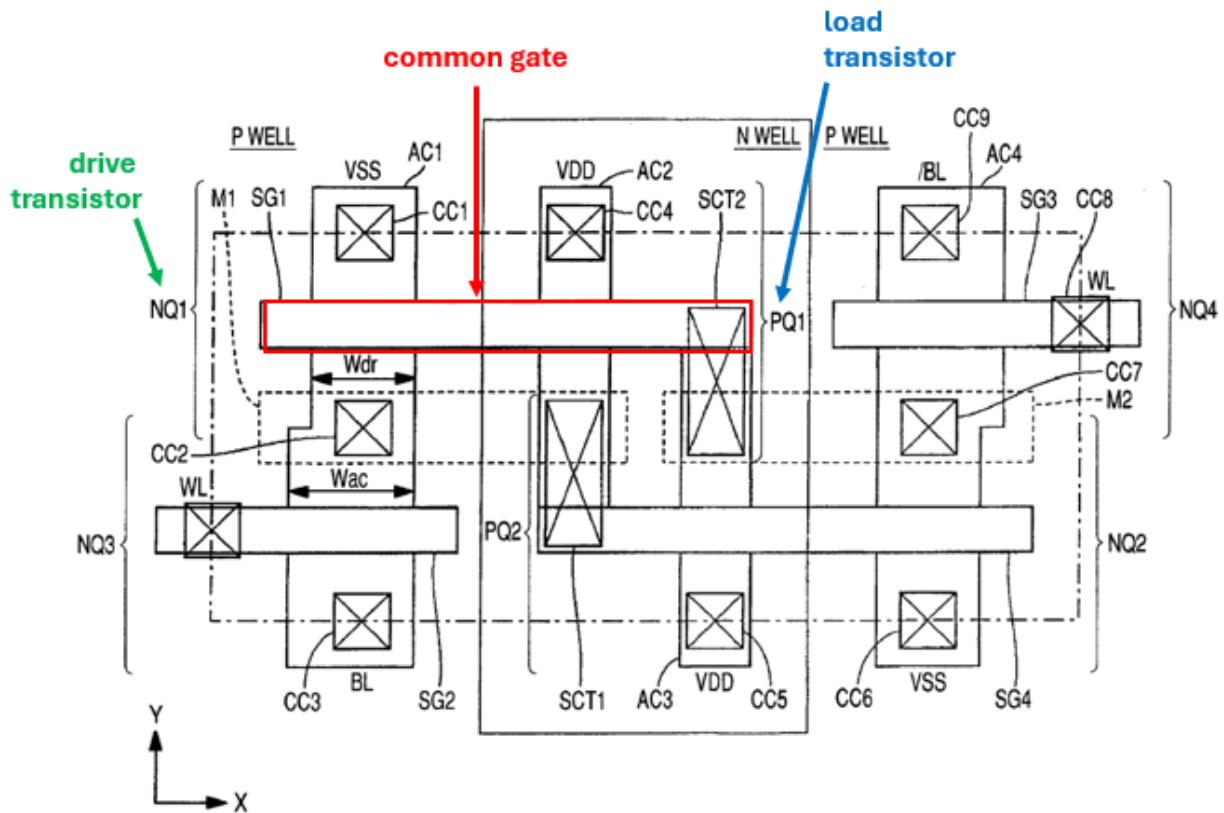
a. SRAM Memory Cell

Igarashi's memory array includes multiple SRAM memory cells (MCs). An exemplary 6-Transistor SRAM memory cell (Figure 2 (below-right)) comprises two access transistors (NQ3/NQ4) for enabling read/write operations and a pair of cross-coupled inverters, each having a load PMOS transistor (PQ1/PQ2) and a drive NMOS transistor (NQ1/NQ2). (*See*, Igarashi, ¶¶49-50, Figure 2 (below); Weste, 715-716.)



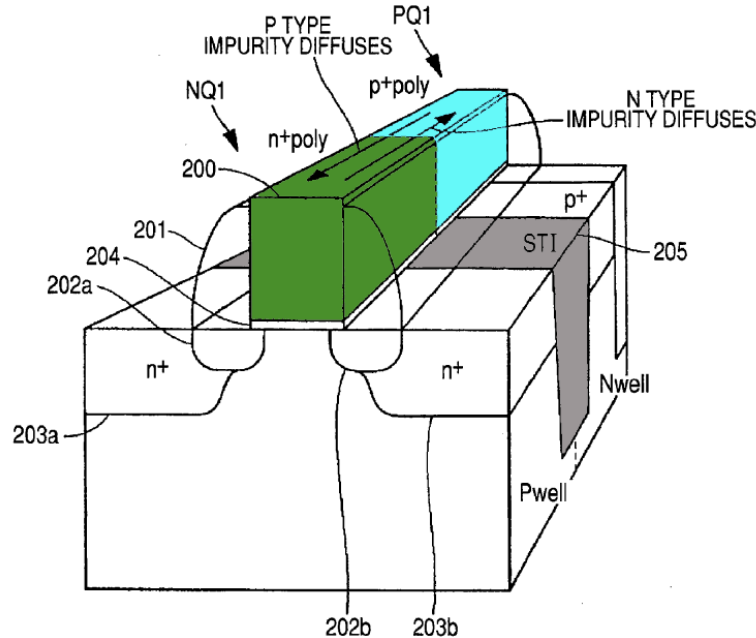
Igarashi, Figure 1 (left), Figure 2 (right)

In the Figure 3 layout, load transistors (PQ1/PQ2) “are formed in active regions AC2 and AC3” and drive transistors (NQ1/NQ2) are formed “[i]n active regions AC1 and AC4.” (TSMC-1007, ¶53.) “Polysilicon wiring SG1 forms the common gate of load transistor PQ1 and driver transistor NQ1” and “[p]olysilicon wiring SG4 forms the common gate of load transistor PQ2 and driver transistor NQ2.” (TSMC-1007, ¶¶57, 60.)



Igarashi, Figure 3

Figure 9, reproduced below, illustrates SRAM memory cell inverter having a drive transistor (NQ1) “which shares a **polysilicon** gate” with a load transistor (PQ1). (TSMC-1007, ¶85.) NMOS drive transistor NQ1 “is formed on” the p-well and load PMOS transistor PQ1 is formed on the n-well, separated by STI (gray). (TSMC-1007, ¶¶86-88.) Polysilicon gate 200 includes an “impurity of an N type [green] implanted to the region (N+poly) at the side of transistor NQ1” and an “impurity of a P type [blue] implanted to the region (P+poly) at the side of transistor PQ1.” (TSMC-1007, ¶86.)



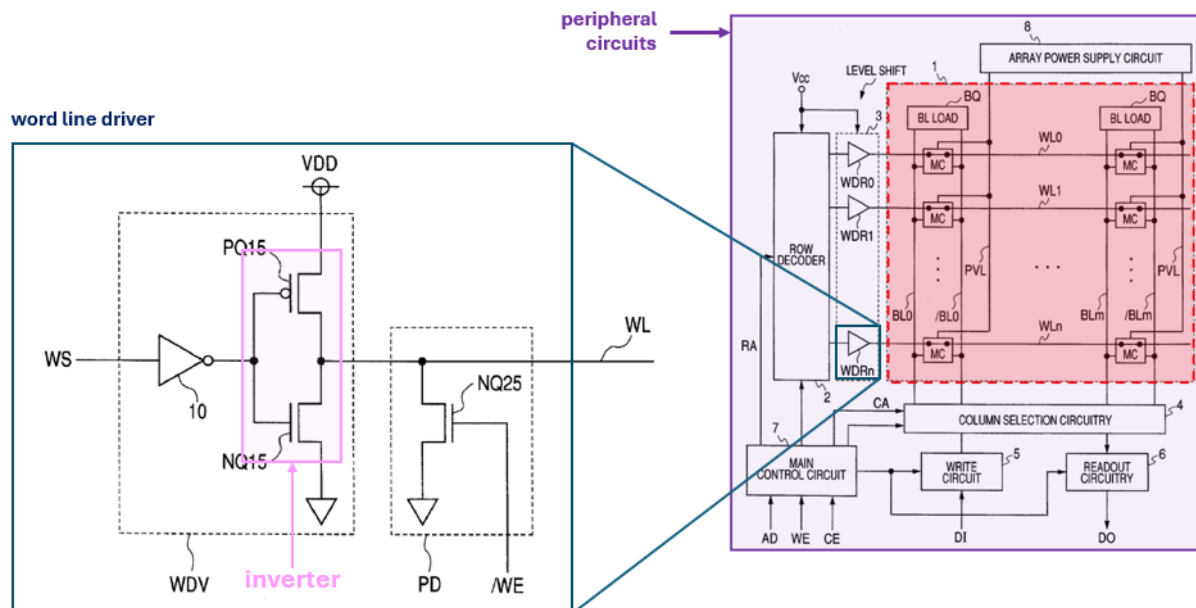
Igarashi, Figure 9

Thus, the PMOS transistor of the SRAM memory cell inverter includes a “*gate electrode... having a [] silicon film [polysilicon] of a [] conductivity type [p-type]*” and the NMOS transistor includes a “*gate electrode ... having a [] silicon film [polysilicon] of a [] conductivity type [n-type]*” [1C]. (TSMC-1003, ¶248.) Collectively, these form a “*dual-gate electrode*” [1A] and “*are connected to each other on the isolation region [STI]*” [1F], as shown in Figure 9 above. (TSMC-1003, ¶248; *see, e.g.*, Igarashi, ¶88 (“polysilicon gate 200 is shared”).)

b. Peripheral (Logic) Circuit

Igarashi’s device also includes PMOS and NMOS transistors “which form [the] peripheral circuit, that is, the circuit for controlling the interior action of a memory array”; i.e., a logic circuit. (TSMC-1007, ¶96; TSMC-1003, ¶249.) The

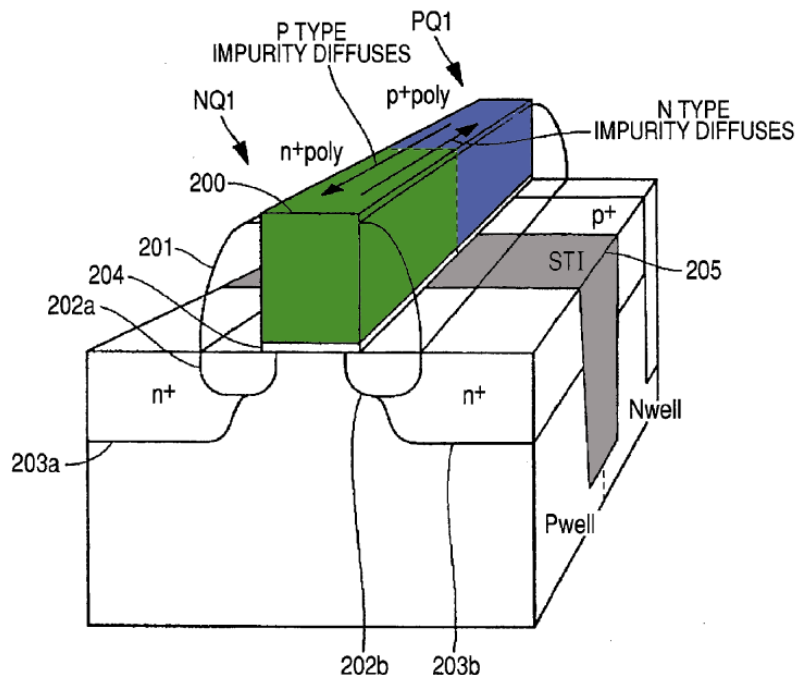
peripheral circuit includes, e.g., word line driver (WDR) circuit 3 comprising an inverter (shaded pink) which consists of PMOS transistor (PQ15) and NMOS transistor (NQ15) sharing a common gate electrode. (TSMC-1007, ¶¶37-48, 134-136, Figure 15 (below).)



Igarashi, Figure 15 (left), Figure 1 (right)

A POSITA would recognize the similarity between the inverter circuits shown in Figure 15 of the WDR circuit and Figure 2 of the MC, and would consider them to be effectively identical dual-gate electrode structures. (TSMC-1003, ¶250). As discussed above, Igarashi's Figure 9 (reproduced below) illustrates an inverter structure in which the PMOS and NMOS transistors share a polysilicon gate electrode. (TSMC-1007, ¶¶85, 88.) Although Igarashi describes Figure 9 with respect to an SRAM memory cell, a POSITA would have understood this shared-

gate configuration (dual-gate electrode) applies not only to inverters in the SRAM region but also to inverters in the peripheral logic circuits or would have been motivated to use such a structure. (TSMC-1003, ¶250.) First, the '373 patent admits that “conventional semiconductor devices” used dual-gate electrodes in the logic section. (TSMC-1001, 1:48-52, 2:43-46, 7:33-43, Figures 15A-15B, 16 (“prior art”).) Second, using a unified inverted design approach across memory and logic circuitry promotes process uniformity by limiting design variability and reduces fabrication complexity (e.g., mask layers, etching steps, and material changes), leading to more efficient production and lower costs. (TSMC-1003, ¶251.)



Igarashi, Figure 9

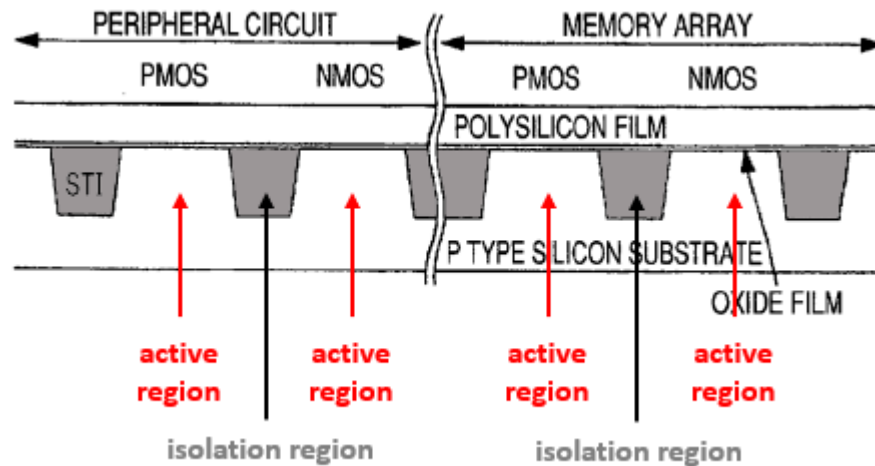
Accordingly, like the SRAM memory cell inverter, the PMOS transistor of the WDR inverter includes a “*gate electrode... having a [] silicon film [polysilicon] of a [] conductivity type [p-type]*” and the NMOS transistor includes a “*gate electrode ... having a [] silicon film [polysilicon] of a [] conductivity type [n-type]*” [1C]. (TSMC-1003, ¶252.) Collectively, these form a “*dual-gate electrode*” [1A] and “*are connected to each other on the isolation region*” [1F], as shown in Figure 9 above. (TSMC-1003, ¶252; *see, e.g.*, Igarashi, ¶88.)

c. Transistor Formation

The process of forming the memory array and peripheral circuit transistors confirms the arrangement discussed above. First, an oxide film is formed on the substrate and “the polysilicon film is formed on it.” (TSMC-1007, ¶99, Figure 11A (below).) That is, the SRAM transistor includes a “*silicon film*” and the logic transistor also includes a “*silicon film*.” Igarashi teaches the NMOS transistor “is formed on” the p-well, while the PMOS transistor is “formed on an n-well.”⁷ (TSMC-1007, ¶¶86, 99.) A POSITA would have understood “*active region(s)*” are in these wells. (TSMC-1003, ¶253; *see, e.g.*, Igarashi, ¶52 (describing “active

⁷ Igarashi omits the n-well and p-well from Figure 11A “to simplify.” (TSMC-1007, ¶99.)

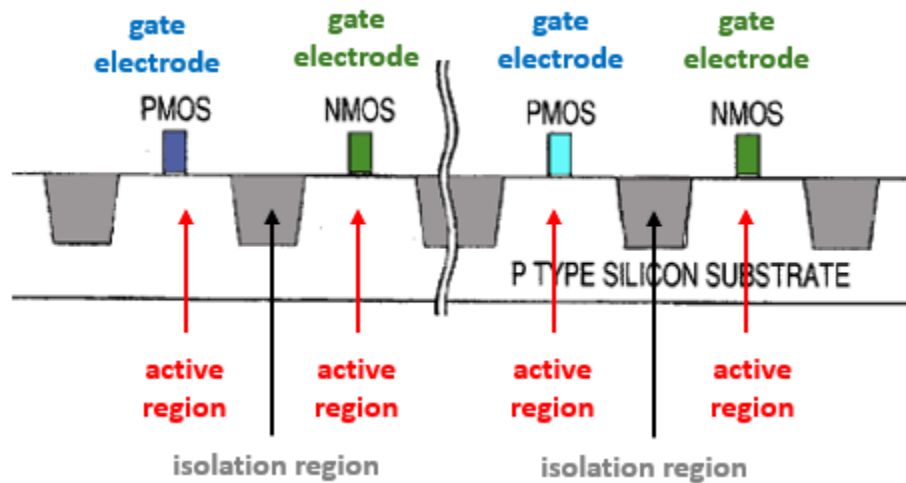
regions ... formed in N well region” and active regions formed “in each of P well region”), ¶53); *see also*, TSMC-1001, 1:65-2:4 (describing NMIS/PMIS transistors formed in n-well and p-well); Weste, 117-118; Plummer, 60-63.)



Igarashi, Figure 11A

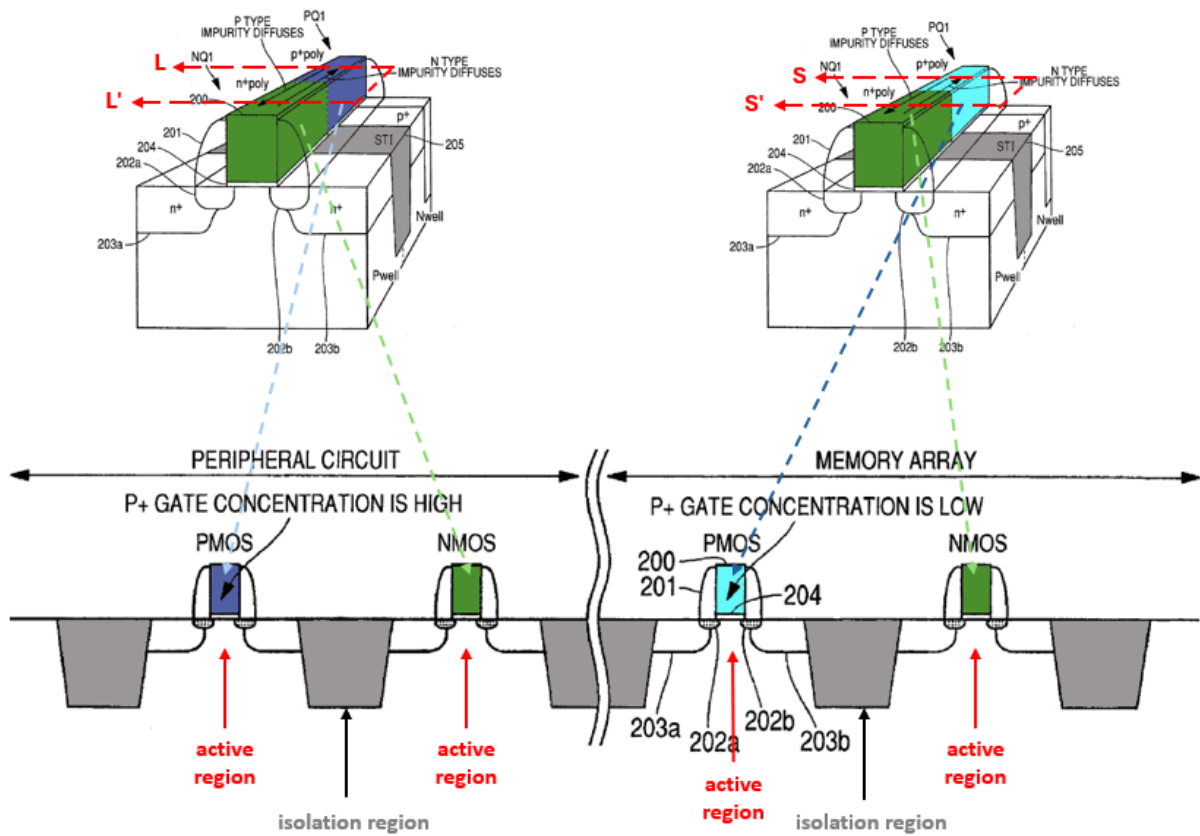
As shown in Figure 11A, an STI region is formed between the PMOS and NMOS active regions. (See, Weste, 119-120; Plummer, 57-60 (describing use of isolation structures); TSMC-1001, 1:65-2:7 (describing AAPA including isolation regions between active regions).) Thus, Igarashi discloses or suggests the PMOS transistor “*active region*” and the NMOS transistor “*active region*” “*are isolated from each other with an isolation region interposed therebetween*” [1E]. (TSMC-1003, ¶254; *see also*, Igarashi, Figure 9, ¶88.)

Subsequently, the polysilicon gates are formed “by etching.” (TSMC-1007, ¶102, Figure 11D (below).) As shown, each gate electrode is formed on an “*active region*.” (TSMC-1003, ¶255.)



Igarashi, Figure 11D

Igarashi’s Figure 10 “is a drawing explaining the impurity concentration implanted into the transistor formed in the memory array and peripheral circuit.” (See Igarashi, ¶¶95, 27-28.) Based on this disclosure, a POSITA would have understood the peripheral circuit (left) depicts the inverter of Figure 9 along the L-L’ line (left-top) and the memory array (right) depicts the inverter of Figure 9 along the S-S’ line. (TSMC-1003, ¶¶256-257.)



Igarashi, Figure 9 (top-left and top-right), Figure 10 (bottom)

Igarashi meets limitations [1A]-[1F] in the manner set forth in the following table for Scenarios A-1, A-2, B-1, and B-2:

		A-1	A-2	B-1	B-2
first dual-gate electrode	first gate electrode on a first active region and having a first silicon film of a first conductivity type	logic NMOS	SRAM NMOS	logic PMOS	SRAM PMOS
	second gate electrode on a second active region and	logic PMOS	SRAM PMOS	logic NMOS	SRAM NMOS

	<i>having a first silicon film of a second conductivity type</i>				
<i>second dual-gate electrode</i>	<i>third gate electrode located on a third active region and having a second silicon film of the first conductivity type</i>	SRAM NMOS	logic NMOS	SRAM PMOS	logic PMOS
	<i>fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type</i>	SRAM PMOS	logic PMOS	SRAM NMOS	logic NMOS

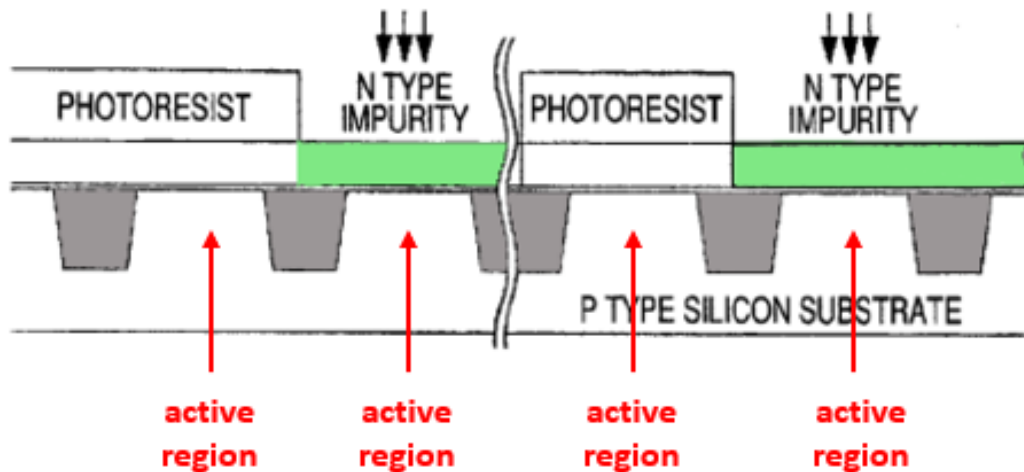
Igarashi also discloses the “*second dual-gate electrode being separated from the first dual-gate electrode*” [1B] under each Scenario. (TSMC-1003, ¶259.)

Figures 10, 11A-11E show a physical separation between the peripheral circuit and the memory array. Igarashi confirms the structure of the figures teaching memory array 1 is formed separately from the “peripheral circuits, such as word line drive circuit 3.” (TSMC-1007, ¶¶37, 48.)

3. Limitation [1G]

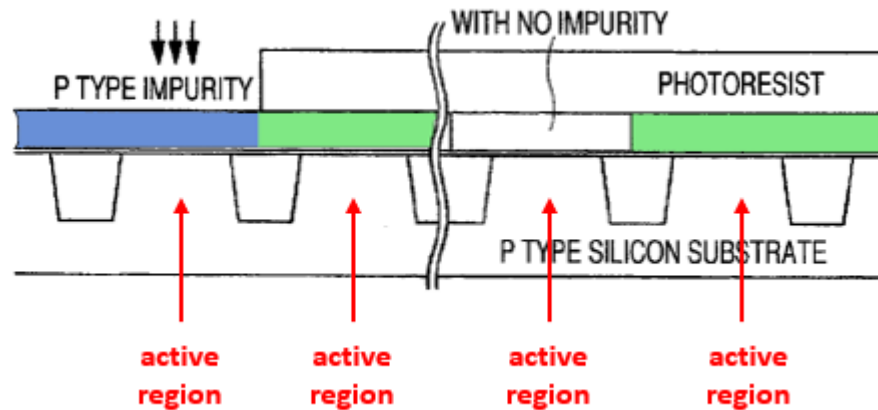
Igarashi discloses doping of the polysilicon gate electrodes in both the peripheral (logic) and SRAM circuits. Specifically, during fabrication of the peripheral (logic) circuits, an N-type impurity (e.g., phosphorus) is implanted into the polysilicon gate of the NMOS transistors in both the peripheral (logic) and SRAM circuits. (TSMC-1007, ¶100, Figure 11B (below).) For example,

phosphorus is implanted at a dose of about 4×10^{15} to 6×10^{15} atoms/cm². (TSMC-1007, ¶100.)



Igarashi, Figure 11B

To form the logic PMOS transistor gate, a P-type impurity (e.g., boron) is implanted after masking the NMOS region of the peripheral circuit and the entire SRAM (memory) circuit. (TSMC-1007, ¶101, Figure 11C.) For example, Boron is implanted at a dose of about 2×10^{15} to 4×10^{15} atoms/cm² in the logic PMOS transistor gate electrode. (TSMC-1007, ¶101.) Because the gate of the SRAM PMOS transistor “is covered with resist, a P type impurity is not implanted” in SRAM PMOS transistor. (TSMC-1007, ¶101, Figure 11C (below).) Consequently, “it is possible to change the implantation concentration of a P type impurity” of the device such that the implantation concentration in the SRAM PMOS gate is lower than that in the peripheral (logic) PMOS gate. (TSMC-1007, ¶¶110-111.)



Igarashi, Figure 11C

After lithographic patterning of the gate electrodes (TSMC-1007, ¶102, Figure 11D), additional source/drain implants are performed. Igarashi masks all regions except the memory PMOS transistor and implants boron or BF_2^+ at 1×10^{14} to 5×10^{14} atoms/cm². (TSMC-1007, ¶103.) Because the gate electrode is unmasked, this dopant is also introduced into the SRAM PMOS transistor's gate. (TSMC-1007, ¶103.) Next, Igarashi masks all regions except the peripheral PMOS transistor and implants boron or boron fluoride (B or BF_2^+) at 1×10^{14} to 5×10^{14} atoms/cm² into the unmasked PMOS region—including its gate electrode. (TSMC-1007, ¶104.)

To dope the source/drain of the memory NMOS transistor, arsenic is implanted at 0.5×10^{15} to 1×10^{15} atoms/cm² after masking the rest of the chip. (TSMC-1007, ¶105.) As the NMOS gate is unmasked, the gate also receives this dopant. Subsequently, arsenic (As) is implanted at 0.5×10^{15} to 1×10^{15} atoms/cm²

into the NMOS source/drain region of the peripheral transistor, again affecting the unmasked NMOS gate electrode. (TSMC-1007, ¶106.)

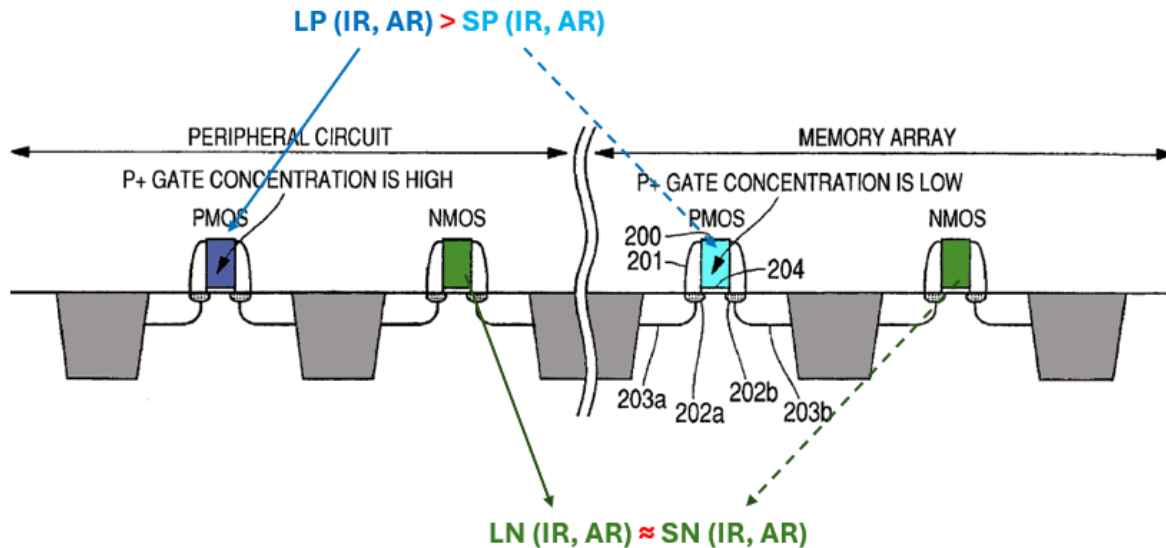
Further processing steps include an additional boron or BF_2^+ implant into the PMOS region (3×10^{15} to 4×10^{15} atoms/cm²) and a final arsenic implant into the NMOS region (1×10^{15} to 4×10^{15} atoms/cm²). (TSMC-1007, ¶¶108–109.) Because the respective gates are unmasked during these steps, the implanted dopants also affect the gate electrodes.

The following table summarizes the exemplary implants discussed above for both the memory and peripheral transistors.

	PMOS-Peripheral	PMOS-Memory
gate electrode implant	2×10^{15} – 4×10^{15} atoms/cm ²	N/A
1 st S/D implant	1×10^{14} – 5×10^{14} atoms/cm ²	1×10^{14} – 5×10^{14} atoms/cm ²
2 nd S/D implant	3×10^{15} – 4×10^{15} atoms/cm ²	3×10^{15} – 4×10^{15} atoms/cm ²
	NMOS-Peripheral	NMOS-Memory
gate electrode implant	4×10^{15} – 6×10^{15} atoms/cm ²	4×10^{15} – 6×10^{15} atoms/cm ²
1 st S/D implant	0.5×10^{15} – 1×10^{15} atoms/cm ²	0.5×10^{15} – 1×10^{15} atoms/cm ²
2 nd S/D implant	1×10^{15} – 4×10^{15} atoms/cm ²	1×10^{15} – 4×10^{15} atoms/cm ²

Accordingly, the impurity concentration relationship disclosed in Igarashi's second embodiment can be expressed as follows:

Igarashi's Second Embodiment
$LP (IR, AR) > SP (IR, AR)$
$LN (IR, AR) \approx SN (IR, AR)$
LP: peripheral (logic) PMOS SP: SRAM PMOS LN: peripheral (logic) NMOS SN: SRAM NMOS



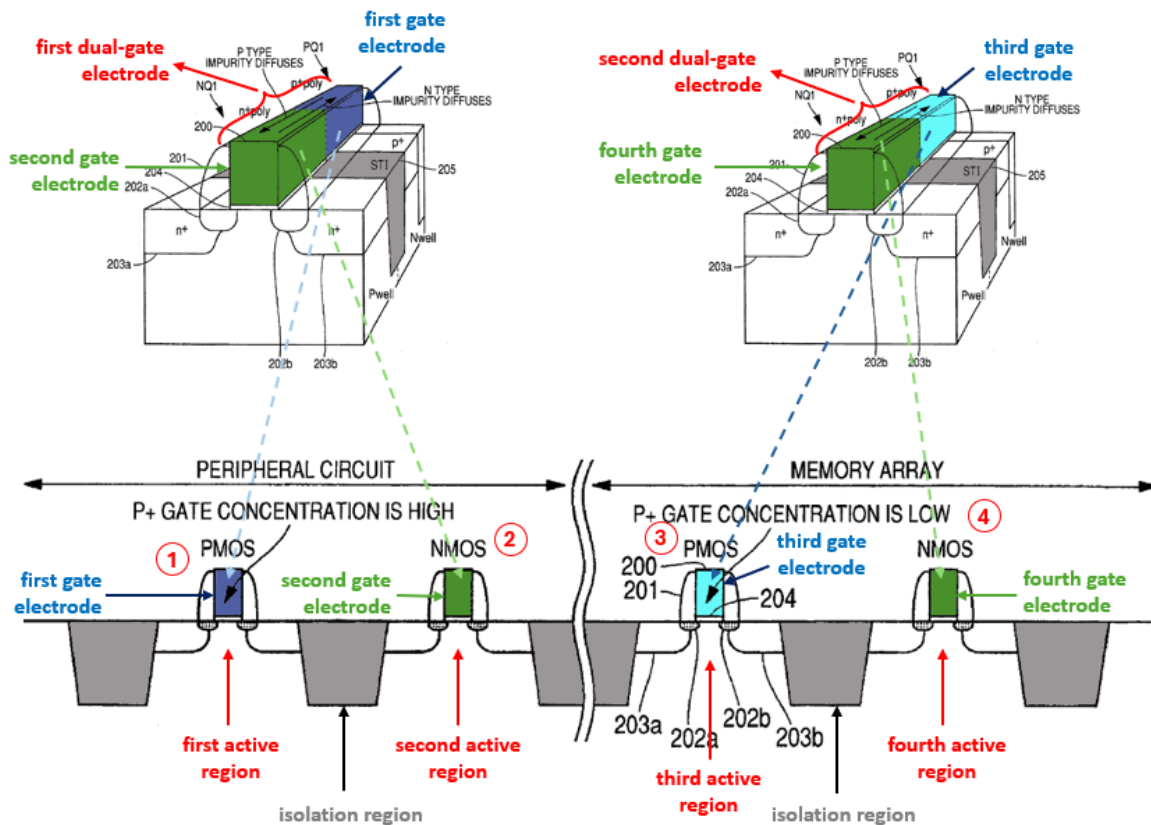
Igarashi, Figure 10

Igarashi therefore discloses limitation [1G]: “at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region” under scenario B-1. (TSMC-1003, ¶¶260-267.)

	Claimed Impurity Concentration Relationship Under Each Scenario	Igarashi Impurity Concentration Relationship
A-1	LN(IR, AR) > SN(AR)	
A-2	SN(IR, AR) > LN(AR)	
B-1	LP(IR, AR) > SP(AR)	LP(IR, AR) > SP(IR, AR)
B-2	SP(IR, AR) > LP(AR)	

4. Summary

In summary, Igarashi renders claim 1 obvious under Scenario B-1 as shown in the illustration below.



Igarashi, Figure 9 (left/right-top), Figure 10 (bottom)

C. Claim 2

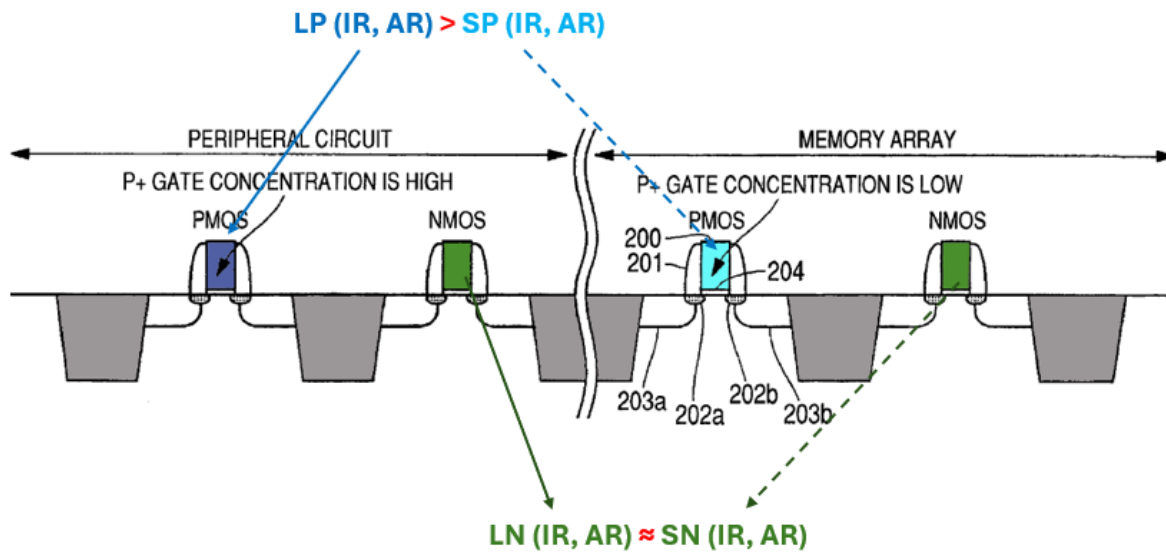
Igarashi's second embodiment explicitly discloses an SRAM memory array containing SRAM memory cells (TSMC-1007, ¶¶92, 96) and logic circuits. (TSMC-1007, ¶96 (peripheral circuit is “**the circuit for controlling the interior action of a memory array**”).) Igarashi acknowledges the trend toward a larger SRAM bit capacities and system integration, and notes the resulting demand to shrink SRAM cell sizes. (TSMC-1007, ¶4.)

Accordingly, a POSITA would understand integrating SRAM and logic circuits using Igarashi’s dual-gate structure layout demands circuit-specific layout strategies. (TSMC-1003, ¶271.) SRAM requires high density and low leakage, while logic circuitry typically demands greater spacing and isolation for signal integrity and noise suppression. (TSMC-1003, ¶271.) Given these distinct requirements, a POSITA would naturally increase isolation widths between peripheral circuit transistors (“*between the first active region and the second active region*”) compared to those in the memory array (“*between the third active region and the fourth active region*”), rendering claim 2 obvious. (TSMC-1003, ¶¶269-272.)

D. Claims 3 and 11

In the polysilicon gate of the memory cell NMOS transistor, “the impurity of an N type **is implanted like** the [NMOS] transistor of a peripheral circuit.” (TSMC-1007, ¶111.) Therefore, as discussed in §VII.B.3, the impurity concentration relationship disclosed in Igarashi’s second embodiment is:

Igarashi’s Second Embodiment
$LP(IR, AR) > SP(IR, AR)$
$LN(IR, AR) \approx SN(IR, AR)$



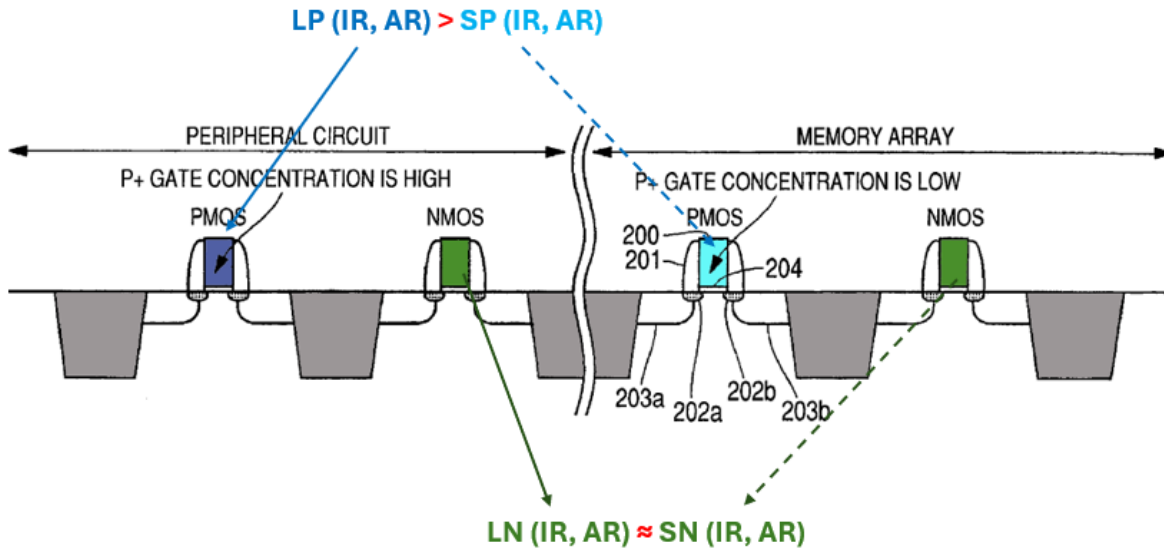
Igarashi, Figure 10

Accordingly, the portion of the logic NMOS gate electrode over the active region, **LN (AR)** (“at least a portion of the first silicon film of the second conductivity type”) has a substantially equal n-type impurity concentration (“second-conductivity-type impurity concentration”) to the portion of the SRAM NMOS gate electrode over the active region, **LN (AR)**. That is, **LN (IR, AR) $\approx$ SN (AR)**, satisfying both claims 3 and 11 under Scenario B-1. (TSMC-1003, ¶¶274-276.)

E. Claim 4

As discussed in §VII.B.3, Igarashi’s impurity concentration relationship is summarized below:

Igarashi's Second Embodiment
LP (IR, AR) > SP (IR, AR)
LN (IR, AR) ≈ SN (IR, AR)



Igarashi, Figure 10

Accordingly, the portion of the gate electrode over the first active region, **LP(AR)**, (“the first silicon film of the first conductivity type located on the first active region”) has a higher p-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of electrode over the third active region, **SP(AR)**, (“the second silicon film of the first conductivity type located on the third active region”). That is, **LP(AR) > SP(AR)**, satisfying claim 4 under Scenario B-1.

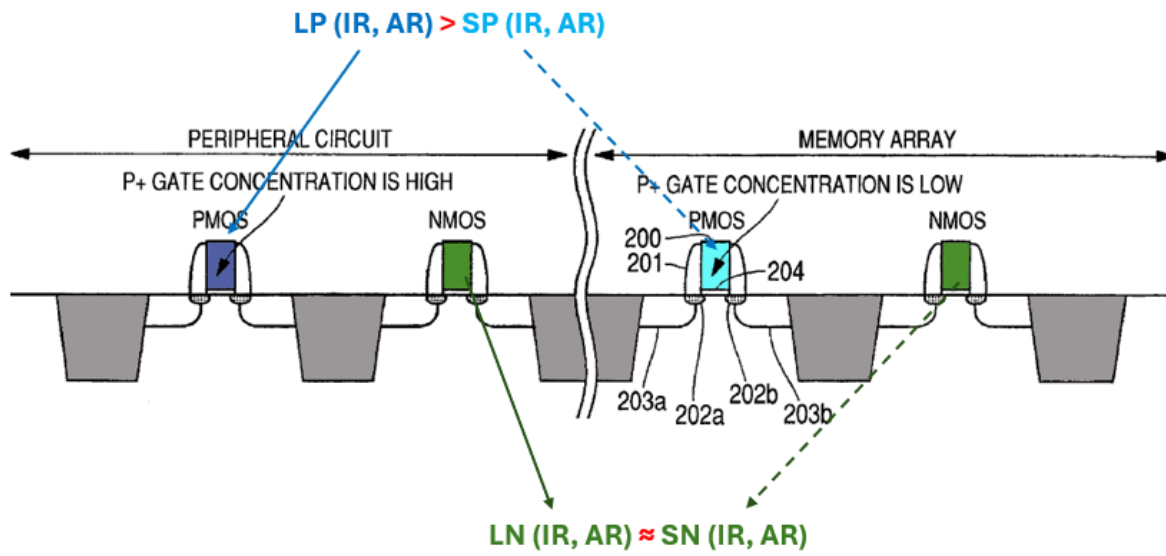
F. Claim 8

As discussed in §VII.B.3, the entire film of the logic PMOS transistor gate is implanted simultaneously and therefore the portion over the active region has substantially the same impurity concentration as the portion over the isolation region ($LP(IR) \approx LP(AR)$). (TSMC-1003, ¶280.) And both are higher than the portion over the SRAM active region. (§VII.B.3(1G).) Igarashi discloses claim 8 under Scenario B-1.

G. Claim 9

As discussed in §VII.B.3, the impurity concentration relationship disclosed in Igarashi's second embodiment is:

Igarashi's Second Embodiment
$LP(IR, AR) > SP(IR, AR)$
$LN(IR, AR) \approx SN(IR, AR)$



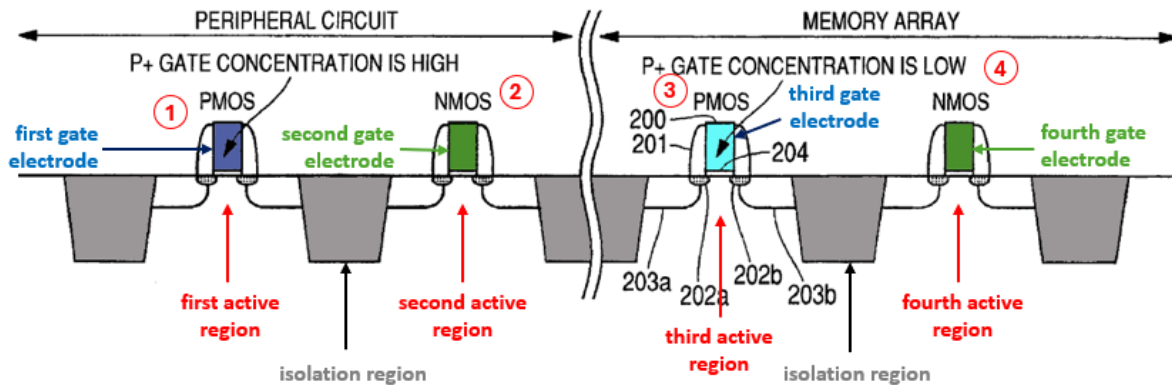
Igarashi, Figure 10

Accordingly, the portion of logic gate electrode over the isolation region, $LP(IR)$, (“the first silicon film of the first conductivity type located on the isolation region”) has a higher p-type impurity concentration (“first-conductivity-type impurity concentration”) than the portion of SRAM gate electrode over the active region, $SP(AR)$, (“the second silicon film of the first conductivity type located on the third active region”). That is, $LP(IR) > SP(AR)$, satisfying claim 9 under Scenario B-1.

H. Claims 13-14

Igarashi’s second embodiment device discloses PMOS and NMOS transistors forming the peripheral (logic) circuit and PMOS and NMOS transistors

forming the SRAM memory cell. (TSMC-1007, ¶96, Figure 10 (below).) Igarashi therefore discloses claim 13 under Scenario B-1.



Igarashi, Figure 10

Each of the first and second gate electrodes is part of the peripheral circuit, including, e.g., row decoder 2, word line driver circuit 3, column selection circuitry 4, write circuit 5, read-out circuit 6, control circuit 7, and power supply circuit 8, which “control[s] the interior action of a memory array,” i.e., “a logic circuit.” (TSMC-1007, ¶96; TSMC-1003, ¶287.) Each of the third and fourth gate electrodes is part of the SRAM memory cell. (TSMC-1007, ¶96.) Thus, Igarashi discloses or renders claim 14 obvious under Scenario B-1. (TSMC-1003, ¶287.)

I. Claims 6 and 12

1. Claim 6

Igarashi renders obvious “a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-

type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.” (TSMC-1003, ¶¶288-296.)

As discussed in §VII.B.3, the NMOS gate electrodes in the memory array and logic circuit are doped through **separate and distinct sequential steps**. (TSMC-1003, ¶289.) First, “regions other than an N channel MOS transistor of a memory array” are masked. (TSMC-1007, ¶105.) Arsenic (As) of about $0.5\text{E}+15 \sim 1\text{E}+15$ atoms/cm² is implanted “to the first impurity layer that forms the source/drain region” of the memory NMOS transistor and arsenic (As) of about $0.5\text{E}+15 \sim 1\text{E}+15$ atoms/cm² is implanted “also to the polysilicon gate which forms the gate region” of the NMOS memory transistor. (TSMC-1007, ¶105.)

Subsequently, “regions other than an N channel MOS transistor of a peripheral circuit” are masked. (TSMC-1007, ¶106.) Arsenic (As) of about $0.5\text{E}+15 \sim 1\text{E}+15$ atoms/cm² is implanted “to the first impurity layer that forms the source/drain region” of the logic NMOS transistor and arsenic (As) of about $0.5\text{E}+15 \sim 1\text{E}+15$ atoms/cm² is implanted “to the polysilicon gate which forms the gate region” of the logic NMOS transistor. (TSMC-1007, ¶106.)

Because these implantation steps are **independent**, i.e., decoupled, and each uses dopant **dose ranges** rather than fixed values, a POSITA would have understood and been motivated to adjust dopant levels in the gate electrodes

independently to obtain desired impurity concentrations. (TSMC-1003, ¶289.) As such, a POSITA would have understood that **three** impurity concentrations alternatives are achievable through Igarashi's process:

- i. Peripheral (logic) NMOS gate has a higher impurity concentration than the memory NMOS gate (**LN (IR, AR) > SN (IR, AR)**);
- ii. Both polysilicon gates have substantially equal impurity concentrations (**LN (IR, AR) ≈ SN (IR, AR)**); or
- iii. Peripheral (logic) NMOS gate has a lower impurity concentration than the memory array NMOS gate (**LN (IR, AR) < SN (IR, AR)**).

(TSMC-1003, ¶291.) A POSITA would have had a reasonable expectation of success in pursuing each alternative because the options are well-defined, predictable and technically straightforward for a POSITA to implement using routine process optimization. (TSMC-1003, ¶¶293-294.) Because of the predictable nature of the electrical and performance characteristics resulting from varying impurity concentrations, trying each alternative is "the product not of innovation but of ordinary skill and common sense." *See Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2004), quoting *KSR*, 550 U.S. at 421.

Accordingly, Igarashi renders claim 6 obvious under alternative (3): **LN (IR, AR) < SN (IR, AR)** under Scenario B-1.

2. Claim 12

As discussed in §VII.E, Igarashi's second embodiment discloses an impurity concentration relationship of $LP(AR) > SP(AR)$, satisfying limitation [12A].

As discussed above, it would have been obvious to a POSITA to try the three impurity concentration relationship alternatives for the logic and SRAM NMOS transistors, including alternative (1) $LN(IR, AR) > SN(IR, AR)$.

Accordingly, Igarashi renders obvious limitation [12B]: “*a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region*” under Scenario B-1. (TSMC-1003, ¶¶297-301.)

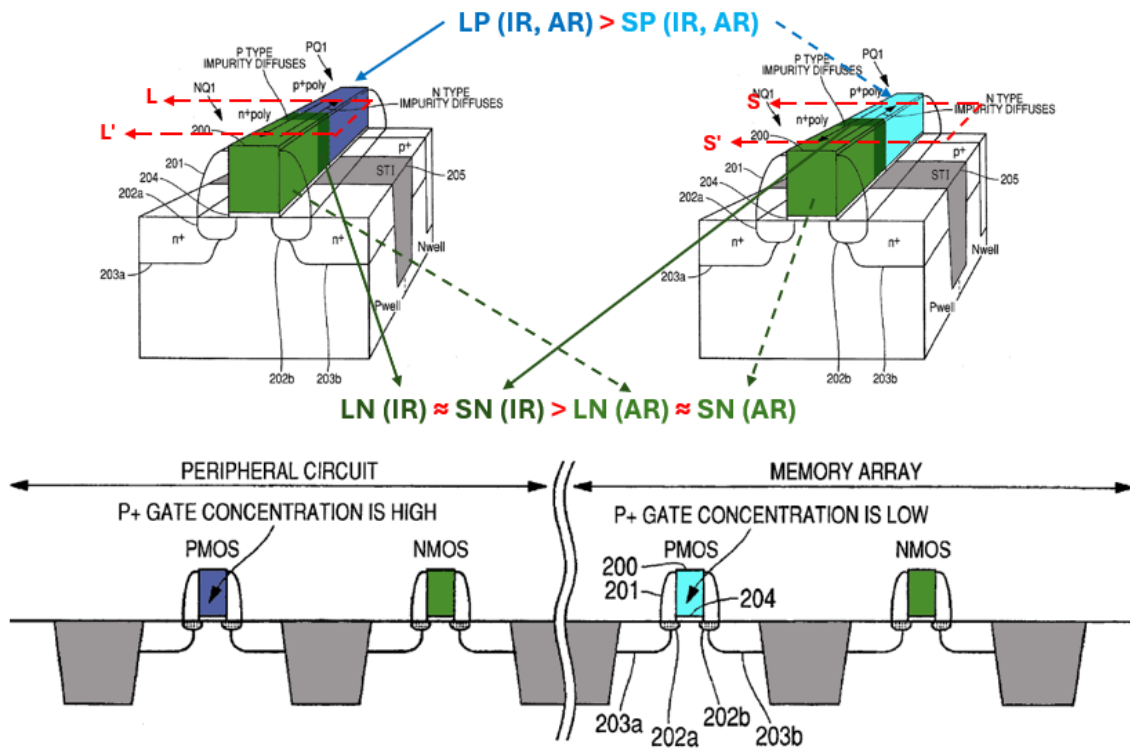
VIII. GROUND 4: Igarashi-Sumi Combination Renders Claims 1-14 Obvious.

As discussed in §VII, Igarashi renders claim 1 obvious under Scenario B-1. Should an argument be made that Igarashi does not disclose limitations [1A] and [1F] because it does not expressly illustrate a dual-gate electrode in the logic section inverter, it would have been obvious to combine Igarashi with Sumi's teaching related to dual-gate electrodes, discussed in §VIII.A below. (TSMC-1003, ¶¶302-303.)

Igarashi does not explicitly disclose the limitations of claims 5 and 7. Sumi provides these teachings, as discussed in §VI.A.2.

A. Combination Overview

A POSITA would have been motivated to combine Sumi's teaching regarding use of a high-concentration region in a dual-gate electrode structure into Igarashi's dual-gate electrode structure. (TSMC-1003, ¶304.) Specifically, a POSITA would have been motivated to form a high-concentration impurity region (e.g., region 21D) at the pn junction in Igarashi's dual-gate electrode structure depicted in Figure 9 for both the peripheral (logic) circuit and SRAM circuits—i.e., over a portion of the STI region, as taught by Sumi and illustrated in Figure 9 below, for both Igarashi's peripheral and SRAM inverters.



Igarashi, Modified Figure 9 (left and right-top), Figure 10 (bottom)

The impurity concentration relationship for Igarashi's second embodiment combined with Sumi, illustrated above, is:

Igarashi's Second Embodiment + Sumi
$LP (IR, AR) > SP (IR, AR)$
$LN (IR) \approx SN (IR) > LN (AR) \approx SN (AR)$

Igarashi and Sumi are in the same field of endeavor as the '373 patent, semiconductor devices. (TSMC-1001, 3:42-46; Igarashi, ¶¶14-17, Sumi, ¶¶11, 13.)

A POSITA would have been motivated to make the above combination because both Igarashi and Sumi motivate the combination. Igarashi observes

SRAM transistors are more aggressively scaled than other transistors on a chip to increase the density of SRAM regions. (TSMC-1007, ¶¶4–7.) Igarashi further notes the “formation of [a] gate depletion [region due] to gate mutual [dopant] diffusion” leads to undesirable threshold voltage variations in CMOS transistor pairs used in SRAM. (TSMC-1007, ¶¶89–90.) Specifically, at the pn-junction of a dual-gate electrode in an SRAM transistor pair, p-type dopants diffuse into the n⁺ polysilicon gate electrode, while n-type dopants diffuse into the p⁺ polysilicon gate electrode; resulting in undesirable threshold voltage variations. (TSMC-1003, ¶307.)

To address the variation in transistor characteristics arising from the mutual diffusion of dopants, particularly between the gate electrodes of the driver and load transistors in an SRAM memory cell, Igarashi adjusts the p-type impurity concentration in the polysilicon gate of the PMOS transistor of the SRAM to be lower than the corresponding PMOS transistor of the peripheral circuit. (TSMC-1007, ¶¶92, 97.) Although Igarashi’s approach mitigates mutual dopant diffusion, it does not fully eliminate it. (TSMC-1003, 308.) Accordingly, as discussed in §VI.A.3 for Tamaki, a POSITA would be motivated to look beyond Igarashi’s teachings for further improvements and to facilitate further scaling of the SRAM region in Igarashi’s design. (TSMC-1003, ¶308.)

For the reasons discussed in §VI.A.3, Sumi also expressly motivates the combination with Igarashi. The combination reduces dopant interdiffusion across

the dual-gate electrode and, by extension, minimizes variations in transistor characteristics, including threshold voltage variation. (TSMC-1003, ¶309.)

Finally, the combination is nothing more than the application of a known technique (Sumi's fabrication of dual-gate electrode devices) to a known device (Igarashi's SRAM section) ready for improvement for the reasons discussed above. (TSMC-1003, ¶310.) *KSR Int'l. Co. v. Teleflex Inc.*, 550 U.S. 398, 416-417.

A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable. (TSMC-1003, ¶311.) The Igarashi-Sumi combination would merely implement standard fabrication techniques to incorporate Sumi's high concentration phosphorous-doped region in Igarashi's dual-gate electrode structure. (TSMC-1003, ¶311.) Implementing Sumi's teachings into Igarashi's dual-gate electrode structure would have been well within the skill set of a POSITA because the combination involves standard fabrication techniques and concepts well understood before the earliest priority date of the '373 patent. (TSMC-1003, ¶311.)

A POSITA would have understood the process steps for forming Sumi's high concentration phosphorous-doped region are compatible with Igarashi's process steps, for at least two reasons. (TSMC-1003, ¶312.) First, forming the high concentration region is an independent step requiring its own dedicated photolithography mask for the phosphorous implant step at the pn junction over a

portion of the isolation structure, as discussed above in connection to Figure 6(2). (TSMC-1009, ¶¶72-73.) Second, Igarashi does not disclose any other masks or process steps specifically targeting the pn junction of the p-type and n-type electrodes over the isolation structure, and therefore introducing Sumi's steps for forming the high concentration phosphorous-doped region would not interfere with other process steps. (TSMC-1003, ¶312.) For example, in connection with Figure 11E, Igarashi discloses forming a silicide wall of an oxide film on the sidewall of Igarashi's polysilicon gates (TSMC-1007, ¶107), following with steps for implanting the impurities in the substrate to form the source and drains of the P- and N-MOS transistors. (TSMC-1007, ¶¶108-110.) A POSITA would have been motivated to introduce Sumi's steps for forming the high concentration phosphorous-doped region before the formation of the source and drain regions of the Igarashi's MOS transistors, because in Sumi's process, the high concentration phosphorous-doped region is formed prior to the source and drain formation (TSMC-1009, ¶¶73-75), which also aligns with in Igarashi's gate electrode dopant flow. (TSMC-1003, ¶¶313.)

B. Independent Claim 1

1. Limitations [1A] and [1F]

Should an argument be made that Igarashi does not disclose limitations [1A] and [1F], it would have been obvious to combine Igarashi with Sumi's teaching of

a logic circuit with a dual-gate electrode, where the gate electrodes are connected to each other on an isolation region.

A POSITA would have been motivated to make this combination because, as discussed in §VII.B.2.b, Igarashi suggests the use of a dual-gate structure for its peripheral circuits and the '373 patent admits conventional prior art devices used dual-gate electrodes in the logic section. (TSMC-1001, 1:48-52, 2:43-46, 7:33-43, Figures 15A-15B, 16A.) Moreover, a POSITA would have recognized in standard CMOS/CMIS layout practices, an isolation region is used to electrically isolate adjacent diffusion regions. However, when a continuous gate electrode spans across two separate active regions physically separated by an isolation structure, the gate electrode necessarily passes over the intervening isolation region. (TSMC-1003, ¶316.) This results in a shared gate electrode that controls two distinct channel regions, one in each active area, thereby forming two transistors that are connected on the isolation region. (TSMC-1003, ¶316.) The connection occurs via the continuous gate, not through diffusion or direct substrate contact, while the isolation structure maintains electrical separation between the underlying source/drain regions. This type of configuration is common in logic circuits and SRAM cells, where compact layouts and shared control of complementary transistors (e.g., PMOS and NMOS) are often required. Accordingly, when two active regions are separated by an isolation structure, a gate electrode spans

laterally across both active areas and the intervening isolation structure, and a circuit calls for shared gate control, like an inverter, then the two gate electrodes would be connected on the isolation structure. These configurations are well-understood by circuit designers and layout engineers and are widely used in standard cell libraries and SRAM or logic blocks. (TSMC-1003, ¶316.)

Accordingly, the Igarashi-Sumi combination discloses limitations [1A] and [1F]. (TSMC-1003, ¶¶315-317.)

2. Limitations [1B]-[1E]

The combination discloses limitations [1B]-[1E] for the same reasons discussed in §VII.B.2.

3. Limitation [1G]

As discussed in §VII.B.2, Igarashi discloses [1A]-[1F] under Scenarios A-1, A-2, B-1, and B-2. And as discussed in §VII.B.3, the impurity concentration relationship for Igarashi's second embodiment combined with Sumi is:

Igarashi's Second Embodiment + Sumi
LP (IR, AR) > SP (IR, AR)
LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)

The combination of Igarashi and Sumi therefore also discloses [1G] under Scenarios A-1 and A-2 as well as B-1 (§VII.B.3):

	Claimed Impurity Concentration Relationship	Igarashi + Sumi Impurity Concentration Relationship
A-1	LN(IR or AR) > SN(AR)	LN (IR) > SN (AR)
A-2	SN(IR or AR) > LN(AR)	SN (IR) > LN (AR)
B-1	LP(IR or AR) > SP(AR)	LP(IR, AR) > SP(IR, AR)
B-2	SP(IR or AR) > LP(AR)	

C. Claims 2-4, 8, 11-14

The Igarashi-Sumi device renders obvious claims 2-4, 8, 11-14 under Scenario B-1, for the reasons discussed in §§VII.C, D, E, F, H-I.

D. Claims 5 and 7

Claim 5 differs from claim 7 in that it requires that the impurity concentration of the “*first gate electrode*” be lower at a portion located at the first active region compared to a portion located at the isolation region, while claim 7 requires that the impurity concentration of the “*second gate electrode*” is lower at a portion located at the second active region compared to a portion located at the isolation region.

As discussed in §VIII.B.3, the impurity concentration relationship for Igarashi’s second embodiment combined with Sumi is:

Igarashi's Second Embodiment + Sumi
LP (IR, AR) > SP (IR, AR)
LN (IR) $\approx$ SN (IR) > LN (AR) $\approx$ SN (AR)

The Igarashi-Sumi combination discloses claim 5 under Scenario A-1 and Scenario A-2: “a portion of the first silicon film of the first conductivity type located on the first active region [LN(AR) or SN(AR)] has a first-conductivity-type impurity concentration [n-type] lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region [LN(IR) or SN(IR)]” (that is: “LN(AR) < LN (IR)” (Scenario A-1) or “SN(AR) < SN(IR)” (Scenario A-2)). (TSMC-1003, ¶323-325.)

The Igarashi-Sumi combination discloses claim 7 under Scenario B-1: “a portion of the first silicon film of the second conductivity type located on the second active region [LN(AR)] has a second-conductivity-type impurity concentration [n-type] lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region [LN(IR)]” (that is: “LN(AR) < LN(IR)” (Scenario B-1)). (TSMC-1003, ¶¶326-327.)

E. Claim 6

As discussed in §VIII.B.3, the impurity concentration relationship for Igarashi's second embodiment combined with Sumi is:

Igarashi's Second Embodiment + Sumi
LP (IR, AR) > SP (IR, AR)
LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)

The Igarashi-Sumi device discloses claim 6 under Scenario A-2: “a portion of the first silicon film of the second conductivity type located on the second active region [SP(AR)] has a second-conductivity-type impurity concentration [p-type] lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region [LP(AR)].” That is, “SP(AR) < LP(AR)” (Scenario A-2). (TSMC-1003, ¶329.)

F. Claim 9

In addition to the reasons discussed in §VII.G under Scenario B-1, the Igarashi-Sumi combination renders claim 9 obvious under Scenario A-1 and Scenario A-2. The impurity concentration relationship for Igarashi's second embodiment combined with Sumi is:

Igarashi's Second Embodiment + Sumi
LP (IR, AR) > SP (IR, AR)
LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)

Accordingly, the portion of logic NMOS gate electrode over the isolation region, **LN(IR) or SN(IR)**, (“the first silicon film of the first conductivity type

located on the isolation region”) has a higher n-type impurity concentration (*“first-conductivity-type impurity concentration”*) than the portion of SRAM NMOS gate electrode over the active region, **SN(AR) or LN(AR)**, (*“the second silicon film of the first conductivity type located on the third active region”*). That is, **LN(IR) > SN(AR)** (Scenario A-1) and **SN(IR) > LN(AR)** (Scenario A-2). (TSMC-1003, ¶¶331-332.)

G. Claim 10

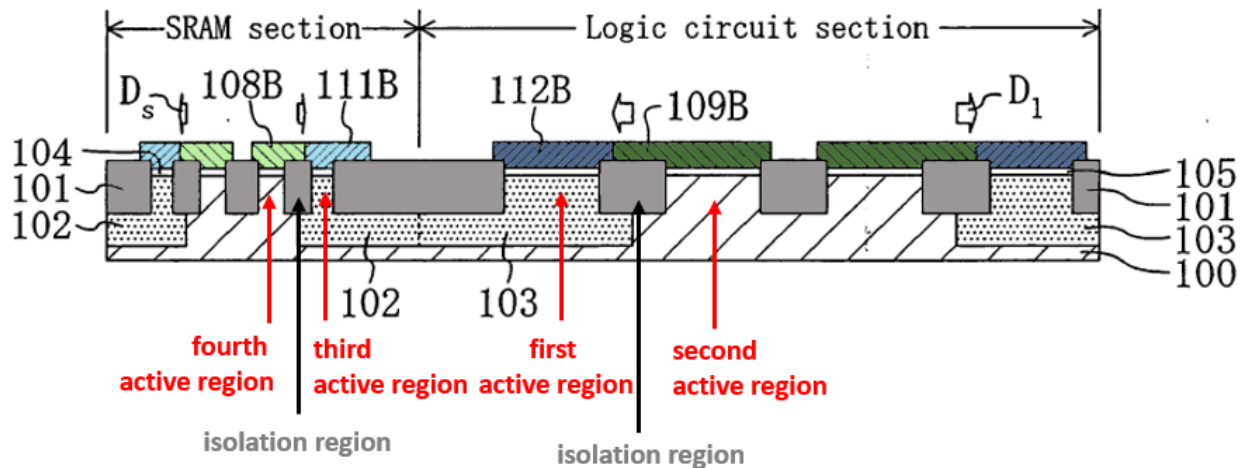
As discussed in §VIII.B.3, the impurity concentration relationship disclosed in Igarashi’s second embodiment is:

Igarashi’s Second Embodiment + Sumi
LP (IR, AR) > SP (IR, AR)
LN (IR) ≈ SN (IR) > LN (AR) ≈ SN (AR)

Thus, Igarashi-Sumi combination discloses *“a portion of the first silicon film of the first conductivity type located on the first active region [LN(AR) or SN(AR)] has a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region [SN(AR) or LN(AR)]”* under Scenarios A-1 and A-2. That is, **LN(AR) > SN(AR)** (Scenario A-1) and **SN(IR) > LN(AR)** (Scenario A-2). (TSMC-1003, ¶¶335-336.)

IX. GROUNDS 5-6: Combination of Tamaki with Igarashi (Ground 5) or with Igarashi-Sumi (Ground 6) Renders Claim 2 Obvious.

Should an argument be made that Igarashi does not disclose or suggest claim 2, Tamaki provides this teaching as discussed in §V.B.2 and illustrated below. (See, e.g., ¶¶83, 116, Figure 3B (below), Figure 5B.)



Tamaki, Figure 3B

Thus, the Igarashi-Tamaki (Ground 5) combination and Igarashi-Sumi-Tamaki combination (Ground 6) each discloses “an isolation width between the first active region and the second active region is larger than [an isolation width] between the third active region and the fourth active region” [2].

Igarashi, Sumi, and Tamaki are in same field of endeavor as the '373 patent, semiconductor devices. (Compare TSMC-1001, 3:42-46, with Igarashi, ¶¶14-17 and Tamaki, ¶¶3, 147.) A POSITA would have been motivated to combine Tamaki's teachings of an isolation region having a larger width between active

regions in a logic circuit compared to the width between active regions in an SRAM circuit with Igarashi's or Igarashi-Sumi dual-gate electrode semiconductor devices in the peripheral circuit area and the memory array area. (TSMC-1003, ¶339.)

Tamaki motivates the combination, teaching transistor layout techniques directly addressing the need to control variability, leakage currents, and performance across different functional blocks in an integrated circuit. (TSMC-1003, ¶341.) Specifically, Tamaki discloses forming gate electrodes with different widths and layouts depending on the performance and leakage needs of specific circuit regions, such as logic and memory. (*See, e.g.*, Tamaki, ¶¶82-83, 109-112, 141-144.) Tamaki explains that gate width and layout are adjusted to manage threshold voltage variation and process-induced fluctuations, which become increasingly problematic as device dimensions shrink. (*See, e.g.*, Tamaki, ¶147.) Igarashi, in turn, describes a semiconductor device structure including dual-gate electrodes formed on isolated active regions, with impurity concentrations tailored to provide different threshold voltages, and emphasizes the need to reduce memory cell sizes and mitigate process variation in high-density SRAM arrays. (*See, e.g.*, Igarashi, ¶¶4-5.)

U.S. Patent No. 8,355,269 to Zampaglione (“Zampaglione”; TSMC-1016) confirms SRAM bit cells are typically formed using **tighter design rules** than

those applied to general-purpose logic transistors on the same chip. Zampaglione discloses that SRAM layouts use reduced feature sizes and spacings compared to the rest of the integrated circuit, which includes logic circuitry. (TSMC-1016, 3:58-64.) A POSITA would have understood this difference in scaling implies the **isolation width in SRAM regions**—which must support high-density layout—would also be smaller than the isolation widths used in logic circuitry, such as the row decoder, write circuit, readout circuitry, column selection circuitry, main control circuit, and word line drive circuit as depicted in Igarashi's Figure 1. (TSMC-1003, ¶342.)

Moreover, a POSITA would have understood that to implement Igarashi's dual-gate structure where both SRAM and logic circuits coexist, it would be necessary to adopt layout strategies accommodating different electrical and spatial requirements of these circuits. (TSMC-1003, ¶343.) Specifically, SRAM circuits prioritize compactness and low leakage, while logic circuits often require stronger isolation to ensure robust signal integrity and prevent noise coupling. (TSMC-1003, ¶343.) This dichotomy in design priorities would naturally lead a POSITA to consider modifying the isolation widths between active regions depending on their function. (TSMC-1003, ¶343.)

Tamaki reinforces this design perspective, teaching that varying the layout and physical dimensions of transistors, such as gate width and spacing, helps

optimize performance across different circuit types. (*See, e.g.,* Tamaki, ¶32.) Thus, applying Tamaki's teaching to Igarashi's structure, a POSITA would have found it obvious to increase the isolation width between the first and second active regions (e.g., assigned to logic circuits) while reducing it between the third and fourth active regions (e.g., assigned to SRAM circuits). (TSMC-1003, ¶344.)

Moreover, the combination involves only routine design considerations within the capabilities of a POSITA. (TSMC-1003, ¶345.) It would have been obvious to a POSITA at the time to adopt well-known layout differentiation techniques, such as those taught by Tamaki, to further optimize Igarashi's structure for embedded memory applications, particularly where isolation width impacts both device performance and area efficiency. (TSMC-1003, ¶345.)

Finally, the combination is nothing more than the application of a known technique (Tamaki's fabrication of dual-gate electrode devices) to a known device (Igarashi's logic circuit and SRAM section) ready for improvement for the reasons discussed above. (TSMC-1003, ¶346.)

A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable. (TSMC-1003, ¶347.) The Igarashi-Tamaki combination would merely implement standard fabrication techniques to fabricate Tamaki's semiconductor devices in Igarashi's integrated system. Implementing Tamaki's teachings into Igarashi's system would have been

well within the skill set of a POSITA because the combination involves standard fabrication techniques and concepts well understood before the earliest priority date of the '373 patent. (TSMC-1003, ¶347.)

X. Mandatory Notices

A. Real Party in Interest

The Petitioner and real party in interest is Taiwan Semiconductor Manufacturing Company Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '373 patent is involved in the following ongoing litigation:

- *Advanced Integrated Circuit Process LLC, v. Taiwan Semiconductor Manufacturing Company Limited*, No. 2:25-CV-324 (E.D.T.X.)

C. Notice of Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints the following lead and backup counsel:

Lead Counsel	Back Up Counsel
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XI. Conclusion

IPR is respectfully requested.

U.S. Patent 8,884,373
IPR2025-01302

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,884,373**, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,980. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies, in accordance with 37 C.F.R. § 42.105,
that the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S.
PATENT NO. 8,884,373**, TSMC's Power of Attorney, and all supporting exhibits
were served via FedEx Next Business Day Delivery, in their entirety on the Patent
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Appendix A: Challenged Claims Listing

[1P] A semiconductor device comprising:

[1A] a first dual-gate electrode; and

[1B] a second dual-gate electrode being separated from the first dual-gate electrode, wherein

[1C] the first dual-gate electrode includes a first gate electrode located on a first active region and having a first silicon film of a first conductivity type and a second gate electrode located on a second active region and having a first silicon film of a second conductivity type,

[1D] the second dual-gate electrode includes a third gate electrode located on a third active region and having a second silicon film of the first conductivity type and a fourth gate electrode located on a fourth active region and having a second silicon film of the second conductivity type,

[1E] the first active region and the second active region are isolated from each other with an isolation region interposed therebetween,

[1F] the first gate electrode and the second gate electrode are connected to each other on the isolation region, and

[1G] at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

[2] The semiconductor device of claim 1, wherein an isolation width between the first active region and the second active region is larger than that between the third active region and the fourth active region.

[3] The semiconductor device of claim 1, wherein at least a portion of the first silicon film of the second conductivity type has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

[4] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

[5] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region.

[6] The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

[7] The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region.

[8] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region.

[9] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region.

[10] The semiconductor device of claim 1, wherein a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region.

[11] The semiconductor device of claim 1, wherein a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

[12P] The semiconductor device of claim 1, wherein

[12A] a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity

concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region, and

[12B] a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region.

[13P] The semiconductor device of claim 1, wherein

[13A] the first gate electrode is a gate electrode of a first PMIS transistor,

[13B] the second gate electrode is a gate electrode of a first NMIS transistor,

[13C] the third gate electrode is a gate electrode of a second PMIS transistor, and

[13D] the fourth gate electrode is a gate electrode of a second NMIS transistor.

[14P] The semiconductor device of claim 1, wherein

[14A] each of the first gate electrode and the second gate electrode is a gate electrode of a transistor for a logic circuit, and

[14B] each of the third gate electrode and the fourth gate electrode is a gate electrode of a transistor for an SRAM circuit.

Appendix B

Claim Language		Scenarios Covered			
		A-1	A-2	B-1	B-2
<i>first dual-gate electrode</i>	<i>first gate electrode</i>	logic NMOS	SRAM NMOS	logic PMOS	SRAM PMOS
	<i>second gate electrode</i>	logic PMOS	SRAM PMOS	logic NMOS	SRAM NMOS
<i>second dual-gate electrode</i>	<i>third gate electrode</i>	SRAM NMOS	logic NMOS	SRAM PMOS	logic PMOS
	<i>fourth gate electrode</i>	SRAM PMOS	logic PMOS	SRAM NMOS	logic NMOS

Concentration Relationships Claims

	Scenario			
	A-1	A-2	B-1	B-2
[1G]	“at least a portion of the first silicon film of the first conductivity type has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region”			
	$LN(IR, AR) > SN(AR)$	$SN(IR, AR) > LN(AR)$	$LP(IR, AR) > SP(AR)$	$SP(IR, AR) > LP(AR)$
[3]	“at least a portion of the first silicon film of the second conductivity type has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region”			
	$LN(IR, AR) > SN(AR)$ $LP(IR, AR) \approx SP(AR)$	$SN(IR, AR) > LN(AR)$ $SP(IR, AR) \approx LP(AR)$	$LP(IR, AR) > SP(AR)$ $LN(IR, AR) \approx SN(AR)$	$SP(IR, AR) > LP(AR)$ $LN(IR, AR) \approx SN(AR)$
[4]	“a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region”			
	$LN(AR) > SN(AR)$	$SN(AR) > LN(AR)$	$LP(AR) > SP(AR)$	$SP(AR) > LP(AR)$

[5]	“a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the first conductivity type located on the isolation region”			
	$\text{LN}(\text{IR}) > \text{LN}(\text{AR}) > \text{SN}(\text{AR})$	$\text{SN}(\text{IR}) > \text{SN}(\text{AR}) > \text{LN}(\text{AR})$	$\text{LP}(\text{IR}) > \text{LP}(\text{AR}) > \text{SP}(\text{AR})$	$\text{SP}(\text{IR}) > \text{SP}(\text{AR}) > \text{LP}(\text{AR})$
[6]	“a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the second silicon film of the second conductivity type located on the fourth active region”			
	$\text{LN}(\text{IR}, \text{AR}) > \text{SN}(\text{AR})$ $\text{LP}(\text{AR}) < \text{SP}(\text{AR})$	$\text{SN}(\text{IR}, \text{AR}) > \text{LN}(\text{AR})$ $\text{SP}(\text{AR}) < \text{LP}(\text{AR})$	$\text{LP}(\text{IR}, \text{AR}) > \text{SP}(\text{AR})$ $\text{LN}(\text{AR}) < \text{SN}(\text{AR})$	$\text{SP}(\text{IR}, \text{AR}) > \text{LP}(\text{AR})$ $\text{SN}(\text{AR}) < \text{LN}(\text{AR})$
[7]	“a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration lower than that of a portion of the first silicon film of the second conductivity type located on the isolation region”			
	$\text{LN}(\text{IR}, \text{AR}) > \text{SN}(\text{AR})$ $\text{LP}(\text{AR}) < \text{LP}(\text{IR})$	$\text{SN}(\text{IR}, \text{AR}) > \text{LN}(\text{AR})$ $\text{SP}(\text{AR}) < \text{SP}(\text{IR})$	$\text{LP}(\text{IR}, \text{AR}) > \text{SP}(\text{AR})$ $\text{LN}(\text{AR}) < \text{LN}(\text{IR})$	$\text{SP}(\text{IR}, \text{AR}) > \text{LP}(\text{AR})$ $\text{SN}(\text{AR}) < \text{SN}(\text{IR})$
[8]	“a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the first silicon film of the first conductivity type located on the isolation region”			
	$\text{LN}(\text{IR}) \approx \text{LN}(\text{AR}) > \text{SN}(\text{AR})$	$\text{SN}(\text{IR}) \approx \text{SN}(\text{AR}) > \text{LN}(\text{AR})$	$\text{LP}(\text{IR}) \approx \text{LP}(\text{AR}) > \text{SP}(\text{AR})$	$\text{SP}(\text{IR}) \approx \text{SP}(\text{AR}) > \text{LP}(\text{AR})$

[9]	“portion of the first silicon film of the first conductivity type located on the isolation region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region”			
	$LN(IR) > SN(AR)$	$SN(IR) > LN(AR)$	$LP(IR) > SP(AR)$	$SP(IR) > LP(AR)$
[10]	“a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the first conductivity type located on the third active region”			
	$LN(AR) > SN(AR)$	$SN(AR) > LN(AR)$	$LP(AR) > SP(AR)$	$SP(AR) > LP(AR)$
[11]	“a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration substantially equal to that of a portion of the second silicon film of the second conductivity type located on the fourth active region”			
	$LN(IR, AR) > SN(AR)$ $LP(AR) \approx SP(AR)$	$SN(IR, AR) > LN(AR)$ $SP(AR) \approx LP(AR)$	$LP(IR, AR) > SP(AR)$ $LN(AR) \approx SN(AR)$	$SP(IR, AR) > LP(AR)$ $LN(AR) \approx SN(AR)$
[12]	“a portion of the first silicon film of the first conductivity type located on the first active region has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region” [12A] “a portion of the first silicon film of the second conductivity type located on the second active region has a second-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the second conductivity type located on the fourth active region” [12B].			
	$LN(AR) > SN(AR)$ $LP(AR) > SP(AR)$	$SN(AR) > LN(AR)$ $SP(AR) > LP(AR)$	$LP(AR) > SP(AR)$ $LN(AR) > SN(AR)$	$SP(AR) > LP(AR)$ $SN(AR) > LN(AR)$

