

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

IPR2025-01211

U.S. Patent No. 7,439,623

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,439,623**

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,439,623
1002	File History of U.S. Patent No. 7,439,623 (“the ’623 File History”)
1003	Declaration of Dr. Reinhold Dauskardt
1004	U.S. Patent Publication No. 2003/0116852 to Watanabe et al. (“Watanabe”)
1005	U.S. Patent Publication No. 2004/0113238 to Hasunuma et al. (“Hasunuma”)
1006	Reserved
1007	U.S. Patent No. 6,717,267 to Kunikiyo (“Kunikiyo”)
1008	U.S. Patent No. 5,250,465 to Iizuka et al. (“Iizuka”)
1009	U.S. Patent Publication No. 2004/0173905 to Kamoshima et al. (“Kamoshima”)
1010	JP2002299437 (“Fukazawa”) and Certified Translation of Fukazawa with Certification of Translation
1011	U.S. Patent No. 7,042,099 to Kurashima (“Kurashima”)
1012	P. Andricacos, “Copper On-Chip Interconnections,” <i>Interface, The Electrochemical Society</i> , pp. 32-37, 1999
1013	U.S. Patent No. 5,885,857 to Yamaha et al. (“Yamaha”)
1014	U.S. Patent Publication No. 2003/0005399 to Igarashi et al. (“Igarashi”)

Exhibit No.	Description
1015	U.S. Patent No. 6,717,268 to Hau-Riege (“Hau-Riege”)
1016	U.S. Patent No. 6,468,894 to Yang (“Yang”)
1017	U.S. Patent No. 6,022,808 to Nogami (“Nogami”)
1018	AICP’S P.R. 3-1 Disclosure of Asserted Claims and Infringement Contentions and P.R. 3-2 Document Production Against TSMC (cover document only)
1019	Kaanta et al., “Dual Damascene: A ULSI Wiring Technology,” <i>VMIC Conference</i> , IEEE, Jun. 11-12, 1991, pp. 144-152
1020	U.S. Patent No. 5,032,890 to Ushiku (“Ushiku”)
1021	Reserved
1022	Reserved
1023	Reserved
1024	U.S. Patent No. 6,156,660 to Liu et al. (“Liu”)
1025	U.S. Patent No. 5,798,298 to Yang (“Yang 2”)
1026	T. I. Bao <i>et al.</i> , “90 nm Generation Cu/CVD Low-k ($k < 2.5$) Interconnect Technology,” <i>Digest. International Electron Devices Meeting</i> , San Francisco, CA, USA, 2002, pp. 583-586
1027	A. Loke, “Process Integration Issues of Low-Permittivity Dielectrics With Copper for High-Performance Interconnects,” Dissertation, Stanford University (1999)
1028	K.N. Tu, “Recent advances on electromigration in very-large-scale-integration of interconnects,” <i>Applied Physics Review</i> –

Exhibit No.	Description
	<i>Focused Review, Journal of Applied Physics</i> , Vol. 94, No. 9 (November 1, 2003), pp. 5451-5473
1029	T. C. Huang, <i>et al.</i> , “Numerical Modeling and Characterization of the Stress Migration Behaviour Upon Various 90 nanometer Cu/Low k Interconnects,” <i>Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695)</i> , Burlingame, CA, USA, 2003 (added to IEEE Xplore 8-11-2003), pp. 207-209
1030	JPH10214893 to Fujii (“Fujii”) and Certified Translation of Fujii with Certification of Translation
1031	Reserved
1032	JP2000012688 to Nasu (“Nasu”) and Certified Translation of Nasu with Certification of Translation
1033	U.S. Patent Publication No. 2001/0030365 to Otsuka et al. (“Otsuka”)
1034	Wolf, Stanley, <i>Silicon Processing for the VLSI Era: Deep-Submicron Process Technology</i> , Lattice Press, 2002 (excerpted) (“Wolf”)
1035	Reserved
1036	Ogawa, E.T., <i>et al.</i> , “Stress-Induced Voiding Under Vias Connected To Wide Cu Metal Leads,” IEEE 02CH37320, <i>40th Annual International Reliability Physics Symposium</i> , Dallas, Texas, 2002, pp. 312-21
1037	von Glasow, A., <i>et al.</i> , “Geometrical Aspects of Stress-Induced Voiding in Copper Interconnects,” <i>Proceedings of the Advanced Metallization Conference 2002 (AMC 2002)</i> , San Diego, CA, October 1-3, 2002, Tokyo, Japan, October 29-30, 2002, Materials Research Society, pp. 161-67
1038	U.S. Patent No. 6,215,189 to Toyoda et al. (“Toyoda”)

Petition for *Inter Partes* Review
Patent No. 7,439,623

Exhibit No.	Description
1039	U.S. Patent No. 6,238,850 to Bula et al. (“Bula”)

LIST OF CHALLENGED CLAIMS

Claim Element	Claim Language
[1.pre] ¹	A semiconductor device comprising:
[1.a]	a semiconductor substrate;
[1.b]	a first interconnect formed on the semiconductor substrate;
[1.c]	a first insulating film formed on the first interconnect;
[1.d]	a second interconnect formed on the first insulating film;
[1.e]	a via formed through the first insulating film and connecting between the first and second interconnects; and
[1.f]	a dummy via connected to the second interconnect,
[1.g]	wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough;
[1.h]	the second interconnect and the via form a dual damascene structure, and
[1.i]	the second interconnect and the dummy via form a dual damascene structure.
[2.a]	The semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,

¹ Claims 1, 2, and 45 are not challenged in this petition, but are listed here because various challenged claims depend therefrom.

[2.b]	wherein the first interconnect is formed on the second insulating film, and
[2.c]	the dummy via is connected to a first dummy interconnect formed on the second insulating film.
[5.a]	The semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view, and
[5.b]	a diameter of the dummy via is substantially equal to a width of the first dummy interconnect.
[6.a]	The semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square, and
[6.b]	a side of the dummy via is substantially equal to a width of the first dummy interconnect.
[10.a]	The semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square, and
[10.b]	a side of the dummy via is smaller than a width of the first dummy interconnect.
19	The semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square.

20	The semiconductor device of claim 19, wherein a length of a side of the via and a length of a side of the dummy via are substantially equal to each other.
[23.a]	The semiconductor device of claim 1, wherein the via is substantially circular in a plan view, and
[23.b]	a diameter of the via is substantially equal to a width of the first interconnect.
[24.a]	The semiconductor device of claim 1, wherein a planar shape of the via is substantially a square, and
[24.b]	a side of the via is substantially equal to a width of the first interconnect.
27	The semiconductor device of claim 1, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width.
[29.a]	The semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view, and
[29.b]	a diameter of the dummy via is smaller than a diameter of the via.
[30.a]	The semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square, and

[30.b]	a side of the dummy via is smaller than a side of the via.
[31.a]	The semiconductor device of claim 1, wherein the dummy via is substantially rectangular in a plan view, and
[31.b]	a longer side of the dummy via in a plan view and a shorter side of the second interconnect are provided along a same direction.
33	The semiconductor device of claim 1, wherein the dummy via is connected to the upper surface of the second interconnect.
34	The semiconductor device of claim 33, wherein the dummy via is formed in a third insulating film formed on the second interconnect.
35	The semiconductor device of claim 34, wherein the third insulating film has a multilayer structure including a SiN film and a SiO ₂ film.
36	The semiconductor device of claim 33, wherein the dummy via includes a second barrier film and a second conductive film.
37	The semiconductor device of claim 36, wherein the second conductive film includes copper.

38	The semiconductor device of claim 33, wherein a second dummy interconnect is provided on the dummy via so as to come in contact with a top of the dummy via.
41	The semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film.
43	The semiconductor device of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via
[44.a]	The semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,
[44.b]	wherein the first interconnect is formed on the second insulating film, and
[44.c]	a bottom of the dummy via is located in the second insulating film.
[45.a]	The semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and
[45.b]	the via is connected to the second interconnect portion.

[48.a]	The semiconductor device of claim 45, wherein the dummy via is substantially rectangular in a plan view, and
[48.b]	a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction.

I. RELIEF REQUESTED

Applying the following grounds, Petitioner petitions for *Inter Partes* Review (“IPR”) of U.S. Patent No. 7,439,623 (“the ’623 patent”) and cancellation of claims 5-6, 10, 19-20, 23-24, 27, 29-31, 33-38, 41, 43-44, and 48:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	10, 19-20, 24, 27	102	Watanabe
1B	27	103	Watanabe
2	23	103	Watanabe + Iizuka
3	5	103	Watanabe + Iizuka + Kurashima
4	6	103	Watanabe + Kurashima
5	29-30	103	Watanabe + Nasu
6	31	103	Watanabe + Fujii
7	48	103	Watanabe + Kamoshima + Fukazawa
8	23, 27, 41, 43-44	102	Hasunuma
9	5	103	Hasunuma + Kurashima
10	6	103	Hasunuma + Kurashima + Iizuka
11	19-20	103	Hasunuma + Watanabe

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
12	24	103	Hasunuma + Iizuka
13	29-30	103	Hasunuma + Nasu
14	33-38	103	Hasunuma + Kamoshima

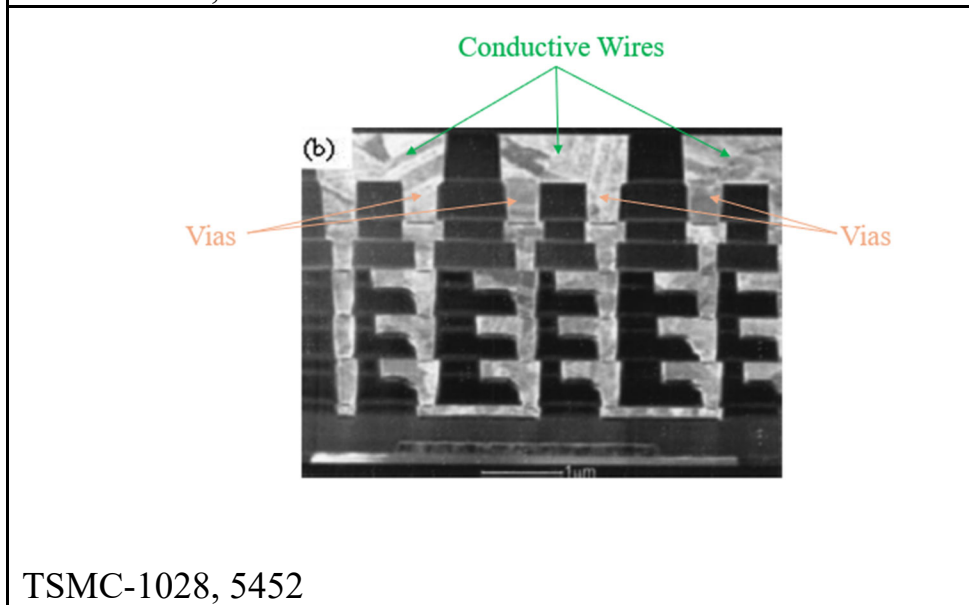
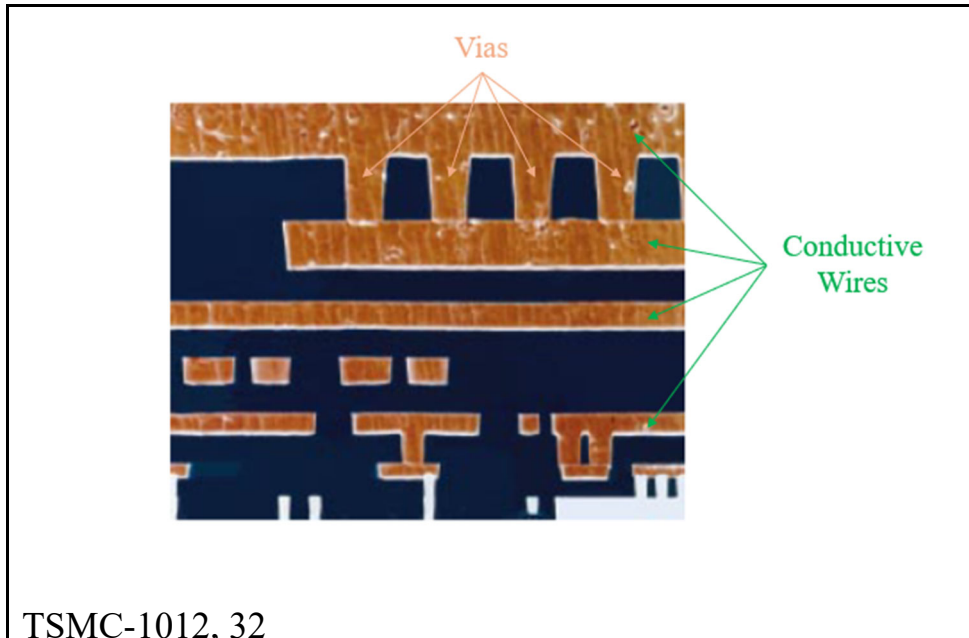
Independent claim 1 and dependent claims 2 and 45 are formally challenged in IPR2025-01212. This petition addresses further dependent claims that merely add conventional features that were well-known prior to the '623 patent. This petition is supported by the declaration of Dr. Reinhold Dauskardt, an expert in the field of interconnect technology. TSMC-1003, ¶¶1-39.

II. STATE OF THE ART

The '623 patent describes the use of dummy structures to reduce stress-induced void formation in interconnect structures. Such dummy structures, for the same purposes, were already well-known. TSMC-1003, ¶¶40-46.

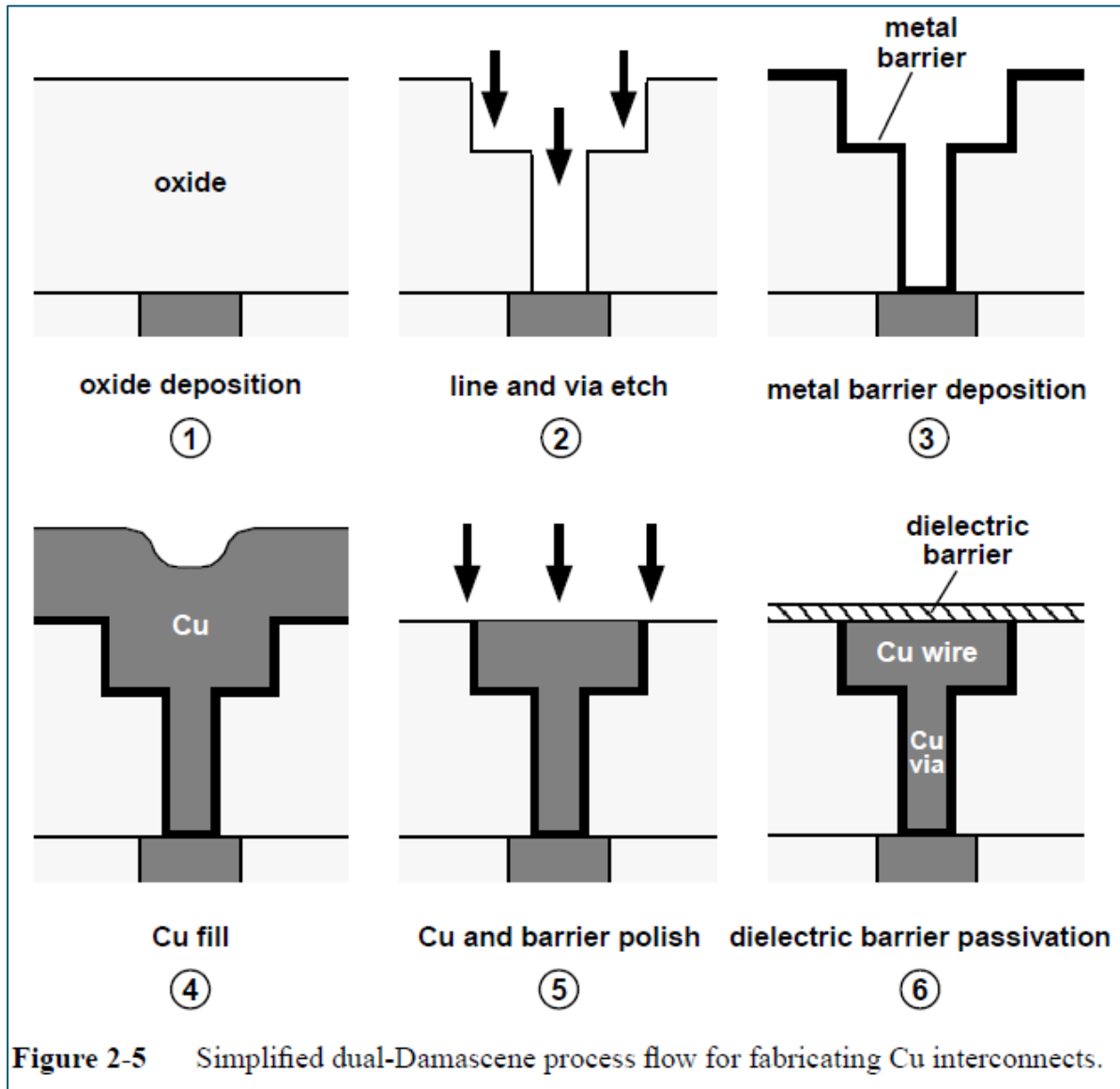
A. Interconnects and Dual Damascene

Semiconductor chips have multiple levels of conductive wires (“interconnects”) for controlling chip operation, with vias connecting wires between different levels when needed; such interconnect structures are commonly made of aluminum or copper. TSMC-1015, 1:13-24; *see also* TSMC-1012, 32; TSMC-1017, 2:53-58. Exemplary interconnect structures are shown below:



Dual damascene is a manufacturing process where patterns of trenches and underlying via holes are filled with conductive metal(s) to simultaneously form the interconnects on a given level and the vias below that level. TSMC-1015, 4:20-23;

TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract; TSMC-1034, 671-76. This process is illustrated below:



TSMC-1027, 25. Steps ④→⑤ are typically performed using chemical mechanical polishing (“CMP”). TSMC-1034, 322-34, 675.

B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength

Stress migration and electromigration involve the movement of metal atoms and vacancies within the interconnect structure; because vacancies tend to aggregate in/under vias, voids can form and cause electrical disconnects. TSMC-1029, 207; TSMC-1028, 5455-56, 5458-59; TSMC-1015, 1:32-37, 2:61-63. In addition, insulating films, especially low-k materials, can have poorer mechanical strength and adhesion, making them susceptible to damage during CMP. TSMC-1016, 1:53-2:7; TSMC-1026, 583.

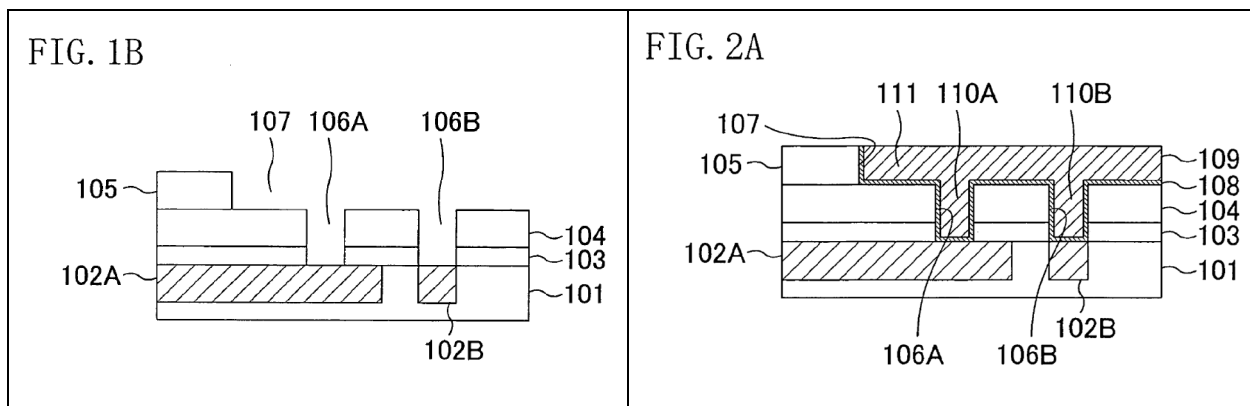
Dummy structures were used long before the '623 patent for addressing these problems. For example, dummy vias have been added near active vias to arrest stress-induced vacancy migration and void formation. TSMC-1029, Abstract, 208; TSMC-1015, 2:64-3:14. Dummy structures were also known to alleviate electromigration concerns, acting as reservoirs for metallic ions. *See* TSMC-1015, 1:66-2:11; TSMC-1032, ¶¶[0012]-[0016]. Migrating vacancies/microvoids get distributed between vias and dummy vias, reducing their concentration in/under active vias. TSMC-1029, 208; TSMC-1009, ¶[0088]. Dummy vias also improve mechanical strength, preventing damage during CMP. TSMC-1016, 4:42-47; TSMC-1026, 584-85.

Similar to dummy vias, dummy wirings/interconnects also improve mechanical properties, helping adhesion across multiple insulating layers and improving the CMP process by reducing dishing. TSMC-1020, Abstract; TSMC-1024, 2:55-58; TSMC-1025, Abstract; TSMC-1026, 584-85. Connecting dummy wirings to dummy vias was well-known to increase the mechanical strength of the combined insulating layer and upper-level wiring, as well as enhance the durability of multi-layered insulating films. TSMC-1011, 8:35-54.

III. THE '623 PATENT

A. Overview

The '623 patent relates to a semiconductor device having multilevel interconnection structures. TSMC-1001, 7:47-50. A first interconnect 102A (and optionally a dummy interconnect 102B) is formed in insulating film 101. *Id.*, 10:56-63, Figs. 1A, 2B. After forming intermediate insulating layers 103-105, the dual damascene process is used to form second interconnect 111 on/in the insulation layer stack, which is connected to first interconnect 102A by via 110A:



Id., 11:5-21; 6:38-40, Figs. 1B-1C, 2A-2B. Dummy via 110B, formed in dummy hole 106B simultaneously with via 110A and interconnect 111, connects dummy interconnect 102B with second interconnect 111. *Id.*, 11:15-21; Figs. 2A-2B.

First interconnect 102A, via 110A and second interconnect 111 constitute part of a closed-circuit during device operation, while neither dummy interconnect 102B nor dummy via 110B does. *Id.*, 10:24-28. That is, the device remains operable even if dummy interconnect 102B and dummy via 110B are omitted from the structure. *Id.*, 10:28-32.

According to the '623 patent, vacancies in copper film 109 of second interconnect 111 are divided and respectively flow into via 110A and dummy via 110B, thereby reducing vacancies flowing into via 110A and reducing the associated stress gradient. *Id.*, 11:36-42. The '623 patent says this suppresses occurrences of voids in via hole 106A. *Id.*, 11:38-45.

B. Prosecution History

The '623 application was filed on December 2, 2004, claiming priority to a Japanese application filed December 3, 2003. Following the addition of claims 27-86 in a restriction response, the USPTO issued multiple Office Actions rejecting the claims over U.S. Patent No. 6,919,637 to He. TSMC-1002, 237-47, 285-97. The Examiner also rejected dependent claims reciting relative interconnect widths, via diameters, and their spacing, stating that “one of ordinary skill in the art would

have been led to the recited shapes, sizes and dimensions through routine experimentation and optimization.” *Id.*, 244-45, 295-96. Applicant responded first by requiring that the dummy via be conductive, then adding “dual damascene” limitations, but later deleted these limitations and instead required that the dummy via be incapable of current flow. *Id.*, 266, 301, 331. The NOA re-added the dual-damascene limitations, while stating that the prior art did not teach the “dummy via made of a conductive film and being arranged as in the context of claim 27.” *Id.*, 354-55.

C. Claim Construction

The Board construes claims under the standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For purposes of this proceeding, Petitioner does not believe that any claim terms need construction to resolve the unpatentability issues presented in this Petition. TSMC-1003, ¶57.

IV. ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. TSMC-1003, ¶37. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. *Id.*

V. PRIOR ART²

Reference	Filed	Published	Pre-AIA Prior Art Qualification
Watanabe	12/4/2002 (USPTO)	6/26/2003	§§102(a),(b),(e)
Hasunuma	9/3/2003 (USPTO)	6/17/2004	§102(e)
Iizuka	1/24/1992 (USPTO)	10/5/1993	§§102(a),(b),(e)
Kurashima	8/14/2003 (USPTO)	5/9/2006	§102(e)
Nasu	6/24/1998 (JPO)	1/14/2000	§§102(a),(b)
Fujii	10/8/1997 (JPO)	8/11/1998	§§102(a),(b)
Kamoshima	9/9/2003 (USPTO)	9/9/2004	§102(e)
Fukazawa	3/29/2001 (JPO)	10/11/2002	§§102(a),(b)

VI. DETAILED EXPLANATION OF GROUNDS

A. Ground 1A: Watanabe Anticipates Claims 10, 19-20, 24, and 27

Watanabe anticipates claims 10, 19-20, 24, and 27. TSMC-1003, ¶¶106-194.

² All references are prior art regardless of any priority claim to the Japanese application filed December 3, 2003. Petitioner does not acquiesce that any claims are so entitled.

C. Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3) and 42.10(a), Petitioner provides the following counsel and service information. Pursuant to 37 C.F.R. §42.10(b), a Power of Attorney accompanies this Petition.

Lead Counsel	Back-Up Counsel
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Petitioner consents to electronic service directed to the following email address: Foley_TSMC_623-2_IPR2025-01211@foley.com.

IX. PAYMENT OF FEES

The Office is authorized to charge fees for this Petition to Deposit Account No. 19-0741. Any additional fees that might be due are also authorized.

X. CONCLUSION

For the reasons given above, Petitioner requests IPR be instituted for the challenged claims.

Respectfully submitted,

Dated: July 25, 2025

By: /Michael R. Houston/

Michael R. Houston
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FOLEY & LARDNER LLP
Counsel for Petitioner

**CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME
LIMITATION, TYPEFACE REQUIREMENTS, AND TYPE STYLE
REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,966 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. §42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. §42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

Respectfully submitted,

Date: July 25, 2025

By: /Michael R. Houston/

Michael R. Houston
Reg. No. 58,486
FOLEY & LARDNER LLP
Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on July 25, 2025, true and correct copies of the foregoing document and supporting materials were served in its entirety on the Patent Owner at the following address of record listed on the USPTO's Patent Center via overnight service:

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Courtesy copies of the same documents were served electronically on prosecution counsel and Patent Owner's litigation counsel by email at the following addresses:

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Respectfully submitted,

Date: July 25, 2025

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