

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

IPR2025-01302
U.S. Patent 8,884,373

**PETITIONER'S OPPOSITION TO PATENT
OWNER'S DISCRETIONARY DENIAL REQUEST
[PUBLIC REDACTED VERSION]**

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I. Introduction

A core purpose of the PTAB under the American Invents Act (AIA) is to strengthen the integrity of the U.S. patent system by ensuring only valid and properly granted patents remain in force. The challenged patent, U.S. Patent 8,884,373, issued as a result of material error by the Examiner. Specifically, among other errors, the Examiner ignored core technical teachings in Tamaki, applied here as a single reference §103 ground, which included two separate embodiments each disclosing the limitation the Examiner contended it and all other prior art of record lacked. Applicant's misleading and erroneous representations regarding Tamaki further contributed to the Examiner's error. Institution is warranted to address these errors.

The merits of TSMC's Petition are exceedingly strong. Tamaki (§103) and Igarashi (§103) each disclose all limitations of the independent claim, including the limitation leading to the '373 patent's allowance, as well as many dependent claims.

The settled interests of TSMC outweigh any settled interests of AICP warranting a merits determination. First, TSMC has an expectation the '373 patent, directed to polysilicon gates, would not be enforced against its fundamentally different metal gate products. Yet all but one of the accused 28nm and 22nm products are metal gate products. And TSMC has an expectation of non-enforcement against the sole polysilicon gate product because that product was announced and offered for sale before the '373 patent. TSMC's settled expectations were further strengthened

due to the lack of any evidence of commercialization, licensing, or marking in the “technology space” where it is now asserted. For more than a decade after the ’373 patent’s issuance, TSMC manufactured the accused chips without incident, including for American customers who integrate those chips into their products.

Institution is an efficient use of Board resources in view of the *Fintiv* factors. First, TSMC has proffered an extraordinarily broad stipulation removing absolutely any overlap between the IPR and parallel litigation by foregoing all §§102 and 103 prior art challenges upon institution. Instituting TSMC’s Petition provides a true alternative to adjudicate invalidity, and the Board, with its specialized resources and efficient processes, is best suited to do so. Second, a final written decision (“FWD”) is more likely than not to issue before the trial date. Although the trial date is currently scheduled a few months before the statutory due date for the FWD, the official U.S. Courts trial statistics suggest trial would occur **over 3 months after** the FWD. This fact, combined with the uncertainty due to the current shutdown of the Federal Government, counsels against discretionary denial.

Finally, compelling economic, national security, and other public interest considerations all make IPR of this patent a compelling use of the Office’s resources. Despite AICP’s allegations to the contrary, its complaint seeks an injunction against TSMC and this requested remedy has not been withdrawn. For the ’373 patent alone, AICP alleges infringement by TSMC’s 28nm and 22nm process nodes. AICP’s

allegations under the other asserted patents involve TSMC's 3nm-16nm FinFET process nodes. It is implausible that such a wide-ranging infringement campaign would not impact U.S. national security and public interests. TSMC, a trusted foundry and the world's largest chip maker (reportedly providing around 90% of the world's advanced chips), is vital to the U.S. supply chain with a wide range of applications, including AI (e.g., NVIDIA's AI supercomputers) and military/defense applications (e.g., the F-35 stealth fighter). Given TSMC's vital and strategic contribution in the U.S. supply chain, the Administration has a heightened interest in ensuring the error in issuing this patent is corrected.

II. Institution is Warranted in View of the Material Errors by the Examiner and Strong Technical Merits of the Petition

A. The Examiner Materially Erred by Overlooking Disclosures in Tamaki, Applied as a Secondary Reference During Prosecution.

The merits here are particularly strong due to errors made during prosecution, warranting institution to correct those mistakes. During prosecution, the Examiner applied Tamaki as a secondary reference in an obviousness rejection. The Examiner, however, failed to appreciate that two embodiments of Tamaki individually disclose or render obvious every limitation of claim 1, including the limitation added by amendment which the Examiner incorrectly found to be missing from Tamaki and all prior art of record when allowing the claims. (*See* Paper-2, 16-52; *see* §II.B.)

Applicant filed an IDS citing both the International Search Report for the

corresponding PCT application (PCT/JP2011/00616) and Tamaki which “corresponds to JP 2008-042092 [JP-Tamaki]” listed as an X reference on the search report. (TSMC-1002, 6-7.) The Examiner then issued an Office Action that rejected pending claims as obvious over the combination of Shimomura (JP2010-067812) and Tamaki. For claim 1, the Examiner only cited Tamaki’s ¶¶9 and 47-50 for a disclosure of “a silicon film¹ of a conductivity type to all four regions” (TSMC-1002, 208-09) that the Examiner mapped to the “conductivity type” recitations of limitations [1C]-[1D]. The record contains no indication that the Examiner reviewed the entirety of Tamaki or appreciated its disclosure.

In response, Applicant added the limitation reciting the “*second dual-gate electrode being separated from the first dual-gate electrode*” to claim 1. (TSMC-1002, 239, 243-46.) Applicant argued incorrectly that Tamaki “fail[ed] to disclose or suggest a device including two dual-gate electrodes that are separated from each other and independent of each other.” (TSMC-1002, 246.) Crediting Applicant’s arguments, in the Examiner’s reasons for allowance, the Examiner stated that the “prior arts of record do not teach or fairly suggest” a device comprising “a second dual-gate electrode being separated from the first dual-gate electrode” and concluded

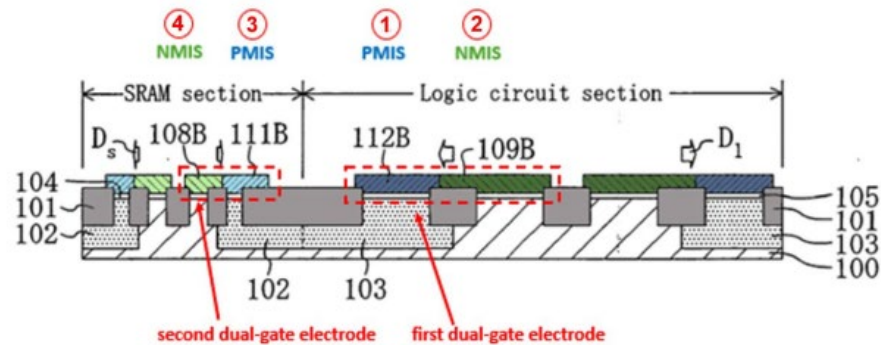
¹ The Examiner erred by equating Tamaki’s gate insulating films 104 and 105 to the claimed gate electrodes’ “*silicon films*.” (See TSMC-1002, 208; TSMC-1006, ¶84.)

“[t]hus, it is possible to reduce degradation of characteristics of FETs due to the mutual diffusion of impurities **between the n-type region and the p-type region in the polysilicon gate electrodes.**” (TSMC-1002, 257-58.)

The allowance was erroneous for multiple reasons. First, contra to Applicant’s argument accepted by the Examiner, the claim does not require the two dual-gate electrodes to be “independent”—only “*separated.*” Second, the Examiner misunderstands Tamaki and the claims because diffusion between n-type and p-type regions relates to a single dual-gate electrode, and is irrelevant to separation between two dual-gate electrodes. Despite filing an amendment after allowance, Applicant neglected to bring this error to the Examiner’s attention. (TSMC-1002, 288-90.) Third, the Examiner was incorrect that the prior art of record failed to disclose the added “*separated from*” limitation given that the ’373 patent’s own background admits that such a structure was known in the art. (*See* TSMC-1001, 1:48-3:15, Figure 1A (logic dual-gate electrode not connected to any other circuitry); Paper-2, 6-12.)

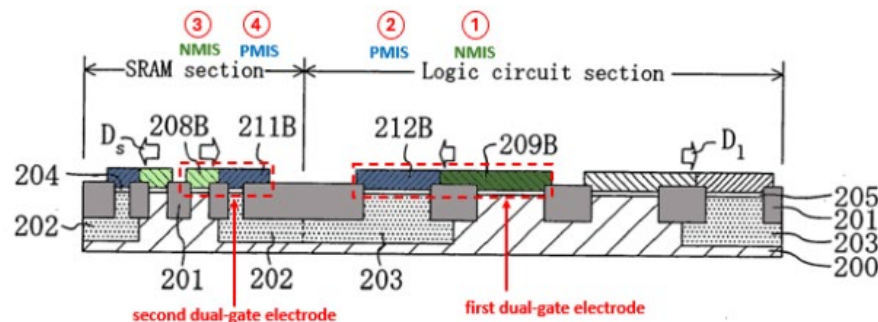
Tamaki’s first and second embodiment each independently discloses this “*separated from*” limitation, as TSMC’s Petition establishes and AICP does not dispute. (Paper-2, 26-29, 43-45.) For example, Tamaki teaches that after forming SRAM gate insulating film 104 and logic gate insulating film 105 during manufacture of the first embodiment device, the gate electrode formation film 106—which is “formed of a polysilicon film”—is formed “on the entirety of the semiconductor

substrate.” (Paper-2, 23 *citing* TSMC-1006, ¶84.) After implanting impurities, “patterning is performed” to form a logic dual-gate electrode with n-type gate electrode 109 and p-type gate electrode 112 as well as a separate SRAM dual-gate electrode with n-type gate electrode 108 and p-type gate electrode 111, as shown in Figure 3B. After patterning, the “*second dual-gate electrode*” is “*separated from the first dual-gate electrode*” [1B]. Thus, Tamaki’s first embodiment expressly discloses the allegedly missing limitation.



Tamaki, Figure 3B

Tamaki’s second embodiment, illustrated in Figure 5B (below), also discloses that after patterning, the “*second dual-gate electrode*” is “*separated from the first dual-gate electrode*.” (Paper-2, 43-44, *citing* TSMC-1006, ¶¶130-31.)



Tamaki, Figure 5B

The Examiner committed material error by relying on Applicant's erroneous and misleading representations regarding Tamaki, by failing to appreciate Applicant's admissions in the patent's Background regarding the prior art, by overlooking multiple disclosures in Tamaki of the allegedly missing separated dual-gate electrodes, and by allowing the '373 patent because of this limitation.

The severity of the Examiner's material error here is as strong as, if not stronger than, the material errors the Director has found justify referral. *See, e.g., Samsung Elecs. v. Wilus Inst. of Standards and Tech.*, IPR2025-00933, Paper-11, 4 (Oct. 10, 2025) (referring, despite earlier trial date, because "Office erred in overlooking teachings of" reference applied by Examiner during prosecution); *Taiwan Semiconductor Mfg. Co. Ltd., et al v. Marlin Semiconductor Ltd.*, IPR2025-00847, Paper-11, 3-4 (Sept. 3, 2025) (referring, despite challenged patent being in force for 15 years, because the "Office erred in a manner material to the patentability of the challenged claims during patent examination" by "overlook[ing] certain teachings in" a reference applied in a rejection during prosecution "that appear to disclose the claimed features that the patent examiner indicated were not taught by the prior art of record, including" the applied reference); *Freightcar Am., Inc. v. Nat'l Steel Car Ltd.*, IPR2025-1046, Paper-20, 2-3 (Oct. 10, 2025) (referring petition for a 13-year old patent, based on examiner error where "examiner overlooked certain teachings of" a disclosed reference "that appear[s] to disclose the allowable features").

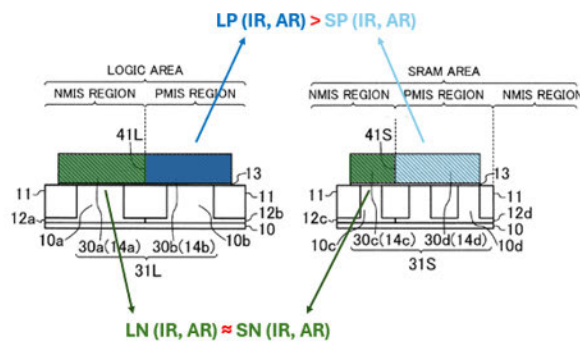
Applicant's unfair dealings during prosecution weigh heavily against discretionary denial. *See Tessell, Inc. v. Nutanix, Inc.*, IPR2025-00322, Paper-14, 2 (June 12, 2025) (finding Office "may consider unfair dealings as a factor" in discretionary denial). **Nine months** before the '373 patent's filing, Applicant received the Written Opinion of the International Searching Authority determining a claim with the same scope as as-filed U.S. claim 1 lacked novelty and inventive step over JP-Tamaki (corresponding to Tamaki). (TSMC-1020, 5.) Applicant obscured this Written Opinion from the U.S. Examiner by filing an untranslated version as part of a miscellaneous incoming letter. (TSMC-1002, 18-22, 133.) Applicant did not list the Written Opinion on the filed IDS or provide a translation. (TSMC-1002, 6.) Despite knowing the clear relevance of Tamaki as indicated in the Opinion, Applicant misrepresented Tamaki's teachings to the U.S. Examiner by stating that Tamaki "fails to disclose or suggest" the added separated dual-gate electrodes limitation. (TSMC-1002, 246.) Such actions compel institution to address and rectify.

B. Tamaki and Igarashi (Both Single-Reference §103) Disclose All Claim 1 Limitations Including the Limitation Leading to '373 Patent Allowance

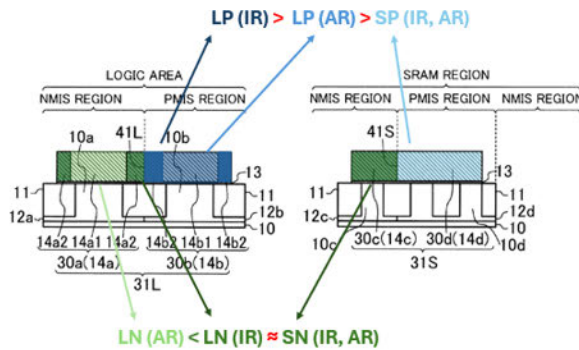
The Petition's merits are strong, well-supported, and well-reasoned, and the invalidity positions are straightforward. TMSC presents three single-reference §103 grounds against the sole independent claim—two embodiments of Tamaki and Igarashi. (Paper-2, 2.) The device of independent claim 1, specified in limitations [1A]-[1F], is broadly claimed and covers the following device type-conductivity type

scenarios discussed in embodiments 1-4 of the '373 specification (illustrated below):

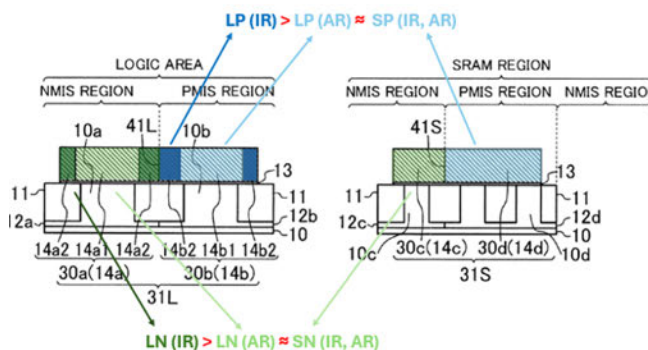
Claim Language		Scenarios Covered by Independent Claim			
		A-1	A-2	B-1	B-2
<i>first dual-gate electrode</i>	<i>first gate electrode</i>	logic NMOS	SRAM NMOS	logic PMOS	SRAM PMOS
	<i>second gate electrode</i>	logic PMOS	SRAM PMOS	logic NMOS	SRAM NMOS
<i>second dual-gate electrode</i>	<i>third gate electrode</i>	SRAM NMOS	logic NMOS	SRAM PMOS	logic PMOS
	<i>fourth gate electrode</i>	SRAM PMOS	logic PMOS	SRAM NMOS	logic NMOS



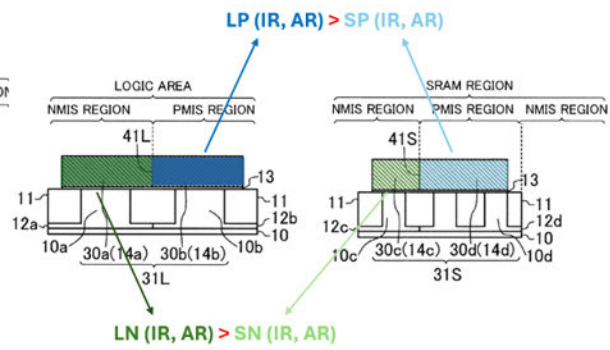
'373 Patent, Figures 1B(left), 1D(right)



'373 Patent, Figures 9B(left), 9D(right)



'373 Patent, Figures 11B(left), 11D(right)



'373 Patent, Figures 13B(left), 13D(right)

Limitation [1G] then specifies an impurity concentration relationship (illustrated for each scenario): “at least a portion of the first silicon film of the first conductivity type

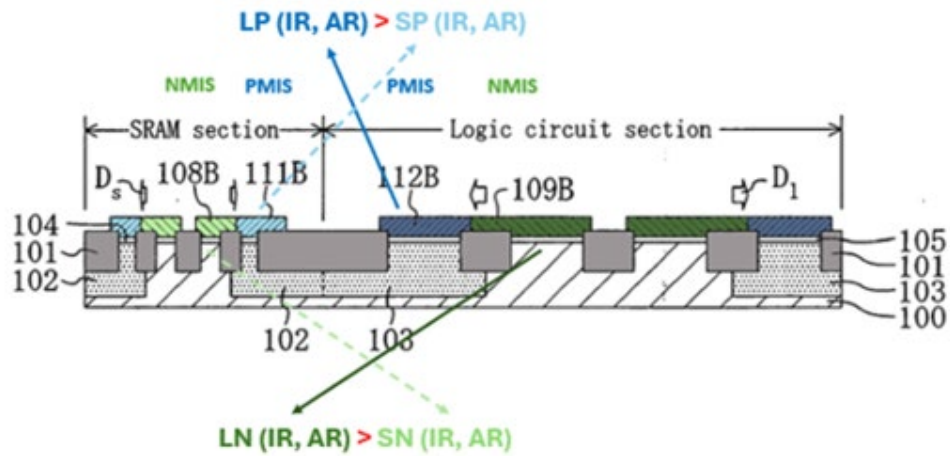
[portion over isolation region (IR) and/or active region (AR)] *has a first-conductivity-type impurity concentration higher than that of a portion of the second silicon film of the first conductivity type located on the third active region [AR].”*

	Claimed Impurity Concentration Relationship
A-1	$LN(IR, AR) > SN(AR)$
A-2	$SN(IR, AR) > LN(AR)$
B-1	$LP(IR, AR) > SP(AR)$
B-2	$SP(IR, AR) > LP(AR)$
LP: Logic-PMIS gate electrode SP: SRAM-PMIS gate electrode LN: Logic-NMIS gate electrode SN: SRAM-NMIS gate electrode (IR, AR): isolation region and/or active region LP (IR, AR): Portion of logic-PMIS gate electrode over IR and/or portion over AR LN (IR, AR): Portion of logic-NMIS gate electrode over IR and/or portion over AR SP (IR, AR): Portion of SRAM-PMIS gate electrode over IR and/or portion over AR SN (IR, AR): Portion of SRAM-NMIS gate electrode over IR and/or portion over AR SN/LN/SP/LP (AR): Portion of gate electrode over AR	

Tamaki’s two embodiments disclose claim 1’s device structure, which Applicant acknowledged was known, and concentration relationship. (Paper-2, 21-30, 41-46; TSMC-1001, 2:11-42.) The primary distinction between Tamaki’s embodiments is the impurity concentration relationship of the NMIS and PMIS gate electrodes in the SRAM and logic sections. (Paper-2, 16 *citing* TSMC-1006, ¶¶86-106, 118-35.)

As shown in Figure 3B below, the impurity relationship disclosed in the Tamaki’s first embodiment meets the claimed impurity concentration under both scenarios A-1 and B-1, like the ’373 patent’s fourth embodiment (Figures 13B, D).

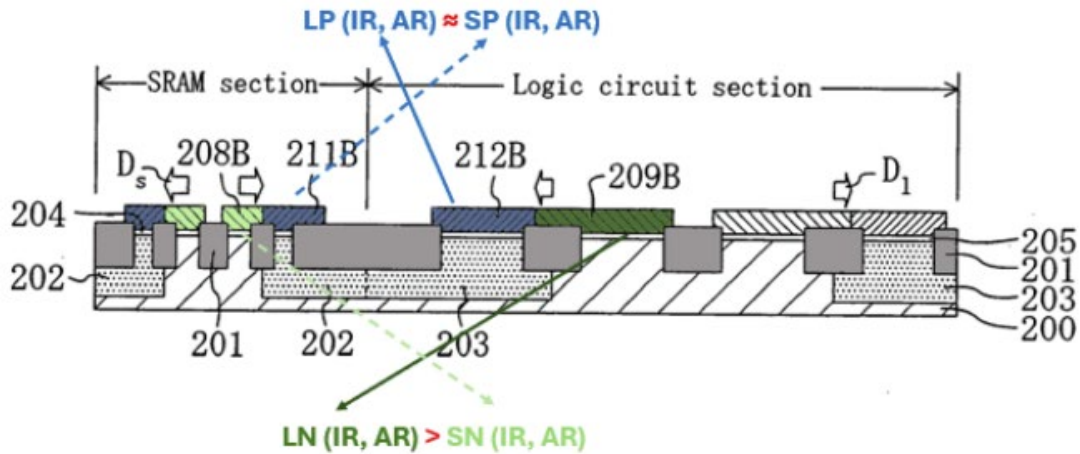
	Claimed Impurity Concentration Relationship	Tamaki-First Embodiment Impurity Concentration Relationship Meeting Claimed Relationship
A-1	$LN(IR, AR) > SN(AR)$	$LN(IR, AR) > SN(IR, AR)$
B-1	$LP(IR, AR) > SP(AR)$	$LP(IR, AR) > SP(IR, AR)$



Tamaki, Figure 3B

As shown in Figure 5B below, the impurity relationship disclosed in the Tamaki's second embodiment meets the claimed impurity concentration under scenario A-1.

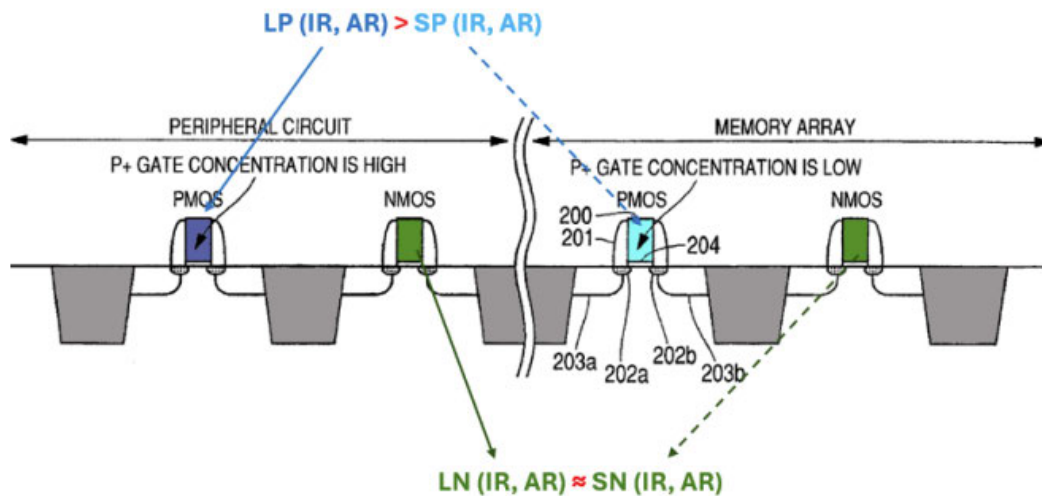
	Claimed Impurity Concentration Relationship	Tamaki-First Embodiment Impurity Concentration Relationship Meeting Claimed Relationship
A-1	$LN(IR, AR) > SN(AR)$	$LN(IR, AR) > SN(IR, AR)$



Tamaki, Figure 5B

Igarashi also discloses the same structure and impurity concentration as recited in claim 1 (scenario B-1), as illustrated below. (Paper-2, 67-82.)

	Claimed Impurity Concentration Relationship	Igarashi Impurity Concentration Relationship Meeting Claimed Relationship
B-1	$LP(IR, AR) > SP(AR)$	$LP(IR, AR) > SP(IR, AR)$



Igarashi, Figure 10

III. Institution is Warranted Because the Settled Expectations of Petitioner and Others Outweigh AICP's Alleged Expectations

Petitioner's settled expectations outweigh AICP's alleged expectations. First, the '373 patent is directed to a device having two dual-gate electrodes, each with two gate electrodes having a "silicon film." That is, the '373 patent is directed to devices with (doped) **polysilicon** gate electrodes. TSMC has a settled expectation the challenged patent would not be asserted against its fundamentally different 22nm and 28nm **metal gate** devices, which do not incorporate (poly)silicon films in their gate electrodes. Instead, the metal gate electrodes are formed from a stack of thin metallic layers, rather than a (poly)silicon film or layer.

AICP has asserted the '373 patent against the 28nm High Performance Low Power (HPL), 28nm Ultra Low Power (ULP) and 28nm Low Power (LP) process node and the 22nm ULP and 22nm Ultra Low Leakage (ULL) process node. (*See* EX2001, ¶¶107-24.) The 28nm HPL, 28nm ULP, 22nm ULP, and 22nm ULL process nodes use **replacement metal gate (RMG)/high-k metal gates (HKMG)** and as such the gate electrodes do not have a "silicon film." (*See, e.g.*, TSMC-1021 (showing process node 28ULP and 28HPL use metal gates); TSMC-1022 (discussing 22nm ULL uses HKMG gate-last process); TSMC-1023.) The '373 patent is therefore directed at fundamentally different technology than in TSMC's 28nm HPL and ULP and 22nm ULP and ULL using HKMG—i.e., high-k gate dielectric/metal gate electrodes. TSMC has settled expectation the '373 patent would not be asserted

against these fundamentally different technologies. *BOE Technology Group Co., LTD v. Optronics Sci. LLC*, IPR2025-00238, Paper-11, 2 (July 29, 2025) (agreeing Petitioner has settled expectations “the challenged patents would not be asserted against it because the [] patents are directed to technology that is fundamentally different from what Petitioner uses in its products”).

Second, TSMC has a settled expectation the ’373 patent would not be asserted against products that pre-date its priority date. Specifically, only the accused 28nm LP process node uses a conventional polysilicon gate. (See TSMC-1021.) TSMC has a settled expectation the ’373 patent would not be asserted against the 28nm LP product because this product predates the alleged priority date of the ’373 patent (Mar. 25, 2011). [REDACTED]

[REDACTED]

Third, TSMC and its customers have settled expectations that the ’373 patent would not apply due to the prior owner’s inaction over the decade since the ’373 patent issued. The accused 28nm LP product entered volume production in October 2011. For over a decade after the November 11, 2014 issue date of the ’373 patent, TSMC invested billions of dollars in fabrication facilities to manufacture millions of wafers per year using the accused 28nm technology, and its customers similarly invested significant resources into designs based on that technology. During this time, the prior owner of the ’373 patent remained silent and inactive. TSMC’s continuous

manufacturing and extensive investments, beginning before the '373 patent issued and with no enforcement after, show that TSMC and its customers relying on its accused technology all have settled expectations that the patent would not apply. Other analysis of a property owner's extended periods of inaction routinely finds the equities favor innocent actors such as TSMC. *See* Restatement (First) of Prop. § 459 cmt. a (1993) ("Through lapse of time old rights become obscure. A long continued use raises reasonable expectations of its continuance."); *Anaheim Gardens, L.P. v. United States*, 953 F.3d 1344, 1350-51 (Fed. Cir. 2020); *Nordlinger v. Hahn*, 505 U.S. 1, 12-13 (1992) ("[A]n existing owner rationally may be thought to have vested expectations in his property or home that are more deserving of protection than the anticipatory expectations of a new owner at the point of purchase.").

Fourth, AICP has not presented any evidence that the '373 patent was ever "commercialized, asserted, marked, licensed, or otherwise applied" in the same "particular technology space" where it now seeks to assert it, weighing against any claim by AICP of "settled expectations." *Intel Corp. v. Proxense LLC*, IPR2025-00327, Paper-12, 2-3 (June 26, 2025). Indeed, the '373 patent appears to have been asserted for the first time only after AICP acquired it more than a decade after issuance. (TSMC-1041.) When AICP acquired patents (like the '373 patent) that had never been asserted, with the intention of asserting them, the only reasonable expectation is that their validity would be challenged. *See Anaheim Gardens*, 953 F.3d at 1350-

51 (“timing” of a property purchase and “knowledge of the purchaser” are relevant in determining whether purchaser had reasonable investment-backed expectations); *Celgene Corp. v. Peter*, 931 F.3d 1342, 1361-63 (Fed. Cir. 2019) (patent owners know their patents may be subject to post-issuance reconsideration proceedings).

There is no evidence in the record that the ’373 patent was licensed, let alone licensed in TSMC’s particular technology space. In response to TSMC’s request to produce any license to the ’373 patent in Patent Owner’s possession, AICP produced nothing more than the PPA (EX2026) and responded “AICP is not withholding production of any documents in its possession that are responsive to this request.” (TSMC-1064, 1.) AICP has also not produced any evidence of marking or commercialization of the ’373 patent.

AICP’s supposed “rel[iance] on the fact that no party had ever challenged” the ’373 patent ignores that no party previously attempted to publicly assert, commercialize, or mark products with the ’373 patent. So, the public’s “settled expectations” are at least as strong as any expectations of the previous owner. (Paper-9, 20.)

Fifth, AICP’s primary argument for discretionary denial—that “[t]hree of the Four Patents are *expired*,” and a majority of challenged claims “are both *unasserted and expired*”—is meritless. (Paper-9, 1.) The ’373 is unexpired and therefore this argument is inapplicable. Regardless, two of the remaining three patents expired prior to filing of the complaint, a fact that AICP acknowledges. (Paper-9, 4;

EX2001.) TSMC thus has a settled expectation that it would not be sued on expired patents. *See Google v. Sandpiper CDN*, IPR2025-00806, Paper-13, 2 (Sept. 12, 2025) (referring, despite patent being “in force for many years” where patent expired prior to assertion).

AICP further contends “there is nothing ‘cost-effective’ about using limited public resources to adjudicate the validity of expired patents.” (Paper-9, 2.) But AICP sued TSMC in district court claiming infringement of these expired patents, and AICP’s suit will require expenditure of limited public resources to address validity of these expired patents somewhere. The only question is whether addressing the patents’ invalidity will occur in district court or the PTAB. As AICP itself says, “Congress created IPRs to provide a ‘*quick and cost effective alternative*’[] to litigation.” (Paper-9, 1-2) (emphasis in original). And that is why IPR should be instituted for all four patents.

AICP further faults TSMC for challenging “unasserted” claims. AICP is wrong. Indeed, TSMC filed the majority of its current IPRs (including this IPR) before AICP served its infringement contentions—i.e., before there was any identifiable group of “asserted” versus “unasserted” claims. (*Compare* EX2004, 5 (contentions served on July 16, 2025) *with* Paper-2 (filed July 15, 2025); IPR2025-01210, Paper-1 (filed July 15, 2025); IPR2025-01305, Paper-1 (filed July 15, 2025).) Since AICP did not identify asserted claims in its complaint, its position would require a

petitioner to wait to file until after receiving infringement contentions, a fact which AICP uses as a reason for denial under *Fintiv*. Moreover, AICP has made no representations that it will not add claims to the pending litigation. TSMC however stipulates that if AICP provides a covenant not to sue TSMC and its customers on the non-asserted claims, TSMC would seek authorization to withdraw challenges against such claims. And AICP's argument ignores that under *Fintiv* Factor 4, "additional challenged claims not at issue in the district court ... weigh[] against exercising discretion to deny institution." *Samsung Display Co. Ltd. v. Pictiva Displays Int'l Ltd.*, IPR2024-01222, Paper-12, 8 (Mar. 6, 2025).

In sum, the settled expectations of TSMC, its customers, and the public, spanning over a decade, cannot be overridden merely based on AICP's acquisition of the '373 patent. AICP acquired it subject to prior third-party expectations, which were reasonable in view of the prior owner's inaction.

IV. Institution Is Warranted by the Other *Fintiv* Factors

TSMC acted diligently by filing its Petition 3 months after the Complaint was filed. The *Fintiv* factors demonstrate it is an efficient use of Office resources to consider the merits of the Petition and therefore weigh against denial.

Fintiv* Factor 4 Weighs Heavily Against Discretionary Denial.** TSMC proffered an extraordinarily broad stipulation, offering to remove ***all invalidity grounds under Sections 102 and 103, involving any type of legally recognized prior art in

the parallel litigation, if TSMC's Petition is instituted, making the Board a true alternative venue for invalidity. (*See* TSMC-1019, 1-2.) This stipulation weighs heavily against discretionary denial. *See, e.g., Tesla, Inc. v. U.S. Sec'y of the Navy*, IPR2025-00341, Paper-12, 2 (June 13, 2025); *Tesla, Inc. v. Intell. Ventures II*, IPR2025-00339, Paper-10, 2 (June 13, 2025). It ensures this IPR, if instituted, is a true alternative for this phase of the litigation.

***Fintiv* Factor 2 Weighs Against Discretionary Denial:** Based on the current U.S. Courts time-to-trial statistics, it is unclear whether a FWD will issue after the District Court trial occurs, rendering Factor 2 at least neutral. The projected FWD due date is January 28, 2027, while the district court's currently scheduled trial date is November 16, 2026 (*See* EX2027). But the latest time-to-trial statistics from the U.S. Courts suggest trial will not begin until May 2027. (*See* TSMC-1042 (median time to trial in E.D. Texas of 25.9 months), 35.) Such considerations neither favor nor counsel against discretionary denial. *See Tanklogix v. Sitepro*, IPR2025-00761, Paper-10, 2 (Sept. 3, 2025) (finding factor 2 neutral where FWD expected after district court's scheduled trial but before trial date suggested by time-to-trial statistics).

Here, it is more likely than not the Board will issue its FWD before trial begins. Looking specifically at Judge Gilstrap's *patent jury trials* over the past year—the most relevant comparator pool—the median time to trial is 25.5 months, consistent with the latest statistics from the U.S. Courts. That would place the trial date

for the litigation around May 18, 2027, over three months later than the projected January 28, 2027 statutory deadline. (*See* TSMC-1043, 4.) AICP, however, ignores this evidence and misleadingly cites non-analogous data associated with all trials before Judge Gilstrap to imply the associated patent trial is likely to occur prior to the FWD. (Paper-9, 12-13.) AICP further suggests that because the trial date has not changed in the case’s first 5 months, the only reasonable assumption is it will never change. (Paper-9, 12.) These citations and suggestions fly in the face of common sense and overwhelming evidence of recent delays in Judge Gilstrap’s original scheduled patent trials. (*See, e.g.*, TSMC-1044 (moving Oct. 3 trial to Oct. 27); TSMC-1045 (same); TSMC-1046 (delaying Nov. jury trial without explanation); TSMC-1047 (same); TSMC-1048 (same).) Moreover, the uncertain duration of the current U.S. government shutdown may impact the trial date.

***Fintiv* Factor 3 Weighs Against Discretionary Denial:** Based on the current schedule, at the time of institution (“DI”), the District Court case will still be in its early stages—prior to the initial exchange of claim constructions, over two months before any claim construction briefing, over three months before the *Markman* hearing, five months before close of fact discovery, and over six months before close of expert discovery and dispositive motions. (*See* EX2027, 3-5.) AICP points only to the parties’ early invalidity and infringement contentions. (*See* Paper-9, 13-14.) That is not enough as the minimal investment by the parties and the Court weighs against

discretionary denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper-11, 10 (Mar. 20, 2020; *Am. Airlines, Inc., et al. v. Intell. Ventures I, LLC*, IPR2025-00786, Paper-12, 2-3 (Aug. 29, 2025) (referring, despite patent being in force for 18 years, where “little investment in the district court” proceeding).

***Fintiv* Factor 1 Weighs Against Discretionary Denial:** As AICP admits, TSMC’s previous motion to stay was denied without prejudice, and TSMC can re-new after institution. (Paper-9, 9-10.) As discussed above, the DI occurs at an early stage of the case, before opening claim construction briefs are even due. (Paper-9, 10.) Stay motions after institution are generally granted on timelines like this. *See, e.g., Resonant Sys., Inc. v. Samsung Elecs. Co.*, No. 2:22-CV-00423-JRG, 2024 WL 1021023, *2-4 (E.D. Tex. Mar. 8, 2024) (granting stay with claim construction briefing underway, close of fact discovery two months away, and IPR filed three months after invalidity contentions). AICP’s argument that the district court would only stay the case if TSMC’s IPR petitions are instituted against all asserted patents requires the circular assumption some will not be—a poor and speculative assumption.

***Fintiv* Factor 5 Should Weigh Against Denial:** As AICP notes, “factor 5 generally follows factor 2” and therefore weighs against denial here. (Paper-9, 15.)

***Fintiv* Factor 6 Weighs Against Denial.** The district court case here is complex, involving the assertion of 28 claims across four patents. (Paper-9, 1.) The underlying technology is also complex, involving technologically complicated aspects

of semiconductor design and manufacture; trained PTAB judges would be better suited than a lay jury to assess validity. The complexity of the case and technology both weigh *against* discretionary denial. *See, e.g., Navy*, IPR2025-00341, Paper-12, 2-3.

AICP contends that under *Fintiv* Factor 6 “foreign third-party discovery in Japan weighs in favor of discretionary denial” because “[t]hree of TSMC’s five petitions rely on references that TSMC concedes are prior art, if at all only under §102(e).” (Paper-9, 17.) AICP’s argument is inapplicable to the ’373 Petition, which relies on §102(b) prior art. (Paper-2, 1-2.) AICP’s argument strains credibility because AICP did not identify a priority date earlier than the filing date of JP2011-068131 (Mar. 25, 2011), had ample opportunity to obtain such information before asserting the patent (EX2026, 5), and only offers speculation such evidence exists.

V. Review is an Appropriate Use of Office Resources in View of the Compelling National Security, Economic, and Public Interest Considerations

The semiconductor chips manufactured by TSMC are vital to U.S. industries and to the U.S. military. As Secretary Lutnick explained in April 2025, “national security” is the “key” reason to “bring semiconductors home.” (TSMC-1050, 3.) That has been a key principle of President Trump’s agenda: “Our national security depends on bringing our supply chain home. This is especially true when we are dealing with critical technology, computer chips that are not only important to our civilian world ... but also to our military.” (TSMC-1051, 40; *see also* TSMC-1052;

TSMC-1053.) President Trump praised that “TSMC, the greatest manufacturer of chips in the world, is coming to America with a \$100 billion investment.” (TSMC-1055; <https://www.youtube.com/watch?v=tGPWU3NmbVE>, at 0:05-0:23, 0:30-0:44 (praising TSMC in Arizona).)

TSMC is investing \$165 billion in the U.S. (an unprecedented direct foreign investment) and is a trusted partner for the U.S. supply chain—reportedly providing around 90% of the world’s advanced chips (*see* TSMC-1049)—contributing to American national security, economy, innovation, and public interest, and achieving the goals of protecting the U.S. supply chain in high-tech industries and preserving U.S. leadership in artificial intelligence (AI). These vital U.S. economic and national security interests and TSMC’s unprecedented investments, however, are threatened by AICP’s infringement allegations, which implicate a wide range of these TSMC-made chips—manufactured using TSMC’s 22, 28nm planar FET process technologies (’373 patent) and using TSMC’s 3nm-16nm FinFET process technologies (’572, ’751, ’623 patents). Specifically, AICP threatens these interests with an injunction² based on the erroneously-issued ’373 patent. Given the breadth of AICP’s infringement allegations and the extraordinarily broad impact of TSMC’s

² AICP represents it “will not seek injunctive relief” and “cannot do so” for expired patents. (Paper-9, 19.) But AICP seeks an injunction for all asserted patents, including the unexpired ’373 patent, and has not withdrawn this request. (EX2001, 36.)

technology on U.S. national security, economy, innovation, and public interest, it is difficult to imagine a more compelling case for use of the Board's resources.

Indeed, TSMC makes semiconductors for a wide range of "military-grade" devices used by the Department of Defense. (TSMC-1056, 5; TSMC-1057, 59 ("U.S. Department of Defense rel[ies] heavily on Taiwan foundries (particularly TSMC) to manufacture the computer chips needed for their products."); TSMC-1058, 2-3 (TSMC is world's leading manufacturer of radar system chips).) TSMC offers multiple technologies, ranging from 28nm to 3nm, to power widespread military/defense applications like avionics, missile guidance, radar systems, radar electronic warfare, radiation-hardened systems, power systems, imaging for defense and aerospace, and secure communications. The U.S. Air Force estimates "90% of its precision-guided munitions rely on TSMC chips." (TSMC-1054, 4.) A similar calculus applies to warships, satellites, and communication systems. (*Id.*) For example, chips manufactured using TSMC's 28nm process nodes (e.g. 28nm HPL) are used by TSMC's customers such as AMD/Xilinx for defense-grade FPGA chips in military avionics, missiles, & munitions, and electronic warfare. (*See, e.g.*, TSMC-1060, 4; TSMC-1061, 1; TSMC-1062, 1 (Xilinx portfolio using TSMC's 28nm HPL process is suitable for "secure software defined military radios").)

AICP incorrectly argues that these national security concerns should be disregarded if TSMC cannot specifically identify the affected military products. (Paper-

9, 18-19.) Although TSMC's multi-level supply chain has no direct supply relationship with the U.S. government, multiple third-party sources confirm that TSMC's products and processes, including those accused by AICP, are essential to a wide array of U.S. military hardware. Given the nature of the industry (and the heightened difficulty of obtaining public documentation of the military's use of specific chips), TSMC has provided adequate evidence of the importance of the accused process nodes for national security.

The implications of TSMC-built chips for America's economy go far beyond national security. TSMC-built chips power the vast majority of electronic devices in the world, including smartphones, laptops, computer servers, and other devices used in cars and consumer goods. (TSMC-1063, 2.) TSMC enables innovations by its customers, including Apple, NVIDIA, AMD, Broadcom, Microsoft, Amazon, and Tesla, and many others, securing U.S. leadership in high-tech competition.

Given the extraordinarily broad impact of TSMC's technology on U.S. economy and national security, review is an appropriate use of the Board's resources.

VI. Conclusion

For the foregoing reasons, this Petition should be instituted.

Date: October 28, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies, in accordance with 37 C.F.R. § 42.6(e), that the foregoing **Petitioner's Opposition to Patent Owner's Discretionary Denial Request [Public Redacted Version]** was served on December 3, 2025, via e-mail directed to counsel of record for Patent Owner at the following:

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