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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/051,415	03/18/2011	Shunsuke ISONO	085393-0521

CONFIRMATION NO. 4503

POWER OF ATTORNEY NOTICE



OC000000082298627

53080
Rimon PC - Panasonic Corporation
8300 Greensboro Dr.
Suite 500
McLean, VA 22102

Date Mailed: 12/26/2024

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/19/2024.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/sltorres/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/051,415	03/18/2011	Shunsuke ISONO	085393-0521

CONFIRMATION NO. 4503

POA ACCEPTANCE LETTER



OC000000082298639

27197
MICHAEL J. CHERSKOV
SZYMON M. GURDA
903 COMMERCE DR
SUITE 310
OAK BROOK, IL 60523

Date Mailed: 12/26/2024

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/19/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/s/torres/



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
13/051,415

RECEIPT DATE / TIME
12/19/2024 12:14:38 AM Z ET

ATTORNEY DOCKET #
085393-0521

Title of Invention

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	8329572
CONFIRMATION #	4503	FILED BY	Yi Lu
PATENT CENTER #	68437381	FILING DATE	03/18/2011
CUSTOMER #	53080	FIRST NAMED INVENTOR	Shunsuke ISONO
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Szymon Gurda

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA.pdf	2	Power of Attorney	1163 KB
aia0096.pdf	3	Assignee showing of ownership per 37 CFR 3.73	121 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA.pdf	ECBD17696152E1EEC855582EEB520D1FBB759F1067CFFE8D FD2239709901172D3B5DDEED16DBA5F6F9F0D40FA32AAE59 A67432DBE53E12FDC1728795B09E1E0B
aia0096.pdf	33F4054F76582662B53677CBC845778FDCA9B45E58B317C6A ECD31B8905F86B5D3BBC094B27D147C58E263562A441D1439

CECD38C2A4621B2D81A0A0C0FC258D

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

**PATENT - POWER OF ATTORNEY
OR
REVOCATION OF POWER OF ATTORNEY
WITH A NEW POWER OF ATTORNEY
AND
CHANGE OF CORRESPONDENCE ADDRESS**

Patent Number	8329572
Issue Date	December 11, 2012
First Named Inventor	Shunsuke ISONO
Title	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
Attorney Docket No.	0889-04193

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

27197

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or
Individual Name
Address

City

State

Zip

Country

Telephone

Email

I am the:

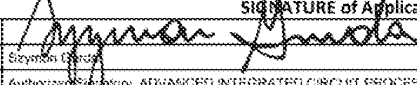
☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Patent Owner

Signature		Date	November 18, 2024
Name	Shunsuke Isono	Telephone	
Title and Company	Authorized Signatory, ADVANCED INTEGRATED CIRCUIT PROCESS LLC		

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: ADVANCED INTEGRATED CIRCUIT PROCESS LLC

Application No./Patent No.: 8329572 Filed/Issue Date: December 11, 2012

Titled: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

ADVANCED INTEGRATED CIRCUIT PROCESS LLC, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: the inventor(s) To: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

The document was recorded in the United States Patent and Trademark Office at
Reel 015826, Frame 0905, or for which a copy thereof is attached.

2. From: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. To: PANASONIC CORPORATION

The document was recorded in the United States Patent and Trademark Office at
Reel 022434, Frame 0348, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: PANASONIC CORPORATION To: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD.

The document was recorded in the United States Patent and Trademark Office at
Reel 052755, Frame 0917, or for which a copy thereof is attached.

4. From: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD. To: NUVOTON TECHNOLOGY CORPORATION JAPAN

The document was recorded in the United States Patent and Trademark Office at
Reel 067711, Frame 0965, or for which a copy thereof is attached.

5. From: NUVOTON TECHNOLOGY CORPORATION JAPAN To: ADVANCED INTEGRATED CIRCUIT PROCESS LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 068118, Frame 0314, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Szymon M. Gurda/

Signature

Szymon M. Gurda

Printed or Typed Name

December 18, 2024

Date

58451

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/051,415	12/11/2012	8329572	085393-0521	4503

53080 7590 11/21/2012
MCDERMOTT WILL & EMERY LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 82 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Shunsuke ISONO, Osaka, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
 or **Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 08/10/2012
 MCDERMOTT WILL & EMERY LLP
 600 13TH STREET, NW
 WASHINGTON, DC 20005-3096

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

53080

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/051,415	03/18/2011	Shunsuke ISONO	085393-0521	4503

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$ 1770	\$300	\$0	\$ 2070	11/13/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, LONG K	2829	438-618000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev. 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

McDermott Will & Emery LLP

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Panasonic Corporation

Osaka, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☒ Advance Order - # of Copies 4

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 500417 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date November 12, 2012

Typed or printed name Michael E. Fogarty

Registration No. 36,139

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		13051415		
Filing Date:		18-Mar-2011		
Title of Invention:		SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
First Named Inventor/Applicant Name:		Shunsuke ISONO		
Filer:		Michael E. Fogarty/Tatiana Tucker		
Attorney Docket Number:		085393-0521		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1770	1770
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	4	3	12
Total in USD (\$)				2082

Electronic Acknowledgement Receipt	
EFS ID:	14205189
Application Number:	13051415
International Application Number:	
Confirmation Number:	4503
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Shunsuke ISONO
Customer Number:	53080
Filer:	Michael E. Fogarty/Tatiana Tucker
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0521
Receipt Date:	12-NOV-2012
Filing Date:	18-MAR-2011
Time Stamp:	16:10:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 2082
RAM confirmation Number	13340
Deposit Account	500417
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Issue Fee Payment (PTO-85B)	if_085393-0521.PDF	98965 b564b09339a712ea63de9afe28fe286f94b97df9	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	33723 a7048e383db7081787eb003cf729a2e6e46e1c33	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			132688		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

53080 7590 08/10/2012
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER

TRAN, LONG K

ART UNIT

PAPER NUMBER

2829

DATE MAILED: 08/10/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/051,415	03/18/2011	Shunsuke ISONO	085393-0521	4503

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	11/13/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 08/10/2012
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/051,415	03/18/2011	Shunsuke ISONO	085393-0521	4503

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	11/13/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, LONG K	2829	438-618000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/051,415	03/18/2011	Shunsuke ISONO	085393-0521	4503
53080	7590	08/10/2012	EXAMINER	
MCDERMOTT WILL & EMERY LLP			TRAN, LONG K	
600 13TH STREET, NW			ART UNIT	
WASHINGTON, DC 20005-3096			PAPER NUMBER	

2829

DATE MAILED: 08/10/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 84 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 84 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.		Applicant(s)	
	13/051,415		ISONO, SHUNSUKE	
	Examiner		Art Unit	
	LONG TRAN		2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Peliminary AMDT on 03/18/2011.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 23-29.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>03/18/2011</u> 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other ____.
---	--

/Long K. Tran/ Primary Examiner, Art Unit 2829	
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DETAILED ACTION

Response to Preliminary Amendment

1. This office action is in response to Amendment filed on 03/18/2011.
Claims 1 – 22 have been cancelled.
Claim 23 has been amended.
Claims 28 and 29 have been added.
Claims 23 – 29 are presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on 04/05/2011.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 03/18/2011, including a fee set forth in § 1.17(p), has been filed and has been considered by the examiner.

Allowable Subject Matter

4. Claims 23 – 29 are allowed.
5. The following is an examiner's statement of reasons for allowance: Claims 23 – 29 are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

Forming an interconnect layer in at least an upper portion of a first insulating film;
forming an oxidation-resistant conductor film covering the top of the interconnect layer;
forming a second insulating film on the first insulating film and the oxidation-resistant
conductor film; and combination of other steps of the independent claims 23 and 28.

Any comments considered necessary by applicant must be submitted no later than
the payment of the issue fee and, to avoid processing delays, should preferably accompany
the issue fee. Such submissions should be clearly labeled "Comments on Statement of
Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the
examiner should be directed to LONG TRAN whose telephone number is (571)272-
1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's
supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for
the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the
Patent Application Information Retrieval (PAIR) system. Status information for
published applications may be obtained from either Private PAIR or Public PAIR.
Status information for unpublished applications is available through Private PAIR only.
For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should
you have questions on access to the Private PAIR system, contact the Electronic

Application/Control Number: 13/051,415

Page 4

Art Unit: 2829

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Long K. Tran/
Primary Examiner, Art Unit 2829

August 6, 2012

Notice of References Cited	Application/Control No. 13/051,415	Applicant(s)/Patent Under Reexamination ISONO, SHUNSUKE	
	Examiner LONG TRAN	Art Unit 2829	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0020168	01-2003	Watanabe et al.	257/760
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Receipt date: 03/18/2011

13051415 - GAU: 2829

SHEET 1 OF 2

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)				ATTY. DOCKET NO. 085393-0521		SERIAL NO. Divisional of U.S. Serial No. 12/153,028	
				APPLICANT Shunsuke ISONO			
				FILING DATE March 18, 2011		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)		Publication Date MM-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US	7,041,586 B2	05-2006	KUDO ET AL.	Corresponding to JP 11-274122 A	
		US	6,730,590 B2	05-2004	OHASHI ET AL.	Corresponding to JP 11-145288 A	
		US	6,908,847	06-2005	SAITO et al.		
		US	6,281,535	08-2001	MA et al.		
		US	6,417,116	07-2002	KUDO et al.		
		US	6,479,366	11-2002	MIYAMOTO		
		US	2002/0079585	06-2002	WONG		
		US	2005/0054122	03-2005	CELII et al.		
		US	6,114,243	09/2000	GUPTA et al.		
		US	6,589,863	07/2003	USAMI, Tatsuya		
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes -Number 4-Kind Codes (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No
		JP 2002-118078 A		04-19-2002	TOSHIBA CORP		
		JP 11-274122 A		10-08-1999	FUJITSU LTD	Corresponding to US 7,041,586 B2	
		JP 11-145288 A		05-28-1999	HITACHI LTD	Corresponding to US 6,730,590 B2	
		JP 2002-373937 A		12-26-2002	FUJITSU LTD		
		JP 2002-289689 A		10-04-2002	FUJITSU LTD		
		JP 2002-270608 A		09-20-2002	FUJITSU LTD		
		JP 2000-174123 A		06-23-2000	NEC CORP		
		JP 8-83780 A		03-26-1996	TOSHIBA CORP		
		JP 2003-133314 A		05-09-2003	HITACHI LTD		
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
		Japanese Office Action issued in corresponding Japanese Patent Application No. 2003-335185, dated August 22, 2006.					
EXAMINER /Long Tran/				DATE CONSIDERED 08/06/2012			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.T./

Receipt date: 03/18/2011

13051415 - GAU: 2829

SHEET 2 OF 2

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 085393-0521		SERIAL NO. Divisional of U.S. Serial No. 12/153,028	
				APPLICANT Shunsuke ISONO			
				FILING DATE March 18, 2011		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US	2002/0125577 A1	09-12-2002	KOMADA		
		US	2005/0085066 A1	04-21-2005	TSAO et al.		
		US	6,313,028 B2	11-06-2001	HUANG et al.		
		US	6,838,370 B1	01-04-2005	NIUYA et al.		
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EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No
		JP 2002-246391		08-30-2002	NEC CORPORATION	Corresponds w/ US 2002/0155702	
		JP 08-264538		10-11-1996	SUMITOMO METAL IND. LTD.		
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
		Japanese Notice of Reasons for Rejection, with English Translation, issued in Japanese Patent Application No. 2006-281346, mailed on October 5, 2010.					
EXAMINER /Long Tran/				DATE CONSIDERED 08/06/2012			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.T./

Search Notes 	Application/Control No. 13051415	Applicant(s)/Patent Under Reexamination ISONO, SHUNSUKE
	Examiner LONG TRAN	Art Unit 2829

SEARCHED			
Class	Subclass	Date	Examiner
438	618	08/05/2012	LT
438	620	08/05/2012	LT
438	622	08/05/2012	LT
438	672	08/05/2012	LT
438	673	08/05/2012	LT
438	700	08/05/2012	LT
438	631	08/05/2012	LT
438	637	08/05/2012	LT
257	E21.59	08/05/2012	LT
257	E21.641	08/05/2012	LT

SEARCH NOTES		
Search Notes	Date	Examiner
EAST SEARCHED	08/05/2012	LT
EAST SEARCHED	08/06/2012	LT
INTERFERENCE CLAIMS SEARCHED	08/06/2012	LT

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
438	ALL ABOVE	08/05/2012	LT
257	ALL ABOVE	08/05/2012	LT

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Index of Claims 	Application/Control No. 13051415	Applicant(s)/Patent Under Reexamination ISONO, SHUNSUKE
	Examiner LONG TRAN	Art Unit 2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	08/06/2012									
	1	-									
	2	-									
	3	-									
	4	-									
	5	-									
	6	-									
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S287	718	438/631.ccls. and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 11:44
S288	2688	438/637.ccls. and @ad<"20040922"	US-PGPUB; USPAT; USOCR	OR	ON	2012/08/05 11:52
S289	1	13/051415	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/08/05 12:10
S290	21	isono-shunsuke.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 12:11
S291	1283	438/618.ccls. and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 12:14
S292	288	438/620.ccls. and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 12:25
S293	3704	438/622,672.ccls. and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 12:30
S294	2692	438/622.ccls. and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 12:31
S295	36	("20020079585" "20020125577" "20020155702" "20030003733" "20030118798" "20050054122" "20050085066" "6114243" "6281535" "6313028" "6417116" "6479366" "6589863" "6730590"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/08/05 17:41

		"6828222" "6838370" "6908847" "7041586").PN.				
S296	9	(US-20030003733-\$ or US-20020079585-\$ or US-20020109229-\$).did. or (US-6730590-\$ or US-6479366-\$ or US-6114243-\$ or US-7041586-\$ or US-6589863-\$ or US-6417116-\$).did.	US-PGPUB; USPAT	OR	OFF	2012/08/05 17:42
S297	19	S295 or S296	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	ON	2012/08/05 17:43
S298	10	S295 not S296	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	ON	2012/08/05 17:43
S299	1160	438/672.ccls. and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 18:19
S301	159	438/673.ccls. and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 23:19
S302	1208	438/700.ccls. and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 23:26
S303	1294	257/e21.59,e21.641.ccls. and @pd<="20030926"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/05 23:53
S304	249	("oxidation-resistant" oxidation\$resistant) near3 (SiN TiN silicon adj nitride titanium adj nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 09:37
S305	55	("oxidation-resistant" oxidation\$resistant) near (SiN TiN silicon adj nitride titanium adj nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 09:38
S306	44	S305 and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 09:39

S307	405	(SiON) near insulat\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 09:52
S308	135	S307 and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 09:53
S309	36	(FSG) near insulat\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 10:00
S310	13	S309 and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 10:00
S311	1	((("oxidation-resistant" oxidation\$resistant) near conductor) near3 (SiN TiN silicon adj nitride titanium adj nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 10:18
S312	7	((("oxidation-resistant" oxidation\$resistant) near conductor) near5 (SiN TiN silicon adj nitride titanium adj nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 10:19
S313	12267	conductor near5 (SiN TiN silicon adj nitride titanium adj nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 10:20
S314	158	conductor near (SiN silicon adj nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 10:20
S315	71	S314 and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 10:21
S316	521	conductor near (Ta TaN tantalum tantalum adj nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 10:52

S317	187	S316 and @ad<"20040922"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 10:53
S320	22	((("oxidation-resistant" oxidation\$resistant) near conductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 11:00
S321	0	((("oxidation-resistant" oxidation\$resistant) near conductor) near10 (Ta TaN tantalum tantalum adj nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 11:41
S322	2	((("oxidation-resistant" oxidation\$resistant) near5 conductor) near10 (Ta TaN tantalum tantalum adj nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 11:41
S323	34	((("oxidation-resistant" oxidation\$resistant) near2 conductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 11:43
S324	12	S323 not S320	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 11:43
S325	16	insulat\$3 near (film layer) and interconnect\$3 near (film layer) and (oxidat\$3 near3 resistant near3 conduct\$3) and photoresist	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2012/08/06 11:50
S326	14	("20020098639" "20030235953" "5072286" "5132771" "5239196" "5364810" "5550396" "6451665" "6483136" "6661063" "6693008" "6740921" "6747324" "7598133").PN. OR ("7981738").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/08/06 11:53

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S327	23	interconnect and ("oxidation-resistant" oxidation\$resistant oxidation adj resistant) and (removing near (photoresist mask photo adj resist)).clm.	US- PGPUB; USPAT; UPAD	OR	ON	2012/08/06 15:23
S328	4	interconnect and ((("oxidation-resistant" oxidation\$resistant oxidation adj resistant) near conductor) and (removing near	US- PGPUB; USPAT;	OR	ON	2012/08/06 15:31

EAST Search History

		(photoresist mask photo adj resist)).clm.	UPAD			
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Issue Classification 	Application/Control No. 13051415	Applicant(s)/Patent Under Reexamination ISONO, SHUNSUKE
	Examiner LONG TRAN	Art Unit 2829

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
438		618				H	0	1	L	21 / 4763 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
438	620	631	637	672	673													
438	700																	
257	E21.59	E21.641																

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	23														
2	24														
3	25														
4	26														
5	27														
6	28														
7	29														

NONE		Total Claims Allowed:	
		7	
(Assistant Examiner)	(Date)	O.G. Print Claim(s)	O.G. Print Figure
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(Primary Examiner)	(Date)		



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BIB DATA SHEET

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SERIAL NUMBER 13/051,415	FILING or 371(c) DATE 03/18/2011 RULE	CLASS 438	GROUP ART UNIT 2829	ATTORNEY DOCKET NO. 085393-0521		
APPLICANTS Shunsuke ISONO, Osaka, JAPAN; ** CONTINUING DATA ***** This application is a DIV of 12/153,028 05/13/2008 PAT 7,935,623 which is a DIV of 11/716,704 03/12/2007 PAT 7,400,045 which is a DIV of 10/945,920 09/22/2004 PAT 7,215,028 ** FOREIGN APPLICATIONS ***** JAPAN 2003-335185 09/26/2003 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/29/2011						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/LONG K TRAN/</u> Examiner's Signature		☒ Met after Allowance <u>/LT/</u> Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 5	TOTAL CLAIMS 7	INDEPENDENT CLAIMS 2
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TITLE SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME						
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				☐ 1.16 Fees (Filing)		
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MCDERMOTT WILL & EMERY LLP
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JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出 願 年 月 日
Date of Application: 2003年 9月26日

出 願 番 号
Application Number: 特願2003-335185

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に用いる優先権の主張の基礎
となる出願の国コードと出願
番号
The country code and number
of your priority application,
to be used for filing abroad
under the Paris Convention, is

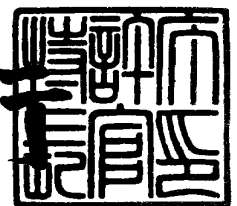
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出 願 人
Applicant(s): パナソニック株式会社

2011年 4月 5日

特許庁長官
Commissioner,
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【発明者】	
【住所又は居所】	大阪府門真市大字門真 1 0 0 6 番地 松下電器産業株式会社内
【氏名】	磯野 俊介
【特許出願人】	
【識別番号】	000005821
【氏名又は名称】	松下電器産業株式会社
【代理人】	
【識別番号】	100077931
【弁理士】	
【氏名又は名称】	前田 弘
【選任した代理人】	
【識別番号】	100094134
【弁理士】	
【氏名又は名称】	小山 廣毅
【選任した代理人】	
【識別番号】	100110939
【弁理士】	
【氏名又は名称】	竹内 宏
【選任した代理人】	
【識別番号】	100113262
【弁理士】	
【氏名又は名称】	竹内 祐二
【選任した代理人】	
【識別番号】	100115059
【弁理士】	
【氏名又は名称】	今江 克実
【選任した代理人】	
【識別番号】	100117710
【弁理士】	
【氏名又は名称】	原田 智雄
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【物件名】	明細書 1
【物件名】	図面 1
【物件名】	要約書 1
【包括委任状番号】	0217869

【書類名】特許請求の範囲

【請求項 1】

半導体基板と、
上記半導体基板の上方に設けられた第 1 の絶縁膜と、
上記第 1 の絶縁膜の少なくとも上部に設けられた配線層と、
上記第 1 の絶縁膜および上記配線層の上に設けられた第 2 の絶縁膜と、
上記第 2 の絶縁膜の上に設けられた第 3 の絶縁膜と、
上記第 3 の絶縁膜および上記第 2 の絶縁膜を貫通し、上記配線層に到達する、少なくとも 1 つのコンタクト導体部とを備える半導体装置であって、
上記配線層の上部には凹部が設けられており、上記第 2 の絶縁膜のうち上記配線層の上に位置する部分の膜厚は、上記第 2 の絶縁膜のうち上記第 1 の絶縁膜の上に位置する部分の膜厚よりも厚い、半導体装置。

【請求項 2】

請求項 1 に記載の半導体装置であって、
上記配線層は、第 1 の配線層であって、
上記コンタクト導体部は、第 1 のコンタクト導体部であって、
上記第 1 の絶縁膜の少なくとも上部に設けられた第 2 の配線層と、
上記第 3 の絶縁膜および上記第 2 の絶縁膜を貫通し、上記第 2 の配線層に到達する第 2 のコンタクト導体部とをさらに備え、
上記第 2 の絶縁膜のうち上記第 1 の配線層の上に位置する部分の膜厚は、上記第 2 の絶縁膜のうち上記第 2 の配線層の上に位置する部分の膜厚よりも厚い、半導体装置。

【請求項 3】

請求項 2 に記載の半導体装置であって、
上記第 1 の配線層の幅は、上記第 2 の配線層の幅より大きい、半導体装置。

【請求項 4】

請求項 2 または 3 に記載の半導体装置であって、
上記第 1 の配線層の側方にはダミー配線層が形成されている、半導体装置。

【請求項 5】

請求項 2 ～ 4 のうちいずれか 1 項に記載の半導体装置であって、
上記第 1 のコンタクト導体部は、矩形あるいは帯状の平面形状を有し、
上記第 2 のコンタクト導体部は、円形あるいは正方形の平面形状を有している、半導体装置。

【請求項 6】

請求項 2 ～ 5 のうちいずれか 1 項に記載の半導体装置であって、
上記第 1 の配線層及び上記第 1 のコンタクト導体部は、リング状に設けられたシールリングである、半導体装置。

【請求項 7】

請求項 1 に記載の半導体装置であって、
上記半導体基板内には素子が設けられており、
上記配線層は、上記素子と電気的に接続されている、半導体装置。

【請求項 8】

請求項 1 ～ 7 のうちいずれか 1 項に記載の半導体装置であって、
上記第 2 の絶縁膜は、炭素を含むシリコン絶縁膜である、半導体装置。

【請求項 9】

半導体基板と、
上記半導体基板の上方に設けられた第 1 の絶縁膜と、
上記第 1 の絶縁膜の少なくとも上部に設けられた配線層と、
上記配線層の上を覆う耐酸化性導体膜と、
上記第 1 の絶縁膜および上記耐酸化性導体膜の上に設けられた第 2 の絶縁膜と、
上記第 2 の絶縁膜の上に設けられた第 3 の絶縁膜と、

上記第3の絶縁膜および上記第2の絶縁膜を貫通し、上記耐酸化性導体膜に到達する、少なくとも1つのコンタクト導体部とを備える、半導体装置。

【請求項10】

請求項9に記載の半導体装置であって、
上記耐酸化性導体膜は、上記配線層の上部領域に窒素が導入された窒素導入層である、半導体装置。

【請求項11】

請求項9に記載の半導体装置であって、
上記耐酸化性導体膜は、チタンナイトライドである、半導体装置。

【請求項12】

請求項9～11のうちいずれか1項に記載の半導体装置であって、
上記配線層は、第1の配線層であって、
上記耐酸化性導体膜は、上記第1の配線層の上に設けられた第1の耐酸化性導体膜であって、
上記コンタクト導体部は、第1のコンタクト導体部であって、
上記第1の絶縁膜の少なくとも上部に設けられた第2の配線層と、
上記第2の配線層の上を覆う第2の耐酸化性導体膜と、
上記第3の絶縁膜および上記第2の絶縁膜を貫通し、上記第2の耐酸化性導体膜に到達する第2のコンタクト導体部とをさらに備え、
上記第1のコンタクト導体部は、上記第2のコンタクト導体部に比べて上面の面積が大きい、半導体装置。

【請求項13】

請求項12に記載の半導体装置であって、
上記第1のコンタクト導体部は、矩形あるいは帯状の平面形状を有し、
上記第2のコンタクト導体部は、円形あるいは正方形の平面形状を有している、半導体装置。

【請求項14】

請求項12または13に記載の半導体装置であって、
上記第1の配線層及び上記第1のコンタクト導体部は、リング状に設けられたシールリングである、半導体装置。

【請求項15】

請求項9～11のうちいずれか1項に記載の半導体装置であって、
上記半導体基板内には素子が設けられており、
上記配線層は、上記素子と電気的に接続されている、半導体装置。

【請求項16】

請求項9～15のうちいずれか1項に記載の半導体装置であって、
上記第2の絶縁膜は、炭素を含むシリコン絶縁膜である、半導体装置。

【請求項17】

半導体基板の上方に、第1の絶縁膜を形成する工程（a）と、
上記第1の絶縁膜の少なくとも上部に、配線層を形成する工程（b）と、
上記配線層の上部に凹部を形成する工程（c）と、
上記第1の絶縁膜および上記配線層の上に、上記凹部を埋める第2の絶縁膜を形成する工程（d）と、
上記第2の絶縁膜の上面を平坦化する工程（e）と、
上記工程（e）の後に、上記第2の絶縁膜の上に第3の絶縁膜を形成する工程（f）と、
上記第3の絶縁膜および上記第2の絶縁膜のうち上記配線層の上方に位置する部分を、フォトリソをマスクにして上記配線層に到達しない深さまで除去し、上記配線層上に上記第2の絶縁膜の一部を残存させる工程（g）と、
上記フォトリソを除去する工程（h）と

を備える、半導体装置の製造方法。

【請求項 18】

請求項 17 に記載の半導体装置の製造方法であって、

上記工程 (c) では、化学的機械研磨、ドライエッチングまたはウエットエッチングによって、上記配線層の上記上部をリセスさせることにより、上記凹部を形成する、半導体装置の製造方法。

【請求項 19】

請求項 17 または 18 に記載の半導体装置の製造方法であって、

上記工程 (b) では、上記配線層として、第 1 の配線層と第 2 の配線層とを形成し、

上記工程 (c) では、少なくとも上記第 1 の配線層の上部に上記凹部を形成し、

上記工程 (g) では、上記第 3 の絶縁膜および上記第 2 の絶縁膜のうち上記第 1 の配線層の上方に位置する部分の一部を除去することによりトレンチパターンを形成し、上記第 3 の絶縁膜および上記第 2 の絶縁膜のうち上記第 2 の配線層の上方に位置する部分の一部を除去することにより、ホールパターンを形成する、半導体装置の製造方法。

【請求項 20】

請求項 19 に記載の半導体装置の製造方法であって、

上記工程 (b) では、上記第 1 の配線層の幅を、上記第 2 の配線層の幅よりも大きく形成する、半導体装置の製造方法。

【請求項 21】

請求項 19 または 20 に記載の半導体装置の製造方法であって、

上記工程 (b) では、上記第 1 の配線層の側方に、ダミー配線層を形成する、半導体装置の製造方法。

【請求項 22】

請求項 17 または 18 に記載の半導体装置の製造方法であって、

上記工程 (a) の前に、上記半導体基板内に素子を形成する工程 (i) をさらに備え、

上記工程 (b) では、上記素子と電気的に接続される上記配線層を形成する、半導体装置の製造方法。

【請求項 23】

半導体基板の上方に、第 1 の絶縁膜を形成する工程 (a) と、

上記第 1 の絶縁膜の少なくとも上部に、配線層を形成する工程 (b) と、

上記配線層の上を覆う耐酸化性導体膜を形成する工程 (c) と、

上記第 1 の絶縁膜および上記耐酸化性導体膜の上に、第 2 の絶縁膜を形成する工程 (d) と、

上記第 2 の絶縁膜の上に、第 3 の絶縁膜を形成する工程 (e) と、

上記第 3 の絶縁膜および上記第 2 の絶縁膜のうち上記配線層の上方に位置する部分を、フォトリソをマスクにして除去する工程 (f) と、

上記フォトリソを除去する工程 (g) と

を備える、半導体装置の製造方法。

【請求項 24】

請求項 23 に記載の半導体装置の製造方法であって、

上記工程 (c) では、上記配線層の上部に、プラズマ処理、ウエット処理またはイオン注入を行って窒素を導入することにより、上記耐酸化性導体膜を形成する、半導体装置の製造方法。

【請求項 25】

請求項 23 に記載の半導体装置の製造方法であって、

上記工程 (c) では、上記耐酸化性導体膜として、窒素を含む膜を上記配線層の上に堆積する、半導体装置の製造方法。

【請求項 26】

請求項 23 ～ 25 のうちいずれか 1 項に記載の半導体装置の製造方法であって、

上記工程 (b) では、上記配線層として、第 1 の配線層と第 2 の配線層とを形成し、

上記工程（c）では、上記第 1 の配線層および上記第 2 の配線層の上に耐酸化性導体膜を形成し、

上記工程（f）では、上記第 3 の絶縁膜および上記第 2 の絶縁膜のうち上記第 1 の配線層の上方に位置する部分を除去することにより、トレンチパターンを形成し、上記第 3 の絶縁膜および上記第 2 の絶縁膜のうち上記第 2 の配線層の上方に位置する部分を除去することにより、ホールパターンを形成する、半導体装置の製造方法。

【請求項 27】

請求項 23～25 のうちいずれか 1 項に記載の半導体装置の製造方法であって、

上記工程（a）の前に、上記半導体基板内に素子を形成する工程（g）をさらに備え、

上記工程（b）では、上記素子と電氣的に接続される上記配線層を形成する、半導体装置の製造方法。

【書類名】明細書

【発明の名称】半導体装置およびその製造方法

【技術分野】

【0001】

本発明は半導体装置とその製造方法に関するものであり、特に、配線層上にコンタクト導体部を有する半導体装置とその製造方法に関するものである。

【背景技術】

【0002】

近年、半導体集積回路の微細化、高集積化が著しく進んでいる。微細化を進めていくにしたがって、トランジスタの動作による遅延時間は短縮できるが、配線抵抗や寄生容量が増加するため、配線遅延時間の短縮は困難になる。配線遅延時間を短縮するための対策として、配線抵抗を低減させるために、従来のアルミニウムに代わる配線の材料として、より抵抗率の低い銅が採用されている。また、寄生容量を低減するために、層間絶縁膜等の材料として低誘電率絶縁膜が採用されている。

【0003】

銅に対してエッチングを行うのは困難である。そのため、銅を用いて配線を形成する際には、象嵌法によって絶縁膜にホールパターンやトレンチパターンを形成した後に銅を埋め込む方法が用いられている。

【0004】

ところで、半導体装置のチップには、チップ内に設けられたトランジスタや配線などを外部の湿気から保護するために、シールリングというトレンチパターンが形成される。シールリングは、トランジスタや配線の周囲を囲むように形成される。シールリングは、ホールパターン（ビア）を形成するためのエッチング時に同時に形成される。

【0005】

ホールパターンおよびシールリングのためのトレンチパターンは、以下の方法により形成される。

【0006】

まず、ホールパターンおよびトレンチパターンを形成するために、フォトリジストをマスクとして、層間絶縁膜を途中の深さまで除去する。ここで、工程を途中で止めるのは、もしこの時点でホールパターンおよびトレンチパターンの下に位置する配線層が露出してしまうと、その後にフォトリジストを除去するアッシングやポリマー除去を行う際に、配線層が腐食するからである。そのため、層間絶縁膜を一部の厚みだけ残した状態でアッシングやポリマー除去を行い、その後に、層間絶縁膜自体をマスクとして、ホールパターンおよびトレンチパターンを配線層に到達させるのである。

【特許文献1】特開2002-118078号公報

【発明の開示】

【発明が解決しようとする課題】

【0007】

しかしながら、従来の半導体装置では、以下のような不具合が生じていた。

【0008】

一般的に、エッチングを行う際のエッチングレートは、開口面積が大きくなるにつれて大きくなる。ここで、トレンチパターンの開口面積は、ホールパターンの開口面積よりも大きい。そのため、トレンチパターンとホールパターンとをエッチングにより同時に形成すると、トレンチパターンの方が深く形成されてしまう。そのため、トレンチパターンの深さを層間絶縁膜の途中までで止めることができず、下に位置する配線層の金属が露出してしまふおそれがある。この段階で金属が露出すると、後にアッシングによるレジスト除去、ポリマー洗浄の工程を経ることによって金属が腐食するという不具合があった。

【0009】

このような不具合は、層間絶縁膜に複数のホールパターンを形成する際にも生じる。つまり、各ホールパターンのパターン密度などが異なることから、ホールパターンを形成す

る際には均一な深さで絶縁膜を除去することができない。そのため、ホールパターンの下に位置する配線層が露出するという不具合が起こってしまう。

【0010】

本発明の目的は、ホールパターンやトレンチパターンを形成する際に、配線層を露出させないための手段を講ずることにより、配線層における金属の腐食の起こりにくい半導体装置の製造方法を提供することにある。

【課題を解決するための手段】

【0011】

本発明の第1の半導体装置は、半導体基板と、上記半導体基板の上方に設けられた第1の絶縁膜と、上記第1の絶縁膜の少なくとも上部に設けられた配線層と、上記第1の絶縁膜および上記配線層の上に設けられた第2の絶縁膜と、上記第2の絶縁膜の上に設けられた第3の絶縁膜と、上記第3の絶縁膜および上記第2の絶縁膜を貫通し、上記配線層に到達する、少なくとも1つのコンタクト導体部とを備える半導体装置であって、上記配線層の上部には凹部が設けられており、上記第2の絶縁膜のうち上記配線層の上に位置する部分の膜厚は、上記第2の絶縁膜のうち上記第1の絶縁膜の上に位置する部分の膜厚よりも厚い。

【0012】

このように、第2の絶縁膜のうち配線層の上に位置する部分が厚く形成されているので、コンタクト導体部を形成するために第3の絶縁膜と第2の絶縁膜とを除去する工程において、配線層上に第2の絶縁膜の一部を残存させることが容易となり、配線層が露出しにくくなる。この状態で、アッシングやポリマー除去等の金属を腐食させるおそれのある処理を行い、その後に、第3の絶縁膜と第2の絶縁膜とをさらに除去して配線層を露出させ、コンタクト導体部用の導体を埋めることができる。つまり、配線層が露出しにくい状態で金属を腐食させるおそれのある処理を行うことができるので、配線層の腐食を防止することができる。

【0013】

一方、第2の絶縁膜のうち配線層の上に位置する部分以外の膜厚は厚くならないので、層間の誘電率を一定に保つことができる。

【0014】

上記配線層は、第1の配線層であって、上記コンタクト導体部は、第1のコンタクト導体部であって、上記第1の絶縁膜の少なくとも上部に設けられた第2の配線層と、上記第3の絶縁膜および上記第2の絶縁膜を貫通し、上記第2の配線層に到達する第2のコンタクト導体部とをさらに備え、上記第2の絶縁膜のうち上記第1の配線層の上に位置する部分の膜厚は、上記第2の絶縁膜のうち上記第2の配線層の上に位置する部分の膜厚よりも厚くてもよい。この場合には、コンタクト導体部を形成するために第3の絶縁膜および第2の絶縁膜を除去しても、第2の絶縁膜のうち第1のコンタクト導体部が形成される領域は厚く形成されているので、第1の配線層を露出しにくくすることができる。したがって、第1のコンタクト導体部の形成される面積が第2のコンタクト導体部よりも大きいときのように、コンタクト導体部を形成するために第3の絶縁膜および第2の絶縁膜を除去すると第1のコンタクト導体部の形成される領域の方が深く除去されてしまう場合であっても、第1の配線層を露出しにくくすることができる。

【0015】

上記第1の配線層の幅は、上記第2の配線層の幅より大きく形成してもよい。この場合には、第1の配線層の形成される領域のほうが、第2の配線層の形成される領域よりも、導体（金属）の占める割合が大きくなる。したがって、第1の配線層および第2の配線層の上方から化学的機械研磨等の処理を行うと、ディッシングの金属占有率依存性により、第1の配線層の上部に形成される凹部の深さを深くすることができる。

【0016】

上記第1の配線層の側方にはダミー配線層が形成されていてもよい。この場合には、第1の配線層の形成される領域の周囲のほうが、第2の配線層の形成される領域の周囲より

も、導体（金属）の占める割合が大きくなる。したがって、第1の配線層および第2の配線層の上方から化学的機械研磨等の処理を行うと、ディッシングの金属占有率依存性により、第1の配線層の上部に形成される凹部の深さを深くすることができる。

【0017】

上記第1のコンタクト導体部は、矩形あるいは帯状の平面形状を有し、上記第2のコンタクト導体部は、円形あるいは正方形の平面形状を有していてもよい。

【0018】

上記第1の配線層及び上記第1のコンタクト導体部は、リング状に設けられたシールリングであってもよい。この場合には、シールリングである第1のコンタクト導体部と第2のコンタクト導体部とは面積が大きく相違するが、上述の構造を有することにより、第1の配線層が露出するのを防止することができる。

【0019】

上記半導体基板内には素子が設けられており、上記配線層は、上記素子と電気的に接続されていてもよい。この場合には、配線層を形成する際に第3の絶縁膜および第2の絶縁膜を除去する際に、除去する深さに誤差が生じても、配線層を露出しにくくすることができる。

【0020】

上記第2の絶縁膜は、炭素を含むシリコン絶縁膜であることが好ましい。

【0021】

本発明の第2の半導体装置は、半導体基板と、上記半導体基板の上方に設けられた第1の絶縁膜と、上記第1の絶縁膜の少なくとも上部に設けられた配線層と、上記配線層の上を覆う耐酸化性導体膜と、上記第1の絶縁膜および上記耐酸化性導体膜の上に設けられた第2の絶縁膜と、上記第2の絶縁膜の上に設けられた第3の絶縁膜と、上記第3の絶縁膜および上記第2の絶縁膜を貫通し、上記耐酸化性導体膜に到達する、少なくとも1つのコンタクト導体部とを備える。

【0022】

これにより、コンタクト導体部を形成するために第3の絶縁膜と第2の絶縁膜とを除去する工程において、耐酸化性導体膜が露出した状態で、アッシングやポリマー除去等の金属を腐食させるおそれのある処理を行った場合にも、配線層の腐食を防止することができる。一方、第2の絶縁膜のうち配線層の上に位置する部分以外の膜厚は厚くならないので、層間の誘電率を一定に保つことができる。

【0023】

上記耐酸化性導体膜は、上記配線層の上部領域に窒素が導入された窒素導入層であってもよい。

【0024】

上記耐酸化性導体膜は、チタンナイトライドであってもよい。

【0025】

上記配線層は、第1の配線層であって、上記耐酸化性導体膜は、上記第1の配線層の上に設けられた第1の耐酸化性導体膜であって、上記コンタクト導体部は、第1のコンタクト導体部であって、上記第1の絶縁膜の少なくとも上部に設けられた第2の配線層と、上記第2の配線層の上を覆う第2の耐酸化性導体膜と、上記第3の絶縁膜および上記第2の絶縁膜を貫通し、上記第2の耐酸化性導体膜に到達する第2のコンタクト導体部とをさらに備え、上記第1のコンタクト導体部は、上記第2のコンタクト導体部に比べて上面の面積が大きい。この場合には、これらのコンタクト導体部を形成する際に第3の絶縁膜および第2の絶縁膜を除去すると、第1のコンタクト導体部の形成される領域の方が深く除去されてしまう。しかし、第1の配線層の上は耐酸化性膜によって覆われているので、たとえ耐酸化性膜が露出しても、第1の配線層の腐食を防止することができる。

【0026】

上記第1のコンタクト導体部は、矩形あるいは帯状の平面形状を有し、上記第2のコンタクト導体部は、円形あるいは正方形の平面形状を有していてもよい。

【0027】

上記第1の配線層及び上記第1のコンタクト導体部は、リング状に設けられたシールリングであってもよい。この場合には、シールリングである第1のコンタクト導体部と第2のコンタクト導体部とは面積が大きく相違するが、上述の構造を有することにより、第1の配線層が露出するのを防止することができる。

【0028】

上記半導体基板内には素子が設けられており、上記配線層は、上記素子と電気的に接続されていてもよい。この場合には、配線層を形成する際に第3の絶縁膜および第2の絶縁膜を除去する際に、除去する深さに誤差が生じて、配線層を腐食しにくくすることができる。

【0029】

上記第2の絶縁膜は、炭素を含むシリコン絶縁膜であることが好ましい。

【0030】

本発明の第1の半導体装置の製造方法は、半導体基板の上方に、第1の絶縁膜を形成する工程(a)と、上記第1の絶縁膜の少なくとも上部に、配線層を形成する工程(b)と、上記配線層の上部に凹部を形成する工程(c)と、上記第1の絶縁膜および上記配線層の上に、上記凹部を埋める第2の絶縁膜を形成する工程(d)と、上記第2の絶縁膜の上面を平坦化する工程(e)と、上記工程(e)の後に、上記第2の絶縁膜の上に第3の絶縁膜を形成する工程(f)と、上記第3の絶縁膜および上記第2の絶縁膜のうち上記配線層の上方に位置する部分を、フォトリソをマスクにして上記配線層に到達しない深さまで除去し、上記配線層上に上記第2の絶縁膜の一部を残存させる工程(g)と、上記フォトリソを除去する工程(h)とを備える。

【0031】

これにより、第2の絶縁膜のうち配線層の上に位置する部分を厚く形成することができるので、工程(g)において、より確実に、配線層を露出しない状態に保つことができる。したがって、工程(g)の後に、アッシング等の金属を腐食するおそれのある処理を行っても、配線層が腐食するのを防止することができる。一方、第2の絶縁膜のうち配線層の上に位置する部分以外の膜厚は厚くならないので、この方法により製造した半導体装置においては、層間の誘電率を一定に保つことができる。

【0032】

上記工程(c)では、化学的機械研磨、ドライエッチングまたはウェットエッチングによって、上記配線層の上部をリセスさせることにより、上記凹部を形成してもよい。なお、この場合には、上述の効果に加えて、第1の絶縁膜と第2の絶縁膜との密着性を向上させることができるという効果を得ることができる。

【0033】

上記工程(b)では、上記配線層として、シールリング用の第1の配線層と、上記第1の配線層に囲まれる領域内に位置する第2の配線層とを形成し、上記工程(c)では、少なくとも上記第1の配線層の上部に上記凹部を形成し、上記工程(g)では、上記第3の絶縁膜および上記第2の絶縁膜のうち上記第1の配線層の上方に位置する部分の一部を除去することにより、シールリング用のトレンチパターンを形成し、上記第3の絶縁膜および上記第2の絶縁膜のうち上記第2の配線層の上方に位置する部分の一部を除去することにより、ホールパターンを形成してもよい。この場合には、トレンチパターンの開口面積は、ホールパターンの開口面積よりも広いので、工程(g)では、ホールパターンよりもトレンチパターンの方が深く形成されてしまう。しかし、第2の絶縁膜のうちトレンチパターンが形成される領域は厚く形成されているので、第1の配線層を露出しにくくすることができる。

【0034】

上記工程(b)では、上記第1の配線層の幅を、上記第2の配線層の幅よりも大きく形成してもよい。この場合には、第1の配線層の形成される領域のほうが、第2の配線層の形成される領域よりも、導体(金属)の占める割合が大きくなる。したがって、工程(c)

）において、第1の配線層および第2の配線層の上方から化学的機械研磨等の処理を行うと、ディッシングの金属占有率依存性により、第1の配線層の上部に形成される凹部の深さを深くすることができる。

【0035】

上記工程（b）では、上記第1の配線層の側方に、ダミー配線層を形成してもよい。この場合には、第1の配線層の形成される領域の周囲のほうが、第2の配線層の形成される領域の周囲よりも、導体（金属）の占める割合が大きくなる。したがって、工程（c）において、第1の配線層および第2の配線層の上方から化学的機械研磨等の処理を行うと、ディッシングの金属占有率依存性により、第1の配線層の上部に形成される凹部の深さを深くすることができる。

【0036】

上記工程（a）の前に、上記半導体基板内に素子を形成する工程（h）をさらに備え、上記工程（b）では、上記素子と電氣的に接続される上記配線層を形成してもよい。この場合には、工程（g）において、除去する深さに誤差が生じても、配線層を露出しにくくすることができる。

【0037】

本発明の第2の半導体装置の製造方法は、半導体基板の上方に、第1の絶縁膜を形成する工程（a）と、上記第1の絶縁膜の少なくとも上部に、配線層を形成する工程（b）と、上記配線層の上を覆う耐酸化性導体膜を形成する工程（c）と、上記第1の絶縁膜および上記耐酸化性導体膜の上に、第2の絶縁膜を形成する工程（d）と、上記第2の絶縁膜の上に、第3の絶縁膜を形成する工程（e）と、上記第3の絶縁膜および上記第2の絶縁膜のうち上記配線層の上方に位置する部分を、フォトレジストをマスクにして除去する工程（f）と、上記フォトレジストを除去する工程（g）とを備える。

【0038】

これにより、配線層の上を耐酸化性導体膜で覆うことができるので、工程（f）において、耐酸化性導体膜が露出させた後に、アッシング等の金属を腐食するおそれのある処理を行っても、配線層が腐食するのを防止することができる。一方、第2の絶縁膜のうち配線層の上に位置する部分以外の膜厚は厚くならないので、この方法により製造した半導体装置においては、層間の誘電率を一定に保つことができる。

【0039】

上記工程（c）では、上記配線層の上部に、プラズマ処理、ウエット処理またはイオン注入を行って窒素を導入することにより、上記耐酸化性導体膜を形成してもよい。

【0040】

上記工程（c）では、上記耐酸化性導体膜として、窒素を含む膜を上記配線層の上に堆積してもよい。

【0041】

上記工程（b）では、上記配線層として、シールリング用の第1の配線層と、上記第1の配線層に囲まれる領域内に位置する第2の配線層とを形成し、上記工程（c）では、上記第1の配線層および上記第2の配線層の上に耐酸化性導体膜を形成し、上記工程（f）では、上記第3の絶縁膜および上記第2の絶縁膜のうち上記第1の配線層の上方に位置する部分の一部を除去することにより、シールリング用のトレンチパターンを形成し、上記第3の絶縁膜および上記第2の絶縁膜のうち上記第2の配線層の上方に位置する部分の一部を除去することにより、ホールパターンを形成してもよい。この場合には、トレンチパターンの開口面積は、ホールパターンの開口面積よりも広いので、工程（f）では、ホールパターンよりもトレンチパターンの方が深く形成されてしまう。しかし、第2の絶縁膜のうちトレンチパターンが形成される領域は厚く形成されているので、第1の配線層を露出しにくくすることができる。

【0042】

上記工程（a）の前に、上記半導体基板内に素子を形成する工程（g）をさらに備え、上記工程（b）では、上記素子と電氣的に接続される上記配線層を形成してもよい。この

場合には、工程（f）において、除去する深さに誤差が生じても、配線層を露出しにくくすることができる。

【発明の効果】

【0043】

本発明の半導体装置およびその製造方法においては、配線層の腐食を防止することができる。

【発明を実施するための最良の形態】

【0044】

（第1の実施形態）

以下に、本発明の第1の実施形態に係る半導体装置の製造方法について、図1（a）～（f）を参照しながら説明する。図1（a）～（f）は、第1の実施形態の半導体装置の製造方法を示す断面図である。なお、図1（a）～（f）には、配線形成領域R1と、配線形成領域R1を外部の湿気から保護するためのシールリング領域R2とを示している。シールリング領域R2は配線形成領域R1の側方を囲んでいる。

【0045】

まず、図1（a）に示す工程で、シリコン基板（図示せず）上にシリコン酸化膜からなる、厚さ500nmの第1の絶縁膜101を形成する。そして、第1の絶縁膜101の上に、フォトリソグラフィにより、配線パターン形成位置に開口を有するフォトレジスト（図示せず）を形成する。そのフォトレジストをマスクとしてドライエッチングを行うことにより、第1の絶縁膜101の一部を除去して、深さ250nmの配線溝108、109を形成する。その後、フォトレジストを除去した後、基板上に、タンタルナイトライドとタンタルとからなる厚さ30nmの積層膜（図示せず）と、厚さ1000nmの銅膜（図示せず）とを形成する。その後、化学的機械研磨法を用いて銅膜と積層膜とを研磨することにより、配線形成領域R1に、配線溝108の内表面を覆う表面導体膜102aと、表面導体膜102aを介して配線溝108を埋める金属配線膜102bとからなる第1の金属配線102を形成する。このとき、シールリング領域R2には、表面導体膜103aと金属配線膜103bとからなる第2の金属配線103を形成する。

【0046】

次に、図1（b）に示す工程で、化学的機械研磨法か、または硝酸などを用いた金属の選択的なエッチングによって、第1の金属配線102および第2の金属配線103の上部をリセスさせることにより、深さ20nm～40nm程度のリセス形状（凹部110）を形成する。

【0047】

次に、図1（c）に示す工程で、基板上に、凹部110を埋め、厚さ100nm～150nmのシリコン窒化炭化膜からなる第2の絶縁膜104を堆積する。このとき、第2の絶縁膜104の材料としては、シリコン窒化膜、シリコン炭化膜、シリコン酸化炭化膜などを用いてもよい。また、これらの膜の積層体を形成してもよい。

【0048】

この時点では、第1の金属配線102および第2の金属配線103のリセス形状を反映して、第2の絶縁膜104の上面には段差が形成されている。

【0049】

次に、図1（d）に示す工程で、化学的機械研磨、硫酸や硝酸などを用いたウェットエッチング、またはエッチバックを行うことにより、第2の絶縁膜104の上面の平坦化を行う。これにより、第2の絶縁膜104のうち第1の金属配線102および第2の金属配線103の上に位置する部分の膜厚は70nm～90nm程度になり、それ以外の部分の厚さは50nmになる。

【0050】

次に、図1（e）に示す工程で、基板上に、炭素含有シリコン酸化膜からなる第3の絶縁膜105を堆積する。このとき、第3の絶縁膜105としては、FSG（Fluorinated Silicate Glass）膜、BPSG（Boron Phospho Silicate Glass）膜または多孔質膜を用

いてもよい。また、これらの膜の積層膜を用いてもよい。

【0051】

その後、フォトリソグラフィによって、第3の絶縁膜105の上に、ホールパターン形成領域およびトレンチパターン形成領域に開口を有するフォトレジスト（図示せず）を形成する。その後、フォトレジストをマスクとしてドライエッチングを行うことにより、配線形成領域R1にはホールパターン（スルーホール）106を形成し、シールリング領域R2にはトレンチパターン107を形成する。このドライエッチングは、ホールパターン106およびトレンチパターン107が第2の絶縁膜104の途中の深さになるまで行う。このとき、トレンチパターン107の開口面積はホールパターン106の開口面積よりも広いので、トレンチパターン107の方が深く除去される。その後、アッシングによりフォトレジストを除去し、ウエットエッチング時およびドライエッチング時のポリマーを除去する。

【0052】

次に、図1（f）に示す工程で、パターン内に残存する第2の絶縁膜104をエッチングしてホールパターン106とトレンチパターン107とを第1の金属配線102および第2の金属配線103に到達させ、それを導体で埋めることにより、平面形状が円形あるいは正方形のホールコンタクト導体部106'、および、リング状のトレンチコンタクト導体部107'を形成する。なお、この工程は、アッシング、ポリマー除去等の金属を腐食させるおそれのある処理を終了した後に行う。

【0053】

次に、本実施形態の半導体装置のうち配線およびシールリングの構造について、図1（f）を再度参照しながら説明する。

【0054】

図1（f）に示すように、本実施形態の半導体装置は、配線形成領域R1と、配線形成領域R1の側方を囲むシールリング領域R2とを有している。そして、配線形成領域R1には第1の金属配線102が設けられ、シールリング領域R2には第2の金属配線103が設けられている。第1の金属配線102は、配線溝108の表面を覆う表面導体膜102aと、その上を覆う金属配線膜102bとを有している。第2の金属配線103も、配線溝109の表面を覆う表面導体膜103aと、その上に設けられた金属配線膜103bとを有している。第1の金属配線102および第2の金属配線103の上部はリセスされており、凹部110が形成されている。

【0055】

第1の絶縁膜101、第1の金属配線102および第2の金属配線103の上には、第2の絶縁膜104が設けられている。第2の絶縁膜104は凹部110を埋めているので、第2の絶縁膜104は、第1の金属配線102および第2の金属配線103の上に位置する部分が他の部分よりも厚く形成されている。第2の絶縁膜104の上面は平坦化されている。

【0056】

第2の絶縁膜104の上には第3の絶縁膜105が設けられている。そして、配線形成領域R1には、第3の絶縁膜105と第2の絶縁膜104とを貫通するホールコンタクト導体部106'が設けられている。同様に、シールリング領域R2には、トレンチコンタクト導体部107'が形成されている。従って、シールリング領域R2には、配線形成領域R1の第1の金属配線102およびホールコンタクト導体部106'を取り囲むように、第2の金属配線103及びトレンチコンタクト導体部107'からなるリング状のシールリングが設けられる。

【0057】

以下に、本実施形態で得られる効果について、従来と比較しながら説明する。

【0058】

従来では、第1の金属配線および第2の金属配線の上面は平坦なままであり、第1の金属配線および第2の金属配線の上には、均一な厚さの第2の絶縁膜が形成されていた。そ

のため、ホールパターンおよびトレンチパターンを形成すると、トレンチパターンが第2の絶縁膜を貫通してしまい、第2の金属配線を露出させてしまうおそれがあった。

【0059】

これに対し、本実施形態では、第2の絶縁膜104のうち第1の金属配線102および第2の金属配線103の上に位置する部分のみを厚く形成することができる。そのため、トレンチパターン107が第2の金属配線103に到達するのを防止することができる。そのため、アッシングやポリマー洗浄を行っても、第1の金属配線102の腐食が起らない。ここで、第2の絶縁膜104のうち第1の絶縁膜101の上に位置する部分は厚くならないため、層間の誘電率を一定に保つことができる。

【0060】

さらに、第1の金属配線102および第2の金属配線103の上部をリセスさせるために化学的機械研磨法あるいは選択エッチングを行うことにより、第1の絶縁膜101と第2の絶縁膜104との密着性を向上させることができる。

【0061】

なお、本実施形態では、化学的機械研磨法等により、第1の金属配線102および第2の金属配線103の上部にリセス形状を形成した。しかし、本発明では、熱を加えると圧縮するという銅の性質を利用して、リセス形状を形成してもよい。具体的には、図1(a)に示す工程で、第1の金属配線102および第2の金属配線103を形成した後に、200度～500度の熱処理を行う。これにより、銅からなる金属配線膜102b、103bが圧縮して、第1の金属配線102および第2の金属配線103の上部にリセスが形成される。この方法によっても、上述した効果と同様の効果を得ることができる。

【0062】

(第2の実施形態)

以下に、本発明の第2の実施形態に係る半導体装置の製造方法について、図2(a)～(f)を参照しながら説明する。図2(a)～(f)は、第2の実施形態の半導体装置の製造方法を示す断面図である。なお、図2(a)～(f)には、配線形成領域R1と、配線形成領域R1を外部の湿気から保護するためのシールリング領域R2とを示している。シールリング領域R2は配線形成領域R1の側方を囲んでいる。

【0063】

まず、図2(a)に示す工程で、シリコン基板(図示せず)上にシリコン酸化膜からなる、厚さ500nmの第1の絶縁膜111を形成する。そして、第1の絶縁膜111の上に、フォトリソグラフィ法により、金属配線パターン形成領域に開口を有するフォトレジスト(図示せず)を形成する。そのフォトレジストをマスクとしてドライエッチングを行うことにより、配線形成領域R1には配線溝118を形成し、シールリング形成領域R2には配線溝119を形成する。このとき、配線溝119の幅を配線溝118の幅よりも広くする。具体的には、配線溝118の幅が2μmより小さい場合に、配線溝119の幅を2μm以上とする。

【0064】

その後、フォトレジストを除去した後、基板上に、タンタルナイトライドとタンタルとからなる厚さ30nmの積層膜(図示せず)と、厚さ1000nmの銅膜(図示せず)とを形成する。その後、化学的機械研磨法を用いて銅と積層膜とを研磨することにより、配線形成領域R1に、配線溝118の内表面を覆う表面導体膜112aと、表面導体膜112aを介して配線溝118を埋める金属配線膜112bとからなる、幅が2μm以上の第1の金属配線112を形成する。このとき、シールリング領域R2には、表面導体膜113aと金属配線膜113bとからなる、幅が2μm以上の第2の金属配線113を形成する。

【0065】

次に、図2(b)に示す工程で、化学的機械研磨法を行う。このとき、ディッシングの金属占有率依存性を利用して、第2の金属配線113の上部をリセスさせる。以下に詳細に説明する。金属が埋め込まれた基板に対して化学的機械研磨法を行うと、金属が除去さ

れる深さは、その領域のうち金属の占める割合が高くなるにつれて深くなる性質がある。本実施形態では、第2の金属配線113の幅が、第1の金属配線112の幅よりも広く形成されている。言い換えると、単位面積あたりに占める金属の割合は第2の金属配線113の形成された領域の方が高い。そのため、第2の金属配線133の上部が、他の領域よりも深くリセスされるのである。

【0066】

なお、第2の金属配線113の幅を第1の金属配線112よりも広くする方法のかわりに、第2の金属配線113の周りにダミーパターンを形成することによって単位面積あたりの金属の占有率を上げてよい。

【0067】

次に、図2(c)に示す工程で、第1の絶縁膜111、第1の金属配線112および第2の金属配線113の上にシリコン窒化炭化膜からなる第2の絶縁膜114を堆積する。このとき、第2の絶縁膜114の材料としては、シリコン窒化膜、シリコン酸化膜、シリコン酸化炭化膜などを用いてもよい。また、これらの膜の積層体を形成してもよい。

【0068】

この時点では、第2の金属配線113のリセス形状を反映して、第2の絶縁膜114の上には段差が形成されている。

【0069】

次に、図2(d)に示す工程で、化学的機械研磨、ウエットエッチングまたはエッチバックを行うことにより、第2の絶縁膜114の平坦化を行う。

【0070】

次に、図2(e)に示す工程で、基板上に、炭素含有シリコン酸化膜からなる第3の絶縁膜115を堆積する。このとき、第3の絶縁膜115としては、FSG(Fluorinated Silicate Glass)膜、BPSG(Boron Phospho Silicate Glass)膜または多孔質膜を用いてもよい。また、これらの膜の積層膜を用いてもよい。

【0071】

その後、フォトリソグラフィによって、第3の絶縁膜115の上に、ホールパターン形成領域およびトレンチパターン形成領域に開口を有するフォトレジスト(図示せず)を形成する。その後、フォトレジストをマスクとしてドライエッチングを行うことにより、配線形成領域R1にはホールパターン116を形成し、シールリング領域R2にはトレンチパターン117を形成する。このドライエッチングは、トレンチパターン117が第2の絶縁膜114の途中の深さになるまで行う。このとき、トレンチパターン117の開口面積はホールパターン116の開口面積よりも広いので、トレンチパターン117のほうが深く除去される。その後、アッシングによりフォトレジストを除去し、ウエットエッチング時およびドライエッチング時のポリマーを除去する。

【0072】

次に、図2(f)に示す工程で、パターン内に残存する第2の絶縁膜114を除去してホールパターン116とトレンチパターン117とを第1の金属配線112および第2の金属配線113に到達させて、それを導体で埋めることにより、平面形状が円形あるいは正方形のホールコンタクト導体部116'、および、リング状のトレンチコンタクト導体部117'を形成する。なお、この工程は、アッシング、ポリマー除去等の金属を腐食させるおそれのある処理を終了した後に行う。

【0073】

次に、本実施形態の半導体装置のうち配線およびシールリングの構造について、図2(f)を再度参照しながら説明する。

【0074】

図2(f)に示すように、本実施形態の半導体装置は、配線形成領域R1と、配線形成領域R1の側方を囲むシールリング領域R2とを有している。そして、配線形成領域R1には第1の金属配線112が設けられ、シールリング領域R2には第2の金属配線113が設けられている。ここで、第2の金属配線113の幅は、第1の金属配線112の幅よ

りも広く設けられている。

【0075】

第1の金属配線112は、配線溝118の表面を覆う表面導体膜112aと、その上を覆う金属配線膜112bとを有している。第2の金属配線113も、配線溝119の表面を覆う表面導体膜113aと、その上に設けられた金属配線膜113bとを有している。第2の金属配線113の上部はリセスされており、凹部120が形成されている。

【0076】

第1の絶縁膜111、第1の金属配線112および第2の金属配線113の上には、第2の絶縁膜114が設けられている。第2の絶縁膜114は凹部120を埋めているので、第2の絶縁膜114は、第2の金属配線113の上に位置する部分が他の部分よりも厚く形成されている。第2の絶縁膜114の上面は平坦化されている。

【0077】

第2の絶縁膜114の上には第3の絶縁膜115が設けられている。そして、配線形成領域R1には、第3の絶縁膜115と第2の絶縁膜114と貫通するホールコンタクト導体部116'が設けられている。同様に、シールリング領域R2には、トレンチコンタクト導体部117'が形成されている。従って、シールリング領域R2には、配線形成領域R1の第1の金属配線112およびホールコンタクト導体部116'を取り囲むように、第2の金属配線113及びトレンチコンタクト導体部117'からなるリング状のシールリングが設けられる。

【0078】

以下に、本実施形態で得られる効果について、従来と比較しながら説明する。

【0079】

従来では、第2の金属配線の上面は平坦なままであり、第2の金属配線の上には、均一な厚さの第2の絶縁膜が形成されていた。そのため、ホールパターンおよびトレンチパターンを形成すると、トレンチパターンが第2の絶縁膜を貫通してしまい、第2の金属配線を露出させてしまうおそれがあった。

【0080】

これに対し、本実施形態では、工程数が増加することなく、第2の絶縁膜114のうち第2の金属配線113の上に位置する部分のみを厚く形成することができる。そのため、トレンチパターン117が第2の金属配線113に到達するのを防止することができる。そのため、アッシングやポリマー洗浄を行っても、第1の金属配線の腐食が起らない。ここで、第2の絶縁膜114のうち第1の絶縁膜111の上に位置する部分は厚くならないため、層間の誘電率を一定に保つことができる。

【0081】

さらに、第2の金属配線113の上部をリセスさせるために化学的機械研磨法あるいはエッチングを行うことにより、第1の絶縁膜111と第2の絶縁膜114との密着性を向上させることができる。

【0082】

なお、本実施形態では、ディッシングの金属占有率依存性を利用してリセス形状を形成したが、パターン密度依存性を利用してエッチングにより形成してもよい。あるいは、本発明の図2(b)に示す工程において、第2の金属配線113を除く領域の上をフォトリジスト等で覆った状態でエッチングを行うことにより、第2の金属配線113の上部にリセス形状を形成してもよい。この場合には、工程数が増加するという点を除いて、上述した効果と同様の効果を得ることができる。

【0083】

また、本実施形態では、図2(b)に示す工程で化学的機械研磨を行う際に、例えば過酸化水素などの溶解性の強いスラリーを用いてもよい。これにより、金属の研磨レートが上昇するので、第2の金属配線113をより深くリセスさせることができる。

【0084】

(第3の実施形態)

本発明の第3の実施形態に係る半導体装置の製造方法について、図3(a)～(e)を参照しながら説明する。図3(a)～(e)は、第3の実施形態の半導体装置の製造工程を示す断面図である。なお、図3(a)～(e)には、配線形成領域R1と、配線形成領域R1を外部の湿気から保護するためのシールリング領域R2とを示している。なお、シールリング領域R2は配線形成領域R1の側方を囲んでいる。

【0085】

まず、図3(a)に示す工程で、シリコン基板(図示せず)上にシリコン酸化膜からなる、厚さ500nmの第1の絶縁膜121を形成する。そして、第1の絶縁膜121の上に、フォトリソグラフィにより、金属配線パターン形成領域に開口を有するフォトレジスト(図示せず)を形成する。そのフォトレジストをマスクとしてドライエッチングを行うことにより、第1の絶縁膜121の一部を除去して、深さ250nmの配線溝128、129を形成する。その後、フォトレジストを除去した後、基板上に、タンタルナイトライドとタンタルとからなる厚さ30nmの積層膜(図示せず)と、厚さ1000nmの銅膜(図示せず)とを形成する。その後、化学的機械研磨法を用いて銅膜と積層膜とを研磨することにより、配線形成領域R1に、配線溝128の内表面を覆う表面導体膜122aと、表面導体膜122aを介して配線溝128を埋める金属配線膜122bとからなる第1の金属配線122を形成する。このとき、シールリング領域R2には、表面導体膜123aと金属配線膜123bとからなる第2の金属配線123を形成する。

【0086】

つぎに、図3(b)に示す工程で、窒素を含むガスを用いたプラズマ処理、アンモニア、ベンゾトリアゾール(BTA)またはキナルジン酸を用いたウエット処理、またはイオン注入を行うことによって、第1の金属配線122および第2の金属配線123の上部に窒素を供給する。これにより、第1の金属配線122および第2の金属配線123の上部が耐酸化性膜130に変質する。このとき同時に、第1の絶縁膜121と後工程で形成する第2の絶縁膜124との密着性を向上させることができる。

【0087】

次に、図3(c)に示す工程で、第1の絶縁膜121および耐酸化性膜130の上に、シリコン窒化炭化膜からなる第2の絶縁膜124を堆積する。このとき、第2の絶縁膜124の材料としては、シリコン窒化膜、シリコン炭化膜、シリコン酸化炭化膜などを用いてもよい。また、これらの膜の積層体を形成してもよい。

【0088】

次に、図3(d)に示す工程で、基板上に、炭素含有シリコン酸化膜からなる第3の絶縁膜125を堆積する。このとき、第3の絶縁膜125としては、FSG(Fluorinated Silicate Glass)膜、BPSG(Boron Phospho Silicate Glass)膜または多孔質膜を用いてもよい。また、これらの膜の積層膜を用いてもよい。

【0089】

その後、フォトリソグラフィによって、第3の絶縁膜125の上に、ホールパターン形成領域およびトレンチパターン形成領域に開口を有するフォトレジスト(図示せず)を形成する。その後、フォトレジストをマスクとしてドライエッチングを行うことにより、配線形成領域R1にはホールパターン126を形成し、シールリング領域R2にはトレンチパターン127を形成する。このドライエッチングは、トレンチパターン127が第2の絶縁膜124の途中で止まってもよいし、第2の絶縁膜124を貫通して、耐酸化性膜130に到達してもよい。その後、アッシングによりフォトレジストを除去し、ウエットエッチング時およびドライエッチング時のポリマーを除去する。

【0090】

次に、図3(e)に示す工程で、パターン内に残存している第2の絶縁膜124を除去してホールパターン126とトレンチパターン127とを耐酸化性膜130に到達させて、トレンチを導体で埋めることにより、平面形状が円形あるいは正方形のホールコンタクト導体部126'、および、リング状のトレンチコンタクト導体部127'を形成する。

【0091】

次に、本実施形態の半導体装置のうち配線およびシールリングの構造について、図3（e）を再度参照しながら説明する。

【0092】

図3（e）に示すように、本実施形態の半導体装置は、配線形成領域R1と、配線形成領域R1の側方を囲むシールリング領域R2とを有している。そして、配線形成領域R1には第1の金属配線122が設けられ、シールリング領域R2には第2の金属配線123が設けられている。第1の金属配線122は、配線溝128の表面を覆う表面導体膜122aと、その上を覆う金属配線膜122bとを有している。第2の金属配線123も、配線溝129の表面を覆う表面導体膜123aと、その上に設けられた金属配線膜123bとを有している。金属配線膜122b、123bの上部には窒素が含まれており、耐酸化性膜130が形成されている。

【0093】

第1の絶縁膜121、第1の金属配線122および第2の金属配線123の上には、第2の絶縁膜124が設けられている。第2の絶縁膜124の上には第3の絶縁膜125が設けられている。そして、配線形成領域R1には、第3の絶縁膜125と、第2の絶縁膜124とを貫通するホールコンタクト導体部126'が設けられている。同様に、シールリング領域R2には、トレンチコンタクト導体部127'が形成されている。従って、シールリング領域R2には、配線形成領域R1の第1の金属配線122およびホールコンタクト導体部126'を取り囲むように、第2の金属配線123及びトレンチコンタクト導体部127'からなるリング状のシールリングが設けられる。

【0094】

以下に、本実施形態で得られる効果について、従来と比較しながら説明する。

【0095】

従来では、ホールパターンおよびトレンチパターンを形成する際にトレンチパターンが第2の金属配線に到達すると、その後のアッシングやポリマー除去の工程において、第2の金属配線が腐食してしまっていた。

【0096】

これに対し、本実施形態では、第2の金属配線123の上部が耐酸化性膜130に変化している。そのため、トレンチパターン127が第2の金属配線123に到達している状態でアッシングやポリマー除去の工程を行っても、第2の金属配線123の上部が腐食されることはない。ここで、第2の絶縁膜124のうち第1の絶縁膜121の上に位置する部分は厚くならないため、層間の誘電率を一定に保つことができる。

【0097】

また、第1の金属配線122および第2の金属配線123の上部に窒素を含有させることにより、ホールパターン126およびトレンチパターン127を形成するときのエッチング耐性が向上するという利点もある。

【0098】

また、図3（d）に示す工程で、ホールパターン126およびトレンチパターン127を耐酸化性膜130に到達させた場合には、後に、ホールパターン126やトレンチパターン127と耐酸化性膜130との間に残存する第2の絶縁膜124を除去する工程を省略することができるという利点もある。

【0099】

（第4の実施形態）

本発明の第4の実施形態に係る半導体装置の製造方法について、図4（a）～（e）を参照しながら説明する。図4（a）～（e）は、第4の実施形態の半導体装置の製造工程を示す断面図である。なお、図4（a）～（e）には、配線形成領域R1と、配線形成領域R1を外部の湿気から保護するためのシールリング領域R2とを示している。なお、シールリング領域R2は配線形成領域R1の側方を囲んでいる。

【0100】

まず、図4（a）に示す工程で、シリコン基板（図示せず）上にシリコン酸化膜からな

る、厚さ500nmの第1の絶縁膜131を形成する。そして、第1の絶縁膜131の上に、フォトリソグラフィにより、金属配線パターン形成領域に開口を有するフォトレジスト（図示せず）を形成する。そのフォトレジストをマスクとしてドライエッチングを行うことにより、第1の絶縁膜131の一部を除去して、深さ250nmの配線溝138、139を形成する。その後、フォトレジストを除去した後、基板上に、タンタルナイトライドとタンタルとからなる厚さ30nmの積層膜（図示せず）と、厚さ1000nmの銅膜（図示せず）とを形成する。その後、化学的機械研磨法を用いて銅膜と積層膜とを研磨することにより、配線形成領域R1に、配線溝138の内表面を覆う表面導体膜132aと、表面導体膜132aを介して配線溝138を埋める金属配線膜132bとからなる第1の金属配線132を形成する。このとき、シールリング領域R2には、表面導体膜133aと金属配線膜133bとからなる第2の金属配線133を形成する。

【0101】

次に、図4（b）に示す工程で、第1の金属配線132および第2の金属配線133の上に、選択的に耐酸化性の金属膜140を堆積する。金属膜140の材料としては、例えば窒化チタン（TiN）がある。

【0102】

その後、図4（c）に示す工程で、第1の絶縁膜131および金属膜140の上に、シリコン窒化炭化膜からなる第2の絶縁膜134を堆積する。このとき、第2の絶縁膜134の材料としては、シリコン窒化膜、シリコン炭化膜、シリコン酸化炭化膜などを用いてもよい。また、これらの膜の積層体を形成してもよい。その後、化学的機械研磨、ウエットエッチングまたはエッチバックを行うことにより、第2の絶縁膜134の平坦化を行う。

【0103】

次に、図4（d）に示す工程で、基板上に、炭素含有シリコン酸化膜からなる第3の絶縁膜135を堆積する。このとき、第3の絶縁膜135としては、FSG（Fluorinated Silicate Glass）膜、BPSG（Boron Phospho Silicate Glass）膜または多孔質膜を用いてもよい。また、これらの膜の積層膜を用いてもよい。

【0104】

その後、フォトリソグラフィによって、第3の絶縁膜135の上に、ホールパターン形成領域およびトレンチパターン形成領域に開口を有するフォトレジスト（図示せず）を形成する。その後、フォトレジストをマスクとしてドライエッチングを行うことにより、配線形成領域R1にはホールパターン136を形成し、シールリング領域R2にはトレンチパターン137を形成する。このドライエッチングは、トレンチパターン137が第2の絶縁膜134の途中の深さまで形成されていてもよいし、第2の絶縁膜134を貫通して、金属膜140に到達してもよい。その後、アッシングによりフォトレジストを除去し、ウエットエッチング時およびドライエッチング時のポリマーを除去する。

【0105】

次に、図4（e）に示す工程で、パターン内に残存する第2の絶縁膜134を除去してホールパターン136とトレンチパターン137とを第1の金属配線132および第2の金属配線133に到達させて、それを導体で埋めることにより、平面形状が円形あるいは正方形のホールコンタクト導体部136'、および、リング状のトレンチコンタクト導体部137'を形成する。

【0106】

次に、本実施形態の半導体装置のうち配線およびシールリングの構造について、図4（e）を再度参照しながら説明する。

【0107】

図4（e）に示すように、本実施形態の半導体装置は、配線形成領域R1と、配線形成領域R1の側方を囲むシールリング領域R2とを有している。そして、配線形成領域R1には第1の金属配線132が設けられ、シールリング領域R2には第2の金属配線133が設けられている。第1の金属配線132は、配線溝138の表面を覆う表面導体膜13

2 a と、その上を覆う金属配線膜 1 3 2 b とを有している。第 2 の金属配線 1 3 3 も、配線溝 1 3 9 の表面を覆う表面導体膜 1 3 3 a と、その上に設けられた金属配線膜 1 3 3 b とを有している。

【0108】

第 1 の金属配線 1 3 2 および第 2 の金属配線 1 3 3 の上には、窒化チタンなどの耐酸化性の金属膜 1 4 0 が設けられている。そして、第 1 の絶縁膜 1 3 1 および金属膜 1 4 0 の上には、第 2 の絶縁膜 1 3 4 が設けられている。第 2 の絶縁膜 1 3 4 の上には第 3 の絶縁膜 1 3 5 が設けられている。そして、配線形成領域 R 1 には、第 3 の絶縁膜 1 3 5 と第 2 の絶縁膜 1 3 4 とを貫通するホールコンタクト導体部 1 3 6' が設けられている。同様に、シールリング領域 R 2 には、トレンチコンタクト導体部 1 3 7' が形成されている。従って、シールリング領域 R 2 には、配線形成領域 R 1 の第 1 の金属配線 1 3 2 およびホールコンタクト導体部 1 3 6' を取り囲むように、第 2 の金属配線 1 3 3 及びトレンチコンタクト導体部 1 3 7' からなるリング状のシールリングが設けられる。

【0109】

本実施形態では、第 2 の金属配線 1 3 3 の上が耐酸化性の金属膜 1 4 0 によって覆われている。そのため、トレンチパターン 1 3 7 が金属膜 1 4 0 に到達している状態でアッシングやポリマー除去の工程を行っても、第 2 の金属配線 1 3 3 の上部が腐食することはない。ここで、第 2 の絶縁膜 1 3 4 のうち第 1 の絶縁膜 1 3 1 の上に位置する部分は厚くならないため、層間の誘電率を一定に保つことができる。

【0110】

また、第 1 の金属配線 1 3 2 および第 2 の金属配線 1 3 3 の上部に耐酸化性の金属膜 1 4 0 を形成することにより、ホールパターン 1 3 6 およびトレンチパターン 1 3 7 を形成するときのエッチング耐性が向上するという利点もある。

【0111】

(第 5 の実施形態)

以下に、本発明の第 5 の実施形態に係る半導体装置の製造方法について、図 5 (a) ~ (f) を参照しながら説明する。図 5 (a) ~ (f) は、第 5 の実施形態において、半導体装置のうち配線領域の製造方法を示す断面図である。なお、第 1 ~ 第 4 の実施形態では、配線領域およびシールリング領域において、ホールパターンとトレンチパターンとの深さの違いが生じる場合を示した。それに対し、本実施形態では、配線領域に多数のホールパターンを形成する場合に、ホールパターンごとに深さの違いが生じる場合について示す。

【0112】

まず、図 5 (a) に示す工程で、シリコン基板 (図示せず) 上にシリコン酸化膜からなる、厚さ 500 nm の第 1 の絶縁膜 1 4 1 を形成する。そして、第 1 の絶縁膜 1 4 1 の上に、フォトリソグラフィにより、金属配線パターン形成領域に開口を有するフォトレジスト (図示せず) を形成する。そのフォトレジストをマスクとしてドライエッチングを行うことにより、第 1 の絶縁膜 1 4 1 の一部を除去して、深さ 250 nm の配線溝 1 4 8 を形成する。その後、フォトレジストを除去した後、基板上に、タンタルナイトライドとタンタルとからなる厚さ 30 nm の積層膜 (図示せず) と、厚さ 1000 nm の銅膜 (図示せず) とを形成する。その後、化学的機械研磨法を用いて銅膜と積層膜とを研磨することにより、配線溝 1 4 8 の内表面を覆う表面導体膜 1 4 2 a と、表面導体膜 1 4 2 a を介して配線溝 1 4 8 を埋める金属配線膜 1 4 2 b とからなる金属配線 1 4 2 を形成する。

【0113】

次に、図 5 (b) に示す工程で、化学的機械研磨法か、または硝酸などを用いた金属の選択的なエッチングによって、金属配線 1 4 2 の上部をリセスさせることにより、深さ 20 nm ~ 40 nm 程度のリセス形状 (凹部 1 5 0) を形成する。

【0114】

次に、図 5 (c) に示す工程で、基板上に、凹部 1 5 0 を埋め、厚さ 100 nm ~ 150 nm のシリコン窒化炭化膜からなる第 2 の絶縁膜 1 4 4 を堆積する。このとき、第 2 の

絶縁膜144の材料としては、シリコン窒化膜、シリコン炭化膜、シリコン酸化炭化膜などを用いてもよい。また、これらの膜の積層体を形成してもよい。

【0115】

この時点では、金属配線142のリセス形状を反映して、第2の絶縁膜144の上には段差が形成されている。

【0116】

次に、図5(d)に示す工程で、化学的機械研磨、ウエットエッチングまたはエッチバックを行うことにより、第2の絶縁膜144の上面の平坦化を行う。これにより、第2の絶縁膜144のうち金属配線142の上に位置する部分の膜厚は70nm～90nm程度になり、それ以外の部分の厚さは50nmになる。

【0117】

次に、図5(e)に示す工程で、基板上に、炭素含有シリコン酸化膜からなる第3の絶縁膜145を堆積する。このとき、第3の絶縁膜145としては、FSG(Fluorinated Silicate Glass)膜、BPSG(Boron Phospho Silicate Glass)膜または多孔質膜を用いてもよい。また、これらの膜の積層膜を用いてもよい。

【0118】

その後、フォトリソグラフィによって、第3の絶縁膜145の上に、ホールパターン形成領域に開口を有するフォトレジスト(図示せず)を形成する。その後、フォトレジストをマスクとしてドライエッチングを行うことにより、ホールパターン146を形成する。このドライエッチングは、ホールパターン146が第2の絶縁膜144の途中の深さになるまで行う。このとき、パターンの疎密等の影響により、複数のホールパターン146の深さはそれぞれ異なる。その後、アッシングによりフォトレジストを除去し、ウエットエッチング時およびドライエッチング時のポリマーを除去する。

【0119】

次に、図5(f)に示す工程で、パターン内に残存する第2の絶縁膜144を除去してホールパターン146を金属配線142に到達させ、それを導体で埋めることにより、平面形状が円形あるいは正方形のホールコンタクト導体部146'を形成する。なお、この工程は、アッシング、ポリマー除去等の金属を腐食させるおそれのある処理を終了した後に行う。

【0120】

次に、本実施形態の半導体装置のうち配線およびホールコンタクト導体部の構造について、図5(f)を再度参照しながら説明する。

【0121】

図5(f)に示すように、本実施形態の半導体装置では、第1の絶縁膜141中に、表面導体膜142aと、その上を覆う金属配線膜142bとを有する金属配線142が設けられている。金属配線142の上部はリセスされており、凹部150が設けられている。

【0122】

第1の絶縁膜141および金属配線142の上には、第2の絶縁膜144が設けられている。第2の絶縁膜144は凹部150を埋めているので、第2の絶縁膜144は、金属配線142の上に位置する部分が他の部分よりも厚く形成されている。第2の絶縁膜144の上面は平坦化されている。

【0123】

第2の絶縁膜144の上には第3の絶縁膜145が設けられている。そして、第3の絶縁膜145と第2の絶縁膜144とを貫通するホールコンタクト導体部146'が設けられている。

【0124】

以下に、本実施形態で得られる効果について、従来と比較しながら説明する。

【0125】

従来では、金属配線の上面は平坦なままであり、金属配線の上には第2の絶縁膜と第3の絶縁膜が形成されていた。この状態で、複数のホールパターンを形成すると、パターン

の疎密やプロセスのばらつきにより、ホールパターンごとに深さが異なっていた。そのため、ホールパターンのうちのいくつかは、第2の絶縁膜を貫通して金属配線に到達するおそれがあった。特に多数のホールパターンを形成する場合には、このおそれが大きくなっていた。

【0126】

これに対し、本実施形態では、第2の絶縁膜144のうち金属配線142の上に位置する部分のみを厚く形成することができる。そのため、ホールパターン146が金属配線142に到達するのを防止することができる。そのため、アッシングやポリマー洗浄を行っても、金属配線142の腐食が起こらない。ここで、第2の絶縁膜144のうち第1の絶縁膜141の上に位置する部分は厚くならないため、層間の誘電率を一定に保つことができる。

【0127】

さらに、金属配線142の上部をリセスさせるために化学的機械研磨法あるいは選択エッチングを行うことにより、第1の絶縁膜141と第2の絶縁膜144との密着性を向上させることができる。

【0128】

なお、本実施形態では、第1の実施形態の方法を、配線領域に複数のホールパターンを形成する場合に適用したものである。しかし、本発明では、第3および第4の実施形態の方法を、配線領域に複数のホールパターンを形成する場合にも適用することができる。

【0129】

また、第1～第4の実施形態では、トレンチコンタクト導体部をリング状に形成しシールリングに用いた場合について説明したが、矩形あるいは帯状に形成して電極の一部として用いてもよい。

【産業上の利用可能性】

【0130】

以上説明したように、層間絶縁膜における誘電率を一定に保ちつつ、ホールパターンやトレンチパターンの下に位置する配線の金属が腐食するのを防止することができる点で、産業利用可能性は高い。

【図面の簡単な説明】

【0131】

【図1】(a)～(f)は、第1の実施形態の半導体装置の製造方法を示す断面図である。

【図2】(a)～(f)は、第2の実施形態の半導体装置の製造方法を示す断面図である。

【図3】(a)～(e)は、第3の実施形態の半導体装置の製造工程を示す断面図である。

【図4】(a)～(e)は、第4の実施形態の半導体装置の製造工程を示す断面図である。

【図5】(a)～(f)は、第5の実施形態において、半導体装置のうち配線領域の製造方法を示す断面図である。

【符号の説明】

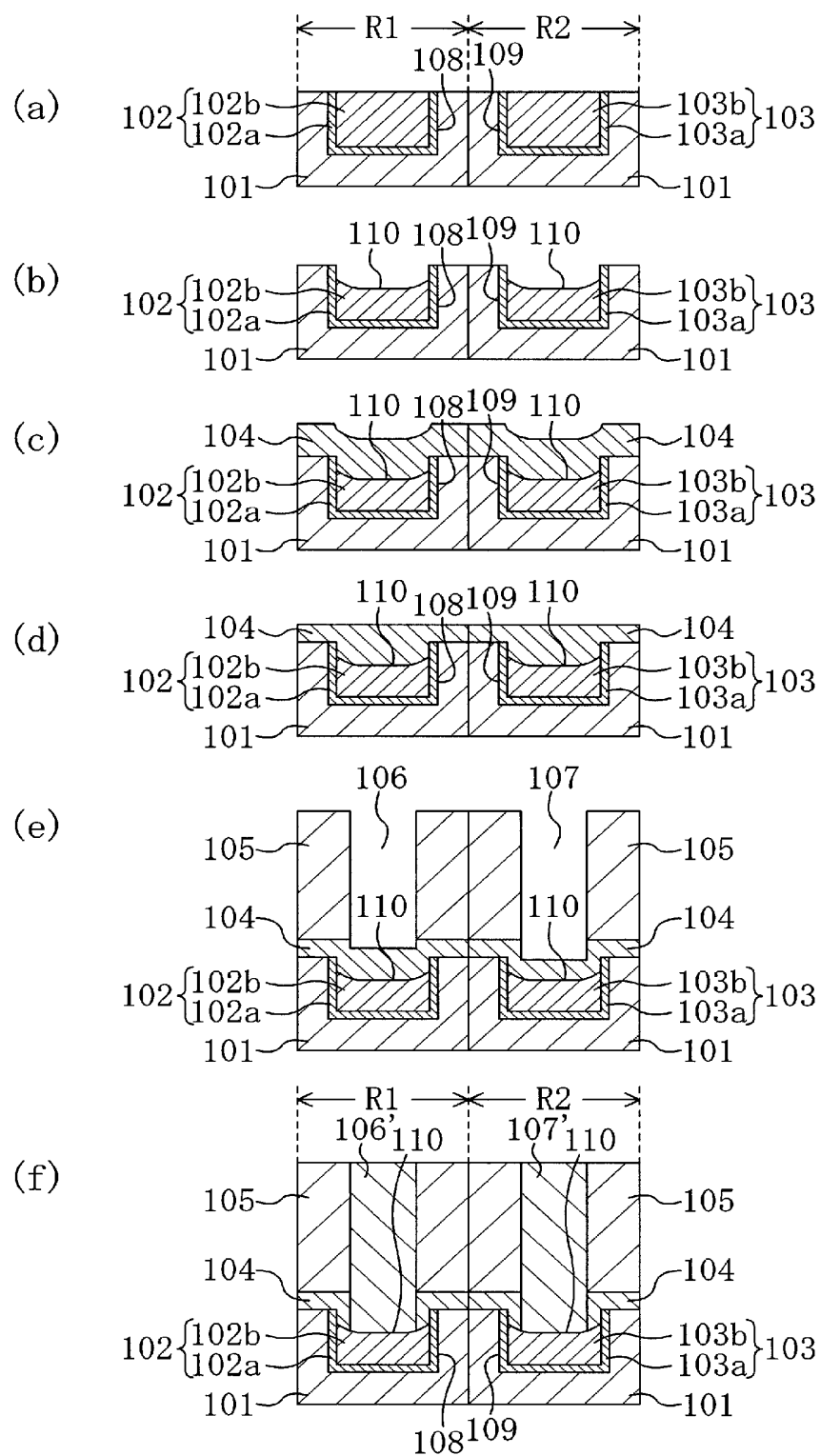
【0132】

101	第1の絶縁膜
102	第1の金属配線
102a	表面導体膜
102b	金属配線膜
103	第2の金属配線
103a	表面導体膜
103b	金属配線膜
104	第2の絶縁膜

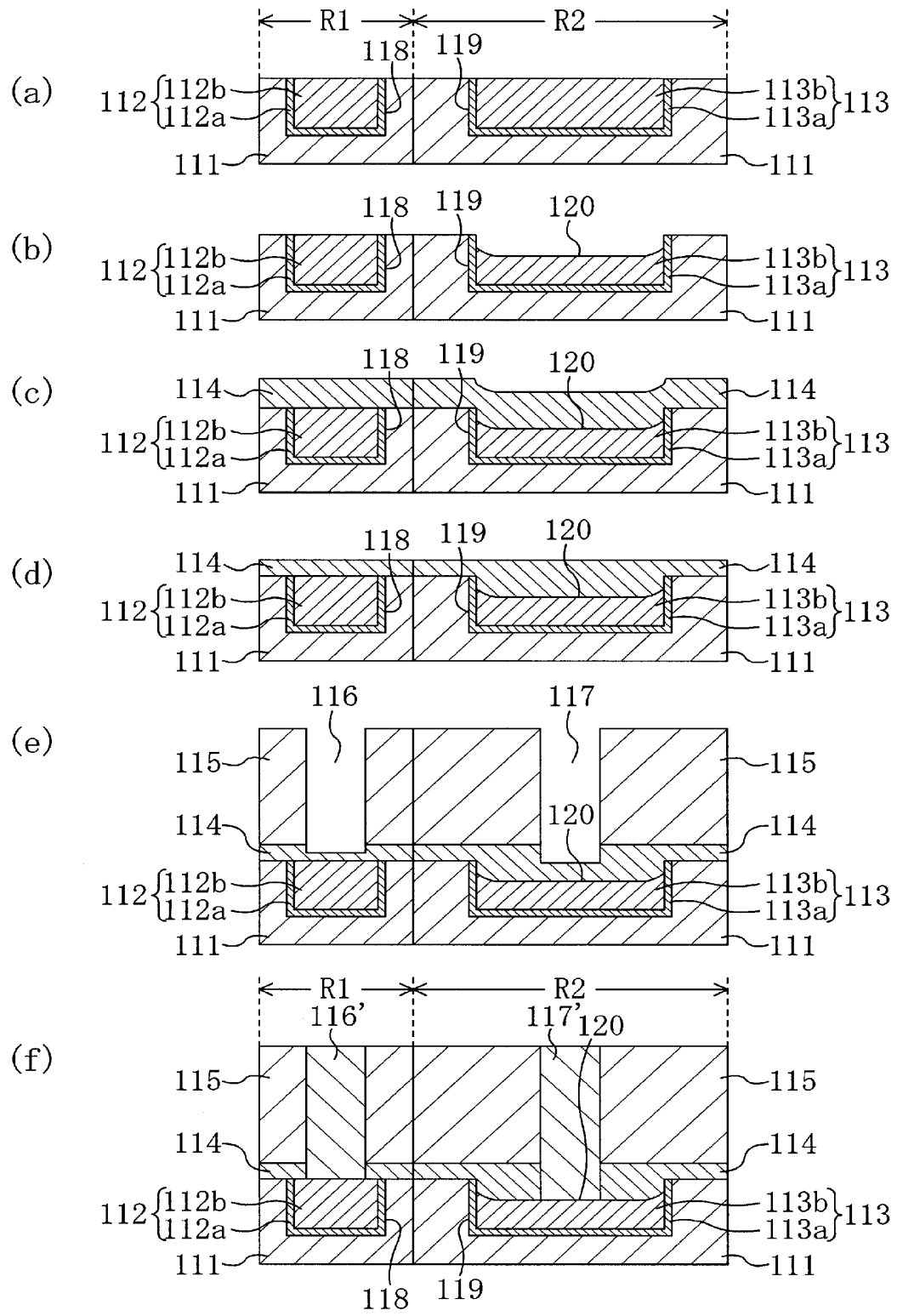
1 0 5	第3の絶縁膜
1 0 6	ホールパターン
1 0 6'	ホールコンタクト導体部
1 0 7	トレンチパターン
1 0 7'	トレンチコンタクト導体部
1 0 8	配線溝
1 0 9	配線溝
1 1 0	凹部
1 1 1	第1の絶縁膜
1 1 2	第1の金属配線
1 1 2 a	表面導体膜
1 1 2 b	金属配線膜
1 1 3	第2の金属配線
1 1 3 a	表面導体膜
1 1 3 b	金属配線膜
1 1 4	第2の絶縁膜
1 1 5	第3の絶縁膜
1 1 6	ホールパターン
1 1 6'	ホールコンタクト導体部
1 1 7	トレンチパターン
1 1 7'	トレンチコンタクト導体部
1 1 8	配線溝
1 1 9	配線溝
1 2 0	凹部
1 2 1	第1の絶縁膜
1 2 2	第1の金属配線
1 2 2 a	表面導体膜
1 2 2 b	金属配線膜
1 2 3	第2の金属配線
1 2 3 a	表面導体膜
1 2 3 b	金属配線膜
1 2 4	第2の絶縁膜
1 2 5	第3の絶縁膜
1 2 6'	ホールコンタクト導体部
1 2 6	ホールパターン
1 2 7	トレンチパターン
1 2 7'	トレンチコンタクト導体部
1 2 8	配線溝
1 2 9	配線溝
1 3 0	耐酸化性膜
1 3 1	第1の絶縁膜
1 3 2	第1の金属配線
1 3 2 a	表面導体膜
1 3 2 b	金属配線膜
1 3 3	第2の金属配線
1 3 3 a	表面導体膜
1 3 3 b	金属配線膜
1 3 4	第2の絶縁膜
1 3 5	第3の絶縁膜
1 3 6	ホールパターン

1 3 6'	ホールコンタクト導体部
1 3 7	トレンチパターン
1 3 7'	トレンチコンタクト導体部
1 3 8	配線溝
1 3 9	配線溝
1 4 0	金属膜
1 4 1	第1の絶縁膜
1 4 2	金属配線
1 4 2 a	表面導体膜
1 4 2 b	金属配線膜
1 4 3	金属配線
1 4 4	第2の絶縁膜
1 4 5	第3の絶縁膜
1 4 6	ホールパターン
1 4 6'	ホールコンタクト導体部
1 4 8	配線溝
1 5 0	凹部

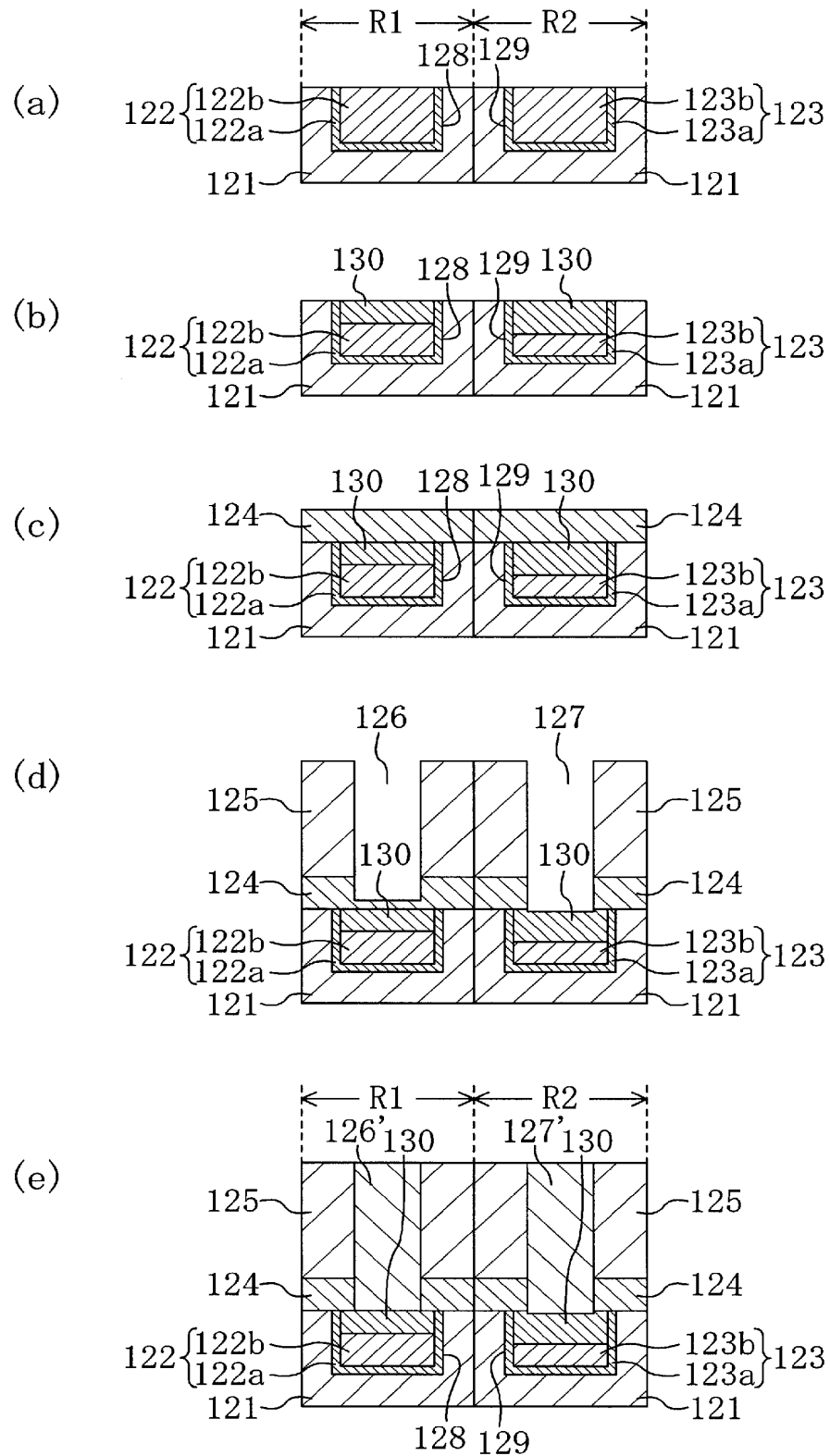
【書類名】 図面
【図 1】



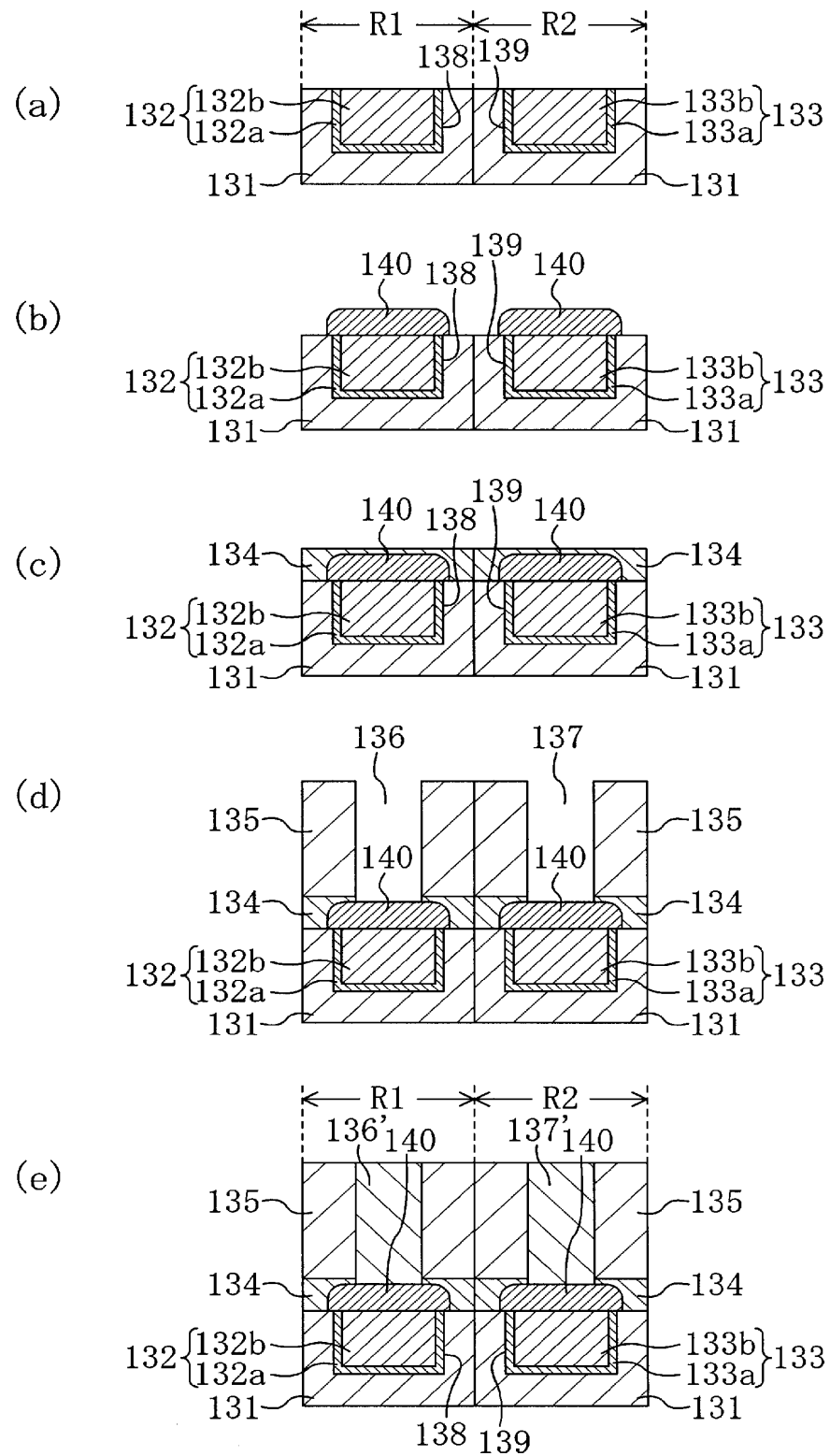
【図2】



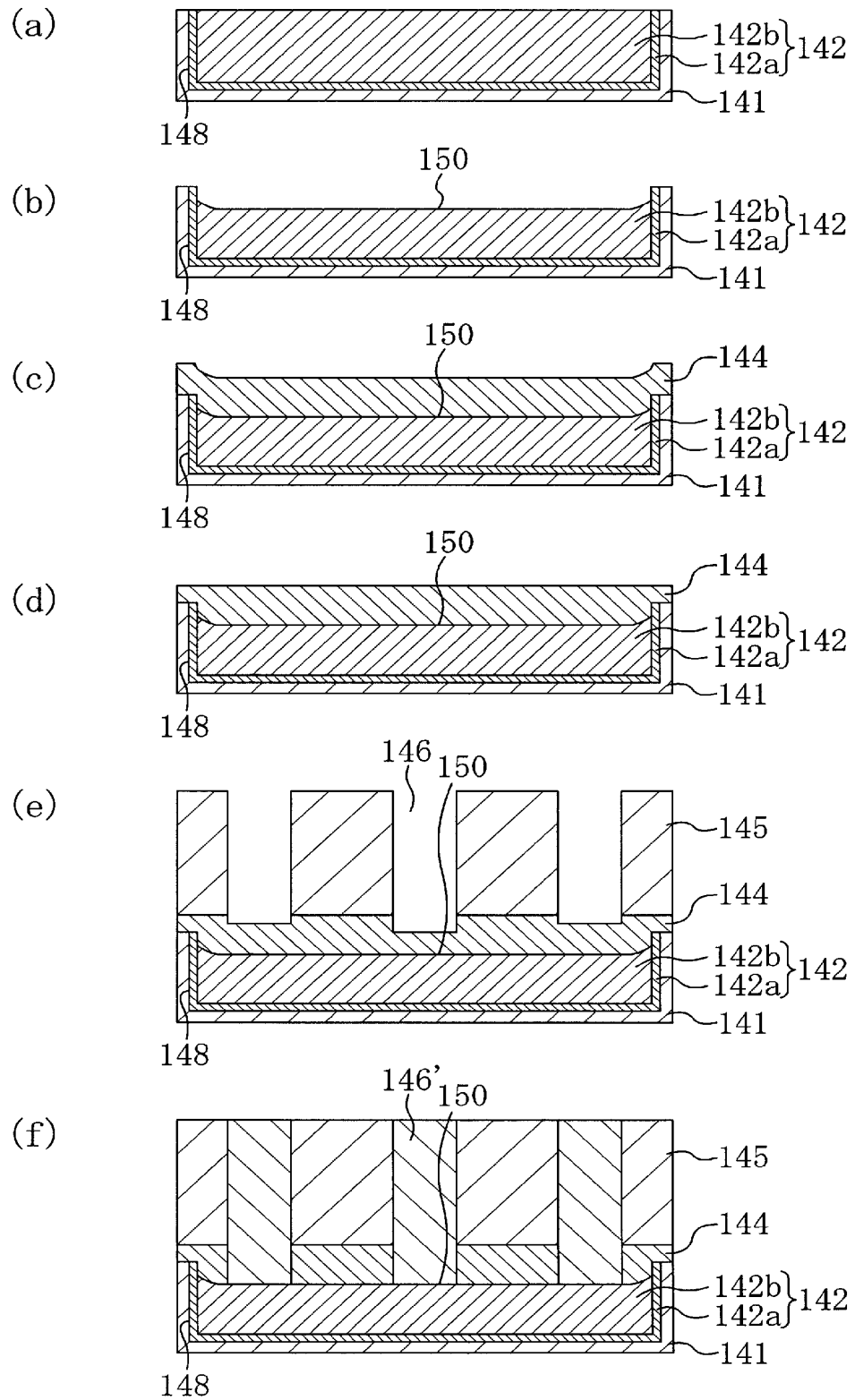
【図3】



【図4】



【図 5】



【書類名】 要約書

【要約】

【課題】 ホールパターンとシールリングのためのトレンチパターンを形成する際に、トレンチパターンやホールパターンが下の配線層に到達して、配線層における金属が腐食するのを防止する。

【解決手段】 本実施形態の半導体装置の製造方法では、まず、配線形成領域R 1 に第1の金属配線1 0 2を形成し、シールリング領域R 2 に第2の金属配線1 0 3を形成する。次に、化学的機械研磨法やエッチングによって、第1の金属配線1 0 2および第2の金属配線1 0 3の上部をリセスさせて凹部1 1 0を形成する。その後、基板上に、凹部1 1 0を埋める第2の絶縁膜1 0 4を形成し、その上面を平坦化する。次に、ホールパターン1 0 6およびトレンチパターン1 0 7を、第2の絶縁膜1 0 4の途中の深さまで形成し、アッシングやポリマー除去を行う。その後、ホールパターン1 0 6およびトレンチパターン1 0 7を第1の金属配線1 0 2および第2の金属配線1 0 3に到達させる。

【選択図】 図1

【書類名】 手続補正書
【整理番号】 2926450111
【提出日】 平成18年10月16日
【あて先】 特許庁長官 殿
【事件の表示】
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【補正をする者】
【識別番号】 000005821
【氏名又は名称】 松下電器産業株式会社
【代理人】
【識別番号】 100077931
【弁理士】
【氏名又は名称】 前田 弘
【発送番号】 362983
【手続補正1】
【補正対象書類名】 特許請求の範囲
【補正対象項目名】 全文
【補正方法】 変更
【補正の内容】
【書類名】 特許請求の範囲
【請求項1】

半導体基板の上方に、第1の絶縁膜を形成する工程（a）と、

上記第1の絶縁膜の少なくとも上部に、第1の表面導体膜と上記第1の表面導体膜に囲まれた第1の金属配線膜とからなる第1の配線層と、第2の表面導体膜と上記第2の表面導体膜に囲まれた第2の金属配線膜とからなる第2の配線層とを形成する工程（b）と、

少なくとも上記第1の配線層の上部に、上記第1の表面導体膜の上面と上記第1の金属配線膜の上面とが互いの境界部において段差を形成するように第1の凹部を形成する工程（c）と、

上記第1の絶縁膜および上記第1の配線層と上記第2の配線層の上に、上記第1の凹部を埋める第2の絶縁膜を形成する工程（d）と、

上記第2の絶縁膜の上面を平坦化し、上記第2の絶縁膜のうち上記第1の金属配線膜の上方に位置する部分の膜厚を、上記第2の絶縁膜のうち上記第1の絶縁膜の上方に位置する部分の膜厚よりも厚くする工程（e）と、

上記工程（e）の後に、上記第2の絶縁膜の上に第3の絶縁膜を形成する工程（f）と

、上記第3の絶縁膜および上記第2の絶縁膜のうち上記第1の配線層と上記第2の配線層の上方に位置する部分を、フォトレジストをマスクにして上記第1の配線層と上記第2の配線層に到達しない深さまで除去し、上記第1の配線層と上記第2の配線層上に上記第2の絶縁膜の一部を残存させる工程（g）と、

上記フォトレジストを除去する工程（h）とを備える、半導体装置の製造方法。

【請求項2】

請求項1に記載の半導体装置の製造方法であって、

上記工程（c）では、上記第2の配線層の上部に、上記第2の表面導体膜の上面と上記第2の金属配線膜の上面とが互いの境界部において段差を形成するように上記第1の凹部よりも浅い第2の凹部を形成し、

上記工程（d）では、上記第2の絶縁膜で上記第2の凹部を埋め、

上記工程（e）では、上記第2の絶縁膜のうち上記第2の金属配線膜の上方に位置する部分の膜厚を、上記第2の絶縁膜のうち上記第1の金属配線膜の上方に位置する部分の膜厚よりも薄く、上記第2の絶縁膜のうち上記第1の絶縁膜の上方に位置する部分の膜厚よりも厚く形成する、半導体装置の製造方法。

【請求項 3】

請求項 1 または 2 に記載の半導体装置の製造方法であって、

上記工程（c）では、化学的機械研磨によってリセスさせる、半導体装置の製造方法。

【請求項 4】

請求項 1 または 2 に記載の半導体装置の製造方法であって、

上記工程（c）では、ドライエッチングによってリセスさせる、半導体装置の製造方法。

【請求項 5】

請求項 1 または 2 に記載の半導体装置の製造方法であって、

上記工程（c）では、ウエットエッチングによってリセスさせる、半導体装置の製造方法。

【請求項 6】

請求項 1 または 2 に記載の半導体装置の製造方法であって、

上記工程（c）では、加熱により銅を圧縮させてリセスさせる、半導体装置の製造方法。

【請求項 7】

請求項 1 ～ 6 のいずれか 1 項に記載の半導体装置の製造方法であって、

上記工程（g）では、上記第 1 の配線層の上方にトレンチパターンを形成し、上記第 2 の配線層の上方にホールパターンを形成する、半導体装置の製造方法。

【請求項 8】

請求項 7 に記載の半導体装置の製造方法であって、

上記トレンチパターンは矩形あるいは帯状の平面形状を有し、
上記ホールパターンは円形あるいは正方形の平面形状を有している、半導体装置の製造方法。

【請求項 9】

請求項 7 に記載の半導体装置の製造方法であって、

上記第 1 の配線層および上記トレンチパターンは、リング状に形成されたシールリングである、半導体装置の製造方法。

【請求項 10】

請求項 1 ～ 9 のいずれか 1 項に記載の半導体装置の製造方法であって、

上記工程（b）では、上記第 1 の配線層の幅を、上記第 2 の配線層の幅よりも大きく形成する、半導体装置の製造方法。

【請求項 11】

請求項 1 ～ 10 のいずれか 1 項に記載の半導体装置の製造方法であって、

上記工程（b）では、上記第 1 の配線層の側方に、ダミー配線層を形成する、半導体装置の製造方法。

【請求項 12】

請求項 1 ～ 11 のいずれか 1 項に記載の半導体装置の製造方法であって、

上記工程（a）の前に、上記半導体基板内に素子を形成する工程（i）をさらに備え、
上記工程（b）では、上記第 1 の配線層または上記第 2 の配線層が上記素子と電氣的に接続されるように形成する、半導体装置の製造方法。

【請求項 13】

請求項 1 ～ 12 のいずれか 1 項に記載の半導体装置の製造方法であって、

上記第 2 の絶縁膜は、炭素を含むシリコン絶縁膜である、半導体装置の製造方法。

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【識別番号】 100077931
【弁理士】
【氏名又は名称】 前田 弘
【発送番号】 305228
【手続補正1】
【補正対象書類名】 特許請求の範囲
【補正対象項目名】 全文
【補正方法】 変更
【補正の内容】

【書類名】 特許請求の範囲

【請求項1】

半導体基板の上方に、第1の絶縁膜を形成する工程（a）と、
上記第1の絶縁膜の少なくとも上部に、第1の金属配線膜と第2の金属配線膜とを形成する工程（b）と、

上記第2の金属配線膜の上部に凹部を形成する工程（c）と、

上記第1の絶縁膜、上記第1の金属配線膜および上記第2の金属配線膜の上に、上記凹部を埋め込むように、第2の絶縁膜を形成する工程（d）と、

上記第2の絶縁膜の上面を平坦化することにより、上記第2の絶縁膜のうち上記第2の金属配線膜の上方に位置する部分の膜厚を、上記第2の絶縁膜のうち上記第1の金属配線膜の上方に位置する部分の膜厚よりも厚くする工程（e）と、

上記工程（e）の後に、上記第2の絶縁膜の上に第3の絶縁膜を形成する工程（f）と

、
フォトリソをマスクに用いたエッチングにより、上記第3の絶縁膜および上記第2の絶縁膜のうち上記第1の金属配線膜の上方に位置する部分を上記第1の金属配線膜に到達しない深さまで除去することによってホールパターンを形成すると共に、上記第3の絶縁膜および上記第2の絶縁膜のうち上記第2の金属配線膜の上方に位置する部分を上記第2の金属配線膜に到達しない深さまで除去することによって開口面積が前記ホールパターンの開口面積よりも広いトレンチパターンを形成する工程（g）と、

上記フォトリソを除去する工程（h）と、

前記工程（h）の後に、前記ホールパターンの底部における前記第2の絶縁膜を除去して前記第1の金属配線膜を露出させると共に、前記トレンチパターンの底部における前記第2の絶縁膜を除去して前記第2の金属配線膜を露出させる工程（i）とを備える、半導体装置の製造方法。

【請求項2】

請求項1に記載の半導体装置の製造方法において、

上記工程（c）は、化学的機械研磨によって、前記凹部を形成する工程である、半導体装置の製造方法。

【請求項3】

請求項1に記載の半導体装置の製造方法において、

上記工程（c）は、エッチングによって、前記凹部を形成する工程である、半導体装置

の製造方法。

【請求項4】

請求項1に記載の半導体装置の製造方法において、
上記トレンチパターンは矩形あるいは帯状の平面形状を有し、
上記ホールパターンは円形あるいは正方形の平面形状を有している、半導体装置の製造方法。

【請求項5】

請求項1に記載の半導体装置の製造方法において、
上記工程（i）の後に、前記ホールパターンに導体を埋め込んでホールコンタクト導体部を形成すると共に前記トレンチパターンに導体を埋め込んでトレンチコンタクト導体部を形成する工程をさらに備え、
上記第2の金属配線膜およびトレンチコンタクト導体部は、リング状に形成されたシールリングである、半導体装置の製造方法。

【請求項6】

請求項1に記載の半導体装置の製造方法において、
上記工程（b）において、前記第2の金属配線膜の幅は、前記第1の金属配線膜の幅よりも広い、半導体装置の製造方法。

【請求項7】

請求項1に記載の半導体装置の製造方法において、
上記工程（b）は、前記第2の金属配線膜の周りにダミーパターンを形成することによって単位面積あたりの金属の占有率を上昇させる工程を含む、半導体装置の製造方法。

【請求項8】

請求項1～7のいずれか1項に記載の半導体装置の製造方法において、
上記工程（a）の前に、上記半導体基板内に素子を形成する工程（j）をさらに備え、
上記工程（b）では、上記第1の金属配線膜または上記第2の金属配線膜が上記素子と電氣的に接続されるように形成する、半導体装置の製造方法。

【請求項9】

請求項1～8のいずれか1項に記載の半導体装置の製造方法において、
上記第2の絶縁膜は、シリコン窒化炭化膜である、半導体装置の製造方法。

【請求項10】

請求項1～8のいずれか1項に記載の半導体装置の製造方法において、
上記第2の絶縁膜は、シリコン酸化炭化膜である、半導体装置の製造方法。

【手続補正2】

【補正対象書類名】 明細書

【補正対象項目名】 発明の名称

【補正方法】 変更

【補正の内容】

【発明の名称】 半導体装置の製造方法

出願人履歴

000005821

19900828

新規登録

506178449

大阪府門真市大字門真1006番地

松下電器産業株式会社

000005821

20081001

名称変更

506178449

大阪府門真市大字門真1006番地

パナソニック株式会社

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/051,415			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	540		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220		
TOTAL CLAIMS (37 CFR 1.16(i))	7	minus 20 =				x 52 =	0.00		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 =				x 220 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
				TOTAL		TOTAL	1090		
* If the difference in column 1 is less than zero, enter "0" in column 2.									
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	x	=
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	x	=
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
13/051,415	03/18/2011	2812	1090	085393-0521	7	2

CONFIRMATION NO. 4503

53080
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

FILING RECEIPT



Date Mailed: 04/01/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Shunsuke ISONO, Osaka, JAPAN;

Assignment For Published Patent Application

PANASONIC CORPORATION, Osaka, JAPAN

Power of Attorney:

Kenneth Cage--26151	Edward Kubasiewicz--30020
Jack Lever Jr--28149	Michael Fogarty--36139
Raphael Lupo--28363	Brian Ferguson--36801
Paul Devinsky--28553	Robert Zelnick--36976
Stanislaus Aksman--28562	Willem Gadiano--37136

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Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)
JAPAN 2003-335185 09/26/2003

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 03/29/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/051,415**

Projected Publication Date: 07/14/2011

Non-Publication Request: No

Early Publication Request: No
Title

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

Preliminary Class

438

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Docket No.: 085393-0521

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Shunsuke ISONO	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Divisional of U.S.		
Serial No. 12/153,028	:	Group Art Unit: Not Yet Assigned
	:	
Filed: March 18, 2011	:	Examiner: Not Yet Assigned
	:	
For:		SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Divisional of U.S. Serial No. 12/153,028

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial no. 12/153,028, filed May 13, 2008, which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

**Please recognize our Customer No. 53080
as our correspondence address.**

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ln
Facsimile: 202.756.8087
Date: March 18, 2011

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)				ATTY. DOCKET NO. 085393-0521		SERIAL NO. Divisional of U.S. Serial No. 12/153,028	
				APPLICANT Shunsuke ISONO			
				FILING DATE March 18, 2011		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)		Publication Date MM-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US	7,041,586 B2	05-2006	KUDO ET AL.	Corresponding to JP 11-274122 A	
		US	6,730,590 B2	05-2004	OHASHI ET AL.	Corresponding to JP 11-145288 A	
		US	6,908,847	06-2005	SAITO et al.		
		US	6,281,535	08-2001	MA et al.		
		US	6,417,116	07-2002	KUDO et al.		
		US	6,479,366	11-2002	MIYAMOTO		
		US	2002/0079585	06-2002	WONG		
		US	2005/0054122	03-2005	CELII et al.		
		US	6,114,243	09/2000	GUPTA et al.		
		US	6,589,863	07/2003	USAMI, Tatsuya		
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes -Number 4-Kind Codes (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No
		JP 2002-118078 A		04-19-2002	TOSHIBA CORP		
		JP 11-274122 A		10-08-1999	FUJITSU LTD	Corresponding to US 7,041,586 B2	
		JP 11-145288 A		05-28-1999	HITACHI LTD	Corresponding to US 6,730,590 B2	
		JP 2002-373937 A		12-26-2002	FUJITSU LTD		
		JP 2002-289689 A		10-04-2002	FUJITSU LTD		
		JP 2002-270608 A		09-20-2002	FUJITSU LTD		
		JP 2000-174123 A		06-23-2000	NEC CORP		
		JP 8-83780 A		03-26-1996	TOSHIBA CORP		
		JP 2003-133314 A		05-09-2003	HITACHI LTD		
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
		Japanese Office Action issued in corresponding Japanese Patent Application No. 2003-335185, dated August 22, 2006.					
EXAMINER				DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 085393-0521		SERIAL NO. Divisional of U.S. Serial No. 12/153,028	
				APPLICANT Shunsuke ISONO			
				FILING DATE March 18, 2011		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US	2002/0125577 A1	09-12-2002	KOMADA		
		US	2005/0085066 A1	04-21-2005	TSAO et al.		
		US	6,313,028 B2	11-06-2001	HUANG et al.		
		US	6,838,370 B1	01-04-2005	NIUYA et al.		
		US	2003/0118798 A1	06-26-2003	FUJI		
		US	6,828,222 B2	12-07-2004	OYAMATSU		
		US	2002/0155702 A1	10/24/2002	Aoki et al.	Corresponds w/ JP 2002- 246391	
		US	2003/0003733	01-2003	Ohashi et al.		
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No
		JP 2002-246391		08-30-2002	NEC CORPORATION	Corresponds w/ US 2002/0155702	
		JP 08-264538		10-11-1996	SUMITOMO METAL IND. LTD.		
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
		Japanese Notice of Reasons for Rejection, with English Translation, issued in Japanese Patent Application No. 2006-281346, mailed on October 5, 2010.					
EXAMINER				DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
First Named Inventor/Applicant Name:		Shunsuke ISONO		
Filer:		Michael E. Fogarty/Lydia Nguyen		
Attorney Docket Number:		085393-0521		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Electronic Acknowledgement Receipt	
EFS ID:	9690580
Application Number:	13051415
International Application Number:	
Confirmation Number:	4503
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Shunsuke ISONO
Customer Number:	53080
Filer:	Michael E. Fogarty/Lydia Nguyen
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0521
Receipt Date:	18-MAR-2011
Filing Date:	
Time Stamp:	15:16:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1090
RAM confirmation Number	1556
Deposit Account	500417
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	P03558306_TRN_085393-0521.PDF	62221	no	3
			6a7c903a266fcb923d8c76164876d4449351a37a		
Warnings:					
Information:					
2		P03558306_SPEC_085393-0521.pdf	1571143	yes	38
			4e390f9d936a36a52be457673adcf07b1ea4435		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	31	
	Claims		32	37	
	Abstract		38	38	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	P03558306_DRW_085393-0521.pdf	211997	no	5
			9e326c1224c0ea766d24146cae88cc84b3f2d1dd		
Warnings:					
Information:					
4	Oath or Declaration filed	P03558306_DEC_085393-0521.pdf	99639	no	2
			6833b0b844d24f7445e1c8befd0912a68fc8f358		
Warnings:					
Information:					
5	Preliminary Amendment	P03558306_AMEND-P_085393-0521.PDF	87988	no	8
			ffc2abaffb81c359c81c3d92f277684850d05092		
Warnings:					
Information:					
6	Drawings-only black and white line drawings	P03558306_MISC-NEW-DRW_085393-0521.PDF	64351	no	2
			0b86a2fc46e569b77c98d004425633c5ff64117b		
Warnings:					
Information:					
7	Specification	P03558306_MISC-SUBSPEC-MARKED_085393-0521.PDF	1478755	no	32
			e270c76b7d60ccc46b7231e89ebb088a041c14dc		

Warnings:					
Information:					
8	Specification	P03558306_MISC-SUBSPEC-CLEAN_085393-0521.PDF	1474665 17081e00a38afa96068d0baf64f1ecd75fed9df1	no	32
Warnings:					
Information:					
9	Information Disclosure Statement (IDS) Filed (SB/08)	P03558306_IDS_085393-0521.PDF	112810 9aea69737a9d9ea6fca1102f158f29cfc524dc1	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
10	Fee Worksheet (PTO-875)	fee-info.pdf	33051 03b96e78b1be378c940666edce1a7ce995f687a3	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			5196620		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

REQUEST FORM FOR DIVISIONAL APPLICATION UNDER 37 CFR 1.53(b)

DOCKET NUMBER: 085393-0521

Prior Application:

Art Unit: 2818

Examiner: TRAN, LONG K.

BOX New Applications

FEE

Mail Stop New Applications

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

This is a Request for filing a Divisional application under 37 CFR 1.53(b) of pending prior application

No. 12/153,028 filed on May 13, 2008, entitled **SEMICONDUCTOR DEVICE AND METHOD FOR
FABRICATING THE SAME**, by the following named inventor(s): Shunsuke ISONO.

1. ☒ I hereby state that the enclosed application contains no new matter.
2. Oath or Declaration
 - a. ☐ Newly executed (original or copy)
 - b. ☒ Copy from a prior application (37 CFR 1.63(d))
 - i. ☐ Deletion of inventor(s)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
3. ☒ Incorporation By Reference (useable if Box 2b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 2b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
4. ☒ Preliminary Amendment is enclosed.
5. ☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.
6. ☒ Cancel claims 1-22.

DOCKET NUMBER: 085393-0521

7. The filing fee is calculated on the basis of the claims existing in the prior application as amended at 4 and 6 above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	7	-20	0	\$52.00	\$0.00
Independent Claims	2	-3	0	\$220.00	\$0.00
Multiple Dependent Claim(s)					\$0.00
Sheets of specification and drawing (\$270.00 for each 50 sheets in excess of 100)					\$0.00
Basic Filing Fee					\$330.00
Patent Search Fee					\$540.00
Patent Examination Fee					\$220.00
Total of Above Calculations					\$1,090.00
Less ½ for Small Entity					\$0.00
Assignment & Recording Fee					\$0.00
Total Fee					\$1,090.00

8. ☐ A Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 was filed in prior application and such status is still proper and desired.
9. ☒ **PLEASE CHARGE DEPOSIT ACCOUNT 500417 in the amount of \$1,090.00.** Commissioner is authorized to charge any fees which may be required or credit any overpayment to Deposit Account No. 500417.
10. ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees to maintain the pendency of the parent Application No. 12/153,028 or credit any overpayment to Deposit Account No. 500417.
11. ☒ Priority of Application No. 2003-335185 filed on September 26, 2003, in Japan is claimed under 35 USC 119. The certified priority document(s) were filed in Application No. 10/945,920 on September 22, 2004.
12. ☒ The prior application is assigned of record to
- PANASONIC CORPORATION**
Osaka, Japan
13. ☒ The power of attorney in the prior application is to:
- McDermott Will & Emery LLP
14. ☐ Also enclosed:

DOCKET NUMBER: 085393-0521

15. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until .

Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, D.C. 20005-3096

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our
correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ln
Facsimile: 202.756.8087
Date: March 18, 2011

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

5 This application claims priority under 35 U.S.C. §119 on Patent Application No. 2003-335185 filed in Japan on September 26, 2003, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

10 (a) Fields of the Invention

 The present invention relates to semiconductor devices and methods for fabricating the same. In particular, the present invention relates to semiconductor devices having contact portions of conductor (referred hereinafter to as conductor contact portions) on an interconnect layer and methods for fabricating such a device.

15

(b) Description of Related Art

 In recent years, miniaturization and high degree of integration of semiconductor integrated circuits have been rapidly proceeding. In accordance with the proceeding miniaturization of the circuit, delay time caused by transistor operation can be cut in the device while interconnect resistance and parasitic capacitance increase therein. This makes it difficult to cut delay time caused in an interconnect. In a measure to cut the interconnect delay time, in order to reduce the interconnect resistance, copper having a lower resistivity than aluminum used as a conventional interconnect material is employed as a substitute for aluminum. Moreover, in order to reduce the parasitic capacitance, an insulating film having a low dielectric constant is employed as a material for an interlayer insulating film and the like.

20

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 Copper is difficult to etch. Therefore, formation of an interconnect with copper is

made by a damascene process: a hole pattern and a trench configuration are formed in an insulating film, after which the patterns are filled with copper.

In a chip of a semiconductor device, a trench configuration called a seal ring is formed to protect transistors and interconnects provided in the chip against outside
5 moisture. The seal ring is formed to surround an area containing the transistors and the interconnects. The seal ring is formed simultaneously with the etching for forming a hole pattern (vias).

The hole pattern and the trench configuration serving as the seal ring are formed in the following manner.

10 First, to form the hole pattern and the trench configuration, an interlayer insulating film is halfway removed using photoresist as a mask. The reason why the removal is stopped halfway is that if an interconnect layer located below the hole pattern and the trench configuration is exposed therefrom during the removal, the interconnect layer corrodes during subsequent ashing for removing the photoresist and subsequent polymer
15 removal. To avoid such a problem, ashing and polymer removal are performed with only part of the thickness of the interlayer insulating film remaining. Thereafter, using the resulting interlayer insulating film itself as a mask, the hole pattern and the trench configuration are made to reach the interconnect layer.

However, the conventional semiconductor device has caused the following
20 problems.

Generally, during etching, the etching rate rises as the area of an opening increases. In this device, the opening area of the trench is greater than that of the hole. Thus, when the trench and the hole are formed at the same time by a single etching, the trench is formed deeper. Therefore, it might be unable to stop etching of the trench halfway through
25 the interlayer insulating film, resulting in exposure of metal of the interconnect layer located therebelow. If the metal is exposed in this process, then the disadvantage arises that the metal corrodes by subjecting itself to subsequent photoresist removal by ashing

and to subsequent polymer removal.

Such a disadvantage also arises when the interlayer insulating film is formed with multiple types of hole patterns. Specifically, the hole patterns have different pattern densities or the like, so that it is impossible, in forming the different hole patterns, to partly
5 remove the insulating film to form the hole patterns with a uniform depth. This causes the disadvantage that the interconnect layer located below the hole patterns is exposed.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method for fabricating a
10 semiconductor device resistant to metal corrosion in an interconnect layer by taking measures to prevent exposure of the interconnect layer during formation of a hole pattern and a trench pattern.

A first semiconductor device of the present invention comprises: a semiconductor substrate; a first insulating film provided over the semiconductor substrate; an interconnect
15 layer provided in at least an upper portion of the first insulating film; a second insulating film provided on the first insulating film and the interconnect layer; a third insulating film provided on the second insulating film; and at least one conductor contact portion passing through the third insulating film and the second insulating film to reach the interconnect layer. In this device, an upper portion of the interconnect layer is provided with a recess
20 and a portion of the second insulating film located on the interconnect layer has a greater thickness than a portion thereof located on the first insulating film.

With this device, the portion of the second insulating film located on the interconnect layer is formed thick. Therefore, in the step of partly removing the third insulating film and the second insulating film to form the conductor contact portion, part of
25 the second insulating film can be easily left on the interconnect layer, which makes it difficult to expose the interconnect layer. The semiconductor surface in this condition can be subjected to a process that may corrode metal, such as ashing or polymer removal.

Subsequently, the unremoved parts of the third insulating film and the second insulating film can be removed to expose the interconnect layer, and a conductor for the conductor contact portion can fill the removed portion. That is to say, a process that may corrode metal can be carried out on the semiconductor surface with the interconnect layer not exposed, whereby corrosion of the interconnect layer can be prevented.

On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

The interconnect layer may comprise a first interconnect layer. The conductor contact portion may comprise a first conductor contact portion. The device may further comprise: a second interconnect layer provided in at least an upper portion of the first insulating film; and a second conductor contact portion passing through the third insulating film and the second insulating film to reach the second interconnect layer. A portion of the second insulating film located on the first interconnect layer may have a greater thickness than a portion thereof located on the second interconnect layer. In this case, even if the third insulating film and the second insulating film are partly removed in order to form the conductor contact portion, it can become difficult to expose the first interconnect layer because the region of the second insulating film formed with the first conductor contact portion is formed thick. As is the case where the area in which the first conductor contact portion is formed is greater than the area in which the second conductor contact portion is formed, when the third insulating film and the second insulating film are partly removed to form the conductor contact portion, the region where the first conductor contact portion is formed is removed deeper. Even in such a circumstance, it can become difficult to expose the first interconnect layer.

The first interconnect layer may have a greater width than the second interconnect layer. In this case, the region where the first interconnect layer is formed has a higher area ratio of conductor (metal) than the region where the second interconnect layer is formed.

Therefore, when chemical mechanical polishing or similar treatment is carried out on the first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

5 A dummy interconnect layer may be formed beside the first interconnect layer. In this case, the surrounding of the region where the first interconnect layer is formed has a higher area ratio of conductor (metal) than the surrounding of the region where the second interconnect layer is formed. Therefore, when chemical mechanical polishing or similar treatment is carried out on the first interconnect layer and the second interconnect layer
10 from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

The first conductor contact portion may be of rectangular or strip-like plane, and the second conductor contact portion may be of circular or square plane.

The first interconnect layer and the first conductor contact portion may constitute a
15 seal ring provided in ring shape. In this case, even though the first conductor contact portion serving as the seal ring differs greatly in area from the second conductor contact portion, the structure described above can prevent the first interconnect layer from being exposed.

An element may be provided in the semiconductor substrate, and the interconnect
20 layer may be electrically connected to the element. In this case, when the third insulating film and the second insulating film are partly removed in forming the conductor contact portion, an error would arise in the depth to be removed. Even though such an error arises, it can become difficult to expose the interconnect layer.

The second insulating film is preferably an insulating film of silicon compound
25 containing carbon.

A second semiconductor device of the present invention comprises: a semiconductor substrate; a first insulating film provided on the semiconductor substrate; an

interconnect layer provided in at least an upper portion of the first insulating film; an oxidation-resistant conductor film covering the top of the interconnect layer; a second insulating film provided on the first insulating film and the oxidation-resistant conductor film; a third insulating film provided on the second insulating film; and at least one
5 conductor contact portion passing through the third insulating film and the second insulating film to reach the oxidation-resistant conductor film.

With this device, even if, in the step of partly removing the third insulating film and the second insulating film to form the conductor contact portion, treatment that may corrode metal, such as ashing and polymer removal, is carried out on the semiconductor
10 surface with the oxidation-resistant conductor film exposed, corrosion of the interconnect layer can be prevented. On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

The oxidation-resistant conductor film may be a nitrogen introduced layer produced
15 by introducing nitrogen into an upper region of the interconnect layer.

The oxidation-resistant conductor film may be made of titanium nitride.

The interconnect layer comprises a first interconnect layer. The oxidation-resistant conductor film comprises a first oxidation-resistant conductor film provided on the first interconnect layer. The conductor contact portion comprises a first conductor contact
20 portion. The device comprises: a second interconnect layer provided in at least an upper portion of the first insulating film; a second oxidation-resistant conductor film covering the top of the second interconnect layer; and a second conductor contact portion passing through the third insulating film and the second insulating film to reach the second oxidation-resistant conductor film. The first conductor contact portion has a greater upper
25 surface area than the second conductor contact portion. In this case, if the third insulating film and the second insulating film are partly removed in forming these conductor contact portions, the region where the first conductor contact portion is formed is removed deeper.

However, since the top of the first interconnect layer is covered with the oxidation resistant film, corrosion of the first interconnect layer can be prevented even though the oxidation resistant film is exposed.

The first conductor contact portion may be of rectangular or strip-like plane, and
5 the second conductor contact portion may be of circular or square plane.

The first interconnect layer and the first conductor contact portion may constitute a seal ring provided in ring shape. In this case, even though the first conductor contact portion serving as the seal ring differs greatly in area from the second conductor contact portion, the structure described above can prevent the first interconnect layer from being
10 exposed.

An element may be provided in the semiconductor substrate, and the interconnect layer may be electrically connected to the element. In this case, when the third insulating film and the second insulating film are partly removed in forming the conductor contact portion, an error would arise in the depth to be removed. Even though such an error arises,
15 it can become difficult to expose the interconnect layer.

The second insulating film is preferably an insulating film of silicon compound containing carbon.

A first method for fabricating a semiconductor device according to the present invention comprises: the step (a) of forming a first insulating film on a semiconductor
20 substrate; the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film; the step (c) of forming a recess in an upper portion of the interconnect layer; the step (d) of forming, on the first insulating film and the interconnect layer, a second insulating film filling the recess; the step (e) of planarizing an upper surface of the second insulating film; the step (f) of forming a third insulating film on the second
25 insulating film after the step (e); the step (g) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located above the interconnect layer so that the removed part does not reach the interconnect layer, thereby

leaving part of the second insulating film on the interconnect layer; and the step (h) of removing the photoresist.

With this method, the portion of the second insulating film located on the interconnect layer can be formed thick. Therefore, in the step (g), the state in which the interconnect layer is not exposed can be kept more certainly. This prevents corrosion of the interconnect layer even though treatment that may corrode metal, such as ashing, is carried out after the step (g). On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed thick. Therefore, in the semiconductor device fabricated by the first method, the dielectric constant between the layers can be kept constant.

In the step (c), the upper portion of the interconnect layer may be recessed by chemical mechanical polishing, dry etching, or wet etching to form the recess. In this case, in addition to the above effect, the effect of improving the adhesion between the first insulating film and the second insulating film can be provided.

In the step (b), a first interconnect layer for a seal ring and a second interconnect layer located in a region surrounded with the first interconnect layer may be formed as the interconnect layer. In the step (c), the recess may be formed in at least an upper portion of the first interconnect layer. In the step (g), portions of the third insulating film and the second insulating film located above the first interconnect layer may be partly removed to form a trench for the seal ring, and portions of the third insulating film and the second insulating film located above the second interconnect layer may be partly removed to form a hole. Since, in this case, the opening area of the trench is greater than that of the hole, the trench is formed to have a greater depth than the hole in the step (g). However, the region of the second insulating film to be formed with the trench is formed thick, whereby it can become difficult to expose the first interconnect layer.

In the step (b), the first interconnect layer may be formed to have a greater width than the second interconnect layer. In this case, the region where the first interconnect

layer is formed has a higher area ratio of conductor (metal) than the region where the second interconnect layer is formed. Therefore, when, in the step (c), chemical mechanical polishing or similar treatment is carried out on the first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

In the step (b), a dummy interconnect layer may be formed beside the first interconnect layer. In this case, the surrounding of the region where the first interconnect layer is formed has a higher area ratio of conductor (metal) than the surrounding of the region where the second interconnect layer is formed. Therefore, when, in the step (c), chemical mechanical polishing or similar treatment is carried out on the first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

The first method may further comprise, prior to the step (a), the step (i) of forming an element in the semiconductor substrate. In the step (b), the interconnect layer may be formed to be electrically connectable to the element. In this case, even though an error in the depth to be removed arises in the step (g), it can become difficult to expose the interconnect layer.

A second method for fabricating a semiconductor device according to the present invention comprises: the step (a) of forming a first insulating film on a semiconductor substrate; the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film; the step (c) of forming an oxidation-resistant conductor film covering the top of the interconnect layer; the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film; the step (e) of forming a third insulating film on the second insulating film; the step (f) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located above the interconnect layer; and the step (g) of removing the photoresist.

With this method, the oxidation-resistant conductor film can cover the top of the interconnect layer. Therefore, in the step (f), even if treatment that may corrode metal, such as ashing, is carried out after exposure of the oxidation-resistant conductor film, corrosion of the interconnect layer can be prevented. On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed thick. Therefore, in the semiconductor device fabricated by the second method, the dielectric constant between the layers can be kept constant.

In the step (c), plasma treatment, wet treatment, or ion implantation may be performed to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film.

In the step (c), a film containing nitrogen may be deposited, as the oxidation-resistant conductor film, on the interconnect layer.

In the step (b), a first interconnect layer for a seal ring and a second interconnect layer located in a region surrounded with the first interconnect layer may be formed as the interconnect layer. In the step (c), an oxidation-resistant conductor film may be formed on the first interconnect layer and the second interconnect layer. In the step (f), portions of the third insulating film and the second insulating film located above the first interconnect layer may be partly removed to form a trench for the seal ring, and portions of the third insulating film and the second insulating film located above the second interconnect layer may be partly removed to form a hole. Since, in this case, the opening area of the trench is greater than that of the hole, the trench is formed to have a greater depth than the hole in the step (f). However, the region of the second insulating film to be formed with the trench is formed thick, whereby it can become difficult to expose the first interconnect layer.

The second method may further comprise, prior to the step (a), the step (h) of forming an element in the semiconductor substrate, and in the step (b), the interconnect layer may be formed to be electrically connectable to the element. In this case, even though an error in the depth to be removed arises in the step (f), it can become difficult to

expose the interconnect layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1A** to **1F** are sectional views showing a semiconductor device fabrication
5 method according to a first embodiment.

FIGS. **2A** to **2F** are sectional views showing a semiconductor device fabrication
method according to a second embodiment.

FIGS. **3A** to **3E** are sectional views showing a semiconductor device fabrication
method according to a third embodiment.

10 FIGS. **4A** to **4E** are sectional views showing a semiconductor device fabrication
method according to a fourth embodiment.

FIGS. **5A** to **5F** are sectional views showing a fabrication method of an
interconnect region of a semiconductor device according to a fifth embodiment.

15 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a first
embodiment of the present invention will be described with reference to FIGS. **1A** to **1F**.
FIGS. **1A** to **1F** are sectional views showing the semiconductor device fabrication method
20 of the first embodiment. Note that FIGS. **1A** to **1F** show an interconnect formation region
R1 and a seal ring region **R2** for protecting the interconnect formation region **R1** against
outside moisture. The seal ring region **R2** surrounds the sides of the interconnect
formation region **R1**.

First, in the step shown in FIG **1A**, a first insulating film **101** of a silicon oxide film
25 having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first
insulating film **101**, a photoresist (not shown) having openings in interconnect trace
formation positions is formed by photolithography. The formed photoresist is used as a

mask to perform dry etching, thereby removing part of the first insulating film **101** to form interconnect grooves **108** and **109** with a depth of 250 nm. Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper
5 film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first metal interconnect **102** consisting of a conductor surface film **102a** and a metal interconnect film **102b**. The conductor surface film **102a** covers the inside surface of the interconnect groove **108**, and the metal interconnect film **102b** fills the interconnect groove **108** with the conductor surface film **102a** interposed
10 between the first insulating film **101** and the metal interconnect film **102b**. During this formation, in the seal ring region **R2**, a second metal interconnect **103** is formed which consists of a conductor surface film **103a** and a metal interconnect film **103b**.

In the step shown in FIG **1B**, by chemical mechanical polishing or selective metal etching with nitric acid or the like, the upper portions of the first metal interconnect **102**
15 and the second metal interconnect **103** are recessed to form recessed shapes (recesses **110**) having depths of about 20 to 40 nm.

Next, in the step shown in FIG **1C**, on the substrate, a second insulating film **104** is deposited which is made of a silicon carbon nitride film with a thickness of 100 to 150 nm and which fills the recess **110**. In this deposition, as the material for the second insulating
20 film **104**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **104**.

At the time of this deposition, depressions affected by the recess shapes of the first metal interconnect **102** and the second metal interconnect **103** are created in the upper
25 surface of the second insulating film **104**.

Then, in the step shown in FIG **1D**, chemical mechanical polishing, wet etching with sulfuric acid, nitric acid, or the like or etch back is performed to planarize the upper

surface of the second insulating film **104**. By this planarization, portions of the second insulating film **104** located on the first metal interconnect **102** and the second metal interconnect **103** have thicknesses of about 70 to 90 nm and the remaining portions thereof have a thickness of 50 nm.

5 In the step shown in FIG **1E**, a third insulating film **105** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **105**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **105**.

10 Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region and a trench formation region is formed on the third insulating film **105**. Then, dry etching is performed using the photoresist as a mask to form a hole (through hole) **106** in the interconnect formation region **R1** and a trench **107** in the seal ring region **R2**. This dry etching is performed so that the hole **106** and the trench
15 **107** extend halfway through the second insulating film **104**. Since, in this etching, the opening area of the trench **107** is greater than that of the hole **106**, the trench **107** is etched deeper. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

 In the step shown in FIG **1F**, the remaining portions of the second insulating film
20 **104** within the hole and trench are etched, whereby the hole **106** and the trench **107** reach the first metal interconnect **102** and the second metal interconnect **103**, respectively. The resulting hole and trench are filled with a conductor to form a hole-contact portion **106'** made of conductor (referred hereinafter to as a conductor hole-contact portion) in circular or square plane and a trench-contact portion **107'** of conductor (referred hereinafter to as a
25 conductor trench-contact portion) in ring shape. This step is performed after completion of processes that may corrode metal, such as ashing and polymer removal.

 With reference to FIG **1F** again, next description will now be made of the structure

of the interconnect and the seal ring of the semiconductor device according to the first embodiment.

As shown in FIG 1F, the semiconductor device of the first embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of the interconnect formation region **R1**. The interconnect formation region **R1** is provided with the first metal interconnect **102**, and the seal ring region **R2** is provided with the second metal interconnect **103**. The first metal interconnect **102** includes the conductor surface film **102a** covering the surface of the interconnect groove **108** and the metal interconnect film **102b** covering the conductor surface film **102a**. Likewise, the second metal interconnect **103** includes the conductor surface film **103a** covering the surface of the interconnect groove **109** and the metal interconnect film **103b** provided on the conductor surface film **103a**. The upper portions of the first metal interconnect **102** and the second metal interconnect **103** are recessed to form the recesses **110**.

The second insulating film **104** is provided on the first insulating film **101**, the first metal interconnect **102** and the second metal interconnect **103**. The second insulating film **104** fills the recess **110**, so that in the second insulating film **104**, the portions thereof located on the first metal interconnect **102** and the second metal interconnect **103** are formed thicker than the other portions thereof. The upper surface of the second insulating film **104** is planarized.

The third insulating film **105** is provided on the second insulating film **104**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **106'** passing through the third insulating film **105** and the second insulating film **104**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **107'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **103** and the conductor trench-contact portion **107'** is provided to surround the first metal interconnect **102** and the conductor hole-contact portion **106'** in the interconnect formation region **R1**.

The effects obtained by the first embodiment will be described below in comparison with the conventional device.

In the conventional device, the upper surfaces of the first metal interconnect and the second metal interconnect remain flat, and the second insulating film with a uniform thickness is formed on the first metal interconnect and the second metal interconnect. By such a structure, when the hole and the trench are formed, the trench might pass through the second insulating film to expose the second metal interconnect.

In contrast to this, in the first embodiment, only the portions of the second insulating film **104** located on the first metal interconnect **102** and the second metal interconnect **103** can be formed thick. This prevents the trench **107** from reaching the second metal interconnect **103**. Therefore, even if ashing and polymer removal are performed on the semiconductor surface, the first metal interconnect **102** will not corrode. On the other hands, the portion of the second insulating film **104** located on the first insulating film **101** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, chemical mechanical polishing or selective etching is performed to recess the upper surfaces of the first metal interconnect **102** and the second metal interconnect **103**. This improves the adhesion between the first insulating film **101** and the second insulating film **104**.

In the first embodiment, by chemical mechanical polishing or the like, the recessed shapes are formed in the upper portions of the first metal interconnect **102** and the second metal interconnect **103**. However, in the present invention, the recessed shape may be formed by utilizing the property of copper in which copper is compressed by heat added thereto. To be more specific, in the step shown in FIG **1A**, the first metal interconnect **102** and the second metal interconnect **103** are formed and then heat treatment is performed at 200 to 500°C. This compresses the metal interconnect films **102b** and **103b** made of copper to form recesses in the upper portions of the first metal interconnect **102** and the

second metal interconnect **103**. Also by this procedure, the same effects as those described above can be obtained.

(Second Embodiment)

5 Hereinafter, a method for fabricating a semiconductor device according to a second embodiment of the present invention will be described with reference to FIGS. **2A** to **2F**. FIGS. **2A** to **2F** are sectional views showing the semiconductor device fabrication method of the second embodiment. Note that FIGS. **2A** to **2F** show an interconnect formation region **R1** and a seal ring region **R2** for protecting the interconnect formation region **R1**
10 against outside moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region **R1**.

 First, in the step shown in FIG **2A**, a first insulating film **111** of a silicon oxide film having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **111**, a photoresist (not shown) having openings in a metal interconnect trace
15 formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby forming an interconnect groove **118** in the interconnect formation region **R1** and an interconnect groove **119** in the seal ring formation region **R2**. In this etching, the width of the interconnect groove **119** is made greater than that of the interconnect groove **118**. To be more specific, when the interconnect groove **118** has a
20 width smaller than 2 μm , the interconnect groove **119** has a width of 2 μm or greater.

 Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first
25 metal interconnect **112** having a width of 2 μm or greater and consisting of a conductor surface film **112a** and a metal interconnect film **112b**. The conductor surface film **112a** covers the inside surface of the interconnect groove **118**, and the metal interconnect film

112b fills the interconnect groove **118** with the conductor surface film **112a** interposed between the first insulating film **111** and the metal interconnect film **112b**. During this formation, in the seal ring region **R2**, a second metal interconnect **113** with a width of 2 μm or greater is formed which consists of a conductor surface film **113a** and a metal
5 interconnect film **113b**.

In the step shown in FIG **2B**, chemical mechanical polishing is performed. In this step, the upper portion of the second metal interconnect **113** is recessed by utilizing the metal area ratio dependence of dishing. Details of this step are as follows. If a substrate with metal embedded therein is subjected to chemical mechanical polishing, the depth to
10 which the metal is removed tends to be greater as the percentage of metal contained in the region to be removed rises. In the second embodiment, the second metal interconnect **113** is formed to have a greater width than the first metal interconnect **112**. In other words, the region where the second metal interconnect **113** is formed has a higher ratio of metal per unit area. This allows the upper portion of the second metal interconnect **113** to be
15 recessed deeper than the other regions.

As a substitute for the method in which the depth of the second metal interconnect **113** is made greater than that of the first metal interconnect **112**, the percentage of metal content per unit area may be raised by forming a dummy pattern around the second metal interconnect **113**.

20 Next, in the step shown in FIG **2C**, a second insulating film **114** made of a silicon carbon nitride film is deposited on the first insulating film **111**, the first metal interconnect **112** and the second metal interconnect **113**. In this deposition, as the material for the second insulating film **114**, use may be made of a silicon nitride film, a silicon oxide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films
25 may be formed as the second insulating film **114**.

At the time of this deposition, a depression affected by the recess shape of the second metal interconnect **113** is created in the upper portion of the second insulating film

114.

Then, in the step shown in FIG **2D**, chemical mechanical polishing, wet etching, or etch back is performed to planarize the second insulating film **114**.

In the step shown in FIG **2E**, a third insulating film **115** made of a carbon-
5 containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **115**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **115**.

Subsequently to this, by photolithography, a photoresist (not shown) having
10 openings in a hole formation region and a trench formation region is formed on the third insulating film **115**. Then, dry etching is performed using the photoresist as a mask to form a hole **116** in the interconnect formation region **R1** and a trench **117** in the seal ring region **R2**. This dry etching is performed so that the trench **117** extends halfway through the second insulating film **114**. Since, in this etching, the opening area of the trench **117** is
15 greater than that of the hole **116**, the trench **117** is etched deeper. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG **2F**, the remaining portions of the second insulating film **114** within the hole and trench are removed, whereby the hole **116** and the trench **117** reach
20 the first metal interconnect **112** and the second metal interconnect **113**, respectively. The resulting hole and trench are filled with a conductor to form a conductor hole-contact portion **116'** in circular or square plane and a conductor trench-contact portion **117'** in ring shape. This step is performed after completion of processes that may corrode metal, such as ashing and polymer removal.

25 With reference to FIG **2F** again, next description will now be made of the structure of the interconnect and the seal ring of the semiconductor device according to the second embodiment.

As shown in FIG 2F, the semiconductor device of the second embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of the interconnect formation region **R1**. The interconnect formation region **R1** is provided with the first metal interconnect **112**, and the seal ring region **R2** is provided with the
5 second metal interconnect **113**. The second metal interconnect **113** is formed to have a greater width than the first metal interconnect **112**.

The first metal interconnect **112** includes the conductor surface film **112a** covering the surface of the interconnect groove **118** and the metal interconnect film **112b** covering the conductor surface film **112a**. Likewise, the second metal interconnect **113** includes the
10 conductor surface film **113a** covering the surface of the interconnect groove **119** and the metal interconnect film **113b** provided on the conductor surface film **113a**. The upper portion of the second metal interconnect **113** is recessed to form a recess **120**.

The second insulating film **114** is provided on the first insulating film **111**, the first metal interconnect **112** and the second metal interconnect **113**. The second insulating film
15 **114** fills the recess **120**, so that in the second insulating film **114**, the portion thereof located on the second metal interconnect **113** is formed thicker than the other portions thereof. The upper surface of the second insulating film **114** is planarized.

The third insulating film **115** is provided on the second insulating film **114**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **116'**
20 passing through the third insulating film **115** and the second insulating film **114**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **117'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **113** and the conductor trench-contact portion **117'** is provided to surround the first metal interconnect **112** and the conductor hole-contact portion **116'** in the interconnect formation
25 region **R1**.

The effects obtained by the second embodiment will be described below in comparison with the conventional device.

In the conventional device, the upper surface of the second metal interconnect remains flat, and the second insulating film with a uniform thickness is formed on the second metal interconnect. By such a structure, when the hole and the trench are formed, the trench might pass through the second insulating film to expose the second metal
5 interconnect.

In contrast to this, in the second embodiment, only the portion of the second insulating film **114** located on the second metal interconnect **113** can be formed thick without increasing the number of fabrication steps of the device. This prevents the trench **117** from reaching the second metal interconnect **113**. Therefore, even if ashing and
10 polymer removal are performed on the semiconductor surface, the first metal interconnect will not corrode. On the other hands, the portion of the second insulating film **114** located on the first insulating film **111** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, chemical mechanical polishing or etching is performed to recess the
15 upper portion of the second metal interconnect **113**. This improves the adhesion between the first insulating film **111** and the second insulating film **114**.

In the second embodiment, the recessed shape is formed by utilizing the metal area ratio dependence of dishing. However, it may be formed by etching utilizing the pattern density dependence. Alternatively, in the step shown in FIG **2B** in the present invention,
20 the recessed shape may be formed in the upper portion of the second metal interconnect **113** by performing etching with a photoresist or the like covering all the region but the second metal interconnect **113**. In this case, the same effects as those described above can be obtained except that the number of fabrication steps of the device increases.

In the second embodiment, in performing chemical mechanical polishing in the step
25 shown in FIG **2B**, slurry with high solubility, such as hydrogen peroxide, may be used. This raises the polishing rate of metal, which allows the second metal interconnect **113** to be recessed deeper.

(Third Embodiment)

A method for fabricating a semiconductor device according to a third embodiment of the present invention will be described with reference to FIGS. 3A to 3E. FIGS. 3A to 3E are sectional views showing the semiconductor device fabrication steps of the third embodiment. Note that FIGS. 3A to 3E show an interconnect formation region **R1** and a seal ring region **R2** for protecting the interconnect formation region **R1** against outside moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region **R1**.

First, in the step shown in FIG 3A, a first insulating film **121** of a silicon oxide film having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **121**, a photoresist (not shown) having openings in a metal interconnect trace formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby removing part of the first insulating film **121** to form interconnect grooves **128** and **129** with a depth of 250 nm. Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first metal interconnect **122** consisting of a conductor surface film **122a** and a metal interconnect film **122b**. The conductor surface film **122a** covers the inside surface of the interconnect groove **128**, and the metal interconnect film **122b** fills the interconnect groove **128** with the conductor surface film **122a** interposed between the first insulating film **121** and the metal interconnect film **122b**. During this formation, in the seal ring region **R2**, a second metal interconnect **123** is formed which consists of a conductor surface film **123a** and a metal interconnect film **123b**.

In the step shown in FIG 3B, plasma treatment using a gas containing nitrogen, wet treatment using ammonia, benzotriazole (BTA), or quinaldic acid, or ion implantation is

performed to supply nitrogen to the upper portions of the first metal interconnect **122** and the second metal interconnect **123**. This alters the upper portions of the first metal interconnect **122** and the second metal interconnect **123** into an oxidation resistant film **130**. Simultaneously, this step can improve the adhesion between the first insulating film **121** and a second insulating film **124** that will be formed in a subsequent step.

Next, in the step shown in FIG **3C**, the second insulating film **124** made of a silicon carbon nitride film is deposited on the first insulating film **121** and the oxidation resistant film **130**. In this deposition, as the material for the second insulating film **124**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **124**.

In the step shown in FIG **3D**, a third insulating film **125** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **125**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **125**.

Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region and a trench formation region is formed on the third insulating film **125**. Then, dry etching is performed using the photoresist as a mask to form a hole **126** in the interconnect formation region **R1** and a trench **127** in the seal ring region **R2**. This dry etching may be performed either so that the trench **127** extends only halfway through the second insulating film **124** or so that the trench **127** passes through the second insulating film **124** to reach the oxidation resistant film **130**. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG **3E**, the remaining portions of the second insulating film **124** within the hole and trench are removed, whereby the hole **126** and the trench **127**

reach the oxidation resistant film **130**. The resulting hole and trench are filled with a conductor to form a conductor hole-contact portion **126'** in circular or square plane and a conductor trench-contact portion **127'** in ring shape.

With reference to FIG **3E** again, next description will now be made of the structure of the interconnect and the seal ring of the semiconductor device according to the third embodiment.

As shown in FIG **3E**, the semiconductor device of the third embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of the interconnect formation region **R1**. The interconnect formation region **R1** is provided with the first metal interconnect **122**, and the seal ring region **R2** is provided with the second metal interconnect **123**. The first metal interconnect **122** includes the conductor surface film **122a** covering the surface of the interconnect groove **128** and the metal interconnect film **122b** covering the conductor surface film **122a**. Likewise, the second metal interconnect **123** includes the conductor surface film **123a** covering the surface of the interconnect groove **129** and the metal interconnect film **123b** provided on the conductor surface film **123a**. The upper portions of the metal interconnect films **122b** and **123b** contain nitrogen and thus are formed into the oxidation resistant film **130**.

The second insulating film **124** is provided on the first insulating film **121**, the first metal interconnect **122** and the second metal interconnect **123**. The third insulating film **125** is provided on the second insulating film **124**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **126'** passing through the third insulating film **125** and the second insulating film **124**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **127'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **123** and the conductor trench-contact portion **127'** is provided to surround the first metal interconnect **122** and the conductor hole-contact portion **126'** in the interconnect formation region **R1**.

The effects obtained by the third embodiment will be described below in

comparison with the conventional device.

In the conventional device, if a trench reaches the second metal interconnect during formation of the hole pattern and the trench pattern, then the second metal interconnect corrodes in subsequent ashing and polymer removal.

5 In contrast to this, in the third embodiment, the upper portion of the second metal interconnect **123** is altered into the oxidation resistant film **130**. Therefore, even if ashing and polymer removal are performed in the state in which the trench **127** reaches the second metal interconnect **123**, the upper portion of the second metal interconnect **123** will not corrode. On the other hands, the portion of the second insulating film **124** located on the
10 first insulating film **121** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, the upper portions of the first metal interconnect **122** and the second metal interconnect **123** are made to contain nitrogen, which also provides the advantage that the etching resistance in the formation of the hole **126** and the trench **127** is improved.

15 In the step shown in FIG **3D**, in the case where the hole **126** and the trench **127** reach the oxidation resistant film **130**, the later step of removing portions of the second insulating film **124** remaining between the oxidation resistant film **130** and each of the hole **126** and the trench **127** can be advantageously omitted.

20 (Fourth Embodiment)

A method for fabricating a semiconductor device according to a fourth embodiment of the present invention will be described with reference to FIGS. **4A** to **4E**. FIGS. **4A** to **4E** are sectional views showing the semiconductor device fabrication steps of the fourth embodiment. Note that FIGS. **4A** to **4E** show an interconnect formation region **R1** and a
25 seal ring region **R2** for protecting the interconnect formation region **R1** against outside moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region **R1**.

First, in the step shown in FIG 4A, a first insulating film **131** of a silicon oxide film having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **131**, a photoresist (not shown) having openings in a metal interconnect trace formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby removing part of the first insulating film **131** to form interconnect grooves **138** and **139** with a depth of 250 nm. Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first metal interconnect **132** consisting of a conductor surface film **132a** and a metal interconnect film **132b**. The conductor surface film **132a** covers the inside surface of the interconnect groove **138**, and the metal interconnect film **132b** fills the interconnect groove **138** with the conductor surface film **132a** interposed between the first insulating film **131** and the metal interconnect film **132b**. During this formation, in the seal ring region **R2**, a second metal interconnect **133** is formed which consists of a conductor surface film **133a** and a metal interconnect film **133b**.

In the step shown in FIG 4B, an oxidation-resistant metal film **140** is selectively deposited on the first metal interconnect **132** and the second metal interconnect **133**. An exemplary material for the metal film **140** is titanium nitride (TiN).

Next, in the step shown in FIG 4C, a second insulating film **134** made of a silicon carbon nitride film is deposited on the first insulating film **131** and the metal film **140**. In this deposition, as the material for the second insulating film **134**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **134**. Subsequently to the deposition, chemical mechanical polishing, wet etching, or etch back is performed to planarize the second insulating film **134**.

In the step shown in FIG 4D, a third insulating film **135** made of a carbon-

containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **135**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **135**.

5 Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region and a trench formation region is formed on the third insulating film **135**. Then, dry etching is performed using the photoresist as a mask to form a hole **136** in the interconnect formation region **R1** and a trench **137** in the seal ring region **R2**. This dry etching may be performed either so that the trench **137** extends only
10 halfway through the second insulating film **134** or so that the trench **137** passes through the second insulating film **134** to reach the metal film **140**. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

 In the step shown in FIG **4E**, the remaining portions of the second insulating film **134** within the hole and trench are removed, whereby the hole **136** and the trench **137**
15 reach the first metal interconnect **132** and the second metal interconnect **133**, respectively. The resulting hole and trench are filled with a conductor to form a conductor hole-contact portion **136'** in circular or square plane and a conductor trench-contact portion **137'** in ring shape.

 With reference to FIG **4E** again, next description will now be made of the structure
20 of the interconnect and the seal ring of the semiconductor device according to the fourth embodiment.

 As shown in FIG **4E**, the semiconductor device of the fourth embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of the interconnect formation region **R1**. The interconnect formation region **R1** is provided
25 with the first metal interconnect **132**, and the seal ring region **R2** is provided with the second metal interconnect **133**. The first metal interconnect **132** includes the conductor surface film **132a** covering the surface of the interconnect groove **138** and the metal

interconnect film **132b** covering the conductor surface film **132a**. Likewise, the second metal interconnect **133** includes the conductor surface film **133a** covering the surface of the interconnect groove **139** and the metal interconnect film **133b** provided on the conductor surface film **133a**.

5 The oxidation-resistant metal film **140** made of, for example, titanium nitride is provided on the first metal interconnect **132** and the second metal interconnect **133**. The second insulating film **134** is provided on the first insulating film **131** and the metal film **140**. The third insulating film **135** is provided on the second insulating film **134**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **136'**
10 passing through the third insulating film **135** and the second insulating film **134**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **137'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **133** and the conductor trench-contact portion **137'** is provided to surround the first metal interconnect **132** and the conductor hole-contact portion **136'** in the interconnect formation
15 region **R1**.

 In the fourth embodiment, the metal film **140** resistant to oxidation covers the top of the second metal interconnect **133**. Therefore, even if ashing and polymer removal are performed in the state in which the trench **137** reaches the metal film **140**, the upper portion of the second metal interconnect **133** will not corrode. On the other hands, the
20 portion of the second insulating film **134** located on the first insulating film **131** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

 Moreover, the upper portions of the first metal interconnect **132** and the second metal interconnect **133** are formed with the metal film **140** resistant to oxidation, which also provides the advantage that the etching resistance in the formation of the hole **136** and
25 the trench **137** is improved.

(Fifth Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a fifth embodiment of the present invention will be described with reference to FIGS. **5A** to **5F**. FIGS. **5A** to **5F** are sectional views showing a method for fabricating an interconnect region of a semiconductor device according to the fifth embodiment. The foregoing first to 5 fourth embodiments have shown the case where a difference in depth arises between the hole in the interconnect region and the trench in the seal ring region. On the other hands, the fifth embodiment shows the case where in forming a number of hole patterns in the interconnect region, a difference in depth arises among the hole patterns.

First, in the step shown in FIG **5A**, a first insulating film **141** of a silicon oxide film 10 having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **141**, a photoresist (not shown) having openings in a metal interconnect trace formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby removing part of the first insulating film **141** to form an interconnect groove **148** with a depth of 250 nm. Thereafter, the photoresist is removed, 15 and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper film and the stacked film are polished using chemical mechanical polishing to form a metal interconnect **142** consisting of a conductor surface film **142a** and a metal interconnect film **142b**. The conductor surface film **142a** covers the inside surface of the interconnect 20 groove **148**, and the metal interconnect film **142b** fills the interconnect groove **148** with the conductor surface film **142a** interposed between the insulating film **141** and the metal interconnect film **142b**.

In the step shown in FIG **5B**, by chemical mechanical polishing or selective metal etching with nitric acid or the like, the upper portion of the metal interconnect **142** is 25 recessed to form a recessed shape (recess **150**) having a depth of about 20 to 40 nm.

Next, in the step shown in FIG **5C**, on the substrate, a second insulating film **144** is deposited which is made of a silicon carbon nitride film with a thickness of 100 to 150 nm

and which fills the recess **150**. In this deposition, as the material for the second insulating film **144**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **144**.

5 At the time of this deposition, a depression affected by the recess shape of the metal interconnect **142** is created in the top of the second insulating film **144**.

Then, in the step shown in FIG **5D**, chemical mechanical polishing, wet etching or etch back is performed to planarize the upper surface of the second insulating film **144**. By this planarization, a portion of the second insulating film **144** located on the metal
10 interconnect **142** has a thickness of about 70 to 90 nm and the remaining portions thereof have a thickness of 50 nm.

In the step shown in FIG **5E**, a third insulating film **145** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **145**, use may be made of an FSG (fluorinated silicate glass) film, a
15 BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **145**.

Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region is formed on the third insulating film **145**. Then, dry etching is performed using the photoresist as a mask to form holes **146**. This dry etching is
20 performed so that the holes **146** extend halfway through the second insulating film **144**. At the time of completion of this etching, respective holes **146** of multiple hole patterns have different depths due to influences of the pattern density or the like. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

25 In the step shown in FIG **5F**, the remaining portions of the second insulating film **144** within the holes are removed, whereby the holes **146** reach the metal interconnect **142**. The resulting holes are filled with a conductor to form conductor hole-contact portions

146' in circular or square plane. This step is performed after completion of processes that may corrode metal, such as ashing and polymer removal.

With reference to FIG **5F** again, next description will now be made of the structure of the interconnect and the conductor hole-contact portion of the semiconductor device
5 according to the fifth embodiment.

As shown in FIG **5F**, in the semiconductor device of the fifth embodiment, the metal interconnect **142** which includes the conductor surface film **142a** and the metal interconnect film **142b** covering the top of the conductor surface film **142a** is provided in the first insulating film **141**. The upper portion of the metal interconnect **142** is recessed to
10 form the recess **150**.

The second insulating film **144** is provided on the first insulating film **141** and the metal interconnect **142**. The second insulating film **144** fills the recess **150**, so that in the second insulating film **144**, the portion thereof located on the metal interconnect **142** is formed thicker than the other portions thereof. The upper surface of the second insulating
15 film **144** is planarized.

The third insulating film **145** is provided on the second insulating film **144**. Further, the conductor hole-contact portion **146'** is provided which passes through the third insulating film **145** and the second insulating film **144**.

The effects obtained by the fifth embodiment will be described below in
20 comparison with the conventional device.

In the conventional device, the upper surface of the metal interconnect remains flat, and the second insulating film and the third insulating film are formed on the metal interconnect. If multiple types of hole patterns are formed in such a structure, the formed hole patterns have different hole depths due to nonuniform pattern densities or fabrication
25 process variations. This might cause some of the hole patterns to pass through the second insulating film to reach the metal interconnect. Such a possibility increases particularly in the case where a number of hole patterns are formed in the device.

In contrast to this, in the fifth embodiment, only the portion of the second insulating film **144** located on the metal interconnect **142** can be formed thick. This prevents the holes **146** from reaching the metal interconnect **142**. Therefore, even if ashing and polymer removal are performed on the semiconductor surface, the metal interconnect **142** will not corrode. On the other hands, the portion of the second insulating film **144** located on the first insulating film **141** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, chemical mechanical polishing or selective etching is performed to recess the upper surface of the metal interconnect **142**. This improves the adhesion between the first insulating film **141** and the second insulating film **144**.

The fifth embodiment is composed by applying the method of the first embodiment to the case where multiple types of hole patterns are formed in an interconnect region. However, in the present invention, methods of the third and fourth embodiments can also be applied to that case.

In the first to fourth embodiments, description has been made of the case where the conductor trench-contact portion is formed in ring shape to use the portion as the seal ring. Alternatively, the portion may be formed in rectangular shape or strip shape to use the portion as part of an electrode.

CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
 - 5 a semiconductor substrate;
 - a first insulating film provided over the semiconductor substrate;
 - an interconnect layer provided in at least an upper portion of the first insulating film;
 - a second insulating film provided on the first insulating film and the interconnect
 - 10 layer;
 - a third insulating film provided on the second insulating film; and
 - at least one conductor contact portion passing through the third insulating film and the second insulating film to reach the interconnect layer,
 - wherein an upper portion of the interconnect layer is provided with a recess and a
 - 15 portion of the second insulating film located on the interconnect layer has a greater thickness than a portion thereof located on the first insulating film.
2. The device of claim 1,
 - wherein the interconnect layer comprises a first interconnect layer,
 - the conductor contact portion comprises a first conductor contact portion,
 - 20 the device further comprises: a second interconnect layer provided in at least an upper portion of the first insulating film; and a second conductor contact portion passing through the third insulating film and the second insulating film to reach the second interconnect layer, and
 - a portion of the second insulating film located on the first interconnect layer has a
 - 25 greater thickness than a portion thereof located on the second interconnect layer.
3. The device of claim 2,
 - wherein the first interconnect layer has a greater width than the second interconnect

layer.

4. The device of claim 2,
wherein a dummy interconnect layer is formed beside the first interconnect layer.

5. The device of claim 2,
5 wherein the first conductor contact portion is of rectangular or strip-like plane, and
the second conductor contact portion is of circular or square plane.

6. The device of claim 2,
wherein the first interconnect layer and the first conductor contact portion
constitute a seal ring provided in ring shape.

10 7. The device of claim 1,
wherein an element is provided in the semiconductor substrate, and
the interconnect layer is electrically connected to the element.

8. The device of claim 1,
wherein the second insulating film is an insulating film of silicon compound
15 containing carbon.

9. A semiconductor device comprising:
a semiconductor substrate;
a first insulating film provided over the semiconductor substrate;
an interconnect layer provided in at least an upper portion of the first insulating
20 film;

an oxidation-resistant conductor film covering the top of the interconnect layer;
a second insulating film provided on the first insulating film and the oxidation-
resistant conductor film;
a third insulating film provided on the second insulating film; and
25 at least one conductor contact portion passing through the third insulating film and
the second insulating film to reach the oxidation-resistant conductor film.

10. The device of claim 9,

wherein the oxidation-resistant conductor film is a nitrogen introduced layer produced by introducing nitrogen into an upper region of the interconnect layer.

11. The device of claim 9,

wherein the oxidation-resistant conductor film is made of titanium nitride.

5 12. The device of claim 9,

wherein the interconnect layer comprises a first interconnect layer,

the oxidation-resistant conductor film comprises a first oxidation-resistant conductor film provided on the first interconnect layer,

the conductor contact portion comprises a first conductor contact portion,

10 the device comprises: a second interconnect layer provided in at least an upper portion of the first insulating film; a second oxidation-resistant conductor film covering the top of the second interconnect layer; and a second conductor contact portion passing through the third insulating film and the second insulating film to reach the second oxidation-resistant conductor film, and

15 the first conductor contact portion has a greater upper surface area than the second conductor contact portion.

13. The device of claim 12,

wherein the first conductor contact portion is of rectangular or strip-like plane, and the second conductor contact portion is of circular or square plane.

20 14. The device of claim 12,

wherein the first interconnect layer and the first conductor contact portion constitute a seal ring provided in ring shape.

15. The device of claim 9,

25 wherein an element is provided in the semiconductor substrate, and the interconnect layer is electrically connected to the element.

16. The device of claim 9,

wherein the second insulating film is an insulating film of silicon compound

containing carbon.

17. A method for fabricating a semiconductor device, comprising:

the step (a) of forming a first insulating film over a semiconductor substrate;

the step (b) of forming an interconnect layer in at least an upper portion of the first
5 insulating film;

the step (c) of forming a recess in an upper portion of the interconnect layer;

the step (d) of forming, on the first insulating film and the interconnect layer, a
second insulating film filling the recess;

the step (e) of planarizing an upper surface of the second insulating film;

10 the step (f) of forming a third insulating film on the second insulating film after the
step (e);

the step (g) of removing, using a photoresist as a mask, portions of the third
insulating film and the second insulating film located over the interconnect layer so that the
removed part does not reach the interconnect layer, thereby leaving part of the second
15 insulating film on the interconnect layer; and

the step (h) of removing the photoresist.

18. The method of claim 17,

wherein in the step (c), the upper portion of the interconnect layer is recessed by
chemical mechanical polishing, dry etching, or wet etching to form the recess.

20 19. The method of claim 17,

wherein in the step (b), a first interconnect layer and a second interconnect layer are
formed as the interconnect layer,

in the step (c), the recess is formed in at least an upper portion of the first
interconnect layer, and

25 in the step (g), portions of the third insulating film and the second insulating film
located above the first interconnect layer are partly removed to form a trench, and portions
of the third insulating film and the second insulating film located above the second

interconnect layer are partly removed to form a hole.

20. The method of claim 19,

wherein in the step (b), the first interconnect layer is formed to have a greater width than the second interconnect layer.

5 21. The method of claim 19,

wherein in the step (b), a dummy interconnect layer is formed beside the first interconnect layer.

22. The method of claim 17, further comprising, prior to the step (a), the step (i) of forming an element in the semiconductor substrate,

10 wherein in the step (b), the interconnect layer is formed to be electrically connectable to the element.

23. A method for fabricating a semiconductor device, comprising:

the step (a) of forming a first insulating film over a semiconductor substrate;

15 the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film;

the step (c) of forming an oxidation-resistant conductor film covering the top of the interconnect layer;

the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film;

20 the step (e) of forming a third insulating film on the second insulating film;

the step (f) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located over the interconnect layer; and

the step (g) of removing the photoresist.

24. The method of claim 23,

25 wherein in the step (c), plasma treatment, wet treatment, or ion implantation is performed to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film.

25. The method of claim 23,

wherein in the step (c), a film containing nitrogen is deposited, as the oxidation-resistant conductor film, on the interconnect layer.

26. The method of claim 23,

5 wherein in the step (b), a first interconnect layer and a second interconnect layer are formed as the interconnect layer,

in the step (c), an oxidation-resistant conductor film is formed on the first interconnect layer and the second interconnect layer, and

10 in the step (f), portions of the third insulating film and the second insulating film located over the first interconnect layer are removed to form a trench, and portions of the third insulating film and the second insulating film located over the second interconnect layer are removed to form a hole.

27. The method of claim 23, further comprising, prior to the step (a), the step (h) of forming an element in the semiconductor substrate,

15 wherein in the step (b), the interconnect layer is formed to be electrically connectable to the element.

ABSTRACT OF THE DISCLOSURE

In a method for fabricating a semiconductor device, first, a first metal interconnect is formed in an interconnect formation region, and a second metal interconnect is formed
5 in a seal ring region. Subsequently, by chemical mechanical polishing or etching, the upper portions of the first metal interconnect and the second metal interconnect are recessed to form recesses. A second insulating film filling the recesses is then formed above a substrate, and the upper portion of the second insulating film is planarized. Next, a hole and a trench are formed to extend halfway through the second insulating film, and
10 ashing and polymer removal are performed. Subsequently to this, the hole and the trench are allowed to reach the first metal interconnect and the second metal interconnect.

FIG. 1A

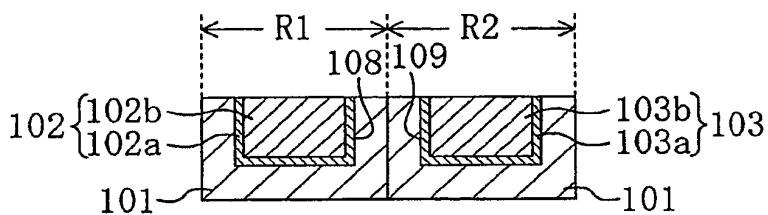


FIG. 1B

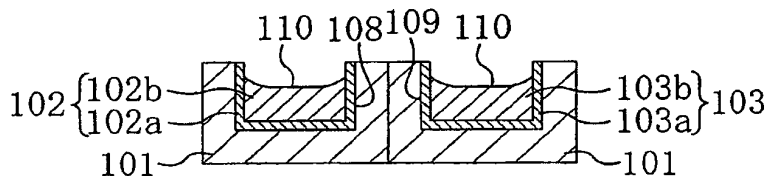


FIG. 1C

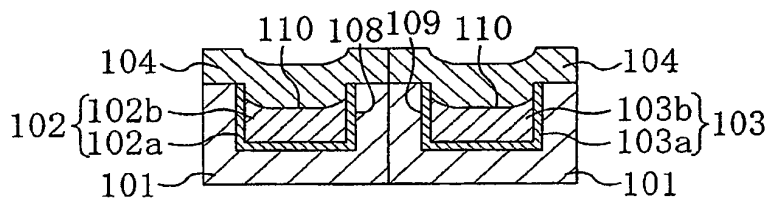


FIG. 1D

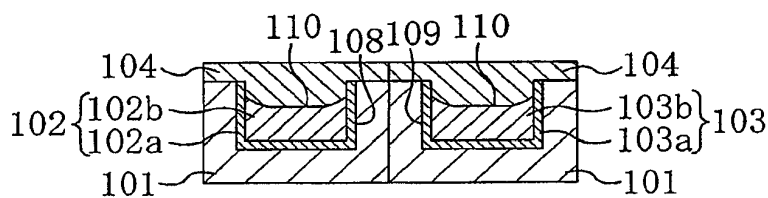


FIG. 1E

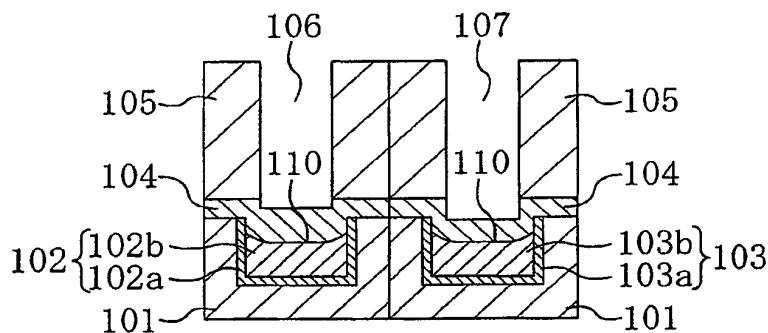


FIG. 1F

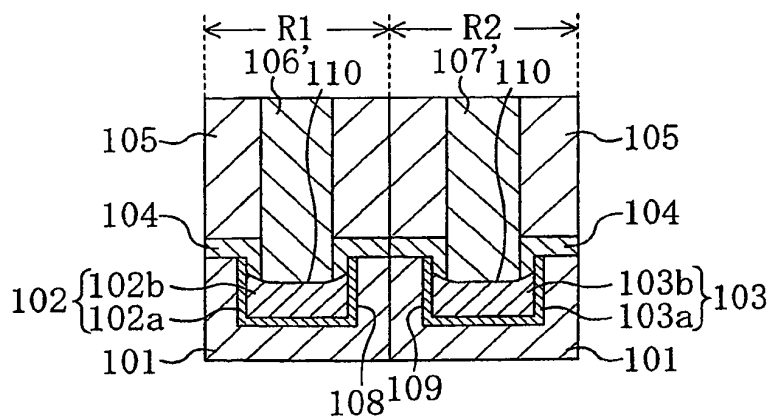


FIG. 2A

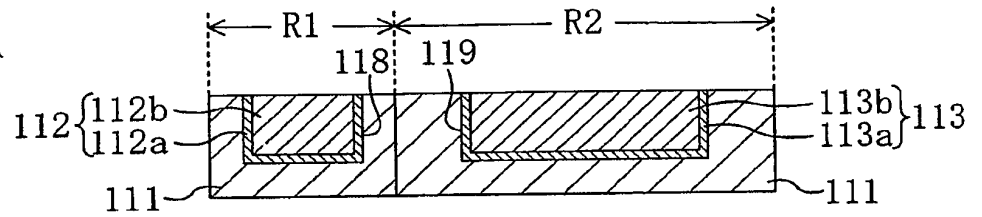


FIG. 2B

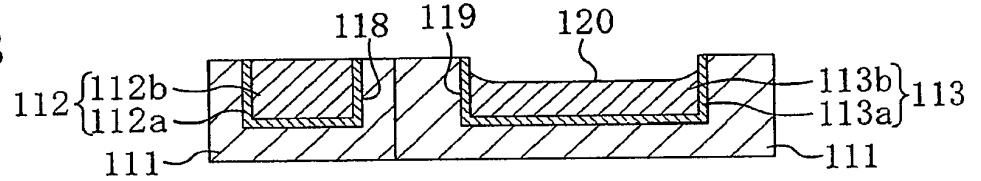


FIG. 2C

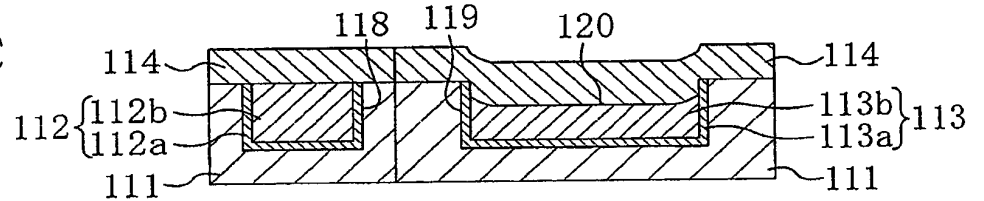


FIG. 2D

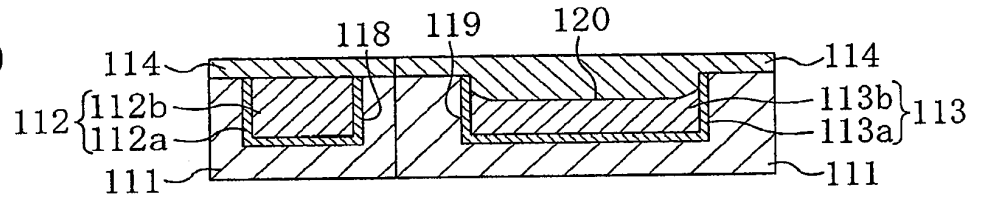


FIG. 2E

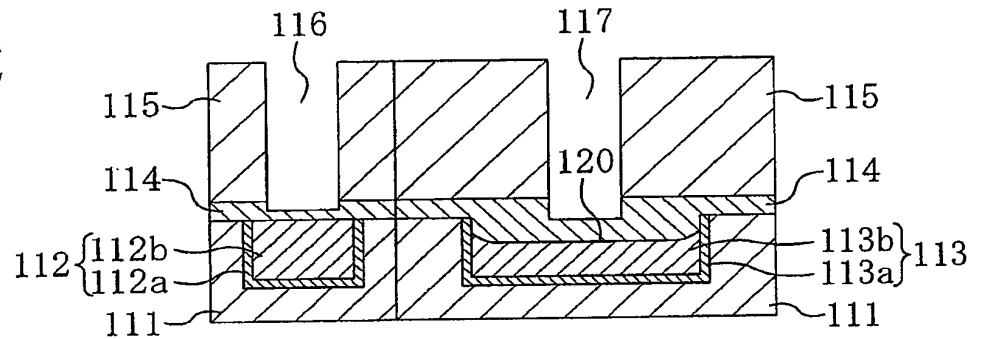


FIG. 2F

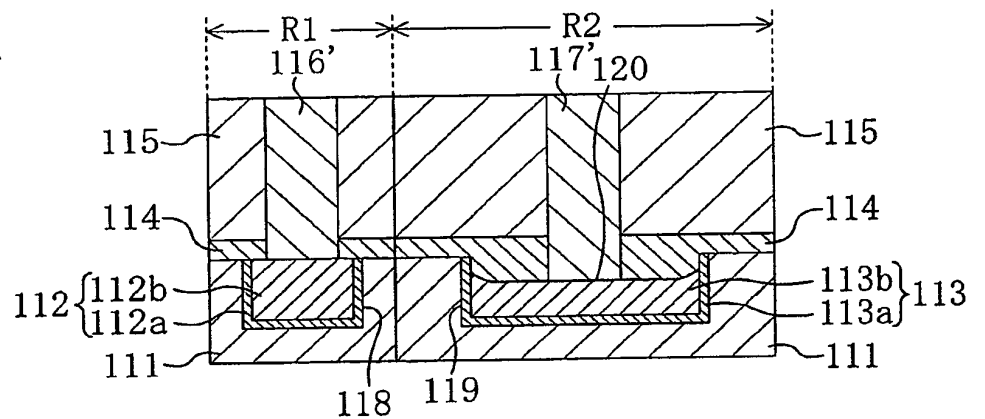


FIG. 3A

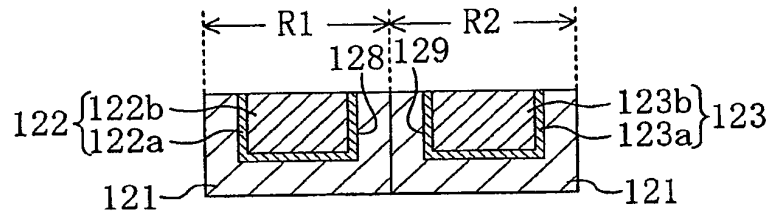


FIG. 3B

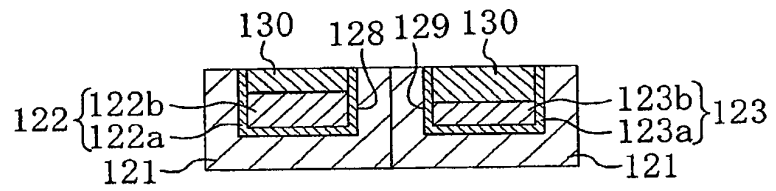


FIG. 3C

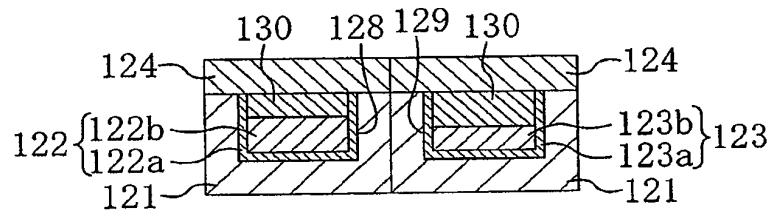


FIG. 3D

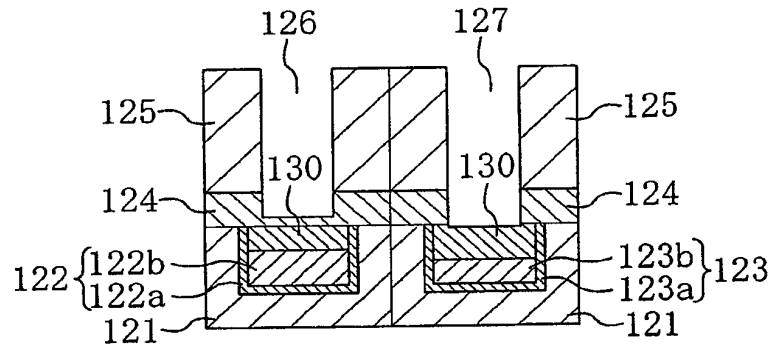


FIG. 3E

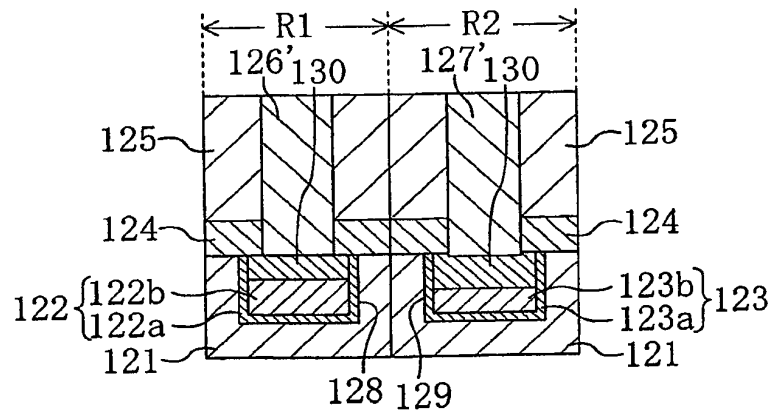


FIG. 4A

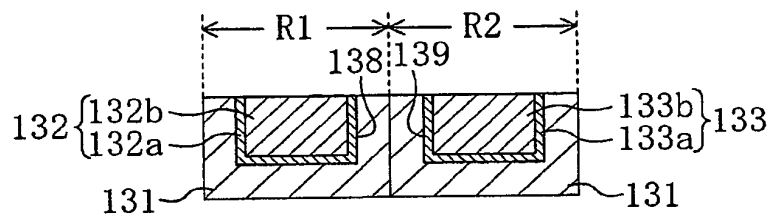


FIG. 4B

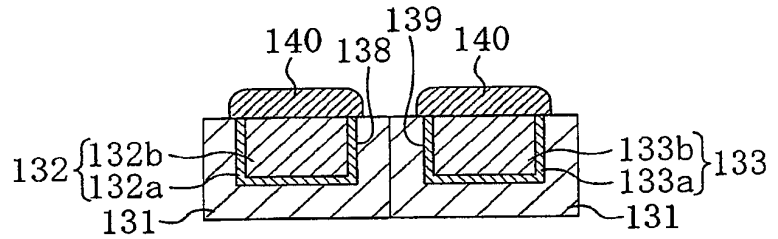


FIG. 4C

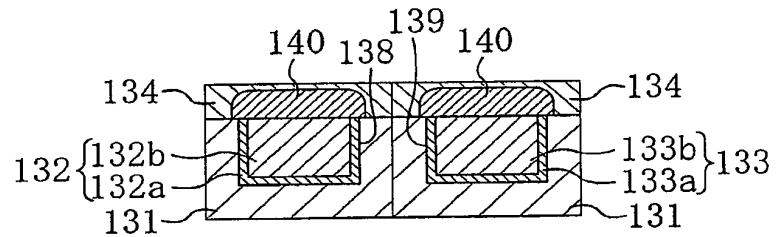


FIG. 4D

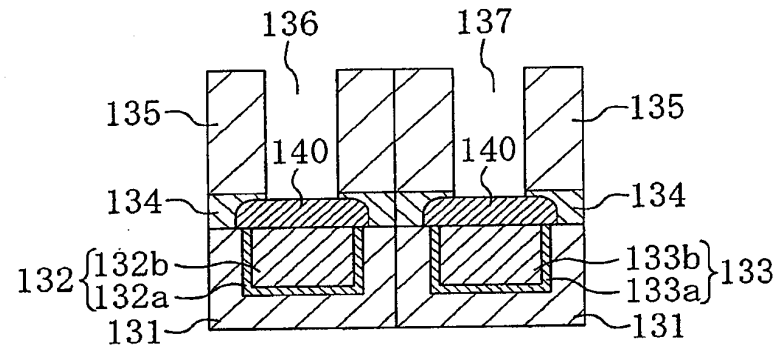


FIG. 4E

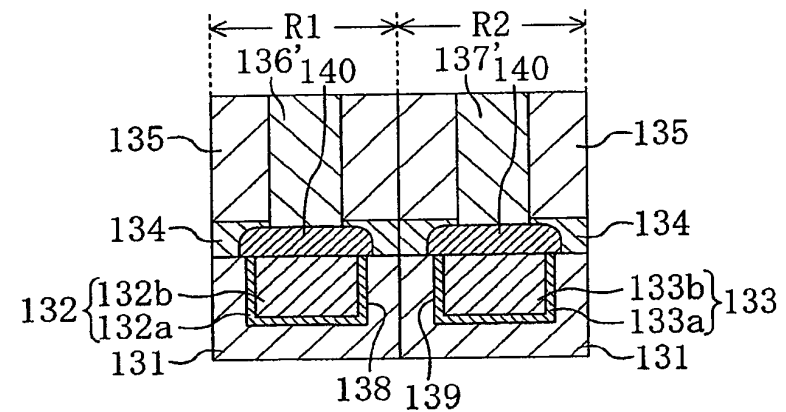


FIG. 5A

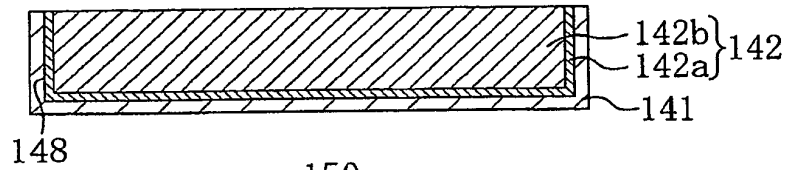


FIG. 5B

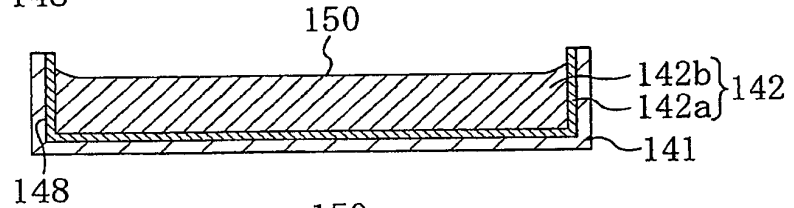


FIG. 5C

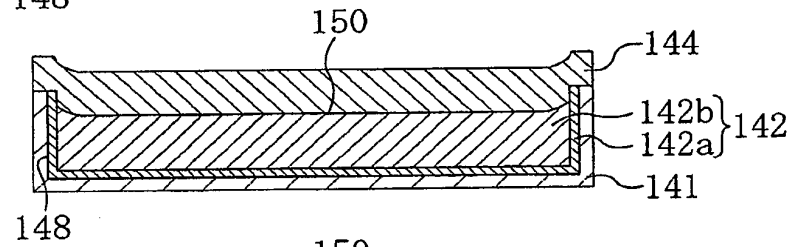


FIG. 5D

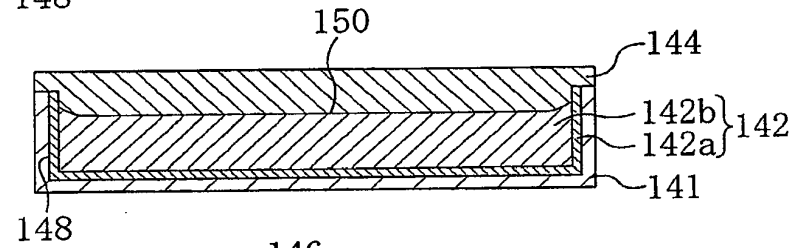


FIG. 5E

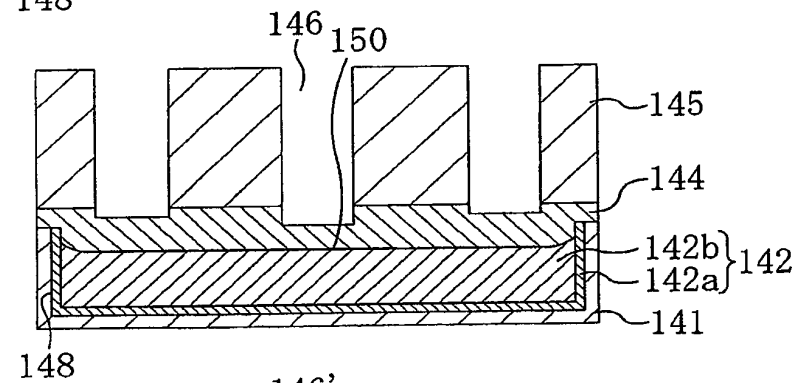
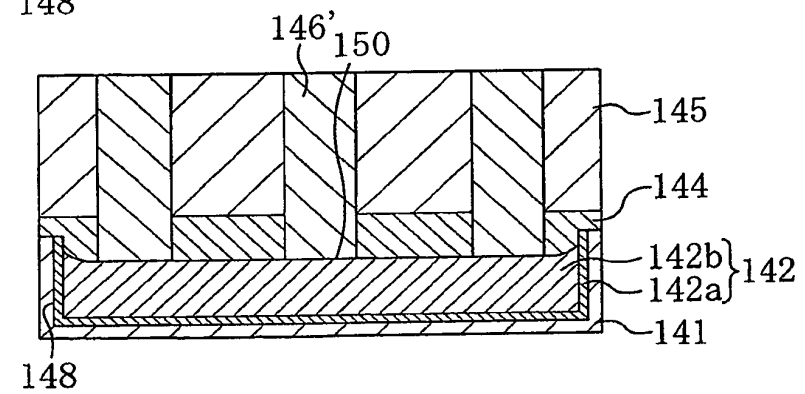


FIG. 5F



Docket No. _____

COMBINED DECLARATION/POWER OF ATTORNEY
FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

_____, the specification of which

(check one) X is attached hereto.

_____ was filed on _____ as
Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
<u>2003-335185</u> (Number)	<u>JAPAN</u> (Country)	<u>26/09/2003</u> (Day/Month/Year Filed)	<u> X </u> Yes ___ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Paul Devinsky (Reg. No. 28,553); Edward E. Kubasiewicz (Reg. No. 30,020), Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); and Wilhlem F. Gadiano (Reg. No. 37,136).

Please address all correspondence and telephone calls to:

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY LLP
600 Thirteenth Street, N.W.
Washington, D.C. 20005-3096
(202) 756-8000

The undersigned hereby authorizes the U.S. attorneys named herein to accept and follow instructions from Maeda Patent Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by the undersigned.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Shunsuke ISONO

Inventor's signature Shunsuke ISONO Date September 14, 2004

Residence* Osaka, Japan Citizenship Japan

Post Office Address 1-11-1-602, Noe, Joto-ku, Osaka-shi, Osaka 536-0006, Japan

* City and State, or City and Country for foreign inventors

Docket No.: 085393-0521

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Shunsuke ISONO	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Divisional of	:	
U.S. Serial No. 12/153,028	:	Group Art Unit: Not Yet Assigned
	:	
Filed: March 18, 2011	:	Examiner: Not Yet Assigned
	:	
For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME	:	

PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

Amendments to the Specification begin on Page 2;

Amendments to the Claims begin on Page 3;

Amendments to the Drawings begin on Page 7;

Remarks begin on Page 8; and

An **Appendix** including the Substitute Specifications (Marked-up and Clean copies) and 2 sheets of New Drawings for Figures 6A-6E and 7A-7F is attached following page 8 of this paper.

IN THE SPECIFICATION:

On page 1 of the specification, please amend the first paragraph, spanning lines 5-7 as follows:

This application is a Divisional of U.S. Application No. 12/153,028, filed on May 13, 2008, which is a Divisional of U.S. Application No. 11/716,704, filed March 12, 2007, now U.S. Patent No. 7,400,045, which is a Divisional of U.S. Application No. 10/945,920, filed September 22, 2004, now U.S. Patent No. 7,215,028, and claims priority under 35 U.S.C. §119 on Patent Application No. 2003-335185 filed in Japan on September 26, 2003, the entire contents of each of which are hereby incorporated by reference.

*Please insert the following new paragraphs on page 11 of the specification, at the bottom of the **BRIEF DESCRIPTION OF THE FIGURES** section, and immediately above the title “**DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**”:*

--FIGS. **6A** to **6E** are planar views of the first metal interconnect, the hole-contact portion, the second metal interconnect, and the trench-contact portion of embodiments 1-4.--

--FIGS. **7A** to **7F** are views showing a method of forming a semiconductor device including dummy interconnects 213 (213a and 213b), and 313 (313a and 313b), which are formed adjacent the first interconnect layer 113 (113a and 113b).—

Please amend the following paragraph starting on page 5, line 5 of the specification as follows:

[[A]] As shown in Figs. 7A – 7F, a dummy interconnect layer may be formed beside the first interconnect layer. In this case, the surrounding of the region where the first interconnect layer is formed has a higher area ratio of conductor (metal) than the surrounding of the region where the second interconnect layer is formed. Therefore, when chemical mechanical polishing or similar treatment is carried out on the first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

IN THE CLAIMS:

A listing of the claims presented in this patent application appears below. This listing replaces all prior versions and listing of claims in this patent application.

1-22. (Cancelled)

23. (currently amended) A method for fabricating a semiconductor device, comprising:

the step (a) of forming a first insulating film over a semiconductor substrate;

the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film;

the step (c) of forming an oxidation-resistant conductor film covering the top of the interconnect layer;

the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film;

the step (e) of forming a third insulating film on the second insulating film;

the step (f) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located over the interconnect layer until the oxidation-resistant conductor film is exposed in one step; and

the step (g) of removing the photoresist.

24. (original) The method of claim 23,

wherein in the step (c), plasma treatment, wet treatment, or ion implantation is performed to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film.

25. (original) The method of claim 23,

wherein in the step (c), a film containing nitrogen is deposited, as the oxidation-resistant conductor film, on the interconnect layer.

26. (original) The method of claim 23,

wherein in the step (b), a first interconnect layer and a second interconnect layer are formed as the interconnect layer,

in the step (c), an oxidation-resistant conductor film is formed on the first interconnect layer and the second interconnect layer, and

in the step (f), portions of the third insulating film and the second insulating film located over the first interconnect layer are removed to form a trench, and portions of the third insulating film and the second insulating film located over the second interconnect layer are removed to form a hole.

27. (original) The method of claim 23, further comprising, prior to the step (a), the step (h) of forming an element in the semiconductor substrate,

wherein in the step (b), the interconnect layer is formed to be electrically connectable to the element.

28. (new) A method for fabricating a semiconductor device, comprising:

- the step (a) of forming a first insulating film over a semiconductor substrate;
- the step (b) of forming a first interconnect layer and a second interconnect layer in at least an upper portion of the first insulating film;
- the step (c) of forming an oxidation-resistant conductor film covering tops of the first interconnect layer and the second interconnect layer;
- the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film;
- the step (e) of forming a third insulating film on the second insulating film;
- the step (f) of forming a trench pattern by removing portions of the third insulating film and the second insulating film located over the first interconnect layer, and forming a part of a hole pattern by removing portions of the third insulating film and the second insulating film located over the second interconnect layer; and
- the step (g) of removing portions of the second insulating film located over the second interconnect layer until the hole pattern reaches the oxidation-resistant conductor film.

29. (new) The method of claim 28, wherein

- in the step (f), when the trench pattern is formed, portions of the third insulating film and the second insulating film located over the first interconnect layer are removed until the oxidation-resistant conductor film is exposed in one step.

IN THE DRAWINGS:

The attached drawing sheets labeled “New Sheet” contain new Figures 6A to 6E and Figures 7A to 7F.

New Figures 6A to 6E are planar views of the first metal interconnect 102, the hole-contact portion 106', the second metal interconnect 103, and the trench-contact portion 107' from Figure 1F. These new figures are not new matter, and are supported, at a minimum, by the specification at page 18, lines 18-24.

New Figures 7A to 7F are views showing a method of forming a semiconductor device including dummy interconnects, which are formed adjacent the first interconnect layer.

Attachment: 2 New Sheets of Drawings

REMARKS

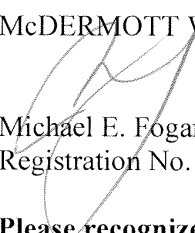
The drawings and specification have been amended to incorporate the continuity data and any amendments made during the prosecution of the parent application no. 12/153,028. The Substitute Specifications (marked-up and clean copies) attached include no new matter.

Additionally, the amendment cancels claims 1-22, without prejudice. Claims 23-27 and new claims 28-29 are pending.

No new matter has been introduced. Entry of this amendment is respectfully requested.

Respectfully submitted,

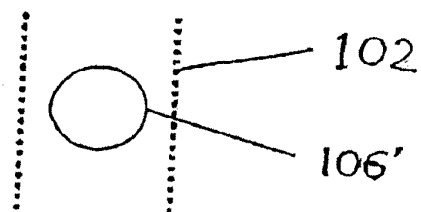
McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

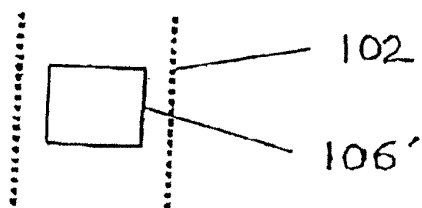
**Please recognize our Customer No. 53080
as our correspondence address.**

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ln
Facsimile: 202.756.8087
Date: March 18, 2011

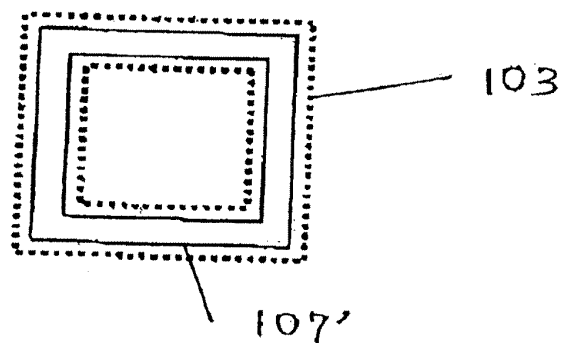
Fig,6A



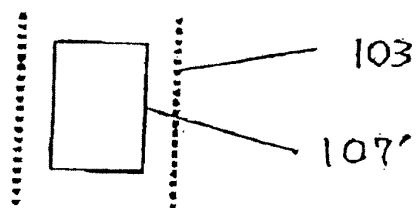
Fig,6B



Fig,6C



Fig,6D



Fig,6E

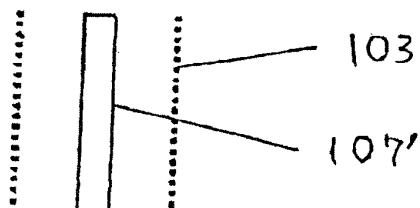


FIG. 7A

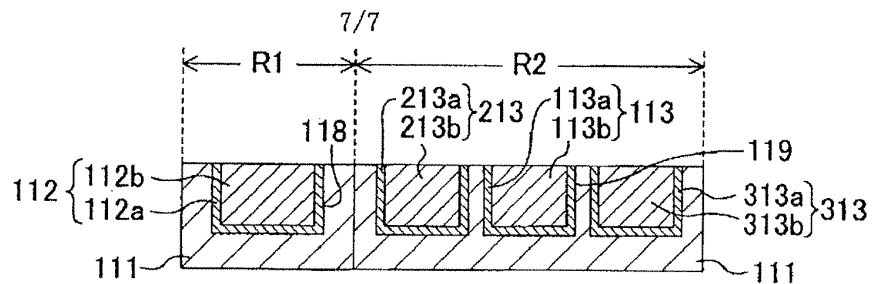


FIG. 7B

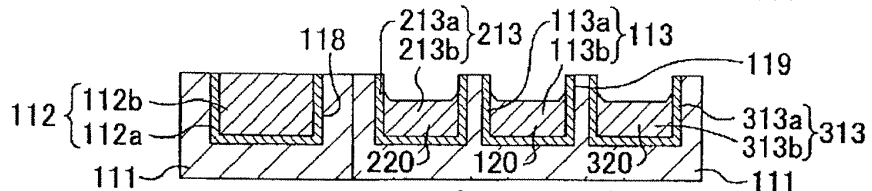


FIG. 7C

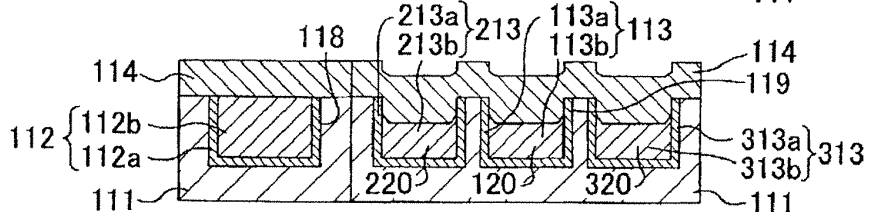


FIG. 7D

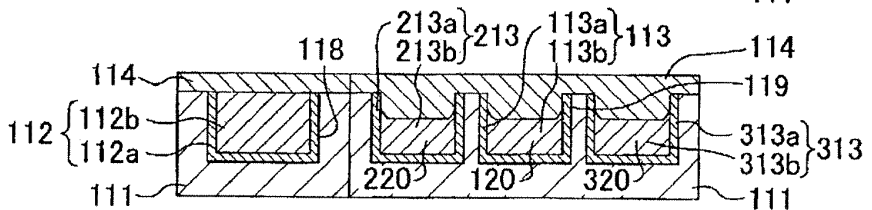


FIG. 7E

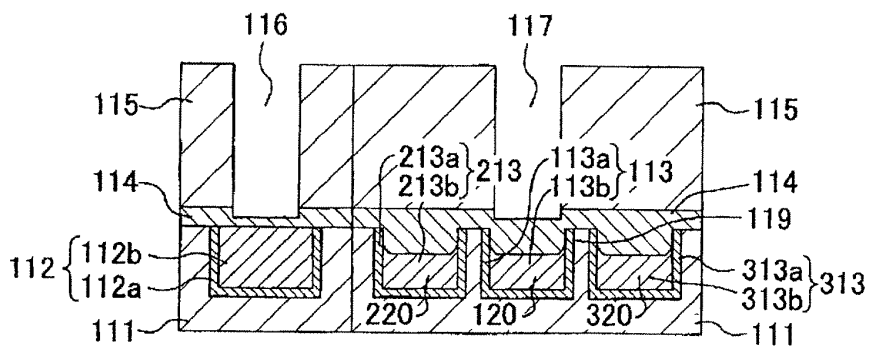
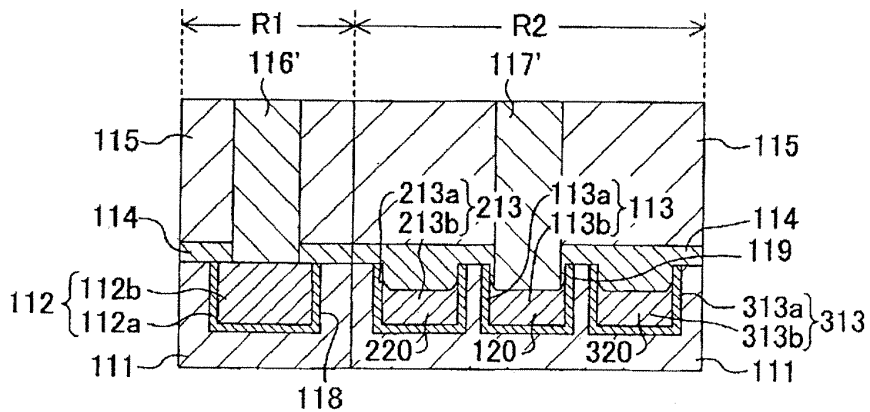


FIG. 7F



SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

5 This application is a Divisional of U.S. Application No. 12/153,028, filed on May
13, 2008, which is a Divisional of U.S. Application No. 11/716,704, filed March 12, 2007,
now U.S. Patent No. 7,400,045, which is a Divisional of U.S. Application No. 10/945,920,
filed September 22, 2004, now U.S. Patent No. 7,215,028, and claims priority under 35
U.S.C. §119 on Patent Application No. 2003-335185 filed in Japan on September 26,
10 2003, the entire contents of each of which are hereby incorporated by reference. .

BACKGROUND OF THE INVENTION

(a) Fields of the Invention

 The present invention relates to semiconductor devices and methods for fabricating
15 the same. In particular, the present invention relates to semiconductor devices having
contact portions of conductor (referred hereinafter to as conductor contact portions) on an
interconnect layer and methods for fabricating such a device.

(b) Description of Related Art

20 In recent years, miniaturization and high degree of integration of semiconductor
integrated circuits have been rapidly proceeding. In accordance with the proceeding
miniaturization of the circuit, delay time caused by transistor operation can be cut in the
device while interconnect resistance and parasitic capacitance increase therein. This makes
it difficult to cut delay time caused in an interconnect. In a measure to cut the interconnect
25 delay time, in order to reduce the interconnect resistance, copper having a lower resistivity
than aluminum used as a conventional interconnect material is employed as a substitute for
aluminum. Moreover, in order to reduce the parasitic capacitance, an insulating film

having a low dielectric constant is employed as a material for an interlayer insulating film and the like.

Copper is difficult to etch. Therefore, formation of an interconnect with copper is made by a damascene process: a hole pattern and a trench configuration are formed in an
5 insulating film, after which the patterns are filled with copper.

In a chip of a semiconductor device, a trench configuration called a seal ring is formed to protect transistors and interconnects provided in the chip against outside moisture. The seal ring is formed to surround an area containing the transistors and the interconnects. The seal ring is formed simultaneously with the etching for forming a hole
10 pattern (vias).

The hole pattern and the trench configuration serving as the seal ring are formed in the following manner.

First, to form the hole pattern and the trench configuration, an interlayer insulating film is halfway removed using photoresist as a mask. The reason why the removal is
15 stopped halfway is that if an interconnect layer located below the hole pattern and the trench configuration is exposed therefrom during the removal, the interconnect layer corrodes during subsequent ashing for removing the photoresist and subsequent polymer removal. To avoid such a problem, ashing and polymer removal are performed with only part of the thickness of the interlayer insulating film remaining. Thereafter, using the
20 resulting interlayer insulating film itself as a mask, the hole pattern and the trench configuration are made to reach the interconnect layer.

However, the conventional semiconductor device has caused the following problems.

Generally, during etching, the etching rate rises as the area of an opening increases.
25 In this device, the opening area of the trench is greater than that of the hole. Thus, when the trench and the hole are formed at the same time by a single etching, the trench is formed deeper. Therefore, it might be unable to stop etching of the trench halfway through

the interlayer insulating film, resulting in exposure of metal of the interconnect layer located therebelow. If the metal is exposed in this process, then the disadvantage arises that the metal corrodes by subjecting itself to subsequent photoresist removal by ashing and to subsequent polymer removal.

5 Such a disadvantage also arises when the interlayer insulating film is formed with multiple types of hole patterns. Specifically, the hole patterns have different pattern densities or the like, so that it is impossible, in forming the different hole patterns, to partly remove the insulating film to form the hole patterns with a uniform depth. This causes the disadvantage that the interconnect layer located below the hole patterns is exposed.

10

SUMMARY OF THE INVENTION

 An object of the present invention is to provide a method for fabricating a semiconductor device resistant to metal corrosion in an interconnect layer by taking measures to prevent exposure of the interconnect layer during formation of a hole pattern
15 and a trench pattern.

 A first semiconductor device of the present invention comprises: a semiconductor substrate; a first insulating film provided over the semiconductor substrate; an interconnect layer provided in at least an upper portion of the first insulating film; a second insulating film provided on the first insulating film and the interconnect layer; a third insulating film
20 provided on the second insulating film; and at least one conductor contact portion passing through the third insulating film and the second insulating film to reach the interconnect layer. In this device, an upper portion of the interconnect layer is provided with a recess and a portion of the second insulating film located on the interconnect layer has a greater thickness than a portion thereof located on the first insulating film.

25 With this device, the portion of the second insulating film located on the interconnect layer is formed thick. Therefore, in the step of partly removing the third insulating film and the second insulating film to form the conductor contact portion, part of

the second insulating film can be easily left on the interconnect layer, which makes it difficult to expose the interconnect layer. The semiconductor surface in this condition can be subjected to a process that may corrode metal, such as ashing or polymer removal. Subsequently, the unremoved parts of the third insulating film and the second insulating
5 film can be removed to expose the interconnect layer, and a conductor for the conductor contact portion can fill the removed portion. That is to say, a process that may corrode metal can be carried out on the semiconductor surface with the interconnect layer not exposed, whereby corrosion of the interconnect layer can be prevented.

On the other hands, all portions of the second insulating film but the portion located
10 on the interconnect layer are not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

The interconnect layer may comprise a first interconnect layer. The conductor contact portion may comprise a first conductor contact portion. The device may further comprise: a second interconnect layer provided in at least an upper portion of the first
15 insulating film; and a second conductor contact portion passing through the third insulating film and the second insulating film to reach the second interconnect layer. A portion of the second insulating film located on the first interconnect layer may have a greater thickness than a portion thereof located on the second interconnect layer. In this case, even if the third insulating film and the second insulating film are partly removed in order to form the
20 conductor contact portion, it can become difficult to expose the first interconnect layer because the region of the second insulating film formed with the first conductor contact portion is formed thick. As is the case where the area in which the first conductor contact portion is formed is greater than the area in which the second conductor contact portion is formed, when the third insulating film and the second insulating film are partly removed to
25 form the conductor contact portion, the region where the first conductor contact portion is formed is removed deeper. Even in such a circumstance, it can become difficult to expose the first interconnect layer.

The first interconnect layer may have a greater width than the second interconnect layer. In this case, the region where the first interconnect layer is formed has a higher area ratio of conductor (metal) than the region where the second interconnect layer is formed. Therefore, when chemical mechanical polishing or similar treatment is carried out on the
5 first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

[[A]] As shown in Figs. 7A – 7F, a dummy interconnect layer may be formed beside the first interconnect layer. In this case, the surrounding of the region where the first
10 interconnect layer is formed has a higher area ratio of conductor (metal) than the surrounding of the region where the second interconnect layer is formed. Therefore, when chemical mechanical polishing or similar treatment is carried out on the first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of
15 dishing.

The first conductor contact portion may be of rectangular or strip-like plane, and the second conductor contact portion may be of circular or square plane.

The first interconnect layer and the first conductor contact portion may constitute a seal ring provided in ring shape. In this case, even though the first conductor contact
20 portion serving as the seal ring differs greatly in area from the second conductor contact portion, the structure described above can prevent the first interconnect layer from being exposed.

An element may be provided in the semiconductor substrate, and the interconnect layer may be electrically connected to the element. In this case, when the third insulating
25 film and the second insulating film are partly removed in forming the conductor contact portion, an error would arise in the depth to be removed. Even though such an error arises, it can become difficult to expose the interconnect layer.

The second insulating film is preferably an insulating film of silicon compound containing carbon.

A second semiconductor device of the present invention comprises: a semiconductor substrate; a first insulating film provided on the semiconductor substrate; an
5 interconnect layer provided in at least an upper portion of the first insulating film; an oxidation-resistant conductor film covering the top of the interconnect layer; a second insulating film provided on the first insulating film and the oxidation-resistant conductor film; a third insulating film provided on the second insulating film; and at least one conductor contact portion passing through the third insulating film and the second
10 insulating film to reach the oxidation-resistant conductor film.

With this device, even if, in the step of partly removing the third insulating film and the second insulating film to form the conductor contact portion, treatment that may corrode metal, such as ashing and polymer removal, is carried out on the semiconductor surface with the oxidation-resistant conductor film exposed, corrosion of the interconnect
15 layer can be prevented. On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

The oxidation-resistant conductor film may be a nitrogen introduced layer produced by introducing nitrogen into an upper region of the interconnect layer.

20 The oxidation-resistant conductor film may be made of titanium nitride.

The interconnect layer comprises a first interconnect layer. The oxidation-resistant conductor film comprises a first oxidation-resistant conductor film provided on the first interconnect layer. The conductor contact portion comprises a first conductor contact portion. The device comprises: a second interconnect layer provided in at least an upper
25 portion of the first insulating film; a second oxidation-resistant conductor film covering the top of the second interconnect layer; and a second conductor contact portion passing through the third insulating film and the second insulating film to reach the second

oxidation-resistant conductor film. The first conductor contact portion has a greater upper surface area than the second conductor contact portion. In this case, if the third insulating film and the second insulating film are partly removed in forming these conductor contact portions, the region where the first conductor contact portion is formed is removed deeper.

5 However, since the top of the first interconnect layer is covered with the oxidation resistant film, corrosion of the first interconnect layer can be prevented even though the oxidation resistant film is exposed.

 The first conductor contact portion may be of rectangular or strip-like plane, and the second conductor contact portion may be of circular or square plane.

10 The first interconnect layer and the first conductor contact portion may constitute a seal ring provided in ring shape. In this case, even though the first conductor contact portion serving as the seal ring differs greatly in area from the second conductor contact portion, the structure described above can prevent the first interconnect layer from being exposed.

15 An element may be provided in the semiconductor substrate, and the interconnect layer may be electrically connected to the element. In this case, when the third insulating film and the second insulating film are partly removed in forming the conductor contact portion, an error would arise in the depth to be removed. Even though such an error arises, it can become difficult to expose the interconnect layer.

20 The second insulating film is preferably an insulating film of silicon compound containing carbon.

 A first method for fabricating a semiconductor device according to the present invention comprises: the step (a) of forming a first insulating film on a semiconductor substrate; the step (b) of forming an interconnect layer in at least an upper portion of the

25 first insulating film; the step (c) of forming a recess in an upper portion of the interconnect layer; the step (d) of forming, on the first insulating film and the interconnect layer, a second insulating film filling the recess; the step (e) of planarizing an upper surface of the

second insulating film; the step (f) of forming a third insulating film on the second insulating film after the step (e); the step (g) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located above the interconnect layer so that the removed part does not reach the interconnect layer, thereby
5 leaving part of the second insulating film on the interconnect layer; and the step (h) of removing the photoresist.

With this method, the portion of the second insulating film located on the interconnect layer can be formed thick. Therefore, in the step (g), the state in which the interconnect layer is not exposed can be kept more certainly. This prevents corrosion of
10 the interconnect layer even though treatment that may corrode metal, such as ashing, is carried out after the step (g). On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed thick. Therefore, in the semiconductor device fabricated by the first method, the dielectric constant between the layers can be kept constant.

15 In the step (c), the upper portion of the interconnect layer may be recessed by chemical mechanical polishing, dry etching, or wet etching to form the recess. In this case, in addition to the above effect, the effect of improving the adhesion between the first insulating film and the second insulating film can be provided.

In the step (b), a first interconnect layer for a seal ring and a second interconnect
20 layer located in a region surrounded with the first interconnect layer may be formed as the interconnect layer. In the step (c), the recess may be formed in at least an upper portion of the first interconnect layer. In the step (g), portions of the third insulating film and the second insulating film located above the first interconnect layer may be partly removed to form a trench for the seal ring, and portions of the third insulating film and the second
25 insulating film located above the second interconnect layer may be partly removed to form a hole. Since, in this case, the opening area of the trench is greater than that of the hole, the trench is formed to have a greater depth than the hole in the step (g). However, the

region of the second insulating film to be formed with the trench is formed thick, whereby it can become difficult to expose the first interconnect layer.

In the step (b), the first interconnect layer may be formed to have a greater width than the second interconnect layer. In this case, the region where the first interconnect
5 layer is formed has a higher area ratio of conductor (metal) than the region where the second interconnect layer is formed. Therefore, when, in the step (c), chemical mechanical polishing or similar treatment is carried out on the first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

10 In the step (b), a dummy interconnect layer may be formed beside the first interconnect layer. In this case, the surrounding of the region where the first interconnect layer is formed has a higher area ratio of conductor (metal) than the surrounding of the region where the second interconnect layer is formed. Therefore, when, in the step (c), chemical mechanical polishing or similar treatment is carried out on the first interconnect
15 layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

The first method may further comprise, prior to the step (a), the step (i) of forming an element in the semiconductor substrate. In the step (b), the interconnect layer may be
20 formed to be electrically connectable to the element. In this case, even though an error in the depth to be removed arises in the step (g), it can become difficult to expose the interconnect layer.

A second method for fabricating a semiconductor device according to the present invention comprises: the step (a) of forming a first insulating film on a semiconductor
25 substrate; the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film; the step (c) of forming an oxidation-resistant conductor film covering the top of the interconnect layer; the step (d) of forming a second insulating film on the

first insulating film and the oxidation-resistant conductor film; the step (e) of forming a third insulating film on the second insulating film; the step (f) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located above the interconnect layer; and the step (g) of removing the photoresist.

5 With this method, the oxidation-resistant conductor film can cover the top of the interconnect layer. Therefore, in the step (f), even if treatment that may corrode metal, such as ashing, is carried out after exposure of the oxidation-resistant conductor film, corrosion of the interconnect layer can be prevented. On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed
10 thick. Therefore, in the semiconductor device fabricated by the second method, the dielectric constant between the layers can be kept constant.

 In the step (c), plasma treatment, wet treatment, or ion implantation may be performed to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film.

15 In the step (c), a film containing nitrogen may be deposited, as the oxidation-resistant conductor film, on the interconnect layer.

 In the step (b), a first interconnect layer for a seal ring and a second interconnect layer located in a region surrounded with the first interconnect layer may be formed as the interconnect layer. In the step (c), an oxidation-resistant conductor film may be formed on
20 the first interconnect layer and the second interconnect layer. In the step (f), portions of the third insulating film and the second insulating film located above the first interconnect layer may be partly removed to form a trench for the seal ring, and portions of the third insulating film and the second insulating film located above the second interconnect layer may be partly removed to form a hole. Since, in this case, the opening area of the trench is
25 greater than that of the hole, the trench is formed to have a greater depth than the hole in the step (f). However, the region of the second insulating film to be formed with the trench is formed thick, whereby it can become difficult to expose the first interconnect layer.

The second method may further comprise, prior to the step (a), the step (h) of forming an element in the semiconductor substrate, and in the step (b), the interconnect layer may be formed to be electrically connectable to the element. In this case, even though an error in the depth to be removed arises in the step (f), it can become difficult to
5 expose the interconnect layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A to 1F are sectional views showing a semiconductor device fabrication method according to a first embodiment.

10 FIGS. 2A to 2F are sectional views showing a semiconductor device fabrication method according to a second embodiment.

FIGS. 3A to 3E are sectional views showing a semiconductor device fabrication method according to a third embodiment.

15 FIGS. 4A to 4E are sectional views showing a semiconductor device fabrication method according to a fourth embodiment.

FIGS. 5A to 5F are sectional views showing a fabrication method of an interconnect region of a semiconductor device according to a fifth embodiment.

FIGS. 6A to 6E are planar views of the first metal interconnect, the hole-contact portion, the second metal interconnect, and the trench-contact portion of embodiments 1-4.

20 FIGS. 7A to 7F are views showing a method of forming a semiconductor device including dummy interconnects 213 (213a and 213b), and 313 (313a and 313b), which are formed adjacent the first interconnect layer 113 (113a and 113b).

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

25 (First Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a first

embodiment of the present invention will be described with reference to FIGS. **1A** to **1F**. FIGS. **1A** to **1F** are sectional views showing the semiconductor device fabrication method of the first embodiment. Note that FIGS. **1A** to **1F** show an interconnect formation region **R1** and a seal ring region **R2** for protecting the interconnect formation region **R1** against
5 outside moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region **R1**.

First, in the step shown in FIG. **1A**, a first insulating film **101** of a silicon oxide film having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **101**, a photoresist (not shown) having openings in interconnect trace
10 formation positions is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby removing part of the first insulating film **101** to form interconnect grooves **108** and **109** with a depth of 250 nm. Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum
15 film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first metal interconnect **102** consisting of a conductor surface film **102a** and a metal interconnect film **102b**. The conductor surface film **102a** covers the inside surface of the interconnect groove **108**, and the metal interconnect film **102b** fills the interconnect groove **108** with the conductor surface film **102a** interposed
20 between the first insulating film **101** and the metal interconnect film **102b**. During this formation, in the seal ring region **R2**, a second metal interconnect **103** is formed which consists of a conductor surface film **103a** and a metal interconnect film **103b**.

In the step shown in FIG. **1B**, by chemical mechanical polishing or selective metal etching with nitric acid or the like, the upper portions of the first metal interconnect **102**
25 and the second metal interconnect **103** are recessed to form recessed shapes (recesses **110**) having depths of about 20 to 40 nm.

Next, in the step shown in FIG. **1C**, on the substrate, a second insulating film **104** is

deposited which is made of a silicon carbon nitride film with a thickness of 100 to 150 nm and which fills the recess **110**. In this deposition, as the material for the second insulating film **104**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be
5 formed as the second insulating film **104**.

At the time of this deposition, depressions affected by the recess shapes of the first metal interconnect **102** and the second metal interconnect **103** are created in the upper surface of the second insulating film **104**.

Then, in the step shown in FIG. **1D**, chemical mechanical polishing, wet etching
10 with sulfuric acid, nitric acid, or the like or etch back is performed to planarize the upper surface of the second insulating film **104**. By this planarization, portions of the second insulating film **104** located on the first metal interconnect **102** and the second metal interconnect **103** have thicknesses of about 70 to 90 nm and the remaining portions thereof have a thickness of 50 nm.

15 In the step shown in FIG. **1E**, a third insulating film **105** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **105**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **105**.

20 Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region and a trench formation region is formed on the third insulating film **105**. Then, dry etching is performed using the photoresist as a mask to form a hole (through hole) **106** in the interconnect formation region **R1** and a trench **107** in the seal ring region **R2**. This dry etching is performed so that the hole **106** and the trench
25 **107** extend halfway through the second insulating film **104**. Since, in this etching, the opening area of the trench **107** is greater than that of the hole **106**, the trench **107** is etched deeper. Thereafter, the photoresist is removed by ashing, and polymers created during wet

etching and dry etching are removed.

In the step shown in FIG. 1F, the remaining portions of the second insulating film **104** within the hole and trench are etched, whereby the hole **106** and the trench **107** reach the first metal interconnect **102** and the second metal interconnect **103**, respectively. The
5 resulting hole and trench are filled with a conductor to form a hole-contact portion **106'** made of conductor (referred hereinafter to as a conductor hole-contact portion) in circular or square plane and a trench-contact portion **107'** of conductor (referred hereinafter to as a conductor trench-contact portion) in ring shape. This step is performed after completion of processes that may corrode metal, such as ashing and polymer removal.

10 With reference to FIG. 1F again, next description will now be made of the structure of the interconnect and the seal ring of the semiconductor device according to the first embodiment.

As shown in FIG. 1F, the semiconductor device of the first embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of
15 the interconnect formation region **R1**. The interconnect formation region **R1** is provided with the first metal interconnect **102**, and the seal ring region **R2** is provided with the second metal interconnect **103**. The first metal interconnect **102** includes the conductor surface film **102a** covering the surface of the interconnect groove **108** and the metal interconnect film **102b** covering the conductor surface film **102a**. Likewise, the second
20 metal interconnect **103** includes the conductor surface film **103a** covering the surface of the interconnect groove **109** and the metal interconnect film **103b** provided on the conductor surface film **103a**. The upper portions of the first metal interconnect **102** and the second metal interconnect **103** are recessed to form the recesses **110**.

The second insulating film **104** is provided on the first insulating film **101**, the first
25 metal interconnect **102** and the second metal interconnect **103**. The second insulating film **104** fills the recess **110**, so that in the second insulating film **104**, the portions thereof located on the first metal interconnect **102** and the second metal interconnect **103** are

formed thicker than the other portions thereof. The upper surface of the second insulating film **104** is planarized.

The third insulating film **105** is provided on the second insulating film **104**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **106'** passing through the third insulating film **105** and the second insulating film **104**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **107'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **103** and the conductor trench-contact portion **107'** is provided to surround the first metal interconnect **102** and the conductor hole-contact portion **106'** in the interconnect formation region **R1**.

The effects obtained by the first embodiment will be described below in comparison with the conventional device.

In the conventional device, the upper surfaces of the first metal interconnect and the second metal interconnect remain flat, and the second insulating film with a uniform thickness is formed on the first metal interconnect and the second metal interconnect. By such a structure, when the hole and the trench are formed, the trench might pass through the second insulating film to expose the second metal interconnect.

In contrast to this, in the first embodiment, only the portions of the second insulating film **104** located on the first metal interconnect **102** and the second metal interconnect **103** can be formed thick. This prevents the trench **107** from reaching the second metal interconnect **103**. Therefore, even if ashing and polymer removal are performed on the semiconductor surface, the first metal interconnect **102** will not corrode. On the other hands, the portion of the second insulating film **104** located on the first insulating film **101** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, chemical mechanical polishing or selective etching is performed to recess the upper surfaces of the first metal interconnect **102** and the second metal

interconnect **103**. This improves the adhesion between the first insulating film **101** and the second insulating film **104**.

In the first embodiment, by chemical mechanical polishing or the like, the recessed shapes are formed in the upper portions of the first metal interconnect **102** and the second metal interconnect **103**. However, in the present invention, the recessed shape may be formed by utilizing the property of copper in which copper is compressed by heat added thereto. To be more specific, in the step shown in FIG. **1A**, the first metal interconnect **102** and the second metal interconnect **103** are formed and then heat treatment is performed at 200 to 500°C. This compresses the metal interconnect films **102b** and **103b** made of copper to form recesses in the upper portions of the first metal interconnect **102** and the second metal interconnect **103**. Also by this procedure, the same effects as those described above can be obtained.

(Second Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a second embodiment of the present invention will be described with reference to FIGS. **2A** to **2F**. FIGS. **2A** to **2F** are sectional views showing the semiconductor device fabrication method of the second embodiment. Note that FIGS. **2A** to **2F** show an interconnect formation region **R1** and a seal ring region **R2** for protecting the interconnect formation region **R1** against outside moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region **R1**.

First, in the step shown in FIG. **2A**, a first insulating film **111** of a silicon oxide film having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **111**, a photoresist (not shown) having openings in a metal interconnect trace formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby forming an interconnect groove **118** in the interconnect formation region **R1** and an interconnect groove **119** in the seal ring formation region **R2**.

In this etching, the width of the interconnect groove **119** is made greater than that of the interconnect groove **118**. To be more specific, when the interconnect groove **118** has a width smaller than 2 μm , the interconnect groove **119** has a width of 2 μm or greater.

Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first metal interconnect **112** having a width of 2 μm or greater and consisting of a conductor surface film **112a** and a metal interconnect film **112b**. The conductor surface film **112a** covers the inside surface of the interconnect groove **118**, and the metal interconnect film **112b** fills the interconnect groove **118** with the conductor surface film **112a** interposed between the first insulating film **111** and the metal interconnect film **112b**. During this formation, in the seal ring region **R2**, a second metal interconnect **113** with a width of 2 μm or greater is formed which consists of a conductor surface film **113a** and a metal interconnect film **113b**.

In the step shown in FIG. **2B**, chemical mechanical polishing is performed. In this step, the upper portion of the second metal interconnect **113** is recessed by utilizing the metal area ratio dependence of dishing. Details of this step are as follows. If a substrate with metal embedded therein is subjected to chemical mechanical polishing, the depth to which the metal is removed tends to be greater as the percentage of metal contained in the region to be removed rises. In the second embodiment, the second metal interconnect **113** is formed to have a greater width than the first metal interconnect **112**. In other words, the region where the second metal interconnect **113** is formed has a higher ratio of metal per unit area. This allows the upper portion of the second metal interconnect **113** to be recessed deeper than the other regions.

As a substitute for the method in which the depth of the second metal interconnect **113** is made greater than that of the first metal interconnect **112**, the percentage of metal

content per unit area may be raised by forming a dummy pattern around the second metal interconnect **113**.

Next, in the step shown in FIG. **2C**, a second insulating film **114** made of a silicon carbon nitride film is deposited on the first insulating film **111**, the first metal interconnect **112** and the second metal interconnect **113**. In this deposition, as the material for the second insulating film **114**, use may be made of a silicon nitride film, a silicon oxide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **114**.

At the time of this deposition, a depression affected by the recess shape of the second metal interconnect **113** is created in the upper portion of the second insulating film **114**.

Then, in the step shown in FIG. **2D**, chemical mechanical polishing, wet etching, or etch back is performed to planarize the second insulating film **114**.

In the step shown in FIG. **2E**, a third insulating film **115** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **115**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **115**.

Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region and a trench formation region is formed on the third insulating film **115**. Then, dry etching is performed using the photoresist as a mask to form a hole **116** in the interconnect formation region **R1** and a trench **117** in the seal ring region **R2**. This dry etching is performed so that the trench **117** extends halfway through the second insulating film **114**. Since, in this etching, the opening area of the trench **117** is greater than that of the hole **116**, the trench **117** is etched deeper. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG. 2F, the remaining portions of the second insulating film 114 within the hole and trench are removed, whereby the hole 116 and the trench 117 reach the first metal interconnect 112 and the second metal interconnect 113, respectively. The resulting hole and trench are filled with a conductor to form a conductor hole-contact portion 116' in circular or square plane and a conductor trench-contact portion 117' in ring shape. This step is performed after completion of processes that may corrode metal, such as ashing and polymer removal.

With reference to FIG. 2F again, next description will now be made of the structure of the interconnect and the seal ring of the semiconductor device according to the second embodiment.

As shown in FIG. 2F, the semiconductor device of the second embodiment includes the interconnect formation region R1 and the seal ring region R2 surrounding the sides of the interconnect formation region R1. The interconnect formation region R1 is provided with the first metal interconnect 112, and the seal ring region R2 is provided with the second metal interconnect 113. The second metal interconnect 113 is formed to have a greater width than the first metal interconnect 112.

The first metal interconnect 112 includes the conductor surface film 112a covering the surface of the interconnect groove 118 and the metal interconnect film 112b covering the conductor surface film 112a. Likewise, the second metal interconnect 113 includes the conductor surface film 113a covering the surface of the interconnect groove 119 and the metal interconnect film 113b provided on the conductor surface film 113a. The upper portion of the second metal interconnect 113 is recessed to form a recess 120.

The second insulating film 114 is provided on the first insulating film 111, the first metal interconnect 112 and the second metal interconnect 113. The second insulating film 114 fills the recess 120, so that in the second insulating film 114, the portion thereof located on the second metal interconnect 113 is formed thicker than the other portions thereof. The upper surface of the second insulating film 114 is planarized.

The third insulating film **115** is provided on the second insulating film **114**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **116'** passing through the third insulating film **115** and the second insulating film **114**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **117'**. Thus, in
5 the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **113** and the conductor trench-contact portion **117'** is provided to surround the first metal interconnect **112** and the conductor hole-contact portion **116'** in the interconnect formation region **R1**.

The effects obtained by the second embodiment will be described below in
10 comparison with the conventional device.

In the conventional device, the upper surface of the second metal interconnect remains flat, and the second insulating film with a uniform thickness is formed on the second metal interconnect. By such a structure, when the hole and the trench are formed, the trench might pass through the second insulating film to expose the second metal
15 interconnect.

In contrast to this, in the second embodiment, only the portion of the second insulating film **114** located on the second metal interconnect **113** can be formed thick without increasing the number of fabrication steps of the device. This prevents the trench **117** from reaching the second metal interconnect **113**. Therefore, even if ashing and
20 polymer removal are performed on the semiconductor surface, the first metal interconnect will not corrode. On the other hands, the portion of the second insulating film **114** located on the first insulating film **111** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, chemical mechanical polishing or etching is performed to recess the
25 upper portion of the second metal interconnect **113**. This improves the adhesion between the first insulating film **111** and the second insulating film **114**.

In the second embodiment, the recessed shape is formed by utilizing the metal area

ratio dependence of dishing. However, it may be formed by etching utilizing the pattern density dependence. Alternatively, in the step shown in FIG. **2B** in the present invention, the recessed shape may be formed in the upper portion of the second metal interconnect **113** by performing etching with a photoresist or the like covering all the region but the
5 second metal interconnect **113**. In this case, the same effects as those described above can be obtained except that the number of fabrication steps of the device increases.

In the second embodiment, in performing chemical mechanical polishing in the step shown in FIG. **2B**, slurry with high solubility, such as hydrogen peroxide, may be used. This raises the polishing rate of metal, which allows the second metal interconnect **113** to
10 be recessed deeper.

(Third Embodiment)

A method for fabricating a semiconductor device according to a third embodiment of the present invention will be described with reference to FIGS. **3A** to **3E**. FIGS. **3A** to
15 **3E** are sectional views showing the semiconductor device fabrication steps of the third embodiment. Note that FIGS. **3A** to **3E** show an interconnect formation region **R1** and a seal ring region **R2** for protecting the interconnect formation region **R1** against outside moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region **R1**.

20 First, in the step shown in FIG. **3A**, a first insulating film **121** of a silicon oxide film having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **121**, a photoresist (not shown) having openings in a metal interconnect trace formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby removing part of the first insulating film **121** to form
25 interconnect grooves **128** and **129** with a depth of 250 nm. Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper

film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first metal interconnect **122** consisting of a conductor surface film **122a** and a metal interconnect film **122b**. The conductor surface film **122a** covers the inside surface of the interconnect groove **128**, and the metal interconnect film

5 **122b** fills the interconnect groove **128** with the conductor surface film **122a** interposed between the first insulating film **121** and the metal interconnect film **122b**. During this formation, in the seal ring region **R2**, a second metal interconnect **123** is formed which consists of a conductor surface film **123a** and a metal interconnect film **123b**.

In the step shown in FIG. **3B**, plasma treatment using a gas containing nitrogen, wet

10 treatment using ammonia, benzotriazole (BTA), or quinaldic acid, or ion implantation is performed to supply nitrogen to the upper portions of the first metal interconnect **122** and the second metal interconnect **123**. This alters the upper portions of the first metal interconnect **122** and the second metal interconnect **123** into an oxidation resistant film **130**. Simultaneously, this step can improve the adhesion between the first insulating film **121**

15 and a second insulating film **124** that will be formed in a subsequent step.

Next, in the step shown in FIG. **3C**, the second insulating film **124** made of a silicon carbon nitride film is deposited on the first insulating film **121** and the oxidation resistant film **130**. In this deposition, as the material for the second insulating film **124**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film,

20 or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **124**.

In the step shown in FIG. **3D**, a third insulating film **125** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **125**, use may be made of an FSG (fluorinated silicate glass) film, a

25 BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **125**.

Subsequently to this, by photolithography, a photoresist (not shown) having

openings in a hole formation region and a trench formation region is formed on the third insulating film **125**. Then, dry etching is performed using the photoresist as a mask to form a hole **126** in the interconnect formation region **R1** and a trench **127** in the seal ring region **R2**. This dry etching may be performed either so that the trench **127** extends only
5 halfway through the second insulating film **124** or so that the trench **127** passes through the second insulating film **124** to reach the oxidation resistant film **130**. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG. **3E**, the remaining portions of the second insulating film
10 **124** within the hole and trench are removed, whereby the hole **126** and the trench **127** reach the oxidation resistant film **130**. The resulting hole and trench are filled with a conductor to form a conductor hole-contact portion **126'** in circular or square plane and a conductor trench-contact portion **127'** in ring shape.

With reference to FIG. **3E** again, next description will now be made of the structure
15 of the interconnect and the seal ring of the semiconductor device according to the third embodiment.

As shown in FIG. **3E**, the semiconductor device of the third embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of the interconnect formation region **R1**. The interconnect formation region **R1** is provided
20 with the first metal interconnect **122**, and the seal ring region **R2** is provided with the second metal interconnect **123**. The first metal interconnect **122** includes the conductor surface film **122a** covering the surface of the interconnect groove **128** and the metal interconnect film **122b** covering the conductor surface film **122a**. Likewise, the second metal interconnect **123** includes the conductor surface film **123a** covering the surface of
25 the interconnect groove **129** and the metal interconnect film **123b** provided on the conductor surface film **123a**. The upper portions of the metal interconnect films **122b** and **123b** contain nitrogen and thus are formed into the oxidation resistant film **130**.

The second insulating film **124** is provided on the first insulating film **121**, the first metal interconnect **122** and the second metal interconnect **123**. The third insulating film **125** is provided on the second insulating film **124**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **126'** passing through the third
5 insulating film **125** and the second insulating film **124**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **127'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **123** and the conductor trench-contact portion **127'** is provided to surround the first metal interconnect **122** and the conductor hole-contact portion **126'** in the interconnect formation region **R1**.

10 The effects obtained by the third embodiment will be described below in comparison with the conventional device.

In the conventional device, if a trench reaches the second metal interconnect during formation of the hole pattern and the trench pattern, then the second metal interconnect corrodes in subsequent ashing and polymer removal.

15 In contrast to this, in the third embodiment, the upper portion of the second metal interconnect **123** is altered into the oxidation resistant film **130**. Therefore, even if ashing and polymer removal are performed in the state in which the trench **127** reaches the second metal interconnect **123**, the upper portion of the second metal interconnect **123** will not corrode. On the other hands, the portion of the second insulating film **124** located on the
20 first insulating film **121** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, the upper portions of the first metal interconnect **122** and the second metal interconnect **123** are made to contain nitrogen, which also provides the advantage that the etching resistance in the formation of the hole **126** and the trench **127** is improved.

25 In the step shown in FIG. **3D**, in the case where the hole **126** and the trench **127** reach the oxidation resistant film **130**, the later step of removing portions of the second insulating film **124** remaining between the oxidation resistant film **130** and each of the hole

126 and the trench **127** can be advantageously omitted.

(Fourth Embodiment)

A method for fabricating a semiconductor device according to a fourth embodiment
5 of the present invention will be described with reference to FIGS. **4A** to **4E**. FIGS. **4A** to
4E are sectional views showing the semiconductor device fabrication steps of the fourth
embodiment. Note that FIGS. **4A** to **4E** show an interconnect formation region **R1** and a
seal ring region **R2** for protecting the interconnect formation region **R1** against outside
moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region
10 **R1**.

First, in the step shown in FIG. **4A**, a first insulating film **131** of a silicon oxide film
having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first
insulating film **131**, a photoresist (not shown) having openings in a metal interconnect
trace formation region is formed by photolithography. The formed photoresist is used as a
15 mask to perform dry etching, thereby removing part of the first insulating film **131** to form
interconnect grooves **138** and **139** with a depth of 250 nm. Thereafter, the photoresist is
removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum
and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper
film and the stacked film are polished using chemical mechanical polishing to form, in the
20 interconnect formation region **R1**, a first metal interconnect **132** consisting of a conductor
surface film **132a** and a metal interconnect film **132b**. The conductor surface film **132a**
covers the inside surface of the interconnect groove **138**, and the metal interconnect film
132b fills the interconnect groove **138** with the conductor surface film **132a** interposed
between the first insulating film **131** and the metal interconnect film **132b**. During this
25 formation, in the seal ring region **R2**, a second metal interconnect **133** is formed which
consists of a conductor surface film **133a** and a metal interconnect film **133b**.

In the step shown in FIG. **4B**, an oxidation-resistant metal film **140** is selectively

deposited on the first metal interconnect **132** and the second metal interconnect **133**. An exemplary material for the metal film **140** is titanium nitride (TiN).

Next, in the step shown in FIG. **4C**, a second insulating film **134** made of a silicon carbon nitride film is deposited on the first insulating film **131** and the metal film **140**. In this deposition, as the material for the second insulating film **134**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **134**. Subsequently to the deposition, chemical mechanical polishing, wet etching, or etch back is performed to planarize the second insulating film **134**.

In the step shown in FIG. **4D**, a third insulating film **135** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **135**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **135**.

Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region and a trench formation region is formed on the third insulating film **135**. Then, dry etching is performed using the photoresist as a mask to form a hole **136** in the interconnect formation region **R1** and a trench **137** in the seal ring region **R2**. This dry etching may be performed either so that the trench **137** extends only halfway through the second insulating film **134** or so that the trench **137** passes through the second insulating film **134** to reach the metal film **140**. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG. **4E**, the remaining portions of the second insulating film **134** within the hole and trench are removed, whereby the hole **136** and the trench **137** reach the first metal interconnect **132** and the second metal interconnect **133**, respectively. The resulting hole and trench are filled with a conductor to form a conductor hole-contact portion **136'** in circular or square plane and a conductor trench-contact portion **137'** in ring

shape.

With reference to FIG. 4E again, next description will now be made of the structure of the interconnect and the seal ring of the semiconductor device according to the fourth embodiment.

5 As shown in FIG. 4E, the semiconductor device of the fourth embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of the interconnect formation region **R1**. The interconnect formation region **R1** is provided with the first metal interconnect **132**, and the seal ring region **R2** is provided with the second metal interconnect **133**. The first metal interconnect **132** includes the conductor
10 surface film **132a** covering the surface of the interconnect groove **138** and the metal interconnect film **132b** covering the conductor surface film **132a**. Likewise, the second metal interconnect **133** includes the conductor surface film **133a** covering the surface of the interconnect groove **139** and the metal interconnect film **133b** provided on the conductor surface film **133a**.

15 The oxidation-resistant metal film **140** made of, for example, titanium nitride is provided on the first metal interconnect **132** and the second metal interconnect **133**. The second insulating film **134** is provided on the first insulating film **131** and the metal film **140**. The third insulating film **135** is provided on the second insulating film **134**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **136'**
20 passing through the third insulating film **135** and the second insulating film **134**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **137'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **133** and the conductor trench-contact portion **137'** is provided to surround the first metal interconnect **132** and the conductor hole-contact portion **136'** in the interconnect formation
25 region **R1**.

In the fourth embodiment, the metal film **140** resistant to oxidation covers the top of the second metal interconnect **133**. Therefore, even if ashing and polymer removal are

performed in the state in which the trench **137** reaches the metal film **140**, the upper portion of the second metal interconnect **133** will not corrode. On the other hands, the portion of the second insulating film **134** located on the first insulating film **131** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

5 Moreover, the upper portions of the first metal interconnect **132** and the second metal interconnect **133** are formed with the metal film **140** resistant to oxidation, which also provides the advantage that the etching resistance in the formation of the hole **136** and the trench **137** is improved.

10 (Fifth Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a fifth embodiment of the present invention will be described with reference to FIGS. **5A** to **5F**. FIGS. **5A** to **5F** are sectional views showing a method for fabricating an interconnect region of a semiconductor device according to the fifth embodiment. The foregoing first to
15 fourth embodiments have shown the case where a difference in depth arises between the hole in the interconnect region and the trench in the seal ring region. On the other hands, the fifth embodiment shows the case where in forming a number of hole patterns in the interconnect region, a difference in depth arises among the hole patterns.

First, in the step shown in FIG. **5A**, a first insulating film **141** of a silicon oxide film
20 having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **141**, a photoresist (not shown) having openings in a metal interconnect trace formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby removing part of the first insulating film **141** to form an interconnect groove **148** with a depth of 250 nm. Thereafter, the photoresist is removed,
25 and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper film and the stacked film are polished using chemical mechanical polishing to form a metal

interconnect **142** consisting of a conductor surface film **142a** and a metal interconnect film **142b**. The conductor surface film **142a** covers the inside surface of the interconnect groove **148**, and the metal interconnect film **142b** fills the interconnect groove **148** with the conductor surface film **142a** interposed between the insulating film **141** and the metal
5 interconnect film **142b**.

In the step shown in FIG. **5B**, by chemical mechanical polishing or selective metal etching with nitric acid or the like, the upper portion of the metal interconnect **142** is recessed to form a recessed shape (recess **150**) having a depth of about 20 to 40 nm.

Next, in the step shown in FIG. **5C**, on the substrate, a second insulating film **144** is
10 deposited which is made of a silicon carbon nitride film with a thickness of 100 to 150 nm and which fills the recess **150**. In this deposition, as the material for the second insulating film **144**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **144**.

15 At the time of this deposition, a depression affected by the recess shape of the metal interconnect **142** is created in the top of the second insulating film **144**.

Then, in the step shown in FIG. **5D**, chemical mechanical polishing, wet etching or etch back is performed to planarize the upper surface of the second insulating film **144**. By this planarization, a portion of the second insulating film **144** located on the metal
20 interconnect **142** has a thickness of about 70 to 90 nm and the remaining portions thereof have a thickness of 50 nm.

In the step shown in FIG. **5E**, a third insulating film **145** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **145**, use may be made of an FSG (fluorinated silicate glass) film, a
25 BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **145**.

Subsequently to this, by photolithography, a photoresist (not shown) having

openings in a hole formation region is formed on the third insulating film **145**. Then, dry etching is performed using the photoresist as a mask to form holes **146**. This dry etching is performed so that the holes **146** extend halfway through the second insulating film **144**. At the time of completion of this etching, respective holes **146** of multiple hole patterns have
5 different depths due to influences of the pattern density or the like. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG. **5F**, the remaining portions of the second insulating film **144** within the holes are removed, whereby the holes **146** reach the metal interconnect **142**.
10 The resulting holes are filled with a conductor to form conductor hole-contact portions **146'** in circular or square plane. This step is performed after completion of processes that may corrode metal, such as ashing and polymer removal.

With reference to FIG. **5F** again, next description will now be made of the structure of the interconnect and the conductor hole-contact portion of the semiconductor device
15 according to the fifth embodiment.

As shown in FIG. **5F**, in the semiconductor device of the fifth embodiment, the metal interconnect **142** which includes the conductor surface film **142a** and the metal interconnect film **142b** covering the top of the conductor surface film **142a** is provided in the first insulating film **141**. The upper portion of the metal interconnect **142** is recessed to
20 form the recess **150**.

The second insulating film **144** is provided on the first insulating film **141** and the metal interconnect **142**. The second insulating film **144** fills the recess **150**, so that in the second insulating film **144**, the portion thereof located on the metal interconnect **142** is formed thicker than the other portions thereof. The upper surface of the second insulating
25 film **144** is planarized.

The third insulating film **145** is provided on the second insulating film **144**. Further, the conductor hole-contact portion **146'** is provided which passes through the third

insulating film **145** and the second insulating film **144**.

The effects obtained by the fifth embodiment will be described below in comparison with the conventional device.

In the conventional device, the upper surface of the metal interconnect remains flat,
5 and the second insulating film and the third insulating film are formed on the metal interconnect. If multiple types of hole patterns are formed in such a structure, the formed hole patterns have different hole depths due to nonuniform pattern densities or fabrication process variations. This might cause some of the hole patterns to pass through the second insulating film to reach the metal interconnect. Such a possibility increases particularly in
10 the case where a number of hole patterns are formed in the device.

In contrast to this, in the fifth embodiment, only the portion of the second insulating film **144** located on the metal interconnect **142** can be formed thick. This prevents the holes **146** from reaching the metal interconnect **142**. Therefore, even if ashing and polymer removal are performed on the semiconductor surface, the metal interconnect
15 **142** will not corrode. On the other hands, the portion of the second insulating film **144** located on the first insulating film **141** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, chemical mechanical polishing or selective etching is performed to recess the upper surface of the metal interconnect **142**. This improves the adhesion
20 between the first insulating film **141** and the second insulating film **144**.

The fifth embodiment is composed by applying the method of the first embodiment to the case where multiple types of hole patterns are formed in an interconnect region. However, in the present invention, methods of the third and fourth embodiments can also be applied to that case.

25 In the first to fourth embodiments, description has been made of the case where the conductor trench-contact portion is formed in ring shape to use the portion as the seal ring. Alternatively, the portion may be formed in rectangular shape or strip shape to use the

portion as part of an electrode.

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

5 This application is a Divisional of U.S. Application No. 12/153,028, filed on May
13, 2008, which is a Divisional of U.S. Application No. 11/716,704, filed March 12, 2007,
now U.S. Patent No. 7,400,045, which is a Divisional of U.S. Application No. 10/945,920,
filed September 22, 2004, now U.S. Patent No. 7,215,028, and claims priority under 35
U.S.C. §119 on Patent Application No. 2003-335185 filed in Japan on September 26,
10 2003, the entire contents of each of which are hereby incorporated by reference. .

BACKGROUND OF THE INVENTION

(a) Fields of the Invention

 The present invention relates to semiconductor devices and methods for fabricating
15 the same. In particular, the present invention relates to semiconductor devices having
contact portions of conductor (referred hereinafter to as conductor contact portions) on an
interconnect layer and methods for fabricating such a device.

(b) Description of Related Art

20 In recent years, miniaturization and high degree of integration of semiconductor
integrated circuits have been rapidly proceeding. In accordance with the proceeding
miniaturization of the circuit, delay time caused by transistor operation can be cut in the
device while interconnect resistance and parasitic capacitance increase therein. This makes
it difficult to cut delay time caused in an interconnect. In a measure to cut the interconnect
25 delay time, in order to reduce the interconnect resistance, copper having a lower resistivity
than aluminum used as a conventional interconnect material is employed as a substitute for
aluminum. Moreover, in order to reduce the parasitic capacitance, an insulating film

having a low dielectric constant is employed as a material for an interlayer insulating film and the like.

Copper is difficult to etch. Therefore, formation of an interconnect with copper is made by a damascene process: a hole pattern and a trench configuration are formed in an
5 insulating film, after which the patterns are filled with copper.

In a chip of a semiconductor device, a trench configuration called a seal ring is formed to protect transistors and interconnects provided in the chip against outside moisture. The seal ring is formed to surround an area containing the transistors and the interconnects. The seal ring is formed simultaneously with the etching for forming a hole
10 pattern (vias).

The hole pattern and the trench configuration serving as the seal ring are formed in the following manner.

First, to form the hole pattern and the trench configuration, an interlayer insulating film is halfway removed using photoresist as a mask. The reason why the removal is
15 stopped halfway is that if an interconnect layer located below the hole pattern and the trench configuration is exposed therefrom during the removal, the interconnect layer corrodes during subsequent ashing for removing the photoresist and subsequent polymer removal. To avoid such a problem, ashing and polymer removal are performed with only part of the thickness of the interlayer insulating film remaining. Thereafter, using the
20 resulting interlayer insulating film itself as a mask, the hole pattern and the trench configuration are made to reach the interconnect layer.

However, the conventional semiconductor device has caused the following problems.

Generally, during etching, the etching rate rises as the area of an opening increases.
25 In this device, the opening area of the trench is greater than that of the hole. Thus, when the trench and the hole are formed at the same time by a single etching, the trench is formed deeper. Therefore, it might be unable to stop etching of the trench halfway through

the interlayer insulating film, resulting in exposure of metal of the interconnect layer located therebelow. If the metal is exposed in this process, then the disadvantage arises that the metal corrodes by subjecting itself to subsequent photoresist removal by ashing and to subsequent polymer removal.

5 Such a disadvantage also arises when the interlayer insulating film is formed with multiple types of hole patterns. Specifically, the hole patterns have different pattern densities or the like, so that it is impossible, in forming the different hole patterns, to partly remove the insulating film to form the hole patterns with a uniform depth. This causes the disadvantage that the interconnect layer located below the hole patterns is exposed.

10

SUMMARY OF THE INVENTION

 An object of the present invention is to provide a method for fabricating a semiconductor device resistant to metal corrosion in an interconnect layer by taking measures to prevent exposure of the interconnect layer during formation of a hole pattern
15 and a trench pattern.

 A first semiconductor device of the present invention comprises: a semiconductor substrate; a first insulating film provided over the semiconductor substrate; an interconnect layer provided in at least an upper portion of the first insulating film; a second insulating film provided on the first insulating film and the interconnect layer; a third insulating film
20 provided on the second insulating film; and at least one conductor contact portion passing through the third insulating film and the second insulating film to reach the interconnect layer. In this device, an upper portion of the interconnect layer is provided with a recess and a portion of the second insulating film located on the interconnect layer has a greater thickness than a portion thereof located on the first insulating film.

25 With this device, the portion of the second insulating film located on the interconnect layer is formed thick. Therefore, in the step of partly removing the third insulating film and the second insulating film to form the conductor contact portion, part of

the second insulating film can be easily left on the interconnect layer, which makes it difficult to expose the interconnect layer. The semiconductor surface in this condition can be subjected to a process that may corrode metal, such as ashing or polymer removal. Subsequently, the unremoved parts of the third insulating film and the second insulating
5 film can be removed to expose the interconnect layer, and a conductor for the conductor contact portion can fill the removed portion. That is to say, a process that may corrode metal can be carried out on the semiconductor surface with the interconnect layer not exposed, whereby corrosion of the interconnect layer can be prevented.

On the other hands, all portions of the second insulating film but the portion located
10 on the interconnect layer are not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

The interconnect layer may comprise a first interconnect layer. The conductor contact portion may comprise a first conductor contact portion. The device may further comprise: a second interconnect layer provided in at least an upper portion of the first
15 insulating film; and a second conductor contact portion passing through the third insulating film and the second insulating film to reach the second interconnect layer. A portion of the second insulating film located on the first interconnect layer may have a greater thickness than a portion thereof located on the second interconnect layer. In this case, even if the third insulating film and the second insulating film are partly removed in order to form the
20 conductor contact portion, it can become difficult to expose the first interconnect layer because the region of the second insulating film formed with the first conductor contact portion is formed thick. As is the case where the area in which the first conductor contact portion is formed is greater than the area in which the second conductor contact portion is formed, when the third insulating film and the second insulating film are partly removed to
25 form the conductor contact portion, the region where the first conductor contact portion is formed is removed deeper. Even in such a circumstance, it can become difficult to expose the first interconnect layer.

The first interconnect layer may have a greater width than the second interconnect layer. In this case, the region where the first interconnect layer is formed has a higher area ratio of conductor (metal) than the region where the second interconnect layer is formed. Therefore, when chemical mechanical polishing or similar treatment is carried out on the
5 first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

As shown in Figs. 7A – 7E, a dummy interconnect layer may be formed beside the first interconnect layer. In this case, the surrounding of the region where the first
10 interconnect layer is formed has a higher area ratio of conductor (metal) than the surrounding of the region where the second interconnect layer is formed. Therefore, when chemical mechanical polishing or similar treatment is carried out on the first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of
15 dishing.

The first conductor contact portion may be of rectangular or strip-like plane, and the second conductor contact portion may be of circular or square plane.

The first interconnect layer and the first conductor contact portion may constitute a seal ring provided in ring shape. In this case, even though the first conductor contact
20 portion serving as the seal ring differs greatly in area from the second conductor contact portion, the structure described above can prevent the first interconnect layer from being exposed.

An element may be provided in the semiconductor substrate, and the interconnect layer may be electrically connected to the element. In this case, when the third insulating
25 film and the second insulating film are partly removed in forming the conductor contact portion, an error would arise in the depth to be removed. Even though such an error arises, it can become difficult to expose the interconnect layer.

The second insulating film is preferably an insulating film of silicon compound containing carbon.

A second semiconductor device of the present invention comprises: a semiconductor substrate; a first insulating film provided on the semiconductor substrate; an
5 interconnect layer provided in at least an upper portion of the first insulating film; an oxidation-resistant conductor film covering the top of the interconnect layer; a second insulating film provided on the first insulating film and the oxidation-resistant conductor film; a third insulating film provided on the second insulating film; and at least one conductor contact portion passing through the third insulating film and the second
10 insulating film to reach the oxidation-resistant conductor film.

With this device, even if, in the step of partly removing the third insulating film and the second insulating film to form the conductor contact portion, treatment that may corrode metal, such as ashing and polymer removal, is carried out on the semiconductor surface with the oxidation-resistant conductor film exposed, corrosion of the interconnect
15 layer can be prevented. On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

The oxidation-resistant conductor film may be a nitrogen introduced layer produced by introducing nitrogen into an upper region of the interconnect layer.

20 The oxidation-resistant conductor film may be made of titanium nitride.

The interconnect layer comprises a first interconnect layer. The oxidation-resistant conductor film comprises a first oxidation-resistant conductor film provided on the first interconnect layer. The conductor contact portion comprises a first conductor contact portion. The device comprises: a second interconnect layer provided in at least an upper
25 portion of the first insulating film; a second oxidation-resistant conductor film covering the top of the second interconnect layer; and a second conductor contact portion passing through the third insulating film and the second insulating film to reach the second

oxidation-resistant conductor film. The first conductor contact portion has a greater upper surface area than the second conductor contact portion. In this case, if the third insulating film and the second insulating film are partly removed in forming these conductor contact portions, the region where the first conductor contact portion is formed is removed deeper.

5 However, since the top of the first interconnect layer is covered with the oxidation resistant film, corrosion of the first interconnect layer can be prevented even though the oxidation resistant film is exposed.

 The first conductor contact portion may be of rectangular or strip-like plane, and the second conductor contact portion may be of circular or square plane.

10 The first interconnect layer and the first conductor contact portion may constitute a seal ring provided in ring shape. In this case, even though the first conductor contact portion serving as the seal ring differs greatly in area from the second conductor contact portion, the structure described above can prevent the first interconnect layer from being exposed.

15 An element may be provided in the semiconductor substrate, and the interconnect layer may be electrically connected to the element. In this case, when the third insulating film and the second insulating film are partly removed in forming the conductor contact portion, an error would arise in the depth to be removed. Even though such an error arises, it can become difficult to expose the interconnect layer.

20 The second insulating film is preferably an insulating film of silicon compound containing carbon.

 A first method for fabricating a semiconductor device according to the present invention comprises: the step (a) of forming a first insulating film on a semiconductor substrate; the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film; the step (c) of forming a recess in an upper portion of the interconnect layer; the step (d) of forming, on the first insulating film and the interconnect layer, a second insulating film filling the recess; the step (e) of planarizing an upper surface of the

25

second insulating film; the step (f) of forming a third insulating film on the second insulating film after the step (e); the step (g) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located above the interconnect layer so that the removed part does not reach the interconnect layer, thereby
5 leaving part of the second insulating film on the interconnect layer; and the step (h) of removing the photoresist.

With this method, the portion of the second insulating film located on the interconnect layer can be formed thick. Therefore, in the step (g), the state in which the interconnect layer is not exposed can be kept more certainly. This prevents corrosion of
10 the interconnect layer even though treatment that may corrode metal, such as ashing, is carried out after the step (g). On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed thick. Therefore, in the semiconductor device fabricated by the first method, the dielectric constant between the layers can be kept constant.

15 In the step (c), the upper portion of the interconnect layer may be recessed by chemical mechanical polishing, dry etching, or wet etching to form the recess. In this case, in addition to the above effect, the effect of improving the adhesion between the first insulating film and the second insulating film can be provided.

In the step (b), a first interconnect layer for a seal ring and a second interconnect
20 layer located in a region surrounded with the first interconnect layer may be formed as the interconnect layer. In the step (c), the recess may be formed in at least an upper portion of the first interconnect layer. In the step (g), portions of the third insulating film and the second insulating film located above the first interconnect layer may be partly removed to form a trench for the seal ring, and portions of the third insulating film and the second
25 insulating film located above the second interconnect layer may be partly removed to form a hole. Since, in this case, the opening area of the trench is greater than that of the hole, the trench is formed to have a greater depth than the hole in the step (g). However, the

region of the second insulating film to be formed with the trench is formed thick, whereby it can become difficult to expose the first interconnect layer.

In the step (b), the first interconnect layer may be formed to have a greater width than the second interconnect layer. In this case, the region where the first interconnect
5 layer is formed has a higher area ratio of conductor (metal) than the region where the second interconnect layer is formed. Therefore, when, in the step (c), chemical mechanical polishing or similar treatment is carried out on the first interconnect layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

10 In the step (b), a dummy interconnect layer may be formed beside the first interconnect layer. In this case, the surrounding of the region where the first interconnect layer is formed has a higher area ratio of conductor (metal) than the surrounding of the region where the second interconnect layer is formed. Therefore, when, in the step (c), chemical mechanical polishing or similar treatment is carried out on the first interconnect
15 layer and the second interconnect layer from above, the recess formed in the upper portion of the first interconnect layer can be deepened by the metal area ratio dependence of dishing.

The first method may further comprise, prior to the step (a), the step (i) of forming an element in the semiconductor substrate. In the step (b), the interconnect layer may be
20 formed to be electrically connectable to the element. In this case, even though an error in the depth to be removed arises in the step (g), it can become difficult to expose the interconnect layer.

A second method for fabricating a semiconductor device according to the present invention comprises: the step (a) of forming a first insulating film on a semiconductor
25 substrate; the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film; the step (c) of forming an oxidation-resistant conductor film covering the top of the interconnect layer; the step (d) of forming a second insulating film on the

first insulating film and the oxidation-resistant conductor film; the step (e) of forming a third insulating film on the second insulating film; the step (f) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located above the interconnect layer; and the step (g) of removing the photoresist.

5 With this method, the oxidation-resistant conductor film can cover the top of the interconnect layer. Therefore, in the step (f), even if treatment that may corrode metal, such as ashing, is carried out after exposure of the oxidation-resistant conductor film, corrosion of the interconnect layer can be prevented. On the other hands, all portions of the second insulating film but the portion located on the interconnect layer are not formed
10 thick. Therefore, in the semiconductor device fabricated by the second method, the dielectric constant between the layers can be kept constant.

 In the step (c), plasma treatment, wet treatment, or ion implantation may be performed to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film.

15 In the step (c), a film containing nitrogen may be deposited, as the oxidation-resistant conductor film, on the interconnect layer.

 In the step (b), a first interconnect layer for a seal ring and a second interconnect layer located in a region surrounded with the first interconnect layer may be formed as the interconnect layer. In the step (c), an oxidation-resistant conductor film may be formed on
20 the first interconnect layer and the second interconnect layer. In the step (f), portions of the third insulating film and the second insulating film located above the first interconnect layer may be partly removed to form a trench for the seal ring, and portions of the third insulating film and the second insulating film located above the second interconnect layer may be partly removed to form a hole. Since, in this case, the opening area of the trench is
25 greater than that of the hole, the trench is formed to have a greater depth than the hole in the step (f). However, the region of the second insulating film to be formed with the trench is formed thick, whereby it can become difficult to expose the first interconnect layer.

The second method may further comprise, prior to the step (a), the step (h) of forming an element in the semiconductor substrate, and in the step (b), the interconnect layer may be formed to be electrically connectable to the element. In this case, even though an error in the depth to be removed arises in the step (f), it can become difficult to
5 expose the interconnect layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A to 1F are sectional views showing a semiconductor device fabrication method according to a first embodiment.

10 FIGS. 2A to 2F are sectional views showing a semiconductor device fabrication method according to a second embodiment.

FIGS. 3A to 3E are sectional views showing a semiconductor device fabrication method according to a third embodiment.

15 FIGS. 4A to 4E are sectional views showing a semiconductor device fabrication method according to a fourth embodiment.

FIGS. 5A to 5F are sectional views showing a fabrication method of an interconnect region of a semiconductor device according to a fifth embodiment.

FIGS. 6A to 6E are planar views of the first metal interconnect, the hole-contact portion, the second metal interconnect, and the trench-contact portion of embodiments 1-4.

20 FIGS. 7A to 7F are views showing a method of forming a semiconductor device including dummy interconnects 213 (213a and 213b), and 313 (313a and 313b), which are formed adjacent the first interconnect layer 113 (113a and 113b).

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

25 (First Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a first

embodiment of the present invention will be described with reference to FIGS. **1A** to **1F**. FIGS. **1A** to **1F** are sectional views showing the semiconductor device fabrication method of the first embodiment. Note that FIGS. **1A** to **1F** show an interconnect formation region **R1** and a seal ring region **R2** for protecting the interconnect formation region **R1** against
5 outside moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region **R1**.

First, in the step shown in FIG. **1A**, a first insulating film **101** of a silicon oxide film having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **101**, a photoresist (not shown) having openings in interconnect trace
10 formation positions is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby removing part of the first insulating film **101** to form interconnect grooves **108** and **109** with a depth of 250 nm. Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper
15 film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first metal interconnect **102** consisting of a conductor surface film **102a** and a metal interconnect film **102b**. The conductor surface film **102a** covers the inside surface of the interconnect groove **108**, and the metal interconnect film **102b** fills the interconnect groove **108** with the conductor surface film **102a** interposed
20 between the first insulating film **101** and the metal interconnect film **102b**. During this formation, in the seal ring region **R2**, a second metal interconnect **103** is formed which consists of a conductor surface film **103a** and a metal interconnect film **103b**.

In the step shown in FIG. **1B**, by chemical mechanical polishing or selective metal etching with nitric acid or the like, the upper portions of the first metal interconnect **102**
25 and the second metal interconnect **103** are recessed to form recessed shapes (recesses **110**) having depths of about 20 to 40 nm.

Next, in the step shown in FIG. **1C**, on the substrate, a second insulating film **104** is

deposited which is made of a silicon carbon nitride film with a thickness of 100 to 150 nm and which fills the recess **110**. In this deposition, as the material for the second insulating film **104**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be
5 formed as the second insulating film **104**.

At the time of this deposition, depressions affected by the recess shapes of the first metal interconnect **102** and the second metal interconnect **103** are created in the upper surface of the second insulating film **104**.

Then, in the step shown in FIG. **1D**, chemical mechanical polishing, wet etching
10 with sulfuric acid, nitric acid, or the like or etch back is performed to planarize the upper surface of the second insulating film **104**. By this planarization, portions of the second insulating film **104** located on the first metal interconnect **102** and the second metal interconnect **103** have thicknesses of about 70 to 90 nm and the remaining portions thereof have a thickness of 50 nm.

15 In the step shown in FIG. **1E**, a third insulating film **105** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **105**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **105**.

20 Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region and a trench formation region is formed on the third insulating film **105**. Then, dry etching is performed using the photoresist as a mask to form a hole (through hole) **106** in the interconnect formation region **R1** and a trench **107** in the seal ring region **R2**. This dry etching is performed so that the hole **106** and the trench
25 **107** extend halfway through the second insulating film **104**. Since, in this etching, the opening area of the trench **107** is greater than that of the hole **106**, the trench **107** is etched deeper. Thereafter, the photoresist is removed by ashing, and polymers created during wet

etching and dry etching are removed.

In the step shown in FIG. 1F, the remaining portions of the second insulating film **104** within the hole and trench are etched, whereby the hole **106** and the trench **107** reach the first metal interconnect **102** and the second metal interconnect **103**, respectively. The
5 resulting hole and trench are filled with a conductor to form a hole-contact portion **106'** made of conductor (referred hereinafter to as a conductor hole-contact portion) in circular or square plane and a trench-contact portion **107'** of conductor (referred hereinafter to as a conductor trench-contact portion) in ring shape. This step is performed after completion of processes that may corrode metal, such as ashing and polymer removal.

10 With reference to FIG. 1F again, next description will now be made of the structure of the interconnect and the seal ring of the semiconductor device according to the first embodiment.

As shown in FIG. 1F, the semiconductor device of the first embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of
15 the interconnect formation region **R1**. The interconnect formation region **R1** is provided with the first metal interconnect **102**, and the seal ring region **R2** is provided with the second metal interconnect **103**. The first metal interconnect **102** includes the conductor surface film **102a** covering the surface of the interconnect groove **108** and the metal interconnect film **102b** covering the conductor surface film **102a**. Likewise, the second
20 metal interconnect **103** includes the conductor surface film **103a** covering the surface of the interconnect groove **109** and the metal interconnect film **103b** provided on the conductor surface film **103a**. The upper portions of the first metal interconnect **102** and the second metal interconnect **103** are recessed to form the recesses **110**.

The second insulating film **104** is provided on the first insulating film **101**, the first
25 metal interconnect **102** and the second metal interconnect **103**. The second insulating film **104** fills the recess **110**, so that in the second insulating film **104**, the portions thereof located on the first metal interconnect **102** and the second metal interconnect **103** are

formed thicker than the other portions thereof. The upper surface of the second insulating film **104** is planarized.

The third insulating film **105** is provided on the second insulating film **104**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **106'** passing through the third insulating film **105** and the second insulating film **104**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **107'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **103** and the conductor trench-contact portion **107'** is provided to surround the first metal interconnect **102** and the conductor hole-contact portion **106'** in the interconnect formation region **R1**.

The effects obtained by the first embodiment will be described below in comparison with the conventional device.

In the conventional device, the upper surfaces of the first metal interconnect and the second metal interconnect remain flat, and the second insulating film with a uniform thickness is formed on the first metal interconnect and the second metal interconnect. By such a structure, when the hole and the trench are formed, the trench might pass through the second insulating film to expose the second metal interconnect.

In contrast to this, in the first embodiment, only the portions of the second insulating film **104** located on the first metal interconnect **102** and the second metal interconnect **103** can be formed thick. This prevents the trench **107** from reaching the second metal interconnect **103**. Therefore, even if ashing and polymer removal are performed on the semiconductor surface, the first metal interconnect **102** will not corrode. On the other hands, the portion of the second insulating film **104** located on the first insulating film **101** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, chemical mechanical polishing or selective etching is performed to recess the upper surfaces of the first metal interconnect **102** and the second metal

interconnect **103**. This improves the adhesion between the first insulating film **101** and the second insulating film **104**.

In the first embodiment, by chemical mechanical polishing or the like, the recessed shapes are formed in the upper portions of the first metal interconnect **102** and the second metal interconnect **103**. However, in the present invention, the recessed shape may be formed by utilizing the property of copper in which copper is compressed by heat added thereto. To be more specific, in the step shown in FIG. **1A**, the first metal interconnect **102** and the second metal interconnect **103** are formed and then heat treatment is performed at 200 to 500°C. This compresses the metal interconnect films **102b** and **103b** made of copper to form recesses in the upper portions of the first metal interconnect **102** and the second metal interconnect **103**. Also by this procedure, the same effects as those described above can be obtained.

(Second Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a second embodiment of the present invention will be described with reference to FIGS. **2A** to **2F**. FIGS. **2A** to **2F** are sectional views showing the semiconductor device fabrication method of the second embodiment. Note that FIGS. **2A** to **2F** show an interconnect formation region **R1** and a seal ring region **R2** for protecting the interconnect formation region **R1** against outside moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region **R1**.

First, in the step shown in FIG. **2A**, a first insulating film **111** of a silicon oxide film having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **111**, a photoresist (not shown) having openings in a metal interconnect trace formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby forming an interconnect groove **118** in the interconnect formation region **R1** and an interconnect groove **119** in the seal ring formation region **R2**.

In this etching, the width of the interconnect groove **119** is made greater than that of the interconnect groove **118**. To be more specific, when the interconnect groove **118** has a width smaller than 2 μm , the interconnect groove **119** has a width of 2 μm or greater.

Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first metal interconnect **112** having a width of 2 μm or greater and consisting of a conductor surface film **112a** and a metal interconnect film **112b**. The conductor surface film **112a** covers the inside surface of the interconnect groove **118**, and the metal interconnect film **112b** fills the interconnect groove **118** with the conductor surface film **112a** interposed between the first insulating film **111** and the metal interconnect film **112b**. During this formation, in the seal ring region **R2**, a second metal interconnect **113** with a width of 2 μm or greater is formed which consists of a conductor surface film **113a** and a metal interconnect film **113b**.

In the step shown in FIG. **2B**, chemical mechanical polishing is performed. In this step, the upper portion of the second metal interconnect **113** is recessed by utilizing the metal area ratio dependence of dishing. Details of this step are as follows. If a substrate with metal embedded therein is subjected to chemical mechanical polishing, the depth to which the metal is removed tends to be greater as the percentage of metal contained in the region to be removed rises. In the second embodiment, the second metal interconnect **113** is formed to have a greater width than the first metal interconnect **112**. In other words, the region where the second metal interconnect **113** is formed has a higher ratio of metal per unit area. This allows the upper portion of the second metal interconnect **113** to be recessed deeper than the other regions.

As a substitute for the method in which the depth of the second metal interconnect **113** is made greater than that of the first metal interconnect **112**, the percentage of metal

content per unit area may be raised by forming a dummy pattern around the second metal interconnect **113**.

Next, in the step shown in FIG. **2C**, a second insulating film **114** made of a silicon carbon nitride film is deposited on the first insulating film **111**, the first metal interconnect **112** and the second metal interconnect **113**. In this deposition, as the material for the second insulating film **114**, use may be made of a silicon nitride film, a silicon oxide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **114**.

At the time of this deposition, a depression affected by the recess shape of the second metal interconnect **113** is created in the upper portion of the second insulating film **114**.

Then, in the step shown in FIG. **2D**, chemical mechanical polishing, wet etching, or etch back is performed to planarize the second insulating film **114**.

In the step shown in FIG. **2E**, a third insulating film **115** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **115**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **115**.

Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region and a trench formation region is formed on the third insulating film **115**. Then, dry etching is performed using the photoresist as a mask to form a hole **116** in the interconnect formation region **R1** and a trench **117** in the seal ring region **R2**. This dry etching is performed so that the trench **117** extends halfway through the second insulating film **114**. Since, in this etching, the opening area of the trench **117** is greater than that of the hole **116**, the trench **117** is etched deeper. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG. 2F, the remaining portions of the second insulating film **114** within the hole and trench are removed, whereby the hole **116** and the trench **117** reach the first metal interconnect **112** and the second metal interconnect **113**, respectively. The resulting hole and trench are filled with a conductor to form a conductor hole-contact portion **116'** in circular or square plane and a conductor trench-contact portion **117'** in ring shape. This step is performed after completion of processes that may corrode metal, such as ashing and polymer removal.

With reference to FIG. 2F again, next description will now be made of the structure of the interconnect and the seal ring of the semiconductor device according to the second embodiment.

As shown in FIG. 2F, the semiconductor device of the second embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of the interconnect formation region **R1**. The interconnect formation region **R1** is provided with the first metal interconnect **112**, and the seal ring region **R2** is provided with the second metal interconnect **113**. The second metal interconnect **113** is formed to have a greater width than the first metal interconnect **112**.

The first metal interconnect **112** includes the conductor surface film **112a** covering the surface of the interconnect groove **118** and the metal interconnect film **112b** covering the conductor surface film **112a**. Likewise, the second metal interconnect **113** includes the conductor surface film **113a** covering the surface of the interconnect groove **119** and the metal interconnect film **113b** provided on the conductor surface film **113a**. The upper portion of the second metal interconnect **113** is recessed to form a recess **120**.

The second insulating film **114** is provided on the first insulating film **111**, the first metal interconnect **112** and the second metal interconnect **113**. The second insulating film **114** fills the recess **120**, so that in the second insulating film **114**, the portion thereof located on the second metal interconnect **113** is formed thicker than the other portions thereof. The upper surface of the second insulating film **114** is planarized.

The third insulating film **115** is provided on the second insulating film **114**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **116'** passing through the third insulating film **115** and the second insulating film **114**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **117'**. Thus, in
5 the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **113** and the conductor trench-contact portion **117'** is provided to surround the first metal interconnect **112** and the conductor hole-contact portion **116'** in the interconnect formation region **R1**.

The effects obtained by the second embodiment will be described below in
10 comparison with the conventional device.

In the conventional device, the upper surface of the second metal interconnect remains flat, and the second insulating film with a uniform thickness is formed on the second metal interconnect. By such a structure, when the hole and the trench are formed, the trench might pass through the second insulating film to expose the second metal
15 interconnect.

In contrast to this, in the second embodiment, only the portion of the second insulating film **114** located on the second metal interconnect **113** can be formed thick without increasing the number of fabrication steps of the device. This prevents the trench **117** from reaching the second metal interconnect **113**. Therefore, even if ashing and
20 polymer removal are performed on the semiconductor surface, the first metal interconnect will not corrode. On the other hands, the portion of the second insulating film **114** located on the first insulating film **111** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, chemical mechanical polishing or etching is performed to recess the
25 upper portion of the second metal interconnect **113**. This improves the adhesion between the first insulating film **111** and the second insulating film **114**.

In the second embodiment, the recessed shape is formed by utilizing the metal area

ratio dependence of dishing. However, it may be formed by etching utilizing the pattern density dependence. Alternatively, in the step shown in FIG. **2B** in the present invention, the recessed shape may be formed in the upper portion of the second metal interconnect **113** by performing etching with a photoresist or the like covering all the region but the
5 second metal interconnect **113**. In this case, the same effects as those described above can be obtained except that the number of fabrication steps of the device increases.

In the second embodiment, in performing chemical mechanical polishing in the step shown in FIG. **2B**, slurry with high solubility, such as hydrogen peroxide, may be used. This raises the polishing rate of metal, which allows the second metal interconnect **113** to
10 be recessed deeper.

(Third Embodiment)

A method for fabricating a semiconductor device according to a third embodiment of the present invention will be described with reference to FIGS. **3A** to **3E**. FIGS. **3A** to
15 **3E** are sectional views showing the semiconductor device fabrication steps of the third embodiment. Note that FIGS. **3A** to **3E** show an interconnect formation region **R1** and a seal ring region **R2** for protecting the interconnect formation region **R1** against outside moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region **R1**.

20 First, in the step shown in FIG. **3A**, a first insulating film **121** of a silicon oxide film having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **121**, a photoresist (not shown) having openings in a metal interconnect trace formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby removing part of the first insulating film **121** to form
25 interconnect grooves **128** and **129** with a depth of 250 nm. Thereafter, the photoresist is removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper

film and the stacked film are polished using chemical mechanical polishing to form, in the interconnect formation region **R1**, a first metal interconnect **122** consisting of a conductor surface film **122a** and a metal interconnect film **122b**. The conductor surface film **122a** covers the inside surface of the interconnect groove **128**, and the metal interconnect film
5 **122b** fills the interconnect groove **128** with the conductor surface film **122a** interposed between the first insulating film **121** and the metal interconnect film **122b**. During this formation, in the seal ring region **R2**, a second metal interconnect **123** is formed which consists of a conductor surface film **123a** and a metal interconnect film **123b**.

In the step shown in FIG. **3B**, plasma treatment using a gas containing nitrogen, wet
10 treatment using ammonia, benzotriazole (BTA), or quinaldic acid, or ion implantation is performed to supply nitrogen to the upper portions of the first metal interconnect **122** and the second metal interconnect **123**. This alters the upper portions of the first metal interconnect **122** and the second metal interconnect **123** into an oxidation resistant film **130**. Simultaneously, this step can improve the adhesion between the first insulating film **121**
15 and a second insulating film **124** that will be formed in a subsequent step.

Next, in the step shown in FIG. **3C**, the second insulating film **124** made of a silicon carbon nitride film is deposited on the first insulating film **121** and the oxidation resistant film **130**. In this deposition, as the material for the second insulating film **124**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film,
20 or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **124**.

In the step shown in FIG. **3D**, a third insulating film **125** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **125**, use may be made of an FSG (fluorinated silicate glass) film, a
25 BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **125**.

Subsequently to this, by photolithography, a photoresist (not shown) having

openings in a hole formation region and a trench formation region is formed on the third insulating film **125**. Then, dry etching is performed using the photoresist as a mask to form a hole **126** in the interconnect formation region **R1** and a trench **127** in the seal ring region **R2**. This dry etching may be performed either so that the trench **127** extends only
5 halfway through the second insulating film **124** or so that the trench **127** passes through the second insulating film **124** to reach the oxidation resistant film **130**. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG. **3E**, the remaining portions of the second insulating film
10 **124** within the hole and trench are removed, whereby the hole **126** and the trench **127** reach the oxidation resistant film **130**. The resulting hole and trench are filled with a conductor to form a conductor hole-contact portion **126'** in circular or square plane and a conductor trench-contact portion **127'** in ring shape.

With reference to FIG. **3E** again, next description will now be made of the structure
15 of the interconnect and the seal ring of the semiconductor device according to the third embodiment.

As shown in FIG. **3E**, the semiconductor device of the third embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of the interconnect formation region **R1**. The interconnect formation region **R1** is provided
20 with the first metal interconnect **122**, and the seal ring region **R2** is provided with the second metal interconnect **123**. The first metal interconnect **122** includes the conductor surface film **122a** covering the surface of the interconnect groove **128** and the metal interconnect film **122b** covering the conductor surface film **122a**. Likewise, the second metal interconnect **123** includes the conductor surface film **123a** covering the surface of
25 the interconnect groove **129** and the metal interconnect film **123b** provided on the conductor surface film **123a**. The upper portions of the metal interconnect films **122b** and **123b** contain nitrogen and thus are formed into the oxidation resistant film **130**.

The second insulating film **124** is provided on the first insulating film **121**, the first metal interconnect **122** and the second metal interconnect **123**. The third insulating film **125** is provided on the second insulating film **124**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **126'** passing through the third
5 insulating film **125** and the second insulating film **124**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **127'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **123** and the conductor trench-contact portion **127'** is provided to surround the first metal interconnect **122** and the conductor hole-contact portion **126'** in the interconnect formation region **R1**.

10 The effects obtained by the third embodiment will be described below in comparison with the conventional device.

In the conventional device, if a trench reaches the second metal interconnect during formation of the hole pattern and the trench pattern, then the second metal interconnect corrodes in subsequent ashing and polymer removal.

15 In contrast to this, in the third embodiment, the upper portion of the second metal interconnect **123** is altered into the oxidation resistant film **130**. Therefore, even if ashing and polymer removal are performed in the state in which the trench **127** reaches the second metal interconnect **123**, the upper portion of the second metal interconnect **123** will not corrode. On the other hands, the portion of the second insulating film **124** located on the
20 first insulating film **121** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, the upper portions of the first metal interconnect **122** and the second metal interconnect **123** are made to contain nitrogen, which also provides the advantage that the etching resistance in the formation of the hole **126** and the trench **127** is improved.

25 In the step shown in FIG. **3D**, in the case where the hole **126** and the trench **127** reach the oxidation resistant film **130**, the later step of removing portions of the second insulating film **124** remaining between the oxidation resistant film **130** and each of the hole

126 and the trench **127** can be advantageously omitted.

(Fourth Embodiment)

A method for fabricating a semiconductor device according to a fourth embodiment
5 of the present invention will be described with reference to FIGS. **4A** to **4E**. FIGS. **4A** to
4E are sectional views showing the semiconductor device fabrication steps of the fourth
embodiment. Note that FIGS. **4A** to **4E** show an interconnect formation region **R1** and a
seal ring region **R2** for protecting the interconnect formation region **R1** against outside
moisture. The seal ring region **R2** surrounds the sides of the interconnect formation region
10 **R1**.

First, in the step shown in FIG. **4A**, a first insulating film **131** of a silicon oxide film
having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first
insulating film **131**, a photoresist (not shown) having openings in a metal interconnect
trace formation region is formed by photolithography. The formed photoresist is used as a
15 mask to perform dry etching, thereby removing part of the first insulating film **131** to form
interconnect grooves **138** and **139** with a depth of 250 nm. Thereafter, the photoresist is
removed, and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum
and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper
film and the stacked film are polished using chemical mechanical polishing to form, in the
20 interconnect formation region **R1**, a first metal interconnect **132** consisting of a conductor
surface film **132a** and a metal interconnect film **132b**. The conductor surface film **132a**
covers the inside surface of the interconnect groove **138**, and the metal interconnect film
132b fills the interconnect groove **138** with the conductor surface film **132a** interposed
between the first insulating film **131** and the metal interconnect film **132b**. During this
25 formation, in the seal ring region **R2**, a second metal interconnect **133** is formed which
consists of a conductor surface film **133a** and a metal interconnect film **133b**.

In the step shown in FIG. **4B**, an oxidation-resistant metal film **140** is selectively

deposited on the first metal interconnect **132** and the second metal interconnect **133**. An exemplary material for the metal film **140** is titanium nitride (TiN).

Next, in the step shown in FIG. **4C**, a second insulating film **134** made of a silicon carbon nitride film is deposited on the first insulating film **131** and the metal film **140**. In this deposition, as the material for the second insulating film **134**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **134**. Subsequently to the deposition, chemical mechanical polishing, wet etching, or etch back is performed to planarize the second insulating film **134**.

In the step shown in FIG. **4D**, a third insulating film **135** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **135**, use may be made of an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **135**.

Subsequently to this, by photolithography, a photoresist (not shown) having openings in a hole formation region and a trench formation region is formed on the third insulating film **135**. Then, dry etching is performed using the photoresist as a mask to form a hole **136** in the interconnect formation region **R1** and a trench **137** in the seal ring region **R2**. This dry etching may be performed either so that the trench **137** extends only halfway through the second insulating film **134** or so that the trench **137** passes through the second insulating film **134** to reach the metal film **140**. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG. **4E**, the remaining portions of the second insulating film **134** within the hole and trench are removed, whereby the hole **136** and the trench **137** reach the first metal interconnect **132** and the second metal interconnect **133**, respectively. The resulting hole and trench are filled with a conductor to form a conductor hole-contact portion **136'** in circular or square plane and a conductor trench-contact portion **137'** in ring

shape.

With reference to FIG. 4E again, next description will now be made of the structure of the interconnect and the seal ring of the semiconductor device according to the fourth embodiment.

5 As shown in FIG. 4E, the semiconductor device of the fourth embodiment includes the interconnect formation region **R1** and the seal ring region **R2** surrounding the sides of the interconnect formation region **R1**. The interconnect formation region **R1** is provided with the first metal interconnect **132**, and the seal ring region **R2** is provided with the second metal interconnect **133**. The first metal interconnect **132** includes the conductor
10 surface film **132a** covering the surface of the interconnect groove **138** and the metal interconnect film **132b** covering the conductor surface film **132a**. Likewise, the second metal interconnect **133** includes the conductor surface film **133a** covering the surface of the interconnect groove **139** and the metal interconnect film **133b** provided on the conductor surface film **133a**.

15 The oxidation-resistant metal film **140** made of, for example, titanium nitride is provided on the first metal interconnect **132** and the second metal interconnect **133**. The second insulating film **134** is provided on the first insulating film **131** and the metal film **140**. The third insulating film **135** is provided on the second insulating film **134**. The interconnect formation region **R1** is provided with the conductor hole-contact portion **136'**
20 passing through the third insulating film **135** and the second insulating film **134**. Likewise, the seal ring region **R2** is formed with the conductor trench-contact portion **137'**. Thus, in the seal ring region **R2**, the seal ring in ring shape formed of the second metal interconnect **133** and the conductor trench-contact portion **137'** is provided to surround the first metal interconnect **132** and the conductor hole-contact portion **136'** in the interconnect formation
25 region **R1**.

In the fourth embodiment, the metal film **140** resistant to oxidation covers the top of the second metal interconnect **133**. Therefore, even if ashing and polymer removal are

performed in the state in which the trench **137** reaches the metal film **140**, the upper portion of the second metal interconnect **133** will not corrode. On the other hands, the portion of the second insulating film **134** located on the first insulating film **131** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

5 Moreover, the upper portions of the first metal interconnect **132** and the second metal interconnect **133** are formed with the metal film **140** resistant to oxidation, which also provides the advantage that the etching resistance in the formation of the hole **136** and the trench **137** is improved.

10 (Fifth Embodiment)

Hereinafter, a method for fabricating a semiconductor device according to a fifth embodiment of the present invention will be described with reference to FIGS. **5A** to **5F**. FIGS. **5A** to **5F** are sectional views showing a method for fabricating an interconnect region of a semiconductor device according to the fifth embodiment. The foregoing first to
15 fourth embodiments have shown the case where a difference in depth arises between the hole in the interconnect region and the trench in the seal ring region. On the other hands, the fifth embodiment shows the case where in forming a number of hole patterns in the interconnect region, a difference in depth arises among the hole patterns.

First, in the step shown in FIG. **5A**, a first insulating film **141** of a silicon oxide film
20 having a thickness of 500 nm is formed on a silicon substrate (not shown). On the first insulating film **141**, a photoresist (not shown) having openings in a metal interconnect trace formation region is formed by photolithography. The formed photoresist is used as a mask to perform dry etching, thereby removing part of the first insulating film **141** to form an interconnect groove **148** with a depth of 250 nm. Thereafter, the photoresist is removed,
25 and then a 30 nm-thick stacked film (not shown) of tantalum nitride and tantalum and a 1000 nm-thick copper film (not shown) are formed above the substrate. The copper film and the stacked film are polished using chemical mechanical polishing to form a metal

interconnect **142** consisting of a conductor surface film **142a** and a metal interconnect film **142b**. The conductor surface film **142a** covers the inside surface of the interconnect groove **148**, and the metal interconnect film **142b** fills the interconnect groove **148** with the conductor surface film **142a** interposed between the insulating film **141** and the metal
5 interconnect film **142b**.

In the step shown in FIG. **5B**, by chemical mechanical polishing or selective metal etching with nitric acid or the like, the upper portion of the metal interconnect **142** is recessed to form a recessed shape (recess **150**) having a depth of about 20 to 40 nm.

Next, in the step shown in FIG. **5C**, on the substrate, a second insulating film **144** is
10 deposited which is made of a silicon carbon nitride film with a thickness of 100 to 150 nm and which fills the recess **150**. In this deposition, as the material for the second insulating film **144**, use may be made of a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like. Also, a structure made by stacking the listed films may be formed as the second insulating film **144**.

15 At the time of this deposition, a depression affected by the recess shape of the metal interconnect **142** is created in the top of the second insulating film **144**.

Then, in the step shown in FIG. **5D**, chemical mechanical polishing, wet etching or etch back is performed to planarize the upper surface of the second insulating film **144**. By this planarization, a portion of the second insulating film **144** located on the metal
20 interconnect **142** has a thickness of about 70 to 90 nm and the remaining portions thereof have a thickness of 50 nm.

In the step shown in FIG. **5E**, a third insulating film **145** made of a carbon-containing silicon oxide film is deposited above the substrate. In this deposition, as the third insulating film **145**, use may be made of an FSG (fluorinated silicate glass) film, a
25 BPSG (boron phosphorus silicate glass) film, or a porous film. Also, a structure made by stacking the listed films may be used as the third insulating film **145**.

Subsequently to this, by photolithography, a photoresist (not shown) having

openings in a hole formation region is formed on the third insulating film **145**. Then, dry etching is performed using the photoresist as a mask to form holes **146**. This dry etching is performed so that the holes **146** extend halfway through the second insulating film **144**. At the time of completion of this etching, respective holes **146** of multiple hole patterns have
5 different depths due to influences of the pattern density or the like. Thereafter, the photoresist is removed by ashing, and polymers created during wet etching and dry etching are removed.

In the step shown in FIG. **5F**, the remaining portions of the second insulating film **144** within the holes are removed, whereby the holes **146** reach the metal interconnect **142**.
10 The resulting holes are filled with a conductor to form conductor hole-contact portions **146'** in circular or square plane. This step is performed after completion of processes that may corrode metal, such as ashing and polymer removal.

With reference to FIG. **5F** again, next description will now be made of the structure of the interconnect and the conductor hole-contact portion of the semiconductor device
15 according to the fifth embodiment.

As shown in FIG. **5F**, in the semiconductor device of the fifth embodiment, the metal interconnect **142** which includes the conductor surface film **142a** and the metal interconnect film **142b** covering the top of the conductor surface film **142a** is provided in the first insulating film **141**. The upper portion of the metal interconnect **142** is recessed to
20 form the recess **150**.

The second insulating film **144** is provided on the first insulating film **141** and the metal interconnect **142**. The second insulating film **144** fills the recess **150**, so that in the second insulating film **144**, the portion thereof located on the metal interconnect **142** is formed thicker than the other portions thereof. The upper surface of the second insulating
25 film **144** is planarized.

The third insulating film **145** is provided on the second insulating film **144**. Further, the conductor hole-contact portion **146'** is provided which passes through the third

insulating film **145** and the second insulating film **144**.

The effects obtained by the fifth embodiment will be described below in comparison with the conventional device.

In the conventional device, the upper surface of the metal interconnect remains flat,
5 and the second insulating film and the third insulating film are formed on the metal interconnect. If multiple types of hole patterns are formed in such a structure, the formed hole patterns have different hole depths due to nonuniform pattern densities or fabrication process variations. This might cause some of the hole patterns to pass through the second insulating film to reach the metal interconnect. Such a possibility increases particularly in
10 the case where a number of hole patterns are formed in the device.

In contrast to this, in the fifth embodiment, only the portion of the second insulating film **144** located on the metal interconnect **142** can be formed thick. This prevents the holes **146** from reaching the metal interconnect **142**. Therefore, even if ashing and polymer removal are performed on the semiconductor surface, the metal interconnect
15 **142** will not corrode. On the other hands, the portion of the second insulating film **144** located on the first insulating film **141** is not formed thick. Therefore, the dielectric constant between the layers can be kept constant.

Moreover, chemical mechanical polishing or selective etching is performed to recess the upper surface of the metal interconnect **142**. This improves the adhesion
20 between the first insulating film **141** and the second insulating film **144**.

The fifth embodiment is composed by applying the method of the first embodiment to the case where multiple types of hole patterns are formed in an interconnect region. However, in the present invention, methods of the third and fourth embodiments can also be applied to that case.

25 In the first to fourth embodiments, description has been made of the case where the conductor trench-contact portion is formed in ring shape to use the portion as the seal ring. Alternatively, the portion may be formed in rectangular shape or strip shape to use the

portion as part of an electrode.