

Silicon Processing

for the VLSI Era
Volume 1—Process Technology

S. Wolf and R.N. Tauber



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**SILICON PROCESSING
FOR
THE VLSI ERA
VOLUME 1:
PROCESS TECHNOLOGY**

SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1: PROCESS TECHNOLOGY

STANLEY WOLF Ph.D.

Professor, Department of Electrical Engineering
California State University, Long Beach
Long Beach, California

and

Instructor, Engineering Extension, University of California, Irvine

RICHARD N. TAUBER Ph.D.

Manager of VLSI Fabrication
TRW - Microelectronics Center
Redondo Beach, California

and

Instructor, Engineering Extension, University of California, Irvine

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BASICS OF THIN FILMS

A large variety of "thin films" are used in the fabrication of VLSI devices. These films may be thermally grown or deposited from the vapor phase. They can be metals, semiconductors, or insulators. Figure 1 shows a cross-section of an advanced CMOS device illustrating some of the instances in which thin films are used. Since thin films are so important to VLSI devices, an understanding of their chemical and physical properties leads to a better understanding of their behavior in devices.

Thin films for use in VLSI fabrication must satisfy a large set of rigorous chemical, structural, and electrical requirements. Film composition and thickness must be strictly controlled to facilitate etching of submicron features. Very low densities of both particulate defects and film imperfections, such as pinholes, become critical for the small linewidths, high densities, and large areas necessary for VLSI. These small geometries also create highly rugged topography for overlying films to cover. Therefore, excellent adhesion, low stress, and conformal step coverage are required of a VLSI thin film, and its own surface topography should reduce or even planarize the underlying steps if possible. Finally, non-conducting thin films must have low dielectric constants to reduce parasitic capacitances exacerbated by the scaled down film thicknesses.

Although the properties of a bulk material may be well characterized, the same material in its thin film form may have properties substantially different from those of the bulk. One reason is that thin film properties are strongly influenced by surface properties, while in bulk materials this is not the case. The thin film, by its very definition has a substantially higher surface-to-volume ratio than does a bulk material. The structure of thin films, and their method of preparation also play a vital role in determining the film properties.

The formation of such films is accomplished by a large variety of techniques (which are the subject of subsequent chapters), but which can conceptually be divided into two groups: 1) film growth by interaction of a vapor-deposited species with the substrate; and 2) film formation by

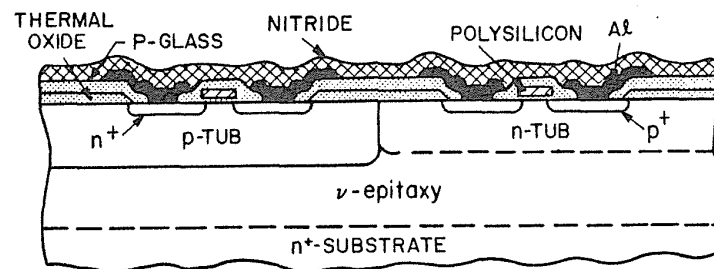


Fig. 1 Examples of types of thin films used in VLSI fabrication¹⁴. (© 1980 IEEE.)

deposition without causing changes to the substrate material. The first category includes thermal oxidation and nitridation of single crystal silicon (Chap. 7) and polysilicon (Chap. 6), and the formation of silicides by direct reaction of a deposited metal and the substrate (Chap. 11).

The second group includes another three subclasses of deposition: a) chemical vapor deposition, or CVD, in which solid films are formed on a substrate by the *chemical* reaction of vapor phase chemicals that contain the required constituents; b) physical vapor deposition, or PVD, in which the species of the thin film are *physically* dislodged from a source (to form a vapor), which is transported across a reduced pressure region to the substrate, where it condenses to form the thin film; and c) coating of the substrate with a liquid, which is then dried to form the solid thin film. When CVD process are used to form single-crystal thin films, the process is termed *epitaxy* and is the subject of Chap. 5. The formation of amorphous and polycrystalline thin films by CVD is discussed in Chaps 6 and 11. The formation of thin films by PVD includes the processes of sputtering and evaporation (Chap. 10), and molecular beam epitaxy (Chap. 5). The deposition of a liquid on a substrate to form thin films, most commonly by spin-coating, is discussed in Chap. 12 as part of the photoresist process presentation.

The purpose of this chapter is to discuss the terminology and properties common to thin films in general. That is, basic background information on the growth mechanism, structure, mechanical properties, and electrical properties of thin films is provided for readers not well acquainted with materials science concepts. By defining these properties in a stand-alone chapter, it is not necessary to repeat this information each time a new thin film deposition method is introduced. The specific formation and associated processing of particular films is described in detail in later chapters.

THIN FILM GROWTH

Thin films are most commonly prepared by condensation of atoms or molecules from the vapor phase. This implies that during formation, a change of phase from the vapor to the solid occurs (also termed *condensation*). Deposition on a substrate different from the film requires the consideration of a third phase (i.e. that of the adsorbed atoms which have not yet combined with other adsorbed atoms). Condensation is initiated by the formation of small *clusters* (or *nuclei*) through the random agglomeration of several adsorbed atoms. The enlargement of these nuclei to form a coherent film is termed *growth*. Often nucleation and growth can occur simultaneously during film formation. The growth of thin films is discussed in detail in many standard reference works (e.g. Maissel and Glang¹, and Chopra²).

Thin Film Nucleation

The condensation of vapor atoms requires that attraction occurs as the vapor atoms impinge upon the surface. Either dipole or quadropole attractive forces can result in an atom becoming attached to the surface (which after becoming attached to the surface, is then referred to as an *adatom*). In order to undergo attachment, the atom must transfer the normal component of its velocity to the surface. If the attachment occurs without a transfer of electrons, the adsorption mechanism is known *physisorption*, while if electrons are transferred, it is termed *chemisorption*. The binding energies associated with physisorption are typically much smaller than those of chemisorption (i.e. ~ 0.25 eV vs. 8-10 eV). Adsorbed atoms may continue to move along the surface by jumping into other positions (i.e. by moving from potential well-to-potential well), as a result of the kinetic energy associated with their initial lateral velocity, or by thermal

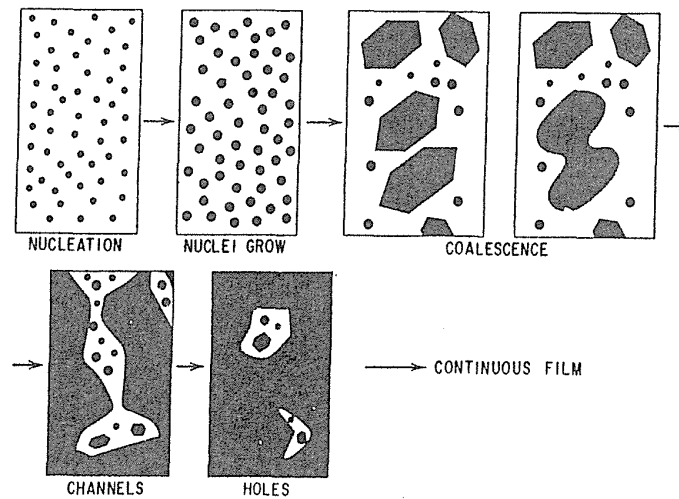


Fig. 2 Schematic of the stages of thin film growth. From Maissel and Glang, Eds. *Handbook of Thin Film Technology*, 1970¹. Reprinted with permission of McGraw-Hill Book Co.

activation from the surface. On the other hand, in some cases the adatoms may re-evaporate from the surface into the vapor phase. As the adatoms migrate along the surface they can interact with other adatoms to form stable clusters, called *nuclei*, and the mechanism of their formation is known as *nucleation*. The onset of *condensation* is also marked by the initial formation of the nuclei. The theory of nucleation (see Chap. 2) was developed by Gibbs for the case of liquid droplet condensation from a vapor. Basically, the theory shows that for molecular clusters greater than a critical size, the total free energy of the system decreases with increasing size, so that continued growth is energetically favorable. This model is also applicable to cases of condensation on surfaces. If the critical radius is not reached, atom clusters are more likely to shrink and re-evaporate. The tendency for nuclei to form and remain stable results from the lowering of the total system free energy as the nuclei grow above the critical radius. The higher the supersaturation in the vapor phase the smaller the critical radius that results.

After the formation of critical sized nuclei (which also tend to grow to supercritical dimensions by depleting the adatoms in the "capture zones" around them), the film *growth stage* begins. Film growth has been studied with the aid of electron microscopy and several stages of growth have been observed (Fig. 2). The *island stage* occurs when nuclei grow in three dimensions, but growth parallel to the substrate exceeds growth normal to the substrate. This effect arises as a result of diffusion of adatoms along the surface. In the island stage, nuclei may have well-defined crystallographic shapes. This stage is followed by *coalescence*, where nuclei contact each other and form new larger and rounded shapes. The total area projected on the substrate is reduced at this step (Fig. 2), but the height of the deposit is increased. Eventually during coalescence, larger islands may again take on a crystallographic appearance, in the form of hexagonal shapes (Fig. 2). Since the surface area covered by these structures decreases, fresh substrate surface is exposed, allowing for additional nucleation in these areas (secondary nucleation). The large islands continue to grow, leaving behind channels or holes of exposed substrate (*channel stage*). The channels are then filled by secondary nucleation, to result in a continuous film.

STRUCTURE OF THIN FILMS

Thin film generally have smaller grain size than do bulk materials. *Grain size* is a function

of the deposition conditions and annealing temperatures. Larger grains are observed for increased film thickness, with the effect increasing with increasing substrate (deposition) temperature. It is also noted that the grain size saturates under these conditions, indicating that new grains nucleate upon existing ones. Larger grains are expected for increased substrate and annealing temperatures, as a result of the increased surface mobility. Annealing a film at a temperature equal to that at which it was deposited does not produce as large grains. The initial deposition temperature plays a more important role in determining the final grain size. The dependence on deposition rate is due to the fact that even if clusters have high mobility, at high deposition rate they are quickly buried under subsequent layers. For very high deposition rates, the heat of condensation can raise the substrate temperature (thereby producing increased grain size from thermal effects).

The *surface roughness* of films occurs as a result of the randomness of the deposition process. Real films almost always show surface roughness, even though this represents a higher energy state than that of a perfectly flat film. Depositions at high temperatures tend to show less surface roughness. This is because increased surface mobility from the higher substrate temperatures can lead to filling of the peaks and valleys. On the other hand, higher temperatures can also lead to the development of crystal facets, which may continue to grow in favored directions, leading to *increased* surface roughness. At low temperatures the surface roughness (as measured by surface area) tends to increase with increased film thickness. Oblique deposition which results in shadowing, also increases surface roughness. Epitaxial and amorphous deposits have shown measured surface area nearly equal to the geometrical area, implying the existence of very flat films. This has been confirmed by SEM examination of these films. Surface roughness has also been observed to increase as a result of the presence of contamination on the substrate (or in the vapor phase) during deposition.

The *density* of a thin film provides information about its physical structure. Density is usually determined by weighing the film and measuring its volume (area x thickness). If a film is porous from the deposition process, it generally has a lower density than bulk material.

The *crystallographic structure* of thin films depends on the adatom mobility, and can vary from a highly disordered (or amorphous-like) state, to a well-ordered state (e.g. epitaxial growth on a single crystal substrate). The amorphous structures are frequently observed for the deposited dielectrics such as SiO_2 , SiO , and Si_3N_4 , while most metals result in polycrystalline structure. Silicon can be either amorphous, polycrystalline, or single crystal, depending on the deposition parameters and the substrate material.

Some polycrystalline films deposit with a *fiber texture* or *preferred orientation*. This texture can be described as having a preponderance of grains with the same orientation in a direction normal to the substrate. Deposition of polycrystalline Si on SiO_2 can occur in this manner. The observed fiber texture in that case has been reported as $\{110\}$ for poly-Si deposited at 600-650°C.

Epitaxy describes the phenomenon of an oriented overgrowth of one substance on the crystal surface of another substance. If the film and the substrate are composed of the same material, this growth is termed *homoepitaxy* (e.g. Si on Si, GaAs on GaAs), while if the film and substrate are different materials, such growth is termed *heteroepitaxy* (e.g. Si on Al_2O_3).

The single crystal substrate is the dominant factor in epitaxy. Some crystal symmetry must exist between the deposit and the substrate, and the lattice parameters of each material must be close to the same value. The lattice misfit, which is the percentage difference between the lattice constant of the deposit and that of the substrate plane in contact, must be small to achieve epitaxy. The deposition temperature also plays a role in epitaxy. Elevated temperatures increase the propensity for epitaxial growth. This is engendered by several mechanisms, including: cleaner surfaces; decreased supersaturation; and increased adatom energy.

The deposition rate also plays a role in epitaxy. Lower rates tend toward epitaxy, while

higher deposition rates lead to polycrystalline or amorphous deposition. Three growth regimes are observed for the deposition of Si on a clean Si substrate: a) at low temperature and high deposition rates the deposits are amorphous; b) at high substrate temperatures and low rate deposition they tend to be single crystal; and c) at intermediate conditions polycrystalline films tend to form. Chapter 5 discusses the growth of epitaxial silicon films in much more detail.

MECHANICAL PROPERTIES OF THIN FILMS

Adhesion

The adhesion of grown and deposited films used in VLSI processing must be excellent (both *as deposited*, and after subsequent processing). If films lift from the substrate device failure can result, and thus poor adhesion represents a potential reliability problem.

Early attempts at measuring adhesion used: a) the *tape test*; or b) a method of *abrasion testing*. The tape method consists of pressing a piece of adhesive tape to the film. When the tape is pulled off, the film is either removed (in whole or in part), or remains on the substrate. This method is qualitative, and if the film remains on the substrate, it provides no data as to the magnitude of the adhesion forces. If the film is removed, a quantitative value of the adhesion can be obtained by measuring the force to remove it. For most films used in VLSI processing, failure of the tape test implies that the film is unsuitable for device fabrication.

The *abrasion* or *scratch method* gives results which depend both on the film hardness, as well as on its adhesion. A vertical load is applied to a chrome-steel point which is drawn across the film surface. The load is increased until the point strips the film completely from the substrate leaving a deep channel (i.e. critical load is reached). The stripping is generally observed with a microscope. The critical load is taken as a measure of the adhesion. Critical loads ranging from several grams to hundreds of grams are observed, depending on the film and the substrate. It has been found that the critical load depends strongly on the film thickness. The stylus scratches the film so the mechanical strength and hardness of the film also play a role in this test. Therefore the method is least valid for films greater than $2000\text{\AA}$ thick.

A relatively simple quantitative pull test can also measure adhesion. In this test, a small metal pin is attached to the film surface (after the surrounding film material has been removed), with an epoxy that does not react with the film material (Fig. 3). An increasing force is applied normal to the substrate surface, until either the film-substrate or film-epoxy bond fails.

Adhesion energy values between film and substrate have been measured, and range from several tenths of an electron volt to 10 eV or more. In order to explain this wide range of values,

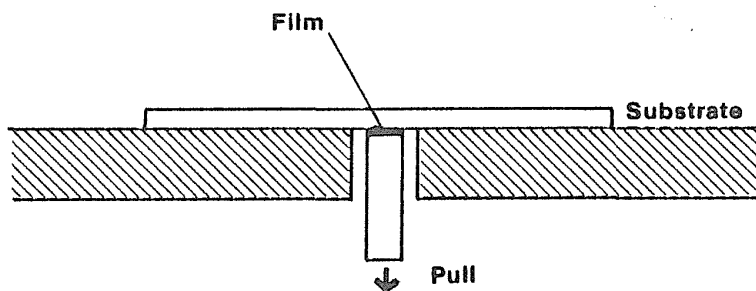


Fig. 3 Apparatus for measuring the force required to detach a film from its substrate.

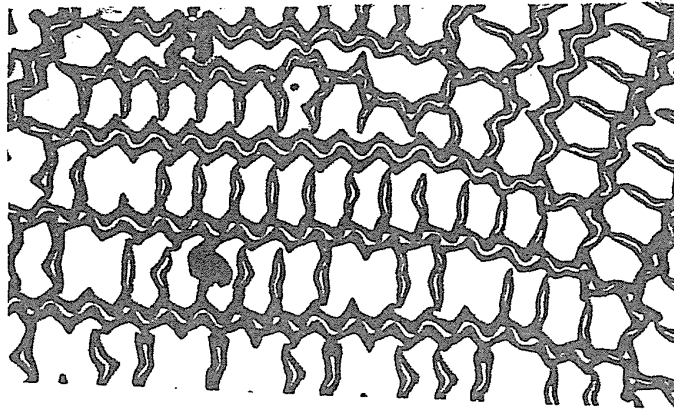


Fig. 4 W on mica at 300°C, showing buckle waves. From K.I. Chopra, *Thin Film Phenomena*, 1969². Reprinted with permission of McGraw-Hill Book Co.

two adhesion mechanisms have been postulated. For low values of adhesion, it is surmised that the electron shells of the adsorbed atoms remain intact, and these atoms are held to the surface by *Van der Waals forces*. These forces hold to approximately 0.4 eV, and the atoms are said to be physisorbed on the substrate. Above 0.4 eV, sharing of electrons between the film and substrate occurs, and the atoms are chemisorbed. Generally adhesion is greater the higher the adsorption energy of the deposit and /or the higher the number of nucleation centers in the early growth stage of the film. Chemisorption due to an intermediate-layer formation that allows a continuous transition from one lattice to the other results in excellent adhesion. This is particularly true for the adhesion of strong oxide formers, such as Ti and Al on silicon dioxide. If intermetallic metal alloys form, adhesion is also improved.

Adhesion is also strongly effected by the cleanliness of the substrate. Contamination generally results in reduced adhesion, as does an adsorbed gas layer. Cleaning the substrate prior to deposition is therefore important to insure good film adhesion.

Substrate surface roughness can also affect adhesion. For example, increased roughness may promote adhesion because: a) the substrate exhibits more surface area than a flat surface; and b) mechanical interlocking between the film and substrate may also occur. Excessive roughness, on the other hand, may result in coating defects, which may promote adhesion failure.

It is highly advantageous to include a layer of a strong oxide-forming element between an oxide substrate and the metallization. This is particularly true for gold-based metallization, where a chromium layer can be used to serve as an intermediate "adhesion layer". Intrinsic stress in a thin film is generally not sufficient to result in delamination, unless the film is extremely thick. More often, high stress results in the cracking of films.

Stress in Thin Films

Nearly all films are found to be in a state of internal stress, regardless of the means by which they have been produced. The stress may be *compressive* or *tensile*. Compressively stressed films would like to *expand* parallel to the substrate surface, and in the extreme, films in compressive stress will buckle up on the substrate, as shown in Fig. 4. Films in *tensile stress*, on the other hand, would like to *contract* parallel to the substrate, and may crack if their elastic

limits are exceeded. In general, the stresses in thin films are in the range of 10^8 - 5×10^{10} dynes/cm². Highly stressed films are generally undesirable for VLSI applications for several reasons, including: a) they are more likely to exhibit poor adhesion; b) they are more susceptible to corrosion; c) brittle films, such as inorganic dielectrics, may undergo cracking in tensile stress; and d) the resistivity of stressed metallic films is higher than that of their annealed counterparts. The *total stress*, σ , in a film is the sum of: a) any *external stress*, σ_{ext} , on the film, perhaps from another film; b) the *thermal stress*, σ_{th} ; and c) the *intrinsic stress*, σ_{int} . The total stress is written as:

$$\sigma = \sigma_{ext} + \sigma_{th} + \sigma_{int} \quad (1)$$

Thermal stress results from the difference in the coefficients of thermal expansion between the film and the substrate. The intrinsic stress results from the structure of the growing films. The *thermal stress* is due to the constraint imposed by the film-substrate bonding and is given by:

$$\sigma_{th} = (\alpha_f - \alpha_s) (\Delta T) E_f \quad (2)$$

where: α_f and α_s are the average coefficients of thermal expansion for the film and the substrate, respectively; ΔT is the temperature of film growth (or deposition), minus the temperature of measurement; and E_f is the Young's modulus of the film. The σ_{th} can be of either sign (positive is tensile, negative is compressive), based on the relative values of α_f and α_s . For example, SiO₂ grown or deposited on silicon at elevated temperatures will have a compressive component as part of its total stress, since $\alpha_{Si} > \alpha_{SiO_2}$.

The *intrinsic stress* reflects the film structure in ways not yet completely understood. It has been observed that the intrinsic stress in a film depends on thickness, deposition rate, deposition temperature, ambient pressure, method of film preparation, and type of substrate used, among other parameters.

At low substrate temperatures, metal films tend to exhibit tensile stress. This decreases with increasing substrate temperature (often in a linear manner), finally going through zero (or even becoming compressive). The changeover to compressive stress occurs at lower temperatures for lower melting point metals.

The stress in a thin film is known to vary with depth. This may be a manifestation of a

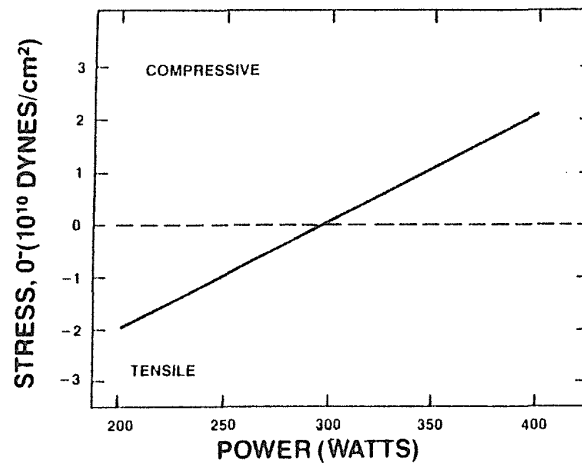


Fig. 5 Variation of stress in sputter-deposited thin film tungsten, versus sputter deposition power. Courtesy of Materials Research Corp (MRC).

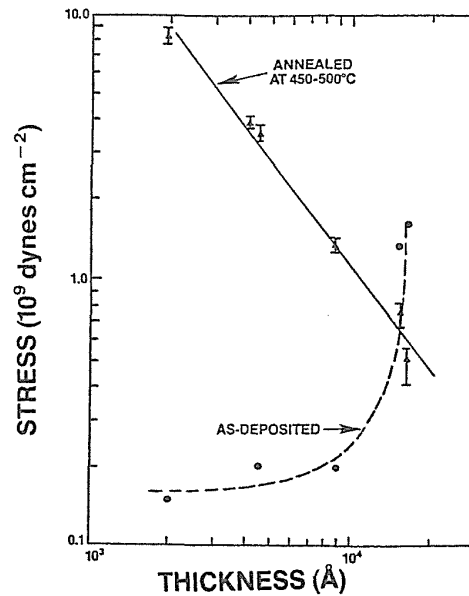


Fig. 6 Stress *versus* thickness for annealed aluminum films. Courtesy of Materials Research Corp (MRC).

change in film structure with depth. Figure 5 shows film stress as a function of thickness for aluminum films, both as-deposited and annealed. In the range of interest of films for VLSI the stress is relatively low and constant. The as-deposited films show an increase in stress with thickness. With no stress relief during cooling from the annealing temperature, a stress of 10^{10} dyne/cm² would be expected. Clearly stress relief has occurred as evidenced by a lower stress value. Crystalline slip (see Chap. 2) is a mechanism of stress relief.

The effect of deposition rate on film stress is ambiguous. Figure 5 shows data for stress as a function of power (deposition rate) for sputtered tungsten. The film stress starts out tensile, decreases as the power increases, and finally becomes compressive with further power increase.

The origin of thermal stress is easily understood. Intrinsic stresses however are more difficult to explain as they may arise from several causes. Several models relating to the origins of intrinsic stress have been proposed. These invoke the following stress-causing mechanisms: a) lattice mismatch between the substrate and the film; b) rapid film growth (which locks in defects); and c) incorporation of impurities into the film.

Measurement of stress is a relatively straight-forward procedure based upon beam bending. It can be performed on commercial laser wafer-flatness measuring equipment. This technique also allows the stress to be directly determined on the substrate that the film is deposited upon. The procedure is based upon the phenomenon that the stresses in a film on a thin substrate will result in the bending of the substrate.

A tensile stress in the film bends the substrate so that it becomes concave (Fig. 7a), while a compressive stress makes the substrate convex (Fig. 7b). In the wafer or disc method, the film is deposited on one side, and stress is determined by measuring the deflection of the wafer center. Use of laser flatness equipment allows direct measurement of the disc deflection. Previously, use of an optical flat was required, so that deflection could be determined from the interference fringes (Newton's rings) in an interferometer. Stress in films using this method is found from:

$$\sigma = \frac{E_s D}{6 r T} \quad (6)$$

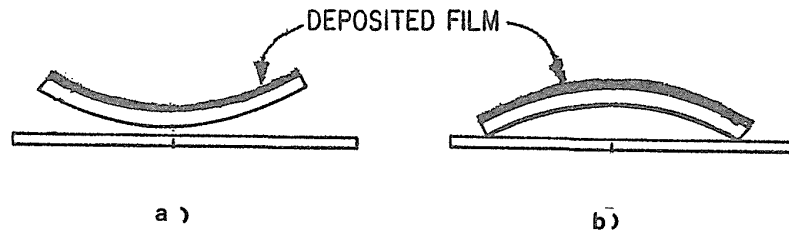


Fig. 7 (a) Tensile stress causes *concave* bending, and (b) compressive stress causes *convex* bending of substrate.

where: r is the measured radius of curvature of the bent substrate; E_s is Young's modulus of the substrate; D is the thickness of the substrate; and t is the thickness of the film. For films used in silicon processes, the assumption that $t \ll D$, is generally valid. Films are typically less than $1 \mu\text{m}$ (1×10^{-4} cm) thick, while wafers are 5×10^{-2} cm thick, and $D \sim 5 \times 10^{-2}$ cm. Any curvature that is inherent in the substrate must be measured before the film is deposited and algebraically added to the final measured radius of curvature. In reality this method measures the product $\sigma t = F$, called the force per unit width, from which the average stress can be calculated. The instantaneous stress is given by dF/dt . For very thin films (i.e. $t \rightarrow 0$), the measurement is dubious, unless it is known that the film stress is independent of thickness.

Another method of measuring the radius of curvature or deflection of the substrate involves measuring a capacitance change. This is achieved by using the film as one plate of the capacitor. Stress may also be measured by use of x-ray or electron diffraction of the stressed thin film. In such techniques, the changes in the lattice parameter and diffraction line broadening are excellent measures of the films' strain (which in turn can be used to calculate the stress).

The stress in the film is determined from the lattice parameter change and is given by:

$$\sigma = \frac{E_f}{2\mu_f} \left[\frac{a_o - a}{a_o} \right] \quad (4)$$

where: a_o and a are the unstressed and stressed lattice constants, respectively; and μ_f is the Poisson ratio; and E_f Young's modulus of the film.

Equation 4 is valid for the case of the lattice constant perpendicular to the film plane. For the case of the lattice constant *in* the plane of the film, the stress is given by:

$$\sigma = \frac{E_f}{1 - \mu_f} \left[\frac{a - a_o}{a_o} \right] \quad (5)$$

The use of diffraction line broadening to determine the strain in the film requires the apportioning of the measured value between small crystallite effects, and the strain in the film.

Other Mechanical Properties

Stress-strain curves of thin films can often be obtained by several techniques. Values of the *elastic modulus* can be measured from the slope of the curve in the linear region. The total elongation at fracture in a metal film may be only 1-2%, and may exhibit a large elastic component. The *tensile strength* is the maximum value of the breaking force divided by the original cross-sectional area. The tensile strength of thin metal films has been measured to be

up to 200 times larger than annealed bulk samples.

The *microhardness* of a film shows a strong correlation with tensile strength. For example, the value of both properties decreases as the deposition temperature is increased. Palatnik⁷ studied the effect on the microhardness of aluminum thin film due to the presence of aluminum oxide and alloying additions of Cu, as well as other materials. Both the aluminum oxides and the alloying additions were found to increase the microhardness of the film. Knowledge of the hardness of thin films is important in developing such processes as attaching wires from integrated circuit packages to the chip bonding pads. The hardness of the film is one parameter that establishes the bonding-tool pressure required to form a strong wire-bond.

Microhardness can be measured by pressing a hard, specially shaped point into the surface, and observing the indentation. Read⁸ has reviewed the available methods for hardness measurements. The Vicker microhardness measuring procedure uses a diamond pyramid of four faces with edges of equal length, while the Knoop system uses a pyramid in which the length of two edges is seven times that of the other two. The Knoop's penetration into the film is one-third less than the Vickers. The minimum limiting film thickness for valid measurements is about $1.5 \times 10^4 \text{ \AA}$ for the Knoop test, since the film thickness must be at least ten times the penetration depth. That is, for deeper indentations, as the indenter penetrates toward the interface, the substrate begins to interfere with the measurement).

ELECTRICAL PROPERTIES OF METALLIC THIN FILMS

The electrical conductivity of a material is due to the motion of charge carriers (electrons in metals, electrons or holes in semiconductors) through the lattice under the influence of applied electric fields⁹. These electrons are affected by non-periodicity in the lattice. Such non-periodicity results from the lattice vibrations (phonons) that exist at all temperatures above absolute zero (0°K), and lattice defects, such as impurities, vacancies, interstitials, dislocations, grain boundaries, and alloying additions. The total resistivity is given by Mathiessen's rule, which states the resistivity of a material is the arithmetic sum of the individual contributions made by all sources of resistance. It is convenient to combine all contributions other than the thermal component of resistivity into a term referred to as *residual resistivity*. That is:

$$\rho = \rho_{\text{temp}} + \rho_{\text{residual}} \quad (6)$$

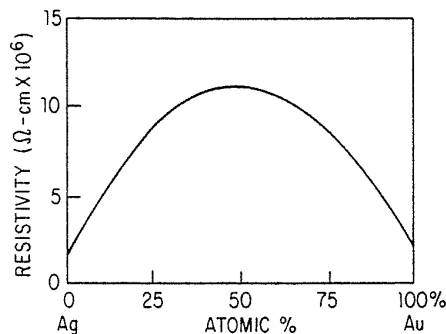


Fig. 8 Resistivity vs. composition for the gold-silver system. From Maissel and Glang, Eds., *Handbook of Thin Film Technology*, 1970¹. Reprinted by permission of McGraw-Hill Book Co.

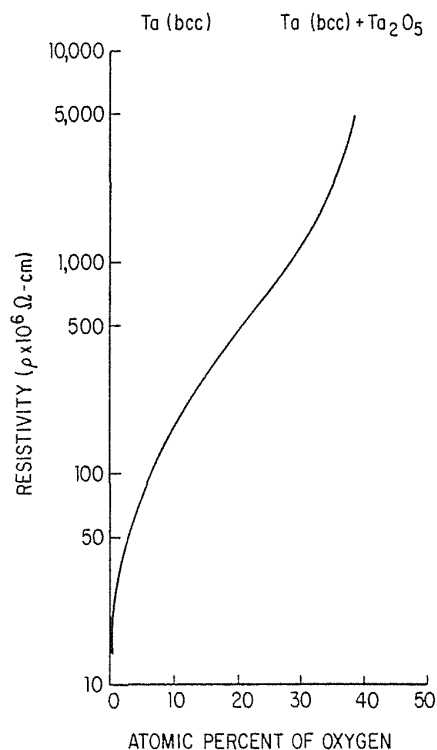


Fig. 9 Resistivity of Ta as function O impurity concentration. From Maissel and Glang, Eds., *Handbook of Thin Film Technology*, 1970¹. Reprinted with permission of McGraw-Hill Book Co.

The resistivity of metal thin films is generally higher than that of the bulk counterpart. This results from the fact that films generally contain more defects (e.g. dislocations $\sim 10^{10} \text{ cm}^{-2}$), and grain boundaries, than do bulk materials.

The composition of the thin film may also play a major role in the resistivity that it exhibits. Figure 8 shows the effect of alloy additions on the resistivity of the Ag-Au system (which shows complete solid solubility). The resistivity increases with the addition of solute. The addition of small amounts of impurities can cause very large changes in resistivity. For example, the addition of oxygen in tantalum (Fig. 9) results in resistivity increases several orders of magnitude, as Ta_2O_5 (an insulator) is formed. The contribution of *vacancies* and *interstitials* to the resistivity, on the other hand, is on the order of $1 \mu\Omega\text{-cm}$ per atomic percent per vacancy or interstitial, and can therefore generally be neglected. The scattering power of dislocations is also small. The effect of grain boundaries on the resistivity of bulk materials is relatively small, since grain boundaries can be treated arrays of dislocations.

Measurement of the Electrical Properties of Thin Films

As shown in Fig. 10 the resistance of a rectangular shaped section of film of length, l , width, b , and thickness, t (measured in the direction parallel to the film), is given by:

$$R = \frac{\rho l}{t b} \quad (7)$$

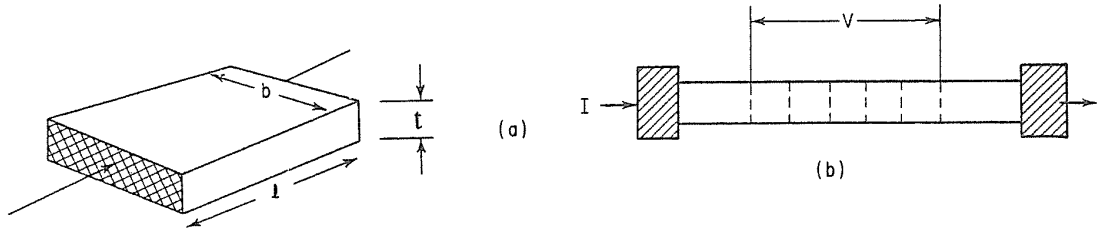


Fig. 10 (a) Definition of sheet resistance. (b) Direct measurement of sheet resistance. From Maissel and Glang, Eds., *Handbook of Thin Film Technology*, 1970¹. Reprinted with permission of McGraw-Hill Book Co.

where R is the resistance of the film, ρ is the resistivity, and t is the film thickness. If $l = b$, Eq. 7 then becomes:

$$R = \rho / t = R_s \quad (8)$$

where R_s is the sheet resistance in Ω /square of the film, and is independent of the size of the square (but depends only on the film resistivity, and thickness of the film). If the thickness and sheet resistance are known, the film resistivity is given by:

$$\rho = R_s t \quad (9)$$

The sheet resistance, R_s , can be measured by several techniques. In the direct measurement, a conductor strip is fabricated (Fig. 10b). The voltage drop across the length of the strip is measured, as a current is driven through the conductor. The resistance of the conductor is given by $R = V / I$. The number of squares are counted between the voltage terminals, and $R_s = R / N$, when N is the number of squares ($N = L / b$).

A second method which does not require the use of a strip is the *4-point probe method*, described in detail by Valdes¹² (Fig. 11). If the sample is semi-infinite with regards to the probe spacings, and the probe spacings s are equal, then the resistivity is given by:

$$\rho = \frac{V}{I} 2\pi s \quad (10)$$

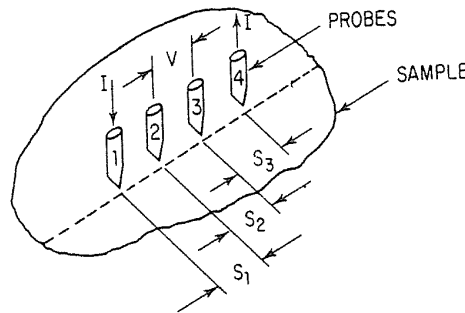


Fig. 11 In-line four point probe. From Maissel and Glang, Eds., *Handbook of Thin Film Technology*, 1970¹. Reprinted with permission of McGraw-Hill Book Co.

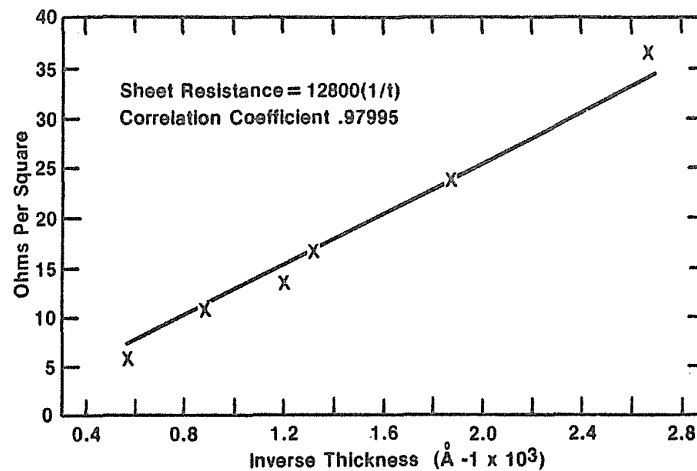


Fig. 12 TiW sheet resistance as a function of $1/t$. From S. Lim and D. Ridley, *Solid State Tech.*, Feb. 83, p. 99. Reprinted with permission of Solid State Technology, Published by Technical Publishing, A Company of Dun & Bradstreet.

If the material on which the probe is placed is an infinitely thin slice on an insulating substrate, then Eq. 10 reduces to:

$$\rho = \frac{V t \pi}{I \ln 2} \quad (11)$$

Depending on the probe spacing relative to the boundaries, and thickness of the sample, there are various geometric correction factors that apply to Eq. 1. The reader is referred to Valdes paper or page 268 of this text for these corrections. Commercial equipment is used for measuring R_s in thin metal films, and semiconductor layer is available.

The sheet resistivity measurement technique is also used to indirectly measure the thickness of conductive films deposited on insulating substrates (e.g. metal, silicide, or semiconductor films), especially if the films are less than 1000Å thick (since stylus profilometer instruments are difficult to use with such thin films). The thickness, t , and the sheet resistance are related by Eq. 9. Thus, the sheet resistance can be utilized to determine thickness only if the resistivity of the film is known. Since the resistivity of thin films is generally different from that of the bulk resistivity, the thin film resistivity is usually measured independently. The preferred method utilizes the fact that the sheet resistance is linear with the inverse of the thickness, and that the slope is equal to the resistivity. Thus, by depositing films of varying thickness, and measuring R_s and t (an independent technique, utilizing a surface profilometer, or SEM, is used to measure t), a plot of R_s vs $1/t$ can be generated. A least square fit of the data will yield a curve from which ρ can be determined. With this information, measurements of R_s on sample films can yield the thickness by using Eq. 9. Figure 12 illustrates such a curve for TiW films. Implicit in this method is the assumption that resistivity is independent of thickness. This assumption is no longer valid when the thickness becomes less than the electron mean free path, since the resistivity will then exhibit a contribution from the surface scattering of the electrons.

An improvement over the 4-point probe is the use of eddy currents, as this is a contactless method. High frequency current through a coil induces current in conducting films placed under the coil, which unbalances the oscillator circuit. The change in the circuit is related to the resistance of the conducting film, which is dependent on the resistivity and the film thickness. Two examples of this type of instrument are the Eddy Co. Model E-1, and the Tencor M-Gage.

The 4-point probe technique also offers one great advantage for showing variations in sheet resistance or thickness by stepping the probes over a test wafer to provide contour maps. This technique is described in additional detail in Chap. 9, in the section dealing with the monitoring of ion implant doses.

The *temperature coefficient of resistance*, α_T (TCR) at a temperature T , is determined from:

$$\alpha_T = \frac{(R_1 - R_2)}{R_T (T_1 - T_2)} \quad (13)$$

where $T_1 > T > T_2$, and the R 's are the resistance values at T_1 , T_2 , and T . A minimum of three resistance measurements must be made (the third being required to see if changes in temperature have resulted in any permanent changes in the resistance of the film). When the TCR is quoted without specifying temperature, T is generally assumed to be 20°C.

Electrical Transport in Thin Metal Films

Although most metal films used in IC fabrication are sufficiently thick to be continuous, and not have surface scattering as a major factor, it is still informative to briefly review the electrical properties exhibited by such thinner films.

As previously discussed, the resistivity of a metal arises from scattering of electrons. Electrons will be scattered when they reach the surface of the film, and the resistivity will increase when the film becomes thin enough so that collisions with surface become a significant fraction of the total number of collisions. This occurs when the film thickness approaches the electron mean free path (mfp) at a given temperature. A mathematical analysis of the problem was first treated by Thomson, who concluded that the conductivity σ at any film thickness is given by:

$$\sigma = \sigma_0 \left[1 - \frac{3(1-p)}{8k} \right] \quad (k \gg 1) \quad (13a)$$

$$\sigma = \sigma_0 \frac{3k}{4} (1 + 2p) \left[\ln \frac{1}{k} + 0.423 \right] \quad (k \ll 1) \quad (13b)$$

where σ_0 is the conductivity of a thick film, k is the ratio of the film thickness to the mean free path, and p is the fraction of electrons elastically scattered.

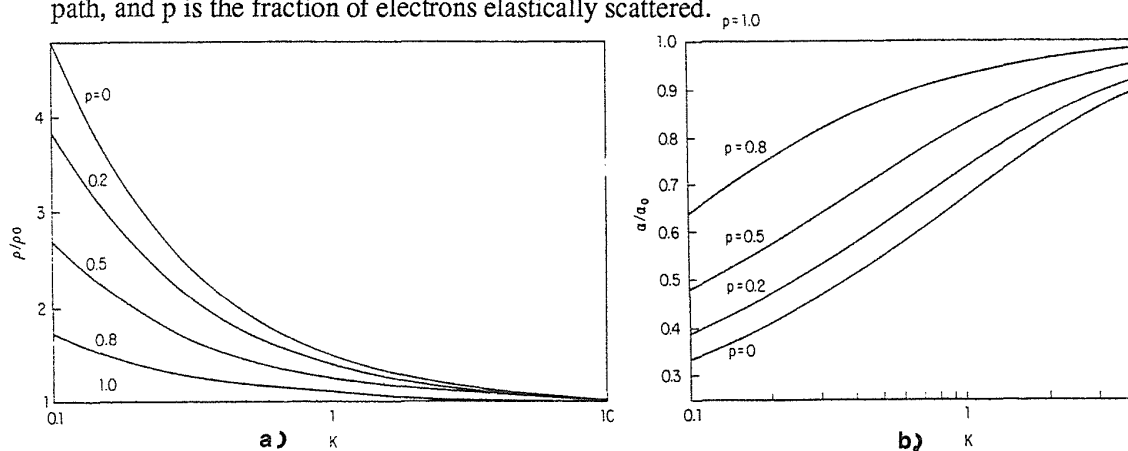


Fig. 13 (a) Effect of film thickness on resistivity. (b) Effect of film thickness on temperature coefficient of expansion. From Maissel and Glang, Eds., *Handbook of Thin Film Technology*, 1970¹. Reprinted with permission of McGraw-Hill Book Co.

Figure 13a is a plot of ρ/ρ_0 (reciprocal of σ) as a function of the ratio k , for different values of p . Figure 13b shows the dependence of α_T on the k factor. Values of the mean free path of the electrons in metals λ depend on temperature, but are typically several hundred Å at 300°K.

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PROBLEMS

1. Calculate the resistance of a Ti:W interconnect line that is 2μm wide, 1500 μm long and (a) 1000 Å thick, and (b) 3000 Å thick (see Fig. 12).
2. The linear thermal coefficient of expansion of Al is on the order of 25×10^{-6} cm / cm /°C, and that for Si is 2.6×10^{-6} cm / cm /°C. Using this information offer an explanation of why thin films of Al on Si substrates exhibit hillocks (See Fig. 36, p. 371, Chap. 10) after being subjected to elevated temperatures (e.g. > 250°C).
3. Explain why compressive stresses in thin films can cause convex bending, and tensile stresses concave bending, of the substrates on which they are deposited.
4. The correction factor for R_s when thick materials are being measured with a four-point probe is shown in Fig. P1. Equation 11 in Chap. 4 must be multiplied by this factor to obtain accurate R_s values from V/I measurements. If a uniformly doped silicon layer with a thickness equal to the probe spacings is measured and $V/I = 45$, calculate its R_s .

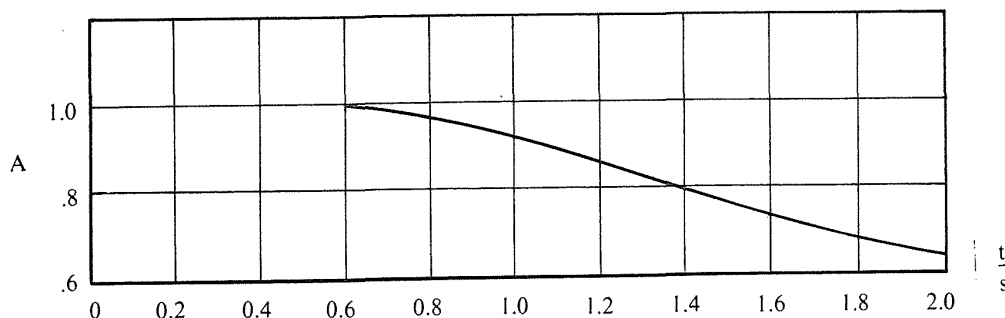


Fig. P1 Correction factor for thick materials on a four-point probe.

CHEMICAL VAPOR DEPOSITION of AMORPHOUS and POLYCRYSTALLINE THIN FILMS

Chemical vapor deposition (CVD) is defined as the formation of a non-volatile solid film on a substrate by the reaction of vapor phase chemicals (reactants) that contain the required constituents. The reactant gases are introduced into a reaction chamber and are decomposed and reacted at a heated surface to form the thin film. A wide variety of thin films utilized in VLSI fabrication is prepared by CVD^{1,2}. In Chap. 5, the growth of single-crystal silicon films by CVD epitaxial techniques is presented. The deposition of amorphous and polycrystalline thin films by CVD is the subject of this chapter (and to a lesser degree, of Chap. 11).

The deposition technology and equipment used to prepare such films by CVD will first be considered. Next a discussion of the properties and deposition conditions of some of the most widely used films deposited by CVD will be undertaken (including polycrystalline silicon, silicon dioxide, and silicon nitride). Information about the properties and deposition of refractory metals and their silicides by CVD is given in Chap. 11. Also note that the measurement of many of the properties of CVD films is virtually identical to the measurement of the same properties in other thin films. Thus, only the measurement of those properties that are unique to the specific thin films under discussion will be mentioned in this chapter. Readers should consult the index for information on various generic thin film measurement methods.

As discussed in Chap. 4, thin films are used in a host of different applications in VLSI fabrication, and can be prepared using a variety of techniques. Regardless of the method by which they are formed, however, the process must be economical (high throughput), and the resultant films must exhibit the following characteristics: a) good thickness uniformity; b) high purity and density; c) controlled composition and stoichiometries; d) high degree of structural perfection; e) good electrical properties; f) excellent adhesion; and g) good step coverage.

Specific deposition methods are developed to form such thin films, based on their potential capabilities for satisfying these demanding criteria. CVD processes are often selected over competing deposition techniques because they offer the following advantages: a) high purity deposits can be achieved; b) a great variety of chemical compositions can be deposited; c) some films cannot be deposited with adequate film properties by any other method; and d) good economy and process control are possible for many films.

BASIC ASPECTS OF CHEMICAL VAPOR DEPOSITION

A CVD process can be summarized as consisting of the following sequence of steps: a) a given composition (and flow rate) of reactant gases and diluent inert gases is introduced into a reaction chamber; b) the gas species move to the substrate; c) the reactants are adsorbed on the substrate; d) the adatoms undergo migration and film-forming chemical reactions, and e) the gaseous by-products of the reaction are desorbed and removed from the reaction chamber. Energy to drive the reactions can be supplied by several methods (e.g. thermal, photons, or electrons), with thermal energy being the most commonly used.

In practice, the chemical reactions of the reactant gases leading to the formation of a solid material may take place not only on (or very close to) the wafer surface (*heterogeneous reaction*), but also in the gas phase (*homogeneous reaction*). Heterogeneous reactions are much more desirable, as such reactions occur selectively only on heated surfaces, and produce good quality films. Homogeneous reactions, on the other hand are undesirable, as they form *gas phase clusters* of the depositing material, which can result in poorly adhering, low density films, or defects in the depositing film. In addition, such reactions also consume reactants and can cause decreases in deposition rates. Thus, one important characteristic of a chemical reaction for CVD application is the degree to which heterogeneous reactions are favored over gas phase reactions.

Since the aforementioned steps of a CVD process are sequential, the one which occurs at the slowest rate will determine the rate of deposition. The steps can be grouped into 1) gas-phase processes, and 2) surface processes. As discussed in Chap. 5, the *gas phase phenomenon of interest* is the rate at which gases impinge on the substrate. This is modeled by the rate at which gases cross the boundary layer that separates the bulk regions of flowing gas and substrate surface. Such transport processes occur by gas-phase diffusion, which is proportional to the diffusivity of the gas, D , and concentration gradient across the boundary layer, dC/dx , see Chap. 5). The rate of mass transport is only relatively weakly influenced by temperature ($D \propto T^{1.5-2.0}$).

Several *surface processes* can be important once the gases arrive at the hot substrate surface, but the *surface reaction*, in general, can be modeled by a thermally activated phenomenon which proceeds at a rate, R , given by:

$$R = R_0 e^{-E_a/kT} \quad (1)$$

where R_0 is the frequency factor, E_a is the activation energy in eV, and T is temperature in °K (see Appendix 3). According to Eq. 1, the surface reaction rate increases with increasing temperature. For a given surface reaction, the temperature may rise high enough so that the reaction rate exceeds the rate at which reactant species arrive at the surface. In such cases, the reaction cannot proceed any more rapidly than the rate at which reactant gases are supplied to the substrate by mass transport, no matter how high the temperature is increased. This situation is referred to as a *mass-transport limited* deposition process.

On the other hand, at lower temperatures, the surface reaction rate is reduced, and eventually the arrival rate of reactants exceeds the rate at which they are consumed by the surface reaction process. Under such conditions the deposition rate is *reaction rate limited*. Thus, at high temperatures, the deposition is usually mass-transport limited, while at lower temperatures it is surface-reaction rate-limited (Fig. 1). In actual processes the temperature at which the deposition condition moves from one of these growth regimes to the other is dependent on the activation energy of the reaction, and the gas flow conditions in the reactor.

In processes that are run under *reaction rate-limited conditions*, the temperature of the

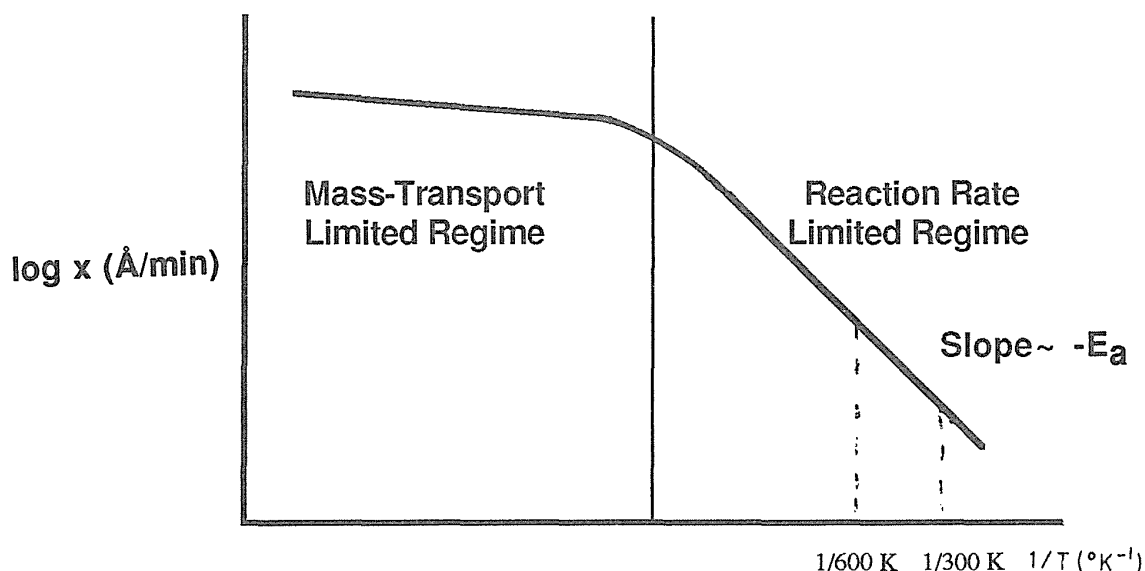


Fig. 1 Temperature dependence of growth rate for CVD films.

process is an important parameter. That is, uniform deposition rates throughout a reactor require conditions that maintain a constant reaction rate. This in turn implies that a constant temperature must also exist everywhere at all wafer surfaces. On the other hand, under such conditions the rate at which reactant species arrive at the surface is not as important, since their concentration does not limit the growth rate. Thus, it is not as critical that a reactor be designed to supply an equal flux of reactants to all locations of a wafer surface. It will be seen that in low-pressure CVD (LPCVD) reactors, wafers can be stacked vertically and at very close spacing because such systems operate in a reaction rate limited mode. The reason for this is as follows:

Under the low pressure of an LPCVD reactor (~1 torr) the diffusivity of the gas species is increased by a factor of 1000 over that at atmospheric pressure, and this is only partially offset by the fact that the boundary layer (the distance across which the reactants must diffuse) increases by less than the square root of the pressure. The net effect is that there is more than an order of magnitude increase in the transport of reactants to (and by-products away from) the substrate surface, and the rate-limiting step is thus the surface reaction⁴. Note, however, that since the surface reaction rate also generally increases with increasing surface concentration, non-uniform gas phase concentrations produced by local depletion of reactants within the reactor can result in deposition non-uniformities. An example of a such an effect is the depletion of reactants from a gas by their deposition on wafers located at the inlet of an end-feed reactor tube. Wafers near the outlet end are consequently exposed to gases containing lower concentrations of reactants than those at the inlet end of the tube.

In deposition processes that are *mass-transport limited*, however, the temperature control is not nearly as critical. As mentioned earlier, the mass transport process which limits the growth rate is only weakly dependent on temperature. On the other hand, it is very important that the same concentration of reactants be present in the bulk gas regions adjacent to all locations of a wafer, as the arrival rate is directly proportional to the concentration in the bulk gas. Thus, to insure films of uniform thickness across a wafer, reactors which are operated in the mass transport limited regime must be designed so that all locations of wafer surfaces and all wafers in a run are supplied with an equal flux of reactant species. Atmospheric pressure reactors that deposit SiO_2 at ~400°C operate in the mass-transport limited regime. The most widely used

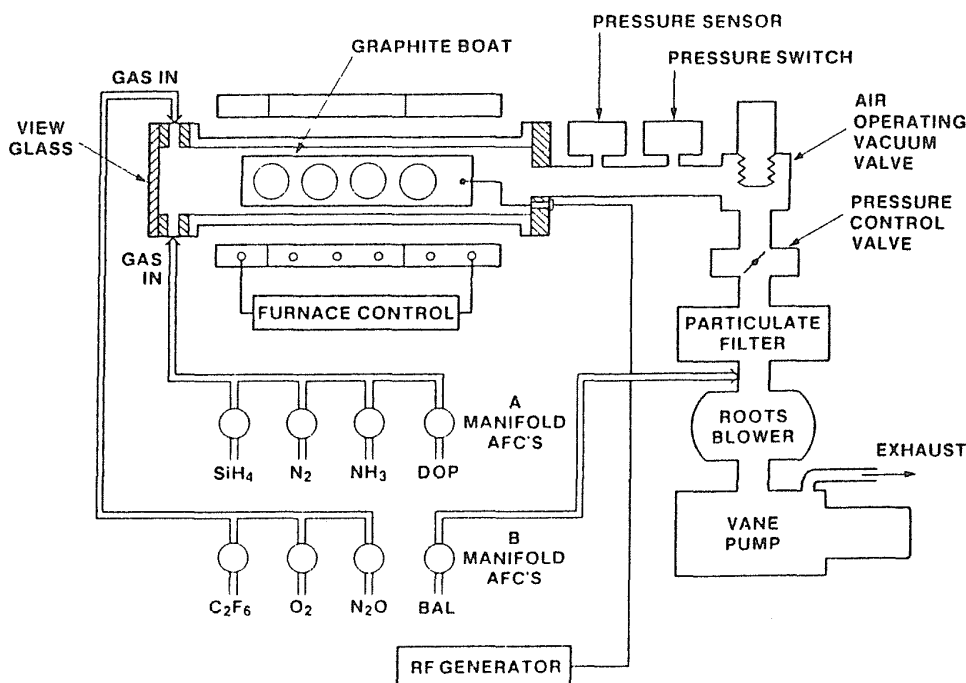


Fig. 2 Diagram of a typical commercial PECVD system. Courtesy of Pacific Western Systems.

APCVD reactor designs provide a uniform supply of reactants by horizontally positioning the wafers and moving them under a gas stream.

CHEMICAL VAPOR DEPOSITION SYSTEMS

Components of CVD Systems

A schematic diagram of a CVD system is shown in Fig. 2. Actually, this figure shows a plasma-enhanced [PECVD] system. Non-plasma enhanced CVD systems can be identically represented, minus the rf generator and matching network, and pump [in atmospheric systems]. CVD reactors are generally *open-flow* systems, in which gases continuously flow into the reaction chamber (where the deposition occurs), and gaseous by-products are exhausted together with unused reactant and diluent gases. Reactant gases are typically carried by diluent (*carrier*) gases such as H_2 , N_2 , or Ar. Corrosive and hazardous gases pumped from the chamber are removed from the exhaust gas flow by a *scrubber*, and the remainder are vented to the atmosphere.

CVD systems usually contain the following components: a) gas sources; b) gas feed lines; c) mass-flow controllers (for metering the gases into the system); d) a reaction chamber (or reactor); e) a method for heating the wafers onto which the film is to be deposited (and in some types of systems, for adding additional energy by other means); and f) temperature sensors. LPCVD and PECVD systems (to be defined) also contain pumps for establishing the reduced pressure and exhausting the gases from the chamber. With the exception of the reaction chamber configurations and mass-flow controllers, a discussion of the operating procedures of all of the components of CVD systems is undertaken in other chapters of the book since they find use in various wafer processing systems besides CVD equipment. As a result, only mass-flow controller operation is described in this section, and reactor configurations are covered in

later sections of this chapter.

Mass-flow Controllers

CVD reactors and other process systems (e.g. dry-etchers, diffusion furnaces), require that the rates of introduction of process gases into the process chambers be controlled. In some applications, this is achieved by adjusting the gas influx to maintain a constant chamber pressure. More commonly, the process gas flow is directly controlled. In the latter case, an instrument known as a *mass-flow controller* performs this function. Mass flow controllers consist of a mass-flowmeter, a controller, and a valve. They are located between the gas source and the chamber, where they can monitor and dispense the gases at predetermined rates.

Gas flow is measured in units of volume /unit-time, where the volume measurement assumes standard temperature and pressure. A flow of one *standard cubic centimeter per minute* (sccm) is thus defined as a flux of one cm^3 of gas per minute at 273 °K and 760 torr. Since one mole of gas at STP occupies 22.414 liters, one sccm = $(1/22,414)$ moles /min.

The heart of the mass-flow controller is its mass flowmeter, of which there are two types, the *differential pressure type*, and the *thermal type*. The differential type relates a pressure drop at a flow restriction to mass rate of flow. In semiconductor applications, however, the thermal type is more widely used, as a result of its relatively rapid response time (e.g. 2-3 sec), and its low cost. We describe its operation in more detail.

The operation of thermal mass flowmeters relies on the ability of a flowing gas to transfer heat. A schematic of a mass-flow controller is shown in Fig. 3. The mass flowmeter consists of a small sensor tube in parallel with the larger main gas flow tube. A heating coil is wrapped around the sensor tube midway along its length, and temperature sensors (typically resistance thermometers) are located both upstream and downstream of the heated point. When gas is not flowing, and the heat input is constant, the temperatures at both sensors are equal. Flowing gas causes the temperature distribution in the sensor tube to change. The temperature downstream of the heater becomes higher than the temperature upstream since the flowing gas conducts heat away from the heated point. It can be shown that the mass flow, m_f is given by:

$$m_f = (\kappa W_h \Delta T)^{1.25} \quad (1)$$

where W_h is the heater power, ΔT is the temperature difference between the points where the sensors are located ($\cong 1^\circ\text{C}$), and κ is a constant that depends on heat transfer coefficients, the specific heat of the gas, the density of the gas, and the thermal conductivity of the gas. It is assumed that these characteristics remain constant over the flow range measured, and hence mass rate can be obtained by measuring the temperature difference. Each of the resistance thermometers are connected to one arm of an unbalanced Wheatstone bridge, and the temperature difference is converted to a voltage signal. Calibration factors are used so that the voltage output derived from the sensor tube can express the flow (in units of sccm) through the entire flow controller. As the flow rate is determined, its value is compared by the controller to the setpoint value. If necessary, the controller adjusts the valve setting so that the flow returns to the specified value.

During the startup of a process from a condition of zero flow, the feedback and control loop operation is hindered by the slow response of the sensor (i.e. it takes time for the temperature sensors to heat). As a result, the initial gas flow may initially overshoot the setpoint value. Two techniques have been devised to reduce this problem. They are: 1) *setpoint ramping*, by which the setpoint value is slowly ramped up from zero to the final value during startup; and 2) use of *mass flow sensors* with much faster response times. Microscopic mass flow sensors micromachined on silicon substrates have been recently developed for this application³.

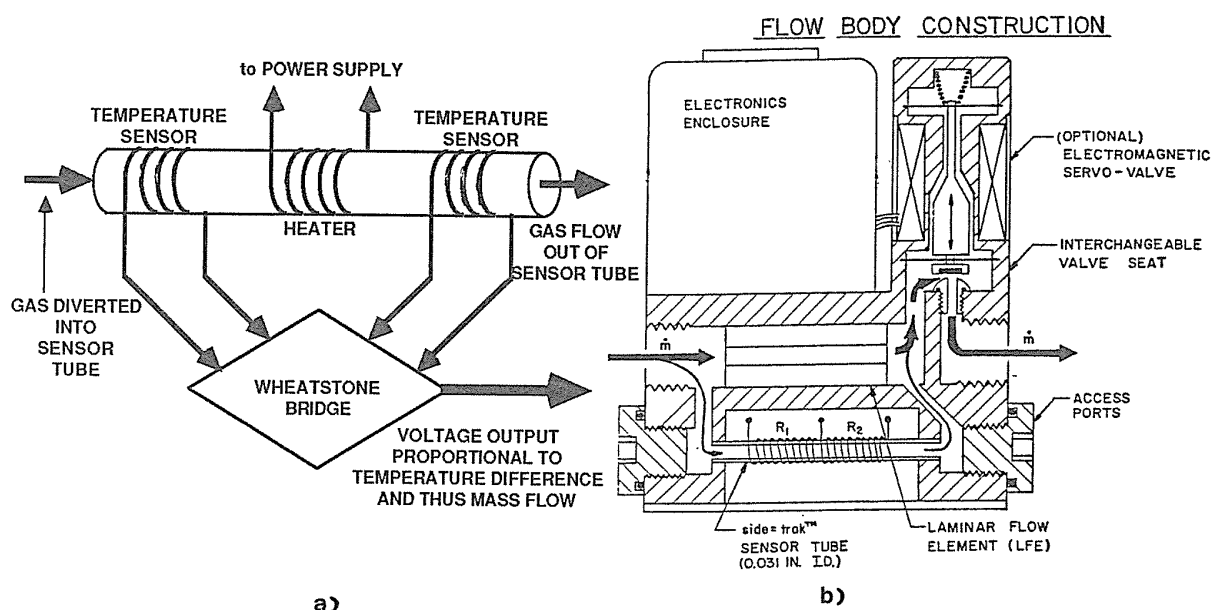


Fig. 3 (a) Operating principle, and (b) cutaway drawing of a mass flow controller. Courtesy of Sierra Instruments.

Due to their extremely small thermal mass, such sensors are capable of responding to heat flux differences (and hence to gas flow rate changes) in times on the order of milliseconds.

Some other requirements of mass flow controllers include: a) that they be immune to stray rf fields (in plasma equipment, for example); b) that they be extremely leak-tight, to prevent leakage of hazardous process gases; c) that they be resistant to damage by corrosive process gases; and d) that they be easy to clean and maintain.

Terminology of CVD Reactor Design

The design and operation of CVD reactors depends on a variety of factors, and hence they can be categorized in several ways. Figure 4 illustrates one way of grouping CVD reactor types. The first distinction between reactor types is whether they are *hot-wall* or *cold-wall* reactors, and this is dependent on the method used to heat the wafers. The next criterion used to distinguish reactor types is their pressure regime of operation (*atmospheric pressure* or *reduced pressure* reactors). Finally, the reduced pressure group is split into: a) low-pressure reactors (the so called *low-pressure CVD*, or *LPCVD* reactors, in which the energy input is entirely thermal); and b) those in which energy is partially supplied by a plasma as well (known as *plasma-enhanced CVD*, or *PECVD* reactors). Each of the reactor types in the two pressure regimes are further divided into sub-groups, defined by reactor configuration and method of heating.

Four methods of heating the wafers and their holder (e.g. a susceptor) have been adopted. They are: a) resistance heating; b) rf induction heating; c) energy from a glow discharge (plasma), and d) photons. Energy may be transferred either to the reactant gases themselves or to the

substrate. When radiant heating from resistance-heated coils surrounding the reaction tube is utilized, not only the wafers but also the reaction chamber walls become hot, and hence such designs are known as *hot-wall* reactors. In these systems, film forming reactions (and as a result, film deposition) occurs on reaction chamber walls as well as on substrates. This implies that such systems will require frequent cleaning.

On the other hand, energy input via infrared lamps mounted within the reactor or rf induction, primarily heats the wafers and susceptor, and does not cause appreciable heating of the reaction chamber walls. Consequently systems heated by these methods are termed *cold-wall* reactors. In some cold-wall systems, however, significant chamber wall heating can still take place, and provisions for cooling the walls must be implemented (e.g. by water cooling) to prevent reactions or depositions from occurring there.

Reactor geometry is constrained by the pressure regime and energy source used, and is an important factor in throughput. Since atmospheric pressure reactors by and large operate in the mass-transport limited regime, they must be designed so that an equal flux of reactants is delivered to each wafer. As a result wafers are never stacked vertically at close spacing, but are rather laid flat on a horizontal surface. An undesirable consequence of this design is the high susceptibility of the wafers to incorporate falling particles. LPCVD reactors are not constrained by the mass-transfer rate limitation, allowing designs that accomodate a large number of wafers per run. That is, wafers can be stacked side by side, only a few mm apart in a quartz reaction tube. Quartz wafer holders (boats) can hold up to 200 wafers. Since LPCVD reactors operate in the surface reaction limited mode, they must, however, be capable of precise temperature control. Table 1 summarizes the characteristics and applications of the various CVD reactor designs.

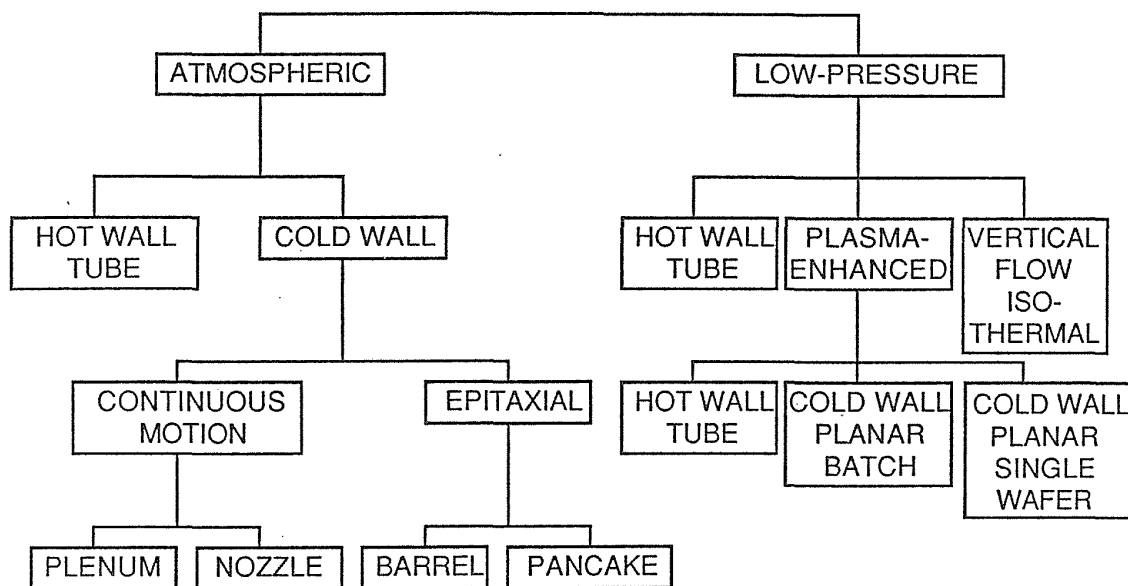


Fig. 4 CVD reactor types.

Table 1. CHARACTERISTICS and APPLICATIONS OF CVD REACTORS

PROCESS	ADVANTAGES	DISADVANTAGES	APPLICATIONS
APCVD (Low Temperature)	Simple Reactor, Fast Deposition, Low Temperature	Poor Step Coverage, Particle Contamination	Low Temperature Oxides, both doped and undoped
LPCVD	Excellent Purity and Uniformity, Conformal Step Coverage, Large Wafer Capacity	High Temperature Low Deposition Rate	High Temperature Oxides, both doped and undoped, Silicon Nitride, Poly-Si, W, WSi_2
PECVD	Low Temperature, Fast Deposition, Good Step Coverage	Chemical (e.g. H_2) and Particulate Contamination	Low Temperature Insulators over Metals, Passivation (Nitride)

Atmospheric Pressure CVD Reactors

Atmospheric pressure CVD reactors (APCVD) were the first to be used by the microelectronics industry^{4,5}. Operation at atmospheric pressures kept reactor design simple and allowed high film-deposition rates. APCVD, however, is susceptible to gas phase reactions, and the films typically exhibit poor step coverage. Since APCVD processes are also generally conducted in the mass-transport limited regime, the reactant flux to all parts of every substrate in the reactor must be precisely controlled. This places constraints on reactor geometry and gas flow patterns. Nevertheless, APCVD processes for deposition of oxides, nitrides and polysilicon were developed, only to be supplanted by superior LPCVD processes (see below). Currently, atmospheric reactors are primarily used for low-temperature oxide (LTO) deposition and epitaxy.

Figure 5 shows schematics of the two types of atmospheric systems. The first is the *horizontal tube type* (Fig. 5a). Such systems consist of a horizontal quartz tube, with the wafers

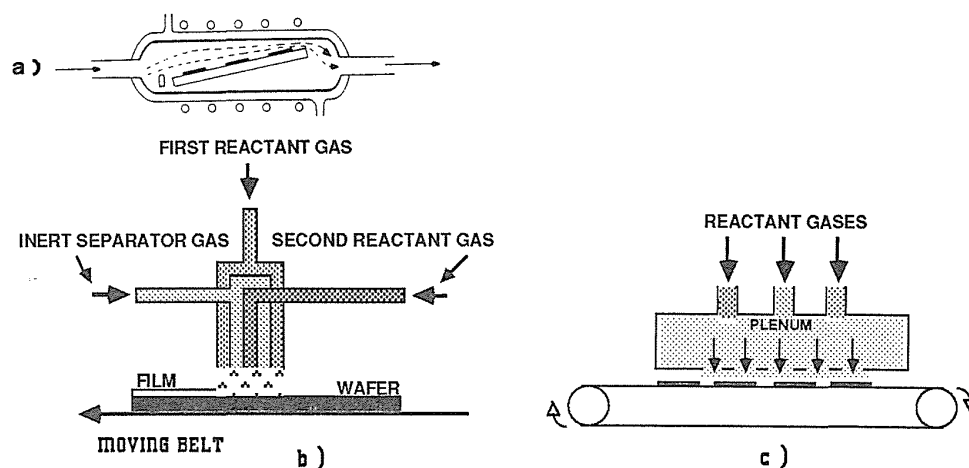


Fig. 5 (a) Horizontal tube APCVD reactor. (b) Gas injector type continuous processing APCVD reactors. (c) Plenum-type continuous processing APCVD reactor.

lying flat on a fixed horizontal plate, while gas flows parallel to the wafer surface. Reactant gases are metered into one end of the tube, and unused or by-product gases exhausted out through the other. Energy is supplied by radiant heating from resistance-heated coils that surround the tube (hot wall). It is possible to deposit polysilicon and SiO_2 in these systems, but as the systems suffer from low throughput, poor uniformity and particulate contamination, they find little use in VLSI fabrication.

The second AP type is the *continuous processing APCVD reactor* (Fig. 5b and c). This configuration is the the most widely used design for depositing low temperature CVD SiO_2 films in production applications. Continuous processing APCVD reactors move the wafers at constant speed through a heated reactor(s), either on a moving plate or continuous conveyor belt. The deposition region is carefully isolated from outside air by curtains of flowing inert gas. Reactant gases may either: a) be mixed in a *plenum* (i.e. from the Latin, full), which is a confined volume filled with flowing process gases at a positive pressure (i.e. slightly greater than atmospheric pressure); or b) be injected from cooled, nitrogen shrouded nozzles, so that mixing occurs only millimeters above the wafer surface (thus reducing gas phase reactions).

Film deposition also takes place on the plate or belt, as well as on the wafers, so frequent cleaning of the system is necessary. At least one commercial system offers an *in situ* HF vapor clean, which allows the continuous belt to be cleaned without disassembly. Modern continuous belt reactors are capable of the thickness uniformity, low contamination, and high throughputs required of VLSI CVD SiO_2 films.

Low-Pressure Chemical Vapor Deposition Reactors

Low pressure chemical vapor deposition (LPCVD) in some cases is able to overcome the uniformity, step coverage, and particulate contamination limitations of early APCVD systems^{6,7,8}. By operating at medium vacuum (30-250 Pa or 0.25-2.0 torr), and higher temperatures (550-600°C), LPCVD reactors typically deposit films in the reaction rate limited regime. As described earlier, at reduced pressure the diffusivity of the reactant gas molecules is sufficiently increased so that mass-transfer to the substrate no longer limits the growth rate. The surface reaction rate is very sensitive to temperature (Eq. 1), but precise temperature control is relatively easy to achieve. The elimination of mass-transfer constraints on reactor design allows the reactor to be optimized for high wafer capacity. Low pressure operation also decreases gas phase reactions, making LPCVD films less subject to particulate contamination. LPCVD is used for depositing many types of films, including poly-Si, Si_3N_4 , SiO_2 , PSG, BPSG, and W.

The two main disadvantages of LPCVD are the relatively low deposition rates, and the relatively high operating temperatures. Attempting to increase deposition rates by increasing the reactant partial pressures, tends to initiate gas phase reactions. Attempting to operate at lower temperatures, results in unacceptably slow film deposition. LPCVD reactors are designed in two primary configurations: a) horizontal tube reactors; and b) vertical flow isothermal reactors.

Horizontal Tube LPCVD Reactors (Hot Wall)

Horizontal tube, hot wall reactors are the most widely used LPCVD reactors in VLSI processing. They are employed for depositing poly-Si, silicon nitride, and undoped and doped SiO_2 films. They find such broad applicability primarily because of their superior economy, throughput, uniformity, and ability to accommodate large diameter (e.g. 150 mm) wafers. Their main disadvantages are susceptibility to particulate contamination¹³ and low deposition rates.

Conventional LPCVD tube reactors are very similar to APCVD tube reactors, in that the wafers are radiantly heated by resistive heating coils surrounding the tube. Reactant gases are

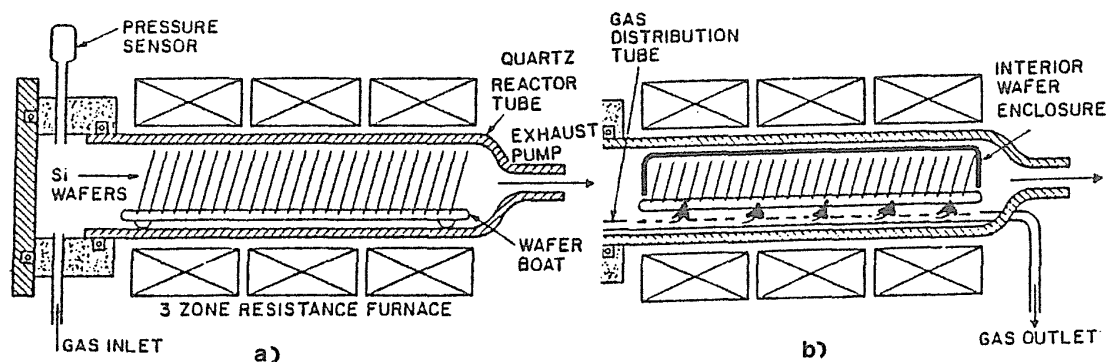


Fig. 6 (a) End feed LPCVD reactor. (b) Distributed-feed LPCVD reactor². Reprinted with permission of Semiconductor International.

also metered into one end of a horizontal quartz tube (using mass flow controllers), and reaction by products are pumped out the other. Vacuum pumps are used to establish the required reduced pressure, typically 0.25-2.0 torr, in the tube. An oil-sealed rotary mechanical pump is generally utilized, often augmented with a Roots pump. A pressure controller⁹, with feedback control of the gas flow or the pump inlet valve may be also be included.

The fact that LPCVD processes operate in a reaction rate limited regime allows wafers to be arranged differently inside the tube than in APCVD tube reactors (since equal mass transport to all parts of every wafer is no longer critical). That is, wafers are positioned vertically (Fig. 6) at very close spacing (e.g. 5-6 mm), perpendicular to the gas flow, in quartz *boats* (in a manner similar to that used in diffusion furnaces, as described in Chap. 7). Up to 200 wafers can be processed per run. The large number of wafers processed in a single process cycle allows greater throughput than with horizontal-tube APCVD reactors, in spite of the relatively low deposition rates of LPCVD processes (100-500 Å/min).

Depletion effects which reduce gas phase concentrations as reactants are consumed by reactions on wafer surfaces, are still operative in such end-fed reactors. That is, wafers near the inlet are exposed to higher concentrations of reactant gases. As a result, deposition rates are greater on wafers placed near the inlet end of the tube. Since the reaction rates increase with increasing temperature, these deposition rate variations can be minimized by linearly increasing temperature along the length of the tube (e.g. by 25-40°C). Such temperature ramping compensates for the reactant gas depletion, and better thickness uniformity is obtained (Fig. 6a). Nonuniform temperatures along the tube length, however, will affect deposition temperature-dependent film properties. This is a particular problem for poly-Si and low-temperature (~400°C) deposition of doped SiO₂. Hence, conventional end-feed LPCVD reactors are used for high temperature deposition (800-850°C) of silicon nitrides and oxynitrides, and for undoped poly-Si films (~600°C), in which the temperature differential does not significantly impact film properties.

Another technique to alleviate the depletion effect, known as *distributed feed*, has been developed for hot-wall tube reactors. In this approach, special injection systems supply fresh reactants at a number of points along the length of the tube (Fig. 6b). Although this requires the use of specially designed quartzware, it allows the temperature along the tube to remain constant. Distributed feed LPCVD hot wall reactors are used for low-temperature (<600°C) deposition of SiO₂, PSG, and BPSG films, and *in situ* doped poly-Si films.

Vertical Flow Isothermal LPCVD Reactors (Cold-Wall)

The vertical flow isothermal LPCVD reactor further extends the distributed gas feed technique, so that each wafer receives an identical supply of fresh reactants¹⁰. Wafers are again stacked side by side, but are placed in perforated-quartz cages. The cages are positioned beneath long, perforated, quartz reaction-gas injector tubes (one tube for each reactant gas). Gas flows vertically from the injector tubes, through the cage perforations, past the wafers (parallel to the wafer surface, Fig. 7) and into exhaust slots below the cage. The size, number, and location of cage perforations are used to control the flow of reactant gases to the wafer surfaces. By properly optimizing cage perforation design, each wafer can be supplied with identical quantities of fresh reactants from the vertically adjacent injector tubes. Thus, this design can avoid the wafer-to-wafer reactant depletion effects of the end-feed tube reactors, requires no temperature ramping, produces highly uniform depositions, and reportedly achieves low particulate contamination.

Plasma Enhanced CVD: Physics, Chemistry, & Reactor Designs

The third and last of the major CVD deposition methods is categorized not only by pressure regime, but also by its method of energy input. Rather than relying solely on thermal energy to initiate and sustain chemical reactions, plasma enhanced CVD (or PECVD) uses an rf-induced glow discharge to transfer energy into the reactant gases, allowing the substrate to remain at a lower temperature than in APCVD or LPCVD processes. Lower substrate temperature is the major advantage of PECVD, and in fact, PECVD provides a method of depositing films on substrates that do not have the thermal stability to accept coating by other methods (the most important being the formation of silicon nitride and SiO_2 over metals). In addition, PECVD can enhance the deposition rate when compared to thermal reactions alone, and produce films of unique compositions and properties. Desirable properties such as good adhesion, low pinhole density, good, step coverage, adequate electrical properties, and compatibility with fine-line pattern transfer processes, have led to application of these films in VLSI.

The plasma (more correctly a *glow discharge*) is generated by the application of an rf field to a low pressure gas, thereby creating free electrons within the discharge region. There is a thorough discussion of glow discharge physics in Chap. 10. The electrons gain sufficient energy from

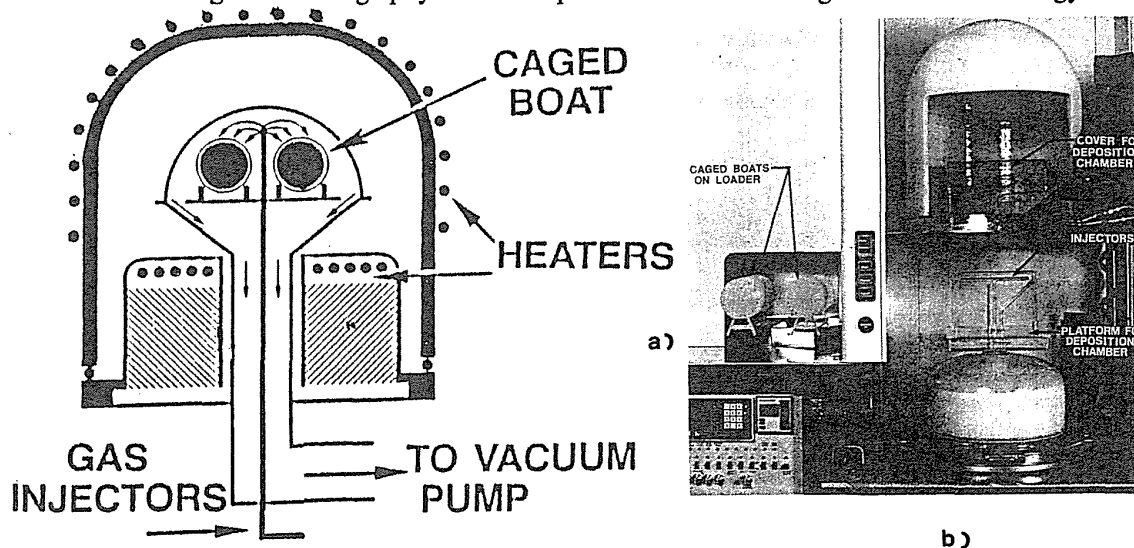


Fig. 7 Vertical isothermal LPCVD reactor. (a) Schematic drawing. (b) Photograph of system. Courtesy of Anicon, Inc.

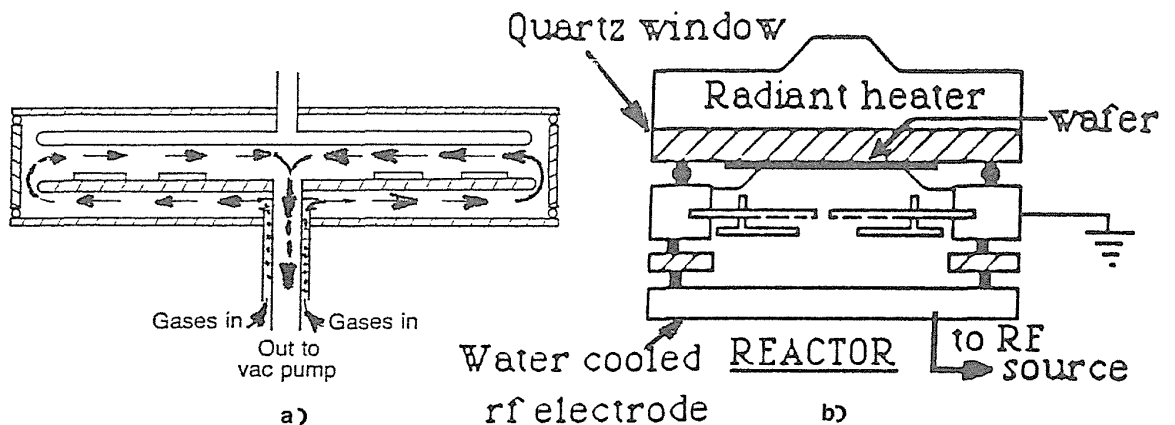


Fig. 8 (a) Radial flow reactor's inward flow (Reinberg design). Reprinted with permission of Semiconductor International¹³ (b) Single wafer PECVD reactor. Courtesy of CVD Spectrum, Inc.

the electric field so that when they collide with gas molecules, gas-phase dissociation and ionization of the reactant gases (e.g. silane and nitrogen or oxygen-containing species) then occurs.

The energetic species (predominantly radicals, as described in Chap. 16) are then adsorbed on the film surface. (Note that the radicals tend to have high sticking coefficients, and also appear to migrate easily along the surface after adsorption. These two factors can lead to excellent film conformality). Upon being adsorbed on the substrate, they are subjected to ion and electron bombardment, rearrangements, reactions with other adsorbed species, new bond formations and film formation and growth. Adatom rearrangement includes the diffusion of the adsorbed atoms onto stable sites and concurrent desorption of reaction products. Desorption rates are dependent on substrate temperature, and higher temperatures produce films with fewer entrapped by-products. Note that gas-phase nucleation should be avoided to reduce particulate contamination.

The fact that the radicals formed in the plasma discharge are highly reactive, presents some options as well as some problems, to the process engineer. PECVD films, in general, are not stoichiometric because the deposition reactions are so varied and complicated. Moreover, by-products and incidental species are incorporated into the resultant films (especially hydrogen, nitrogen, and oxygen), in addition to the desired products. Excessive incorporation of these contaminants may lead to outgassing and concomitant bubbling, cracking, or peeling during later thermal cycling, and to threshold shifts in MOS circuits.

A plasma process requires control and optimization of several deposition parameters besides those of an LPCVD process, including rf power density, frequency, and duty cycle. The deposition process is dependent in a very complex and interdependent way on these parameters, as well as on the usual parameters of gas composition, flow rates, temperature, and pressure. Furthermore, as with LPCVD, the PECVD method is surface reaction limited, and adequate substrate temperature control is thus necessary to ensure film thickness uniformity.

Three types of PECVD reactors are available: 1) the *parallel plate* type; 2) the *horizontal tube* type; and 3) the *single wafer* type. It should be noted that with one major exception, the discussion on glow discharges and rf diode sputtering in Chap. 10, and rf generated plasmas for dry etching in Chap. 16, applies to the production of rf generated plasma in PECVD reactors. Thus it is recommended that readers study these sections for information dealing with the generation of rf plasmas.

The one key difference in designing the reactor and electrode configuration in PECVD systems (compared to those in rf sputtering systems), is that in PECVD systems it is desired that the potential of both the powered and the grounded electrode(s), relative to the plasma, be

approximately equal. Rf tuning networks of PECVD systems therefore usually employ an inductor which shunts the powered electrode to ground to establish this condition. Grounding prevents the powered electrode from developing a larger self-bias, thereby maintaining approximately equal average potentials between the plasma and the powered and grounded electrodes. The walls of parallel plate reactors are made of either quartz, ceramic, or aluminum oxide coated steel, in order to place them at a floating potential with respect to the plasma. This minimizes wall bombardment and sputtering, which reduces contamination of the growing films. (Note that the quartz tube of tube PECVD reactors is an insulator, and thus does not require such coating).

Parallel Plate PECVD Reactors

The radial parallel plate reactor was developed by Reinberg⁵² in the early 1970's, and the first commercial model was offered in 1976. A schematic of this reactor type is shown in Fig. 8a. The reaction chamber is a short, vertically oriented cylinder, typically constructed of stainless steel. The rf power (at frequencies of 450 kHz-13.5 MHz) which establishes the plasma is applied to the upper electrode, and the wafers reside on the bottom grounded electrode, which can be rotated for improved uniformity, and be heated up to 400°C. The electrode spacing is typically 5 to 10 cm, and such systems operate in the pressure range of 0.1-5 torr. The reactants are introduced either through the center and removed from the periphery (Reinberg design), or from the periphery and removed from the center. Despite depletion effects, uniform deposition can be achieved by correctly balancing the plasma density and gas flows. Parallel plate systems, however, suffer from low throughput for large diameter wafers. In addition, particulates flaking off walls or the upper electrode, can fall onto the horizontally positioned wafers.

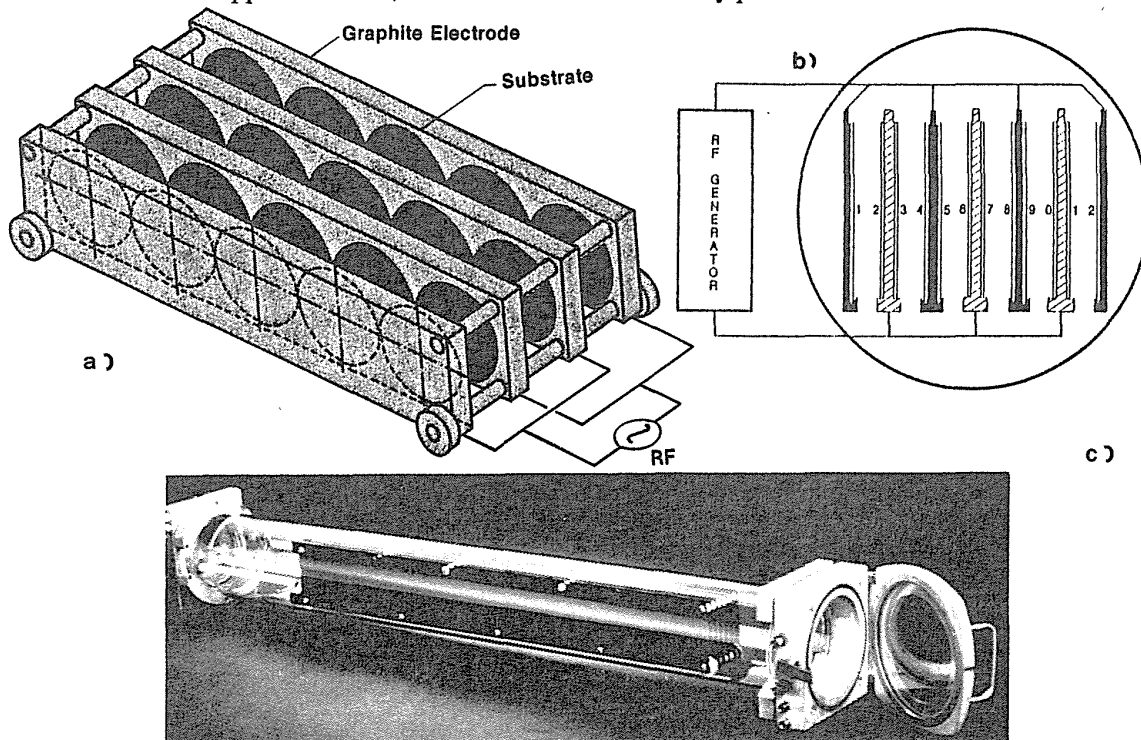


Fig. 9 (a) Long, multiple plate reactor generates plasma between the wafers facing each other on graphite electrodes¹⁴. (b) Cross section of electrode assembly and wafers shown in (a). Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet. (c) Photograph of tubular PECVD reactor. Courtesy of Pacific Western Systems.

Horizontal Tube PECVD Reactors

In 1979 a new PECVD reactor design, the *horizontal tube* reactor, was introduced. This design allows PECVD reactor throughputs to be greatly increased. The reactor resembles a "hot wall" LPCVD system. It consists of a long horizontal quartz tube that is radiantly heated. Gas is fed into one end, and flows linearly to the other. Special long rectangular graphite plates (Fig. 9) serve both as the electrodes that are needed to establish a plasma, and as holders of the wafers (the electrode configuration is also designed to provide a uniform plasma environment for each wafer, to ensure uniformity of deposition). These vertically-oriented graphite electrodes are stacked parallel to one another, side-by-side, with alternating plates serving as power and ground for the rf voltage. A plasma is formed in the space between each pair of plates.

The use of several long slabs allows an increased number of wafers (up to 120 100mm wafers) to be loaded into the reactor at one time. Most systems consist of two stacked deposition tubes. In addition, since the wafers are held vertically, most particulates do not fall on the wafer surfaces. The entire graphite assembly is withdrawn from the reactor for wafer loading, and then reinserted for processing. Care must be exercised, however, to prevent particulate contamination when loading and unloading wafers from these systems.

Tubular PECVD reactors, like horizontal tube LPCVD reactors, suffer from a depletion effect, but resultant deposition nonuniformities can be minimized by temperature ramping. Another technique used to combat depletion effect nonuniformities is to pulse the plasma, so that during the off phase of the duty cycle, fresh reactant gases fill the tube and replace depleted gases.

Single Wafer PECVD Reactors

The most recently introduced PECVD reactor is the single-wafer design (Fig. 8b). The reactor is load locked, offers cassette-to-cassette operation, provides rapid radiant heating of each wafer, and allows *in situ* monitoring of the film deposition. Wafers ≥ 200 mm can be accommodated. Little direct information on the operational characteristics of such reactors was available at the time of publication, but such reactors are clearly being designed to allow fabrication of large wafers in low-particulate, automated environments.

Photon-Induced Chemical Vapor Deposition

A final CVD method, which may fill the need for an extremely low temperature deposition process without the film composition problems of PECVD, is PHoton-induced Chemical Vapor Deposition (PHCVD). PHCVD uses high-energy, high-intensity photons to either heat the substrate surface, or to dissociate and excite reactant species in the gas phase. In the case of substrate surface heating, the reactant gases are transparent to the photons, and the potential for gas phase reactions is completely eliminated. In the case of reactant gas excitation, the energy of the photons can be chosen for efficient transfer of energy to either the reactant molecules themselves, or to a catalytic intermediary, such as mercury vapor. This technique enables deposition at extremely low (i.e. room) substrate temperatures. PHCVD films show good step coverage, but may suffer from low density and molecular contamination as a result of the low deposition temperature.

There are two classes of PHCVD reactors, depending on energy source: a) UV lamp; and b) laser. *UV lamp reactors*¹⁵ generally use mercury vapor for energy transfer between photons and the reactant gases. UV radiation at 2537Å is efficiently absorbed by mercury atoms, which then transfer energy to the reactant species. Deposition rates for UV PHCVD reactors are typically much slower than in other low temperature techniques. *Laser PHCVD reactors*¹⁶ offer the advantages of *frequency tunability* and a high intensity light source. Tunability is useful in that

specific photon energies targeted for particular dissociation reactions can be dialed in, enabling greater control of the deposition reaction. The energy from the high intensity laser also increases reaction rates. Laser PHCVD opens the possibility of CVD *writing* (i.e. patterned deposition by spatial control of the laser). Nevertheless, the deposition rates of current PHCVD processes are still too low to allow them to be adopted for production microelectronic applications.

POLYCRYSTALLINE SILICON: PROPERTIES AND CVD DEPOSITION METHODS

Polycrystalline silicon (also called *polysilicon*, *poly-Si* or *poly*) in thin film form has many important applications in integrated circuit technology. Heavily doped poly-Si films have been widely used as gate electrodes and interconnections in MOS circuits. Poly-Si is utilized in these roles because of its compatibility with subsequent high temperature processing, its excellent interface with thermal SiO₂ (low concentration of interface states), its higher reliability than Al gate materials⁵¹, and its ability to be deposited conformally over steep topography. In some such applications more than one layer of poly-Si is utilized, and a layer of SiO₂ must be thermally grown or deposited on the first layer to electrically isolate it from subsequent layers. More recently, VLSI MOS devices have been fabricated with high conductivity films deposited onto the poly-Si, to create interconnect structures with lower sheet resistances than are possible with poly-Si alone (see Chap. 11 for more information on this subject). Heavily doped poly-Si films are also utilized to form emitter structures in advanced bipolar technologies. Selective growth of poly-Si is being studied as a planarization technique for filling contact holes¹⁷. Lightly doped poly-Si films are used as high-value load resistors in static memories, and to refill trenches employed in dielectric isolation technologies. In this section the properties of poly-Si films and CVD methods for preparing such films are presented.

Properties of Polysilicon Thin Films

Physical Structure and Mechanical Properties of Poly-Si

Thin films of polycrystalline silicon are made up of small (on the order of 1000Å) single crystal regions (*crystallites* or *grains*) separated by grain boundaries. It is of interest to note that *as-deposited* poly-Si films can be amorphous or polycrystalline, but subsequently exhibit a polycrystalline structure if subjected to elevated temperatures after deposition. Polycrystalline silicon films exhibit many mechanical material properties close to those of bulk single-crystal Si (e.g. the density of poly-Si is 2.3 g/cm³, the coefficient of thermal expansion is 2x10⁻⁶/°C, and the temperature coefficient of resistance is 1x10⁻³/°C). The intrinsic stress in thin polysilicon films is compressive (e.g. the stress in 2000-5000Å films is 1-5x10⁹ dynes/cm² *compressive* over the range of doping from undoped material to 10²⁰ atoms/cm³, and annealing temperatures from 250–1100°C)¹⁸. The effect of deposition conditions and post-deposition annealing on poly-Si film structure is discussed in more detail in a later section.

The grain boundaries are composed of disordered atoms, and contain large numbers of defects due to incomplete bonding; while inside each grain, atoms are arranged in a periodic structure. The silicon material in the interior (bulk) of the grains consequently behaves similarly to that of bulk single crystal silicon (e.g. diffusion constants and substitutional impurity properties are assumed to be roughly identical). The defects and departure from periodicity at the grain boundaries, however, substantially alter the behavior of two important material properties of polysilicon, its diffusion characteristics, and its dopant distribution. That is, diffusion

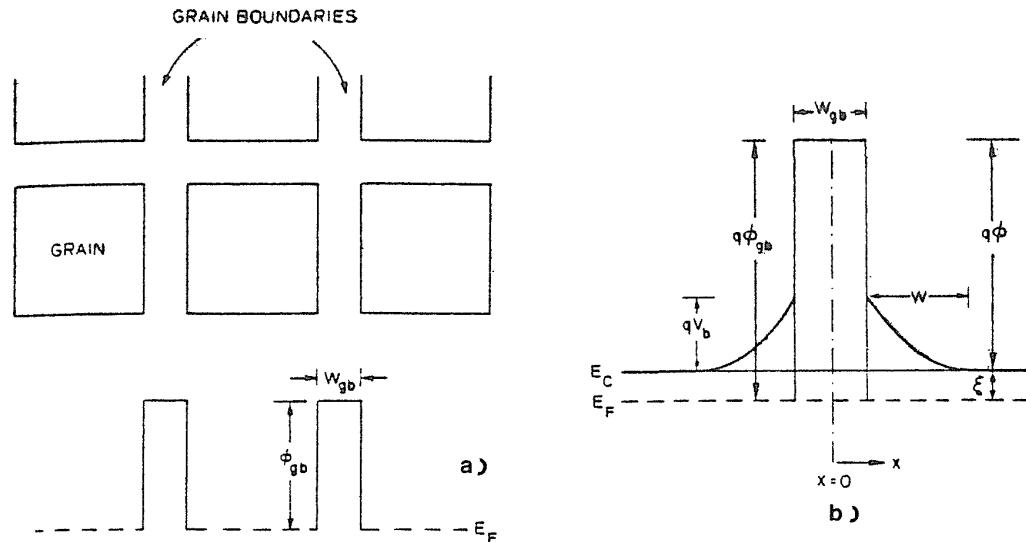


Fig. 10 (a) Schematic representation of potential barriers generated by the grain boundaries. (b) Energy band diagram near a grain boundary under zero applied voltage¹⁹. (© 1981, IEEE).

constants in grain boundary regions are significantly higher than those in single crystal regions. As a result, dopants are capable of diffusing much more rapidly along grain boundaries than through crystallites. Likewise, dopant redistribution is also impacted, as some dopants (e.g. As and P, but not B) exhibit segregation coefficients which favor their moving from single crystal regions into grain boundary regions at low temperatures, and back again at high temperatures¹⁹. See Chap. 4 for an introduction to thin film properties, and Chap. 8 for diffusion in poly-Si.

Electrical Properties of Polysilicon

The electrical properties of poly-Si films are functions of both their semiconductor nature and their polycrystalline structure and doping. That is, single crystal regions of poly-Si are assumed to behave electrically in a manner similar to bulk single crystal silicon. As in single crystal silicon, low resistivity is obtained through heavy doping with impurity atoms.

At a given dopant concentration, polysilicon exhibits significantly higher resistivity than single crystal silicon (except at very high dopant concentrations, where the resistivity is only slightly greater). This is primarily due to two mechanisms: 1) under heat treatment some of the dopant atoms (e.g. As and P, but not B) segregate to the grain boundaries, where they do not effectively produce free carriers. Thus, the concentration of dopant atoms remaining in single crystal regions, and thus still able to contribute charge carriers, is decreased; and 2) the grain boundaries are rich with incomplete bonds, which traps some free carriers at the grain boundaries. Not only does such trapping decrease the overall free carrier concentration, but the trapped charge in the grain boundaries causes local regions of neighboring single crystal material to become depleted of carriers (and creates local potential variations in the material). These changes in potential at grain boundaries (Fig. 10) are detrimental to carrier movement, and also lead to an increase in apparent resistivity. The grain boundary region itself, approximately 5-10 angstroms wide, can be modeled as a separate, amorphous silicon region with increased bandgap. This larger bandgap represents another potential barrier for charge carriers to overcome, although it is so narrow that quantum tunneling effects prevail. Finally, the defects in the grain boundaries decrease the carrier mobility, also causing the resistivity to increase.

Based on the above model for resistivity degradation effects, the behavior of poly-Si

resistivity as a function of dopant concentration and grain size, can be qualitatively understood. First, films with larger grain sizes (at the same dopant concentration) exhibit lower resistivity. That is, since surface area does not increase with grain size as quickly as volume, films with larger grains have proportionally smaller grain boundary densities, and thus less deviation from bulk-silicon resistivity values is observed. Second, grain size and dopant concentration effects interact to determine the degree to which each crystallite is depleted of free charge. Very small grains will become fully depleted more easily than larger grains, and high dopant concentrations result in narrower depleted regions, thus making full depletion of the grains more difficult. If the grains do become completely depleted, the resistivity increases dramatically. As a result, there is a sharp transition region between *very high resistivity*, where grain size is small and/or doping is low and the grains are completely depleted, and *lower resistivity*, where grain size is large and/or doping is high.

In practice, sheet resistances as low as 10-30 Ω /square may be obtained by several techniques (see below) in poly-Si films used in integrated circuits. Note that the work function of poly-Si, important in MOS device threshold voltage values, is also impacted by the dopng level.

Chemical Vapor Deposition of Polysilicon

Poly-Si is generally deposited by the pyrolysis (i.e. thermal decomposition) of silane (SiH_4) in the temperature range 580-650°C. The main technique used to deposit poly-Si is LPCVD because of its uniformity, purity, and economy^{20,21}. The deposition reaction sequence is:

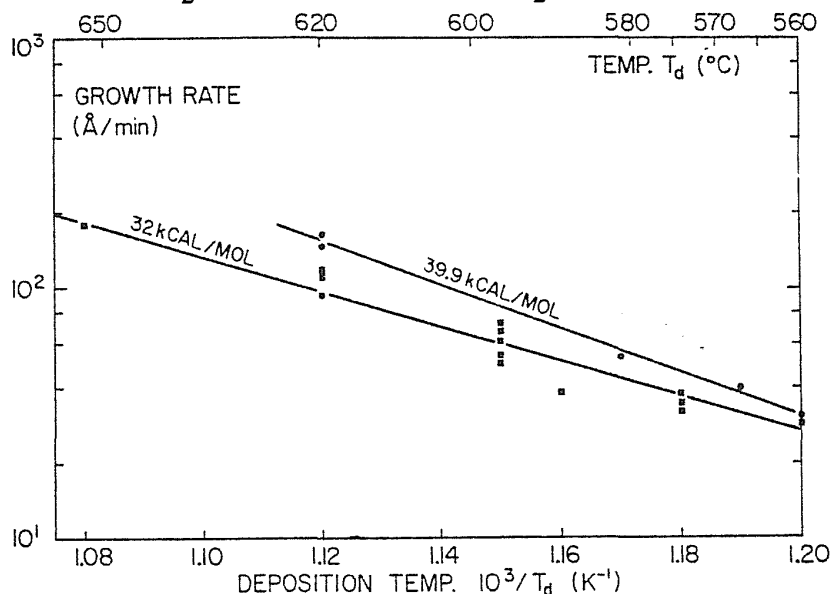
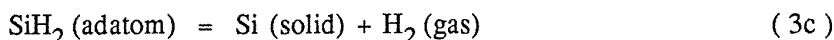
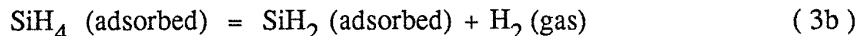
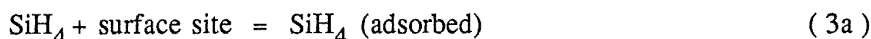
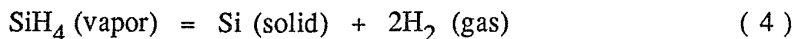


Fig. 11 Growth rate as a function of deposition temperature T_d for two different deposition conditions²⁰. (● 350 mtorr, $\text{SiH}_4 = 200 \text{ cm}^3/\text{min}$ and ■ 120 mtorr, $\text{SiH}_4 = 50 \text{ cm}^3/\text{min}$). Reprinted by permission of the publisher, the Electrochemical Society, Inc.

where adsorption of the SiH_4 is followed by decomposition to an intermediate compound, SiH_2 . Then, upon evolution of the remaining hydrogen, the solid film forms. The overall reaction is generally given as:



Three processes are commonly used in conventional LPCVD systems. The first uses 100% SiH_4 at total pressures from 0.3-1 torr, while the second uses approximately 25% SiH_4 in a nitrogen carrier at approximately the same pressures. A third technique, performed in vertical flow isothermal reactor configurations, uses 25% SiH_4 diluted in hydrogen, also at ~ 1 torr.

Deposition Parameters

The deposition rate shows an exponential dependence on temperature. Figure 11 is a plot of deposition rate vs. reciprocal temperature. Apparent activation energies are found to depend on the silane pressure and range from 1.36 to 1.7 eV. Depositions are limited to the 580-650°C range, since at higher temperatures gas phase reactions occur (leading to rough and loosely adhering films), and below 580°C the rate is too slow for practical use ($< 50 \text{ \AA}/\text{min}$).

The polysilicon deposition rate depends on the silane (SiH_4) pressure as shown in Fig. 12. The dependence is not linear except for low values of pressure. Such behavior may be due to homogeneous reactions, adsorption of hydrogen on the surface sites, or transport phenomena. The total pressure in the reactor can be varied by: a) changing the flow rate of silane at constant pump speed; b) changing the pump speed at constant flow rate; and c) in processes which use diluted silane, by changing the nitrogen flow to adjust the silane concentration. It appears that changing pumping speed to control total pressure provides the best control of deposition rates.

In conventional LPCVD systems it is necessary to ramp the temperature by as much as 30°C from the gas inlet tube end to the outlet. This is done to overcome the effects of the depletion of SiH_4 , and the attendant decrease in deposition rate down the length of the tube. The increased deposition rate resulting from increased temperatures is intended to just compensate for the decrease due to silane depletion. A difficulty with this process is that poly-Si properties depend very strongly on deposition temperature, and will thus vary with wafer position along the tube. A newly designed vertical flow reactor (see section on LPCVD) circumvents this problem.

Polysilicon can be doped during deposition (*in-situ*), or after deposition by diffusion or ion implantation. The addition of diborane to the silane during deposition (boron doping) causes

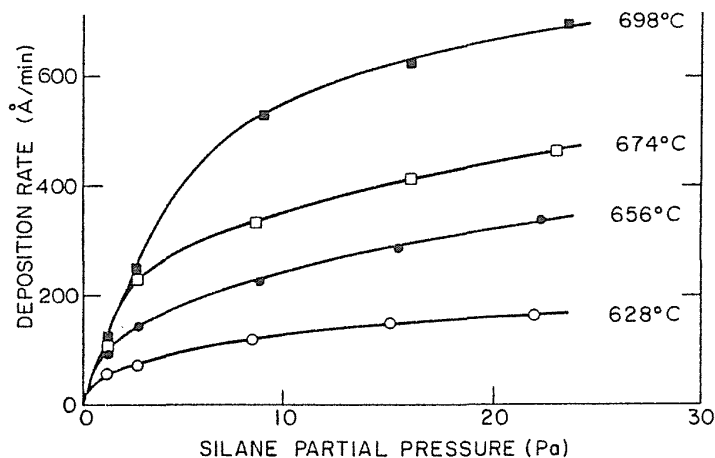


Fig. 12 The effect of silane concentration on the polysilicon deposition rate¹. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted with permission.

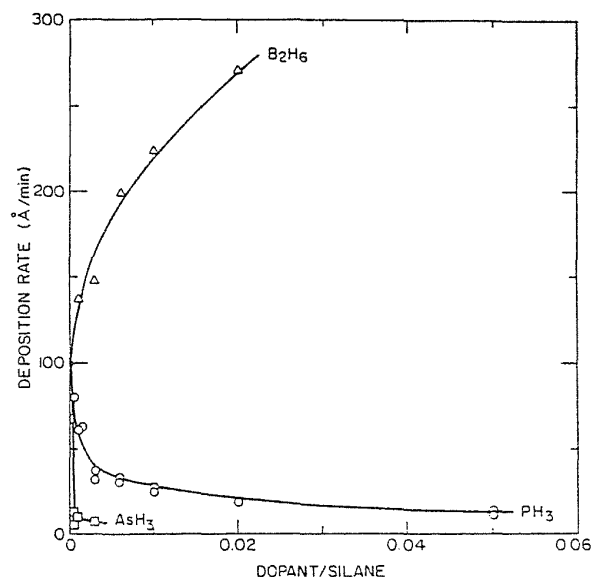


Fig. 13 The effect of dopants on the polysilicon deposition rate at 610°C ¹. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted with permission.

rapid increases in the deposition rates, while addition of phosphine or arsine to the silane results in significant growth rate reductions. Figure 13 shows a plot of the deposition rate of polysilicon at 610°C as a function of the volume fraction of dopant added to the silane. *In-situ* doping of polysilicon has not been popular even though it is considerably less complex than post-deposition doping, because of the difficulty of maintaining thickness and doping uniformity from wafer to wafer and across the wafer. Meyerson and Olbricht have shown that the factor of 20 reduction in deposition rate, which is observed when a PH_3/SiH_4 ratio of 1:40 is used, can be attributed to the adsorption of a phosphine layer on the substrate²². This inhibits subsequent silane adsorption and heterogeneous silane decomposition.

Structure of Polysilicon: Deposition Condition Dependence

The structure and properties of poly-Si depend very much on the deposition temperature, the dopant type and concentration, and subsequent thermal cycling. At temperatures below 580°C , the as-deposited film is essentially amorphous²³. At temperatures above 580°C , the films deposit as polycrystalline, with preferred orientation. The $\{110\}$ fiber axis with columnar grains is dominant in the 625°C range while the $\{100\}$ predominates in the 675°C range. The $\{110\}$ -preferred orientation also dominates at higher temperatures²⁴. Harbeke, *et al* found a $\{311\}$ -preferred orientation for films deposited between 580 - 600°C ²⁰. Films that are recrystallized at 900 - 1000°C from the amorphous state tend towards a strong $\{111\}$ fiber texture (Fig. 14). It was also observed that the texture and grain size are exceptionally reproducible in films crystallized from the amorphous phase, and the average grain size is somewhat larger than in the as-deposited polycrystalline film. Figure 15 shows the average grain size of as deposited and recrystallized films (undoped and P-doped). In addition, it was found that as-deposited amorphous films tend to have a smoother surface than do films grown at 600°C (which occasionally show rough surfaces), and films grown at 620°C (which always show surface roughness). The smooth surfaces of the as-deposited amorphous films are maintained even after annealing at 900 - 1000°C . The penalty paid for achieving smoother surfaces is slower deposition rates at 580°C (~ 50 Å/min versus 100 Å/min at 600°C). The average grain size

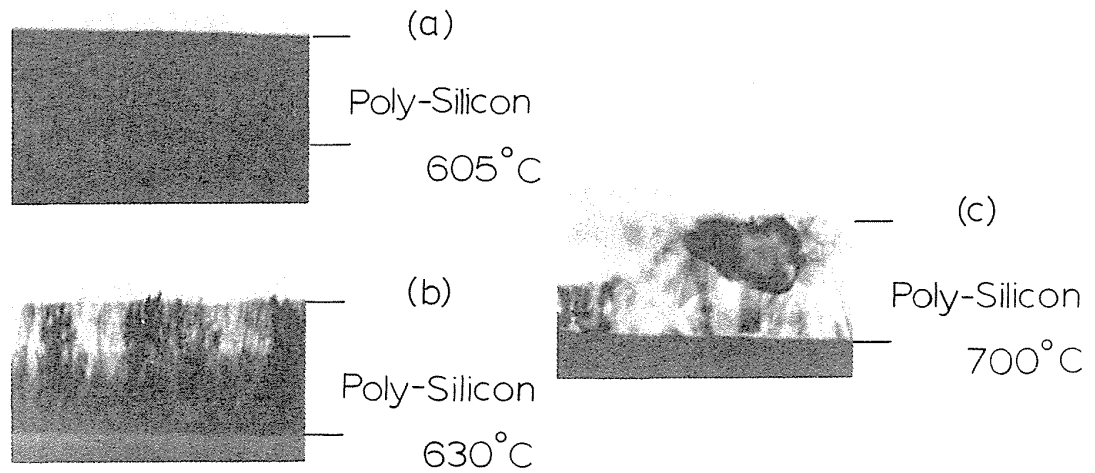


Fig. 14 TEM cross sections (60,000X) of polysilicon. (a) Amorphous structure deposited at 605°C. (b) Columnar structure deposited at 630°C. (c) Crystalline grains formed by annealing an amorphous sample at 700°C¹. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted with permission.

has been observed to increase with film thickness²⁶, and it was also found that the resistivity in boron doped films increases exponentially as thickness decreases.

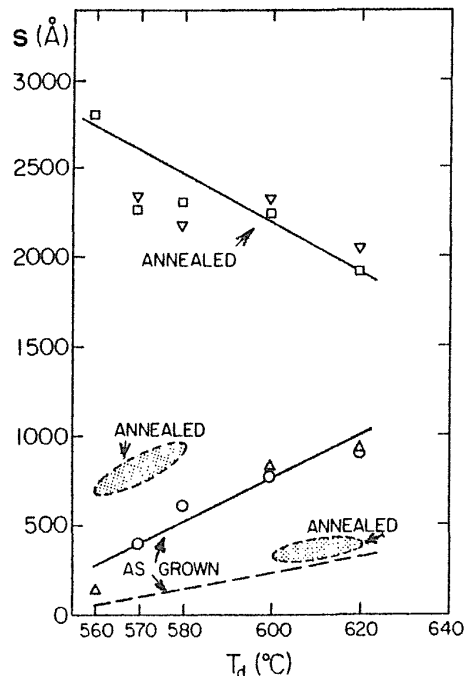


Fig. 15 Average crystallite size S for phosphorus-doped LPCVD silicon layers as-grown (o = interface, Δ = surface), and annealed at 1000°C ($\diamond$ = interface, ∇ = surface) as a function of deposition temperature, T_d . Undoped layers (dashed lines) are shown for comparison. From G. Harbeke, *et al.*, RCA Review, 44, 287 (June, 1983).

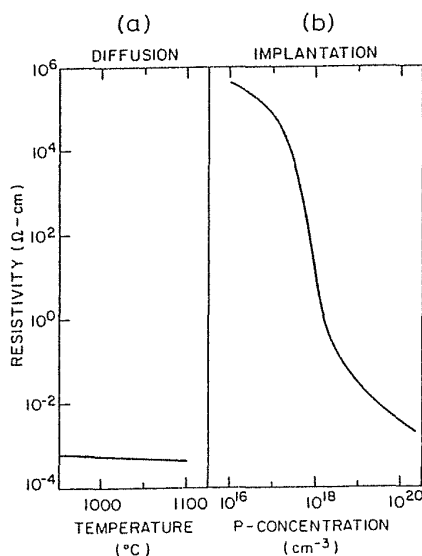


Fig. 16 Resistivity of P-doped polysilicon. (a) Diffusion, 1 h at the indicated temperature²⁵. Reprinted by permission of the publisher, the Electrochemical Society, Inc. (b) Implantation, 1 h anneal at 1100°C¹⁹. (© 1981, IEEE).

Doping Techniques for Polysilicon

Three techniques are used to dope polysilicon: 1) diffusion; 2) ion implantation; and 3) *in situ* doping. In most applications, poly-Si is deposited undoped, and is subsequently doped by diffusion or implantation.

Diffusion Doping of Polysilicon

Diffusion doping (see Chap. 8) is a relatively high-temperature process (900-1000°C) wherein a highly doped glass is grown or deposited on undoped polysilicon, and serves as a solid source for dopant diffusion. The advantage of this method is its ability to introduce very high concentrations of dopants into the poly-Si film (above solid-solubility limits, because of grain-boundary segregation effects), resulting in low resistivity. A high temperature diffusion doping step can also serve double duty as the polysilicon anneal step. Lower final resistivities have been reported for diffusion doping of as-deposited amorphous (low deposition temperature) poly-Si compared to as-deposited polycrystalline poly-Si (Fig. 16a). The disadvantages of diffusion doping are its high temperature and the possibility of increasing film surface roughness.

Ion Implantation Doping of Polysilicon

The second doping technique is ion implantation and subsequent anneal. See Chap. 9 for more on Ion Implantation. This method has the advantage of precise control of dopant dose, and is well suited for applications that do not require a maximally doped polysilicon film (e.g. high value load resistors used in static memories, or doping studies). The resistivity of heavily doped implanted poly-Si is about ten times higher than that of diffusion doped poly-Si (Fig. 16b). The implantation energy is generally selected so that the impurity peak is produced at the center of the film. A subsequent anneal step (e.g. ~900°C, 30 min) redistributes and activates the implanted dopant. Rapid thermal processing (see Chaps. 2 and 9) is also being investigated as an annealing and activating technique²⁸. With the increased diffusion rates of dopants along grain

boundaries, dopant redistribution and activation of implanted polysilicon can be achieved by RTP in less than 30 seconds at 1150°C. The advantage of using RTP is its short duration, which avoids redistributing dopants in the single crystal silicon substrate. Note that ion implantation of poly-Si with As, followed by a rapid-thermal processing step, has also been investigated as a method for forming shallow emitters in advanced bipolar technologies.

***In Situ* Doping of Polysilicon**

In situ doping involves adding doping gases such as diborane and phosphine to the CVD reactant gases⁵⁰. Although combining doping and deposition in one step may appear simple, the control of film thickness, dopant uniformity, and deposition rate is greatly complicated by the addition of the dopant gases. Moreover, the physical properties of the film are affected. Adding phosphine can change the temperature dependence of the polycrystalline film structure, grain size, and grain orientation. In undoped films, it is reported that depositing an initially amorphous film results in superior structural perfection after anneal²¹. Note that for *in-situ* arsenic or phosphorus doped poly-Si, an oxide capping layer must either be deposited or thermally grown before or during the anneal cycle, in order to avoid outdiffusion of the dopant through the top surface of the polysilicon during the anneal. If the deposition temperature is high enough (>600°C) to result in an as-deposited polycrystalline film with sufficiently low resistivity, then the high temperature anneal step may be skipped altogether.

Oxidation of Polysilicon

Polysilicon, like single crystal silicon, can be thermally oxidized. Its oxidation rate depends on grain orientation, dopant type, and dopant concentration. In general, lightly doped poly-Si oxidizes more rapidly in wet O₂ than {111} or {100} single crystal silicon²⁹. Polysilicon heavily-doped with phosphorus oxidizes more rapidly than undoped poly-Si, but not as rapidly as heavily-doped single crystal Si²⁸. The ratio of poly-Si consumed during oxidation, to the thickness of the oxide, is about the same as in single-crystal Si (1:1.56).

Of particular importance in some applications (especially in which a double-poly, or even triple-poly structure is used) is that SiO₂ thermally grown on the poly-Si exhibits adequate breakdown strength. This strength is strongly influenced by the smoothness of the polysilicon surface prior to oxidation. That is, a rough surface leads to high local electric fields and lower oxide dielectric strength. Again, low temperature poly-Si depositions (<600°C) have been reported to produce smoother surfaces and grown oxides with higher breakdown voltages than obtained under higher temperature depositions. Another technique reported to increase the smoothness of the poly-Si /SiO₂ interface is to grow the oxide at higher temperatures. It is believed that the viscous flow of the oxide can moderate the surface roughness produced by oxidation. A method for reducing leakage and increasing the breakdown strength of oxides grown on phosphorus-doped poly-Si is to dope it to an optimum level ($\sim 6 \times 10^{20} \text{ cm}^{-3}$), with a high temperature anneal in an inert ambient ($\sim 1100^\circ\text{C}$, 10 min, N₂) prior to a 950°C oxidation³⁰. This is thought to improve interface flatness by phosphorus-enhanced grain growth during the anneal.

PROPERTIES AND DEPOSITION OF CVD SiO₂

Chemical vapor deposited (CVD) SiO₂ films, and their binary and ternary silicates, find wide use in VLSI processing. These materials are used as insulation between polysilicon and metal layers, between metal layers in multilevel metal systems, as getters, as diffusion sources, as diffusion and implantation masks, as capping layers to prevent outdiffusion, and as final

Table 2. PROPERTIES OF CVD AND THERMAL SILICON DIOXIDE¹

FILM TYPE:	THERMAL	PECVD	APCVD	SiCl ₂ H ₂ +N ₂ O	TEOS
Deposition Temp. (°C):	800-1200	200	450	900	700
Step Coverage:	conformal	good	poor	conformal	conformal
Stress (x10 ⁹ dynes/cm ²):	3C	3C-3T	3T	3T	1C
Dielectric Strength (10 ⁶ V/cm):	3 - 6	8	10	10	
Etch Rate (Å /min): (100:1, H ₂ O:HF)		400	60	30	30

passivation layers. In general, the deposited oxide films must exhibit uniform thickness and composition, low particulate and chemical contamination, good adhesion to the substrate, low stress to prevent cracking, good integrity for high dielectric breakdown, conformal step coverage for multilayer systems, low pinhole density, and high throughput for manufacturing.

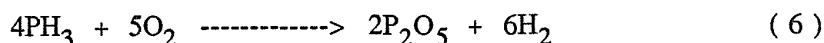
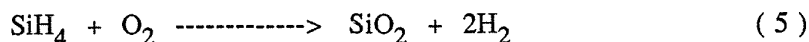
CVD silicon dioxide is an amorphous structure of SiO₄ tetrahedra with an empirical formula SiO₂. (See Chap. 7, section on *Properties of Silica Glass*.) Depending on the deposition conditions, as summarized in Table 2, CVD silicon dioxide may have lower density and slightly different stoichiometry from thermal silicon dioxide, causing changes in mechanical and electrical film properties (such as index of refraction, etch rate, stress, dielectric constant and high electric-field breakdown strength). Deposition at high temperatures, or use of a separate high temperature post-deposition anneal step (referred to as *densification*) can make the properties of CVD films approach those of thermal oxide.

Deviation of the CVD silicon dioxide film's refractive index, *n*, from that of the thermal SiO₂ value of 1.46 is an often used as an indicator of film quality. A value of *n* greater than 1.46 indicates a silicon rich film, while smaller values indicate a low density, porous film. CVD SiO₂ is deposited with or without dopants, and each type has unique properties and applications.

Chemical Reactions for CVD SiO₂ Formation

There are various reactions that can be used to prepare CVD SiO₂. The choice of reaction is dependent on the temperature requirements of the system, as well as the equipment available for the process. The deposition variables that are important for CVD SiO₂ include: temperature, pressure, reactant concentrations and their ratios, presence of dopant gases, system configuration, total gas flow, and wafer spacing. There are three temperature ranges in which SiO₂ is formed by CVD, each with its own chemical reactions and reactor configurations. These are: 1) low temperature deposition (300-450°C); 2) medium temperature deposition (650-750°C); and 3) high temperature deposition (~900°C).

The *low temperature deposition* of SiO₂ utilizes a reaction of silane and oxygen to form undoped SiO₂ films. The depositions are carried out in APCVD reactors (primarily of the continuous belt type), in distributed feed LPCVD reactors, or in PECVD reactors. The depletion effect precludes the use of conventional LPCVD for the SiH₄ + O₂ reaction. The addition of PH₃ to the gas flow forms P₂O₅, which is incorporated into the SiO₂ film to produce a phosphosilicate glass (PSG)³¹. The reactions are given by:

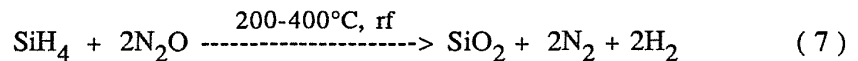


The reaction between silane and excess oxygen forms SiO_2 by heterogeneous surface reaction. Homogeneous gas-phase nucleation also occurs, leading to small SiO_2 particles that form a white powder on the reaction chamber walls (and which may potentially cause particulate contamination in the deposited films).

The deposition rate increases slowly with increased temperature between 310 and 450°C. An apparent activation energy of less than 0.4 eV has been measured which is indicative of a surface adsorption or gas phase diffusion deposition process. The deposition rate can be increased at constant temperature (up to a limit) by increasing the O_2 : SiH_4 ratio. Continued increase in the ratio eventually results in a decrease in deposition rate, as a result of O_2 being adsorbed on the substrate, thus inhibiting the SiH_4 decomposition.

Silicon dioxide films deposited at low temperatures exhibit lower densities than thermal SiO_2 , and have an index of refraction of ~ 1.44 . They also exhibit substantially higher etch rates in buffered hydrofluoric acid (HF) solutions than thermal SiO_2 . Subsequent heating of such films to temperatures between 700-1000°C causes *densification*. That is, this step causes the density of the material to increase from 2.1 g/cm³ to 2.2 g/cm³, the film thickness to decrease, and the etch rate in HF to decrease.

SiO_2 can also be deposited by a plasma enhanced reaction between SiH_4 and N_2O (nitrous oxide) or O_2 at temperatures between 200-400°C³²:

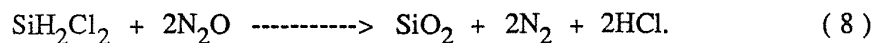


Nitrogen and/or hydrogen is often incorporated in PECVD SiO_2 . A low ratio of N_2O / SiH_4 will increase the index of refraction, due to large amounts of nitrogen incorporated in the film and the formation of silicon rich films. Nearly stoichiometric ($n = 1.46$) plasma oxide films can be achieved by reacting SiH_4 and O_2 mixtures. The buffered HF etch rate is a sensitive measure of the film's stoichiometry and density. Lower deposition temperatures and higher N_2O / SiH_4 ratios lead to less dense films and faster etch rates. As with nitride films, PECVD oxides also contain 2-10 at% H_2 in the form of Si-H, Si-O-H, and H-O-H³². The hydrogen concentration is a strong function of the deposition parameters. Low deposition temperatures, high rf power, and high carrier-gas flow rates are required to prevent gas phase nucleation and its attendant particulate problems.

Plasma oxide films are generally deposited in compressive stress, with values ranging between 1×10^8 - 4×10^9 dynes/cm², depending on deposition temperature and rate. Dielectric strengths of 4 - 8×10^6 V/cm, and dielectric constants ranging from 4-5 have been obtained. Low pinhole counts have been obtained with PECVD oxides, as have very conformal coatings. Adhesion to metal is also reported to be excellent³⁴.

In the *medium temperature range*, SiO_2 is deposited in LPCVD reactors by decomposing tetraethoxysilane, $\text{Si}(\text{OC}_2\text{H}_5)_4$, also known as tetraethyl orthosilicate, or TEOS. The deposition rate for TEOS shows an exponential increase with temperature in the range of 650-800°C with an apparent activation energy of 1.9 eV³³. This pronounced temperature dependence can lead to thickness control problems. The deposition rate is also dependent on the TEOS partial pressure. It is linearly dependent at low partial pressures, and tends to level off as the adsorbed TEOS saturates the surface. TEOS films generally show excellent conformality.

At *high temperatures* (near 900°C) SiO_2 is formed by an LPCVD process in which dichlorosilane and nitrous oxide are reacted⁸. The reaction is given by:



Such depositions produce films having excellent uniformity, and with properties close to those of thermal SiO_2 . High-temperature LPCVD is sometimes used to deposit SiO_2 over poly-Si.

Step Coverage of As-Deposited CVD SiO_2 Films

The manner in which a thin film covers (or conforms to) the underlying features on a substrate is an important characteristic of a deposited film. Film conformality of CVD films is a function of film species and reactor type, and deposition conditions. *Conformal coverage* is coverage in which equal film thickness exists over all substrate topography regardless of its slope (i.e. vertical and horizontal surfaces are coated with equal film thickness, Fig. 17a). The thickness of deposited films at any given point in the mass-transport limited case is dependent on the supply of reactants to that point, which itself is set by process pressure and adatom migration. The following model has been proposed to explain step coverage in terms of these parameters¹.

If adsorbed reactants are able to migrate rapidly across a substrate surface, they will be found with equal probability on any part of the substrate, regardless of topography. This situation results in conformal step coverage, as shown in Fig. 17a. Adatom mobility is a function of adatom species and energy. Both higher substrate temperature and ion bombardment of adatoms enhance adatom migration. Note that under the relatively high temperature conditions used to deposit LPCVD poly-Si and Si_3N_4 films, excellent (i.e. highly conformal) step coverage is usually achieved. Thus, only SiO_2 step coverage need be further considered in this discussion.

If on the other hand, reactant surface migration is slow, then the arrival flux of gaseous reactants at a given point becomes more important in determining the local film thickness. In such cases, it is useful to introduce the concept of the *arrival angle* to help model step coverage. That is, the flux of reactant molecules arriving from an angle between θ and $\theta + d\theta$ can be expressed as $P(\theta) d\theta$ (in a 2-dimensional analysis). Then the total flux arriving at any

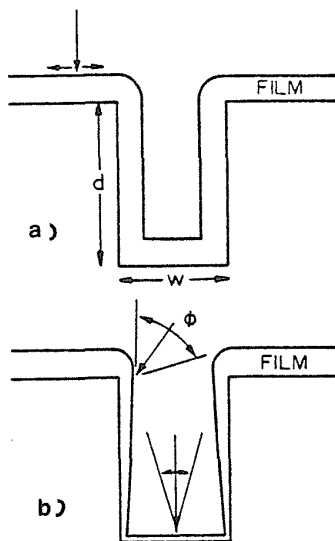


Fig. 17 Schematic diagrams showing types of step coverage. (a) Conformal coverage resulting from rapid surface migration; (b) Non-conformal coverage caused by no surface migration³³. Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet.

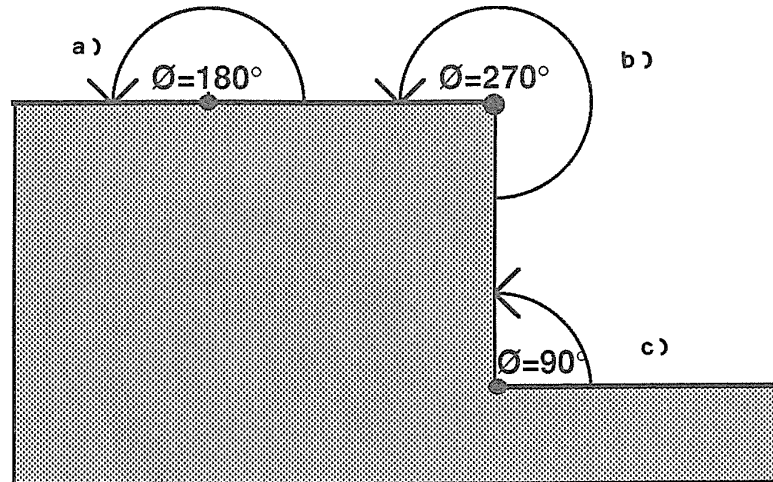


Fig. 18 The concept of *arrival angle* and its effect on step coverage. (a) 180° (b) 270° (c) 90° .

point is $\int_0^{2\pi} P(\theta) d\theta$. For an atmospheric pressure reactor, the mean free path for reactant gas molecules is short, and the frequent collisions of gas molecules with each other completely randomize their velocity vectors. Under such conditions, $P(\theta)$ is a constant, independent of the value of θ . However, $P(\theta)$ is zero for values of θ which are blocked by the substrate. For example, in Fig. 18a, $P(\theta)$ is zero for any angle from 180° to 360° , and constant for $0^\circ < \theta < 180^\circ$.

In short, the value of the flux integral (and thus the eventual film thickness), is directly proportional to the range of angles for which $P(\theta)$ is not zero. This range is called the *arrival angle*. As seen in Fig. 18b, at the top corner of a step, $P(\theta)$ is non-zero over a range of 270° . The resultant film thickness is $270/180$, or 1.5 times greater than for the planar case of Fig. 18a. Similarly in Fig. 18c (i.e. at the bottom corner of a step, or trench) the arrival angle is only 90° , and the film thickness is $90/180$, or one-half that of the planar case. This explains the thickness cross-section that is observed when APCVD SiO_2 is deposited over a sharp step (Fig. 19a). The film is thickest at the upper corner and thinnest at the bottom of the step. This causes the slope in SiO_2 films at the bottom corner to be $>90^\circ$ (i.e. a so-called *re-entrant angle*) making deposition and anisotropic etching of subsequently deposited films extremely difficult.

On the other hand, if the mean free path of the reactant gases is high (e.g. due to the low operating pressure of LPCVD and PECVD reactors), a *shadowing* effect can occur. That is, no longer do frequent collisions over very small distances randomize the gas molecule velocity vectors. Instead, reactant molecules experience few collisions, and follow straight line trajectories over distances comparable to substrate topography dimensions. Substrate surface features near to points being impinged upon can block the straight paths of reactant molecules. Thus such points can be *shadowed* from the reactant flux, and will experience less deposition, and thus less resulting film thickness, than those points which are not shadowed. The arrival angle for the given point now depends on the range of unobstructed *lines of sight* from that point to the reaction chamber (see Fig. 17b). In such long mean free path cases the arrival angle, and thus film thickness, decreases with depth into a trench (as shown in Fig. 17c).

The reactor type and deposition conditions impact step coverage insofar as reactant gas mean free path and adatom migration is affected. The reactor operating pressure determines mean free path lengths, while adatom migration is affected by substrate temperature and also by energy transfer method. For example, due to rapid surface migration, SiO_2 films prepared by TEOS

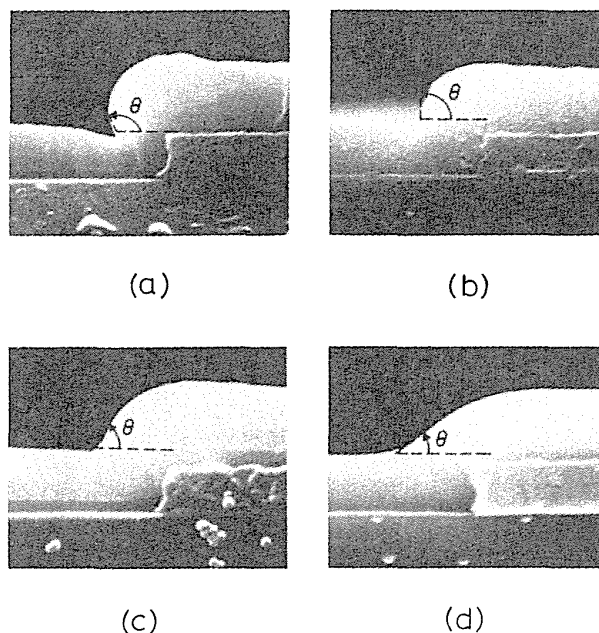


Fig. 19 SEM cross-sections (10,000X) of samples annealed in steam at 1100°C for 20 min for the following weight of phosphorus: (a) 0.0 wt.% P; (b) 2.2 wt.% P; (c) 4.6 wt.% P; 7.2 wt.% P.³³ Reprinted by permission of the publisher, the Electrochemical Society, Inc.

decomposition, or by the high temperature reaction of $\text{SiCl}_2\text{H}_2\text{-N}_2\text{O}$ under LPCVD conditions, exhibit nearly conformal coverage. Conversely, during low temperature deposition of SiO_2 by APCVD, almost no surface migration takes place, and step coverage is dependent only on the arrival angle (and is quite poor, as noted earlier). On the other hand, PECVD produces reactants which arrive at the substrate with more energy (obtained from the glow-discharge) than in APCVD. This results in increased adatom migration. Thus, improved step coverage by PECVD SiO_2 films can be obtained compared to APCVD depositions made at the same temperature. Note that the mechanisms of this model can also be applied to analyzing the step coverage effects seen in evaporated and sputtered films.

CVD and Applications of Undoped and Doped SiO_2 Films

Both undoped and doped films of SiO_2 are easily deposited at low temperatures. Doping of TEOS and high temperature CVD SiO_2 films is more difficult. As we shall see, doping of the SiO_2 can produce a variety of desirable film properties for some applications.

Undoped CVD SiO_2

Undoped CVD SiO_2 is similar to its thermally grown counterpart in many respects, with some exceptions being its as-deposited density and etch rate, and a lower quality SiO_2/Si interface (higher density of interface states). Due to its poor interface qualities, CVD SiO_2 is therefore only used as a temporary structure if it is used in contact with single crystal silicon (e.g. as a capping layer over doped regions to prevent outdiffusion during thermal processes or as an ion-implantation mask). Its chief use, however, is as a permanent structure, whose function

is to increase the thickness of field oxides, or to provide isolation between conductors.

When the underlying conductor is able to withstand high temperatures (e.g. polysilicon or refractory metal silicides) one of the LPCVD methods may be utilized, because of their excellent uniformity, good step coverage, low particulate contamination, and high purity.

Often the film must be deposited over aluminum, and therefore the process must take place at less than 450°C. At these temperatures LPCVD reactions exhibit extremely low deposition rates (Fig. 20b). On the other hand the reaction of silane and oxygen mixtures at atmospheric pressure and temperatures from 300-500°C provides adequately high deposition rates. Therefore such APCVD processes are widely used, despite their particulate and step coverage problems. Undoped oxide can also be deposited by PECVD techniques, with generally improved step coverage as compared to APCVD.

Phosphosilicate Glass

Adding phosphorus dopant during the deposition, typically in the form of phosphine, PH_3 , forms phosphosilicate glass, or PSG. Since PSG consists of two compounds, P_2O_5 and SiO_2 , it is a *binary glass* (or binary silicate), and some of its properties are considerably different from those of undoped CVD SiO_2 . That is, APCVD PSG shows reduced stress and somewhat improved, though still relatively poor, step coverage as compared to undoped CVD SiO_2 . Moreover PSG is a diffusion barrier to moisture, and getters alkali ions. Finally PSG can be *flowed* at high temperatures to create a smoother surface topography, and thereby facilitate the step coverage of subsequently deposited films. The flow step is performed at 1000-1100°C, at pressures from 1-25 atm, and in gas ambients of H_2O , N_2 and O_2 . The glass becomes viscous and responds to surface tension forces, rounding sharp corners. The extent of flow is often measured as the reduction in slope angle of the flowed film surface over an underlying step (Fig. 19), and is a function of flow temperature and phosphorus concentration. Increasing temperature, duration of the flow step, or phosphorus concentration in the oxide will increase film flow. Note that for concentrations less than 6 wt% phosphorus, PSG does not readily flow.

It is relatively easy to incorporate the P_2O_5 into the PSG, as the $\text{SiH}_4:\text{PH}_3$ ratio in the gas flow controls the $\text{SiO}_2:\text{P}_2\text{O}_5$ ratio in the deposited film. PSG, however, becomes increasingly hygroscopic at high phosphorus levels. Thus, it is recommended that its concentration in the oxide film be limited to 6-8 wt% P to minimize phosphoric acid formation, and consequent Al corrosion. Rapid thermal processes have also been reported to successfully flow PSG. It should be noted, however, that if PSG is to be used as a final passivation layer (in which no glass flow

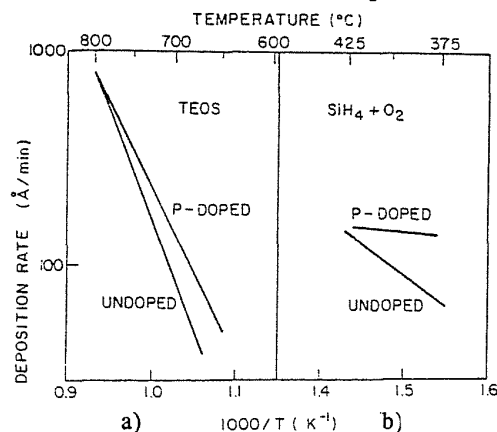


Fig. 20 Arrhenius plots for the deposition of (a) LPCVD TEOS, and (b) LPCVD SiO_2 (P-doped and undoped)³³. Reprinted with permission of the publisher, the Electrochemical Society, Inc.

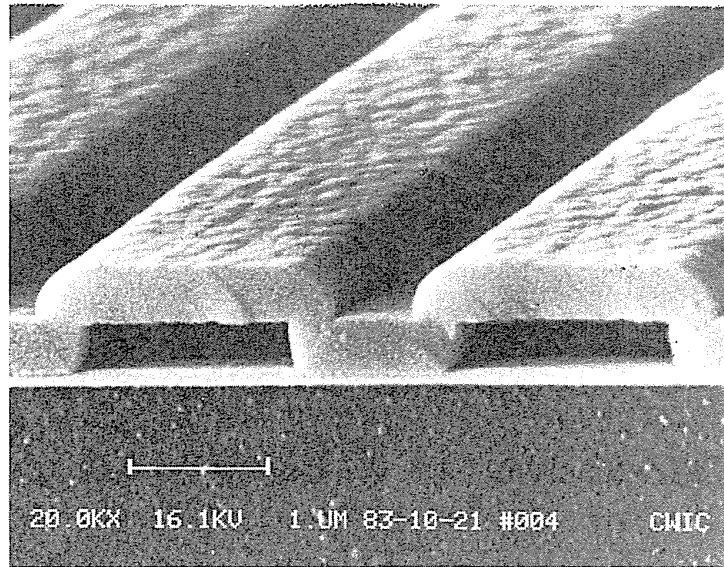


Fig. 21 SEM of PECVD oxide over polysilicon lines. Poly has been removed by wet etch to show detail¹². Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet.

is performed), the maximum permitted phosphorus content is 6 wt%. This is a precaution taken to again minimize the risk of phosphoric acid formation, particularly when in contact with Al.

PSG has been deposited in PECVD systems by the reaction of SiH_4 , N_2 , O_2 , and PH_3 with Ar as a carrier gas. It is reported that the films are more conformal (Fig. 21), crack resistant, and pinhole free than APCVD films³⁴. The phosphorus content is a function of the SiH_4/PH_3 ratio, deposition temperature and $\text{N}_2\text{O}/(\text{SiH}_4 + \text{PH}_3)$ ratio³⁵. The plasma PSG films can be flowed under conditions similar to those for flowing APCVD PSG films.

Borophosphosilicate Glass

Some VLSI processes would benefit from being performed at lower temperatures than those necessary for PSG reflow (1000-1100°C) because such high temperatures result in excessive diffusion of shallow junctions. Furthermore, radiation-hard MOS gate oxides cannot be exposed to high temperature processing (>900°C). But flowable glass is still very desirable for easing film coverage over abrupt steps in the substrate topography. Glass flow temperatures as low as

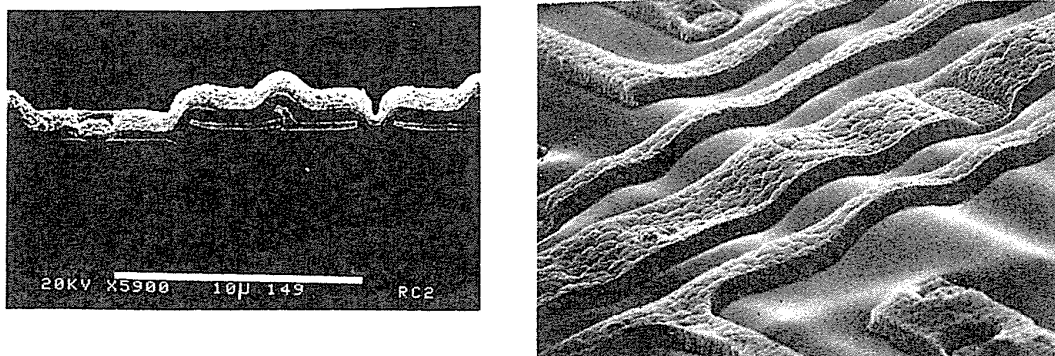


Fig. 22 Micrographs showing BPSG as the interlevel dielectric under the metal. Reprinted with permission of Semiconductor International².

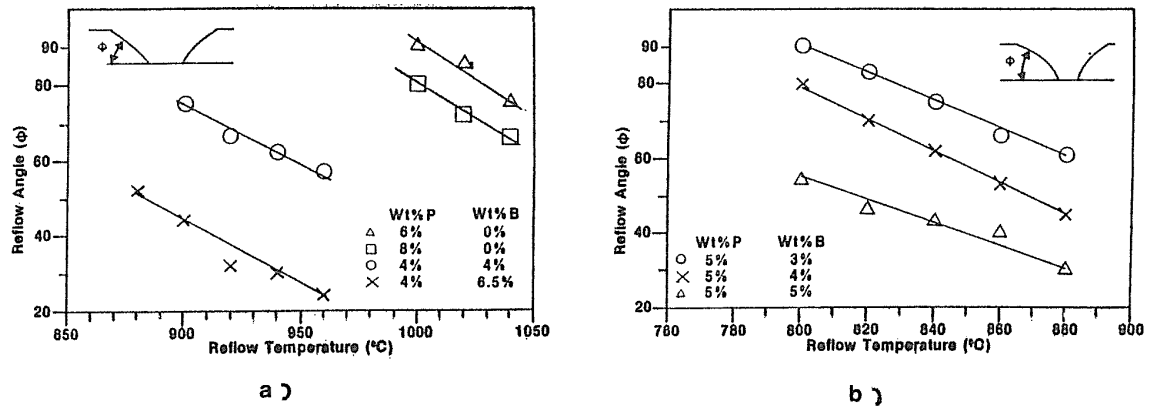


Fig. 23 (a) Reflow angle vs. reflow temperatures in a nitrogen ambient (30 min). (b) Reflow angle vs. reflow temperatures in a steam ambient (30 min). Reprinted by permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet³⁷.

700°C can be obtained by adding boron dopant (e.g. B_2H_6) to the PSG gas flow to form the *ternary* (three component) oxide system $B_2O_3-P_2O_5-SiO_2$, borophosphosilicate glass, or BPSG³⁶ (Fig. 22).

BPSG flow depends upon film composition, flow temperature, flow time, and flow ambient. It has been reported that an increase in boron concentration of 1 wt% in BPSG decreases the required flow temperature by $\sim 40^\circ C$ ³⁶. A plot of required flow temperatures vs. BPSG dopant concentrations in LPCVD films is shown in Fig. 23. In general, increasing the P concentration beyond ~ 5 wt% does not further decrease BPSG flow temperatures. An upper limit on boron concentration is imposed by film stability. That is, BPSG films containing over 5 wt% boron tend to be very hygroscopic and unstable, and if used, should be flowed immediately following deposition. It has also been reported that rapid thermal annealing for 30 s at a temperature 100-175°C higher than that used in a conventional furnace step will result in equivalent BPSG flow³⁶. The ambient gas of the flow cycle also affects the flow mechanism. By using a steam ambient instead of N_2 , the minimum required flow temperature is reduced by $\sim 70^\circ C$ ³⁷.

In addition to exhibiting these low temperature flow properties, BPSG (like PSG) is an alkali ion getter and exhibits low stress. Because of its doping, however, BPSG can also be an unwanted diffusion source to underlying silicon. It is found that BPSG is primarily a source of phosphorus, and the phosphorus outdiffusion is increased at higher boron concentrations.

Besides being useful for isolation, passivation, and surface planarization, BPSG is also more attractive for use than PSG in a process known as *contact reflow*. Following anisotropic etching, contact holes have sharp upper corners which make them difficult to fill (Fig. 24a). By successfully rounding these sharp edges with a *second* thermal flow (or *reflow*) cycle (Fig. 24b), contact coverage by a subsequent metal film is significantly improved. (Note that two separate flow cycles are preferred to a single post-etch flow cycle, since the appropriate degree of flow desired in the second cycle is normally less than that required for the first flow step). The ambient is also usually inert, rather than oxidizing, in order to avoid SiO_2 growth in the contacts during the reflow step. Because flow depends on BPSG composition, precise control of dopant uniformity across substrates is necessary to ensure uniform flow and consequent control of contact size.

BPSG deposition reactions for APCVD⁴, LPCVD³⁸, and PECVD^{39, 40} processes have all been reported. If hot-wall LPCVD reactors are used, they must be equipped with distributed feed gas systems so that adequately uniform BPSG films can be deposited. During deposition, the

source gases for B and P compete with one another for inclusion into the final deposited film. This makes for a complex relation of reactant gas composition to eventual film doping³⁶.

The chemical composition of BPSG (and PSG), can be determined by several techniques, including the following: a) *wet chemical colorimetry*, which is the most accurate, analyzes the dissolved BPSG film; b) *x-ray photoelectron spectroscopy* (see Chap. 17), which is useful for determining the phosphorus content of the film; c) *Fourier transform infrared spectroscopy* (see Chaps. 1 and 5) which can measure boron levels quite accurately, but phosphorus levels less well accurately (due to the presence of a partially obscured phosphorus-oxygen absorption band); and d) *film etch rates in buffered HF*. Since the etch rate of BPSG in buffered HF depends on the concentration of both B and P in the film, a determination of the etch rate can provide a rapid, qualitative comparison of the composition between BPSG samples.

PROPERTIES AND CHEMICAL VAPOR DEPOSITION OF SILICON NITRIDE

Silicon nitride films are amorphous insulating materials that find three main applications in VLSI fabrication: 1) as final passivation and mechanical protective layers for integrated circuits, especially for parts encapsulated in plastic packages; 2) as a mask for the selective oxidation of silicon; and 3) as a gate dielectric material in MNOS devices. Silicon nitride also has a high dielectric constant (6-9 vs ~4.2 for CVD SiO₂), making it less attractive for interlevel insulation, because of the resultant higher capacitance between conductor layers.

Silicon nitride is highly suitable as a *passivation layer* because of its following properties: a) it behaves as a nearly impervious barrier to diffusion (in particular, moisture and sodium find it very difficult to diffuse through the nitride film); b) it can be prepared by PECVD to have a low compressive stress, which allows it to be subjected to severe environmental stress with less likelihood of delamination or cracking; c) its coverage of underlying metal is conformal; and d) it is deposited with acceptably low pinhole densities.

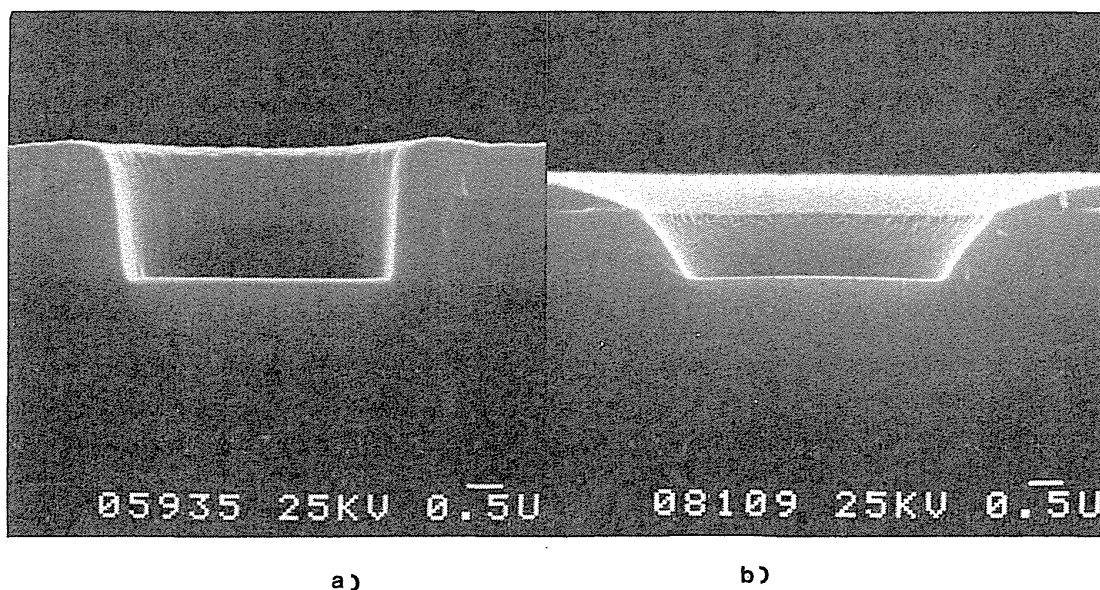


Fig. 24 (a) SEM of dry-etched contact window before reflow. (b) Reflowed BPSG film with 4 wt% P and 4 wt% B. Reflow was 930°C in N₂ for 25 min³⁷. Courtesy of Applied Materials, Inc.

Silicon nitride is useful as a *masking layer for selective oxidation*⁴⁴, since oxygen also finds it difficult to penetrate silicon nitride. That is, silicon nitride is deposited directly on a silicon substrate (actually onto a thin, thermal stress-relief SiO_2 layer, called a *pad oxide*) and patterned. The wafer is then subjected to an oxidation step. The silicon nitride itself oxidizes very slowly, but is not penetrated by the oxygen. As a result it protects the underlying Si from oxidizing, while allowing a thermal SiO_2 layer to grow on regions of exposed Si. For example, at 1000°C in steam for 10 hours, only a few hundred Å of silicon nitride is converted to SiO_2 , while more than $1\text{ }\mu\text{m}$ of SiO_2 can be grown on the exposed silicon. The silicon nitride is removed after the oxidation step.

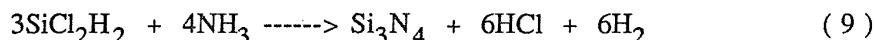
As shown in Table 3, two techniques are used for depositing silicon nitride. When used as a mask for selective oxidation or as a gate dielectric material in MNOS structures, silicon nitride is generally deposited by high-temperature ($700\text{--}800^\circ\text{C}$) LPCVD techniques, for reasons of film uniformity and lower processing cost^{8,31}. When used as a passivation layer, the deposition process must be compatible with such low-melting-point metals as aluminum. Thus silicon nitride must be deposited by a low temperature process ($300\text{--}400^\circ\text{C}$). For such applications PECVD is the deposition method of choice, as it can deposit nitride films at $200\text{--}400^\circ\text{C}$ ^{32,43,44}. PECVD silicon nitride, however, tends to be nonstoichiometric, and

Table 3. Properties of PECVD Silicon Nitride and High Temperature CVD Nitride

Property	HT-CVD—NP 900°C	PE-CVD—LP 300°C
Composition	Si_3N_4	$\text{Si}_x\text{N}_y\text{H}_z$
Si/N ratio	0.75	0.8–1.0
Density	$2.8\text{--}3.1\text{ g/cm}^3$	$2.5\text{--}2.8\text{ g/cm}^3$
Refractive index	2.0–2.1	2.0–2.1
Dielectric constant	6–7	6–9
Dielectric strength	$1 \times 10^7\text{ V/cm}$	$6 \times 10^6\text{ V/cm}$
Bulk resistivity	$10^{15}\text{--}10^{17}\text{ ohms/cm}$	10^{15} ohms/cm
Surface resistivity	$> 10^{13}\text{ ohms/square}$	$1 \times 10^{13}\text{ ohms/square}$
Stress at 23°C on Si	$1.2\text{--}1.8 \times 10^{10}\text{ dyn/cm}^2$ (tensile)	$1\text{--}8 \times 10^9\text{ dyn/cm}^2$ (compressive)
Thermal expansion	$4 \times 10^{-6}/^\circ\text{C}$	$> 4 < 7 \times 10^{-6}/^\circ\text{C}$
Color, transmitted	None	Yellow
Step coverage	Fair	Conformal
H_2O permeability	Zero	Low–none
Thermal stability	Excellent	Variable $> 400^\circ\text{C}$
Solution etch rate		
HFB $20\text{--}25^\circ\text{C}$	$10\text{--}15\text{ Å/min}$	$200\text{--}300\text{ Å/min}$
49% HF 23°C	80 Å/min	$1500\text{--}3000\text{ Å/min}$
85% H_3PO_4 155°C	15 Å/min	$100\text{--}200\text{ Å/min}$
85% H_3PO_4 180°C	120 Å/min	$600\text{--}1000\text{ Å/min}$
Plasma etch rate		
70% CF_4 /30% O_2 , 150 W, 100°C	200 Å/min	500 Å/min
Na^+ penetration	$< 100\text{ Å}$	$< 100\text{ Å}$
Na^+ retained in top 100 Å	$> 99\%$	$> 99\%$
IR absorption		
Si–N max	$\sim 870\text{ cm}^{-1}$	$\sim 830\text{ cm}^{-1}$
Si–H minor	—	2180 cm^{-1}

contains substantial quantities of atomic H (10-30 at%). For this reason it is sometimes chemically represented as $\text{Si}_x\text{N}_y\text{H}_z$. Comparison of the refractive index of CVD silicon nitride with that of thermal silicon nitride gives a quick estimate of the stoichiometry of the CVD film. Higher refractive indices indicate silicon rich films. Table 3 compares the properties of LPCVD and PECVD silicon nitride films.

LPCVD silicon nitride is formed by reacting dichlorosilane (SiCl_2H_2) and ammonia (NH_3) at temperatures between 700-800°C according to the overall reaction:



Silicon nitride depositions by LPCVD are controlled by a large number of deposition parameters including, temperature, total pressure, reactant ratios, and temperature gradients in the reactor. The deposition rate increases with increasing total pressure, or SiCl_2H_2 partial pressure, but decreases as the $[\text{NH}_3] : [\text{SiCl}_2\text{H}_2]$ ratio gets larger. A temperature ramp, as discussed in the section on hot-wall tube LPCVD reactors, is required for obtaining uniform depositions. In general, LPCVD silicon nitride films have a high density (2.9-3.1 g/cm³), a dielectric constant of 6, and are more stoichiometric than PECVD silicon nitride films. Their etch rate in buffered HF is very slow (less than 10 Å/min), and their hydrogen content (up to 8 at%) is less than in PECVD films. In addition, they exhibit excellent step coverage and relatively low particulate contamination. Such films, however, have tensile stresses of $\sim 1 \times 10^{10}$ dynes/cm², which is about an order of magnitude higher than that of TEOS-deposited SiO_2 . This may cause LPCVD silicon nitride films greater than ~ 2000 Å to crack. Sufficient NH_3 is also needed to insure that all of the SiH_4 is consumed. If insufficient NH_3 is available, the films become silicon rich. As a result, depositions are usually carried out with significant excess flow of NH_3 . It should also be mentioned that, as described in Chap. 7, an anneal in hydrogen is often performed on MOS circuits to reduce the interface trapped charge density, Q_{it} , after the final Al layer is deposited and patterned. Since silicon nitride is such an impervious diffusion barrier, this anneal must be performed on wafers prior to depositing a silicon nitride passivation layer.

Silicon nitride deposition by PECVD was described by Sterling and Swann in 1965. The

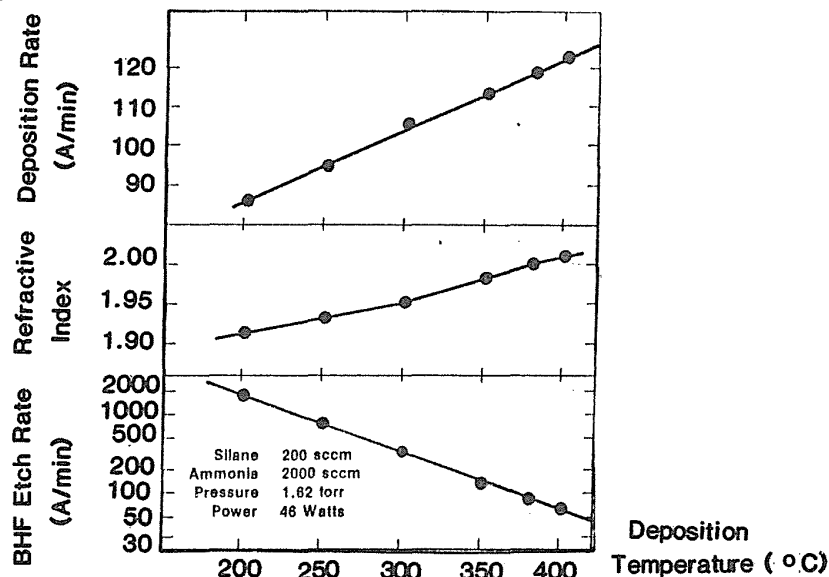
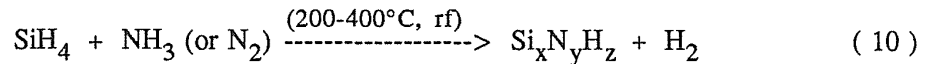


Fig. 25 Effect of deposition temperature on PECVD nitride parameters. Reprinted by permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet¹².

Table 4. CVD DEPOSITION REACTIONS

PRODUCT	REACTANTS	METHOD	TEMP (°C)	COMMENTS
Polysilicon	SiH ₄	LPCVD	580-650	may be <i>in situ</i> doped
Silicon Nitride	SiH ₄ + NH ₃	LPCVD	700-900	
	SiCl ₂ H ₂ + NH ₃	LPCVD	650-750	
	SiH ₄ + NH ₃	PECVD	200-350	
	SiH ₄ + N ₂	PECVD	200-350	
SiO ₂	SiH ₄ + O ₂	APCVD	300-500	poor step coverage
	SiH ₄ + O ₂	PECVD	200-350	good step coverage
	SiH ₄ + N ₂ O	PECVD	200-350	
	Si(OC ₂ H ₅) ₄ [TEOS]	LPCVD	650-750	liquid source, conformal
	SiCl ₂ H ₂ + N ₂ O	LPCVD	850-900	conformal
Doped SiO ₂	SiH ₄ + O ₂ + PH ₃	APCVD	300-500	PSG
	SiH ₄ + O ₂ + PH ₃	PECVD	300-500	PSG
	SiH ₄ + O ₂ + PH ₃ + B ₂ H ₆	APCVD	300-500	BPSG, low temperature flow
	SiH ₄ + O ₂ + PH ₃ + B ₂ H ₆	PECVD	300-500	BPSG, low temperature flow

overall deposition reaction is written as:



where silane and ammonia or nitrogen are reacted in a plasma at 200-400°C. The use of a high (100-1000:1) N₂: SiH₄ ratio is required to prevent silicon rich film formation (since the N₂ dissociation rate is much lower than that of silane). On the other hand, NH₃ dissociates much more readily, and thus lower NH₃: SiH₄ ratios can be used (e.g. 5-20:1).

The deposition rate depends strongly on rf power, gas flow, chamber pressure and frequency (Fig. 25). If a PECVD deposition process is to be developed, it would be useful to approach the problem with a statistically-based set of experiments as discussed in Chap. 18. A case study of such a process development effort is found in Ref. 44. The stress in PECVD silicon nitride films can also be changed by altering a variety of deposition conditions.

Infrared spectroscopy shows that an appreciable amount of hydrogen in the form of Si-H and N-H is found in PECVD silicon nitride films. The total amount of hydrogen can reach 18-22 at% in films deposited from SiH₄-NH₃ near 300°C. Lower hydrogen content is reportedly found in films from SiH₄-N₂¹². The presence of large quantities of hydrogen has been reported to be detrimental to IC devices. For example, significant threshold shifts are observed, and etching characteristics (both wet and dry) of the films are impacted. Another advantage of using N₂ rather than NH₃ is that it yields compressive silicon nitride films over a wider range of deposition conditions. Oxygen in the form of Si-O bonds has also been detected in PECVD silicon nitride films. Oxygen concentration increases as the deposition temperature decreases, and is believed to be due to moisture or oxygen released from the reaction chamber walls. Table 4 is a summary of the CVD reactions for poly-Si, SiO₂, PSG, BPSG, as well as silicon nitride.

OTHER DIELECTRIC FILMS DEPOSITED BY CVD

Silicon Oxynitrides

Materials can be prepared with characteristics between those of nitrides and oxides, and these are called silicon oxynitrides [$\text{SiO}_x\text{N}_y(\text{H}_2)$]. They are formed by reacting SiH_4 with N_2O and NH_3 . Properties can be tailored for improved thermal stability, low stress, and crack resistance⁴⁵. Such films are also less permeable to moisture and other contaminants than deposited oxides. The use of helium as a carrier gas is reported to increase the uniformity of the refractive index of the films⁴⁶. Silicon oxynitrides also are reported to exhibit good properties for use as low-temperature deposited insulators between Al conductors. Two-layer films of PECVD silicon oxynitride and silicon nitride have been used in multilevel interconnect planarization schemes utilizing the differential etch rates of the two materials⁴⁶.

SIPOS

Silicon rich oxide films (i.e. the so-called semi-insulating polycrystalline silicon, or SIPOS) can also be deposited in APCVD, LPCVD, and PECVD reactors. This material has been reported to be excellent for passivating high field transistors⁴⁸, and has been studied for use as an injector in electrically-erasable read-only memories (EEROMs)⁴⁹ as well as a material for forming emitters in advanced super-gain bipolar transistors⁵². The chemical composition of SIPOS is SiO_x , where x ranges from 0.48 to <2 . Such films can be formed by keeping the O_2 : SiH_4 flow rate ratio to <3.5 . The composition of the films can be analyzed with Auger emission spectroscopy (Chap. 17), with a thermal SiO_2 film as a standard.

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PROBLEMS

1. Exponential temperature dependence is alternately represented by the form $\exp(-E_a/kT)$, or by $\exp(-\Delta H/RT)$, where E_a is the value of the activation energy in electron volts, and ΔH is its value in Kcal /mole. Show that if $E_a = 1$ eV, the corresponding value of ΔH is 23 Kcal /mole.
2. If a film is deposited conformally into a window that is 0.5 μm high and 1.0 μm wide, sketch the film when it has a thickness of 2000Å, 5000Å, 10,000Å. If the coverage is like that shown in Fig. 19a, what will the deposited film look like when its thickness is 0.5 μm . What does this effect imply for the application of depositing conformal (and nonconformal) films over high aspect ratio windows?
3. Conjecture why diffusion doped polysilicon can exhibit lower resistivities than polysilicon doped with ion implantation.
4. The activation energy of the $\text{SiH}_4\text{-O}_2$ reaction is ~ 0.6 eV for undoped oxides, while that for the undoped TEOS reaction is ~ 1.9 eV. If the deposition rate of CVD SiO_2 by the $\text{SiH}_4\text{-O}_2$ reaction is 250Å /min at 400°C, and is the same for the TEOS reaction at 700°C, find the temperatures for both of these reactions at which the deposition rate will double.
5. As CVD reactors are being designed as single wafer machines (as opposed to batch deposition systems), comment on some of the problems that have to be overcome in single wafer designs.
6. The minimum temperature for flow in phosphorus-doped SiO_2 is $\sim 1000^\circ\text{C}$. For some VLSI fabrication processes, the maximum allowable temperature is 900°C. Suggest four techniques that are candidates for producing layers of dielectric material between two conducting layers that is planarized, without having to heat the wafers to 1000°C.
7. Explain the difference between the terms *flow* and *reflow*.
8. Summarize the differences in the properties of high-temperature deposited silicon nitride, and plasma-deposited silicon nitride.

ALUMINUM THIN FILMS and PHYSICAL VAPOR DEPOSITION in VLSI

This chapter is divided into four major topics involved in the formation of interconnect structures in VLSI. They are:

1. *The Properties of Aluminum (and Aluminum Alloy) Thin Films in VLSI.* This section considers the advantages and limitations of such films for VLSI applications. It should be noted, however, that many of the fabrication processes that involve aluminum are also discussed elsewhere in the chapter (e.g. deposition of aluminum films by evaporation or sputtering), or in other chapters of this volume (e.g. wet etching of aluminum in Chap. 15). A variety of issues associated with the use of thin film aluminum are addressed in other parts of this text as well, including: a) step coverage (this chapter); b) effects of gas incorporation in the deposited film (this chapter); c) electromigration (Vol. 2 of this text); d) hillocks in Al thin films and their suppression (Vol. 2); and e) contact formation to silicon, including spiking, contact electromigration failure, and contact structures /barrier layers (this chapter and Vol. 2).

2. *Physical Vapor Deposition (PVD) by Sputtering.* The discussion on sputtering is quite extensive, as this is the primary PVD method utilized in VLSI applications. The sputtering presentation covers the following subjects: a) glow-discharge physics; b) the physics of sputtering; c) the deposition kinetics of sputtered films; d) sputter system configurations (dc, rf, and magnetron); e) commercially available sputtering equipment for microelectronic applications; and f) sputter deposition processing issues.

3. *Physical Vapor Deposition of Thin Films by Evaporation.* This section is less detailed, as evaporation is not as extensively used in VLSI applications as sputtering.

4. *Thickness Evaluation of Opaque (Especially Metallic) Thin Films.*

Since the key topic of this chapter is *physical vapor deposition* (PVD) it is useful to define the concept and introduce the common characteristics shared by PVD processes. All PVD processes proceed according to the following sequence of steps:

- a) The material to be deposited (solid or liquid source) is physically converted to a vapor phase;
- b) The vapor is transported across a region of reduced pressure (from the source to the substrate); and
- c) The vapor condenses on the substrate to form a thin film.

The conversion to a gaseous phase (Step a) is done by the addition of heat (in evaporation deposition), or through the physical dislodgement of surface atoms by momentum transfer (in

Table 1. PROPERTIES OF ALUMINUM AND ALUMINUM ALLOY THIN FILMS

Name	Symbol	Melting Point (°C)	Al /Si Eutectic (°C)	Density (g/cm ³)	Resistivity (μΩ-cm)
Aluminum	Al	660	577	2.70	2.7
Aluminum/ 4% Copper	Al 4%Cu	650	~577	2.95	3.0
Aluminum/ 2% Silicon	Al 2%Si	640	~577	2.69	2.9
Aluminum/ 4% Copper 2% Silicon	Al 4%Cu 2%Si		~577	2.93	3.2

sputter deposition). It is this step which will receive the most attention in the chapter, as some of the aspects of film condensation and formation are discussed in the earlier chapters dealing with Thin Films, Epitaxy, and CVD. It is also worth mentioning that many concepts used to describe PVD processes, such as vacuum pressure, mean free path, impingement rate, monolayer time, vapor pressure, molecular and viscous flow, are presented in Chap. 3.

ALUMINUM THIN FILMS IN VLSI

Aluminum is the third material in the trinity of matrix substances employed to fabricate silicon solid-state components (the other two being silicon and silicon dioxide). Aluminum is primarily utilized in these applications in thin-film form, and it functions as a material which interconnects the device structures formed in the silicon substrate. It has emerged as the most important material for such applications because of its low resistivity ($\rho_{\text{Al}} = 2.7 \mu\Omega\text{-cm}$), and its compatibility with the other two matrix substances^{1,49}. For example, aluminum thin films adhere well to SiO_2 . (During the thermal step that sinters the metal silicon contacts, the aluminum atop SiO_2 forms a thin layer of Al_2O_3 at the Al/ SiO_2 interface, and this promotes good adhesion.) The material properties of aluminum films which are of most interest for silicon device fabrication are listed in Table 1. Aluminum alloys are also often utilized in microelectronic applications, including: a) Al-1wt%Si; b) Al-2wt%Cu; c) Al-4wt%Cu; d) Al-1wt%Si-2wt%Cu; and e) Al-1.2wt%Si-0.15wt%Ti. Note that the relatively low values of the melting point of Al (660°C) and the Al-Si eutectic temperature (577°C), restrict the maximum value of subsequent processing temperatures once the Al film has been deposited.

Aluminum thin-films are deposited as polycrystalline materials, usually in the 0.5 μm-1.5 μm thickness range. Early microelectronic devices utilized evaporation to deposit pure Al, Al-Si, or Al-Cu alloys, but the stringent alloy-composition requirements of VLSI (and other limitations of evaporation) have made sputtering the dominant PVD technology for aluminum films. The development of magnetron sputtering (which allows aluminum to be deposited at deposition rates of up to ~1μm/min), further decreased the use of evaporated Al film deposition. Aluminum alloys are used more frequently than pure aluminum because they possess enhanced properties for certain interconnect requirements, including superior contact formation characteristics and better resistance to electromigration. A brief introduction to these topics

follows, but the reader is directed to Vol. 2 for a more detailed discussion of them.

The use of *Al-Si* in place of *pure Al* stems from problems of *junction spiking* that occur at the interface of pure Al and Si, when the interface is heated. That is, the solubility of silicon in aluminum (Fig. 1) rises as the temperature increases (e.g. to about 0.5% at 400°C). Thus, when the silicon substrate is put into intimate contact with a pure aluminum film, the silicon substrate acts as a source of the silicon that the aluminum can take up in solution. In addition, the diffusivity of silicon along the grain-boundaries of the aluminum film at 400°C is quite high. Thus, a significant quantity of Si can move from the region below the metal-substrate interface and into the aluminum film. Simultaneously, aluminum from the film will move to fill the voids created by the departing Si (Fig. 2). If the penetration by the aluminum is deeper than the p-n junction depth below the contact, the junction will be electrically shorted (junction spiking). To suppress this mechanism, an alloy of Al which contains a concentration of Si in excess of the Si solubility at the maximum process temperature, can be used in lieu of pure aluminum. Thus, when the (Al-Si)-silicon interface is heated, the aluminum alloy film does not need to receive silicon into solution from the substrate, and junction spiking is avoided.

Although this remedy has been successfully applied in the past, it appears to be inadequate for VLSI applications. The shallower junctions, narrower metal lines, and more severe topography of VLSI are less tolerant of Si precipitation in the Al-Si film that occurs when such films are cooled down from 400°C temperature steps. In addition, electromigration failure effects at Al-Si-silicon contacts become more severe as the contacts get smaller. More elaborate contact structures employing barrier materials, and other layers, appear to be necessary replacements (e.g. Si/W/Al, or Si/PtSi/Ti:W/Al contact structures). Volume 2 discusses the topic of metal-silicon contacts and the inadequacies of Al-Si for VLSI in substantially more detail.

It has also been found that the addition of small quantities (0.1-4%) of other materials [e.g.

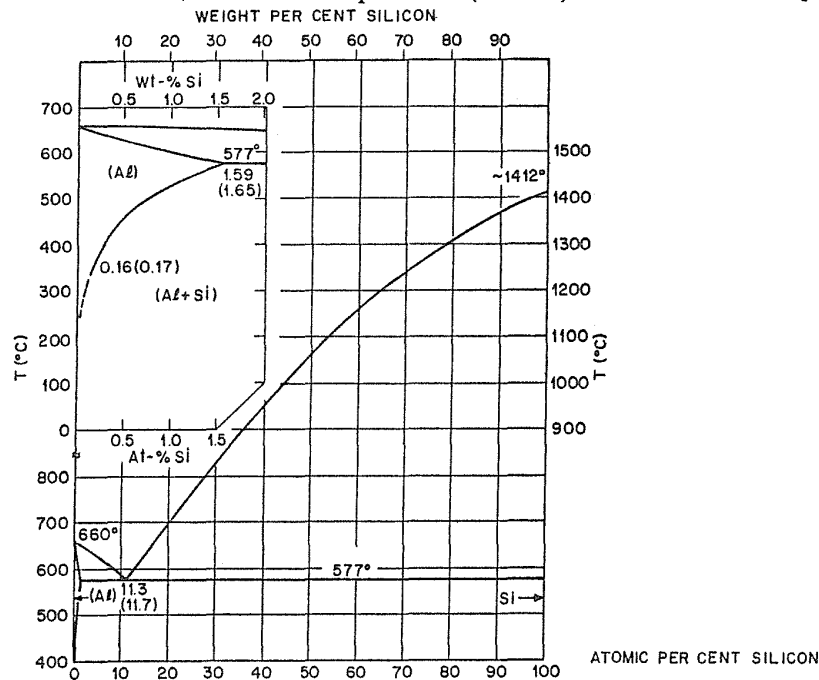


Fig. 1 Phase diagram of the aluminum-silicon system. From M. Hansen and A. Anderko, *Constitution of Binary Alloys*, 1958. Reprinted with permission of McGraw-Hill Book Co.

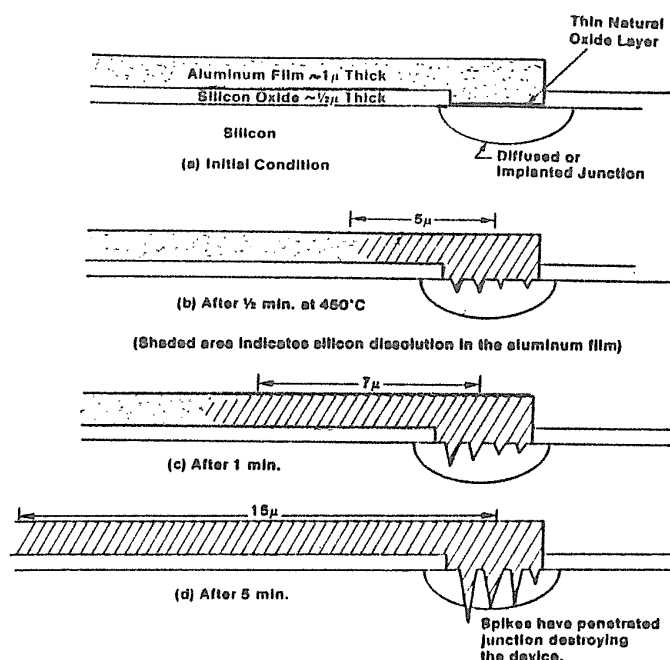


Fig. 2 Junction spiking and silicon migration during contact sintering.

Cu (0.5-4wt%), and more recently Ti (0.1-0.5wt%)] to the aluminum, improves the electromigration resistance and reduces the propensity of aluminum thin-films to form hillocks (i.e. protrusions on the Al film surface, see Fig. 36). One penalty for such improvements is that the resistivity of such films is increased (by ~10-30%) over that of pure aluminum films. Other drawbacks that must be accepted in exchange for the enhanced behavior of such alloys include added process complexity, and more stringent process controls. That is, an appropriate combination of alloy composition, film deposition, annealing, and etch processes must be selected, developed, evaluated, and maintained. Furthermore, some processes are more difficult to perform on alloy films than on pure Al films, such as dry etching of Al-Cu films (Chap. 16). Details of the issues that must be considered in developing and evaluating processes that utilize Al alloy films are discussed elsewhere, both in this volume and Vol. 2 of this text.

Some other characteristics of aluminum thin films also need to be described at this point. Aluminum readily forms a thin native oxide (Al_2O_3) on its surface upon exposure to oxygen, even at room temperature. The presence of this oxide can effect the contact resistance when another metal layer is deposited on the Al, and can inhibit both the sputtering of an aluminum target and the etching of aluminum films. Aluminum thin films can also suffer corrosion problems as a result of some fabrication processes. For example, if phosphorus-doped SiO_2 is deposited onto Al films, phosphoric acid (HPO_3) can be formed if moisture is absorbed by the glass. This acid will attack Al and cause corrosion. In addition, dry etching of Al may leave chlorine residues on the Al surfaces. Exposure to ambient moisture can lead to the formation of HCl. If Cu is present as an alloy in the Al film, severe corrosion can occur (as the CuAl_2 compound and the Al form microelectrodes of a battery, and HCl acts as the electrolyte). Both of these problems are discussed elsewhere in the text in more detail (see Index, under *Al, corrosion*).

SPUTTER DEPOSITION FOR VLSI

Sputtering is a term used to describe the mechanism in which atoms are dislodged from the surface of a material by collision with high energy particles. It has become the most widely utilized deposition technique for a variety of metallic films in VLSI fabrication, including aluminum, aluminum alloys, platinum, gold, titanium:tungsten and tungsten. It is also used in some applications to deposit molybdenum, Si, SiO₂ (silica glass), and refractory metal silicides, although CVD or evaporation may be more frequently used to deposit this group of materials.

Sputtering has displaced evaporation as the workhorse PVD method for VLSI because of the following advantages:

- a) Sputtering can be accomplished from large-area targets, which simplifies the problem of depositing films with uniform thickness over large wafers;
- b) Film thickness control is relatively easily achieved by selecting a constant set of operating conditions and then adjusting the deposition time to reach it;
- c) The alloy composition of sputter-deposited films can be more tightly (and easily) controlled than that of evaporated films;
- d) Many important film properties, such as step coverage and grain structure, can be controlled by varying the negative bias and heat applied to the substrates. Other film properties, including stress and adhesion, can be controlled by altering other process conditions, such as power and pressure;
- e) The surface of the substrates can be sputter-cleaned in vacuum prior to initiating film deposition (and the surface is not exposed again to ambient after such cleaning);
- f) There is sufficient material in most sputter targets to allow many deposition runs before target replacement is necessary, and;
- g) Device damage from x-rays generated during electron-beam evaporation is eliminated (although some other radiation damage may still occur).

As is true with other processes, however, sputtering also has its drawbacks. They are:

- a) Sputtering processes involve high capital equipment costs;
- b) The deposition rates of some materials are quite slow (e.g. SiO₂);
- c) Some materials (e.g. organic solids) are frequently unable to tolerate ionic bombardment, and degrade in a sputter environment; and,
- d) Since the process is carried out in low-medium vacuum ranges (compared to the high vacuum conditions under which evaporation is conducted), there is greater possibility of incorporating impurities into the deposited film.

In general, the sputtering process consists of four steps: 1) ions are generated and directed at a target; 2) the ions sputter target atoms; 3) the ejected (sputtered) atoms are transported to the substrate, where; 4) they condense and form a thin film. Although it is of interest to note that sputtering can be conducted by generating the energetic incident ions by other means (e.g. ion beams), in virtually all VLSI sputtering processes their source is a glow-discharge. The discussion of sputtering in this section will be limited to *glow-discharge sputtering*^{4,5,12}.

Properties of Glow Discharges

The energetic particles used to strike target materials to be sputtered in VLSI sputter deposition systems are generated by glow-discharges^{4,5}. A *glow-discharge* is a self-sustaining

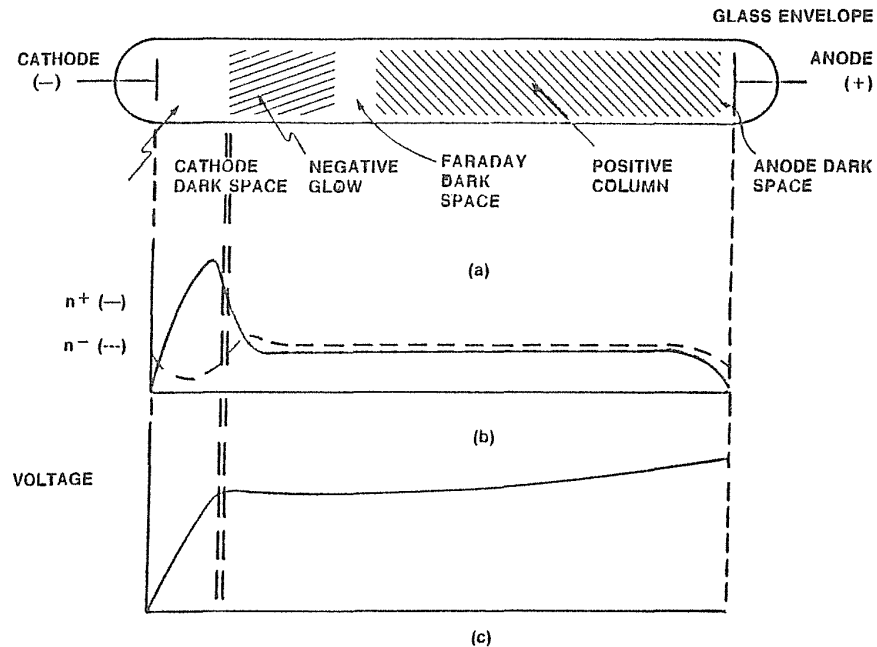


Fig. 3 (a) Structure of a glow discharge in a dc diode system. (b) Charged particle concentration in a glow discharge. (c) Voltage variation in a dc diode glow discharge. Courtesy of MRC.

type of plasma (i.e. a *plasma* is defined as a partially ionized gas containing an equal number of positive and negative charges, as well as some other number of non-ionized gas particles). In Fig. 3 we show a simple *dc diode type* system that can be employed to study the properties of glow-discharges used in sputtering. It consists of a glass tube which is evacuated and then filled with a gas at low pressures. Within the tube there are two electrodes (a positively charged *anode* and a negatively charged *cathode*) between which a dc potential difference is applied.

Creation of Glow Discharges

Let us consider this system to examine the situation when the tube is filled with argon at an initial pressure of 133 Pa (1 torr), the distance between the electrodes is 15 cm, and a 1.5 kV potential difference is applied between the cathode and anode. At the outset no current flows in the circuit, as all the argon gas molecules are neutral and there are no charged particles in the gas. The full 1.5 kV is thus dropped between the electrodes. If a free electron is introduced into the tube (most likely created from the ionization of an argon atom by a passing cosmic ray), it will be accelerated by the electric field existing between the electrodes (whose magnitude is: $E = V/d = 1.5 \text{ kV} / 15 \text{ cm} = 100 \text{ V/cm}$).

The average distance that a free electron will travel in an Ar gas at 133 Pa before colliding with an Ar atom (i.e. the mean free path), is 0.0122 cm (see Chap. 3). Most electron-atom collisions are *elastic*, in which virtually no energy is transferred between the electron and gas atom (because of the very light mass of the electron compared to a gas atom). Thus, the mean distance traveled by an electron before it makes an *inelastic* collision (in which significant energy is transferred to the atom, by the excitation of an atomic electron to a higher energy level in the atom, or to escape from the atom) is about ten times the mean free path, or 0.122 cm. If this is the *mean distance traveled by electrons between inelastic collisions*, there must be a significant

number of electron path lengths between inelastic collisions in the range of 0.5-1.0 cm. If a free electron travels 1 cm in the 100 V/cm electric field, it will have picked up 100 eV of kinetic energy. This is sufficiently high so that during an inelastic collision, enough energy can be transferred to the orbital electrons of the Ar atoms to cause their excitation or ionization. If the transferred energy, E , is less than the ionization potential (e.g. $11.5 \text{ eV} < E < 15.7 \text{ eV}$ for Ar), the orbital electron will be excited to a higher energy state for about 10^{-8} sec, and then return to the ground state with the emission of visible-light photons. Such excitation is the source of light emission in glow-discharges.

If the energy transferred is greater than the ionization potential (i.e. $>15.7 \text{ eV}$ for Ar), a second free electron (and positive ion) will be created. Subsequently, both free electrons will become accelerated again, and the opportunity for cascading the number of free electrons and creating a condition known as *gas breakdown* exists. Figure 4 shows the breakdown voltage required to initiate discharge, as function of the product of the pressure, P , and the electrode spacing, d . When the condition of gas breakdown is reached, current flows in the external circuit as the collision-generated free electrons are collected by the anode. Each new ionization event, however, will take place closer to the positively charged anode (as the electrons are accelerated in its direction). Therefore, the current will increase to a maximum and quickly decay to zero, unless there is a mechanism available for generating additional free electrons for sustaining the current flow. When a sufficient number of electrons are available to maintain the discharge, the discharge is said to be *self-sustained*. The source of such electrons is discussed later.

Structure of Self-Sustaining Glow Discharges and Their Dark Spaces

A self-sustaining discharge in a system (as shown in Fig. 3) exhibits certain characteristics. First, at equilibrium the voltage drop between the electrodes is reduced (e.g. in our example, from 1.5 kV to about 150 V), and the discharge current builds up to the point that the voltage drop across the current limiting resistor is equal to the difference between the supply voltage and the electrode potential difference. Second, the discharge has a particular structure, as shown in Fig. 3a. The most important region of the discharge is the *Crookes dark space* between the negative glow and the cathode. In Fig. 6b, we see that the positive ions of the discharge are present in higher density in front of the negatively charged cathode, producing a localized *space charge* there. Any electrons near the cathode are rapidly accelerated *away* from it, due to their relatively light

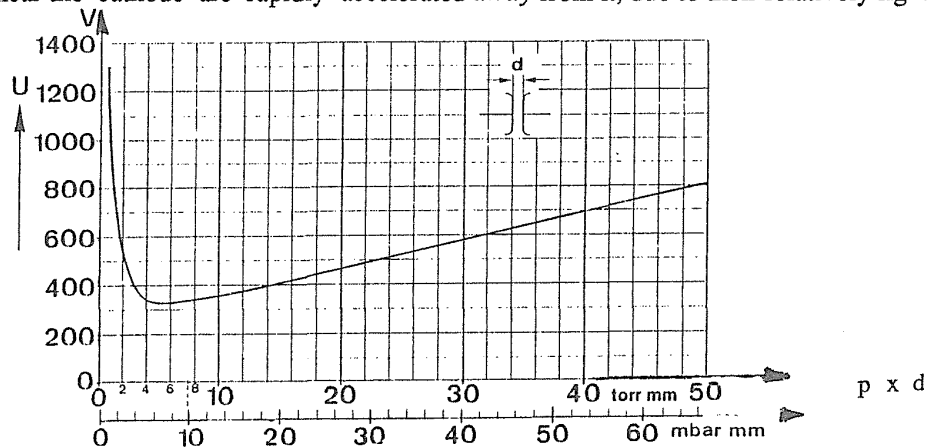


Fig. 4 Breakdown voltage, U , between two parallel plane electrodes in a homogeneous electric field as a function of gas pressure, p , and electrode distance, d , for air (Paschen's curve).

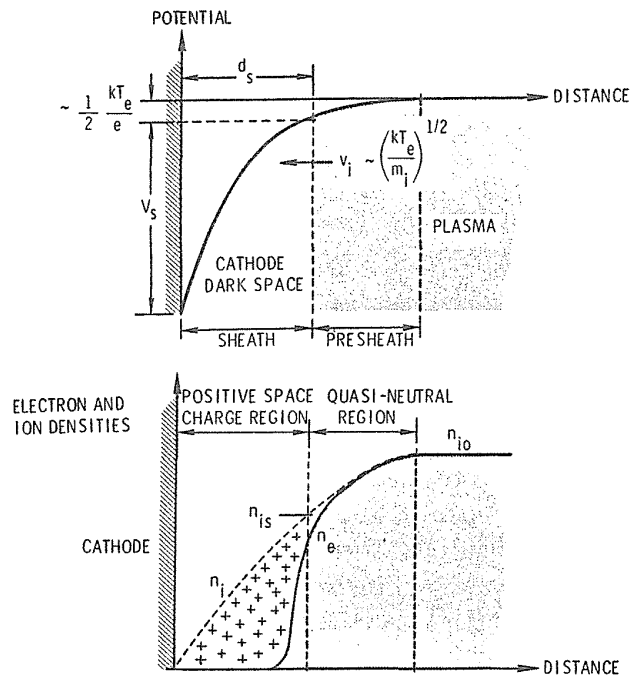


Fig. 5 Schematic representation of the positive space charge region that develops over a cathode¹³. Reprinted with permission of Academic Press.

mass. The much more massive ions are accelerated *toward* the cathode, but much less quickly. Thus, on average, they spend more time than electrons traversing the Crookes dark space, and at any instant their concentration in the dark space is greater than that of electrons.

This has the net effect of greatly increasing the electric field immediately in front of the cathode, and also of screening the remainder of the discharge from the cathode voltage. As a result, the electric field in the rest of the discharge is rather low and uniform, and the glow regions of the discharge are therefore more truly plasma-like (as defined at the outset of this section), than the dark space regions, which do not contain equal concentrations of positive and negatively charged particles. The greatest part of the voltage between the anode and cathode is thus dropped across the Crookes dark space, and therefore charged particles (ions and electrons) experience their largest acceleration in this region.

The reduced luminosity of the dark space is also due to the electric field present across the dark space. That is, since electrons in the dark space are strongly accelerated and traverse through the space quickly, the electron density at any instant in the dark space is drastically reduced (Fig. 5). Although there are fewer electrons, those present can gain high energies from acceleration by the electric field. When they collide with gas atoms in the dark space, they are thus more likely to cause *ionization*, rather than *excitation* events. As a result fewer light-generating electron-atom collisions occur than in the negative and positive glow regions.

When positive ions from the negative glow region enter the Crookes dark-space, they experience the strong local electric field and become accelerated toward the cathode. They also have a high probability of exchanging their charge with neutral atoms in the dark space. In doing so, they retain their momentum, while losing their charge. The formerly neutral recipient atom becomes an ion, and only at that time can begin accelerating towards the cathode. The effect of

this *charge transfer mechanism* was studied by Davis and Vanderslice, and a summary of their results is shown in Fig. 6. The data concludes that *virtually no ions reach the target with the full dark space energy*. In addition, it implies that the *cathode is bombarded by energetic neutral atoms as well as energetic ions*, and thus both species apparently produce sputtering events.

The source of electrons that sustains the discharge is the cathode, which emits secondary electrons when struck by ions. (The mechanisms of such emission are discussed in more detail in a subsequent section.) Thus, upon entering the dark space from the cathode, the electrons are accelerated by the dark space field toward the anode. Upon colliding with atoms in the dark space, they cause ionization, and are also slowed. As slower electrons, they are less energetic and thus the probability of colliding with Ar atoms and causing excitation rather than ionization events is increased. The edge of the negative glow region therefore provides an indication of where such slowed electrons start to be created in large numbers (as a result of high energy, inelastic collisions). If the pressure in the tube is reduced, the distance that the emitted electrons travel before colliding and becoming slowed, becomes longer. Consequently, the dark space lengthens. If the pressure becomes too low, the dark space extends the full length between the electrodes, and the glow-discharge extinguishes. For dc diode sputtering systems, this effect limits the minimum practical pressure for sputter deposition to the range of 10-40 mtorr (1.3-5.2 Pa). The long dark spaces of dc diodes are also an indication that the electrons are not efficiently utilized to produce ions. Thus, we shall see later how magnetic fields are employed to increase the electron path length in the course of traversing the region between cathode to anode [magnetron sputtering]. This increases the probability that the electrons undergo an ionizing collision before being collected by the anode. The dark space in such magnetron sputtering systems is typically reduced from 1-2 cm to ~0.5 mm.

Obstructed Glow Discharges and Dark-Space Shielding

In dc diode configurations, there must be sufficient electrons emitted at the cathode to keep the discharge self-sustaining, and these electrons must undergo an adequate number of

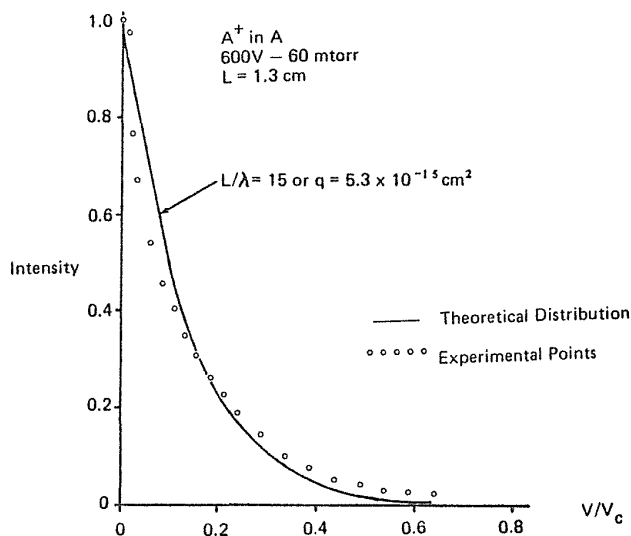


Fig. 6 Energy distribution for Ar^+ from an argon discharge⁷. Reprinted with permission of the American Physical Society.

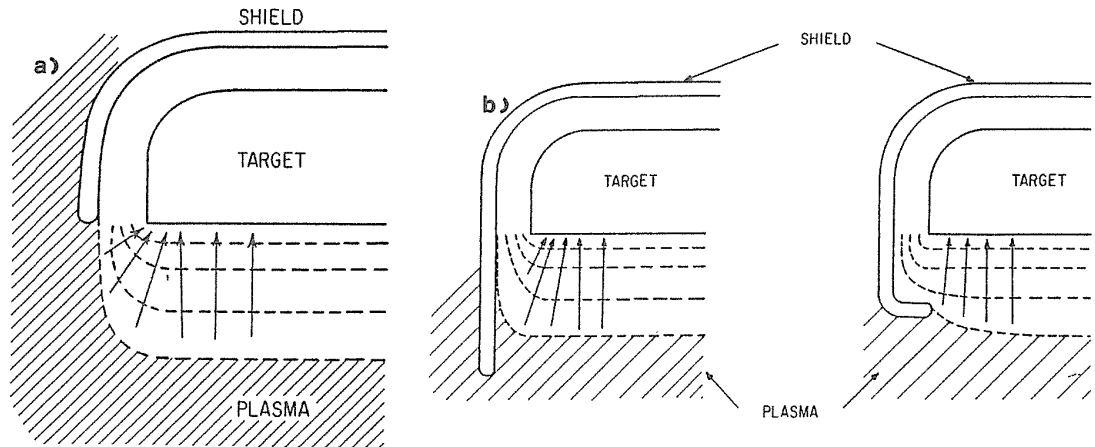


Fig. 7 (a) Potential distribution in vicinity of cathode shield (b) Reducing rim effect by extending cathode shield. (c) Reducing rim effect by wrapping shield around the cathode¹⁵. From L. Maissel and R. Glang, Eds., *Handbook of Thin Film Technology*, 1970. Reprinted with permission of McGraw-Hill Book Company.

ion-producing collisions with the sputter gas. These electrons are produced by ion bombardment of the cathode. Thus, there only needs to be a sufficient number of ions produced in the dark space (and in the glow regions) to produce enough secondary electrons to sustain the glow-discharge. As a result, as long as enough ions are produced in the dark space and glow regions, the exact location of the anode is not important. In fact, if the anode is gradually moved closer to the cathode, the positive column shown in Fig. 3 first disappears, then the Faraday dark space vanishes. Finally, a substantial fraction of the negative glow may be extinguished, before any significant effect on the electrical characteristics is observed. If the anode gets too close to the dark space, the ion production rate becomes reduced, and the voltage across the electrodes must rise to increase the secondary electron emission. Such a glow is known as an *obstructed glow*. In most practical sputter deposition systems the glow is obstructed. That is, in order to most effectively collect the sputtered material onto the substrate, the anode (on which the wafers are sometimes mounted) is placed as close to the cathode as possible (typically just far enough away to avoid extinguishing the negative glow).

On the other hand, it is typically necessary to insure that sputtering is allowed to occur only at the front side of the target, as the back side contains cooling coils, attachment fixtures, etc., which are definitely not to be sputtered. To guarantee that no sputtering takes place except from desired surfaces, a shield of metal (at a potential equal to that of the anode) is placed at a distance less than the Crookes dark space at all other cathode surfaces (Fig. 7). Since no discharge will take place between two electrode surfaces separated by less than this distance, such shielding (termed *dark-space shielding*) is effective in preventing sputtering from unwanted cathode surfaces.

Physics of Sputtering

When a solid surface is bombarded by atoms, ions, or molecules, many phenomena can occur. The kinetic energy of the impinging particles largely dictates which events are most likely to take place. For low energies (<10 eV), most interactions occur only at the surface of the target material. At very low energies (<5 eV) such events are likely to be limited to

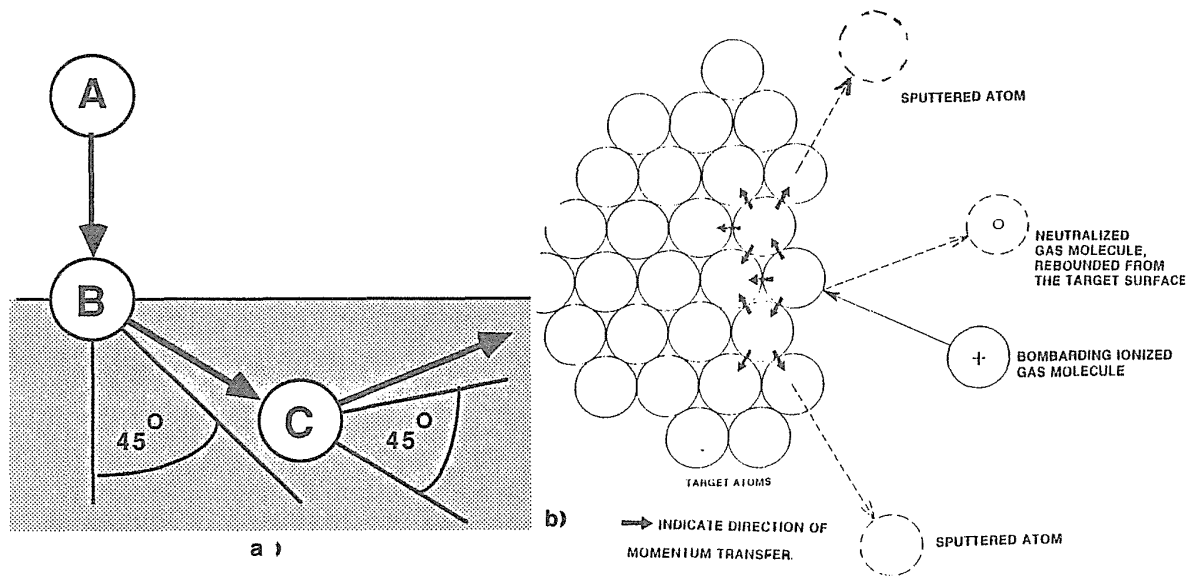


Fig. 8 (a) Binary collision between atom A and B, followed by a binary collision between atom B and C. (b) Collision process responsible for sputtering and fast neutral generation.

reflection or physisorption of the bombarding species. For low energies which exceed the binding energy of the target material (5-10 eV), surface migration and surface damage effects can take place. At much higher energies (>10 keV), the impinging particles are most likely to be embedded in the target, and this mechanism is the basis of ion-implantation. At energies between the two extremes, two other effects also arise: 1) some fraction of the energy of the impinging ions is transferred to the solid in the form of heat, and lattice damage; and 2) another fraction of such energy causes atoms from the surface to be dislodged and ejected into the gas phase (*Sputtering*).

Billiard Ball Model of Sputtering

The exact mechanisms which lead to the ejection of atoms under ion bombardment are not known, and a comprehensive theory of sputtering is not likely to be developed in the near future since many parameters are involved, including the kinetic energy of the ions, lattice structure, and binding energy of lattice atoms. Some of the details, however, are reasonably well understood and can be aptly described with a relatively simple momentum-transfer model. G.K. Wehner, whose theoretical work first established a solid scientific basis for sputtering, often described sputtering as a game of three-dimensional billiards, played with atoms⁷. Using this analogy, it is possible to visualize how atoms may be ejected from a surface as the result of two binary collisions (Fig. 8b & c) when a surface is struck by a particle with a velocity normal to the surface (e.g. atom A in Fig. 8b). Note that a *binary collision* is one in which the primary particle strikes a single object (e.g. atom B in Fig. 8b), and gives up a significant fraction of its energy to the struck atom, while retaining the remaining fraction. As a consequence of the collision, atom B may leave the point of impact at an angle greater than 45°. If atom B then undergoes a secondary collision with atom C, the angle at which atom C leaves the secondary impact point may again be greater than 45°. Thus, it is possible that atom C can have a velocity component greater than 90° (and thus be directed outward from the surface). As a result, there is

a finite probability that atom C will be ejected from the surface as a result of the surface being struck by atom A.

When the directions of sputtered atoms from the surface of polycrystalline materials (and most cathode materials in sputter applications are polycrystalline) are measured for the case of *normal incidence*, it is found that the ejected atoms leave the surface in essentially a cosine distribution. A cosine distribution, however, does not describe the sort of small-angle ejections that would be expected from the simple collision processes described above. Evidently in actual sputtering events, more than two collisions are involved, and the energy delivered by impinging ions *during normal incidence* is so randomly distributed that the effect of the incident momentum vector is lost. Note that the energy range of sputtered atoms leaving the target is typically 3-10 eV, and that the bombarding species also recoil from the cathode face with some energy. Thus, the target surface is a source of sputtered atoms as well as energetic backscattered species.

For the case when the surface is bombarded by ions at an oblique angle (i.e. $>45^\circ$), there is a higher probability that the primary collision between the incident ion and the surface atom will lead to a sputtering event. Furthermore, oblique incidence confines the action closer to the surface, and thus sputtering is enhanced. In cases of oblique bombardment, the incident momentum vector becomes important, and sputtered atoms are ejected strongly in the forward direction. In addition, the *sputtering yield*, defined as the number of atoms ejected per incident ion, may be as much as an order of magnitude larger than that resulting from normal incidence by bombarding ion (Fig. 9). This effect also leads to *faceting*, which is discussed in a later section.

Sputtering Yield

The *sputtering yield* is important because it largely (but not completely) determines the rate of sputter deposition. Sputtering yield depends on a number of factors besides the direction of incidence of the ions, including: a) target material; b) mass of bombarding ions; and c) the energy of the bombarding ions. There is a minimum energy threshold for sputtering that is approximately equal to the heat of sublimation (e.g. 13.5 eV for Si). In the energy range of sputtering (10-5000 eV), the yield increases with ion energy and mass. Figure 10 shows the sputtering yields of copper as a function of energy for various noble gas ions. The sputtering yields of various materials in argon at different energies is given in Table 2¹⁴.

Several matters related to sputtering yield should also be noted. First, although the sputtering yields of various materials are different, as a group they are much closer in value to one another than, for example, the vapor pressure of comparable materials. This makes the

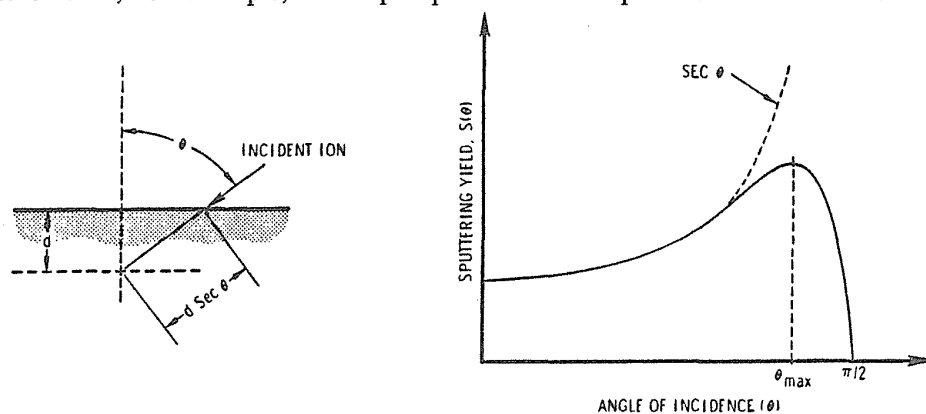


Fig. 9 Schematic diagram showing variation of sputtering yield with ion angle of incidence.

Table 2. SPUTTERING YIELDS FOR METALS IN ARGON IN ATOMS /ION

Target	At.Wt. /Dens.	100 eV	300 eV	600 eV	1000 eV	2000 eV
Al	10	0.11	0.65	1.2	1.9	2.0
Au	10.2	0.32	1.65	2.8	3.6	5.6
Cu	7.09	0.5	1.6	2.3	3.2	4.3
Ni	6.6	0.28	0.95	1.5	2.1	
Pt	9.12	0.2	0.75	1.6		
Si	12.05	0.07	0.31	0.5	0.6	0.9
Ta	10.9	0.1	0.4	0.6	0.9	
Ti	10.62	0.08	0.33	0.41	0.7	
W	14.06	0.12	0.41	0.75		

deposition of multilayer films or multi-component films much more controllable by sputtering. We discuss the details of sputtering from multi-component targets in the section on *Process Considerations in Sputter Deposition*. Second, since the bombarding ions are by no means monoenergetic in glow discharge sputtering, it is not necessarily valid to use the sputtering yield values for pure metals when alloys, compounds, or mixtures are being sputtered. The tabulations of sputter yields, however, are useful for obtaining rough indications of deposition or etch rates of various materials.

Selection Criteria for Process Conditions and Sputter Gas

The information gleaned from sputtering yields and the physics of sputtering can also be usefully applied toward an understanding of how process conditions and materials are selected for sputtering including: a) type of sputtering gas; b) pressure range of operation; and c) electrical conditions for the glow discharge^{4,15}. That is, in pure physical (as opposed to reactive

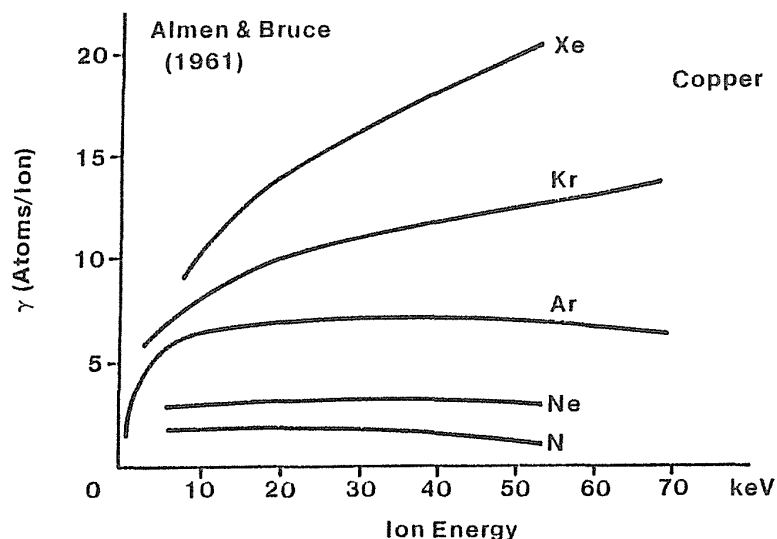


Fig. 10 Sputtering yields of the noble gases on copper, as a function of energy⁵⁵.

sputtering) it is important that the ions or atoms of the sputtering gas not react with the growing film. This limits the selection of sputtering species to the noble gases. Furthermore, argon is virtually the unanimous choice, since it is easily available, is less costly than xenon or krypton, and still gives adequate sputtering yields. The *pressure range of operation* is set by the requirements of the glow discharge (lower limit ~2-3 mtorr for magnetron sputtering) and the scattering of sputtered atoms by the sputtering gas (upper limit 100 mtorr). In addition, a desired goal of sputter deposition is to obtain maximum deposition rates. So *electrical conditions* are selected to give a maximum sputter yield per unit energy. That is, as energy is increased, each incremental energy addition gives a progressively smaller incremental sputtering yield increase. This occurs because higher energy ions implant themselves, and thus end up dissipating a greater proportion of their energy via non-sputtering processes. The most efficient ion energies for sputtering are typically obtained for electrode voltages of several hundred volts.

In general, the higher the current at the cathode, the higher is the deposition rate, since more ions are striking the cathode (and thus are causing more sputtering). The product of the cathode current and the electrode voltage gives the input power of the sputtering process. In magnetron sputtering, cathode current densities of 10-100 mA/cm² at a few hundred volts are typical.

From the foregoing discussion on the mechanism of sputtering, it is also reasonable to surmise that sputtering is a highly inefficient process. This is true, and in fact, ~70% of the energy consumed during the sputtering process is dissipated as heat in the target, and ~25% by emission of secondary electrons and photons by the target. The target heating can raise target temperatures to levels capable of damaging the target, associated vacuum components, or the bonding of the target and the backing electrode. Cooling of the target with water, or other suitable liquids is typically used to maintain low target temperatures.

Secondary Electron Production for Sustaining the Discharge

Near the outset of the discussion on glow-discharges, it was also observed that the glow-discharge must be continuously provided with free electrons to keep it self-sustaining. In most dc sputtering systems, the source of such electrons is secondary electron emission from the target. An important mechanism for such secondary electron emission is Auger emission, although other emission mechanisms are also responsible for generating secondary electrons. The *Auger emission* process occurs according to the following sequence of events (Fig. 11): when a positive ion comes close to the target surface it appears as a potential-well of 15.67 eV to the free electrons of the target. The target electrons require a minimum of energy, $q\Phi$, to escape from the target (where Φ is the work function of the target material, and $q\Phi$ is typically 3-5 eV). Thus, some of the target electrons can tunnel into the Ar potential-well and escape the target. The energy difference between 15.67 eV and the minimum escape energy is released in the form of a photon. If this photon (e.g. of energy 15.67 eV - 5 eV = 10.67 eV), is absorbed by another target electron near the surface, this electron may then possess enough energy to be emitted from the target (i.e. the Auger electron). This sequence of events is however, rather improbable. As a result, several ion bombardment events must occur at the cathode in order for a single secondary Auger electron to be emitted. The secondary electron yield per bombarding ion, γ_i , has been measured to be ~0.1 for metal targets, but is considerably higher for dielectric targets.

Besides providing a source of electrons to sustain the discharge, electron emission is also important to the sputtering process in other ways. First, ions bombarding the cathode are neutralized. Thus, it is highly probable that each ion that closely approaches the target will extract an electron from the target, and return to the discharge as a neutral atom. Second, the

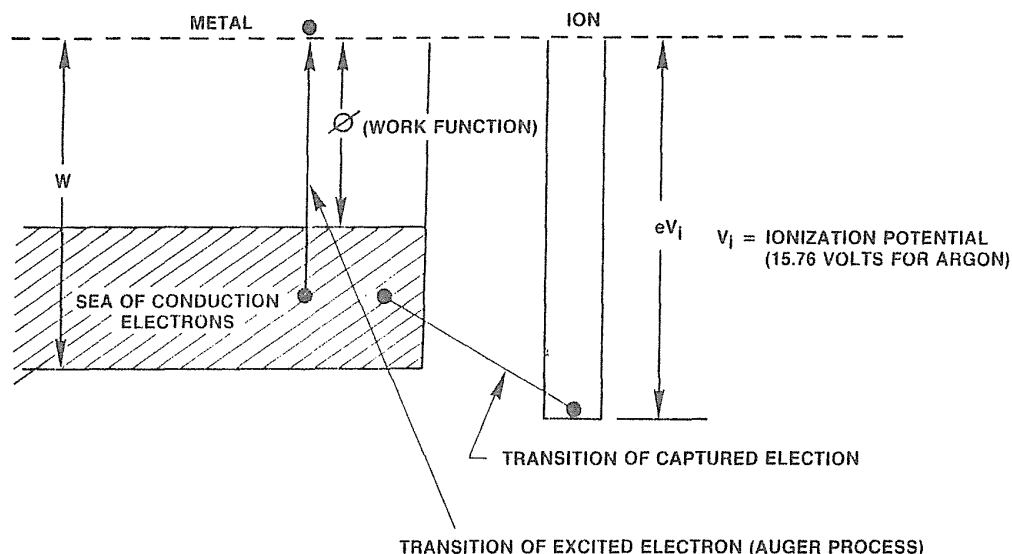


Fig. 11 Potential energy diagram for ion approaching a metal target. Courtesy of MRC.

total target current, I , is the sum of the ion flux striking the target, I_i , and the secondary electron current leaving the electrode, I_e . Since γ_i is larger for dielectric materials, their I_e is also larger. This implies that for the same cathode current, I , dielectrics will sputter more slowly than metals. That is, in dielectric sputtering a larger fraction of I is due to electron emission, and thus for equal values of I , a smaller ion flux is striking the dielectric target.

Sputter Deposited Film Growth

Upon being ejected from the target surface, sputtered atoms have velocities of $3\text{--}6 \times 10^5$ cm/sec and energies of 10–40 eV. It is desirable that as many of these sputtered atoms as possible be deposited upon the substrates and form the specified thin film. To accomplish this goal, the target and wafers are closely spaced, and target-to-wafer spacings of 5–10 cm are typical. The mean free path, λ , of such sputtered atoms at typical sputter pressures is less than 5–10 cm (e.g. at 5 mtorr, $\lambda \cong 1$ cm). Thus, it is likely that the sputtered atoms will suffer collisions with the sputter gas atoms before reaching the substrate (Fig. 12). The sputtered atoms may therefore: a) arrive at the substrate with reduced energy ($\sim 1\text{--}2$ eV); b) be backscattered to the target or the chamber walls; or c) lose enough energy so that they are thereafter transported by diffusion in the same manner as neutral sputter gas atoms. As a result of these events during the transport of sputtered atoms to the substrate, we can see how that sputtering gas pressure can alter various deposition parameters (such as deposition rate).

The formation and growth of the thin film on the substrate proceeds according to the general discussion on thin film formation given in Chap. 4. Therefore, we restrict our discussion to the events that uniquely impact the formation and growth of glow-discharge sputtered films.

The substrate surface on which we desire to deposit a film of the sputtered target material, is also subjected to impingement by many species during this process. The sputtered atoms arrive and condense onto the substrate. For a deposition rate of $200\text{\AA}/\text{min}$, a monolayer of deposited film will form approximately every second (assuming the size of a typical atom is $\sim 3\text{\AA}$). For this case, and even for much higher deposition rates of Al (e.g. $6200\text{\AA}/\text{min}$) the heat of

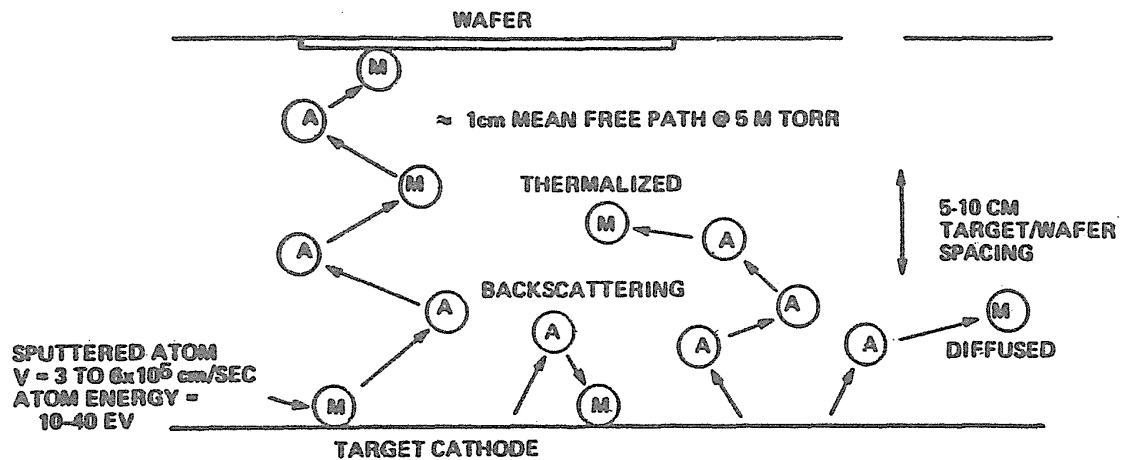


Fig. 12 Gas scattering events.

condensation is not necessarily the most important source of substrate heating.

Species that Strike the Substrate During Film Deposition

In addition to the sputtered atoms, the substrate is also struck by many other species (Fig. 13), the most important being: a) *fast neutral sputter gas atoms*, which retain significant energy after having struck and recoiled from the cathode. As they impinge upon the substrate, some may embed themselves in the growing film; b) *negative ions*, formed near the cathode surface by the reaction of secondary electrons and impurity gas atoms, such as O and N. These can acquire substantial energy from the Crookes dark space electric field, and thus also strike the substrate with appreciable energy; c) *high energy electrons*, which are accelerated across the Crookes dark space, and then impinge on the substrates. (In dc diode and rf diode sputtering

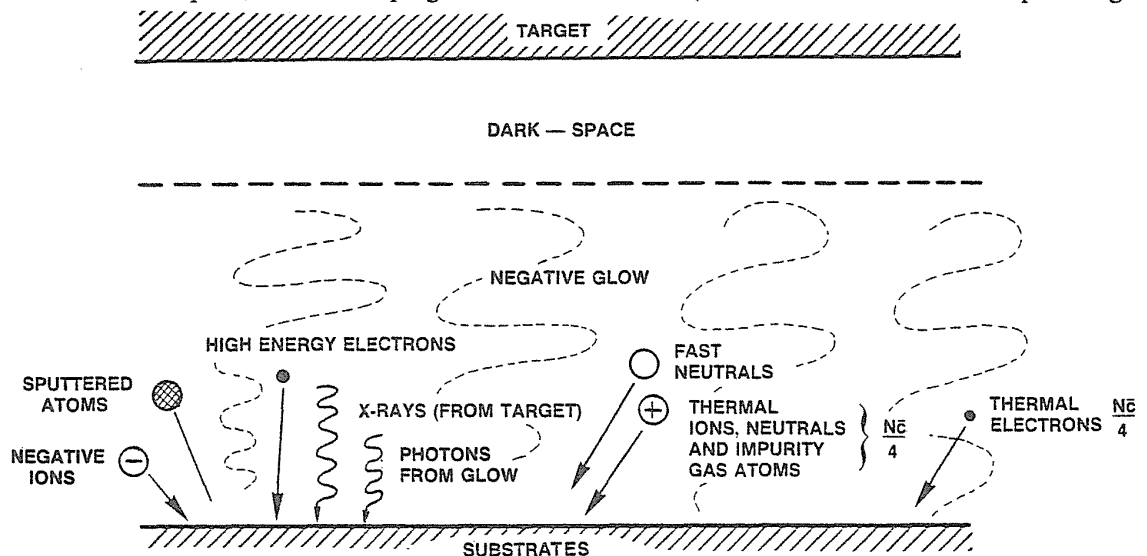


Fig. 13 Species arriving at the substrate in a sputtering system.

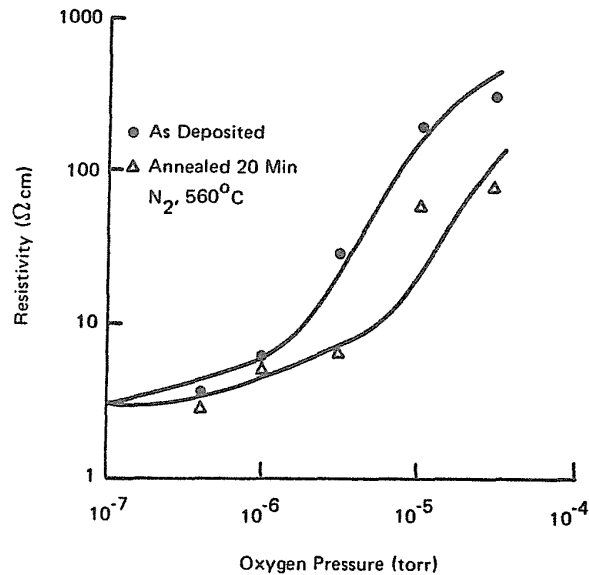


Fig. 14 Room temperature resistivity vs oxygen pressure during evaporation of 5000 Å Al films at 200°C and 20 Å/s. Reprinted with permission from TRANSACTIONS OF THE METALLURGICAL SOCIETY, Vol. 242, pp. 205, a publication of the Metallurgical Society, Warrendale, Penn.

they can represent a major source of substrate heating); d) *low energy neutral sputter gas atoms* (Ar), which strike the substrate at a high flux (e.g. at 20 mtorr, the Ar flux is several thousand times greater than the arrival rate of sputtered material). However, the sticking coefficient of low energy neutral Ar atoms is considered to be negligibly small, and thus the only incorporation of Ar atoms into the growing film arises from fast neutral embedment [species (a)]; and e) *contaminants present in the form of residual gases* in the chamber can be incorporated into the growing film, particularly if they are chemically active. For example, if a sputtering system contains oxygen in the partial pressure of 10^{-6} torr, the substrate surface will be struck by $\sim 10^{15}$ oxygen atoms/sec (or 1 monolayer/sec). In Fig. 14⁸ we observe that at O_2 partial pressures of 10^{-6} torr and Al deposition rates of 1,200 Å/min, the resistivity of the Al film has increased significantly due to the oxidation of some of the Al material.

The sources of residual gases can include: a) impure sputtering gas; b) outgassing from wafers/palette (or wafer holder); c) outgassing from chamber walls; and d) leaks. To minimize the presence of residual gases in sputtering, it is advisable to use highly pure sputter gases, and to continually evacuate and refill the sputter chamber to flush any residual gases being introduced through outgassing or leaks. Additional details on the effects of residual gases on sputter deposited films is given in the section on *Sputter Processing Issues*.

Up to this point in our discussion, the glow-discharge and the sputtering phenomena we have been describing, were produced by the application of a *dc voltage* between the electrodes. Sputtering performed with such systems is known as *dc glow-discharge sputtering*. The diode configuration is the simplest glow-discharge based sputtering system, and consequently it is appropriate to consider its characteristics at the outset of the discussion on sputtering. In general, however, dc diode sputtering processes possess severe limitations that render them unsuitable for most VLSI sputtering applications. As a consequence, two other glow-discharge based sputtering modes are used instead to sputter deposit thin films in semiconductor manufacture: a) radio-frequency (rf) sputtering; and b) magnetron sputtering.

Radio-Frequency (RF) Sputtering

One of the drawbacks of dc diode systems is that they cannot be used to sputter insulators (dielectrics). As we shall explain, this is due to the fact that glow-discharges cannot be maintained with a dc voltage if the electrodes are covered with insulating layers. This represents a significant limitation, as there are several important applications which call for the sputtering of insulators, or the maintenance of a continuous discharge in the face of dielectric-covered electrodes, including: a) sputter-deposition of SiO_2 films, which can be deposited as planarizing inter-metallic dielectric layers; b) the *in situ* sputter removal of thin *native-oxide* layers from silicon and aluminum surfaces prior to the deposition of overlying films (i.e. *in situ* implies that sputter etch and deposition are performed sequentially without breaking vacuum); and c) the condition of glow-discharge must be continuously maintained in some dry-etching process chambers that are equipped with electrodes coated with insulating materials.

The claim that a glow-discharge cannot be sustained if an insulator is sputtered using dc voltages is supported by the following argument: When the negatively charged cathode in dc diode systems is bombarded by ions, an electron is stripped from the cathode surface each time an impinging positive ion is neutralized. If the cathode material is a *conductor*, such electrons can be replaced by electrical conduction, and the cathode surface maintains the negative potential required to sustain the discharge. If the material is an *insulator*, the electrons lost from the cathode surface are not replaced, since electrical conduction from the insulator interior to the sputtered surface, is not possible. Therefore, the front surface accumulates a positive charge that increases with time of bombardment. This causes the potential difference (between the cathode sputter surface and the surface of the anode) to decrease (Fig. 15). As soon as it drops below the value needed to sustain the discharge, the discharge extinguishes. In practical glow-discharge configurations, the time for the insulator surface to acquire this charge is $\sim 1\text{-}10\ \mu\text{s}$ (see Prob. 5).

A technique was developed to allow replenishment of such lost electrons to the insulator surface. This involves the application of an ac voltage (rather than a dc voltage) to the electrodes, and sputtering processes based on applying this method are known as *rf sputtering*^{4,15}. As may be expected, however, this solution introduces other complications. That is, in order to achieve a practical sputtering process by the application of ac voltages, the following conditions need to be established: a) the electrons lost from the insulator surface, by the mechanism observed in dc glow-discharge sputtering, must be periodically replenished; b) the glow-discharge must be continuously sustained under ac conditions over the full period of the ac waveform; c) an electric field configuration must be created in the process chamber which allows ions of sufficient energy to bombard and sputter the target insulator; d) sputtering in the process chamber should be

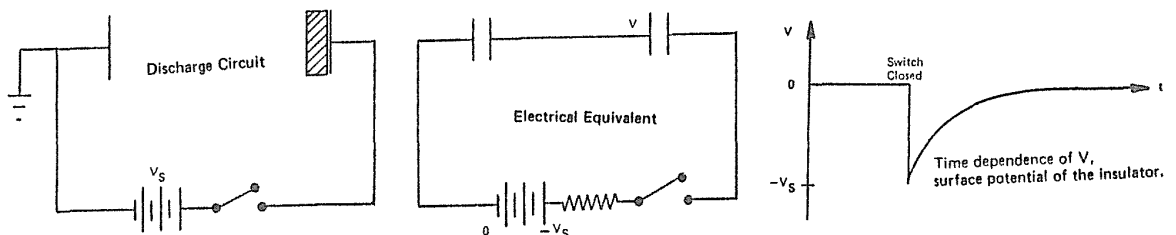


Fig. 15 Surface charging of an insulating cathode. From B. Chapman, *Glow Discharge Processes*, 1980, Copyright © John Wiley & Sons. Reprinted with permission of John Wiley & Sons.

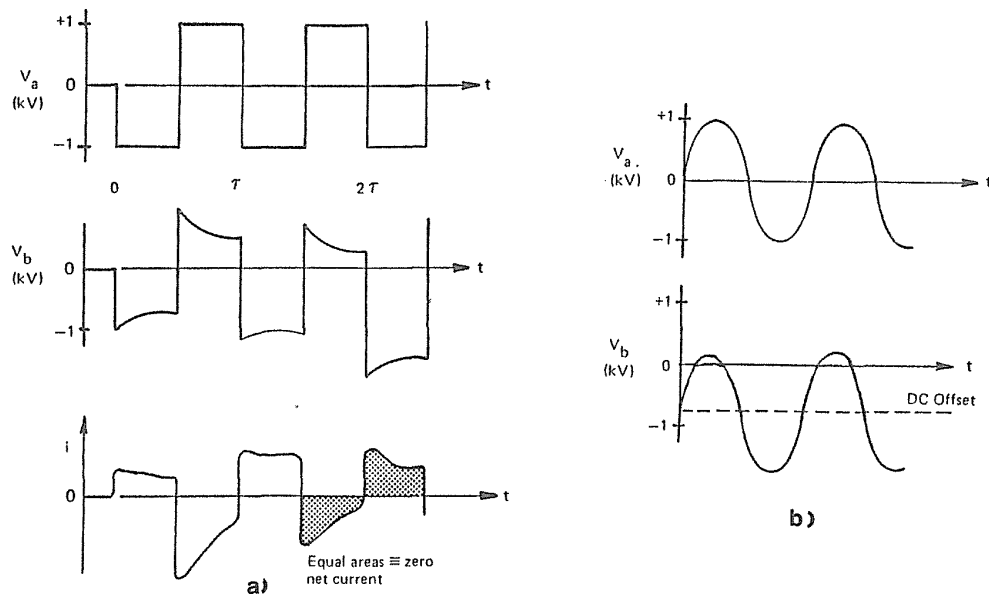


Fig. 16 (a) Voltage and target current waveforms when the circuit of Fig. 15 is square wave excited. (b) Voltage waveforms at generator (V_A) and target (V_B) in a conventionally sinusoidally excited rf discharge. From B. Chapman, *Glow Discharge Processes*, 1980, Copyright © John Wiley & Sons. Reprinted with permission of John Wiley & Sons.

suppressed at all surfaces except the target surface (i.e. sputtering should not occur at the chamber or non-target electrode surfaces); and e) the rf power must be efficiently coupled to the glow-discharge to maximize sputter deposition rates. We will discuss rf sputtering by explaining how each of these requirements is met. The system used to apply an ac signal to the process chamber is shown in Fig. 16. Note that we refer to the two electrodes as A and B, and no longer as cathode and anode, since the signal polarity applied to both electrodes alternates between positive and negative values.

Assume that the rf generator in Fig. 16 produces a signal of alternating polarity with an amplitude, V_0 , that is large enough to cause breakdown of the process chamber gas. When such a signal is applied to the electrodes, positive ions from the discharge are accelerated toward an electrode when it is subjected to the negative-bias portion of the waveform (and electrons during the positive-bias portion). In *steady-state conditions* (to be defined), the positive charge at the target surface (e.g. electrode A) accumulated during the negative part of the cycle, is replaced by impinging electrons during the positive part of the cycle. The net surface charge accumulated by the insulator during each complete cycle of the waveform is zero, and the lost electrons are thus replenished, and condition (a) is satisfied (Fig. 17).

As pointed out earlier, the time required to sufficiently charge the insulator surface during the negative part of the cycle to extinguish the glow-discharge is only 1-10 μ s. Therefore, low frequency ac signals to the electrodes (e.g. 60 Hz) are ineffective at maintaining a continuous glow-discharge. That is, the discharge remains ignited for only a very small fraction of the input signal period (e.g. 1-10 μ s of the 16 ms period of a 60 Hz signal). Thus, in order to satisfy condition (b) above, the charging time of insulator surfaces implies that an ac signal with a minimum frequency of 100 kHz-1 MHz must be applied to the electrodes. In practice, most ac glow-discharges are operated at 13.56 MHz (i.e. glow-discharge sputtering processes and plasma

/RIE dry etch processes). The applied power has a frequency in the radio-frequency range (hence the name *rf sputtering*), and the 13.56 MHz frequency is utilized because it is one of the frequencies designated by international communications authorities at which electromagnetic energy can be radiated without interfering with other radio-transmitted signals.

At this point it is also important to mention that rf excited discharges can be sustained without relying on the emission of secondary electrons from the target. The mechanism that allows rf excited glow-discharges to be thus sustained is not well understood, although several theories have been advanced. One theory postulates that ionization is produced by free electrons oscillating in the very weak rf field that penetrates the plasma. Such oscillations, combined with properly timed elastic collisions between the electron and gas atoms, permit the electrons to gain sufficient energy to cause ionization (despite the weak field). Two important effects are associated with this phenomenon. First, it is observed that rf excited discharges remain sustained at lower minimum pressures than dc discharges (e.g. 10 mtorr versus 40 mtorr). Second, we see that rf excitation provides a mechanism to create glow-discharges for dry etch processes without needing to be concerned about a source of electrons to sustain the discharge.

To meet condition (c) above, an electric-field in front of the target electrode must exist to accelerate the glow-discharge ions to sufficient energy to produce sputtering. Such an electric-field is produced in rf excited systems by a phenomenon known as *self-bias*. To study this phenomenon, let us examine the events that occur when the ac signal is initially applied to the insulating electrode (Fig. 16). At the time the switch is closed ($t = 0$), the electrode surfaces contain no charge. The applied negative bias causes positive ions from the discharge to strike electrode A (an insulator), and to leave behind a positive charge on the surface as electrons are removed. During the positive portion of the cycle, the electrode attracts and collects electrons. The mass of the electrons is much smaller than that of ions, and the electric field accelerates them more rapidly to the electrode surface. Thus, during the two halves of the first ac cycle, many more electrons are initially collected at the electrode than ions. At the end of the first complete period, the electrode surface therefore has a net negative charge. As more cycles transpire, the negative charge continues to build up. Such negative surface charge, however, also has the

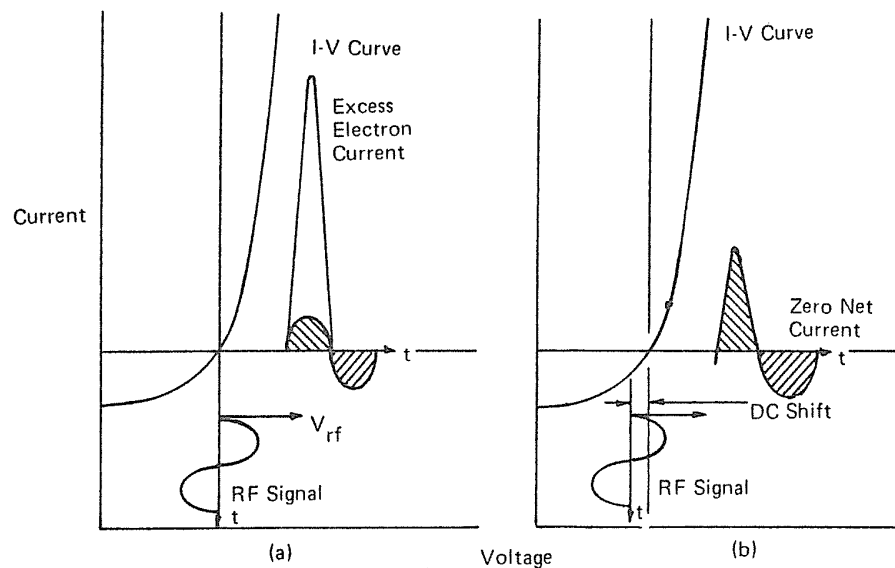


Fig. 17 Self-biasing of a dielectric surface⁵⁶. Reprinted with permission of American Phys. Soc.

effect of repelling some electrons during the positive part of the cycle, and attracting positive ions more strongly during the negative parts. In the steady state, an equal number of positive ions and electrons strike the electrode during each complete signal period. The *average* charge build-up on the electrode which occurred during the first few cycles is negative, and remains constant in value under steady-state conditions. This also results in a negative dc offset voltage between the electrode and the discharge. Such a *self-bias voltage* is almost equal to the peak of the applied voltage (Fig. 16b) of the rf input signal. If the potential difference between the discharge and the self-biased electrode is sufficiently large, ions will be accelerated strongly enough toward the cathode to cause sputtering at the electrode [thus satisfying condition (c)].

Unfortunately, this effect can occur at both electrodes, as well as at any surface in the chamber connected electrically to the rf signal. To restrict the sputtering only to the target surface, the electrode configuration in the system must be altered. First, the non-sputtering electrode is grounded, and this may also be a convenient location for placing the substrate wafers onto which the sputtered film is to be deposited. Next we note that there are voltages V_A and V_B (called *sheath voltages*) occurring between the discharge and electrodes A and B respectively. To restrict sputtering only to the target (e.g. electrode A), it is necessary for sheath voltage V_A to be large, and V_B to be as small as possible. We assume that the electrodes A and B have areas A_A and A_B , respectively.

To see how to establish such sheath voltages, we make use of an expression that describes the relationship between ion flux through the sheath, and the voltage across the sheath (Fig. 18). If a space-charge limited current is assumed, the ion current flux, J , is given by Child-Langmuir equation¹⁰:

$$J = \frac{K V^{3/2}}{\sqrt{m} D^2} \quad (1)$$

where V is the voltage drop across the sheath, D is the dark-space thickness, m is ion mass, and K is a constant. Since the current density of positive ions must be equal at both electrodes, Eq. 1 indicates that:

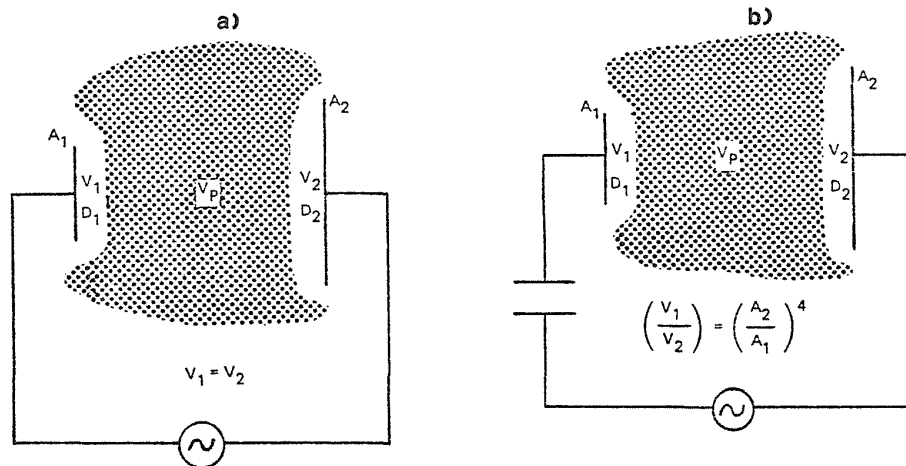


Fig. 18 (a) Voltage distribution with equal area electrodes and no blocking capacitor. (b) Voltage distribution with unequal area electrodes and blocking capacitor¹⁰. Copyright 1970 by International Business Machines Corporation; reprinted with permission.

$$\frac{V_1^{3/2}}{D_1^2} = \frac{V_2^{3/2}}{D_2^2} \quad (2)$$

Since there is a large voltage drop across the dark space, this implies that the dark space is a region of very limited conductivity. Thus, we can model the electrode-dark space-plasma as a capacitor, with capacitance proportional to electrode area and inversely proportional to D :

$$C \propto A / D \quad (3)$$

Now, an rf voltage will divide between two capacitances in series according to:

$$V_A / V_B = C_B / C_A \quad (4)$$

Using Eqs. 3 and 4, we can write:

$$V_A / V_B = (A_B / D_B) (D_A / A_A) \quad (5)$$

and substituting into Eq. 2, we get:

$$V_A / V_B = (A_B / A_A)^4 \quad (6)$$

Thus, the larger dark-space voltage will develop at the electrode having the smaller area. The fourth-power dependence is not observed in real systems (the value of the exponent is more typically determined experimentally to be <2), but the principle of increasing the sheath voltage ratio by controlling the relative electrode areas is valid. In actual sputtering systems, the larger electrode consists of the entire sputtering chamber, including the wafer holder, which has a common electrical ground with the rf power supply. The relatively large area causes a small dark space voltage to exist, and no sputtering takes place from these surfaces. The target material is attached to the smaller electrode, which therefore develops a large dark-space voltage, and can thus experience strong sputtering. In this manner, condition (d) is satisfied.

Since the dark-space voltages V_A and V_B will not be equal if the areas of the electrodes are not equal (and the plasma is a region of equipotential), a dc voltage between the electrodes will exist. If the target is a conductor, a blocking capacitor (Fig. 19) is needed to prevent this self-bias voltage from being grounded through the rf generator. If the target was an ideal

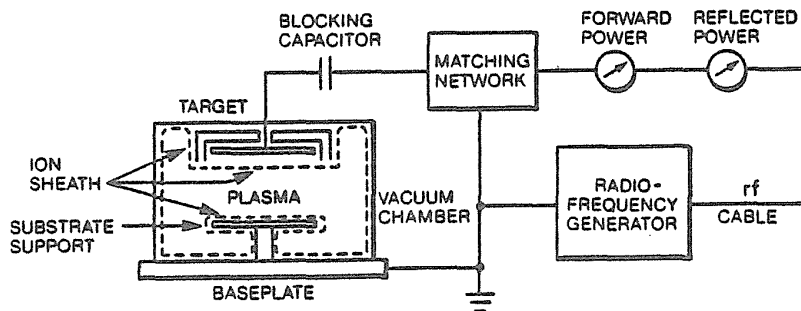


Fig. 19 Radio frequency sputtering system.

insulator, it would not be necessary to use an external *blocking capacitor*. It is common practice however, to design systems with external blocking capacitors to remove any possibility of leakage through or around the edges of the target in the presence of the plasma.

The final requirement (e), that must be satisfied in order to realize an useful rf sputter process, is to be able to couple the maximum power from the rf generator to the discharge. The output impedance Z_o of rf power supplies is designed to be purely resistive (with the value $Z_o = 50 \Omega$), while the discharge has a larger and partially capacitive impedance. Therefore, an *impedance matching network* is required between the generator and discharge chamber (Fig. 19). Most systems use feedback control to tune the network to the generator by automatically maintaining minimum reflected power. This also protects the generator and coupling lines.

Rf diode sputtering systems behave in other respects much like dc diode systems. That is, secondary electrons are still emitted by the target, and subsequently accelerated through the dark space. Most still end up being collected by the grounded electrode, and thus such electrons usually represent a source of substantial substrate heating. In addition, the target is also the source of fast neutral sputter gas atoms, negative ions, and electromagnetic radiation. These species are generated in the same manner as in dc diode systems. Furthermore, rf diode configurations suffer the same inefficiency of secondary electron utilization. That is, since most electrons emitted from the target are collected by the anode, and do not cause ionization, ion production (and consequent ion bombardment of the target) is not significantly greater than in dc diode systems. Thus, for processes that require conductive materials to be deposited at high rates (e.g. aluminum or aluminum alloys), rf diode sputtering is not an optimum process.

Magnetron Sputtering

In both dc and rf diode sputtering, most secondary electrons emitted from the target do not cause ionization events with Ar atoms. They end up being collected by the anode, substrates, etc., where they cause unwanted heating. Since most electrons pass through the discharge region without creating ions, the ionic bombardment and sputtering rate of the target (and the deposition rate on the substrates) is much lower than if more of these electrons were involved in ionizing collisions. Thus, dc diode and rf diode sputtering processes normally exhibit inadequately low deposition rates.

A technique known as *magnetron sputtering* increases the percentage of electrons that cause ionizing collisions, by utilizing magnetic fields to help confine the electrons near the target surface. By using magnetron sputtering, current densities at the target can be increased to 10-100 mA/cm², from about 1 mA/cm² for non-magnetron configurations.

To describe the principle of magnetron configurations, first consider the motion of a charged particle of charge q , mass m , and initial velocity v_o , that is perpendicular to a uniform magnetic field, B , as shown in Fig. 20. The charged particle experiences a magnetic force, $F = q v \times B$, which is perpendicular to both its velocity and the direction of B . If no other forces are exerted on such a particle, it will continuously be acted upon by the force, F , and this will induce a circular motion, with radius, r_g :

$$r_g = (m v) / q B \quad (7)$$

where v is the velocity of the particle.

For electrons and Ar⁺ ions, the equation for r_g can be expressed in terms of the energy, E , of the particles (in eV), and of the magnetic field, B (in gauss), or:

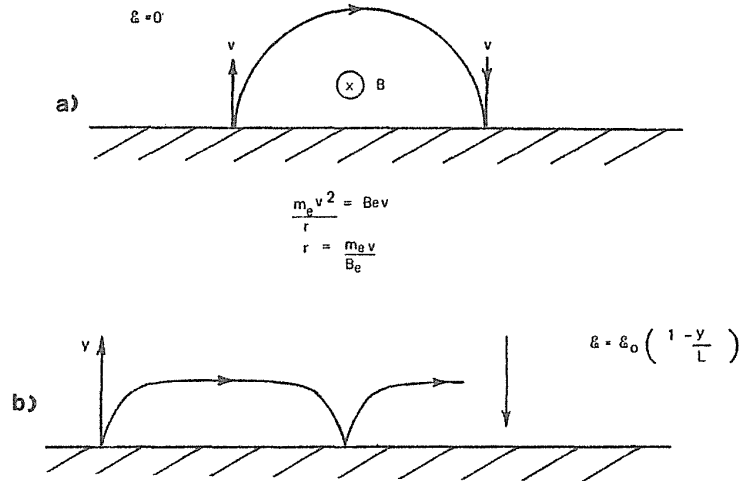


Fig. 20 (a) Motion of an electron in a region of magnetic field B parallel to the surface. (b) Motion of an electron ejected from a surface with velocity v into a region magnetic field B parallel to the surface, with no electric field and, (c) with a linearly decreasing field. From B. Chapman, *Glow Discharge Processes*, 1980, Copyright © John Wiley & Sons. Reprinted with permission of John Wiley & Sons.

$$r_g(\text{electron}) = 3.37 \times [E^{1/2}(\text{eV}) / B(\text{gauss})] \quad (8)$$

$$r_g(\text{Ar}^+) = 9.11 \times 10^2 [E^{1/2}(\text{eV}) / B(\text{gauss})] \quad (9)$$

From these equations, we can see that Ar^+ ions have motion radii which are ~ 300 times larger than electrons for equivalent conditions of B and particle energy. Thus, as an ion moves thorough the region containing the magnetic field, its r_g is so large that it essentially moves in a straight line when crossing the dark space. This illustrates that the direction of electron motion in magnetron discharges is strongly influenced by the magnetic field, while the magnetic field does not significantly change the direction of ions as they cross the dark space.

In the next case, examine the situation of an electron which is emitted from a sputtering target surface. Let there be a magnetic field, B , parallel to the surface, and an electric-field perpendicular to the surface (due to the dark space). Assume the electron is initially at rest (e.g. having just been emitted from the target), and that the magnitude of the electric-field is given by:

$$E = E_0 (1 - y/L) \quad (10)$$

where E_0 is the magnitude at the surface of the target, L is the length of the dark space, and y is the vertical distance above the target. Now the electron will be initially accelerated away from the target in a direction perpendicular to the target surface by the electric field, but simultaneously it will experience a force due to the magnetic field, $F = qv \times B$.

The electron velocity will therefore be altered from a direction perpendicular to the surface. If the magnetic field is strong enough to deflect the electron velocity so that it begins to return to the target surface before it leaves the magnetic field, its motion will be roughly cycloidal as shown in Fig. 20c. That is, as it approaches the target surface after having been deflected, the electron will be *decelerated* by the electric field, and eventually will come to rest (momentarily) at

the target surface. At that point, the next period of the cycloid motion will be initiated, as it is once again repelled by the electric-field. The maximum excursion of the electron (with charge e and mass m) from the target during such motion, $y_{\max}$, is given by:

$$y_{\max} = \frac{1}{B} \left[\frac{2m}{e} (V - V_T) \right]^{1/2} \quad (11)$$

where V_T is the negative target voltage, and V is the potential in the dark space at $y_{\max}$.

The net result is that secondary electrons are trapped near the target surface by the combination of the magnetic and electric fields, and continue to move with cycloid (or *hopping*) motion until they collide with an Ar atom. Even though not every such collision produces an ionization event, many more ions are generated than if the secondary electron escaped the discharge without undergoing any collisions with Ar. The magnitude of the electron velocity *parallel* to the target surface, v_D (also known as the $E \times B$, or *magnetron drift velocity*), is given by:

$$v_D = \frac{10^8 E_{\perp} \text{ (V/cm)}}{|B| \text{ (gauss)}} \quad (12)$$

There are two principal magnetron electrode configuration designs used in VLSI sputtering systems: a) the *planar magnetron*; and b) the *circular magnetron*. Figure 21a shows a variety of

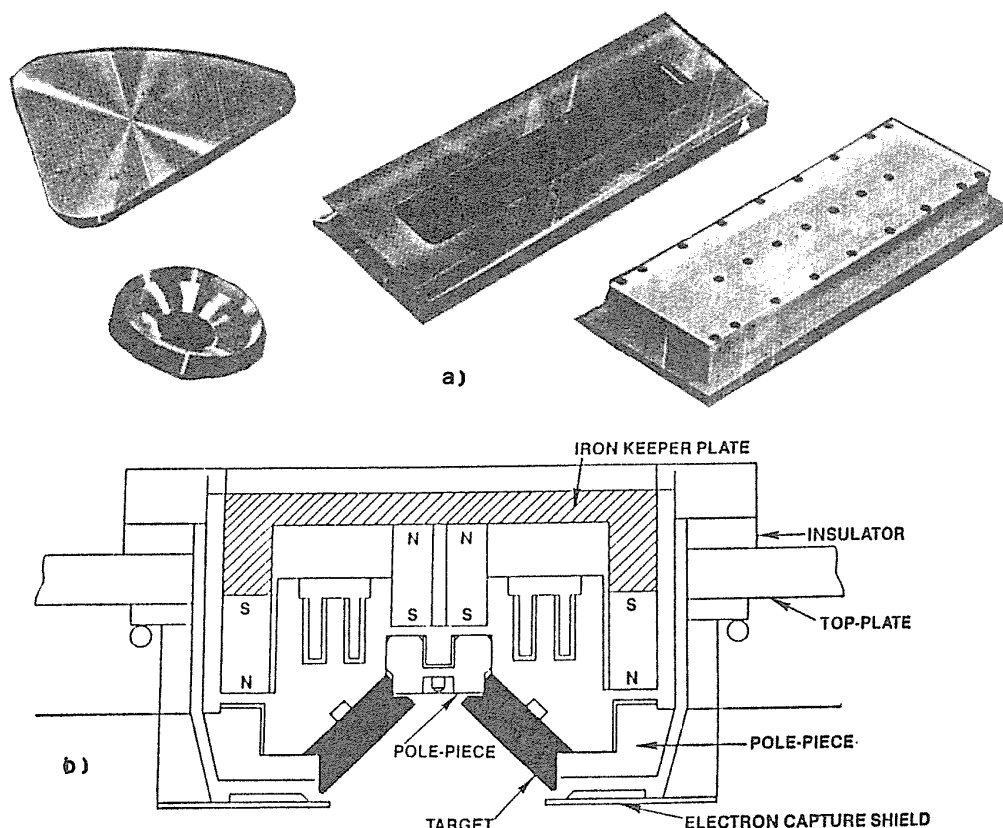


Fig. 21 (a) Sputtering targets. Reprinted with permission of Semiconductor International. (b) Focest[®] sputtering targets for MRC sputtering systems. Courtesy of MRC.

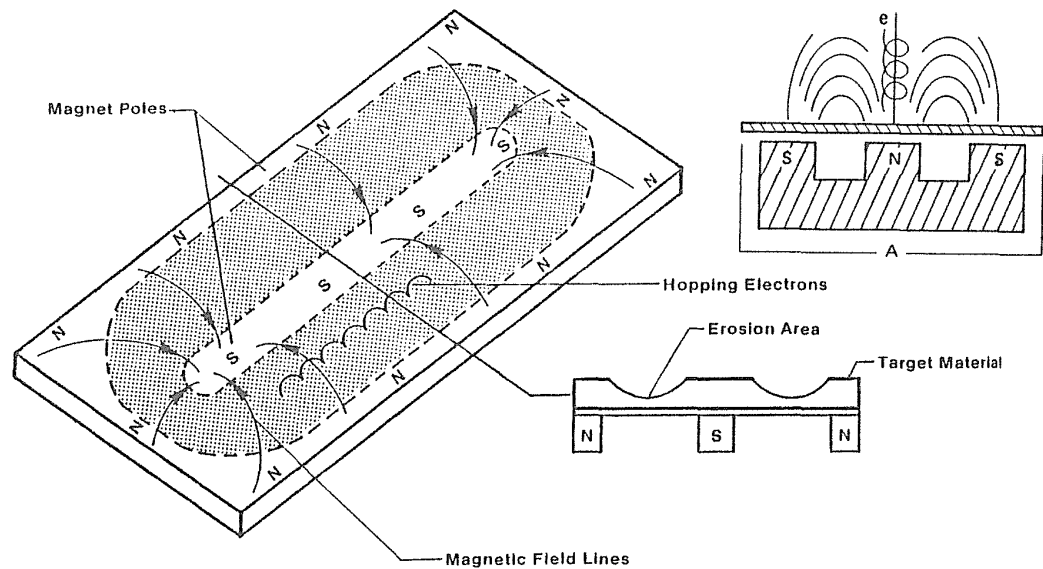


Fig. 22 Schematic drawing of planar magnetron target and magnets.

target shapes used in these systems. Note that the planar magnetron targets can be rectangular or wedge shaped. Some of such rectangular targets (e.g. MRC Focest[®] targets, Fig. 21b) are still thought of as planar targets, although they no longer look very planar. The shape of the planar targets are dictated by system design, although they all basically share the same principle of operation. Therefore, we limit our discussion to the rectangular planar magnetron for purposes of describing the characteristics of all planar magnetrons.

In *planar magnetrons*, the target surface is planar, and the B -field is created by magnets behind the target^{4,5,12,39}. The anode is usually a rod placed along side the cathode. (Apparently the location of the anode relative to the cathode is not critical to effective operation.) During deposition the substrates pass in front of the target. A planar-magnetron target is shown in Fig. 22a, and its cross-section, cut along A-A, to show the magnets and magnetic-field orientation, in Fig. 22b. In examining these illustrations, three things should be noted: a) half-way between the magnet poles, the magnetic field lies parallel to the target face. This is the region where the magnetron drift velocity, v_D occurs; b) the $E \times B$ field that formed in this region closes on itself. Thus, a continuous path that the "hopping" electrons can traverse is established; and c) the plasma density is greatest where $E \times B$ is maximized. This region is called the *race-track* and sputtering is very rapid in the race-track portion of the target. Since the race-track path is continuous, and rectangular planar magnetron targets are normally long and narrow, they form a *two-line sputter deposition source* for wafers that pass in front of the target during deposition.

Figure 22a also shows the hopping motion of the electrons as it follows the race track. Near the center of the track the maximum excursion, y_{max} , is ~ 0.5 cm. The dark-space is also significantly reduced (to about 0.5 mm). Since magnetrons are much more effective in causing secondary electrons to undergo ionization collisions, much higher target currents occur for comparable voltage levels. Thus, magnetron devices have impedances of $\sim 50 \Omega$, as opposed to $40,000 \Omega$ for dc diode devices. Planar magnetron devices can be operated with either dc or rf power supplies.

The particular configuration of *circular magnetrons* used in VLSI sputters systems was

invented by Clarke¹³, and are known as the Sputter Gun[®] (registered trademark of Sloan Associates), and the S-Gun[®] (registered trademark of Varian Associates). Figure 23a shows an example of the target shape used in such magnetrons, and Fig. 23b shows a cross-section of an S-Gun. As in other magnetrons, an intense plasma region is formed near the cathode, due to the $E \times B$ field orientation (Fig. 23b). The anode is concentrically located, and the magnetic field is generated by annular permanent magnets as shown in Fig. 23a. In modern high-rate circular magnetron systems, the substrates are placed close to the cathode (Fig. 23d), and only a single wafer is deposited at a time. This maximizes deposition rates and efficiently collects a large percentage of the sputtered species. Figure 23d also qualitatively illustrates the flux of the sputtered species that are produced in such a circular magnetron. Note that in early systems which used circular magnetrons, the substrates were mounted on a planetary or other movable support system, as discussed in the *Evaporation* section. This also provided an inexpensive vehicle for implementing a sputtering capability, because existing evaporation systems could be retrofitted with an S-Gun.

The hopping motion along the target surface that constrains electrons to the region near the cathode surface of the circular magnetron is shown in Fig. 23b. The target erodes as material is sputtered away as shown in Fig. 23c. Efforts to maintain satisfactory film thickness uniformity across large diameter wafers together with a higher percentage of material utilization from the target, have lead to such modifications in circular target designs as: a) multiple concentric cathodes; and b) non-planar target cathode surfaces.

Bias Sputtering

The surfaces of the substrates during glow-discharge sputtering always acquire a negative potential, albeit usually small, with respect to the plasma. Thus, they are subject to some

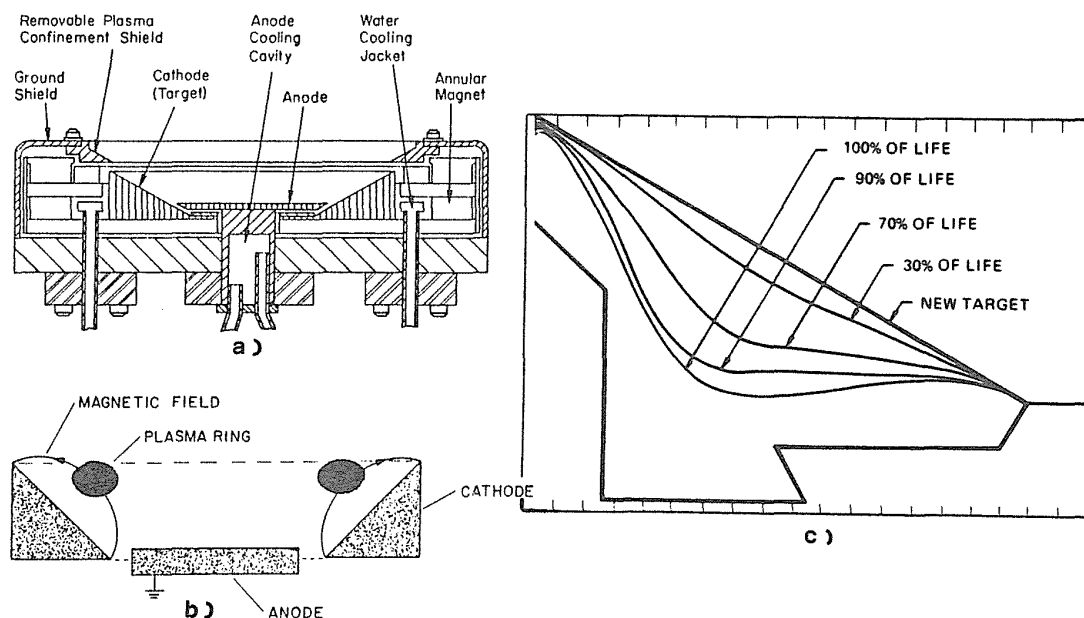


Fig. 23 Conical magnetron target and magnet configuration. Courtesy of Varian Associates.

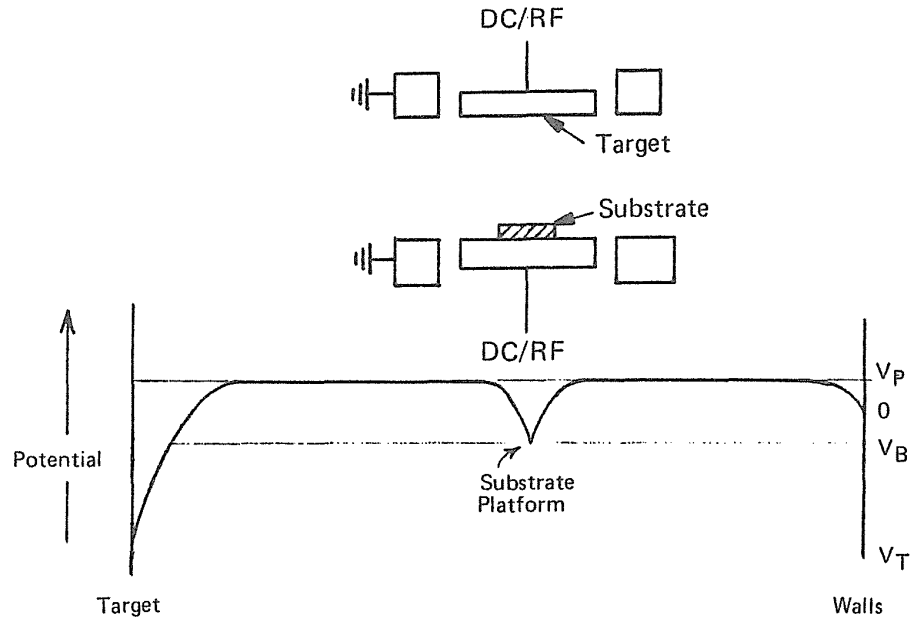


Fig. 24 Potential distribution in bias sputtering systems. From B. Chapman, *Glow Discharge Processes*, 1980 Copyright © John Wiley & Sons. Reprinted by permission of John Wiley & Sons

bombardment by positive ions. This bombardment may cause sputtering of the substrate surface. The value of the potential difference between the plasma and substrate can be left uncontrolled. If, however, the substrates are deliberately given a *negative bias* with respect to the plasma (usually smaller than the negative bias applied to the target), this *bias sputtering* effect can be harnessed to modify some of the properties of the films deposited on the substrates^{4,15}. Most commonly, an rf bias on the substrate is used, with dc or rf power applied to the target.

In Fig. 24a, it is shown how the substrates in such a configuration are electrically isolated from ground, and biased. In Fig. 24b the potential distribution of the configuration is illustrated. Since this arrangement allows the bias voltage on the substrate to be adjusted, this also permits the flux and energy of electrically-charged particles striking the substrates to be varied. In fact, use of bias sputtering enables a large number of film properties to be controlled including gas incorporation, step coverage, stress, reflectivity, grain size, resistivity, surface roughness, hardness, and alloy composition.

As an example, Winters and Kay¹⁶ measured the incorporation of Ar in a growing Ni film as a function of substrate bias (Fig. 25). For low bias voltages less Ar was found in the films, because incoming Ar ions sputtered the previously sorbed Ar, but did not embed themselves in the film. An increase in the bias voltage, however, also raises the kinetic energy of the impinging ions. Thus, they eventually become energetic enough (at ~100 eV) to occasionally be implanted into the growing film. For energies greater than this value, the implantation effect becomes increasingly dominant, and the percentage of incorporated Ar starts to rise again.

The bias voltage can also impact the film properties in several other ways including: a) the incoming ions add energy to the surface ions and thus increase surface migration or chemical reaction rates at the surface; b) if the ions possess sufficient energy (~100 eV), resputtering of the deposited film atoms can occur; c) the incoming ions can damage the surface of the growing film; and d) the growing film can be heated by the ion bombardment. All of these mechanisms

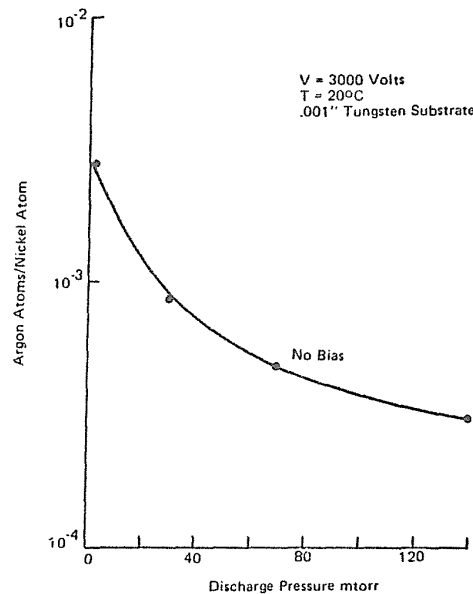


Fig. 25 Argon content in sputtered nickel film as a function of argon discharge pressure¹⁶. Reprinted with permission of the American Physical Society.

can alter the properties of the growing film, often in unexpected ways. References 4,17,18,31,35 describe how bias sputtering has been used to modify a variety of specific film properties.

Sputter Deposition Equipment

A large and stringent set of material properties must be exhibited by VLSI interconnect films. In order to successfully deposit such films by sputtering, complex and sophisticated sputtering systems must be utilized. These are offered commercially in a variety of configuration designs. Each has certain advantages and limitations, and it is up to the user to determine the best equipment type for specific applications. In this section we discuss the various equipment types, after first describing the generic components of a VLSI fabrication sputtering system.

Before discussing the details of sputtering equipment, it is useful to list the most important requirements of VLSI interconnect films, and the equipment used to deposit them. The necessary film properties, and how they are achieved by various sputtering processes, are the subjects of a later section. The requirements placed on sputter deposition equipment will be explored here.

In general, there are some desired qualities shared by all processing equipment including: a) safe operation; b) adequate process throughput; c) compatibility with the required processes to be performed; and d) compatibility with the VLSI manufacturing environment. Let us see what attributes need to be possessed by sputtering equipment to meet goals (b), (c), and (d), as any machine not capable of safe operation would automatically be disqualified.

The *throughput* of a sputtering system depends on such factors as: maximum deposition rates; single-wafer vs. batch operation; pumpdown times; pre-processing cycle times; reliability (i.e. percentage uptime of equipment); and scheduled maintenance requirements (e.g. time between regeneration of cryopumps, or time between target replacement). In general, magnetron sputtering with power supplies capable of supplying high power and optimally designed targets

are utilized to maximize deposition rates.

The *process compatibility* characteristics of a sputter system involve such questions as: a) should the system be flexible or not? (i.e. will it be called upon to deposit a wide variety of materials, multilayers, etc., or will it only be dedicated to a narrowly defined set of sputter depositions?); b) what size wafers can the system handle?; and c) can the system perform all the aspects of the desired processes, such as sputter etching, wafer heating, dc or rf magnetron sputtering, rf diode sputtering, or bias sputtering?

The *compatibility with the VLSI manufacturing environment* addresses the following issues: a) compatibility with clean-rooms (i.e. the systems must be clean, should occupy as small a space as possible in the clean-room, and ought to be serviceable from outside the clean-room); b) capability of interfacing with factory automation-computer systems; and c) compatibility with robotic loading and unloading.

The schematic of a sputtering system is shown in Fig. 26. It consists of the following components: a) sputter chamber, in which reside the electrodes and sputtering targets and possibly shutters; b) pre-processing chamber, which may contain wafer heaters, rf sputter etch electrodes, and also function as a load-lock; c) vacuum pumps; d) power supplies (dc and /or rf); e) sputtering targets; f) sputtering gas supply and flow controllers; g) monitoring equipment (pressure gauges, voltmeters, and residual-gas analyzers); h) wafer holders and handling mechanisms; and i) microcomputer controller. We will present information only on items (a), (b), (c), (d), and (e), as these components operate somewhat differently in sputtering systems than in other equipment. The remaining subsystems, on the other hand, play the same role in sputtering systems as they do in many other semiconductor equipment applications.

The *sputter chamber* (and its associated subcomponents), not only make up the heart of a sputtering system, but each design is also the most unique part of the commercial systems. Therefore we will delay the discussion on sputter chambers until the various system configurations are compared.

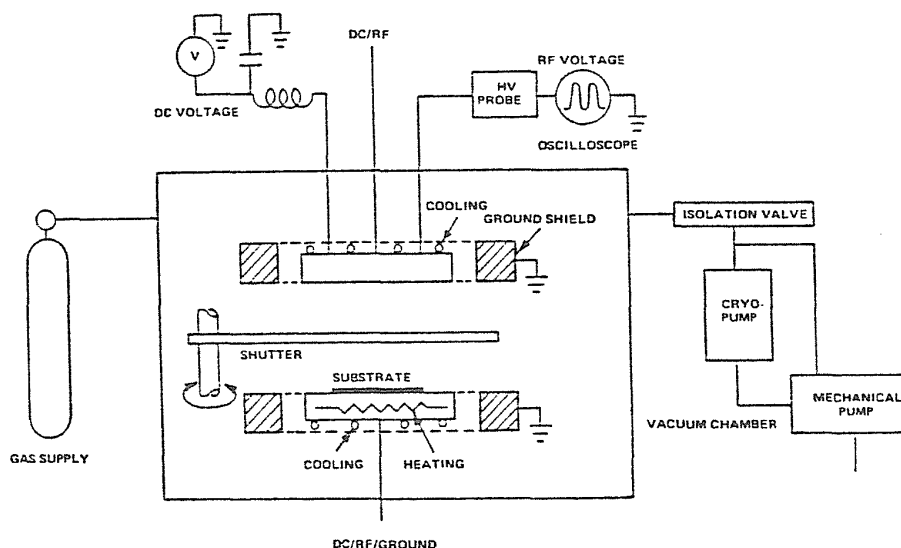


Fig. 26 Schematic drawing showing some of the components of a sputtering system.

The *pre-processing chamber* (or *station*), is normally a chamber into which the wafers are first transferred from the ambient. Several procedures may be conducted in the pre-process chamber (PPC), depending on the system design, including: a) pumpdown of the PPC; b) heating of the wafers; and c) cleaning of the wafer surface by sputter etching or other means (e.g. plasma etching). The purpose of the *pumpdown* is to allow the sputter chamber to be loadlocked (i.e. wafers can be introduced into the sputter chamber without requiring that it be vented to atmosphere). After the deposition is completed, the wafers can be transferred through the same PPC, or another loadlock chamber, and brought out of the system. The sputter chamber itself is normally kept under high vacuum when sputtering is not taking place. *Wafer heating* may be used to accomplish several purposes, including desorption of moisture, etc., from the wafer surfaces, and /or preheating to improve step coverage during deposition. In some systems, however, such step coverage heating may be done in the sputter chamber during deposition.

The *vacuum pumps* are also an important part of the sputtering system. For cleanliness sake, most sputtering equipment manufacturers have opted to use cryopumps to keep the sputtering chamber under high vacuum between times of sputtering¹⁹. This pump is normally also used during the sputter process to continually pump the chamber (at pressures ~ 1 Pa). In order to use high vacuum cryopumps to maintain such medium vacuum pressures, the pump must be throttled, and this reduces its pumping speed. Since the purpose of pumping during a sputter process is to remove evolving gas contaminants (especially moisture) on a continuous basis, the reduction of pumping speed is undesirable. Thus, *Meissner traps*²⁰ (described in Chap. 3) are sometimes placed in sputter chambers to maintain high water vapor pumping speed. Some systems are also offered with *titanium sublimation pumps* for gettering the large volumes of hydrogen evolved in the chamber during sputtering (i.e. from residual moisture on wafers and holders that dissociates into H and O, and from the H_2 absorbed in stainless steel chamber fixtures). This allows the cryopump to be operated for longer periods between regeneration, as saturation with H_2 is usually the condition that mandates pump regeneration²⁰.

The vacuum in the loadlock PPC may be created by a rough pump or turbomolecular pump. Some reports indicate that the loadlock should be pumped to <1 mtorr in order to prevent excess N_2 from being introduced into the sputter chamber from the PPC²⁰. This would require a high vacuum pump to evacuate the loadlock.

The *power supplies* in a sputtering system may be dc or rf. Dc power supplies can be built to supply up to 20 kW of power, whereas rf power supplies are limited to ~ 3 kW. As a result, dc magnetron sputtering can provide higher deposition rates than rf magnetron sputtering, and consequently is the operational mode of choice for high deposition rate processes. Dc power supplies for sputtering, however, must be designed to be capable of withstanding arcs without damage¹². Such arcs are thought to arise from the local dielectric breakdown of native oxides on freshly installed targets, or from other surface regions on which contaminant insulator layers have formed. Conversely, rf sputtering removes such regions as a matter of course, and thus rf supplies are not subjected to arcing. The dc supplies, however, must be designed to handle such local arcing without shutting down or damage, as the regions responsible for such arcing are normally cleaned within minutes after the power is supplied to the system, and arcing then ceases. On the other hand, the supply must be able to sense large arcs caused by such events as metal flaking between the target and ground, and to be able to switch off soon enough to prevent damage to the target. Saturable reactor power supplies are used for dc magnetron applications, as they are tolerable of arcs, and yet can maintain a constant current output for a wide range of loads. When bias sputtering is carried out, a separate supply may be provided, or power from a single

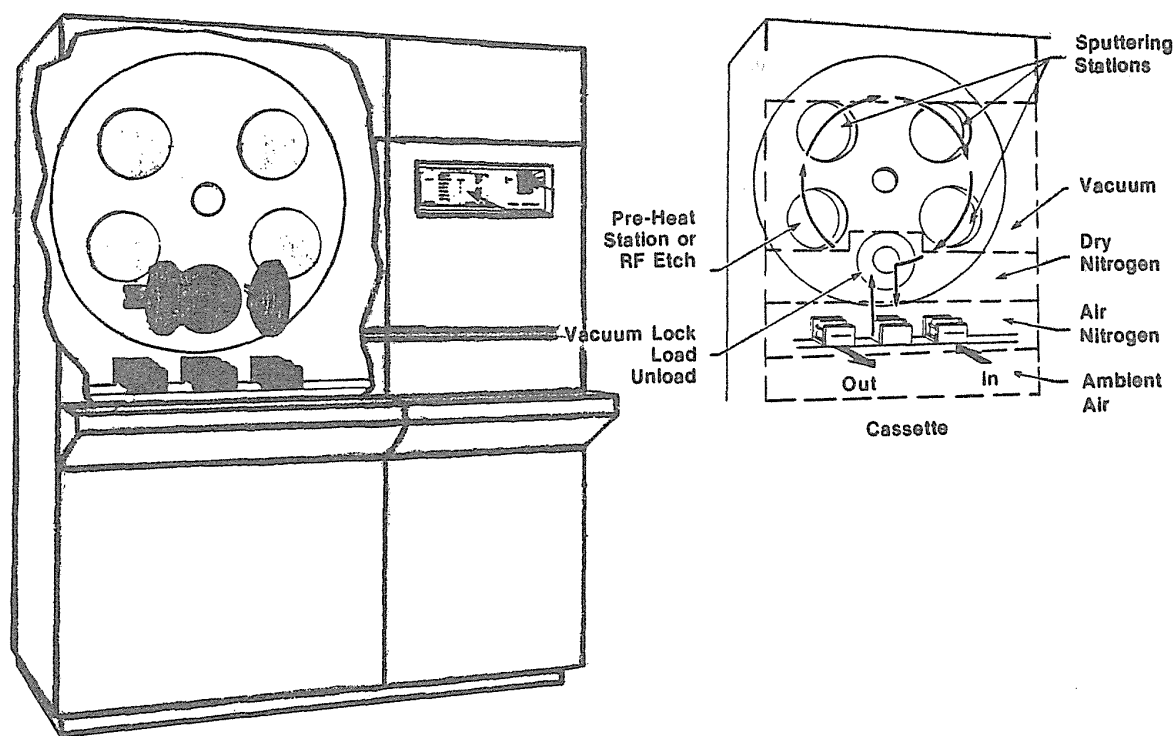


Fig. 27 Static sputtering system, Varian 3180. Courtesy of Varian Associates.

supply may be split and fed to both target and substrate electrodes at the required voltage and phase difference.

The *target* consists of the material that is to be sputter-deposited onto the substrate. Target shapes depend on the material to be deposited and the sputtering system design. Figure 21 shows some of the target shapes in common use²¹. Sizes range from round targets only a few inches in diameter, to rectangular targets several feet long. Targets are mounted to the cathode in such a way that they are in intimate contact with a water-cooled backing plate. Since it is estimated that over 70% of the energy incident on the target goes into heating, targets must be adequately cooled to prevent warpage, deposition rate changes due to thermal restructuring, or even melting. Most metal targets are fabricated from high-purity, vacuum cast materials (e.g. 99.999 - five nines, 99.9995 - five nines five, or 99.9999 - six nines pure, for aluminum targets, as four nines purity is generally unacceptable for semiconductor metallization). Some applications also demand material that is very low in alpha-particle emitting elements (e.g. low thorium and uranium content). Other desirable characteristics of targets include: high percent utilization of the target material; the ability to perform a large number of runs between target replacements; and accurate alloy composition. *Composite targets* consist of two or more metals in unalloyed form with a selected ratio of surface areas mechanically arranged, so that sputtering takes place simultaneously to yield an alloy in the deposited film.

Presputtering of targets is done to clean their surfaces prior to film deposition. Shutters may be used to protect wafers present in the chamber from being deposited with the target surface contaminants, during such target cleaning. Once the target surface is clean, sputter deposition

can be initiated. As discussed in the power supply presentation, arcing may occur at the target surface in dc sputtering until the surface is cleaned. Thus, it is common practice to *condition* freshly installed targets by slowly increasing the applied power, until all the material that causes the arcing has been sputtered away.

Commercial Sputtering System Configurations

The systems commercially offered for VLSI sputtering applications²⁹ differ primarily in the design of the sputter chamber, electrode arrangement, and wafer-target relationship. Note that virtually all systems have load-locked sputter chambers, and offer wafer heating, rf sputter etching, and bias-sputter deposition capabilities. The following are examples which represent most of the variations offered in sputter system design. They are:

a) The *static* sputter configuration (Fig. 27), in which the electrodes are in an S-gun® (or Sputter gun®) configuration, and the wafers (normally smaller in diameter than the S-gun cathode) are placed within 5-10 cm of the target¹³. Only one wafer at a time is sputter deposited from each target, and the wafer and the target are held in fixed positions during the deposition, hence the name, *static deposition*. Note that systems may have more than one sputter station, so that several wafers may be sputtered simultaneously, and multi-layered films can be deposited by moving a wafer between stations. Normally, the wafer is held vertically, and this positioning is known as *side-sputtering*. In such systems, each wafer can be individually heated during deposition. Advanced S-gun, circular magnetron configurations have been designed to allow large diameter wafers (150-200 mm) to be deposited with films possessing $\pm 5\%$ thickness uniformities.

b) The *in-line sputter* configuration (Fig. 28)^{5,11}, in which the wafers travel in a straight

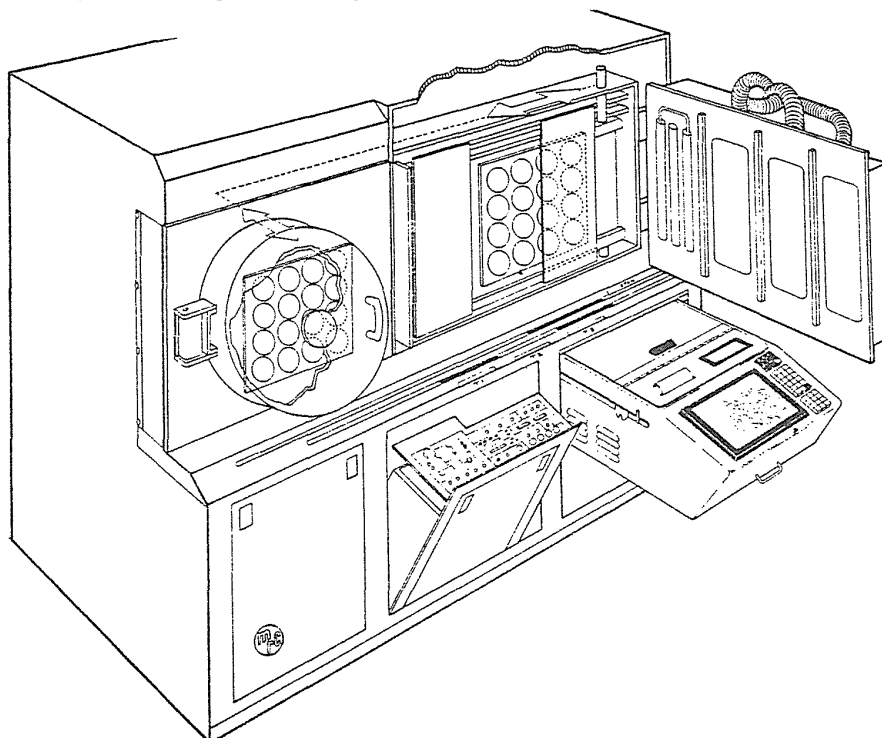


Fig. 28 MRC model 603 in-line side sputtering system. Courtesy of MRC.

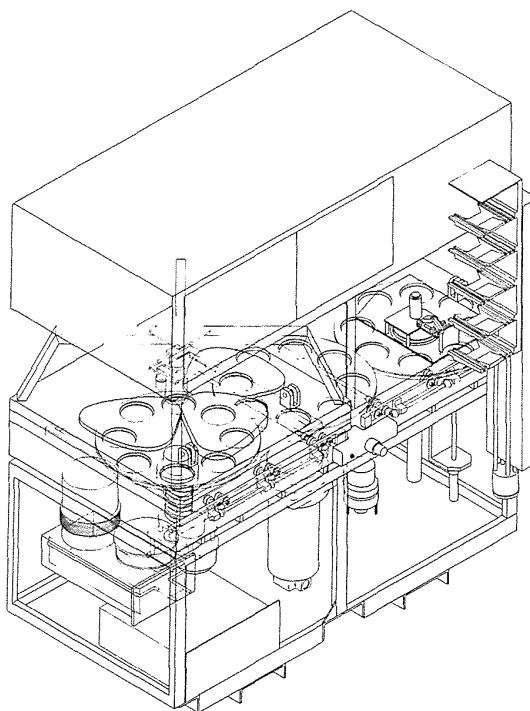


Fig. 29 Planar rotation sputtering system. Courtesy of Gryphon Products.

path and in front of a rectangular shaped planar magnetron target (Fig. 21b & 22). Normally the deposition occurs as the result of a single pass, but multiple passes under the target can also be performed, if desired. In such systems, the deposition rate is determined, and then the transit speed in front of the target is adjusted to yield the desired film thickness. Such systems are batch systems, and the number of wafers per batch is dependent on the wafer diameter. In-line systems can contain more than one sputtering station. This allows several types of materials to be deposited without having to change targets, or to deposit multilayered structures in one vacuum pumpdown. Wafers are again held vertically, and thus side-sputtering is used.

c) In *rotating platter*^{20,23} sputter systems (Fig. 29 & 30a) the wafers make multiple passes in front of the planar magnetron target, as the platter on which they are mounted rotates. Such systems are batch systems, and the size of the batch depends on the wafer diameter, although most systems have a maximum wafer size that can be accommodated. Multiple targets can be used, so that multiple layer films can be easily deposited in a number of various structures (e.g. layered films of Al-Si and Ti, which are reported to prevent hillock formation). The target, typically wedge-shaped as shown in Fig. 21a, can be above or below the wafers. In most rotating platter systems (Fig. 30), the wafers pass below the wafer target (sputter-down mode). For processes in which spalling and flaking result in large particle generation (i.e. Ti:W or silicide process film depositions), this configuration would not be feasible, as the particles would fall onto the wafers. For aluminum depositions, or multi-layer depositions in which underlying

Ti:W layers are immediately covered with Al, the films are highly adherent. Any micrometer size particles that might exist in the sputter environment, are directed by electric fields, and not by gravitational fields. Hence, it is claimed that the spatial orientation of the sputtering process is not relevant, and that sputter-down systems produce no more particles on wafers than do systems which sputter up or sideways. The combination of rotary motion, target design, and heating has been reported to produce enhanced step coverage in Al films with some of these systems.

d) In *rotary drum* sputter systems, wafers are mounted on the surface of a rotating cylinder, and make multiple passes in front of planar magnetron targets as the cylinder or drum rotates. The principle is similar to the in-line systems, except that the motion is rotary rather than linear. If multiple passes before the target are advantageous to a process (compared to a single pass, or vice versa), the rotary versus in-line configurations offer a choice. Side-sputtering is used in most drum type systems.

Process Considerations in Sputter Deposition

The goal of a deposition process for producing an interconnect layer is to create a film having all of the properties required for the VLSI technology that is being fabricated. In this section, we list the desirable properties of an interconnect film and discuss factors that impact the quality of such characteristics. Some of the relevant information was presented earlier in the sputtering discussion, but other practical considerations still need to be addressed.

A deposited interconnect film must satisfy a large number of requirements in order to effectively perform its role in an integrated circuit. (Note that the film properties necessary to meet these requirements must be exhibited by both sputtered and evaporated films.) A "wish list" of some of the most important of these characteristics that depend on the deposition process includes: a) correct nominal thickness; b) thickness uniformity of at least $\pm 5\%$ (across the wafer, and wafer-to-wafer); c) low resistivity; d) uniform resistivity of at least $\pm 5\%$; e) good adhesion to underlying and overlying layers; f) good step coverage (e.g. usually $>50\%$ is desired); g) high electromigration resistance; h) good resistance to hillock formation; i) controllable reflectivity; j) film hardness is controllable to a desired specification, for wire-bonding compatibility; k) the layer can make low-resistance contacts to Si and /or other interconnect layers; l) the films can be

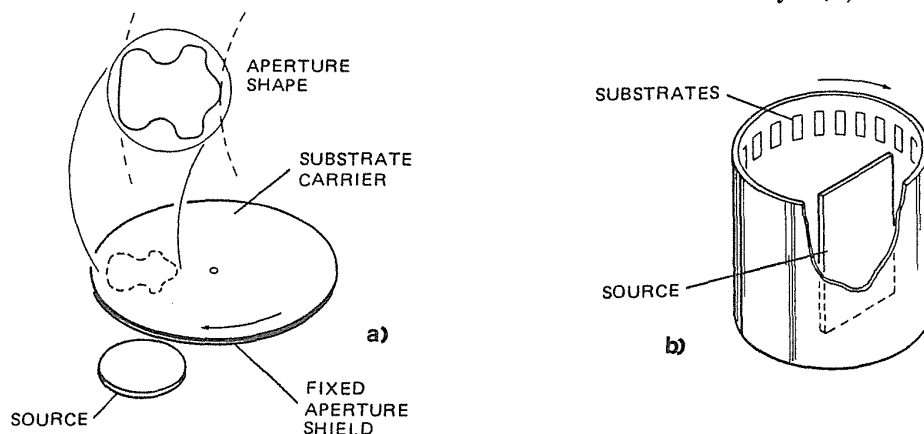


Fig. 30 Planar magnetron deposition with substrate motion: (a) planar rotation with aperture shield. (b) drum rotation³⁹. Reprinted with permission of Academic Press.

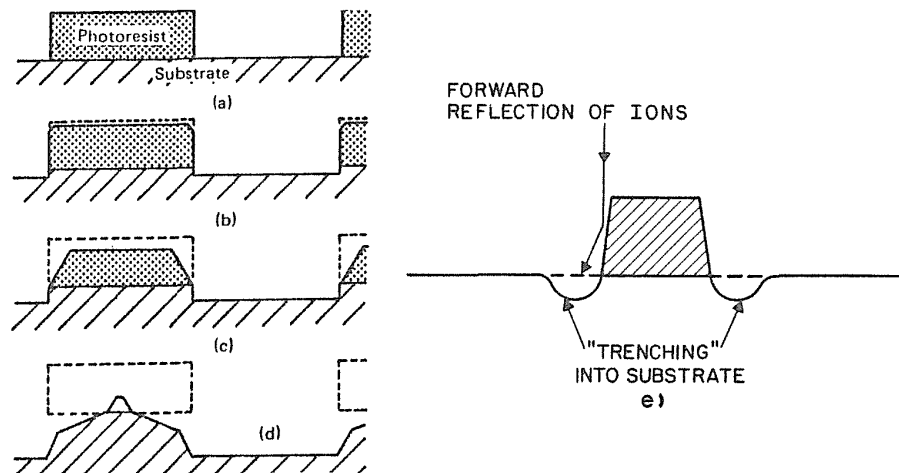


Fig. 31 Faceting results from the dependence of sputter etch rate on the angle of incidence of ions striking the surface. (a) prior to etching, (b) initiation of the facet, (c) facet intersects the substrate surface, (d) substrate is exposed and forms its own facet. (e) Trench formation arises from an excess flux of ions resulting from reflection off the sidewall. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

deposited as an alloy with tightly controlled composition; m) the film may be required to possess a multilayer structure; n) grain sizes in the film can be controlled; o) deposited films are low in alpha-particle emitting elements (uranium and thorium); p) stresses in the deposited film are low; and r) there is a reasonable latitude in the process conditions that effect the desired film properties.

In the following discussion we will focus on the aspects of the sputtering process that impact many of the above properties, especially, alloy composition, step coverage, resistivity, hillocks, electromigration, hardness, stress, and reflectivity. Additional information on stress, adhesion, and resistivity of thin films is found in Chap. 4, and a detailed discussion of electromigration and hillocks is undertaken in Vol. 2 of this text.

Faceting and Trenching

Faceting and trenching are two effects arising from sputtering that can impact the results of sputter etch processes, as well as the reactive-ion etching processes discussed in Chap. 16.

The effect of *faceting* is illustrated in Fig. 31a-d, in which the sidewall of a feature is seen to develop an increasingly larger facet as the sputtering continues. (The term *facet* originated as a description of the *small faces* that are cut from the surface of a jewel.) The faceting effect arises from the fact that sputtering yield is greater from surfaces which are inclined at a non-90° angle to the incoming ions (Fig. 10). The facet usually starts on corners, which always have some rounding, but is also more pronounced in bias-sputtering processes due to the increased electric field at sharp corners. The facet is inclined in the direction of the incident angle corresponding to the angle of maximum sputtering yield. The faceting effect can *directly* alter substrate step profiles if an unprotected substrate is sputter etched. On the other hand, as shown in Fig. 31a-d, if a protective layer (e.g. photoresist) is used during a sputter etch or RIE process, the facet developed in the masking layer can still be *indirectly* transferred into the etched film, if the etching proceeds long enough that the facet intersects the surface.

The phenomenon of *trenching* is illustrated in Fig. 31e. It stems from the enhanced ion

flux at the base of a step due to ion reflection off the side of the step, which causes etching to occur more rapidly there.

Wafer Heating During Sputter Deposition

Heating of the wafers can occur during sputter deposition. This heating may be a natural consequence of the process, or may be deliberately produced by auxiliary heating procedures. In some cases heating produces beneficial effects, especially if it can be controlled, while in other instances the heating can degrade the deposited film properties.

Unintentional heating is primarily caused by the following: a) high-energy electrons striking the substrates; b) the heat-of-condensation of the depositing film (this component is more important in high deposition rate processes); and c) the kinetic energy of the arriving film atoms. In magnetron sputtering, fewer high energy electrons escape from the target region to strike the substrates, and electron capture shields are utilized to suppress this effect even further. Thus, in modern sputtering systems, this heating effect has been significantly reduced. The heat of condensation and kinetic energy of the incoming film atoms will cause only small temperature increases in low-deposition-rate processes, while in high deposition-rate processes (e.g. 1 $\mu\text{m}/\text{min}$ Al depositions), temperature increases of $\sim 50^\circ\text{C}^{24}$ to 100°C^{25} have been reported.

Heating by auxiliary means to improve film properties (e.g. step coverage), is conducted by lamps, backside heating with hot Ar gas, and other techniques. It should be noted that although it is difficult to measure the exact temperature on the wafer surface during deposition, in practice it is possible to reproduce the same heating from run-to-run.

Deposition of Alloy Films

In many sputter deposition applications, it is desired that alloys, rather than pure films be deposited (e.g. Al-alloys, or Ti:W). They may be deposited by co-sputtering from multiple targets, but it is more common that single, multicomponent targets are used. In steady-state sputtering conditions, the elements are sputtered from the target in the same ratio as are present in the alloy. Let us discuss the mechanism associated with such single target depositions that causes the composition of the sputtered film to track that of the target alloy composition^{4,15,21}.

When the surface of a metal alloy is initially exposed to the impinging ions in a sputter process, it will have its nominal composition (e.g. 2at%Cu: 98at%Al). Since Cu has a slightly higher sputter yield than Al (e.g. ~ 2.7 vs. ~ 2 , for 1000 keV Ar ions), the ratio of Cu to Al atoms sputtered would be higher than the ratio of Cu to Al in the target, if 1000 keV ions are used. But this situation would not persist for very long. As the surface gets relatively depleted of Cu, the sputtering rate of Al atoms increases (and that of Cu decreases), until in the steady-state, the material is leaving the surface in the ratio of 2Cu : 98Al. It is useful to use a shutter during the period in which the surface concentration is stabilizing, to prevent deposition of material with non-desired alloy composition onto the substrate.

The composition of the deposited film, however, may not exactly mirror the composition of the target because of other factors. For example, if the alloy constituent atoms differ greatly in mass, the lighter atoms will be more strongly scattered by Ar atoms as they move from the cathode to the substrate. In addition, if bias-sputtering is utilized, resputtering of the deposited film may alter the film composition (often in unexpected ways). Thus, the film composition must be measured for each process condition. Again, once a set of process conditions is fixed, it is possible to obtain reproducible results from run-to-run.

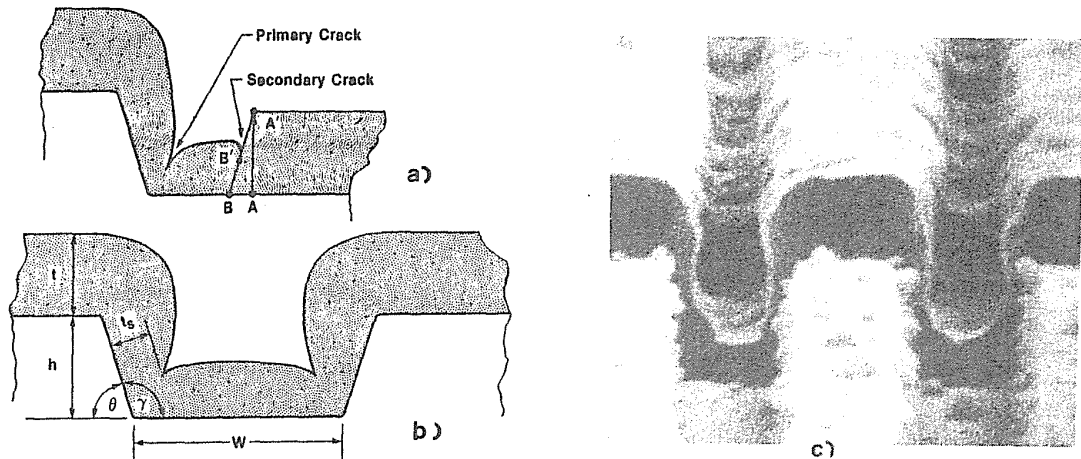


Fig. 32 Computer simulated film growth on a step: (a) Point source planetary system; (b) dc magnetron sputtering system⁴⁷. Reprinted with permission of Solid State Technology, published by Technical Publishing, company of Dun & Bradstreet. (c) Example of poor metal step coverage.

Sputter Deposition Process Control of Step Coverage

In most applications it is desired that thin films maintain a uniform thickness and freedom from cracks or voids. As thin films cross steps that occur on the surface of the underlying substrate, they may suffer unwanted deviations from the ideal, such as thinning or cracking⁴⁷. A measure of how well a film maintains its nominal thickness is expressed by the ratio of the minimum thickness of a film as it crosses a step, t_s , to the nominal thickness of the film on flat regions, t_n (Fig. 32). This film property is referred to as the *step coverage* of the film, and is expressed as the percentage of the nominal thickness that occurs at the step:

$$\text{Step Coverage (\%)} = (t_s / t_n) \times 100\% \quad (13)$$

Step coverage of 100% is ideal, but each process is normally specified by a lesser minimum value that is acceptable for a given application. It is important, however, that the circuit designers understand the actual step coverage value, and derate the maximum allowable current in an interconnect line to reflect the step coverage limitation. The height of the step and the *aspect-ratio* of the feature being covered, also determine the expected step coverage. That is, the greater the height of the step, or the aspect ratio (i.e. the height-to-spacing ratio of two adjacent steps), the more difficult it is to cover the step without thinning of the film, and hence the worse the expected step coverage. Besides the step height and aspect ratio, the step coverage depends on two other factors which are not controllable by the sputtering process: 1) the *shape*; and 2) the *slope*, of the step. In general, the smoother the contour and the smaller the slope of the step, the better the expected coverage. Assuming that the four above factors have been fixed as a result of previous process steps, there are then several conditions of the sputtering process that can be adjusted to improve step coverage, including: a) sputter etching the underlying substrate prior to film deposition, to reduce the slope of surface steps; b) optimization of the target design; c) substrate heating; and d) substrate-bias sputter deposition.

One purpose of *sputter etching* of the substrate surface is to reduce the severe slopes of the steps. This phenomenon makes use of faceting effect described earlier. It should be noted, however, that much more material from the surface layer must be removed to achieve significant

slope-reduction of steps, than is removed during the more common sputter-etch steps that remove thin [$\sim 50\text{\AA}$] native oxides. The utilization of this effect to enhance step-coverage in a three-level metallization process is discussed in Ref. 27.

By optimizing the *shape of the target* and by *controlling the target regions where maximum sputtering occurs*, step coverage can also be enhanced. The details of such target and related system design practices are generally unique to each sputtering system, and some designs are apparently more effective at improving step coverage than others. The general idea is that the extended source configurations of the sputtering systems can offer the potential of such improvements. As progress is continuing to be made in this area, it will be up to users to monitor the claims of enhanced performance by equipment suppliers, and decide for themselves which improvements can best benefit their processes.

Heating the substrate has been shown to improve step coverage²⁰. This effect occurs because the migration of the surface atoms of deposited films increases with substrate temperature (Fig. 33a & b). As a result, the atoms tend to move toward regions where the least amount of material has been deposited, thereby averaging out the film thickness (i.e. the concentration gradient of material favors diffusion toward less populated locations). For aluminum films, the substrates must be heated to $>250^\circ\text{C}$ before significant coverage improvements are observed. It has been postulated that intermittent deposition, or thin $\sim 200\text{\AA}$ thick films (e.g. from multiple passes before the sputter target) is especially effective. That is, during the times that the heated film is not being coated, surface atoms are given the opportunity to migrate. If they are sufficiently mobile, they will equalize their distributions across the surfaces. The optimum temperature and deposition parameters will depend on the particular step topography, and must be determined for each process. An understanding of surface migration phenomena is necessary for developing adequate models of this mechanism. It should also be noted excessive heating during deposition can cause hillock formation in Al films. Thus, the step-coverage heat cycle often represents a compromise temperature. This effect also emphasizes the importance of being able to control the temperature.

Bias-sputtering (introduced earlier) is another technique that has been utilized to increase step coverage of deposited films (Fig. 34)^{23,26}. That is, an rf bias is applied to the wafers, causing them to be bombarded by energetic sputter gas ions (e.g. Ar^+), as the film is being deposited.

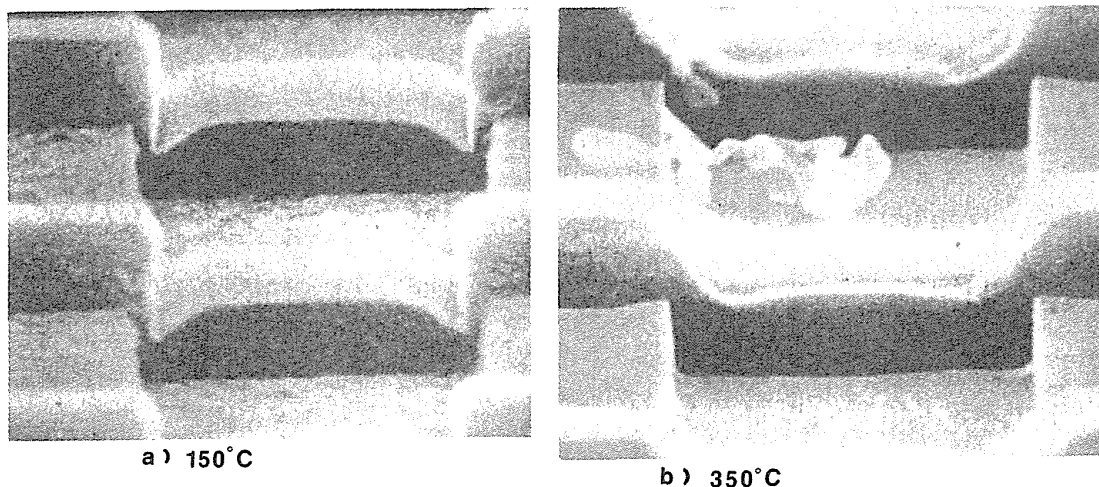


Fig. 33 Effect of heat on step coverage. Courtesy of Varian Associates.

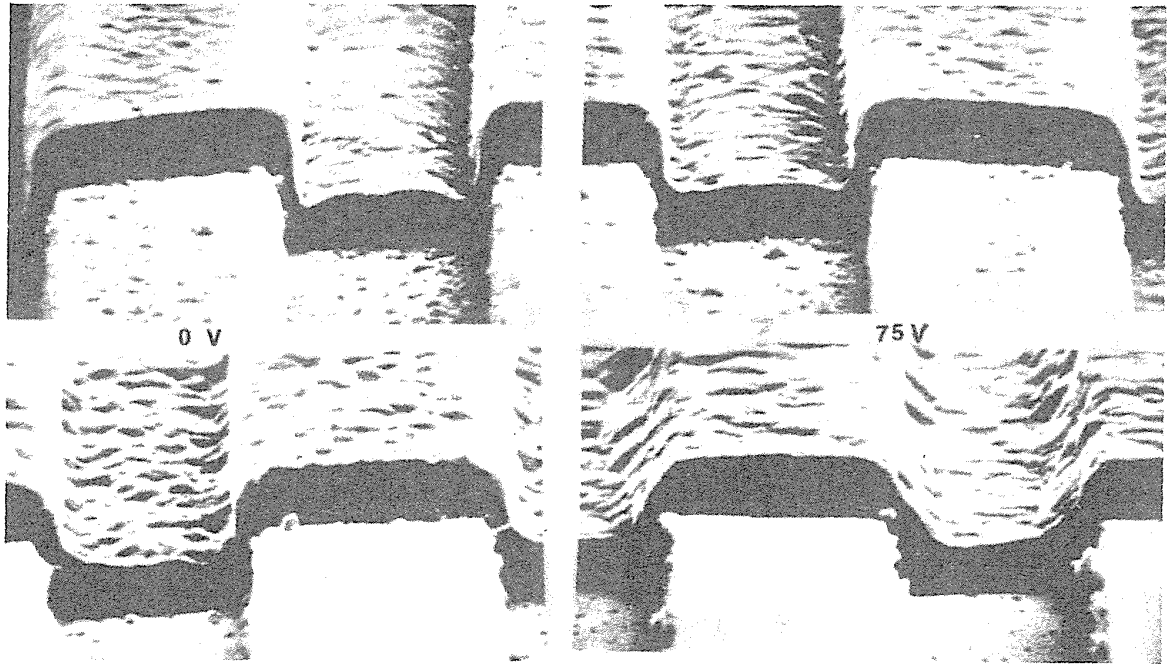


Fig. 34 Effect of different bias voltages on sputter deposited films. Courtesy of MRC.

The applied rf causes the wafers to acquire a negative self-bias, and thereby accelerates ions from the discharge toward their surfaces. The impinging ions transfer energy to surface atoms, and cause them to be transported to the sidewalls of steps, where they accumulate and locally increase the film thickness. Two mechanisms have been suggested as being responsible for such atomic transport: a) the transferred energy from the bombarding ions increases *surface atom migration*, thereby improving step coverage (much as in substrate heating); and b) the transferred ion energy causes *re-sputtering from the surface of the depositing film*³⁵. Since the directions of the atoms emitted in such re-sputtering is thought to occur according to an

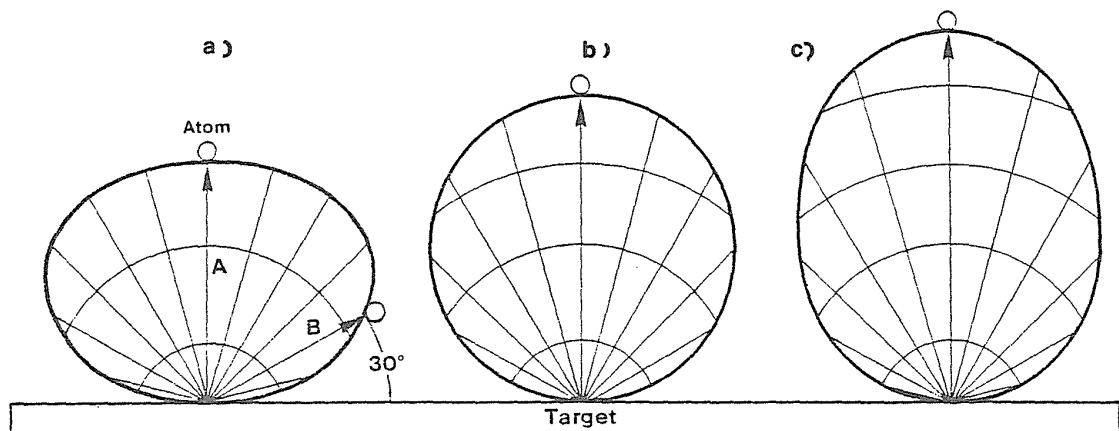


Fig. 35 (a) Under-cosine emission distribution. (b) Cosine emission distribution. (c) Over-cosine emission distribution.

under-cosine distribution (Fig. 35), more atoms will be directed at the sidewalls of steps, where they accumulate. The surface migration model enjoys more support, as it is argued that energies of impinging ions in bias sputtering appear to be too small to cause appreciable resputtering.

Sputter Processes for Various Thin Film Materials

This section discusses process conditions used to sputter deposit a variety of films for VLSI applications, including: a) aluminum and aluminum alloys; b) titanium-tungsten; c) platinum; d) refractory metal silicides; and e) fused silica (also referred to as quartz).

Aluminum and aluminum alloy films of $\sim 3000\text{--}12,000\text{\AA}$ thickness are deposited by dc magnetron sputtering, since high deposition rates are normally required ($3000\text{--}10,000\text{\AA}/\text{min}$). Substrate heating and/or bias-sputtering are frequently used to enhance step coverage. Film reflectance and alloy composition to some degree are also impacted by bias-sputtering conditions. Residual gases (O, N, and H)⁴⁶ can cause deleterious effects in the deposited film. For example, in the discussion on process of film formation during sputter deposition, it was noted that small amounts of O_2 can lead to large resistivity increases in the Al films. In addition, O_2 can produce an increase in the film *hardness* (which can cause difficulty in forming strong wire-bonds to such hardened films). The presence of N_2 has been shown to produce stress in Al films. This leads to cracking and voids, which can contribute to early failures from electromigration²⁸.

It has also been reported²⁰ that an excess quantity of H_2 present in the chamber also increases the propensity of the Al films to form hillocks (Fig. 36). In addition, the pumping of large volumes of H_2 will cause the cryopump to saturate more quickly, requiring increased system down-time to regenerate the pumps.

To minimize problems from residual gas incorporation, some or all of the following procedures are utilized: a) the chamber is pumped to a low base pressure before being back-filled with Ar at the start of the deposition process; b) the wafers and wafer holders are pre-heated in the load-lock chamber to desorb surface moisture; c) high purity Ar gas is used; d) in some systems Ti sublimation pumps are offered for pumping H_2 ; e) residual-gas analyzers are used to monitor the gas composition during the sputter process; f) the chamber is pumped during the process with a high-throughput pump (e.g. cryopump and Meissner trap) so that the residence time of any desorbing contaminant gases is short; and g) high deposition rate processes are used, so that the

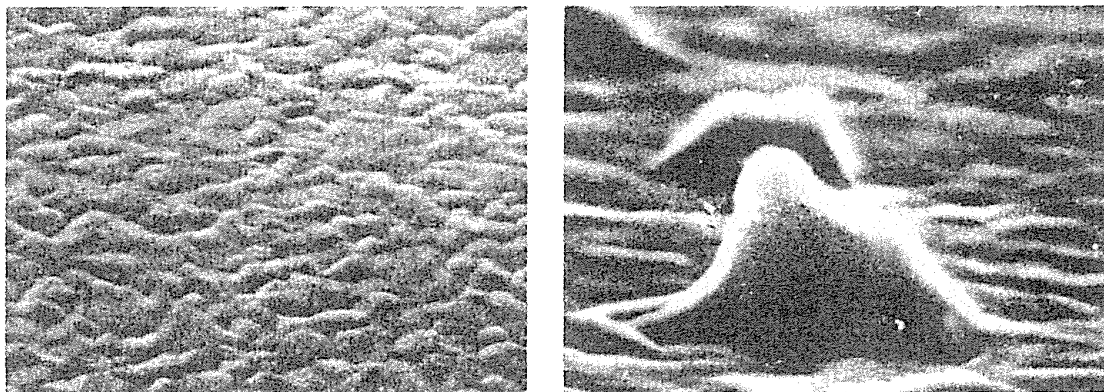


Fig. 36 Comparison of hillock-free and hillock containing films.

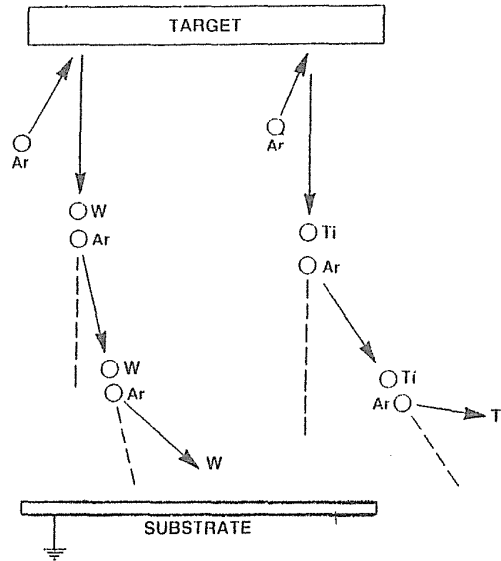


Fig. 37 Titanium-tungsten gas scattering model. Courtesy of MRC.

growing film is exposed to any impinging contaminant gases for the shortest possible time.

Aluminum alloy films are usually deposited from a single compound target, but successful deposition by co-sputtering has also been reported, especially if the alloy material is to be introduced as a series of thin layers^{20,23}. In many cases, an underlying layer (e.g. Ti:W), or overlying layer (e.g. TiSi₂) is applied during the same pumpdown, and in such instances the sputtering system must have the capability of depositing several materials in a single process.

Titanium-tungsten is also deposited using magnetron sputtering (dc or rf). The deposited film contains less Ti than the target alloy (~ 50% less), since the Ti atoms are lighter than W, and are strongly scattered by the Ar gas atoms (Fig. 37). The trajectories of the heavier W atoms, on the other hand, are less perturbed by collisions with Ar. As a result, more of the scattered Ti ends up on the chamber walls, and less on the substrate. (Thus, to get a film of 10% Ti, 90% W, by weight, a target containing ~19% Ti must be used.³⁰) This effect has two important implications: 1) the resistivity of the deposited film depends on the Ti concentration since $\rho_{\text{Ti}} = 48 \mu\Omega\text{-cm}$, and $\rho_{\text{W}} = 5.5 \mu\Omega\text{-cm}$. In some applications the resistivity of the Ti:W film is a critical parameter³¹ (e.g. in fuse links of some memory devices); and 2) the back-scattered Ti atoms form dendrites on the target, which eventually flake off³⁰. A sputter-sideways technique must therefore be used in systems that are dedicated to Ti-W deposition, so that these flakes fall down in the space between the target and substrates (and not on the substrates). It has also been found that the addition of N₂ into the chamber during Ti:W deposition both increases the diffusion-barrier properties of Ti:W films and alters the film resistivity. If N₂ is added (e.g. by using pre-mixed N₂: Ar gases), and the second film cannot tolerate substantial nitrogen partial pressures, a high-vacuum pumping step must be used between sequential deposition steps (e.g. Al following Ti:W). The intrinsic stress and resistivity in Ti:W sputter deposited films can also be controlled by altering the Ar pressure and bias-sputter voltage levels³¹.

Platinum is normally used in VLSI applications to form a PtSi layer in Si /PtSi /Ti:W /Al contact structures (see Vol. 2 for more details on such contact structures), and to form Schottky diodes. The Pt layers required for these uses are very thin (e.g. 500Å). In order to controllably

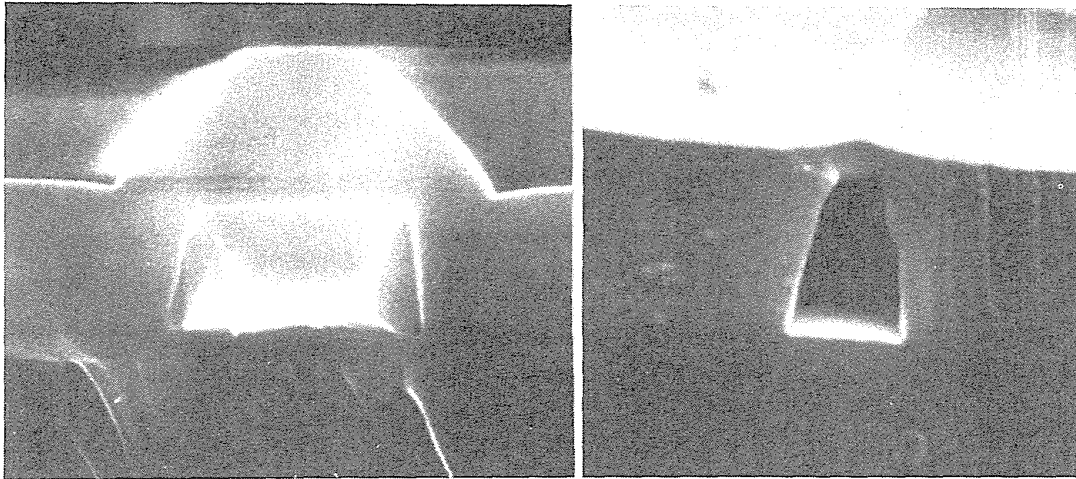


Fig. 38 Partially and fully planarized bias sputtered quartz films. Courtesy of Temescal.

deposit thin layers, a slower deposition method than dc magnetron sputtering is advantageous. Thus, sputtering of Pt is usually carried out using an rf diode or rf magnetron configuration.

Refractory metal silicides (e.g. Me(metal)Si_x) is the desired silicide film, where x for the best quality is determined experimentally, and may range from ~2.0-2.6) are sputter deposited both by co-sputtering^{32,33,50} and by sputtering from a single source (such as a composite or sintered target). In co-sputtered films, high purity targets are used, and calibration runs must be conducted to measure the deposition rate vs. power for each target. Then x is measured in the deposited films, and the procedure is adjusted until desired values of x are obtained. In compound target processes, several targets of different composition must be initially purchased to home-in on the best value of x. There is still some question, however, as to how reproducibly vendors will supply targets so as to maintain the necessary x in the deposited film from target to target. Bias sputtering is also normally used to promote good step coverage. The as-deposited sputtered silicide films are amorphous and possess high resistivities. A high temperature anneal (in Ar) is used to form the silicide and reduce the resistivity (e.g. a 1000°C anneal reduces resistivity by a factor of ~10). A full discussion on refractory metal silicides in VLSI is undertaken in Chap. 11.

SiO₂ is typically sputter deposited to provide dielectric layers for multilevel interconnect structures. The SiO₂ is rf sputtered from a silica glass target (although it is commonly, but incorrectly, referred to as a quartz target), and an rf bias is applied to the substrates as well, hence the name *bias-sputtered quartz*, or BSQ^{34,35,36}. By this procedure, reduced slope steps in the deposited BSQ are achieved. In fact, the surface can be entirely planarized under certain deposition conditions (Fig. 38). The process, however, has several limitations, including: a) the deposition rate is quite slow (e.g. several hours generally are needed to deposit suitably planarized films of adequate thickness); b) the purity of glass targets is still an area of uncertainty; c) the SiO₂ deposits on chamber walls, as well as on the substrate. If these deposits get too thick they will flake off and form particulates. To avoid the problem, the system must be regularly and thoroughly cleaned. This may be a arduous task.

Reactive Sputtering

The introduction of reactive gases into the sputtering chamber during the deposition process

allows material sputtered from the target to combine with such gases to obtain chemical compound films³⁷. In addition, compound targets of some substances can be rf sputtered, and controlled partial pressures of reactive gases can be added to compensate for any loss of gaseous constituents of the compound if the sputtering target dissociates. Although these advantages appear to offer interesting process possibilities, the technique has not found wide application in the silicon microelectronic industry. Two examples of its use, however, do include: a) the addition of N₂ into the Ar ambient during Ti:W depositions, as discussed earlier; and b) in the deposition of the barrier film material, TiN⁵⁴, by the sputtering of a pure Ti target with a sputter gas of Ar mixed with N₂. The complexity of the mechanisms that can take place in the chamber when reactive gases are added to the Ar, and the difficulty in obtaining adequately pure compound targets, have otherwise restricted reactive sputtering to VLSI research laboratories.

Future Trends in Sputter Deposition Processes

It appears that sputter deposition will continue to be the most important PVD process in silicon VLSI fabrication for some time. It is also likely that even more demands will be made on sputter deposition equipment as processing technology proceeds to evolve. The following are some of the challenges to equipment design that will arise: a) wafers will grow larger, and uniform films on such wafers will need to be deposited with high throughput; b) the machines will need to operate at higher levels of cleanliness (i.e. less particulate production); c) greater reliability (e.g. >90% up-time) will be expected; d) the machines will become progressively more automated and controllable from a central factory computer; e) the ability to improve step coverage or even planarize deposited films is an important capability being developed, and this feature will be avidly sought in new sputtering equipment designs^{51,52}; f) alternative techniques to replace (or enhance) sputter etching for *in situ* cleaning of small area openings will be developed⁵³; and g) as multilevel interconnect technologies are developed, more multilayer films (e.g. Ti:W /Al-Cu; or Ti /Al-Si /Ti /Al-Si /Ti) will be utilized. Sputter equipment will be called upon to deposit such complex films with high throughput.

PHYSICAL VAPOR DEPOSITION BY EVAPORATION

Evaporation Basics

Thin films can be deposited by applying heat to the source of film material, thereby causing evaporation³⁸. If the heated source resides in a high-vacuum environment, the vaporized atoms /molecules are likely to strike the substrates (or chamber walls) without suffering any intervening collisions with other gas molecules. The rate of mass lost from the source per unit area per unit time, R , as a result of such evaporation, can be estimated from the Langmuir-Knudsen relation:

$$R = 4.43 \times 10^{-4} (M/T)^{1/2} p_e \quad (14a)$$

$$R = 5.83 \times 10^{-2} (M/T)^{1/2} p_e \quad (14b)$$

where: M is the gram-molecular mass; T is the temperature in °K; and p_e is the vapor pressure in Pa (Eq. 14a), or torr (Eq. 14b).

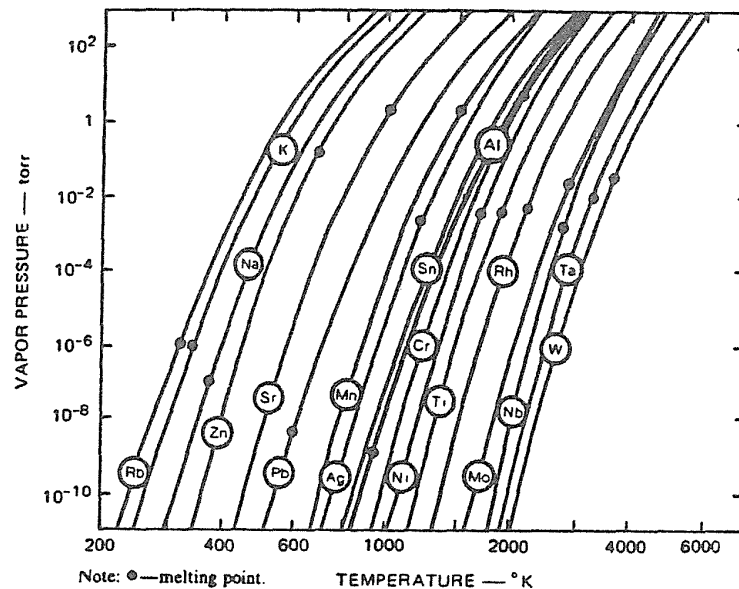


Fig. 39 Vapor pressure of metals commonly deposited by evaporation.

Figure 39 shows the vapor pressure (defined in Chap. 3) of a variety of metals commonly deposited by evaporation. To achieve deposition rates which are high enough for practical manufacturing processes, vapor pressures of >1.5 Pa (>10 mtorr) must be achieved. From Fig. 39 we see that there is a significant variation in the temperatures which must be applied to various materials in order to achieve such vapor pressures (e.g. Al must be heated to 1200°K , while W must be at 3230°K , before their vapor pressures exceed 10 mtorr).

Evaporation has been widely utilized for depositing Al and other metallic films in microelectronic fabrication. Some of the characteristics that were responsible for the widespread use of evaporation include: a) films can be deposited at high rates (e.g. $0.5 \mu\text{m}/\text{min}$. for Al); b) the low energy of the impinging metal atoms onto the substrate (~ 0.1 eV) leaves the substrate surface undamaged; c) due to the high vacuums under which evaporation is performed, films can be deposited with very little residual gas incorporation, and thus the deposited film is about as pure as the source material; and d) unintentional substrate heating is only caused by the heat of condensation of the depositing film, and by heat radiation from the source.

For VLSI applications, however, evaporation suffers from the following limitations: a) accurately controlled alloy compositions are more difficult to achieve with evaporation than with sputtering; b) *in situ* cleaning of the substrate surfaces is not possible with evaporation systems, but is an option in sputter systems (i.e. by performing a sputter-etch step prior to deposition); c) use of extended sources in sputter deposition can improve step coverage vis-a-vis evaporation; and d) x-ray damage, caused by electron-beam evaporation processes, is avoided in sputter deposition.

The successful deposition of thin films onto a wafer surface also implies that the following film characteristics can be achieved: a) the nominal film thickness can be controlled; b) adequate film thickness uniformity exists across the wafer; c) uniform thickness is exhibited when the

film crosses over steps (i.e. good step coverage). In evaporation processes, a different approach is used to achieve each of these three goals. To obtain the desired nominal thickness the rate of mass loss per unit area of source R , as well as data about the directions of evaporated atoms, is needed. Equation 14 can be used to calculate R . Information about the directions of evaporating atoms is more difficult to determine. The flux of atoms leaving a small area *plane source* (Fig. 40a) was theoretically postulated to exhibit a cosine distribution, and this predicts that the mass dM_e collected by an area $d\omega$ in Fig. 40a can be calculated from:

$$dM_e = (M_e / \pi) \cos \phi \, d\omega \quad (15)$$

where, M_e is the total mass emitted by the source. Experimental information which confirmed this model was first obtained by Knudsen, who measured the evaporation from a small area plane source onto the inner surface of a sphere (Fig. 40b). In this experiment, $\cos \vartheta = \cos \phi = r / 2r_0$, for each point on the sphere. Thus, the amount of deposit according to Eq. 15 should be uniform for every point on the sphere, and this was indeed observed. From this data, it would seem that to obtain uniform coating of wafers, it would only be necessary to mount them on an inner surface of a sphere, and evaporate from a source as shown in Fig. 40b.

Unfortunately, actual sources do not have infinitesimally small areas, but are in fact *extended* sources. Thus, the directions of emission do not follow the ideal cosine distribution. In addition, the region directly above high-rate evaporation sources is populated by evaporant atoms with a density large enough to cause them to exhibit *viscous* rather than *molecular* flow. This disturbs the directional distribution even further (Fig. 40c). As a result of these (and other non-ideal emission effects), uniform distribution at every point on a sphere surface does not occur.

The technique developed to achieve maximum uniformity during evaporation, in spite of deviations from the ideal, is to mount the wafers onto a mechanical *planetary* fixture inside the chamber (Fig. 41). During deposition, the entire fixture rotates about the vertical axis of the vacuum chamber, and each wafer is also rotated about a second axis. The combination of rotary motions results in maximum thickness uniformity across a substrate, as well as substrate-to-

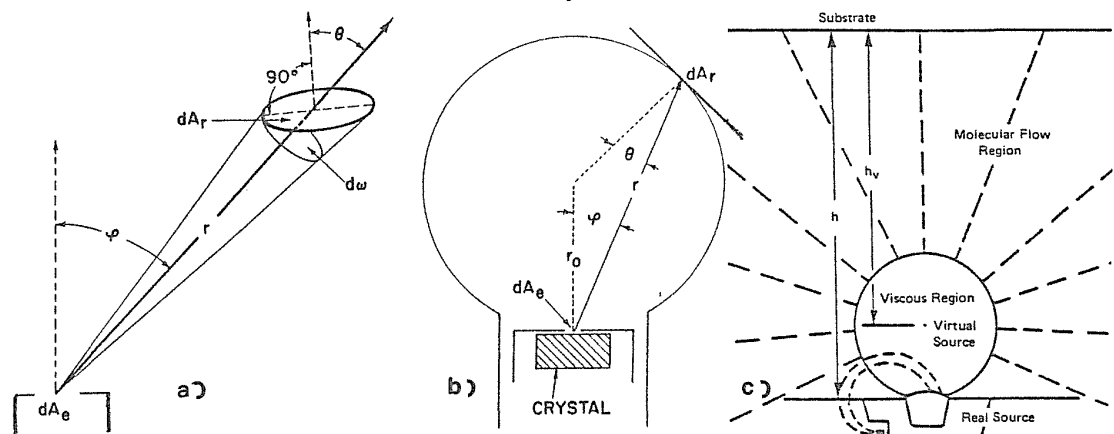


Fig. 40 (a) Surface element dA_r receiving deposit from a small-area source dA_s . (b) Evaporation from a small-area source onto a spherical receiving surface³⁸. From L. Maissel and R. Glang, Eds., *Handbook of Thin Film Technology*, 1970. Reprinted with permission of McGraw-Hill Book Co. (c) Schematic diagram showing regions of viscous flow and molecular flow around an electron beam heated crucible. Courtesy of Temescal.

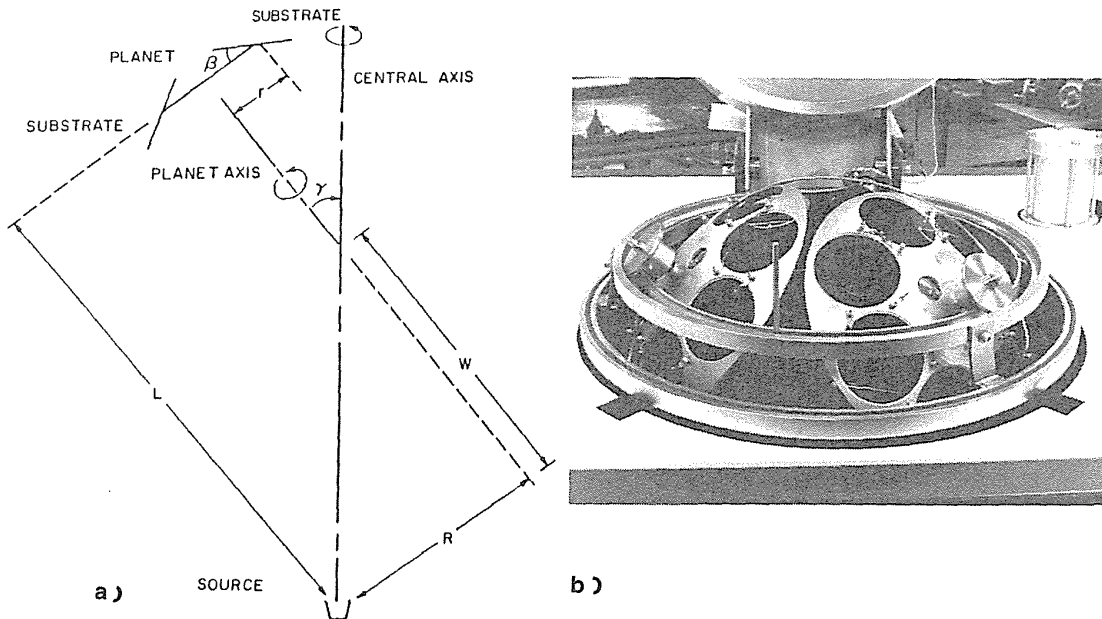


Fig. 41 (a) Schematic of planetary evaporator geometry⁴⁸. Reprinted with permission of the American Physical Society. (b) Photograph of a planetary system. Courtesy of Temescal.

substrate. As a result, adequate control of film thickness and thickness uniformity is achievable.

The problem of maintaining adequate thickness as the film crosses steps, however, is not solved satisfactorily by the planetary⁴⁸. That is, even when a planetary is used, thinning of the film and microcracks can occur, because of the shadowing effect of the step. Substrate heating (as discussed earlier), is one technique used to reduce the severity of this problem.

Evaporation Methods

Evaporation is carried out under high-vacuum conditions. Typically the chamber is pumped down to $\sim 5 \times 10^{-7}$ torr before the evaporation is initiated. At such pressures the mean free path, λ is ~ 100 m. As the source is heated, the pressure rises somewhat as contaminants are desorbed from its surface.

The least complex method of depositing thin films by evaporation is with *resistance-heated* sources. That is, a wire of low vapor pressure metal (e.g. W), is used to support small strips of the metal to be evaporated. The W-wire is then resistively-heated. The metal to be evaporated first melts and wets the heated filament, and evaporation ensues. Although the technique is simple, it has several drawbacks which make other evaporation techniques more useful for microelectronic applications, including: a) evaporation from the filament may contaminate the deposited film; b) refractory metals cannot be deposited because of their high melting points; and c) the small charges limit the ultimate film thickness. As a result, two other techniques have come to be widely adopted for performing evaporation depositions in microelectronic applications: 1) electron-beam evaporation; and 2) inductive-heating evaporation.

Electron-Beam Evaporation

In electron beam evaporation, a stream of electrons is accelerated to high kinetic energy

(5-30 keV)⁴⁰. The beam is directed at the material to be evaporated, and the kinetic energy is transformed to thermal energy upon impact. The electron stream can melt and evaporate any material, provided the beam can supply energy to the evaporant at an equal or greater rate than the rate at which heat is lost, as the material is held at high temperature. Electron beam *guns* (Fig. 42a and b) can be built to supply up to 1200 kW of highly concentrated electron beam power for evaporation applications. Very high film deposition rates can thereby be attained (e.g. 0.5 $\mu\text{m}/\text{min}$), as a result of the high power available.

The beam energy is concentrated on the surface of the target, and thus a molten region can be supported by a cooled structure. In fact, the target material itself provides a solid layer that separates the molten portion of the evaporant material from the wafer-cooled crucible. This eliminates the problem of reaction with, or dissolution of the crucible by the melt, and allows highly pure films to be deposited.

The self-accelerating, 270° beam guns have become the standard gun design. Earlier electron beam guns aimed the electron beam directly at the source, and hence the gun filaments would get coated and short circuited during the deposition cycle. In the 270° guns, a magnetic field simultaneously bends the beams through 270° and focuses them. The electron emission surface is hidden from the evaporating source, and the substrates are also protected from contamination by material evaporating from the heated filament. Movement of the beam (which allows the source to be scanned) is accomplished by electromagnetic deflection. This avoids the problem of nonuniform deposition that would be caused by the formation of a cavity in the molten source if the beam were stationary.

Two problems can arise from use of electron-beam evaporation: 1) At voltages >10 kV, the incident electron beam will cause Al to emit K-shell x-rays. These x-rays cause such damage as the creation of trapped charges in the gate oxides of MOS devices. The silicon devices interconnected by electron-beam Al must therefore be subjected to subsequent annealing to remove such damage, and as a result, restore device characteristics to their pre-metal deposition values; and 2) If excessive power is applied to the source, metal droplets that have been blown out of the source by the expanding metal vapor may be deposited on the substrates.

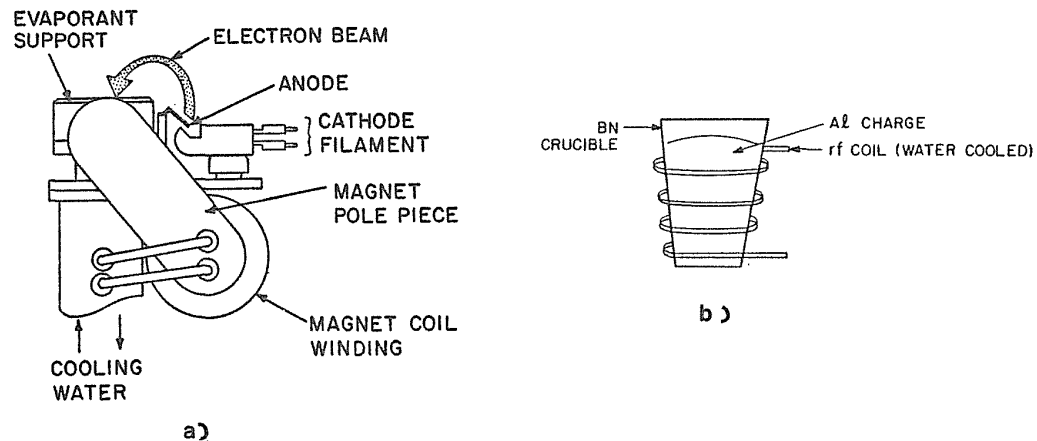


Fig. 42 (a) and (b) Bent beam electron gun. Courtesy of Temescal. (c) Inductively heated evaporation source. The molten Al charge is contained by the BN crucible.

Inductive Heating Evaporation

High-rate evaporation deposition can also be accomplished by heating the source with rf energy. As shown in Fig. 42c, an rf induction heating coil surrounds a crucible containing the evaporation source. The crucible is commonly made of BN, because it is not attacked by molten Al, has excellent heat-shock resistance, and is an insulator that is easy to machine. The main advantage of inductive heating over electron-beam heating is that the wafers are not subject to ionizing radiation. Two of its disadvantages are: a) the mandatory use of a crucible that is in direct contact with the molten evaporant; and b) the increased complexity of rf equipment and process development.

Evaporation Process Considerations

In addition to the information provided on evaporation, some topics related to practical processes need to be addressed including: a) evaporation of alloys; b) evaporation of multilayer films; c) effect of substrate temperature on aluminum film deposition; and) use of shutters.

Evaporation of *alloys* is a complex process, since alloys consist of mixtures of elements that seldom have similar vapor pressures at a given temperature. In addition, *Raoult's Law* states that the vapor pressure of a solution is lower than that of a pure solvent by an amount proportional to the concentration of the solute. Alloy films are therefore evaporated using one of two techniques: a) evaporation from a *single source* composed of an alloy, but not necessarily containing the constituent elements in the same percentage ratio as in the deposited film; and b) simultaneous co-evaporation using *two electron guns and two sources*, with each source containing only one of the alloy constituents.

The *single-source method* is only practical if the vapor pressures are within a factor of 100 of each other at a given temperature. The composition of the film, however, is difficult to control, since as evaporation occurs, the compositions of both source and vapor change continuously. That is, the source becomes richer in the less volatile element. Alloy films of Al-0.5wt%Cu are typically evaporated using a single source of Al-2wt%Cu⁴³.

The *dual-source* method offers the promise of better control, at the price of added system complexity. In addition, the uniformity of deposition across large substrates from two sources is reduced, and the relative power applied to the two sources must be well controlled to insure that the desired evaporation rates are maintained. By using the two-source method, however, it is even possible to co-deposit materials that form neither compounds nor solid solutions. Alloys of Al-Si are normally co-evaporated in two-source systems^{41,42}. On the whole, however, it is significantly more difficult to deposit alloys with highly controlled compositions by either evaporation method than by sputter deposition.

Multilayer films can be deposited in a system containing several sources and a single electron-gun, or several guns can be aimed at multiple crucibles, to evaporate film layers in a planned sequence.

The variation of film thickness of Al films as they *cross steps* can be reduced in evaporation processes by applying heat to the substrates during deposition. For example, a significant improvement in Al film step coverage is observed as the wafer temperature is increased to 350°C during evaporation. The temperature increase is also seen to increase the grain size of the deposited film. As described in the sputtering discussion, substrate heating has the effect of creating greater surface mobility of the deposited material. Film atoms are thereby more likely to migrate toward regions which have received less material deposition. This enhances thickness

uniformity. Infrared lamps are commonly used to provide heat to the wafers.

Shutters are frequently employed in evaporation systems to prevent contaminants adsorbed on the source surface from being incorporated into the deposited films. That is, if the evaporation chamber and source are exposed to ambient conditions in the loading and unloading of wafers, the source surface may adsorb moisture, or form a native oxide layer. When the source is initially heated, such surface contaminants will vaporize (together with the source material). By interposing a shutter between the source and substrates (and postponing deposition by keeping the shutter closed until the source surface has been cleaned), the purity of the deposited film can remain uncompromised. Normally, the gas pressure rises upon initially heating the source and substrates, as a result of the contaminant desorption, and shutter opening is delayed until the chamber pressure returns to an acceptable level.

METAL FILM THICKNESS MEASUREMENT and MONITORING

Metal thickness is usually monitored during evaporation, but is generally deposited without monitoring in sputter deposition. In both cases, the films are normally measured after deposition.

Post-deposition measurements of metal film thickness are most commonly performed either directly with a surface profiling device (known as a *stylus profilometer*), or indirectly by electrical measurement of sheet resistivity⁴⁵. The basic aspects of sheet resistivity measurements are covered in Chap. 4, but it also should be mentioned at this point that the technique offers an important benefit for VLSI fabrication applications. That is, the probes can be stepped over a test wafer to provide contour maps of sheet resistance or thickness. This particular sheet resistance measuring method is discussed in more detail in Chap. 9, in the section dealing with

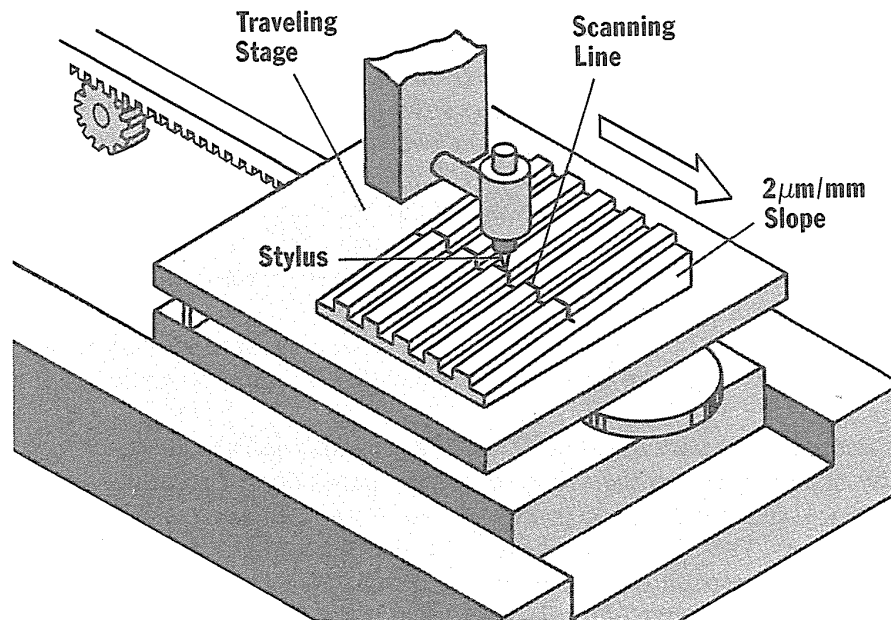


Fig. 43 Schematic drawing of a surface profilometer. Courtesy of Sloan Technology Corporation.

the monitoring of ion implant doses.

In the technique that uses the stylus profilometer, a step in the deposited film is first created, either by masking during deposition, or by a post-deposition etch process. Next, the profiling instrument draws a fine stylus along the surface containing the stepped film (Fig. 43). Whenever the stylus encounters a step, a signal variation (based on differential capacitance or inductance techniques), yields an indication of the step height. The information is displayed on a chart recorder or CRT. Two examples of commercially available instruments are the Sloan Dektak, and the Tencor Alpha-step. Films less than 1000Å thick can be measured with such instruments, but films much thinner than 1000Å are normally measured with sheet resistivity techniques. Vibration, surface roughness, and greater criticality of leveling the profilometer, all make such thin film measurements more difficult with the stylus-type instruments.

Periodic calibration of stylus profilometers is also required, using calibration standards traceable to the National Bureau of Standards. If the instrument is to be used to measure films whose thickness differ greatly from the calibration standard, a reference can be created by etching a step in thermally grown SiO₂, and accurately measuring its height with an ellipsometer.

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PROBLEMS

1. Calculate the mean free path of a sputtered atom in an Ar glow discharge at 10 mtorr pressure. If the cathode-to-substrate spacing is 5 cm, how many gas-phase collisions is a sputtered atom likely to encounter as it traverses this distance?
2. Aluminum is bombarded by 1000 eV Ar ions. (a) What is the maximum energy that can be transferred to the target atom. (b) What is the maximum value that the mean energy of a struck target atom can attain if the threshold sputtering energy for the Ar-Si ion-target combination is 13 eV. The atomic number and mass of Al and Ar, respectively are $Z_{Al} = 13$, $M_{Al} = 27$, $Z_{Ar} = 18$, $M_{Ar} = 39.44$.
3. The sputtering yield of aluminum in Ar is known to be $S = 1.2$ at an ion energy of 600 eV. The measured rate of deposition in a specific sputtering system is $400 \text{ \AA} / \text{min}$ when the external electron current is $I_0 = 100 \text{ mA}$. (a) Calculate the ion current, I , using the Townsend equation:

$$I = (I_0 \exp [\alpha d]) / (1 - \gamma [\exp \{\alpha d\} - 1]),$$

where, $\alpha = 6 \text{ ions/cm}$ and γ , the secondary electron yield = 0.08 electrons per ion, and the interelectrode spacing is $d = 5 \text{ cm}$. (b) Find the new deposition rate when the ion energy is increased to 1000 eV, and $S = 1.9$, $\alpha = 3 \text{ ions/cm}$, and $\gamma = 0.1$ electrons per ion.

4. Explain how the faceting effect is utilized to produce planarized films of so-called bias-sputtered quartz.
5. If a target is made of fused silica with a thickness of 2.5 mm, it has a capacitance of $\sim 1 \text{ pF/cm}^2$. If the current density during rf sputtering of this target is 1 mA/cm^2 and the applied voltage is 1000 V, calculate the time required to charge this capacitance. This roughly represents the time interval during which a glow discharge can remain "on".
6. Explain why the higher secondary electron emission from insulators leads to slower sputter deposition of these materials.