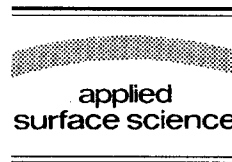




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Advanced multilevel metallization technology

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Abstract

In order for ULSI manufacturing to minimize the COO (cost of ownership) aspect in the wiring process and realize fabricating over 256M bits DRAM, several wiring technologies have been proposed. The evidential criteria in choosing the most probable one are physical or material limitations (e.g. step-coverage and resistivity) and requirements from manufacturing (e.g. process complexity, reliability, throughput, and total cost). Therefore, a combination of metallurgy using chemical vapor deposition (CVD) with simplified multilevel interconnects has a high potential in overcoming those difficulties. In this paper, an integrated multilevel metallization (IMM) by considering the above criteria is discussed. Alternatives of improved W-CVD, TiN-CVD using diborane (B_2H_6) and methylhydrazine (MH) reduction, selective W-CVD, and Cu wiring are described from our recent studies.

1. Introduction

In giga-scale integrated (GSI) devices and circuits down to 0.1 μm design rule, a number of metal interconnection problems have arisen. One is evidently the physical limitation such as the poor step coverage of sputtered aluminum (Al) wire, barrier metal (e.g. titanium nitride = TiN), and contact metal (e.g. Ti). In addition, these have a material limitation due to electromigration (EM), stress migration (SM), resistivity, and contact resistance to Si, respectively.

This is the reason why tungsten (W), TiN, and copper (Cu) wiring by chemical vapor deposition (CVD) have been studied and developed. How to

combine sputtering with CVD (integrated multilevel metallization, IMM) is a key to fabricate GSI devices [1]. Another issue is how to reduce the process complexity and process cost, and how to integrate interconnects by selecting the appropriate alternatives and planarization techniques, whether the conventional or a use of chemical mechanical polishing (CMP). In this paper, the trend towards multilevel metallization for devices over 256M bits is discussed. We describe the simple and feasible IMM using W, TiN, and Cu-CVD based on our recent studies.

2. Via-plug technologies for next generation

As to now, in general, four different contact and via-plug processes have been proposed (Fig. 1). Comparing a number of steps to be filled via-holes,

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the process complexity increases as follows: selective W-CVD, blanket TiN-CVD, sputtered Al with reflow, and blanket W-CVD. A common process in these is the surface cleaning which must be carefully done and which is also a key technology for an ideal metallization with good electrical properties. Among these via-plug processes, the blanket W and sputtered Al are limited by the poor step-coverage of the contact and barrier metal underlayers such as titanium (Ti) and TiN. This is because the degradation of the junction leakage current and void formation take place by the poor step-coverage [1]. One of the more serious problems is the thickness of the barrier metal. Since the barrier metal has to have an adequate thickness in order to prevent unexpected diffusion, via-holes will be consequently filled with the barrier metal in GSI with decreasing the feature size, as shown in Fig. 2. Due to such geometrical problems, the same thing would occur in Cu wiring. Therefore, before GSI generation, via-hole filling

using blanket W-CVD and Al sputtering will be used, and TiN-CVD and selective W-CVD or Al-CVD will be adopted afterwards.

On the other hand, the investigation of selective W-CVD would be appropriate for developing selective Al-CVD and Cu-CVD, because the selective W-CVD is a well-known example in the understanding of the surface cleaning and the reaction mechanism. The current chemical-mechanical polish (CMP) as an alternative planarization technique helps to reduce the difficulty of selectivity loss by polishing-off unexpected W particles formed on a dielectric surface. TiN-CVD, used as a barrier metal of W-CVD and Al, is used instead of the sputtering since some drawbacks such as, Al corrosion due to chlorine (Cl), trade-off of the lowering deposition temperature, and film resistance have been solved, e.g. a use of monomethyl hydrazine reduction chemistry. For contact metallization, a combination of collimated sputtered-Ti, plasma Ti-CVD, and other metals enough

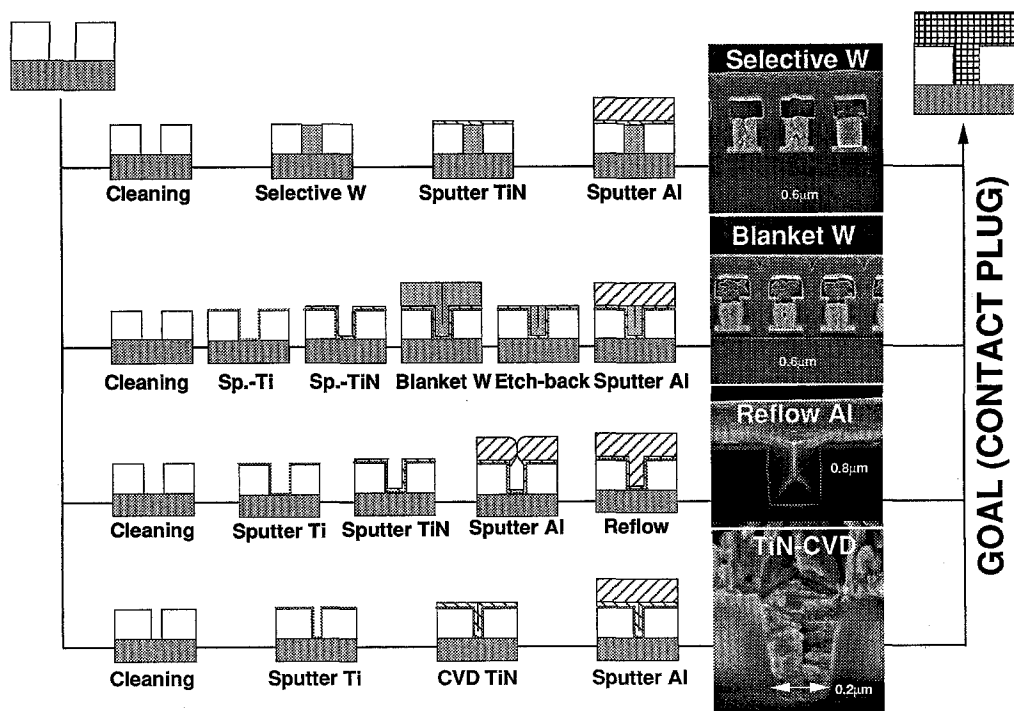


Fig. 1. Via-plug process using selective W-CVD, blanket W-CVD, Al sputtering, and TiN-CVD for 0.2 to 0.8 μm size.

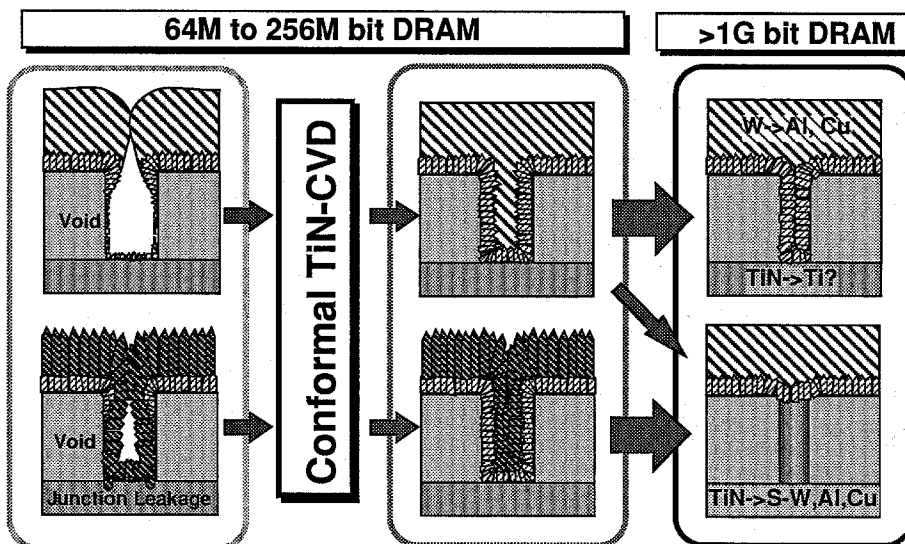


Fig. 2. A use of TiN-CVD film for the underlayer of Al sputtering and blanket W-CVD and results from 64 Mbit to 256 Mbit DRAM wiring. An alternative technology will be required beyond 1 Gbit fabrication.

to achieve lower contact resistance for $\text{Si}(\text{n}^+)$ and $\text{Si}(\text{p}^+)$ would be necessary to realize GSI devices.

3. Low resistance W-CVD

Most companies use blanket W-CVD processes to fabricate 16M and 64M bits DRAMs because of the productivity benefits [2]. At high current density, about 10^6 A/cm^2 , blanket W wire is used instead of Al in order to prevent the open failure from electromigration (EM). High resistivity of W-CVD wires, however, may cause serious problems such as RC delay due to high wiring resistance and a high wiring capacitance due to the feature of a high aspect ratio.

Recently, we found that blanket W-CVD using a diborane (B_2H_6) reduction achieves low resistance (e.g. $7.0 \text{ } \Omega \cdot \text{cm}$ at 440°C) rather than H_2 reduction as shown in Fig. 3 [3]. This difference can be explained from decreasing of fluorine (F) remaining in the W film (Fig. 4). Thus B_2H_6 reduces WF_x ($1 < x < 6$) easier than that of H_2 reduction. The resistivity of the B_2H_6 - H_2 -reduced film is about 50% lower than those of H_2 -reduced film even at a thickness of 150 nm. At the low temperature region, the blanket W contained a high boron (B) concentration, as seen in

Fig. 4. This W layer consisted of β -phase or α -phase structure with some undefined structures such as WB crystal, as shown in Fig. 5.

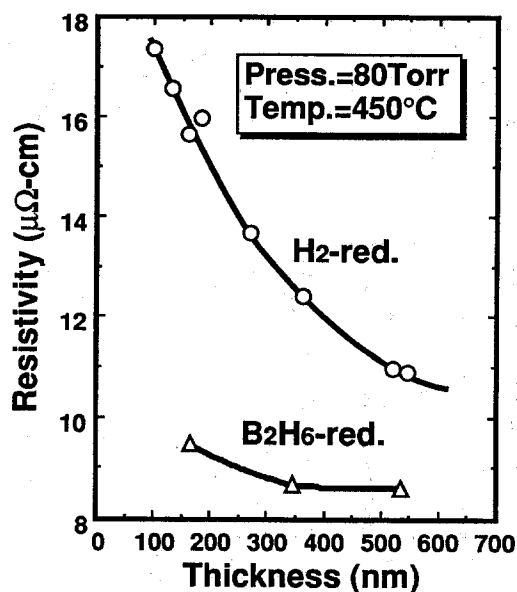


Fig. 3. Resistivity of blanket W-CVD using H_2 - and B_2H_6 -reduction as a function of film thickness.

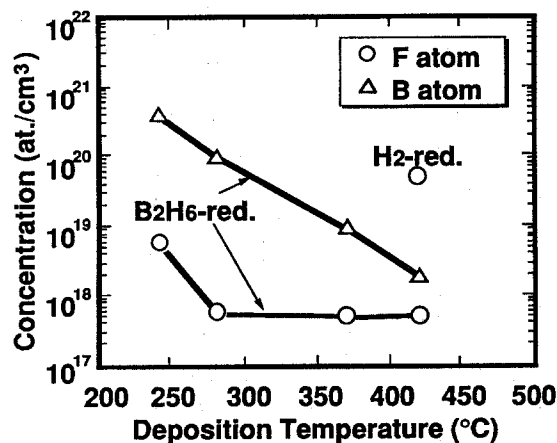


Fig. 4. Fluorine (F) and boron (B) concentration in blanket W as a function of deposition temperature.

Fig. 6 shows film resistivity as a function of B_2H_6 flow rate. There was an optimum region giving low resistivity. B_2H_6 with H_2 reduction achieved 100% of step-coverage at 0.6 μm in diameter and aspect ratio 1.4 without degrading resistivity, as shown in Fig. 7. This is because two kinds of effect such as high step-coverage in H_2 reduction and lowering impurities in B_2H_6 reduction are simultaneously taking place, which may be followed by the so-called concerted reaction [4]. Using this B_2H_6 - H_2 -reduced blanket W, similar electrical properties in contact resistance to $TiSi_2$ were obtained (Fig. 8), which proved the feasibility for practical devices.

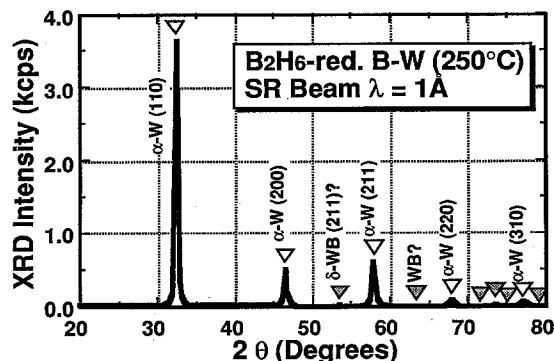


Fig. 5. High resolution X-ray diffraction pattern of B_2H_6 -reduced blanket W formed at 250°C.

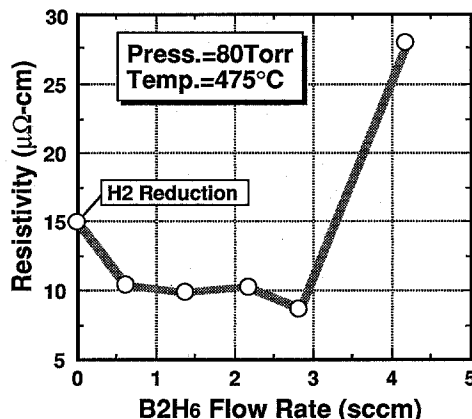
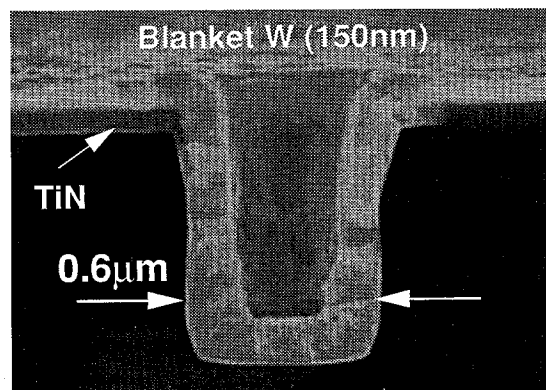


Fig. 6. Film resistivity of blanket W as a function of gas flow rate of B_2H_6 .

4. Low temperature TiN-CVD

On the basis of poor adhesion and chemical etching by WF_6 , the blanket W must be used with a TiN underlayer with the condition of being thick enough to prevent peeling-off of the film and diffusion. Although the TiN-CVD has a capability of conformal deposition, there are some problems concerning resistivity (due to a residue of carbon or chlorine)



WF_6 - H_2 - B_2H_6 Reaction System
 $Q_{H_2}/Q_{B_2H_6} = 666.7$
 (Stepcoverage = 100%)

Fig. 7. SEM cross-sectional view of B_2H_6 - H_2 -reduced blanket W at a contact hole of 0.6 μm in diameter and an aspect ratio 1.4.

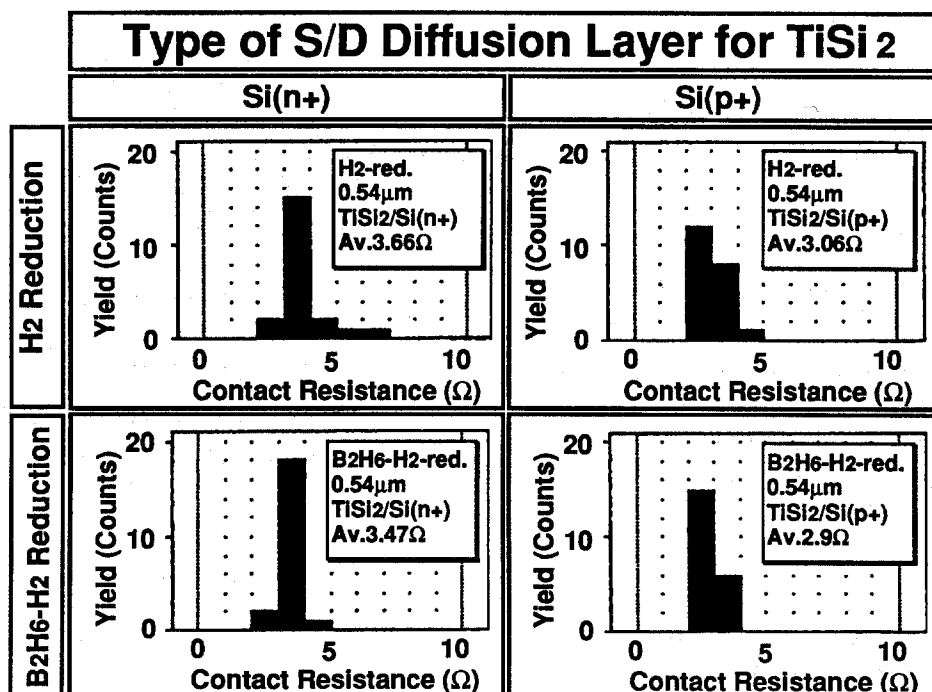


Fig. 8. Contact resistance of W to TiSi_2 formed on $\text{Si}(n^+)$ and $\text{Si}(p^+)$ source/drain (S/D) regions.

and trade-off for deposition temperature. Especially, TiN-CVD using the ammonia (NH_3) reduction [5–9] cannot be used for the via-plug process over the Al wire, since its deposition temperature is higher than 600°C .

TiN-CVD using a methylhydrazine (MH) reduction reaction of titanium-tetrachloride (TiCl_4) realized a low chlorine (Cl) impurity in TiN films even at low temperatures ($< 500^\circ\text{C}$) [10,11]. Fig. 9 shows film resistivity of TiN using MH- and NH_3 -reduction as a function of deposition temperature. The decreasing resistivity with temperature is explained by the reactivity of MH to TiCl_4 as well as the B_2H_6 -reduction as discussed above. Furthermore, the reaction kinetics in MH- NH_3 -reduction apparently changed with the flow-rate ratio of MH/ TiCl_4 at a constant of NH_3 , as shown in Fig. 10, approaching to the mass-transported reaction at MH/ $\text{TiCl}_4 = 0.15$ and the rate-limited at no MH [12]. MH gas has an extra reaction to Ti prior to TiN deposition. Ti was nitrided by MH at low temperatures, as shown in Fig. 11 [13]. Thus, MH acts as a reduction gas for

TiCl_4 and nitrogen source for nitridation instead of NH_3 and N_2 at low temperatures.

According to these reaction kinetics, high step-coverage with low resistivity was achieved as shown in Fig. 12. Therefore, at via-holes below $0.2 \mu\text{m}$ in

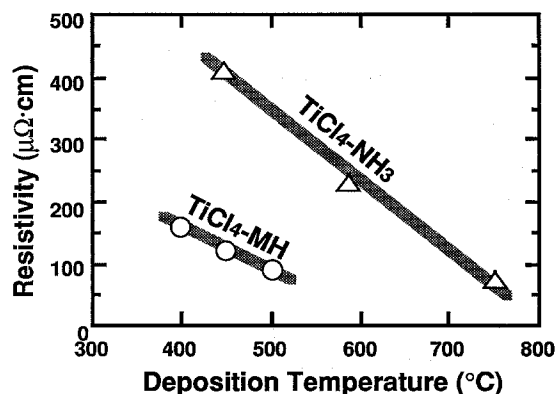


Fig. 9. Resistivity of TiN-CVD film using NH_3 - and MH-reduction of TiCl_4 as a function of deposition temperature.

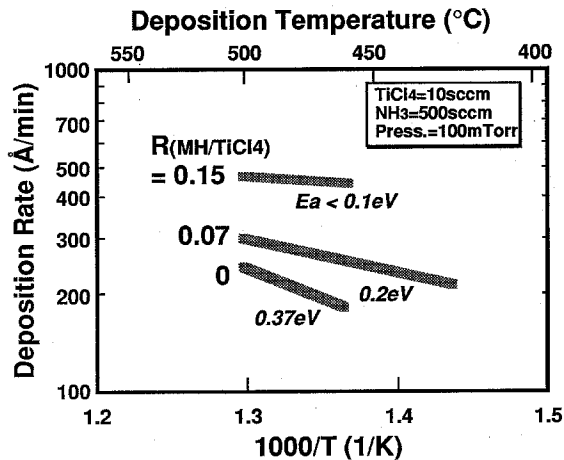


Fig. 10. Arrhenius plot of MH-NH₃-reduction for various flow rate ratios of MH/TiCl₄ at constant NH₃.

diameter, blanket W or Al plug is no longer necessary. Since MH-reduced TiN has high enough to prevent diffusion, the lowest junction leakage current at the Si contact holes was succeeded (Fig. 13) [14]. Also, an ideal contact resistance change was obtained down to 0.2 μm in diameter as shown in Fig. 14 [15]. These electrical properties can be explained by the fine step-coverage as shown in Fig. 15. Therefore, a use of TiN contact plug would promise and solve semiconductor manufacturing beyond 256M bits DRAM without increasing the process complexity and the total cost in multilevel metallization.

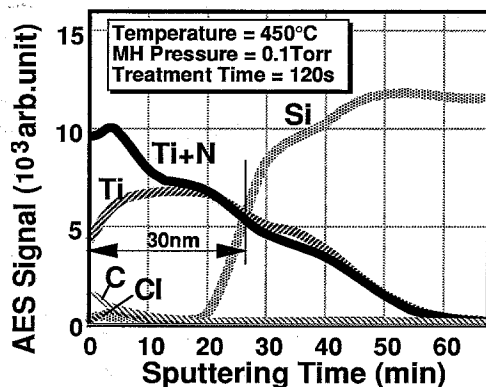


Fig. 11. AES depth profile of sputtered Ti after MH treatment at 450°C.

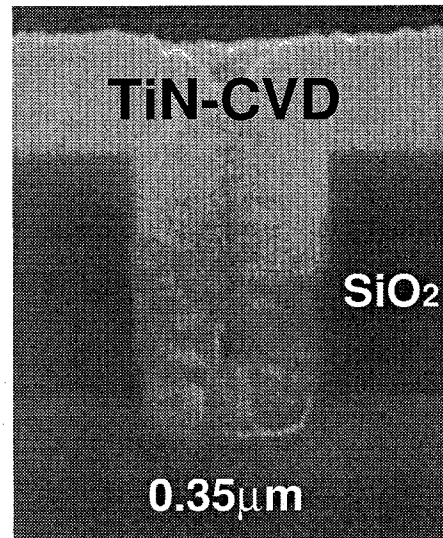


Fig. 12. SEM cross-sectional view of a completely filled contact hole using MH-reduced TiN-CVD.

5. Selective tungsten plug

Since via-holes are filled in one process step, selective W-CVD is very cost-effective when compared to other plug processes. Selective W-CVD can also fill via-holes with no limitation for the hole size if the clean surface on the bottom of the via-holes is obtained. Thus, most studies in selective W-CVD have been focused on the cleaning being compatible

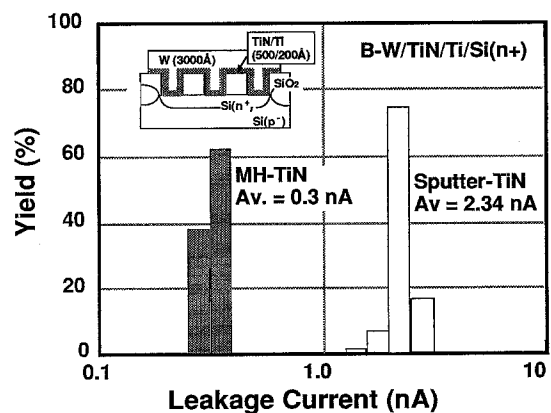


Fig. 13. Junction leakage current of blanket W/TiN/Ti/Si(n⁺) using MH-reduction and conventional sputtering at parallel contact holes of 0.5 μm in diameter each.

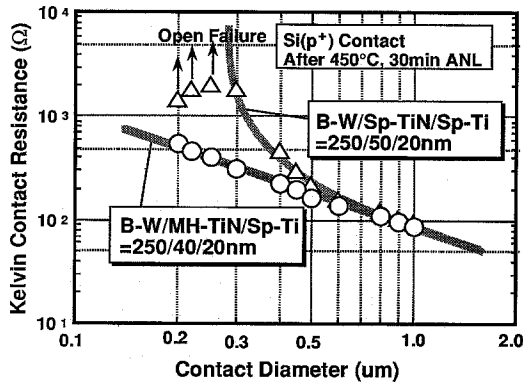


Fig. 14. Kelvin contact resistance of blanket W/TiN/Ti/Si(p⁺) structure using MH-reduction and conventional sputtering as a function of contact diameter down to 0.5 μm .

with high selectivity. Such surface cleanliness also has an effect on the contact resistance not only in selective W but in general metallization, so we should discuss the surface cleaning at the same time.

Wet cleaning is no longer an adequate cleaning for the selective W-CVD. Highly adsorbed moisture tends to degrade selectivity as shown in Fig. 16. An alternative dry cleaning using nitrogen trifluoride (NF_3) and hydrogen (H_2) chemical cleaning allows sufficient W growth on Si and WSi_2 surfaces with high yield in practical devices (Fig. 17) [16,17]. RF plasma cleaning would damage the oxide surface but it can be reduced by halogen termination on the

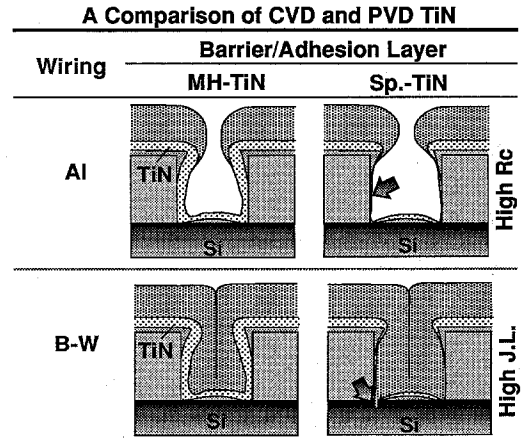


Fig. 15. Schematic diagram of electrical properties for a use of conformal TiN-CVD versus sputtered TiN in Al and blanket-W.

oxide surface. A similar effect was seen in chlorine trifluoride (ClF_3) cleaning as shown in Fig. 18. The selectivity was improved with increasing fluorine (F) concentration on the SiO_2 surface. Using ClF_3 cleaning, low contact resistance and high selectivity was achieved at the via-holes formed on the TiN/Al wires on the entire 6 inch wafer surfaces (Fig. 19).

On the other hand, we have another choice to avoid selectivity loss with a combination of the CMP technique, which is starting to be used for the global planarization of dielectrics [18]. A combination of selective W-CVD with CMP realizes a plane W

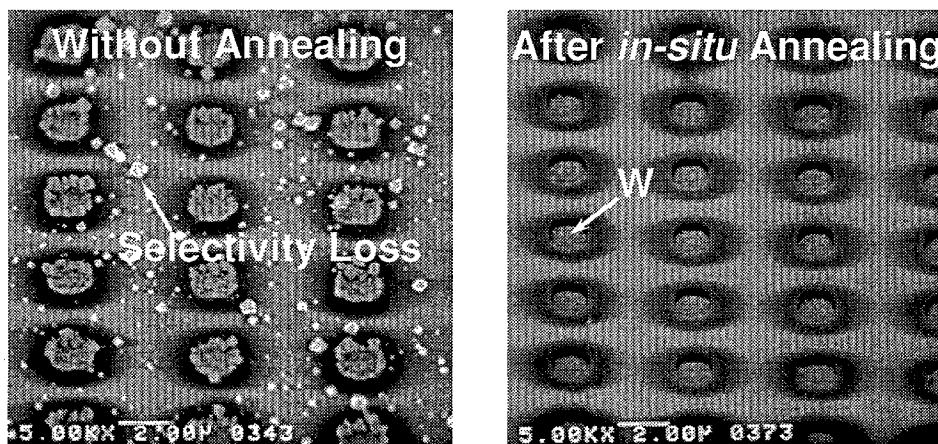


Fig. 16. SEM images of selectivity loss with no treatment (left) and after annealing (right).

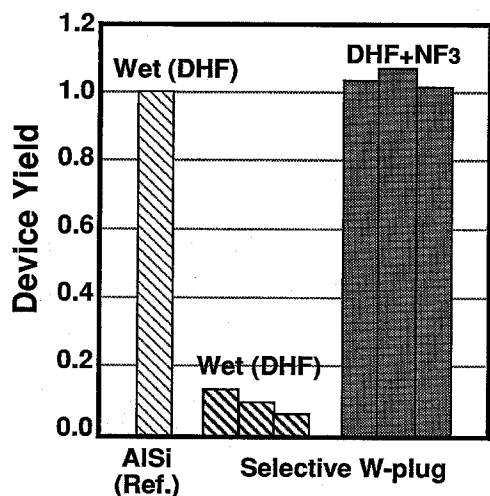


Fig. 17. Device yield using selective W-CVD formed simultaneously on Si-S/D and WSi₂ contacts after DHF or DHF+NF₃ cleaning.

plugs, even some selectivity loss and over filling take place as shown in Fig. 20.

Although there are several solutions to overcome selectivity loss, an ideal deposition atmosphere is needed to achieve highly reproducibility with high throughput in the manufacturing. To reduce unexpected by-products and achieve ideal gas flow are important for controlling precise atomic level deposition even on 12 inch wafers being used in the next generation. We are investigating a silane (SiH₄) reduction process [19,20] and have developed a low pressure CVD reactor as shown in Fig. 21. This

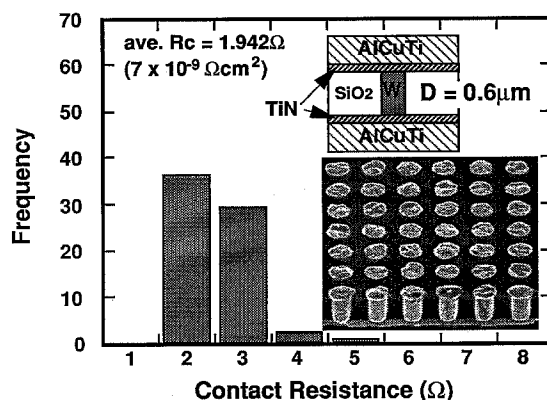


Fig. 19. Contact resistance of selective W deposited on TiN at 0.6 μm via-holes using a 6 inch wafer.

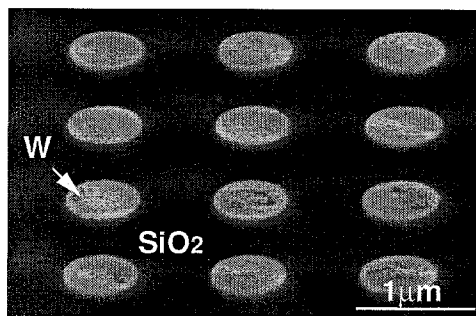


Fig. 20. SEM top-view of selective W-CVD over-filled above 1 μm after polished-off using CMP.

reactor provided a showerhead, so-called matrix showerhead, capable of no gas mixture within the showerhead when several gases were used. The ma-

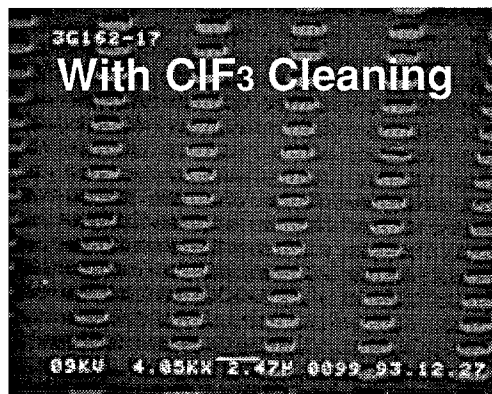
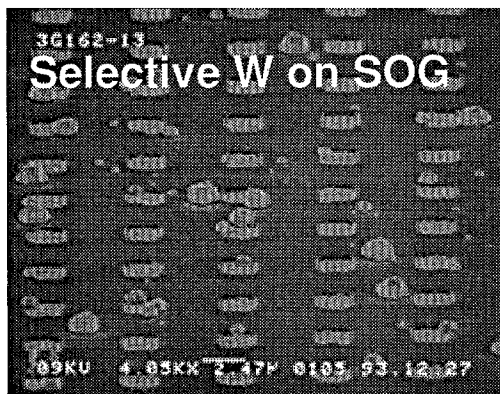


Fig. 18. SEM images of selectivity loss at patterned SOG surface with no treatment (left) and after ClF₃ cleaning (right).

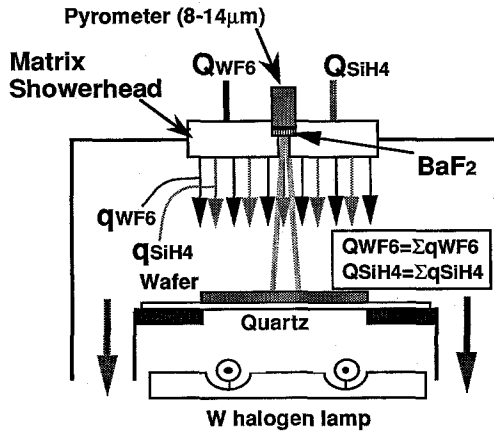


Fig. 21. Schematic diagram of a low pressure CVD reactor provided a matrix showerhead.

trix shower head has no limitation for the wafer size. Using this matrix showerhead, we revealed that selectivity changed with gas flow and its velocity even under the same conditions of gas flow rate of WF_6 and SiH_4 [21]. This suggested that we must carefully control the gas concentration on the wafer surfaces more than the gas flow rate of the mass flow controller (MFC). The reaction kinetics using partial pressure of gas is not enough to discuss practical deposition.

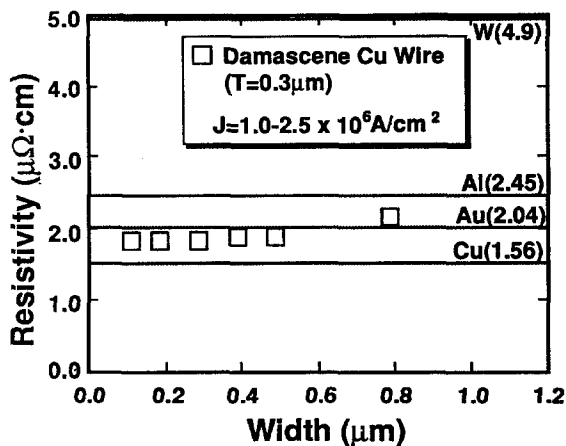


Fig. 22. Resistivity of Damascene Cu formed by CVD as a function of Cu wire width.

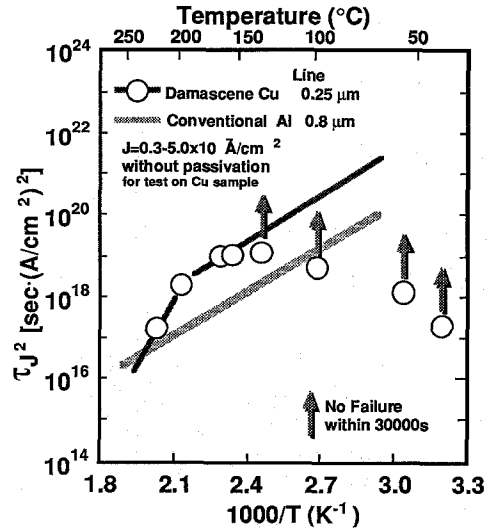


Fig. 23. Lifetime of open failure due to electromigration for 0.25 μm Damascene Cu wire.

6. Cu metallization

Copper (Cu) metallization is one of the most attractive of the alternate choices for GSI devices because of its lowest resistivity among Al, W, and Au, and higher resistance to electromigration failure, as shown in Figs. 22 and 23 [22,23]. Higher reliability more than two orders of magnitude has been

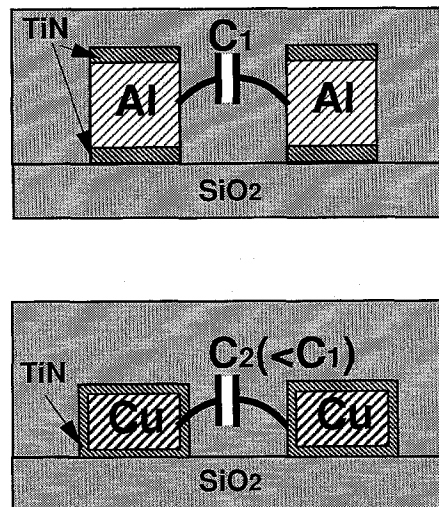


Fig. 24. Schematic diagram of wiring capacitance for Al (top) and Cu (bottom).

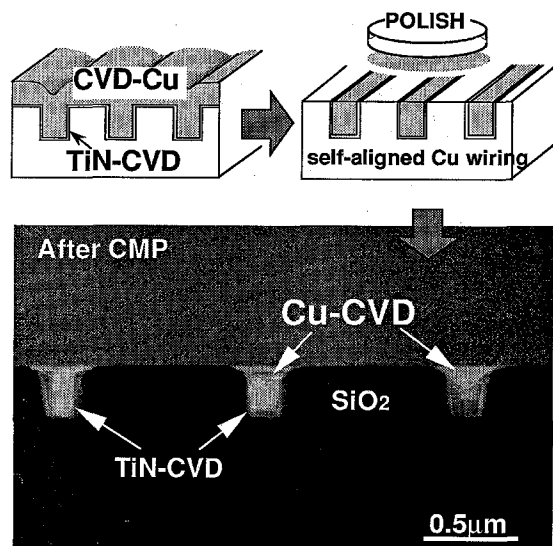


Fig. 25. Damascene process and cross-sectional view of 0.2 μm Cu wires.

proved in Cu wiring compared to conventional Al even at a quarter-micron width. According to the lower resistivity, we can expect an aspect ratio of wire less than Al, and low wiring capacitance which reduces the RC delay (Fig. 24). Using a self-aligned wiring such as the Damascene method, a 0.2 μm Cu wiring appropriate to GSI interconnects has been successful, as shown in Fig. 25. Damascene Cu wiring can be adopted alternatively to the conventional etching processes, which have some drawbacks due to the high temperature process and corrosion.

However, since Cu is easily oxidized and corroded, a sufficient barrier metal and its combination must be provided. For instance, a part of the Cu wire can consequently disappear as well as blanket W and Al, according to shrinking design rule of wires less than the total thickness of the barrier metal. Therefore, most of the concern in Cu wiring is the thin barrier metal, chemical-mechanical polish (CMP), and a high enough step-coverage to fill Cu into the groove and via-hole. To reduce process complexity, a dual-Damascene method has been attempted since it needs only single step Cu deposition for wiring at the via-hole and interconnects simultaneously. Practically, it is worth developing the Damascene process using CVD and sputtering for vias and interconnects,

respectively, before sufficient Cu filling is established.

7. Summary

By GSI generation, either blanket W-CVD or Al combined with flow process will be used in via-plug and wiring. As B_2H_6 reduction realized about 50% reduction of resistivity of W film, W local interconnects instead of Al is appropriate. A single step process such as TiN-CVD and selective W-CVD can be used beyond 256M bits DRAMs because the thickness of TiN is being limited from barrier property in blanket W-CVD and Al. Thus TiN-CVD and selective W-CVD have to have sufficient step-coverage and selectivity, respectively.

TiN-CVD using methylhydrazine reduction for Si contact holes down to 0.2 μm is discussed, and surface cleaning using NF_3 and ClF_3 proves that selectivity and device yield was improved. Use of tungsten CVD for practical multilevel interconnection has provided much information that will help to develop the worthwhile production processes of other CVD metals, such as for Al- or Cu-CVD interconnection.

Since the resistivity of via-holes beyond GSI increases the total resistance of the interconnects, Cu wiring is the best candidate as compared to Al, TiN, and W. The Damascene method, an alternative to conventional patterning, an adequate Cu filling process, and thin barrier layer must be developed. For giga-bit device fabrication, production of worthy CVD metallization has great advantages over conventional sputter processing, but we must weigh the total metallization cost, including equipment cost, number of process steps, throughput, and reliability, against the process features described above.

Acknowledgements

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