

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner

Case IPR2025-01305

Patent No. 8,329,572

**DECLARATION OF DR. BANERJEE
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,329,572**

TABLE OF CONTENTS

I.	INTRODUCTION.....	4
II.	BACKGROUND AND QUALIFICATIONS.....	4
III.	MATERIALS REVIEWED	8
IV.	UNDERSTANDING OF PATENT LAW	11
A.	Claim Construction	11
B.	Anticipation and Obviousness.....	12
V.	PERSON OF ORDINARY SKILL IN THE ART AND THE TIME OF THE ALLEGED INVENTION	15
VI.	TECHNICAL BACKGROUND	16
VII.	STATE OF THE ART	17
A.	Semiconductor manufacturing	17
B.	Material Deposition and Layer Preparation	20
C.	Passivation Layer / Barrier Layer/ Oxidation-Resistant Layer.....	23
D.	Photolithography	25
E.	Etching.....	26
VIII.	THE '572 PATENT	27
A.	Overview	27
B.	Prosecution History	28
IX.	THE PRIOR ART DISCLOSES AND/OR SUGGESTS ALL RECITED FEATURES OF CLAIMS 1-7 OF THE '572 PATENT	29
A.	Ground 1: Parikh, alone (1A) or in combination with Komada (1B).....	29
1.	Parikh.....	29
2.	Komada	31
3.	Combination of Parikh and Komada.....	32
4.	Claim 1	36
5.	Claims 2-3	55
6.	Claim 4	59
7.	Claim 5	69
8.	Claims 6-7	73
B.	Ground 2: Claim 2 Is Obvious Over Parikh, Komada, and Maeda	75

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

1. Maeda	75
2. Combination of Parikh, Komada, and Maeda.....	76
3. Claim 2.	80
C. Ground 3: Roberts, alone (3A) or in combination with Parikh (3B), renders obvious claims 1-3	81
1. Roberts.....	81
2. Combination of Roberts and Parikh.....	82
3. Claim 1	88
4. Claims 2-3	101
D. Ground 4: Claim 2 Is Obvious Over Roberts, Parikh, and Maeda	103
E. Ground 5: Claims 4-7 Are Obvious Over Roberts, Parikh, and Komada	105
1. Combination of Roberts, Parikh, Komada	105
2. Claim 4	111
3. Claim 5	112
4. Claim 6	112
5. Claim 7	117
X. CONCLUSION.....	118

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

I, Sanjay K. Banerjee, declare as follows:

I. INTRODUCTION

1. I have been retained as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“USPTO”) regarding U.S. Patent No. 8,329,572 (“the ’572 patent”) (EX1001).¹ I have been asked to consider whether prior art references disclose or suggest the features recited in claims 1-7 (“the Challenged Claims”) of the ’572 patent. My opinions are set forth below.

II. BACKGROUND AND QUALIFICATIONS

2. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. I have been a faculty member at UT Austin since 1987.

3. I have also been active in industries related to the relevant field of art. As a Member of the Technical Staff, Corporate Research, Development and Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by Texas Instruments in the world’s first 4-Megabit DRAM, for which I was co-

¹ In this Declaration, I refer to exhibits that I understand are to be attached to the petition for Inter Partes Review of the ’572 patent.

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

4. I received a B. Tech. degree from the Indian Institute of Technology, Kharagpur, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

5. I am a leading researcher and educator in various areas of CMOS transistor device Front End of Line (FEOL) and Back End of Line (BEOL) fabrication technology, including the fabrication, characterization and application of CMOSFETs, FinFETs, DRAM, SRAM and flash memory devices, and nanotechnology. I have published numerous experimental and theoretical papers on planar and vertical transistors, and relevant process technologies including lithography, chemical vapor deposition (CVD), including plasma enhanced CVD (PECVD) of dielectrics such as SiO_2 and Si_3N_4 , reactive ion etching, high-k gate dielectric deposition by atomic layer deposition, metal (e.g. Al, Cu, Ti, TiN) interconnect deposition by sputtering and evaporation, chemical mechanical polishing, and epitaxy of strained Si-Ge-C heterostructures. My research has been funded by the Texas Advanced Technology Program (ATP), the Texas Higher Education Coordinating Board, the National Science Foundation, the SEMATECH (Semiconductor Manufacturing Technology) consortium, the SRC (Semiconductor

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

Research Corporation) consortium, DARPA, and the Department of Energy, among others.

6. At the University of Texas, I served as the director of the Microelectronics Research Center from Sept. 1999 to Jan. 2025. I also served as the director of the South West Academy of Nanoelectronics from its inception through the end (Dec. 2017), one of three centers in the United States established to develop a replacement for MOSFETs. I have been the Site Director of the NSF Nanofabrication Coordinated Infrastructure Facility from 2004-2025.

7. I have published over 1,200 technical articles, many related to semiconductor fabrication technology, most at highly competitive refereed conferences and rigorously reviewed journals. I have also published 8 books or chapters on transistor device physics and fabrication, and have supervised over 90 Ph.D. and 60 MS students.

8. I have been a member of scientific organizations and committees, including the IEEE Dan Noble Award Committee from 2010–2013, serving as Chair from 2012–2013, the International Technology Roadmap for Semiconductors, the International Conference on MEMS (Microelectromechanical Systems) and Nanotechnology, the IEEE International Conference on Communications, Computers, Devices, the International Electron Devices Meeting, the International Conference on Simulation of Semiconductor Processes and Devices, and the IEEE

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

Symposium on VLSI (Very-Large-Scale Integration) Technology. I have served as the Session Chair for the “Device Technology” Session conducted at the IEEE International Electron Devices Meeting in 1989–1990. I have also served as the General Chairman for the IEEE University Government Industry Microelectronics Symposium in 1994–1995, and Chair of the IEEE Device Research Conference.

9. I have previously served on the Technical Advisory Boards of AstroWatt, DSM Semiconductors, Cambrios, Nanocoolers Inc., BeSang Memories, Organic ID and ITU Ventures; Gerson Lehmann Group, NY; Austin Community College; Asia Pacific IIT; Rochester Institute of Technology, and HSMC Foundry. I currently serve on the Advisory Board of Advanced Nano Devices who fabricate vertical power transistors.

10. I received the Engineering Foundation Advisory Council Halliburton Award (1991), the Texas Atomic Energy Fellowship (1990–1997), Cullen Professorship (1997–2001) and the Hocott Research Award from UT Austin (2007). I also received the IEEE Grove Award (2014), Distinguished Alumnus Award, IIT (2005), Industrial R&D 100 Award (2004), ECS Callinan Award, 2003, IEEE Millennium Medal, 2000, NSF Presidential Young Investigator Award in 1988, and several SRC Inventor Recognition and Best Paper Awards. I was a Distinguished Lecturer for IEEE Electron Devices Society, and am a Fellow of the Institute of the

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

Electrical and Electronics Engineers (IEEE), the American Physical Society (APS) and the American Association for the Advancement of Science (AAAS).

11. I am the inventor or co-inventor of over 35 United States patents in various areas of transistor device fabrication technology. I was elected a Fellow of the National Academy of Inventors in 2021.

12. Additional details about my employment history, fields of expertise, and publications are further included in my curriculum vitae.

13. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the substance of my opinions, or the outcome of any proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '572 patent.

III. MATERIALS REVIEWED

14. The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding systems and processes in the field of semiconductor fabrication technologies.

15. In forming my opinions expressed in this Declaration, I reviewed the following materials:

EX1001	U.S. Patent No. 8,329,572 (the “’572 patent”)
EX1002	Reserved.
EX1003	File history of the ’572 Patent
EX1004	US Patent Publication No. 2003/0148618 (“Parikh”)
EX1005	Japan Patent No. JP20020289689 (“Komada”)
EX1006	Japan Patent Publication No. JPH1116906A (“Maeda”)
EX1007	U.S. Patent No. 6,461,914 (“Roberts”)
EX1008- EX1010	Reserved.
EX1011	Chang <i>et al.</i> , “ULSI Technology,” (1996)
EX1012	Wolf, “Silicon Processing for the VLSI Era” (1986)
EX1013	S. K. Ghandi, VLSI Fabrication Principles (2nd, 1994)
EX1014	K. Kamoshida, <i>et al.</i> , “Self-aligned TiN Formation by Nz Plasma Bias Treatment of TiSi, Deposited by Selective Chemical Vapor Deposition” <i>36 Jpn. J. Appl. Phys.</i> (1997)
EX1015	T. Ohba, “Advanced multilevel metallization technology” 1995 Applied Surface Science 91 (1995)
EX1016	L. E. Griffiths, “Low temperature electrochemical synthesis of titanium nitride,” <i>2001 The Royal Society of Chemistry</i> (2001)

EX1017	J.S. Colligon, "Composition and chemical state of titanium nitride films obtained by different methods" <i>1994 Elsevier Science S.A.</i> (1994)
EX1018	H. Hamamura, "Composition and chemical state of titanium nitride films obtained by different methods," <i>2001 The Japan Society of Applied Physics</i> (2001)
EX1019	S.M. Sze, <i>et al.</i> , <i>Semiconductor Devices: Physics and Technology</i> , (2nd ed. 2002)

I also considered any other documents and materials I refer to in this Declaration.

16. My opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the state of the art, the prior art, and the claims and the specification of the '572 patent at the time of the alleged invention, which I discuss below.

17. I have been asked to assume that the time of the alleged invention of the '572 patent was around early 2003 (including and up to September 26, 2003), which I am told corresponds to the filing date of the earliest application associated with the '572 patent.

18. Based on my experience and expertise, it is my opinion that certain reference(s) disclose and/or suggest all the features recited in the Challenged Claims of the '572 patent, as I discuss in detail below.

IV. UNDERSTANDING OF PATENT LAW

19. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

20. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the Phillips standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a person of ordinary skill in the art (POSITA) at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

21. I understand that when considering the meaning of patent claims, one must consider the language of the claims, the specification, and the prosecution history of the patent. I also understand that claim terms are typically given their ordinary and customary meanings as would have been understood by a person of ordinary skill in the art at the time of the invention for the patent.

22. I do not believe any claim terms require explicit construction in this proceeding to resolve the patentability of the Challenged Claims. I have therefore applied the ordinary and customary meanings of claim terms in my analysis.

B. Anticipation and Obviousness

23. I have been informed that a patent claim is anticipated if a single prior art reference, such as a patent or a publication, discloses all the limitations of the claimed invention arranged as in the claim.

24. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

25. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a

combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, I have been informed that it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed limitations represent one of a limited number of known design choices;
- whether the combination of references would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known limitations in the manner described in the claim;
- whether the change was merely the predictable result of using prior art elements according to their known functions, or whether it was the result of true inventiveness;

- whether the invention merely substituted one known element for another known element in order to obtain predictable results;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of limitations claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

26. I understand that a POSITA has ordinary creativity and is not an automaton.

27. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

28. I understand that prior art to the '572 patent for purposes of my opinion herein includes patents and printed publications in the relevant art that predate the priority date of the '572 patent.

29. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things,

commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field.

30. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

V. PERSON OF ORDINARY SKILL IN THE ART AND THE TIME OF THE ALLEGED INVENTION

31. I am familiar with the level of ordinary skill in the art regarding the '572 patent as of around September 26, 2003. Considering the '572 patent, the technology, the educational level and experience of workers in the field relating to the patent, and problems and solutions in that field, and drawing on my own experience, I believe a person of ordinary skill in the art at the time of the alleged invention (which I am asked to assume to be around September 26, 2003) would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in

semiconductor manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.

32. My opinions in this Declaration regarding the '572 patent and the prior art (including the state of the art) are from the perspective of one of ordinary skill in the art as I defined above, during the relevant timeframe (e.g., the time of the alleged invention), which I am asked to assume to be around September 26, 2003, as discussed above.

VI. TECHNICAL BACKGROUND

33. Below, I present a brief overview of certain aspects of semiconductor devices and processes at the time of the alleged invention for the '572 patent. The functionalities and concepts I describe below in this technical background section reflect the state of the art that a person of ordinary skill in the art would have had knowledge of and understood prior to and at the time of the alleged invention of the '572 patent. I rely on, and incorporate as applicable (even if not expressly mentioned below in Section IX), the following disclosures and opinions to support my opinions in this Declaration, including those opinions relating to how the prior art discloses and/or suggests the challenged claims of the '572 and how and why a person of ordinary skill in the art would have been motivated to consider and combine the disclosures and suggestions from that prior art as I explain below in Section IX. The

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

concepts below would have been within the knowledge and mindset of a person of ordinary skill in the art at the time.

VII. STATE OF THE ART

A. Semiconductor manufacturing

34. By the early 2000s, semiconductor manufacturing was a process that formed electronic components, primarily transistors, on a silicon substrate. EX1011, xv-xxi. The process began with wafer preparation, producing a high-purity, single-crystal silicon substrate that served as the foundation for all subsequent device fabrication. EX1011, 107. Then, an active device layer was formed by selectively doping regions to create n-well, p-well, or twin-well structures in a CMOS structure. EX1011, 474-475; EX1012, 109-110, Fig. 1. Active regions which house the devices, such as transistors, diodes, and other components, are created, and separated by isolation regions which prevent undesirable electrical cross-talk between adjacent transistors. EX1011, 474-475; EX1012, 109-110, Fig. 1.

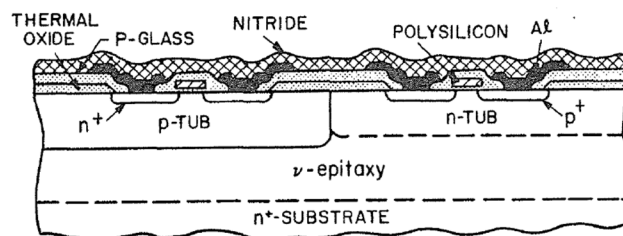


Fig. 1 Examples of types of thin films used in VLSI fabrication¹⁴. (© 1980 IEEE.)

EX1012, 109, Fig. 1. Above these active regions, a multi-level, metallization (wiring structure) was fabricated to link the active components into functional logic

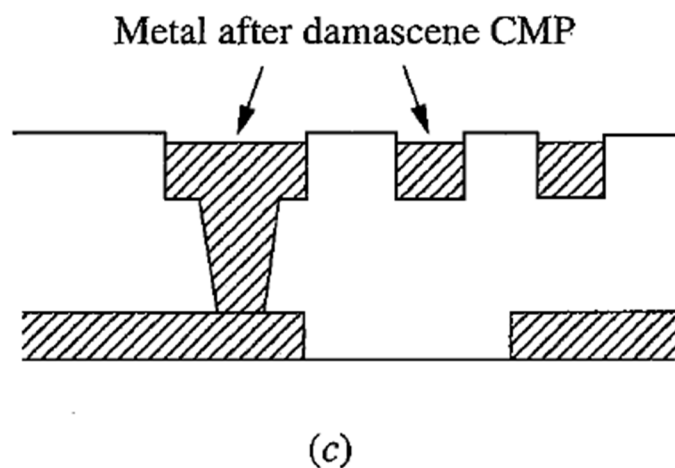
or analog circuits. EX1011, 378-379. Large bonding pads were formed to provide robust electrical connections between the internal circuitry and the external circuits. EX1005, Abstract; *see also* EX1011, 448, 530-531. Other structures, such as a moisture seal ring, may have been formed at the periphery of the chip, and an overcoat deposited to protect the core region of the functional circuits from the ambient environment. EX1005, Abstract; EX1011, 530-531, 552. Finally, the entire chip was encapsulated within a protective package for mounting and connecting the chip to printed circuit boards or other system-level assemblies. EX1011, 530-532, 535-537.

35. One step in this process was the formation of the interconnect (wiring) structure. The '572 patent and references cited in this expert declaration primarily focus on the manufacturing of these interconnect structures, such as through a damascene process. *See e.g.*, EX1001, 1:41-44; EX1004, [0005]; EX1007, 7:28-32. Interconnect structures typically comprised alternating stacks of insulating dielectric layers (generally called “interlayer dielectric” or “ILD”), such as silicon oxide, and layers of patterned metal traces, made of, e.g., aluminum, copper, or the like. EX1011, 378-379, 488-489. These different layers of metal traces were vertically connected through vias (vertical through holes or openings within an ILD layer filled with conductive material). EX1011, 378-379, 488-489. In a damascene process, horizontal metal traces were formed by filling metal in trenches in the ILD layer;

Declaration of Dr. Banerjee

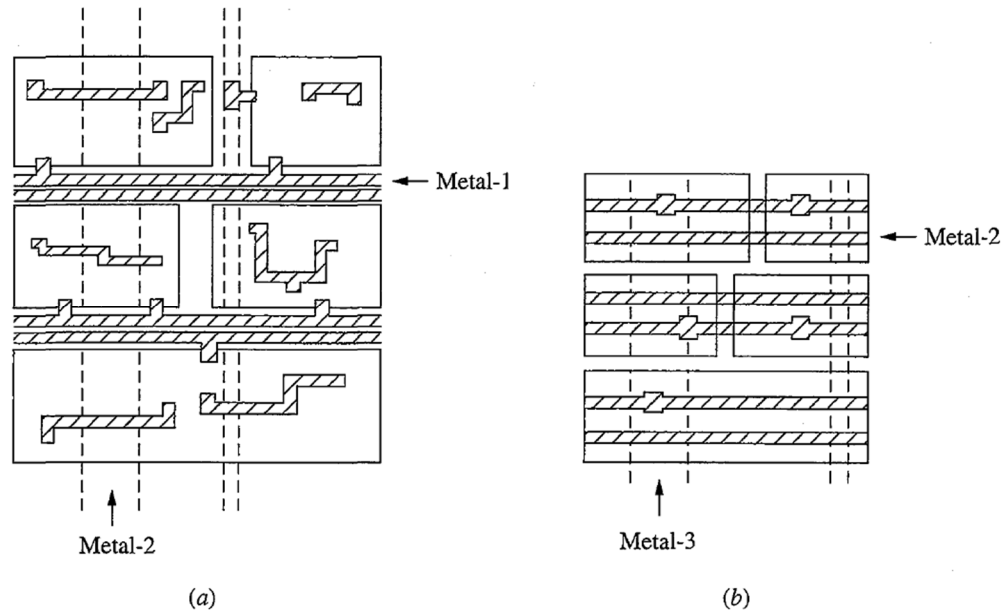
U.S. Patent No. 8,329,572

vertical vias were formed by filling metal in via openings in the ILD layer, and then polishing or planarizing the structure using chemical mechanical polishing (CMP). This is more attractive than the earlier interconnect fabrication process where the metal layers themselves were patterned and etched. This is because it is easier to pattern and etch the ILD. EX1011 at 444-445, Fig. 48(c).



EX1011, Fig. 48 (c).

36. The metal interconnect in a chip could comprise two to five, or more, levels of stacks to achieve the necessary density and performance. EX1011, 377-379, Fig. 5.



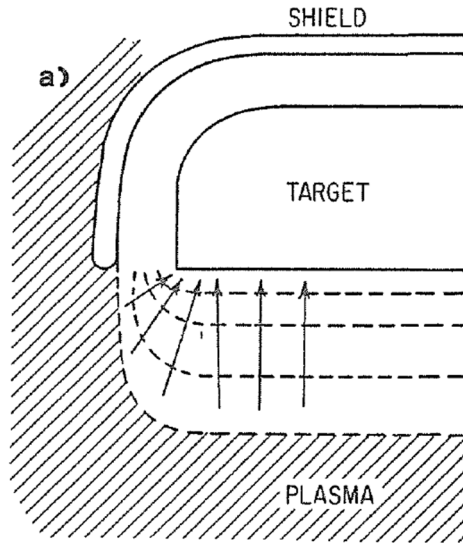
EX1011, Fig. 5. The damascene process, commonly used to form metal traces and vias, involved either forming vias first and then trenches (single damascene) or forming both vias and trenches simultaneously (dual damascene). EX1007, 7:28-32. The general process included the deposition of material layers, photolithographic patterning, and etching to define the interconnect architecture.

B. Material Deposition and Layer Preparation

37. By the early 2000s, deposition of materials on a substrate to form ultra-thin films was another step in semiconductor manufacturing. The primary categories of deposition techniques were chemical vapor deposition (CVD), physical vapor deposition (PVD), and wet deposition (electroplating/electroless plating). EX1011, Chapter 8; EX1013, 510-518. CVD involved the chemical reaction of vapor-phase precursors at the substrate surface to form a solid film. EX1011, 386-

394, 205; EX1012, 161-162. PVD, on the other hand, physically transferred material from a source to the substrate. EX1011, 380-381; EX1012, 335-336. The primary PVD method utilized in VLSI and ULSI fabrication was sputtering, which was widely used for depositing metals such as aluminum, tungsten, titanium, and their alloys like titanium nitride. EX1012, 335 (“Sputtering has displaced evaporation as the workhorse PVD method for VLSI.” “It has become the most widely utilized deposition technique for a variety of metallic films in VLSI fabrication, including aluminum, aluminum alloys, platinum, gold, titanium, tungsten and tungsten.”); EX1013, 514; EX1018, 1517 (“Conventionally, TiN films are deposited by physical vapor deposition (PVD) using reactive sputtering.”).

38. Sputtering operated by bombarding a solid target with energized ions, typically argon ions, in a low-pressure plasma environment. EX1013, 514; EX1012, 335 (“Sputtering is a term used to describe the mechanism in which atoms are dislodged from the surface of a material by collision with high energy particles.”).



EX1012, Fig. 7a. When these ions struck the target surface, they transferred momentum to the atoms in the target, causing some of those atoms to be dislodged (or “sputtered”) from the surface. *Id.* The dislodged atoms then travel through the vacuum and condense onto the substrate, forming a thin film. Sputtering was “extensively used in the deposition of thin films” because of “(a) the ability to deposit a wide variety of metals and insulators, as well as their mixtures, (b) the replication of target composition in the deposited film, and (c) the capability for *insitu* cleaning of the substrate prior to film deposition.” EX1013, 514. Similarly, *Wolf* also recognized that sputtering was “the workhorse PVD method for VLSI.” EX1012, 335. Therefore, a POSITA would have understood that, by the early 2000s, PVD typically referred to sputtering, which was a form of plasma treatment.

39. Electroplating and electroless plating were performed in a liquid bath, where the wafer or substrate was immersed in a solution containing metal ions and

a chemical reducing agent. EX1011, 394-395. In the liquid bath, metal ions were reduced and form a solid metal film on the substrate. *Id.* Electroplating involved applying external electrical current while electroless plating did not. *Id.* Therefore, a POSITA would have understood that electroplating and electroless plating were forms of wet treatment.

40. Following a deposition process, a deposited layer might have been planarized (e.g., CMP), cleaned, and plasma-activated or primed to prepare the surface, remove residues, control roughness, and provide additional properties. EX1011, 386, 394-395, 444-445.

C. Passivation Layer / Barrier Layer/ Oxidation-Resistant Layer

41. By the early 2000s, protective measures were often taken, before or after the formation of the interconnect layer, to inhibit unwanted properties such as chemical reactions or diffusion of the metal. EX1011, 215-218; EX1012, 191-192. A challenge in semiconductor processing was the oxidation of metal conductors during subsequent manufacturing steps, such as plasma ashing or exposure to ambient air. *See e.g.*, EX1004, Abstract; EX1005, [0005], [0113]; EX1010, 451; EX1011, 563. Therefore, a passivation/barrier layer was often used to prevent metal (such as copper) from corrosion (e.g., oxidation) during the following steps, like ashing, and to inhibit diffusion. EX1011, 452 (“To protect Cu from corrosion, passivation layers are needed”); EX1004, [0032] (“One purpose of the metal

passivation layer is to prevent the conductive metal from diffusing into the dielectric.”).

42. The passivation layer might be either conductive or non-conductive, depending on the circuit design and the specific materials selected. For example, silicon nitride was widely used as a non-conductive passivation layer due to its excellent insulating properties and ability to protect devices from environmental contaminants and moisture. EX1011, 260; EX1012, 192. In contrast, titanium nitride (TiN), which is chemically stable, was a conductive material that was often employed as a passivation or barrier layer, particularly in applications where electrical conductivity and chemical stability were required. EX1011, 260; EX1012, 192. EX1014, 642; EX1016, 1 (“Titanium nitride is a technologically important material that exhibits excellent chemical stability, good wear resistance, and high electrical conductivity.”); EX1018, 1517; EX1005, [0004]. [0016]. Therefore, in my opinion, a passivation or barrier layer formed of TiN is an oxidation-resistant conductive layer.

43. By the early 2000s, methods for forming a TiN passivation or barrier layer were well-known in the art, including CVD (EX1014, EX1018), ion assisted deposition and ion plating (EX1017), wet treatment (electrochemical) (EX1016), and plasma treatment (sputtering) (EX1014, EX1015).

D. Photolithography

44. By the early 2000s, photolithography was the central patterning technique in semiconductor manufacturing, enabling the precise transfer of intricate circuit patterns onto a substrate. EX1011, 407-409. In this process, the substrate was coated with a thin film of light-sensitive polymer (photoresist). *Id.* The substrate coated with photoresist was then exposed to ultra violet light through a mask or reticle, which defined the regions to be retained or removed by inducing chemical changes in the photoresist. *Id.* Then, the photoresist went through a development process in which unwanted regions were dissolved away, resulting in a patterned resist layer based on the light pattern projected through the mask. *Id.* This patterned photoresist acted as a protective mask during subsequent etching or ion implantation steps, enabling selective processing of the underlying material. *Id.*

45. After it had served its purpose as a processing mask, the photoresist was removed (stripped) in subsequent cleaning or stripping steps to prevent contamination and ensure the integrity of the device layers. EX1011, 428-429, Fig. 14. The removal of photoresist was critical, as any residue could interfere with later processing steps or degrade device performance. *Id.*

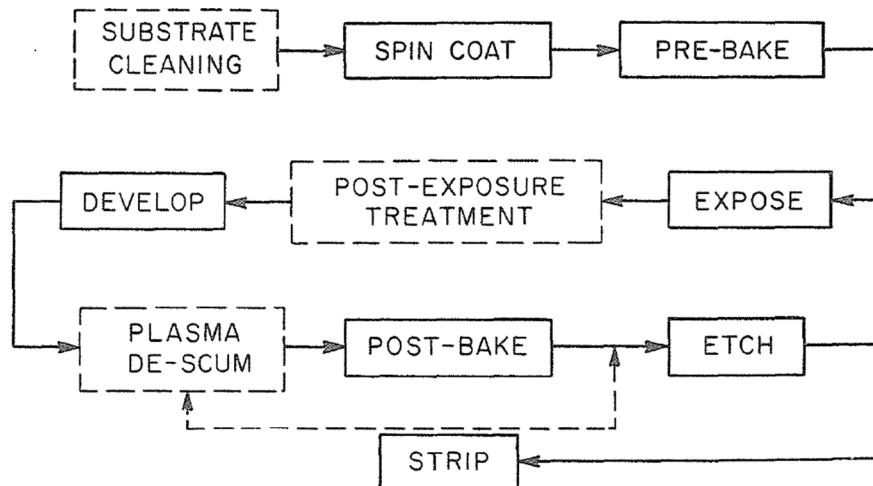


Fig. 14 Flow chart of a typical resist process. Steps in broken lines are not used for all materials. Reprinted from Ref. 8 with permission of the American Chemical Society.

EX1011, Fig. 14.

E. Etching

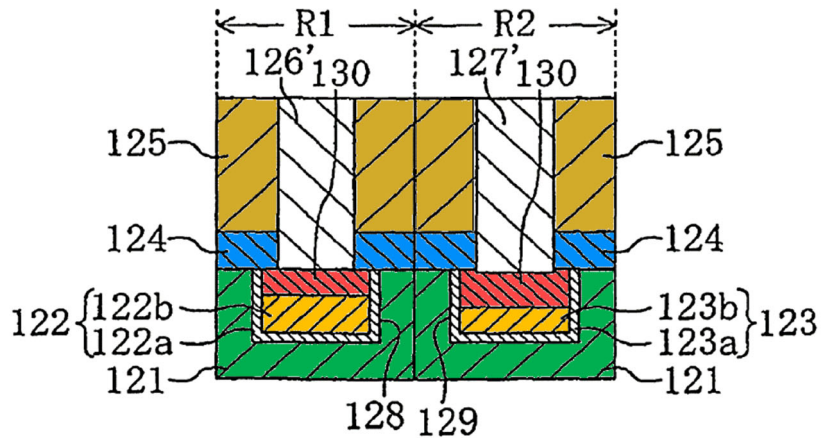
46. By the early 2000s, etching was another process in semiconductor manufacturing, used to selectively remove material following a pattern defined by a mask. EX1011, 329; EX1013, 587. In forming a multi-layered interconnect structure discussed above, etching was used to form via openings and trenches according to the pattern. As disclosed above, after etching, the via openings and trenches were filled with conductive metals, creating vertical and horizontal conductive paths of the multi-layered interconnect structure. To increase efficiency and enable certain features, etching through multiple ILD layers in one step was a well-known, common textbook practice. *See e.g.*, EX1010, 510 (“The poly 1 photomask is applied and the composite film is plasma-etched as a stack.”); EX1011, 535 (“composite layers (e.g. Al I Ti I Al) can be sequentially deposited and

then patterned with a single liftoff, as opposed to removal by multiple etch steps in an etching process”); EX1013, 615 (“It is particularly suited for systems with multiple layers, where all layers have to be etched with a minimum of undercutting.”).

VIII. THE '572 PATENT

A. Overview

47. The '572 patent pertains to the fabrication of a semiconductor device with interconnect layers. EX1001, Abstract, Fig. 3E, 12:42-44. At my suggestion, colors are added to Figure 3E below for better visible understanding of the various elements. Figure 3E depicts a multi-layer structure having a first insulating film 121 in which metal interconnect films 122 and 123, and oxidation-resistant films 130, are formed. *Id.*, 12:62-13:18. A second insulating film 124 is deposited over the oxidation-resistant films 130 and the first insulating film 121. *Id.*, 13:19-26. A third insulating film 125 is formed on the second insulating film 124. *Id.*, 13:27-33. Hole 126 and trench 127 are formed by etching both second and third insulating films 124 and 125. *Id.*, 13:34-52.



EX1001, Fig. 3E. Moreover, I found that the '572 patent states that it was known in the art that a seal ring may be formed to protect transistors and interconnects, and that the ring trench for the seal ring may be etched concurrently with the via etching. EX1001, 1:45-52. I also found that the '572 Patent states that it was known in the art to remove photoresist after the insulating film is etched or partially etched. EX1001, 1:60-65.

B. File History

48. I have reviewed the prosecution history of the '572 Patent. The '572 Patent issued from a divisional application filed on Mar. 18, 2011, and claims priority to other applications. EX1003, 35. During prosecution, the applicant submitted a preliminary amendment introducing a new limitation "until the oxidation-resistant conductor film is exposed in one step" into claim 1, without citing support from the specification. *Id.*, 136. The applicant also submitted new

sets of figures—Figs. 6A-6E and 7A-7F. *Id.*, 141-142. I note that the application was allowed in the first Office Action. *Id.*, 17.

IX. THE PRIOR ART DISCLOSES AND/OR SUGGESTS ALL RECITED FEATURES OF CLAIMS 1-7 OF THE '572 PATENT

49. In my opinion, the prior art discussed below discloses and/or suggests the limitations of claims 1-7.²

A. Ground 1: Parikh, alone (1A) or in combination with Komada (1B)

1. Parikh

50. Parikh discloses a method of semiconductor fabrication. EX1004, Abstract, [0002], Figs. 2-7. Based upon my review of Parikh, I have determined that it introduces a sequence of steps similar to claim 1 of the '572 patent, including (a) forming a substrate with a first dielectric layer (820), (b) forming conductive elements in the first dielectric layer (820); (c) depositing a metal passivation layer on the conductive elements (822), (d) depositing a second dielectric layer over the metal passivation layer and the first dielectric layer (824); (e) depositing a third dielectric layer over the second dielectric layer (826); and (f)

² In this section (Section IX), I refer to exhibits other than those identified prior art reference(s) that disclose and/or suggest the claimed limitations. Such exhibits reflect the state of the art known to a person of ordinary skill in the art at the time of the alleged invention.

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

forming vias and trenches in the second and third dielectric layer (828-830).

EX1004, Table I. I had the below chart created, comparing Parikh's steps and claim 1 of the '572 Patent.

TABLE I	
Station	Processing Step
820	Forming a conductive element on a substrate comprising a first dielectric layer and one or more conductive material embedded in the first dielectric layer
822	Selectively depositing a metal passivation layer on the conductive element
824	Depositing a second dielectric layer over the metal passivation layer and the first dielectric layer
826	Depositing a third dielectric layer over the second dielectric layer
828	Forming a via in the second dielectric layer
830	Forming a line in the third dielectric layer
832	Depositing a conductive material in the line and the via

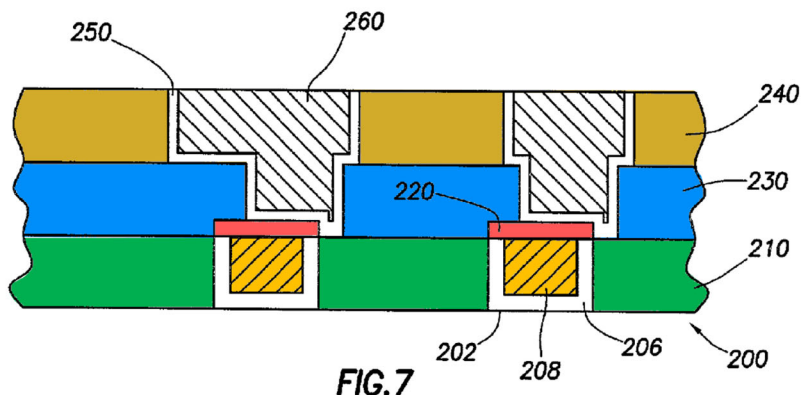
1. A method for fabricating a semiconductor device, comprising: the step (a) of forming a first insulating film over a semiconductor substrate; the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film; the step (c) of forming an oxidation-resistant conductor film covering the top of the interconnect layer; the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film; the step (e) of forming a third insulating film on the second insulating film; the step (f) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located over the interconnect layer until the oxidation-resistant conductor film is exposed in one step; and the step (g) of removing the photoresist.

EX1004, Table I; EX1001, cl. 1. Though not shown in Table 1, Parikh discloses photoresist is used for etching the dielectric layers and removed thereafter. EX1004, [0006], [0031].

51. In the multi-layer structure of Parikh, “lines and vias are patterned at different levels and then filled with a conductive material such as copper.” EX1004, [0005]. Parikh also teaches that the lines and vias are formed by one-step or two-step etching of the dielectric layers until the metal passivation layer is exposed. *Id.*, [0026]-[0027].

52. In Figure 7 below with annotation added, the line and via openings are filled with conductive materials 250 and 260. EX1004, Fig. 7. Further, because the metal passivation layers 220 are conductive, conductive elements 208 are electrically connected to the lines and vias. *Id.*, [0018], Fig. 7. The metal passivation

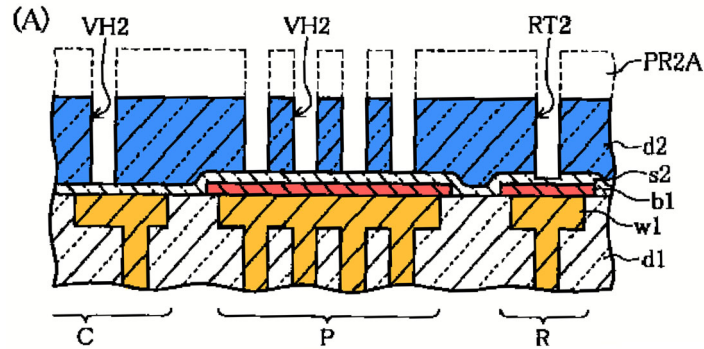
layers 220 inhibit metal (e.g., copper) diffusion into the ILD from the conductive elements 208 and protect the conductive elements 208 from being etched during the formation of the line and via openings. *Id.*, [0018], [0026].



EX1004, Fig. 7.

2. Komada

53. Komada discloses a method of semiconductor fabrication. EX1005, Abstract, [0001], [0035]. As shown in the annotated figure below, Komada's method includes (a) depositing a dielectric layer d1 on a substrate, (b) forming **conductive elements w1** in the dielectric layer d1, (c) generating **an upper conductive barrier layer b1** formed of oxidation-resistant materials (e.g., TaN/TiN) on **the conductive elements w1** and dielectric layer d1; (d) forming **dielectric layers d2** on **the upper conductive barrier layer b1**; (e) etching via holes (VH) and ring trenches (RT) using photoresist as a mask. *See e.g.*, EX1005, Fig. 3(A), [0062]-[0076], [0093]-[102].



EX1005, Fig. 3(A).

54. Komada further discloses a moisture resistant ring that “surrounds the circuit region in a loop.” EX1005, [0006], [0005], [0018], [0020]. The moisture resistant ring is formed through “an etching process performed at the same time as the etching performed to form via holes in the interlayer insulating layer, and then by filling the ring trench with an interconnection layer ...” *Id.*

3. Combination of Parikh and Komada

55. I have considered the teachings of Parikh and Komada and have determined that a POSITA would have been motivated to combine Komada with Parikh. Parikh describes metal passivation layer 220 that can be formed from titanium nitride (TiN). EX1004, [0019]. It also describes using photoresist as a mask when forming via openings. EX1004, [0006], [0031]. Like Parikh, Komada discloses (1) using TiN to form a conductive, oxidation-resistant layer, and (2) using a photoresist pattern as a mask to create openings. EX1005, [0004], [0016], [0023]. It further teaches forming a ring trench around the circuit region, such as Parikh's

core region, with a predictable benefit of protecting the core region from moisture permeation. EX1005, [0005]-[0006], [0048].

56. In my opinion, a POSITA would have been motivated to combine these references for several reasons. **First**, both Parikh and Komada are in the same field as the '572 patent and focus on semiconductor device fabrication, specifically the formation and protection of metal interconnects, including the use of barrier or oxidation-resistant layers. The '572 patent addresses the problem of maintaining the integrity of copper interconnects during manufacturing, which is also a concern in both Parikh and Komada. EX1001, 1:55-60, 2:53-56; EX1004 [0007]; EX1005, [0004], [0014], [0061]. Parikh discusses selective deposition of metal passivation layers to protect copper and improve reliability, while Komada details the use of a conductive antioxidant film, such as TiN, to prevent oxidation and enhance device performance. EX1004 [0009], [0018], [0032]; EX1005 [0004], [0014], [0061]. These solutions are relevant to the '572 patent's problem of protecting copper during fabrication. Thus, both Parikh and Komada are reasonably pertinent to the problems faced by the '572 patent and are analogous. *See e.g.*, EX1001, Abstract; EX1004, Abstract, [0002]; EX1005, [0001].

57. **Second**, a POSITA would have recognized that Parikh and Komada solve similar problems with similar methods. For example, both references recognize that in conventional devices, when the overall vertical distance between

two interconnect layers remains unchanged, etch stop films can undesirably increase capacitance, and complicate integration. EX1004, [0008] (“the etch stop layer usually has a higher dielectric constant than the dielectric material.”); EX1005, [0027] (“A thicker etching stopper layer 122 increases the associated capacitance between the interconnect lines within the same layer.”). Both references propose adding a barrier layer or a passivation layer on the conductive element to eliminate the need for an etch-stop film. EX1004, [0002] (“embodiments relate to forming metal interconnects without etch stops.”), [0026] (“the via etch will stop on the metal passivation layer 220”), [0022]; EX1005, [0004], [0016] (“...the antioxidant film covers the surface of the Cu interconnect so as to act as an etching stopper.”), [0059] (“Said upper conductive barrier layer 18 acts as an etching stopper layer when a trench for the moisture-resistant ring is etched into the upper layer.”).

58. As another example, both references emphasize the use of copper for interconnect elements due to its superior electrical conductivity. EX1004, [0007] (“copper is a better material for interconnect lines and Vias because of its low resistivity property”); EX1005, [0010] (“it has been proposed to use metals with high melting points, such as Cu, which have lower resistivity than Al, as interconnect materials”). Both references acknowledge the problem that copper can readily diffuse through dielectric layers, degrading device performance, necessitating a layer to inhibit diffusion. EX1004, [0017]-[0018] (“A conductive material 208, such

a copper, is then deposited over the barrier layer 206 to fill the feature 202...The metal chosen for the metal passivation layer 220 is required to be a barrier to diffusion of the conductive material 208.”); EX1005, [0016] (“It should be noted that Cu, by nature, is diffused in the insulating layer”).

59. Moreover, Parikh and Komada recognize the benefits of using metal nitrides, such as TiN, in a layer that reduces copper diffusion and mitigates the risk of over-etching. EX1004, [0032] (“One purpose of the metal passivation layer is to prevent the conductive metal from diffusing into the dielectric.”), cl. 10 (“wherein selectively depositing a metal passivating layer comprises selectively chemical vapor depositing a metal selected from the group consisting of tungsten, tantalum nitride, titanium nitride, titanium silicon nitride, or a combination thereof”); EX1005, [0016] (“In order to prevent the diffusion of Cu, a barrier layer formed of TiN, TaN, etc., is formed”). Thus, it is my opinion that a POSITA would have applied Komada’s teachings when implementing the semiconductor manufacturing process of Parikh, and would have understood the benefits of doing so, as described in detail below regarding claims 1 and 4-7.

60. In my opinion, a POSITA would have had a reasonable expectation of success in combining these teachings, as both references describe compatible materials (e.g., TiN, Cu) and process steps (e.g., use of photoresist masks, and damascene etching and filling). Thus, the combination would have involved the

application of known technologies according to known methods, yielding predictable results such as improved etch selectivity, reduced capacitance, and enhanced reliability by inhibiting copper diffusion.

4. Claim 1

(i) [1.pre] A method for fabricating a semiconductor device, comprising

61. I understand that these features are preambles of claim 1. I have been asked to assume that these preambles are limiting. Under that assumption, Parikh discloses this preamble. Parikh generally describes “the formation of structures on a substrate.” EX1004, Field of the Invention, [0002]. It teaches a method of “forming dual damascene structures on a substrate with increase[sic] reliability and performance.” *Id.*, [0009]; *see also id.*, Abstract, Table I, Fig. 5, [0035]. In addition, Parikh describes “FIG. 1A illustrates a planarized semiconductor substrate 100 having a bottom layer 110 that includes conductive elements 112.” EX1004, [0006]. And, claim 1 of Parikh recites, in part, “A method of forming a structure on a substrate....” EX1004, claim 1. The method disclosed in Parikh is nearly identical to claim 1 of the ’572 patent.

TABLE I

Station	Processing Step
820	Forming a conductive element on a substrate comprising a first dielectric layer and one or more conductive material embedded in the first dielectric layer
822	Selectively depositing a metal passivation layer on the conductive element
824	Depositing a second dielectric layer over the metal passivation layer and the first dielectric layer
826	Depositing a third dielectric layer over the second dielectric layer
828	Forming a via in the second dielectric layer
830	Forming a line in the third dielectric layer
832	Depositing a conductive material in the line and the via

CLAIM 1

A method for fabricating a semiconductor device, comprising:

the step (a) of forming a first insulating film over a semiconductor substrate; the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film; the step (c) of forming an oxidation-resistant conductor film covering the top of the interconnect layer; the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film; the step (e) of forming a third insulating film on the second insulating film; the step (f) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located over the interconnect layer until the oxidation-resistant conductor film is exposed in one step; and the step (g) of removing the photoresist.

EX1004, Table I; EX1001, Claim 1.

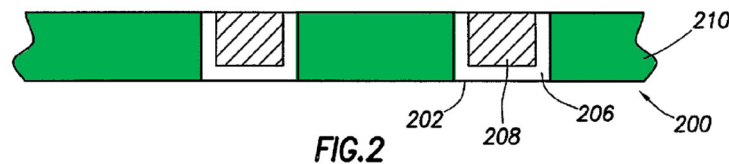
62. The disclosed method in Parikh focuses on a process that eliminates the need for traditional etch stop layers. EX1004, Title (“Selective metal passivated copper interconnect with zero etch stops”), [0010], Abstract. This approach is designed to improve the reliability and performance of integrated circuits by reducing overall capacitance and simplifying the manufacturing process. *Id.*, [0008]-[0009].

Another factor that determines IC performance is capacitance. Lower capacitance is ideal because it reduces crosstalk between the metal lines. One way to reduce capacitance of the IC is to use dielectric materials with a low dielectric constant. In a dual damascene structure, the etch stop layer usually has a higher dielectric constant than the dielectric material. The prior art dual damascene example above contains two etch stop layers 120, 140. Thus, it would be desirable to eliminate the etch stop layer.

63. Thus, Parikh discloses Claim [1.pre].

(ii) [1.a] the step (a) of forming a first insulating film over a semiconductor substrate

64. In my opinion, Parikh discloses “forming a first insulating film over a semiconductor substrate” as claimed. For example, Parikh states that “[e]mbodiments of the present invention generally relate to the formation of structures on a substrate.” EX1004 [0002]. In Parikh, a first dielectric layer 210 is one of those structures that are formed on the substrate 200. EX1004, [0017]. Parikh explains, with reference to Fig. 2, that “a first dielectric layer 210 is initially deposited.” EX1004, Fig. 2, [0017]. In Fig. 2, Parikh illustrates the first dielectric layer 210 formed on the substrate 200. EX1004, Fig. 2.



EX1004, Fig. 2.

65. In Station 820 of Table I, Parikh describes “forming a conductive element *on a substrate* comprising a first dielectric layer and one or more conductive material embedded in the first dielectric layer.” EX1004, Table I, ¶¶ [0034]-[0036].

TABLE I

Station	Processing Step
820	Forming a conductive element on a substrate comprising a first dielectric layer and one or more conductive material embedded in the first dielectric layer
822	Selectively depositing a metal passivation layer on the conductive element
824	Depositing a second dielectric layer over the metal passivation layer and the first dielectric layer
826	Depositing a third dielectric layer over the second dielectric layer
828	Forming a via in the second dielectric layer
830	Forming a line in the third dielectric layer
832	Depositing a conductive material in the line and the via

EX1004, Table I.

66. The process begins with the preparation of a substrate, which serves as the foundational platform for subsequent device fabrication. *Id.*, [0002] (“Embodiments of the present invention generally relate to the formation of structures on a substrate.”) This substrate may be a silicon wafer or another suitable semiconductor material, and it is typically planarized to ensure a flat and uniform surface. *See supra* § VII.A; EX1010, xv-xix, 107, 474. The substrate may already include previously formed dielectric and conductive layers from earlier process steps, depending on the complexity and integration level of the device being manufactured. *Id.* The initial preparation ensures that the substrate is ready to receive additional dielectric and conductive structures in a controlled and repeatable manner. EX1004, [0017].

67. Following substrate preparation, a first dielectric layer is deposited over the substrate. EX1004, [0017]. This dielectric layer is generally formed using chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), or other suitable deposition techniques. *Id.*, [0024]. The dielectric material may be silicon oxide, doped silicon oxide, or other low-k materials, selected for their electrical insulation properties and compatibility with subsequent processing. *Id.* The thickness and composition of this dielectric layer are tailored to provide the necessary electrical isolation and mechanical support for the conductive elements that will be embedded within it. *Id.*, Abstract, [0017, [0024].

68. In my opinion, a POSITA would have understood that Fig. 2 of Parikh shows that the first dielectric layer is formed on the substrate. Afterall, it is well known in the art that a substrate wafer needs to be prepared before depositing any dielectric layer on it. *See supra* §§VII.A, VII.B.

69. It is established in the field that a dielectric layer is characterized by its low electrical conductivity, thereby serving as an electrical insulator between conductive elements. EX1019, 370 (“Dielectric layers such as silicon dioxide and silicon nitride are used for insulation between conducting layers”); 378 (“Deposited dielectric films are used mainly for insulation and passivation of discrete devices and integrated circuits.”); EX1010, 205 (“Dielectric films, including silicon dioxide and silicon nitride, are used as the isolation, mask, and passivation layers.”).

70. A dielectric layer is considered an insulating film due to its inability to conduct electricity and its material properties that prevent free charge movement. EX1019, 370, 378; EX1010, 205. A dielectric layer functions as an insulating film because it does not conduct electricity and inhibits the movement of free charge carriers. EX1019, 370, 378; EX1010, 205. When a dielectric layer is deposited, it serves as an insulator that prevents electrical current from passing between conductive layers or components. EX1019, 370, 378; EX1010, 205. The distinction between the terms “dielectric layer” and “insulating film” is primarily a matter of terminology, rather than substantive technical difference. Thus, in my opinion, the choice of wording of “dielectric layer” or “insulating film” is largely wording preferences.

71. Therefore, a POSITA would have understood that the recited “first insulating film” is the disclosed “first dielectric layer 210,” the recited “semiconductor substrate” is the disclosed “substrate 200,” and the “first dielectric layer 210” is formed on the “substrate 200.” Thus, it is my opinion that Parikh discloses Claim [1.a]. *Id.*

(iii) [1.b] the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film;

72. In my opinion, Parikh discloses “forming an interconnect layer in at least an upper portion of the first insulating film” as claimed. In particular, Parikh

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

discloses depositing a **conductive material 208**, such as copper, in a recess feature 202 formed in an upper portion of the **first dielectric layer (insulating film)**. EX1004, [0017] (“[A] **first dielectric layer 210** is initially deposited. A feature 202 is then patterned and etched in the first dielectric layer 210 by a photolithography process. After the feature 202 is formed, a barrier layer 206 is deposited over the **first dielectric layer 210**. A **conductive material 208**, such as copper, is then deposited over the barrier layer 206 to fill the feature 202.”); Table 1, Fig. 2. As shown below in Fig. 2, the resulting **conductive material 208** is formed in an upper portion of the **first insulating film 210**. Thus, in my opinion, a POSITA would have understood that the recited “**interconnect layer**” is the disclosed “**conductive material 208**” and the recited “**insulating film**” is the disclosed “**first dielectric layer 210**.”



EX1004, Fig. 2.

73. The feature 202 is patterned and etched into the **first dielectric layer 210** using a photolithography process, thereby defining the regions where the conductive elements will be formed. EX1004, [0017]. After the feature is formed, a barrier layer 206 is deposited over the exposed surfaces of the **first dielectric layer 210** to prevent diffusion of the conductive material into the surrounding dielectric. *Id.*,

[0017], [0032]. Subsequently, a conductive material 208, such as copper, is deposited over the barrier layer 206, filling the patterned feature to create the desired conductive element. *Id.*, [0017]. Any excess conductive material is then removed through planarization processes, such as chemical mechanical polishing, resulting in a planarized surface with embedded conductive elements 206 and 208. *Id.*

74. In my opinion, a POSITA would have understood that conductive materials 206 and 208 function as interconnect layers because they provide the essential electrical pathways that connect various electronic elements within an integrated circuit. EX1004, [0004]. The primary purpose of these interconnect layers is to enable the transmission of electrical signals between different components of the device, such as transistors, capacitors, and external contact points. *Id.*

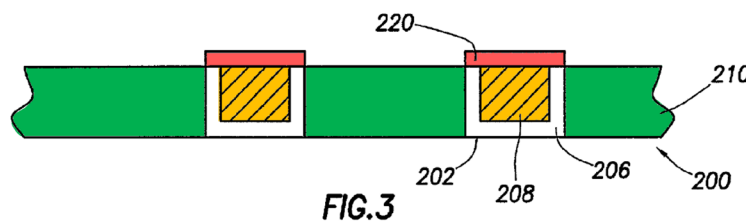
A key component of the IC is the interconnects. Interconnects provide the electrical connections between the various electronic elements of an IC and between these elements and the device's external contact elements, such as pins, for connecting the IC to other circuits.

Id., [0004]. By using materials like copper, which have low resistivity, the interconnect layers 206 and 208 ensure efficient signal conduction, reduced power loss, and improved overall circuit performance. *Id.*, [0004], [0008].

75. Thus, Parikh discloses Claim [1.b].

(iv) [1.c] the step (c) of forming an oxidation-resistant conductor film covering the top of the interconnect layer;

76. In my opinion, Parikh alone, or combined with Komada, teaches “forming an oxidation-resistant conductor film covering the top of the interconnect layer.”



EX1004, Fig. 3. Parikh discloses forming a metal passivation layer 220 on the conductor layer 208. *Id.*, [0018] (“a metal passivation layer 220 is formed on the conductive elements 206, 208 using a selective deposition process. The metal chosen for the metal passivation layer 220 is required to be a barrier to diffusion of the conductive material 208.”). The metal for the metal passivation layer 220 may include “tantalum nitride, titanium nitride, tungsten, titanium silicon nitride, titanium, tantalum, or a combination thereof.” *Id.*, [0019]; cl. 10 (“depositing a metal passivation layer comprises ... depositing a metal selected from the group consisting of tungsten, tantalum nitride, titanium nitride, titanium silicon nitride, or a combination thereof”).

77. I have determined that this understanding is also confirmed by the '572 patent's own description that the claimed oxidation-resistant conductor film may be made of titanium nitride. *See* EX1001, 16:8-9 ("The oxidation-resistant metal film 140 made of, for example, titanium nitride is provided . . ."). Therefore, according to the '572 patent, Parikh's **metal passivation layer 220**, made of the same material recited in the '572 patent (titanium nitride), is also an oxidation-resistant conductor film.

78. A POSITA would have understood that Parikh's **metal passivation layer** inhibits chemical reactions of the underlying metal layer, such as oxidation. *See also supra* § VII.C. Accordingly, a POSITA would have recognized the metal passivation layer is oxidation-resistant.

79. Additionally, it is known in the art that titanium nitride (TiN) has good conductive and anti-oxidation properties. *See supra* § VII.C. The metal passivation layer 220 serves a dual purpose of inhibiting the diffusion of conductive metal into the dielectric material and preventing over-etching into the metal conductive layer. The metal chosen for the metal passivation layer must act as an effective barrier to prevent diffusion of the underlying conductive material, such as copper, into adjacent dielectric regions. EX1004, [0018]. This is why claim 7 of Parikh states, "The method of claim 1, wherein the metal passivation layer is also barrier layer." *Id.*, cl. 7.

80. Therefore, it is my opinion that a POSITA would have understood from Parikh alone that the recited “oxidation-resistant conductor film” is the disclosed “metal passivation layer 220.”

81. I have determined that Komada confirms this understanding by expressly teaching that a film of TiN possesses good conductivity and anti-oxidation properties. EX1005, [0004] (“an anti-oxidation layer, such as a TiN layer, is also formed on the main Al or W interconnection layer to **prevent oxidation** of the interconnect pattern's surface”); cl. 2 (“The aforementioned first and second upper **conductive** barrier layers and the lower **conductive** barrier layer each include a layer formed of titanium, **a titanium compound**, tantalum, a tantalum compound, or a mixture thereof.”), [0069], [0086], [0093]. Accordingly, Komada recognizes that TiN is conductive and oxidation-resistant. In my opinion, a POSITA would have therefore understood that the recited “oxidation-resistant conductor film” is the disclosed “metal passivation layer 220” of Parikh, made of titanium nitride, as taught by Komada.

82. In my opinion, a POSITA would have been motivated to combine Komada and Parikh. *See also supra* § IX.A.3. In addition to the reasons explained in §IX.A.3, a POSITA would have recognized that the oxidation resistant and conductive properties of TiN, as taught by Komada, would have applied to the use of TiN in the metal passivation layer 220 of Parikh, at least because both references

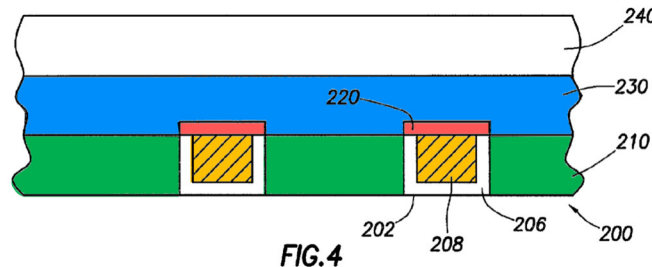
already use TiN in a similar manner. Both Komada and Parikh describe process flows (e.g., damascene and selective CVD) that are compatible with the deposition of TiN. Komada establishes the effectiveness and reliability of TiN as an anti-oxidation layer with conductive properties in copper interconnect technology, and Parikh explicitly contemplates its use for the same purpose. EX1005, [0004]; In my opinion, a POSITA would therefore have had a reasonable expectation of success in using TiN as the conductive, oxidation-resistant metal passivation layer 220 in Parikh, based at least on the compatible teachings of Komada and Parikh regarding the material's properties, deposition methods, and functional benefits in copper interconnect structures. Making the combination is nothing more than using a "known technique to improve similar devices (methods, or products) in the same way."

83. Therefore, Parikh alone, or with Komada, discloses Claim [1.c].

(v) [1.d] the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film;

84. In my opinion, Parikh discloses "forming a second insulating film on the first insulating film and the oxidation-resistant conductor film" as claimed. Referring back to Table I, Parikh discloses that, at station 824, "a second dielectric layer 230 is deposited over the metal passivation layer 220 and the first dielectric layer 210." EX1004, [0021], Fig. 4, Table I. Here, a POSITA would have

understood that Parikh's "second dielectric layer 230" is electrically insulative and thus is the claimed "second insulating film." *See supra* §IX.A.4(ii).



EX1004, Fig. 4.

TABLE I

Station	Processing Step
820	Forming a conductive element on a substrate comprising a first dielectric layer and one or more conductive material embedded in the first dielectric layer
822	Selectively depositing a metal passivation layer on the conductive element
824	Depositing a second dielectric layer over the metal passivation layer and the first dielectric layer
826	Depositing a third dielectric layer over the second dielectric layer
828	Forming a via in the second dielectric layer
830	Forming a line in the third dielectric layer
832	Depositing a conductive material in the line and the via

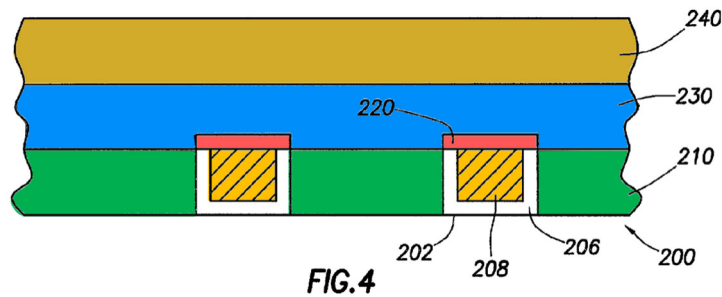
EX1004, Table I.

85. Thus, Parikh discloses Claim [1.d].

(vi) [1.e] the step (e) of forming a third insulating film on the second insulating film;

86. In my opinion, Parikh discloses "forming a third insulating film on the second insulating film" as claimed. Parikh discloses that "[a] third dielectric layer 240 is then deposited over the second dielectric layer 230 without depositing an etch stop layer between the two dielectric layers 230, 240." EX1004, [0023], Fig. 4,

Table I. Here, a POSITA would have understood that Parikh’s “third dielectric layer 240” is electrically insulative and is the claimed “third insulating film.” *See supra* §IX.A.4(ii).



EX1004, Fig. 4.

TABLE I

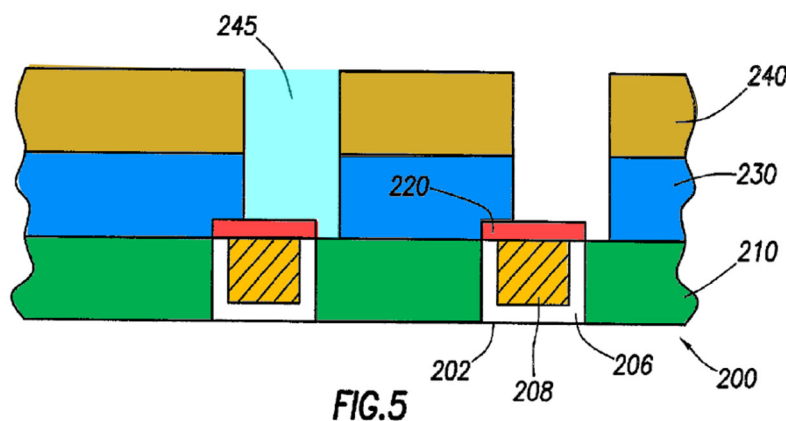
Station	Processing Step
820	Forming a conductive element on a substrate comprising a first dielectric layer and one or more conductive material embedded in the first dielectric layer
822	Selectively depositing a metal passivation layer on the conductive element
824	Depositing a second dielectric layer over the metal passivation layer and the first dielectric layer
826	Depositing a third dielectric layer over the second dielectric layer
828	Forming a via in the second dielectric layer
830	Forming a line in the third dielectric layer
832	Depositing a conductive material in the line and the via

EX1004, Table I.

87. Thus, Parikh discloses Claim [1.e].

(vii) [1.f] the step (f) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located over the interconnect layer until the oxidation-resistant conductor film is exposed in one step; and

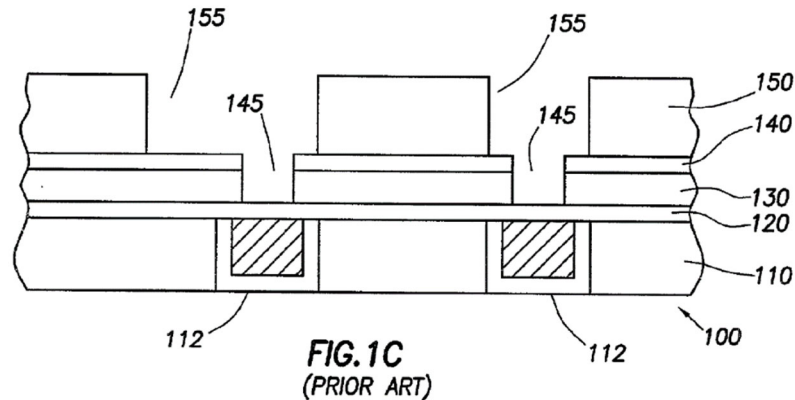
88. In my opinion, Parikh discloses “removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located over the interconnect layer until the oxidation-resistant conductor film is exposed in one step” as claimed. Parikh discloses forming a via opening by etching the second and third dielectric layers in one step. EX1004, [0025] (“the interconnect via 245 is first patterned and etched through the second dielectric layer 230 and third dielectric layer 240 to expose the top of the metal passivation layer 220.”), [0027] (“Alternatively, the via 245 may be etched in one step. ... [O]ne etch chemistry may be selected to effectively etch both the second and the third dielectric layers 230, 240”), Fig. 5.



EX1004, Fig. 5. As shown in Fig. 5, the one step etching operation removes portions of dielectric layers 240 and 230 located over the interconnect layer 208 “to expose

the top of the metal passivation layer 220.” EX1004, [0025] (“the interconnect via 245 is first patterned and etched through the second dielectric layer 230 and third dielectric layer 240 to expose the top of the metal passivation layer 220.”).

89. Parikh further teaches that via 245 is formed using a photoresist as a mask. In describing a conventional damascene process, Parikh discloses that a “photoresist layer (not shown) is formed over the second etch stop layer 140 and is patterned to define the vias 145.” EX1004, [0006]. “After the vias 145 are defined in the etch stop layer 140, the photoresist is removed.” *Id.* Parikh adds that layer 150 is then deposited and “[a]nother photolithography process is performed to define the lines 155 in the second dielectric layer 150 and the vias 145 in the first dielectric layer 130.” *Id.* A POSITA would have understood that Parikh’s “photolithography process” refers to depositing a photoresist layer on the second dielectric layer 150, patterning the photoresist layer, and using the photoresist layer as a mask to etch dielectric layers 150 and 130, resulting in the structure shown in Fig. 1C. EX1004, 1C, [0006]. A POSITA would have further understood that the photoresist is removed after “defining the lines 155 in the second dielectric layer 150 and the vias 145 in the first dielectric layer 130,” just as in the process for defining via 145 where “after the vias 145 are defined in the etch stop layer 140, the photoresist is removed.” *Id.* Thus, in my opinion, Parikh directly teaches using photoresist as a mask for via formation in the conventional damascene process.



EX1004, Fig. 1C.

90. In my opinion, a POSITA would have understood that the photoresist used as a mask to pattern via 145 in the conventional damascene process may also be used as a mask to pattern via 245. Indeed, Parikh describes via 245 “is first **patterned** and etched through the second dielectric layer 230 and third dielectric layer 240 to expose the top of the metal passivation layer 220.” EX1004, [0025]. A POSITA would have understood that the patterning and etching in forming via 245 uses photoresist as a mask, as in the conventional damascene process. Parikh further supports this by stating that the photoresist is removed after the features described and illustrated in Figures 2-6, including via 245, are formed. EX1004, [0031] (“After the features are formed and the photoresist is removed, a barrier layer is deposited.”). A POSITA would have reasonably recognized that the removal of a photoresist would be unnecessary unless it had first been used, such as to form via 245.

91. In addition, the numbering convention used in Parikh indicates that the formation of via opening 245 utilizes photoresist, akin to the formation of via opening 145. In the prior art, dielectric layers are designated as 110 and 130, whereas in the improved method, they are numbered as 220 and 230. EX1004, [0006], [0021], Figs. 1D, 6.

92. As stated above, a POSITA would have understood that photoresist is used in photolithography, where a light-sensitive photoresist coating is precisely exposed to a light pattern. EX1013, 662-664. This exposure creates a temporary reticle mask on the wafer's surface, mirroring the intended circuit design for a given layer. *Id.* 669-676. EX1013, Fig. 10.5.

93. Komada confirms that a POSITA would consider it obvious to employ the well-known and common approach of using photoresist as a mask to form openings. EX1005, [0023] (“a photoresist pattern PR is used as an etching mask to etch the interlayer insulating layer 123”), [0012] (“a photoresist pattern for via holes is formed on the insulating layer in the lower level; via holes are formed by means of etching”). Indeed, photoresist-based photolithography is a well-known and common approach for achieving the necessary resolution and alignment in these processes. A POSITA would have found it obvious to apply Komada's teachings regarding the use of a photoresist as a mask to define **via 245** of Parikh, aligning

with the rationale of applying a known method to improve similar devices in the same way.

94. In particular, both Komada and Parikh demonstrate that photoresist masking is a mature, reliable, and compatible technique for defining features. Both references describe manufacturing processes involving repeated cycles of deposition, patterning, and etching using photoresist as a mask in some embodiments. *See e.g.*, EX1004, [0006]; EX1005, [0003]-[0004]. Photoresist masks are easily integrated into these process flows and are compatible with the materials and chemistries described in both references. Additionally, using photoresist as a mask is a mature, well-understood technology that provides predictable results, aligning with the rationale of combining prior art elements according to known methods to yield predictable results. Given the explicit teachings of both references, a POSITA would have reasonably expected that using a photoresist as a mask to define **via 245** in Parikh would be successful.

95. Parikh alone, or with Komada, discloses Claim [1.f].

(viii) [1.g] the step (g) of removing the photoresist.

96. As discussed above, Parikh discloses using the photoresist. *See supra* §IX.A.4(vii). Parikh also discloses removing the photoresist. EX1004, [0031] (“the photoresist is removed”). A POSITA would have understood that the photoresist is engineered to act as a temporary stencil. *See supra* § VII.D. Typically, it is an

organic polymer that possesses none of the electrical or structural properties required of a finished semiconductor device. *Id.* Its continued presence would physically obstruct the subsequent deposition of new material layers and block the formation of electrical pathways between the circuit's vertically stacked components. *Id.*

97. Furthermore, leaving the photoresist on the wafer would usually lead to catastrophic device failure. *Id.* During subsequent high-temperature manufacturing steps, such as thermal annealing, the organic resist would decompose and release carbon and other impurities. *Id.* These contaminants would diffuse into the pristine silicon substrate, irreversibly altering its electrical characteristics and destroying the functionality of the transistors. *Id.* For these reasons, the removal of the photoresist, through a standard industry process known as ‘stripping’ or ‘ashing,’ is a step performed after a photolithography-based patterning cycle to ensure the device’s integrity and operability. *Id.*

98. Thus, Parikh discloses Claim [1.g].

5. Claims 2-3

(i) Claim 3. “The method of claim 1, wherein in the step (c), a film containing nitrogen is deposited, as the oxidation-resistant conductor film, on the interconnect layer.”⁹

99. In my opinion, Parikh alone, or combined with Komada, discloses depositing the oxidation-resistant conductor film on the interconnect layer. *See supra* §IX.A.4(iv). In addition to what I discuss above, Parikh further discloses that

“selectively depositing a metal passivation layer comprises selectively chemical vapor **depositing** a metal selected from the group consisting of tungsten, tantalum nitride, **titanium nitride**, titanium silicon nitride, or a combination thereof.”

EX1004, cl. 10 (“The method of claim 1, wherein selectively depositing a metal passivation layer comprises selectively chemical vapor depositing a metal selected from the group consisting of tungsten, tantalum nitride, titanium nitride, titanium silicon nitride, or a combination thereof.”); *see also* EX1005, [0004], [0016]. A POSITA would have understood that the disclosed film formed of **titanium nitride** is the recited “film containing nitrogen . . . as the oxidation-resistant conductor film.”

Thus, Parikh alone, or with Komada, discloses claim 3.

(ii) Claim 2. “The method of claim 1, wherein in the step (c), plasma treatment, wet treatment, or ion implantation is performed to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film”

100. In my opinion, Parikh alone, or combined with Komada, teaches that the metal passivation layer 220 (i.e., the recited oxidation-resistant layer) can be formed through electroless deposition. EX1004, cl. 8; *see supra* §IX.A.4(iv). A POSITA would have understood, based on background knowledge, that electroless deposition is a form of “wet treatment,” as claimed. The entire process of electroless deposition is conducted by submerging the substrate, which is the object to be coated, into a liquid chemical bath. *See supra*, §VII.B. EX1010, 315. This aqueous

solution contains the dissolved metal ions that will form the coating, as well as a chemical reducing agent. *Id.* The deposition of the solid metal film onto the substrate's surface is driven by a controlled, autocatalytic chemical reaction that occurs exclusively within this liquid medium. *Id.* The liquid is the essential environment that contains the reactants and facilitates the chemical reaction necessary for the coating to form. *Id.* Therefore, because electroless deposition must occur in a liquid chemical solution, a POSITA would have understood it as a wet treatment.

101. In addition, Parikh discloses using plasma treatment to form the oxidation-resistant conductor film. Parikh discloses using PVD to deposit TiN to form a barrier layer. EX1004, [0031]. Because Parikh teaches using the same material for metal passivation layer and using the metal passivation layer as the barrier layer, a POSITA would have understood that the metal passivation layer 220 could be formed in the same manner as the barrier layer 250. EX1004, [0019]; cls. 10, 7. As previously discussed, sputtering, which is a type of plasma treatment, is the primary technique employed in PVD processes for TiN deposition. *See supra*, § VII.B; EX1018, 1517 (“Conventionally, TiN films are deposited by physical vapor deposition (PVD) using reactive sputtering.”). Accordingly, a POSITA would have understood that Parikh teaches using sputtering, a plasma treatment, to introduce

nitrogen, thereby forming the oxidation-resistant conductor film. Therefore, a POSITA would have found that Parikh's PVD renders plasma treatment obvious.

102. As Parikh indicates that the metal passivation layer may function as a barrier layer, a POSITA would have found it obvious to use sputtering to introduce nitrogen into the upper portion of the interconnect layer. A POSITA would also have recognized that sputtering is a form of plasma treatment. *See supra* § VII.B; EX1013, 514; EX1011, 335-336. In reactive sputtering, an inert gas like argon is ionized to create a plasma, which then bombards a titanium target to release titanium atoms. *See supra* § VII.B; EX1013, 514; EX1012, 335-336. These atoms react with nitrogen in the plasma to form TiN, which deposits onto the substrate. *See supra* § VII.B; EX1013, 514; EX1012, 335-336. Plasma not only facilitates the sputtering and reaction processes but also enhances film adhesion and density through ion bombardment of the growing film. *See supra* § VII.B; EX1013, 514; EX1012, 335-336. Because plasma is essential for generating and controlling the energetic species involved in these deposition mechanisms, it is standard and expected in TiN PVD processes. *See supra* § VII.B; EX1013, 514; EX1012, 335-336. Therefore, the use of plasma in TiN deposition via PVD is considered obvious and conventional.

103. Therefore, Parikh alone, or combined with Komada, discloses claim 2.

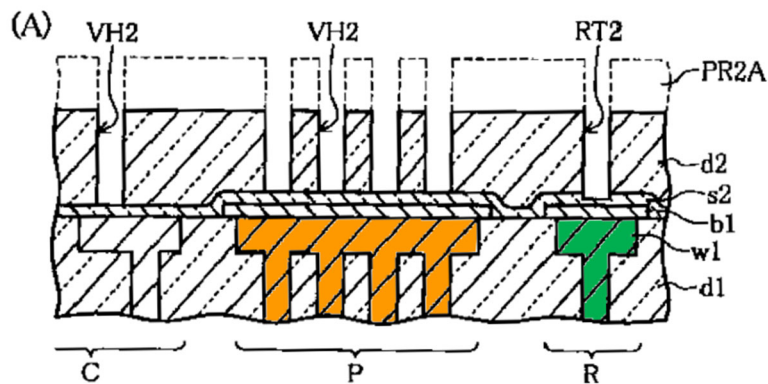
6. Claim 4

(i) [4.a] The method of claim 1, wherein in the step (b), a first interconnect layer and a second interconnect layer are formed as the interconnect layer,

104. In my opinion, the Parikh-Komada combination teaches this limitation.

Komada discloses multiple interconnect layers formed as the interconnect layer.

EX1005, Fig. 3A.



EX1005, Fig. 3A.

105. Komada discloses forming a “**first wiring structure W1 in the pad portion P**” and another “**first wiring structure w1 in the moisture-resistant ring R.**” EX1005, [0063]; *see also id.*, [0006] (“A moisture-resistant ring is formed by forming a ring trench that surrounds the circuit region in a loop, doing so through an etching process performed at the same time as the etching performed to form via holes in the interlayer insulating layer, and then by filling the ring trench with an interconnection layer formed through a interconnect formation step for patterning.”), [0029] (“The first interconnection layer, w1, is embedded in the interlayer insulating

layer d1 with one layering surface.”), cl. 1 (“A first conductive layer embedded in the aforementioned first insulating layer, said first conductive layer comprising a first interconnection layer, a first pad layer, and a first moisture-resistant ring layer. ... A second conductive layer embedded and thus formed in the aforementioned second insulating layer, said second conductive layer comprising a second interconnection layer as well as a second pad layer and a second moisture-resistant ring layer.”), cl. 3, Fig, Fig. 3A.

106. A POSITA would have understood that the recited “first interconnect layer” is the disclosed “wiring structure w1 in the moisture-resistant ring R” and that the recited “second interconnect layer” is the disclosed “wiring structure W1 in the pad portion P” which collectively form the recited “interconnect layer”. A POSITA would have understood that, optionally for convenience, the ring trench for the moisture-resistant ring could be etched in the same manner and at the same time as the formation of the via openings 245. Therefore, a POSITA would have found that the Parikh-Komada combination teaches a first interconnect layer and a second interconnect layer.

107. A POSITA would have been motivated to combine Parikh and Komada. As explained in IX.A.3, a POSITA would have found it obvious to incorporate Komada’s ring trench to surround Parikh’s core region. It was known in the art that a ring trench can be added along the periphery of core components to reduce

moisture permeation and enhance structural strength. *See supra* §§IX.A.2, 3.

Komada's ring trench provides the benefit of inhibiting moisture ingress, which can otherwise degrade device performance and reliability, especially as device geometries shrink and interconnects become more vulnerable. A POSITA would have understood that combining Komada's ring trench with Parikh's device would have involved applying a known technique (e.g., Komada's ring trench) to improve similar devices (e.g., multi-layer semiconductor structure on a substrate) in the same way.

108. A POSITA would have further understood that the ring trench may have been used in Parikh to improve the same type of device—a semiconductor structure that includes multiple interconnect layers formed using a damascene process—by sealing the porous dielectric layers to inhibit moisture ingress, in the same way as in Komada. The process for forming the ring trench in Komada—patterning with a photoresist, etching the insulating layer, and filling the trench with a conductive material—mirrors the damascene techniques used to form vias and interconnects, in Parikh. As the process steps for forming the ring trench in Komada are the same as those used to form vias and interconnects in Parikh, a POSITA would have found a high degree of process compatibility between these references. The materials used (e.g., copper, TiN, dielectric layers) are also common to both references, thereby supporting material compatibility between these references.

109. A POSITA would have had a reasonable expectation of success in combining the ring trench of Komada with Parikh, based at least on the compatibility of materials, process steps, and underlying objectives of both references. In particular, both references contemplate the use of similar dielectric and conductive materials, and both employ photolithographic and etching techniques that are industry standard.

110. For example, Komada's moisture-resistant ring is formed by etching a trench in the interlayer dielectric and filling it with a conductive material such as copper, often in conjunction with barrier layers, like TiN. EX1005, [0011], [0014]. Parikh's device structure similarly relies on copper interconnects, barrier layers, and low-k dielectrics, and employs standard photolithography, etching, and chemical mechanical polishing (CMP) steps. EX1004, [0017-0033]. The process steps for forming the moisture-resistant ring in Komada align with those used for forming vias and interconnects in Parikh, indicating a high degree of process compatibility.

111. In addition, Parikh's disclosure, which utilizes damascene processing, is compatible with the addition of a ring trench. For example, the moisture-resistant ring in Komada is located at the periphery of the chip, surrounding the active circuit region, and is not intended to interfere with the core interconnect or via structures. EX1005, [0018]. Parikh's architecture allows for the addition of such a peripheral feature, as Parikh's dual damascene process can accommodate additional patterned

features in the dielectric layers. There is no indication in Parikh of any device structure, material, or process constraint that would be incompatible with the introduction of a ring trench at the chip periphery.

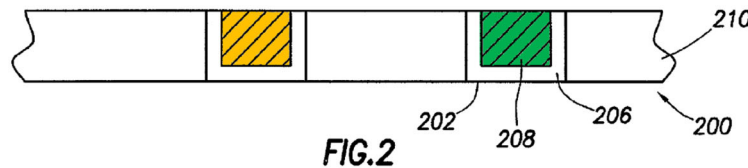
112. In my opinion, a POSITA would have had a reasonable expectation of success in combining the ring trench of Komada with Parikh, based at least on the compatibility of materials, process steps, and underlying objectives of both references. Both references contemplate the use of similar dielectric and conductive materials, and both employ photolithographic and etching techniques that are industry standard. Given the shared technological context and the predictability of results when combining Komada's ring trench with Parikh, a POSITA would have reasonably expected such a combination to be successful.

113. Additionally, or alternatively, a POSITA would have been motivated to implement this limitation in view of Parikh and found it obvious to do so. For example, Parikh discloses at least two instances of conductive material 208. *See supra* §IX.A.4(iii); EX1004, [0017]. A POSITA would have understood that the recited first interconnect layer is either the left or the right instance, with the other mapping to the second interconnect layer because the two instances share the same structure. For the ease of discussion, the **right conductive material 208** maps to the first interconnect layer and the **left conductive material 208** maps to the second

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

interconnect layer, while a POSITA would have understood that reversing this mapping does not alter the underlying principle.



EX1004, Fig. 2.

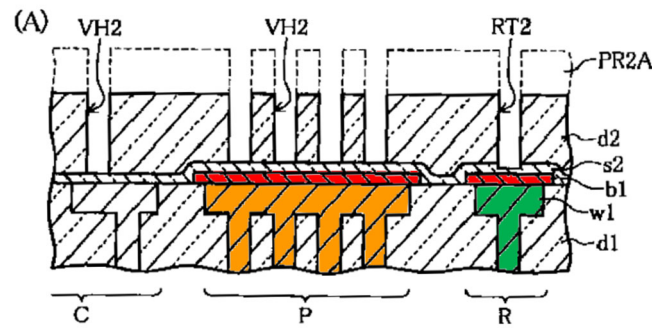
114. Therefore, the Parikh-Komada combination discloses Claim [4.a].

(ii) [4.b] in the step (c), an oxidation-resistant conductor film is formed on the first interconnect layer and the second interconnect layer, and

115. In my opinion, the Parikh-Komada combination teaches this limitation.

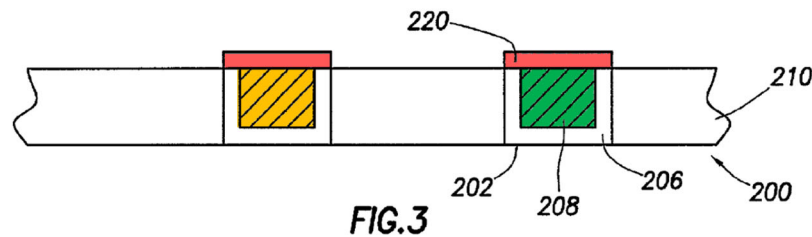
see also, §IX.A.4(iv).

116. As shown in Figure 3 below, Komada discloses forming a **conductive barrier layer** (the recited “oxidation-resistant conductor film”) on each the **first interconnect** and **second interconnect material** (the recited “interconnect layer”). *See also supra* §IX.A.4(iv); EX1005, Fig. 3A, [0064] (“The first **upper conductive barrier layer b1** is formed on the first interlayer insulating layer d1 so as to cover **the pad pattern** and **moisture-resistant ring pattern** of the first interconnect structure w1.”).



EX1005, Fig. 3A. As discussed above, a POSITA would have been motivated to combine Komada with Parikh. *See supra*, §§IX.A.3, IX.A.6(i).

117. Parikh alone also discloses forming a metal passivation layer (oxidation-resistant conductor film) on each interconnect material (the recited “interconnect layer”). *See also supra* §IX.A.4(iv); EX1004, Fig. 3, [0017].



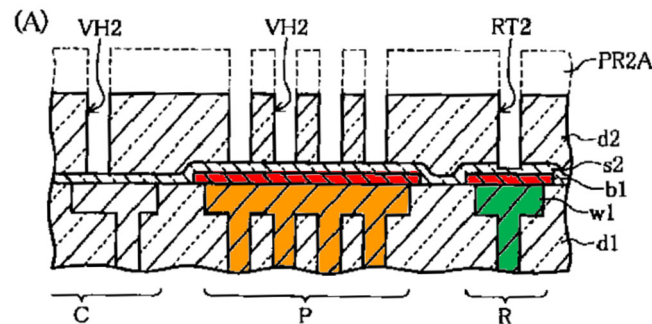
EX1004, Fig. 3.

118. Therefore, Parikh alone, or combined with Komada, discloses Claim [4.b].

(iii) [4.c] in the step (f), portions of the third insulating film and the second insulating film located over the first interconnect layer are removed to form a trench, and portions of the third insulating film and the second insulating film located over the second interconnect layer are removed to form a hole.

119. In my opinion, the Parikh-Komada combination teaches this limitation.

As shown in Figure 3A, Komada discloses forming a RT (ring trench) above the first interconnection layer w1 in the R region, and a VH (via hole) above first interconnection layer w1 in the P region. EX1005, [0064]-[0066].



EX1005, Figure 3A.

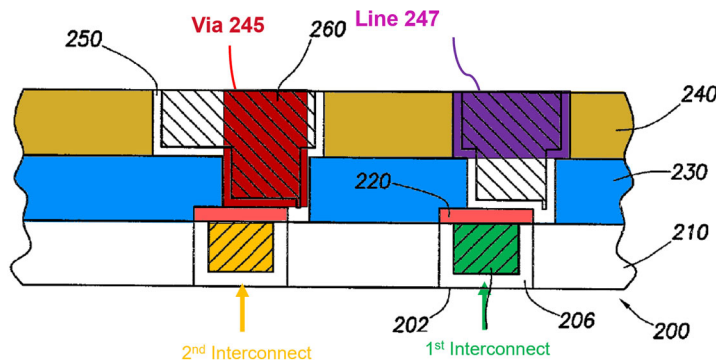
120. Furthermore, Parikh discloses forming via openings by etching through the second and third dielectric layers. EX1004, [0025] (“the interconnect via 245 is first patterned and etched through the second dielectric layer 230 and third dielectric layer 240.”), [0027] (“one etch chemistry may be selected to effectively etch both the second and the third dielectric layers 230, 240”), Fig. 5. A POSITA would have understood that the ring trench (RT) could be formed using the same process as the

formation of the via openings because the ring trench is as deep as the via openings 245, traverses the same dielectric layers, and exposes the same barrier layer. Both Komada and Parikh involve etching features (trenches or holes) into the same dielectric layer using similar photolithographic and etching steps, followed by filling these features with barrier and conductive materials through damascene or dual damascene processes. EX1005, [0007]; EX1004, [0005]. The technological processes—etching, barrier deposition, metal fill, and planarization—are the same for both the moisture-resistant ring and via openings, making it efficient and logical to fabricate them simultaneously using the same sequence of steps and materials. Accordingly, a POSITA would have found it obvious to remove portions of the second and third dielectric layers over the first interconnection layer to form the ring trenches. *See also supra* §IX.A.3

121. Additionally, or alternatively, a POSITA would have been motivated to implement this limitation in view of Parikh and found it obvious to do so. As discussed above, Parikh discloses forming first interconnect and second interconnect 208. *See supra* §IX.A.6(i). As shown in the figure below, Parikh discloses forming trench 260 over the first interconnect layer and via 245 over the second interconnect layer. EX1004, [0025] (“the interconnect via 245 is first patterned and etched through the second dielectric layer 230 and third dielectric layer 240 to expose the top of the metal passivation layer 220.”), [0028] (“After the interconnect vias 245

U.S. Patent No. 8,329,572

are etched and the metal passivation layers 220 are exposed, the interconnect lines 247 are patterned and etched.”). A POSITA would have understood that the recited trench is the disclosed “interconnect lines 247” and that the recited “hole” is the disclosed “interconnect vias 245.”



EX1004, Fig. 7. While Figure 7 appears to suggest that the line 247 requires removing only the third insulating layer, a POSITA would have understood that trenches may have different depths in order to serve different purposes (e.g., seal rings). When a deeper trench is needed, a POSITA would have understood that the second and third insulating layers need to be removed.

122. The Parikh-Komada combination discloses forming a Ring Trench (RT) above the first interconnect layer and forming Via Holes 245 above the second interconnect layer. *See supra*, §§IX.A.3, IX.A.6(i).

123. Thus, the Parikh-Komada combination discloses Claim [4.c].

7. Claim 5

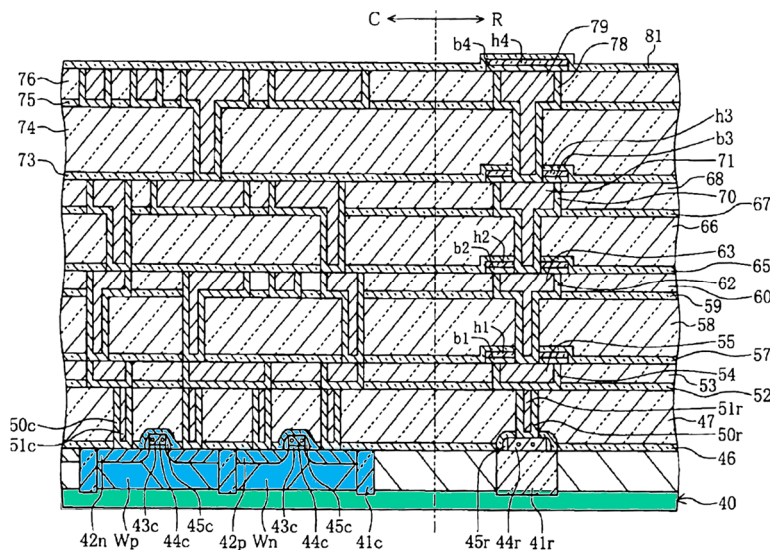
(i) The method of claim 1, further comprising, prior to the step (a), the step (h) of forming an element in the semiconductor substrate, wherein in the step (b), the interconnect layer is formed to be electrically connectable to the element

124. In my opinion, the Parikh-Komada combination teaches Claim 5. As an initial matter, a POSITA would have known that the multi-level interconnect structure of a chip provides electrical interconnection among various electric components inside the chip (e.g., transistors, resistors, etc.) and provides an electrical connection to components outside the chip. EX1011, 378-379, 444-445, 488-489. A POSITA would have understood that an interconnect layer is “electrically connectable” to elements in the semiconductor substrate of a chip. Figure 7 of Komada depicts a cross-sectional view of the circuit region and the moisture-resistant ring region of the semiconductor device. EX1005, [0084]. As shown, a MOSFET inverter (comprising p-well W_p, n-well W_n, n-type source/drain region 42n, p-type source/drain region 42p, Gate electrodes 44c, Shallow Trench Isolations 41c) is formed in the silicon substrate 40 prior to forming any other layers. EX1005, [0094]-[0098]. The MOSFET inverter is connected to the interconnect layer w1 (not shown) through conductive region 51c. EX1005, [0102]-[0103] (“one of the source/drain regions in an n-channel MOS transistor and one of the source/drain regions in a p-channel MOS transistor are connected to each other

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

through the interconnect in the first layer”). In my opinion, a POSITA would have understood that the recited “element in the semiconductor substrate” is the disclosed MOSFET inverter of Komada.



EX1005, Fig. 7.

125. A POSITA would have been motivated to implement this limitation in view of the combined teachings of Parikh and Komada, and found it obvious to do so. A POSITA would have understood that Parikh’s multi-layer structure would have incorporated the MOSFET inverter from Komada, and that, for the MOSFET inverter to function, the electrodes—Gate, Source, and Drain—would be connected to the interconnect(s). A POSITA would have understood that the recited “element in the semiconductor substrate” is therefore electrically connectable to the interconnect material 208.

126. In my opinion, a POSITA would have been motivated to combine Komada with Parikh. In addition to the reasons explained in §IX.A.3, a POSITA would have been motivated to add Komada's MOSFET inverter ("element in the semiconductor substrate") to Parikh's substrate because it is combining prior art elements according to known methods to yield predictable results. Forming a MOSFET inverter in a substrate is known in the art. Both Parikh and Komada concern forming an interconnect structure that is designed to electrically connect to elements in the substrate. A POSITA would have known that applying Komada's MOSFET to Parikh would yield predictable results (i.e., form the MOSFET in a substrate and electrically connect to an interconnect).

127. In addition, a POSITA would have understood that one purpose of the damascene structure described in Parikh is to connect an interconnect to elements in the substrate, such as Komada's MOSFET. *Id.* Indeed, Parikh itself suggests connecting an element, such as a MOSFET, to interconnects. EX1004, [0004] ("A key component of the IC is the interconnects. Interconnects provide the electrical connections between the various electronic elements of an IC and between these elements and the device's external contact elements, such as pins, for connecting the IC to other circuits. Typically, interconnect lines form the horizontal connections between the electronic elements while interconnect Vias form the vertical

connections between the electronic elements or between an electronic element and an external contact element.”)

128. A POSITA would have had a reasonable expectation of success in forming Komada’s MOSFET inverter within the substrate of Parikh and making it electrically connectable to an interconnect because both references disclose well-established, compatible semiconductor fabrication techniques. Komada details the formation of MOSFET inverters in a semiconductor substrate, and explicitly providing for their electrical connection to overlying interconnect layers through standard via and plug structures. EX1005, [0094]-[0098], [0103], Fig. 7. Parikh describes a process for forming interconnects and vias above a substrate to establish electrical connectivity to underlying conductive elements, which would include active devices such as MOSFETs. EX1004, [0004]. A POSITA would have recognized that combining such known elements using established methods would maintain their respective functions and achieve the intended electrical connectivity. Thus, based on the disclosures and the routine nature of the integration, a POSITA would reasonably expect the combination to function as intended.

129. Thus, the Parikh-Komada combination discloses Claim 5.

8. Claims 6-7

(i) [6.pre] A method for fabricating a semiconductor device, comprising:

130. I have been asked to assume that these preambles are limiting. Under that assumption, it is my opinion that the Parikh-Komada combination discloses the preamble. *See supra* § IX.A.4(i).

(ii) [6.a] the step (a) of forming a first insulating film over a semiconductor substrate;

131. It is my opinion that the Parikh-Komada combination discloses this limitation. *See supra* § IX.A.4(ii).

(iii) [6.b] the step (b) of forming a first interconnect layer and a second interconnect layer in at least an upper portion of the first insulating film;

132. It is my opinion that the Parikh-Komada combination discloses this limitation. *See supra* §§ IX.A.4(iii).

(iv) [6.c] the step (c) of forming an oxidation-resistant conductor film covering tops of the first interconnect layer and the second interconnect layer;

133. It is my opinion that the Parikh-Komada combination discloses this limitation. *See supra* § IX.A.4(iv); IX.A.6(ii).

(v) [6.d] the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film;

134. It is my opinion that the Parikh-Komada combination discloses this limitation. *See supra* § IX.A.4(v).

(vi) [6.e] the step (e) of forming a third insulating film on the second insulating film;

135. It is my opinion that the Parikh-Komada combination discloses this limitation. *See supra* §§ IX.A.4(vi).

(vii) [6.f] the step (f) of forming a trench pattern by removing portions of the third insulating film and the second insulating film located over the first interconnect layer, and forming a part of a hole pattern by removing portions of the third insulating film and the second insulating film located over the second interconnect layer; and

136. It is my opinion that the Parikh-Komada combination discloses this limitation. *See supra* § IX.A.4(vii); IX.A.6(iii).

(viii) [6.g] the step (g) of removing portions of the second insulating film located over the second interconnect layer until the hole pattern reaches the oxidation-resistant conductor film.

137. It is my opinion that the Parikh-Komada combination discloses this limitation. *See supra* § IX.A.4(vii); IX.A.6(iii).

(ix) Claim 7. The method of claim 6, wherein in the step (f), when the trench pattern is formed, portions of the third insulating film and the second insulating film located over the first interconnect layer are removed until the oxidation-resistant conductor film is exposed in one step.

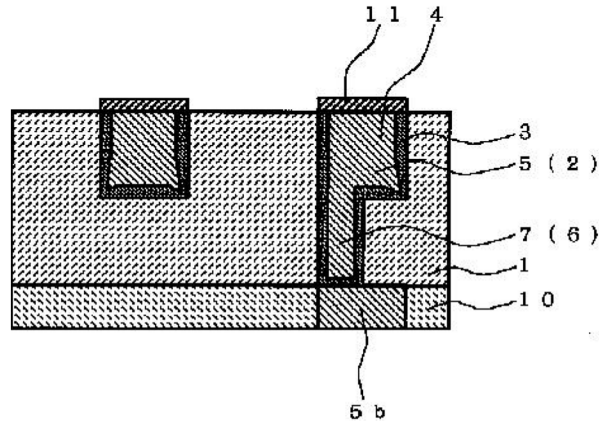
138. It is my opinion that the Parikh-Komada combination discloses this limitation. *See supra* § IX.A.4(vii).

B. Ground 2: Claim 2 Is Obvious Over Parikh, Komada, and Maeda

1. Maeda

139. Maeda discloses a method for semiconductor device fabrication. EX1006, Abstract. One objective of Maeda is to “prevent surface oxidation of interconnects formed through embedded interconnect technology to prevent an increase in the resistance and a decrease in the reliability.” EX1006, Abstract. Maeda provides a detailed method for forming an oxidation resistant layer on the interconnect layer. EX1006, Abstract, [0009] (“The semiconductor device according to the present invention enables the prevention of oxidation on the surface of the trench-type interconnect by forming an antioxidant film.”), [0020].

140. As shown in Figure 4 below, Maeda teaches forming an antioxidation film 11 over the interconnect material (4, 5, 6, 7). EX1006, [0047]-[0049], Fig. 1.



EX1006, Fig. 1. Maeda provides four working examples to achieve the same structure as described in Figure 1, each of which illustrates a variation of the method for forming the oxidation resistant layer. EX1006, [0025], [0038], [0047], [0050].

141. Notably, Maeda teaches forming the antioxidation film through a plasma treatment, an electroless plating method, or a selective CVD method. *Id.*, [0010], [0023].

2. Combination of Parikh, Komada, and Maeda

142. A POSITA would have understood that Maeda teaches a method for forming an anti-oxidation film “by irradiating nitrogen plasma” and that it would have been obvious to combine Maeda’s teaching with Parikh alone, or with Komada. EX1006, [0023];

143. A POSITA would have been motivated to combine the references for several reasons. **First**, the references are in the same field as the ’572 patent and directed to solving the same problem as each other and the ’572 patent. In particular,

all three references focus on semiconductor device fabrication, specifically the formation and protection of metal interconnects, including the use of barrier or oxidation-resistant layers. *See supra* §IX.A.3. Additionally, Maeda teaches forming an antioxidant film “on the surface of the trench-type interconnect in a self-aligned manner” to “prevent surface oxidation of interconnects formed through embedded interconnect technology to prevent an increase in the resistance and a decrease in the reliability.” EX1006, Abstract; [0001], [0005], [0007], Cl. 1. This parallels the ’572 patent’s concern with protecting metal interconnects using barrier or oxidation-resistant layers during semiconductor device fabrication. *See e.g.*, EX1001, Abstract; EX1004, Abstract, [0002]; EX1005, [0001].

144. **Second**, Parikh and Maeda aim to solve similar problems with similar methods. For example, both references emphasize the use of copper for interconnect elements due to its superior electrical conductivity. EX1004, [0007] (“copper is a better material for interconnect lines and Vias because of its low resistivity property,”); EX1006, [0018] (“it is preferable to use copper-based interconnect materials”). Both references acknowledge the problem that copper can readily diffuse into and through dielectric layers, necessitating a barrier layer. EX1004, [0007] (“copper is more difficult to etch than aluminum”); EX1006, [0005] (“Due to the surface oxidation, copper ions diffuse into the interlayer insulating film.”).

145. Parikh and Maeda recognize the benefits of using metal nitrides, such as TiN, to form a layer that reduces copper diffusion and mitigates the risk of over-etching. EX1004, cl. 10 (“depositing a metal selected from the group consisting of tungsten, tantalum nitride, titanium nitride, titanium silicon nitride, or a combination thereof”); EX1006, [0017] (“metallic barrier layer 3 may be a single film of a high-melting-point metal such as Ti, TiN, TiON, W, WN, TiW, TiWN, Ta or TaN, or a compound film thereof, or a laminate film thereof”).

146. **Third**, a POSITA would have found that the combination uses known techniques to improve similar devices in the same way. Using plasma treatment to introduce nitrogen is known in the art. *Id.* In Maeda, the plasma treatment is used to introduce nitrogen into the interconnect element to form an oxidation-resistant film that reduces oxidation and diffusion. EX1006, [0005], [0023], [0051]-[0052]. In addition, the benefit of plasma treatment was well known in the art. EX1014, 642 (“The nitrogen plasma bias treatment method makes it possible to form self-aligned TiN ... [and] requires fewer processing steps than the conventional two step annealing TiN/TiSi₂ formation technology does.”). In my opinion, a POSITA would have recognized that combining the teachings of Maeda and Parikh would improve the multi-layer structure of Parikh in the same way as achieved in Maeda. A POSITA would have understood that in the combination, the plasma treatment would have been used to introduce nitrogen into the conductive element to form an

oxidation-resistant film. *Id.* Using Maeda's plasma treatment to form Parikh's TiN metal passivation layers is advantageous due to its low-temperature, low thermal budget characteristics, particularly in scenarios where higher-temperature thermal processes may induce undesirable diffusion of the underlying copper layers. EX1012, 168.

147. A POSITA would have had a reasonable expectation of success in combining Maeda's teaching of forming an anti-oxidation film by irradiating nitrogen plasma with the copper interconnect processes described in Parikh and Komada. Maeda explicitly demonstrates that nitrogen plasma treatment can form a copper nitride film that prevents oxidation on the surface of the interconnect material. EX1006, [0048]-[0052]. Both Parikh and Komada already emphasize the importance of robust passivation/barrier layers to prevent copper diffusion and oxidation EX1004, [0010], [0018]; EX1005, [0016], [0017]. Nitrogen plasma treatment is a well-established, low-temperature, conformal process compatible with damascene flows, and is routinely used in semiconductor fabrication. Thus, a POSITA would have recognized that integrating this step into the existing process flows of Parikh would be technically straightforward and effective to yield the predictable result of protecting copper interconnects from oxidation.

3. Claim 2.

(i) The method of claim 1, wherein in the step (c), plasma treatment, wet treatment, or ion implantation is performed to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film.

148. In my opinion, the Parikh-Komada-Maeda combination, or the Parikh-Maeda combination discloses this claim. For example, Maeda discloses that the “anti-oxidation film 11 can be formed by irradiating the surfaces of the groove wirings 5 with nitrogen-containing plasma generated by various methods such as ICP (Inductive Coupled Plasma), ECR plasma, parallel-plate plasma, and magnetron plasma.” EX1006, [0023]; *see also id.*, [0027] (“Next, a Ti layer and a TiN layer were sequentially formed as the barrier metal layer 3 by magnetron sputtering in a high vacuum under the following film formation conditions (FIG. 2 b).”). A POSITA would have understood that this procedure involves creating and maintaining nitrogen-containing plasma on the surface of the wirings 5, bombarding the surface with energized ions such as nitrogen, thereby introducing nitrogen atoms into the upper portion of the wirings 5. Therefore, a POSITA would have understood that the recited “plasma treatment... performed to introduce nitrogen” is the disclosed method in Maeda of irradiating with nitrogen-containing plasma.

149. As explained above, a POSITA would have been motivated to combine Maeda with Parikh, and would have been motivated to combine Maeda with the

Parikh-Komada combination. *See supra* § IX.B.3. Thus, the Parikh-Maeda combination and/or the Parikh-Komada-Maeda combination discloses this claim.

C. Ground 3: Roberts, alone (3A) or in combination with Parikh (3B), renders obvious claims 1-3

1. Roberts

150. Roberts discloses forming a multi-layer structure on a substrate. The process includes “forming a recess in the dielectric layer (20) of a semiconductor substrate (10). A first capacitor electrode (30, 40) is formed in the recess having a copper first metal layer (30) with a conductive oxidation barrier (40) formed over the first metal layer (30). ... An insulator (50) is formed over the first capacitor electrode (30, 40)” and “an ILD 90 is deposited over the semiconductor substrate 10” EX1007, Abstract, 6:3-8, Fig. 10.

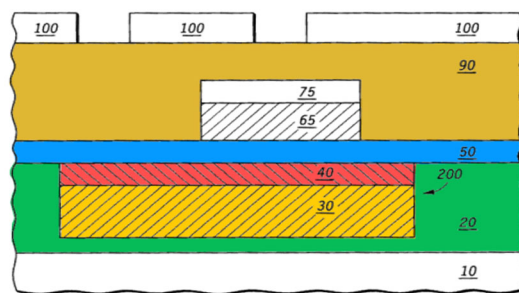


FIG.10

EX1007, Fig. 10 (annotated).

151. After the layers are formed, a photoresist layer 100 is deposited and patterned. EX1007, 5:63-66. The photoresist layer is then used as a mask to etch the dielectric layers 90 and to form a via opening 110. *Id.*, 5:62-6:22.

2. **Combination of Roberts and Parikh**

152. It would have been obvious to a POSITA to combine Parikh with Roberts at least because both references address the same technical challenges in copper metallization, teach compatible solutions involving barrier/passivation layers, and because the combination would predictably yield improved device reliability, manufacturability, and performance. As explained above, Parikh discloses a method for etching two insulating layers in a single step. *See supra*, §A.4(vii); EX1004, [0027]. A POSITA would have found it obvious to apply Parikh's one-step etching technique to the formation of via 110 in Roberts for several reasons.

153. **First**, both references are in the same field as the '572 patent because all three focus on semiconductor device fabrication, specifically the formation and protection of metal interconnects, including the use of barrier or oxidation-resistant layers. The '572 patent is concerned with maintaining the integrity of copper interconnects during manufacturing, which is also a concern in both Parikh and Roberts. EX1001, 1:55-60, 2:53-56; EX1004 [0007]; EX1007, 1:36-52. Parikh discusses selective deposition of metal passivation layers to protect copper and improve reliability, while Roberts details the use of conductive oxidation barrier layers to stabilize copper interfaces and enhance device performance. EX1004 [0009], [0018], [0032]; EX1007, 2:54-59, 4:62-67. These solutions are relevant to

the '572 patent's problem of protecting copper during fabrication. Thus, a POSITA would have concluded that both Parikh and Roberts are reasonably pertinent to the problems faced by the '572 patent. *See also e.g.*, EX1001, Abstract; EX1004, Abstract, [0002]; EX1007, Abstract, 1:17-19.

154. **Second**, a POSITA would have recognized that both references solve similar problems with similar methods, and that the combination represents the use of a known technique to improve similar devices in the same way because both references address the fabrication of multi-layer semiconductor damascene structures involving copper and dielectric layers. For example, both references are directed to the fabrication of semiconductor structures that utilize copper as a primary conductive material. EX1007, 1:31-33 ("Copper is replacing aluminum and aluminum alloys as the predominant material for metal interconnects in Semiconductor manufacturing."); EX1004, [0007] ("copper is a better material for interconnect lines and Vias because of its low resistivity property"). Both references identify the challenges associated with copper, specifically its tendency to oxidize and diffuse into surrounding dielectric materials, which can degrade device performance and reliability. EX1007, 1:42-47 ("Known problems with using copper as an electrode material include adverse effects caused by poor mechanical and chemical stability of the copper Surface, and other interactions of the copper with

the capacitor dielectric materials (e.g. copper diffusion).’); EX1004, [0007](“copper is more difficult to etch than aluminum”).

155. Roberts and Parikh both propose using a metal nitride layer over copper to address these challenges, by preventing copper oxidation and diffusion, thereby improving the interface stability and overall device reliability. EX1007, 2:54-59; EX1004, Abstract; [0018] (“The metal chosen for the metal passivation layer 220 is required to be a barrier to diffusion of the conductive material 208.”). Both references suggest a similar metal nitride for the barrier/passivation layer, including titanium nitride, which is well-known in the art for its effectiveness in preventing copper diffusion and oxidation. *See supra* VII.C; EX1007, 4:24-28 (“Materials that are both good oxidation and barrier layers to materials including copper are tantalum, titanium, platinum, iridium, aluminum, ruthenium, tungsten, tantalum nitride, titanium nitride, and the like.”); EX1004, cl. 10. Thus, a POSITA would have considered Parikh when implementing the manufacturing techniques of Roberts.

156. Moreover, both Roberts and Parikh explicitly recognize the importance of managing the interface between copper and dielectric materials to ensure device integrity and performance. *See e.g.*, EX1007, 2:54-59 (“By forming a conductive oxidation barrier layer 40 between the copper electrode 30 and the metal oxide 50 in accordance with the present invention, a MIM capacitor with a high capacitance

density and good adhesion between a metal oxide dielectric 50 and a copper electrode 30 is formed.”); EX1004, Abstract (“A metal passivation layer is selectively formed on conductive elements of the Substrate.”); [0018] (“The metal chosen for the metal passivation layer 220 is required to be a barrier to diffusion of the conductive material 208,” and that “[o]ne purpose of the metal passivation layer is to prevent the conductive material from diffusing into the dielectric.”); cl. 10 (“depositing a metal selected from the group consisting of tungsten, tantalum nitride, titanium nitride, titanium silicon nitride, or a combination thereof”). A POSITA would have determined that this shared focus on managing the interface between copper and dielectric materials further supports the compatibility and motivation to combine the teachings of Roberts and Parikh.

157. **Third**, a POSITA would have been motivated to apply Parikh’s “one-step” etching process to Roberts’ interlayer dielectric layer 90 and capacitance dielectric layer 50 because the combination exemplifies the rationale of “combining prior art elements according to known methods to yield predictable results.” Roberts already discloses that one chemistry may be used to etch both dielectric layers 90 and 50 and the etching process can be carried out in the same tool or even in the same chamber. EX1006, 5:62-6:14 (“Thus, the first chemistry needs to be selective to the ESL layer material and perhaps even the capacitor dielectric layer 50.”). Parikh explicitly teaches that the use of metallic nitride layers over copper enables

the elimination of etch stop layers, exposing the underlying structure “in one step”.

EX1004, [0027] (“the via 245 may be etched in one step”); [0028] (“After the interconnect vias 245 are etched and the metal passivation layers 220 are exposed, the interconnect lines 247 are patterned and etched.”). A POSITA would have recognized that, by etching multiple layers in one step, not multiple steps, the process is simplified, leading to increased efficiency, throughput and reduced cost. EX1004, [0029].

158. A POSITA would have recognized that the combination would yield predictable results at least because both references use compatible materials and processes. Both references apply a metallic nitride layer as a passivation, or a barrier, layer for protecting the underlying copper. EX1007, 4:24-28 (“Materials that are both good oxidation and barrier layers to materials including copper are tantalum, titanium, platinum, iridium, aluminum, ruthenium, tungsten, tantalum nitride, titanium nitride, and the like.”); EX1004, cl. 10 (“depositing a metal selected from the group consisting of tungsten, tantalum nitride, titanium nitride, titanium silicon nitride, or a combination thereof”).

159. Parikh teaches that this metal passivation layer, in addition to inhibiting diffusion, may also serve as an etch stop. EX1004, [0007] (“Taking advantage of dissimilar etch properties between the first and second dielectric layers 210, 230, the via etch will stop on the metal passivation layer 220 or the first dielectric layer 210

if misaligned.”). Both references acknowledge the problem that copper can readily diffuse through dielectric layers, necessitating a barrier layer. EX1007, 1:42-47 (“Known problems with using copper as an electrode material include adverse affects[sic] caused by poor mechanical and chemical stability of the copper surface, and other interactions of the copper with the capacitor dielectric materials (e.g. copper diffusion).”). Parikh further teaches that one-step etching involves selecting an etching chemistry for deposited dielectric layers with dissimilar etch characteristics, an approach also recognized in Roberts. EX1004, [0010], [0012], [0022], [0026], [0030]; EX1007, 5:62-14. Therefore, a POSITA would have understood that one-step etching is compatible with Roberts and can be performed without damaging the underlying copper. This compatibility of materials and processes would have led a POSITA to have a reasonable expectation of success in modifying Roberts’ fabrication process to include the one-step etching process of Parikh, as the combination would be expected to function as intended to achieve predictable results.

160. **Fourth**, the Roberts-Parikh combination represents the use of a known technique to improve similar devices in the same way because both references address the fabrication of multi-layer semiconductor damascene structures involving copper and dielectric layers. Etching multiple dielectric layers in one step is known in the art. *Id.* In Parikh, one chemistry is selected to etch both the second and third

dielectric layers. EX1004, [0027] (“one etch chemistry may be selected to effectively etch both the second and the third dielectric layers 230, 240.”). Similarly, Roberts also suggests that the first chemistry used to etch ILD layer 90 may not be stopped by the dielectric layer 50. EX1006, 5:62-6:14 (“Thus, the first chemistry needs to be selective to the ESL layer material and perhaps even the capacitor dielectric layer 50.”).

161. Parikh demonstrates that by engineering the dielectric stack so that adjacent layers have different etch rates, both multiple dielectric layers can be patterned and etched in a single step, which streamlines the dual damascene process, reducing process complexity and improving throughput and device performance. This compatibility of materials and processes would have led a POSITA to have a reasonable expectation of success in combining Parikh’s one-step etching process with Roberts’ fabrication process, as the combination would be expected to function as intended to achieve predictable results.

3. Claim 1

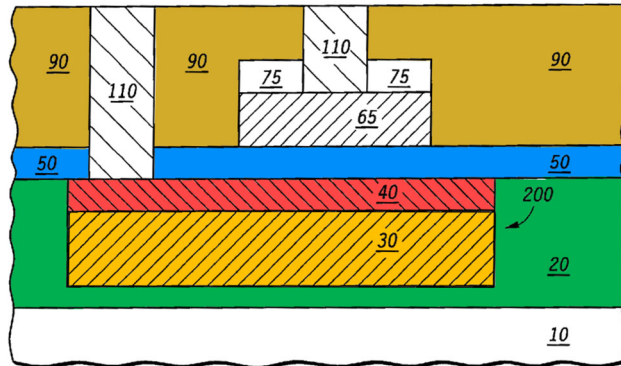
(i) [1.pre] A method for fabricating a semiconductor device, comprising

162. In my opinion, Roberts discloses the preamble. Roberts generally relates to “the field of semiconductor devices and more particularly to metal-insulator-metal (MIM) capacitors as used in semiconductor devices.” EX1007, Field of the Invention. Specifically, Roberts provides a method of forming a

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

semiconductor device comprising an MIM capacitor overlying a semiconductor substrate. EX1007, 3:5-9.



EX1007, Fig. 11 (annotated).

(ii) [1.a] the step (a) of forming a first insulating film over a semiconductor substrate

163. In my opinion, Roberts discloses this limitation. Roberts discloses “a dielectric layer 20 formed overlying a semiconductor substrate 10.” EX1007, 3:7-9, Fig. 1.

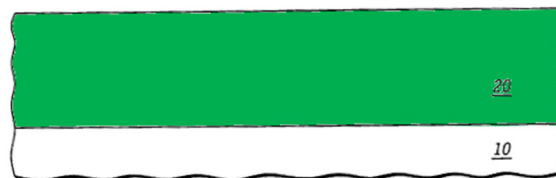


FIG.1

EX1007, Fig. 1 (annotated). In Roberts, the dielectric layer 20 “can be any dielectric material, such as silicon oxide.” *Id.*, 3:19-22.

164. A POSITA would have considered “a dielectric layer” as the claimed “insulating film.” A dielectric layer is considered an insulating film due to its inability to conduct electricity and its material properties that prevent free charge movement. *See supra*, § IX.A.4(ii); EX1019, 370, 378; EX1010, 205.

165. When a dielectric layer is deposited, it serves as an insulator that prevents electrical current from passing between conductive layers or components. *Id.* The choice of wording of “dielectric layer” or “insulating film” is largely wording preferences.

166. A POSITA would have understood the term “a dielectric layer” to correspond to the claimed “insulating film.” A dielectric layer functions as an insulating film because it does not conduct electricity and inhibits the movement of free charge carriers. *See supra*, § IX.A.4(ii); EX1019, 370, 378; EX1010, 205. Upon deposition, a dielectric layer acts as an electrical insulator, preventing current flow between adjacent conductive layers or components. *Id.* The distinction between the terms “dielectric layer” and “insulating film” is primarily a matter of terminology, rather than substantive technical difference.

167. Therefore, a POSITA would have understood that the recited “first insulating film” is the disclosed “the dielectric layer 20,” the recited “semiconductor substrate” is the disclosed “substrate 10,” and the “first dielectric layer 20” is formed on the “substrate 10.” Thus, Roberts discloses Claim [1.a].

(iii) [1.b] the step (b) of forming an interconnect layer in at least an upper portion of the first insulating film;

168. In my opinion, Roberts discloses this limitation. Roberts discloses forming a first metal layer 30 within an opening in the dielectric layer 20. EX1007, 3:25-28, Figs. 2-3.

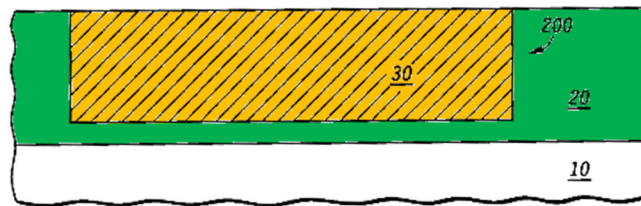


FIG. 3

EX1007, Fig. 3. In Fig. 3, the first metal layer 30 is formed in an upper portion of the dielectric layer 20. The first metal layer 30 can be copper or an aluminum copper alloy “deposited using PVD, CVD, atomic layer deposition (ALD), electroplating, combinations of the above or the like.” *Id.*, 3:30-35. As shown in the final device structure in Fig. 11, at least a portion of the first metal layer 30 does not overlap with the electrode 65. *Id.*, Fig. 11, 6:46-50.

169. In forming the structure shown in Fig. 3, “the dielectric layer 20 is patterned and etched to form an opening 200”; next, the first metal layer 30 “is formed over the dielectric layer 20 and within the opening,” and then planarization is carried out. EX1007, 3:24-42. As shown in Figure 3, the first metal layer 30 is located within the opening of dielectric layer 20 and thus “in an upper portion” of the dielectric layer 20.

170. A POSITA would have understood that the metal layer is the interconnect layer. Copper is widely used in modern integrated circuits specifically for interconnects due to its low resistivity and superior electromigration resistance. Metal layer 30 (copper electrode 30) serves as the bottom electrode of the metal-insulator-metal (MIM) capacitor. EX1007, Abstract (“A first capacitor electrode (30, 40)”), 1:34-36, 3:25-28. In integrated circuits, capacitor electrodes serve to connect the capacitor to the other components of the circuit, including the transistors located beneath them. EX1007, 3:12-15.

171. Therefore, a POSITA would have understood that the recited “interconnect layer” is the disclosed “first metal layer 30,” including the portion of the “first metal layer 30” that does not overlap with the electrode 65, and the recited “insulating film” is the disclosed “the dielectric layer 20” which a POSITA would have understood is an electrical insulator. EX1007, 4:39-44, 6:64-7:3. Thus, Roberts discloses Claim [1.b].

(iv) [1.c] the step (c) of forming an oxidation-resistant conductor film covering the top of the interconnect layer;

172. In my opinion, Roberts discloses this limitation. Roberts discloses forming a conductive oxidation barrier layer 40 as shown in FIG. 6. EX1007, 4:16-19, Figs. 5-6; 4:19-21 (“The conductive oxidation barrier layer 40 is deposited over the surface of the dielectric layer 20 and the recessed first metal layer 30.”).

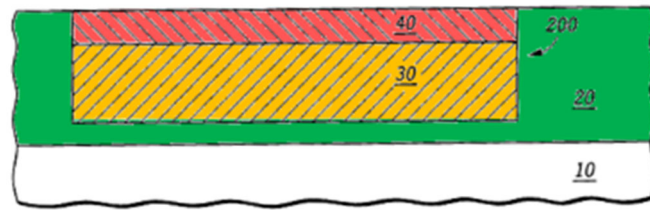


FIG. 6

EX1007, Fig. 6. The **conductive oxidation barrier layer 40** can be “any material that can serve as both an oxidation and barrier layer to the underlying **first metal layer 30**”—including “tantalum, titanium, platinum, iridium, aluminum, ruthenium, tungsten, tantalum nitride, titanium nitride, and the like.” *Id.*, 4:21-28.

173. Therefore, a POSITA would have understood that the recited “oxidation-resistant conductor film” is at least the disclosed “**conductive oxidation barrier layer 40**.”

174. Additionally, the '572 patent describes that the claimed oxidation-resistant conductor film may be made of titanium nitride. *See* EX1001, 4:11-15, 15:16-19, 16:8-9 (“The oxidation-resistant metal film 140 made of, for example, titanium nitride is provided...”). Therefore, according to the '572 patent, Roberts’ **conductive oxidation barrier layer 40**, made of the same material recited in the '572 patent (titanium nitride), is also an oxidation-resistant conductor film.

175. Thus, Roberts discloses Claim [1.c].

(v) [1.d] the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film;

176. In my opinion, Roberts discloses this limitation. After forming the conductive oxidation barrier layer 40, Roberts discloses forming “a capacitor dielectric layer 50 ... over the semiconductor substrate 10.” EX1007, 5:1-3. The capacitor dielectric layer 50 is “an insulator formed on the conductive oxidation barrier layer 40.” *Id.*, 5:3-7.

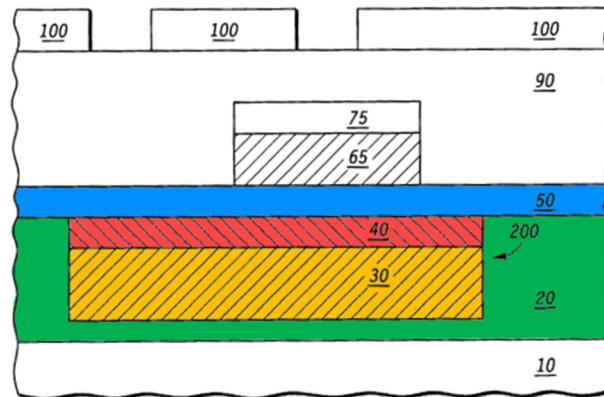


FIG.10

EX1007, Fig. 10. Also shown in Figure 10, the dielectric layer 50 is formed on the dielectric layer 20.

177. A POSITA would have understood that the recited “second insulating film” is the disclosed electrically insulative “dielectric layer 50.” Thus, Roberts discloses Claim [1.d].

(vi) [1.e] the step (e) of forming a third insulating film on the second insulating film;

178. In my opinion, Roberts discloses this limitation. Roberts discloses forming an interlayer dielectric (ILD) layer 90 (third insulating film) on the capacitor dielectric layer 50 (second insulating film). EX1007, 5:62-66, Fig. 10.

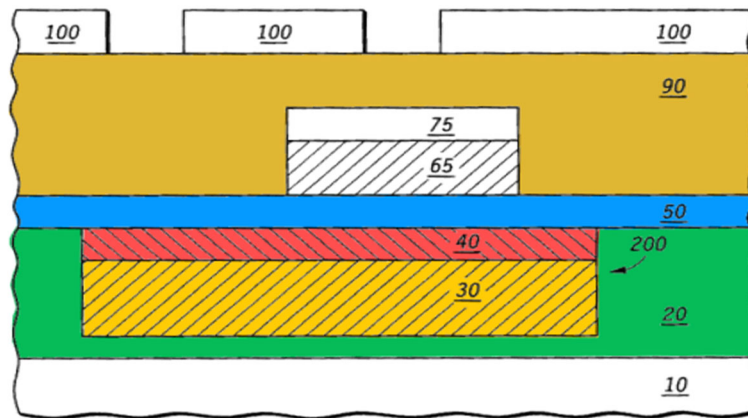


FIG. 10

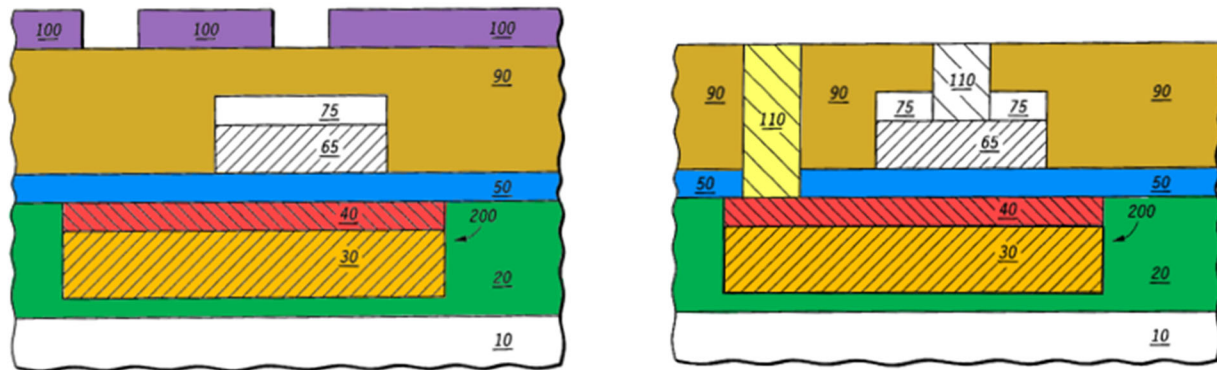
EX1007, Fig. 10 (annotated).

179. Therefore, a POSITA would have understood that the recited “third insulating film” is the disclosed “interlayer dielectric (ILD) layer 90.” Thus, Roberts discloses Claim [1.e].

(vii) [1.f] the step (f) of removing, using a photoresist as a mask, portions of the third insulating film and the second insulating film located over the interconnect layer until the oxidation-resistant conductor film is exposed in one step; and

180. In my opinion, Roberts discloses this limitation. First, Roberts discloses using a photoresist as a mask for etching the interlayer dielectric (ILD) layer 90 and capacitor dielectric layer 50 until the conductive oxidation-resistant

film 40 is exposed. EX1007, 5:62-66 (“a second photoresist layer 100 is deposited and patterned in order to etch the ILD layer 90 to form via openings, which are filled with metal to form conductive vias 110, shown in FIG. 11.”). Roberts further discloses etching the dielectric layers 90 and 50 until exposing the underlying conductive portions. EX1007, 6:15-18 (“expose underlying conductive portions”).



EX1007, Figs. 10-11.

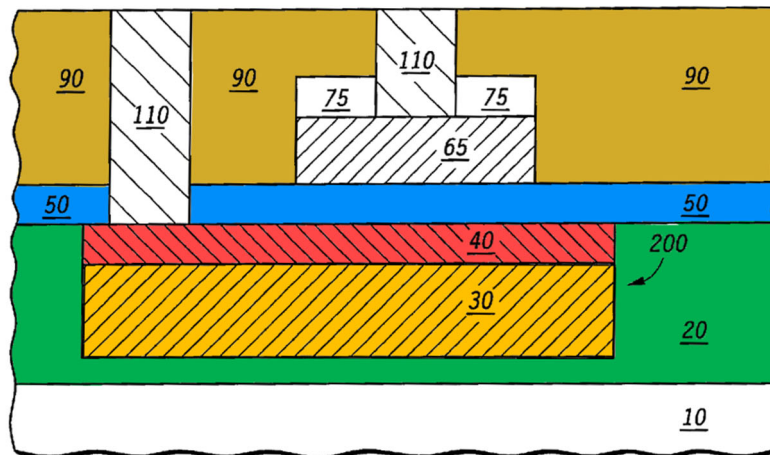
181. Second, Roberts discloses removing portions of the ILD layer 90 (the third insulating layers) and capacitor dielectric layer 50 (second insulating layer) in one step. In particular, Roberts discloses forming the via openings using “a first chemistry” to remove ILD layer 90 and a “second chemistry” to remove the capacitor dielectric layer 50, exposing “underlying conductive portions.” EX1007, 5:66-6:3; 6:14-17. Roberts further discloses that “the etching of the via openings can occur in the *same tool* and even the *same chamber* for improved throughput and manufacturing efficiency.” *Id.*, 6:19-22 (emphasis added). A POSITA would have found it obvious that the process is performed and completed in one step because the

process is conducted in the same chamber and using the same tool. Therefore, a POSITA would have understood that the recited “removing portions of the third insulating film and the second insulating film in one step” is the disclosed etching process performed in the same chamber using the same tool.

182. Additionally, according to the '527 patent, Roberts' two-chemistry etch would be in one step. The '572 patent discloses that the claimed third insulating layer is made of “a carbon-containing silicon oxide film,” an FSG (fluorinated silicate glass) film, a BPSG (boron phosphorus silicate glass) film, or a porous film” and the claimed second insulating layer is made of “a silicon carbon nitride film,” “a silicon nitride film, a silicon carbide film, a silicon oxycarbide film, or the like.” A POSITA would have understood that it would have required two chemistries to etch the two layers and the '572 patent claims the etching of two layers as being performed in one step. Thus, like the '527 patent, Roberts discloses etching “in one step.”

183. The “in one step” limitation is also met because Roberts teaches that the first chemistry can be used to etch both layers 90 and 50. Specifically, Roberts states that “the first chemistry needs to be selective to the ESL layer material and *perhaps even* the capacitor dielectric layer 50.” EX1007, 6:12-14 (emphasis added). A POSITA would have understood that, while selectivity to the ESL layer 75 is required, selectivity to the capacitor dielectric layer 50 is optional. In this context,

“selective” means that the first chemistry should not etch the ESL layer 75, and that the ESL layer 75 functions as an etch stop for the first chemistry. EX1007, 5:66-6:3. With an optional etch selectivity to the capacitor dielectric layer 50, a POSITA would have understood that the first chemistry may also etch layer 50 in addition to layer 90 in some embodiments. Accordingly, a POSITA would have found it obvious that the first chemistry is used to etch the **ILD layer 90 as well as the capacitor insulating layer 50** in one step.



EX1007, Fig. 11.

184. Furthermore, a POSITA would have understood that unlike ESL layer 75, the capacitor insulating layer 50 does not necessarily serve as the etch stop layer for the first chemistry and therefore can be etched through using the first chemistry. The ESL layer 75 is included to protect the top electrode 65 from over-etching while the first chemistry completes etching to expose the conductive barrier layer 40. Because the barrier layer 40 is positioned deeper than the top electrode 65, it would

not be exposed to the first chemistry long enough to risk over-etching. Accordingly, the capacitor insulating layer 50 does not need to function as an etch stop and can be etched in a single step along with the ILD layer 90.

185. Therefore, a POSITA would have understood that the recited “removing portions of the third insulating film and the second insulating film in one step” is the disclosed etching of the dielectric layers 90 and 50 using the first chemistry.

186. Moreover, a POSITA would have been motivated to combine Roberts with Parikh and that the combination discloses/suggests this limitation. Parikh teaches etching two insulating layers to expose the barrier layer in one step. *See supra* § IX.A.4(vii); EX1004, [0027]. As discussed above, a POSITA would have found it obvious to use Parikh’s one step etching process in the formation of openings that expose the conductive oxidation barrier layer 40 of Roberts. *See supra* § IX.C.2.

(viii) [1.g] the step (g) of removing the photoresist.

187. In my opinion, Roberts discloses this limitation. Roberts discloses that “[t]he first photoresist layer 80 is removed after patterning using conventional methods.” EX1007, 5:56-5:60. A POSITA would have understood that Roberts treats photoresist layer 80 and 100 in the same way. Figures 10 and 11 of Roberts

silicon substrate, irreversibly altering its electrical characteristics and destroying the functionality of the transistors. *Id.* For these reasons, the complete removal of the photoresist, through a standard industry process known as "stripping" or "ashing," is performed after a photolithography-based patterning cycle to ensure the device's integrity and operability.

4. Claims 2-3

(i) **Claim 3. "The method of claim 1, wherein in the step (c), a film containing nitrogen is deposited, as the oxidation-resistant conductor film, on the interconnect layer."**

190. In my opinion, Roberts discloses claim 3. Roberts discloses depositing a conductive oxidation barrier layer 40 that may be made from a metal nitride. *Id.*, 4:19-21 ("The **conductive oxidation barrier layer 40** is **deposited** over the surface of the dielectric layer 20 and the recessed **first metal layer 30**."), 4:21-28, ("Materials that are both good oxidation and barrier layers to materials including copper are tantalum, titanium, platinum, iridium, aluminum, ruthenium, tungsten, tantalum nitride, titanium nitride, and the like.").

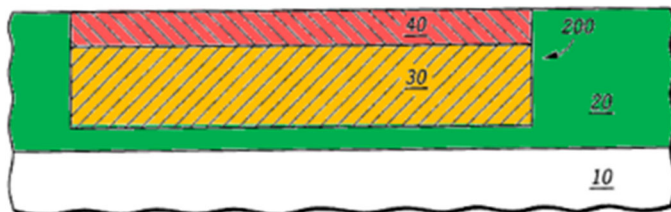


FIG.6

191. EX1007, Fig. 6. A POSITA would have understood that the metal nitride, such as TiN, contains nitrogen. Therefore, a POSITA would have understood that the recited “a film containing nitrogen” is the disclosed “**conductive oxidation barrier**” formed of a metal nitride. Thus, Roberts discloses Claim 3.

(ii) Claim 2. “The method of claim 1, wherein in the step (c), plasma treatment, wet treatment, or ion implantation is performed to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film

192. In my opinion, Roberts discloses claim 2. Roberts discloses that the “conductive oxidation barrier layer is formed by PVD, CVD, ALD, electroplating, electroless plating, combinations of the above or the like.” *Id.*, 4:16-19. A POSITA would have understood that electroplating and electroless plating are types of “wet treatment” as recited in Claim 2. As discussed above, a POSITA would have understood Roberts discloses or suggests plasma treatment in view of Roberts’ PVD disclosure. *See supra* §§IX.A.5(ii), VII.B.

193. Therefore, a POSITA would have understood that the disclosed “electroplating” and/or “electroless plating” is the recited “wet treatment,” that the PVD is the recited plasma treatment, and that the recited “to introduce nitrogen into an upper portion of the interconnect layer” is the disclosed forming the conductive oxidation barrier layer with the metal nitride. Thus, Roberts discloses Claim 2.

D. Ground 4: Claim 2 Is Obvious Over Roberts, Parikh, and Maeda

194. As explained above, Maeda teaches performing plasma treatment to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film. *See supra* §IX.B.3.

195. A POSITA would have found it obvious to combine the teachings of Maeda, Parikh, and Roberts. All references are in the same field as the '572 patent and directed to solving the same problem as each other and the '572 patent. In particular, Roberts and Parikh focus on semiconductor device fabrication, specifically the formation and protection of metal interconnects, including the use of barrier or oxidation-resistant layers. *See supra* §IX.C.2. Additionally, Maeda is from the same field of semiconductor device fabrication and teaches forming an antioxidant film “on the surface of the trench-type interconnect in a self-aligned manner” to “prevent surface oxidation of interconnects formed through embedded interconnect technology to prevent an increase in the resistance and a decrease in the reliability.” EX1006, Abstract; [0001], [0005], [0007], cl. 1. This parallels the '572 patent's concern with protecting metal interconnects using barrier or oxidation-resistant layers during semiconductor device fabrication.

196. As explained above, a POSITA would have been motivated to combine Maeda and Parikh. *See supra* §IX.B.2. A POSITA would have been motivated to combine Maeda and Roberts for several reasons. Additionally, Maeda recognizes

that copper is susceptible to oxidation when exposed to air during semiconductor processing, which can degrade electrical performance and reliability. EX1006, [0005]. Maeda addresses this problem by teaching the formation of an anti-oxidation film using nitrogen-containing plasma. EX1006, [0023]. Roberts, in the context of MIM capacitors with copper metal layers, also recognizes the need for a barrier to prevent oxidation and diffusion. EX1007, 4:37-39, 4:62-67. A POSITA would have recognized that Maeda's plasma-based anti-oxidation film could be used in Roberts' process to further protect the copper metal layer from oxidation during subsequent processing steps, such as before the deposition of the dielectric. Both Maeda and Roberts describe process flows that are compatible with damascene technology, including the use of CMP and barrier layer deposition. EX1006, [0019], [0021-0022], [0027]; EX1007, 3:42-44, 4:16-21. Maeda's plasma treatment can be readily integrated into the Roberts process after planarization of the metal layer and before dielectric deposition, without introducing significant complexity.

197. In my opinion, a POSITA would have had a reasonable expectation of success in combining Maeda with Roberts because both references teach well-established, compatible methods for protecting copper in semiconductor devices. Maeda demonstrates that nitrogen plasma treatments and TiN barrier layers effectively prevent copper oxidation, while Roberts describes integrating conductive

oxidation barriers (e.g., TiN) for copper electrodes in MIM capacitors. Both processes use standard semiconductor fabrication techniques (e.g., CMP, sputtering), and Maeda explicitly teaches that such anti-oxidation films can be formed in a self-aligned manner, making their integration into Roberts' process straightforward and technically predictable.

198. As explained above, Maeda discloses performing a plasma treatment to introduce nitrogen into an upper portion of the interconnect layer, thereby forming the oxidation-resistant conductor film. *See supra* §IX.B.3. As discussed above, a POSITA would have been motivated to combine Maeda and Roberts. Therefore, a POSITA would have been motivated to make the Roberts-Maeda combination or the Roberts-Parikh-Maeda combination, and would have understood that either combination suggests the limitations of claim 2.

E. Ground 5: Claims 4-7 Are Obvious Over Roberts, Parikh, and Komada

1. Combination of Roberts, Parikh, Komada

199. A POSITA would have been motivated to combine Komada, Parikh, and Roberts. In particular, a POSITA would have found it obvious to incorporate Komada's ring trench into Roberts' semiconductor structure. A POSITA would have understood that the added ring trench is formed along the periphery of Roberts' structure.

200. A POSITA would have been motivated to combine Parikh and Komada. *See supra* § IX.A.3. In addition, a POSITA would have been motivated to combine Roberts and Komada for at least the following reasons. **First**, Roberts and Komada are both in the same field as the '572 patent and directed to solving the same problem as each other and the '572 patent. In particular, both references focus on semiconductor device fabrication, specifically the formation and protection of metal interconnects, including the use of barrier or oxidation-resistant layers. *See supra* § IX.C.2; *see also e.g.*, EX1001, Abstract; EX1004, Abstract, [0002]; EX1007, Abstract. Additionally, Komada is from the same field of semiconductor device fabrication and teaches the use of upper conductive barrier layers (such as titanium nitride) that extend over the surfaces of interconnects, pads, and moisture-resistant rings to act as etch stoppers and to restrict deformation, thereby protecting the underlying metal and improving device reliability. EX1005, Abstract; [0035]–[0038], [0042], [0050]–[0056]. This approach parallels the '572 patent's concern with protecting metal interconnects using barrier or oxidation-resistant layers during semiconductor device fabrication.

201. **Second**, the similarity between Roberts and Komada would have motivated a POSITA to combine them. Both references emphasize the use of copper for interconnect elements. EX1007, 1:31-36 (“Copper is replacing aluminum and aluminum alloys as the predominant material for metal interconnects in

semiconductor manufacturing.” “Therefore, it would be advantageous to use copper as the metal of an MIM capacitor electrode to avoid having to add further materials and processing steps.”); EX1005, [0010] (“it has been proposed to use metals with high melting points, such as Cu, which have lower resistivity than Al, as interconnect materials”). Both references acknowledge the problem associated with copper. EX1007, 1:42-47 (“Known problems with using copper as an electrode material include adverse affects[sic] caused by poor mechanical and chemical stability of the copper surface, and other interactions of the copper with the capacitor dielectric materials (e.g. copper diffusion).”); EX1005, [0016] (“It should be noted that Cu, by nature, is diffused in the insulating layer.”).

202. Both references recognize the benefits of using metal nitrides, such as TiN, to form a layer that reduces copper diffusion and mitigates the risk of over-etching. EX1007, 4:24-28 (“Materials that are both good oxidation and barrier layers to materials including copper are tantalum, titanium, platinum, iridium, aluminum, ruthenium, tungsten, tantalum nitride, titanium nitride, and the like.”); EX1005, [0016] (“a barrier layer formed of TiN, TaN, etc., is formed”).

203. Both references recognize the desirability of integration in semiconductor integrated circuit devices. EX1007, 1:22-23 (“As semiconductor devices shrink, there is a desire to decrease the area occupied by features, such as capacitors.”); EX1005, [0007] (“There is always a demand for improvement in the

degree of integration in semiconductor integrated circuit devices.”). Thus, a POSITA would have considered Komada when implementing Roberts.

204. **Third**, a POSITA would have found that the combination uses a known technique to improve similar devices (methods, or products) in the same way. It is known in the art that a ring trench can be added along the periphery of core components to reduce moisture permeation, thereby protecting the semiconductor device’s properties and improving long-term reliability. *See supra* §§ IX.A.2, A.3; EX1005, [0005]. Roberts’ MIM capacitor, like other active and passive components, is susceptible to degradation from moisture ingress, which can increase leakage, degrade dielectric properties, and reduce long-term reliability. A POSITA would have understood that the ring trench may be used in Roberts to improve the same type of device—namely, a semiconductor chip with a damascene structure—by acting as a barrier to seal the periphery of the chip and protect the internal structures from environmental contaminants, in the same way as achieved in Komada.

205. In addition, Komada itself provides guidance that is also applicable to Roberts on how to create the ring trench. For example, Komada teaches that “[a] moisture-resistant ring is formed by forming a ring trench that surrounds the circuit region in a loop, doing so through an etching process performed at the same time as the etching performed to form via holes in the interlayer insulating layer, and then

by filling the ring trench with an interconnection layer formed through a[n] interconnect formation step for patterning.” EX1005, [0006]. A POSITA would have understood that a ring trench in Roberts may also be formed surrounding the circuit region in a loop and that the ring trench may optionally be formed at the time Roberts forms via openings 110 in the same way as in Komada. A POSITA would have understood that the addition of a ring trench as taught by Komada would not have interfered with the operation or fabrication of the MIM capacitor of Roberts. Roberts’ MIM capacitor is formed within the region protected by the ring trench, thereby benefitting from the enhanced reliability and environmental protection provided.

206. A POSITA would have had a reasonable expectation of success in combining the ring trench of Komada with Roberts, based at least on the compatibility of materials, process steps, and underlying objectives of both references. Roberts’ disclosure, which utilizes damascene processing, is compatible with the addition of a ring trench. EX1007, 3:40-42, 7:28-32, cl. 5. Both references contemplate the use of dielectric and conductive materials, and both employ photolithographic and etching techniques that are industry standard. EX1004, [0006], [0017], [0027], [0031]; EX1007, 3:24-26, 3:40-44, 5:35-42, 5:55-66, 6:12-22. Given the shared technological context and the predictability of results

when combining Komada's ring trench with Roberts, a POSITA would have reasonably expected such an adaptation to be successful.

207. In addition, Roberts acknowledges that using copper as the electrode material may pose challenges related to surface mechanical stability. EX1007, 1:41-47 ("Known problems with using copper as an electrode material include adverse affects[sic] caused by poor mechanical and chemical stability of the copper surface."). Komada also recognizes similar mechanical stability issues. EX1005, [0031] ("when the stress acting on the pad pattern overcomes the adhesion force of the conductive plug for connection, the upper and lower pad layers are delaminated, creating a void V in the middle"). Komada discusses a method to overcome these issues by forming a Ti layer on the upper surface of the interconnect pattern. *Id.*, [0033] ("forming an interconnection layer by employing CMP to over-polish the surfaces of the interconnection layers more than their surrounding insulating layer, followed by laminating a metallic layer, such as Ti, on the over-polished surfaces, and then performing additional polishing with CMP"). Therefore, a POSITA considering Roberts would have been motivated to combine teachings of Komada for solutions to improve the mechanical stability of Roberts' structure.

2. Claim 4

(i) [4.a] The method of claim 1, wherein in the step (b), a first interconnect layer and a second interconnect layer are formed as the interconnect layer,

208. As explained above, Komada discloses this limitation. *See supra* § IX.A.6(i). As explained above, a POSITA would have been motivated to combine the teachings of Roberts and Komada. *See supra* § IX.E.1. Therefore, the Roberts-Komada combination or the Roberts-Parikh-Komada combination teaches this limitation.

(ii) [4.b] in the step (c), an oxidation-resistant conductor film is formed on the first interconnect layer and the second interconnect layer, and

209. As explained above, Komada discloses this limitation. *See supra* § IX.A.6(ii). As explained above, a POSITA would have been motivated to combine teachings of Roberts and Komada. *See supra* § IX.E.1. Therefore, the Roberts-Komada combination or the Roberts-Parikh-Komada combination teaches this limitation.

(iii) [4.c] in the step (f), portions of the third insulating film and the second insulating film located over the first interconnect layer are removed to form a trench, and portions of the third insulating film and the second insulating film located over the second interconnect layer are removed to form a hole.

210. As explained above, Komada discloses this limitation. *See supra* §IX.A.6(iii). As explained above, a POSITA would have been motivated to combine

teachings of Roberts and Komada. *See supra* §IX.E.1. Therefore, the Roberts-Komada combination or the Roberts-Parikh-Komada combination teaches this limitation.

3. Claim 5

(i) The method of claim 1, further comprising, prior to the step (a), the step (h) of forming an element in the semiconductor substrate, wherein in the step (b), the interconnect layer is formed to be electrically connectable to the element.

211. As explained above, Komada discloses this limitation. *See supra* §IX.A.7(i). As explained above, a POSITA would have been motivated to combine the teachings of Roberts and Komada. *See supra* §IX.E.1. Therefore, the Roberts-Komada combination or the Roberts-Parikh-Komada combination teaches this limitation.

4. Claim 6

(i) [6.pre] A method for fabricating a semiconductor device, comprising:

212. I have been asked to assume that these preambles are limiting. Under that assumption, it is my opinion that the Roberts-Komada combination or the Roberts-Parikh-Komada combination discloses the preamble for the same reason explained above in the section regarding limitation [1.pre]. *See supra* § IX.C.3(i).

(ii) [6.a] the step (a) of forming a first insulating film over a semiconductor substrate;

213. It is my opinion that the Roberts-Komada combination or the Roberts-Parikh-Komada combination discloses this limitation for the same reason explained above in the section regarding limitation [1.a]. *See supra* § IX.C.3(ii).

(iii) [6.b] the step (b) of forming a first interconnect layer and a second interconnect layer in at least an upper portion of the first insulating film;

214. It is my opinion that the Roberts-Komada combination or the Roberts-Parikh-Komada combination discloses this limitation for the same reason explained above in the section regarding limitations [1.b] and [4.a]. *See supra* §§ IX.C.3(iii), IX.E.2(i), IX.E.1; IX.A.6(i). As explained in section above in section IX.E.1, a POSITA would have been motivated to combine Roberts, Parikh, and Komada. *See supra* IX.E.1. As further explained above, in sections regarding limitation [4.a] in grounds 1 and 4, Komada discloses the claimed first and second interconnect layers in at least an upper portion of the first insulating film. *See supra*, §§ IX.A.6(i), IX.E.2(i). As explained above in the section regarding limitation [1.b], Roberts discloses forming an interconnect layer in at least an upper portion of the first insulating film. *See supra* § IX.C.3(iii). Therefore, the Roberts-Komada combination or the Roberts-Parikh-Komada combination suggests this limitation.

(iv) [6.c] the step (c) of forming an oxidation-resistant conductor film covering tops of the first interconnect layer and the second interconnect layer;

215. It is my opinion that the Roberts-Komada combination or the Roberts-Parikh-Komada combination discloses this limitation for the same reason explained above in the section regarding limitations [1.c] and [4.b]. *See supra* §§ IX.C.3(iv), IX.E.2(ii), IX.E.1; IX.A.6(ii). As explained in section above in section IX.E.1, a POSITA would have been motivated to combine Roberts, Parikh, and Komada. As further explained above, in sections regarding limitation [4.a] in grounds 1 and 4, Komada discloses forming an oxidation-resistant conductor film covering tops of the first interconnect layer and the second interconnect layer. *See supra*, §§ IX.A.6(i), IX.A.6(ii), IX.E.2(ii). As explained above in the section regarding limitation [1.c], Roberts discloses forming an oxidation-resistant conductor film covering the top of the interconnect layer. *See supra* § IX.C.3(iv). Therefore, the Roberts-Komada combination or the Roberts-Parikh-Komada combination suggests this limitation.

(v) [6.d] the step (d) of forming a second insulating film on the first insulating film and the oxidation-resistant conductor film;

216. It is my opinion that the Roberts-Komada combination or the Roberts-Parikh-Komada combination discloses this limitation for the same reason explained above in the section regarding limitations [1.d]. *See supra* § IX.C.3(v).

(vi) [6.e] the step (e) of forming a third insulating film on the second insulating film;

217. It is my opinion that the Roberts-Komada combination or the Roberts-Parikh-Komada combination discloses this limitation for the same reason explained above in the section regarding limitations [1.e]. *See supra* § IX.C.3(vi).

(vii) [6.f] the step (f) of forming a trench pattern by removing portions of the third insulating film and the second insulating film located over the first interconnect layer, and forming a part of a hole pattern by removing portions of the third insulating film and the second insulating film located over the second interconnect layer; and

218. It is my opinion that the Roberts-Komada combination or the Roberts-Parikh-Komada combination discloses this limitation for the same reason explained above in the section regarding limitations [1.f] and [4.c]. *See supra* §§ IX.C.3(vii); IX.E.2(iii), IX.E.1; IX.A.6(iii). As explained in section above in section IX.E.1, a POSITA would have been motivated to combine Roberts, Parikh, and Komada. *See supra* § IX.E.1. As further explained above, in sections regarding limitation [4.c] in grounds 1 and 4, Komada discloses “forming a trench pattern by removing portions of the third insulating film and the second insulating film located over the first interconnect layer, and forming a part of a hole pattern by removing portions of the third insulating film and the second insulating film located over the second interconnect layer.” *See supra*, §§ IX.A.6(i), IX.A.6(iii), IX.E.2(iii). As explained above in the section regarding limitation [1.f], Roberts discloses “removing portions

of the third insulating film and the second insulating film located over the interconnect layer.” *See supra* § IX.C.3(vii). Therefore, the Roberts-Komada combination or the Roberts-Parikh-Komada combination suggests this limitation.

(viii) [6.g] the step (g) of removing portions of the second insulating film located over the second interconnect layer until the hole pattern reaches the oxidation-resistant conductor film.

219. It is my opinion that the Roberts-Komada combination or the Roberts-Parikh-Komada combination discloses this limitation for the same reason explained above in the section regarding limitations [1.f] and [4.c]. *See supra* §§ IX.C.3(vii); IX.E.2(iii), IX.E.1; IX.A.6(iii). As explained in section above in section IX.E.1, a POSITA would have been motivated to combine Roberts, Parikh, and Komada. As further explained above, in sections regarding limitation [4.c] in grounds 1 and 4, Komada discloses “removing portions of the second insulating film located over the second interconnect layer.” *See supra*, §§ IX.A.6(i), IX.A.6(iii), IX.E.2(iii). As explained above in the section regarding limitation [1.f], Roberts discloses “removing portions of the second insulating film located over the interconnect layer until the oxidation-resistant conductor film is exposed.” *See supra* § IX.C.3(vii). A POSITA would have understood that when the oxidation-resistant conductor film is exposed, the hole pattern reaches the oxidation-resistant conductor film. Therefore, the Roberts-Komada combination or the Roberts-Parikh-Komada combination suggests this limitation.

5. Claim 7

(i) [7.a] The method of claim 6, wherein in the step (f), when the trench pattern is formed, portions of the third insulating film and the second insulating film located over the first interconnect layer are removed until the oxidation-resistant conductor film is exposed in one step.

220. It is my opinion that the Roberts-Komada combination or the Roberts-Parikh-Komada combination discloses this limitation for the same reason explained above in the section regarding limitations [1.f], [4.c], and [6.g]. *See supra* §§ IX.C.3(vii); IX.E.2(iii), IX.E.1; IX.A.6(iii), IX.E.4(viii). As explained in section above in section IX.E.1, a POSITA would have been motivated to combine Roberts, Parikh, and Komada. *See supra*, § IX.E.1. As further explained above, in sections regarding limitation [4.c] in grounds 1 and 4, Komada discloses “portions of the third insulating film and the second insulating film located over the first interconnect layer are removed to form a trench.” *See supra*, §§ IX.A.6(i), IX.A.6(iii), IX.E.2(iii). As explained above in the section regarding limitation [1.f] and [6.g], Roberts discloses “portions of the third insulating film and the second insulating film located over the first interconnect layer are removed until the oxidation-resistant conductor film is exposed in one step.” *See supra* §§ IX.C.3(vii), IX.E.4(viii). Therefore, the Roberts-Komada combination or the Roberts-Parikh-Komada combination suggests this limitation.

Declaration of Dr. Banerjee

U.S. Patent No. 8,329,572

X. CONCLUSION

221. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: July 15, 2025

By: 

Dr. Sanjay K. Banerjee