

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

**SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,**
Petitioners

v.

MAXELL CORPORATION,
Patent Owner

Inter Partes Review: IPR2025-01309

**DECLARATION OF DR. R. JACOB BAKER IN SUPPORT OF PETITION
FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,577,417**

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1001	U.S. Patent No. 7,577,417
1002	File History of U.S. Patent No. 7,577,417
1004	U.S. Patent 5,303,171 (“Belt”)
1005	U.S. Patent 6,223,293 (“Foster”)
1006	U.S. Patent 5,630,148 (“Norris”)
1007	U.S. Patent 6,094,565 (“Alberth”)

CHART OF CLAIMS	
[1pre]	A mobile terminal capable of being changed from an open condition into a closed condition, comprising:
[1a]	a processor which executes program processing; and
[1b]	a clock controller capable of changing a frequency of a clock signal to be fed to the processor;
[1c]	wherein the clock controller controls the frequency of the clock signal so as to become a first frequency when the mobile terminal is in the open condition, and controls the frequency of the clock signal so as to become a second frequency lower than the first frequency when the mobile terminal is in the closed condition, and
[1d]	wherein the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency when a specific processing is executed even if the mobile terminal is in the closed condition, and controls the frequency of the clock signal so as to become the second frequency after the execution of the specific processing is completed.
[2]	The mobile terminal according to claim 1, wherein the specific processing is a processing having an effect on a response to a request from the user.
[3]	The mobile terminal according to claim 1, wherein the specific processing is an image decoding processing or an address retrieval processing or a character conversion processing.
[4pre]	The mobile terminal according to claim 1, further comprising
[4a]	an input unit which allows a user of the mobile terminal to set the frequency of the clock signal,
[4b]	wherein when the frequency is set by the user using the input unit, the first frequency is the frequency set by the user using the input unit.
[5]	The mobile terminal according to claim 4, wherein the user can set the frequency of the clock signal in every processing using the input unit.
[6]	The mobile terminal according to claim 1, further comprising a display which exhibits a display corresponding to the magnitude of the frequency of the clock signal.
[7]	The mobile terminal according to claim 1, wherein the mobile terminal has a folded structure.

I. INTRODUCTION

I, R. Jacob Baker, declare as follows:

1. My name is R. Jacob Baker, Ph.D., P.E.. I have been asked by Petitioners Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. to provide my expert opinions in support of the above-identified petition for inter partes review of claims 1-7 (“Challenged Claims”) of U.S. Patent No. 7,577,417 (“’417 patent,” EX1001), owned by Maxell Corporation (“PO”), pursuant to 35 U.S.C. §§311–19 and 37 C.F.R. §42.100.

2. I currently hold the opinions set forth in this declaration.

3. In summary, it is my opinion that the references cited below anticipate or render obvious the Challenged Claims. My detailed opinions on the claims are set forth below.

4. I am being compensated for my time at the rate of \$765 per hour. This compensation is not contingent upon my performance, the outcome of this matter, or any issues involved in or related to this matter.

II. BACKGROUND AND QUALIFICATION

A. Background

5. My qualifications generally are set forth in my Curriculum Vitae, which is attached as **Appendix B**. Appendix B also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

6. I have been working as an Engineer since 1985 and I have been teaching Electrical and Computer Engineering courses since 1991. I am currently a Professor Emeritus of Electrical and Computer Engineering at the University of Nevada, Las Vegas (“UNLV”).

7. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

8. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled “Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices,” published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

B. Industry Experience

9. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for

underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

10. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively biased voltage regulator and operating method," which was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

11. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. ("MTI") in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts

resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system's performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and

2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

12. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. From 1994 to 1996, I worked on the design of displays at Micron Display and

Micron Technology, Inc. (“Micron”) in Boise, Idaho. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel displays which resulted in 5 patents: 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting electronics for processing video signals. I was involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was also involved with the packaging of the displays including the vacuum sealing and deposition of the phosphors for light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

13. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (LIght Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The

knowledge and experience gained from this effort are reflected in my textbook CMOS Mixed-Signal Circuit Design and a presentation, which I have present-ed at several universities and companies, http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

C. Academic Experience

14. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University (“BSU”), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university’s second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

15. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the “Father of Silicon

Valley”). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

16. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

D. Other Relevant Experience

17. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

18. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-2024). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to *see* what other researchers in the field have been doing.

19. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu

and Tau Beta Pi. I am also the named inventor on over 150 U.S. patents resulting from my industry work in areas related to the technology at issue in the ‘417 patent.

III. DOCUMENTS AND OTHER MATERIALS RELIED UPON

20. In forming the opinions set forth in this declaration, I have reviewed the documents in the following table:

Exhibit No.	Description
1001	U.S. Patent No. 7,577,417
1002	File History of U.S. Patent No. 7,577,417
1004	U.S. Patent 5,303,171 (“Belt”)
1005	U.S. Patent 6,223,293 (“Foster”)
1006	U.S. Patent 5,630,148 (“Norris”)
1007	U.S. Patent 6,094,565 (“Alberth”)

21. Additionally, I have utilized my own experience and expertise, including regarding the knowledge and capabilities of a person of ordinary skill in the relevant art in the timeframe of the claimed priority date of the ‘417 patent.

IV. STATUTORY GROUNDS FOR CHALLENGE

22. In this declaration, I offer opinions on the following grounds that are the basis for this IPR proceeding:

Ground	Claims	Stat. Basis	Prior Art
1	1-2 and 4-7	35 U.S.C. § 103	Belt, Foster and Norris
2	3	35 U.S.C. § 103	Belt, Foster, Norris and Alberth

V. RELEVANT PATENT LAW AND LEGAL STANDARDS

A. Date of Invention

23. I have been asked to use the date of the filing of the earliest application to which priority is claimed (i.e., April 3, 2002) as the date of invention for purposes of my analysis.

B. Anticipation

24. I am informed and understand that a patent claim is invalid under 35 U.S.C. § 102 if a prior art disclosure teaches every element required by the claim, either expressly or inherently. The identical invention must be shown in as complete detail as is contained in the claim. When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art.

C. Obviousness

25. I am informed and understand that a patent claim is invalid under 35 U.S.C. § 103 if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art to which the subject matter pertains. Obviousness, as has been explained to me, is based on (i) the scope and content of the prior art, (ii) the differences between the prior art and the claim, (iii) the level of ordinary skill in the art, and (iv) any secondary indicia of non-obviousness (*e.g.*,

“secondary considerations” such as commercial success in the marketplace of the claimed invention), to the extent that they exist.

26. I further understand that obviousness may be demonstrated by showing that it would have been obvious to combine the teachings of more than one item of prior art. In determining whether a piece of prior art could have been combined with other prior art or with other information within the knowledge of a person having ordinary skill in the art, the following are examples of approaches and rationales that may be considered:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of a known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- Applying a technique or approach that would have been obvious to try (choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success);

- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a person having ordinary skill in the art; and
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

27. I further understand that an invention may be obvious if one of ordinary skill in the art, facing a wide range of needs created by developments in the field, would have *seen* an obvious benefit to the solutions tried by the applicant. When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, it may be obvious to a person of ordinary skill to try the known options. If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious.

28. I further understand that a person of ordinary skill in the art is a hypothetical person who is presumed to be aware of all of the relevant art at the time of the invention. The person of ordinary skill may be able to fit together the

teachings of multiple patents and/or printed publications employing ordinary creativity and the common sense that familiar items may have uses in another context or beyond their primary purposes.

29. I also understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when combining or modifying the prior art. I understand this test should not be applied rigidly, but that the test can be important to avoid such hindsight.

30. I also understand that one of ordinary skill in the art must have a reasonable expectation of success in combining or modifying prior art references.

31. I also understand that all elements of a claim must be considered in an obviousness analysis.

D. Claim Construction

32. I understand that claim construction is a matter for the Board to decide and, in general, the ordinary meaning of the claim terms used in the patent to one of ordinary skill in the art is determined in the context of the patent's specification and the file history.

33. I understand that ultimately the Board will determine how specific terms shall be construed. The intent of this declaration is to help inform the Board about how a person of ordinary skill in the art would have understood the meaning

of certain claim terms at the time of the claimed invention in the context of the '417 Patent's claims, specification, and prosecution history in a manner that will assist the Board in the process of construing the claims.

34. I understand that claims are construed from the perspective of a person of ordinary skill as of the effective filing date of the patent application. A "person of ordinary skill in the art" is a hypothetical person who is presumed to have known the relevant art at the time of the invention.

35. I understand that persons of ordinary skill in the art are deemed to read the claims in the context of the entire patent, including the specification and prosecution history. In other words, the terms are not considered in a vacuum.

36. I understand that the claims define the invention and the terms used in the claims are generally given the plain and ordinary meanings they would have to a person of ordinary skill in the art at the time of the effective filing date of the application. The context of a claim can be particularly helpful, and other claims may inform the meaning of a term in a particular claim. Terms are normally used consistently throughout a patent. Thus, the meaning of a term may help inform the meaning of the same term in other claims. Differences between claims may also help define the terms, although this may not be the case where the specification or prosecution history indicate that such differences do not impact the scope of the claims.

37. I understand that a patentee can act as its own lexicographer by defining a term, in the patent specification, to have specific meaning. It is my understanding that statements made to the patent office by the patentee or its legal representative during prosecution can serve to illuminate, or possibly narrow the proper scope of claim terms, and that such statements must be considered when construing the claim terms. This is sometimes referred to as disclaimer. I have taken into account these principles in my analysis.

38. I understand that reference materials that were publicly available at the time that the patent application was filed, such as dictionaries, treatises or other technical references, may provide context and background for deciphering how one of ordinary skill in the art would have considered the terms used in the claims. However, I understand that such references, as well as testimony (including this report) are generally known as “extrinsic evidence,” and are accorded less weight than evidence found within the patent and prosecution history. In addition, I understand that extrinsic evidence that is inconsistent with the claims, specification, or prosecution history should not be considered in the claim construction process.

E. Section 112(f) Means Plus Function

39. I understand that under pre-America Invents Act (AIA) 35 U.S.C. § 112(6) and post-AIA § 112(f) “*An element in a claim for a combination may be*

expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.”

40. I understand that when claim terms use the words “means . . . for” and recites a function, and the term does not recite any structure for performing that function, the term should be construed pursuant to Section 112(f) looking for a corresponding structure, material, or act described in the specification and equivalents.

F. Section 112 Definiteness

41. I understand that “[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.”¹

42. I understand that the claims must be definite. This means that the claims must particularly point out and distinctly claim the subject matter that the applicant regards as her invention. I understand that indefiniteness is evaluated from the perspective of a person of ordinary skill in the art at the time of a patent’s filing. I understand that a patent claim is indefinite if the claim, when read in light

¹ I understand that the quoted text comes from the patent statute, 35 U.S.C. § 112 ¶ 2.

of the specification and the prosecution history, fails to inform, with reasonable certainty, a person of ordinary skill in the art of the scope of the invention.

Absolute or mathematical precision in claim language is not required and even if more than one interpretation is presented for a claim term, the term may still be definite if an informed and confident choice is available among the contending alternative definitions.

G. Standard of Proof

43. I understand that the standard to prove unpatentability in an *inter partes* review proceeding is by a preponderance of the evidence, which means more likely than not.

VI. LEVEL OF ORDINARY SKILL IN THE ART

44. I have considered the level of ordinary skill in the art relevant to the '417 patent. I understand that factors such as the education level of those working in the field, the sophistication of the technology, the types of problems encountered in the art, the prior art solutions to those problems, and the speed at which innovations are made may help establish the level of skill in the art.

45. After reviewing the '417 patent, the relevant portions of the prosecution history of the '417 patent and its reexamination, and cited references, it is my opinion that the relevant art of the '417 patent is in the field of power management.

46. Based upon my knowledge of this field, I conclude that a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the ’417 patent (April 3, 2002), and for that matter, at all subsequent times through the present, would have had a working knowledge of power management, gained through a degree in Electrical/Computer Engineering or an equivalent degree, and at least one year of experience in the field of power management.” Additional graduate education could substitute for professional experience, and significant experience in the field could substitute for formal education.

47. I am and was at the time of the earliest filing date at least a person of skill in the relevant art and I am able to provide insight and opinions into the understandings of such persons at all relevant times by virtue of my education, training and experience. *See* Section II.

VII. THE ’417 PATENT AND ITS PROSECUTION HISTORY

A. Overview of the ’417 Patent

48. The ’417 patent discloses a central processing unit (CPU) for a mobile terminal, such as a cell phone, that provides “both enhancement in processing speed and reduction in current consumption” through a “clock control means capable of changing the frequency of a clock signal received from an oscillator under control by a [CPU].” EX1001, 1:44-48. The mobile terminal includes a folding condition detector for detecting when the device is in a folded (closed)

condition or in an unfolded (open condition), such that the clock frequency can be changed to a low frequency in the closed condition to reduce power consumption. *Id.*, 5:35-38 and 58-62. When executing a specific processing even in the closed condition, the frequency of the clock is caused to change to a higher frequency, thereby enhancing processing speed, and then goes to a low frequency when the specific processing is completed. *Id.*, 5:62-6:2. The '417 patent further states that the clock signal received by the CPU may either be raised or lowered in frequency—in response to a user request or processing—thereby increasing processing speed or increasing battery life, respectively. *Id.*, 3:7-27 (user requesting a change in CPU clock frequency), 4:32-40 (changing clock frequency in response to “specific processing”).

B. Overview of the '417 patent's File History

49. I have found at least the following from the file history that may be relevant.

50. During prosecution, the originally presented claims 1, 5-6, and 8 were rejected under 35 U.S.C. 35 § 103 as obvious in view of U.S. Patent No. 6,484,041 to Aho *et al.* and U.K. Patent App. No. GB2297661 to Jambhekar *et al.* EX1002, at 30-31 (2008-12-01 Non-Final Office Action, pp. 2-3). Originally presented claim 7 was rejected under 35 U.S.C. 35 § 103 as obvious in view of Aho, Jambhekar,

and U.S. Patent No. 5,881,372 to Kruys. *Id.* at 31-32 (2008-12-01 Non-Final Office Action, pp. 3-4).

51. The examiner objected to claims 2-4 as being dependent on rejected independent claim 1 but noted that claims 2-4 “would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.” *Id.*, at 32 (2008-12-01 Non-Final Office Action, pp. 4). Specifically, the examiner explained that “the applied references fail to disclose or render obvious the claimed limitation of the mobile terminal according to claim 1, wherein the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency when a specific processing is executed even if the mobile terminal is in the closed condition, and controls the frequency of the clock signal so as to become the second frequency after the execution of the specific processing is completed.” *Id.*

52. In response, patent owner cancelled rejected claim 1 and amended then-pending claim 2 to be in independent form by incorporating all limitations of rejected claim 1. *Id.*, at 25 (2009-03-02 Response to OA dated December 1, 2008, p. 2). Subsequently, the examiner allowed claims 2-8 (now, claims 1-7). *Id.*, at 14 (2009-04-14 Notice of Allowability, p. 3).

VIII. CLAIM CONSTRUCTION

53. For each claim term in the '417 patent, I have applied its plain and ordinary meaning to a POSITA at the time of the '417 patent.

IX. OVERVIEW OF THE PRIOR ART REFERENCES

A. EX1004 - Belt

U.S. Patent 5,303,171 (“Belt”), filed on 4/3/1992, issued on 4/12/1994, is prior art under pre-AIA 35 U.S.C. § 102(a) and (b).

B. EX1005 - Foster

U.S. Patent 6,223,293 (“Foster”), filed on 2/16/1995, issued on 4/24/2001, is prior art under pre-AIA 35 U.S.C. § 102(a) and (b).

C. EX1006 - Norris

U.S. Patent 5,630,148 (“Norris”), filed on 2/28/1996, issued on 5/13/1997, is prior art under pre-AIA 35 U.S.C. § 102(a) and (b).

D. EX1007 - Alberth

U.S. Patent 6,094,565 (“Alberth”), filed on 6/30/1997, issued on 7/25/2000, is prior art under pre-AIA 35 U.S.C. § 102(a) and (b).

X. GROUND 1: CLAIMS 1-2, 4-7 ARE RENDERED OBVIOUS BY BELT, FOSTER AND NORRIS

54. The format I use for the discussion of each claim limitation begins with a quote of the claim language in which parentheticals have been added which include exemplary arguments and evidence. This quote of the claim language is to orient the reader and the parentheticals are exemplary of my opinions. However,

my opinions additionally include all of the following discussion and any cross-referenced sections.

A. Claim 1

55. For the reasons set forth in greater detail below, in my opinion, a POSITA would have understood that Belt, in view of Foster or Norris, renders obvious claim 1.

1. [1pre]

56. To the extent that the preamble is limiting, Belt discloses “a mobile terminal (laptop computer system 10) capable of being changed from an open condition into a closed condition, comprising.”

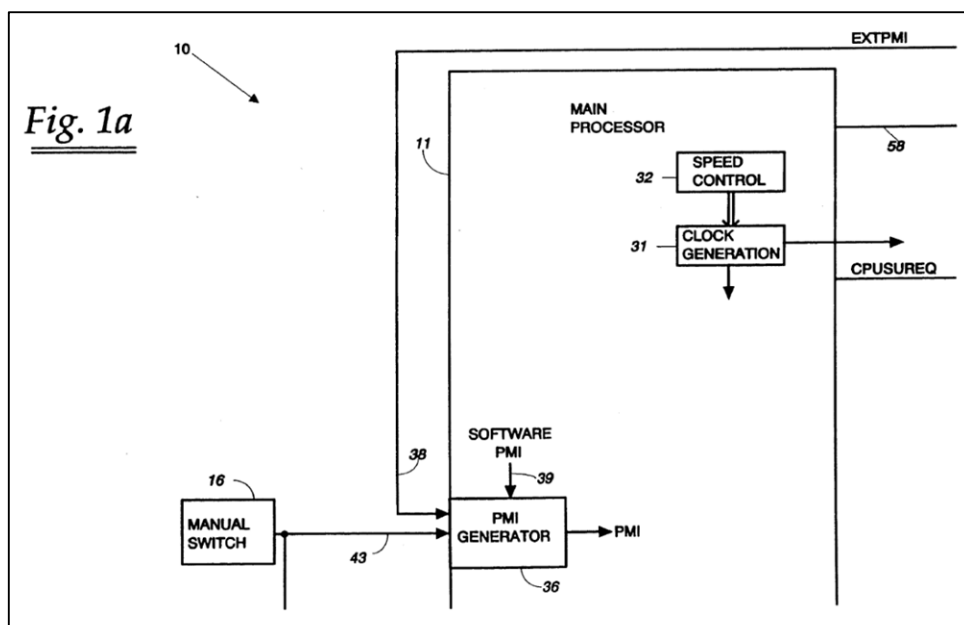
57. Belt discloses a portable computer in the form of “a computer system [] includes a housing, a lid supported on the housing for movement between open and closed positions[.]” EX1004, 1:64-67; *see also id.*, 1:13-17 (“Portable computers of the type commonly referred to as ‘laptop’ computers and ‘notebook’ computers are becoming very popular [and] [t]hey typically include a housing with a lid which is movable between open and closed positions[.]”), 2:40-43 (Fig.1 “show[s] a block diagram of a ‘notebook’ type laptop computer system 10”), 4:67-5:3. Belt’s computer system 10 is indisputably within the scope of the limitation as it is a portable computer and can be folded into a closed position and unfolded into an open position. Indeed, the ’417 patent similarly states that its mobile terminal

can be in “a folded (closed) condition or in an unfolded (open position).” EX1001, 5:35-38, cl.7.

2. [1a]

58. Belt discloses “a processor which executes program processing (main processor 11).”

59. Belt discloses its “laptop computer system 10 includes a main processor 11.” EX1004, 2:43-45, 2:54-67 (main processor 11 may be “implemented with an Intel 386SL, which is a conventional component commercially available”); Fig. 1a. Figure 1a is reproduced below:



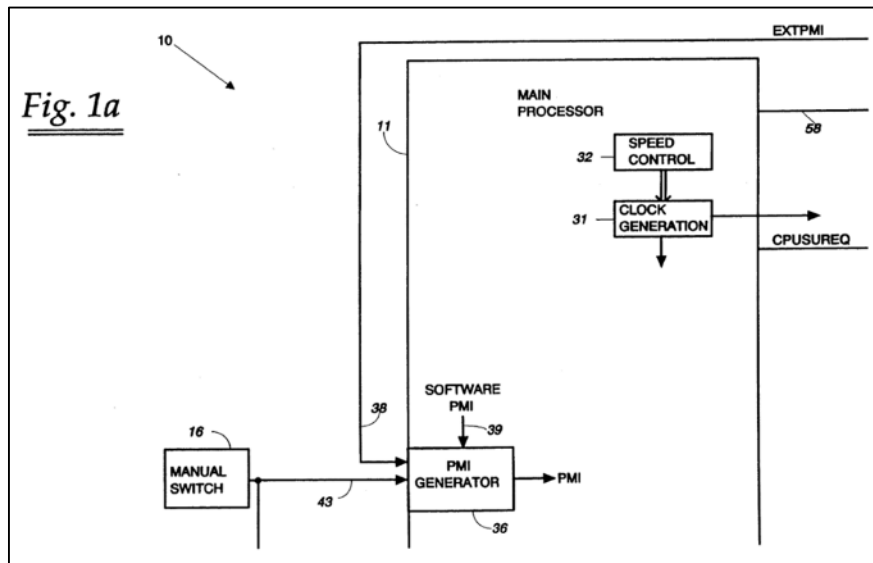
60. In my opinion, Belt expressly discloses that main processor 11 executes program processing. *Id.*, 2:35-37 (“Figs. 4-8 are flowcharts of selected program segments executed by a main processor of the system of Fig. 1.”), 7:47-49

(“the special interrupt handling routine executed by the main processor 11”), 9:22-30. In further discussing the execution of program processing, Belt interchangeably refers to “main processor 11” as “processor 11,” “the processor” (numerically unidentified), and “CPU” (numerically unidentified). *Id.*, 3:47-49 (“[t]he processor 11 has several conventional modes of operation, one of which is ... *the program running in the processor 11* has access to all operational capabilities of the processor 11”) (emphasis added), 3:54-61 (“application program which is running in one of the protected modes” on “processor 11”), 7:68-8:2 (“the processor changes the register 32 in order to force the CPU to run at its fastest clock speed, so that the PMI routine will execute as fast as possible.”), 8:22-24 (“CPU continues with the execution of the program which was interrupted.”).

3. [1b]

61. Belt alone discloses, or in combination with Norris renders obvious, “a clock controller (Belt’s clock generator 31 and speed control register 32, Norris’ clock generator circuit 14) capable of changing a frequency of a clock signal to be fed to the processor (main processor 11).”

62. As shown below in Figure 1a, Belt depicts main processor 11 including speed control register 32 and clock generator 31. EX1004, Fig. 1a, 3:1-5.



63. Regarding Fig. 1a, Belt specifically discloses “the main processor 11 includes a clock generator 31 which generates respective clocks for various components of the system, *including the processor 11 itself*, and which is controlled by a speed control register 32.” EX1004, 3:1-5 (emphasis added); *see also* Fig. 1a.

64. Belt further discloses:

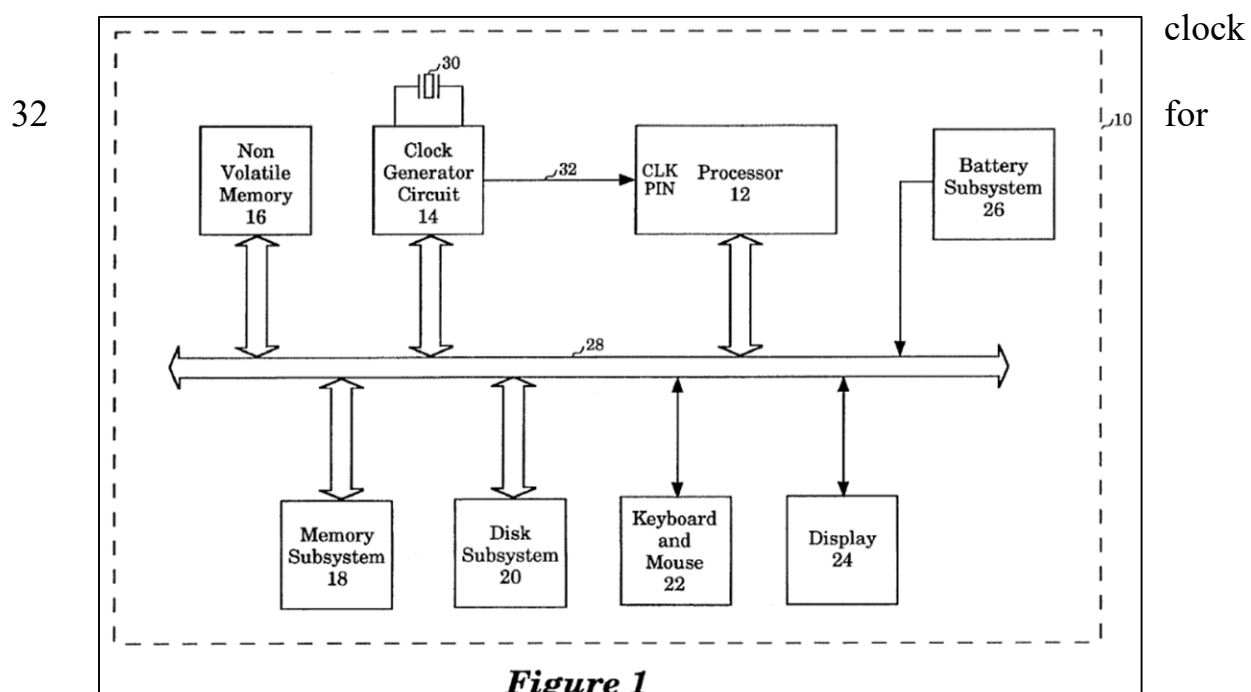
“The processor 11 and some other system components are of a type which use more power when running at a higher clock speed than when running at a lower clock speed. Therefore, clocks can be set to a **higher speed** when rapid processing is required despite the fact that a larger amount of power is drawn from the system battery during a given time period, whereas when processing speed is not critical a **lower clock speed** can be used in order to reduce the amount of power being drawn from the battery.”

Id., 3:5-14 (emphasis added); *see also id.*, 7:63-67 (“main processor 11 “unlocks configuration registers so that they can be altered, such as the control register 32 which can be used to change the speed of the clock.”), 7:67-8:2 (“the processor

changes the register 32 in order to force the CPU to run at its fastest clock speed, so that the PMI routine will execute as fast as possible.”), Fig. 4 (showing the clock signals exiting clock generator 31 and being fed (internally) to main processor 11 and (externally) to other components).

65. Notwithstanding Belt’s express disclosure, to the extent the Board interprets “to be fed” in a manner that requires the clock controller of claim 1 to be external to processor, the above disclosures of Belt, in view of Norris, renders such a configuration obvious.

66. Norris discloses “a computer system comprising a clock generator circuit having a clock speed register and circuitry for generating a processor clock signal at a frequency determined by the clock speed register.” EX1006, 2:43-58; *see also id.*, Abstract, 3:58-63 (“clock generator circuit 14 generates a processor



the processor 12”), Fig. 1 (reproduced below).

67. Norris further discloses its computer system 10 also comprises “a performance manager 44” which is executable software that “processes requests from application programs 50 and 52 to change the performance state for the processor 12.” EX1006, 4:48-56, Fig. 2 (reproduced below):

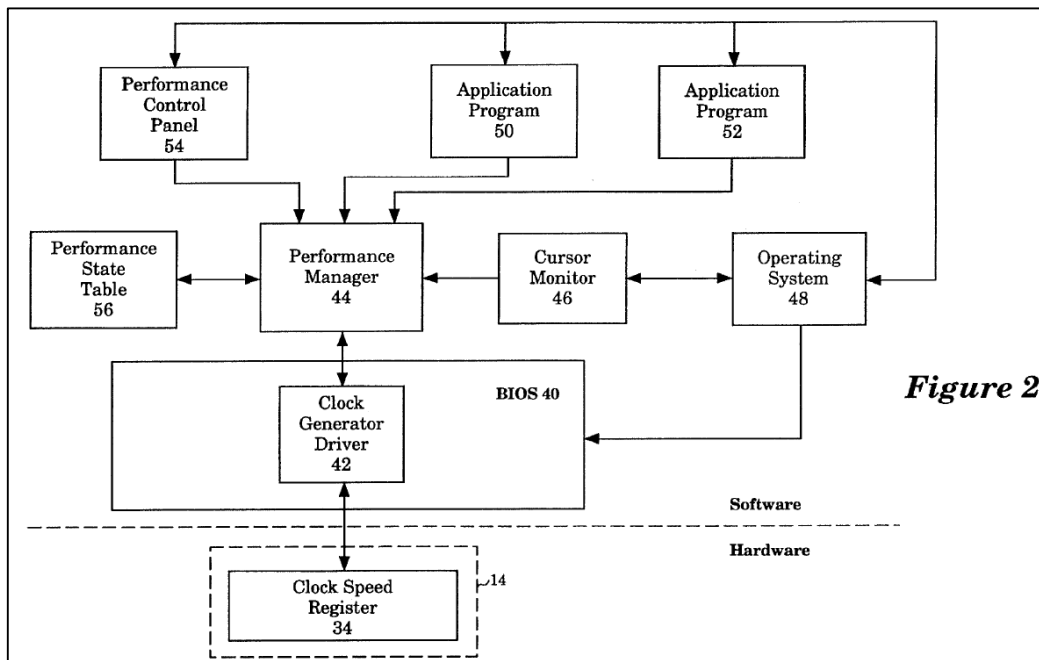


Figure 2

68. Performance manager 44, in response to a request for the processor to enter either a high, medium, or low performance state, determines “the processor clock 32 frequencies that correspond to the high, medium and low performance states of the processor 12” and then “invokes the routines of the clock generator driver 42 to program the clock speed register 34 for the specified frequency of the processor clock 32.” *Id.*, 4:57-5:4.

69. In my opinion, it would have been obvious to a POSITA to combine the teachings of Belt and Norris to arrange Belt's clock generator 31 and/or speed control register 32 outside of Belt's main processor 11, as taught by Norris, so that the clock signal generated by clock generator 31 is externally fed to the main processor 11.

70. Belt and Norris are directed to the same field of endeavor and are analogous prior art to the '417 patent since each relates to power management techniques for portable computer systems that balance performance and battery life by dynamically adjusting a processor's clock speed. *See* EX1001, 1:32-40 ("if the CPU is driven at a high frequency, there has been a tendency toward an increase in current consumption although a processing speed is enhanced" which causes "risk of premature depletion of the battery capacity occurring when the clock signal has been automatically switched over to the high-speed side without knowledge of the user."); EX1004, 3:8-14 ("clocks can be set to a higher speed when rapid processing is required despite the fact that a larger amount of power is drawn from the system battery during a given time period, whereas when processing speed is not critical a lower clock speed can be used in order to reduce the amount of power being drawn from the battery."); EX1006, Abstract, 1:10-2:20 (explaining the problem in the art was that high clock speeds reduced battery life, but slow clock speeds degraded user performance), 2:25-27 ("One object of the present invention

is manage a balance between performance and power consumption in a computer system.”).

71. A POSITA, in my opinion, would have understood the problem to be solved, namely, how to provide a variable frequency clock signal for a processor as disclosed in Belt for microprocessors that rely on external clock signals to operate. To overcome this problem, Norris discloses a computer system with clock generator circuit 14 that is external to the processor 12, wherein the clock signal 32 is fed (from the external source) to the processor 12. EX1006, 3:58-63, Fig. 1. Doing so reflects a design choice regarding whether the source of the clock signals is located in the processor or external to the processor. For example, a POSITA would have been motivated to implement the solution of Norris in the Belt device so that the invention of Belt could be implemented using microprocessors that are designed to operate using clock signals that are externally fed to the processor. Indeed, because Belt teaches that its clock generator and speed control register not only respectively generates and controls a clock signal for the processor, but also for “various components of the system” (EX1004, 3:1-5), a POSITA would have found arranging the clock generator 31 and/or speed control register 32 outside the processor to be an obvious and necessary design choice when such components are not included within a processor.

72. A POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Norris as both references disclose a computer architecture arrangement in which software, in conjunction, with a control register, is capable of changing the frequency of the clock supplied to a processor. Implementing Norris' teaching of an external (to the processor) control register and clock generator in Belt's laptop computer system 10 involves modifications of only routine skill in the art. Moreover, modifying Belt as described above would have involved known methods of chip design and therefore, would have yielded predictable results.

4. [1c]

73. Belt alone discloses or renders obvious, or in combination with Foster renders obvious, "wherein the clock controller controls the frequency of the clock signal so as to become a first frequency when the mobile terminal is in the open condition, and controls the frequency of the clock signal so as to become a second frequency lower than the first frequency when the mobile terminal is in the closed condition."

74. Belt discloses its laptop computer system 10 has a lid which is movable between the open and closed positions. *See* §X.A.1 (preamble). Lid switch 68 indicates whether the lid is open or closed and sends an appropriate signal accordingly. EX1004, 5:7-9.

75. Belt discloses embodiments wherein the user can configure the system such that when the lid of laptop computer system 10 is closed, the system turns off the backlight and/or produces an audible beep “without stopping the system from operating.” *Id.*, 6:42-50 (options 2 or 3). Specifically, Belt provides the following disclosure:

“If it was determined at block 111 that the lid is closed, then control proceeds to block 121, where a check is made to determine what is to happen when the lid is closed. In particular, the user is allowed to configure the system set-up information to specify that a lid close is to (1) place the system in the suspend mode, (2) turn off the backlight without stopping the system from operating, or (3) produce an audible beep and turn off the backlight without stopping system operation.”

76. Belt’s disclosure of a scenario in which the lid of laptop computer system 10 is closed but the system continues operating alone teaches, or at least renders obvious, this limitation. Specifically, a POSITA would have understood that in this scenario, for system operations to continue (without stopping the system from operating), the processor would be receiving an operating clock. Importantly, however, Belt teaches that it would be advantageous for battery performance for a processor to have a lower clock speed when processing speed is not critical. EX1004, 3:5-14. Accordingly, a POSITA would have further understood that when the lid to Belt’s laptop computer system 10 is closed, higher processing speeds are not critical because the system would not be in active use.

EX1004, 1:17-21 (the keyboard and display of portable computer 10 are hidden when the lid is closed.

77. It is therefore my opinion that a POSITA would have also understood or at least found it obvious that when Belt's laptop computer system 10 is closed, Belt's clock controller (*see* limitation 1[b], §X.A.3) would control the frequency of the clock signal to main processor 11 to be a lower clock speed to increase battery performance as taught by Belt, relative to the clock speed when the lid is in the open position.

78. On the other hand, when the lid of Belt's laptop computer system 10 is open and the system is being used, Belt teaches it would then be advantageous for the processor to operate at higher clock speeds to rapidly process information. EX1004, 3:5-14. Accordingly, in my opinion, a POSITA would have further understood or at least found it obvious that when the lid of Belt's laptop computer system 10 is open, Belt's clock controller (*see* limitation 1[b], §X.A.3) would control the frequency of the clock signal to main processor 11 to be a higher clock speed (relative to the clock speed when the lid is closed) to rapidly process information as taught by Belt.

79. Additionally, the combination of Belt and Foster also renders this limitation obvious.

80. Belt discloses another embodiment wherein the user can configure the system such that when the lid of laptop computer system 10 is closed, the system is placed in a suspend mode. *Id.*, 6:42-50 (option 1). Specifically, Belt provides the following disclosure:

“If it was determined at block 111 that the lid is closed, then control proceeds to block 121, where a check is made to determine what is to happen when the lid is closed. In particular, the user is allowed to configure the system set-up information to specify that a lid close is to (1) place the system in the suspend mode, (2) turn off the backlight without stopping the system from operating, or (3) produce an audible beep and turn off the backlight without stopping system operation.”

81. Thus, when Belt’s laptop computer system 10 has its lid open, it is in “a first operational mode in which the processor executes instructions” (i.e., the claimed “first frequency”) and in “respons[e] to movement of the lid to its closed position ... switching the processor to its second operation mode,” “in which the processor is halted in a reduced power state...”. EX1004, 1:64-2:9. This other operation mode is also referred to as a suspend mode, which involves “placing the main processor 11 in a low power mode in which its clock is turned off and program execution is halted” and “remains in this mode until an event occurs which is intended to cause it to resume operation”—e.g., “if the lid is opened, the lid switch 68 will, through the signal processing circuit 13, cause the resume

control circuit 41 to produce a resume reset, which in turn causes the processor 11 to begin executing the reset handler routine of FIG. 7.” *Id.*, 10:58-68.

82. Foster discloses that in addition to a suspend mode—which is substantively similar, if not identical, to the suspend mode of Belt—the Intel 386SL processor may provide “an idle mode” in which “the CPU clock is slowed significantly” from 20 Mhz to 5Hz. *See* EX1005, 79:61-80:1; *compare id.*, with EX1005, 60:18-20 (disclosing stopping the processor’s clock in the suspend mode of Foster). Foster discloses that the idle mode is much simpler than the suspend mode, and it is possible to resume to run mode in a shorter time than required for the suspend mode. *Id.*, 80:7-9.

83. It would have been obvious to a POSITA to combine the teachings of Belt and Foster to modify Belt to enter, when the lid of laptop computer system 10 is closed, an idle mode such that a lower frequency clock signal (relative to the clock frequency when the lid is open) is fed to Belt’s main processor.

84. Belt and Foster are directed to the same field of endeavor and are analogous prior art to the ’417 patent since each relates to performance-based processor clocking power management techniques for portable computer systems. *See* §X.A.3 (discussing the Belt and the ’417 patent being analogous art); EX1005, 19:9-11 (“Power consumption within the processor 311 is dependent on its clock speed, and in particular is lower for lower clock speeds.”), 28:11-18 (“In a

situation where the user is operating on battery power and is running a program which does not require fast processor speed, intentionally reducing the processor speed will reduce power consumption and thus permit the user to operate the system longer before the battery requires recharging.”). Notably, Belt incorporates by reference U.S. App. No. 07/752,342, the application to which Foster claims priority as a continuation thereof. EX1004, 2:57-63; EX1005, 1:6-7. It is also because of this incorporation by reference that a POSITA would have viewed the disclosures of Belt and Foster together.

85. As set forth in Foster, a POSITA would have understood the problem of Belt’s suspend mode was that it would take longer to exit from that suspend mode into a run mode, which would perceptibly degrade performance. *See* EX1005, 79:61-80:17. To overcome this problem, Foster expressly discloses the solution of an “idle mode” in which “the CPU clock is slowed significantly” from 20 Mhz to 5Hz. *See* EX1005, 79:61-80:1. In my opinion, a POSITA would have been motivated to implement Foster’s idle mode in lieu of Belt’s suspend mode because, as disclosed in Foster, the idle mode “is much simpler than the suspend or standby modes” and doing so would make it “possible [for the computer system] to resume to run mode in a shorter time than required for the other modes.” *Id.*, 79:61-80:17.

86. A POSITA would have had a reasonable expectation of success in making this modification since Belt and Foster's computer systems are substantively similar and each are based on the Intel 386SL. Implementing Foster's idle mode in lieu of Belt's suspend mode involves modifications of only routine skill in the art. Moreover, modifying Belt as described above would have involved known programming methods and therefore, would have yielded predictable results.

5. [1d]

87. Belt alone discloses, or in combination with Foster renders obvious, "wherein the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency when a specific processing is executed (PMI Handler routine of Belt, or incoming call processing of Foster) even if the mobile terminal is in the closed condition, and controls the frequency of the clock signal so as to become the second frequency after the execution of the specific processing is completed."

88. Belt alone discloses that when the lid is closed and laptop computer system 10 is in running at a low clock frequency (i.e., user configured operational closed-lid mode with lower clock frequency in Belt—*see* limitation 1[d], §X.A.4), and a PMI interrupt occurs, processor 11 "automatically begins execution of the PMI handler routine." EX1004, 7:46-55, Fig. 4. As part of this routine, "the

processor changes the register 32 in order to force the CPU to run at its fastest clock speed, so that the PMI routine will execute as fast as possible” (i.e., “the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency when a specific processing is executed”). *Id.* 7:67-8:2. After the PMI handler routine is completed, “the main processor restores to register 32 the clock speed which was in effect when the PMI occurred” (i.e. user configured operational closed-lid mode with lower clock frequency in Belt, or Belt’s suspend mode modified by Foster’s idle mode). *Id.*, 8:11-15. Therefore, Belt teaches controlling the frequency of the clock signal so as to become the second (lower) frequency after the execution of the specific processing is completed.

89. Additionally, the combination of Belt and Foster, wherein Belt’s suspend mode is implemented as Foster’s idle mode (*see* limitation 1[d], §X.A.5), renders this limitation obvious.

90. Belt discloses that “if the system is in the suspend mode and the modem 22 receives an incoming telephone call, the modem ring indicator signal MDMRI on line 43 will cause the resume control circuit 41 to produce a resume reset,” but if it is determined that the lid is still closed, “the main processor 11 will return to the suspend mode.” EX1004, 11:14-28.

91. Foster, on the other hand, discloses that when its system is in suspend mode, its processor may “configure[] itself as to which interrupts will wake it up from the suspend mode” such as an “interrupt event from the serial or modem ports, as well as the power management interrupt from the system control processor SCP 316.” EX1005, 60:10-20. Upon receiving such interrupt, Foster discloses that the processor “must restore the main processor 311 to its normal mode of functioning” (i.e., “the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency”), “or else incoming characters from a serial line or from a telephone lines may be lost” (the processing of incoming characters, i.e., “specific processing”). *Id.* Once the incoming characters from the serial line or telephone line are processed, “[t]hen a command within a main processor 311 is executed so that it stops its CPU clock and enters suspend mode” (i.e., “and controls the frequency of the clock signal so as to become the second frequency after the execution of the specific processing is completed”). *Id.*

92. Based on the teachings of Foster, it would have been obvious to a POSITA to further combine the teachings of Belt and Foster to modify Belt’s incoming call procedure when the lid is closed with that of Foster’s so that the clock frequency of Belt’s main processor increases so that incoming characters from a serial line or from a telephone line can be processed and not lost.

93. Belt and Foster are analogous prior art to the '417 patent for the reasons set forth in limitation 1[c], which are incorporated by reference herein. *See* §X.A.4. A POSTIA would have understood that the problem with Belt's closed-lid/suspend mode incoming call procedure is that the incoming call information will not be processed since the system remains in suspend mode. EX1005, 60:10-20. A POSITA would therefore have been motivated to implement Foster's suspend mode incoming call procedure in Belt so that Belt's processor 11 is returned to "its normal mode of functioning" so that "incoming characters from a serial line or from a telephone lines [are not] lost" and after processing the call, returning to idle mode to further conserve battery. EX1005, 60:10-20.

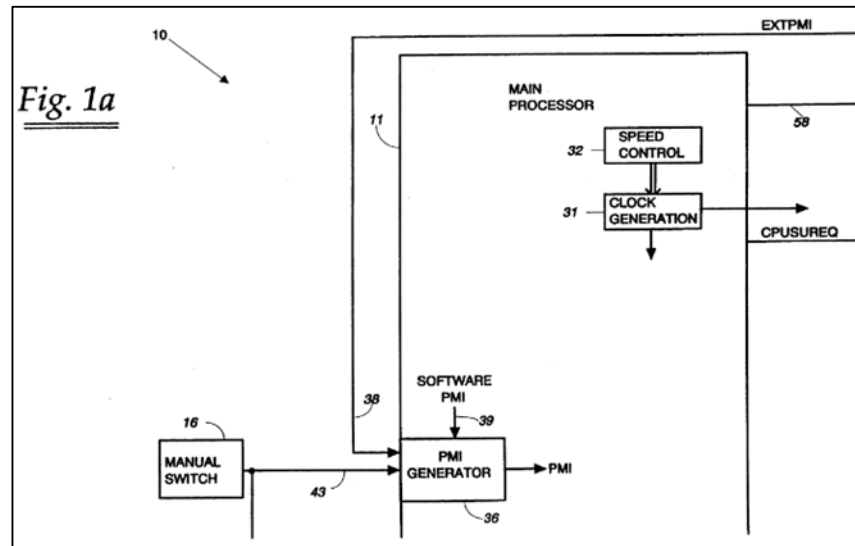
94. And, for the reasons set forth in limitation 1[c], a POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Foster as both references disclose substantively similar computer architectures, and both disclose an incoming call procedure as noted above. Modifying Belt's closed-lid/suspend mode incoming call procedure with Foster's suspend mode incoming call procedure would have involved known programming techniques and therefore, would have yielded predictable results.

B. Claim 2

95. Belt alone discloses, or in combination with Foster (with or without Norris) renders obvious, "the mobile terminal according to claim 1" (*see* claim 1—

§§X.A.1-5), “wherein the specific processing” (Belt’s PMI handler routine, and Belt implementing Foster’s hot key processing) “is a processing having an effect on a response to a request from the user” (a user actuating Belt’s switch 16, and actuating on Belt’s external keyboard Foster’s hot key).

96. Belt alone discloses that its laptop computer system 10 includes “a manually operable power control switch 16.” EX1004, 2:45-46, Fig. 1a (reproduced below).



97. Actuation of switch 16 (i.e., a request from the user) generates a PMI interrupt. *Id.*, 3:22-31. Belt discloses that when a PMI interrupt occurs from any source, the processor 11 “automatically begins execution of the PMI handler routine.” *Id.*, 7:46-55. The specific processing disclosed by Belt is its PMI handler routine. *See* limitation 1[d], §X.A.5. Therefore, Belt’s PMI handler routine is a

processing having an effect on a response to request from the user (actuation of switch 16) as recited in claim 2.

98. It should be noted that Belt discloses notebook computers at this time had a keyboard and display that were hidden and protected when the lid is in the closed position. EX1004, 1:15-21. However, Belt does not disclose hiding its power switch 16 in the closed position. Therefore, in my opinion, a POSITA would have understood the power switch 16 could be actuated when the computer is in the closed position.

99. Additionally, Belt and Foster each disclose that their respective laptop computer systems can be connected to an external keyboard, mouse, and display. EX1004, 4:57-64, Fig. 1b; EX1005, 20:49-58, Fig. 13b.

100. Foster discloses that “[w]hen the processor detects one of several special multi-key combinations [from the internal keyboard], it actuates the EXTPMI line to the main processor,” (i.e., “a request from the user”) which initiates a PMI, “so that any program in progress is immediately interrupted, a special function is carried out” (i.e., “the specific processing). *See* EX1005, 27:61-28:10, 39:63-66 (“a HK bit which indicates that a hot key multi-key combination has been pressed on the keyboard and was the reason for the PMI.”).

101. With respect to an external keyboard, although Foster discloses that “[h]ot keys are recognized only for the internal keyboard and not an external

keyboard” and that “[i]f a hot key actuation were received from an external keyboard, it *could* be discarded” (EX1005, 41:60-63), a POSITA would have understood that the external keyboard hot key could also not be discarded, which would be advantageous when the external keyboard is primarily being used. Indeed, Foster discloses that an external keyboard or mouse can send information to the SCP such that it “executes the interrupt service routine shown in Fig. 30.” EX1005, 41:44-48, 42:1-9 (recognizing external mouse actuation), 71:43-67 (external keyboard interrupt handler routine).

102. As explained previously, Belt and Foster are each analogous art to the ’417 patent. *See* limitation 1[b], §X.A.3 (describing analogousness of Belt and the ’417 patent), limitation 1[c], §X.A.4 (same re Belt, Foster, and the ’417 patent).

103. In my opinion, a POSITA would have understood the problem involved, namely, the need to allow the user of the Belt device the ability to change the clock frequency when desired—including when an external keyboard is primarily being used. To overcome this problem, Foster discloses the solution of providing various mechanisms for the user to change the clock frequency as desired. A POSITA would have been motivated to implement in Belt’s laptop computer system 10 of the Belt-Foster combination (with or without Norris) Foster’s hot key processor speed setting which advantageously allows a user to selectively prioritize “maximum performance” to rapidly execute “processor

intensive functions [] being performed” or “maximum power conservation” when the device is running on battery to prolong operational usability, or “balance between” the two. EX1005, 28:13-18 (“intentionally reducing the processor speed will reduce power consumption and thus permit[s] the user to operate the system longer”).

104. The modification to Belt could be implemented, for example, by adding Foster's hot key processor speed setting to Belt's PMI handler routine, whereby the hot key is entered through an external keyboard as taught, and rendered obvious, by Foster as described above. Indeed, as Belt discloses, the user can configure the laptop computer system 10 to remain in operation even when the lid is closed. *See* limitation 1[c], §X.A.4. Therefore, when the lid of laptop computer system 10 is closed, but the system remains operational and connected to an external keyboard, mouse, and display, a POSITA would have understood that the user may still use laptop computer system 10 in a conventional matter via these external peripherals and, in doing so, desire to increase or decrease the processing speed depending on the situation.

105. Regarding the implementation of Foster's hot key processor speed setting in Belt's laptop computer system 10, for the reasons set forth in limitation 1[c] (§X.A.4), a POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Foster as both references disclose

substantively similar computer architectures, and both disclose an EXTPMI as noted above. Implementing Foster's hot key processor speed setting in Belt's laptop computer system 10 would have involved known programming techniques and therefore, would have yielded predictable results.

C. Claim 4

1. [4a]

106. Belt in combination with Foster or Norris renders obvious “the mobile terminal according to claim 1 (*see* claim 1—§§X.A.1-5), further comprising an input unit (Belt's laptop computer system implementing Foster's hot key functionality, or Norris's performance control panel 54 and control panel 70, or in-BIOS performance state table 56) which allows a user of the mobile terminal to set the frequency of the clock signal.”

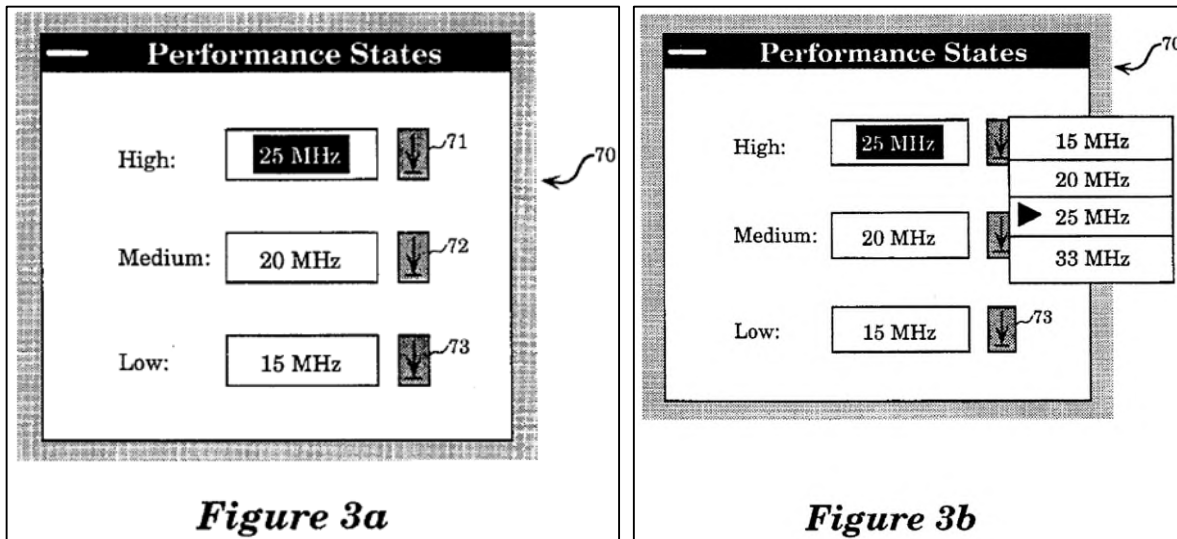
107. Belt discloses laptop computer system 10 includes a “[BIOS] program.” EX1004, 5:45-46. Belt further discloses a “power management interrupt (PMI) generator 36, which generates a special PMI interrupt in response to several conditions,” including an external PMI (EXT PMI) from an external source. EX1004, 3:22-28. In the event of a PMI, “the processor sets up a special stack for use by the PMI handler, and unlocks configuration registers so that they can be altered, such as the control register 32 which can be used to change the speed of the clock.” *Id.*, 7:64-67.

108. Foster discloses that “[w]hen the processor detects one of several special multi-key combinations, it actuates the EXTPMI line to the main processor,” which initiates a PMI, “so that any program in progress is immediately interrupted, a special function is carried out[.]” *See* EX1005, 27:61-28:10, 39:63-66 (“a HK bit which indicates that hot key multi-key combination has been pressed on the keyboard and was the reason for the PMI.”). As part of this PMI routine, “processor 311 unlocks certain internal configuration registers so that they can be altered, such as the control register 388 which can be used to change the speed of the CPU clock.” *Id.*, 23:23-26. Foster further discloses that certain special multi-key combinations, which are input by a user via a keyboard and initiates a PMI via an EXTPMI line, indicates that the special function to be carried out is either to have the “CPU to run at a slow clock speed,” or at a “fast processor speed.” *Id.*, 28:11-13 (hot key for slow clock speed), 28:29-36 (hot key for fast clock speed).

109. Norris discloses in one embodiment a “performance control panel 54 is an application program that enables a user of the computer system 10 to select from a set of predetermined frequencies of the processor clock 32 that correspond to the high, medium, and low performance states of the processor 12. The performance control panel 54 employs the display and interactive input functions provided by the operating system 48 to generate the control panel 70 and to enter the processor clock frequencies.” EX1006, 5:30-37; *id.*, 5:56-59 (“The user

employs a set of pulldown menu areas ... to select a desired processor clock 32 frequency for each [of the performance state]”).

110. Norris further discloses that after a user selects the frequency for the high, medium, low performance states, the “performance control panel 54 transfers



the clock speeds selected through the control panel 70 to the performance manager 44” which, in turn, “stores the selected clock frequencies for the high, medium, and low performance states in the performance state table 56” and “then uses the clock generator driver 42 to write the appropriate value into the clock speed register 34 to set the selected processor clock 32 frequency.” EX1006, 6:5-16; Figs. 3a, 3b (reproduced below).

111. In another embodiment, Norris discloses that “the clock speeds for the performance state table 56 are selected by a clock speed function in the BIOS 40 that enables user selections of clock speeds via command input.” *Id.*, 6:17-20.

112. It would have been obvious to a POSITA to combine the teachings of Belt and Foster or Norris to implement in the Belt-Foster or Belt-Norris combination either Foster's hot key processor speed setting technique or Norris's performance control panels 54 and 70 or user selectable in-BIOS performance state table 56 such that a user can manually set the frequency of the clock signal fed to main processor 11 to increase battery life or performance as desired.

113. As explained previously, Belt, Foster, and Norris are each analogous art to the '417 patent. *See* limitation 1[b], §X.A.3 (describing analogousness of Belt, Norris, and the '417 patent), limitation 1[c], §X.A.4 (same re Belt, Foster, and the '417 patent).

114. A POSITA would have understood the problem involved, namely, the need to allow the user of the Belt device the ability to change the clock frequency when desired. To overcome this problem, Foster and Norris disclose the solution of providing various mechanisms for the user to change the clock frequency as desired. A POSITA would have been motivated to implement in Belt's laptop computer system 10 either Foster's hot key processor speed setting technique or Norris's performance control panel as each advantageously allows a user to selectively prioritize "maximum performance" to rapidly execute "processor intensive functions [] being performed" or "maximum power conservation" when the device is running on battery to prolong operational usability, or "balance

between” the two. EX1006, 5:60-7:4 (allowing a user to select maximum performance, maximum power conservation, or balance between them, as desired), EX1005, 28:13-18 (“intentionally reducing the processor speed will reduce power consumption and thus permit[s] the user to operate the system longer”).

115. Regarding the Belt-Foster combination, for the reasons set forth in limitation 1[c], a POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Foster as both references disclose substantively similar computer architectures, and both disclose an EXTPMI as noted above. Implementing Foster’s hot key processor speed setting in Belt’s laptop in computer system 10 would have involved known programming techniques and therefore, would have yielded predictable results.

116. Regarding the Belt-Norris combination, for the reasons set forth in limitation 1[b], a POSITA would have had a reasonable expectation of success in combining the teachings of Belt and Norris as both references disclose similar implementations for changing the clock frequency (through a control register), and both disclose a BIOS as noted above. Implementing Norris’s performance control panel 54 or user selectable in-BIOS performance state table 56 in Belt’s laptop computer system 10 would have involved known programming techniques and therefore, would have yielded predictable results.

2. [4b]

117. Belt in combination with Foster or Norris renders obvious “wherein when the frequency is set by the user using the input unit (*see* limitation 4[a] — §§X.C.1-2), the first frequency is the frequency set by the user using the input unit.”

118. Petitioner incorporates by reference the discussion of the disclosures in Belt, Foster, and Norris in limitation 4[a] is if fully set forth herein. *See* limitation 4[a].

119. As explained in limitation 1[c] (§X.A.4), Belt discloses main processor 11 operates at higher clock speeds (the first frequency) to rapidly process information. EX1004, 3:5-14.

120. Foster discloses that a user can input a hot key combination to set the main processor 11 to have a “fast processor speed.” EX1005, 28:29-36.

121. Norris discloses that a user sets, among other performance states, the high performance state for the processor 12 via control panel 70 generated by performance control panel 54. EX1006, 5:30-37; *id.*, 5:56-59. Norris further discloses that “[i]f maximum performance for the processor 12 is always desired, then the user selects the fastest processor clock 32 frequency for the high, medium, and low processor states of the processor 12.” *Id.*, 5:60-63.

122. As explained in limitation 4[a], it would have been obvious to a POSITA to combine the teachings of Belt and Foster or Norris. The same reasoning applies to the limitation 4[b].

123. Accordingly, in the Belt-Foster combination, in implementing in Belt's laptop computer system 10 Foster's hot key technique in which a user sets main processor 11 to have a fast processor speed, a POSITA would have understood that "fast processor speed" is Belt's first (i.e., higher) frequency. *See* limitation 1[c], §X.A.4.

124. In the Belt-Norris combination, in implementing in Belt's laptop computer system 10 Norris's performance control panel 54 or user selectable in-BIOS performance state table 56 in which a user sets main processor 11 to set a frequency for a high performance state or the fastest processor clock 32 frequency for each performance state, as taught by Norris, a POSITA would have understood that "high performance state" or the fastest processor clock 32 frequency is Belt's first (i.e., higher) frequency. *See* limitation 1[c], §X.A.4.

D. Claim 5

125. The Belt and Norris combination renders obvious "the mobile terminal according to claim 4 (*see* claim 4—§§X.C.1-2), wherein the user can set the frequency of the clock signal in every processing using the input unit."

126. As set forth in claim limitation [4a], Norris discloses that after a user selects the frequency for the high, medium, low performance states, the “performance control panel 54 transfers the clock speeds selected through the control panel 70 to the performance manager 44” which, in turn, “stores the selected clock frequencies for the high, medium, and low performance states in the performance state table 56” and “then uses the clock generator driver 42 to write the appropriate value into the clock speed register 34 to set the selected processor clock 32 frequency.” EX1006, 6:5-16; Figs. 3a, 3b (reproduced below).

127. In another embodiment, Norris discloses that “the clock speeds for the performance state table 56 are selected by a clock speed function in the BIOS 40 that enables user selections of clock speeds via command input.” *Id.*, 6:17-20.

128. As set forth in claim limitation [4b], Norris discloses, without limitation, that “[i]f maximum performance for the processor 12 is always desired, then the user selects the fastest processor clock 32 frequency for the high, medium, and low processor states of the processor 12.” EX1006, 5:60-63.

129. As explained in limitation 4[a], it would have been obvious to a POSITA to combine the teachings of Belt and Norris to allow the user to set the frequency of the clock signal (using Norris’ performance control panel 54 or clock speed function in the BIOS 40). The same reasoning applies to claim 5, where the user is setting the frequency of the clock signal for every processing using the

input unit so that maximum performance can be achieved when desired as taught by Norris. *Id.*

130. Accordingly, in the Belt-Norris combination wherein a user selects maximum performance for processor 12 is always desired, as taught by Norris, I am of the opinion that a POSITA would have therefore understood that all—and so, *every*—processing by processor 12 would be processed at the fastest processor clock 32 frequency.

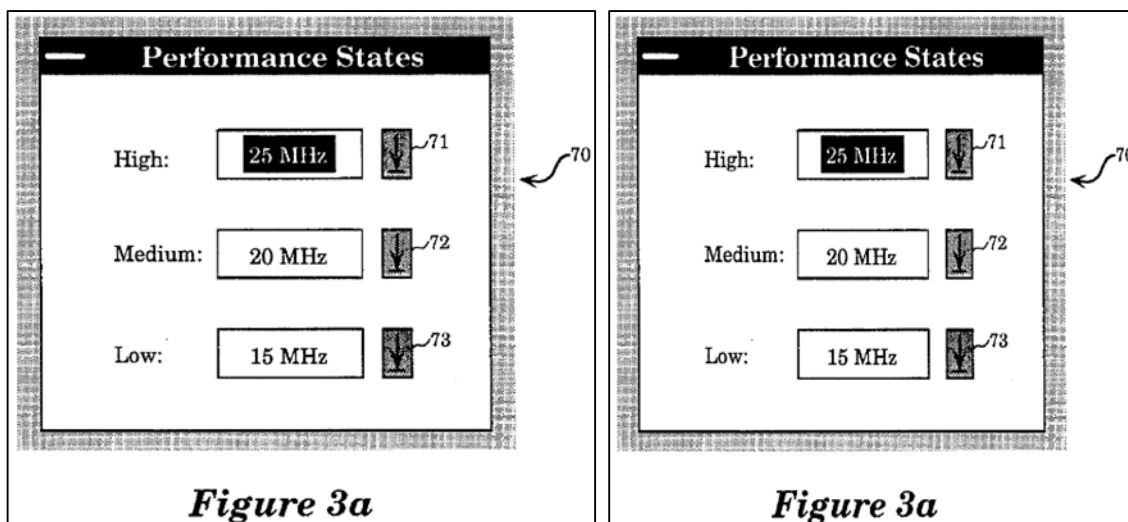
E. Claim 6

131. The Belt-Norris combination renders obvious “the mobile terminal according to claim 1 (*see* claim 1—§§X.A.1-5), further comprising a display which exhibits a display corresponding to the magnitude of the frequency of the clock signal (Belt’s laptop computer system 10 implementing Norris’s performance control manager 54 and control panel 70).”

132. Belt discloses that laptop computer system 10 includes a “display.” EX1004, 2:48-50, 4:67-5:2.

133. Norris discloses that “performance control panel 54 employs *the display and interactive input functions provided by the operating system 48 to generate the control panel 70* and to enter the processor clock frequencies.” EX1006, 5:30-37 (emphasis added); *id.*, 5:56-59 (“The user employs a set of

pulldown menu areas ... to select a desired processor clock 32 frequency for each [of the performance states]”), Figs. 3a & 3b (reproduced below).



134. As shown above in Figures 3a and 3b the control panel 70 displays information “corresponding to the magnitude of the frequency of the clock signal” grammatically (as “high,” “medium,” or low”) and numerically (respectively, in Fig. 3a, e.g., 25MHz, 20Mhz, and 15Mhz). Figs. 3a & 3b.

135. As explained in limitation 4[a], it would have been obvious to a POSITA to combine the teachings of Belt and Norris to allow the user to set the frequency of the clock signal. The same reasoning applies to claim 6, where a display provides the user with a GUI that facilitates the setting of the frequency of the clock signal for the performance states using the input unit so that the desired frequency for each performance state could be set as taught by Norris. *Id.*

136. Accordingly, in the Belt-Norris combination in implementing Norris’s performance control manager 54 in Belt’s laptop computer system 10, performance

control manager 54 would cause Belt's display to display control panel 70, as taught by Norris.

F. Claim 7

137. Belt discloses “the mobile terminal according to claim 1 (*see* claim 1—§§X.A.1-5), wherein the mobile terminal has a folded structure.”

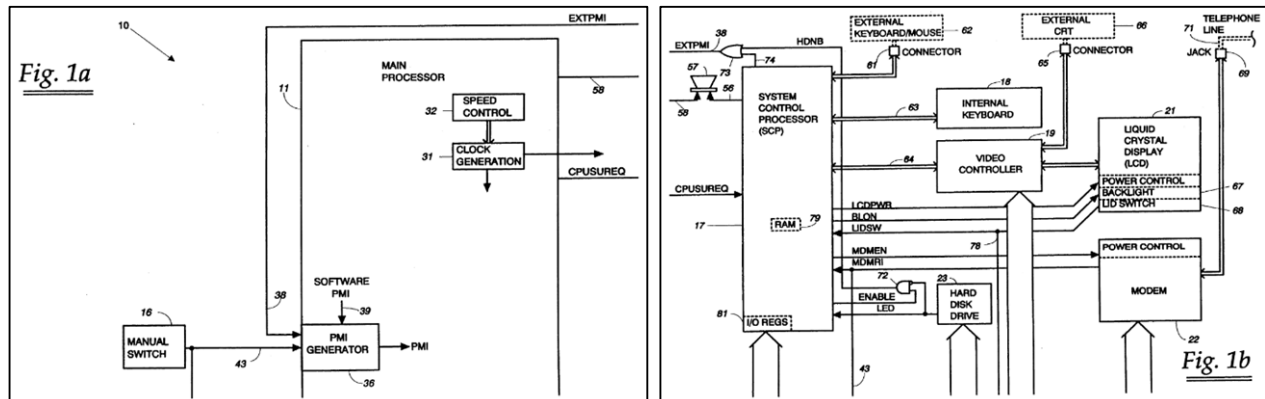
138. *See* claim 1[pre] (§ X.A.1); EX1004, 1:64-67; *see also id.*, 1:13-17 (“Portable computers of the type commonly referred to as ‘laptop’ computers and ‘notebook’ computers are becoming very popular [and] [t]hey typically include a housing with a lid which is movable between open and closed positions[.]”).

XI. GROUND 2: CLAIM 3 IS RENDERED OBVIOUS BY BELT, FOSTER, NORRIS AND ALBERTH

139. The Belt, Foster, Norris and Alberth combination renders obvious claim 3: “the mobile terminal according to claim 1 (*see* claim 1—§§X.A.1-5), wherein the specific processing is an image decoding processing or an address retrieval processing or a character conversion processing.”

140. Belt discloses a speaker 57 that produces an audible beep in response to “a signal produced by the main processor 11 on a line 58.” EX1004, 4:44-46;

see also *Id.*, Figs. 1a (line 58 connected to main processor 11), Fig. 1b (line 58 connected to speaker 57). Figs. 1a and 1b are reproduced below:



141. Belt further discloses that “if the system is in the suspend mode and the modem 22 receives an incoming telephone call, the modem ring indicator signal MDMRI on line 43 will cause the resume control circuit 41 to produce a resume reset,” but if it is determined that “the lid is still closed[,]” “the main processor 11 will return to the suspend mode.” *Id.*, 11:14-28.

142. Foster discloses that a conventional modem contains, for example, “user data stored within EEPROMs 4012.” EX1005, 75:67-76:2. Foster further discloses that “when the modem is [woken] up...the modem is fully programmed to continue normal operation and to respond to an incoming telephone call ... in accordance with the configuration programmed into the modem 332 by whatever program is running within the main processor 311.” *Id.*, 77:65-78:4. In one such example, Foster discloses that the modem is programmed, in part, to “come up with the speaker turned on so that any dialing noises are presented in the speaker of the computer.” *Id.*, 78:4-9.

143. As discussed in limitation 1[d] (*see* §X.A.5), in the Belt-Foster combination, it would have been obvious to modify Belt’s modem with the teachings of Foster’s modem such that modem 22 of Belt’s laptop computer system 10 processes incoming characters from a serial line or from a telephone line even when the lid of Belt’s laptop computer system 10 is closed.

144. Alberth, discloses “a closeable communication device 102 [that] has housing portions 110 and 112” that are “moveable between an open position and a closed position.” EX1007, 2:54-62; *Id.*, 2:63-3:3; *see also Id.*, 2:48-53 (“Although illustrated in a cellular telephone, the apparatus and method described hereinbelow will also find application in cordless telephones, two-way radios, pagers, personal digital assistants, and the like, and ‘device’ as used herein shall refer to each of these and their equivalents.”). Alberth further discloses that the closeable communication device 102 further includes “memory 305 [which] permanently stores operating instructions and user definable information, such as caller information in the form of an electronic phone book of names and associated telephone numbers[.]” *Id.*, 4:55-58; *Id.*, 4:62-65 (memory 305 may include EEPROM).

145. Alberth further discloses a “smart call indication” technique in which a controller—which “includes a microprocessor (not shown) for executing the operational instructions [and] processing the aforementioned received signals”

(5:3-6)—“retrieves the caller identification information of the incoming call ... and compares the caller identification information to caller information, such as telephone numbers, stored in the memory 305[.]” *Id.*, 7:12-18. “If a match between the caller identification information and the stored caller information is found,” an indication corresponding to a found match is produced. *Id.*, 7:18-21. If no match is found, a corresponding indication is produced. *Id.*, 7:27-30. Alberth discloses that these indications may be a ringer “emitting distinctive tones” for the match found and match not found determinations. *Id.*, 7:34-39; *Id.*, 8:53-56 (“The smart call feature embodied in steps 402, 424, 430, 432, 434, 436, 438, and 440 of the method of FIG. 4 provides a user with incoming call information when the housing 105 is in the closed position”).

146. In my opinion, a POSITA would have understood that Alberth’s “smart call indication,” also referred to as caller ID, is within the scope of “address retrieval” in view of the cellular phone embodiment of the ’417 patent.

147. As explained previously, Belt, Foster, and Norris are each analogous art to the ’417 patent. *See* limitation 1[b], §X.A.3 (describing analogousness of Belt, Norris, and the ’417 patent), limitation 1[c], §X.A.4 (same re Belt, Foster, and the ’417 patent). Alberth is also analogous to the ’417 patent because Alberth is directed to “a closeable communication device and method of operating the same that increases the usability of the device in the closed position by, for

example, supporting desirable user features and minimizing power consumption.”

EX1007, 1:63-67.

148. A POSITA would have understood the problem involved, namely, the need to allow the user of the Belt device the ability to determine when a known caller is calling Belt’s device, even when in a closed condition. A POSITA would have been motivated to implement, in Belt’s laptop computer system 10 in the Belt-Foster-Norris combination, Alberth’s smart call indication technique to allow a user to identify, when a device is in a closed position, whether an incoming call is from a known caller. EX1007, 9:6-9 (“This allows the user to view caller identification information of the incoming call on the display 134 of the device 102, which is hidden in the closed position 200[.]”). Further, because neither Belt nor Foster teach specifically how an incoming call is processed (EX1005, 77:65-78:4), a POSITA would have turned to art related to processing incoming calls, like that of Alberth, for such specifics.

149. The modification to Belt could be implemented, for example, by causing Belt’s speaker 57 to output a sound, as described in Norris, corresponding to a caller’s phone number matching that stored in memory, as taught by Alberth. EX1007, 7:34-39.

150. A POSITA would have had a reasonable expectation of success in making this modification since, as noted above, Belt’s modem, in view of Foster’s

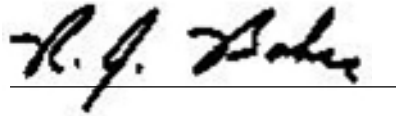
teachings of the same, includes components and functionality similar to those described in Alberth (EEPROM memory for storing user data and incoming call processing performed by a processor). Implementing Alberth's smart call indication techniques involve modifications of only routine skill in the art. Moreover, implementing Alberth's smart call indication techniques in the Belt-Foster-Norris combination as described above would have involved known programming methods and therefore, would have yielded predictable results. *Id.*

XII. CONCLUSION

151. My opinions are based upon the information that I have considered to date. I am unaware of any evidence of secondary considerations with respect to the '417 patent that would render any of the asserted claims non-obvious. I reserve the right, however, to supplement my opinions in the future to respond to any arguments raised by the patent owner of the '417 patent and to consider new information that becomes available to me.

152. I hereby declare under penalty of perjury under the laws of the United States of America that the following is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code.

Date: August 28, 2025

A handwritten signature in black ink, appearing to read "R. J. Baker", written over a horizontal line.

Dr. R. Jacob Baker