

**IN UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.

Petitioners,

v.

MAXELL, LTD.,
Patent Owner

Case: IPR2025-01309
U.S. Patent No. 7,577,417

DECLARATION OF MICHAEL BROGIOLI, PH.D.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and/or imprisonment under Section 1001 of Title 18 of the United States Code, and such willful false statements may jeopardize the validity of the patent which is under review in this proceeding.

Dated: May 5, 2026



Michael Brogioli, Ph.D.

TABLE OF CONTENTS

I. INTRODUCTION AND SUMMARY OF OPINIONS	3
II. MATERIALS CONSIDERED, METHODOLOGY, AND LEVEL OF ORDINARY SKILL	4
III. BACKGROUND AND QUALIFICATIONS	5
IV. TECHNICAL OVERVIEW OF THE '417 PATENT AND ITS PROSECUTION HISTORY	10
V. CLAIM CONSTRUCTION CONSISTENT WITH THE INTRINSIC RECORD.....	11
VI. LEGAL STANDARDS AND ANALYTICAL FRAMEWORK APPLIED	14
VII. GROUND 1: PETITIONERS FAIL TO SHOW THAT INDEPENDENT CLAIM 1 WOULD HAVE BEEN OBVIOUS OVER BELT IN VIEW OF FOSTER AND/OR NORRIS.....	15
A. Preamble [1pre] and “mobile terminal”	15
B. There is No Motivation To Combine Belt and Foster	16
C. Limitation [1c]: No disclosure of closed-condition lower second frequency linked to lid closure.....	24
D. Limitation [1d]: No closed-condition “specific processing” with a transient increase above the second frequency and a return to the second frequency	29
E. Dependent Claims 2 and 4-7 fall with claim 1.....	35
VIII. GROUND 2: PETITIONERS FAIL TO SHOW THAT DEPENDENT CLAIM 3 WOULD HAVE BEEN OBVIOUS OVER BELT IN VIEW OF FOSTER, NORRIS, AND ALBERTH.....	36
IX. ADDITIONAL OBSERVATIONS REGARDING PETITIONERS’ EXPERT DECLARATION (EX1003).....	37
X. CONCLUSION.....	38

I. INTRODUCTION AND SUMMARY OF OPINIONS

1. I have been asked by Patent Owner, Maxell, Ltd. (“Patent Owner” or “Maxell”), to evaluate the technical merits of Petitioners’ challenges to claims 1–7 of U.S. Patent No. 7,577,417 (the “‘417 Patent”) and to provide opinions that correspond to, and expand upon, the arguments in Patent Owner’s Response. My opinions are based on my experience, my review of the ‘417 Patent and its file history, the prior-art references presented in the Petition, and the Petitioners’ expert declaration (EX1003). These opinions are offered from the perspective of a person of ordinary skill in the art (“POSITA”) as of the earliest relevant date, and they address claim construction, the technical disclosures and combinations asserted by Petitioners, and why the asserted Grounds fail to establish unpatentability by a preponderance of the evidence.

2. Depending on new information learned, including positions taken by Petitioners or Petitioners’ expert, I reserve the right to supplement my opinions herein.

3. Although I am being compensated at my usual consulting rate for my time reviewing materials and preparing this declaration, my opinions expressed here are my own. My compensation is in no way dependent on the outcome of this case and I have no other financial interest in this matter or the parties thereto.

4. In forming my opinions, I have relied on my knowledge and experience as well as the documents and information referenced in this declaration.

5. In summary, the intrinsic evidence confines “mobile terminal” to a cellular phone, not a laptop, which defeats Petitioners’ Belt-based mapping to the claim preamble and dependent claims that recite a “mobile terminal.” Petitioners’ expert neither reconciles this intrinsic record nor supplies a supported bridge between Belt’s laptop and the claims when “mobile terminal” is properly construed as a cellular phone.

6. Even if one adopted Petitioners’ broader reading, Ground 1 fails to teach or render obvious limitations [1c] and [1d] because Belt’s closed-lid path either suspends and stops the clock or lacks the claimed closed-condition frequency control tied to “specific processing” with a raise-and-return frequency profile. Substituting Foster’s idle mode for Belt’s suspend mode contradicts Belt’s core power-conservation design, and Petitioners’ expert relies on hindsight and “could”/“would understand” rhetoric rather than prior-art teachings.

7. Ground 2 fails for the same reasons and, in addition, layers Alberth’s caller ID teachings from a closeable cellular device onto Belt’s laptop without a coherent, non-hindsight motivation, while still not supplying the missing closed-condition “raise-and-return” behavior required by limitation [1d].

II. MATERIALS CONSIDERED, METHODOLOGY, AND LEVEL OF ORDINARY SKILL

8. I reviewed the ‘417 Patent (EX1001) and its prosecution history (EX1002); Petitioners’ expert declaration by Dr. R. Jacob Baker (EX1003); the prior art identified in the Petition, including Belt (EX1004), Foster (EX1005), Norris (EX1006), and Alberth (EX1007); the Petition (Paper 3); Patent Owner’s Preliminary Response; and the deposition transcript of Dr. Baker (EX2022). In forming my opinions, I relied on my technical background and the cited materials, applying the perspective of a POSITA at the relevant time.

9. For purposes of this proceeding and consistent with Patent Owner’s Response, I adopt the POSITA definition Petitioners offered, namely, a person with a working knowledge of power management gained through a degree in Electrical/Computer Engineering or an equivalent degree and at least one year of experience in the field of power management. Additional graduate education could substitute for professional experience, and significant experience in the field could substitute for formal education. Pet. at 8–9; EX1003, ¶¶44–47.

III. BACKGROUND AND QUALIFICATIONS

10. Below is a summary of my education and experience. My *curriculum vitae* (“CV”), provided as EX2021, provides additional context regarding my professional background, experience, publications, patents, and other qualifications relevant to providing expert opinions. Here, I highlight experiences that are relevant to the technology described in the patent at issue.

11. I am currently an Adjunct Professor of Electrical and Computer Engineering at Rice University in Houston, Texas, and Managing Director of Polymathic Consulting in Austin, Texas. I received my Bachelor of Electrical Engineering from Rensselaer Polytechnic Institute in 1999, my Master of Science in Electrical and Computer Engineering from Rice University in 2003, and my Doctorate of Electrical and Computer Engineering from Rice University in 2007.

12. While at Rice University, I developed various computer architecture designs for embedded and high-performance systems, including multi-core and low power systems used in processing various workloads, including multimedia, telecommunications and networking. For example, from 1999 to 2003, I worked in the area of low-power computing, specifically focusing on dynamic power management and performance of configurable computing and memory systems with workloads, including multimedia and signal processing. From 2002 to 2004, I developed Spinach, a computer architecture design and modeling toolset, which models system components common to all programmable computing environments, including memory systems, multi-core microprocessor systems, and related hardware components. These systems targeted networking hardware and software solutions. From 2004 to 2009, I developed Spinach DSP-FPGA, a modular and composable simulator design infrastructure for programmable and reconfigurable embedded SOC architectures specifically targeting mobile/cellular, low-power, and

embedded and portable computing devices running networking and multimedia workloads. From 2005 to 2009, I developed and published a retargetable compiler infrastructure and hardware design exploration toolkit for systems microprocessor design, which facilitated the design space exploration of microprocessors and multi-core processor designs. Many of these tools have been used at United States universities in the area of electrical and computer engineering research.

13. In the late 1990s, I was a hardware and software developer at Vicarious Visions in New York, developing third-party titles for Nintendo's handheld consoles, in addition to various hardware and software interfaces and solutions. During my career, I have served as Chief Technology Officer, advisory board member, and board of directors' member, often in co-founding roles.

14. From June 2006 to August 2007, I worked as the Technical Co-Founder of Method Seven LLC in Boston, MA, working with high-performance software and hardware systems architecture. I am currently a co-founder, co-inventor, and Chief Technology Officer of Network Native, an Internet of Things technology company as well as others that are detailed on my CV.

15. I have held the position of Adjunct Professor at Rice University since 2009 and the position of Managing Director at Polymathic Consulting since 2011. At Rice University, I instruct graduate-level curriculum in the areas of computer architecture, hardware and software systems, and technologies related to the subject

matter at hand. At Polymathic Consulting, I work with a range of technologists from early-stage start-ups to Fortune 500 companies on similar technologies.

16. From 2008 to 2009, I was Senior Engineer working in high-performance compiler designs and next-generation multi-core microprocessors and architectures at Freescale Semiconductor in Austin, Texas. From November 2009 to October 2011, I was Chief Architect, Senior Member Technical Staff, at Freescale Semiconductor in Austin, Texas (formerly Motorola), responsible for management of technology, engineering roadmaps, design lead on software infrastructure, and next-generation multi-core microprocessor architectures. During my tenure at Freescale Semiconductor, I was in charge of system developer tools. These included tools used for the programming of processors, simulation and modeling, and related technologies including digital networking and multimedia solutions. Many of these architectures and solutions were used in wireless telecommunications and digital networking products.

17. I have previously worked for Texas Instruments' Advanced Architecture and Chip Technology division in Houston, Texas, in the areas of high-performance mobile and embedded systems design at the hardware and systems software level, specifically around heterogeneous computing, including solutions used in embedded, wireless telecommunications, and multimedia processing. I also

have worked at Intel Corporation's Microprocessor Research Labs in the areas of computer architecture and compiler technologies.

18. I am recognized as an expert in the field of computer architecture, computer hardware and computer software systems as they relate to the subject matter at hand. I am a member of the Institute of Electrical and Electronics Engineers (IEEE) and Association for Computing Machinery (ACM) and have been a steering committee member for the IEEE and ACM Design Automation Conference since 2011 and have previously held the role of Program Chair of Design Automation Conference in the area of Embedded Computing. I have also been a reviewer and contributor to a number of IEEE and ACM technical conferences during the course of my career.

19. Over the past 20 plus years, I have authored numerous peer-reviewed publications, as well as engineering books in the area of computer hardware and software design. Many of these incorporate technologies specific to the subject matter at hand. These publications are disclosed in my CV. I have previously served as an engineering consultant and testifying witness on matters related to, and including, microprocessors and multi-core technology as well as audio and video processing technology, peripherals and interfaces similar to those mentioned in the patents at suit in this matter.

20. My curriculum vitae contains more information on my background and experience, as well as the cases in which I have served as an expert witness.

IV. TECHNICAL OVERVIEW OF THE '417 PATENT AND ITS PROSECUTION HISTORY

21. The '417 Patent addresses power management in a mobile terminal—specifically a cellular phone architecture—that varies CPU clock frequency to balance processing speed and current consumption in response to user inputs and specific processing needs, including when the device is in a closed condition. EX1001, Abstract, 1:15–16.

22. The specification explains that the CPU receives a clock through a clock controller, that the frequency determines processing speed and power draw, and that, during specific processing, the clock can be raised and then returned to a lower level to conserve power. EX1001, 2:46–3:27. The patent discloses a folding condition detector, closed/open behavior, and explicit examples of specific processing such as image decoding, address retrieval, and character conversion processing that affect user responsiveness. EX1001, 5:35–38, 5:58–6:2, 2:65–3:2.

23. Every embodiment disclosed in the specification is directed to a cellular phone:

- FIG. 1 is described as “a block diagram showing the configuration of a first embodiment of a cellular phone according to the invention.” EX1001, 1:55–57.

- FIG. 2 shows “the configuration of a second embodiment of a cellular phone according to the invention.” EX1001, 1:58–60.
- FIG. 3 shows “a third embodiment of a cellular phone.” EX1001, 1:61–63.
- FIG. 4 shows “a fourth embodiment of a cellular phone of a folded structure.” EX1001, 2:1–4.

24. The prosecution history confirms the criticality of the closed-condition frequency control to the patentability of the claims. During prosecution, the Examiner identified the feature now recited in limitation [1d] as the point of distinction over the applied art, explaining that “the applied references fail to disclose or render obvious the claimed limitation of the mobile terminal according to claim 1, wherein the clock controller controls the frequency of the clock signal so as to become a frequency higher than the second frequency when a specific processing is executed even if the mobile terminal is in the closed condition, and controls the frequency of the clock signal so as to become the second frequency after the execution of the specific processing is completed.” EX1002, at 32.

25. The applicant accordingly amended the claims to incorporate this distinguishing limitation, and the Examiner allowed what are now claims 1–7. EX1002, at 14. The prosecution history thus confirms the non-obviousness of the exact closed-condition behavior Petitioners have failed to demonstrate in this IPR.

V. CLAIM CONSTRUCTION CONSISTENT WITH THE INTRINSIC RECORD

26. Patent Owner's Response explains, and I agree from a technical perspective, that "mobile terminal" should be construed in accordance with the intrinsic record to mean a cellular phone, not a laptop computer.

27. The '417 Patent repeatedly and consistently describes a cellular phone throughout. The Abstract states: "There is provided a cellular phone taking into consideration enhancement in processing speed and reduction in current consumption." EX1001, Abstract. The Background section states: "The present invention relates to a cellular phone comprising a central processing unit (CPU)." EX1001, 1:15–16. Every embodiment described in the Detailed Description and shown in Figures 1–4 is expressly directed to a cellular phone. *See, e.g.*, EX1001, 1:55–2:4. The specification discloses "cellular phone" at least forty-six times and does not mention "laptop" even once.

28. The fourth embodiment (FIG. 4) of the '417 Patent specifically describes the cellular phone of a folded structure with a folding condition detector for detecting whether the cellular phone is in a folded (closed) condition or in an unfolded (open) condition, a first display unit disposed at a position visible even in the folded condition, and a second display unit at the folded-down side. EX1001, 5:35–50. These are quintessential cellular phone form-factor features, not laptop features. A POSITA would understand that the '417 Patent's teachings regarding closed-condition clock-frequency management, folding condition detection, image

decoding, address retrieval, and character conversion are all directed to the cellular phone context.

29. A POSITA would also understand that cellular phones of the relevant time period had fundamentally different power management architectures, form factors, and use patterns compared to laptop computers. The specific teachings of the '417 Patent—including clock frequency management tied to specific processing such as image decoding, address retrieval, and character conversion, and user-directed clock manipulation—are all directed to the cellular phone context, not to a laptop context. For example, cellular phones of the relevant time period had fundamentally different power management architectures, form factors, and use cases in comparison with laptop computers in the same time period.

30. Petitioners' expert, Dr. Baker, applied a plain-meaning approach but then equated Belt's "laptop computer system 10" to the claim preamble's "mobile terminal," without supplying any analysis connecting a laptop to the intrinsically-defined cellular phone context. *See* EX1003, ¶¶56–57. This equating lacks an intrinsic-evidence basis. Dr. Baker confirmed at deposition that he has never designed a cellular phone, further underscoring the disconnect between his laptop-centric analysis and the cellular-phone invention of the '417 Patent. EX2022, 14:5-9.

31. Even if the Board were to adopt Petitioners' broader construction, Petitioners' Grounds still fail on the merits for at least the reasons explained in the sections below.

VI. LEGAL STANDARDS AND ANALYTICAL FRAMEWORK APPLIED

32. I am not a lawyer and am not offering any opinions regarding legal matters. However, I have been informed about the legal standards of patent law applicable to this proceeding, which I have used in developing my opinions expressed herein.

33. I understand that a patent claim can be invalid under 35 U.S.C. § 103 if the claimed subject matter would have been "obvious" to a person of ordinary skill in the art as of the priority date of the patent. I understand that an obviousness analysis should consider each of the so-called "Graham factors": (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the pertinent art; and (4) secondary considerations, if any.

34. I understand that a conclusion of obviousness may be based upon either a single prior art reference or a combination of prior art references. However, merely demonstrating that each of the claim elements was, independently, known in the prior art does not prove obviousness. It is a petitioner's burden to demonstrate both that a skilled artisan would have been motivated to combine the teachings of the

prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so. A petitioner must first show that all of the claimed elements are disclosed in the prior art.

35. I understand that expert testimony that merely recites conclusions or parrots petition arguments, without disclosing the underlying facts or data on which the opinion is based, is entitled to little or no weight. There must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

36. I understand that obviousness cannot properly be established through hindsight, and that elements from different prior art references cannot be selected to re-create the claimed invention using the invention itself as a roadmap. When the prior art teaches away from combining certain known elements, discovery of successful means of combining them is not obvious. I have applied these standards in evaluating the asserted Grounds.

**VII. GROUND 1: PETITIONERS FAIL TO SHOW THAT
INDEPENDENT CLAIM 1 WOULD HAVE BEEN OBVIOUS OVER
BELT IN VIEW OF FOSTER AND/OR NORRIS**

A. Preamble [1pre] and “mobile terminal”

37. Petitioners’ mapping relies on Belt’s “laptop computer system 10” to satisfy the preamble’s “mobile terminal capable of being changed from an open condition into a closed condition.” Pet. at 9-10; EX1003, ¶¶56-57. However, when

“mobile terminal” is construed consistent with the intrinsic record as a cellular phone, Belt does not disclose the claimed device. Belt describes a portable computer system (a laptop or notebook) with a housing and a lid, not a cellular phone. EX1004, Abstract.

38. Petitioners’ expert offers no intrinsic-evidence-based analysis linking Belt’s laptop to the patent’s cellular phone—only an assertion that Belt’s computer system is “indisputably within the scope” of the limitation because it can be changed from an open to a closed condition. EX1003, ¶57. This analysis is, at best, incomplete because under Petitioner’s logic, any device that can be in an open or closed position would meet the claim. However, I understand that a proper analysis considers the subject matter as a whole.

39. Even under Petitioners’ broader reading, the closed-condition frequency behaviors remain missing for limitations [1c] and [1d], as detailed below. Thus, Ground 1 fails regardless of the outcome of the preamble dispute.

B. There is No Motivation To Combine Belt and Foster

40. A POSITA would not have been motivated to combine the teachings of Belt with those of Foster to arrive at the claimed invention of the ’417 Patent, nor would such a combination have rendered the claims of the ’417 Patent obvious. The fundamental differences between the systems, their power management

architectures, and their respective approaches to managing device behavior upon lid closure each independently and collectively counsel against such a combination.

41. At the outset, it is critical to understand that both Belt and Foster are directed to portable computers—specifically, laptop or notebook-type personal computer systems—and not to cellular phones or mobile terminals of the type claimed in the '417 Patent. See EX1004, 1:13-23; EX1005, 1:24-35. Belt discloses a “notebook” type laptop computer system 10, which includes a main processor 11 implemented with an Intel 386SL, a hard disk drive 23, a floppy disk drive 26, a main memory 24, and numerous other conventional personal computer peripherals. EX1004, 2:43-53. Foster similarly discloses a conventional portable computer system of the type commonly referred to as a “laptop” personal computer, which includes a processor 311, a main memory 326, a hard disk drive 323, a floppy disk drive 327, a video controller 318, a modem 322, and other peripheral components not found in a cellular phone. EX1005, 5:45-55.

42. The power management concerns and constraints of laptop computers are fundamentally different from those of cellular phones. Laptop computers must manage power to a wide array of peripheral subsystems—hard disk drives, floppy disk drives, video controllers, modems, LCD backlights, and the like—each with its own power-down and power-up sequences. See EX1004, 2:43-53. By contrast, the '417 Patent is directed to a cellular phone in which the primary power management

challenge is controlling the clock frequency of the central processing unit to balance processing speed against current consumption from a small battery. EX1001, 1:43-52. A POSITA would have recognized that the vastly different system architectures, use cases, and design constraints of laptop computers compared to cellular phones would have discouraged any attempt to transplant the power management techniques of one type of device into the other.

43. The power management method disclosed in Belt is fundamentally incompatible with the dynamic clock frequency control taught and claimed in the '417 Patent. Belt's system responds to the closing of the lid by placing the main processor into a "suspend" state—a reduced power mode in which the processor is entirely halted and its clock is turned off. See EX1004, 1:64-2:23. More specifically, Belt discloses that the processor has "a first operational mode in which said processor executes instructions and a second operational mode in which said processor is halted in a reduced power state from which said processor can automatically exit in response to a predetermined condition." EX1004, 2:1-5. When the lid is closed, the system transitions from the first mode to the second mode; the processor's clock is stopped, power is shut off to most system components via the SYSVCC line, and the system enters a very low power state. See EX1004, 3:62-67, 9:6-17.

44. This is a binary, all-or-nothing approach where the processor is either running at its normal operational speed or it is completely halted. See EX1004, 6:45-50, 9:14-17. Belt does not teach, suggest, or contemplate adjusting the frequency of the processor's clock signal in response to the lid being closed while permitting the processor to continue executing instructions. Nor does Belt teach temporarily increasing the clock frequency to execute specific processing while the lid remains closed—the very feature claimed in the '417 Patent. In Belt, once the lid is closed and suspend mode is entered, no processing occurs at all until a resume event (such as opening the lid) restores the processor to its fully operational mode. EX1004, 10:58-68.

45. Belt does reference a speed control register 32 and the ability to run the CPU at different clock speeds. See EX1004, 3:1-5. However, this feature is used in a narrow and specific context: when a PMI (Power Management Interrupt) handler routine is invoked, the system forces the CPU to its fastest clock speed so that the interrupt routine executes as quickly as possible, and upon completion of the interrupt handler, the original clock speed is restored. See EX1004, 8:11-15. This clock speed manipulation is not related to the open or closed state of the lid, is not used to modulate power consumption during normal operation, and does not constitute dynamic frequency scaling of the kind taught by the '417 Patent.

46. Foster likewise fails to teach or suggest modifying the processor's clock frequency in response to the lid being opened or closed. In Foster, the response to closing the lid is minimal: the system control processor (SCP) merely causes the speaker to beep and deactivates the backlight signal BLON to turn off the LCD backlight. See EX1005, 43:37-42. Critically, Foster explicitly teaches that "if the lid is closed during system operation the system does not automatically enter standby mode or suspend mode, but instead simply beeps to warn the user that the system is still active, and turns off the backlight for the LCD in order to conserve power." *Id.* Foster's system continues to run at whatever clock speed was previously in effect because the lid's position has no bearing on the processor's clock frequency.

47. Foster does disclose a mechanism for the user to select between a "fast" and "slow" CPU clock speed via hot key combinations. See EX1005, 28:11-35. When the user presses the "slow" hot key, the system beeps once and clears the FC (fast clock) flag, and when the user presses the "fast" hot key, the system beeps twice and sets the FC flag. See *id.* However, this clock speed selection is entirely user-driven and is not responsive to any physical state of the device such as the lid being open or closed. The hot key mechanism is simply a user preference setting, and Foster does not suggest or contemplate any automatic adjustment of processor speed based on the lid's position. Furthermore, like Belt, Foster forces the CPU to a fast clock speed during execution of the PMI handler routine, restoring the prior speed

only upon exit from the handler. See EX1005, 48:22-24. This, too, has no relationship to the lid's open or closed state.

48. The '417 Patent claims a mobile terminal capable of being changed from an open condition into a closed condition, comprising a processor and a clock controller, wherein the clock controller controls the frequency of the clock signal so as to become a first frequency when the mobile terminal is in the open condition, a second frequency lower than the first frequency when the mobile terminal is in the closed condition, and a frequency higher than the second frequency when specific processing is executed even if the mobile terminal is in the closed condition, with the clock signal returning to the second frequency after the specific processing is completed.

49. Neither Belt nor Foster, individually or in combination, teaches or suggests this particular arrangement. Belt teaches halting the processor entirely upon lid closure—not reducing its clock frequency to a lower operating speed while continuing to process instructions. EX1004, 10:58-61. Foster teaches continuing operation at the same clock speed when the lid is closed, with no adjustment to the processor frequency whatsoever. EX1005, 43:37-42. Neither reference teaches the concept of dynamically raising the clock frequency for specific processing while the device remains in the closed condition and then returning to a lower frequency after the processing is completed, as claimed.

50. Even if one were to assume, *arguendo*, that the teachings of Belt and Foster could theoretically be combined, a POSITA would have lacked motivation to do so. The two references employ fundamentally different and incompatible approaches to power management upon lid closure. Belt teaches complete system suspension—a drastic power-saving measure that halts all processing. See EX1004, 1:64-2:23. Foster teaches a minimal response—a warning beep and backlight deactivation—that does not alter the processor's operational state at all. See EX1005, 43:37-42. A POSITA seeking to improve power management in a cellular phone with a folded structure would not have looked to either of these laptop computer references, which address a different class of device with different power management requirements, and would not have found in them the teaching of dynamically scaling processor clock frequency as a function of the physical open/closed state of the device.

51. Moreover, a POSITA attempting to modify Belt with the teachings of Foster would have arrived at a system that either (a) continues to halt the processor upon lid closure (per Belt's core teaching) while adding a beep and backlight control (per Foster), or (b) simply beeps and turns off the backlight upon lid closure (per Foster) without any change to the processor's operational state. In neither scenario would the combination produce the claimed invention of the '417 Patent—a system that reduces the processor's clock frequency to a lower operational speed upon

closure while allowing the processor to continue executing instructions, and that temporarily increases the clock frequency for specific processing even while in the closed condition.

52. To arrive at the claimed invention by combining Belt and Foster, one would need to: (1) extract from Belt the concept that lid closure should trigger a change in the processor's operational state; (2) discard Belt's teaching that the processor should be completely halted in response to lid closure; (3) import from Foster the concept of variable clock speeds (the fast/slow hot key feature); (4) reconceive this user-driven hot key feature as an automatic response to lid position rather than user input; (5) further add the concept that specific processing should cause a temporary increase in clock frequency even in the closed condition; and (6) transplant all of these reconceived concepts from a laptop computer architecture into a cellular phone. Each of these steps requires the kind of impermissible hindsight reasoning that the law forbids, and none is suggested by the references themselves. The combination would amount to a fundamental redesign of both Belt's and Foster's power management architectures, guided not by the teachings of the references but by knowledge of the '417 Patent's claims.

53. In summary, a POSITA would not have been motivated to combine Belt and Foster to arrive at the claimed invention of the '417 Patent. The references teach different types of devices, employ fundamentally different power management

methods, and neither individually nor collectively teaches or suggests the dynamic clock frequency scaling based on the open or closed condition of a mobile terminal that is claimed in the '417 Patent. Any attempt to combine the two references to reach the claimed invention would require impermissible hindsight and a wholesale reconception of the references' teachings.

C. Limitation [1c]: No disclosure of closed-condition lower second frequency linked to lid closure

54. Limitation [1c] requires that “the clock controller controls the frequency of the clock signal so as to become a first frequency when the mobile terminal is in the open condition, and controls the frequency of the clock signal so as to become a second frequency lower than the first frequency when the mobile terminal is in the closed condition.”

55. Petitioners rely first on Belt's user-configurable options when the lid is closed. Belt, however, merely seeks to “provide an arrangement for causing a system to enter and subsequently exit suspend mode in response to closing and subsequent opening of a lid.” EX1004, 1:58-61. In other words, Belt limits its description to entering into and exiting from suspend mode, with no mention whatsoever of performing any kind of processing while in that suspend mode. Belt specifically mentions “an Intel 386SL” processor (EX1004, 2:53-56). A POSITA would understand that at the time of the invention of the '417 Patent the de facto power management mechanism defined by Intel and Microsoft for personal computers

using chips such as the Intel 386SL was as described, for example, in the Advanced Configuration and Power Interface Specification Revision 1.0 (“ACPI,” EX2023).

56. ACPI represents the knowledge of a POSITA at the time of Belt as it is “the key element in Operating System Directed Power Management (OSPM),” which “describes the structures and mechanisms necessary to move to operation system (OS) directed power management and enable advanced configuration architectures.” EX2023, 15. Under the de facto power management mechanism, five states—S0, S1, S3, S4, and S5—are defined, each representing the following system states:

- a. S0: Full execution
- b. S1: CPU halt (*i.e.*, the idle state of the Intel x86 processor)
- c. S2: Sleeping state
- d. S3: Suspend to RAM
- e. S4: Suspend to Disk
- f. S5: Off (requiring OS booting)

See EX2023, 155-157. Among these, S1 through S5 are all defined as states in which the clock is stopped. For example, in states S1-S4, the “processors are not executing instructions.” EX2023, 155-157. In S5, the “system is in the ‘soft’ off state and requires a complete boot when awakened.” EX2023, 157. Accordingly, a POSITA would understand that all disclosures in the prior art relating to variable clock speed

pertain to S0, the “working” state. *See* EX2023, 155-156. Advanced Configuration and Power Interface Specification Revision 2.0 (EX2024), released July 27, 2000, includes a similar description of states S0, S1, S2, S3, S4, and S5, demonstrating that a POSITA at the time of the ’417 Patent would have the same understanding as that at the time of Belt. *See* EX2024, 222-224.

57. A POSITA’s understanding of these states is mirrored in Belt’s discussion of three options for when the lid closes: “(1) place the system in the suspend mode, (2) turn off the backlight without stopping the system from operating, or (3) produce an audible beep and turn off the backlight without stopping system operation.” EX1004, 6:42-50.

58. Belt’s suspend mode (Option 1) stops the CPU clock and halts execution entirely: the suspend mode involves “placing the main processor 11 in a low power mode in which its clock is turned off and program execution is halted.” EX1004, 10:58-61. There is therefore no “second frequency” in suspend mode—there is no clock frequency at all. As Petitioners’ expert conceded at deposition, “If there is no clock, there is no clock frequency.” EX2022, 23:18-19. This defeats any mapping of Belt’s suspend mode to the “second frequency” of limitation [1c].

59. For the continued-operation options (Options 2 and 3), Belt does not tie any reduction in clock frequency to the act of closing the lid, nor does Belt disclose

that a lower “second frequency” is selected because the lid is closed. The disclosure is completely silent as to any such linkage. *See* EX1004, 6:27-7:10.

60. Petitioners’ expert, Dr. Baker, posits that a POSITA “would have understood” that a lower frequency results when the lid is closed because the system is “not in active use.” EX1003, ¶76. However, Belt does not say that. When asked about functional or performance differences between Belt’s Options 2 and 3, Dr. Baker confirmed the only difference is the audible beep, identifying no other “functional or performance differences” described by Belt. EX2022, 25:22-25. And when pressed, Dr. Baker could not identify any passage in Belt that specifically ties a reduction in clock frequency to the act of closing the lid under those non-suspend options. EX2022, 31:2-9, 32:9-10.

61. Moreover, Belt’s disclosure of continued operation with external peripherals connected (EX1004, 4:57-64) suggests maintaining operational clocking rather than decreasing it upon lid closure, because the processor would be used in conjunction with external keyboard, mouse, and display and would require the clock speed to be maintained to support such external elements.

62. Indeed, any discussion of changing clock speed in Belt is related to increasing clock speed to execute the PMI routine “as fast as possible” before “the main processor restores to register 32 the clock speed which was in effect when the PMI occurred.” EX1004, 7:68-8:2, 8:11-15. This temporary boost occurs during

system operation when the status of the lid is open. *See* EX1004, Fig. 4. Therefore, Belt does not disclose controlling the frequency of the clock signal so as to become a second frequency lower than the first frequency when the mobile terminal is in the closed condition.

63. Petitioners also invoke Foster to substitute “idle mode” for Belt’s suspend mode so that, upon lid closure, the processor could run at a much lower frequency (5Hz) rather than be halted entirely. *See* EX1005, 79:61-80:1; EX1003, ¶¶82-86.

64. However, adopting Foster’s idle mode for Belt’s suspend mode upon lid closure would undermine Belt’s entire design purpose. Belt’s invention is titled “System Suspend on Lid Close and System Resume on Lid Open,” and its core teaching is to maximize power savings by halting the processor entirely when the lid is closed. EX1004, Abstract. Dr. Baker agreed at deposition that “shutting something off will use less power than if something is on, even if that thing that’s on is running at a very low frequency as taught in Foster.” EX2022, 28:19-22. A POSITA would therefore have no reason to adopt the less power-efficient idle mode in place of Belt’s suspend mode when Belt’s specific goal is maximum power conservation upon lid closure.

65. In sum, neither Belt alone nor Belt plus Foster discloses or renders obvious a closed-condition “second frequency lower than the first frequency” tied

to the device being in the closed condition, as required by limitation [1c]. The deficiency is not cured by Norris, which Petitioners did not rely upon for limitation [1c]. *See* Pet. at 17.

D. Limitation [1d]: No closed-condition “specific processing” with a transient increase above the second frequency and a return to the second frequency

66. Limitation [1d] requires that, even when the mobile terminal is in the closed condition, the clock controller raises the frequency above the second frequency when executing a “specific processing,” and then returns the frequency to the second frequency upon completion.

67. Critically, limitation [1d] requires two distinct behaviors operating in concert while the mobile terminal remains in the closed condition: (1) a transient increase in clock frequency triggered by a “specific processing,” and (2) a return to the second frequency—not a stopped clock—after that specific processing is completed. The claimed “specific processing” is further defined by dependent claim 2 as “a processing having an effect on a response to a request from the user” and by claim 3 as “an image decoding processing or an address retrieval processing or a character conversion processing.” EX1001, claims 2–3. These are application-level, user-responsive tasks that require a running processor and a defined baseline clock frequency to which the system returns. None of the cited prior art teaches or suggests this raise-and-return behavior while the device remains closed.

68. Belt’s suspend-mode path when a modem ring occurs while the lid is closed is explicit: “if the system is in the suspend mode and the modem 22 receives an incoming telephone call, the modem ring indicator signal MDMRI on line 43 will cause the resume control circuit 41 to produce a resume reset,” but if it is determined that “the lid is still closed,” “the main processor 11 will return to the suspend mode.” EX1004, 11:14-28.

69. In suspend mode, the CPU clock is off and there is no frequency to raise or restore. Thus, when an incoming telephone call arrives while Belt is in suspend mode with the lid closed, Belt expressly teaches that the system “return[s] to the suspend mode”—*i.e.*, the clock turns off entirely—rather than returning to a “second frequency” as the claims require. As Dr. Baker conceded, if the clock is stopped, there is no clock frequency. EX2022, 23:18-19.

70. Accordingly, Belt does not describe increasing the clock speed while still in a closed condition and then returning to a second frequency, and the Petition offers no explanation regarding this point for claim 1.

71. Moreover, the ACPI framework discussed above with respect to limitation [1c] is equally fatal to Petitioners’ [1d] theory. As explained, the de facto power management mechanism for PCs defined by Intel and Microsoft provides that in any suspend state (S1–S5), processors are “not executing instructions” and the clock is stopped. EX2023, 155-157. Under this framework, there is no mechanism

for a sleeping or suspended PC to transiently raise its clock frequency to execute a “specific processing” and then return to a lower running frequency. The only path from suspend to execution in ACPI is a full system resume to the S0 (working) state—which is the antithesis of the claim’s requirement that the frequency increase occurs “even if the mobile terminal is in the closed condition.” Belt’s architecture, built on the Intel 386SL processor and following this de facto mechanism, inherits these constraints. Thus, a POSITA would understand that there is no technical basis in Belt’s PC architecture for the claimed closed-condition raise-and-return behavior.

72. Petitioners point to Belt’s PMI handler, where upon a PMI the CPU temporarily runs “at its fastest clock speed” and then restores the prior speed. EX1004, 7:67-8:2, 8:11-15. However, Belt’s PMI disclosure is context-sensitive. The “first thing the PMI handler does is to check the resume flag 44 (FIG. 1) in the processor 11 in order to see whether the processor 11 is in the process of resuming from a suspended state.” EX1004, 7:56-60. In a suspend state, “the main processor 11 is in a low power mode in which the clock is turned off and program execution is halted.” EX1004, 10:58-61. Belt discloses a separate “resume handler” that checks lid status and, “if the lid is opened, the lid switch 68 will, through the signal processing circuit 13, cause the resume control circuit 41 to produce a resume reset.” EX1004, 10:63-66. In contrast, if it is “determined that the lid is now closed, [] therefore the resume sequence will be terminated and at block 184 the system will

return to the suspend mode in order to wait for a further resume reset caused by subsequent raising of the lid.” EX1004, 11:39-44.

73. The “fastest clock” PMI execution disclosed in Belt is not tied to the closed condition nor to a specific processing occurring while closed. Rather, the suspend-mode handling, when the lid is closed, returns the system to suspend. Petitioners do not bridge this gap to show that the PMI-driven frequency raise occurs while the device is in the closed condition and that, upon completion of a “specific processing,” the clock is returned to a “second frequency” rather than to a stopped clock in suspend.

74. Additionally, Belt’s PMI handler is fundamentally different from the “specific processing” contemplated by the claims. Belt’s PMI is a system-level power management interrupt—a brief hardware-triggered routine that the operating system uses to manage power states (*e.g.*, checking suspend/resume flags, saving register states). EX1004, 7:50–8:15. It is not a user-responsive application-level task. In contrast, the ’417 Patent’s “specific processing” encompasses tasks such as image decoding, address retrieval, and character conversion—application-level processing that directly responds to user input and has “an effect on a response to a request from the user.” EX1001, 5:35–38, claim 2. A POSITA would not equate Belt’s brief system management routine with the claimed specific processing that triggers a sustained clock frequency increase to serve user-facing tasks. Petitioners offer no

explanation for how or why a hardware power management interrupt constitutes the type of user-responsive processing that the claims require.

75. Petitioners further rely on Foster to cure Belt’s suspend behavior by mapping Foster’s “incoming characters from a serial line or telephone line” processing to the “specific processing,” arguing the system would raise frequency to avoid losing data and then return to idle. EX1003, ¶¶89-94. But this is the same substitution that conflicts with Belt’s suspend-on-lid-close design and, again, presupposes replacing Belt’s resume-and-return-to-suspend behavior in the closed condition with Foster’s raise-and-return-to-idle pattern. The rationale is hindsight-driven, not supported by Belt’s teachings, and fails to account for Belt’s explicit return-to-suspend-when-lid-still-closed logic.

76. Regarding Foster’s idle mode, Dr. Baker conceded that Foster’s idle mode is only “reasonable to say that it could” be triggered by lid closure (EX2022, 29:3-4)—speculation, not a teaching. He further agreed that shutting the system off uses less power than keeping it on even at a very low frequency (EX2022, 28:19-22), confirming that substituting Foster’s idle mode for Belt’s suspend mode would undermine Belt’s design purpose.

77. Regarding limitation [1d] specifically, Dr. Baker could not identify any examples in Belt of specific processing that would increase clock frequency while the lid is closed, stating: “I don’t recall Belt giving those examples.” EX2022, 38:16.

When asked to justify the Petition’s desired closed-condition behaviors, he repeatedly characterized the analysis as a “design choice” that a POSITA “would understand that you could make” (EX2022, 43:13-18)—precisely the kind of hindsight-driven reasoning that cannot substitute for teachings in the references.

78. Dr. Baker’s characterization of the claimed behavior as a mere “design choice” (EX2022, 43:13-18) further underscores the Petition’s failure. A “design choice” argument presupposes that the prior art provides a baseline system in which the claimed feature is merely one of several straightforward options a POSITA would consider. But here, there is no baseline system in the prior art that operates at a reduced clock frequency in the closed condition while continuing to execute programs. Belt’s closed-condition options are either (1) suspend with no clock or (2) continued operation with no frequency reduction. Neither provides the prerequisite “second frequency” baseline from which to make the claimed “design choice” of transiently raising and then returning to that frequency. Thus, Dr. Baker’s “design choice” rhetoric cannot fill the evidentiary gap because the foundational conditions for such a choice do not exist in the cited references.

79. The combination of Belt and Foster also falls short. Petitioners offer no explanation that the interrupt of Foster would occur when “even if the mobile terminal is in the closed condition,” as claimed. *See* Pet. at 24-25. Instead, Petitioners seek support in their deficient expert declaration. *Id.* (citing EX1003, ¶¶92-94).

80. Norris likewise does not cure the deficiencies in the combination. Norris discloses a desktop/laptop performance manager that allows an application program to select a performance state to “maximize performance during processor intensive functions and to maximize power conservation during interactive functions.” EX1006, Abstract. However, Norris is entirely silent on any behavior tied to a closed or open condition of a device. Norris does not disclose a foldable or closeable device at all, let alone the specific behavior of increasing clock frequency for a specific processing “even if the mobile terminal is in the closed condition” and then returning to the second frequency upon completion. A POSITA would find no teaching in Norris that supplies the missing closed-condition raise-and-return behavior that is absent from both Belt and Foster.

81. Accordingly, Petitioners have not shown that Belt alone or Belt combined with Foster and/or Norris discloses or renders obvious the closed-condition “specific processing” frequency raise-and-return required by limitation [1d]. The Examiner’s allowance of the claims was premised on precisely this limitation, which is absent from Petitioners’ mapping.

E. Dependent Claims 2 and 4-7 fall with claim 1

82. Claims 2 and 4-7 depend directly or indirectly from claim 1, and Petitioners’ failure to establish the unpatentability of claim 1 necessarily defeats the challenges to its dependents. Petitioners’ additional mappings for the dependents do

not supply the missing closed-condition [1c] and [1d] behavior, and several dependent limitations (*e.g.*, user-input frequency setting and displays) are expressly disclosed in the '417 Patent's cellular phone context, not in the laptop architecture Petitioners employ.

83. Because Ground 1 fails as to claim 1, it fails as to claims 2 and 4-7 as well.

VIII. GROUND 2: PETITIONERS FAIL TO SHOW THAT DEPENDENT CLAIM 3 WOULD HAVE BEEN OBVIOUS OVER BELT IN VIEW OF FOSTER, NORRIS, AND ALBERTH

84. Claim 3 depends from claim 1 and requires that the “specific processing” is “an image decoding processing or an address retrieval processing or a character conversion processing.” For the reasons expressed above with respect to Ground 1, Petitioners have not met their burden to show that elements [1pre], [1c], and [1d] are rendered unpatentable by the Belt-Foster-Norris combination. Thus, Ground 2 fails at least due to the reasons discussed with respect to independent claim 1 in Ground 1.

85. Moreover, even if the Board were to reach the merits of claim 3, the four-reference combination of Belt, Foster, Norris, and Alberth lacks a coherent, non-hindsight motivation. Petitioners attempt to equate claim 3's “address retrieval processing” with Alberth's “smart call indication” technique—a caller ID feature from a closeable cellular telephone—by grafting it onto Belt's laptop computer

system. Pet. at 42-46. This mapping requires combining four disparate references from different fields—laptop power management (Belt), laptop processor architecture (Foster), desktop/laptop performance management (Norris), and cellular telephone call handling (Alberth)—without a principled reason beyond hindsight to do so.

86. Additionally, even under Petitioners’ proposed combination, the fundamental deficiency remains: Belt’s closed-condition path does not implement the transient frequency-raise-and-return behavior required by limitation [1d]. When Belt receives an incoming call while in suspend mode with the lid closed, Belt expressly teaches that the system checks lid state and, if still closed, “return[s] to the suspend mode”—*i.e.*, the clock turns off entirely. EX1004, 11:14-28. Layering Alberth’s caller ID functionality onto this architecture does not cure the absence of the claimed behavior of raising the clock frequency for specific processing in the closed condition and then returning to a second frequency upon completion.

87. Accordingly, Ground 2 fails for this additional reason.

IX. ADDITIONAL OBSERVATIONS REGARDING PETITIONERS’ EXPERT DECLARATION (EX1003)

88. Throughout EX1003, Dr. Baker relies on assertions about what a POSITA “would have understood” or “could implement,” rather than pointing to disclosures that actually teach the claimed closed-condition frequency control.

89. For example, his analysis of limitation [1c] posits that closed-lid “not in active use” conditions imply lower clock speeds (EX1003, ¶76), yet Belt does not tie any frequency reduction to lid closure under Options 2 or 3, and the continued operation with external peripherals would suggest maintaining operational clocks rather than decreasing them due to lid status.

90. Similarly, for limitation [1d], Dr. Baker cites Belt’s PMI handler “force fastest clock” excerpt and the subsequent “restore” step (EX1003, ¶¶87-88), but the handler expressly distinguishes resumes from suspend and, in the closed-lid suspend path, Belt returns to suspend if the lid remains closed—which means no return to a “second frequency.” Dr. Baker’s reliance on Foster’s idle-mode wake and return does not reconcile Belt’s explicit closed-lid return-to-suspend behavior, and it offers no persuasive reason to replace Belt’s suspend-on-lid-close design with idle mode in a way that still satisfies the claim’s closed-condition requirements.

X. CONCLUSION

91. In addition to the opinions and evidence expressed herein, I reserve the right to rebut any arguments made or evidence presented in response to this report. I also reserve the right to supplement this report based on further investigation or analysis. I also plan to use graphic exhibits and/or demonstratives to help illustrate the facts and opinions I have expressed herein.