

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

RADIAN MEMORY SYSTEMS, LLC,
Patent Owner.

Case IPR2025-01321
Patent 11,709,772

EXHIBIT 2020

DECLARATION OF DR. MARK JONES

TABLE OF CONTENTS

I. INTRODUCTION..... 3

II. QUALIFICATIONS 3

III. BASES OF OPINION 5

IV. APPLICABLE LEGAL STANDARDS 6

 A. Level Of Ordinary Skill In The Art.....6

 B. My Understanding Of Legal Standards8

V. CLAIMS AND GROUNDS AT ISSUE11

VI. OPINIONS 12

 A. Petitioner’s Olbrich/Yamada Combination.....12

 1. Petitioner Does Not Show A Motivation To Combine With A Reasonable Expectation Of Success..... 13

 a) Petitioner Does Not Identify Any Advantages To Its Proposed Modification.....13

 b) Petitioner’s Modification Would Not Provide Any Benefit To Olbrich’s System.14

 c) Petitioner’s Proposal Fails To Reconcile Yamada’s Single-Host-Based Maintenance With Olbrich’s Multi-Host Architecture.....17

 d) Petitioner Does Not Show A Reasonable Expectation Of Success. 23

 2. Petitioner Does Not Show “making a notification available to the host that recommends performing maintenance . . . wherein the recommendation is associated with the zone start logical block address of the specified zone” In Its Olbrich Combination. 27

a)	Petitioner’s “Capacity” Argument Does Not Show The Claimed “Notification.”	28
b)	Petitioner’s “Erase Count” Argument Does Not Show The Claimed “Notification.”	34
c)	Petitioner’s “Error Count” Argument Does Not Show The Claimed “Notification.”	38
VII.	PETITIONER’S GONZALEZ COMBINATIONS.....	39
A.	Petitioner Fails To Show A Motivation To Add Goss’s Host-Notification And Host-Side Maintenance To Gonzalez.....	41
1.	Gonzalez Does Not Motivate Petitioner’s Proposed Modification.....	41
2.	Goss’s Array-Level, User Prompted Notifications Do Not Motivate A Modification Requiring Host Notifications For A Specified Zone Based On Metadata.	43
B.	Petitioner Does Not Show “performing a multi-plane write of said data to erase units on different planes . . . using a common page address for the respective erase units on the different planes” In Its Gonzalez Combinations.	46
VIII.	CONCLUSION	49

I. INTRODUCTION

1. My name is Mark Jones. I have been retained as an expert witness to provide my independent opinion in regard to the matters at issue in *inter partes* review of U.S. Patent No. 11,709,772 (“the ’772 patent”) in IPR2025-001321. I have been retained by Radian Memory Systems, LLC (“Radian” or “Patent Owner”), the Patent Owner in this proceeding. Petitioner is Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (“Samsung” or “Petitioner”).

2. I am being compensated \$750 per hour for my time spent working in connection with this case. My compensation is in no way related to the outcome of this litigation. If called as a witness, I would testify as to the statements and opinions contained in this report.

3. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

II. QUALIFICATIONS

4. I graduated summa cum laude from Clemson University in 1986 with a B.S. in Computer Science and a minor in Computer Engineering, while holding a National Merit Scholarship and the R. F. Poole Scholarship. I graduated from Duke University in 1990 with a Ph.D. in Computer Science, while holding the Von Neumann Fellowship.

5. Upon graduation, I joined the Department of Energy at its Argonne National Laboratory facility. While at the Department of Energy, I received the IEEE Gordon Bell Prize.

6. In 1994, I joined the Computer Science faculty at the University of Tennessee. While at the University of Tennessee, I received a CAREER Award from the National Science Foundation.

7. In 1997, I joined the Electrical and Computer Engineering faculty at Virginia Tech. I was cited multiple times on the College of Engineering's Dean's List for teaching.

8. In 2021, I became a Professor Emeritus of Electrical and Computer Engineering at Virginia Tech.

9. During my academic career, my teaching included courses on computer architecture and computer organization. These classes frequently covered topics specific to storage systems and more specifically to flash storage systems—including, for example, the division of responsibility for storage management between software and hardware on a host system and software and hardware on an embedded controller. My research has also at times involved the integration of flash storage into various computer architectures.

10. In addition to the activities, education, and professional experience listed above, I have been involved in research projects that contribute to my expertise

relating to this report. While at Virginia Tech, for example, I was a primary or co-investigator on government and industrial research grants and contracts in excess of five million dollars.

11. A detailed record of my professional qualifications is set forth in the attached Exhibit A, which is my *curriculum vitae*, including a list of publications, awards, research grants, and professional activities. My *curriculum vitae* also lists the matters in which I have served as an expert.

III. BASES OF OPINION

12. In the course of conducting my analysis and forming my opinions, I have reviewed materials including those listed below:

- i. The Petition filed by Petitioner in IPR2025-01321,
- ii. U.S. Patent No. 11,709,772 (“’772 Patent”) (Ex. 1001);
- iii. The prosecution history of the ’772 Patent (Ex. 1002);
- iv. The Declaration of Dr. Heiner Litz in IPR2025-01321 (Ex. 1003) (the “Litz Declaration” or “Litz-Decl.”);
- v. U.S. Patent No. 8,386,700 (“Olbrich”) (Ex. 1004);
- vi. U.S. Patent Application Publication No. 2011/0271032 (“Yamada”) (Ex. 1005);
- vii. NVMe Base Specification Rev. 1.0b (“NVMe1.0b”) (Ex. 1006);

- viii. U.S. Patent Application Publication No. 2010/0049908 (“Gonzalez”) (Ex. 1007);
- ix. U.S. Pat. Pub. No. 2011/0302477 (“Goss”) (Ex. 1008);
- x. U.S. Pat. Pub. No. 2012/0096217 (“Son”) (Ex. 1009);
- xi. U.S. Patent No. 5,404,485 (“Ban”) (Ex. 1010);
- xii. U.S. Patent Pub. No. 2011/0153911 (“Sprouse”) (Ex. 1011);
- xiii. U.S. Patent Pub. No. 2012/0072807 (“Cornwell”) (Ex. 1012);
- xiv. The exhibits and other documents cited herein.

IV. APPLICABLE LEGAL STANDARDS

A. Level Of Ordinary Skill In The Art

13. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan,” or by the acronyms “POSA,” “POSITA” or “PHOSITA,” as of the time of the invention. I understand that the ’772 patent issued on January 3, 2023, and that it claims priority to Provisional Application No. 61/757,464, which was filed on January 28, 2013.

14. I have been told that the person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. I am instructed that “relevant” means relevant to the challenged claims of the ’772 patent.

15. I understand that factual indicators of the level of ordinary skill in the art include the various prior art approaches employed, the types of problems encountered in the art, the rapidity with which innovations are made, the sophistication of the technology involved, and the educational background of those actively working in the field. I understand that, in assessing the level of skill of a person of ordinary skill in the art, one should consider the type of problems encountered in the art, the prior solutions to those problems found in the prior art references, the rapidity with which innovations are made, the sophistication of the technology, the level of education of active workers in the field, and my own experience working with those of skill in the art at the time of the invention.

16. In this case, Dr. Litz has asserted in his declaration that a person of ordinary skill in the art as of the time of the '772 patent would have had “at least a Bachelor of Science degree in electrical engineering, or an equivalent field, and at least three years of experience with SSDs or other flash memory devices. Ex. 1003 [Litz-Decl.] ¶ 47. Petitioner adds to this description an assertion that “[m]ore education can supplement practical experience and vice versa.” Pet. 4. For the purposes of this declaration, I accept Dr. Litz’s proposed qualifications of a POSITA, as qualified by Petitioner. I exceed this skill level and thus, by Petitioner’s terms, I have the “qualification and experience necessary to assess the '772 Patent

based on the perspective of a POSA.” Pet., 4. I reserve the right to revisit the issue of the level of knowledge of the POSITA should the Petition be instituted.

17. As further discussed below, my opinions as stated in this declaration are valid even if the Board adopts a somewhat higher or somewhat lower level of ordinary skill in the art than proposed. For example, as will be discussed throughout my report, even a person with the level of knowledge or experience described by Dr. Litz or adopted by the Board as described above would not have a reasonable expectation of success in implementing certain aspects of the proposed combination as of the priority date of the ’772 patent.

18. In this report, the absence of an expressed opinion about any section or paragraph of the Petition or Dr. Litz’s declaration, does not indicate my agreement with the section or paragraph.

B. My Understanding Of Legal Standards

19. When considering the ’772 patent and stating my opinions, I rely on the following legal standards as described to me by the attorneys for Radian.

20. I understand that a patent claim is unpatentable if the claimed invention was anticipated by a prior art reference or would have been obvious to a person of ordinary skill in the art at the time of the purported invention.

21. I understand that anticipation requires that every limitation of the claim at issue be disclosed, either expressly or under principles of inherency, in a single prior art reference.

22. I understand that inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. Instead, it must be proven that the claim limitation not expressly found in the reference necessarily follows from what is found there.

23. I understand that an obviousness analysis involves comparing a claim to the prior art to determine whether the claimed invention would have been obvious to a person of ordinary skill in the art at the time of the invention in view of the prior art and in light of the general knowledge in the art as a whole. I also understand that obviousness is ultimately a legal conclusion based on underlying facts of four general types, all of which must be considered: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) any objective indicia of non-obviousness.

24. I also understand that obviousness may be established under certain circumstances by combining or modifying the teachings of the prior art. Specific teachings, suggestions, or motivations to combine any first prior art reference with a second prior art reference can be explicit or implicit, but must have existed before the date of purported invention. I understand that prior art references themselves

may be one source of a specific teaching or suggestion to combine features of the prior art, but that such suggestions or motivations to combine art may come from the knowledge that a person of ordinary skill in the art would have had.

25. I understand that a reference may be relied upon for all that it teaches, including uses beyond its primary purpose, but also including teachings that lead away from the invention. I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, although the mere disclosure of alternative designs does not teach away.

26. I further understand that whether there is a reasonable expectation of success in combining references in a particular way is also relevant to the analysis.

27. I understand that it is improper to use hindsight to combine references or elements of references to reconstruct the invention using the claims as a guide. My analysis of the prior art is made from the perspective of a person of ordinary skill in the art at the time of the invention.

28. I am not offering any legal opinions in this declaration nor am I qualified to do so. I only consider such legal standards in framing my opinions and conclusions as well as placing assertions made by Petitioner in the Petition into the proper context. Additionally, from a subject matter perspective, I understand that

the petitioner always has the burden of persuasion regarding a challenge of patentability of an invention under an inter partes review.

V. CLAIMS AND GROUNDS AT ISSUE

29. I understand that Petitioner has challenged the claims of the '772 patent as follows (Pet., 4):

- Claims 1-6, 8, 11-13, 15- 20, 22, 25-30 based on obviousness over Olbrich, Yamada, NVMe1.0bt (Ground I);
- Claims 1-6 based on obviousness over Gonzalez, Goss, and NVMe1.0b (Ground II);
- Claims 8 based on obviousness over Gonzalez, Goss, Ban, and NVMe1.0b (Ground III);
- Claim 11 based on obviousness over Gonzalez, Goss, Sprouse, and NVMe1.0b (Ground IV);
- Claims 12-13, 15-20, 22, 25-27 based on obviousness over Gonzalez, Goss, Son, and NVMe1.0b (Ground V);
- Claims 28-30 based on obviousness over Gonzalez, Goss, Son, Cornwell, and NVMe1.0b (Ground VI).

VI. OPINIONS

A. Petitioner's Olbrich/Yamada Combination

30. I have reviewed Petitioner's Ground I, which relies upon the combination of Olbrich, Yamada and NVMe1.0b. Pet., 5-40.

31. I understand that all of the challenges in Petitioner's Olbrich/Yamada/NVME ground (Ground I) build upon the argument that Petitioner offers for claim 1. *See, e.g.*, Pet., 16-18, 19-40. Accordingly, I have focused my analysis of Petitioner's Ground I on Petitioner's Ground I argument against claim 1. I reserve the right to supplement my opinions if the Petition is instituted.

32. Petitioner relies upon Olbrich as allegedly supplying the claimed "controller," "host," and "metadata," Pet., 9-13, but Petitioner recognizes that Olbrich does not teach "based on the metadata, making a notification available to the host that recommends performing maintenance on [a] specified zone" Pet., 15-16. Petitioner cites Yamada for this limitation.

33. Petitioner describes its proposed combination of Olbrich and Yamada as "adding a maintenance request module to the controller and translocating the maintenance command responsibility to host-side software" (Pet., 8) or as "incorporat[ing] Yamada's teaching into the system in Olbrich regarding host-initiated maintenance commands, along with the metadata variants triggering maintenance" (Pet., 9). But in my opinion, Petitioner does not show that a POSITA

would be motivated or able to combine Olbrich and Yamada as proposed with a reasonable expectation of success.

1. Petitioner Does Not Show A Motivation To Combine With A Reasonable Expectation Of Success.

a) *Petitioner Does Not Identify Any Advantages To Its Proposed Modification.*

34. Petitioner argues that a POSITA would be motivated to modify Olbrich because of “the benefits taught regarding host-initiated maintenance,” and that “Yamada describes a litany of advantages regarding data retention, longevity and performance of flash memory based on shared control with the host with respect to maintenance activities. Pet., 8-9 (citing Ex. 1003 [Litz-Decl.] ¶ 80, Ex. 1005 [Yamada] [0013], [0036]). But this argument does not identify any such “advantages,” or link them to Petitioner’s proposed modification.

35. Petitioner cites Yamada’s paragraph 13, which describes aspects of what Yamada calls its “adaptive command unit.” Ex. 1005 [Yamada] [0013]. This paragraph does not expressly identify any aspects of what it describes as “advantages,” whether in Yamada’s own system or in flash management generally. And Petitioner does not explain which aspects of this paragraph would motivate its proposed modification of Olbrich.

36. Yamada’s paragraph 36 also contains aspirational statements—that its system overall “improves data retention” and allows maintenance “in a reliable

manner.” But Petitioner does not connect such aspirations to the “maintenance request unit” it proposes to transplant into Olbrich and in my opinion, Petitioner has not shown that Olbrich would benefit from its proposed modification, as explained further below.

b) *Petitioner’s Modification Would Not Provide Any Benefit To Olbrich’s System.*

37. Petitioner suggests that its proposed modification would provide unspecified benefits to Olbrich. In my opinion, however, Petitioner does not show that this is the case.

38. As one example, Petitioner suggests by citation to Yamada’s paragraph 13 (Pet. 9) that Yamada advantageously allows for “data maintenance” “without requiring the data maintenance to be performed together with normal processing of the system.” Ex. 1005 [Yamada] [0036]. Here, however, Yamada discloses an aspect of many flash maintenance systems, including Olbrich and other systems that do not include Yamada’s “adaptive command unit” or Yamada’s “maintenance request unit. This is apparent from how Yamada elsewhere discusses “normal processing.”

39. “Normal processing” is not an established term in the art. In Yamada, “normal processing refers to the processing that involves at least a predetermined amount of communication performed between the access device and the nonvolatile

memory device, and *specifically includes initialization* of the nonvolatile memory device, data reading, and data writing.” Ex. 1005 [Yamada] [0021].

40. Under Yamada’s definition, a POSITA would understand that “normal processing” occurs, for example, when flash storage is being initialized to interact with a specific “access device,” and also when what Yamada refers to as its “access device” (which Yamada also calls its “access module,” Ex. 1005 [Yamada] [0072] & Fig. 1, or perhaps more generally, something often called a “host” in other systems involving flash storage) is requesting to read or write data to flash storage. Conversely, operations that occur without such access module requests would not qualify as “normal processing.”

41. Thus, when Yamada says in its paragraph 36 that maintenance may occur “without . . . normal processing” in its system, Yamada describes “maintenance” performed when the host is not initializing, reading, or writing. But this type of operation is not unique to Yamada.

42. A POSITA would recognize that performing “data maintenance . . . without requiring the data maintenance to be performed together with normal processing of the system” is not unique to Yamada, and not something that requires the components that Petitioner proposes importing from Yamada into Olbrich.

43. Indeed, Olbrich *itself* discloses a system in which what Yamada terms “maintenance” occurs outside of what Yamada terms “normal processing.” Olbrich

describes a “patrol function” on its “SSD Controller” being configured to run periodically, such as every 24 hours. *See, e.g.*, Ex. 1004 [Olbrich] 84:53–85:43. A POSITA would understand that Olbrich’s “patrol function” performs “maintenance” in the sense of Yamada—indeed, “maintenance” on a basis that is similar to what Yamada also describes. *Compare id.*, 86:28-35 (describing Olbrich’s “patrol function” as writing “corrected data . . . into a new SuperPage, using a read-modify-write operation” in the event that the detected “number of errors exceeds the threshold”) *with* Ex. 1005 [Yamada], [0007] (stating that “[w]hen the number of errors exceeds a criterion value, the data stored in the nonvolatile memory is to be refreshed”). Indeed, Petitioner cites this type of maintenance in express connection with its alleged **modification** of Olbrich via Yamada. *See, e.g.*, Pet., 15 (describing Yamada’s “maintenance request unit” determining a need for maintenance based on a “number of errors determined by the error correction unit” in connection with proposed modifications to Olbrich).

44. A POSITA would understand that Olbrich’s “patrol function” can **already** operate outside of what Yamada would term “normal processing.” By running the “patrol function,” *e.g.*, every 24 hours or “the next midnight,” maintenance can occur in Olbrich when the host is not initializing, reading, or writing. Ex. 1004 [Olbrich] 85:43; *see also, e.g., id.* 85:5-7 (“the function is

periodically interrupted to allow other operations to take place), and then shut down until the following midnight”).

45. A capability for flash maintenance to occur outside of what Yamada terms “normal processing” is not a capability that is missing from Olbrich, and for this reason, I do not see how Yamada’s reference to this topic suggests any benefit to Petitioner’s proposed modification.

46. Petitioner also cites Yamada’s paragraph 36 in connection with the alleged “litany of advantages” it alleges to exist in Yamada. Pet., 9. But Petitioner does not discuss this paragraph, and I do not see further support for Petitioner’s argument in that paragraph.

47. Accordingly, in my opinion, Petitioner’s argument—which does not identify any deficiencies in Olbrich that Yamada would rectify or supplement—does not show why a POSITA would be motivated to combine Yamada and Olbrich in the way proposed by Petitioner.

c) *Petitioner’s Proposal Fails To Reconcile Yamada’s Single-Host-Based Maintenance With Olbrich’s Multi-Host Architecture.*

48. Petitioner proposes that Olbrich’s controller be modified by “adding a maintenance request module to the controller and translocating the maintenance command responsibility to host-side software.” Pet., 8-9. Here Petitioner fails to address a key difference between Yamada’s flash management model, which

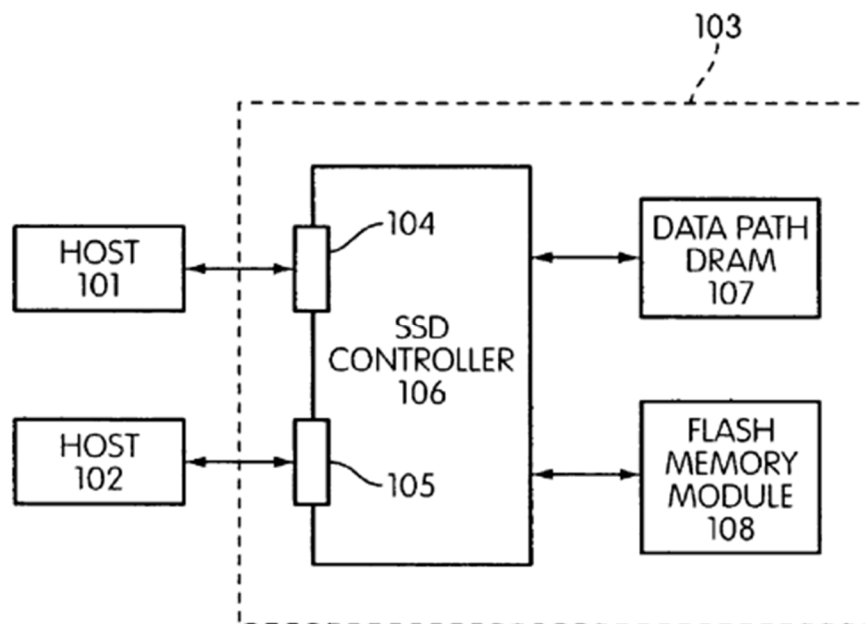
presumes a single host, and Olbrich's system, which is expressly a multi-host system. Any alleged advantages of Yamada that Petitioner would hope to attribute to "translocating ... command responsibility to host-side software" would depend on the details of exactly how this difference between Yamada and Olbrich is reconciled in the combined system. But Petitioner does not acknowledge this difference, let alone address it.

49. Yamada's touted advantage is explicitly based on a single host: Yamada's system-status monitoring and maintenance-determination logic live in the access device (host) and trigger commands when the host is idle. *See, e.g.*, Ex. 1005 [Yamada], Abstract ("An access module (130) receives the status of data stored in a nonvolatile memory (120) from a nonvolatile memory module (100), and . . . determines whether the maintenance is enabled based on the system status of the access module (130)"), [0019] ("the adaptive command unit determines whether maintenance is enabled based on the system status of the access device"), [0021] ("The access device performs maintenance of the nonvolatile memory device while the access device is not engaged in normal processing").

50. This method of scheduling maintenance works because the host can determine when the system is *not* in "normal processing" and order maintenance accordingly. This host-timed model is appropriate in the relatively simple single-host environments Yamada describes—portable products like digital still cameras

and mobile phones, *id.*, [0002]-[0003]—where a single host issues ordinary read/write commands and can readily police its own windows of “normal processing.”

51. Olbrich’s Figure 1 expressly depicts Olbrich’s multi-host architecture when it shows two independent “Hosts” 101 and 102 interacting with the “SSD Controller 106”:



Ex. 1004 [Olbrich] Fig. 1. Olbrich states that its “Hosts” 101 and 102 are “conventional host devices” which may be “servers,” and that each host potentially supports “multiple initiators,” which “may constitute separate physical devices or processes.” *Id.*, 4:64–5:2.

52. Olbrich's Figure 3 also graphically depicts the multi-host nature of Olbrich's system. In this figure, Olbrich's controller (within the "Board 103") has a component called a "host interface 310," which again is expressly depicted as connecting to two hosts.

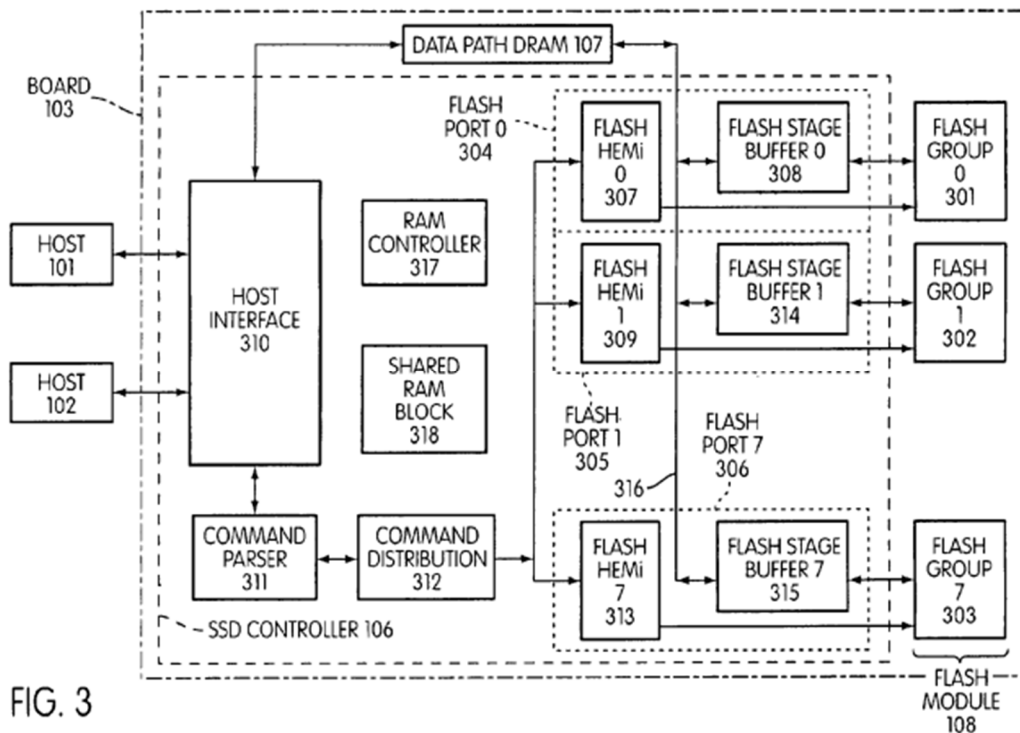


FIG. 3

Id., Fig. 3; *see also id.*, 20:36-43.

53. A POSITA would understand from these disclosures that there may be multiple servers (or Olbrich "hosts") attached to Olbrich's SSD device, as well as possibly multiple separate physical devices per host initiating data transfers to and from that device.

54. Olbrich also emphasizes that "from the perspective of Host 101, Host Interface 310 appears to constitute an interface to a conventional mass storage

device,” *id.*, 7:38-41, and that “Board 103” (containing Olbrich’s controller) “appears to constitute a conventional, rotating disk mass storage device.” *Id.*, 5:7-8. A POSITA would understand from these disclosures that Olbrich’s design does not presume its “Hosts” to have custom flash maintenance logic or the ability to communicate with the controller for purposes of coordinating access across multiple “Hosts.”

55. Although Olbrich expressly depicts two hosts, Petitioner’s suggestion to “translocat[e] the maintenance command responsibility to host-side software” in Olbrich, Pet., 8, does not distinguish between them. Petitioner’s failure to address this issue prevents Petitioner from identifying, let alone motivating, its proposed combination.

56. Petitioner does not address, for example: which of the two “hosts” (or multiple physical devices within those hosts) will contain Yamada’s host-side maintenance controls? Host 101? Host 102? Both? None of these alternatives would appear to work, because at least one of Host 101 and Host 102 would need to be aware of when the other is doing (or is about to do) the “normal processing” of Yamada. But there is no discussion or provision for this type of coordination in Yamada or in Olbrich.

57. Yamada’s “command generation unit,” for example, ultimately sends maintenance commands to the controller on the basis of the Yamada host’s

assessment of its *own* operating status. *See, e.g.*, Ex. 1005 [Yamada], Abstract, [0019], [0021]. Yamada, for example, explains that its single-host-side “adaptive command unit” includes a “system status monitoring unit,” a “maintenance determination unit,” and a “command generation unit”; the monitoring unit “monitor[ing] the system status of the access device”—that is, the host of which the monitoring unit is a part—and, when it determines the host is not engaged in “normal processing,” providing that information to the maintenance determination unit, which triggers command generation. *See id.*, [0014], [0017]. Yamada describes an alternative pathway in which the “system control unit” within Yamada’s “access device” supplies the status of the host directly to Yamada’s adaptive command unit. *Id.*, [0102]-[0104], [0115]. In either case, however, the host’s assessment of its own operating status is crucial to timing maintenance requests. Yamada does not disclose any interaction between its controller and multiple hosts, let alone a pathway by which one host could use the operating status of another host as an input when issuing its own maintenance commands, or a pathway by which one host could tell other hosts to refrain from normal processing because maintenance is occurring.

58. For at least these reasons, it is not clear how Petitioner is proposing to modify Olbrich, and in my opinion, Petitioner and Dr. Litz have not shown why a POSITA would be motivated to make whatever modification they are proposing, let alone be able to do so with a reasonable expectation of success.

d) *Petitioner Does Not Show A Reasonable Expectation Of Success.*

59. Petitioner states that “A POSA would have a reasonable expectation of success in incorporating this shared host functionality—adding a maintenance request module to the controller and translocating the maintenance command responsibility to host-side software—and it would have been straightforward and routine.” *Id.*, 8 (citing Ex. 1003 [Litz-Decl.] ¶ 79). I do not agree. As one example, because of Petitioner’s silence on how the single-host architecture of Yamada would be reconciled with the multi-host architecture of Olbrich, it is not clear what the proposal to “incorporat[e] this shared host functionality” even is, and more information about that proposal would be necessary to even address the ability of the POSITA to implement it.

60. In support of its argument that a POSITA would have had a reasonable expectation of success in implementing its combination of Yamada and Olbrich, Petitioner states:

Olbrich teaches various means to “maximize[] use of the host and flash interfaces” through the “use of multiple microprocessors in the controller design, thereby creating multiple parallel independent pipelines.” [Olbrich] 2:64–3:1. Due to this architecture, the system of Olbrich is capable of ready modification to include Yamada’s discrete maintenance modules.

Pet., 8.

61. But Petitioner does not connect any “use of multiple microprocessors” in Olbrich’s *controller* with its proposed modification, which involves adding “*host*-initiated maintenance commands” and “translocating the maintenance command responsibility to *host-side software*.” Pet., 7-8.

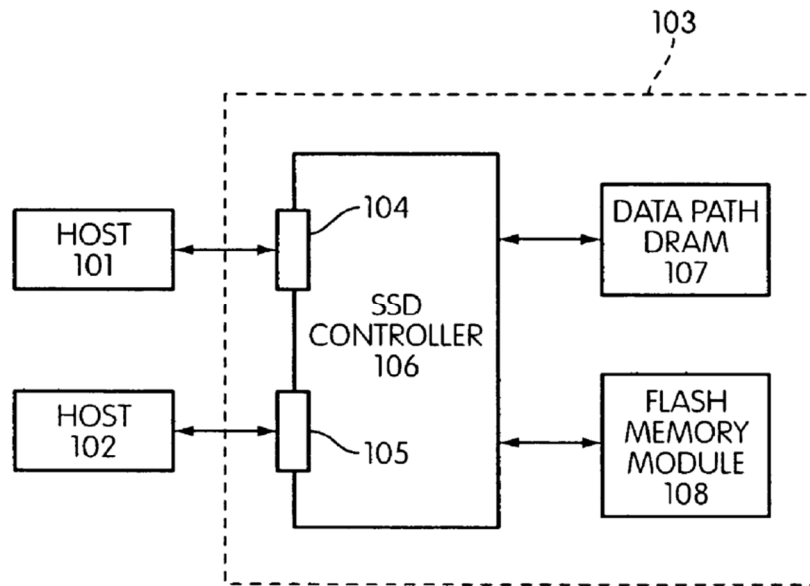
62. The portion of Olbrich cited by Petitioner does not suggest that it would be a “ready modification” of Olbrich to transfer aspects of its flash management to an Olbrich host. Therein, Olbrich emphasizes “the use of multiple microprocessors in the controller design” as part of discussing how Olbrich’s *controller* is able to parallelize individual requests that come from Olbrich’s hosts. *See, e.g.*, Ex. 1004 [Olbrich] 3:13-16 (describing its “*controller* architecture” as “breaking host-initiated transactions into a large number of independent flash reads and writes”), 2:63-67 (stating that “the use of multiple microprocessors in the *controller* design . . . create[es] multiple parallel independent pipelines, each of which is capable of handling a portion of a single transaction”), 3:2-4 (stating that its controller design “allows individual transactions to be broken up into many small portions, which can be reordered and handled in parallel to increase performance”). Olbrich describes this aspect of its controller design as effectively *hidden* from a host that may not even be aware that its requests are being broken into parallel streams. When Olbrich states, for example, that “[t]he use of parallel pipelines allows the controller to effectively mask the write latencies inherent in the use of flash memory,” *id.*, 3:7-

10, Olbrich is saying that one of its design goals is expressly to *hide* issues specific to flash management from its host by managing them internally.

63. Petitioner’s proposal to involve the host in flash management in Olbrich’s system is a technically substantial departure from Olbrich, for example, because while Olbrich’s unmodified controller is described as advantageously able to interface with what it describes as “conventional” hosts, it is not clear that Petitioner’s modified system would be able to do this.

64. Olbrich discloses that “Hosts 101 and 102 are *conventional* host devices, e.g., two servers that use mass storage resources or two host bus adapters serving one such server.” Ex. 1004 [Olbrich] 4:64-66. A POSITA would understand Olbrich’s reference to “conventional host devices” to include host devices that may not be aware that they are interacting with flash storage at all.

65. Olbrich’s focus on flash-agnostic hosts is also evident in Olbrich’s discussion of its Figure 1, which depicts its “SSD CONTROLLER” 106 within a “Board” 103:



Ex. 1004 [Olbrich] Fig. 1.

66. In discussing this figure, Olbrich states:

In the currently preferred embodiment, Board 103 is designed so that, *from the perspective of Hosts 101 and 102, Board 103 appears to constitute a conventional, rotating disk mass storage device*. This requires that Host Ports 104 and 105 be designed so that they are physically and logically indistinguishable from conventional mass storage interfaces for which Hosts 101 and 102 have been designed. Thus, *in the currently preferred embodiment, use of Board 103 does not require any redesign of Hosts 101 or 102*.

Ex. 1004 [Olbrich] 5:6-15.

67. Of course, Petitioner's proposal of "translocating the maintenance command responsibility to host-side software," Pet., 8, **would** require the "redesign" of "Hosts 101 and 102." Petitioner's proposal expressly requires a modified, flash-

aware host to handle what Petitioner identifies as “maintenance commands.” When not paired with such a host, Petitioner’s modified controller would defer flash maintenance indefinitely—waiting for approval that a “Host” in what Olbrich describes as its “currently preferred embodiment” would not be configured to provide.

68. Because Petitioner fails to address the host-side modifications that it is proposing in sufficient detail, it is not possible to determine what sorts of hosts *would* be able to work with Petitioner’s proposed combination of Yamada and Olbrich.

69. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown that a POSITA would have been able to implement the proposed combination with a reasonable expectation of success.

2. Petitioner Does Not Show “making a notification available to the host that recommends performing maintenance . . . wherein the recommendation is associated with the zone start logical block address of the specified zone” In Its Olbrich Combination.

70. Claim 1 recites “based on the metadata, making a notification available to the host that recommends performing maintenance on the specified zone, wherein the recommendation is associated with the zone start logical block address of the specified zone.” *See, e.g.*, Ex. 1001 [’772] cls. 1, 2. Petitioner admits that Olbrich does not disclose “making [any] notification available to the host” and introduces Yamada for this purpose. But Petitioner does not explain how multiple differences

between Olbrich and Yamada would be resolved in the combined system. In failing to explain this, in my opinion, Petitioner fails to show how this limitation is taught in its combination.

71. Petitioner identifies “SuperBlocks” in Olbrich with the claimed “zones,” Pet., 10-11, and garbage collection at the SuperBlock level in Olbrich as the claimed “maintenance on the specified zone.” Pet., 14-15. Petitioner identifies two candidates for “metadata” within Olbrich upon which a hypothetical “notification ... that recommends performing maintenance” could be based: Olbrich’s SuperBlock-level erase counts (Pet., 14) and Olbrich’s SuperBlock-level “capacity” information (Pet., 15). Petitioner suggests that in its combination with Yamada, this alleged “metadata” in Olbrich could be used to generate “maintenance requests” seeking garbage collection of a specified SuperBlock for the host of the combined system to choose to act upon. *See, e.g.,* Pet., 15.

a) *Petitioner’s “Capacity” Argument Does Not Show The Claimed “Notification.”*

72. As noted above, Petitioner argues that one alleged basis for a “making a notification available to a host” in its combined system is when “a ‘Counter value’ (SuperBlock capacity) ‘is at or below the Critical Threshold’” in Olbrich. Pet., 15 (identifying this value as “capacity metadata”). As Petitioner notes, when this condition occurs in unmodified Olbrich, “a Critical Flag is set and the [device] shifts

into critical garbage collection mode.” Pet., 15 (quoting Ex. 1004 [Olbrich] 80:16-24, 81:22-38). Petitioner implicitly proposes that in its Olbrich combination, the same condition would trigger the claimed “notification . . . that recommends performing maintenance on the specified zone,” in which “host-side software” (Pet., 8) on a modified version of Olbrich’s host would decide when to perform the requested garbage collection on some specified SuperBlock. *See* Pet., 15. There are several problems with this proposal.

73. First, the capacity trigger Petitioner cites is on the level of what Olbrich describes as a “Flash Group”—a division of storage that may be one-eighth or one-twelfth of the entire storage in preferred embodiments, Ex. 1004 [Olbrich] 6:39-44—and Olbrich’s system does not identify any particular SuperBlock (what Petitioner identifies as a “zone” in Olbrich) within a “Flash Group” when this condition occurs. Petitioner does not show how its proposed basis for “making a notification available to the host” would identify a “specified zone” under Petitioner’s reading of the claim. *See, e.g.*, Ex. 1004 [Olbrich] 79:40–80:6.

74. In Olbrich, the cited “Counter value” is its “SuperBlock Freelist Counter”—and when it drops to or below the Critical Threshold the controller sets a Critical Flag (for a given “Flash Group”) and enters critical garbage-collection mode. *See, e.g.*, Ex. 1004 [Olbrich] 79:60-67, 80:16-24. This condition does not itself identify any particular SuperBlock within the group as a target for garbage

collection. In Olbrich's design, only *after* garbage collection is initiated does the controller select a SuperBlock to have its valid data moved elsewhere and be erased. This selection is made by scanning Olbrich's "Reverse Table" and choosing the SuperBlock in the group with the highest invalid-page Count (with some provisions for tie-breaking that are not related to this essential point). *See, e.g., id.*, 81:6-31. In other words, even if we take Petitioner's identification of SuperBlocks with the claimed "zones" for granted for purposes of Petitioner's argument, at the moment the capacity condition is reached, there is no "specified zone" to associate with any "zone start logical block address," and Petitioner does not show where one would come from.

75. In the same paragraph that Petitioner cites for its discussion of "critical" garbage collection, Olbrich states that when its system enters "critical" garbage collection, "garbage collection operations tak[es] precedence over *all other operations*, including Host reads and writes." Ex. 1004 [Olbrich] 80:19-21. Olbrich distinguishes such garbage collection from a mode of operation in which "garbage collection operations are initiated, but only after all Host-initiated reads and writes have been handled." *Id.*, 80:27-29.

76. Because "critical" garbage collection preempts all other operations in Olbrich, a POSITA would not find it obvious to make the controller merely

recommend such garbage collection to the host. Deferring “critical” garbage collection can leave the system unable to service host writes.

77. In one embodiment, for instance, Olbrich sets its “Critical Threshold” at two free SuperBlocks—“at least one free SuperBlock [being] needed at all times[] in order to insure that an incoming write can be accommodated,” and another being needed to service “Transfer Requests” that may be queued when the “Critical Threshold” is reached. Ex. 1004 [Olbrich] 80:32-44. In this example, a host that deferred hypothetical requests to perform “critical” garbage collection would soon find that its write commands cannot be completed. And if the host in this example were configured to avoid this issue by *not* deferring “critical” garbage collection—that is, by prioritizing such requests over everything else—a POSITA would recognize that there is no reason for the controller to involve the host at all in “critical” garbage collection. This is why “critical” garbage collection takes precedence over “all other operations” in the unmodified Olbrich without any notification or recommendation to the host, and why what Petitioner terms “translocating the maintenance command responsibility to host-side software,” Pet., 8, makes no sense in the context of Olbrich’s “critical” garbage collection.

78. Although Petitioner does not expressly argue that Yamada might teach a modification of how Olbrich performs garbage collection on the basis of its

capacity data, Yamada does not teach any involvement of its “maintenance request unit” in initiating garbage collection either.

79. A POSITA would understand that Yamada’s “maintenance request unit” does not send requests to Yamada’s host for garbage collection to occur on particular regions of flash memory. Indeed, although Petitioner regards Yamada as a generalized teaching of “benefits” of “host-initiated maintenance,” Pet., 8, Yamada consistently uses the term “maintenance” in a narrow sense, to refer specifically to operations specific to data retention and wear leveling—not to freeing up unused space, as occurs during garbage collection. *See, e.g.*, Ex. 1005 [Yamada] [0007] (referring to “*processing to retain data*, or maintenance, which can be, for example, data refreshing”), [0030] (referring to “maintenance” that “includes refresh and/or wear leveling”), [0033] (same), cl. 9, 10.

80. Every example that Yamada gives of its “maintenance request unit” sending maintenance requests to its host involves the generation of a request to correct and rewrite previously stored data after errors have been detected (for example, during a read operation). *See, id.*, [0032] (stating that “[t]he error correction unit determines the number of errors included in data read from the nonvolatile memory” and that “[t]he maintenance request unit generates a maintenance request . . . when the number of errors determined by the error correction unit is greater than or equal to a criterion value”), [0081] (similar), [0095]-

[0098] (describing the “Data Maintenance Request Generation Cycle”) (similar), [0187]-[0189] (similar). Yamada does not disclose any request from its “maintenance request unit” to its host that seeks that garbage collection be performed at any specific place.

81. A POSITA would further understand that if garbage collection did occur as a downstream consequence of carrying out Yamada’s exemplary “maintenance requests,” it would occur within Yamada’s controller—that is, without the “maintenance request unit” within Yamada’s controller sending a “maintenance request” to Yamada’s host recommending that garbage collection take place. As one example, Yamada discloses only its controller as having access to logical-to-physical mapping information—and the physical mapping information would be needed to determine when and where there is “garbage” in the form of invalid data in pages to be collected in the first instance. Yamada does not disclose that its host has access to this information.

82. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown how what it identifies as “making a notification available” on the basis of Olbrich’s “capacity” metadata would be present in its Olbrich/Yamada combination.

b) *Petitioner's "Erase Count" Argument Does Not Show The Claimed "Notification."*

83. Petitioner states that Olbrich's SuperBlock-level erase counts provide an alternate example of "metadata" on which the claimed step of "based on the metadata, making a notification available to the host that recommends performing maintenance on the specified zone" might be performed. More specifically, Petitioner argues that

Olbrich teaches that a SuperBlock may be selected for garbage collection based on SuperBlock erase count metadata. Thus, Olbrich teaches SuperBlock maintenance [**performing maintenance on the specified zone**], depending on SuperBlock erase count metadata [**based on the metadata**].

Pet., 14 (bracketed insertions and boldface in original) (citing Ex. 1004 [Olbrich] cls. 1, 24, 92:18-22).

84. This use of brackets to identify disclosures Olbrich with claim language does not mention the claimed "making a notification available to the host," or otherwise identify what "notification" would be made available to the "host" in Petitioner's combined system on the basis of erase counts. These statements also fail to explain how the selection of blocks for garbage collection on the basis of erase count information *during* garbage collection relates (if at all) to the *initiation* of garbage collection in Olbrich. Olbrich discloses only the former, while it is the latter

that Petitioner presumably identifies with the claimed “recommend[ing] performing maintenance on the specified zone.” To repeat the essential point, Petitioner is silent in addressing the difference between doing something during a garbage collection operation that has already been initiated and “recommend[ing]” that garbage collection be performed in the first instance.

85. Olbrich describes that *after* garbage collection has been initiated, erase count information may be used as a tie-breaker for selecting a SuperBlock for garbage collection—when the primary basis of selection of a SuperBlock during garbage collection is the SuperBlock’s amount of “invalid pages.” Olbrich states:

Garbage collection requires the selection of a Super Block for erasure. This is represented in Step 5601. . . . [I]t makes sense to choose SuperBlocks that have the least amount of valid data. Thus, *when garbage collection is initiated*, the relevant Flash HEMi checks the Count Field for each SuperBlock The Flash HEMi selects the SuperBlock with the highest Count Field value, indicating the largest number of invalid SuperPages. If more than one SuperBlock is tied for the highest Count Field, in the currently preferred embodiment, the first such SuperBlock encountered is chosen for garbage collection. *In an alternative embodiment, ties could be broken by checking the Erase Count field* in the SuperBlock Metadata Table . . . for each of the tied SuperBlocks, with the SuperBlock having the lowest Erase Count being selected.

Ex. 1004 [Olbrich] 81:6-31.

86. Here Olbrich describes the use of its SuperBlock “erase count” as a secondary, tie-breaking factor in selecting a block for garbage collection *during* a garbage collection—not the use of its SuperBlock “erase count” to decide whether or when to initiate garbage collection in the first instance.

87. And Olbrich does not disclose using its erase counts to initiate garbage collection in any other part of Olbrich, either. Olbrich describes garbage collection as being initiated by the number of “free” SuperBlocks dropping to or below various numerical thresholds: if the count of “free” SuperBlocks is at or below a “Non-Critical Threshold,” garbage collection is performed “after all Host-initiated reads and writes have been handled,” while if the count of “free superblocks” is at or below a (lower) “Critical Threshold,” garbage collection “tak[es] precedence over all other operations.” Ex. 1004 [Olbrich] 80:16-29. And these are the *only* conditions under which garbage collection is initiated in Olbrich. *See id.*, 80:29-31 (“If the amount of available free space is above the Non-Critical Threshold, garbage collection does not occur.”).

88. When Petitioner says that a “SuperBlock [in Olbrich] may be *selected* for garbage collection based on SuperBlock erase count metadata,” Pet., 14, Petitioner does not show how this information would be used to “mak[e] a notification available to the host that recommends performing [garbage collection] on the specified zone” in its combination.

89. A POSITA would not find it obvious to initiate garbage collection of a SuperBlock in Olbrich on the basis of its erase count. The erase count of a SuperBlock typically has no relation whatsoever to how much space could be freed by using that SuperBlock as a basis for garbage collection. By choosing a SuperBlock on the basis of erase count alone, for example, one might choose a block with no invalid pages at all—resulting in increased wear on the SuperBlock with no benefit whatsoever in freeing space.

90. A POSITA would understand that garbage collection of a SuperBlock results in the SuperBlock being erased, which by definition increases wear on the SuperBlock. Wear can be particularly undesirable for SuperBlocks with high erase counts. Olbrich expressly acknowledges this when it states that in some embodiments, “SuperBlocks with an Erase Count value that exceeds a threshold could be identified so that they are preferentially *not* chosen for normal garbage collection, thereby reducing additional wear on such SuperBlocks.” Ex. 1004 [Olbrich] 92:19-22.

91. Olbrich elsewhere describes the SuperBlocks with erase counts “approach[ing] a danger zone” being desirable targets for valid data that is moved out of blocks selected for garbage collection. *Id.*, 92:8-18. But here the motivation is an expectation that in at least some use cases, valid data in blocks selected for garbage collection may be *less* likely to be invalidated in the future, *id.*; *see also*,

e.g., id., 83:36-39 (stating that in some cases “SuperBlocks used as the repository for garbage collection will probably not themselves be subject to garbage collection”). In particular, this disclosure is not a teaching of Olbrich’s system initiating any garbage collection process on the basis of the erase count of a SuperBlock.

92. Petitioner’s discussion of Yamada does not address the use of any “erase count” information in triggering the claimed “making a notification available to the host,” and thus does not shed any other light on this aspect of Petitioner’s argument.

93. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown how any erase-count-based “making a notification available to the host that recommends performing maintenance on the specified zone” would be present in its combination.

c) *Petitioner’s “Error Count” Argument Does Not Show The Claimed “Notification.”*

94. Petitioner makes reference to “the number of errors determined by the error correction unit” in Yamada, perhaps as an analogy to the kind of alleged “metadata” that might trigger the claimed “making a notification available” in its combined system. *See Pet.*, 15 (identifying this “number of errors” with the claimed “metadata”). Petitioner does not argue that this form of alleged “metadata” in

Yamada is ever generated in its combined system. In an earlier-recited step of “generating metadata based on accessing and maintenance of erase units in the specified zone,” for example, Petitioner identifies only Olbrich as a source of the alleged “metadata,” *see, e.g.*, Pet., 13-14, and the claimed step of “based on the metadata, making a notification available to the host ...” refers back to the earlier-recited step of “generating metadata.”

95. For at least these reasons, in my opinion, Petitioner and Dr. Litz have not shown how error counts in Yamada relate to any alleged teaching of the claimed step of “based on the metadata, making a notification available to the host . . .” in its combined system.

96. In sum, in my opinion, for at least the reasons discussed above, Petitioner and Dr. Litz have not shown how the step of “based on the metadata, making a notification available to the host that recommends performing maintenance on the specified zone” is present in the combined system.

VII. PETITIONER’S GONZALEZ COMBINATIONS

97. I have reviewed Petitioner’s Grounds II-VI, which all involve a combination of Gonzalez, Goss, and NVMe1.0b. Pet., 41-73.

98. I understand that all of the challenges in Petitioner’s Gonzalez grounds (Grounds II-VI) build upon a combination that Petitioner offers in Ground II (Gonzalez/Goss/NVMe1.0b) against claim 1. *See, e.g.*, Pet., 47-48 (referring to each

limitation of claim 1 in Petitioner’s Ground II arguments regarding independent claim 2), 48-51 (incorporating Petitioner’s Ground II arguments as to claim 1 and/or 2 into arguments for dependent claims), 52-55 (same), 56 (same), 59-68 (same), 71-72 (same). Accordingly, I have focused my analysis of Petitioner’s Grounds II-VI on Petitioner’s Ground II argument against claim 1. I reserve the right to supplement my opinions if the Petition is instituted.

99. Petitioner relies on Gonzalez for the “host,” “metadata,” and other elements (Pet., 34-45), but does not argue that Gonzalez teaches the claimed step of “based on the metadata, making a notification available to the host that recommends performing maintenance on [a] specified zone” Pet., 45-46.

100. For this limitation, Petitioner proposes adding Goss’s “controller notification” to Gonzalez’s host and “translocating the maintenance command responsibility to host-side software.” Pet., 42. But Petitioner does not explain how a POSA would have been motivated to arrive at its combination, let alone to do so with a reasonable expectation of success. Petitioner also fails to show that its combination teaches “performing a multi-plane write of said data to erase units on different planes . . . using a common page address for the respective erase units on the different planes.”

A. Petitioner Fails To Show A Motivation To Add Goss’s Host-Notification And Host-Side Maintenance To Gonzalez.

101. As part of arguing that a POSITA would be motivated to combine Gonzalez and Goss in the way proposed by Petitioner, Petitioner argues that Gonzalez contemplates “direct control by the host.” *Id.* (citing Gonzalez’s paragraph 37). But the rationale offered for Petitioner’s combination is generic and not specific to the references. Gonzalez’s paragraph 37 is an aside about systems *without* a controller, and does not motivate the proposed modification to Gonzalez’s controller-centric design. Goss’s disclosures also concern alerts relating to large subdivisions of storage which may include the entire device, and such alerts are not analogous to notifications on the basis of a single metablock, which is what Petitioner identifies as a “zone” in Gonzalez.

1. Gonzalez Does Not Motivate Petitioner’s Proposed Modification.

102. Petitioner argues that a POSITA would “have been motivated to incorporate Goss’s teaching . . . because Gonzalez already teaches that memory management responsibilities may be distributed between the host and controller, i.e., including ‘direct control by the host system.’” Pet., 42 (quoting Ex. 1007 [Gonzalez] [0037]). I do not agree. In particular, this argument is unrelated to the modification Petitioner actually proposes; the cited paragraph 37 of Gonzalez concerns systems *other than* Gonzalez that “do not have a dedicated controller,” and Gonzalez itself

does otherwise not teach reallocating responsibility between its host and its controller in the way proposed by Petitioner.

103. When Petitioner cites Gonzalez’s paragraph 37 for the proposition that Gonzalez teaches “direct control by the host system,” Petitioner does not connect this “direct control by the host system” with any specifics of its proposed modification, which includes adding “[a] notification sent to the host [that] would be premised on metadata describing Gonzalez’s metablocks and the notification would identify the metablock in need of maintenance through, e.g., ‘starting LBA.’” Pet., 46.

104. To belabor the point, Petitioner’s proposed modification involves specific proposed changes to Gonzalez’s controller, and sending specifically proposed information of a specific type to Gonzalez’s (modified) host, but Petitioner does not explain how any presumed general desirability of “direct control by the host system” would motivate these specific changes.

105. Nor does Gonzalez’s paragraph 37 actually “teach[] that memory management responsibilities may be distributed between the host and controller,” Pet., 42 (citing Ex. 1007 [Gonzalez], [0037]), in the way that Petitioner claims.

106. Gonzalez’s paragraph 37 contrasts the system in its Figure 2 (which uses “a single controller integrated circuit chip 121”) with *other* systems that “do not have a dedicated controller, but instead rely on direct control by the host system.”

See Ex. 1007 [Gonzalez], Fig. 2. A POSITA would understand that what Gonzalez here presents as “direct control by the host system” is an alternative approach—an approach that is not “typical,” and an approach used in “memory systems [that] *do not have* a dedicated controller.” *Id.*, [0037]. Gonzalez, by contrast, does have a dedicated controller, and Petitioner expressly relies upon Gonzalez’s controller in identifying other aspects of Gonzalez with aspects of claim 1. See, e.g., Pet., 43 (citing Gonzalez’s Figure 2 in connection with the preamble of claim 1), 45 (arguing that “Gonzalez teaches that ‘programming characteristic[s]’ are ‘monitored and stored by the controller’” in Gonzalez).

2. Goss’s Array-Level, User Prompted Notifications Do Not Motivate A Modification Requiring Host Notifications For A Specified Zone Based On Metadata.

107. Petitioner turns to Goss to for alleged teachings of “*based on the metadata*, making a notification available to the host that recommends performing maintenance *on a specified zone*, wherein the recommendation is associated with the zone start logical block address of the specified zone,” Pet., 45-46, where Petitioner has identified a SuperBlock in Gonzalez as a “zone,” Pet., 42, and where Petitioner has identified the “LBA” associated with the first SuperPage of a SuperBlock in Gonzalez with the claimed “zone start logical block address of the specified zone.” Pet., 45. But Goss does not teach such a zone-identified, metadata-based host notification.

108. Petitioner argues that “Goss teaches the benefits of the controller’s ‘real-time notifications to the host.’” Pet., 42 (citing Ex. 1003 [Litz-Decl.] ¶ 217); Pet., 46 (citing Goss for its alleged teaching of “real-time notifications to the host”) (quoting Ex. 1008 [Goss] [0024]). But Petitioner does not identify any disclosure in Goss of a notification associated with a logical address of a single block, or any group of blocks—the phrase “starting LBA” (Petitioner’s “start logical block address of the specified zone”) appears only in Petitioner’s description of what a POSITA “would understand” (Pet., 46).

109. Goss discloses its “real-time notifications” at an aggregate level that may be the entire device, not on the basis of anything resembling Gonzalez’s “metablocks.” *See, e.g.,* Ex. 1008 [Goss] [0024] (“Self-monitoring routines **can provide real-time notifications** to a host with regard to the status of the array and/or the data, allowing the user to take affirmative steps to alter the operation of **the device** to extend its useful life”); *see also, e.g., id.*, [0085] (referring to “a notification to the host that, without data hardening, the data may be below retention specifications” such that “[i]n this way, a user directed prompt may initiate the routine 240,” where routine 240 is a data maintenance routine iterating across multiple blocks). [0086]-[0088], Fig. 12 & [0090] (referring to a “safe-to-shutdown notification to the host” being provided after data maintenance routine 240 has been carried out “for **all blocks** in the array that have been allocated to store data” and

“redundancy information has been generated for *all of the data*”), [0085] (referring to data maintenance routine 240 as “steps carried out by the controller 102 to assess and improve the reliability of *the array 104*”).

110. Goss’s notifications are thus for collections of blocks that may be an entire device, not for anything resembling “a specified zone” as the claim requires, or a Gonzalez “metablock.” Nor are these notifications “based on metadata” at zone granularity or directed towards performing maintenance on a particular zone. Rather, the “real-time notifications to a host with regard to the status of the array and/or the data *allowing the user* to take affirmative steps to alter the operation of the device to extend its useful life.” Ex. 1008 [Goss] [0024]; *see also id.*, [0070] (“Accordingly, in further embodiments *the user* may be directed to signal this intent to shut down the device for an extended period of time.”), [0085] (referring to “a notification to the host that, without data hardening, the data may be below retention specifications,” so that “[i]n this way, a *user directed prompt* may initiate the routine”).

111. Goss does not teach notifying the host about the wear status of individual blocks or metablocks, nor issuing a host notification based on wear metadata for a particular block or group of blocks. The ‘real-time notifications to a host’ in Goss exist to prompt user interaction about device-level conditions (*e.g.*, initiate or defer device routines), not to target a specific block or group of blocks.

Goss’s own example block (‘256 pages × 8192 bytes’) is ~2 MB (Ex. 1008 [Goss] [0034]), and practical systems at the time stored hundreds or thousands of megabytes. A user could not meaningfully respond to hundreds or thousands of block-specific wear notices. Consistent with that scope, Goss’s wear-leveling passages ([0047]–[0051]) contain no hint of host or user involvement at the individual-block level, and nothing in Goss suggests a host notice tied to metadata at the level of groups of blocks analogous to Gonzalez metablocks—much less identification of those metablocks by what Petitioner refers to as their “start LBA.”

112. In my opinion, for at least these reasons, Petitioner and Dr. Litz fail to demonstrate that a POSITA would have been motivated or able to combine Gonzalez with Goss (and its other references in its other grounds) with a reasonable likelihood of success.

B. Petitioner Does Not Show “performing a multi-plane write of said data to erase units on different planes . . . using a common page address for the respective erase units on the different planes” In Its Gonzalez Combinations.

113. Claim 1 recites, among other things, “in response to a write command from the host to write data to the range of logical block addresses of a specified zone, performing a multi-plane write of said data to erase units on different planes in the specified zone using a common page address for the respective erase units on the different planes” Ex. 1001 [’772], 64:52-57.

114. Regarding this limitation, Petitioner states:

Gonzalez teaches that write commands may be directed to metablocks where “[d]ata are simultaneously programmed to one block of each plane making up a metablock” spanning “a number of consecutively addressed data sectors” [*in response to a write command from the host to write data to the range of logical block addresses of a specified zone, performing a multi-plane write of said data to erase units on different planes in the specified zone*]. EX1007, [0057], [0018]; EX1003, ¶229.

Gonzalez further teaches that “[t]he metablock is identified by *a common logical address as a destination for programming* and reading *data*,” [using a common page address for the respective erase units on the different planes]. EX1007, [0010].

Pet., 44 (bracketed insertions and emphases in original).

115. Here Petitioner does not link Gonzalez’s disclosure of a metablock being “identified by common *logical address* as a destination for programming,” with any alleged multi-plane write “using a common *page address* for the respective erase units on the different planes.”

116. A POSITA would recognize that Gonzalez’s “logical addresses” are not the same thing as Gonzalez’s “page addresses.” Gonzalez states, for example:

The metablock is identified by a common logical address as a destination for programming and reading data. . . . The controller . . . performs a number of functions including the *translation* between

logical block addresses (LBAs) received from a host, and physical block numbers (PBNs) and *page addresses* within the memory cell array. This translation often involves use of intermediate terms of a logical block number (LBN) and logical page.

Ex. 1007 [Gonzalez] [0010].

117. Here, Gonzalez explains that its “logical block addresses” in Gonzalez and “page addresses” in Gonzalez are related to one another via a “translation” process that may involve “intermediate terms” like a “logical block number” and “logical page.” A POSITA would understand the details of any relationship between Gonzalez’s “logical block addresses” and Gonzalez’s “page addresses” to be contained within the details of this “translation” process—but Gonzalez does not discuss any details, and Petitioner does not address the issue.

118. A POSITA would generally understand that it is possible for a system of flash management to perform a multi-plane write *without* using a common page address, and that nothing in Gonzalez forecloses this possibility.

119. Thus, in my opinion, Petitioner fails to show “in response to a write command from the host to write data to the range of logical block addresses of a specified zone, performing a multi-plane write of said data to erase units on different planes in the specified zone using a common page address for the respective erase units on the different planes . . .” in its combination of Gonzalez and Goss.

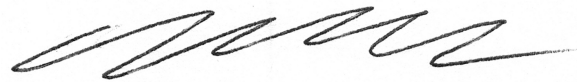
VIII. CONCLUSION

120. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required, I will appear for cross-examination within the United States during the time allotted.

121. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Respectfully submitted,

Dated: October 20, 2025



Dr. Mark Jones

Exhibit A

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**PROFESSIONAL
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Professor Emeritus of Electrical and Computer Engineering, Virginia Tech,
2021-present

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Ph.D., Duke University, Computer Science, May 1990.

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**RECOGNITION
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Virginia Bioinformatics Faculty Fellow
1st prize and Honorable Mention at AOL-CIT Research Day
Virginia Tech College of Engineering Dean's List for Teaching
NSF CAREER Award
University of Tennessee Science Alliance Award
Atanasoff Best Paper Award
Gordon Bell Prize
Von Neumann Fellowship
R. F. Poole Scholarship
National Merit Scholar

**EXPERT
TESTIMONY**

Blackboard v. Desire2Learn
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving Internet-based educational
software employing role-based access control
Testified: Jury trial (infringement and validity), injunction hearing,
contempt hearing, and deposition (4 times)

TechRadium v. Blackboard
United States District Court for the Eastern District of Virginia

United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving network-based emergency notification systems
Testified: Preliminary injunction hearing and deposition

Computer Associates v. Digex
Circuit Court for Prince George's County Maryland
Overview: Contract dispute involving enterprise management systems
Testified: Jury trial and deposition

Computer Associates v. Retired Persons Services
United States District Court for the Eastern District of Virginia
Overview: Contract dispute involving enterprise management systems
Testified: Deposition

DVSI v. University of Phoenix and Walden University
United States District Court for the Eastern District of Virginia
Overview: Patent infringement case involving network-based educational software employing digital rights management
Testified: Deposition (3 days)

VirnetX v. Microsoft
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving VPN software in Microsoft Windows and Microsoft's Unified Communications software
Testified: Jury trial (infringement and validity) and deposition (3 days)

TechRadium v. Twitter
United States District Court for the Southern District of Texas
Overview: Patent infringement case involving network-based notification systems
Testimony: Deposition

Bedrock Computer Tech v. Softlayer et al
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving data structures in the Linux operating system's network stack
Testimony: Jury trial v. Google (infringement and validity), Jury trial v. Yahoo (infringement and validity) and deposition (3 days)

CEATS v. Continental Airlines et al
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving Web-based interactive seat maps
Testimony: Jury trial (infringement and validity) and deposition (2 days)

VirnetX v. Cisco et al
United States District Court for the Eastern District of Texas
Overview: Patent infringement case involving secure communications, VPNs, and Voice-over-IP
Testimony: Jury trial v. Apple (infringement and validity), Jury trial v. Cisco (validity), and deposition (3 days), 2nd jury trial v. Apple (infringement), 3rd jury trial v. Apple (infringement), 4th jury trial v. Apple (infringement), 5th jury trial v. Apple

Summit6 v. Research In Motion et al
United States District Court for the Northern District of Texas

Overview: Patent infringement case involving network-based photo uploading tools on smartphones and web browsers

Testimony: Jury trial v. Samsung (infringement and validity) and deposition (3 days)

Ericsson v. Samsung

International Trade Commission

Overview: Patent infringement case involving Java technology and touchscreen technology on smartphones

Testimony: Deposition

AT Engine Controls LTD. v. Goodrich Corp and Goodrich Pump & Engine Control Systems, Inc.

United States District Court for the District of Connecticut

Overview: Trade secret case involving an embedded computing system design for helicopter engine control

Testimony: Deposition

SmartFlash LLC. v. Apple, et. al.

SmartFlash LLC. v. Samsung, et. al.

United States District Court for the Eastern District of Texas

Overview: Patent infringement case involving digital rights management and content distribution

Testimony: Jury trial v. Apple (infringement and validity) and deposition (4 days)

Unwired Planet v. Apple

United States District Court for the Northern District of California

Overview: Patent infringement case involving several technologies related to mobile devices

Testimony: Deposition (3 days); technology tutorial presentation to the Court

Facebook v. Rembrandt Social Media

Patent Trial and Appeal Board

Overview: Validity of a patent in the area of a web-based diary system

Testimony: Deposition

Motorola Mobility v. Intellectual Ventures

Patent Trial and Appeal Board

Overview: Validity of a patent in the area transmitting and browsing preformatted information

Testimony: Deposition

Summit6 v. Apple et al

United States District Court for the Northern District of Texas

Overview: Patent infringement case involving network-based photo uploading tools on smartphones and web browsers

Testimony: Deposition

EMC v. Pure Storage et al

United States District Court for the District of Delaware

Overview: Patent infringement case involving memory systems

Testimony: Deposition and jury trial (infringement and validity)

Parallel Networks v. IBM

United States District Court for the District of Delaware

Overview: Patent infringement case involving web servers and load balancing
Testimony: Deposition (2 days)

Parallel Networks v. Microsoft

United States District Court for the District of Delaware

Overview: Patent infringement case involving web servers and load balancing
Testimony: Deposition (2 days) and jury trial (infringement and validity)

Microsoft and IBM v. Parallel Networks

Patent Trial and Appeal Board

Overview: Validity of a patent related to web servers and load balancing
Testimony: Deposition

adidas v. Under Armour

United States District Court for the District of Delaware

Overview: Patent infringement case involving fitness tracking
Testimony: Deposition

BMC Software v. ServiceNow

United States District Court for the Eastern District of Texas

Overview: Patent infringement case involving enterprise management software
Testimony: Deposition

Ericsson v. TCL

United States District Court for the Eastern District of Texas

Overview: Patent infringement case involving Java technology and security on smartphones

Testimony: Deposition (3 days) and jury trial (infringement)

REM v. Square

United States District Court for the Eastern District of Missouri

Overview: Intellectual property case involving credit card readers for smartphones

Testimony: Deposition

AARC v. Chrysler et al

United States District Court for the District of Columbia

Overview: Intellectual property case involving car infotainment systems
Testimony: Deposition

Spex Technologies v. Apricorn

United States District Court for the Central District of California

Overview: Patent infringement case involving secure memory devices
Testimony: Deposition, Jury trial

United States Conference of Mayors v. Great-West Life Annuity Insurance Co.

United States District Court for the District of Columbia

Overview: Contract dispute
Testimony: Deposition and jury trial

Tecsec, Inc. v. Adobe Systems Inc. and Oracle (listed as IBM, et.al.).

United States District Court for the Eastern District of Virginia

Overview: Patent infringement case involving secure object technology
Testimony: Adobe: Deposition and jury trial (infringement and validity); Oracle (deposition)

Egenera, Inc. v. Cisco Systems, Inc.

United States District Court for the District of Massachusetts

Overview: Patent infringement case involving an architecture for a processing platform

Testimony: Deposition, bench trial, and jury trial

Unified Patents v. Sound View Innovations

Patent Trial and Appeal Board

Overview: Validity of a patent related to concurrency control

Testimony: Deposition

Hulu v. Sound View Innovations

Patent Trial and Appeal Board

Overview: Validity of a patent related to concurrency control

Testimony: Deposition

Grace and Potter. v. Apple Inc.

United States District Court for the Northern District of California

Overview: Class action case involving FaceTime

Testimony: Deposition

HTC v. Ericsson

United States District Court for the Eastern District of Texas

Overview: Patent licensing related to cellular standards

Testimony: Deposition

Windy City.Innovations v. FaceBook, Inc..

United States District Court for the Northern District of California

Overview: Patent infringement case involving an architecture for a messaging platform

Testimony: Deposition

Hulu v. Sound View Innovations

Patent Trial and Appeal Board

Overview: Validity of a patent related to real time systems

Testimony: Deposition

Citrix Systems, Inc. v. Avi Networks, Inc..

United States District Court for the District of Delaware

Overview: Patent infringement case involving network devices

Testimony: Deposition

Rovi v. Comcast

International Trade Commission

Overview: Patent infringement case set top boxes

Testimony: Deposition, Trial

Seven Networks v. Apple

United States District Court for the Eastern District of Texas

Overview: Patents related to mobile device push-based communication

Testimony: Deposition

Match Group, LLC v. Bumble Trading Inc.

United States District Court for the Western District of Texas

Overview: Patents related to online dating apps

Testimony: Deposition

SAS Institute Inc. v. World Programming Limited, et. al.
United States District Court for the Eastern District of Texas
Overview: Copyright and patents related to statistical software
Testimony: Deposition, Bench trial

Allscripts Healthcare, LLC v. Decision Resources Group,
United States District Court for the District of Massachusetts
Overview: Contract dispute
Testimony: Deposition, jury trial

Clear Imaging v. Samsung
United States District Court for the Eastern District of Texas
Overview: Patents related to image processing
Testimony: Deposition

Nokia v. Lenovo
International Trade Commission
Overview: Patents related to video encoding
Testimony: Deposition

Dish Network v. Sound View Innovations
Patent Trial and Appeal Board
Overview: Validity of a patent related to scheduling for QoS
Testimony: Deposition

Dish Network v. Sound View Innovations
Patent Trial and Appeal Board
Overview: Validity of a patent related real-time multimedia applications
Testimony: Deposition

RFCyber v. Samsung
United States District Court for the Eastern District of Texas
Overview: Patents related to secure payment systems
Testimony: Deposition

RightQuestion LLC v. Samsung
United States District Court for the Eastern District of Texas
Overview: Patents related to hardware-based authentication
Testimony: Deposition

Daedalus Blue, LLC v. MicroStrategy Inc.
United States District Court for the Eastern District of Virginia, Norfolk
Division
Overview: Patent infringement case involving business intelligence software
Testimony: Deposition

Seven Networks v. Motorola Mobility LLC,
United States District Court for the Eastern District of Texas
Overview: Patents related to mobile device communication methods
Testimony: Deposition

HID Global Corp. v. Vector Flow Inc. and Ajay Jain, Vikrant Ghai, and
Shailendra Sharma
United States District Court for the District of Delaware
Overview: Patents related to security monitoring

Testimony: Deposition and Trial

YouToo Technologies, LLC, v. Twitter, Inc.

United States District Court for the Northern District of Texas Dallas Division

Overview: Patents related to video

Testimony: Deposition (2 days) and jury trial

Constellation Designs, LLC v. LG Electronics, Inc., LG Electronics USA, Inc.,
and LG Electronics Alabama, Inc.

U.S. District Court, Eastern District of Texas, Marshall Division

Overview: Patents related to digital communication systems

Testimony: Deposition and Trial

Ryan Hardin, et al. v. Samsung Electronics Co., LTD., et al.

U.S. District Court, Eastern District of Texas, Marshall Division.

Overview: Patents related to geofencing

Testimony: Deposition

Xerox, ACS Transport Solutions, Conduent and New Jersey Transit v.

Bytemark, Inc.

Patent Trial and Appeal Board

Overview: Validity of a patent related to mobile ticketing

Testimony: Deposition

Motista LLC v. Ernst and Young LLP

Arbitration Proceedings

Overview: Matters related to trade secrets

Testimony: Hearing

Inovalon v. Komodo Health

Arbitration Proceedings

Overview: Matters related to trade secrets and breach of contract

Testimony: Hearing

Alacritech, Inc. v. Dell Inc. et al

U.S. District Court, Eastern District of Texas, Marshall Division

Overview: Patents related to network interface devices

Testimony: Deposition

RFCyber v. Apple

United States District Court for the Western District of Texas

Overview: Patents related to secure payment systems

Testimony: Deposition

K. Mizra LLC v. Hewlett Packard Enterprise Co and Aruba Networks LLC

U.S. District Court, Eastern District of Texas, Marshall Division

Overview: Patents related to network security

Testimony: Deposition

Carbyne v. Apple

United States District Court for the Western District of Texas

Overview: Patents related to hardware-based authentication

Testimony: Deposition

Radian Memory Systems LLC, v. Samsung Electronics Co., LTD., et al.

U.S. District Court, Eastern District of Texas, Marshall Division.

Overview: Patents related to flash memory controllers

Testimony: Deposition

Leo Riot, et al. v. Apex Trader Funding Inc., et al.

United States District Court for the Western District of Texas, Austin Division.

Overview: Matters related to trade secrets, copyrights, and breach of contract

Testimony: Deposition

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Tom Canfield, Mark Jones, Paul Plassmann, and Michael Tang, "Thermal Effects on the Frequency Response of Piezoelectric Crystals," *New Methods in Transient Analysis*, Eds. P. Smolinski, W. K. Liu, G. Hulbert, and K. Tamma, PVP-Vol. 246 and AMD-Vol. 143, pp. 103-108, ASME, New York, 1992.

Mark Jones and Paul Plassmann, "The Effect of Many Color Orderings on the Convergence of Iterative Methods," *Proceedings of the Copper Mountain Conference on Iterative Methods*, April 1992.

Mark Jones and Paul Plassmann, "Modeling piezoelectric crystals on the Intel DELTA," *Proceedings of the Intel DELTA Applications Workshop*, Cal Tech, pp. 97-105, 1992.

RESEARCH GRANTS NASA, "Phase II: Integrated Sensors for the Evaluation of Structural Integrity of Inflatable Habitats," with NanoSonic, \$180,000, 9/25/17-9/24/19.

NSF, "SCH: INT: Collaborative Research: Smart Wearable Systems to Support and Measure Movement in Children With and Without Mobility Impairments," \$326,658, 10/1/17-9/30/21.

NASA, "Integrated Sensors for the Evaluation of Structural Integrity of Inflatable Habitats," with NanoSonic, \$35,000, 9/1/2016-8/31/17.

NSF, "SHB: Small: Collaborative Research: Electronic textiles for ambulatory health monitoring," \$306,083, 7/1/2011-6/30/2014.

DARPA, "RECE," With BBN, \$30,000, 4/16/09-10/16/09.

NSF, "Investigating a Novel Embedded Processor Architecture for Electronic Textiles in Wearable and Pervasive Computing," \$220,000, 12/1/08-11/30/10.

NSF, "Fundamental Algorithms to Enable the Simulation of Multi-Scale Biological Systems," \$200,000, 9/1/07-8/31/10.

AFRL, "Phase II: Amorphous Soft-Core Processor for Hardware Anti-Tamper," ~\$230,000, 11/1/06-10/31/08.

Intel, "E-Textile Rug for Gait Analysis, People Tracking and Emergency Directions," \$15,000, 6/1/06-12/31/06.

Carilion, "Quantitative Measurement and Modeling of Early Events in Influenza Pathogenesis," \$20,000, 7/1/05-6/30/06.

AFRL, "Phase I: Wearable Computer for Enhanced Situation Awareness," \$30,000, 5/1/06-1/1/07.

AFRL, "Phase I: Amorphous Soft-Core Processor for Hardware Anti-Tamper," \$35,000, 1/1/06-11/1/06.

MDA, "Phase I: Secure Software Platform for Real-Time Software Anti-Tamper," \$29,994, 6/1/06-11/1/06.

National Science Foundation (NSF), "CRI", (e-textiles equipment), ~\$80,000, 8/05-7/07.

Harris Corporation, "Exploiting the Reconfigurability of a Software-Defined Radio Platform," \$161,070, 9/1/05-6/30/06.

DARPA, "Phase I: Technology for Trusted Circuits," \$31,000, 3/1/05-9/15/05.

Harris Corporation, "Partial Reconfiguration Support for the Harris Programmable Modem Platform," \$73,448, 12/01/04-6/30/05.

NSF, "Phase I: An Electronic Textile System for Gait Analysis", \$33,000, 1/1/2005-6/30/2005.

Office of Naval Research (ONR). "AWINN." \$452,300, 12/20/04-7/31/06.

Office of Secretary of Defense, "Phase II: Reconfigurable Processor Technology for Software Protection," SBIR Subcontract with Luna Innovations, \$237,581, 6/04-5/06.

NSF, REU Supplement to ITR: Tailor-Made: Design of e-Textile Architectures for Wearable Computing, NSF, \$12,000, 6/1/2005 – 8/31/2005.

Office of Secretary of Defense, "Phase I: Reconfigurable Processor Technology for Software Protection," SBIR Subcontract with Luna Innovations, \$33,000, 8/03-2/04.

National Science Foundation (NSF), "ITR: Tailor-Made: Design of e-Textile Architectures for Wearable Computing", \$399,000, 8/02-8/06.

NSF, REU Supplement to above grant, \$10,000.

NSF, REU Supplement to above grant, \$6,000.

NSF, "A Toolbox of Scalable Algorithms and Software for Advanced Scientific Computing Applications", \$300,000, 4/03-4/06.

Defense Advanced Research Projects Agency (DARPA). Computational Fabrics, \$217,000, 3/01-12/02. Subcontract from ISI/University of Southern California.

Office of Naval Research (ONR). Secure Configurable Radio. \$751,000, 4/00-4/04.

NSF, SUCCEED, \$33,000, 9/1/01-8/31/02.

National Science Foundation (NSF). Parallel unstructured mesh algorithms, Amount: \$145,023, 10/99-9/02.

DARPA, Development of algorithms and software for the control of distributed, dynamic sensor networks, Amount \$411,625, 6/99-6/02.

DARPA, Subcontract with USC/ISI. Development of algorithms and runtime software for systems of configurable computers, Amount \$160,000, 10/00-10/01.

Department of Energy, Development of algorithms and software for massively parallel architectures, Amount: \$145,000, 12/98-11/01.

DARPA, Development of Java-based tools and applications for fast, flexible run-time reconfiguration of configurable computing devices, Amount: \$345,574, 9/99-9/01.

DARPA, Development of an application programming interface, algorithms, and applications for run-time reconfiguration on novel adaptive computing architectures, Amount: \$250,000, 6/99-6/01.

Lockheed-Martin/Sanders, A Wireless Link for Remote Telemetry of Compact Airborne System, \$125,000, 5/00-4/01.

DARPA, Development of algorithms and runtime software for systems of configurable computers, Amount \$169,792, 11/99-10/00.

National Security Agency (NSA), Software for the translation of JBits FPGA programs to EDIF programs, Amount \$75,000, 9/99-7/00.

DARPA, Construction of an API & applications for the control of distributed systems of configurable computing nodes, Amount \$162,886, 9/98-10/99.

NSF, Career Award: Parallel algorithms and software for unstructured mesh computations, Amount: \$125,881, 7/96-7/99.

Air Force Research Laboratory, Research and development of an Internet-based, interactive, decision making program, Amount: \$97,425, 11/97-5/99.

NSF, Equipment funding for a 16-node cluster of configurable computers, Amount: \$85,000, 12/97-12/98.

NSF, Scientific applications in a distributed computing environment, Amount: \$318,807, 7/95-7/98.

NSF, Equipment funding for an ATM-based cluster of workstations, Amount, \$100,000, 1/96-12/96.

NSF, Workshop organized at Argonne National Laboratory, Amount, \$10,000, 1996.

PATENTS

Inventor, United States Patent No. 8,473,754, Hardware-Facilitated Secure Software Execution Environment.

SOFTWARE

SLAAC/ACS API (4/99): Software for the control of complex systems of configurable computing nodes and high-speed networks. This code has been distributed to the ACS community. Developed in Configurable Computing Laboratory with Peter Athanas.

BlockSolve (4/93 & 1/96): Software for solving large sparse linear systems on distributed memory architectures. This code has been distributed via netlib and ANL ftp and has been accessed by several hundred people as of 4/4/99. Developed at Argonne National Laboratory with Paul Plassmann.

LANZ (10/90): Software for solving the generalized eigenproblem on shared memory architectures. This code has been distributed via netlib and NASA and has been accessed by over 10,000 people as of 4/4/99. Developed at Duke University and Argonne National Laboratory with Merrell Patrick.

TEACHING

Computer Programming

RESPONSIBILITIES

ECE 5574, *Advanced Software Development for CAE*
ECE 4574, *Large-Scale Software Development for Engineering Systems*
ECE 3574, *Applied Software Design*
ECE 2574, *Data Structures*
ECE 1574, *Engineering Problem Solving with C++*
Computer Simulation and Modeling
CS 371, *Numerical Analysis*
CS 594, *Computational Modeling*
Computer Network, Architecture, and Organization
ECE 2504, *Introduction to Computer Engineering*
CS 594, *Internetworking with TCP/IP*
ECE 4504, *Computer Organization*
ECE 4534, *Design of Embedded Systems*
ECE 5504 (formerly ECE 5515), *Computer and Network Architectures*
ECE Special Studies: *Configurable Computing*, E-Textiles
ECE 5984, *Java-Based Configurable Computing*
ECE 6504, *Applications of Parallel and Distributed Computing*, TV course.
CS 530, *Computer Systems Organization*
CEO of DISC, a student-run virtual corporation, for Fall 1998 and Spring 1999.
