

UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.

Petitioner

v.

BISHOP DISPLAY TECH LLC

Patent Owner

Case No. IPR2025-01330

Patent No. 7,995,047

PETITION FOR *INTER PARTES* REVIEW

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EXHIBIT LIST

Ex.	Description of Documents
1001	U.S. Patent No. 7,995,047 (“’047”)
1002	File History of U.S. Patent No. 7,995,047 (“’047FH”)
1003	Declaration of Dr. Alex Kattamis in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,995,047 (“Kattamis”)
1004	U.S. Patent Pub. No. 2006/0170629 (“Baek”)
1005	U.S. Patent Pub. No. 2005/0231241 (“Date”)
1006	International Patent Pub. No. WO2006/080260 (“Inomoto”)
1007	U.S. Patent Pub. No. 2005/0017765 (“Sasaki”)
1008	Docket Control Order, <i>Bishop Display Tech LLC v. BOE Technology Group Co., Ltd.</i> , No. 2:25-CV-00310-JRG (E.D. Tex. Jul. 23, 2025)
1009	John A. Camara, ELECTRICAL ENGINEERING REFERENCE MANUAL FOR THE ELECTRICAL AND COMPUTER PE EXAM, 6th ed. (Professional Publications, Inc.: 2002), ISBN: 1-888577-56-8 (“Camara”)
1010	Willem den Boer, ACTIVE MATRIX LIQUID CRYSTAL DISPLAYS, 1st ed. (Newnes: 2005), ISBN: 0-750678-13-5 (“den Boer”)
1011	M.K. Han, “AM backplane for AMOLED,” Proc. Of ASID 6 (Oct. 8-12, 2006): 53-58 (“Han”)
1012	U.S. Patent Pub. No. 2006/0227091 (“Nohtomi”)
1013	U.S. Patent Pub. No. 2006/0255787 (“Schaffer”)
1014	U.S. Patent Pub. No. 2003/0025120 (“Chang”)

Other than the prosecution history, Ex. 1002, all citations to exhibits reference original page numbers found in the underlying document. Unless noted, all emphases are added.

LIST OF CHALLENGED CLAIMS

Claim Element	Claim Language from '047 Patent
1(pre)	1. A current driving device, comprising:
1(a)	a first voltage supply source for supplying a first voltage;
1(b)	a first current supply source for supplying a first electric current;
1(c)	a plurality of output terminals; and
1(d)(1)	a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising
1(d)(2)	a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein:
1(e)	each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,
1(f)	under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit, and
1(g)	under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and
1(h)	under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit.

Claim Element	Claim Language from '047 Patent
2	2. The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits, and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common.
3	3. The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode.
4	4. The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode.
5	5. The current driving device according to claim 1, further comprising: a second current supply source for supplying a second electric current that is proportional to said first electric current; and a second current-voltage converting circuit for generating said first voltage by receiving said second electric current, wherein said first voltage supply source controls supplies of said first voltage generated by said second current-voltage converting circuit to said current output circuits.
6	6. The current driving device according to claim 5, wherein said second current-voltage converting circuit comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node.
7	7. The current driving device according to claim 1, further comprising a second voltage supply source with a larger voltage supply capacity than that of said first voltage supply source, wherein the use of said first voltage supply source and the use of said second voltage supply source are switched in accordance with the number of

Claim Element	Claim Language from '047 Patent
	said current output circuits that operate in said voltage supply mode among said plurality of current output circuits.
8	8. The current driving device according to claim 1, wherein said first voltage supply source is configured to change its voltage supply capacity in accordance with the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits.
9	9. A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device.
10(pre)	10. A current driving device, comprising:
10(a)	a current input switch for controlling connection/disconnection states with respect to a current supply source;
10(b)	a voltage holding circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;
10(c)	a calibration switch interposed between said current input switch and said voltage holding circuit;
10(d)	a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding circuit;
10(e)	a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being connected in series to a corresponding one of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;
10(f)	a connection node provided between said current input switch and said calibration switch;

Claim Element	Claim Language from '047 Patent
10(g)	a plurality of current output switches, each being interposed between the connection node and said plurality of current output terminals; and
10(h)	a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit.

Pursuant to §§311-319 and §42.1,¹ BOE Technology Group Co., Ltd. (“Petitioner”) petitions for *inter partes* review (“IPR”) of claims 1-10 (“Claims”) of U.S. Patent No. 7,995,047 (Ex. 1001, “’047”), assigned to Bishop Display Tech LLC (“PO”). There is a reasonable likelihood—and it is highly likely—that at least one challenged claim is unpatentable as explained herein. Petitioner requests review of the Claims and judgment finding them unpatentable under §103.

I. INTRODUCTION

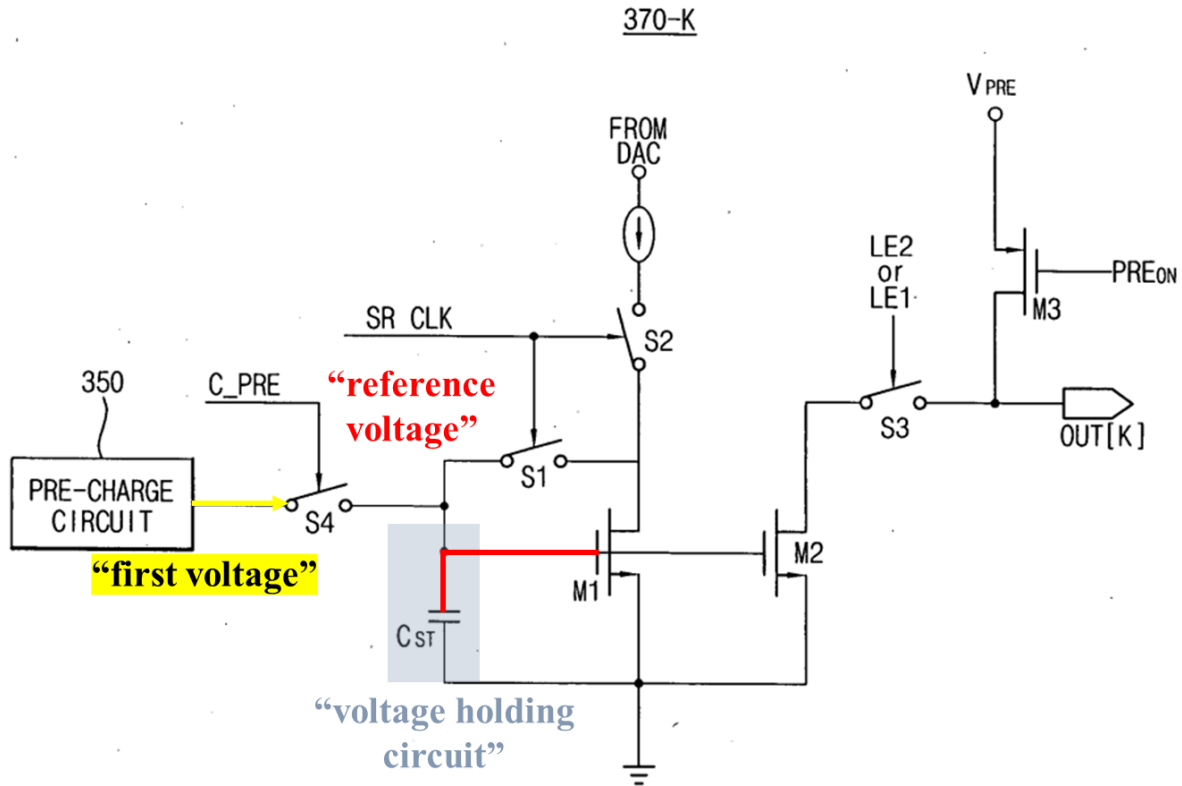
Claim 1 of the ’047 is generally directed to a current driving device that operates in three modes, including a voltage supply mode whereby a voltage holding circuit is charged by a connected voltage source, a current supply mode whereby the voltage holding circuit is charged by a current supplied to a transistor, and a current output mode whereby current is output to a terminal based on the voltage stored in the voltage holding circuit. ’047, cl. 1. Claim 1 was allowed after the claims were amended, whereby the Examiner found the prior art did not disclose “a **voltage holding circuit** having a terminal being connected to a **reference voltage** different

¹ Section cites reference 35 U.S.C. (pre-AIA) or 37 C.F.R. as context indicates. All emphasis/annotations added unless noted. Figure annotations herein generally quote the Claims for reference. Citations herein are exemplary and not meant to be limiting.

from the **first voltage**” and “under said voltage supply mode...the **first voltage** is supplied to another terminal of said **voltage holding circuit.**” ’047 File History (“’047FH, Ex. 1002), 148; Kattamis, ¶¶32-40.

But these concepts were not new. **Baek** discloses a pre-charge circuit 350 that, during a pre-charge mode when switch S4 is “turned on,” supplies a “**pre-charge...voltage**” to “**storage capacitor CST,**” which is connected to the ground terminal and “the gate of the first transistor M1.” Baek, [0052], [0056]-[0058], [0062]. During a current charge mode when switch S4 is turned off, the capacitor CST is charged such that it generates a **reference voltage** at its terminal connected to the transistor M1 that is different from the **pre-charge...voltage.** Baek, [0062]. Kattamis, ¶¶63-67, 90.

FIG. 5



Baek, Fig. 5.

Accordingly, for the reasons further explained below, Petitioner requests that the Board institute trial and find the Claims unpatentable.

II. MANDATORY NOTICES

A. Real Party-In-Interest

Petitioner BOE Technology Group Co., Ltd. is the real party-in-interest. No other parties had access to or control over the present Petition, and no other party funded or participated in preparation of the present Petition.

B. Related Matters

The '047 is the subject of the following co-pending civil action: *Bishop Display Tech LLC v. BOE Tech. Grp. Co., Ltd.*, No. 2:25-cv-00310-JRG (E.D. Tex.) (“Texas Litigation”).

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Petitioner consents to electronic service of documents to the email addresses identified above.

III. PAYMENT OF FEES

The undersigned authorizes the Office to charge the fee required by §42.15(a) and any additional fees that might be due to Deposit Account No. 18-1945, under Order No. 120330-0001-651.

IV. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Pursuant to §42.104(a), Petitioner certifies that the '047 is available for IPR. Petitioner and any real parties-in-interest are not barred or estopped from requesting IPR challenging the Claims on the Grounds identified herein.

B. Identification of Challenge

Pursuant to §§42.104(b)-(b)(1), Petitioner requests IPR of Claims 1-10, and that the Board cancel the same as unpatentable.

a. Specific Art on Which the Challenge is Based

Petitioner relies on the following prior art (Kattamis, ¶16):

Name	Ex.	Publication/Title	Filed	Published/ Issued	Prior art under at least
Baek	1004	US20060170629	1/27/2006	8/3/2006	§102(b)
Date	1005	US20050231241	4/4/2005	10/20/2005	§102(b)
Inomoto	1006	WO2006080260	1/16/2006	8/3/2006	§102(b)
Sasaki	1007	US20050017765	7/14/2004	1/27/2005	§102(b)

Each of **Baek**, **Date**, **Inomoto** and **Sasaki** was published at least one year before the earliest possible claimed priority date of the '047 of 12/12/2007 (US filing date), and therefore qualifies as prior art under §102(b).

b. Statutory Grounds on Which the Challenge Is Based²

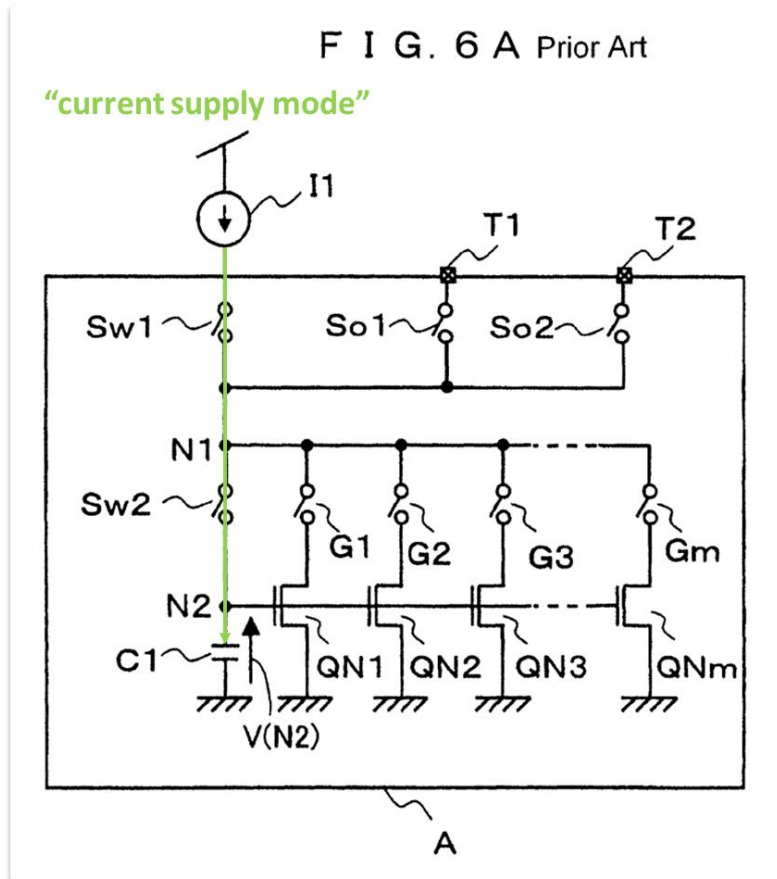
Ground	Claims	Basis	References
1-2	1-4 and 9	§102/§103	Baek
3	5-6	§103	Baek in view of Date
4	7-8	§103	Baek in view of Inomoto
5	10	§103	Sasaki

V. '047 PATENT AND PROSECUTION HISTORY

A. '047

The purported “invention” of the '047 relates to a “current driving device” that operates in three modes, including a mode that “charge[s] the voltage holding part” of the device “to a prescribed voltage at a higher speed.” '047, 3:49-4:3. The '047 discloses a known current driving device that operates in two modes, including “a calibration mode” and a “current output mode.” '047, 1:40-2:7. Under the known calibration mode, the device’s “voltage holding capacitance element C1 is charged” to “store the reference current generated by the reference current source I1.” '047, 1:40-59, Fig. 6A; Kattamis, ¶34.

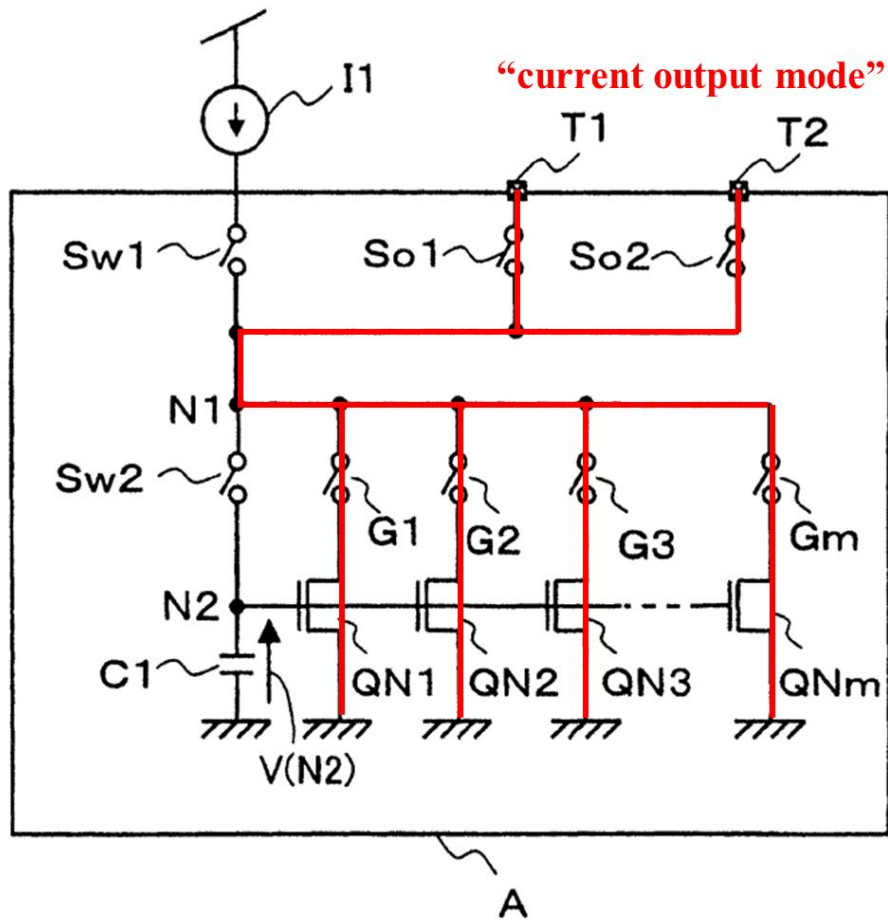
² See Kattamis, ¶¶63-226.



'047, Fig. 6A.

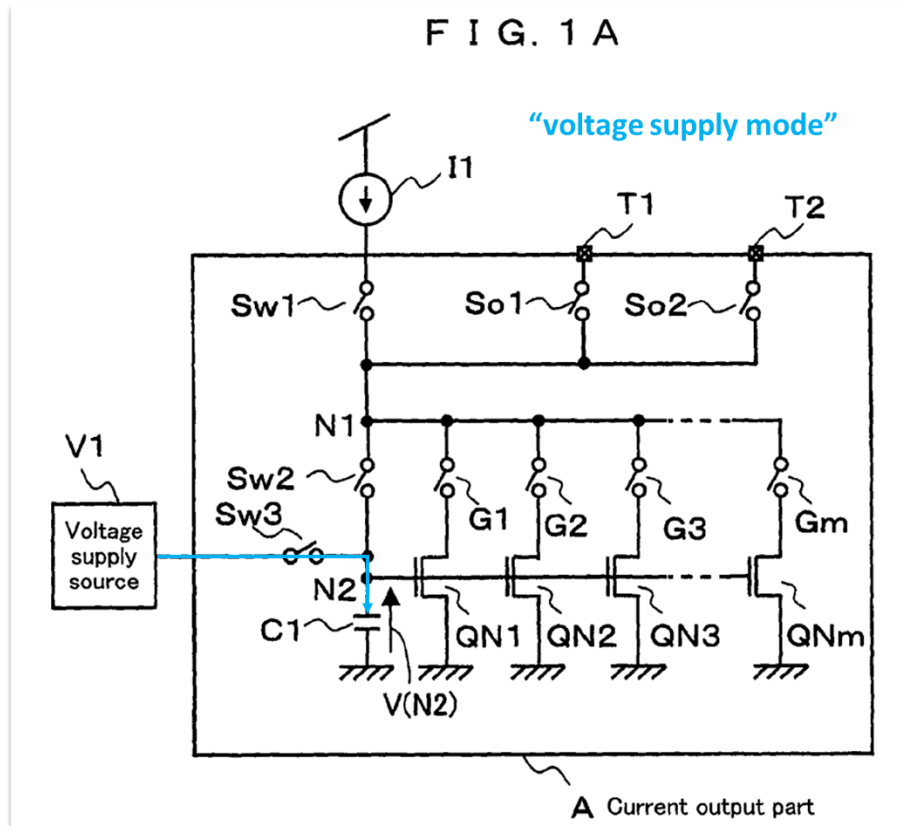
Under the known current output mode, the device's "voltage holding capacitance element $C1$ holds the voltage charged by the calibration action" and the "Nch transistors $QN1$ - QNm output an electric current" from "current output terminals." '047, 1:60-2:7, Fig. 6A; Kattamis, ¶35.

F I G. 6 A Prior Art



'047, Fig. 6A.

The alleged invention of the '047 relates to a third "voltage supply mode," whereby "the voltage holding capacitance element $C1$ is charged to a constant voltage...supplied from the voltage supply source $V1$." '047, 7:44-52, Fig. 1A; Kattamis, ¶36.



'047, Fig. 1A.

B. Prosecution History

The '047 was filed on Dec. 12, 2007 as Application No. 11/954,659 and claims priority to a foreign application filed Dec. 13, 2006. The USPTO examiner issued a rejection requiring the Applicant to designate figures 6A, 6B, and 7-9 as prior art since "only that which is old is illustrated." '047FH, 105. The Examiner further issued two rejections of claims 1-10 under §102 as being anticipated by Date et al. (U.S. Pat. No. 7,466,166) and by Hashido et al. (U.S. Pat. No. 7,221,349). '047FH, 105-115; Kattamis, ¶38.

To overcome these rejections, applicants amended independent claim 1 to specify the voltage holding circuit “having a terminal being connected to a reference voltage different from the first voltage” and claim 10 to specify the “voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage” and to add a “connection node provided between said current input switch and said calibration switch.” ’047FH, 126-130; Kattamis, ¶39.

The claims were subsequently allowed, and the Examiner indicated that the prior art did not teach the following limitations of claim 1: “a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage” and “under said voltage supply mode...the first voltage is supplied to another terminal of said voltage holding circuit.” ’047FH, 148. The Examiner indicated that the prior art did not teach the following limitations of claim 10: “voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage” and “a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit.” ’047FH, 148. As discussed below, the asserted references disclose these and the other claim limitations. Kattamis, ¶40.

VI. §325(D) AND §314(A) DISCRETION DOES NOT APPLY

A. §325(d)

Under the two-part *Advanced Bionics* framework, the Board should not exercise discretion.

The Grounds raised by this Petition are not the same or substantially the same as the art or arguments raised during '047's prosecution. Baek, Inomoto, and Sasaki were not considered during prosecution. These references' disclosures of, e.g., 1(a)-1(h) are not substantially similar to those the Examiner considered. See §IX. While **Date** was used in a rejection of the claims, it was not presented in view of the other asserted prior art in this Petition, and it is used here only in Ground 3 related to dependent claims 5-6. Thus, even considering **Date**, the prior art considered during prosecution is not substantially the same as any of the references in the Grounds of this Petition. This petition raises the same prior art that was raised in the petition in *Samsung Elecs. Co., Ltd. v. Bishop Display Tech LLC*, IPR2022-00501, that challenged '047 claims 1-4 and 9-10, but was settled prior to an institution decision. *Samsung Elecs. Co. v. Bishop Display Tech LLC*, IPR2022-00501, Pap. 7 (P.T.A.B. June 1, 2022). Kattamis, ¶¶38-40.

Even if the art or arguments were substantially the same, the Examiner erred in a manner material to the patentability of the Claims. Because the Examiner “did not expressly consider” **Baek, Inomoto, and Sasaki** as prior art, “[i]t is...difficult, if not impossible, to discern exactly why the Examiner allowed the claims of the ['047] patent, or how the Examiner might have considered

the arguments presented in the Petition, had they been presented to the Examiner.” *Bowtech, Inc. v. MCP IP, LLP*, IPR2019-00379, Pap. 14, *19-20 (declining to exercise §325(d) discretion where Petitioner did not “even attempt[] to explain how the Examiner erred in any way”); *see* §IX.

B. §314(a)

The co-pending Texas Litigation also does not warrant the exercise of discretion under §314(a).

Factor 1 weighs in favor of institution. Petitioner intends to seek a stay of the Texas Litigation pending the outcome of this IPR or in the alternative to bifurcate out this patent from the proceedings and stay that litigation.

Factor 2 weighs in favor of institution, as a trial date is currently scheduled for January 11, 2027, and there will likely be a final written decision rendered around the same time. Ex. 1008, 1.

Factor 3 weighs in favor of institution, as the court and the parties have expended minimal investment in the Texas Litigation. The court has only set a case schedule, and the parties have not exchanged any documents or contentions thus far.

Factor 4 weighs strongly in favor of institution. Upon institution of this IPR proceeding, Petitioner stipulates that it will not pursue in the Texas Litigation the grounds of invalidity asserted in the IPR, or any other ground that was raised or could have reasonably been raised in the IPR with respect to the Challenged Claims.

Factor 5 is neutral or weighs at most only slightly against institution. While Petitioner and PO are the same parties in the Texas Litigation, institution and a public trial record of the important invalidity grounds in the Petition will reduce issues for the public, including all parties besides Petitioner who currently are or may in the future be subject to litigation involving the '047.

Factor 6 weighs strongly in favor of institution. The Petition is strong and presents compelling unpatentability arguments that were overlooked during prosecution. *See* §IX.A-D.

Accordingly, the Board should not exercise its discretion to deny institution. §314(a).

VII. LEVEL OF ORDINARY SKILL IN THE ART

A. Level of Skill in the Art

For purposes of this Petition only, Petitioner assumes the Claims are entitled to the '047's 12/12/2007 US filing date. Kattamis, ¶33.

A person of ordinary skill in the art ("POSITA") would have undergraduate degree in electrical engineering (or equivalent subject) together with two or three years of experience in designing circuits for driving light-emitting devices including organic light-emitting diodes, or a Ph.D. with experience in the same. Kattamis, ¶¶41-42.

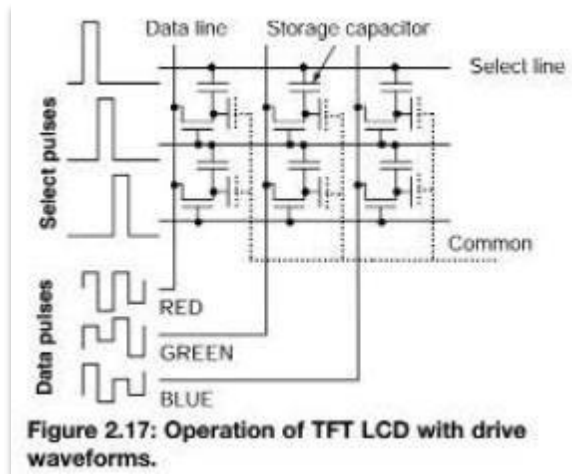
B. Background Knowledge of A POSITA

Inquiring into whether “any ‘differences’ between the invention and the prior art would have rendered the invention obvious ... necessarily depends on [a POSITA’s] knowledge,” including an “assessment of the ... background knowledge possessed” by the POSITA. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020). The subjects below were “within the general knowledge” of a POSITA. *See id.* at 1338; *Dish Network L.L.C. v. Broadband iTV, Inc.*, IPR2020-01267, Paper 15 at 10 n.4 (P.T.A.B. Jan. 21, 2021) (“[W]e do not include the general knowledge of a person of ordinary skill in the art in listing the grounds themselves, recognizing that such knowledge is considered in every analysis.”).

Dr. Kattamis corroborates the general knowledge of a POSITA with engineering references (Ex. 1009, Ex. 1010, Ex. 1011), published well before the ’047 Patent. Camara published in 2002 “as an all-inclusive reference book for both the practicing engineer and the undergraduate electrical engineering student.” Ex. 1009, Preface. Den Boer published in 2005 and summarizes “Active Matrix Liquid Crystal Displays: Fundamentals and Applications.” Ex. 1010, Title. Han published in 2006 and discusses driving LED displays. Ex. 1011; Kattamis, ¶¶45-62. Each of the topics would have been well-known to a POSITA before the priority date of the ’047. Kattamis, ¶¶45-62.

a. Display Background

It was known that active-matrix displays include millions of pixels (e.g., “1080x1920 pixels”), with each pixel having “three subpixels” (e.g., red-green-blue). Ex. 1010, 3, 176; Kattamis, ¶48.



Ex. 1010, 40. It was also known to drive the pixels using a “TFT pixel array circuit (Fig. 2.17) [with] select buslines, data buslines, a TFT at each pixel, and a storage capacitor ... at each pixel.” *Id.*, pp. 39-40. Source drivers use red-green-blue data to drive the columns of lines running vertically in the displays, and gate or row drivers select the rows of horizontal lines and turn on pixels. *Id.*, 93-98; Kattamis, ¶¶48-49.

It was known that OLEDs are semiconductors comprising organic materials that convert electrical energy to light, much like LEDs. Individual OLED pixels are “current driven,” meaning that a pixel’s color and brightness are adjusted by setting the current through the manipulation of TFT(s). Ex. 1011, 53 §1; Kattamis, ¶50.

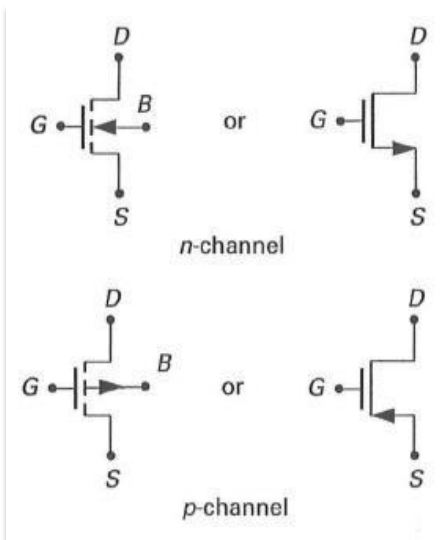
It was known that because of “inherent process variation” that occurs during manufacturing, “[a] number of TFT active matrix pixel circuits have been developed

in order to compensate for TFT parameter variations” and to “compensate the non-uniform characteristics of the current” from those TFTs. Ex. 1011, Abstract, Introduction; Kattamis, ¶51.

b. Basic Circuit Components for Displays

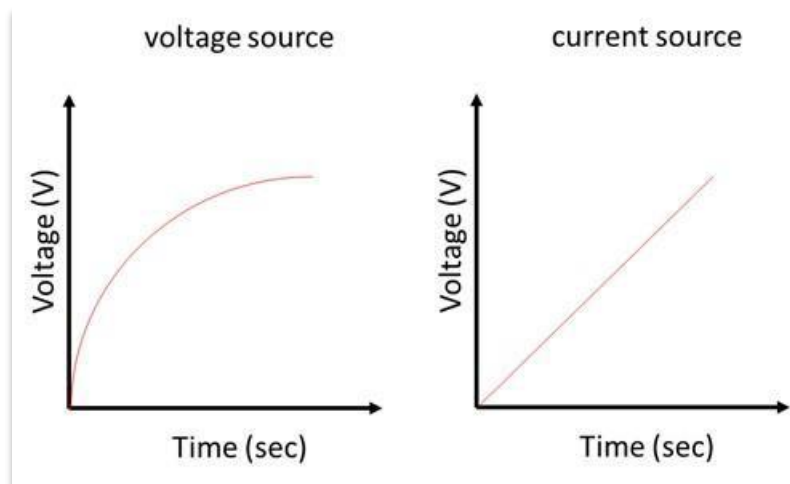
It was known that an ideal voltage source represents a two-terminal device with fixed voltage across its terminals, regardless of current flow or the load that it drives. An ideal current source represents a two-terminal device that delivers fixed current through its terminals, regardless of voltage or the load that it drives. Ex. 1009, 26-4, 26-5; Kattamis, ¶¶52-53.

It was known to convert a voltage signal to a current signal. For example, it was known to configure a transistor to receive an input voltage (V_G) on its gate terminal and produce an output current flowing between drain and source terminals (I_D). Ex. 1009, 43-31, 43-32; Kattamis, ¶54.



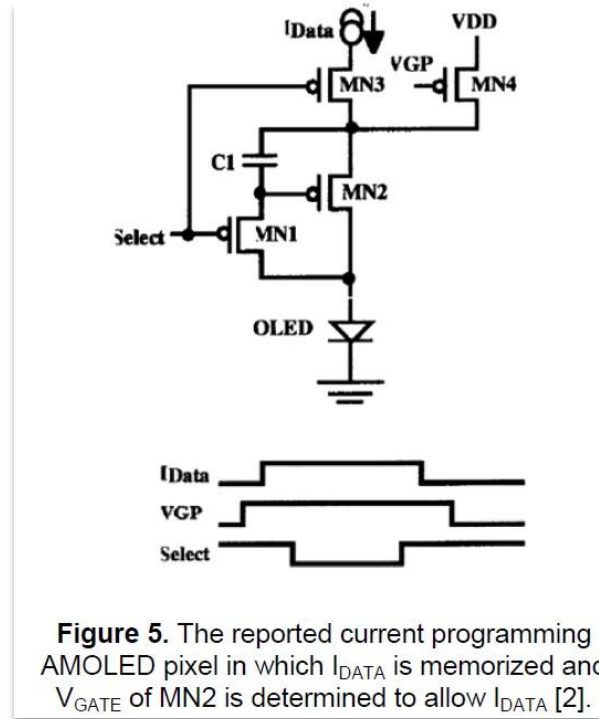
c. Voltage and Current Programming

It was known that capacitors store charge, and it was known to use capacitors as a buffer in pixel circuits. Ex. 1010, 27. It was known that when charging a capacitor, voltage on the capacitor typically rises: exponentially when using a voltage source (referred to as voltage programming), and linearly when using a current source (referred to as current programming). Kattamis, ¶¶55-60.

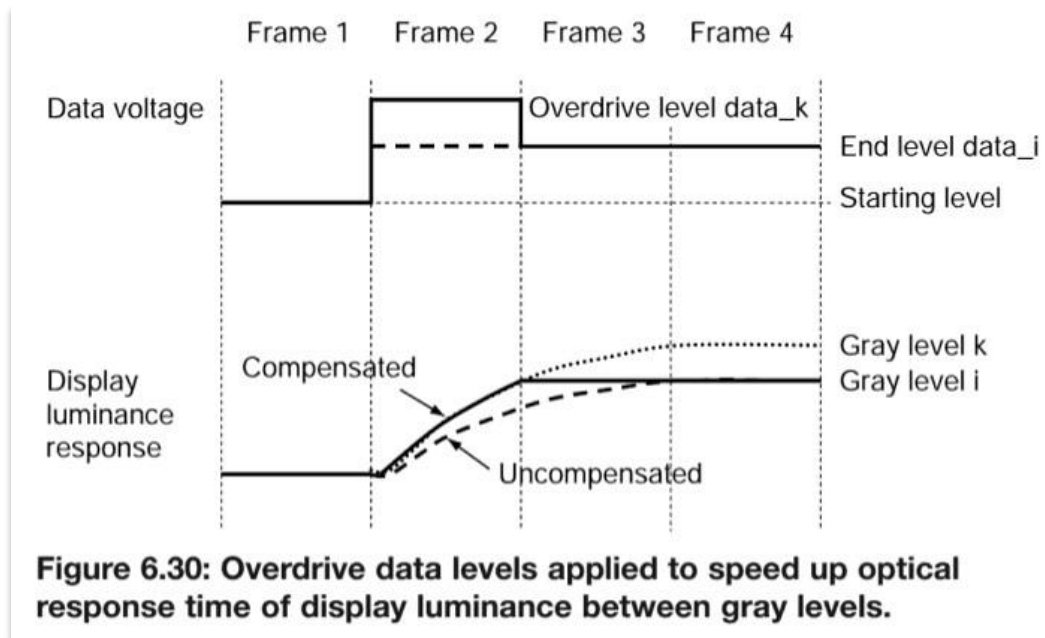


Ex. 1009, 29-4, 30-2 to 30-7. Thus, voltage sources were known to charge the capacitor faster, as compared to current sources. Kattamis, ¶¶55-62.

“[C]urrent programming pixel circuits can compensate mobility variation as well as threshold voltage variation.” Ex. 1011, 53. A known advantage of current programming is that the current remains constant even if there are variations in TFT threshold voltage or mobility. Structures for current programming pixel circuits were known in the art. Kattamis, ¶59.



Ex. 1011, Fig. 5. One known problem was that the relatively lengthy amount of time needed to charge a capacitor under current programming could limit the speed of the display. For example, uncompensated pixels with high capacitance were unable to attain the required brightness level within the timespan of an image frame, so extra drive voltage was applied to enable a compensated response. Kattamis, ¶¶59-62.



Ex. 1010, p. 168 (Fig. 6.30); Kattamis, ¶60.

VIII. CLAIM CONSTRUCTION

Claim terms subject to IPR are construed using *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). 37 C.F.R. §42.100(b). Only terms necessary to resolve the controversy need construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Because the prior art asserted herein discloses embodiments within the Claims' indisputable scope, the Board need not construe the Claims' outer bounds. All claim terms should be construed according to their plain and ordinary meaning. Kattamis, ¶43.

IX. GROUNDS OF UNPATENTABILITY

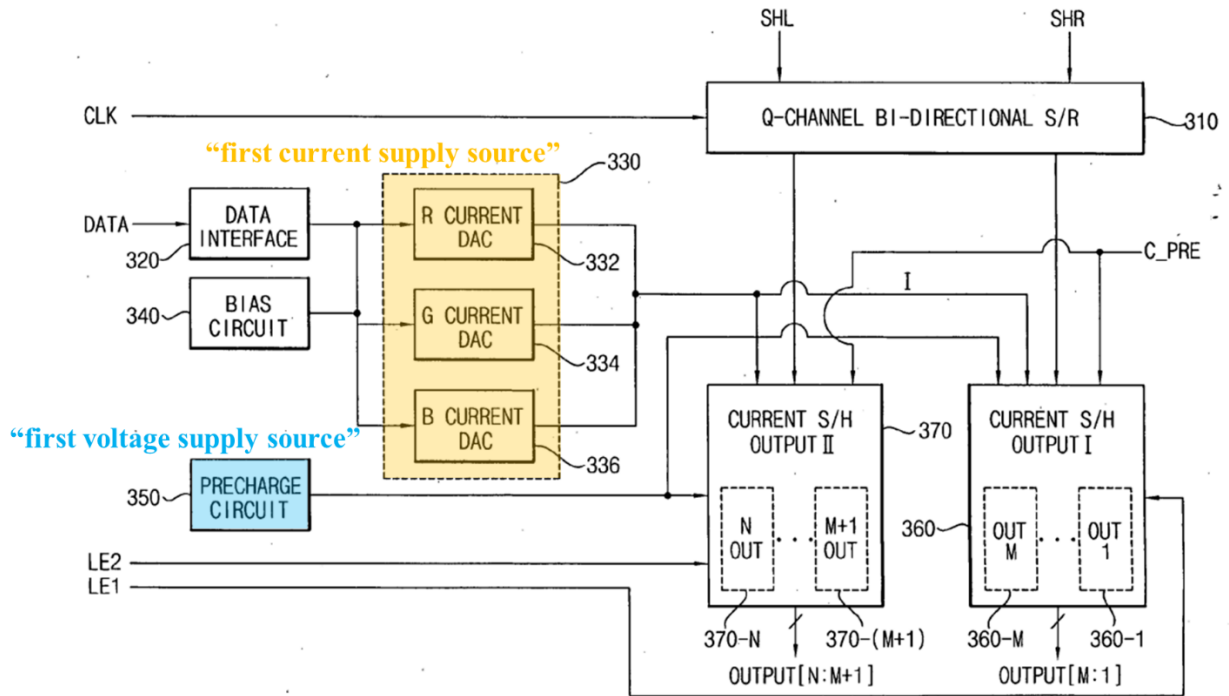
This Petition is supported by the Declaration of Dr. Alex Z. Kattamis, Ph.D., P.E., which describes the prior art's scope and content at the time of and well before

the '047. *See* Ex. 1003 (“Kattamis”). The prior art renders the Claims unpatentable based on the below Grounds. Kattamis, ¶¶63-226.

A. GROUND 1-2: BAEK

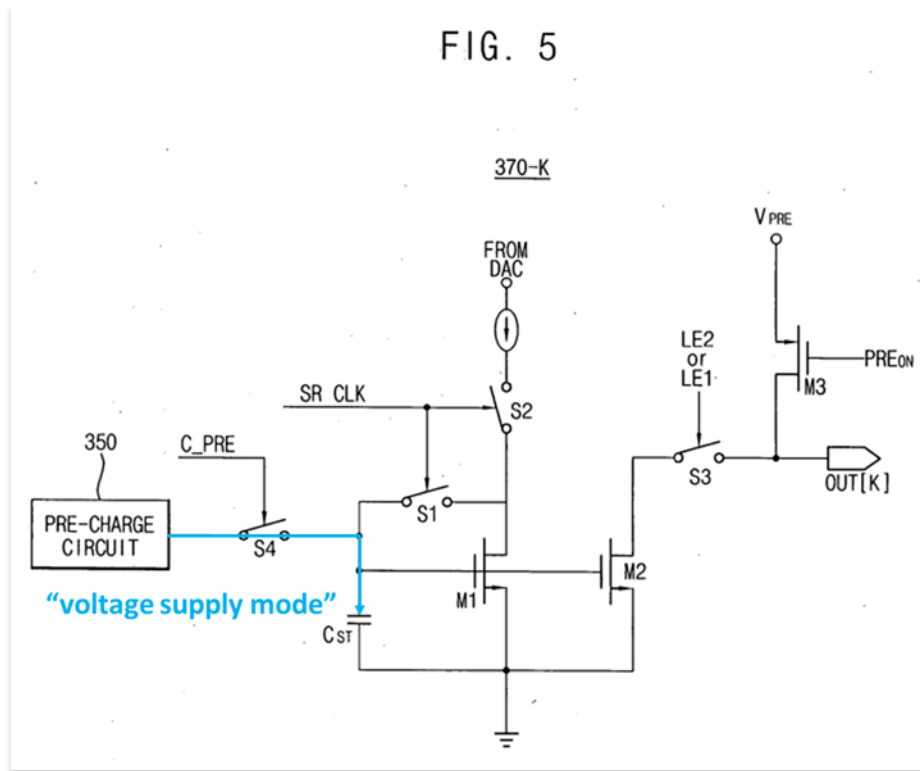
a. Overview of Baek

Similar to the '047, **Baek** is directed to a “display driver circuit” that “drive[s] a display panel...using a smaller current.” Baek, [0019], [0063]; Kattamis, ¶64. For example, as shown in Fig. 3, **Baek** discloses a “display driver circuit” that includes a plurality of “current sample/hold circuits 370-(M+1) through 370-N” that operate in three modes. Baek, [0056], [0058], [0063]. A “current digital-to-analog conversion unit 330” supplies the “current sample/hold circuits” with “analog gray-scale-current,” and a “pre-charge circuit 350” supplies them with a “pre-charge...voltage.” Baek, [0044], [0056], [0062], Fig. 3; Kattamis, ¶¶63-64.



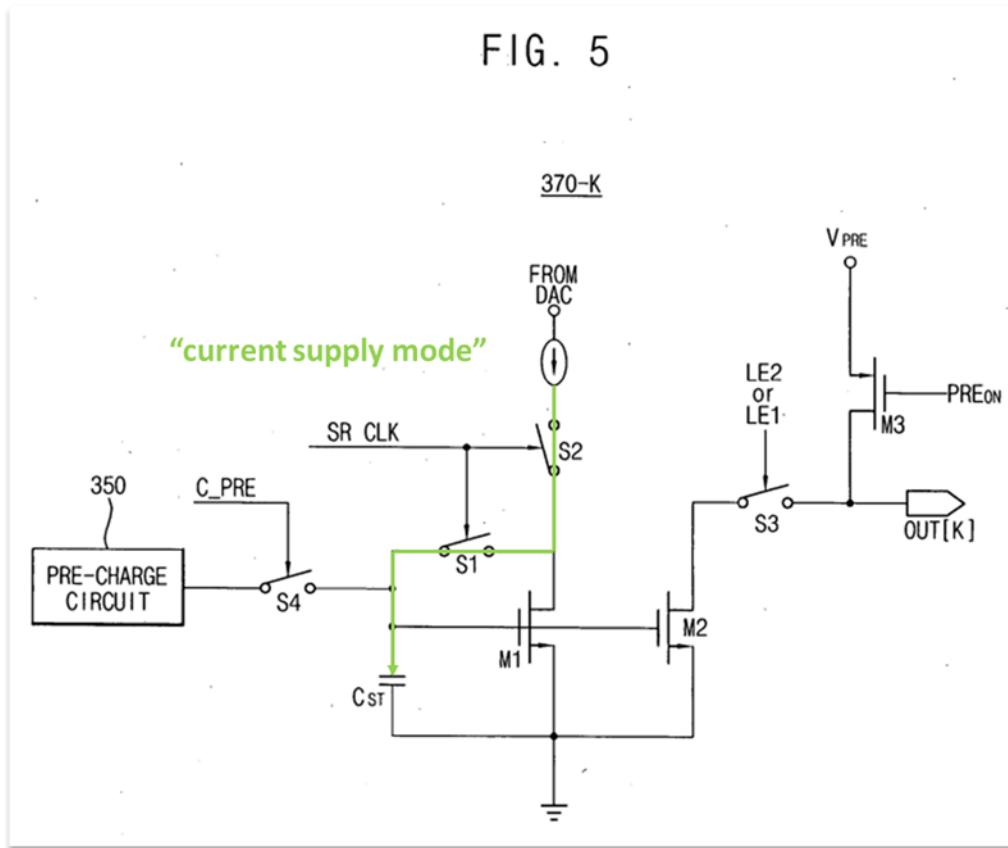
Baek, Fig. 3.

As depicted in Fig. 3, each of these “current sample/hold circuits 370-(M+1) through 370-N” have the same inputs, but each has a separate output. One of these current sample/hold circuits is depicted in Fig. 5, which depicts these common inputs and the individual output (“OUT[K]”). During a pre-charge mode, the “switch S4” is “turned on” and switches S1 and S2 are turned off such that pre-charge circuit 350 “pre-charge[s] a voltage of the storage capacitor CST to a voltage level slightly lower than a threshold voltage of the first transistor M1.” Baek, [0057], [0062]; Kattamis, ¶165.



Baek, Fig. 5.

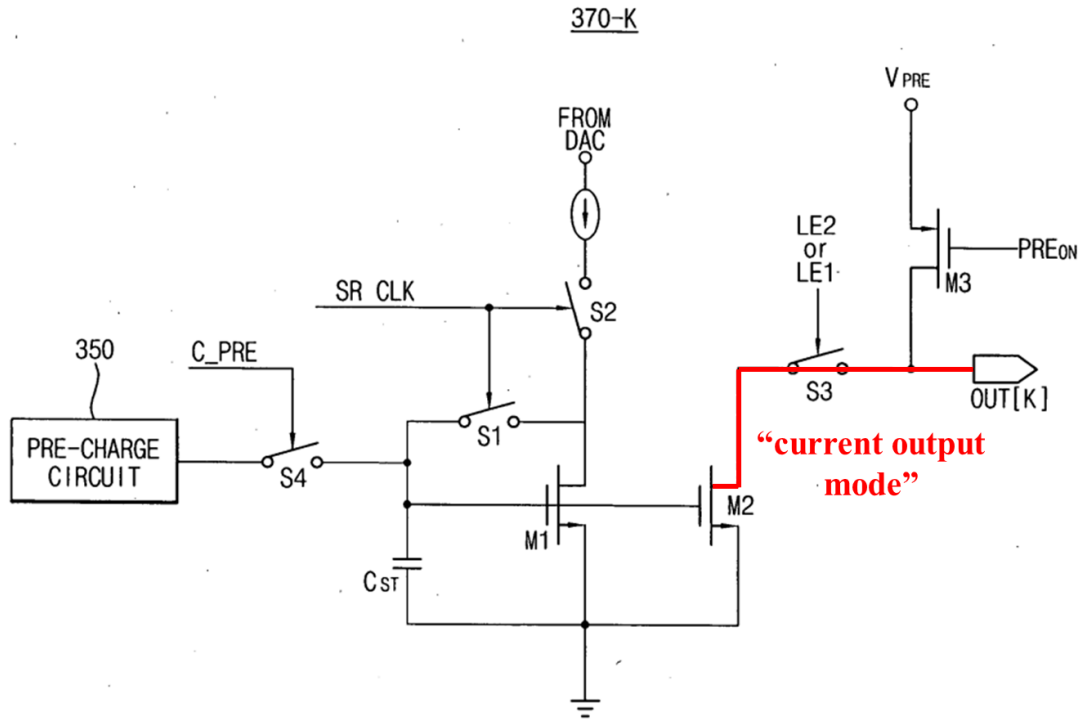
During a current supply mode, switch S_4 is turned off and switches S_1 and S_2 are “turned on” such that “storage capacitor C_{ST} ...charges the analog gray-scale current” from “current digital-to-analog conversion unit 330” to produce a voltage at the terminal of the capacitor C_{ST} coupled to the gate of transistor M_1 . Baek, [0056]-[0057]. Kattamis, ¶66.



Baek, Fig. 5.

Finally, during a current output mode, the second transistor M2 “output[s] the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current.” Baek, [0058]; Kattamis, ¶67.

FIG. 5



Baek, Fig. 5.

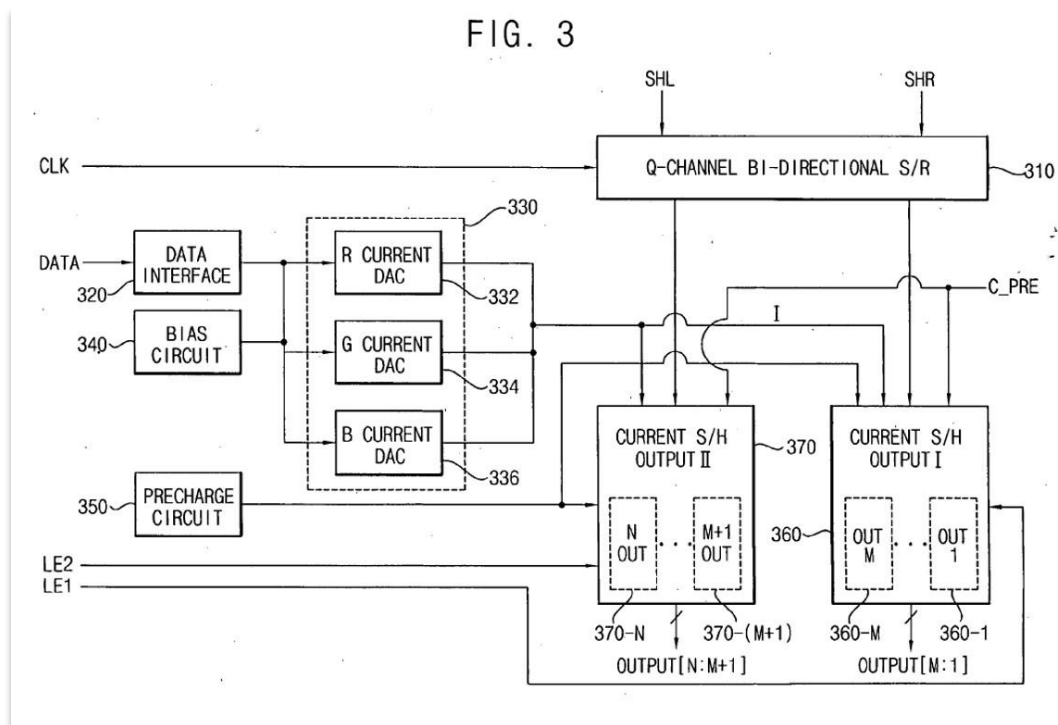
b. Claim 1

As discussed below, Claims 1-4 and 9 are anticipated by, and at minimum obvious over, **Baek**. In addition to §IX.A.a, the following identifies example disclosures that each disclose (Ground 1), and at minimum render obvious (Ground 2), Claims 1-4 and 9. Kattamis, ¶¶68-135.

i. 1(pre): “A current driving device, comprising:”

To the extent the preamble is limiting, **Baek discloses a current driving device** (e.g., “display driver circuit”). Baek, [0035]-[0036], [0064], Fig. 3; Kattamis, ¶¶68-70.

For example, **Baek discloses a “display driver circuit”** that is used for “current-driven active matrix type OLED display devices” as shown in Fig. 3. Baek, [0035], [0064]; Kattamis, ¶70.

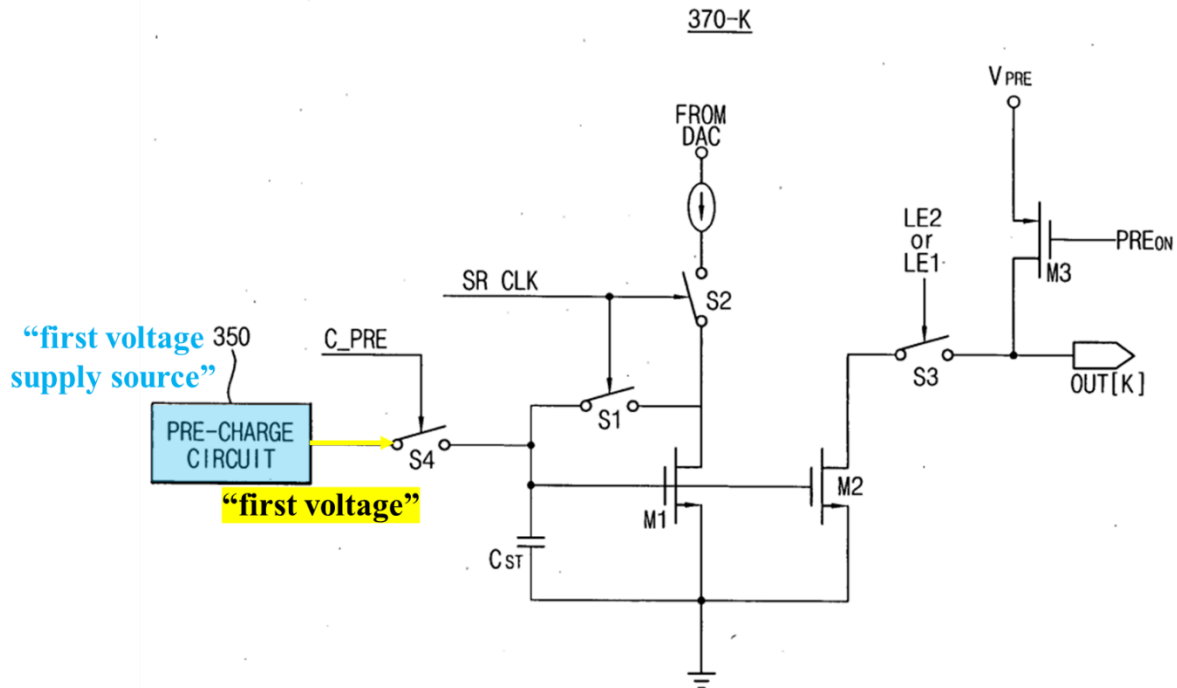


Id., Fig. 3; see [0036] (describing circuitry within “display driver circuit”).

ii. 1(a): “a first voltage supply source for supplying a first voltage;”

Baek discloses a first voltage supply source for supplying a first voltage (e.g., “pre-charge circuit 350” supplying “voltage”). Baek, [0026], [0028], [0036], [0055], [0062], Figs. 3, 5; Kattamis, ¶¶71-73.

FIG. 5

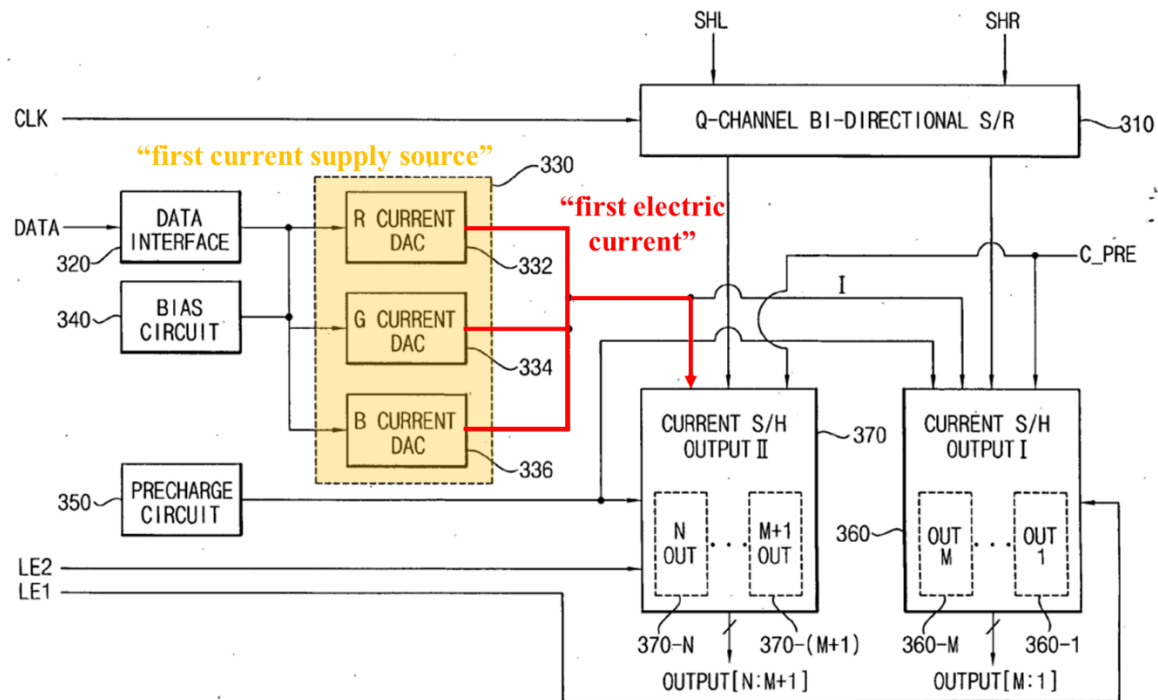


Baek, Fig. 5; see also Baek, Fig. 3.

For example, **Baek** discloses a “pre-charge circuit 350” (annotated blue) that supplies a “voltage...slightly lower than a threshold voltage of the first transistor M1” (annotated yellow). Baek, [0036], [0062]. Kattamis, ¶73.

iii. 1(b): “a first current supply source for supplying a first electric current;”

Baek discloses a first current supply source for supplying a first electric current (e.g., “current digital-to-analog conversion unit 330” for supplying “an analog gray-scale current”). Baek, [0036], [0044], [0055]-[0056], Figs. 3, 5; Kattamis, ¶¶74-76.



Baek, Fig. 3; *see also* Baek, Fig. 5.

For example, **Baek** discloses a “current digital-to-analog conversion unit 330” (annotated gold) that “convert[s] gray-scale data provided from the data interface circuit 320 to an analog gray-scale current” (annotated red) that is “applied” to “current sample/hold circuit[s].” Baek, [0036], [0044], [0055]-[0056]. Kattamis, ¶76.

iv. 1(c): “a plurality of output terminals;”

Beak discloses a plurality of output terminals (*e.g.*, “output terminal[s]”).
Baek, [0045], [0048]-[0049], [0054], [0058], [0063], [0065], Figs. 3, 5; Kattamis,
¶¶77-79.



Baek, Fig. 3.

FIG. 5

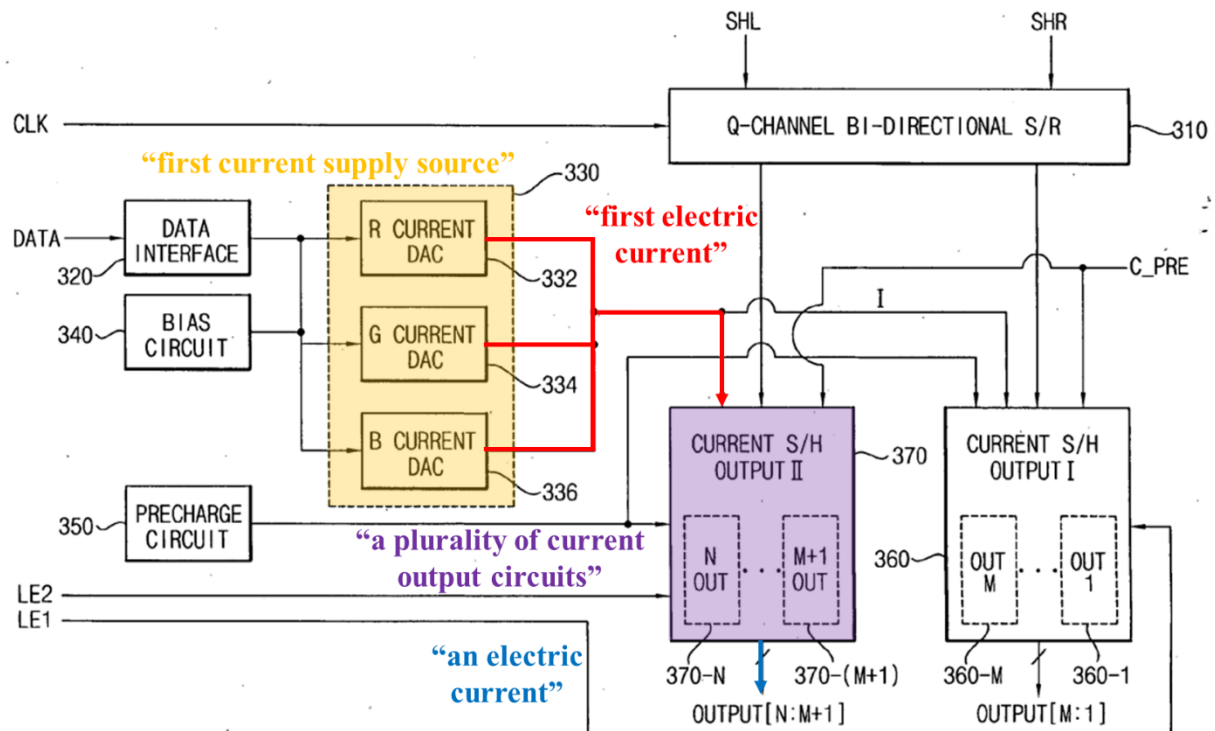


Baek, Fig. 5.

For example, **Baek** discloses a “second current sample/hold output circuit 370” that samples/holds “the analog gray-scale current” and outputs “output signals OUT M+1 through OUT N to the channels M+1 through N” (annotated green). Baek, [0048]-[0049]. These output signals “OUT M+1 through OUT N” disclosed in connection with Figure 3 each correspond to “an output terminal OUT[K]” for “a kth channel” disclosed in connection with Figure 5. Baek, [0049], [0054], [0058]. Output terminals OUT[K] “output the analog gray-scale current” to “drive a display panel...using a smaller current.” Baek, [0058], [0063]. Kattamis, ¶79.

v. 1(d)(1): “a plurality of current output circuits for outputting an electric current in accordance with said first electric current”

Baek discloses a plurality of current output circuits (*e.g.*, “current sample/hold circuits 370-(M+1) through 370-N”) **for outputting an electric current in accordance with said first electric current** (*e.g.*, “output the analog gray-scale current...based on the charged analog gray-scale current”). Baek, [0036], [0039], [0043], [0054], [0058], [0063], Figs. 3, 5; Kattamis, ¶¶80-83. See 1(b)-1(c).



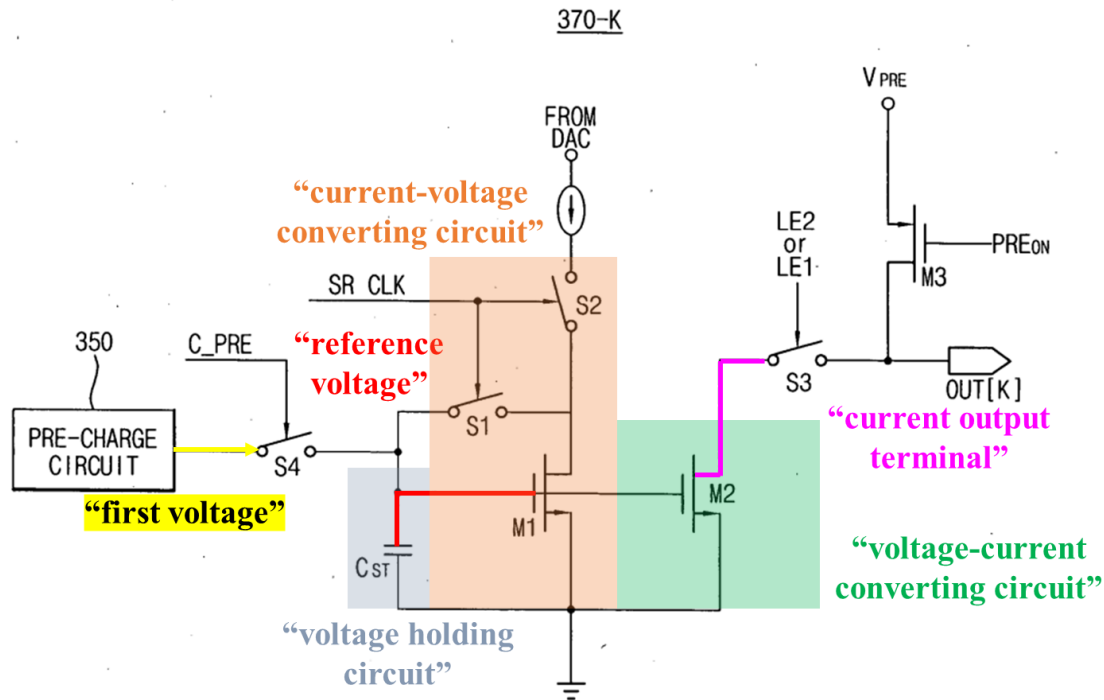
Baek, Fig. 3; *see also* Baek, Fig. 5.

For example, as discussed in 1(b)-1(c), **Baek** discloses a second current sample/hold output circuit 370 (annotated purple) that outputs current to a display panel (annotated blue). Baek, [0036], [0063]. Circuit 370 “include[s] current sample/hold circuits 370-(M+1) through 370-N,” which each receive “analog gray-scale current” (annotated red) from “current digital-to-analog conversion unit 330” (annotated gold). Baek, [0039], [0043]. Each “current sample/hold circuit 370-k, which may correspond to a kth channel,” outputs “the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current” from DAC unit 330. Baek, [0054], [0058]; Kattamis, ¶83.

- vi. **1(d)(2) “each of said current output circuits comprising a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein”**

Baek discloses each of said current output circuits (see 1(d)(1)) comprising a current-voltage converting circuit (e.g., “first transistor M1” connected to a “first switch S1,” a “second switch S2” “charges the analog gray-scale current” in “storage capacitor CST”), a voltage-current converting circuit (e.g., “a second transistor M2” converts voltage of “storage capacitor CST” to “output the analog gray-scale current”), a voltage holding circuit (e.g., “storage capacitor CST”) having a terminal being connected to a reference voltage different from the first voltage (e.g., terminal “coupled to the gate [voltage] of the first transistor M1” has a different voltage from pre-charge circuit 350), and at least one current output terminal (e.g., “drain [terminal] of the second transistor M2” “output[s] the analog gray-scale current”). Baek, [0036], [0052], [0054]-[0059], [0062]-[0063], Fig. 5; Kattamis, ¶¶84-91. See 1(a), 1(d)(1).

FIG. 5



Baek, Fig. 5.

For example, as discussed in 1(d)(1), the second current sample/hold output circuit 370 includes a plurality of current output circuits, which are also depicted in Figure 5. Baek, [0036], [0054], [0058], [0063]; Kattamis, ¶87.

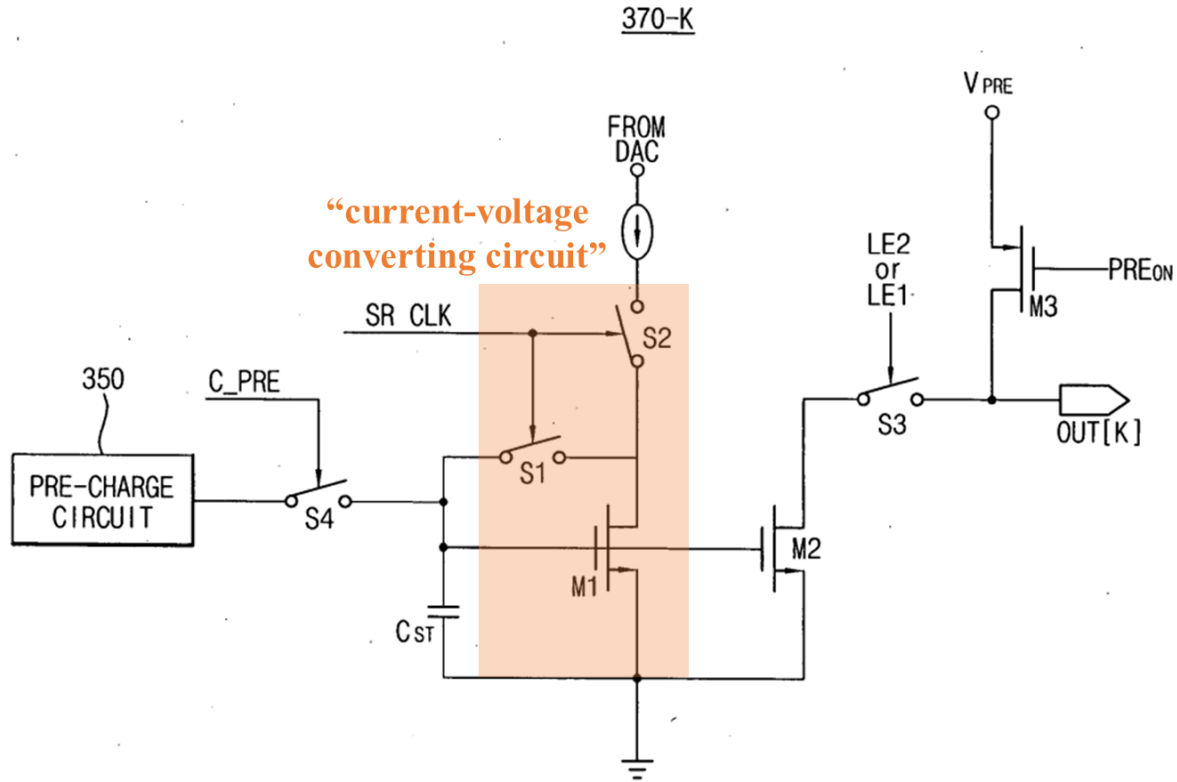
(i) ***"current-voltage converting circuit"***

Regarding the recited "current-voltage converting circuit," **Baek** discloses a "first transistor M1" connected to a "first switch S1 and [a] second switch S2" (annotated orange) that are "turned on," while switches S3 and S4 are turned off, such that an "analog gray-scale current" from "a current digital-to-analog conversion

unit 330” (see Fig. 3) is “applied to a drain of the first transistor M1 via the second switch S2” and to the “gate of the first transistor M1” via switch S1 to “charge[]” “storage capacitor CST” using “the analog gray-scale current.” Baek, [0055]-[0056], [0058]-[0059], Fig. 5.³ The storage capacitor CST is further coupled to “a fourth switch S4 [which] may be turned on to pre-charge a voltage,” as discussed in claim 3 below. Baek, [0062]. Thus, the current coming in via S2 is used to charge the capacitor CST—converting the current to voltage. Kattamis, ¶88.

³ This is consistent with '047, which discloses “a current-voltage converting function is actuated” when “a gate voltage for passing the electric current from the reference current source I1 is generated uniquely at the gates of the Nch transistors QN1-QNm” and “the voltage holding capacitance element C1 accumulates the electric charges in accordance with the gate voltages.” '047, 7:59-8:15. Kattamis, ¶88.

FIG. 5



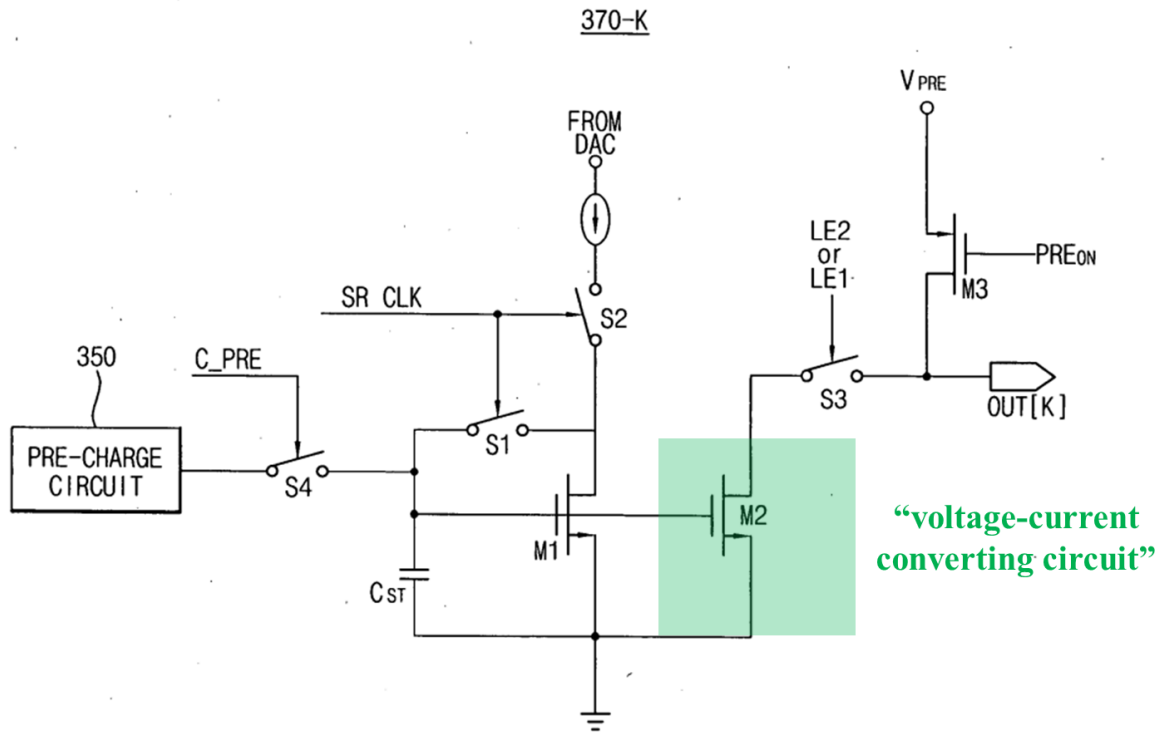
Baek, Fig. 5.

(ii) “voltage-current converting circuit”

Regarding the recited “voltage-current converting circuit,” **Baek** further discloses “a second transistor M2” (annotated dark green) that “ha[s] its gate coupled to the storage capacitor CST” to “output the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current” when switch S3 is “activated” and switches S1, S2, and S4 are turned off. Baek, [0056]-[0058],

[0062].⁴ Thus, the voltage stored in CST is converted to current through S3.
Kattamis, ¶89.

FIG. 5



Baek, Fig. 5.

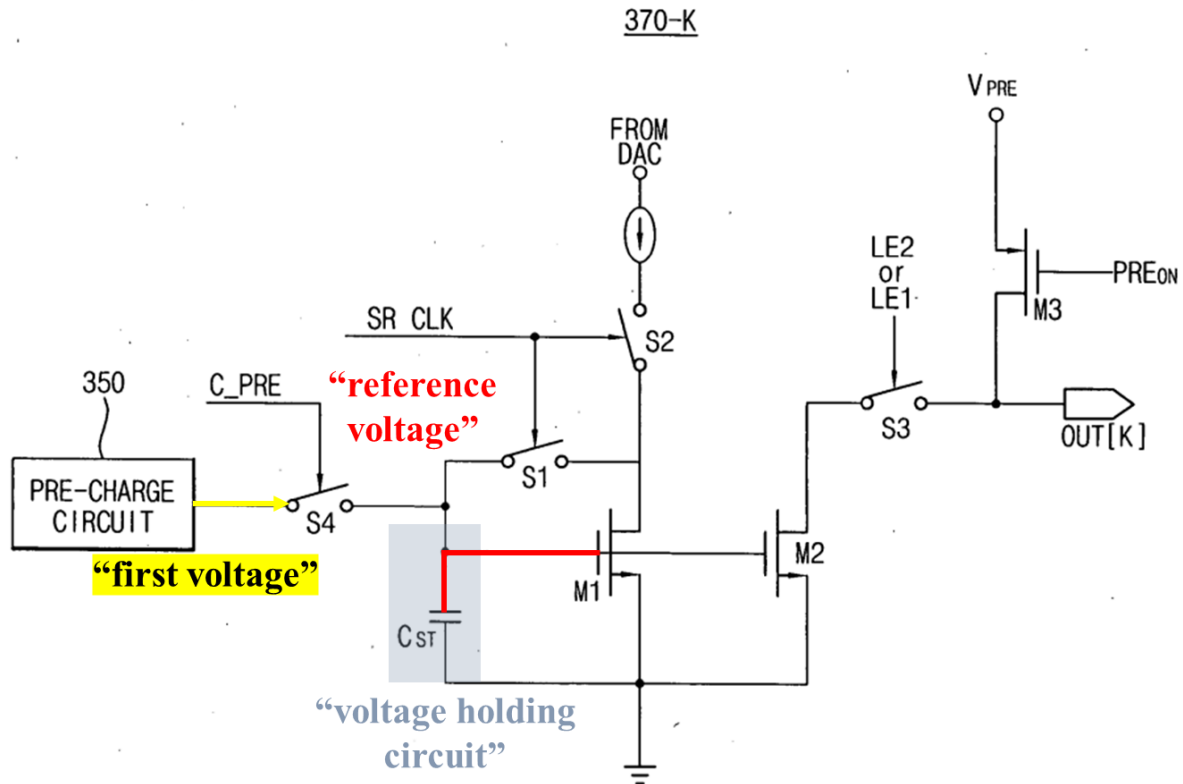
⁴ This is consistent with '047, which discloses “a voltage-current converting function is actuated” when “[a] gate voltage according to the electric charges accumulated in the voltage holding capacitance element C1 is applied to the gates of the Nch transistors QN1-QNm” such that “it is possible to output a sink current having a current value proportional to the reference current.” '047, 8:17-49. Kattamis, ¶89.

(iii) *“voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage”*

Regarding the recited “voltage holding circuit,” **Baek** further discloses a “storage capacitor CST” (annotated gray) with one terminal connected to ground and the other terminal (unannotated) “coupled to the gate of the first transistor M1,” which supplies a reference voltage (annotated red). Baek, [0055]-[0056], Fig. 5. The capacitor also has another terminal connected to pre-charge circuit 350, which supplies the first voltage (annotated yellow). Baek, [0055]-[0056], Fig. 5. In a “pre-charge” mode, “switch S4” is “turned on” and switches S1, S2, and S3 are turned off such that pre-charge circuit 350 “pre-charge[s] a voltage of the storage capacitor CST to a voltage level slightly lower than a threshold voltage of the first transistor M1.” Baek, [0052], [0057]-[0058], [0062]. Thereafter, in a current charge mode, switch S4 is turned off and switches S1 and S2 are “turned on” such that “storage capacitor CST” is “charge[d]” with “the analog gray-scale current” from “current digital-to-analog conversion unit.” Baek, [0056]-[0057], [0062]. A POSITA would have understood or at least found obvious that the analog gray-scale current charges the capacitor as a reference voltage, as this is a fundamental property of capacitors, as discussed in Section VII.B.c. In this current charge mode, the reference voltage on the terminal of capacitor CST coupled to transistor M1 is different from the voltage supplied by pre-charge circuit 350 because switch S4 is turned off and CST

is instead charged with current coming in through S1 and S2. Baek, [0062];⁵
Kattamis, ¶90.

FIG. 5



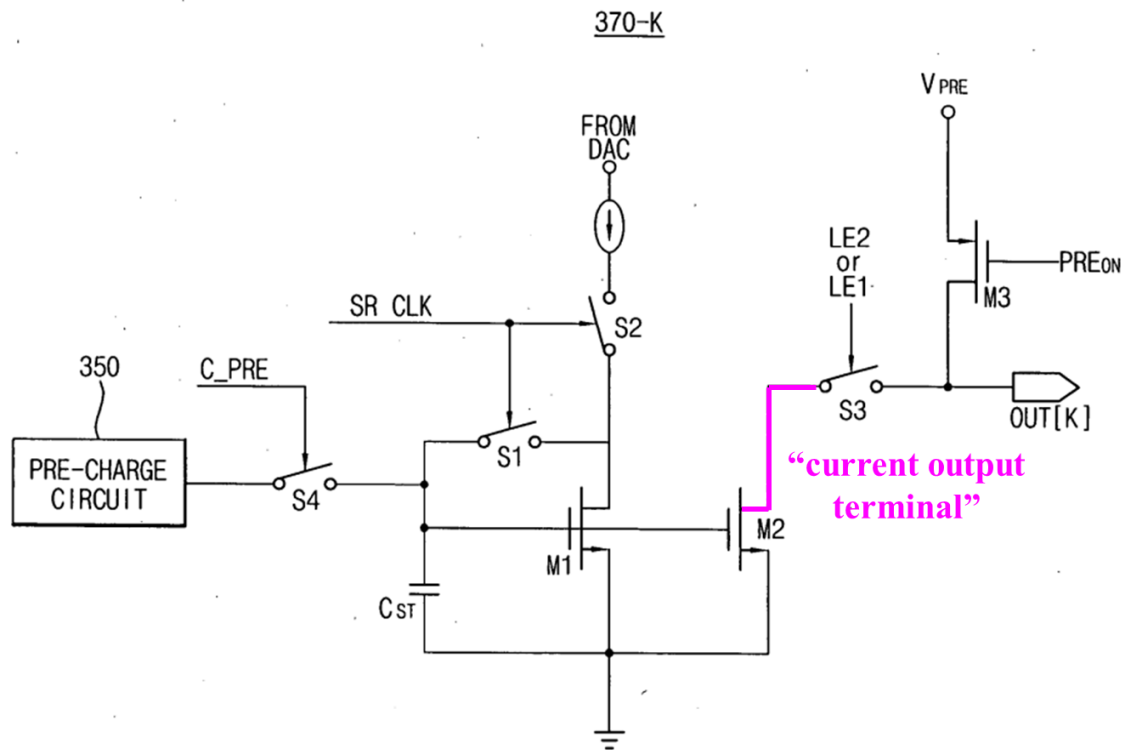
Baek, Fig. 5.

⁵ This is consistent with the '047, which discloses "the voltage holding capacitance element C1 is charged to a constant voltage (this corresponds to the first voltage, and will be referred to as a reference voltage hereinafter) that is supplied from the voltage supply source V1." '047, 7:46-52. Kattamis, ¶90.

(iv) “at least one current output terminal”

Regarding the recited “current output terminal,” **Baek** further discloses that, in a current output mode, switches S1, S2, and S4 are turned off and a “switch S3...couple[s] a drain of the second transistor M2” (annotated pink) to “an output terminal OUT[K].” Baek, [0057]-[0058], [0062]. Transistor M2 “output[s] the analog gray-scale current to the output terminal OUT[K] based on” the “analog gray-scale current” that charges “the storage capacitor CST” connected to transistor M2’s gate. Baek, [0057]-[0058], [0062]; Kattamis, ¶91.

FIG. 5



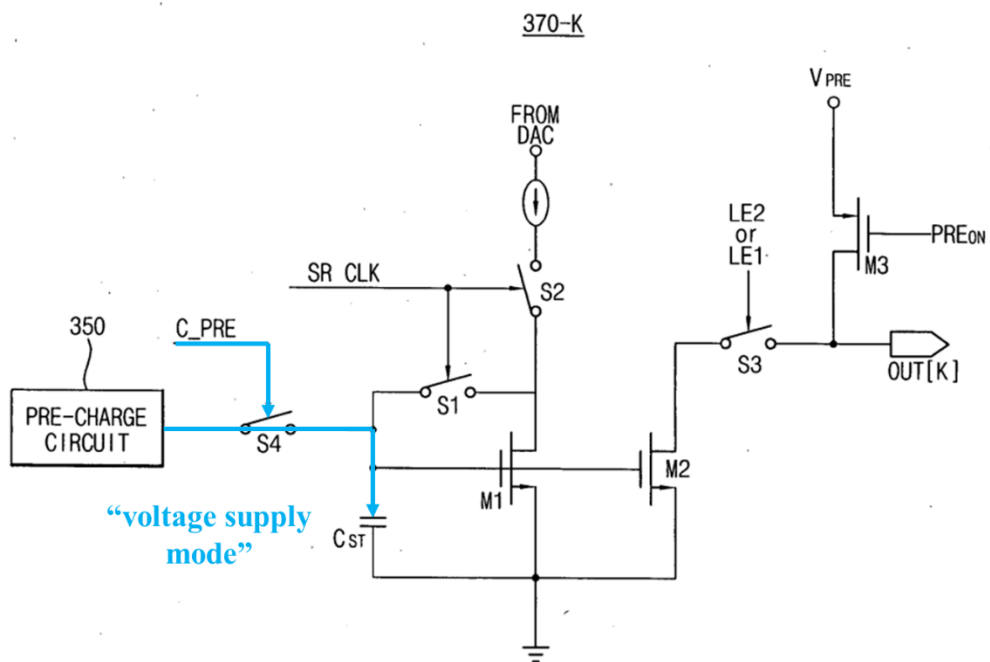
Baek, Fig. 5.

- vii. **1(e): “each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,”**

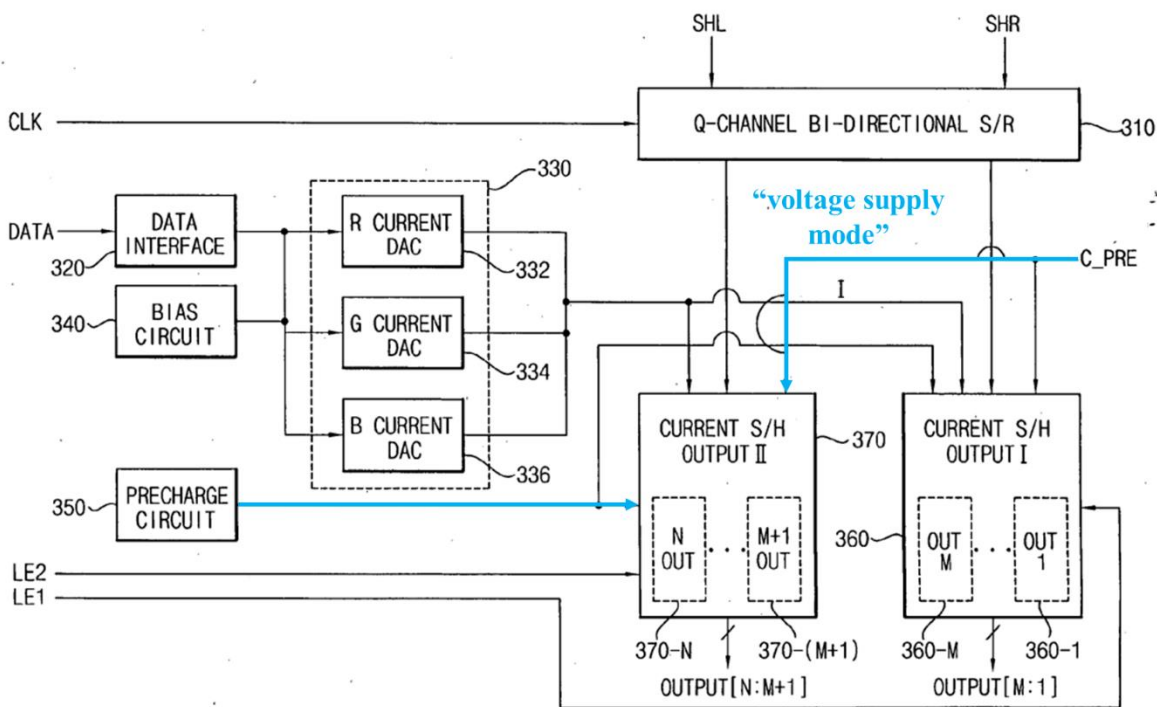
Baek discloses each of said current output circuits (see 1(d)(1)) operates in three operation modes including a voltage supply mode (e.g., “pre-charge” mode to “pre-charge a voltage of the storage capacitor CST”), a current supply mode (e.g., mode supplying “an analog gray-scale current” from “a current digital-to-analog conversion unit 330”), and a current output mode (e.g., mode “output[ting] the analog gray-scale current to the output terminal OUT[K]”). Baek, [0040], [0056]-[0058], [0062], Figs. 3-5; Kattamis, ¶¶92-100. *See* 1(d)(1)-1(d)(2).

For example, as discussed in 1(d)(2), **Baek** discloses a “pre-charge” mode (annotated blue) where a pre-charge circuit 350 “pre-charges a voltage of the storage capacitor CST.” Baek, [0062]. Current output circuit 370 operates in this mode when “pre-charge signal C_PRE” turns on “switch S4” while switches S1, S2, and S3 are “turned off,” as shown in Figure 5. Baek, [0057]-[0058], [0062]. As shown in Figure 3, the C_PRE signal is supplied to the “second sample/hold output circuit 370” such that each “current sample/hold circuits 370-(M+1) through 370-N” receives the C_PRE signal and applies the voltage from pre-charge circuit to the storage capacitor CST in the pre-charge mode. Kattamis, ¶95.

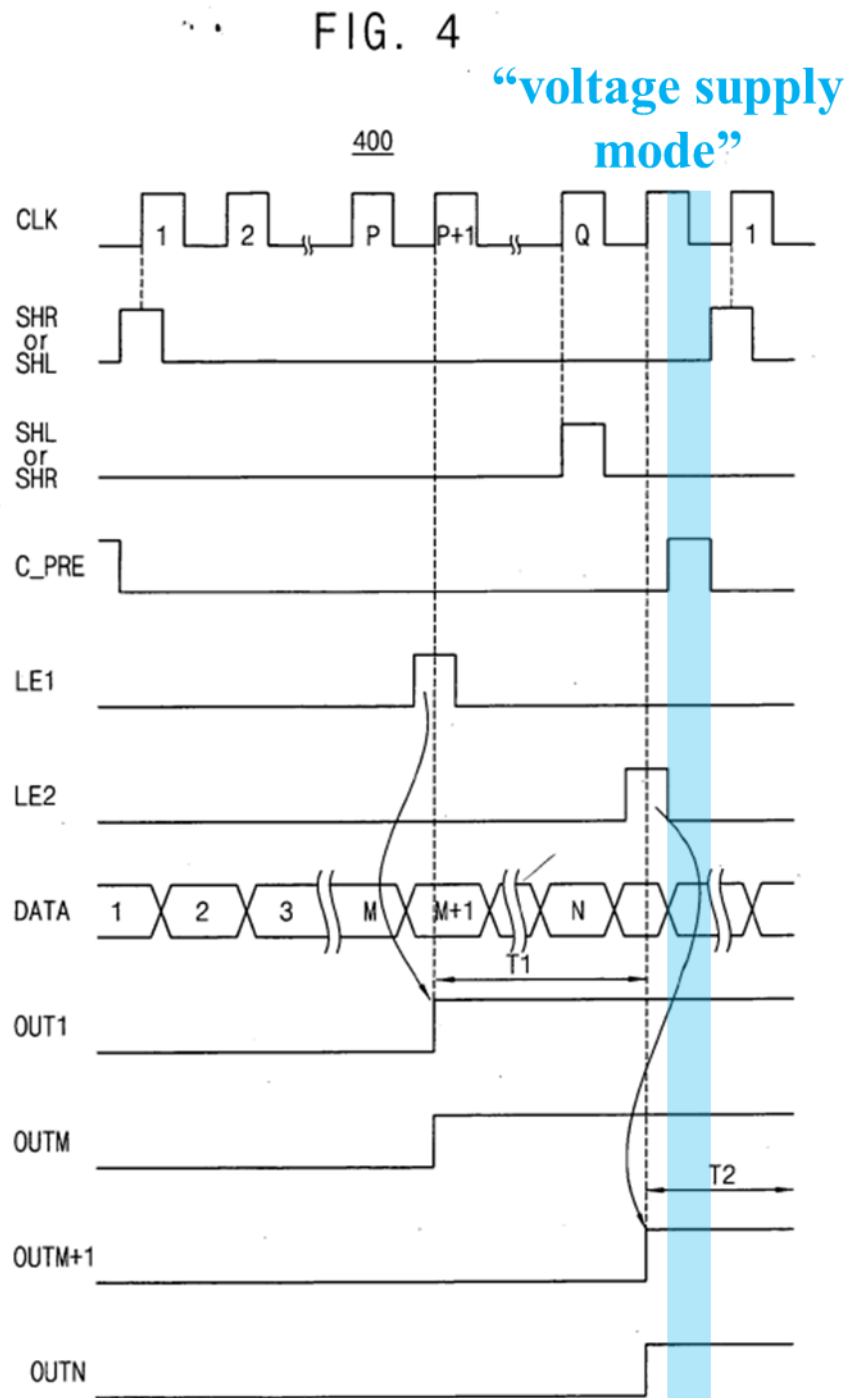
FIG. 5



Baek, Fig. 5.



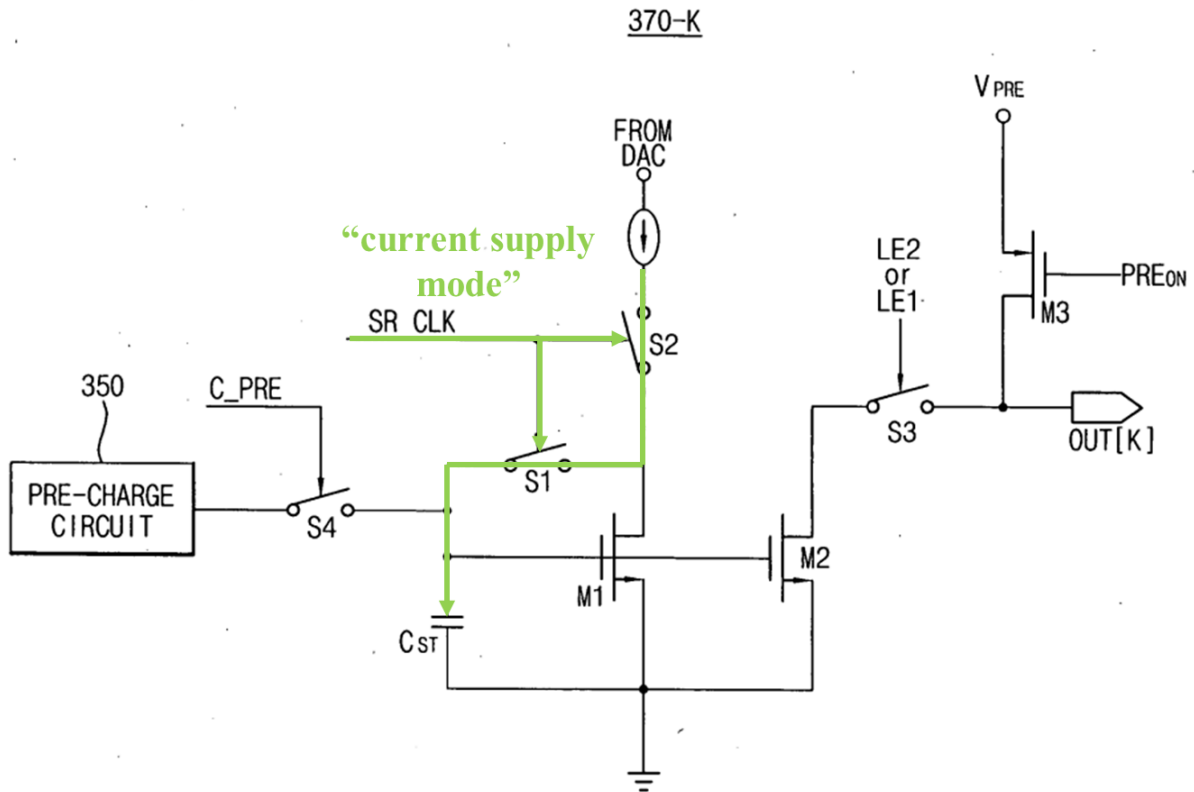
Baek, Fig. 3. Figure 4 discloses the pre-charge mode when the C_PRE signal turns on switch S4 while the other switches are turned off. Kattamis, ¶96.



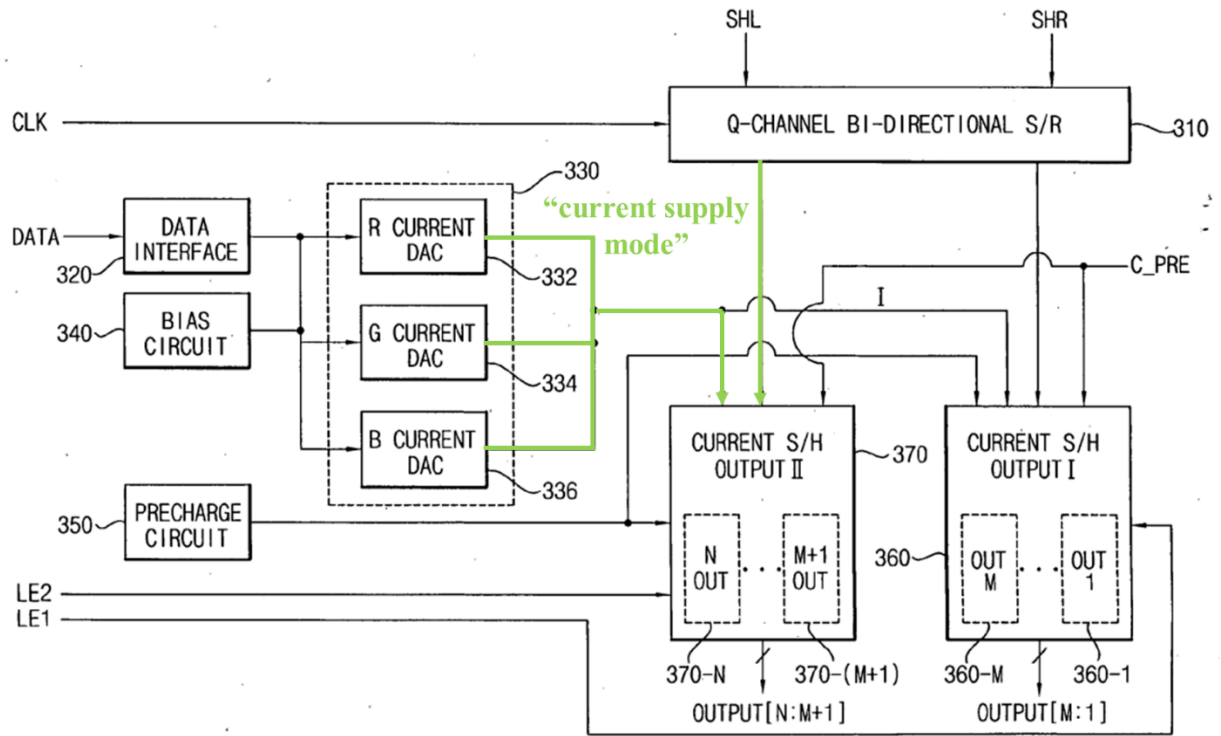
Baek, Fig. 4.

As also discussed in 1(d)(2), **Baek** discloses a current charge mode (annotated green) where “storage capacitor CST” is charged by “the analog gray-scale current” from “current digital-to-analog conversion unit 330.” Baek, [0056]-[0057]. Current output circuit 370 operates in this mode when switches S3 and S4 are turned off and “switch S1 and...switch S2” are “turned on” based on “second clock signal SR CLK.” Baek, [0040], [0056]-[0057], [0062]. As shown in Figure 3, the CLK signal is supplied to the “second sample/hold output circuit 370” such that each “current sample/hold circuits 370-(M+1) through 370-N” receives the CLK signal and applies the analog gray-scale current from current digital-to-analog conversion unit 330 to the storage capacitor CST in the current charge mode. Kattamis, ¶97.

FIG. 5



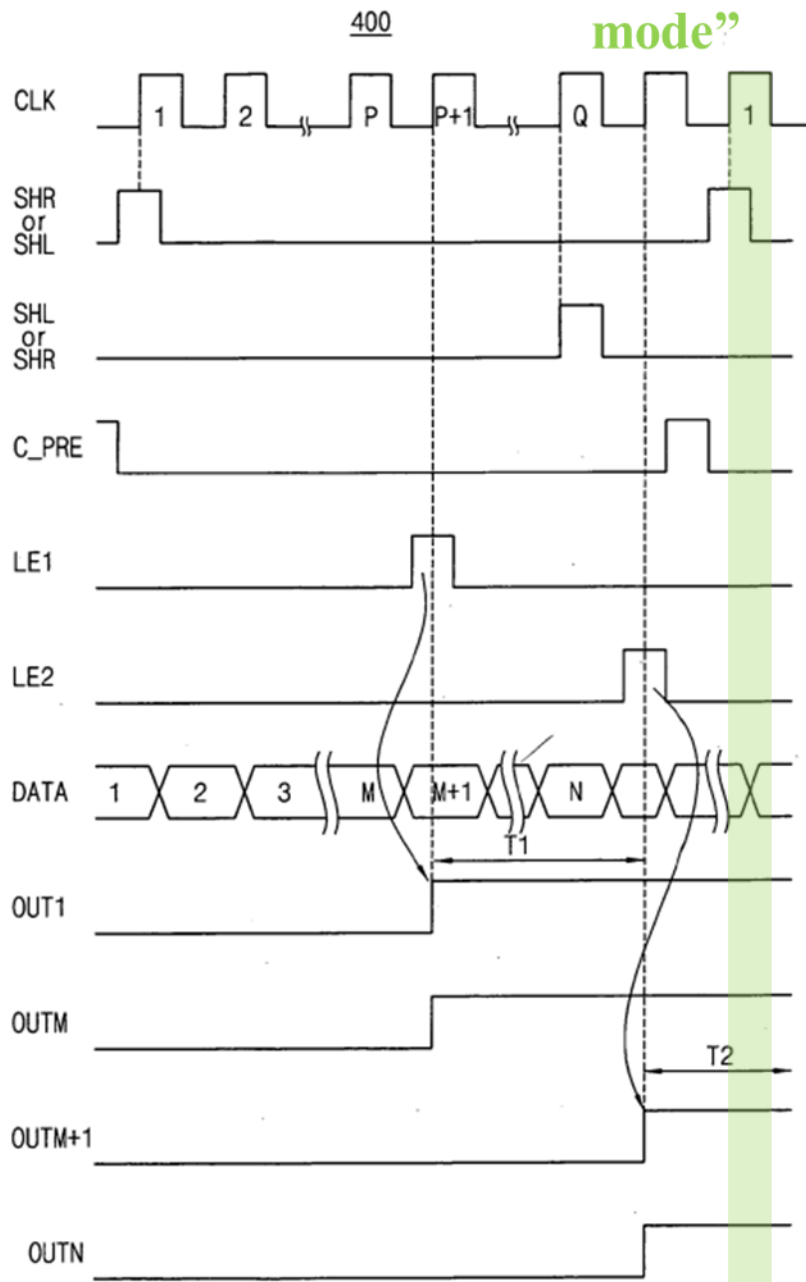
Baek, Fig. 5.



Baek, Fig. 3. Figure 4 discloses the current charge mode when the SR CLK signal turns on switches S1 and S2 while the other switches are turned off. Kattamis, ¶198.

FIG. 4

“current supply mode”

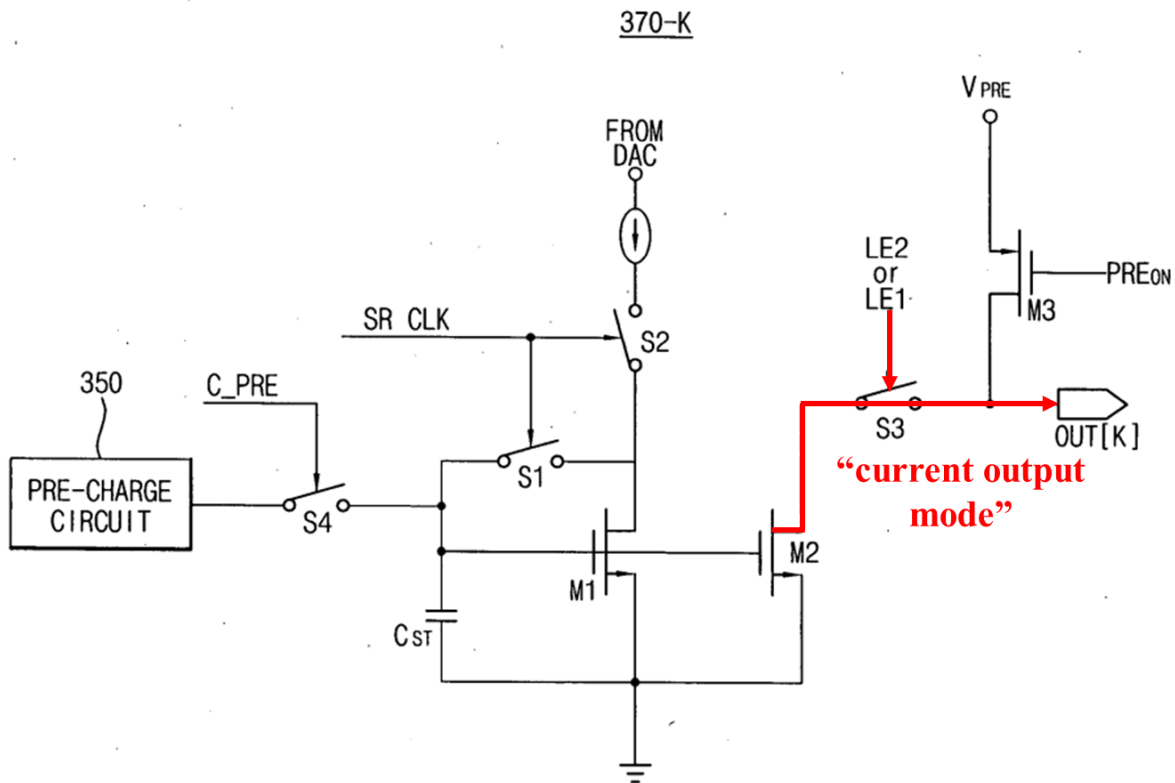


Baek, Fig. 4.

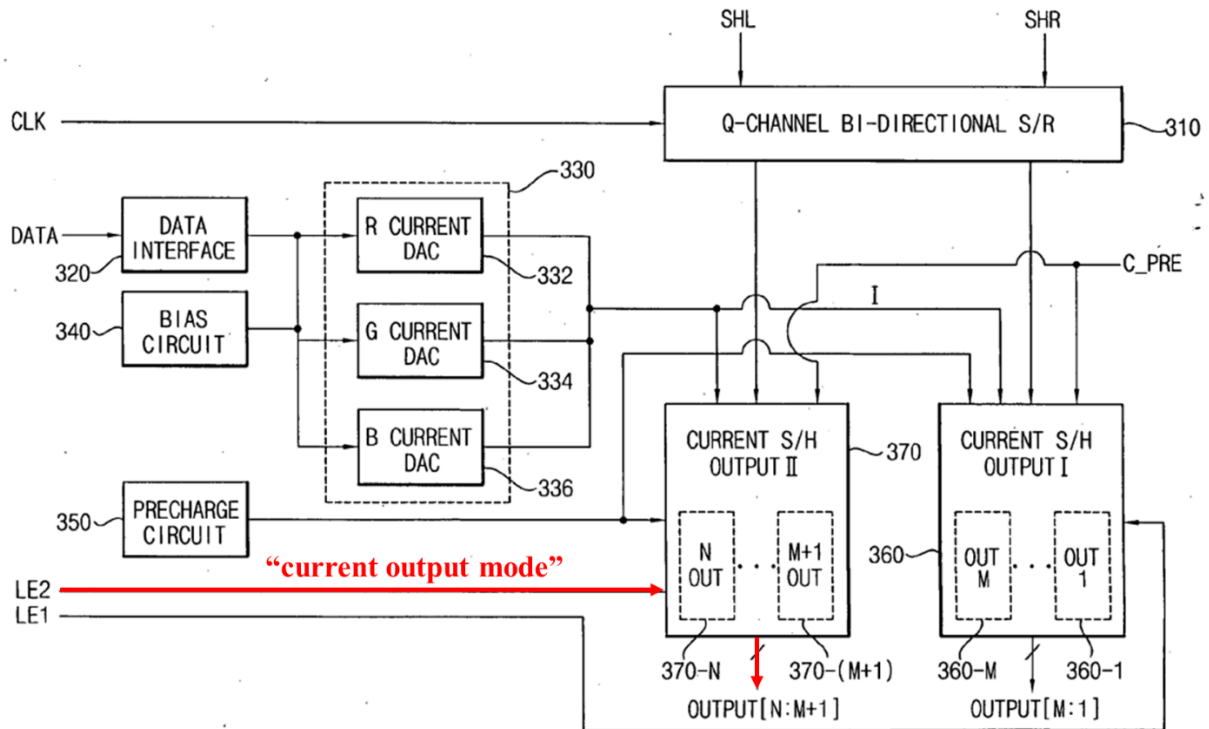
As also discussed in 1(d)(2), **Baek** discloses a current output mode (annotated red) where second transistor M2 “output[s] the analog gray-scale current to the

output terminal OUT[K] based on the charged analog gray-scale current.” Baek, [0058]. Current output circuit 370 operates in this mode when switches S1, S2, and S4 are turned off and switch S3 is turned on based on “the second latch enable signal LE2 [being] activated.” Baek, [0057]-[0058], [0062]. As shown in Figure 3, the LE2 signal is supplied to the “second sample/hold output circuit 370” such that each “current sample/hold circuit[] 370-(M+1) through 370-N” receives the LE2 signal and outputs current to the output terminal in the current output mode. Kattamis, ¶99.

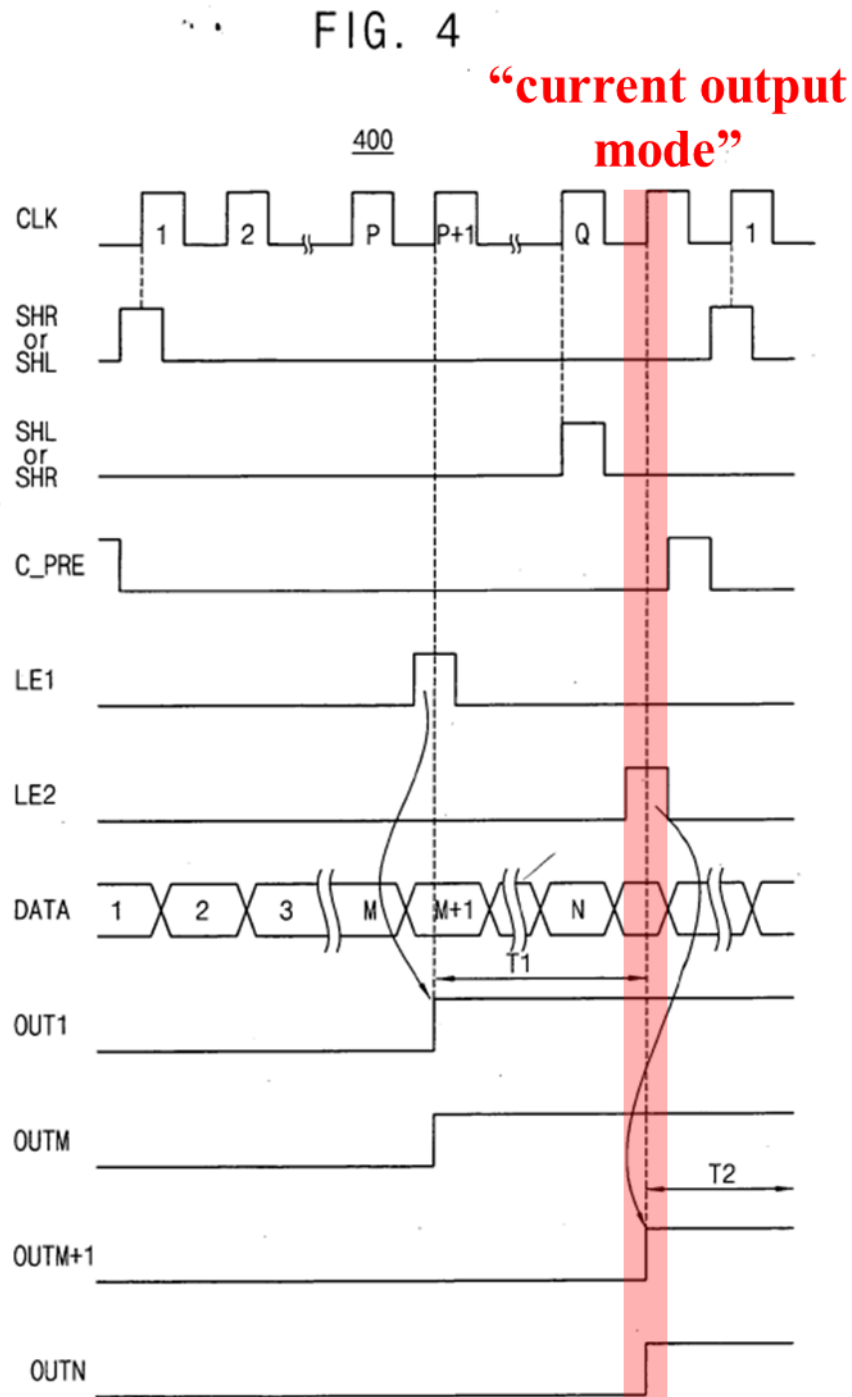
FIG. 5



Baek, Fig. 5.



Baek, Fig. 3. Figure 4 discloses the current output mode when the LE2 signal turns on switch S3 while the other switches are turned off. Kattamis, ¶100.



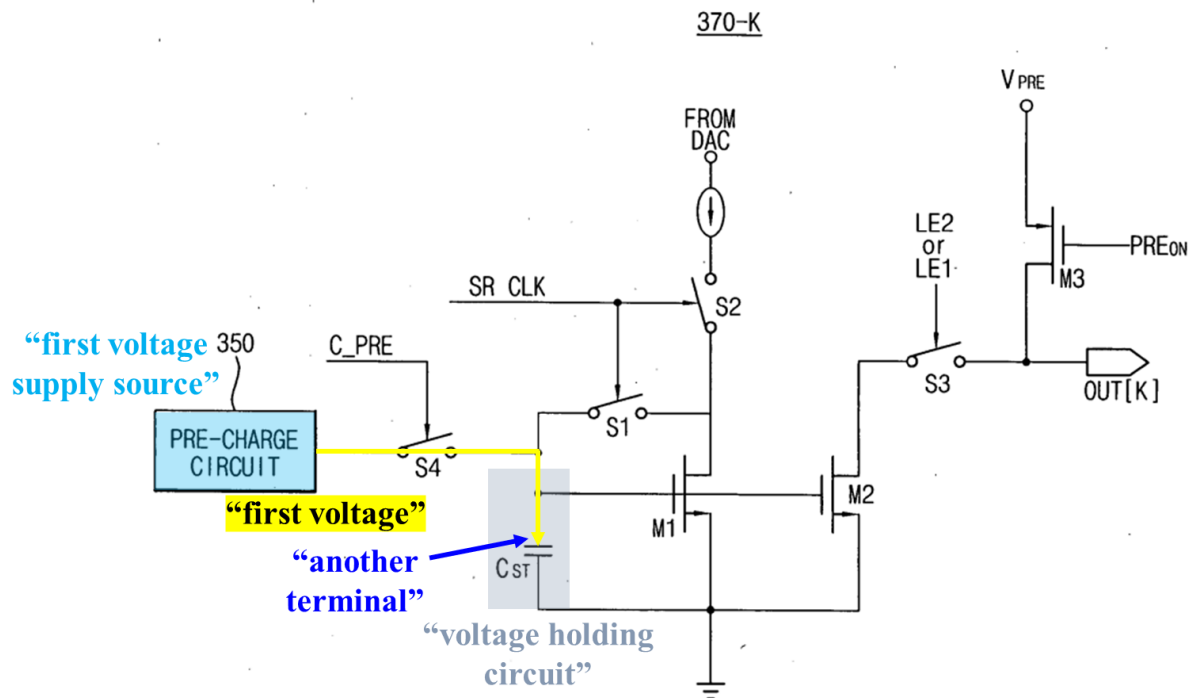
Baek, Fig. 4.

- viii. 1(f): “under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is

supplied to another terminal of said voltage holding circuit,”

Baek discloses under said voltage supply mode (see 1(e)), each of said current output circuits receives said first voltage from said first voltage supply source (e.g., each “current sample/hold output circuit 370” receives “pre-charge...voltage” from “pre-charge circuit 350”), and the first voltage is supplied to another terminal of said voltage holding circuit (e.g., “pre-charge...voltage” is supplied to terminal of “storage capacitor CST” via S4). Baek, [0055]-[0057], [0062], Figs. 3-5; Kattamis, ¶¶101-104. See 1(a), 1(d)(1)-1(e).

FIG. 5



Baek, Fig. 5.

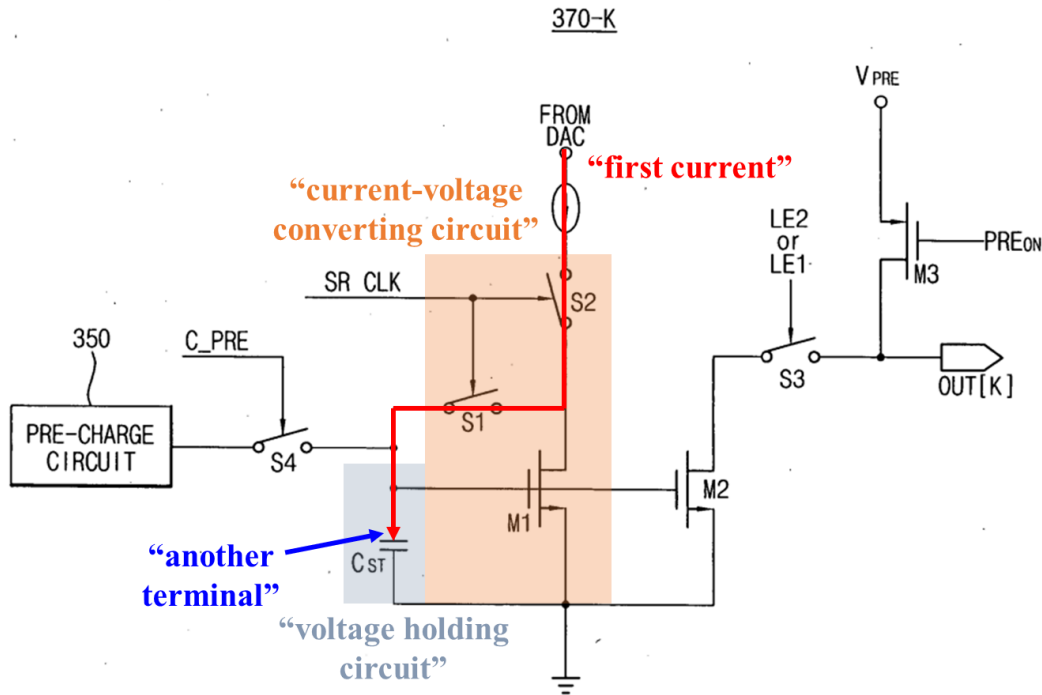
For example, as discussed in 1(d)(2)-1(e), **Baek** discloses that, during a pre-charge mode, “switch S4” is “turned on” and switches S1 and S2 are turned off such that pre-charge circuit 350 (annotated blue) “pre-charge[s] a voltage” (annotated yellow) “of the storage capacitor CST” (annotated gray) “to a voltage level slightly lower than a threshold voltage of the first transistor M1.” Baek, [0057], [0062]. Thus, the pre-charge voltage is supplied to the terminal (annotated dark blue) of the storage capacitor CST that is “coupled to the gate of the first transistor M1.” Baek, [0056].⁶ As discussed in 1(e) and in §IX.A.a, **Baek** discloses that each “current sample/hold circuit 370-k” of the second current sample/hold output circuit 370 receives the voltage from pre-charge circuit 350 when the C_PRE signal is supplied. Kattamis, ¶104.

- ix. **1(g): “under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and”**

⁶ This is consistent with the '047, which discloses, during “voltage supply mode M1,...the voltage holding capacitance element C1 is charged to a constant voltage (this corresponds to the first voltage, and will be referred to as a reference voltage hereinafter) that is supplied from the voltage supply source V1.” '047, 7:41-57. Kattamis, ¶104.

Baek discloses under said current supply mode (see 1(e)), each of said current output circuits receives said first current from said first current supply source (e.g., each “current sample/hold circuit 370” receives “an analog gray-scale current” from “current digital-to-analog conversion unit 330”), and generates a second voltage by said current-voltage converting circuit (e.g., voltage generated by “charg[ing] the analog gray-scale current” in storage capacitor CST), and the first current is supplied to said another terminal of said voltage holding circuit (e.g., “an analog gray-scale current” is supplied to terminal of “storage capacitor CST”). Baek, [0044], [0045], [0056]-[0057], Figs. 3-5; Kattamis, ¶¶105-109. See 1(b), 1(d)(1)-1(e).

FIG. 5

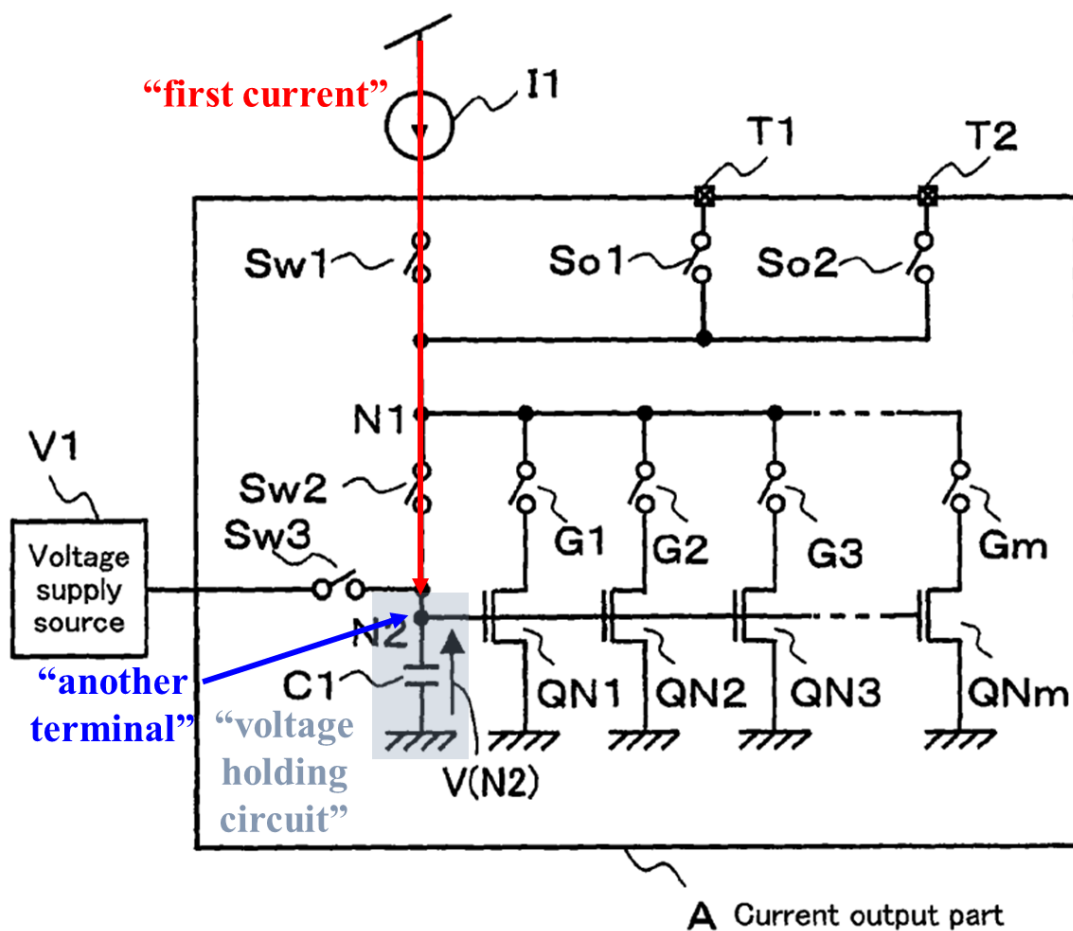


Baek, Fig. 5.

For example, as discussed in 1(e), **Baek** discloses switch S4 is turned off and switches S1 and S2 are “turned on” such that “storage capacitor CST” (annotated gray) “charges the analog gray-scale current” (annotated red) from “current digital-to-analog conversion unit 330” to produce a voltage at the terminal (annotated dark blue) of the capacitor CST coupled to the gate of transistor M1. Baek, [0056]-[0057]. As discussed in 1(e) and in §IX.A.a, **Baek** discloses that each “current sample/hold circuit 370-k” of the second current sample/hold output circuit 370 receives analog gray-scale current when the SR CLK signal is supplied. Kattamis, ¶108.

This is consistent with the description of these elements in the '047, where the first current (annotated red) is supplied to the second terminal (annotated dark blue) of the voltage holding capacitor (annotated gray) in a similar manner to **Baek**. '047, 8:1-15. Figure 1A of the '047 is annotated to show that a first electric current is supplied to the marked “another terminal” of the voltage holding capacitor. Kattamis, ¶109.

F I G. 1 A

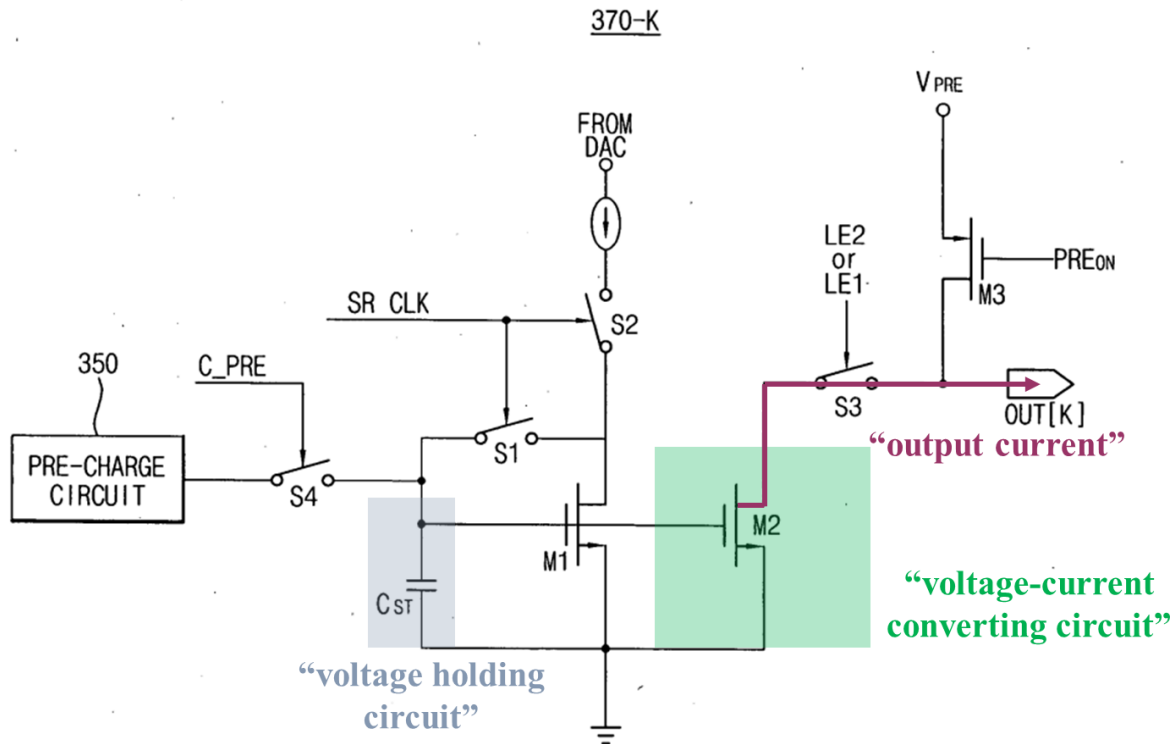


'047, Fig. 1A.

- x. **1(h): “under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit.”**

Baek discloses under said current output mode (see 1(e)), each of said current output circuits outputs an output current (e.g., each “current sample/hold circuit 370” “output[s] the analog gray-scale current”) according to said voltage held in said voltage holding circuit by said voltage-current converting circuit (e.g., “analog gray-scale current” output by transistor M2 is “based on the charged analog gray-scale current” held in “storage capacitor CST”). Baek, [0058], [0062], Figs. 3-5; Kattamis, ¶¶110-113. See 1(d)(1)-1(e).

FIG. 5



Baek, Fig. 5.

For example, as discussed in 1(e), **Baek** discloses a current output mode where second transistor M2 (annotated green) “output[s] the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current” (annotated purple). Baek, [0058]. Transistor M2 has “its gate coupled to the storage capacitor CST” (annotated gray) such that the “voltage of the storage capacitor CST” during the pre-charge mode (see 1(f)) and the “charged analog gray-scale current” held in storage capacitor CST, is converted to an output current, including “based on

the charged analog gray-scale current.” Baek, [0058], [0062]. As discussed in 1(e) and in §IX.A.a, **Baek** discloses that each “current sample/hold circuit 370-k” of the second current sample/hold output circuit 370 outputs the analog gray-scale current stored in the capacitor CST when latch signal LE2 is supplied. Baek, [0052]. Kattamis, ¶113.

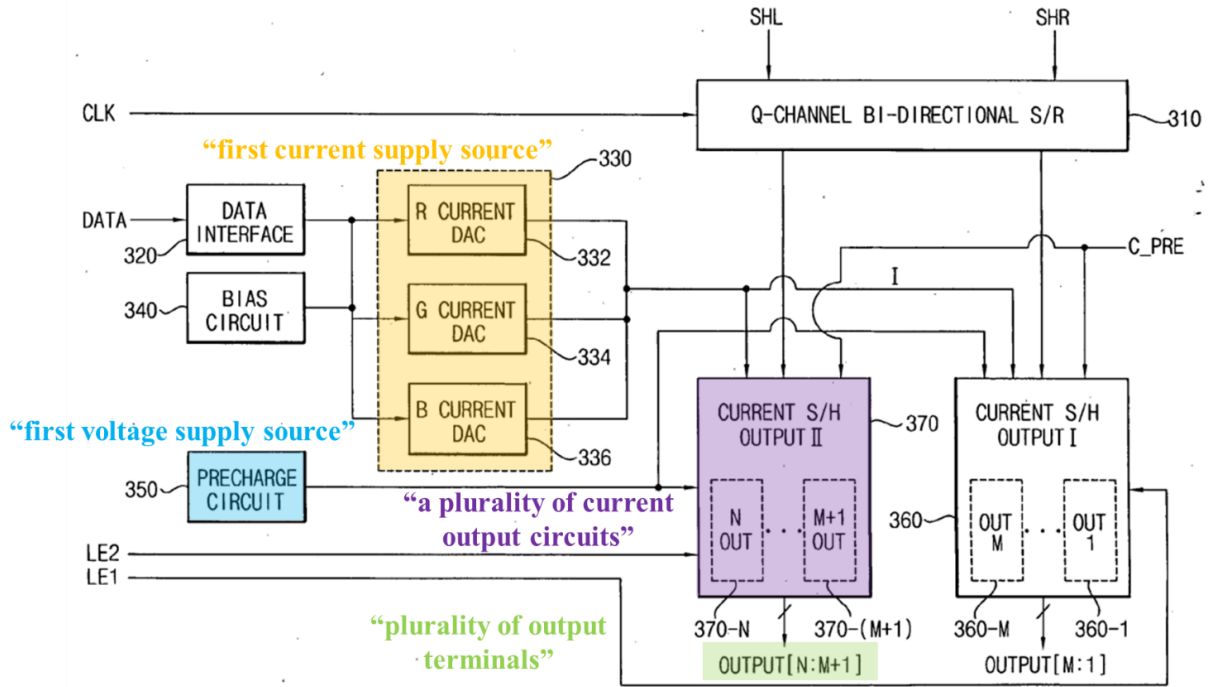
c. Claim 2

Claim 2 recites: “The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits, and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common.” Kattamis, ¶115.

Baek discloses and at minimum renders obvious the current driving device according to claim 1, as discussed above. Kattamis, ¶¶114-119.

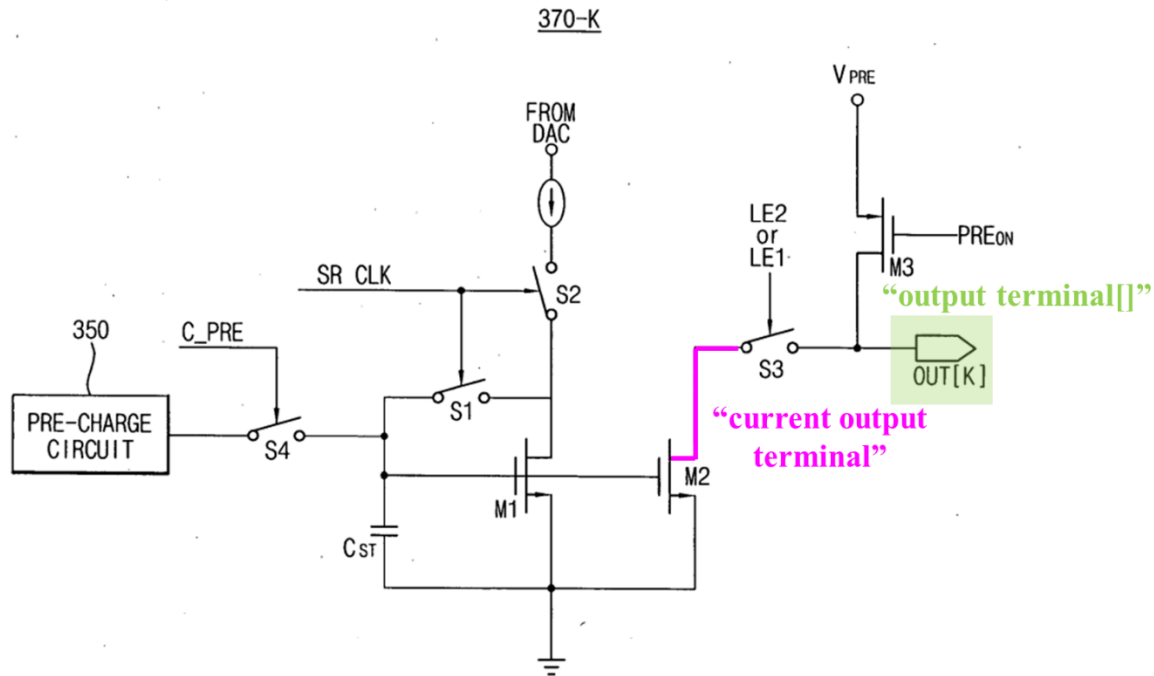
Baek further discloses each of said output terminals (see 1(c)) is connected to said current output terminals provided to said plurality of said current output circuits (e.g., each “output terminal OUT[K]” is connected to “drain [terminals] of the second transistor M2” in the “current sample/hold circuit[s]”), and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common (e.g., each “current sample/hold circuit 370-k” is connected in parallel to “current

digital-to-analog conversion unit 330” and “pre-charge circuit 350”). Baek, [0038], [0039], [0055], [0058], Figs. 3, 5; Kattamis, ¶¶117-119. See 1(a)-1(d)(2).



Baek, Fig. 3.

FIG. 5



Baek, Fig. 5.

For example, as discussed in 1(c) and 1(d)(1), **Baek** discloses each output terminal “OUT[K]” (annotated green) is connected to the drain terminals (annotated pink) of “the second transistor M2” in the current sample/hold circuits. Baek, [0058]. **Baek** further discloses that the current sample/hold circuits within the second current sample/hold output circuit 370 and DAC 330 share a common node. Each current sample/hold circuit 370-k and the pre-charge circuit 350 share a common node. Current sample/hold output circuit 370 is also grounded, because the individual current sample/hold circuits 370-k within the current sample/hold output

circuit 370 are grounded. A POSITA would have understood or at least found obvious that DAC 330 and pre-charge circuit 350 are also grounded because power supplies, including voltage and current sources, are grounded to form a complete loop. Thus, each of the current sample/hold circuits 370-k is connected in parallel to the pre-charge circuit 350 and DAC 330 used in common. Kattamis, ¶119.

d. Claim 3

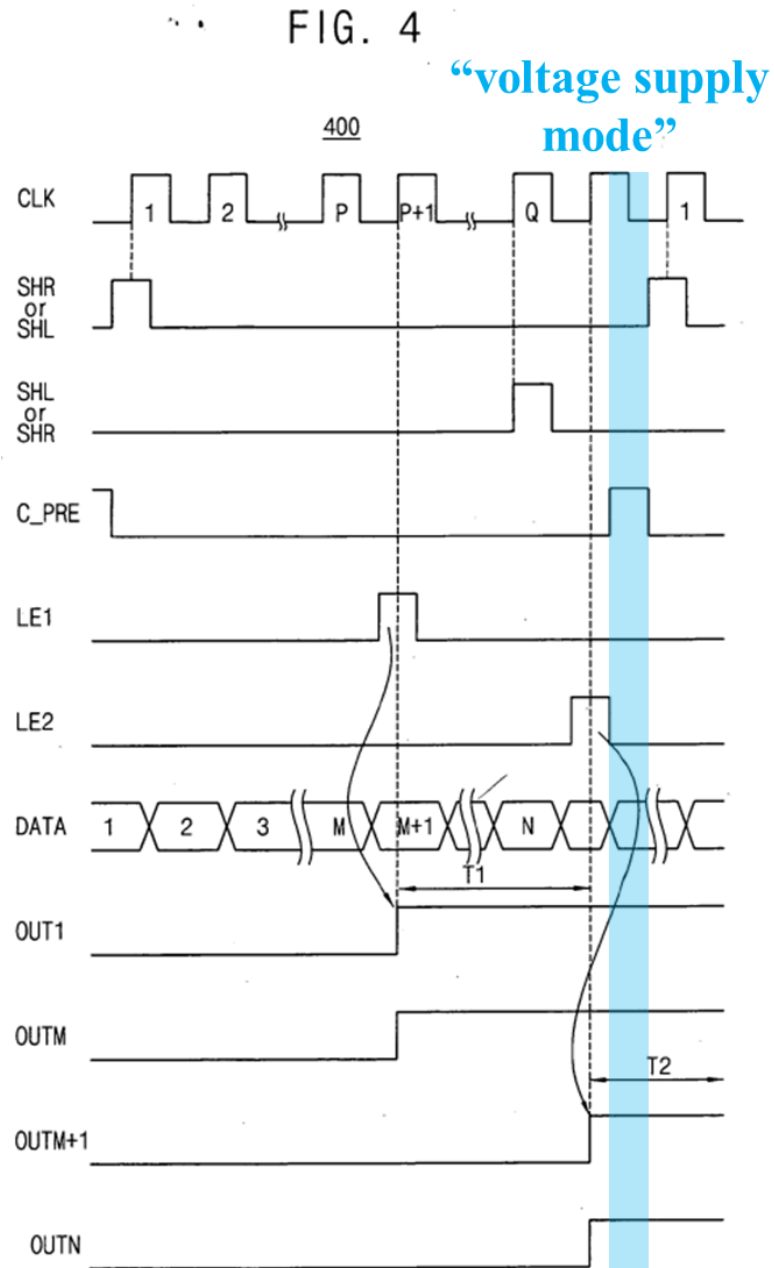
Claim 3 recites: “The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode.” Kattamis, ¶121.

Baek discloses and at minimum renders obvious the current driving device according to claim 1, as discussed above. Kattamis, ¶¶120-125.

Baek further discloses in each of said current output circuits (see 1(d)(1)), said current-voltage converting circuit (see 1(d)(2)) is actuated (e.g., “switch S4 [is] turned on”) under said voltage supply mode (see 1(f)). Baek, [0052], [0056], [0057], [0062], Figs. 3-5; Kattamis, ¶123. See 1(d)(1)-1(f).

For example, as discussed in 1(e)-1(f), **Baek** operates under voltage supply mode when a control signal C_PRE turns on switch S4, causing the circuit to “pre-charge a voltage of the storage capacitor CST,” which is “coupled to the gate of the first transistor M1.” Baek, [0056], [0062]. A POSITA would have understood or at least found obvious that capacitor CST and transistor M1 are actuated in each

“current sample/hold output circuit 370” during a pre-charge mode when the C_PRE signal switches S4 on. Baek, [0052]. Figure 4 of **Baek** shown below discloses that the current output circuits are actuated in a pre-charge mode (annotated blue). Kattamis, ¶125.



Baek, Fig. 4.

e. Claim 4

Claim 4 recites: “The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode.” Kattamis, ¶127.

Baek discloses and at minimum renders obvious the current driving device according to claim 1, as discussed above. Kattamis, ¶¶126-131.

Baek further discloses each of said current output circuits (see 1(d)(1)) is configured to stop said current-voltage converting circuit under said voltage supply mode (*e.g.*, during “pre-charge” mode, “first switch S1 and the second switch S2 [are] turned off”). Baek, [0056]-[0057], [0062], Figs. 3-5; Kattamis, ¶¶129-131. *See* 1(d)(1)-1(g).

For example, as discussed in 1(e)-1(f), **Baek** discloses the switches S1 and S2 are turned off during a pre-charge mode such that the storage capacitor CST is not charged with “the analog gray-scale current.” Baek, [0056]-[0057], [0062]. A POSITA would have understood that without a supplied current from the current source, the transistor M1 does not convert the source’s current to a voltage such that

the current-voltage converting function stops and the pre-charge circuit 350 supplies “pre-charge...voltage” to storage capacitor CST.⁷ Baek, [0062]. Kattamis, ¶131.

f. Claim 9

Claim 9 recites: “A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device.” Kattamis, ¶133.

Baek discloses and at minimum renders obvious the current driving device according to claim 1, as discussed above. Kattamis, ¶¶132-135.

Baek discloses a current-driving-type display device (*e.g.*, “current-driven active matrix type OLED display devices”), **comprising said current driving device according to claim 1** (*see* §IX.A.b) **mounted thereon so as to be driven by said current driving device** (*e.g.*, “display driver circuit” “used to drive a display panel...using a smaller current”). Baek, [0003], [0062], [0064], [0066]; Kattamis, ¶¶134-135.

⁷ This is consistent with the ’047, which discloses “each of the current output parts comprises a function of stopping the current-voltage converting function under the voltage supply mode” such that “all the electric currents supplied from the first voltage supply part [V1] can be utilized for charging the voltage holding part.” ’047, 4:25-31. Kattamis, ¶131.

For example, **Baek** discloses “a display driver circuit for a flat display panel.” **Baek**, [0003]. **Baek** further discloses that “the display driver circuit according to example embodiments of the present invention may be applicable to Organic Light Emitting Diode (OLED) display devices, for example, current-driven active matrix type OLED display devices.” *Id.*, [0064]. A POSITA would have understood, and at minimum it would have been obvious, to mount the display driver circuit on the display device, as opposed to elsewhere, to advantageously “reduce a charge time” and “perform a sampling operation faster” while “more accurately output[ting] output signals to corresponding channels.” **Baek**, [0062], [0066]. Indeed, such implementations were well-known in the art. *See, e.g.*, Ex. 1012 (“Nohtomi”), [0002]-[0004] (discussing “a driver circuit for driving the liquid crystal panel” is “installed” on a “dot matrix type liquid crystal panel”). Kattamis, ¶135.

B. GROUND 3: BAEK IN VIEW OF DATE

a. Claim 5

Claim 5 requires the “current driving device according to claim 1, further comprising a second current supply source for supplying a second electric current that is proportional to said first electric current; and a second current-voltage converting circuit for generating said first voltage by receiving said second electric current, wherein said first voltage supply source controls supplies of said first voltage generated by said second current-voltage converting circuit to said current

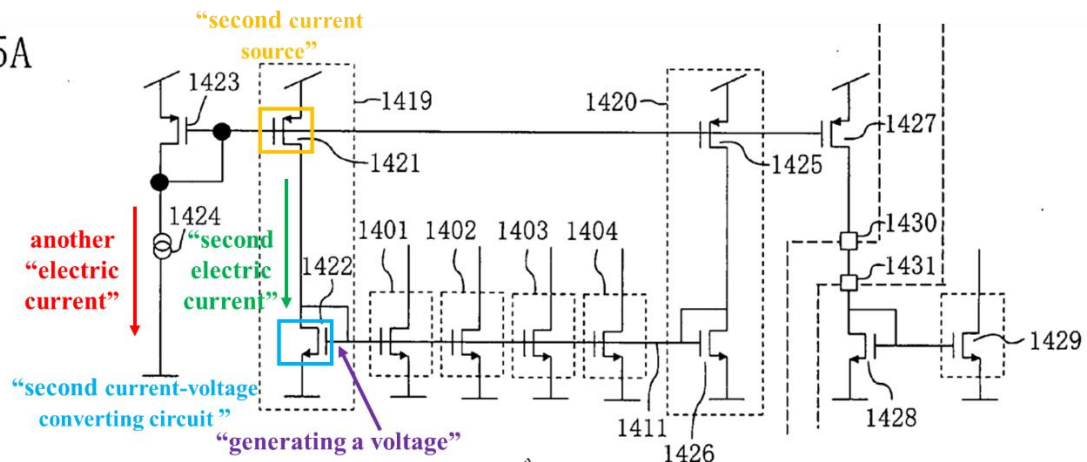
output circuits.” As discussed above in §IX.A.b, Claim 1 is disclosed and at minimum rendered obvious by **Baek**. As discussed further below, Claim 5 is rendered obvious when **Date’s** teachings of a second current supply source and second current-voltage converting circuit are applied to **Baek’s** driver circuit. Kattamis, ¶¶136-138.

Baek discloses the first electric current (*e.g.*, “an analog gray-scale current”), **the first voltage** (*e.g.*, “voltage” from “pre-charge circuit 350”), **the first voltage supply source** (*e.g.*, “pre-charge circuit 350”), **and the current output circuits** (*e.g.*, “current sample/hold circuits 370-(M+1) through 370-N”). See 1(a)-1(b), 1(d). Kattamis, ¶¶139-140.

Date discloses a second current supply source (*e.g.*, “p-transistor 1421”) **for supplying a second electric current that is proportional to an electric current** (*e.g.*, “a current...flows in the p-transistor 1421” based on its “gate-size ratio between...p-transistor 1423 and the p-transistor 1421,” the former of which “draws a current” from “current source 1424”) **and a second current-voltage converting circuit** (*e.g.*, “n-transistor 1422” in addition to “output n-transistors 1405 through 1410”) **for generating a voltage** (*e.g.*, “a gate voltage...generated at the gate of the n-transistor 1422”) **by receiving said second electric current** (*e.g.*, “receiv[ing] a current flowing in the p-transistor 1421”), **wherein a voltage generated by said second current-voltage converting circuit is supplied to said**

current output circuits (*e.g.*, “a gate voltage... [on] the n-transistor 1422” is “supplied to the gates of the output n-transistors” in “current mode D/A converters 1401 through 1404”). Date, [0008]-[0012], Fig. 25A; Kattamis, ¶¶141-150.

FIG. 25A



Date, Fig. 25A. Kattamis, ¶141.

For example, **Date** discloses a “current driver[] suitable as [a] display driver[] for,” for example, “organic EL (electro luminescence) panels, LED (light emitting diode) panels and the like.” Date, [0002]. The driver includes a first “current source 1424” that “draws a current which has been set at an arbitrary current value” in “bias p-transistor 1423.” Date, [0008]-[0009]. The current driver further includes a “current mirror” of “bias p-transistor 1423 and the p-transistor 1421” such that “a current according to the gate-size ratio between the p-transistor 1423 and the p-transistor 1421 flows in the p-transistor 1421.” Date, [0009]. A POSITA would

have understood or at least found it obvious that the p-transistor 1423 is a second current source.⁸ Kattamis, ¶142.

Date further discloses an n-transistor 1422 “receives a current flowing in the p-transistor 1421” and “a gate voltage (bias voltage) according to the current input to the n-transistor 1422 is generated at the gate of the n-transistor 1422” and “supplied to the gates of the output n-transistors 1405 through 1410” via “gate line 1411.” **Date**, [0010]-[0012]. A POSITA would have understood or at least found it obvious that the n-transistor 1422 is a second current-voltage converting circuit.⁹ Kattamis, ¶143.

Like **Baek**, **Date** is in the same field as the '047—which includes driver circuits—and is reasonably pertinent to the problems addressed by the '047—e.g., providing sufficient current to lighting elements of display panels. *E.g.*, '047,

⁸ This is consistent with the '047, which discloses “a reference current supply transistor QP2 that constitutes a second current supply part.” '047, 10:31-33. Kattamis, ¶142.

⁹ This is consistent with the '047, which discloses “current-voltage converting transistor[] QNx” in addition to “Nch transistors QN1-QNm” '047, 8:1-15, 10:34-35. Kattamis, ¶143.

Abstract, 3:18-22, 5:20-25; Baek, [0003], [0005], [0063]; Date, [0002], [0019]-[0020]; Kattamis, ¶¶144-146.

In implementing **Date's** teachings in **Baek's** driver circuit, a POSITA would have understood that, for each current sample/hold circuit 370, the analog gray-scale current from the “current digital-to-analog conversion unit 330” is used as a reference current, mirrored in a p-transistor, and supplied to a corresponding n-transistor. The voltage generated by the n-transistors, as taught by **Date**, would be used as the pre-charge circuit 350, as taught by **Baek**. Such an implementation would have advantageously simplified the circuitry used to drive the LEDs of the display panel, as it would have used the “analog gray-scale current” from “current digital-to-analog conversion unit 330” to create the voltage supplied by the pre-charge circuit 350. Kattamis, ¶147.

Baek does not disclose how the pre-charge circuit 350 is implemented. A POSITA would have understood that one way to implement such circuitry is using the “gate voltage (bias voltage)...generated at the gate of the n-transistor 1422” as taught by **Date**. Date, [0010]-[0012]. Indeed, **Date** discloses that this “gate voltage” is “supplied to the gates of the output n-transistors 1405 through 1410” via “gate line 1411,” and is therefore consistent with **Baek's** pre-charge circuit teachings, whereby the pre-charge circuit supplies voltage to the gates of transistors M1 and M2 to

output current. Date, [0010]-[0012]; Baek, [0036], [0054], [0058], [0063]. Kattamis, ¶148.

Further, a POSITA would have been motivated to use **Date's** bias circuit teachings in implementing **Baek's** driver circuit to advantageously enhance reliability of the circuit by providing a constant voltage based on a constant current source. For example, a POSITA would have understood that the current mirror comprising the two p-transistors taught in **Date** was well-known in the art and provided many advantages, including that the p-transistor 1421 would provide a constant current irrespective of the load applied. *See e.g.*, Ex. 1013 ("Schaffer"), [0005], [0006]; Ex. 1014 ("Chang"), [0020], [0025]. A POSITA would have understood that the constant current provided by p-transistor 1421 to n-transistor 1422 would generate a constant gate voltage based on the constant current. Therefore, the voltage of the gate of the n-transistor 1422 would be constant irrespective of the load, including the load comprising the capacitor CST and transistors M1 and M2 as taught by **Baek**. Kattamis, ¶149.

A POSITA would have had a reasonable expectation of success in applying **Date's** teachings in implementing **Baek's** driver circuit because it is a straightforward use of **Date** for its intended purpose that would have yielded the predictable results of supplying a voltage by using a reference current. Kattamis, ¶150. Indeed, both **Baek** and **Date** disclose using transistors to perform various

current and voltage supplying functions. See Baek, [0055]-[0056]; Date, [0007]-[0010]. This would have been a straightforward application of **Date's** teachings in a manner that advantageously improves **Baek's** driver circuit. Kattamis, ¶150.

b. Claim 6

Claim 6 requires “The current driving device according to claim 5, wherein said second current-voltage converting circuit comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node.” Kattamis, ¶152.

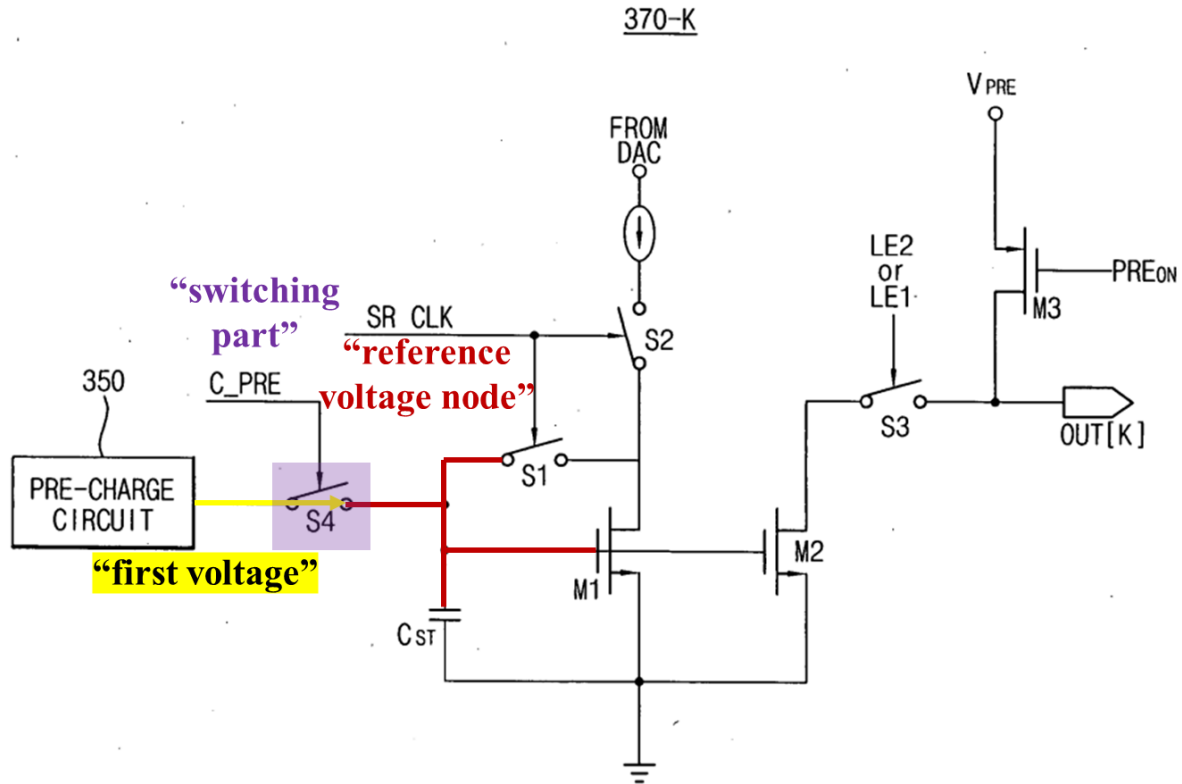
Date discloses the second current-voltage converting circuit. See (5) (§IX.B.a). Kattamis, ¶¶151-153.

Baek discloses a switching part for short-circuiting a node (*e.g.*, “switch S4” is “turned on”) **at which said first voltage** (*e.g.*, “pre-charge...voltage”) **emerges to a reference voltage node** (*e.g.*, supplied to node comprising transistor M1, capacitor CST, and switches S1 and S4). Baek, [0057], [0062], Fig. 5; Kattamis, ¶¶154-158.

As discussed in 1(d)(2)-1(f), **Baek** discloses that, during a pre-charge mode, “switch S4” is “turned on” (annotated purple) and switches S1, S2 and S3 are turned off such that pre-charge circuit 350 “pre-charge[s] a voltage” (annotated yellow) “of the storage capacitor CST” “to a voltage level slightly lower than a threshold voltage of the first transistor M1.” Baek, [0057], [0062]. A POSITA would have understood

or at least found it obvious that turning on a switch short-circuits a node such that the voltages on both sides of the switch become the same. Therefore, a POSITA would have understood that switch S4 turning on short-circuits a node such that the pre-charge voltage emerges at another node (annotated dark red) that includes the connections between transistor M1's gate, capacitor CST, and switches S1 and S4. This is consistent with the '047, which discloses switches G1-Gm and Sw2 are turned on such that "drains and gates of Nch transistors QN1-QNm are short-circuited to receive electric currents from a reference current source I1." '047, 1:40-47. Kattamis, ¶¶155-156.

FIG. 5



Baek, Fig. 5.

In applying **Date**'s second current-voltage converting circuit teachings to **Baek**'s driver circuit (as discussed in (5), §IX.B.a), switch S4 would short-circuit the node containing the gate voltage (e.g., n-transistor 1422 (as taught by **Date**)) so that it emerges at the node (annotated dark red) that includes the connections between transistor M1's gate, capacitor CST, and switches S1 and S4. A POSITA would have found it obvious to apply **Date**'s concepts in implementing **Baek**'s driver circuit as discussed in (5), §IX.B.a. Kattamis, ¶157.

To the extent it is argued that the recited “a reference voltage node” must be different from the node comprising the recited “a terminal being connected to a reference voltage” (from 1(d)(2)), the connection to S4 is different than the connection to M1 discussed in 1(d)(2). Kattamis, ¶158.

C. GROUND 4: BAEK IN VIEW OF INOMOTO

a. Claim 7

Claim 7 requires the “current driving device according to claim 1, further comprising a second voltage supply source with a larger voltage supply capacity than that of said first voltage supply source, wherein the use of said first voltage supply source and the use of said second voltage supply source are switched in accordance with the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits.” As discussed above in §IX.A.b, Claim 1 is disclosed and at minimum rendered obvious by **Baek**. Kattamis, ¶¶160-161.

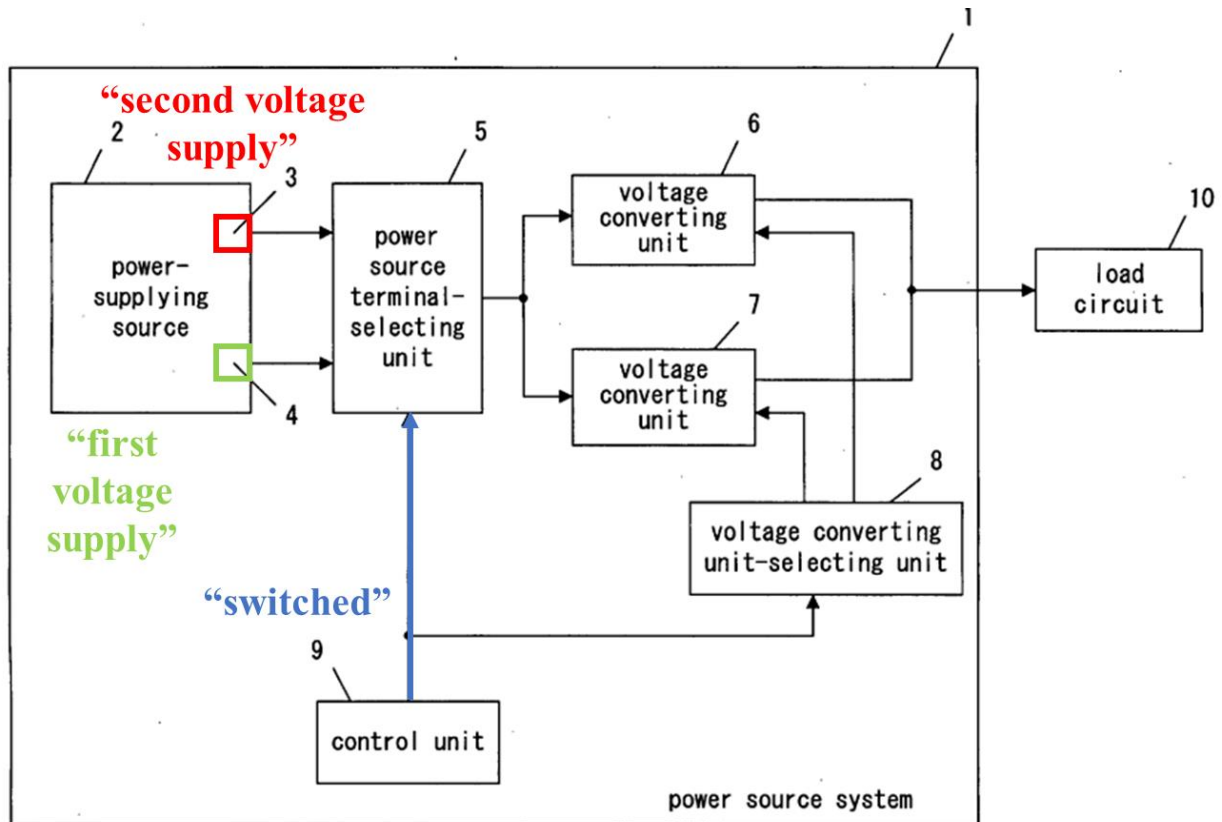
Baek discloses the first voltage supply source (*e.g.*, “pre-charge circuit 350” supplying “voltage”) **and the number of said current output circuits** (*e.g.*, “current sample/hold circuits 370-(M+1) through 370-N”) **that operate in said voltage supply mode** (*e.g.*, “pre-charge” mode to “pre-charge a voltage of the storage capacitor CST”) **among said plurality of current output circuits** (*e.g.*, “current sample/hold circuits 370-(M+1) through 370-N”). *See* 1(a), 1(d)(1), 1(e).

Baek discloses that there are M+1 to N number of current sample/hold circuits. Baek, [0038]-[0039], [0047]-[0049], [0052]; Kattamis, ¶¶162-163.

Inomoto discloses a second voltage supply source (*e.g.*, “power source terminal 3” of “power-supplying source 2”) **with a larger voltage supply capacity** (*e.g.*, “higher...output voltage”) **than that of said first voltage supply source** (*e.g.*, “power source terminal 4”), **wherein the use of a first voltage supply source and the use of said second voltage supply source are switched** (*e.g.*, “selection control signal” selects which voltage to apply) **in accordance with the number of circuits** (*e.g.*, “based on...a quantity of loads...of the load circuit 10”). Inomoto, 1:6-7, 3:3-18, 13:18-14:1, 16:17-20, 17:12-18; Kattamis, ¶¶164-173.

Inomoto discloses a “power source system” that supplies “electrical power” to, for example, “a display panel” to reduce “malfunction[s]” and “wanted power consumption.” Inomoto, 1:6-7, 3:3-18, 13:18-14:1. The system “power-supplying source 2” that includes a “power source terminal 3” that is “higher in output voltage” than a “power source terminal 4.” Inomoto, 13:18-19, 13:27-14:1. Terminal 3 is “connected to the head of the serially interconnected internal power source cells 14” while terminal 4 is only connected at an “intermediate” point, thus receiving less voltage from the power source cells. Inomoto, 13:22-27. A “control unit 9” “selects either one of the power source terminals” using a “selection control signal” that is

“generated based on” a “quantity of loads” active on “the load circuit 10.” Inomoto, 16:17-20, 17:12-18; Kattamis, ¶165.



Inomoto, Fig. 1.

Like **Baek**, **Inomoto** is in the same field as the '047—which includes driver circuits—and is reasonably pertinent to the problems addressed by the '047—e.g., providing sufficient current to lighting elements of display panels. *E.g.*, '047, Abstract, 3:18-22, 5:20-25; Baek, [0003], [0005], [0063]; Inomoto, 1:6-7, 1:15-20, 1:26-2:8, 3:3-27, 13:2-5, 13:18-14:1, 16:17-20, 17:12-18. Kattamis, ¶¶166-168.

A POSITA would have been motivated to apply **Inomoto's** two voltage supplies teachings to **Baek's** driver device, as **Inomoto** provides implementation

details regarding how **Baek's** pre-charge circuit supplies a voltage during a pre-charge mode. **Baek** does not disclose the details of how the pre-charge circuit supplies voltage, and a POSITA would have turned to **Inomoto's** teachings, which provide this known way of using a selectable voltage supply based on the number of current output circuits drawing current. Kattamis, ¶169.

Further, a POSITA would have been motivated to apply **Inomoto's** two voltage supplies teachings in implementing **Baek's** driver device to advantageously enhance the reliability and reduce unwanted power consumption. For example, **Inomoto** teaches “increased consumption current in the load circuit...results in a drop in voltage, thereby reducing the output voltage of the power source terminal,” causing “malfunctions.” Inomoto, 3:3-8. **Inomoto** further teaches providing “a higher voltage...to the load circuit” that “requires a smaller consumption current” causes “unwanted power consumption.” Inomoto, 3:9-18. A POSITA would have been motivated to apply **Inomoto's** variable power supply teachings in implementing **Baek's** driver device to advantageously provide flexibility in the voltage supplied during a pre-charge mode based on the number of sample/hold circuits applied at the load, such that a proper voltage is applied based on number of sample/hold circuits needing the capacitor CST charged as taught by **Baek**. For example, **Baek** discloses that the “first sample/hold output circuit 360...include[s] current sample/hold circuits 360-1 through 360-M” and “second sample/hold output

circuit 370...include[s] current sample/hold circuits 370-(M+1) through 370-N.” Baek, [0038]-[0039]. The “output process” for the first circuit 360 and second circuit 370 “may be alternately performed” such that there are two different groups of outputs (Baek, [0052]), and a POSITA would have been motivated to switch between voltage supplies based on the corresponding number of current output circuits used by the first circuit 360 or second circuit 370. Kattamis, ¶170.

For example, a POSITA would have recognized the benefits of applying **Inomoto’s** teachings of using selectable voltage supplies to implement **Baek’s** pre-charge circuit such that it supplies a first voltage when a smaller number of current output circuits are selected to advantageously reduce unwanted power consumption by using a second, larger voltage supply. Further, a POSITA would have recognized the benefits of applying **Inomoto’s** teachings of using selectable voltage supplies to implement **Baek’s** pre-charge circuit such that it supplies a second, larger voltage when a larger number of current output circuits are selected to advantageously prevent malfunctions by a voltage drop from too many sample/hold circuits as loads to the pre-charge circuit. Kattamis, ¶171.

A POSITA would have had a reasonable expectation of success in applying **Inomoto’s** teachings in implementing **Baek’s** driver circuit because it is a straightforward use of **Inomoto** for its intended purpose that would have yielded the predictable results of switching between two voltage supplies. Kattamis, ¶172.

Indeed, both **Baek** and **Inomoto** disclose voltage supplies. See Baek, [0036], [0062]-[0063]; Inomoto, 13:18-27, 13:27-14:1. This would have been a straightforward application of **Inomoto's** teachings in a manner that advantageously improves **Baek's** driver circuit. Kattamis, ¶172.

In implementing **Inomoto's** two voltage supplies teachings in **Baek**, a POSITA would have understood or at least found obvious that another pre-charge circuit is supplied and switched to when there are many current output circuits drawing current. Kattamis, ¶173.

b. Claim 8

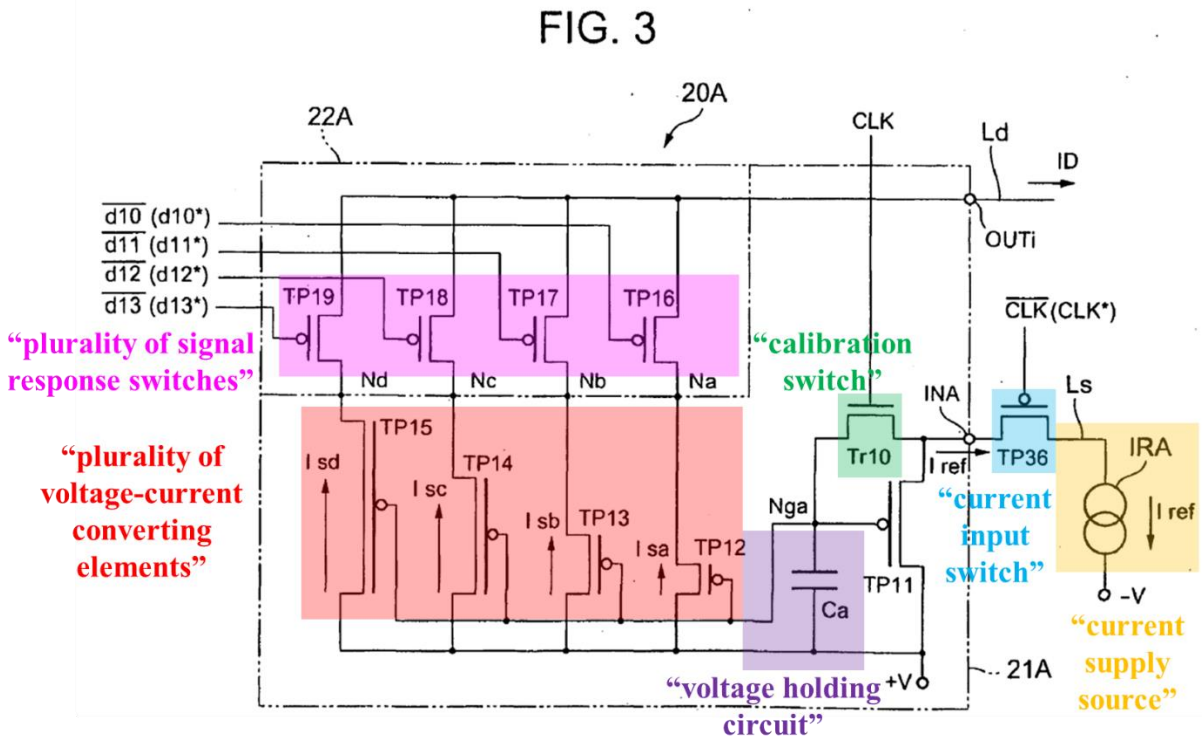
Claim 8 requires the “current driving device according to claim 1, wherein said first voltage supply source is configured to change its voltage supply capacity in accordance with the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits.” As discussed above in §IX.A.b, Claim 1 is disclosed and at minimum rendered obvious by **Baek**. Claim 8 is met for the same reasons as claim 7. While claim 7 recites switching between two voltage supply sources depending on the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits, claim 8 more broadly recites changing the voltage supply capacity in accordance with that number. Kattamis, ¶¶174-175.

D. GROUND 5: SASAKI

As discussed below, Claim 10 is rendered obvious by **Sasaki**. In addition to §IX.D.a, the following identifies example disclosures that each render obvious Claim 10. Kattamis, ¶¶176-226.

a. Overview of Sasaki

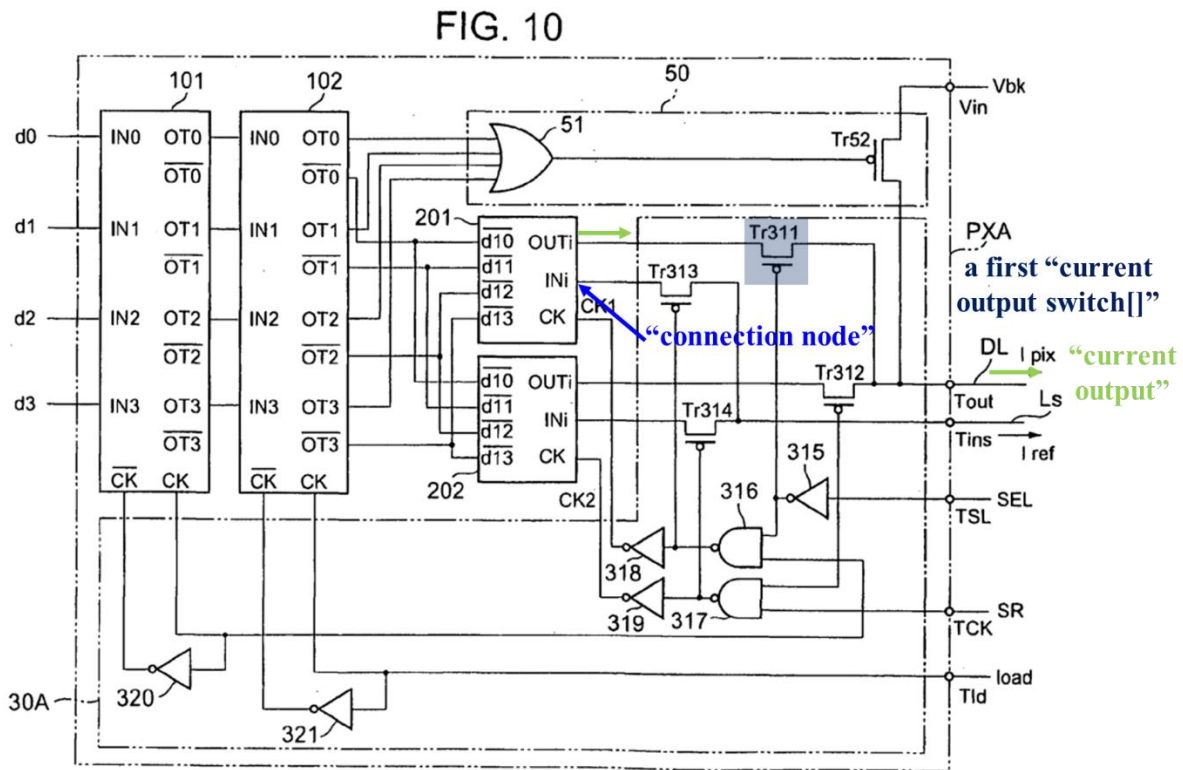
Sasaki discloses a “current generation supply circuit” that “drive[s]” a “display device.” Sasaki, [0003]. The circuit includes a “**current supply source control transistor TP36**” that “switch[es] ‘ON/OFF’” to connect and disconnect a “**constant current generation source IRA**” that “supplie[s]” a “reference current Iref.” Sasaki, [0062]-[0064]. A “**refresh control transistor Tr10**” causes “the reference current **Iref** [to] flow[]” to “charge” **capacitor Ca**. Sasaki, [0063], [0071], [0077], [0138]. When voltage is stored in **capacitor Ca**, the **module current transistors TP12-TP15** are turned on and generate “module currents Isa~Isd...relative to the constant reference current Iref” based on the reference voltage stored in capacitor Ca. Sasaki, [0066]-[0068]. **Switching transistors TP16~TP19** are “connected to each of the module current transistors TP12~TP15” and turn “ON” or “OFF” to supply the “load drive currents ID” comprising “composite value of the[] module currents” to the loads based on “signals d10*~d13*.” Sasaki, [0065], [0069]-[0070], [0152]. The load drive current flow “toward the current output contact OUTi via the drive current supply line Ld.” Sasaki, [0069]. Kattamis, ¶177.



Sasaki, Fig. 3.

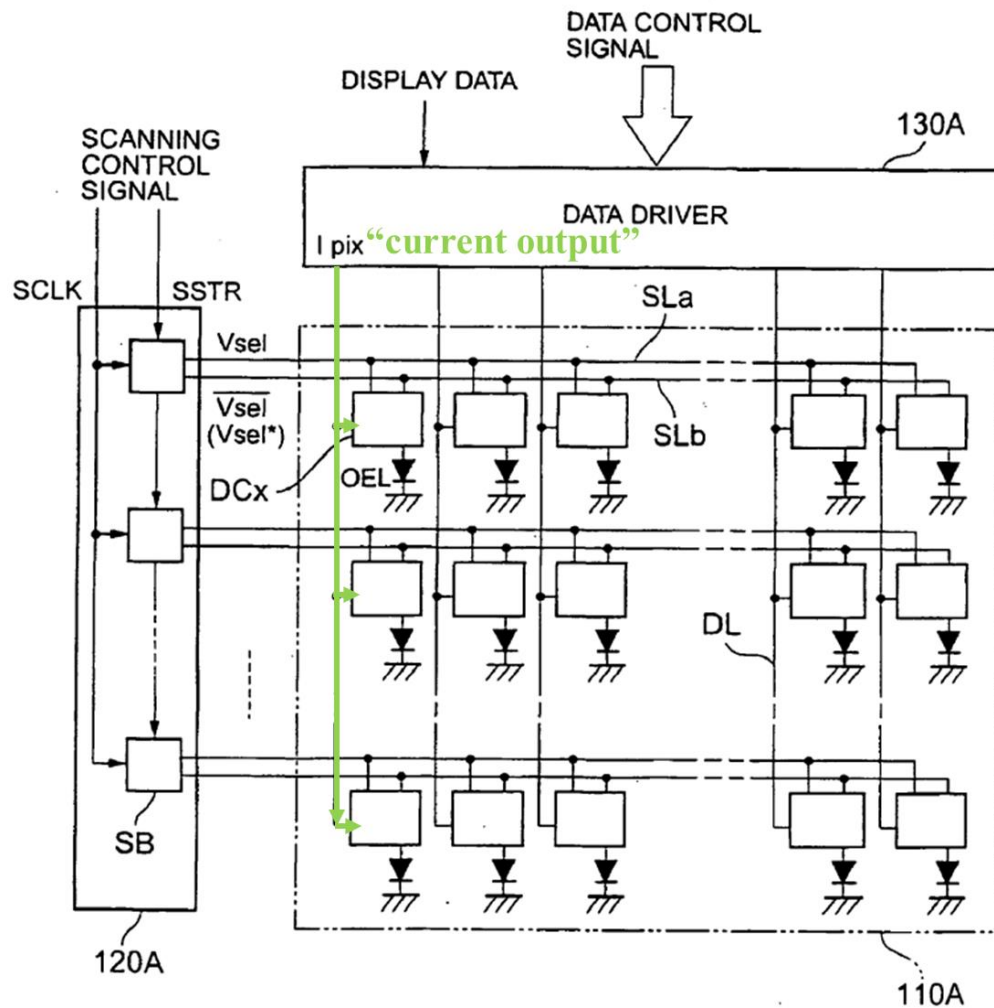
As shown in Fig. 10 below, **Sasaki** further discloses that a “gradation current generation section 201” that “ha[s] an equivalent configuration to the current generation section 20A” discussed above. Sasaki, [0127]. The current generation section 201 includes an INi connection node connected to a “**constant current generation source.**” Sasaki, [0063]-[0064], [0071], [0144]. The current generation section 201 includes a contact OUTi, which supplies the “composite value of the[] module currents” from **switching transistors TP16~TP19** to the loads. Sasaki, [0065], [0069], [0152]. The current generation section 201 is connected to an “**output control transistor[] Tr311**” that outputs **current Ipix**, which is

“equivalent to the drive current supply line Ld mentioned above.” Sasaki, [0124], [0130], [0135], [0142]. Kattamis, ¶178.



Sasaki, Fig. 10.

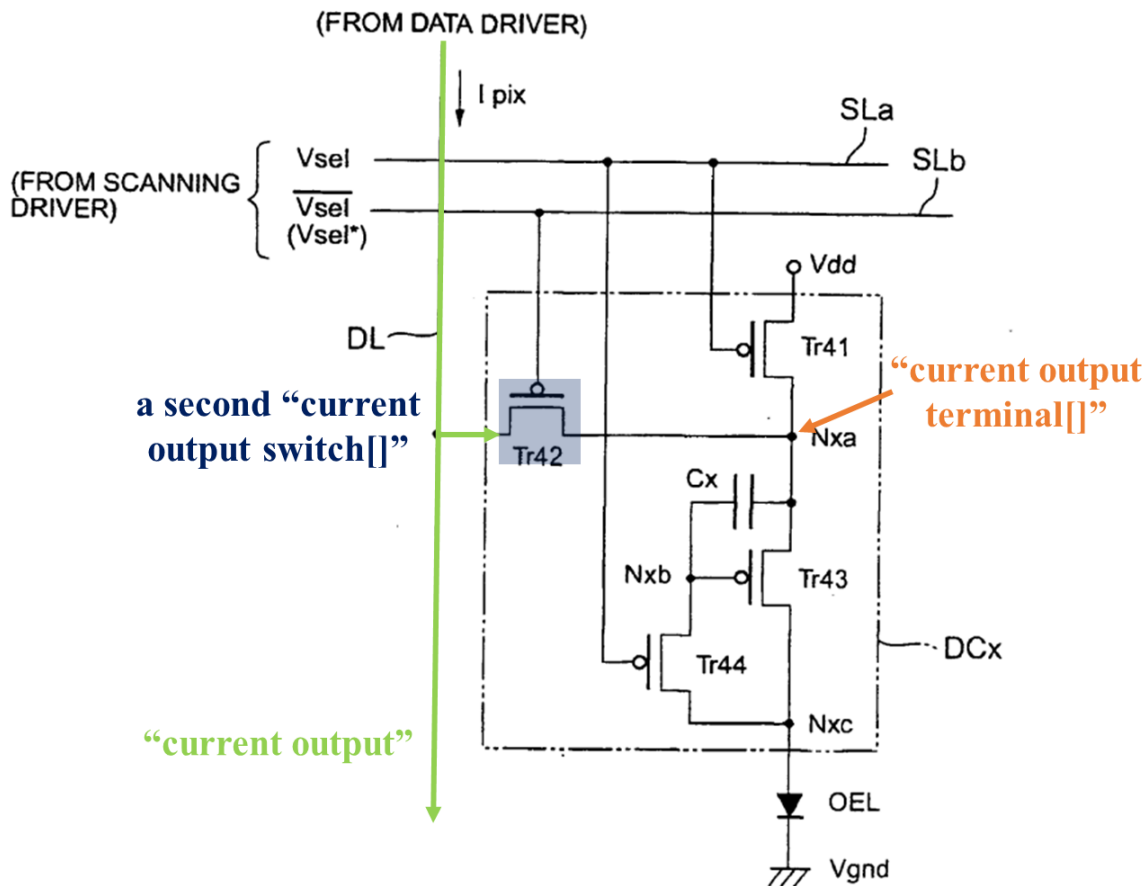
Output current I_{pix} flows through output control transistor Tr311 and into “pixel driver circuits DC_x” (shown in Fig. 7 below) via a data line DL to “control the write-in of the gradation currents I_{pix} in each of the display pixels.” Sasaki, [0102], [0113]-[0117], [0130]-[0131]. Kattamis, ¶179.



Sasaki, Fig. 7.

Each pixel driver circuit DCx includes a “**Pch FET Tr42**” connected to the data line DL that is turned “ON” to supply the **current I_{pix}** to the “light emitting device[]” via “**contact Nxa**.” Sasaki, [0113], [0116]; Kattamis, ¶180.

FIG. 8



Sasaki, Fig. 8.

b. Claim 10

i. 10(pre): "A current driving device, comprising:"

To the extent the preamble is limiting, **Sasaki discloses a current driving device** (e.g., "current generation supply circuit...supplies drive currents"). Sasaki, Abstract, [0003]; Kattamis, ¶¶181-183.

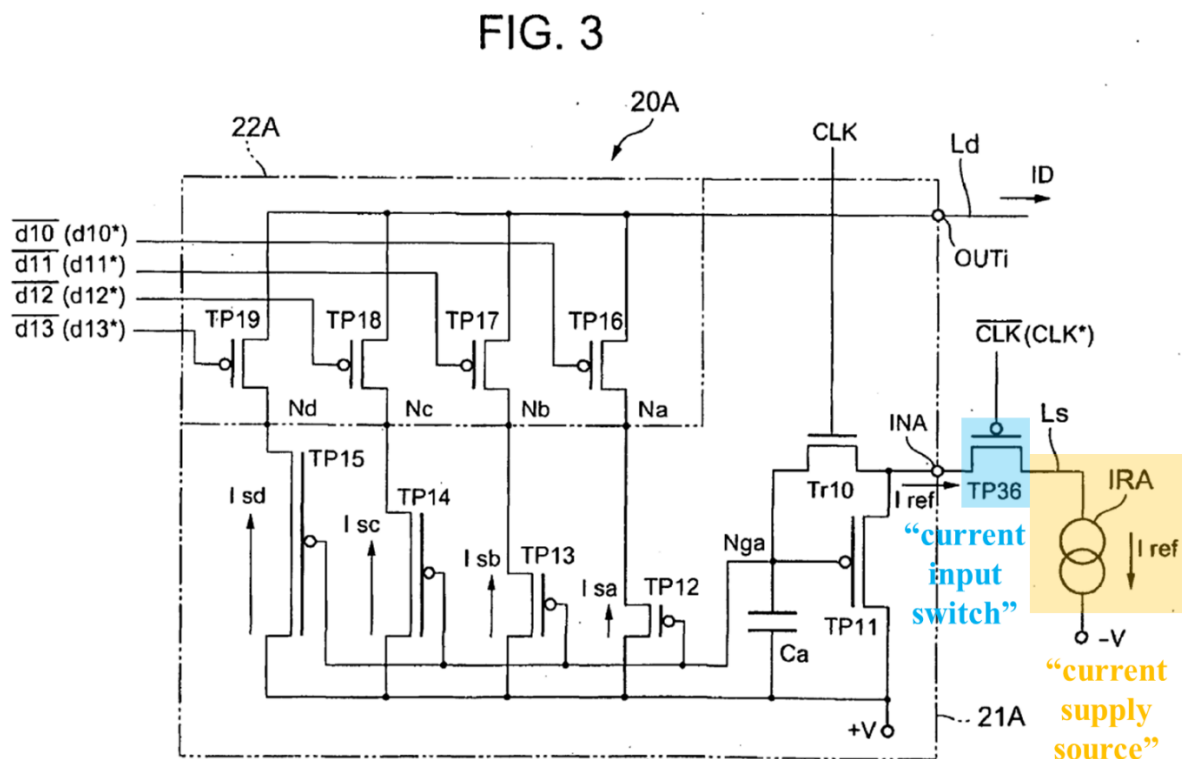
For example, **Sasaki** discloses "a display device comprising [a] current generation supply circuit." Sasaki, [0003]. The current generation supply circuit

“supplies drive currents corresponding to digital signals for a plurality of loads.”

Sasaki, Abstract; Kattamis, ¶183.

- ii. 10(a): “a current input switch for controlling connection/disconnection states with respect to a current supply source;”

Sasaki discloses a current input switch for controlling connection/disconnection states (e.g., “current supply source control transistor TP36” controls connection/disconnection) with respect to a current supply source (e.g., “constant current generation source IRA”). Sasaki, [0062]-[0064], Fig. 3; Kattamis, ¶¶184-186.



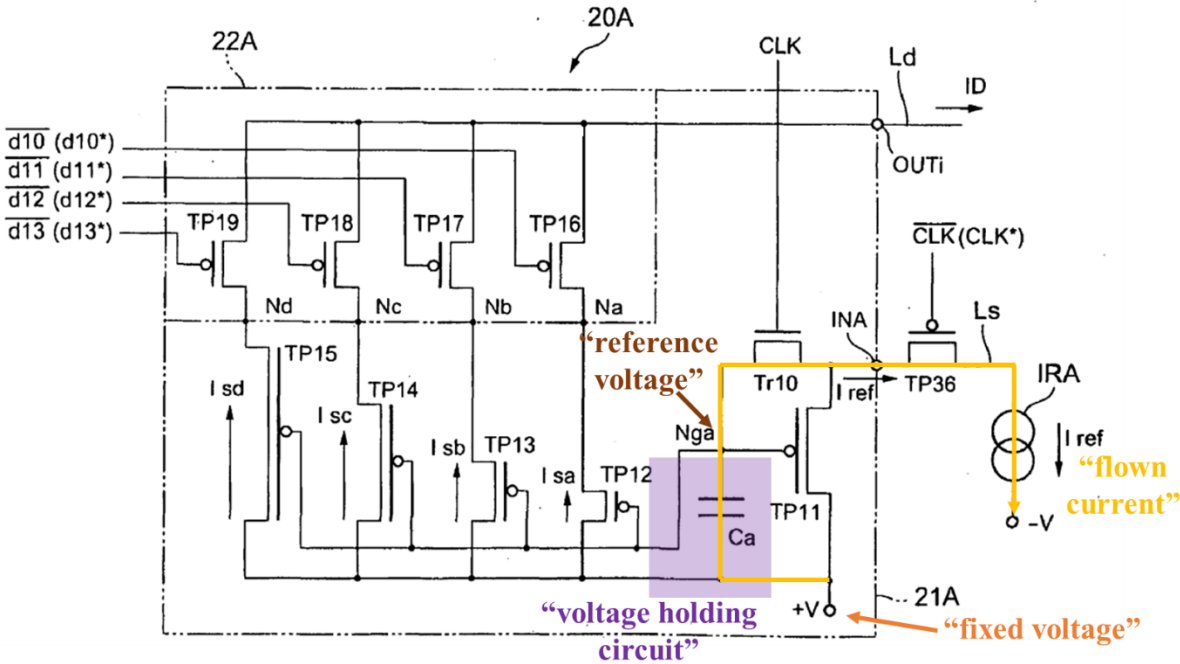
Sasaki, Fig. 3.

For example, **Sasaki** discloses a “current supply source control transistor TP36” (annotated light blue) that “switch[es] ‘ON/OFF’” to connect and disconnect a “constant current generation source IRA” (annotated gold) that “supplie[s]” a “reference current I_{ref} .” *Id.*, [0062]-[0064], Fig. 3. Kattamis, ¶186.

- iii. **10(b): “a voltage holding circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;”**

Sasaki discloses a voltage holding circuit for holding a reference voltage (*e.g.*, “capacitor Ca (charge storage circuit)” for holding “specified voltage”), **which is charged by a flown current** (*e.g.*, “recharg[ed]” by “reference current I_{ref} ”), **the voltage holding circuit having a first terminal** (*e.g.*, “capacitor Ca is connected” to “high electric potential +V”) **and a second terminal** (*e.g.*, “contact Nga (gate terminal of the reference current transistor TP11)”), **the first terminal being connected to a fixed voltage** (*e.g.*, fixed “potential +V”). Sasaki, [0063], [0071], [0077], [0138]; Kattamis, ¶¶187-189.

FIG. 3



Sasaki, Fig. 3.

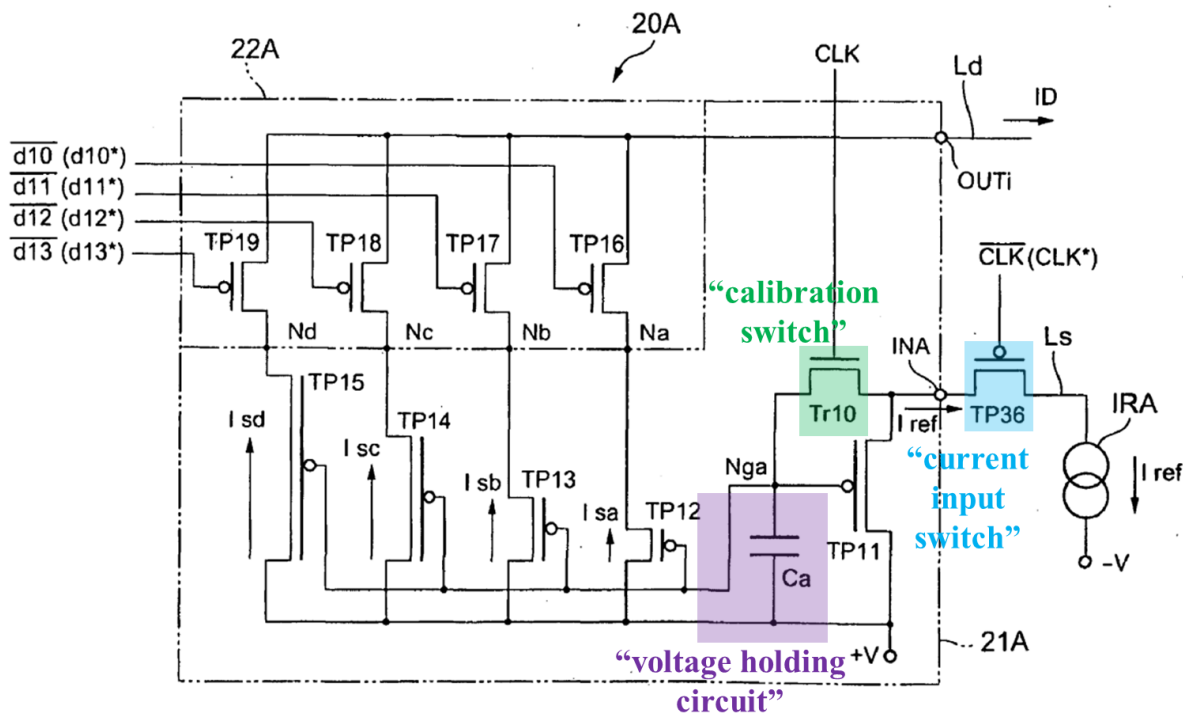
For example, **Sasaki** discloses a “capacitor Ca” (annotated purple) “connected between the high electric potential +V” (annotated orange) and “the contact Nga (gate terminal of the reference current transistor TP11).” Sasaki, [0063]. The capacitor stores “electrical charge supplied to the contact Nga,” including when “recharg[ed]” by the “reference current Iref...flowing in the current path” (annotated gold). Sasaki, [0071], [0077], [0138]. A POSITA would have understood the high electric potential +V represents a constant fixed voltage supply. Designations such as “+V,” in connection with designations such as VDD and VCC, are commonly

used on circuit diagrams to depict a fixed supply voltage that is supplied to the drain of a MOSFET. Kattamis, ¶189.

iv. 10(c): “a calibration switch interposed between said current input switch and said voltage holding circuit;”

Sasaki discloses a calibration switch (e.g., “refresh control transistor Tr10”) interposed between said current input switch (see 10(a)) and said voltage holding circuit (see 10(b)). Sasaki, [0077], Fig. 3; Kattamis, ¶¶190-196. See 10(a)-10(b).

FIG. 3



Sasaki, Fig. 3.

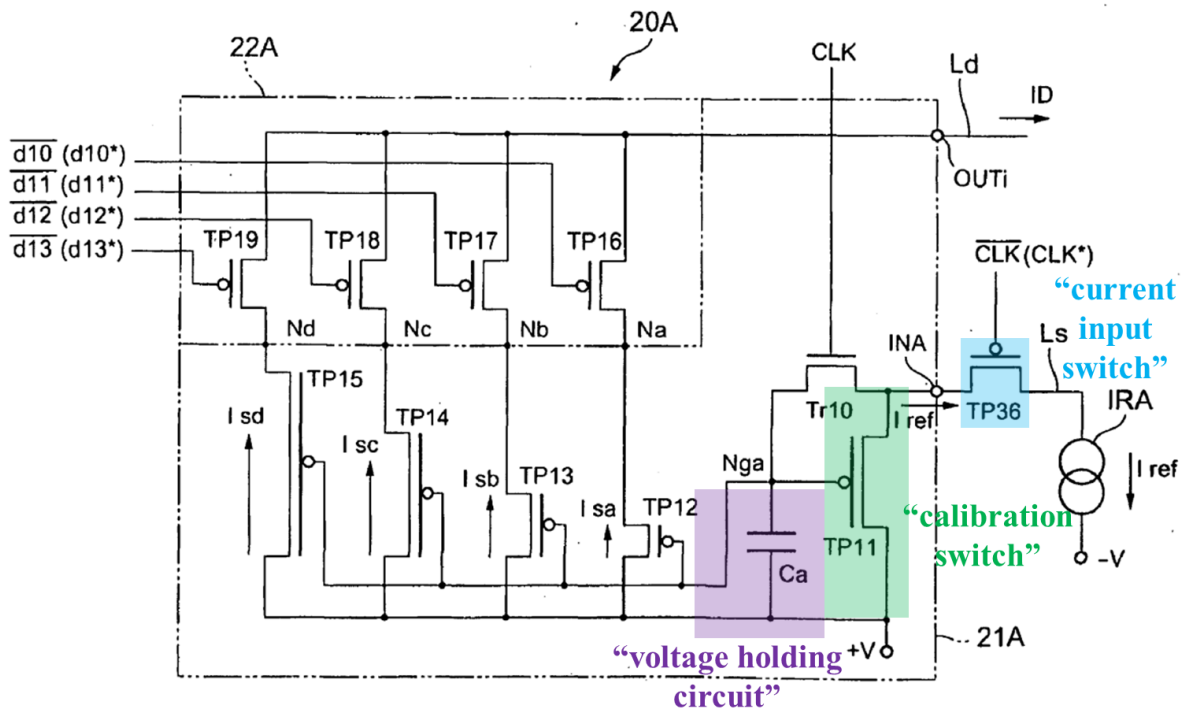
For example, **Sasaki** discloses a “refresh control transistor Tr10” that, when “perform[ing] an ‘ON’ operation,” causes “the reference current Iref [to] flow[]” and

“charge” capacitor Ca. Sasaki, [0077].¹⁰ As illustrated in Figure 3, the refresh control transistor Tr10 is interposed between the current supply source control transistor TP36 and capacitor Ca. Kattamis, ¶193.

Alternatively, **Sasaki discloses a calibration switch** (*e.g.*, “reference current transistor TP11”) **interposed between said current input switch** (*see* 10(a)) **and said voltage holding circuit** (*see* 10(b)). Sasaki, [0063], [0077], Fig. 3; Kattamis, ¶¶194-195. *See* 10(a)-10(b).

¹⁰ This is consistent with the '047, which describes that “[c]alibration’ means to have a reference current value by a reference current source stored in the current output part.” '047, 1:37-39. Kattamis, ¶193.

FIG. 3



Sasaki, Fig. 3.

For example, **Sasaki** discloses a “reference current transistor TP11” (annotated green) with its gate terminal “connected to the contact Nga” and capacitor Ca (annotated purple), allowing current to flow from “the high electric potential +V” to “the current input contact INA to which the reference current Iref is supplied” via current supply source control transistor TP36 (annotated light blue). Sasaki, [0063]. For example, “when both the current supply source control transistor TP36 and the refresh control transistor Tr10” are “ON,” the reference current Iref flows through the reference current transistor TP11 such that “the electrical charge of the reference

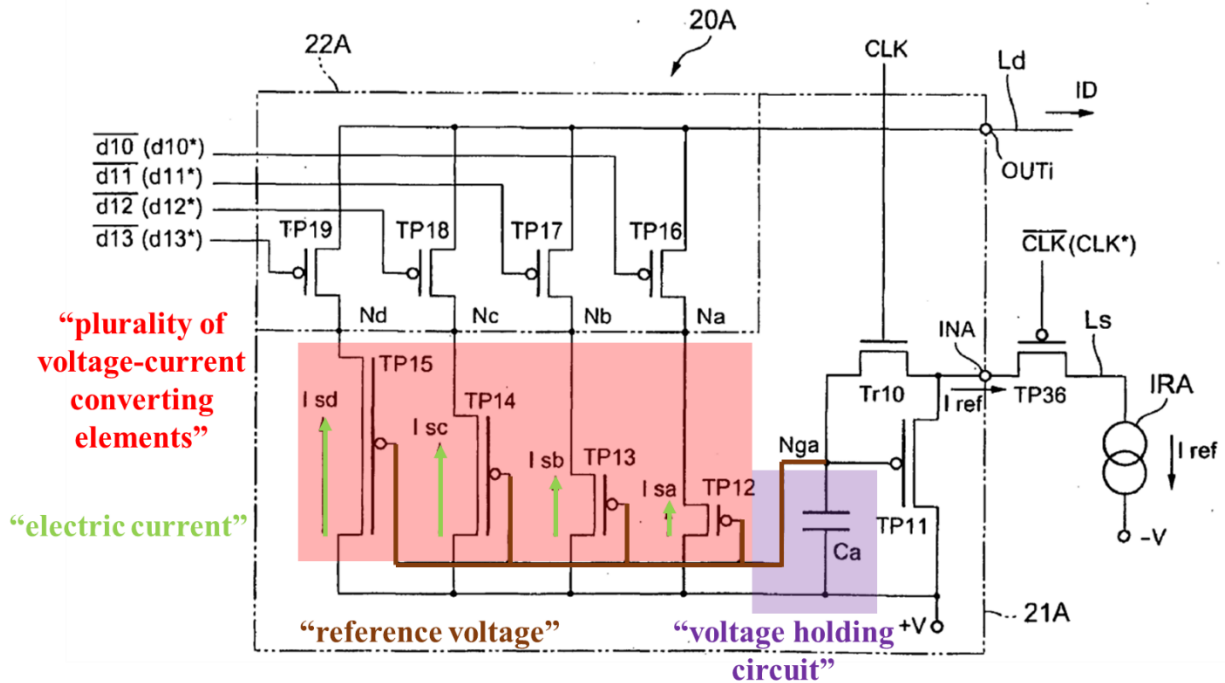
current I_{ref} is supplied to the gate terminal” of transistor TP11.¹¹ Sasaki, [0077]. A POSITA would have understood or at least found it obvious that the reference current transistor TP11 is a switch, as transistors were well understood to be switching devices. As illustrated in Figure 3, the reference current transistor TP11 is interposed between the current supply source control transistor TP36 and capacitor C_a , as the drain of the reference current transistor TP11 is connected to the same node as transistor TP36 and the gate of transistor TP11 is connected to the same node as capacitor C_a . Kattamis, ¶196.

- v. **10(d): “a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding circuit;”**

Sasaki discloses a plurality of voltage-current converting elements (e.g., “a plurality of module current transistors”) for generating an electric current (e.g., generating “currents $I_{sa} \sim I_{sd}$ ”) in accordance with said reference voltage held in said voltage holding circuit (e.g., voltage stored on C_a “relative to the constant reference current I_{ref} ”). Sasaki, [0015], [0063], [0066]-[0068], Fig. 3; Kattamis, ¶¶197-200. *See* 10(b).

¹¹ This is also consistent with '047, 1:37-39. Kattamis, ¶196.

FIG. 3



Sasaki, Fig. 3.

For example, **Sasaki** discloses “a plurality of module current transistors” (TP12-TP15 annotated red) that have their gates “connected in common to the contact Nga” (annotated brown) and their drains connected to “the high electric potential +V.” Sasaki, [0015], [0063]. When voltage is stored in capacitor Ca (annotated purple), as discussed in 10(b), the module current transistors are turned on and generate “module currents $I_{sa} \sim I_{sd}$...relative to the constant reference current I_{ref} ” (annotated green) such that they generate an electric current based on the

reference voltage stored in capacitor Ca, thereby converting voltage to current.

Sasaki, [0066]-[0068]; Kattamis, ¶200.¹²

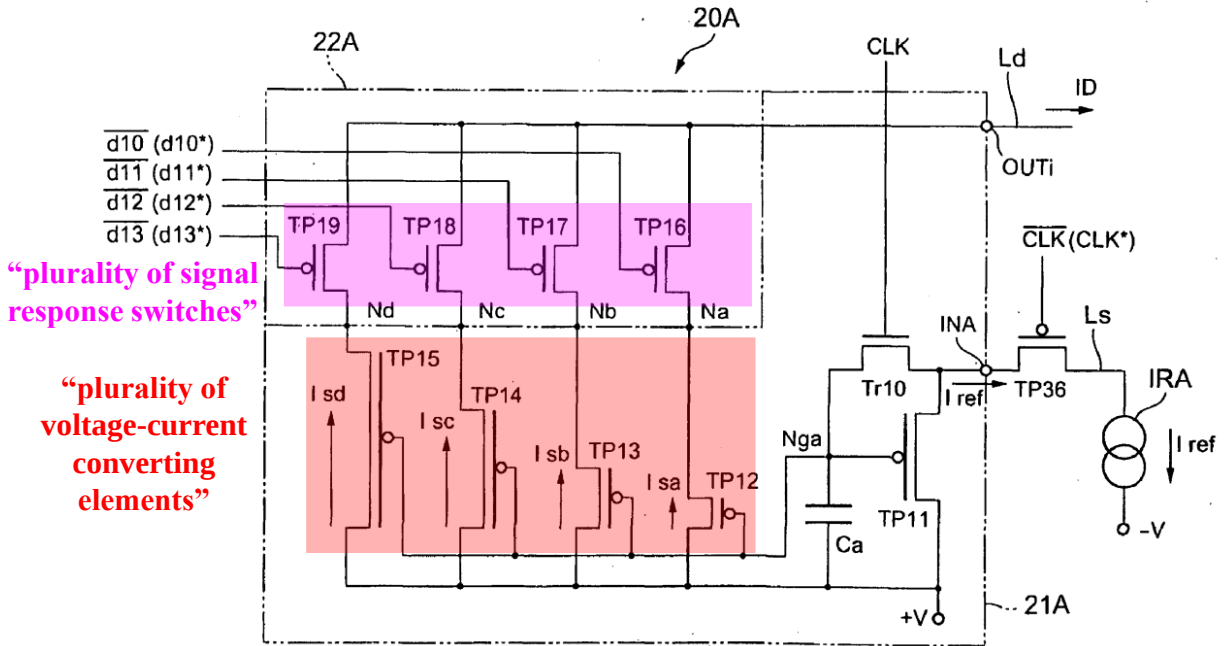
- vi. **10(e): “a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being connected in series to a corresponding one of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;”**

Sasaki discloses a plurality of signal response switches (e.g., “switching transistors TP16~TP19”) that are on/off controlled in accordance with inputted signals (e.g., turn “ON” or “OFF” according to “signals d10*~d13*”), each of said response switches being connected in series to a corresponding one of said voltage-current converting elements (e.g., each “switching transistor[.]” in series to a “module current transistor[.]”), and each of which being connected in parallel to said calibration switch (e.g., each “switching transistor[.]” parallel to “reference

¹² This is consistent with the '047, which discloses “a voltage-current converting function is actuated” when “[a] gate voltage according to the electric charges accumulated in the voltage holding capacitance element C1 is applied to the gates of the Nch transistors QN1-QNm” such that “it is possible to output a sink current having a current value proportional to the reference current.” '047, 8:17-49. Kattamis, ¶200.

current transistor TP11”). Sasaki, [0065], [0069], [0152], Fig. 3; Kattamis, ¶¶201-207. See 10(c).

FIG. 3

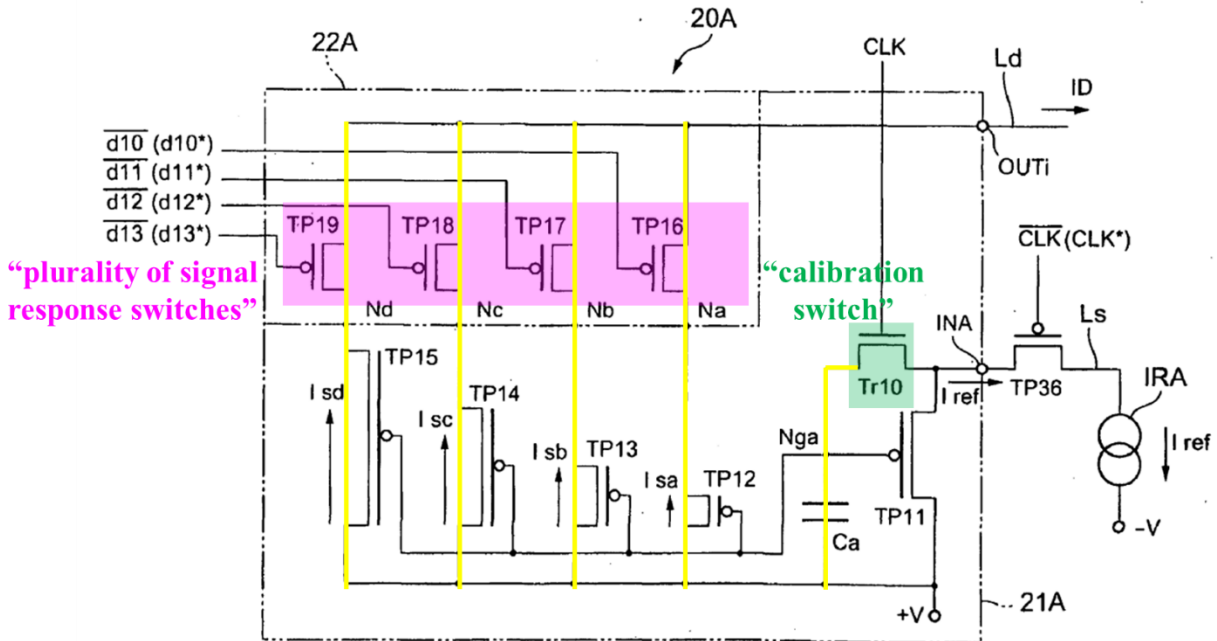


Sasaki, Fig. 3.

For example, **Sasaki** discloses “switching transistors TP16~TP19” (annotated pink) that are “connected to each of the module current transistors TP12~TP15” (annotated red) and turn “ON” or “OFF” to supply the “composite value of the[] module currents” to the loads. Sasaki, [0065], [0069]-[0070], [0152]. These switching transistors are each in series with a corresponding module current transistor. For example, transistor TP19 is connected in series to the module current transistor TP15, transistor TP18 is connected in series to module current transistor TP14, and so on. Kattamis, ¶204.

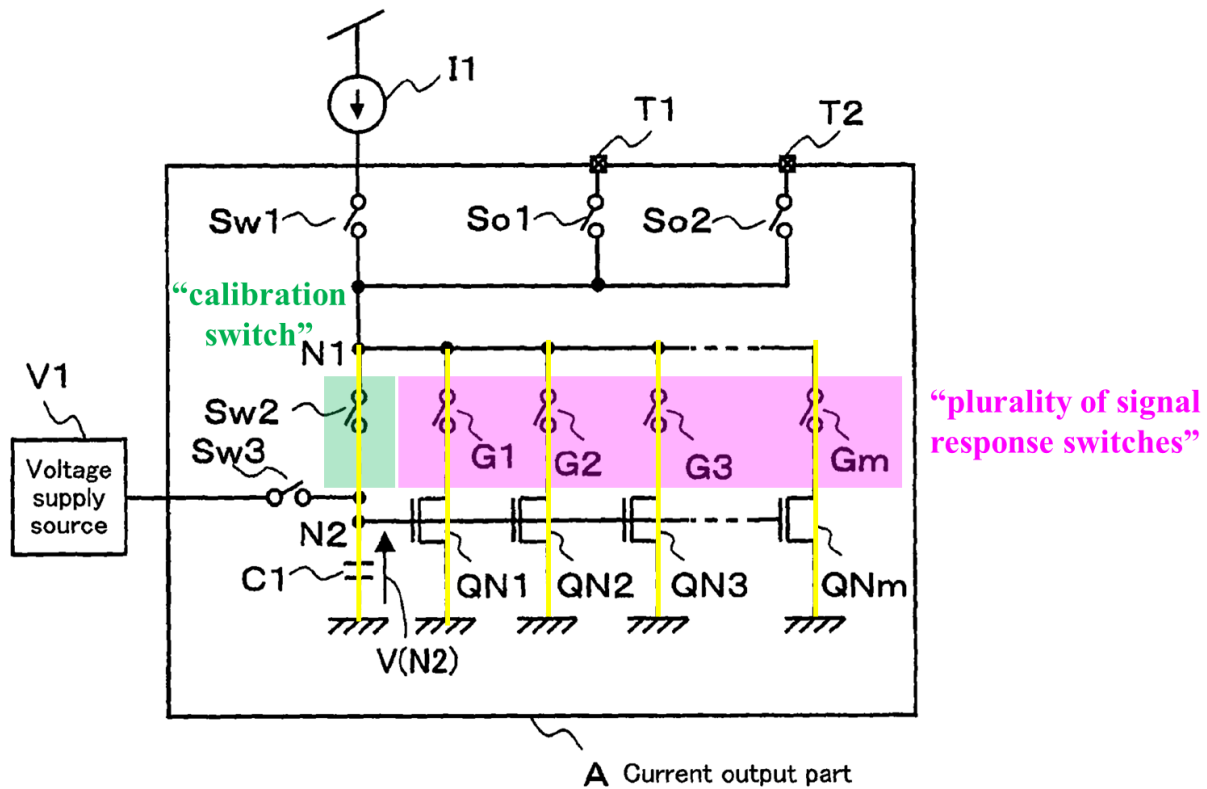
Each of the switches TP16-TP19 is connected in parallel to a refresh control switch, as they share common nodes. First, the on/off states of a switching transistor do not affect the on/off states of another switching transistor. Sasaki, Fig. 3. Second, each switching transistor TP16-TP19 is connected to the high electric potential through a module current transistor TP12-TP15, and Tr10 is also connected to the high electric potential +V via the capacitor Ca (*see* 10(c)). The other side of the switching transistors TP16-TP19 is connected to ground through the load through the OUTi node to form a complete loop for the current (as discussed further in 10(g)). The other side of Tr10 is connected to “the low electric potential –V,” such as “the ground potential” through calibration switch TP36 and current reference IRA. Kattamis, ¶205.

FIG. 3



Sasaki, Fig. 3. This is consistent with the '047, which describes “all the Nch transistors QN1-QNm shown in FIG. 1A are connected in parallel” because the transistors and the switch Sw2 share common nodes to ground and N1 through switches G1-Gm as shown in Figure 1A. '047, 7:1-23, 11:55-12:6; Kattamis, ¶206.

FIG. 1A

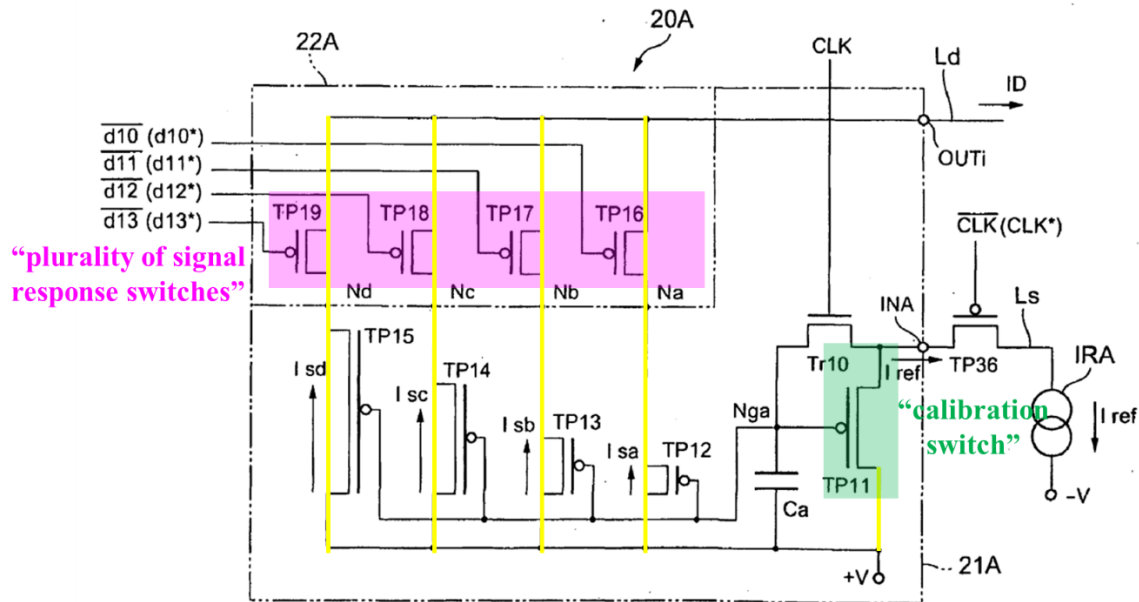


'047, Fig. 1A.

Each of the switches TP16-TP19 (annotated pink) is connected in parallel to reference current transistor TP11 (annotated green), as they share common nodes. First, the on/off states of a switching transistor do not affect the on/off states of another switching transistor. Sasaki, Fig. 3. Second, each switching transistor TP16-TP19 is connected to the high electric potential through a module current transistor TP12-TP15, and reference current transistor TP11 is also connected to the high electric potential $+V$ via the capacitor C_a (see 10(c)). The other side of the switching transistors TP16-TP19 is connected to ground through the load to form a complete

loop for the current. The other side of reference current transistor TP11 is connected to “the low electric potential $-V$,” such as “the ground potential” through calibration switch TP36 and current reference IRA. Kattamis, ¶207.

FIG. 3

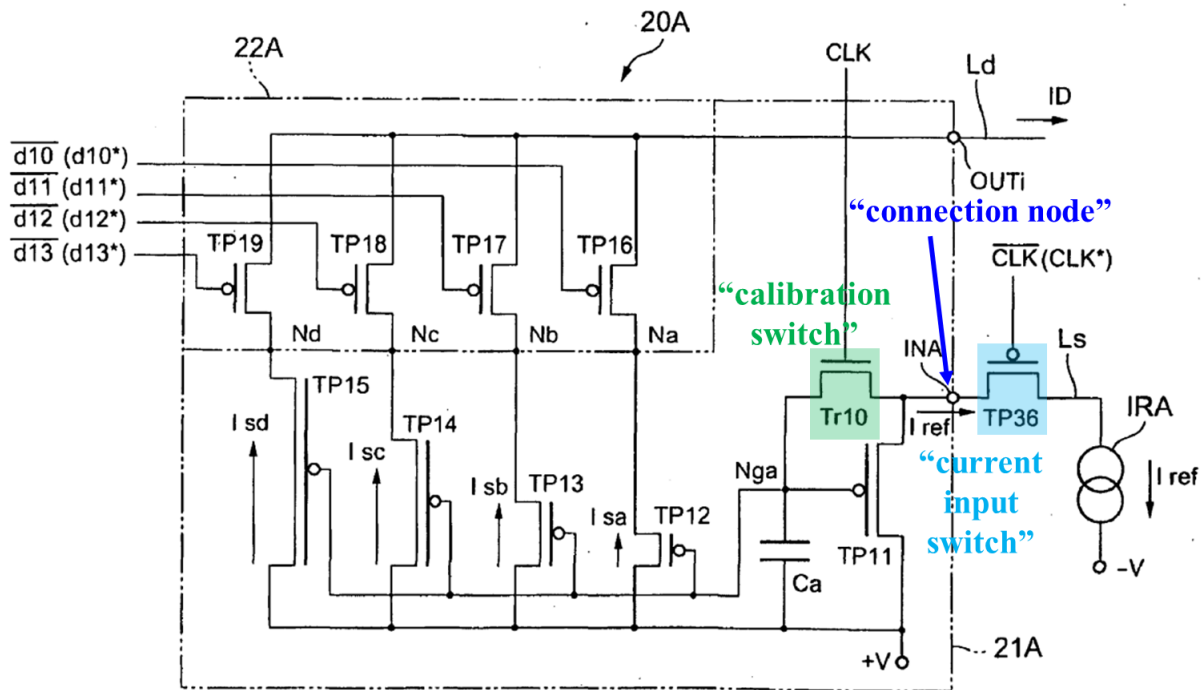


Sasaki, Fig. 3.

- vii. 10(f): “a connection node provided between said current input switch and said calibration switch;”**

Sasaki discloses a connection node (*e.g.*, “current input contact INA”) **provided between said current input switch** (*see* 10(a)) **and said calibration switch** (*see* 10(c)). Sasaki, [0063]-[0064], [0071]; Kattamis, ¶¶208-214. *See* 10(a)-10(c).

FIG. 3



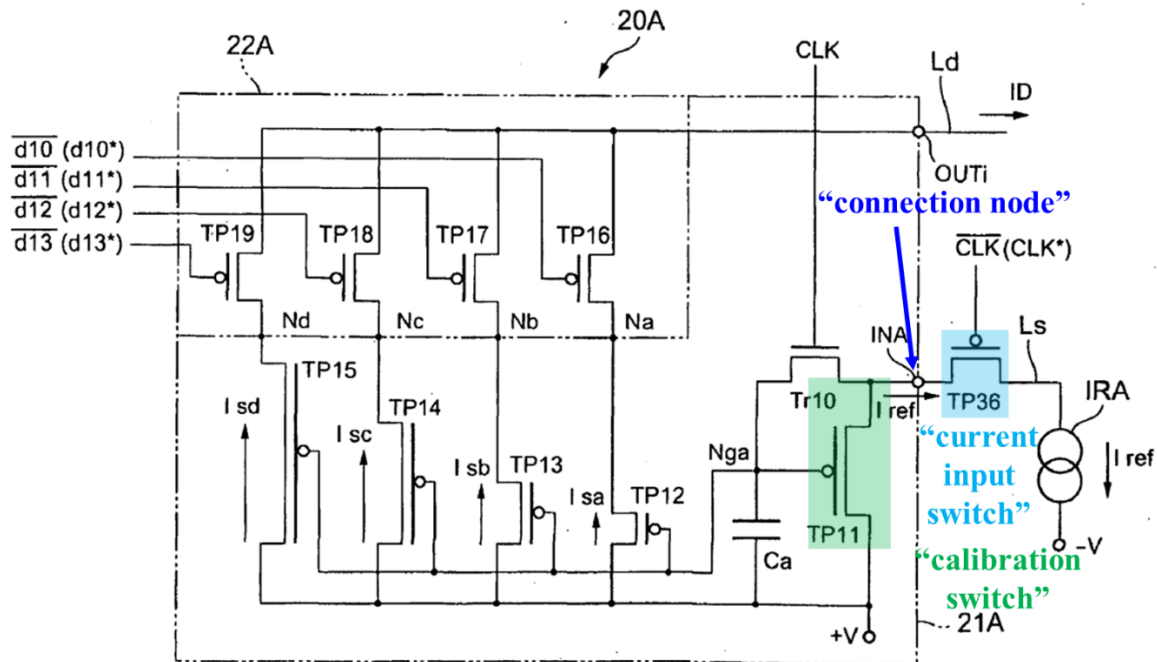
Sasaki, Fig. 3.

For example, **Sasaki** further discloses a “current input contact INA,” which is illustrated in Figure 3 to be “connected to a current supply source control transistor TP36” and the refresh control transistor Tr10. Sasaki, [0063]-[0064], [0071]. The current input contact INA is a node of a corresponding current generation section 20A, receiving a reference current I_{ref} from a corresponding reference current supplier IRA. Sasaki, [0071]; Kattamis, ¶211.

Alternatively, **Sasaki discloses a connection node** (e.g., “current input contact INA”) **provided between said current input switch** (see 10(a)) **and said**

calibration switch (see 10(c)). Sasaki, [0063]-[0064], [0071]; Kattamis, ¶¶212-214. See 10(a)-10(c).

FIG. 3



Sasaki, Fig. 3.

For example, **Sasaki** further discloses a “current input contact INA” (annotated blue), which is illustrated in Figure 3 to be “connected to a current supply source control transistor TP36” (annotated light blue) and the reference current transistor TP11. Sasaki, [0063]-[0064], [0071]. The current input contact INA is a node of a corresponding current generation section 20A, receiving a reference current I_{ref} from a corresponding reference current supplier IRA. Sasaki, [0071]; Kattamis, ¶214.

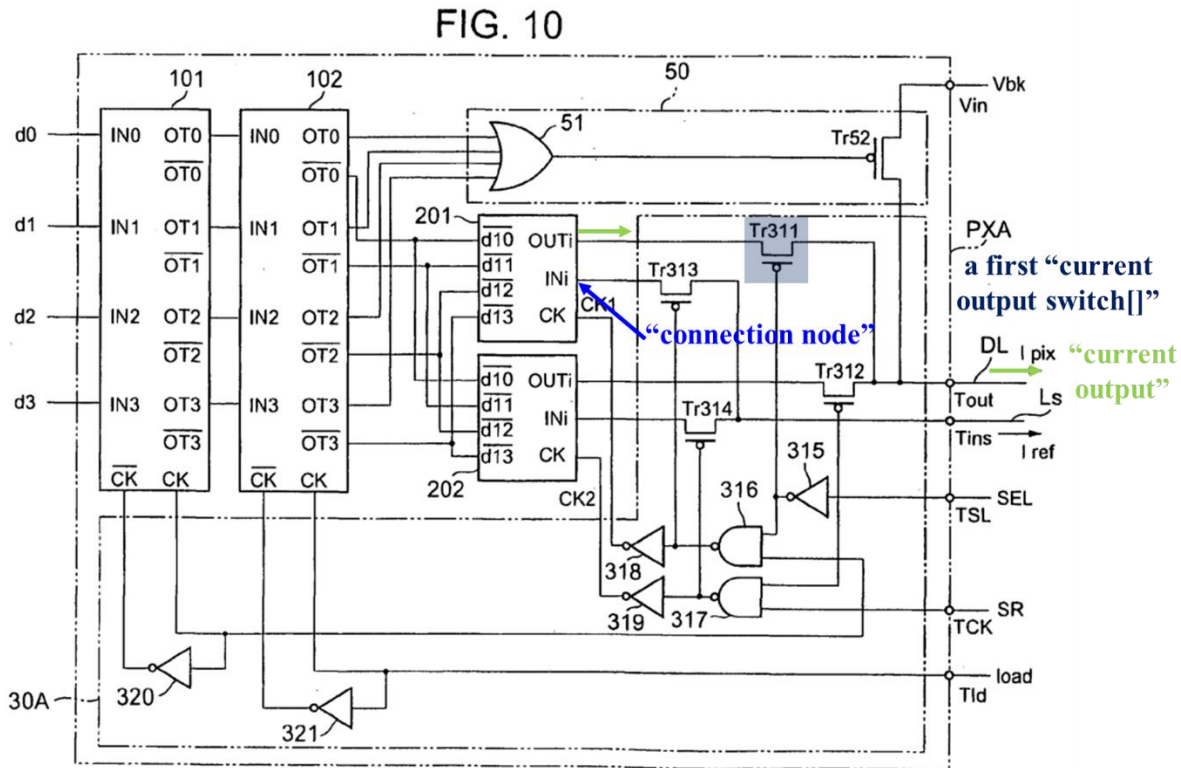
- viii. 10(g): “a plurality of current output switches, each being interposed between the connection node and said plurality of current output terminals; and”**

Sasaki discloses a plurality of current output switches (*e.g.*, “output control transistor[] Tr311” and “Pch FET Tr42”), **each being interposed between the connection node** (*e.g.*, “INi”) **and said plurality of current output terminals** (*e.g.*, “contact Nxa” connected to “Pch FET Tr42”).¹³ Sasaki, [0063]-[0065], [0069], [0071], [0102], [0113]-[0117], [0124], [0127], [0130]-[0131], [0135], [0142], [0152], Figs. 7, 8, 10; Kattamis, ¶¶215-221. *See* 10(f).

For example, **Sasaki** further discloses that a “gradation current generation section 201” that “ha[s] an equivalent configuration to the current generation section 20A” discussed above in 10(pre)-10(f). Sasaki, [0127]. The current generation section 201 includes an INi connection node (annotated blue), as discussed in 10(f), connected to a “constant current generation source.” Sasaki, [0063]-[0064], [0071]. The current generation section 201 includes a contact OUTi, which supplies the “composite value of the[] module currents” (annotated green) from switching

¹³ Claim 10 recites “said plurality of current output terminals,” but lacks antecedent basis as the term “plurality of current output terminals” is not previously used in claim 10. Solely for this petition, Petitioner assumes the term refers to a plurality of current output terminals. Kattamis, ¶216.

transistors TP16~TP19 to the loads as discussed in 10(e). Sasaki, [0065], [0069], [0152]. The OUT_i contact of the current generation section 201 is connected to an “output control transistor[] Tr311” (annotated dark blue) that outputs current I_{pix} (annotated green), which is “equivalent to the drive current supply line L_d”—i.e., the “composite value of the[] module currents” from switching transistors TP16~TP19 as discussed in 10(e). Sasaki, [0069], [0124], [0130], [0135], [0142]. Kattamis, ¶218.

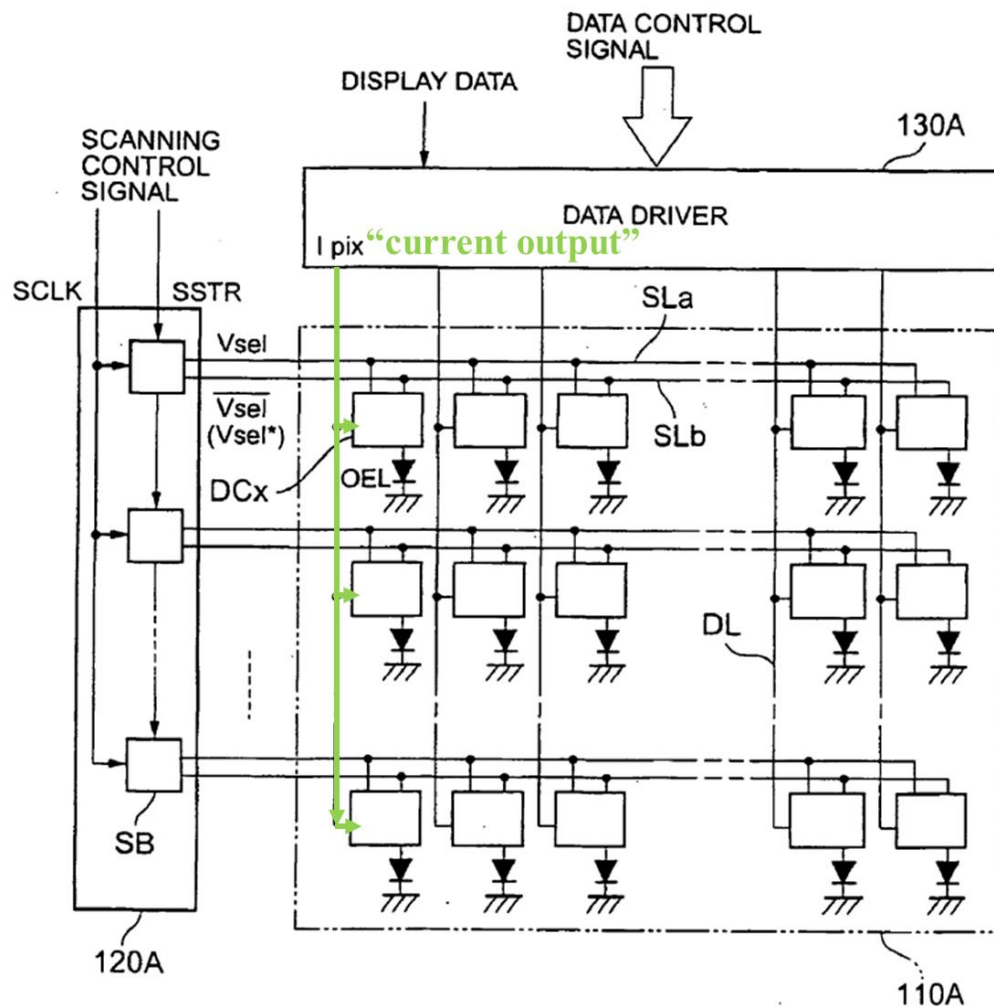


Sasaki, Fig. 10.

Output current I_{pix} (annotated green) flows through output control transistor Tr311 (annotated dark blue) and into “pixel driver circuits DC_x” via a data line DL

to “control the write-in of the gradation currents I_{pix} in each of the display pixels.”

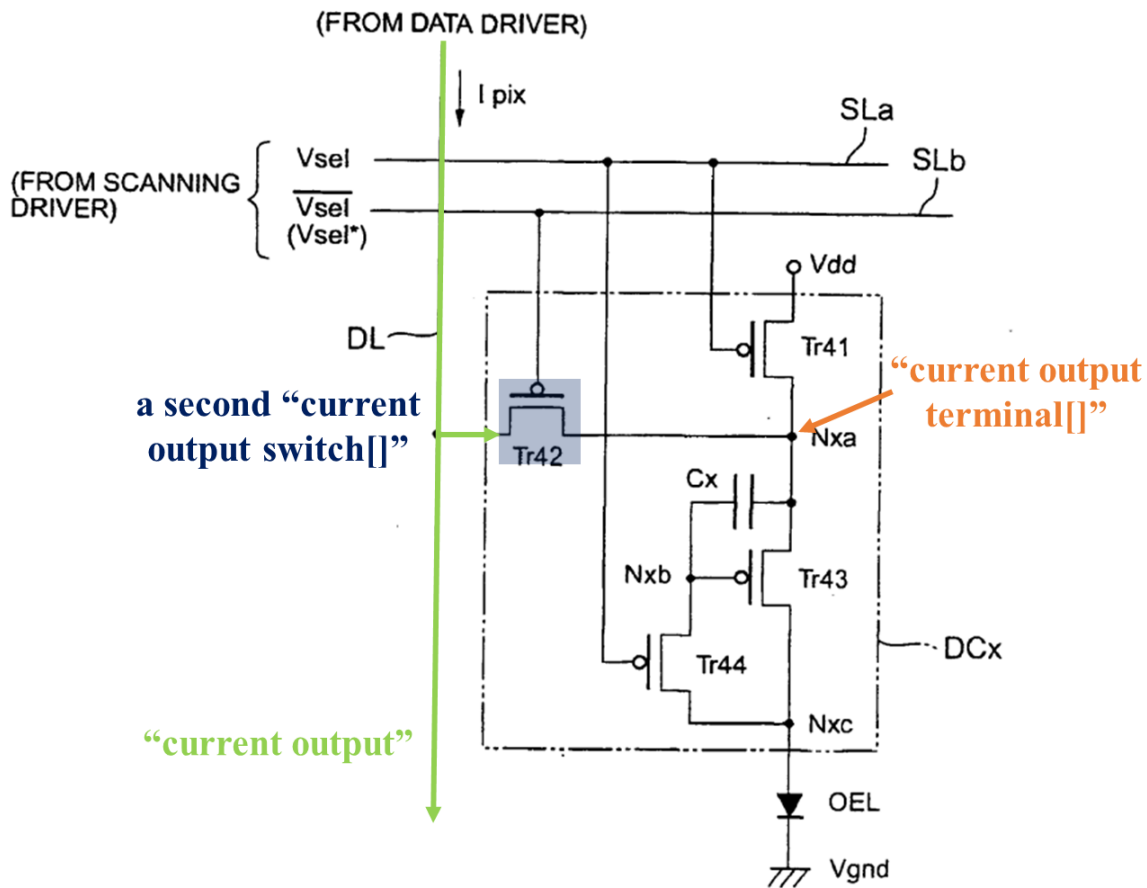
Sasaki, [0102], [0113]-[0117], [0130]-[0131]; Kattamis, ¶219.



Sasaki, Fig. 7.

Each pixel driver circuit DCx includes a “Pch FET Tr42” (annotated dark blue) connected to the data line DL that is turned “ON” to supply the current I_{pix} (annotated green) to the “light emitting device[]” via “contact Nxa” (annotated orange). Sasaki, [0113], [0116]; Kattamis, ¶220.

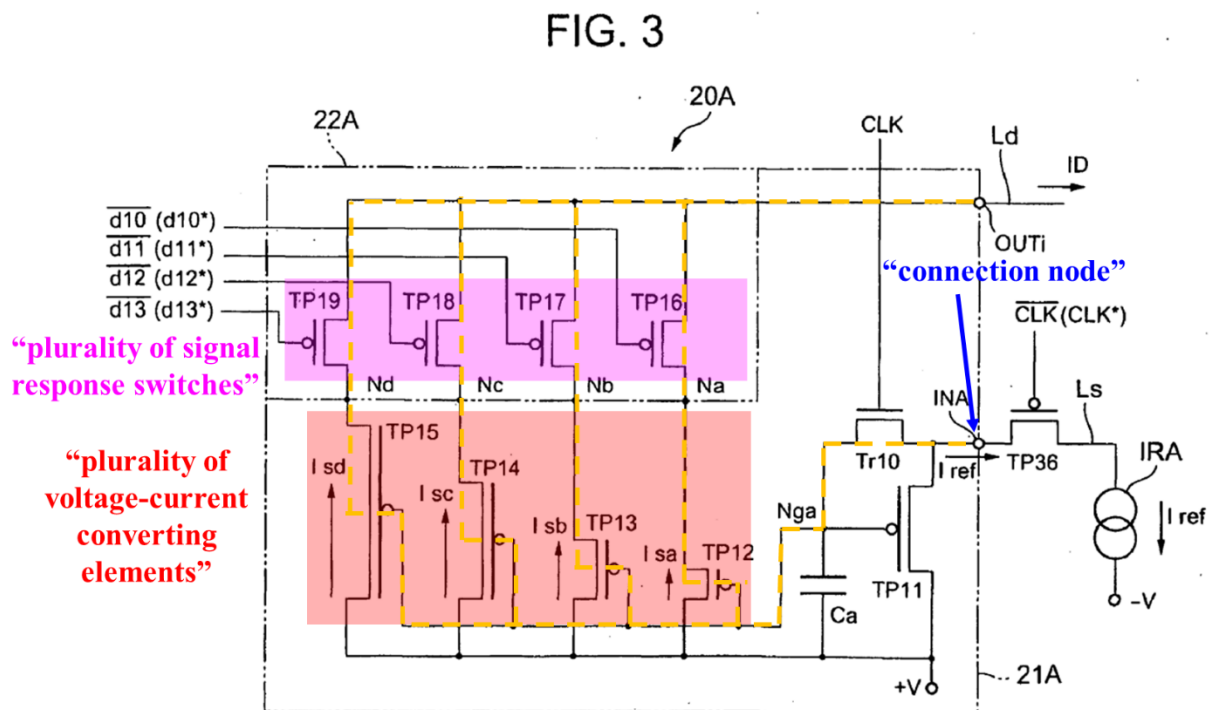
FIG. 8



Sasaki, Fig. 8.

Therefore, "output control transistor[] Tr311" and "Pch FET Tr42" (annotated dark blue) each receive the output current I_{pix} and are interposed between "contact Nxa" (annotated orange) and the INi connection node (annotated blue) in the current generation section 201. Kattamis, ¶221. As discussed in this limitation 10(g), the transistors Tr311 and Tr42 (annotated dark blue) are interposed between "contact Nxa" (annotated orange) and the OUTi contact of the current generation section 201. In addition, the OUTi contact of the current generation section 201 is connected to

“current input contact INA” (see 10(f), and equivalent to terminal IN_i of the current generation section 201). For example, these contacts are connected via the switching transistors TP16~TP19 (annotated pink), module current transistors TP15~TP12 (annotated red), and transistor Tr10 (gold annotation showing that OUT_i and INA are coupled):

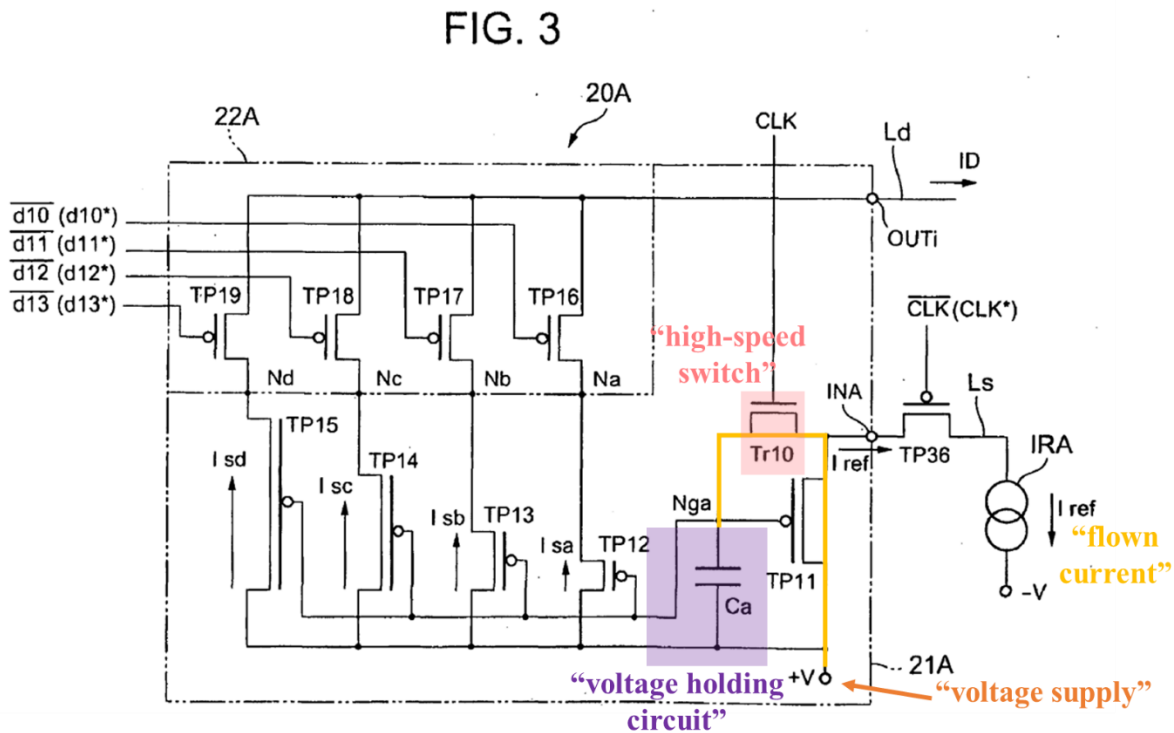


Sasaki, Fig. 3; Kattamis, ¶221.

- ix. 10(h): “a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit.”

Sasaki discloses a high-speed switch (e.g., “refresh control transistor Tr10”) for controlling connection/ disconnection states (e.g., “ON/OFF” states) of said

voltage supply source (e.g., “high electric potential +V”) **with respect to the second terminal of said voltage holding circuit** (e.g., “high electric potential +V” with respect to capacitor Ca via transistor Tr10 and “reference current transistor TP11”).¹⁴ Sasaki, [0063]; Kattamis, ¶¶222-226. See 10(b).



Sasaki, Fig. 3.

¹⁴ Claim 10 recites “said voltage supply source,” but lacks antecedent basis as the term “voltage supply source” is not previously used in claim 10. Solely for this petition, Petitioner assumes the term refers to “a fixed voltage,” which is recited earlier in the claim. Kattamis, ¶223.

For example, **Sasaki** discloses “a reference current transistor TP11” with its gate connected to capacitor Ca (contact Nga) and its source connected to “high electric potential +V.” Sasaki, [0063]. The “refresh control transistor Tr10” (annotated light red) performs a “switch ‘ON/OFF’ operation” so that a “path is connected between the contact Nga,” which is a second terminal of the capacitor Ca as discussed in 10(b), and the “high electric potential +V” through reference current transistor TP11. Sasaki, [0063]. A POSITA would have understood that transistor Tr10 is a high-speed switch because it can be turned on and off within the timespan of a single frame. A POSITA would have further understood a high electric potential +V to be an example of a voltage supply source such that when transistor Tr10 is in an “ON” state, the voltage supply source +V is connected with respect to the contact Nga connected to capacitor Ca. Kattamis, ¶225.

To the extent it is argued that the high-speed switch must be different from the calibration switch, **Sasaki** further discloses reference current transistor TP11 that, when used in combination with refresh control transistor Tr10, connect a path between “contact Nga” and the “high electric potential +V” such that, when “refresh control transistor Tr10” is turned “ON,” the voltage supply source +V is connected with respect to the contact Nga. Sasaki, [0063]; Kattamis, ¶226.

X. SECONDARY CONSIDERATIONS

There is no evidence in the '047's prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any challenged Claim. *See generally* '047 FH; Kattamis, ¶¶38-40. Indeed, as demonstrated by the prior art referenced herein, any purported solutions to problems or unexpected results in the '047 were already well known. Kattamis, ¶227. To the extent PO asserts the existence of any secondary considerations in its responses, Petitioner reserves the right to address any such evidence.

XI. CONCLUSION

Substantial, new, and noncumulative technical teachings have been presented for '047 Claims 1-10, which are anticipated and/or obvious for the reasons set forth above. Kattamis, ¶¶228-233. There is a reasonable likelihood that Petitioner will prevail as to Claims 1-10. *Inter partes* review of Claims 1-10 is accordingly requested.

Respectfully submitted,

Dated: July 28, 2025

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Name: James L. Davis, Jr.
Registration No. 57,325
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to §42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,995,047 contains, as measured by the word-processing system used to prepare this paper, 13,288 words. This word count does not include the items excluded by §42.24 as not counting towards the word limit.

Dated: July 28, 2025

/James L. Davis, Jr./

Name: James L. Davis, Jr.

Registration No. 57,325

Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on July 28, 2025, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,995,047 and supporting exhibits to be served via Federal Express on the Patent Owner at the following correspondence address of record as listed on Patent Center:

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Suite 500
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UNITED STATES

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