

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.

Petitioner

v.

BISHOP DISPLAY TECH LLC

Patent Owner

Case No. IPR2025-01330

Patent No. 7,995,047

DECLARATION OF ALEX Z. KATTAMIS, PH.D., P.E.

TABLE OF CONTENTS

I.	INTRODUCTION	4
II.	EXPERIENCE AND QUALIFICATIONS	4
III.	TASK SUMMARY AND MATERIALS REVIEWED	6
IV.	LIST OF EXHIBITS	6
V.	SUMMARY OF CONCLUSIONS AND GROUNDS FOR CHALLENGE OF '047 PATENT	7
VI.	UNDERSTANDING OF THE GOVERNING LAW	8
	A. LEVEL OF ORDINARY SKILL IN THE ART	8
	B. LEGAL STANDARD FOR CLAIM CONSTRUCTION	8
	C. ANTICIPATION	10
	D. OBVIOUSNESS	10
VII.	OVERVIEW OF THE '047 PATENT	12
	A. PRIORITY DATE FOR CLAIMS OF THE '047 PATENT	12
	B. THE SUBJECT MATTER OF THE '047 PATENT	13
	C. THE CHALLENGED CLAIMS OF THE '047 PATENT	15
	D. PROSECUTION HISTORY OF THE '047 PATENT	18
VIII.	LEVEL OF ORDINARY SKILL IN THE ART FOR THE '047 PATENT	19
IX.	CLAIM CONSTRUCTION	20
X.	TECHNOLOGY BACKGROUND AND STATE OF THE ART FOR THE '047 PATENT	20
	A. EXEMPLARY REFERENCES CORROBORATING THE GENERAL ENGINEERING KNOWLEDGE	20
	a. Camara Handbook (Ex. 1009)	20
	b. den Boer Text (Ex. 1010)	21
	c. Han Article (Ex. 1011)	21
	B. GENERAL DISPLAY BACKGROUND	21
	C. BASIC CIRCUITS FOR DRIVING DISPLAYS	23
	a. Voltage supply source / Voltage supply mode	23
	b. Current supply source / Current supply mode	24
	c. Voltage-current converting circuit	24
	d. Capacitors	25
	e. Voltage and Current Programming	27

XI.	GROUND 3: BAEK IN VIEW OF DATE	30
A.	Grounds 1-2: Baek	30
a.	Overview of Baek	30
b.	Claim 1	34
c.	Claim 2	63
d.	Claim 3	65
e.	Claim 4	67
f.	Claim 9	68
B.	GROUND 3: BAEK IN VIEW OF DATE	70
a.	Claim 5	70
b.	Claim 6	76
C.	Ground 4: Baek in view of Inomoto	79
a.	Claim 7	79
b.	Claim 8	86
D.	Ground 5: Sasaki	87
a.	Overview of Sasaki	87
b.	Claim 10	91
XII.	SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS REGARDING THE CHALLENGED PATENT	112
XIII.	CONCLUSION	112

I. INTRODUCTION

1. My name is Alex Kattamis. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained herein.

2. I am over the age of 21 and am competent to make this declaration.

3. I have been retained by Ropes & Gray LLP on behalf of BOE Technology Group Co., Ltd. to provide technical assistance in the inter partes review of U.S. Patent No. 7,995,047, which I may abbreviate as “**the '047 Patent**” or refer to as the “**Challenged Patent.**” This declaration is a statement of my opinions on issues related to the unpatentability of claims of the Challenged Patent.

4. I am a salaried employee of Exponent. Exponent charges \$575 per hour for my time plus expenses for work performed in connection with this project. I have received no additional compensation for work in this case, and my compensation does not depend upon the contents of this report, any testimony I may provide, or the ultimate outcome of the case.

II. EXPERIENCE AND QUALIFICATIONS

5. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications are stated more fully in my curriculum vitae, which has been provided as Appendix A. My CV also lists publications on which I am a named author and identifies parties on behalf of whom I have previously provided expert testimony within the past four years. Here, I provide a brief summary of my qualifications.

6. I am a Principal Engineer in Exponent’s Electrical Engineering and Computer Science practice. I received my B.A. in Electrical Engineering from the University of Connecticut in 2002 and an M.A. and Ph.D. in Electrical Engineering from Princeton University in 2004 and 2007, respectively.

7. During my time at the University of Connecticut and through a grant from the National Science Foundation, I designed and implemented devices for people with disabilities. This included the design and manufacture of analog and digital control systems for devices including go-karts and electronic lifts.

8. Before joining Princeton University, I worked as a design engineering intern at General Electric Industrial Systems. There I designed and implemented analog and digital circuits. This work included the implementation of current sense devices for feedback in power supplies.

9. At Princeton University my research was focused on designing and fabricating pixel circuits on non-conventional substrates for driving liquid-crystal displays (“LCDs”) and active-matrix organic light emitting diode displays (“AMOLEDs”).

10. Throughout my career at Exponent, I have worked extensively on AMOLED and LCD displays including backlight systems based on LEDs, driver circuits, thin-film transistor and pixel architectures, and waveguides.

11. I am a licensed Professional Engineer in the State of Connecticut, the State of Georgia, the Commonwealth of Massachusetts, the State of New Jersey, the State of New York, the Commonwealth of Pennsylvania, the State of Rhode Island, and in the State of Texas. I am also designated as a Model Law Engineer by the National Council of Examiners for Engineering.

12. I am a Senior Member of the Institute of Electrical and Electronics Engineers (“IEEE”), which is the world’s largest technical professional organization dedicated to advancing technology for the benefit of humanity.

13. Therefore, based on my education, professional experience, scholarly books and publications, I am an expert in the relevant field of the Challenged Patent at issue here and have been an expert in this field since before the Challenged Patent was filed with the United States

Patent and Trademark Office (“USPTO”). I am familiar with how a person having ordinary skill in the art would have understood and used the terminology found in the Challenged Patent at the time of its filing.

III. TASK SUMMARY AND MATERIALS REVIEWED

14. I have been asked to review the Challenged Patent and its prosecution history, to provide an understanding of the technology relevant to the Challenged Patent, to review certain prior-art references, and analyze whether or not those references disclose or teach limitations of claims from the Challenged Patent. The opinions stated in this declaration are from the perspective of a person of ordinary skill in the art.

IV. LIST OF EXHIBITS

15. In forming my opinions, I have reviewed the Challenged Patent, its prosecution history and references cited by the Examiner, the materials cited in the List of Exhibits, and the materials cited throughout my declaration.

Ex.	Description of Exhibits
1001	U.S. Patent No. 7,995,047 (“’047”)
1002	File History of U.S. Patent No. 7,995,047 (“’047FH”)
1004	U.S. Patent Pub. No. 2006/0170629 (“Baek”)
1005	U.S. Patent Pub. No. 2005/0231241 (“Date”)
1006	International Patent Pub. No. WO2006/080260 (“Inomoto”)
1007	U.S. Patent Pub. No. 2005/0017765 (“Sasaki”)
1009	John A. Camara, ELECTRICAL ENGINEERING REFERENCE MANUAL FOR THE ELECTRICAL AND COMPUTER PE EXAM, 6th ed. (Professional Publications, Inc.: 2002), ISBN: 1-888577-56-8 (“Camara”)
1010	Willem den Boer, ACTIVE MATRIX LIQUID CRYSTAL DISPLAYS, 1st ed. (Newnes: 2005), ISBN: 0-750678-13-5 (“den Boer”)

Ex.	Description of Exhibits
1011	M.K. Han, “AM backplane for AMOLED,” Proc. Of ASID 6 (Oct. 8-12, 2006): 53-58 (“Han”)
1012	U.S. Patent Pub. No. 2006/0227091 (“Nohtomi”)
1013	U.S. Patent Pub. No. 2006/0255787 (“Schaffer”)
1014	U.S. Patent Pub. No. 2003/0025120 (“Chang”)

Other than the prosecution history, Ex. 1002, respectively, all citations to exhibits reference original page numbers found in the underlying document, and unless noted, all emphases have been added.

V. SUMMARY OF CONCLUSIONS AND GROUNDS FOR CHALLENGE OF '047 PATENT

16. After reviewing the materials identified in the List of Exhibits, I have concluded that each of Claims 1-10 (“**Challenged Claims**”) of the '047 Patent would have been anticipated and/or obvious to a person of ordinary skill in the art, based on the following grounds. My opinions in this declaration are consistent with the opinions in my declaration submitted in IPR proceeding, *Samsung Elecs. Co. v. Bishop Display Tech LLC*, IPR2022-00501. The Challenged Claims are anticipated and/or obvious for more than one reason and thus my opinions in this declaration may differ from the opinions in my declaration submitted in the prior IPR.

Ground	Claims	Basis	References
1-2	1-4 and 9	§102/§103	Baek
3	5-6	§103	Baek in view of Date
4	7-8	§103	Baek in view of Inomoto
5	10	§103	Sasaki

VI. UNDERSTANDING OF THE GOVERNING LAW

A. LEVEL OF ORDINARY SKILL IN THE ART

17. When analyzing a patent, I understand that it is important to identify the relevant art pertaining to the patent as well as the level of ordinary skill in that art at the time of the claimed invention. The “art” is the field of technology to which the patent is related.

18. I have been instructed by counsel that the person of ordinary skill in the art is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor’s skill is not determinative of the level of ordinary skill. I further understand that the factors that may be considered in determining the level of skill include: the types of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field. I understand that not all such factors may be present in every case, and one or more of them may predominate.

B. LEGAL STANDARD FOR CLAIM CONSTRUCTION

19. I understand that the first step in determining whether a patent claim would have been anticipated or obvious is to ascertain how a person of ordinary skill in the art would have understood the claim terms.

20. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim, or it can further depend from another dependent claim. I understand that a dependent claim includes all the limitations that it recites, in addition to all the limitations recited in the claim(s) from which it depends.

21. It is my understanding that in proceedings before the USPTO, the claims of a patent are to be construed under what is referred to as the “Phillips standard.” I understand that this means that claim terms of a patent are given the meaning the terms would have to a person of ordinary skill in the art, in view of the description provided in the patent itself and the patent’s file history.

22. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood the disputed claim language to mean. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent, and the patent’s prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

23. I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else. In making this determination, the claims, the remainder of the patent, and the prosecution history are of paramount importance. Additionally, the patent and its prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

24. In comparing the claims of the Challenged Patent to the prior art, I have considered the Challenged Patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

C. ANTICIPATION

25. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in a single prior art reference. I understand that inherency requires showing that the missing descriptive matter in the claim is necessarily or implicitly present in the allegedly anticipating reference, and that it would have been so recognized by a person of ordinary skill in the art. In addition, I understand that an enabling disclosure is a disclosure that allows a person of ordinary skill in the art to make the invention without undue experimentation. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the primary reference has enabling disclosure, to explain the meaning of a term used in the primary reference, and/or to show that a characteristic is inherent in the primary reference.

D. OBVIOUSNESS

26. I understand that the prior art may render a patent claim “obvious.” I understand that two or more prior art references (*e.g.*, prior art articles, patents, or publications) that each disclose fewer than all elements of a patent claim may nevertheless be combined to render a patent claim obvious if the combination of the prior art collectively discloses all elements of the claim and one of ordinary skill in the art at the time would have been motivated to combine the prior art in such a way. I understand that this motivation to combine need not be explicit in any of the prior art, but may be inferred from the knowledge of one of ordinary skill in the art at the time the patent was filed. I also understand that one of ordinary skill in the art is not an automaton, but is a person having ordinary creativity. I further understand that one or more prior art references, articles, patents or publications that disclose fewer than all of the elements of a patent claim may render a patent claim obvious if including the missing element would have been obvious to one of skill in

the art (*e.g.*, the missing element represents only an insubstantial difference over the prior art or a reconfiguration of a known system).

27. I understand that under the doctrine of obviousness, a claim may be invalid if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the art to which the subject matter pertains.

28. To assess obviousness, I understand that I am to consider the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and any secondary considerations to the extent they exist.

29. I understand that any evidence of secondary indicia of non-obviousness should be considered when evaluating whether a claimed invention would have been obvious to one of ordinary skill at the time of invention. These secondary indicia of non-obviousness may include, for example:

- a long felt but unmet need in the prior art that was satisfied by the claimed invention;
- commercial success of processes claimed by the patent;
- unexpected results achieved by the invention;
- praise of the invention by others skilled in the art;
- the taking of licenses under the patent by others; and
- deliberate copying of the invention.

I understand that there must be a nexus between any such secondary indicia and the claimed invention.

30. It is also my understanding that there are additional considerations that may be used as further guidance as to when the above factors will result in a finding that a claim is obvious, including the following:

- the claimed subject matter is simply a combination of prior art elements according to known methods to yield predictable results;
- the claimed subject matter is a simple substitution of one known element for another to obtain predictable results;
- the claimed subject matter uses known techniques to improve similar devices or methods in the same way;
- the claimed subject matter applies a known technique to a known device or method that is ready for improvement to yield predictable results;
- the claimed subject matter would have been “obvious to try” choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a person of ordinary skill in the art;
- there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent’s claims; and
- there is some teaching, suggestion, or motivation in the prior art that would have led a person of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed subject matter.

31. Finally, I understand that a claim may be deemed invalid for obviousness in light of a single prior art reference, without the need to combine references, if the elements of the claim that are not found in the reference can be supplied by the knowledge or common sense of one of ordinary skill in the relevant art.

VII. OVERVIEW OF THE '047 PATENT

32. I have reviewed U.S. Patent No. 7,995,047 (“the '047 Patent”), which is entitled “Current Driving Device.” Ex. 1001.

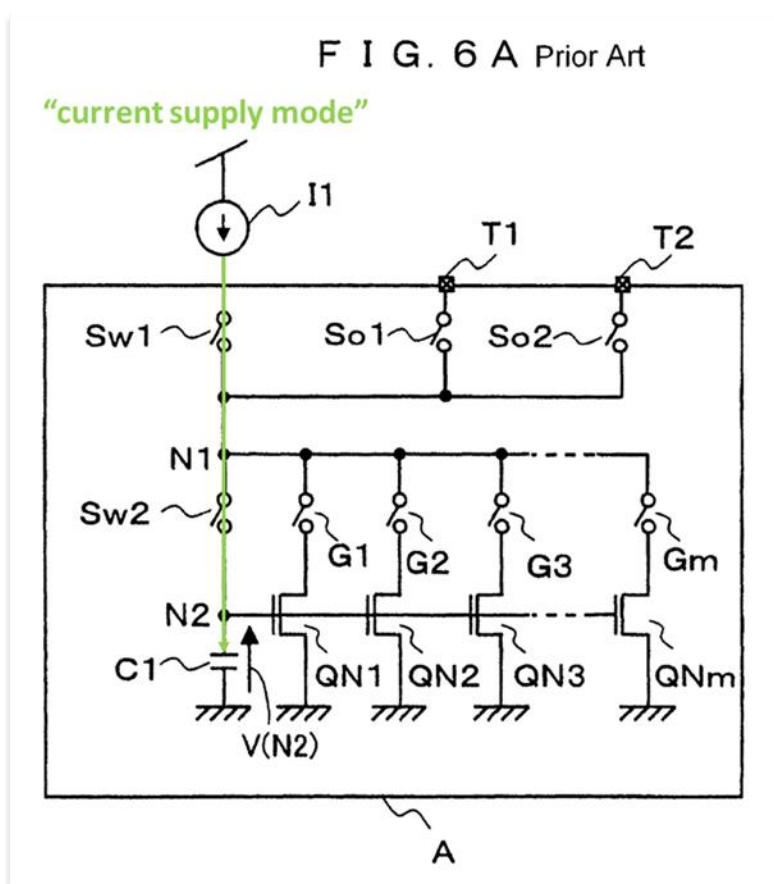
A. PRIORITY DATE FOR CLAIMS OF THE '047 PATENT

33. I understand that the '047 Patent was filed on December 12, 2007, and that it was issued on August 9, 2011. The '047 Patent claims priority to an application filed in Japan on

December 13, 2006. I understand that, regardless of whether the priority date of the '047 Patent is December 12, 2007 (corresponding to its U.S. filing date) or December 13, 2006 (corresponding to the filing date of the Japanese application), the references I rely on qualify as prior art.

B. THE SUBJECT MATTER OF THE '047 PATENT

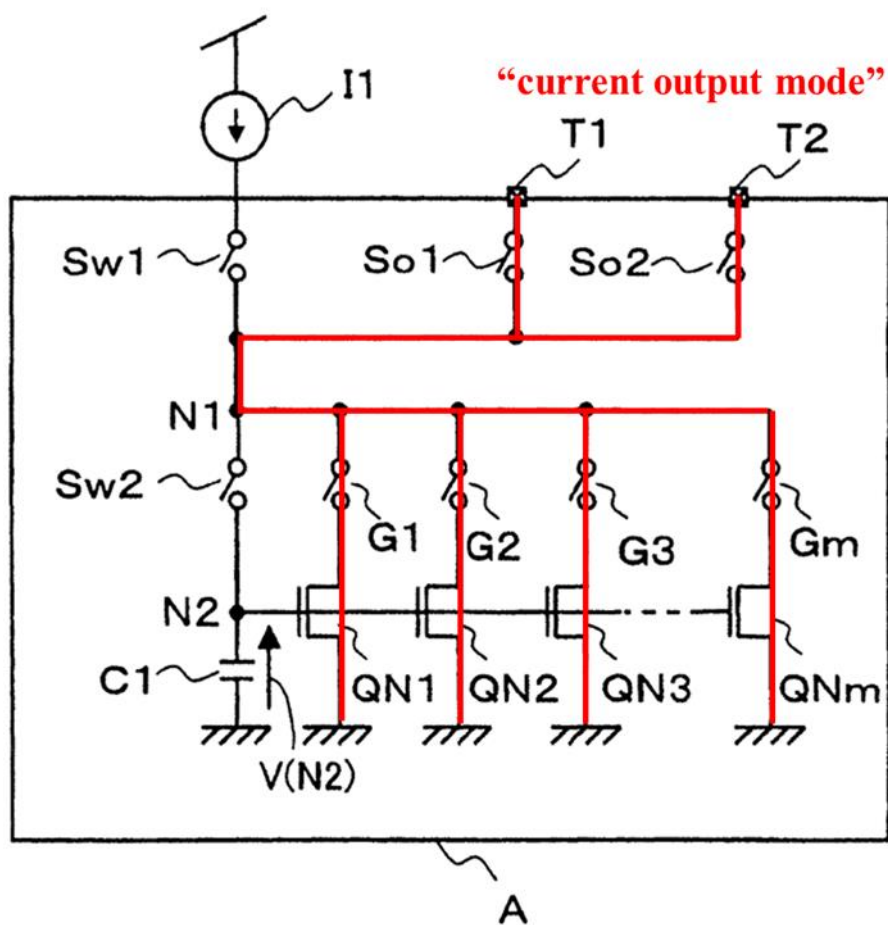
34. The purported “invention” of the '047 Patent relates to a “current driving device” that operates in three modes, including a mode that “charge[s] the voltage holding part” of the device “to a prescribed voltage at a higher speed.” '047 Patent at 3:49-4:3. The '047 Patent discloses a known current driving device that operates in two modes, including “a calibration mode” and a “current output mode.” '047 Patent at 1:40-2:7. Under the known calibration mode, the device’s “voltage holding capacitance element C1 is charged” to “store the reference current generated by the reference current source I1.” '047 Patent at 1:40-59, Figure 6A.



'047 Patent at Figure 6A (annotated).

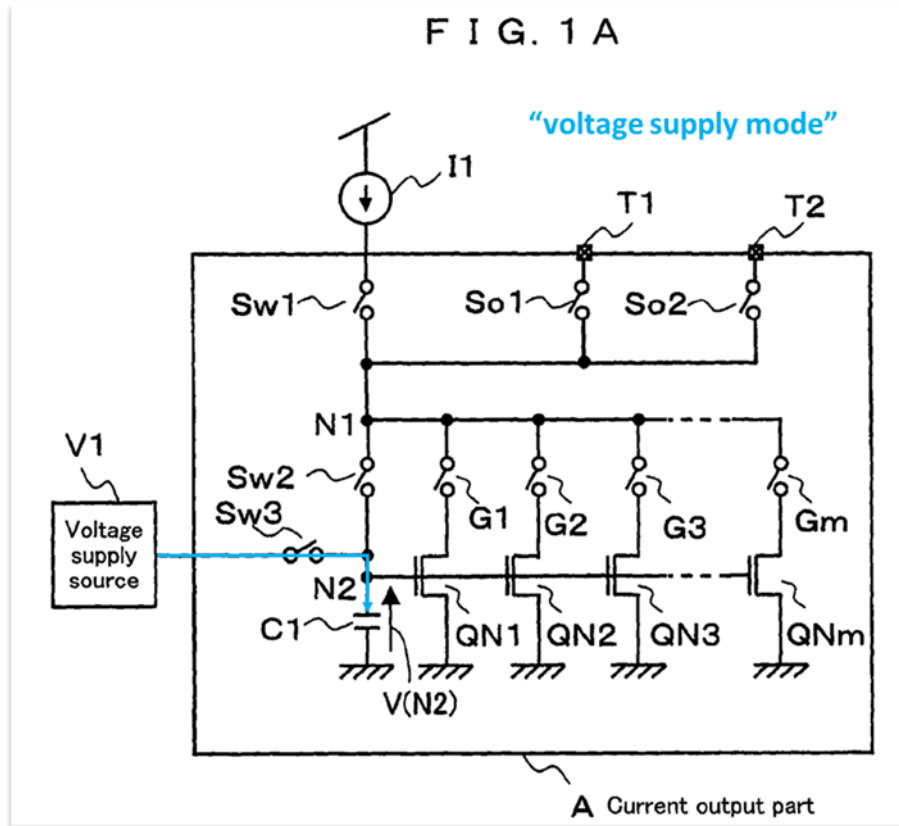
35. Under the known current output mode, the device's "voltage holding capacitance element C1 holds the voltage charged by the calibration action" and the "Nch transistors QN1-QNm output an electric current" from "current output terminals." '047 Patent at 1:60-2:7, Figure 6A.

F I G. 6 A Prior Art



'047 Patent at Figure 6A (annotated).

36. The alleged invention of the '047 Patent relates to a third "voltage supply mode," whereby "the voltage holding capacitance element C1 is charged to a constant voltage ... supplied from the voltage supply source V1." '047 Patent at 7:44-52, Figure 1A.



'047 Patent at Figure 1A (annotated).

C. THE CHALLENGED CLAIMS OF THE '047 PATENT

37. The Challenged Claims are set forth below. I understand that claims 2-5 and 7-9 depend from claim 1 and therefore include all of the limitations from claim 1. I understand that claim 6 depends from claim 5 and therefore includes all of the limitations from claim 5. In the table below, some of the claim elements have been further sub-divided for ease of reference.

Claim Element	Claim Language from '047 Patent
1 (pre)	1. A current driving device, comprising:
1(a)	a first voltage supply source for supplying a first voltage;
1(b)	a first current supply source for supplying a first electric current;
1(c)	a plurality of output terminals; and

Claim Element	Claim Language from '047 Patent
1(d)(1)	a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising
1(d)(2)	a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein:
1(e)	each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,
1(f)	under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit, and
1(g)	under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and
1(h)	under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit.
2	2. The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits, and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common.
3	3. The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode.
4	4. The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode.
5	5. The current driving device according to claim 1, further comprising: a second current supply source for supplying a second electric current that is proportional to said first electric current; and a second current-voltage converting circuit for generating said first voltage by receiving said second electric current, wherein

Claim Element	Claim Language from '047 Patent
	said first voltage supply source controls supplies of said first voltage generated by said second current-voltage converting circuit to said current output circuits.
6	6. The current driving device according to claim 5, wherein said second current-voltage converting circuit comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node.
7	7. The current driving device according to claim 1, further comprising a second voltage supply source with a larger voltage supply capacity than that of said first voltage supply source, wherein the use of said first voltage supply source and the use of said second voltage supply source are switched in accordance with the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits.
8	8. The current driving device according to claim 1, wherein said first voltage supply source is configured to change its voltage supply capacity in accordance with the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits.
9	9. A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device.
10(pre)	10. A current driving device, comprising:
10(a)	a current input switch for controlling connection/disconnection states with respect to a current supply source;
10(b)	a voltage holding circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;
10(c)	a calibration switch interposed between said current input switch and said voltage holding circuit;
10(d)	a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding circuit;
10(e)	a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being connected in series

Claim Element	Claim Language from '047 Patent
	to a corresponding one of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;
10(f)	a connection node provided between said current input switch and said calibration switch;
10(g)	a plurality of current output switches, each being interposed between the connection node and said plurality of current output terminals; and
10(h)	a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit.

D. PROSECUTION HISTORY OF THE '047 PATENT

38. The '047 Patent was filed on December 12, 2007 as Application No. 11/954,659 and claims priority to a foreign application filed December 13, 2006. The USPTO examiner issued a rejection requiring the Applicant to designate Figures 6A, 6B, and 7-9 as prior art since “only that which is old is illustrated.” Ex. 1002 at 105. The Examiner further issued two rejections of claims 1-10 under §102 as being anticipated by Date et al. (U.S. Pat. No. 7,466,166) and by Hashido et al. (U.S. Pat. No. 7,221,349). Ex. 1002 at 105-115.

39. To overcome these rejections, applicants amended independent claim 1 to specify the voltage holding circuit “having a terminal being connected to a reference voltage different from the first voltage” and claim 10 to specify the “voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage” and to add a “connection node provided between said current input switch and said calibration switch.” Ex. 1002 at 126-130. Regarding claim 1, applicants argued the prior art “fails to disclose that a voltage holding circuit has a terminal being connected to a reference voltage different from the first voltage, and under the voltage supply mode, the first voltage is supplied to another terminal of the voltage

holding circuit.” Regarding claim 10, applicants argued the prior art “fails to disclose that the voltage holding circuit has a first terminal and a second terminal, the first terminal being connected to a fixed voltage, and the current driving device includes a high-speed switch for controlling connection/disconnection states of **said voltage supply source with respect to the second terminal of said voltage holding circuit.**” Ex. 1002 at 132-134 (emphasis in original).

40. The claims were subsequently allowed, and the Examiner indicated that the prior art did not teach the following limitations of claim 1: “a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage” and “under said voltage supply mode ... the first voltage is supplied to another terminal of said voltage holding circuit.” ’047FH at 148. The Examiner indicated that the prior art did not teach the following limitations of claim 10: “voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage” and “a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit.” ’047FH at 148. As discussed below, the asserted references disclose these and the other claim limitations.

VIII. LEVEL OF ORDINARY SKILL IN THE ART FOR THE ’047 PATENT

41. In the 2006-2007 timeframe, at the time the Challenged Patent was filed, I believe that a relevant person of ordinary skill in the art would have had an undergraduate degree in electrical engineering (or equivalent subject) together with two or three years of experience in designing circuits for driving light-emitting devices including organic light-emitting diodes, or a Ph.D. with experience in the same. This description is approximate, and a higher level of education or skill might make up for less experience, and vice versa.

42. I would have qualified as a person of ordinary skill in the art at least as of the earliest possible claimed priority date of the ’047 Patent (December 13, 2006, the Japanese priority date),

and that I have a sufficient level of knowledge, experience, and education to provide an opinion in the field of the Challenged Patent. I am familiar with what a person of ordinary skill in the art knew at that time because of my lengthy experience with engineering subjects of a similar nature to the concepts presented in the Challenged Patent. Additionally, at that time, I was familiar with the general subject material in the cited prior art in this Declaration.

IX. CLAIM CONSTRUCTION

43. In my opinion, and for the purposes of this declaration, I apply the ordinary and customary meaning of the claim terms of the Challenged Patent.

X. TECHNOLOGY BACKGROUND AND STATE OF THE ART FOR THE '047 PATENT

44. In the subsections below, I describe some of the basic principles of electrical engineering that would have been well-known to a person of ordinary skill in the art in 2006-2007 timeframe, and long before.

A. EXEMPLARY REFERENCES CORROBORATING THE GENERAL ENGINEERING KNOWLEDGE

a. Camara Handbook (Ex. 1009)

45. As an example of general electrical engineering knowledge, Exhibit 1009 is the handbook published in 2002, entitled “Electrical Engineering Reference Manual,” by John Camara (“Camara”). As implied by the title, this was a basic engineering reference manual that engineers used since 2002 to study for their Professional Engineer (PE) examinations. The cover of Camara states: “The most comprehensive resource available for the electrical PE exam.” Ex. 1009 (Camara). This handbook covers topics on the electrical and computer engineering professional engineering exam (including electric and electronic circuits), and it evidences the level of knowledge one with a bachelor’s degree in electrical engineering would have possessed.

b. den Boer Text (Ex. 1010)

46. As an example of engineering knowledge pertaining to flat-panel displays, Exhibit 1010 is a textbook published in 2005, entitled “Active Matrix Liquid Crystal Displays: Fundamentals and Applications,” by Willem den Boer (“**den Boer**”). This book evidences the state of the art of flat-panel displays as of 2005, including liquid crystal displays and organic electroluminescence displays, and provides a perspective of the knowledge of one of ordinary skill. In this book, thin-film transistors, drive electronics, and drive methods, including compensation methods used for high-speed performance, are discussed in terms of their development, solutions to problems associated with increases in display size, and the rapid developments in these technologies.

c. Han Article (Ex. 1011)

47. As an example of specific pixel circuit design general engineering knowledge pertaining to flat-panel display, Exhibit 1011 is a paper published by the Asian Society for Information Display (“ASID”) in 2006, entitled “AM backplane for AMOLED,” by Min-Koo Han et al. (“**Han**”). I am familiar with the Journal of the Society of Information Display, and ASID is the Asian branch of the SID.

B. GENERAL DISPLAY BACKGROUND

48. It was known that the basic function of a display is to visually present information to a user. There are many flat panel display technologies, including liquid crystal displays (“LCDs”) and organic light-emitting diode (“OLED”) displays. To enable those displays, particularly active-matrix display technologies, switches in the form of electronic transistors were well known, including a subcategory of transistors called thin-film transistors (“TFT”). Ex. 1010 (den Boer) at p. 29-39 (Sections 2.3-2.6). It was known that an active-matrix display includes arrays of TFTs that worked with pixels, source (data) lines, and gate drivers. Ex. 1010 (den Boer)

at 39-43 (Section 2.7). As an example, it was known that an HDTV could have “1080x1920 pixels.” Ex. 1010 (den Boer) at 176 (Section 6.6). It was further known that individual pixels would be comprised of three sub-pixels (*e.g.*, red-green-blue). Ex. 1010 (den Boer) at p. 3, 41, 144. Therefore, in such a known device, there would be 6,220,800 pixels (1920x1080x3) that are actively controlled to create an image.

49. It was also known to drive the pixels using a “TFT pixel array circuit (Figure 2.17) [with] select buslines, data buslines, a TFT at each pixel, and a storage capacitor ... at each pixel.” Ex. 1010 (den Boer) at 39-40. The storage capacitor “acts as a buffer,” helping control gray level of pixels. Ex. 1010 (den Boer) at 27, 39. It was known that panels also include source drivers that use red-green-blue data to drive the columns of lines running vertically in the displays and provide the value of brightness required of each pixel. The gate or row drivers select the rows of lines running horizontally within the displays, and they turn on the switches within pixels of each row in a row-by-row succession. Ex. 1010 (den Boer) at p. 93-98 (Section 4.2).

50. It was known that OLEDs are semiconducting devices comprised of organic materials that convert electrical energy to light, much like LEDs. In OLED displays, the individual pixels comprise OLEDs that are current-driven devices, which means that a given OLED’s brightness is set by a fixed current. Ex. 1011 (Han) at p. 53 Section 1. It was known that a pixel’s color and brightness are electronically adjusted by setting the current and therefore the brightness of each pixel through the manipulation of TFT(s).

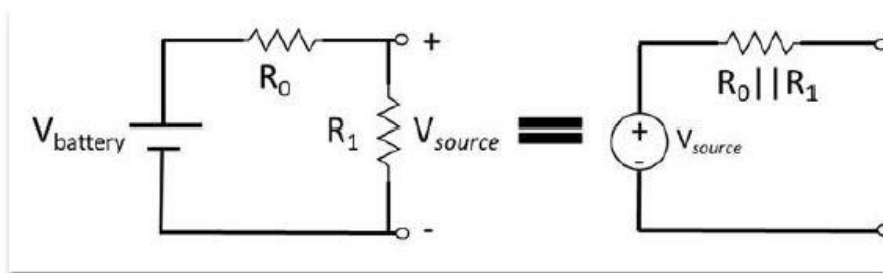
51. It was known that if any pixels had non-uniform characteristics, that could lead to dark dots, bright dots, and other undesirable characteristics in the display. However, it was known that flat-panel displays are made with motherglass, in which microelectronics circuits (including the TFTs) are fabricated across several square meters of surface, and variations in electronic

characteristics or properties are inevitable. Ex. 1011 (Han) at p. 53 (Introduction). Because of known variations in the electronic characteristics across the motherglass and variations in the characteristics of TFTs, it was known to use compensation and calibration to adjust for the variations. Ex. 1011 (Han) at p. 53 at Abstract (“A number of TFT active matrix pixel circuits have been developed in order to compensate for TFT parameter variations ...”), Introduction (“Poly-Si TFT pixel circuit should compensate the non-uniform characteristics of the current, which originate from the inherent process variation of the crystal growth in polycrystalline film.”).

C. BASIC CIRCUITS FOR DRIVING DISPLAYS

a. Voltage supply source / Voltage supply mode

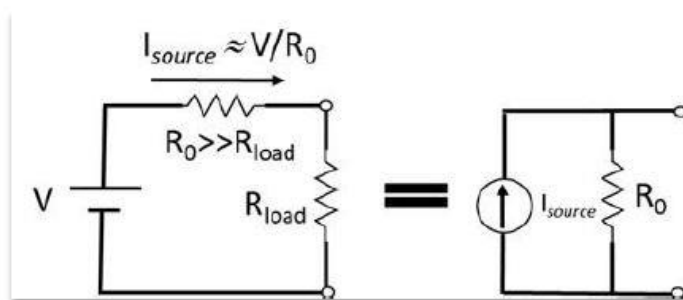
52. It was known that an ideal independent voltage source is modeled as a two-terminal device that has a fixed voltage across its terminals, regardless of the current through it or the load that it is driving. In a generic real-world application, voltage sources can be modeled as an ideal voltage source with internal resistance. Circuitry was well-known to provide voltage sources at various voltage levels to drive components (*e.g.*, capacitors) within systems including drive electronics for flat panel displays. *See, e.g.*, Ex. 1009 (Camara) at p. 26-4. A simple voltage source includes, for example, a battery with low internal resistance R_0 having an output voltage V_0 across R_i that can be used to drive downstream circuits.



There are alternative means to create voltage sources using transistors, transformers, buffers, and repeaters, for example, and a person of ordinary skill in the art would have the requisite experience to use and understand their role in circuitry.

b. Current supply source / Current supply mode

53. It was known that an ideal independent current source is modeled as a two-terminal device that delivers a fixed current flow through its terminals, regardless of the voltage across its terminals and the load that it drives. See, e.g., Ex. 1009 (Camara) at p. 26-4, 26-5. A simple current source includes, for example, a voltage source in series with a high resistance (R_0) that is much higher than the load resistance (R_{load}) such that the current (I_{source}) is essentially constant, as depicted below.

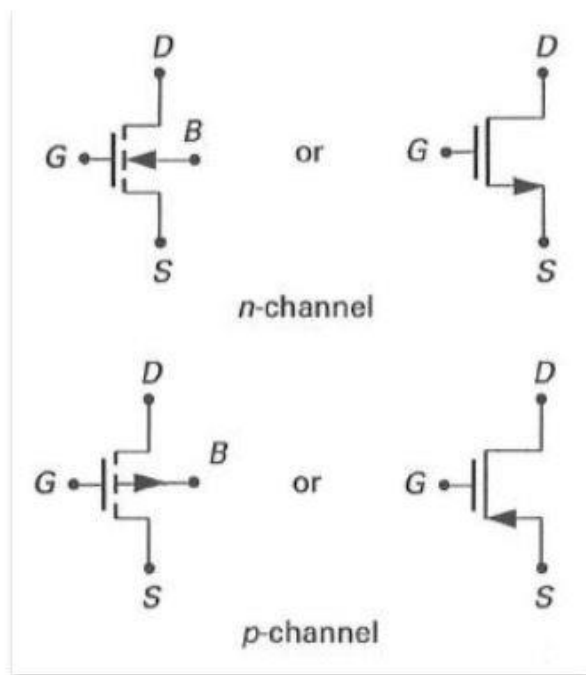


There are alternative means to create microelectronic current sources using transistors, diodes, and op-amps (operational amplifiers), for example, and a person of ordinary skill in the art would have the requisite experience to use and understand their role in circuitry.

c. Voltage-current converting circuit

54. It was known that the conversion of a voltage signal to a current signal can be accomplished with microelectronic devices that take a voltage input and produce a corresponding output current based on some transconductance of the electronic device. A MOSFET was one known type of electronic device that can be configured to take an input voltage (V_G) on its gate

terminal to produce an output current flowing between its drain and source terminals (I_D). See, e.g., Ex. 1009 (Camara) at p. 43-31. An example is shown below.



Ex. 1009 (Camara) at p. 43-32 (Figure 43.37(d)). It was known that other types of semiconductor devices can perform the same function, for example, a bipolar junction transistor. A person of ordinary skill in the art would have the requisite experience to use and understand a MOSFET, which is a basic electronic device.

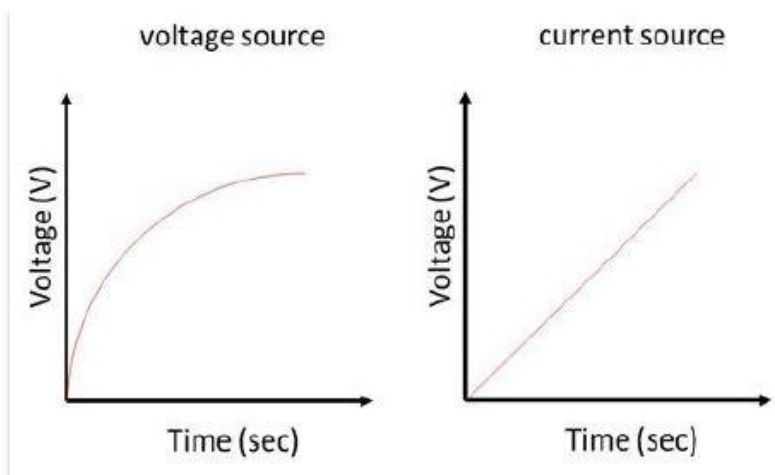
d. Capacitors

55. It was known that a capacitor is an electronic component that has the ability to store charge. Ex. 1009 (Camara) at p. 27-9. It was also known to use capacitors in pixel circuits, for example, as a buffer. Ex. 1010 (den Boer) at 27, 39. When a capacitor is being charged, the time it takes for a capacitor to increase its stored charge depends on its resistance and capacitance. It was known that RC (resistance multiplied by capacitance) represents the time delay. Ex. 1009 (Camara) at p. 30-2. A fundamental and well-known equation governs how a capacitor is charged and discharged,

$$I = C \frac{dV}{dt}$$

where the current (I) through a capacitor is equal to its capacitance (C) multiplied by the rate of change of the voltage across the capacitor $\frac{dV}{dt}$. Ex. 1009 (Camara) at p. 29-4.

56. It was known that the voltage rise on a capacitor increases exponentially when the capacitor is driven by a voltage source; however, it was also known that a linear voltage rise is expected on a capacitor with a current source, as shown below. Ex. 1009 (Camara) at p. 30-6, 30-7. Thus, voltage sources were known to charge the capacitor faster than current sources. A representative figure showing the charging of a capacitor with a voltage source and current source, respectively, is shown below.



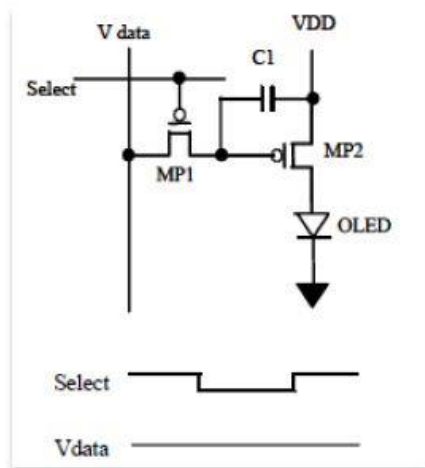
It was known that a small current may not be sufficient to charge a capacitor within a given amount of time (*e.g.*, frame time), as compared to charging the same capacitor with a voltage source.

57. The use of a voltage source to charge the storage capacitor is one aspect of the purported invention of the '047 Patent. Ex. 1001 ('047 Patent) at 3:25. As described above, a person of ordinary skill in the art would have been aware that different amounts of time are required to charge capacitors based on whether a current source (current programming) or a voltage

source (voltage programming) is applied. A person of ordinary skill in the art would have also known that a voltage source can be used to more quickly charge a storage capacitor based on the characteristics of a capacitor.

e. Voltage and Current Programming

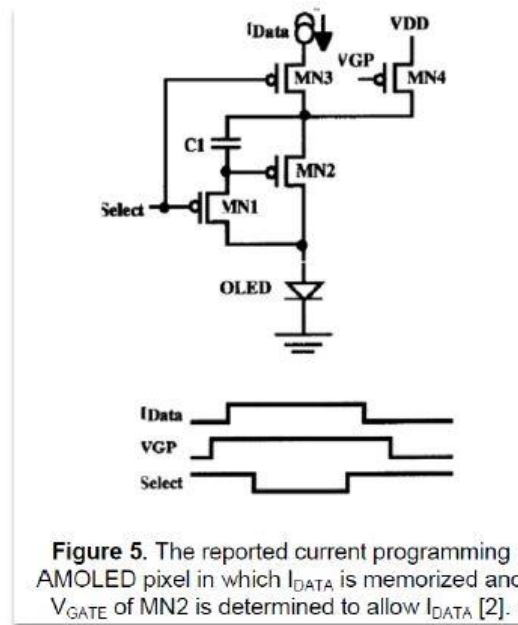
58. It was known that conventional OLED drivers relied on two TFTs as shown below.



Ex. 1011 (Han) at Figure 1(a). In this configuration, transistor MP2 drives the current for the OLED, and transistor MP1 is a switch that samples and holds the voltage on the storage capacitor C1. It was known that variations in TFT threshold voltage and series resistances change the current output to the OLED and therefore change the display brightness. For example, Figure 1(b) of Han reports “brightness non-uniformity (17%) of the conventional 2-TFT pixel.” Ex. 1011 (Han) at p. 54. To compensate for this non-uniformity, current programming schemes have been developed.

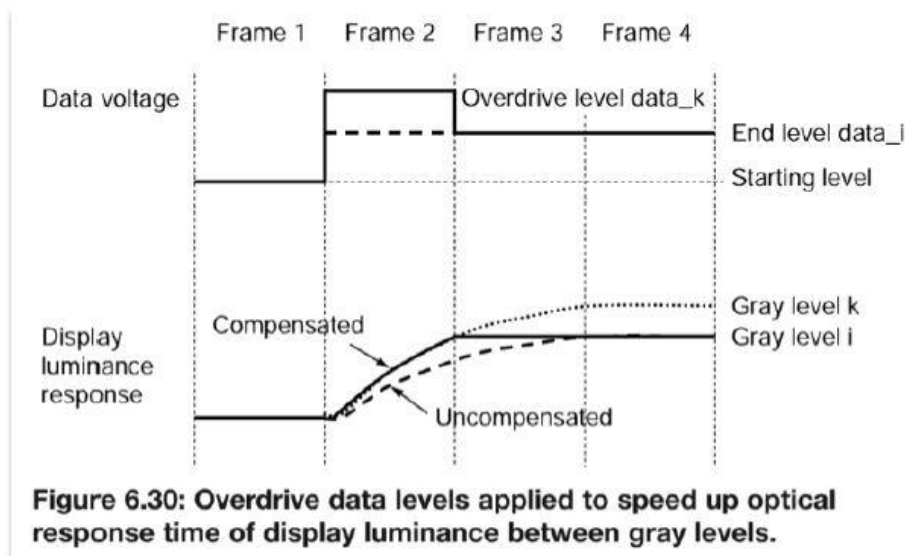
59. It was known that in order to compensate for variation in TFT threshold voltage and mobility, current programming was used for driving OLEDs. Ex. 1011 (Han) at p. 53 (“The current programming pixel circuits can compensate mobility variation as well as threshold voltage variation”). It was known that using current-programming, a current (as opposed to a voltage) is supplied to the pixel to charge a storage capacitor. A basic current-programming circuit (Figure 5

of Han) is shown below. In this circuit, the current I_{DATA} charges capacitor C1 of the driving TFT until transistor MN2 can turn on. By using a current source I_{DATA} to program the pixel, the current charging capacitor C1 remains constant even if there are variations in TFT threshold voltage or mobility.



Ex. 1011 (Han) at Figure 5.

60. One known problem with current programming was that the rate at which a storage capacitor is charged can limit the speed of the display. For example, capacitance within flat panel display pixels provided a slower response time for charging, and overvoltage compensation schemes were implemented to counter the slow response time. In the example shown in Figure 6.30, uncompensated pixels with high capacitance were unable to attain the brightness level required within a frame of the image; hence, extra drive voltage was applied to enable a compensated response to attain the appropriate brightness level within the given amount of time.



Ex. 1010 (den Boer) at p. 168 (Figure 6.30).

61. The '047 Patent discloses that the ability of a small reference current to charge a holding capacitive element becomes insufficient when the current value of the reference current source is very small; hence, a voltage supply (pre-charge) is used to enable faster charging of the holding capacitor. The voltage supply is very similar to the compensation technique described in the den Boer text at Section 6.5.1.

With this method, however, the capacity for charging/discharging the voltage holding capacitance element C1 becomes insufficient when the current value of the reference current source I1 is very small, so that it is difficult to charge the current of the Nch transistors QN1-QNm to accurately meet the value of the current from the reference current source I1 within the calibration period. FIG. 9 shows the state where the voltage holding capacitance element C1 is insufficiently charged because the reference current is very small.

Ex. 1001 ('047 Patent) at 3:1-9.

62. A person of ordinary skill in the art, when faced with the issue of delays in capacitor charging, would have known that the use of a voltage source would allow for a quicker charge time. Furthermore, as described above, the topics of voltage supply sources, current supply

sources, capacitor charging, voltage-current converting circuit, and current programming were all well-known to a person of ordinary skill in the art.

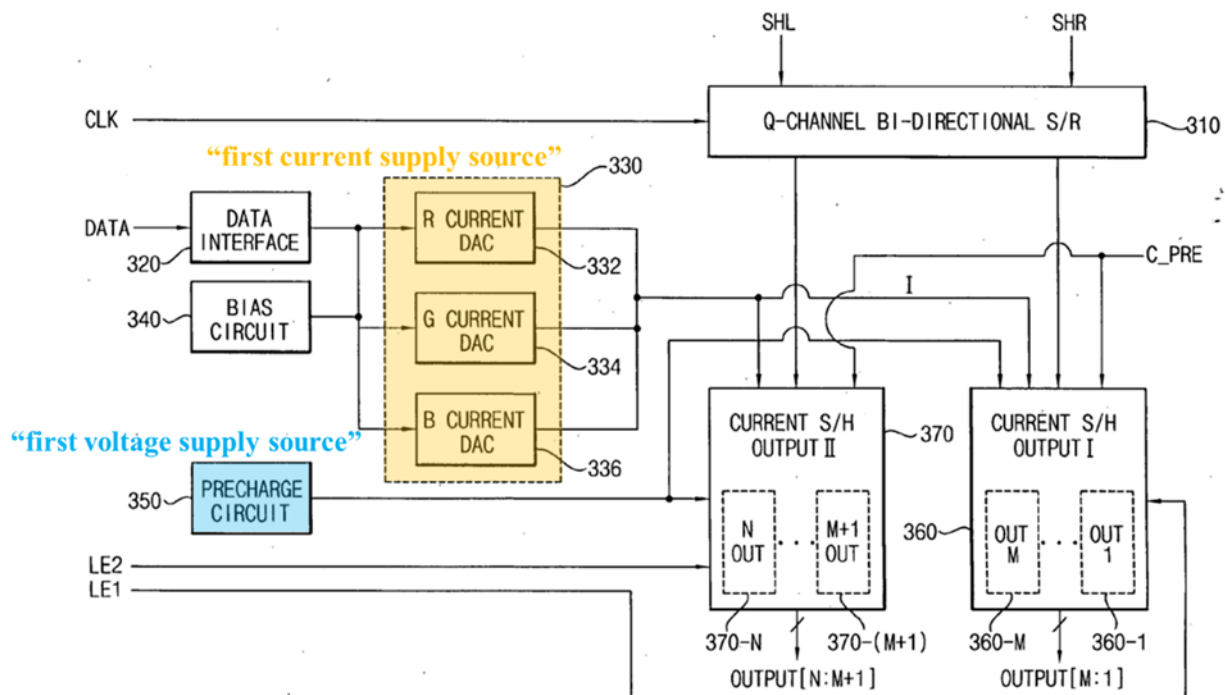
XI. GROUND OF UNPATENTABILITY

A. GROUND 1-2: BAEK

a. Overview of Baek

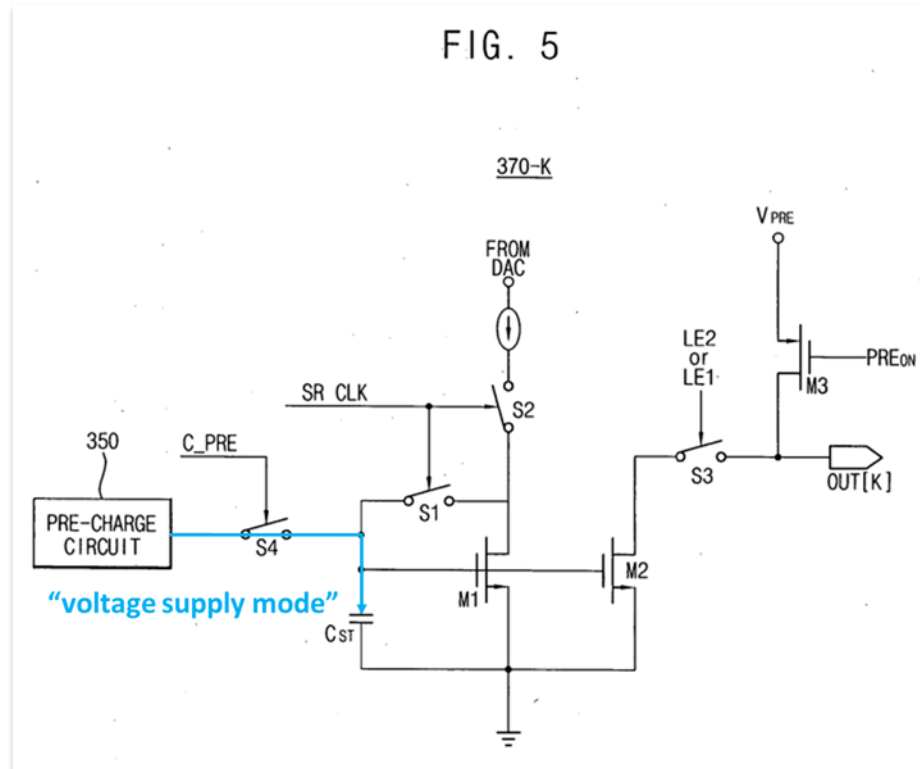
63. “Baek” refers to United States Patent Application Publication No. 2006/0170629, entitled “Display Driver Circuit, Current Sample/Hold Circuit and Display Driving Method Using the Display Driver Circuit.” Baek names Jong-Hak Baek as the sole inventor and was assigned to Samsung Electronics Co., Ltd. Baek was filed in the United States on January 27, 2006 and published on August 3, 2006. Thus, Baek published more than one year before the earliest possible US priority date of the ’047 Patent. Accordingly, I understand that Baek qualifies as prior art to the ’047 Patent.

64. Similar to the ’047 Patent, Baek is directed to a “display driver circuit” that “drive[s] a display panel ... using a smaller current.” Baek at [0019], [0063]. For example, as shown in Figure 3, Baek discloses a “display driver circuit” that includes a plurality of “current sample/hold circuits 370-(M+1) through 370-N” that operate in three modes. Baek at [0056], [0058], [0063]. A “current digital-to-analog conversion unit 330” supplies the “current sample/hold circuits” with “analog gray-scale current,” and a “pre-charge circuit 350” supplies them with a “pre-charge ... voltage.” Baek at [0044], [0056], [0062], Figure 3.



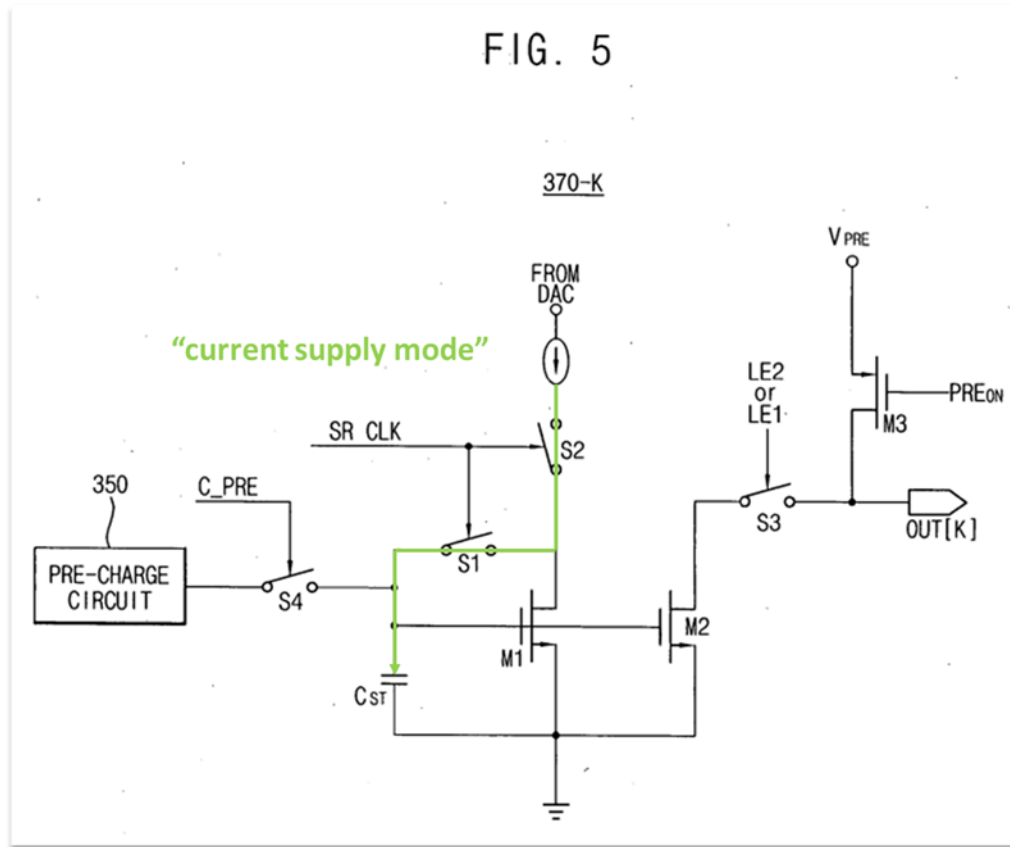
Baek at Figure 3 (annotated).

65. As depicted in Figure 3, each of these “current sample/hold circuits 370-(M+1) through 370-N” have the same inputs, but each has a separate output. One of these current sample/hold circuits is depicted in Figure 5, which depicts these common inputs and the individual output (“OUT[K]”). During a pre-charge mode, the “switch S4” is “turned on” and switches S1 and S2 are turned off such that pre-charge circuit 350 “pre-charge[s] a voltage of the storage capacitor CST to a voltage level slightly lower than a threshold voltage of the first transistor M1.” Baek at [0057], [0062].



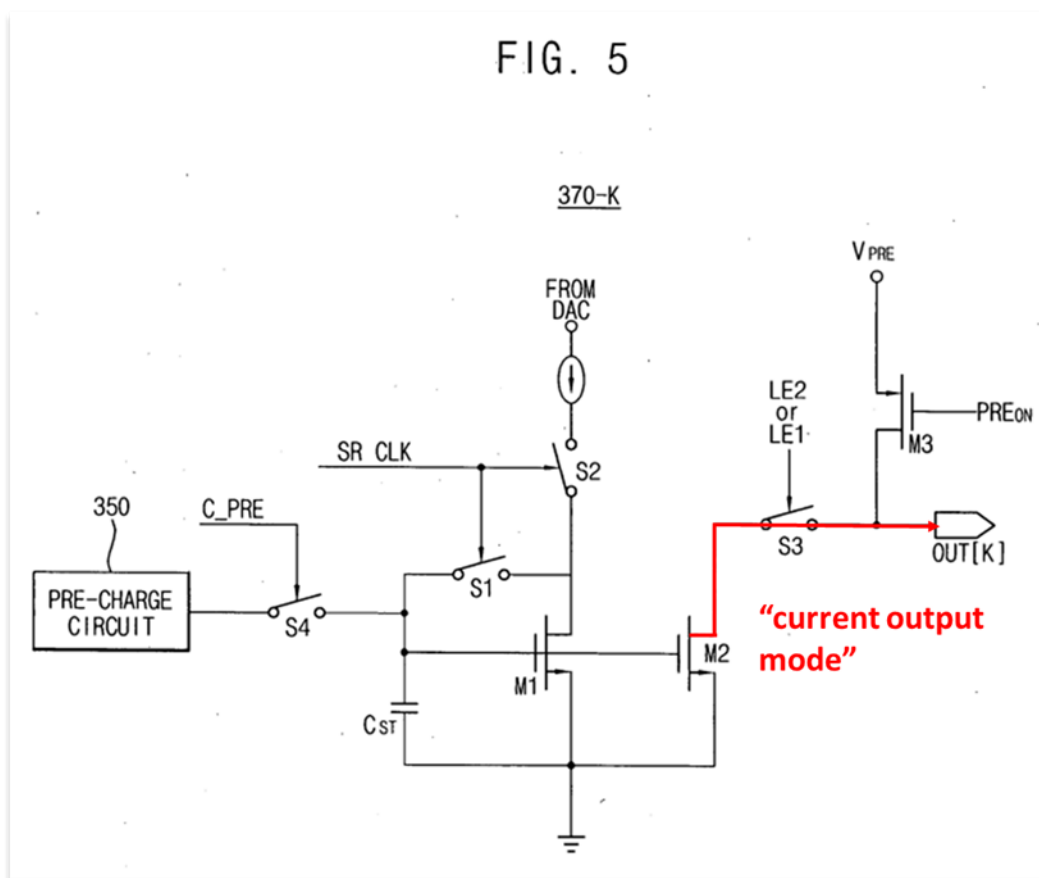
Baek at Figure 5 (annotated).

66. During a current supply mode, switch S4 is turned off, and switches S1 and S2 are “turned on” such that “storage capacitor C_{ST} ... charges the analog gray-scale current” from “current digital-to-analog conversion unit 330” to produce a voltage at the terminal of the capacitor C_{ST} coupled to the gate of transistor M1. Baek at [0056]-[0057].



Baek at Figure 5 (annotated).

67. Finally, during a current output mode, the second transistor M2 “output[s] the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current.” Baek at [0058].



Baek at Figure 5 (annotated).

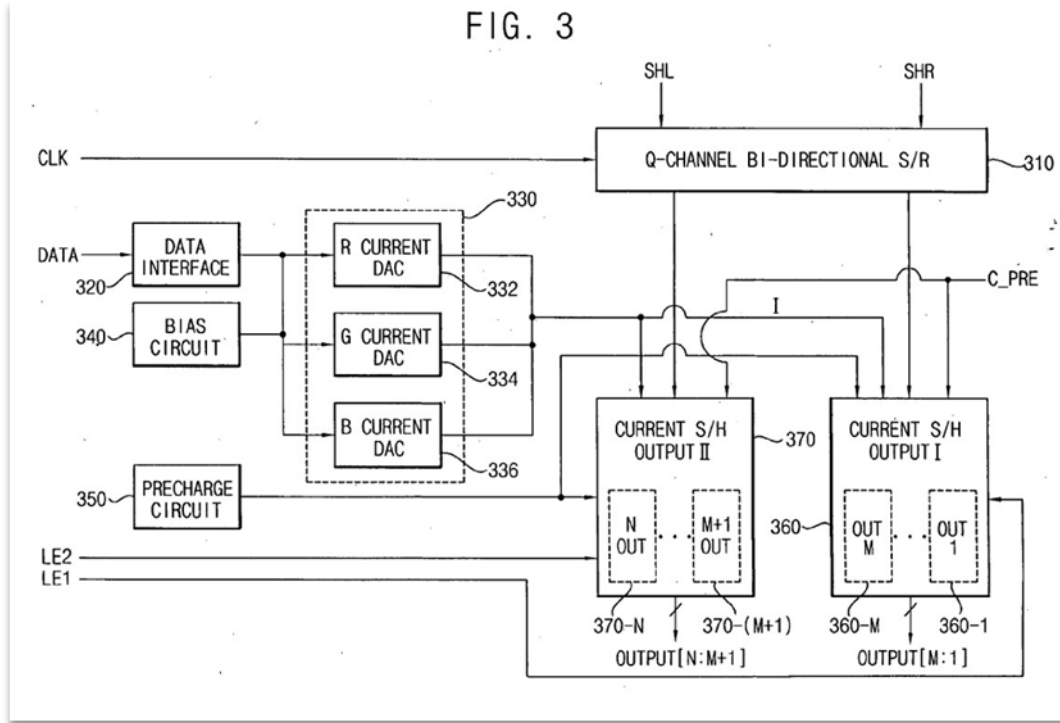
b. Claim 1

i. 1(pre): “A current driving device, comprising:”

68. This limitation is disclosed and at minimum rendered obvious by Baek.

69. To the extent the preamble is limiting, Baek discloses a current driving device (*e.g.*, “display driver circuit”). Baek at [0035]-[0036], [0064], Figure 3.

70. For example, Baek discloses a “display driver circuit” that is used for “current-driven active matrix type OLED display devices” as shown in Figure 3. Baek at [0035], [0064].

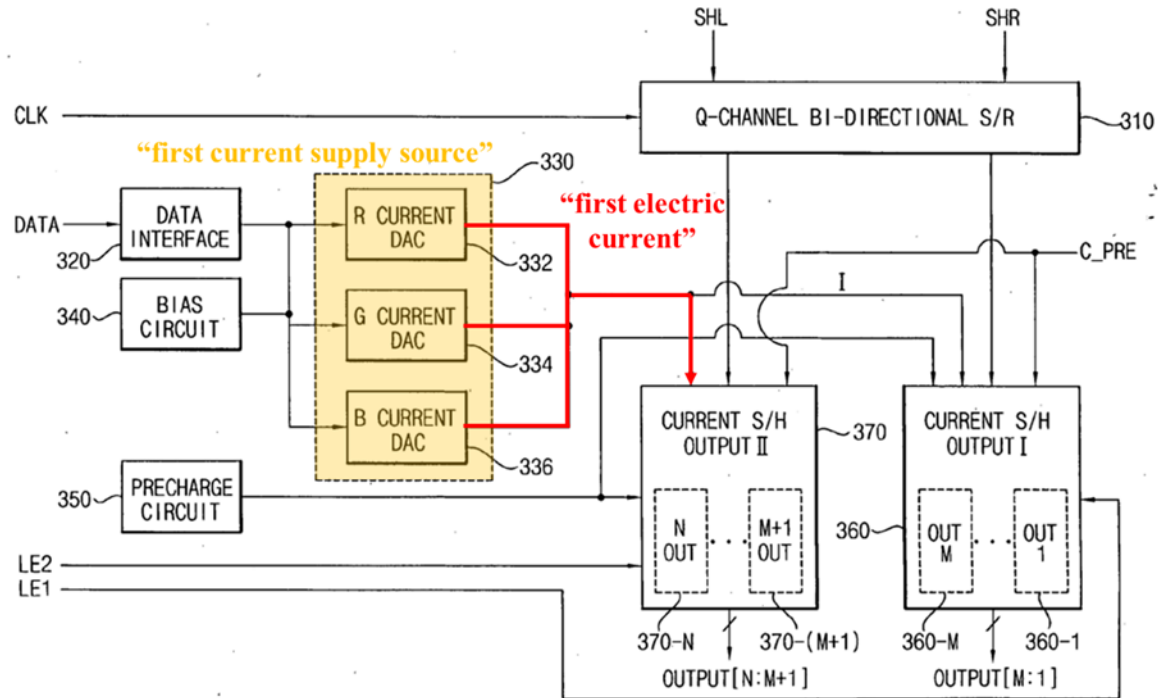


Baek at Figure 3; see [0036] (describing circuitry within “display driver circuit”).

ii. 1(a): “a first voltage supply source for supplying a first voltage;”

71. This limitation is disclosed and at minimum rendered obvious by Baek.

72. Baek discloses a first voltage supply source for supplying a first voltage (*e.g.*, “pre-charge circuit 350” supplying “voltage”). Baek at [0026], [0028], [0036], [0055], [0062], Figures 3, 5.



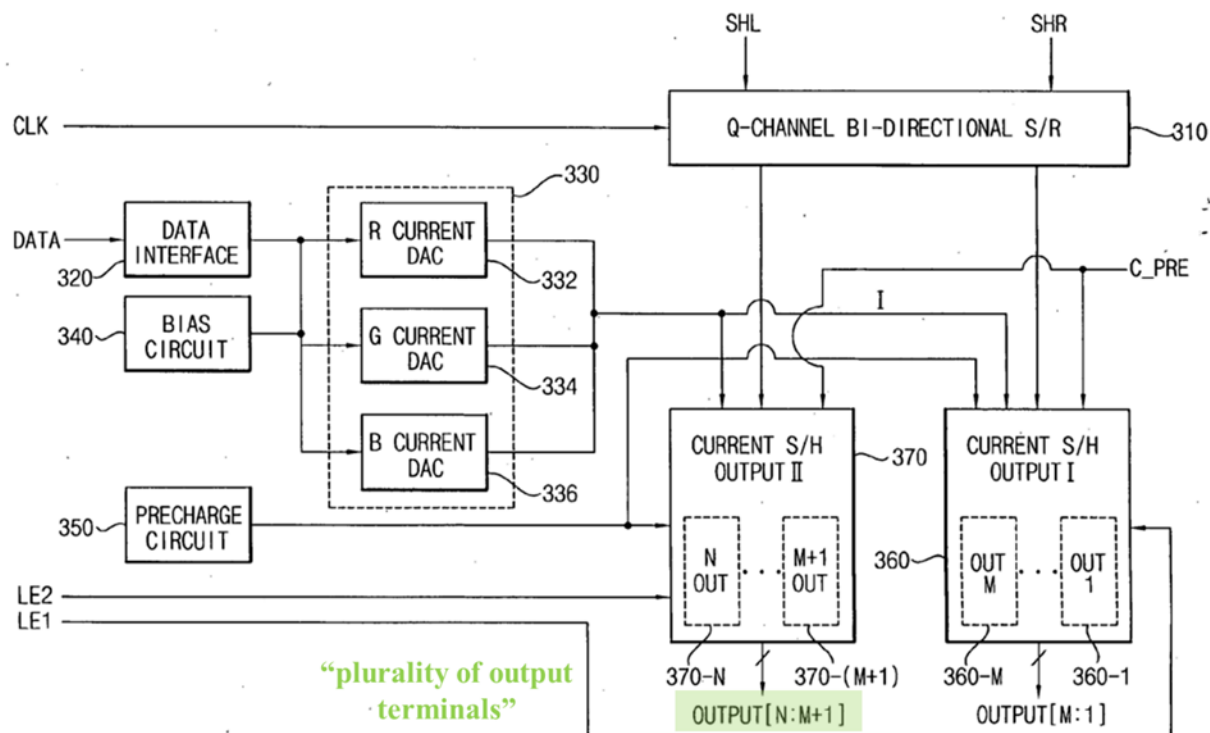
Baek at Figure 3 (annotated), *see also* Baek at Figure 5.

76. For example, Baek discloses a "current digital-to-analog conversion unit 330" that "convert[s] gray-scale data provided from the data interface circuit 320 to an analog gray-scale current" (annotated red) that is "applied" to "current sample/hold circuit[s]." Baek at [0036], [0044], [0055]-[0056].

iv. 1(c): "a plurality of output terminals;"

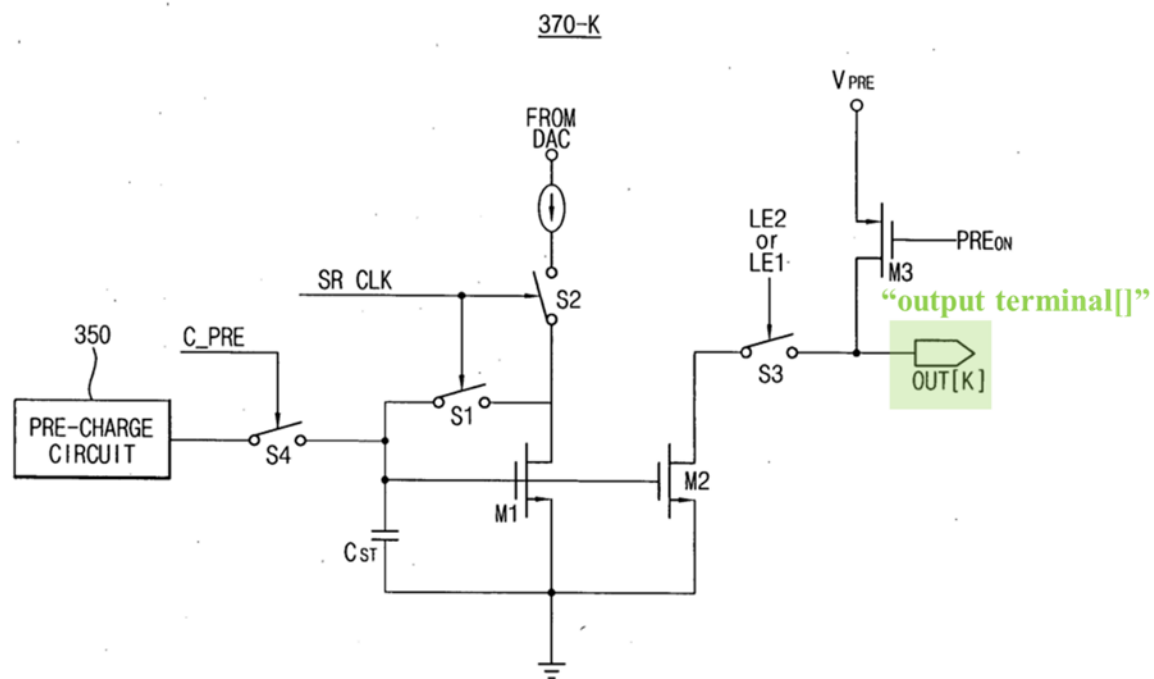
77. This limitation is disclosed and at minimum rendered obvious by Baek.

78. Baek discloses a plurality of output terminals (*e.g.*, "output terminal[s]"). Baek at [0045], [0048]-[0049], [0054], [0058], [0063], [0065], Figures 3, 5.



Back at Figure 3 (annotated).

FIG. 5



Baek at Figure 5 (annotated).

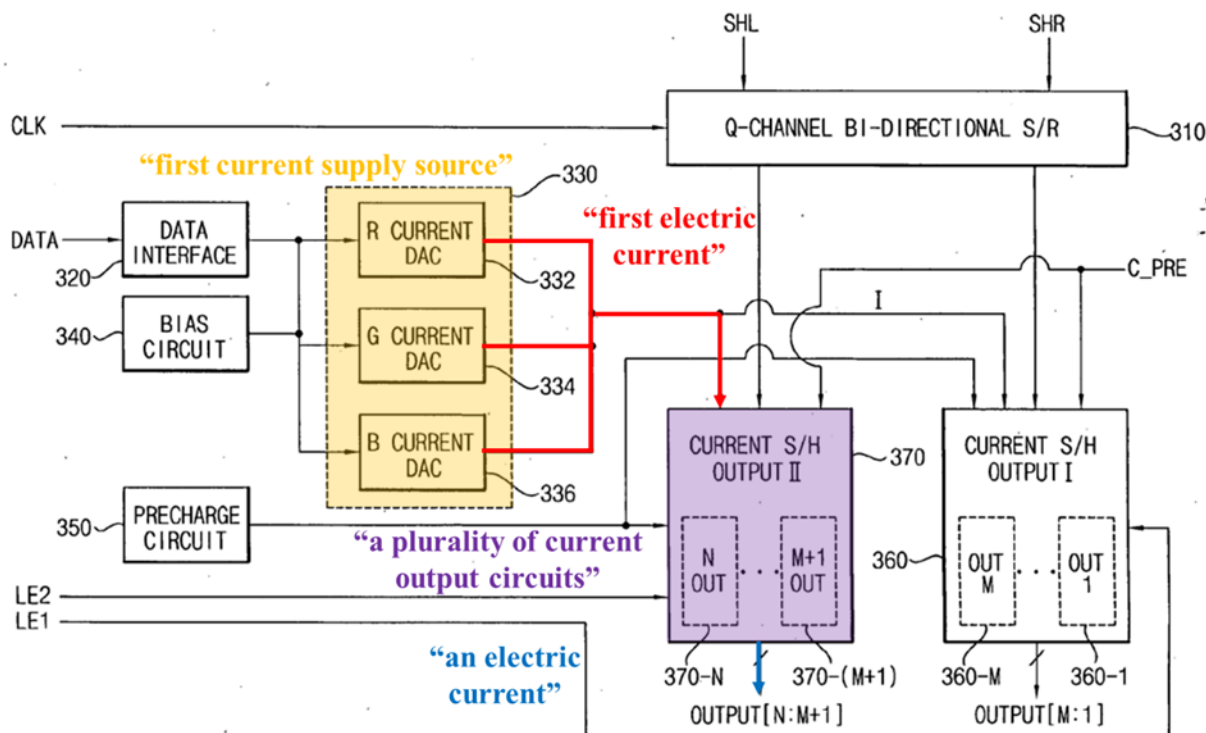
79. For example, Baek discloses a “second current sample/hold output circuit 370” that samples/holds “the analog gray-scale current” and outputs “output signals OUT M+1 through OUT N to the channels M+1 through N” (annotated green). Baek at [0048]-[0049]. These output signals “OUT M+1 through OUT N” disclosed in connection with Figure 3 each correspond to “an output terminal OUT[K]” for “a kth channel” disclosed in connection with Figure 5. Baek at [0049], [0054], [0058]. Output terminals OUT[K] “output the analog gray-scale current” to “drive a display panel ... using a smaller current.” Baek at [0058], [0063].

v. 1(d)(1): “and a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising”

80. This limitation is disclosed and at minimum rendered obvious by Baek.

81. Baek discloses a plurality of current output circuits (*e.g.*, “current sample/hold circuits 370-(M+1) through 370-N”) for outputting an electric current in accordance with said first electric current (*e.g.*, “output the analog gray-scale current ... based on the charged analog gray-scale current”). Baek at [0036], [0039], [0043], [0054], [0058], [0063], Figures 3, 5.

82. See my discussion of elements 1(b)-1(c) above (Sections XI.A.b.iii-iv).



Baek at Figure 3 (annotated); *see also* Baek at Figure 5.

83. For example, as discussed in 1(b)-1(c), Baek discloses a second current sample/hold output circuit 370 (annotated purple) that outputs current to a display panel (annotated blue). Baek at [0036], [0063]. Circuit 370 “include[s] current sample/hold circuits 370-(M+1) through 370-N,” which each receive “analog gray-scale current” (annotated red) from “current digital-to-analog conversion unit 330” (annotated gold). Baek at [0039], [0043]. Each “current sample/hold circuit 370-k, which may correspond to a kth channel,” outputs “the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current” from DAC unit 330. Baek at [0054], [0058].

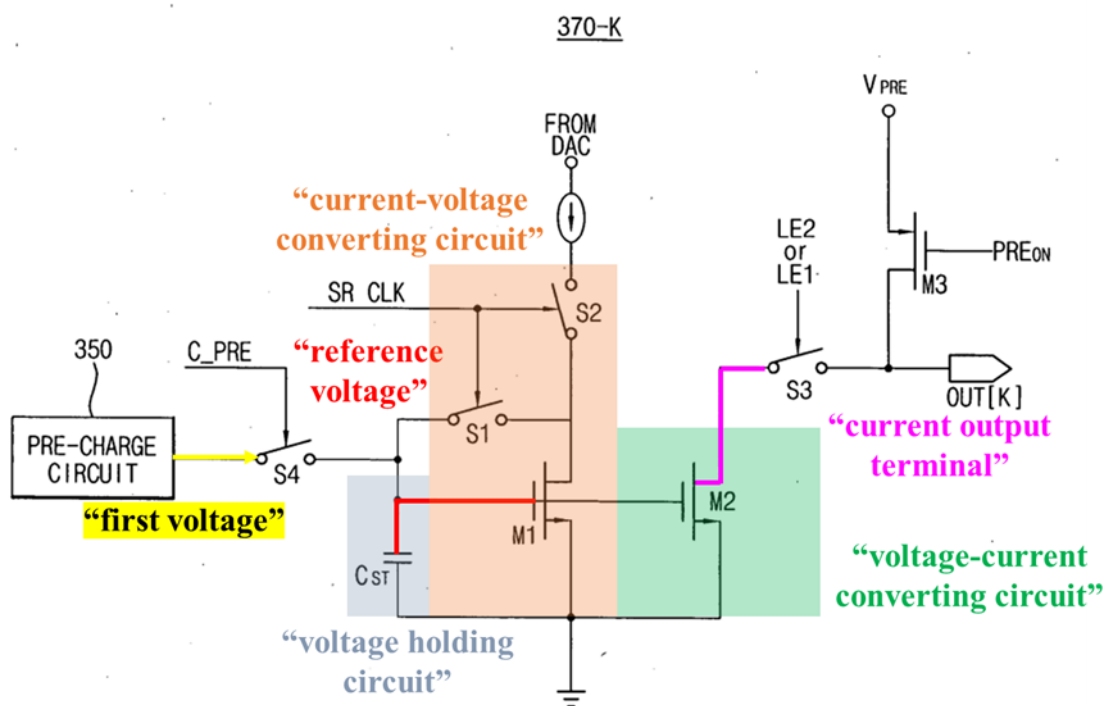
- vi. **1(d)(2): “a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein,”**

84. This limitation is disclosed and at minimum rendered obvious by Baek.

85. Baek discloses each of said current output circuits (*see* 1(d)(1)) comprising a current-voltage converting circuit (*e.g.*, “first transistor M1” connected to a “first switch S1,” a “second switch S2” “charges the analog gray-scale current” in “storage capacitor CST”), a voltage-current converting circuit (*e.g.*, “a second transistor M2” converts voltage of “storage capacitor CST” to “output the analog gray-scale current”), a voltage holding circuit (*e.g.*, “storage capacitor CST”) having a terminal being connected to a reference voltage different from the first voltage (*e.g.*, terminal “coupled to the gate [voltage] of the first transistor M1” has a different voltage from pre-charge circuit 350), and at least one current output terminal (*e.g.*, “drain [terminal] of the second transistor M2” “output[s] the analog gray-scale current”). Baek at [0036], [0052], [0054]-[0059], [0062]-[0063], Figure 5.

86. See my discussion of elements 1(a) and 1(d)(1) above (Sections XI.A.b.ii and v).

FIG. 5



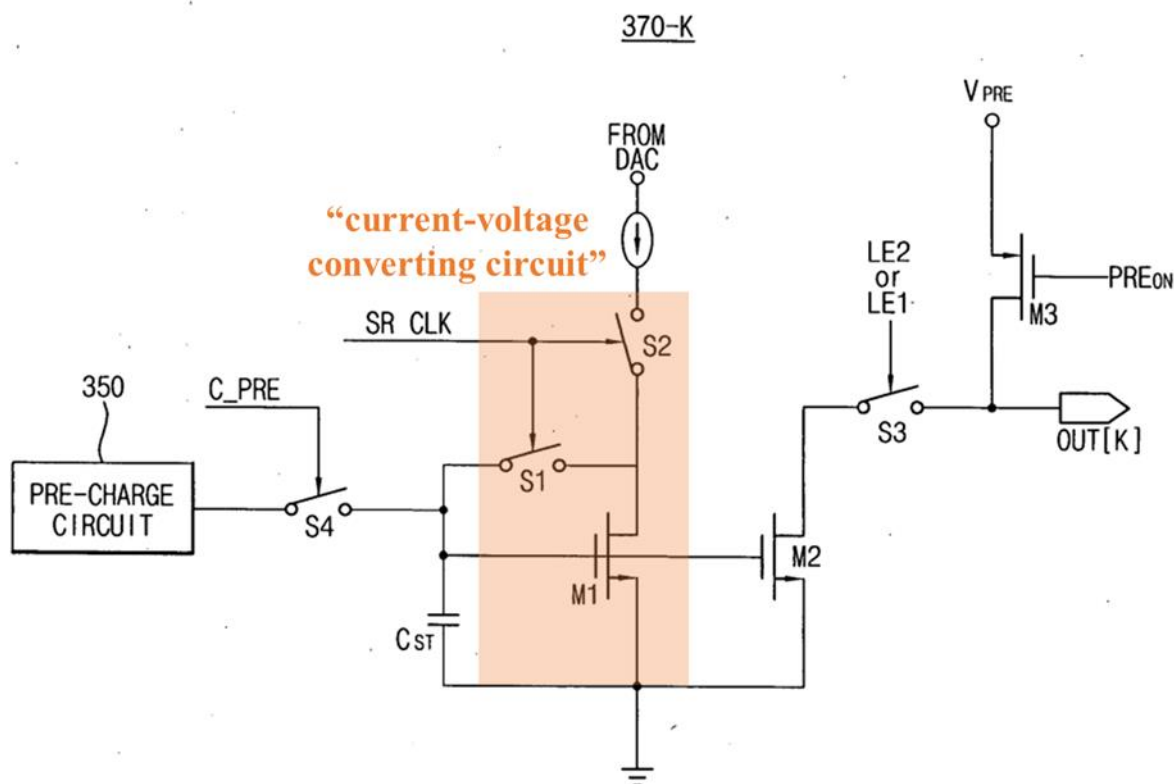
Baek at Figure 5 (annotated).

87. For example, as discussed in 1(d)(1), the second current sample/hold output circuit 370 includes a plurality of current output circuits, which are also depicted in Figure 5. Baek at [0036], [0054], [0058], [0063].

(1) *“current-voltage converting circuit”*

88. Regarding the recited “current-voltage converting circuit,” Baek discloses a “first transistor M1” connected to a “first switch S1 and [a] second switch S2” (annotated orange) that are “turned on,” while switches S3 and S4 are turned off. Baek at [0055]-[0056], [0058]-[0059], Figure 5. This configuration causes an “analog gray-scale current” from “a current digital-to-analog conversion unit 330” (see Figure 3) to be “applied to a drain of the first transistor M1 via the second switch S2” and to the “gate of the first transistor M1” via switch S1 to “charge[]” “storage capacitor CST” using “the analog gray-scale current.” Baek at [0055]-[0056], [0058]-[0059], Figure 5.¹ The storage capacitor CST is further coupled to “a fourth switch S4 [which] may be turned on to pre-charge a voltage,” as discussed in claim 3 below. Baek at [0062]. Thus, the current coming in via S2 is used to charge the capacitor CST—converting the current to voltage.

¹ This is consistent with '047 Patent, which discloses “a current-voltage converting function is actuated” when “a gate voltage for passing the electric current from the reference current source I1 is generated uniquely at the gates of the Nch transistors QN1-QNm” and “the voltage holding capacitance element C1 accumulates the electric charges in accordance with the gate voltages.” '047 Patent at 7:59-8:15.

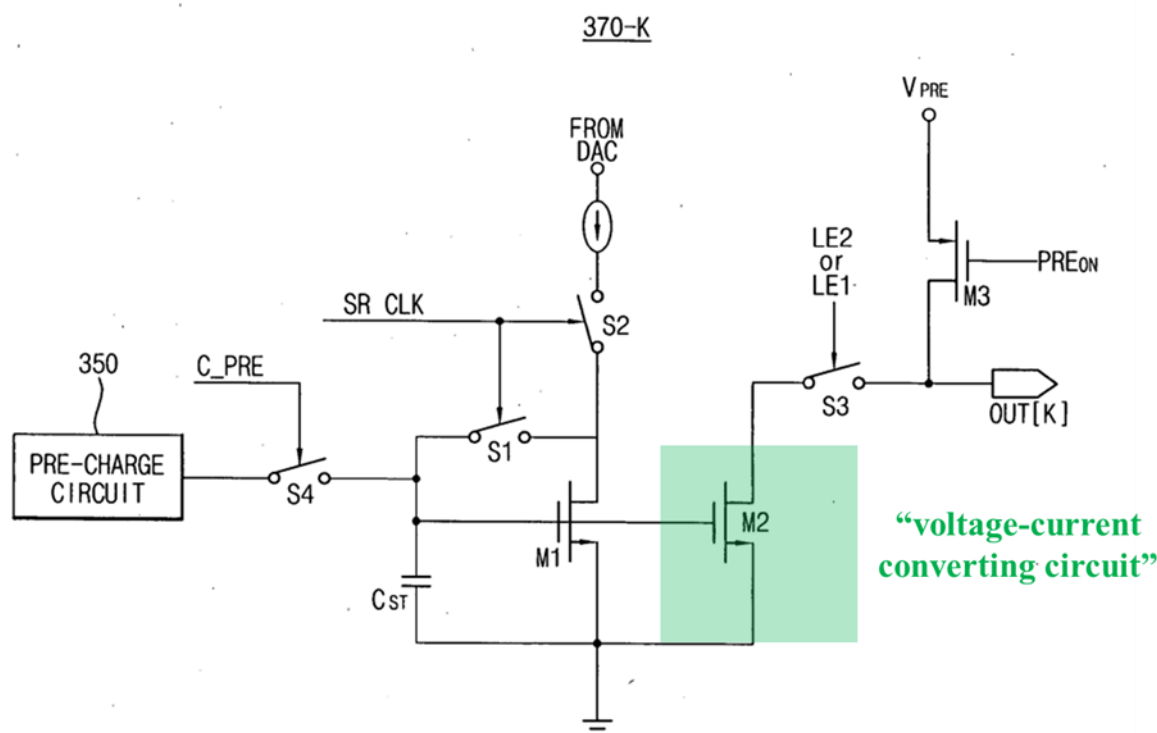


(2) “voltage-current converting circuit”

IPR2025-01330 Page 00043

off. Baek at [0056]-[0058], [0062].² Thus, the voltage stored in CST is converted to current through S3.

FIG. 5



Baek at Figure 5 (annotated).

- (3) ***“voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage”***

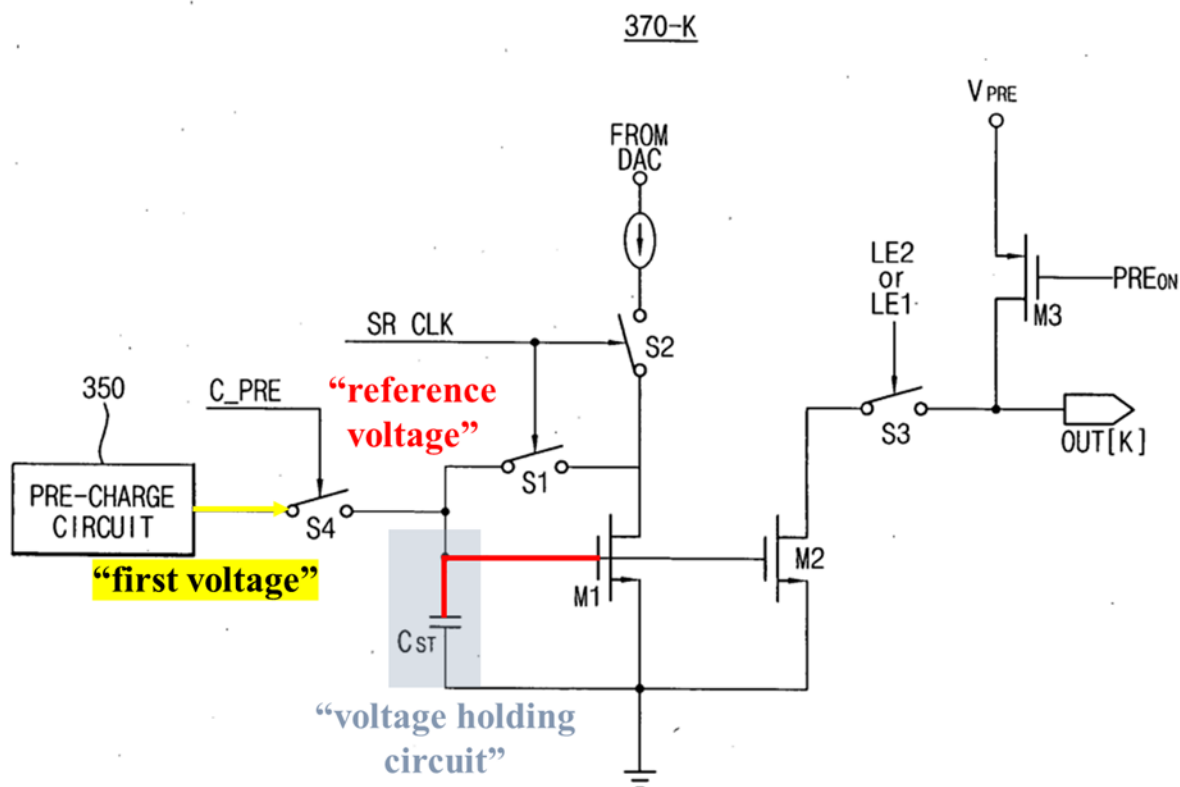
90. Regarding the recited “voltage holding circuit,” Baek further discloses a “storage capacitor CST” (annotated gray) with one terminal connected to ground and the other terminal

² This is consistent with '047 Patent, which discloses “a voltage-current converting function is actuated” when “[a] gate voltage according to the electric charges accumulated in the voltage holding capacitance element C1 is applied to the gates of the Nch transistors QN1-QNm” such that “it is possible to output a sink current having a current value proportional to the reference current.” '047 Patent at 8:17-49.

(unannotated) “coupled to the gate of the first transistor M1,” which supplies a reference voltage (annotated red). Baek at [0055]-[0056], Figure 5. The capacitor also has another terminal connected to pre-charge circuit 350, which supplies the first voltage (annotated yellow). Baek at [0055]-[0056], Figure 5. In a “pre-charge” mode, “switch S4” is “turned on” and switches S1, S2, and S3 are turned off such that pre-charge circuit 350 “pre-charge[s] a voltage of the storage capacitor CST to a voltage level slightly lower than a threshold voltage of the first transistor M1.” Baek at [0052], [0057]-[0058], [0062]. Thereafter, in a current charge mode, switch S4 is turned off and switches S1 and S2 are “turned on” such that “storage capacitor CST” is “charge[d]” with “the analog gray-scale current” from “current digital-to-analog conversion unit.” Baek at [0056]-[0057], [0062]. A person of ordinary skill in the art would have understood or at least found obvious that the analog gray-scale current charges the capacitor as a reference voltage, as this is a fundamental property of capacitors, as I discuss in Section X.C.d. In this current charge mode, the reference voltage on the terminal of capacitor CST coupled to transistor M1 is different from the voltage supplied by pre-charge circuit 350 because switch S4 is turned off and CST is instead charged with current coming in through S1 and S2. Baek at [0062].³

³ This is consistent with the '047 Patent, which discloses “the voltage holding capacitance element C1 is charged to a constant voltage (this corresponds to the first voltage, and will be referred to as a reference voltage hereinafter) that is supplied from the voltage supply source V1.” '047 Patent at 7:46-52.

FIG. 5

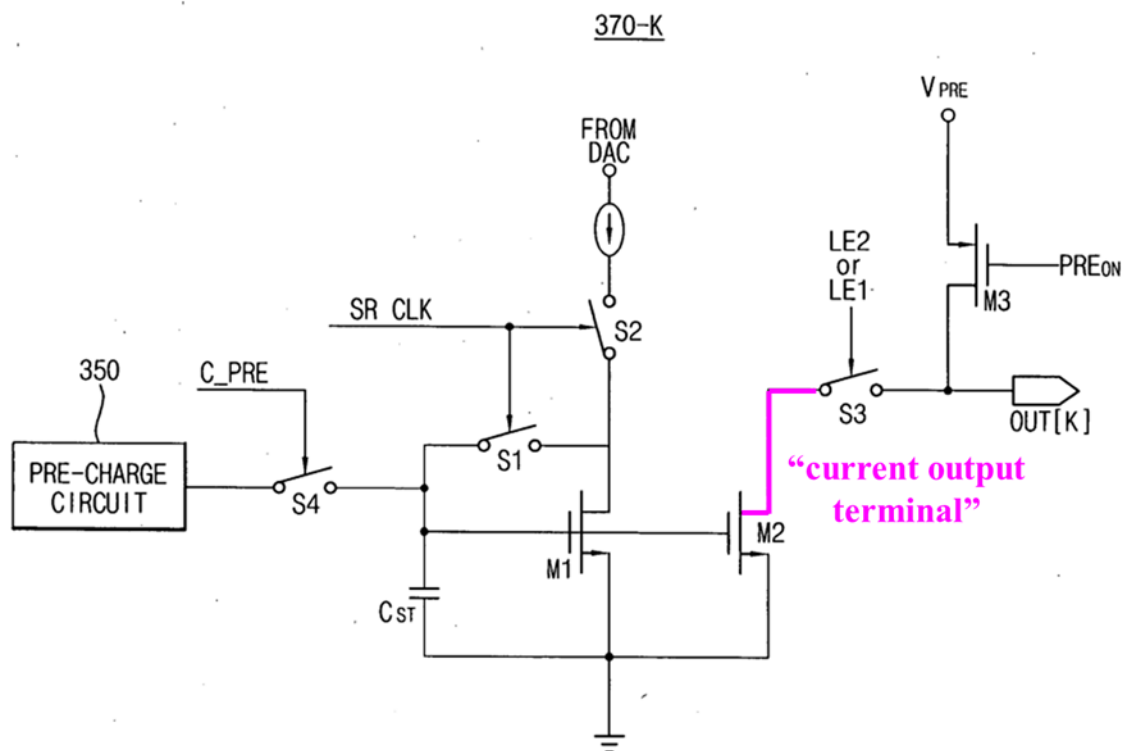


Baek at Figure 5 (annotated).

(4) *“at least one current output terminal”*

91. Regarding the recited “current output terminal,” Baek further discloses that, in a current output mode, switches S1, S2, and S4 are turned off and a “switch S3 ... couple[s] a drain of the second transistor M2” (annotated pink) to “an output terminal OUT[K].” Baek at [0057]-[0058], [0062]. Transistor M2 “output[s] the analog gray-scale current to the output terminal OUT[K] based on” the “analog gray-scale current” that charges “the storage capacitor CST” connected to transistor M2’s gate. Baek at [0057]-[0058], [0062].

FIG. 5



Baek at Figure 5 (annotated).

- vii. **1(e): “each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,”**

92. This limitation is disclosed and at minimum rendered obvious by Baek.

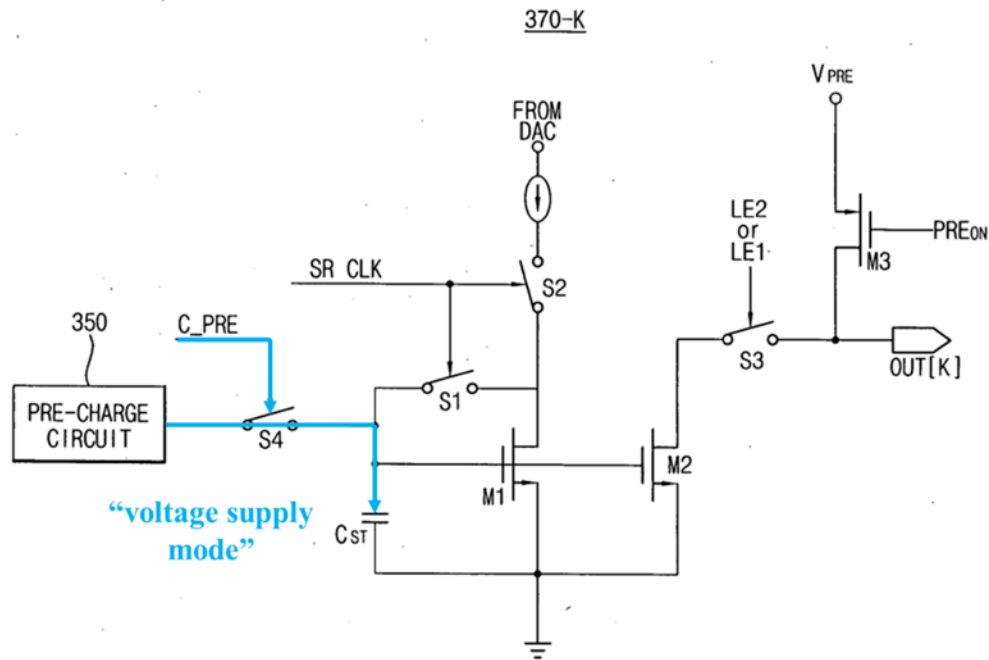
93. Baek discloses each of said current output circuits (*see* 1(d)(1)) operates in three operation modes including a voltage supply mode (*e.g.*, “pre-charge” mode to “pre-charge a voltage of the storage capacitor C_{ST}”), a current supply mode (*e.g.*, mode supplying “an analog gray-scale current” from “a current digital-to-analog conversion unit 330”), and a current output mode (*e.g.*, mode “output[ting] the analog gray-scale current to the output terminal OUT[K]”).

Baek at [0040], [0056]-[0058], [0062], Figures 3, 5.

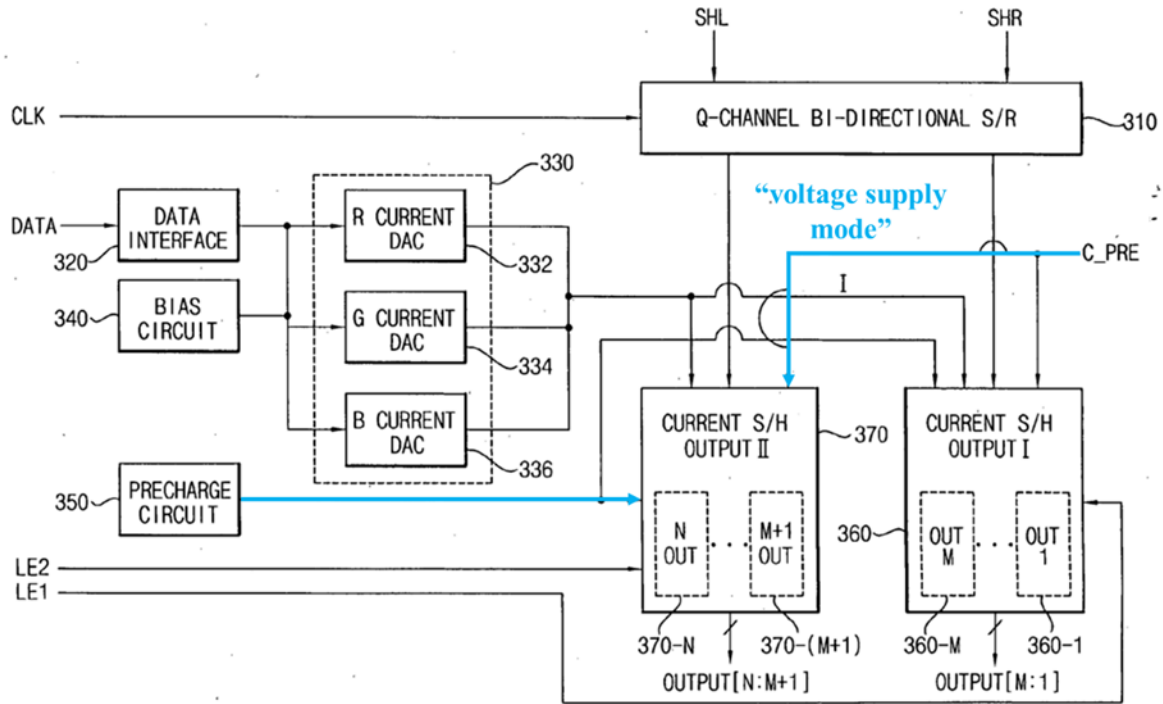
94. See my discussion of elements 1(d)(1)-1(d)(2) above (Sections XI.A.b.v-vi).

95. For example, as discussed in 1(d)(2), Baek discloses a “pre-charge” mode (annotated blue) where a pre-charge circuit 350 “pre-charges a voltage of the storage capacitor CST.” Baek at [0062]. Current output circuit 370 operates in this mode when “pre-charge signal C_PRE” turns on “switch S4” while switches S1, S2, and S3 are “turned off,” as shown in Figure 5. Baek at [0057]-[0058], [0062]. As shown in Figure 3, in the pre-charge mode, the C_PRE signal is supplied to the “second sample/hold output circuit 370” such that each “current sample/hold circuits 370-(M+1) through 370-N” receives the C_PRE signal and applies the voltage from pre-charge circuit to the storage capacitor CST.

FIG. 5

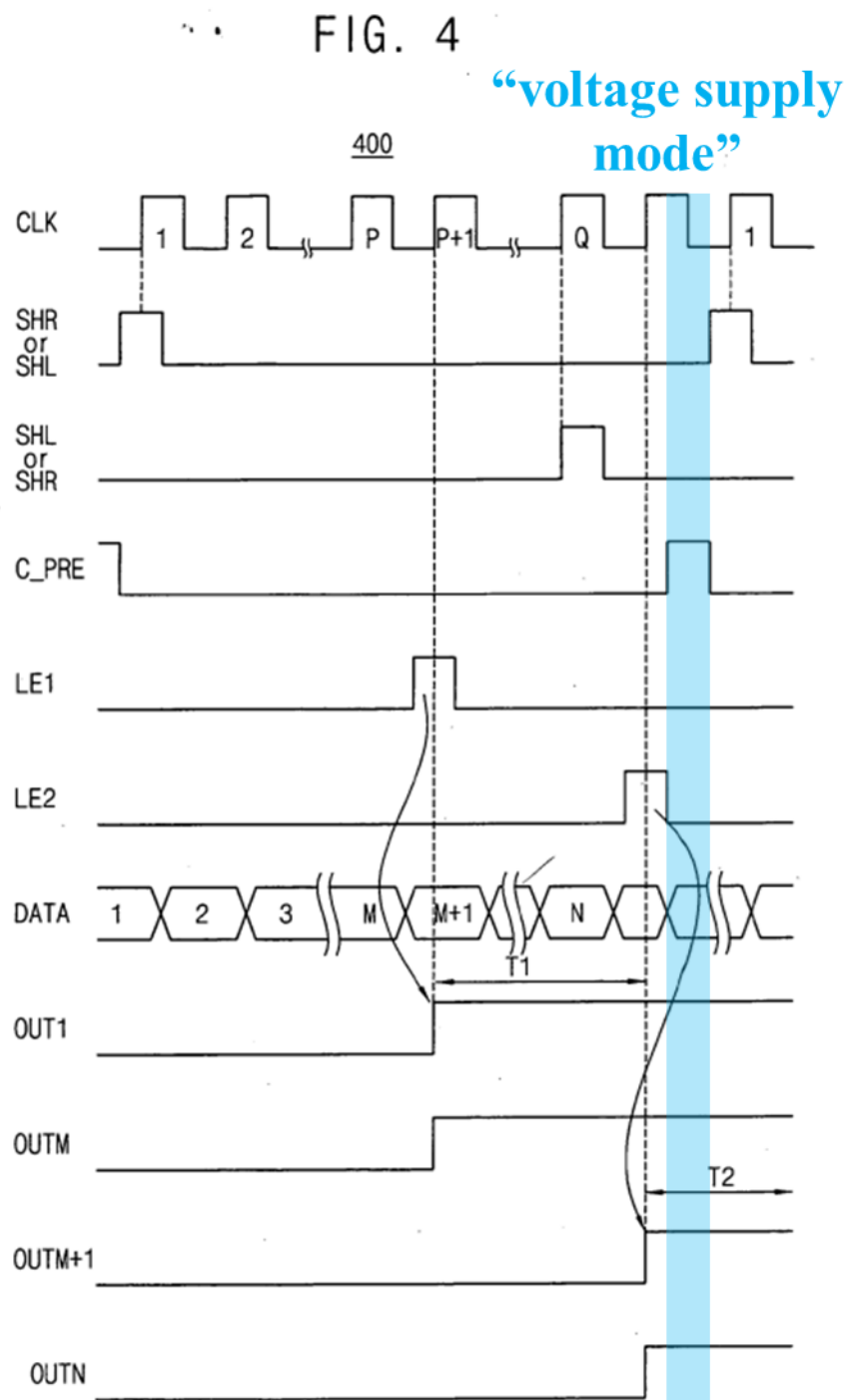


Baek at Figure 5 (annotated).



Back at Figure 3 (annotated).

96. Figure 4 discloses the pre-charge mode when the C_PRE signal turns on switch S4 while the other switches are turned off.

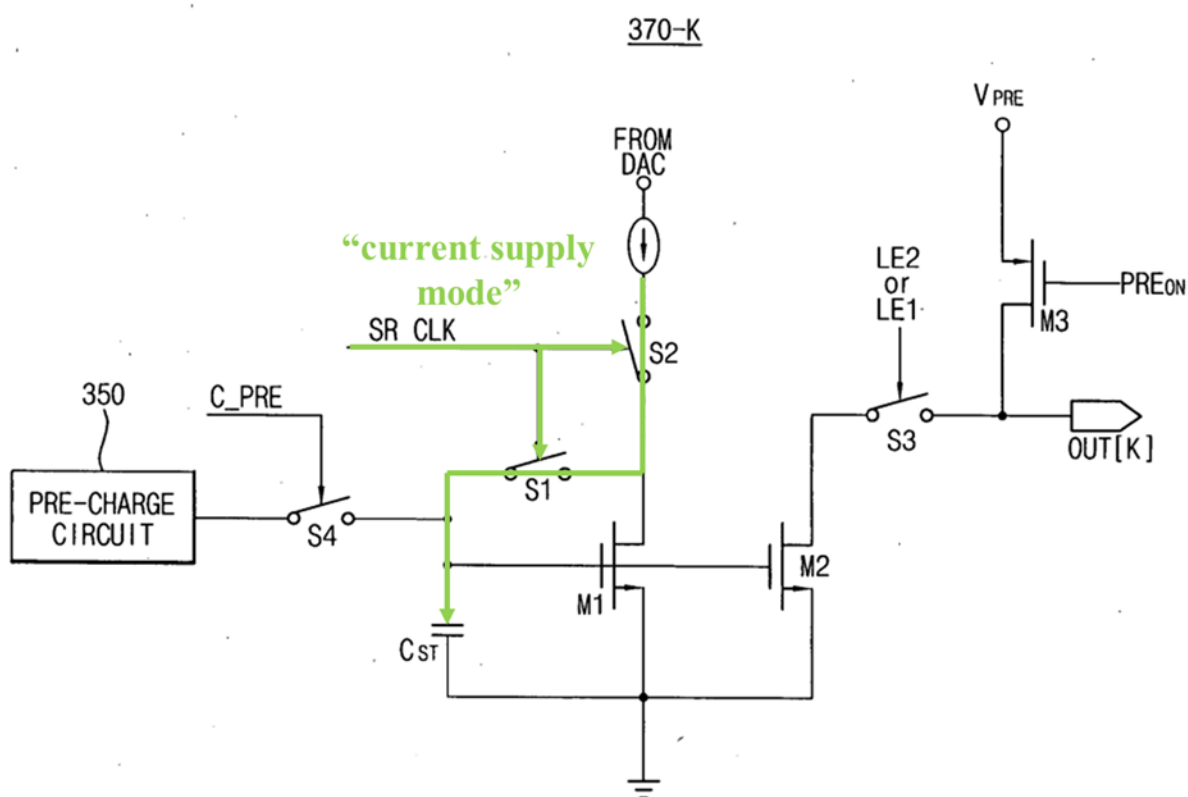


Back at Figure 4 (annotated).

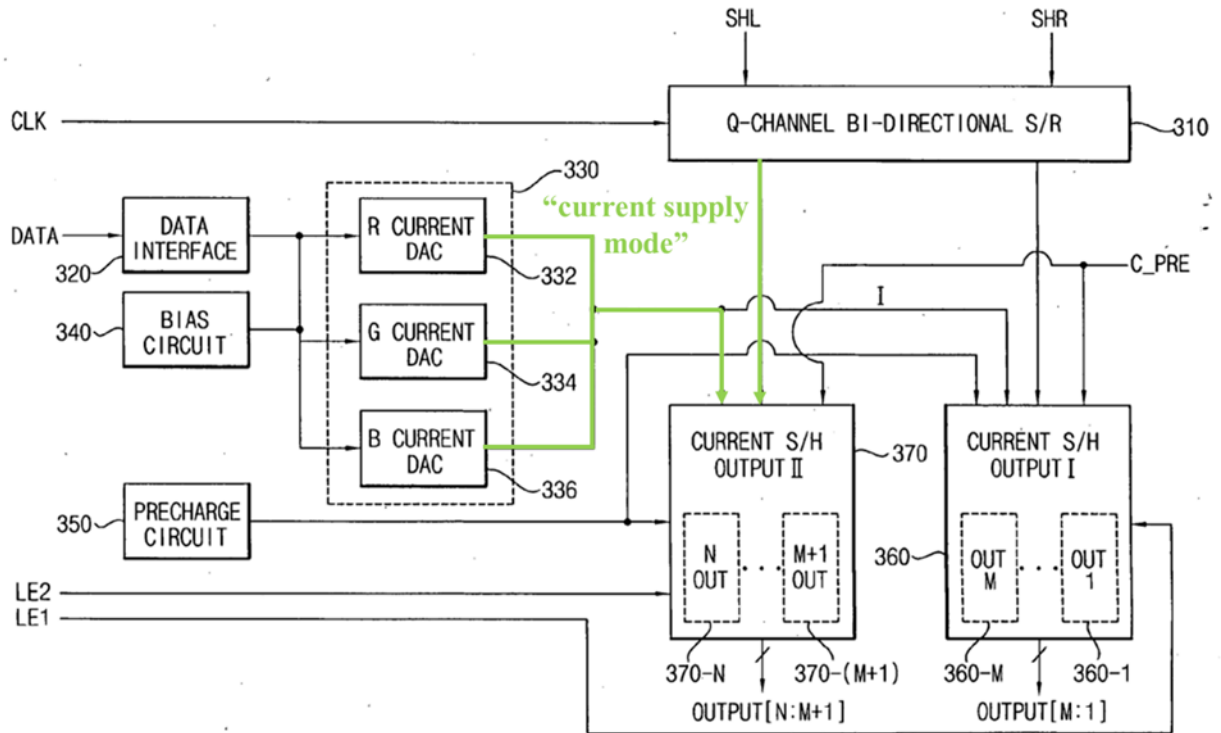
97. As also discussed in 1(d)(2), Baek discloses a current charge mode (annotated green) where “storage capacitor CST” is charged by “the analog gray-scale current” from “current

digital-to-analog conversion unit 330.” Baek at [0056]-[0057]. Current output circuit 370 operates in this mode when switches S3 and S4 are turned off and “switch S1 and ... switch S2” are “turned on” based on “second clock signal SR CLK.” Baek at [0040], [0056]-[0057], [0062]. As shown in Figure 3, the CLK signal is supplied to the “second sample/hold output circuit 370” such that each “current sample/hold circuits 370-(M+1) through 370-N” receives the CLK signal and applies the analog gray-scale current from current digital-to-analog conversion unit 330 to the storage capacitor CST in the current charge mode.

FIG. 5

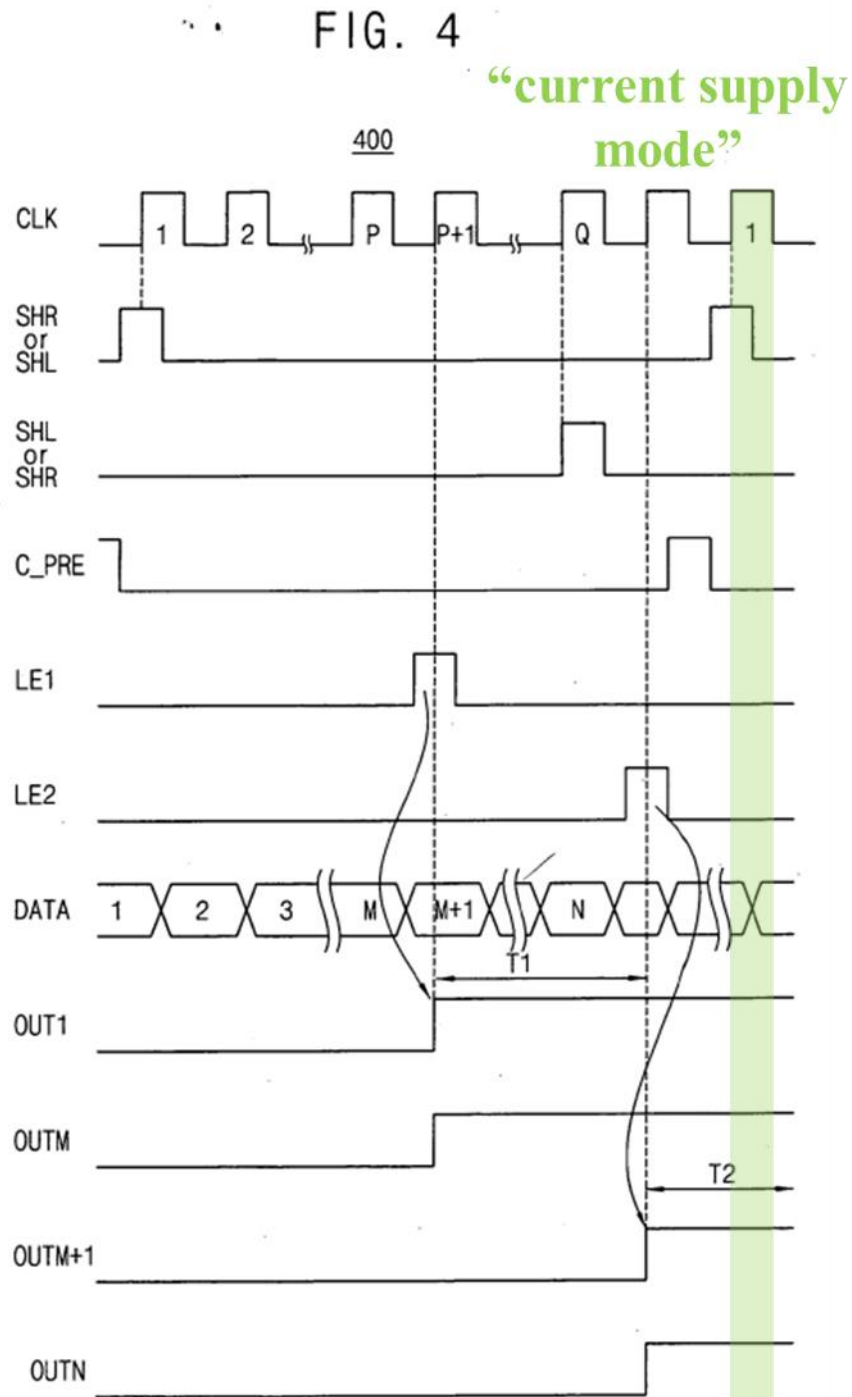


Baek at Figure 5 (annotated).



Back at Figure 3 (annotated).

98. Figure 4 of Baek discloses the current charge mode when the SR CLK signal turns on switches S1 and S2 while the other switches are turned off.

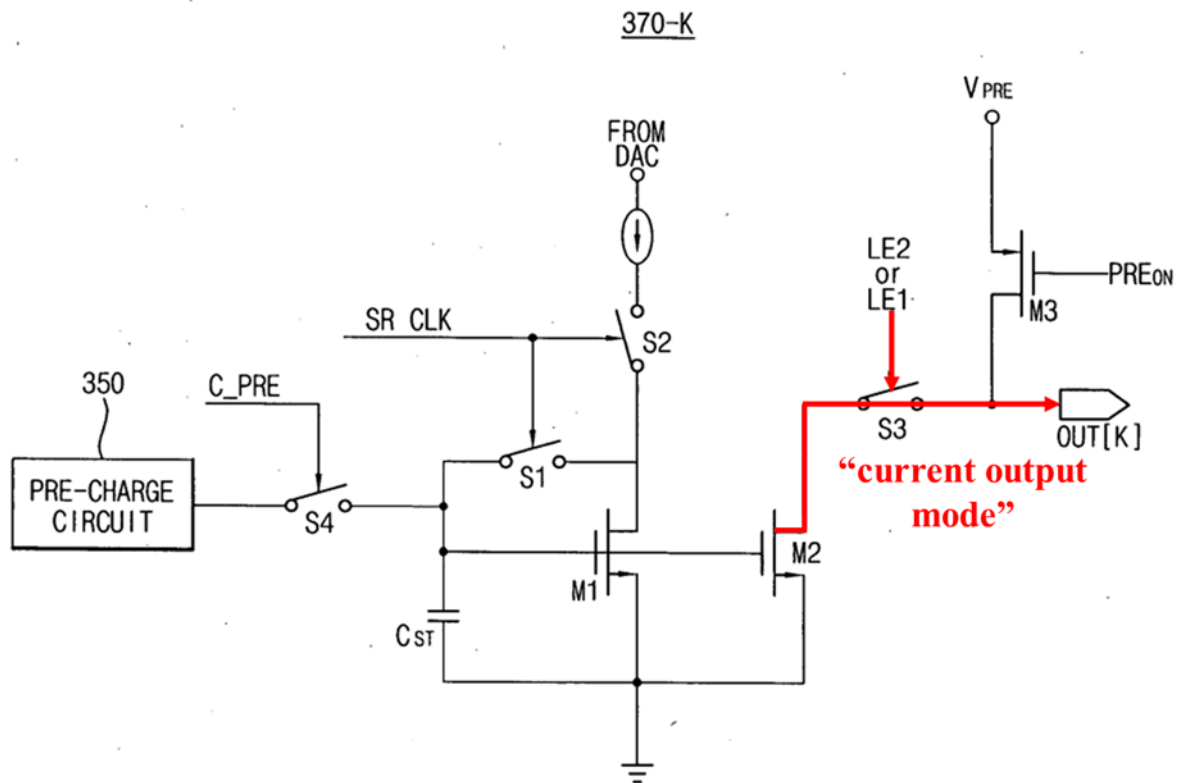


Back at Figure 4 (annotated).

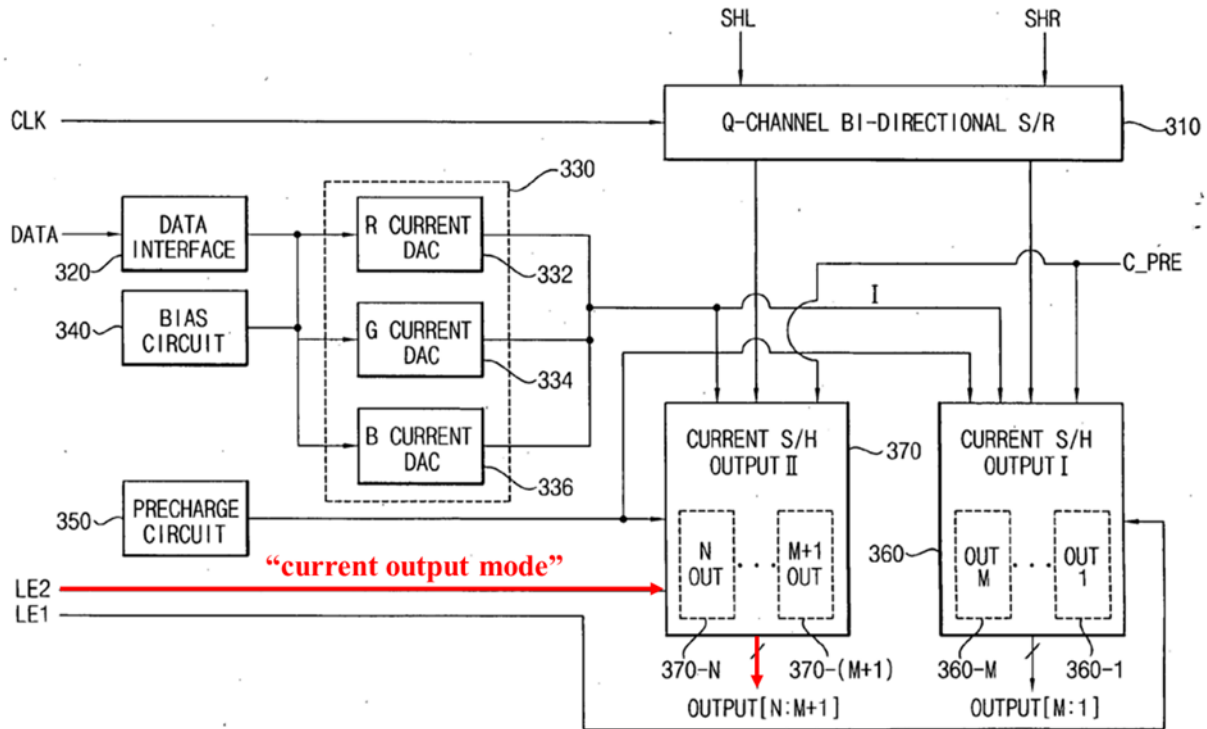
99. As also discussed in 1(d)(2), Baek discloses a current output mode (annotated red) where second transistor M2 “output[s] the analog gray-scale current to the output terminal OUT[K]

based on the charged analog gray-scale current.” Baek at [0058]. Current output circuit 370 operates in this mode when switches S1, S2, and S4 are turned off and switch S3 is turned on based on “the second latch enable signal LE2 [being] activated.” Baek at [0057]-[0058], [0062]. As shown in Figure 3, the LE2 signal is supplied to the “second sample/hold output circuit 370” such that each “current sample/hold circuit[] 370-(M+1) through 370-N” receives the LE2 signal and outputs current to the output terminal, such as output terminal OUT[K] (which corresponds to output terminals N:M+1 in Figure 5), in the current output mode.

FIG. 5

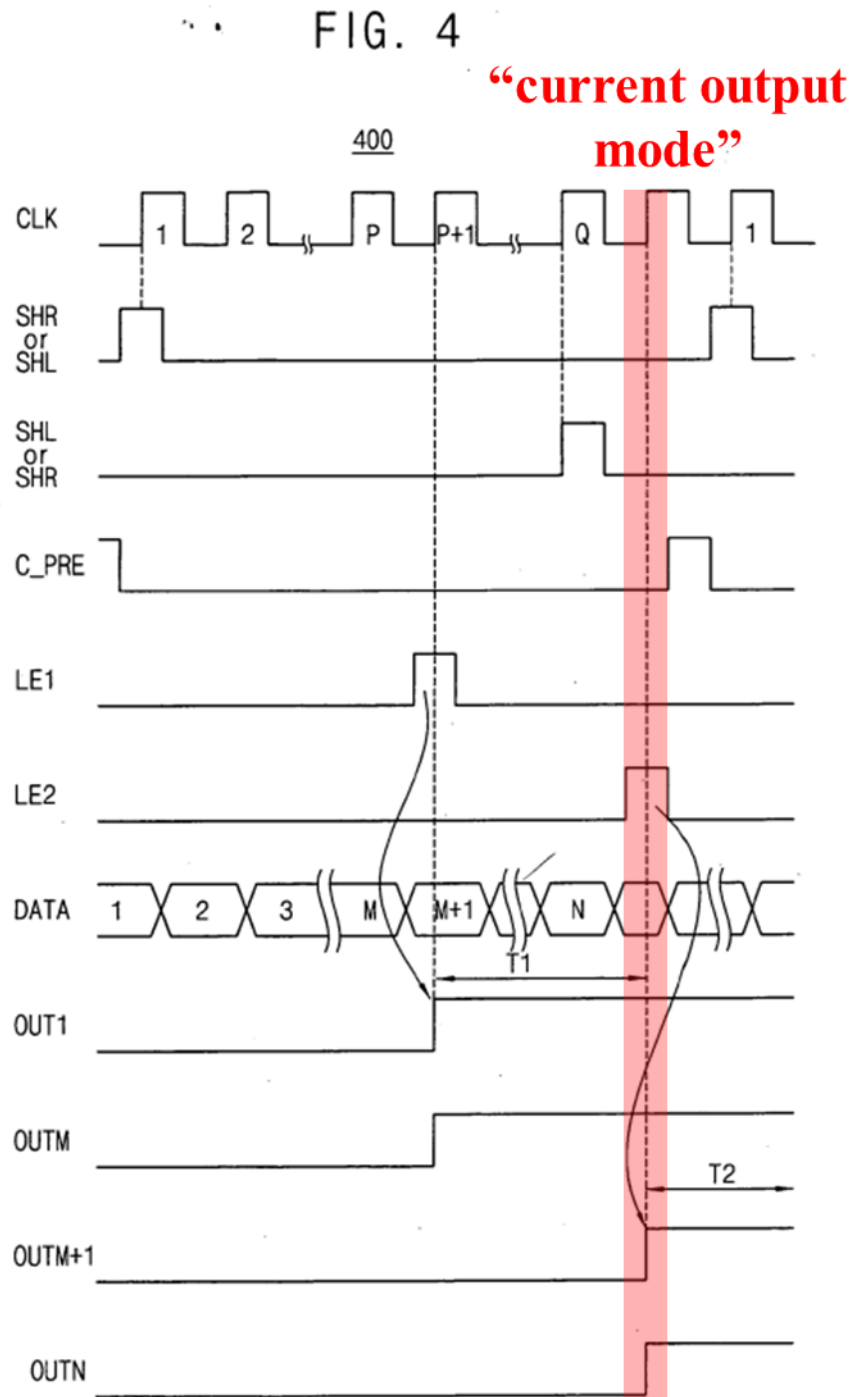


Baek at Figure 5 (annotated).



Back at Figure 3 (annotated).

100. Figure 4 discloses the current output mode when the LE2 signal turns on switch S3 while the other switches are turned off.



Back at Figure 4 (annotated).

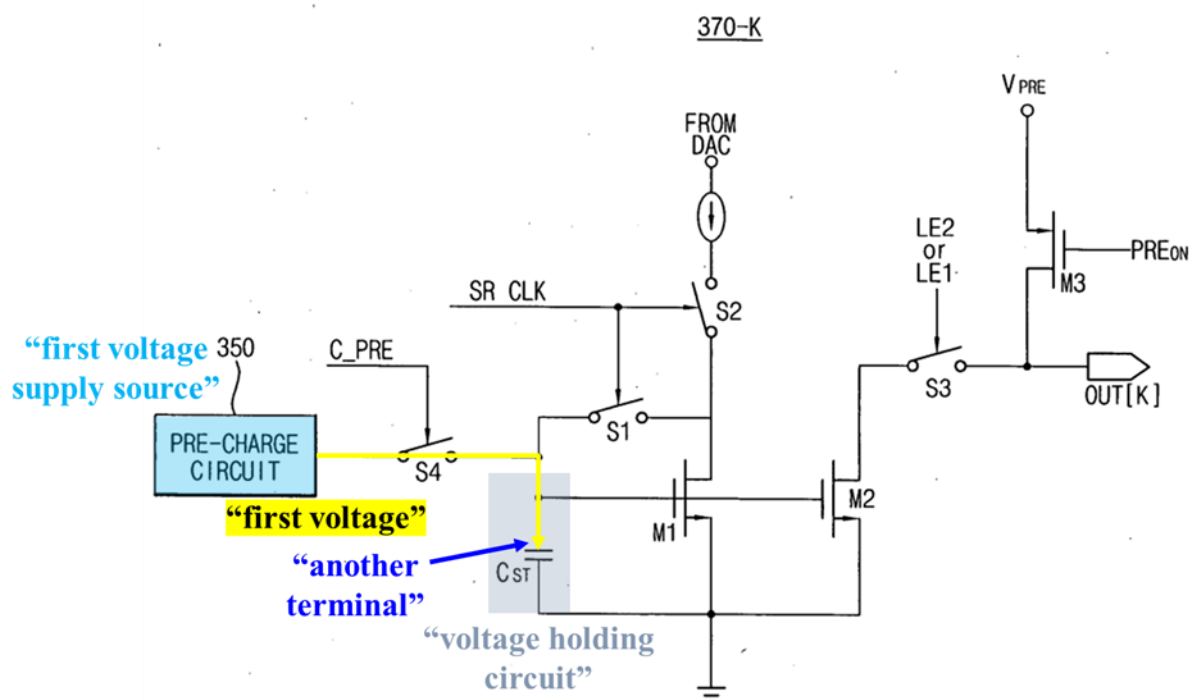
viii. 1(f): “under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit,”

101. This limitation is disclosed and at minimum rendered obvious by Baek.

102. Baek discloses under said voltage supply mode (*see* 1(e)), each of said current output circuits receives said first voltage from said first voltage supply source (*e.g.*, each “current sample/hold output circuit 370” receives “pre-charge ... voltage” from “pre-charge circuit 350”), and the first voltage is supplied to another terminal of said voltage holding circuit (*e.g.*, “pre-charge ... voltage” is supplied to terminal of “storage capacitor CST” via S4). Baek at [0055]-[0057], [0062], Figures 3-5.

103. See my discussion of elements 1(a) and 1(d)(1)-1(e) above (Sections XI.A.b.ii and v-vii).

FIG. 5



Baek at Figure 5 (annotated).

104. For example, as discussed in 1(d)(2)-1(e), Baek discloses that, during a pre-charge mode, “switch S4” is “turned on” and switches S1 and S2 are turned off such that pre-charge circuit 350 (annotated blue) “pre-charge[s] a voltage” (annotated yellow) “of the storage capacitor CST” (annotated gray) “to a voltage level slightly lower than a threshold voltage of the first transistor M1.” Baek at [0057], [0062]. Thus, the pre-charge voltage is supplied to the terminal (annotated dark blue) of the storage capacitor CST that is “coupled to the gate of the first transistor M1.” Baek at [0056].⁴ As discussed in 1(e) and in Section XI.A.a, Baek discloses that each “current

⁴ This is consistent with the '047 Patent, which discloses, during “voltage supply mode M1, ... the voltage holding capacitance element C1 is charged to a constant voltage (this corresponds to the first voltage, and will be referred to as a reference voltage hereinafter) that is supplied from the voltage supply source V1.” '047 Patent at 7:41-57.

sample/hold circuit 370-k” of the second current sample/hold output circuit 370 receives the voltage from pre-charge circuit 350 when the C_PRE signal is supplied.

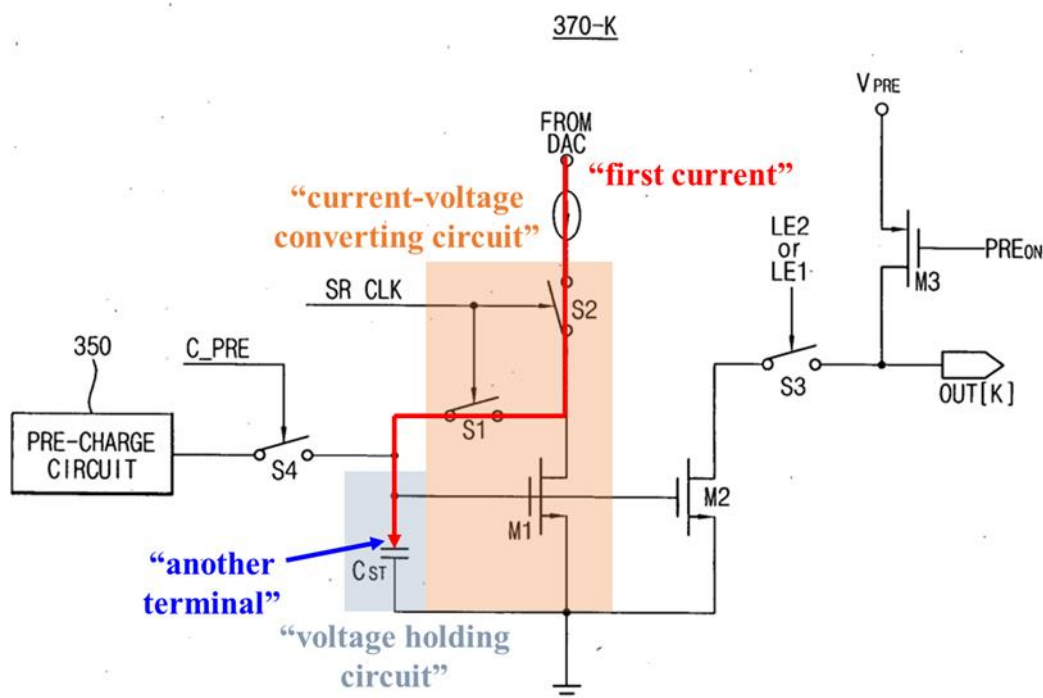
- ix. 1(g): “under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and”**

105. This limitation is disclosed and at minimum rendered obvious by Baek.

106. Baek discloses under said current supply mode (*see* 1(e)), each of said current output circuits receives said first current from said first current supply source (*e.g.*, each “current sample/hold circuit 370” receives “an analog gray-scale current” from “current digital-to-analog conversion unit 330”), and generates a second voltage by said current-voltage converting circuit (*e.g.*, voltage generated by “charg[ing] the analog gray-scale current” in storage capacitor CST), and the first current is supplied to said another terminal of said voltage holding circuit (*e.g.*, “an analog gray-scale current” is supplied to terminal of “storage capacitor CST”). Baek at [0044], [0045], [0056]-[0057], Figures 3-5.

107. See my discussion of elements 1(b) and 1(d)(1)-1(e) above (Sections XI.A.b.iii and v-vii).

FIG. 5



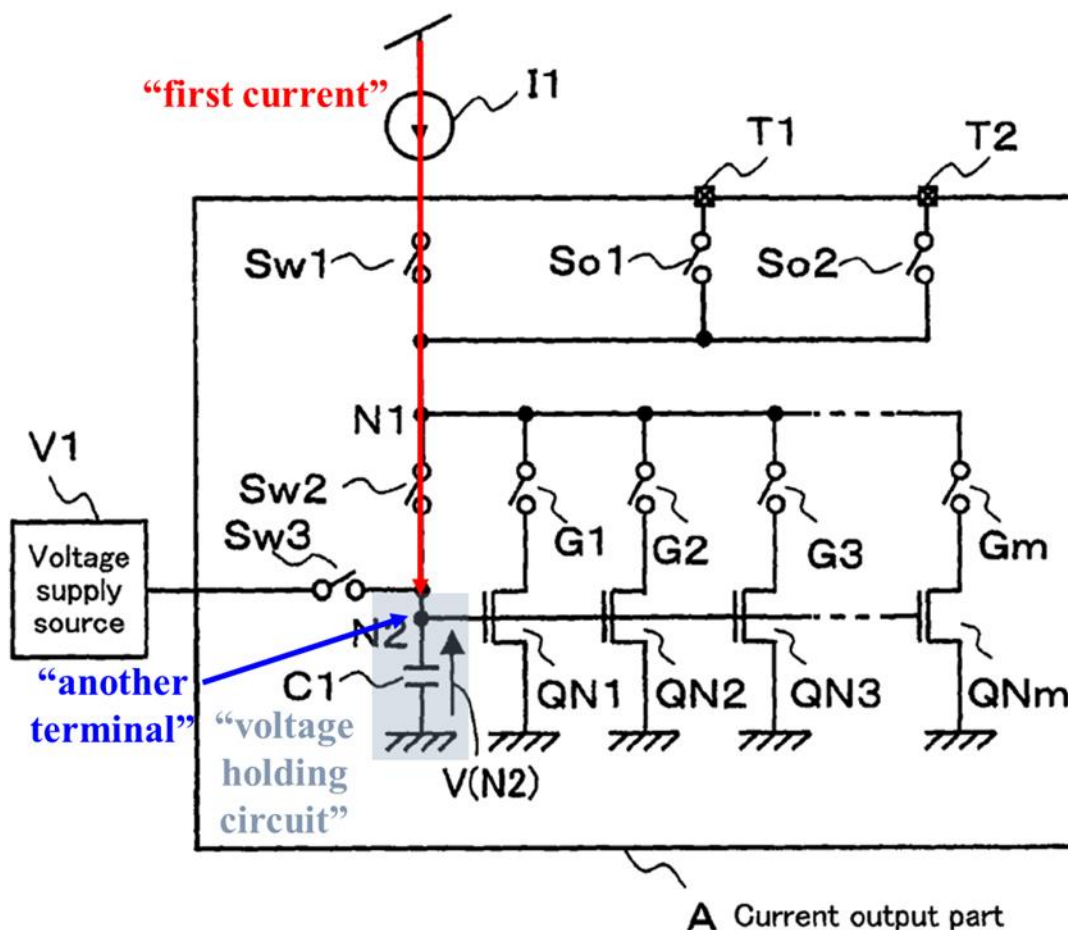
Baek at Figure 5 (annotated), [0056].

108. For example, as discussed in 1(e), Baek discloses switch S4 is turned off and switches S1 and S2 are “turned on” such that “storage capacitor CST” (annotated gray) “charges the analog gray-scale current” (annotated red) from “current digital-to-analog conversion unit 330” to produce a voltage at the terminal (annotated dark blue) of the capacitor CST coupled to the gate of transistor M1. Baek at [0056]-[0057]. As discussed in 1(e) and in Section XI.A.a, Baek discloses that each “current sample/hold circuit 370-k” of the second current sample/hold output circuit 370 receives analog gray-scale current when the SR CLK signal is supplied.

109. This is consistent with the description of these elements in the '047 Patent, where the first current (annotated red) is supplied to the second terminal (annotated dark blue) of the voltage holding capacitor (annotated gray) in a similar manner to Baek. '047 Patent at 8:1-15.

Figure 1A of the '047 Patent is annotated to show that a first electric current is supplied to the marked "another terminal" of the voltage holding capacitor.

F I G. 1 A



'047 Patent at Figure 1A (annotated).

- x. **1(h): "under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit."**

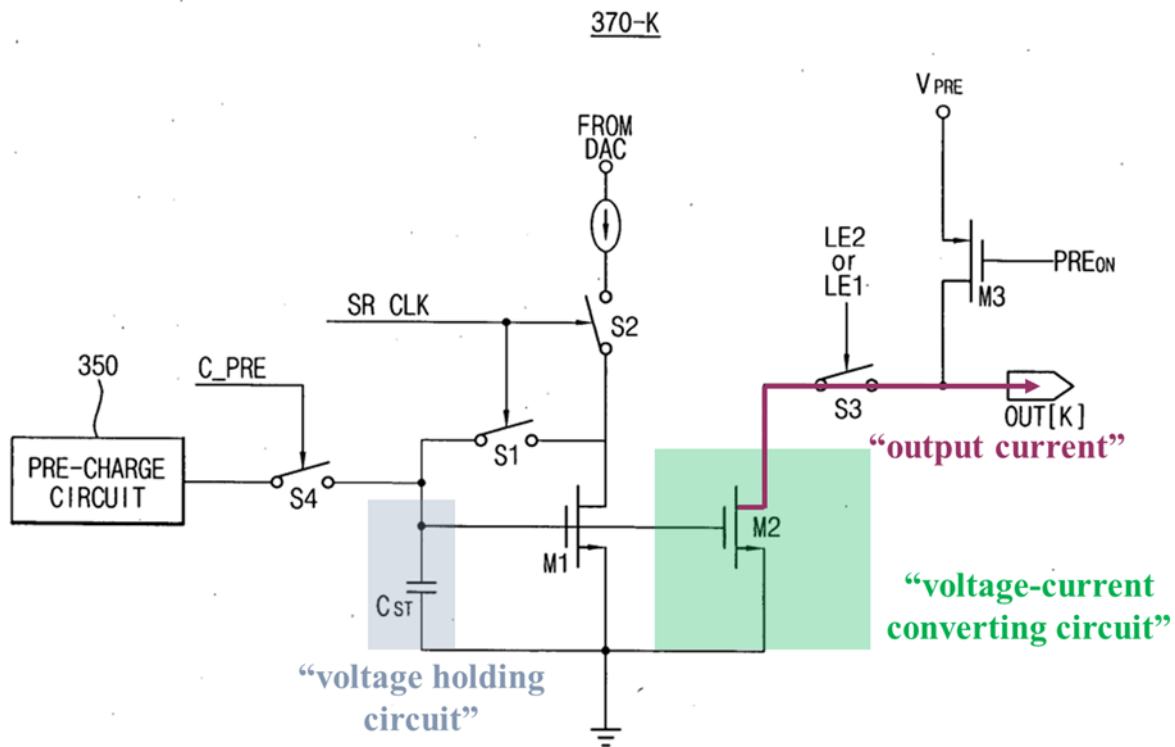
110. This limitation is disclosed and at minimum rendered obvious by Baek.

111. Baek discloses under said current output mode (see 1(e)), each of said current output circuits outputs an output current (e.g., each "current sample/hold circuit 370" "output[s]

the analog gray-scale current”) according to said voltage held in said voltage holding circuit by said voltage-current converting circuit (e.g., “analog gray-scale current” output by transistor M2 is “based on the charged analog gray-scale current” held in “storage capacitor CST”). Baek at [0058], [0062], Figures 3-5.

112. See my discussion of elements 1(d)(1)-1(e) above (Sections XI.A.b.v-vii).

FIG. 5



Baek at Figure 5 (annotated).

113. For example, as discussed in 1(e), Baek discloses a current output mode where second transistor M2 (annotated green) “output[s] the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current” (annotated purple). Baek at [0058]. Transistor M2 has “its gate coupled to the storage capacitor CST” (annotated gray) such

that the “voltage of the storage capacitor CST” during the pre-charge mode (*see* 1(f)) and the “charged analog gray-scale current” held in storage capacitor CST, is converted to an output current “based on the charged analog gray-scale current.” Baek at [0058], [0062]. As discussed in 1(e) and in Section XI.A.a, Baek discloses that each “current sample/hold circuit 370-k” of the second current sample/hold output circuit 370 outputs the analog gray-scale current stored in the capacitor CST when latch signal LE2 is supplied. Baek at [0052].

c. Claim 2

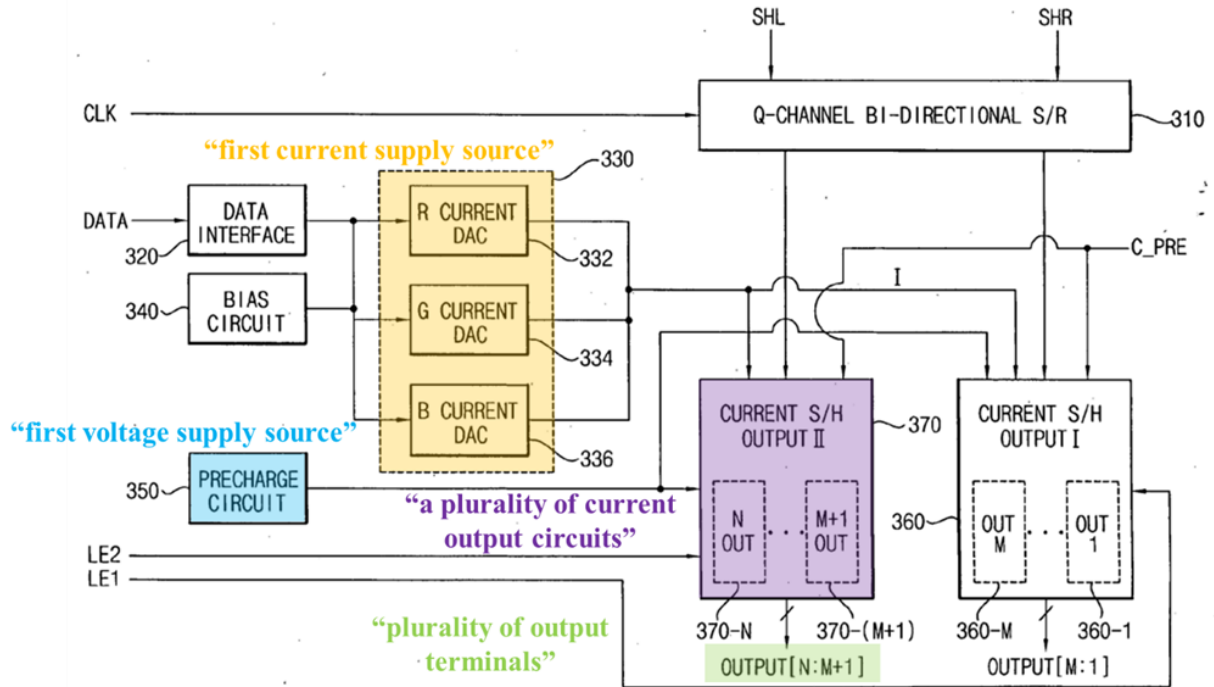
114. This claim is disclosed and at minimum rendered obvious by Baek.

115. Claim 2 recites: “The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits, and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common.”

116. Baek discloses and at minimum renders obvious the current driving device according to claim 1, as discussed above.

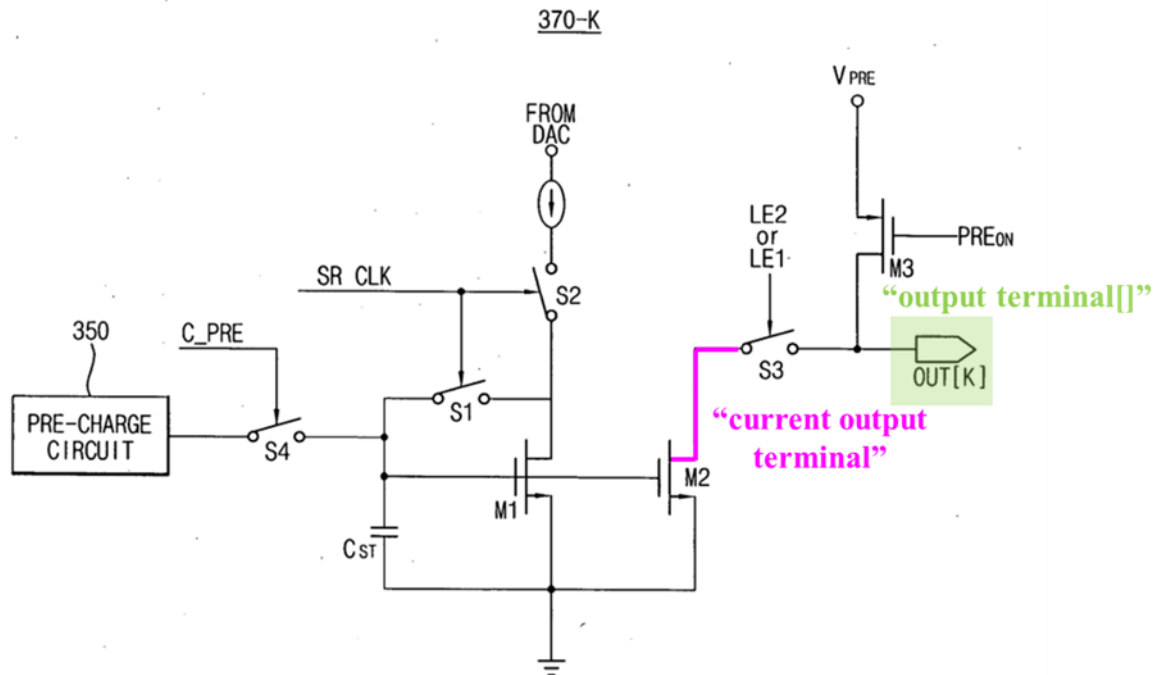
117. Baek further discloses each of said output terminals (*see* 1(c)) is connected to said current output terminals provided to said plurality of said current output circuits (*e.g.*, each “output terminal OUT[K]” is connected to “drain [terminals] of the second transistor M2” in the “current sample/hold circuit[s]”), and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common (*e.g.*, each “current sample/hold circuit 370-k” is connected in parallel to “current digital-to-analog conversion unit 330” and “pre-charge circuit 350”). Baek at [0038], [0039], [0055], [0058], Figures 3, 5.

118. See my discussion of elements 1(a)-1(d)(2) above (Sections XI.A.b.ii-vi).



Back at Figure 3 (annotated).

FIG. 5



Baek at Figure 5 (annotated).

119. For example, as discussed in 1(c) and 1(d)(1), Baek discloses that each output terminal “OUT[K]” (annotated green) is connected to the drain terminals (annotated pink) of “the second transistor M2” in the current sample/hold circuits. Baek at [0058]. Baek further discloses that the current sample/hold circuits within the second current sample/hold output circuit 370 and DAC 330 share a common node. Each current sample/hold circuit 370-k and the pre-charge circuit 350 share a common node. Current sample/hold output circuit 370 is also grounded, because the individual current sample/hold circuits 370-k within the current sample/hold output circuit 370 are grounded. A person of ordinary skill in the art would have understood or at least found obvious that DAC 330 and pre-charge circuit 350 are also grounded because power supplies, including voltage and current sources, are grounded to form a complete loop, as I discuss above further in Section X.C.a-b. Therefore, each of the current sample/hold circuits 370-k is connected in parallel to the pre-charge circuit 350 and DAC 330 used in common.

d. Claim 3

120. This claim is disclosed and at minimum rendered obvious by Baek.

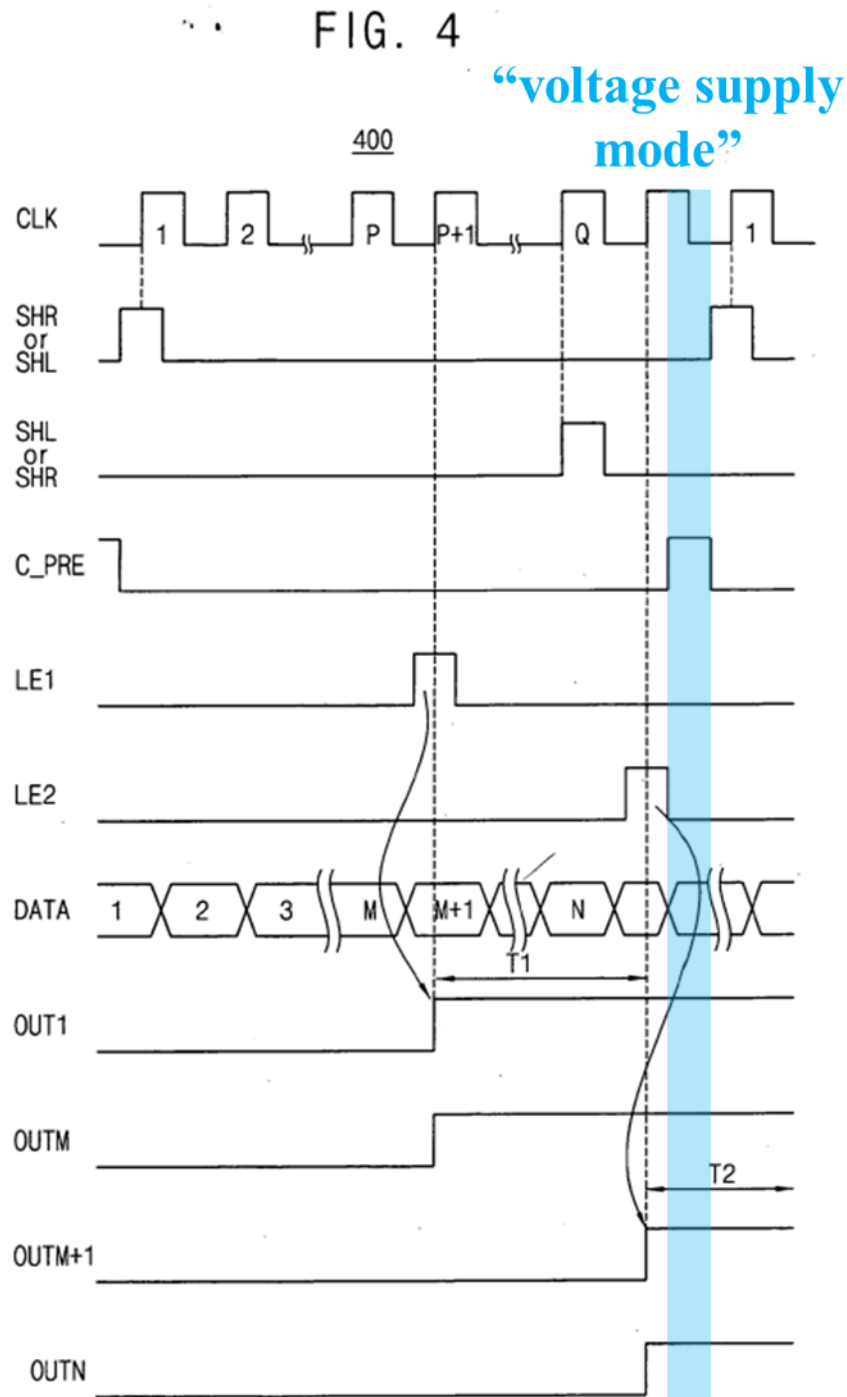
121. Claim 3 recites: “The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode.”

122. Baek discloses and at minimum renders obvious the current driving device according to claim 1, as discussed above.

123. Baek further discloses in each of said current output circuits (*see* 1(d)(1)), said current-voltage converting circuit (*see* 1(d)(2)) is actuated (*e.g.*, “switch S4 [is] turned on”) under said voltage supply mode (*see* 1(f)). Baek at [0052], [0056], [0057], [0062], Figures 3-5.

124. See my discussion of elements 1(d)(1)-1(f) above (Sections XI.A.b.v-viii).

125. For example, as discussed in 1(e)-1(f), Baek operates under voltage supply mode when a control signal C_PRE turns on switch S4, causing the circuit to “pre-charge a voltage of the storage capacitor CST,” which is “coupled to the gate of the first transistor M1.” Baek at [0056], [0062]. A person of ordinary skill in the art would have understood or at least found obvious that capacitor CST and transistor M1 are actuated in each “current sample/hold output circuit 370” during a pre-charge mode when the C_PRE signal switches S4 on. Baek at [0052]. Figure 4 of Baek shown below discloses that the current output circuits are actuated in a pre-charge mode (annotated blue).



Baek at Figure 4 (annotated).

e. Claim 4

126. This claim is disclosed and at minimum rendered obvious by Baek.

127. Claim 4 recites: “The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode.”

128. Baek discloses and at minimum renders obvious the current driving device according to claim 1, as discussed above.

129. Baek further discloses each of said current output circuits (*see* 1(d)(1)) is configured to stop said current-voltage converting circuit under said voltage supply mode (*e.g.*, during “pre-charge” mode, “first switch S1 and the second switch S2 [are] turned off”). Baek at [0056]-[0057], [0062], Figures 3-5.

130. See my discussion of elements 1(d)(1)-1(g) above (Sections XI.A.b.v-ix).

131. For example, as discussed in 1(e)-1(f), Baek discloses the switches S1 and S2 are turned off during a pre-charge mode such that the storage capacitor CST is not charged with “the analog gray-scale current.” Baek at [0056]-[0057], [0062]. A person of ordinary skill in the art would have understood that without a supplied current from the current source, the transistor M1 does not convert the source’s current to a voltage such that the current-voltage converting function stops and the pre-charge circuit 350 supplies “pre-charge ... voltage” to storage capacitor CST.⁵ Baek at [0062]. For example, without receiving the analog gray-scale current from DAC 330 (because the switches S1 and S2 are turned off) during the pre-charge mode (because the switch S4 mode is turned on), the transistor M1 does not perform the current-voltage converting function.

f. Claim 9

132. This claim is disclosed and at minimum rendered obvious by Baek.

⁵ This is consistent with the ’047 Patent, which discloses “each of the current output parts comprises a function of stopping the current-voltage converting function under the voltage supply mode” such that “all the electric currents supplied from the first voltage supply part [V1] can be utilized for charging the voltage holding part.” ’047 Patent at 4:25-31.

133. Claim 9 recites: “A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device.” Baek discloses and at minimum renders obvious the current driving device according to claim 1, as discussed above.

134. Baek discloses a current-driving-type display device (*e.g.*, “current-driven active matrix type OLED display devices”), comprising said current driving device according to claim 1 (*see* Section XI.A.b) mounted thereon so as to be driven by said current driving device (*e.g.*, “display driver circuit” “used to drive a display panel ... using a smaller current”). Baek at [0003], [0062], [0064], [0066].

135. For example, Baek discloses “a display driver circuit for a flat display panel.” Baek at [0003]. Baek further discloses that “the display driver circuit according to example embodiments of the present invention may be applicable to Organic Light Emitting Diode (OLED) display devices, for example, current-driven active matrix type OLED display devices.” Baek at [0064]. A person of ordinary skill in the art would have understood, and at minimum it would have been obvious, to mount the display driver circuit on the display device, as opposed to elsewhere, to advantageously “reduce a charge time” and “perform a sampling operation faster” while “more accurately output[ting] output signals to corresponding channels.” Baek at [0062], [0066]. Further, a person of ordinary skill in the art would have been motivated to mount the display driver circuit on the corresponding display panel to advantageously reduce the lengths of signal lines between the output terminals of the sample/hold circuits and the pixels. Such an implementation would have advantageously reduced a loss in the signals sent from the transistors M2 to the pixels, thereby enhancing the reliability of the circuits. Indeed, it was well-known in the art to mount display driver circuits on display panels. *See, e.g.*, Ex. 1012 (“Nohtomi”), [0002]-[0004] (discussing “a

driver circuit for driving the liquid crystal panel” is “installed” on a “dot matrix type liquid crystal panel”).

B. GROUND 3: BAEK IN VIEW OF DATE

136. “Date” refers to United States Patent Application Publication No. 2005/0231241, entitled “Current Driver.” Date names Yoshito Date and Akira Matsuzawa as inventors and was assigned to Matsushita Electric Industrial Co., Ltd. Date was filed in the United States on April 4, 2005 and published on October 20, 2005. Thus, Date published more than one year before the earliest possible US priority date of the ’047 Patent. Accordingly, I understand that Date qualifies as prior art to the ’047 Patent.

a. Claim 5

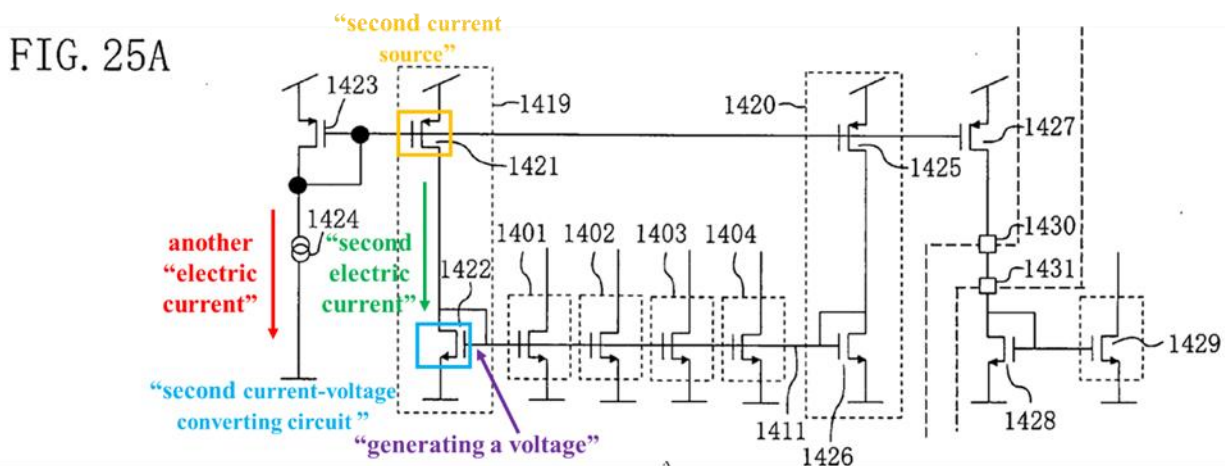
137. This claim is rendered obvious by Baek in view of Date.

138. Claim 5 requires the “current driving device according to claim 1, further comprising a second current supply source for supplying a second electric current that is proportional to said first electric current; and a second current-voltage converting circuit for generating said first voltage by receiving said second electric current, wherein said first voltage supply source controls supplies of said first voltage generated by said second current-voltage converting circuit to said current output circuits.” As discussed above in Section XI.A.b, Claim 1 is disclosed and at minimum rendered obvious by Baek. As discussed further below, Claim 5 is rendered obvious when Date’s teachings of a second current supply source and second current-voltage converting circuit are applied to Baek’s driver circuit.

139. Baek discloses the first electric current (*e.g.*, “an analog gray-scale current”), the first voltage (*e.g.*, “voltage” from “pre-charge circuit 350”), the first voltage supply source (*e.g.*, “pre-charge circuit 350”), and the current output circuits (*e.g.*, “current sample/hold circuits 370-(M+1) through 370-N”).

140. See my discussion of elements 1(a)-1(b) and 1(d) above (Sections XI.A.b.ii-iii and v-vi).

141. Date discloses a second current supply source (*e.g.*, “p-transistor 1421”) for supplying a second electric current that is proportional to an electric current (*e.g.*, “a current ... flows in the p-transistor 1421” based on its “gate-size ratio between ... p-transistor 1423 and the p-transistor 1421,” the former of which “draws a current” from “current source 1424”) and a second current-voltage converting circuit (*e.g.*, “n-transistor 1422” in addition to “output n-transistors 1405 through 1410”) for generating a voltage (*e.g.*, “a gate voltage ... generated at the gate of the n-transistor 1422”) by receiving said second electric current (*e.g.*, “receiv[ing] a current flowing in the p-transistor 1421”), wherein a voltage generated by said second current-voltage converting circuit is supplied to said current output circuits (*e.g.*, “a gate voltage ... [on] the n-transistor 1422” is “supplied to the gates of the output n-transistors” in “current mode D/A converters 1401 through 1404”). Date at [0008]-[0012], Figure 25A.



Date at Figure 25A (annotated).

142. For example, Date discloses a “current driver[] suitable as [a] display driver[] for,” for example, “organic EL (electro luminescence) panels, LED (light emitting diode) panels and the like.” Date at [0002]. The driver includes a first “current source 1424” that “draws a current

which has been set at an arbitrary current value” in “bias p-transistor 1423.” Date at [0008]-[0009]. The current driver further includes a “current mirror” of “bias p-transistor 1423 and the p-transistor 1421” such that “a current according to the gate-size ratio between the p-transistor 1423 and the p-transistor 1421 flows in the p-transistor 1421.” Date at [0009]. A person of ordinary skill in the art would have understood or at least found it obvious that the p-transistor 1423 is a second current source, since it supplies current.⁶

143. Date further discloses an n-transistor 1422 “receives a current flowing in the p-transistor 1421” and “a gate voltage (bias voltage) according to the current input to the n-transistor 1422 is generated at the gate of the n-transistor 1422” and “supplied to the gates of the output n-transistors 1405 through 1410” via “gate line 1411.” Date at [0010]-[0012]. A person of ordinary skill in the art would have understood or at least found it obvious that the n-transistor 1422 is a second current-voltage converting circuit, including because it converts a current into a voltage at the gate of the n-transistor 1422.⁷

144. Like Baek, Date is in the same field as the '047 Patent and is reasonably pertinent to the problems addressed by the '047 Patent. For example, the '047 Patent's field includes driver circuits and the '047 Patent purports to address the problem of providing sufficient current to lighting elements of display panels. '047 Patent at Abstract (“A current driving device ... and a plurality of current output parts ... The current output part takes three operation modes ... By charging the current output part with the reference voltage before the calibration performed by using the reference current, calibration of the current output part is performed at a high speed.”),

⁶ This is consistent with the '047 Patent, which discloses “a reference current supply transistor QP2 that constitutes a second current supply part.” '047 Patent at 10:31-33.

⁷ This is consistent with the '047 Patent, which discloses “current-voltage converting transistor[] QNx” in addition to “Nch transistors QN1-QNm” '047 Patent at 8:1-15, 10:34-35.

3:18-22 (“An object of the present invention therefore is to provide a current driving device which can perform calibration at a high speed and improve the non-uniformity of the output currents even when a reference current is very small and when there is a change in the reference current.”), 5:20-25 (“A display device according to the present invention related to the current driving device described above comprises one of the above-described current driving devices mounted thereon so as to be driven by the current driving device. Displays on the screen can be made uniform with this display device.”).

145. Baek’s field includes driver circuits as well, and Baek is pertinent to the problem of providing sufficient current to lighting elements of display panels. Baek at [0003] (“Example embodiments of the present invention relate to a display driver circuit for a flat display panel and a display driving method using the same. More particularly, example embodiments of the present invention relate to a display driver circuit, a current sample/hold circuit, and a display driving method using the display driver circuit.”), [0005] (“A liquid crystal display (LCD) and a plasma display panel (PDP) are the two most common type of flat panel displays. Recently, an organic light emitting diode (OLED) display, which features higher contrast and/or quicker response time, is a type of display that has gain increased attention.”), [0063] (“The output terminal OUT[K] may be used to drive a display panel (not shown) using a smaller current. The output terminal OUT[K] may be pre-charged, which may be implemented using the third transistor M3, to quickly provide display data to a display panel (not shown). In other words, the third transistor M3 may be turned on to pre-charge the output terminal OUT[K] with a pre-charge voltage VPRE in response to an output pre-charge signal PREON before the output signals are applied to the output terminal OUT[K].”).

146. Date's field also includes driver circuits, and it is pertinent to the problem of providing sufficient current to lighting elements of display panels. Date at [0002] ("The present invention relates to current drivers and particularly to current drivers suitable as display drivers for organic EL (electro luminescence) panels, LED (light emitting diode) panels and the like."), [0019] ("In addition, the current driver is configured as a single semiconductor LSI. Though the configuration for only four outputs is shown in FIG. 25A, current mode D/A converters corresponding to 400 to 600 outputs can be provided on the same semiconductor (i.e., one current driver) as the number of outputs of the current driver increases. On the other hand, a plurality of such semiconductor LSIs (current drivers) provided with current mode D/A converters are used to output a large number of output currents to a flat panel display with a large screen in some cases."), [0020] ("Now, the case of using a plurality of semiconductor LSIs will be described. In this case, the plurality of semiconductor LSIs (two semiconductor LSIs in this case) are arranged in series in a frame portion of a flat panel.").

147. In implementing Date's teachings in Baek's driver circuit, a person of ordinary skill in the art would have understood that, for each current sample/hold circuit 370, the analog gray-scale current from the "current digital-to-analog conversion unit 330" is used as a reference current, mirrored in a p-transistor, and supplied to a corresponding n-transistor. The voltage generated by the n-transistors, as taught by Date, would be used as the pre-charge circuit 350, as taught by Baek. A person of ordinary skill in the art would have understood that such an implementation would have advantageously simplified the circuitry used to drive the LEDs of the display panel, as it would have used the "analog gray-scale current" from "current digital-to-analog conversion unit 330" to create the voltage supplied by the pre-charge circuit 350.

148. Baek does not disclose how the pre-charge circuit 350 is implemented. A person of ordinary skill in the art would have understood that one way to implement such circuitry is using the “gate voltage (bias voltage) ... generated at the gate of the n-transistor 1422” as taught by Date. Date at [0010]-[0012]. Indeed, Date discloses that this “gate voltage” is “supplied to the gates of the output n-transistors 1405 through 1410” via “gate line 1411,” and is therefore consistent with Baek’s pre-charge circuit teachings, whereby the pre-charge circuit supplies voltage to the gates of transistors M1 and M2 to output current. Date at [0010]-[0012]; Baek at [0036], [0054], [0058], [0063].

149. Further, a person of ordinary skill in the art would have been motivated to use Date’s bias circuit teachings in implementing Baek’s driver circuit to advantageously enhance reliability of the circuit by providing a constant voltage based on a constant current source. For example, a person of ordinary skill in the art would have understood that the current mirror comprising the two p-transistors taught in Date was well-known in the art and provided many advantages, including that the p-transistor 1421 would provide a constant current irrespective of the load applied. Ex. 1013 (“Schaffer”) at [0005] (“Furthermore, the device contains a current mirror that mirrors the reference current from the selected leg(s) of the current mirror to the load output current.”), [0006] (“In particular, a dynamic element matching approach employed in the current mirror ensures high accuracy throughout a large range of the output current. Limitations to the voltage headroom or power efficiency at high output currents are eliminated.”); Ex. 1014 (“Chang”) at [0020] (“In view of the foregoing, since the N-mirror transistors or MOSFETs Q 11, Q12, . . . , Q1N are integrated with the same size (W/L ratio), the multiple-output current mirror 30 creates a current mirror effect which is used to generate automatic current sharing which is almost independent of the DC input voltage source providing voltage VDC, almost independent

of the MOSFET's variation from the semiconductor integration process, and almost independent of temperature variation.”), [0025] (“Since the N-mirror transistors or MOSFETs Q 101, Q102 . . . , Q10N and the N-cascode transistors or MOSFETs Q111, Q112, . . . , Q11N are integrated on the same substrate 136 with the same process and with the same size (W/L ratio) and wherein the each mirror-cascode transistor or MOSFET pair MC1, MC2, . . . , MCN have the same source and gate connections, the multiple-output cascode current mirror 130 creates a current mirror effect which is used to generate automatic current sharing which is almost independent of the DC input voltage source VDC, almost independent of the MOSFET's variation from the semiconductor integration process, and almost independent of temperature variation while also improving the output impedance of the constant current mirror which delivers the constant current in the LEDs.”). A person of ordinary skill in the art would have understood that the constant current provided by p-transistor 1421 to n-transistor 1422 would generate a constant gate voltage based on the constant current. Therefore, the voltage of the gate of the n-transistor 1422 would be constant irrespective of the load, including the load comprising the capacitor CST and transistors M1 and M2 as taught by Baek.

150. A person of ordinary skill in the art would have had a reasonable expectation of success in applying Date’s teachings in implementing Baek’s driver circuit because it is a straightforward use of Date for its intended purpose that would have yielded the predictable results of supplying a voltage by using a reference current. Indeed, both Baek and Date disclose using transistors to perform various current and voltage supplying functions. See Baek at [0055]-[0056]; Date at [0007]-[0010]. This would have been a straightforward application of Date’s teachings in a manner that advantageously improves Baek’s driver circuit.

b. Claim 6

151. This claim is rendered obvious by Baek in view of Date.

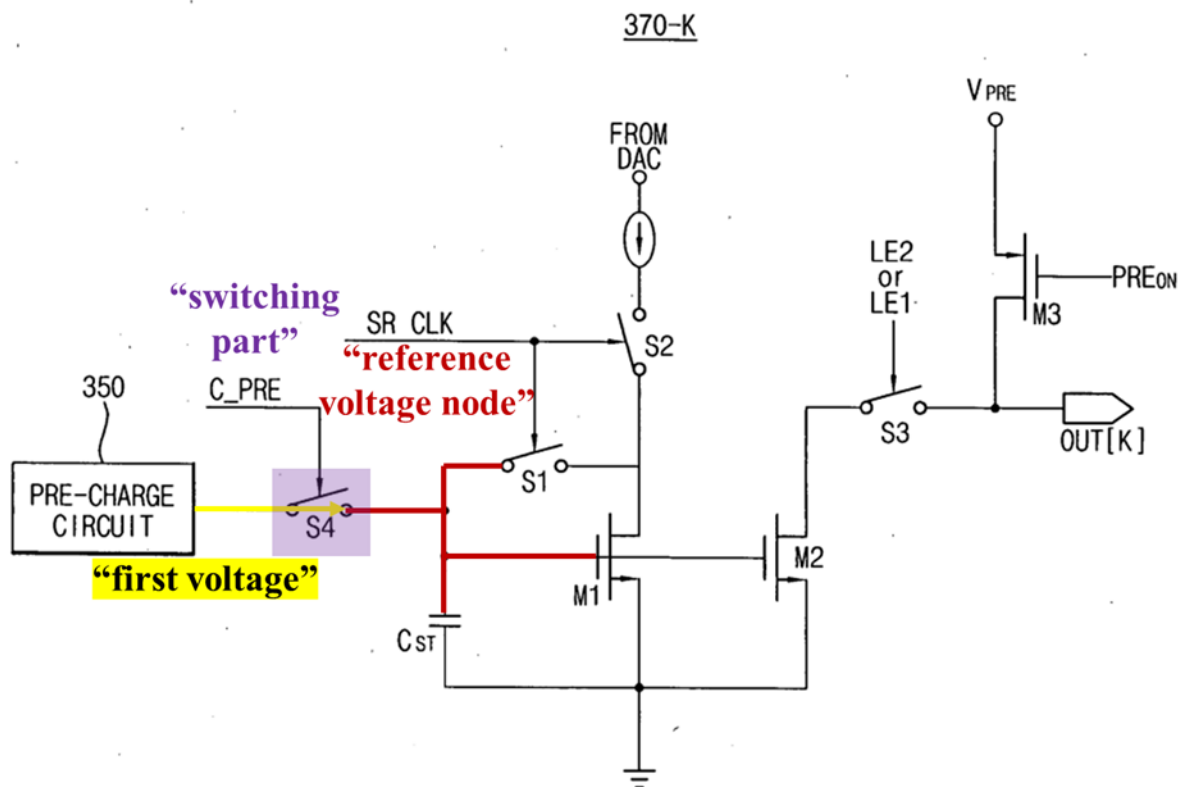
152. Claim 6 requires “The current driving device according to claim 5, wherein said second current-voltage converting circuit comprises a switching part for short-circuiting a node at which said first voltage emerges to a reference voltage node.”

153. Date discloses the second current-voltage converting circuit. *See* (5) (Section XI.B.a).

154. Baek discloses a switching part for short-circuiting a node (*e.g.*, “switch S4” is “turned on”) at which said first voltage (*e.g.*, “pre-charge ... voltage”) emerges to a reference voltage node (*e.g.*, supplied to node comprising transistor M1, capacitor CST, and switches S1 and S4). Baek at [0057], [0062], Figure 5.

155. As discussed in 1(d)(2)-1(f), Baek discloses that, during a pre-charge mode, “switch S4” is “turned on” (annotated purple) and switches S1, S2 and S3 are turned off such that pre-charge circuit 350 “pre-charge[s] a voltage” (annotated yellow) “of the storage capacitor CST” “to a voltage level slightly lower than a threshold voltage of the first transistor M1.” Baek at [0057], [0062]. A person of ordinary skill in the art would have understood or at least found it obvious that turning on a switch short-circuits a node such that the voltages on both sides of the switch become the same. Therefore, a person of ordinary skill in the art would have understood that switch S4 turning on short-circuits a node, newly created by the activation of switch S4 and comprising the node at the first voltage (annotated yellow) and the reference voltage mode (annotated dark red), such that the pre-charge voltage emerges at another node (annotated dark red) that includes the connections between transistor M1’s gate, capacitor CST, and switches S1 and S4.

FIG. 5



Baek at Figure 5 (annotated).

156. This is consistent with the '047 Patent, which discloses switches G1-Gm and Sw2 are turned on such that "drains and gates of Nch transistors QN1-QNm are short-circuited to receive electric currents from a reference current source I1." '047 Patent at 1:40-47.

157. In applying Date's second current-voltage converting circuit teachings to Baek's driver circuit (as discussed in (5), Section XI.B.a), a person of ordinary skill in the art would have found it obvious to implement switch S4 to short-circuit the node containing the gate voltage (e.g., n-transistor 1422 (as taught by Date)) so that it emerges at the node (annotated dark red) that includes the connections between transistor M1's gate, capacitor C_{ST}, and switches S1 and S4.

Therefore, a person of ordinary skill in the art would have found it obvious to apply Date's concepts in implementing Baek's driver circuit.

158. To the extent it is argued that the recited "a reference voltage node" must be different from the node comprising the recited "a terminal being connected to a reference voltage" (from 1(d)(2)), the connection to S4 is different from the connection to transistor M1 discussed in 1(d)(2).

C. GROUND 4: BAEK IN VIEW OF INOMOTO

159. "Inomoto" refers to WIPO Publication No. 2006/080260, entitled "Power source system." Inomoto names Tomoyuki Inomoto as the sole inventor and was assigned to Matsushita Electric Industrial Co., Ltd. Inomoto was published on August 3, 2006. Thus, Inomoto published more than one year before the earliest possible US priority date of the '047 Patent. Accordingly, I understand that Inomoto qualifies as prior art to the '047 Patent.

a. Claim 7

160. This claim is rendered obvious by Baek in view of Inomoto.

161. Claim 7 requires the "current driving device according to claim 1, further comprising a second voltage supply source with a larger voltage supply capacity than that of said first voltage supply source, wherein the use of said first voltage supply source and the use of said second voltage supply source are switched in accordance with the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits." As discussed above in Section XI.A.b, Claim 1 is disclosed and at minimum rendered obvious by Baek.

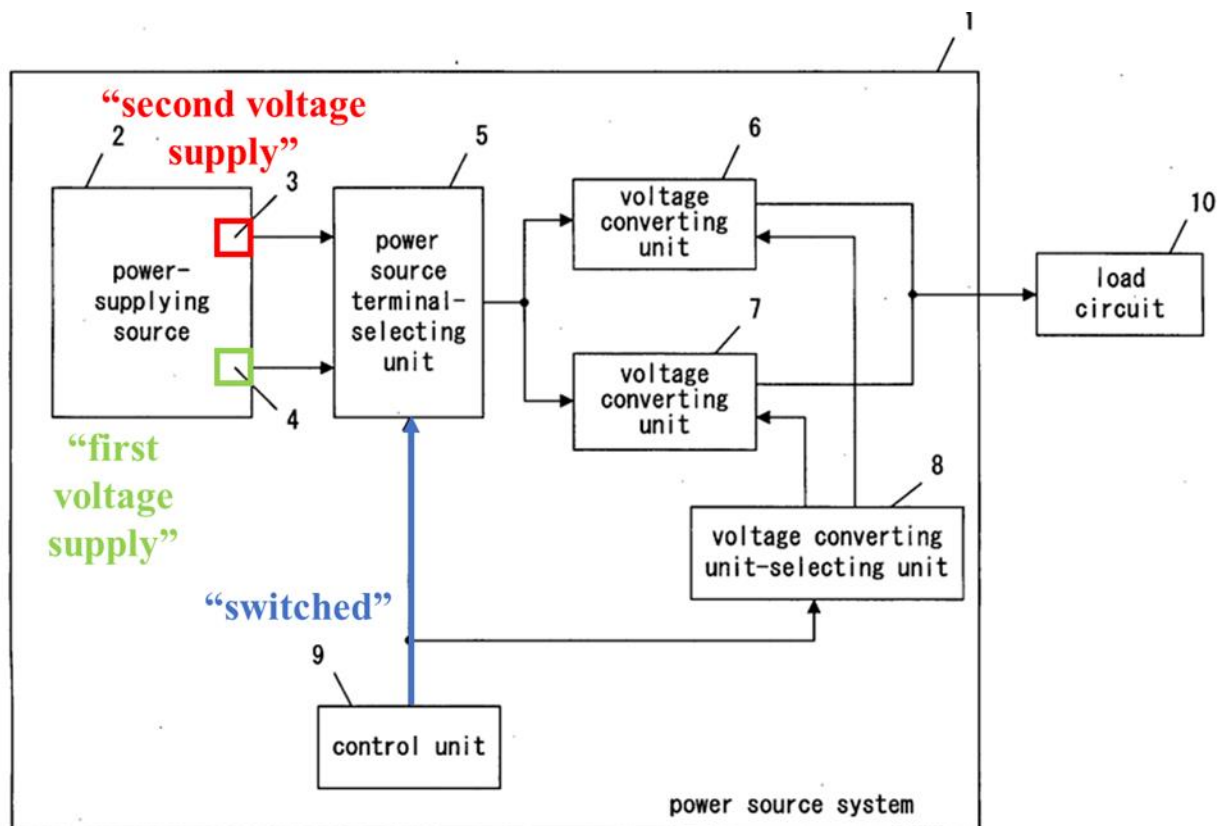
162. Baek discloses the first voltage supply source (*e.g.*, "pre-charge circuit 350" supplying "voltage") and the number of said current output circuits (*e.g.*, "current sample/hold circuits 370-(M+1) through 370-N") that operate in said voltage supply mode (*e.g.*, "pre-charge"

mode to “pre-charge a voltage of the storage capacitor CST”) among said plurality of current output circuits (*e.g.*, “current sample/hold circuits 370-(M+1) through 370-N”). Baek discloses that there are M+1 to N number of current sample/hold circuits. Baek at [0038]-[0039], [0047]-[0049], [0052].

163. See my discussion of elements 1(a), 1(d)(1), and 1(e) above (Sections XI.A.b.ii, v, and vii).

164. Inomoto discloses a second voltage supply source (*e.g.*, “power source terminal 3” of “power-supplying source 2”) with a larger voltage supply capacity (*e.g.*, “higher ... output voltage”) than that of said first voltage supply source (*e.g.*, “power source terminal 4”), wherein the use of a first voltage supply source and the use of said second voltage supply source are switched (*e.g.*, “selection control signal” selects which voltage to apply) in accordance with the number of circuits (*e.g.*, “based on ... a quantity of loads ... of the load circuit 10”). Inomoto at 1:6-7, 3:3-18, 13:18-14:1, 16:17-20, 17:12-18.

165. Inomoto discloses a “power source system” that supplies “electrical power” to, for example, “a display panel” to reduce “malfunction[s]” and “wanted power consumption.” Inomoto at 1:6-7, 3:3-18, 13:18-14:1. The system “power-supplying source 2” that includes a “power source terminal 3” that is “higher in output voltage” than a “power source terminal 4.” Inomoto at 13:18-19, 13:27-14:1. Terminal 3 is “connected to the head of the serially interconnected internal power source cells 14” while terminal 4 is only connected at an “intermediate” point, thus receiving less voltage from the power source cells. Inomoto at 13:22-27. A “control unit 9” “selects either one of the power source terminals” using a “selection control signal” that is “generated based on” a “quantity of loads” active on “the load circuit 10.” Inomoto at 16:17-20, 17:12-18.



Inomoto at Figure 1 (annotated).

166. Like Baek, Inomoto is in the same field as the '047 Patent and is reasonably pertinent to the problems addressed by the '047 Patent. For example, the '047 Patent's field includes driver circuits and the '047 Patent purports to address the problem of providing sufficient current to lighting elements of display panels. '047 Patent at Abstract ("A current driving device ... and a plurality of current output parts ... The current output part takes three operation modes ... By charging the current output part with the reference voltage before the calibration performed by using the reference current, calibration of the current output part is performed at a high speed."), 3:18-22 ("An object of the present invention therefore is to provide a current driving device which can perform calibration at a high speed and improve the non-uniformity of the output currents even when a reference current is very small and when there is a change in the reference current."), 5:20-25 ("A display device according to the present invention related to the current driving device

described above comprises one of the above-described current driving devices mounted thereon so as to be driven by the current driving device. Displays on the screen can be made uniform with this display device.”).

167. Baek’s field includes driver circuits as well, and Baek is pertinent to the problem of providing sufficient current to lighting elements of display panels. Baek at [0003] (“Example embodiments of the present invention relate to a display driver circuit for a flat display panel and a display driving method using the same. More particularly, example embodiments of the present invention relate to a display driver circuit, a current sample/hold circuit, and a display driving method using the display driver circuit.”), [0005] (“A liquid crystal display (LCD) and a plasma display panel (PDP) are the two most common type of flat panel displays. Recently, an organic light emitting diode (OLED) display, which features higher contrast and/or quicker response time, is a type of display that has gain increased attention.”), [0063] (“The output terminal OUT[K] may be used to drive a display panel (not shown) using a smaller current. The output terminal OUT[K] may be pre-charged, which may be implemented using the third transistor M3, to quickly provide display data to a display panel (not shown). In other words, the third transistor M3 may be turned on to pre-charge the output terminal OUT[K] with a pre-charge voltage VPRE in response to an output pre-charge signal PREON before the output signals are applied to the output terminal OUT[K].”).

168. Inomoto’s field also includes driver circuits, and it is pertinent to the problem of providing sufficient current to lighting elements of display panels. Inomoto at 1:6-7 (“The present invention relates to a power source system incorporated in a variety of electronic apparatuses.”), 1:15-20 (“The current trend is that the electronic apparatus is provided with a variety of extended functions, resulting in increase in required electrical power. Meanwhile, the electronic apparatus

must consume reduced electrical power to ensure operating time of the electronic apparatus. These two conflicting issues of the electronic apparatus, i.e., improved electronic apparatus functions and reduced power consumption, must be smoothed out.”), 1:26-2:8 (“The power source system 100, which is operable to supply a load circuit 106 with the electrical power, includes elements as discussed below. A power-supplying source 101 such as a rechargeable battery is an electrical power supplier. The load circuit 106 includes all electronic circuits that must be supplied with the electrical power, such as various electronic components, ICs, and a display panel, each of which actuates the electronic apparatus. The power-supplying source 101 includes a power source terminal 102 connected to both a switching regulator 103 and a series regulator 104. A control unit 105 is operable to select either the switching regular 103 or the series regulator 104 to use the selected regulator. The load circuit 106 is supplied with the electrical power through the output from the selected regulator.”), 3:3-27 (“However, increased consumption current in the load circuit 106 reduces the output voltage of the power source terminal 102 ... brings about a problem of malfunction of the load circuit 106 ... However, as a result of the alternative, a higher voltage is objectionably supplied to the load circuit 106 although the load circuit 106 requires a smaller consumption current, with a consequential increase in unwanted power consumption. In addition, a difference between input and output voltages of each of the switching regulator 103 and the series regulator 104 is increased, thereby increasing a voltage amount required to lower the voltage in each of the switching regulator 103 and the series regulator 104. This causes another problem of increased loss of power consumption in each of the switching regulator 103 and the series regulator 104 as well as that in the load circuit 106 ... One of the problems is that the inability of the proper supply of the electrical power to the load circuit 106 results in increased power consumption. The increased, unwanted power consumption brings about another problem of reduced operating time

of an electronic apparatus. A further problem is that the power reduction-caused malfunction of the load circuit results in reduced reliability of the electronic apparatus in terms of electronic apparatus activities.”), 13:2-5 (“To permit the electronic apparatus to function, the load circuit 10 includes a variety of elements, to which the electrical power must be supplied, such as electronic components, a printed circuit board, a network, an integrated circuit such as an IC and a LSI, a display panel, and an input device.”), 13:18-14:1 (“As illustrated in Fig. 3, the power-supplying source 2 includes a plurality of internal power source cells 14 serially connected together. Each of the internal power source cells 14 has a certain output voltage. The serially interconnected internal power source cells 14 form the power-supplying source 2 having a predetermined output voltage. The power source terminals 3, 4 are connected to the serially interconnected internal power source cells 14 at different connections thereof. As illustrated in Fig. 3(a), the power source terminal 3 is connected to the head of the serially interconnected internal power source cells 14 at an output point thereof, while the power source terminal 4 is connected to intermediate one of the serially interconnected power source cells 14 at an output point thereof. As a result, the power source terminal 3 is higher in output voltage than the power source terminal 4.”), 16:17-20 (“The control unit 9 has control of a selection to be made by each of the power source terminal-selecting unit 5 and the voltage converting unit-selecting unit 8. The power source terminal-selecting unit 5 selects either one of the power source terminals 3, 4.”), 17:12-18 (“The selection control signal is generated based on measured consumption current in the load circuit 10 or otherwise a quantity of loads imposed on processing activities of the load circuit 10. Alternatively, the selection control signal is generated in response to user input from the outside. The control unit 9 may optionally be implemented by a programmably operable processor, and in this option, the selection control signal is generated by input from the outside or otherwise by any predetermined program.”).

169. A person of ordinary skill in the art would have been motivated to apply Inomoto's two voltage supplies teachings to Baek's driver device, as Inomoto provides implementation details regarding how Baek's pre-charge circuit supplies a voltage during a pre-charge mode. Baek does not disclose the details of how the pre-charge circuit supplies voltage, and a person of ordinary skill in the art would have turned to Inomoto's teachings, which provide this known way of using a selectable voltage supply based on the number of current output circuits drawing current.

170. Further, a person of ordinary skill in the art would have been motivated to apply Inomoto's two voltage supplies teachings in implementing Baek's driver device to advantageously enhance the reliability and reduce unwanted power consumption. For example, Inomoto teaches "increased consumption current in the load circuit ... results in a drop in voltage, thereby reducing the output voltage of the power source terminal," causing "malfunctions." Inomoto at 3:3-8. Inomoto further teaches providing "a higher voltage ... to the load circuit" that "requires a smaller consumption current" causes "unwanted power consumption." Inomoto at 3:9-18. A person of ordinary skill in the art would have been motivated to apply Inomoto's variable power supply teachings in implementing Baek's driver device to advantageously provide flexibility in the voltage supplied during a pre-charge mode based on the number of sample/hold circuits applied at the load, such that a proper voltage is applied based on number of sample/hold circuits needing the capacitor CST charged as taught by Baek. For example, **Baek** discloses that the "first sample/hold output circuit 360 ... include[s] current sample/hold circuits 360-1 through 360-M" and "second sample/hold output circuit 370 ... include[s] current sample/hold circuits 370-(M+1) through 370-N." Baek, [0038]-[0039]. The "output process" for the first circuit 360 and second circuit 370 "may be alternately performed" such that there are two different groups of outputs (Baek, [0052]), and a person of ordinary skill in the art would have been motivated to switch

between voltage supplies based on the corresponding number of current output circuits used by the first circuit 360 or second circuit 370.

171. For example, a person of ordinary skill in the art would have recognized the benefits of applying Inomoto's teachings of using selectable voltage supplies to implement Baek's pre-charge circuit such that it supplies a first voltage when a smaller number of current output circuits are selected to advantageously reduce unwanted power consumption by using a second, larger voltage supply. Further, a person of ordinary skill in the art would have recognized the benefits of applying Inomoto's teachings of using selectable voltage supplies to implement Baek's pre-charge circuit such that it supplies a second larger voltage when a larger number of current output circuits are selected to advantageously prevent malfunctions by a voltage drop from too many sample/hold circuits as loads to the pre-charge circuit.

172. A person of ordinary skill in the art would have had a reasonable expectation of success in applying Inomoto's teachings in implementing Baek's driver circuit because it is a straightforward use of Inomoto for its intended purpose that would have yielded the predictable results of switching between two voltage supplies. Indeed, both Baek and Inomoto disclose voltage supplies. *See* Baek at [0036], [0062]-[0063]; Inomoto at 13:18-27, 13:27-14:1. This would have been a straightforward application of Inomoto's teachings in a manner that advantageously improves Baek's driver circuit.

173. In implementing Inomoto's two voltage supplies teachings in Baek, a person of ordinary skill in the art would have understood or at least found obvious that another pre-charge circuit is supplied and switched to when there are many current output circuits drawing current.

b. Claim 8

174. This claim is rendered obvious by Baek in view of Inomoto.

175. Claim 8 requires the “current driving device according to claim 1, wherein said first voltage supply source is configured to change its voltage supply capacity in accordance with the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits.” As discussed above in Section XI.A.b, Claim 1 is disclosed and at minimum rendered obvious by Baek. Claim 8 is met for the same reasons as claim 7. While claim 7 recites switching between two voltage supply sources depending on the number of said current output circuits that operate in said voltage supply mode among said plurality of current output circuits, claim 8 more broadly recites changing the voltage supply capacity in accordance with that number.

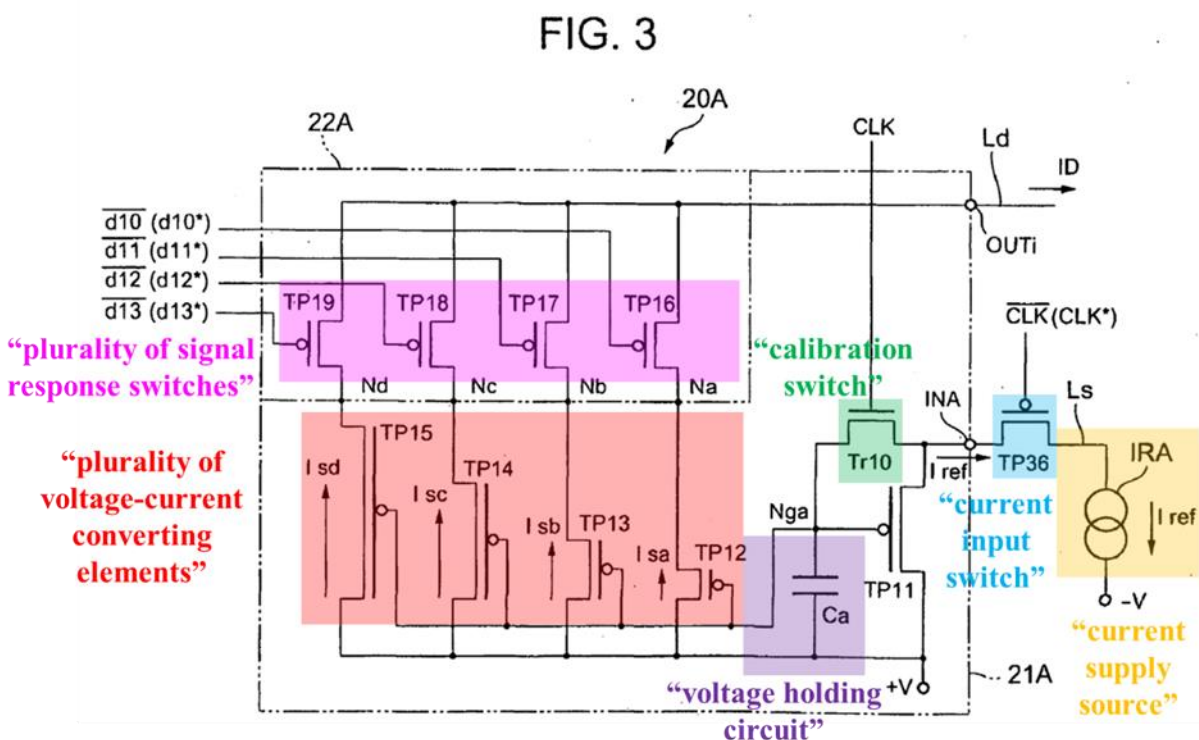
D. GROUND 5: SASAKI

a. Overview of Sasaki

176. “Sasaki” refers to United States Patent Application Publication No. 2005/0017765, entitled “Current Generation Supply Circuit and Display Device.” Sasaki names Kazuhiro Sasaki and Katsuhiko Morosawa as the inventors and was assigned to Casio. Sasaki was filed in the United States on July 14, 2004 and published on January 27, 2005. Thus, Sasaki published more than one year before the earliest possible US priority date of the ’047 Patent. Accordingly, I understand that Sasaki qualifies as prior art to the ’047 Patent.

177. Sasaki discloses a “current generation supply circuit” that “drive[s]” a “display device.” Sasaki at [0003]. The circuit includes a “**current supply source control transistor TP36**” that “switch[es] ‘ON/OFF’” to connect and disconnect a “**constant current generation source IRA**” that “supplie[s]” a “reference current Iref.” Sasaki at [0062]-[0064]. A “**refresh control transistor Tr10**” causes “the reference current Iref [to] flow[]” to “charge” **capacitor Ca**. Sasaki at [0063], [0071], [0077], [0138]. When voltage is stored in **capacitor Ca**, the **module current transistors TP12-TP15** are turned on and generate “module currents Isa~Isd ... relative

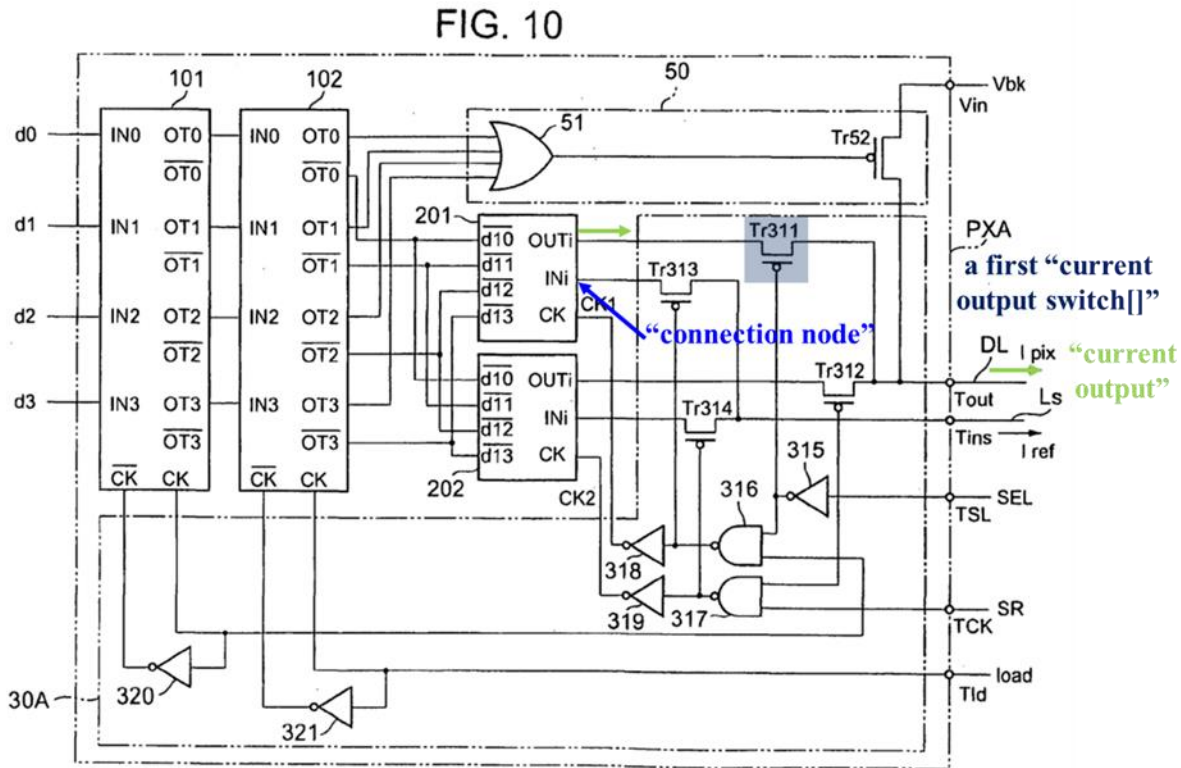
to the constant reference current I_{ref} based on the reference voltage stored in capacitor C_a . Sasaki at [0066]-[0068]. **Switching transistors TP16~TP19** are “connected to each of the module current transistors TP12~TP15” and turn “ON” or “OFF” to supply the “load drive currents I_D ” comprising “composite value of the[] module currents” to the loads based on “signals $d10^* \sim d13^*$.” Sasaki at [0065], [0069]-[0070], [0152]. The load drive current flow “toward the current output contact OUT_i via the drive current supply line L_d .” Sasaki at [0069].



Sasaki at Figure 3 (annotated).

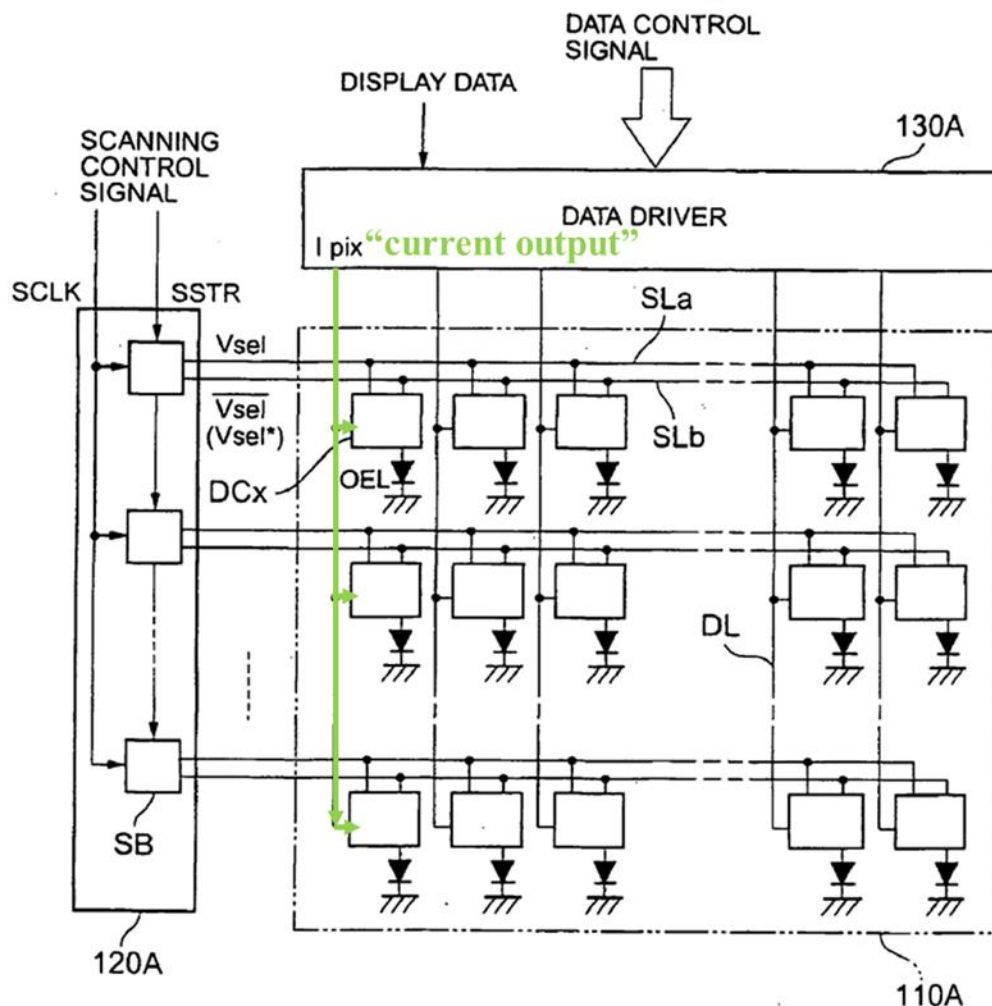
178. As shown in Figure 10 below, Sasaki further discloses that a “gradation current generation section 201” that “ha[s] an equivalent configuration to the current generation section 20A” discussed above. Sasaki at [0127]. The current generation section 201 includes an IN_i connection node connected to a “**constant current generation source.**” Sasaki at [0063]-[0064], [0071], [0144]. The current generation section 201 includes a contact OUT_i , which supplies the

“composite value of the[] module currents” from **switching transistors TP16~TP19** to the loads. Sasaki at [0065], [0069], [0152]. The current generation section 201 is connected to an “**output control transistor[] Tr311**” that outputs **current I_{pix}**, which is “equivalent to the drive current supply line L_d mentioned above.” Sasaki at [0124], [0130], [0135], [0142].



Sasaki at Figure 10 (annotated).

179. **Output current I_{pix}** flows through output control transistor Tr311 and into “pixel driver circuits DC_x” (shown in Figure 7 below) via a data line DL to “control the write-in of the gradation currents I_{pix} in each of the display pixels.” Sasaki at [0102], [0113]-[0117], [0130]-[0131].



Sasaki at Figure 7 (annotated).

180. Each pixel driver circuit DCx includes a “**Pch FET Tr42**” connected to the data line DL that is turned “ON” to supply the **current I_{pix}** to the “light emitting device[.]” via “**contact Nxa**.” Sasaki at [0113], [0116].



i. 10(pre): “A current driving device, comprising:”

182. To the extent the preamble is limiting, Sasaki discloses a current driving device (*e.g.*, “current generation supply circuit ... supplies drive currents”). Sasaki at Abstract, [0003].

IPR2025-01330 Page 00091

185. Sasaki discloses a current input switch for controlling connection/disconnection states (*e.g.*, “current supply source control transistor TP36” controls connection/disconnection) with respect to a current supply source (*e.g.*, “constant current generation source IRA”). Sasaki at [0062]-[0064], Figure 3.

The diagram shows a 4-bit digital-to-analog converter (20A) and its associated current input switch (21A) and current supply source. The converter 20A has four data inputs: $d10^*$ (TP19), $d11^*$ (TP18), $d12^*$ (TP17), and $d13^*$ (TP16). These inputs control transistors Nd, Nc, Nb, and Na. The output of the converter is ID (OUTi). The current input switch 21A is controlled by CLK and CLK^* signals. It includes a current input switch (TP36) and a current supply source (IRA) connected to $-V$. The current supply source provides a reference current I_{ref} to the current input switch. The current input switch also receives a reference current I_{ref} from the current supply source. The current input switch is connected to the output of the converter 20A.

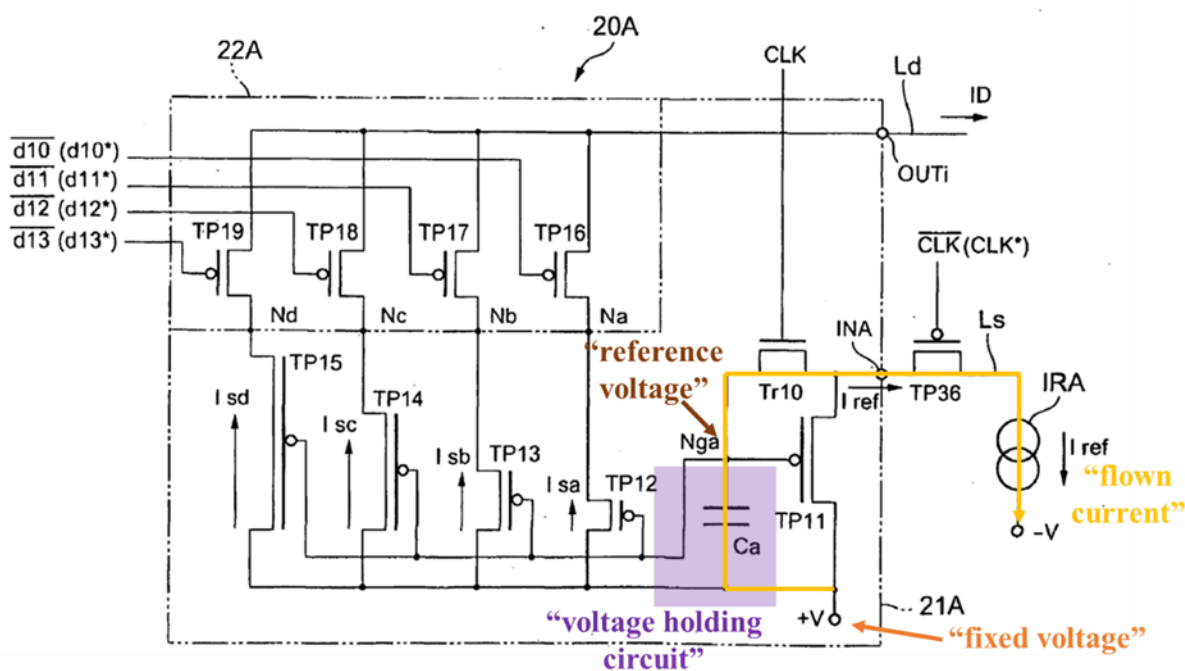
186. For example, Sasaki discloses a “current supply source control transistor TP36” (annotated light blue) that “switch[es] ‘ON/OFF’” to connect and disconnect a “constant current generation source IRA” (annotated gold) that “supplie[s]” a “reference current Iref.” Sasaki at [0062]-[0064], Figure 3.

- iii. 10(b): “a voltage holding circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;”

187. This limitation is disclosed and at minimum rendered obvious by Sasaki.

188. Sasaki discloses a voltage holding circuit for holding a reference voltage (*e.g.*, “capacitor Ca (charge storage circuit)” for holding “specified voltage”), which is charged by a flown current (*e.g.*, “recharg[ed]” by “reference current Iref”), the voltage holding circuit having a first terminal (*e.g.*, “capacitor Ca is connected” to “high electric potential +V”) and a second terminal (*e.g.*, “contact Nga (gate terminal of the reference current transistor TP11)”), the first terminal being connected to a fixed voltage (*e.g.*, fixed “potential +V”). Sasaki at [0063], [0071], [0077], [0138].

FIG. 3



Sasaki at Figure 3 (annotated).

189. For example, Sasaki discloses a “capacitor Ca” (annotated purple) “connected between the high electric potential +V” (annotated orange) and “the contact Nga (gate terminal of the reference current transistor TP11).” Sasaki at [0063]. The capacitor stores “electrical charge supplied to the contact Nga,” including when “recharg[ed]” by the “reference current Iref ... flowing in the current path” (annotated gold). Sasaki at [0071], [0077], [0138]. A person of ordinary skill in the art would have understood the high electric potential +V represents a constant fixed voltage supply. Designations such as “+V,” in connection with designations such as VDD and VCC, are commonly used on circuit diagrams to depict a fixed supply voltage that is supplied to the drain of a MOSFET, as I discuss in Section X.C.a-b, e.

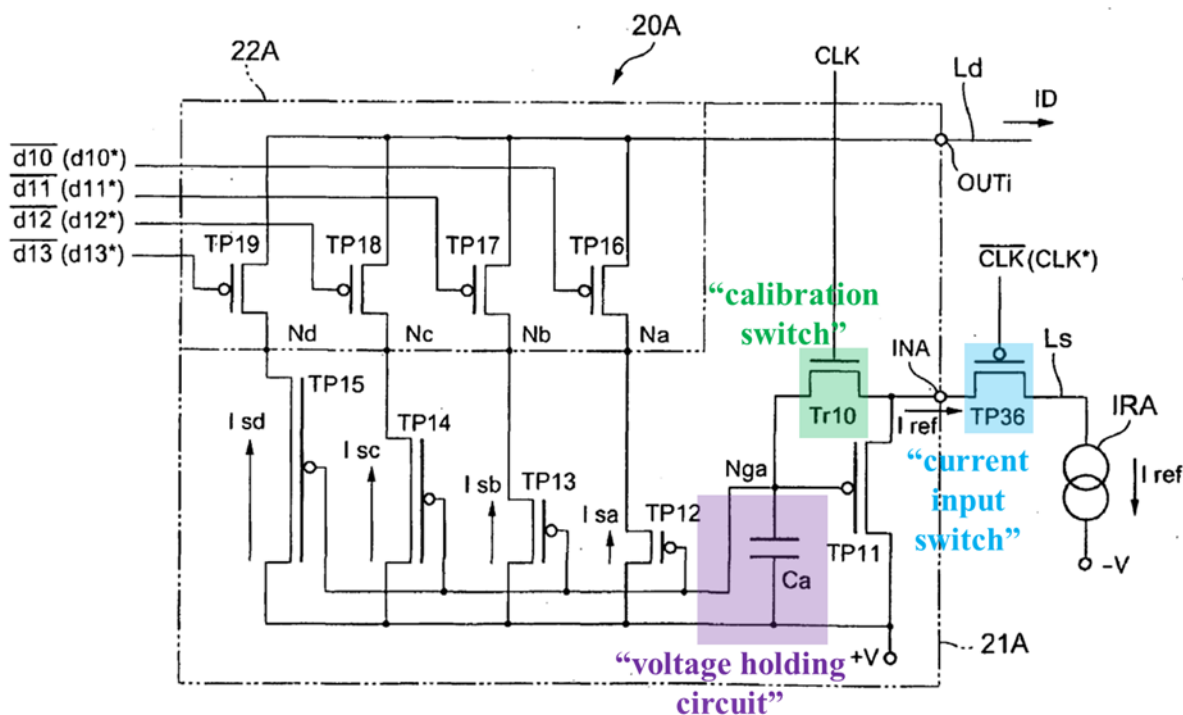
iv. 10(c): “a calibration switch interposed between said current input switch and said voltage holding circuit;”

190. This limitation is disclosed and at minimum rendered obvious by Sasaki.

191. Sasaki discloses a calibration switch (*e.g.*, “refresh control transistor Tr10”) interposed between said current input switch (*see* 10(a)) and said voltage holding circuit (*see* 10(b)). Sasaki at [0077], Figure 3.

192. See my discussion of elements 10(a)-10(b) above (Sections XI.D.b.ii-iii).

FIG. 3



Sasaki at Figure 3 (annotated).

193. For example, Sasaki discloses a “refresh control transistor Tr10” that, when “perform[ing] an ‘ON’ operation,” causes “the reference current Iref [to] flow[.]” and “charge” capacitor Ca. Sasaki at [0077].⁸ As illustrated in Figure 3, the refresh control transistor Tr10 is interposed between the current supply source control transistor TP36 and capacitor Ca.

194. Alternatively, Sasaki discloses a calibration switch (e.g., “reference current transistor TP11”) interposed between said current input switch (see 10(a)) and said voltage holding circuit (see 10(b)). Sasaki at [0063], [0077], Figure 3.

195. See my discussion of elements 10(a)-10(b) above (Sections XI.D.b.ii-iii).

⁸ This is consistent with the '047 Patent, which describes that “[c]alibration” means to have a reference current value by a reference current source stored in the current output part.” ’047 Patent at 1:37-39.

reference current transistor TP11 is a switch, as transistors were well understood to be switching devices. As illustrated in Figure 3, the reference current transistor TP11 is interposed between the current supply source control transistor TP36 and capacitor Ca, as the drain of the reference current transistor TP11 is connected to the same node as transistor TP36 and the gate of transistor TP11 is connected to the same node as capacitor Ca.

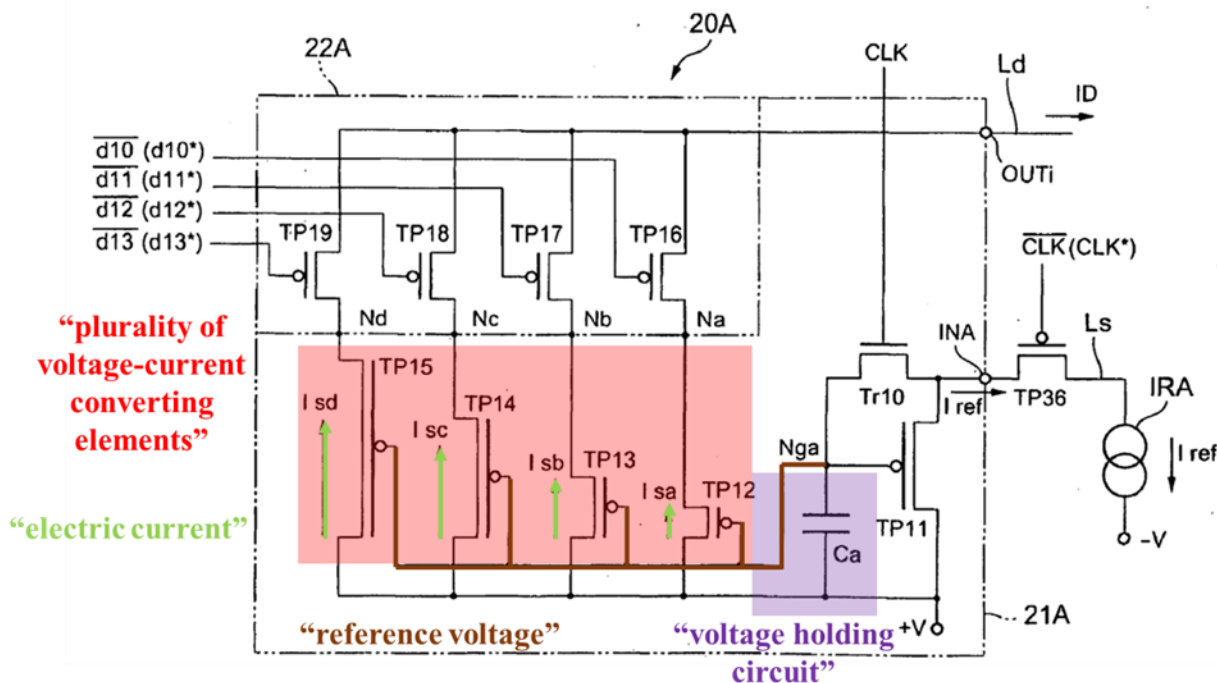
v. 10(d): “a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding circuit;”

197. This limitation is disclosed and at minimum rendered obvious by Sasaki.

198. Sasaki discloses a plurality of voltage-current converting elements (*e.g.*, “a plurality of module current transistors”) for generating an electric current (*e.g.*, generating “currents $I_{sa} \sim I_{sd}$ ”) in accordance with said reference voltage held in said voltage holding circuit (*e.g.*, voltage stored on Ca “relative to the constant reference current I_{ref} ”). Sasaki at [0015], [0063], [0066]-[0068], Figure 3.

199. See my discussion of element 10(b) above (Section XI.D.b.iii).

FIG. 3



Sasaki at Figure 3 (annotated).

200. For example, Sasaki discloses “a plurality of module current transistors” (TP12-TP15 annotated red) that have their gates “connected in common to the contact Nga” (annotated brown) and their drains connected to “the high electric potential +V.” Sasaki at [0015], [0063]. When voltage is stored in capacitor Ca (annotated purple), as discussed in 10(b), the module current transistors are turned on and generate “module currents I_{sa} ~ I_{sd} ... relative to the constant reference current I_{ref} ” such that they generate an electric current based on the reference voltage stored in capacitor Ca, thereby converting voltage to current. Sasaki at [0066]-[0068]¹⁰.

¹⁰ This is consistent with the '047 Patent, which discloses “a voltage-current converting function is actuated” when “[a] gate voltage according to the electric charges accumulated in the voltage holding capacitance element C1 is applied to the gates of the Nch transistors QN1-QNm” such that “it is possible to output a sink current having a current value proportional to the reference current.” '047 Patent at 8:17-49.

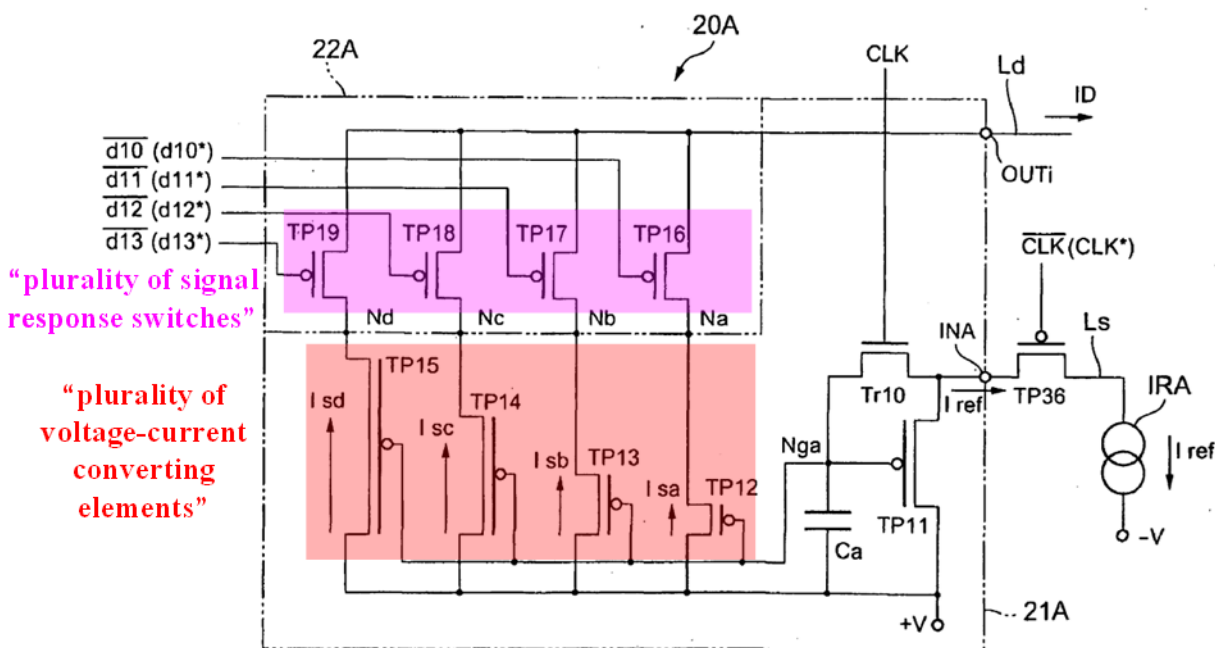
vi. 10(e): “a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being connected in series to a corresponding one of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;”

201. This limitation is disclosed and at minimum rendered obvious by Sasaki.

202. Sasaki discloses a plurality of signal response switches (*e.g.*, “switching transistors TP16~TP19”) that are on/off controlled in accordance with inputted signals (*e.g.*, turn “ON” or “OFF” according to “signals d10*~d13*”), each of said response switches being connected in series to a corresponding one of said voltage-current converting elements (*e.g.*, each “switching transistor[]” in series to a “module current transistor[]”), and each of which being connected in parallel to said calibration switch (*e.g.*, each “switching transistor[]” parallel to “reference current transistor TP11”). Sasaki at [0065], [0069], [0152], Figure 3.

203. See my discussion of element 10(c) above (Section XI.D.b.iv).

FIG. 3

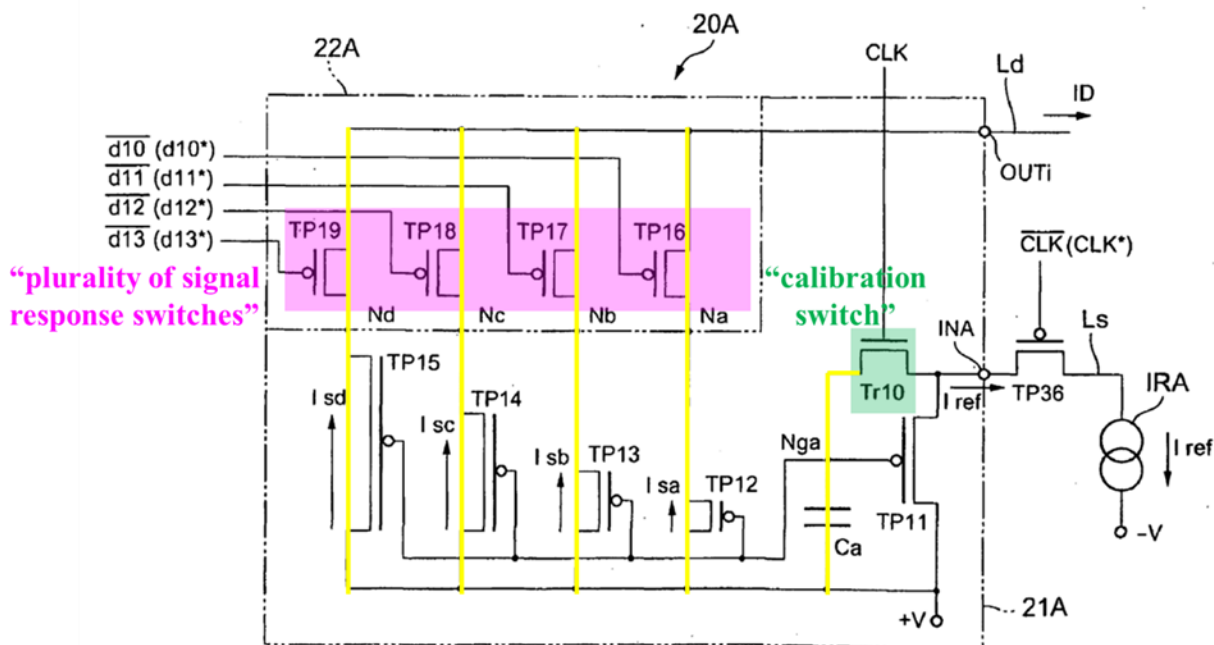


Sasaki at Figure 3 (annotated).

204. For example, Sasaki discloses “switching transistors TP16~TP19” (annotated pink) that are “connected to each of the module current transistors TP12~TP15” (annotated red) and turn “ON” or “OFF” to supply the “composite value of the[] module currents” to the loads. Sasaki at [0065], [0069]-[0070], [0152]. These switching transistors are each in series with a corresponding module current transistor. For example, transistor TP19 is connected in series to the module current transistor TP15, transistor TP18 is connected in series to module current transistor TP14, and so on.

205. Each of the switches TP16-TP19 is connected in parallel to a refresh control switch, as they share common nodes. First, the on/off states of a switching transistor do not affect the on/off states of another switching transistor. Sasaki at Figure 3. Second, each switching transistor TP16-TP19 is connected to the high electric potential through a module current transistor TP12-TP15, and Tr10 is also connected to the high electric potential +V via the capacitor Ca (see 10(c)). The other side of the switching transistors TP16-TP19 is connected to ground through the load through the OUTi node to form a complete loop for the current (as discussed further in 10(g) (Section XI.D.b.viii)). The other side of Tr10 is connected to “the low electric potential –V,” such as “the ground potential” through calibration switch TP36 and current reference IRA.

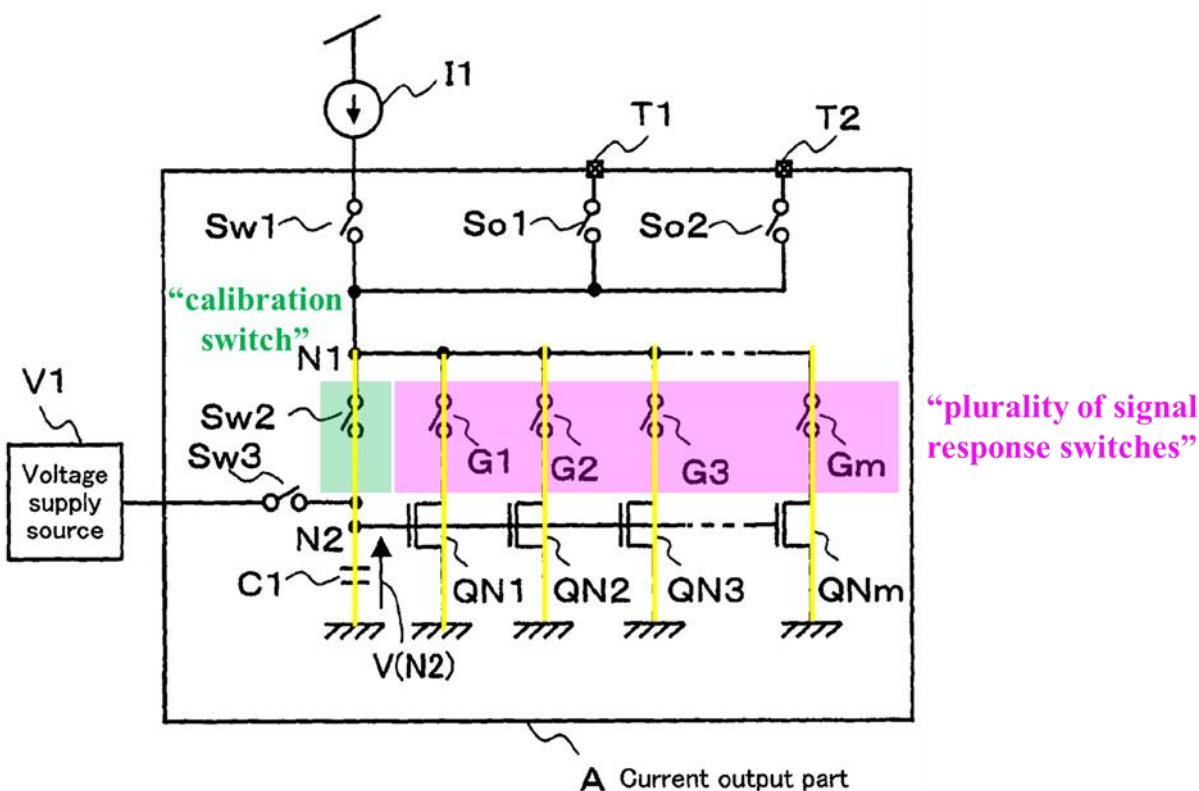
FIG. 3



Sasaki at Figure 3 (annotated).

206. This is consistent with the '047. For example, the '047 Patent describes “all the Nch transistors QN1-QNm shown in FIG. 1A are connected in parallel” because the transistors share common nodes to ground and to a node through switches G1-Gm as shown in Figure 1A. '047 Patent at 7:1-23, 11:55-12:6. Further, Figure 1A of the '047 Patent further shows switch Sw2 in “parallel” with switches G1-Gm, which share a common node and then share another common node through capacitor C1 (for switch Sw2) and transistors QN1-QNm (for switches G1-Gm).

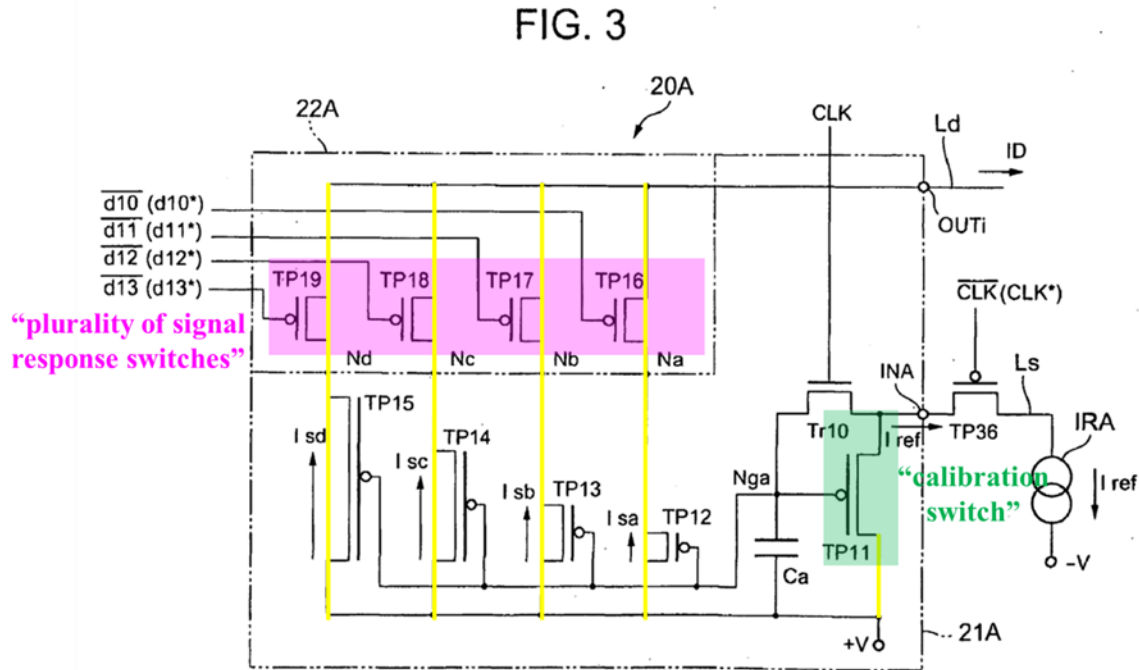
F I G. 1 A



'047 Patent at Figure 1A (annotated).

207. Alternatively, each of the switches TP16-TP19 (annotated pink) is connected in parallel to reference current transistor TP11 (annotated green), as they share common nodes. First, the on/off states of a switching transistor do not affect the on/off states of another switching transistor. Sasaki at Figure 3. Second, each switching transistor TP16-TP19 is connected to the high electric potential through a module current transistor TP12-TP15, and reference current transistor TP11 is also connected to the high electric potential +V via the capacitor Ca (see 10(c)). The other side of the switching transistors TP16-TP19 is connected to ground through the load through the OUTi node to form a complete loop for the current (as discussed further in 10(g) (Section XI.D.b.viii)). The other side of reference current transistor TP11 is connected to “the low

electric potential $-V$,” such as “the ground potential” through calibration switch TP36 and current reference IRA.



Sasaki at Figure 3 (annotated).

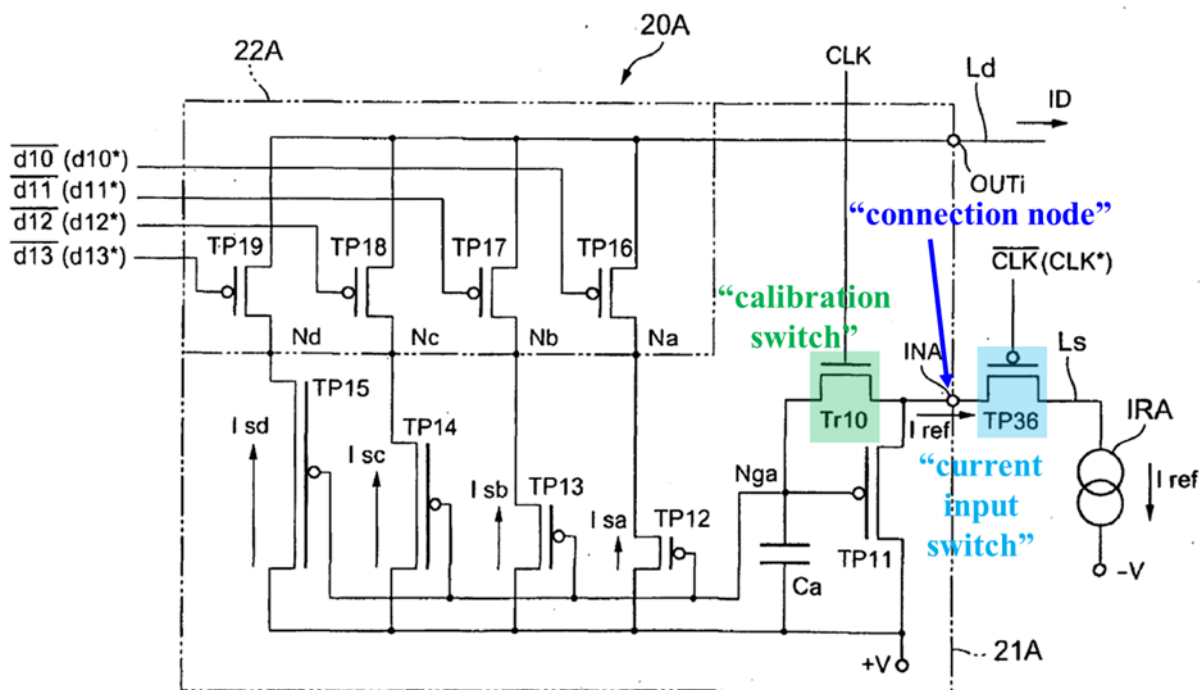
vii. 10(f): “a connection node provided between said current input switch and said calibration switch;”

208. This limitation is disclosed and at minimum rendered obvious by Sasaki.

209. Sasaki discloses a connection node (e.g., “current input contact INA”) provided between said current input switch (see 10(a)) and said calibration switch (see 10(c)). Sasaki at [0063]-[0064], [0071].

210. See my discussion of elements 10(a)-10(c) above (Sections XI.D.b.ii-iv).

Declaration of Dr. Alex Kattamis
IPR of USP 7,995,047



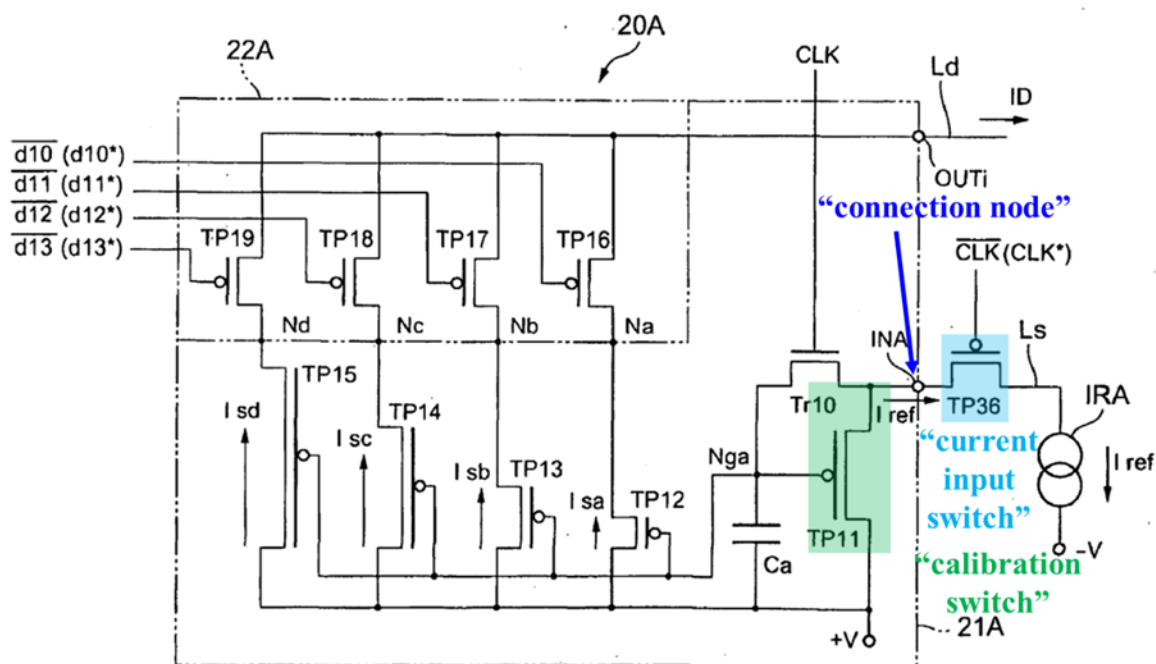
Sasaki at Figure 3 (annotated).

211. For example, Sasaki further discloses a “current input contact INA,” which is illustrated in Figure 3 to be “connected to a current supply source control transistor TP36” and the refresh control transistor Tr10. Sasaki at [0063]-[0064], [0071]. The current input contact INA is a node of a corresponding current generation section 20A, receiving a reference current I_{ref} from a corresponding reference current supplier IRA. Sasaki at [0071].

212. Alternatively, Sasaki discloses a connection node (*e.g.*, “current input contact INA”) provided between said current input switch (*see* 10(a)) and said calibration switch (*see* 10(c)). Sasaki at [0063]-[0064], [0071].

213. See my discussion of elements 10(a)-10(c) above (Sections XI.D.b.ii-iv).

FIG. 3



Sasaki at Figure 3 (annotated).

214. For example, Sasaki further discloses a “current input contact INA” (annotated blue), which is illustrated in Figure 3 to be “connected to a current supply source control transistor TP36” (annotated light blue) and the reference current transistor TP11. Sasaki at [0063]-[0064], [0071]. The current input contact INA is a node of a corresponding current generation section 20A, receiving a reference current I_{ref} from a corresponding reference current supplier IRA. Sasaki at [0071].

viii. 10(g): “a plurality of current output switches, each being interposed between the connection node and said plurality of current output terminals; and”

215. This limitation is disclosed and at minimum rendered obvious by Sasaki.

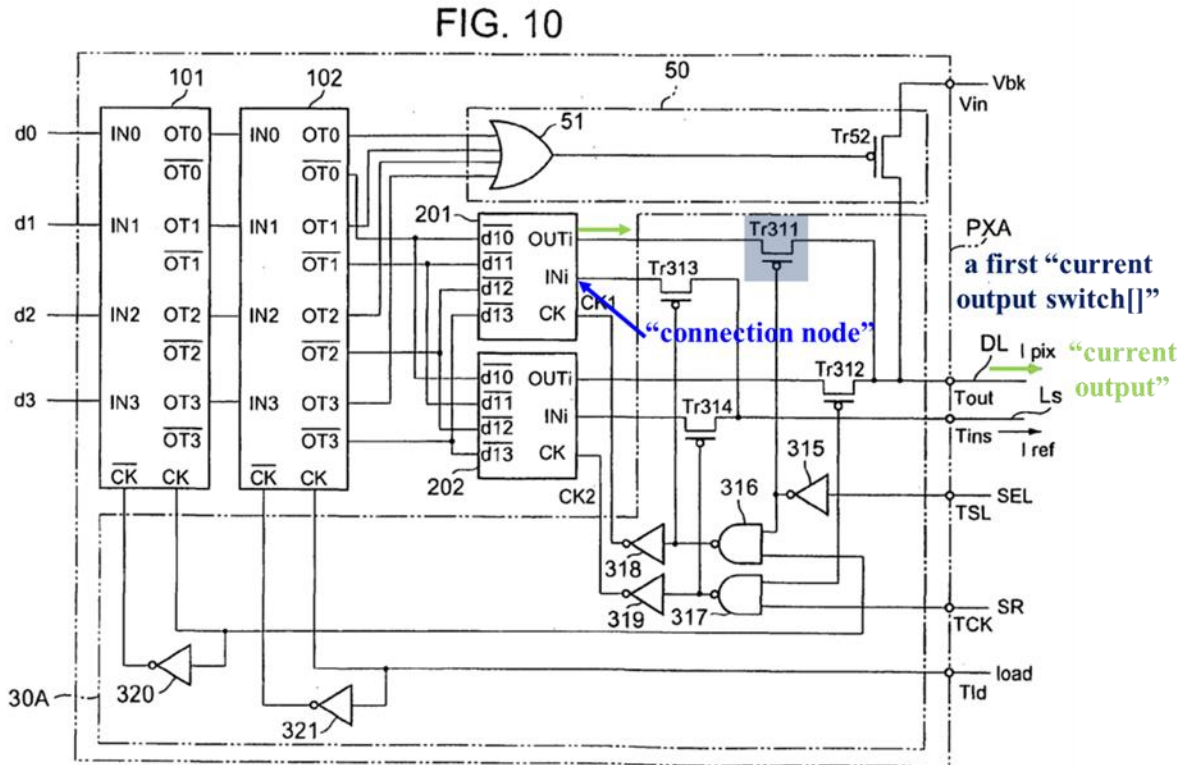
216. Sasaki discloses a plurality of current output switches (e.g., “output control transistor[] Tr311” and “Pch FET Tr42”), each being interposed between the connection node (e.g., “INi”) and said plurality of current output terminals (e.g., “contact Nxa” connected to “Pch FET

Tr42”).¹¹ Sasaki at [0063]-[0065], [0069], [0071], [0102], [0113]-[0117], [0124], [0127], [0130]-[0131], [0135], [0142], [0152], Figures 7, 8, 10.

217. See my discussion of element 10(f) above (Section XI.D.b.vii).

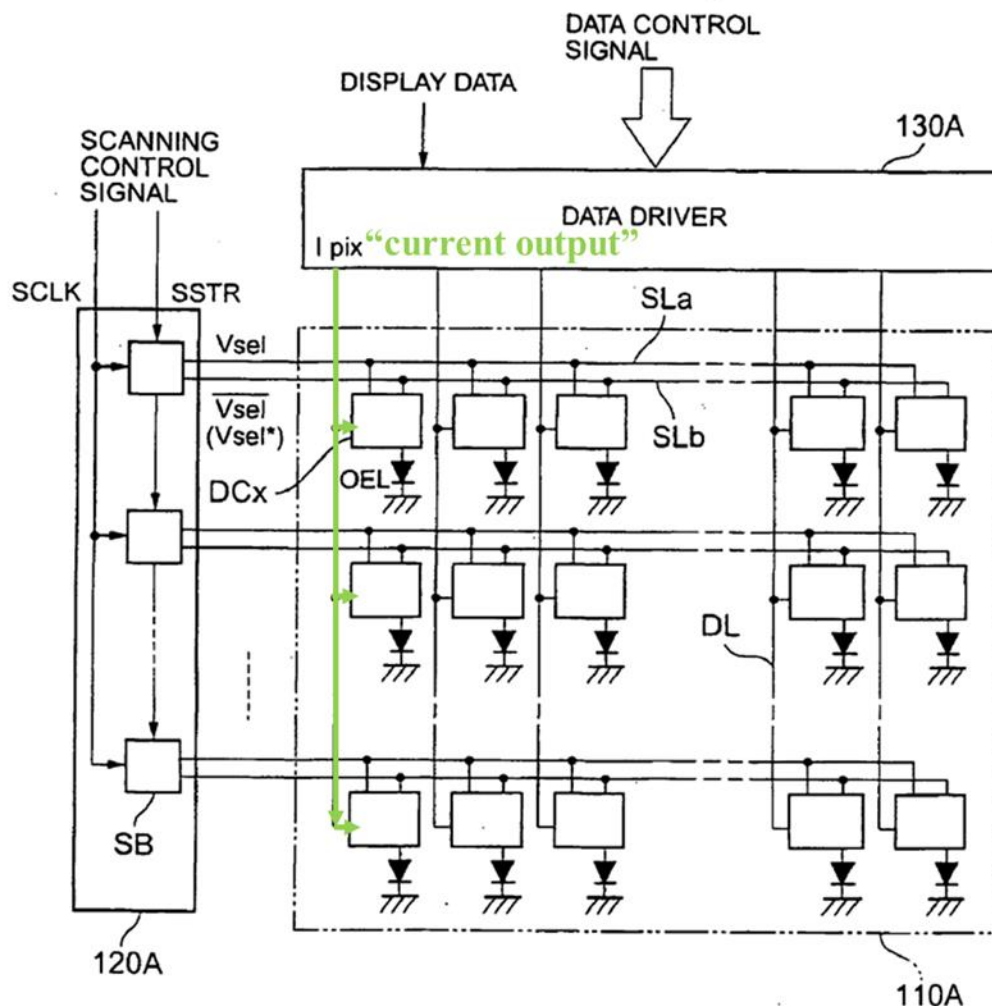
218. For example, Sasaki further discloses that a “gradation current generation section 201” that “ha[s] an equivalent configuration to the current generation section 20A” discussed above in 10(pre)-10(f). Sasaki at [0127]. The current generation section 201 includes an INi connection node (annotated blue), as discussed in 10(f), connected to a “constant current generation source.” Sasaki at [0063]-[0064], [0071]. The current generation section 201 includes a contact OUTi, which supplies the “composite value of the[] module currents” (annotated green) from switching transistors TP16~TP19 to the loads as discussed in 10(e). Sasaki at [0065], [0069], [0152]. The OUTi contact of the current generation section 201 is connected to an “output control transistor[] Tr311” (annotated dark blue) that outputs current Ipix (annotated green), which is “equivalent to the drive current supply line Ld”—i.e., the “composite value of the[] module currents” from switching transistors TP16~TP19 as discussed in 10(e). Sasaki at [0069], [0124], [0130], [0135], [0142].

¹¹ Claim 10 recites “said plurality of current output terminals,” but lacks antecedent basis as the term “plurality of current output terminals” is not previously used in claim 10. Solely for this petition, Petitioner assumes the term refers to a plurality of current output terminals.



Sasaki at Figure 10 (annotated).

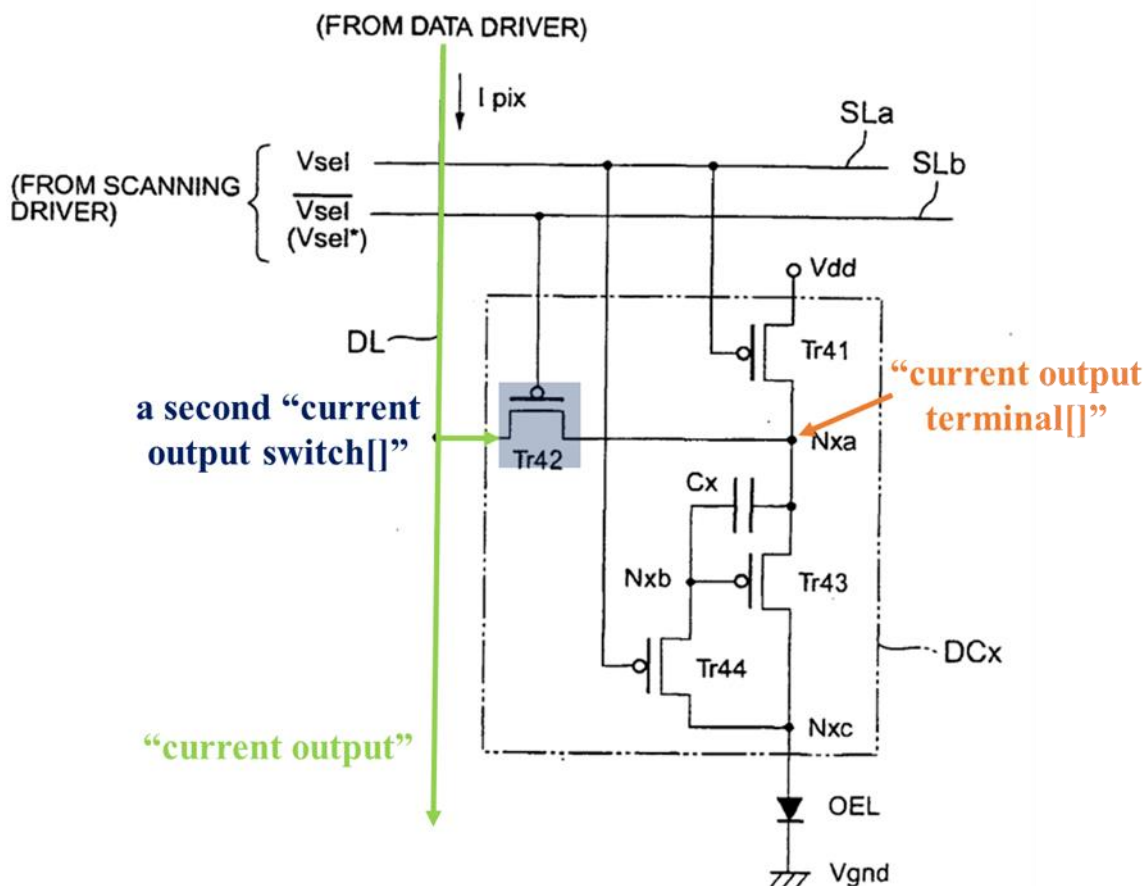
219. Output current I_{pix} (annotated green) flows through output control transistor Tr311 (annotated dark blue) and into “pixel driver circuits DCx” via a data line DL to “control the write-in of the gradation currents I_{pix} in each of the display pixels.” Sasaki at [0102], [0113]-[0117], [0130]-[0131].



Sasaki at Figure 7 (annotated).

220. Each pixel driver circuit DCx includes a “Pch FET Tr42” (annotated dark blue) connected to the data line DL that is turned “ON” to supply the current I_{pix} (annotated green) to the “light emitting device[]” via “contact Nxa” (annotated orange). Sasaki at [0113], [0116].

FIG. 8



Sasaki at Figure 8 (annotated).

221. Therefore, “output control transistor[] Tr311” and “Pch FET Tr42” (annotated dark blue) each receive the output current I_{pix} and are interposed between “contact Nxa” (annotated orange) and the IN_i connection node (annotated blue) in the current generation section 201. As discussed in this limitation 10(g), the transistors Tr311 and Tr42 (annotated dark blue) are interposed between “contact Nxa” (annotated orange) and the OUT_i contact of the current generation section 201. In addition, the OUT_i contact of the current generation section 201 is connected to “current input contact INA ” (see 10(f), and equivalent to terminal IN_i of the current generation section 201). For example, these contacts are connected via the switching transistors

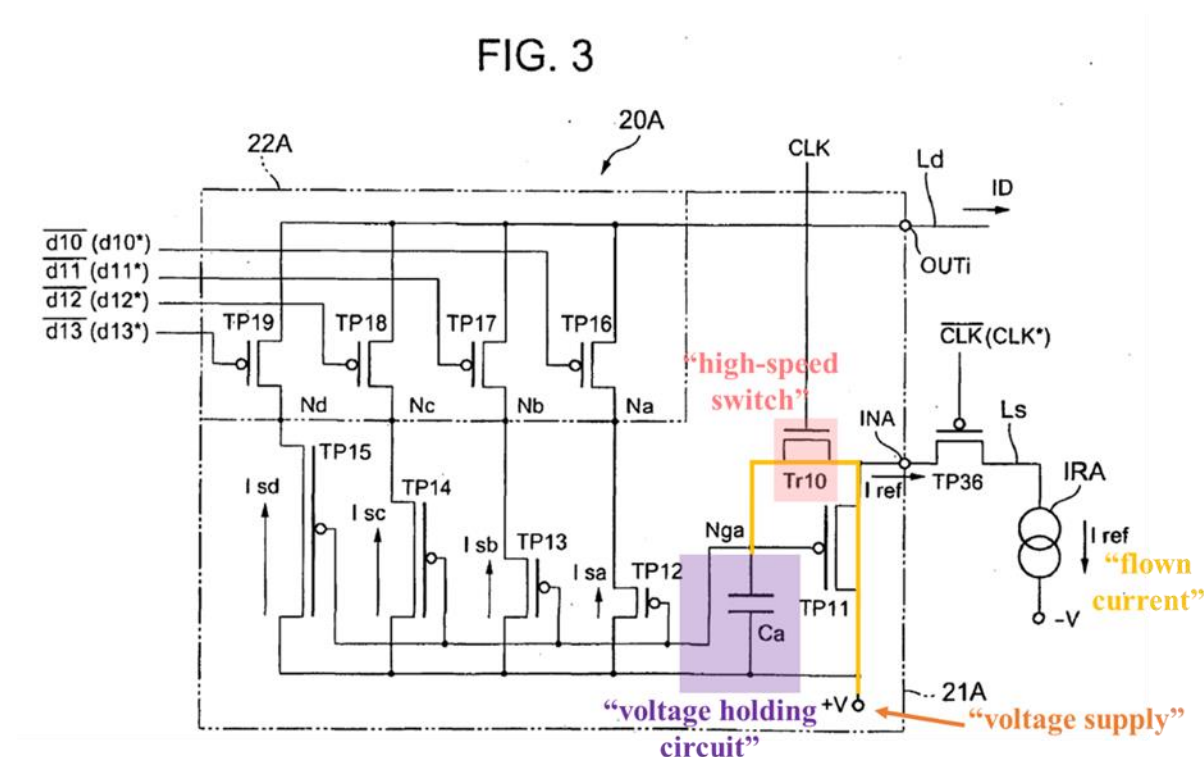
The diagram illustrates a current source circuit 20A. It features a plurality of signal response switches (TP16, TP17, TP18, TP19) and a plurality of voltage-current converting elements (TP12, TP13, TP14, TP15). The circuit is connected to a current source 21A and a current mirror 22A. A connection node is indicated by a blue arrow. The circuit includes a current source 21A, a current mirror 22A, and a connection node. The diagram is annotated with labels like d10, d11, d12, d13, CLK, Ld, ID, OUTi, CLK(CLK*), Ls, IRA, I ref, -V, +Vo, and 21A.

ix. 10(h): “a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit”

223. Sasaki discloses a high-speed switch (*e.g.*, “refresh control transistor Tr10”) for controlling connection/disconnection states (*e.g.*, “ON/OFF” states) of said voltage supply source (*e.g.*, “high electric potential +V”) with respect to the second terminal of said voltage holding

circuit (e.g., “high electric potential +V” with respect to capacitor Ca via transistor Tr10 and “reference current transistor TP11”).¹² Sasaki at [0063].

224. See my discussion of element 10(b) above (Section XI.D.b.iii).



Sasaki at Figure 3 (annotated).

225. For example, Sasaki discloses “a reference current transistor TP11” with its gate connected to capacitor Ca (contact Nga) and its source connected to “high electric potential +V.” Sasaki at [0063]. The “refresh control transistor Tr10” (annotated light red) performs a “switch ‘ON/OFF’ operation” so that a “path is connected between the contact Nga,” which is a second terminal of the capacitor Ca as discussed in 10(b), and the “high electric potential +V” through reference current transistor TP11. Sasaki at [0063]. A person of ordinary skill in the art would

¹² Claim 10 recites “said voltage supply source,” but lacks antecedent basis as the term “voltage supply source” is not previously used in claim 10. Solely for this petition, Petitioner assumes the term refers to “a fixed voltage,” which is recited earlier in the claim.

have understood that transistor Tr10 is a high-speed switch because it can be turned on and off within the timespan of a single frame. A person of ordinary skill in the art would have further understood a high electric potential +V to be an example of a voltage supply source such that when transistor Tr10 is in an “ON” state, the voltage supply source +V is connected with respect to the contact Nga connected to capacitor Ca.

226. To the extent it is argued that the high-speed switch must be different from the calibration switch, Sasaki further discloses reference current transistor TP11 that, when used in combination with refresh control transistor Tr10, connect a path between “contact Nga” and the “high electric potential +V” such that, when “refresh control transistor Tr10” is turned “ON,” the voltage supply source +V is connected with respect to the contact Nga. Sasaki at [0063].

XII. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS REGARDING THE CHALLENGED PATENT

227. During prosecution of the Challenged Patent, the applicants did not discuss any secondary considerations of non-obviousness, and I am not aware of any secondary considerations that would support non-obviousness. Indeed, per my discussion of the prior art referenced herein, any purported solutions to problems or unexpected results in the '047 Patent were already well known. Should the Patent Owner put forth any alleged evidence of secondary considerations in connection with the Challenged Patent, I reserve the right to consider such evidence, to consider whether any such evidence has a nexus to any claims of the Challenged Patent, and to update my analysis.

XIII. CONCLUSION

228. In summary, I have concluded that the Challenged Claims are rendered obvious over the prior art references as discussed above. Specifically, in my opinion, for at least the reasons above, the Challenged Claims of the '047 Patent are disclosed and rendered obvious as follows.

Ground	Claims	Prior Art References
1-2	1-4 and 9	Baek
3	5-6	Baek in view of Date
4	7-8	Baek in view of Inomoto
5	10	Sasaki

229. To the extent it is argued that any further disclosure is required for an element in the Challenged Claims that I have identified as being disclosed, a person of ordinary skill in the art would certainly have found that element obvious to include based on the sample explicit disclosure or inherent disclosures and analysis I have identified above.

230. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner or its expert(s) may raise and to take into account new information as it becomes available to me.

231. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

232. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner or its expert(s) may raise and to take into account new information as it becomes available to me.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on July 25, 2025 in New York, NY.

Respectfully submitted,



Alex Z. Kattamis, Ph.D., P.E.

APPENDIX A



Engineering & Scientific Consulting

Alex Kattamis, Ph.D., P.E, CFEI, CVFI

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Professional Profile

Dr. Kattamis is an electrical engineer with an extensive background in failure analysis and forensic engineering. He performs root cause analyses (RCA) relating to failures and fires in electrical systems ranging from semiconductor devices and consumer electronics to power generation, transmission and distribution equipment.

Dr. Kattamis has also led large-scale condition assessments of mechanical, electrical, and plumbing (MEP) systems following natural disasters. He has an in depth knowledge of relevant electrical codes and standards including those of the IEC, IEEE, NEC, NESC, NFPA, OSHA, and UL.

Dr. Kattamis has expertise in the design, fabrication, and failure analysis of semiconductor devices including thin-film electronics, flexible electronics, memories, LEDs, LCDs, AMOLEDs, integrated circuits, and printed circuit boards. Dr. Kattamis is also has experience in investigating and providing testimony in intellectual property matters.

Dr. Kattamis received his Ph.D. in Electrical Engineering at Princeton University. His research focused on large-area flexible electronics including the design, fabrication and characterization of TFT display backplanes for electrophoretic displays and AMOLEDs on metal foils and polymer substrates. This included significant work in thin-film mechanics. His fabrication experience includes plasma-enhanced chemical vapor deposition, reactive-ion etching, sputter deposition, wet chemical processing, and photolithography.

Prior to his Ph.D., Dr. Kattamis worked at General Electric Industrial Systems, where he designed and implemented electronic trip units and current sensing systems for metering and switchgear. This included analog electronics design, modeling, and firmware coding.

Academic Credentials & Professional Honors

Ph.D., Electrical Engineering, Princeton University, 2007

M.A., Electrical Engineering, Princeton University, 2004

B.S.E., Electrical Engineering, University of Connecticut, 2002

Princeton Plasma Physics Fellowship Recipient

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Citigroup Scholarship Recipient

Licenses and Certifications

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Professional Engineer, Pennsylvania, #PE090289

Professional Engineer Electrical, Rhode Island, #PE.0013344

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Certified Fire and Explosion Investigator (CFEI)

Certified Vehicle Fire Investigator (CVFI)

Prior Experience

Research Assistant; Princeton University (2002-2007)

Design Engineer; General Electric Industrial Systems (Summer 2001, 2002)

Professional Affiliations

Institute of Electrical and Electronic Engineers (member)

Society for Information Display (member)

Materials Research Society (member)

Languages

French

Greek

Publications

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Kattamis AZ, Holmes RJ, Cheng I-C, Long K, Forrest SR, Sturm JC, Wagner S. Nanocrystalline silicon TFTs on Clear Plastic Foil for Flexible OLED Displays. 21st International Conference on Amorphous and Nanocrystalline Semiconductors, 2005.

Kattamis AZ, Cheng I-C, Long K, Sturm JC, Wagner S. Dimensionally stable processing of a-Si TFTs on polymer substrates. Electronic Materials Conference, 2005.

Kattamis AZ, Cheng I-C, Sturm JC, Wagner S. Nanocrystalline silicon thin film transistors on optically clear polymer foil substrates. Materials Research Society Spring Meeting, 2005.

Kattamis AZ, Cheng I-C, Allen S, Wagner S. Hydrogen in ultralow temperature SiO₂ for nanocrystalline silicon thin film transistors. Materials Research Society Spring Meeting, 2004.

Presentations

Kattamis A, Murphy PF, Cotts B. Impacts of Extreme Weather Events on Renewable Energy Generation. Webinar. March 24, 2021.

Cotts B, Kattamis A, Murphy PF. Alternative Energy Liability Claims for Solar Installations Large & Small. Webinar. November 11, 2020.

Kattamis AZ, Widin DR. Power interruption. HarrisMartin: Superstorm Sandy Insurance Coverage Litigation Conference, Borgata Hotel, Atlantic City, NJ, June 26, 2013.

Troisi MA, Kattamis AZ. Power Interruption Coverage and Electrical Engineering Issues - Discussion of the Wakefern Case. HarrisMartin: Superstorm Sandy Insurance Coverage Litigation Conference, InterContinental, New York Barclay, New York, NY, February 26, 2013.

Kattamis AZ, Murphy PF. Innovations in backplane electronics for large-area OLEDs. IEEE Long Island Systems, Applications and Technology Conference, Technology Track, Session 3, 2012.

Project Experience

Failure Analysis

- Root cause analysis of medical device failures

- Root cause analysis of lighting device failures
- Root cause analysis of failures in power strips used in data centers
- Hazard analysis for lighting devices
- Root cause analysis for motor run capacitor failures

Flexible Electronic Circuits

- Flexible aluminum substrate characterization
- Amorphous silicon thin-film transistor deposition
- Aluminum substrate passivation and coating for thin-film processing

Hard Disk Drives

- Patent and trade secret investigations relating to hard disk drive intellectual property
- Infringement analysis of accused hard disk drives products
- Prior art and validity analysis of patents related to hard disk drive patents

Light Emitting Devices

- Patent investigations relating to LED and laser diode intellectual property
- Reverse engineering focusing on device processing and characterization
- Infringement analysis of accused LEDs and laser diodes
- Prior art and validity analysis of patents related LEDs and laser diodes

Semiconductor Devices and Materials

- Patent investigations relating to semiconductor devices
- Reverse engineering focusing on packaging, processing and design of memories and other semiconductor devices
- Infringement analysis of accused memories and other semiconductor devices
- Prior art and validity analysis of patents related to memories and other semiconductor devices

Image Processing Software

- Reverse engineering focusing on image processing software and algorithms
- Infringement analysis of accused image processing products
- Prior art and validity analysis of patents related to image processing patents

Computer Networks

- Reverse engineering focusing on computer networks, including networks for providing financial services
- Infringement analysis of accused computer networking products

Fire Investigations

- Cause and origin of fires relating to wiring, electrical equipment and consumer electronics

CONTINUING EDUCATION (CFEI)

IAAI, "Explosion Dynamics, cfitrainer.net, July 31, 2015

IAAI, "The Practical Application of the Relationship Between NFPA 1033 and NFPA 921, cfitrainer.net, July 31, 2015

IAAI, "Electrical Safety, cfitrainer.net, August 12, 2015

IAAI, "The Potential Value of Electronic Evidence in Fire Investigations," cfitrainer.net, August 17, 2015

IAAI, "Investigating Natural Gas Systems, cfitrainer.net, August 17, 2015

IAAI, "NFPA 921 and 1033 2014 Editions: Important Revisions," cfitrainer.net, August 17, 2015

IAAI, "Fundamentals of Residential Building Construction, cfitrainer.net, August 17, 2015

IAFI, "Fire Chemistry," i-a-fi.org/, August 18, 2015

IAFI, "Hazard and Risk Assessment," i-a-fi.org/, August 18, 2015

IAFI, "The Ten Most Common Fire Scene Errors by Patrick M. Kennedy," i-a-fi.org/, August 18, 2015

IAFI, "Personal Protective Equipment," i-a-fi.org/, August 18, 2015

IAFI, "Better Report Writing for Fire Investigators," i-a-fi.org/, August 18, 2015

IAFI, "Introduction to Fire Investigator Scene Safety," i-a-fi.org/, August 18, 2015

IAAI, "A Ventilation-Focused Approach to the Impact of Building Structures and Systems on Fire," cfitrainer.net, August 25, 2015

IAAI, "Investigating Motor Vehicle Fires," cfitrainer.net, September 11, 2019

IAAI, "Motor Vehicles: Transmission, Exhaust, Brake, and Accessory Systems," cfitrainer.net, September 11, 2019

IAAI, "Motor Vehicles: The Engine and the Ignition, Electrical, and Fuel Systems," cfitrainer.net, September 11, 2019

NAFI, "Vehicle Fire Investigation Training Program," Lexington, Kentucky, September 16 – 19, 2019

IAAI, "Electric & Hybrid Vehicle Fires," cfitrainer.net, January 18, 2022



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Testimony History

Innolux Corporation v. Semiconductor Energy Laboratory Co., Ltd., in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2013-00064/65, 2013

Maxell, Ltd., et al., v. Huawei Device USA Inc., and Huawei Device Co., Ltd., in the United States District Court Eastern District of Texas, Case No. 5:17-cv-00033, 2019

Henry Buseti, et al., v Alltrade Tools, LLC and Costco Wholesale Corporation d/b/a Costco, in the State of Vermont, Civil Docket No. 13-1-18 Lecv, 2020

Zachry Industrial, Inc., v Three Phase Line Construction, Inc., in the United States District Court Southern District of Texas Houston Division, Civil Action No. 4:17-cv-3751, 2020

TrickleStar Inc. v AM Conservation Group, Inc., in the United States District Court Northern District of Illinois, Case No. 1:20-cv-06667, 2021

United States of America Ex. rel. Jay Gallo and Greg Quinn v. Thor Guard, Inc., in the United States District Court for the Middle District of Florida Jacksonville Division, Case No. 3:18-cv-811-J-32MCR, 2021

AZZ, Inc. et al., v. Southern Nuclear Operating Company, Inc. et al., in the United States District Court for the Southern District of Georgia Augusta Division, Civil Action No. 1:19-CV-052, 2021

The NOCO Company, Inc., v. Pilot, Inc., in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2021-00777/65, 2021

Cisco Systems, Inc., v. Wilson Chung et al., in the United States District Court for the Northern District Of California Oakland, Case No. 4:19-CV-07562-PJH, 2022.

Mohamad El-Hajj et al., v. Travelers Insurance Company et al., in the Court of Queen's Bench of Alberta, Edmonton, Court File No. 1403 08357, 2023.



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Samsung Electronics America Inc et al. v. Polaris Powerled Technologies LLC, in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2023-00771, January 2024

Samsung Electronics America Inc et al. v. Polaris Powerled Technologies LLC, in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2023-00771, June 2024

Samsung Display Co., LTD, v. Pictiva Displays International LTD, in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2024-01187, May, 2025

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Testimony History

Innolux Corporation v. Semiconductor Energy Laboratory Co., Ltd., in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2013-00064/65, 2013

Maxell, Ltd., et al., v. Huawei Device USA Inc., and Huawei Device Co., Ltd., in the United States District Court Eastern District of Texas, Case No. 5:17-cv-00033, 2019

Henry Buseti, et al., v Alltrade Tools, LLC and Costco Wholesale Corporation d/b/a Costco, in the State of Vermont, Civil Docket No. 13-1-18 Lecv, 2020

Zachry Industrial, Inc., v Three Phase Line Construction, Inc., in the United States District Court Southern District of Texas Houston Division, Civil Action No. 4:17-cv-3751, 2020

TrickleStar Inc. v AM Conservation Group, Inc., in the United States District Court Northern District of Illinois, Case No. 1:20-cv-06667, 2021

United States of America Ex. rel. Jay Gallo and Greg Quinn v. Thor Guard, Inc., in the United States District Court for the Middle District of Florida Jacksonville Division, Case No. 3:18-cv-811-J-32MCR, 2021

AZZ, Inc. et al., v. Southern Nuclear Operating Company, Inc. et al., in the United States District Court for the Southern District of Georgia Augusta Division, Civil Action No. 1:19-CV-052, 2021

The NOCO Company, Inc., v. Pilot, Inc., in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2021-00777/65, 2021

Cisco Systems, Inc., v. Wilson Chung et al., in the United States District Court for the Northern District Of California Oakland, Case No. 4:19-CV-07562-PJH, 2022.

Mohamad El-Hajj et al., v. Travelers Insurance Company et al., in the Court of Queen's Bench of Alberta, Edmonton, Court File No. 1403 08357, 2023.



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Samsung Electronics America Inc et al. v. Polaris Powerled Technologies LLC, in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2023-00771, June 2024

Samsung Display Co., LTD, v. Pictiva Displays International LTD, in the United States Patent and Trademark Office before the Patent and Trial Board, Case No. IPR2024-01187, May, 2025