UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.

Petitioner

v.

BISHOP DISPLAY TECH LLC

Patent Owner

Case No. IPR2022-00501
Patent No. 7,995,047

PETITION FOR *INTER PARTES* REVIEW

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PETITIONER'S LIST OF EXHIBITS

Ex.	Description of Documents
1001	U.S. Patent No. 7,995,047 to Makoto Mizuki et al., entitled "Current Driving Device" (filed December 12, 2007 and issued August 9, 2011) **("'047 Patent" or "Challenged Patent")**
1002	Declaration of Dr. Alex Kattamis in Support of Petition for *Inter Partes* Review of U.S. Patent No. 7,995,047, with CV attached as Appendix A **("Kattamis Decl.")**
1003	File History of U.S Patent No. 7,995,047 (App. No. 11/954,659) **("'047 Patent File History")**
1004	M. Shimoda, K. Abe, H. Haga, H. Asada, H. Hayama, K, Iguchi, D. Iga, H. Imura, and S. Miyano, "An integrated poly-Si TFT current data driver with a data-line pre-charge function," *Journal of the Society for Information Display* **11/3** (2003): 461-466 **("Shimoda")**
1005	U.S. Patent Publication No. 2006/0170629 to Jong-Hak Baek, entitled "Display Driver Circuit, Current Sample/Hold Circuit and Display Driving Method Using the Display Driver Circuit" (filed January 27, 2006 and published August 3, 2006) **("Baek")**
1006	U.S. Patent Publication No. 2005/0017765 to Kazuhiro Sasaki and Katsuhiko Morosawa, entitled ""Current Generation Supply Circuit and Display Device" (filed July 14, 2004 and published January 27, 2005 **("Sasaki")**
1007	John A. Camara, ELECTRICAL ENGINEERING REFERENCE MANUAL FOR THE ELECTRICAL AND COMPUTER PE EXAM, 6th ed. (Professional Publications, Inc.: 2002), ISBN: 1-888577-56-8 **("Camara")**
1008	Willem den Boer, ACTIVE MATRIX LIQUID CRYSTAL DISPLAYS, 1st ed. (Newnes: 2005), ISBN: 0-750678-13-5 **("den Boer")**
1009	M.K. Han, "AM backplane for AMOLED," *Proc. Of ASID* **6** (Oct. 8-12, 2006): 53-58 **("Han")**

Ex.	Description of Documents
1010	B. Hekmatshoar, A. Kattamis et al., "A Novel TFT-OLED integration for OLED-independent pixel programming in amorphous-Si AMOLED pixels," *Journal of the Society for Information Display* **16/1** (2008): 183-188.
1011	A. Kattamis et al., "Active-matrix organic light-emitting displays employing two thin-film-transistor a-Si:H pixels on flexible stainless-steel foil," *Journal of the Society for Information Display* **15/7** (2007): 433-437.
1012	About the SID (dated June 16, 2004), available at: https://web.archive.org/web/20040616180753/http://www.sid.org/about/about.html
1013-1018	RESERVED
1019	Declaration of Dr. James L. Mullins sponsoring Exhibit 1004 and Exhibits 1020-1027 **("Mullins Decl.")**
1020	Copy of Shimoda owned by the Linda Hall Library
1021	Copy of Shimoda owned by the United States Library of Congress
1022	WorldCat entry for Journal of the Society for Information Display (Missouri)
1023	WorldCat entry for Journal of the Society for Information Display (Washington, DC)
1024	OPAC record from Linda Hall Library for Journal of the Society for Information Display
1025	OPAC record from United States Library of Congress for Journal of the Society for Information Display
1026	J.L. Sanford and F.R. Libsch, "V_t compensated voltage-data a-Si TFT AMOLED pixel circuits," *Journal of the Society for Information Display* **11/1** (2004): 65-73 **("Sanford")**

Ex.	Description of Documents
1027	Y.-S. Son, S.-K. Kim, Y.-J. Jeon et al., "P-40: A Novel Data Driving Method and Circuits for AMOLED Displays," *SID Symposium Digest of Technical Papers* **37** (2006): 343-346 **("Son")**
1028	Amended Complaint, *Bishop Display Tech LLC v. Samsung Electronics Co., LTD.* et al., 2:21-cv-00136-JRG, Dkt. No. 2 (E.D. Tex., Apr. 20, 2021)
1029	Complaint, *Bishop Display Tech LLC v. Samsung Electronics Co., LTD.* et al., 2:21-cv-00139-JRG, Dkt. No. 1 (E.D. Tex., Apr. 20, 2021)
1030	Docket Control Order, *Bishop Display Tech LLC v. Samsung Electronics Co., LTD.* et al., 2:21-cv-00136-JRG, Dkt. No. 55 (E.D. Tex., Nov. 19, 2021)
1031	Docket Control Order, *Bishop Display Tech LLC v. Samsung Electronics Co., LTD.* et al., 2:21-cv-00139-JRG, Dkt. No. 60 (E.D. Tex., Nov. 19, 2021)
1032	Joint Motion for Entry of Partially Disputed Docket Control Order, *Bishop Display Tech LLC v. Samsung Electronics Co., LTD. et al.*, 2:21-cv-00136-JRG, Dkt. No. 51 (E.D. Tex., Oct. 27, 2021)
1033	Joint Motion for Entry of Partially Disputed Docket Control Order, *Bishop Display Tech LLC v. Samsung Electronics Co., LTD. et al.*, 2:21-cv-00139-JRG, Dkt. No. 50 (E.D. Tex., Oct. 27, 2021)
1034	Joint Notice Regarding Consolidation, *Bishop Display Tech LLC v. Samsung Electronics Co., LTD. et al.*, 2:21-cv-00136-JRG, Dkt. No. 49 (E.D. Tex., Oct. 27, 2021)
1035	Joint Notice Regarding Consolidation, *Bishop Display Tech LLC v. Samsung Electronics Co., LTD.* et al., 2:21-cv-00139-JRG, Dkt. No. 48 (E.D. Tex., Oct. 27, 2021)
1036	PACER Calendar Events Set for 12/5/2022, U.S. District Court Eastern District of Texas, Judge Rodney Gilstrap (last accessed Jan. 27, 2022)

Ex.	Description of Documents
1037	Model Order Focusing Patent Claims and Prior Art to Reduce Costs, available at: https://www.txed.uscourts.gov/sites/default/files/forms/ModelPatentOrder.pdf
1038	*Revolaze LLC v. J.C. Penney Co., Inc.*, 2:19-CV-00043-JRG, Dkt. No. 32 (E.D. Tex., June 4, 2019)
1039	*Trioptima AB v. Quantile Techs. Ltd.*, 2:19-CV-390-JRG, Hr'g Tr. (E.D. Tex. Sept. 4, 2020) (excerpted)
1040	Cover Pleading and Appendix 1 to Plaintiff's Disclosure of Asserted Claims and Infringement Contentions, *Bishop Display Tech LLC v. Samsung Electronics Co., LTD. et al.*, 2:21-cv-00139-JRG (E.D. Tex., Sept. 19, 2021)

Other than the prosecution history, Ex. 1003, all citations to exhibits reference original page numbers found in the underlying document. Unless noted, all emphases are added.

MANDATORY NOTICES UNDER 37 C.F.R. §42.8

A. REAL PARTY-IN-INTEREST UNDER 37 C.F.R. §42.8(B)(1)

Samsung Electronics Co., Ltd. (**"Samsung"** or **"Petitioner"**) is a real-party-in-interest for this *inter partes* review ("IPR").

Petitioner also identifies the following real-parties-in-interest: Samsung Electronics America, Inc.; and Samsung Display Co., Ltd. These entities are parties to lawsuits where they have been accused of infringement by Patent Owner in:

- *Bishop Display Tech LLC v. Samsung Electrons. Co.*, No. 2:21-cv-00136-JRG (**"136 Litigation"**); and
- *Bishop Display Tech LLC v. Samsung Electrons. Co.*, No. 2:21-cv-00136-JRG, 2:21-cv-00139-JRG (E.D. Tex.) (**"139 Litigation"**) (collectively, **"Texas Litigations"**).

B. RELATED MATTERS UNDER 37 C.F.R. §42.8(B)(2)

U.S. Patent No. 7,995,047 ("**'047 Patent**" or "**Challenged Patent**") is currently asserted by Patent Owner against Petitioner in a case styled: *Bishop Display Tech LLC v. Samsung Electrons. Co., Ltd. et al.*, No. 2:21-cv-00139-JRG (E.D. Tex.) (**"139 Litigation"**). The original complaint for the 139 Litigation was originally filed April 20, 2021.

In addition, Petitioner is concurrently filing Petitions for IPR against other patents held by Patent Owner, including: IPR2022-00500 against U.S. Patent No. 6,822,706; IPR2022-00502 against U.S. Patent No. 8,016,449; and IPR2022-00503 against U.S. Patent No. 8,093,830.

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C. DESIGNATION OF COUNSEL UNDER 37 C.F.R. §42.8(B)(3)

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D. SERVICE INFORMATION UNDER 37 C.F.R. §42.8(B)(4)

A copy of the entire Petition, including all Exhibits and a Power of Attorney, is being served by FedEx, costs prepaid, to:

- the address of the attorney or agent of record for Patent Owner at the USPTO:

  McDermott Will and Emery LLP
  The McDermott Building
  500 North Capitol Street, N.W.
  Washington DC 20001

- Counsel for the Texas Litigations:

  Patrick J. Conroy
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  2727 North Harwood Street
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Petitioner may be served at lead counsel's address provided above and consents to e-mail service, provided service is made to all the following e-mail addresses: eliot.williams@bakerbotts.com, neil.sirota@bakerbotts.com, david.tobin@bakerbotts.com, and DLBishopDisplaySECBB@BakerBotts.com.

A Power of Attorney is filed herewith under 37 C.F.R. §42.10(b).

CLAIM LISTING

Claim Element	Claim Language from ’047 Patent
1(pre)	1. A current driving device, comprising:
1(a)	a first voltage supply source for supplying a first voltage;
1(b)	a first current supply source for supplying a first electric current;
1(c)	a plurality of output terminals; and
1(d)(1)	a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising
1(d)(2)	a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein:
1(e)	each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,
1(f)	under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit, and
1(g)	under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and
1(h)	under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit.

Claim Element	Claim Language from ’047 Patent
2	2. The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits, and each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common
3	3. The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode.
4	4. The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode.
9	9. A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device.
10(pre)	10. A current driving device, comprising:
10(a)	a current input switch for controlling connection/disconnection states with respect to a current supply source;
10(b)	a voltage holding circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;
10(c)	a calibration switch interposed between said current input switch and said voltage holding circuit;
10(d)	a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding circuit;
10(e)	a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being

Claim Element	Claim Language from ’047 Patent
	connected in series to a corresponding one of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;
10(f)	a connection node provided between said current input switch and said calibration switch;
10(g)	a plurality of current output switches, each being interposed between the connection node and said plurality of current output terminals; and
10(h)	a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit.

I. REQUIREMENTS UNDER 37 C.F.R. §42.104

A. STANDING

Petitioner certifies under 37 C.F.R. §42.104(a) that the ’047 Patent is eligible for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review on the grounds set forth herein.

B. SUMMARY OF GROUNDS

Claims 1-4, 9, and 10 **(“Challenged Claims”)** of the ’047 Patent are unpatentable as follows.

Ground	’047 Claims	Basis for Challenge
1	1-4, 9	Anticipated by Shimoda (Ex. 1004)
2	1-4, 9	Obvious over Shimoda
3	1-4, 9	Anticipated by Baek (Ex. 1005)
4	1-4, 9	Obvious over Baek
5	10	Anticipated by Sasaki (Ex. 1006)
6	10	Obvious over Sasaki

The grounds of unpatentability are supported by the declaration of Dr. Alex Kattamis. Ex. 1002, ¶16.

II. DISCRETIONARY DENIAL IS NOT WARRANTED

The Board should not exercise discretion under 35 U.S.C. §325(d), because ***none*** of the asserted references (Shimoda, Baek, or Sasaki) are cited on the cover of the ’047 Patent.

The existence of parallel proceedings in the Eastern District of Texas should not prevent institution of this Petition under 35 U.S.C. §314(a). The ’047 patent is

asserted among 13 mostly unrelated patents across two lawsuits that Patent Owner brought against Petitioner and other real parties-in-interest ("RPIs"): 7 patents in case no. 2:21-cv-00136 (Ex. 1028), and 6 patents in 2:21-cv-00139 (Ex. 1029).

Petitioner is filing IPR challenges to the majority of these 13 asserted patents. In view of Petitioner's diligence in filing this petition (and others), the uncertainty in the parallel litigation schedule, and the stipulation offered to remove any overlap of issues, the factors described in *Apple, Inc. v. Fintiv, Inc.*, IPR2020-0019, Paper 11 (PTAB March 20, 2020) (precedential) favor institution.

A. FACTOR 1: POTENTIAL FOR A STAY RENDERS THIS FACTOR NEUTRAL

Institution could relieve the district court of addressing liability of the '047 patent. This factor is at least neutral, given the "variety of circumstances and facts beyond [the Board's] control and to which [it] is not privy" relating to how the district court may rule on a stay motion. *Sand Revolution II, LLC v. Cont'l Intermodal Grp-Trucking LLC*, IPR2019-01393, Paper 24, at 7 (PTAB June 16, 2020) (informative); *see also Apple Inc., v. Parus Holdings, Inc.*, IPR2020-00686, Paper 9 at 10-11 (PTAB Sept. 23, 2020).

B. FACTOR 2: UNCERTAINTY IN LITIGATION SCHEDULE FAVORS INSTITUTION

The cases against Petitioner and RPIs are scheduled for jury selection starting December 5, 2022 across 13 asserted patents. Exs. 1030-1031. As the Board has

recognized, when "the *same trial date is set for two cases involving a total of thirteen asserted patents*, there is a possibility that the [scheduled] trial date may be moved back, at least with respect to the [challenged] patent." *HP Inc.* v. *Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (PTAB Jan. 14, 2021) (emphasis added). Here too, there is a real possibility that the trial date may move, and Factor 2 favors institution.

First, the trial date has already moved once. At Patent Owner's request, the parties jointly sought—and the district court granted—a motion to move the trial date from September 12 to December 5, 2022. Exs. 1032-1033. Thus, "it is unclear that the court in the related district court litigation will adhere to any currently scheduled jury trial date or, if it is changed, when such a trial will be held." *Sand Revolution II*, IPR2019-01393, Paper 24 at 9.

Second, Patent Owner has filed two cases against Petitioner and RPIs. Exs. 1028-1029 (complaints). Both cases are currently scheduled to begin jury selection on December 5, 2022. However, the parties did not agree to consolidation, Exs. 1034-1035, so trial of both cases cannot proceed as currently scheduled. Further, there are six *other* cases scheduled for trial on December 5. Ex. 1036. *See Apple Inc. v. Seven Networks, LLC*, IPR2020-00506, Paper 11 at 7-8 (PTAB Sept. 1, 2020) (declining to exercise discretion even though "trial is scheduled to begin … ten

months before" the final written decision, noting the number of other trials scheduled for the same day).

Third, with 13 patents asserted across the two cases, several of the patents will undoubtedly be withdrawn before trials. If Patent Owner does not voluntarily withdraw patents at a reasonable time, the district court previously has required plaintiffs to narrow their case. *See, e.g.,* Ex. 1037 (Model Order); Ex. 1038; Ex. 1039, Hr'g Tr. at 24:8-25:14. Accordingly, even if trials proceed as currently scheduled, there is a real possibility the '047 Patent will not be asserted.

C. FACTOR 3: THE DISTRICT COURT HAS NOT INVESTED SIGNIFICANT RESOURCES, AND PETITIONER HAS ACTED DILIGENTLY, WHICH FAVORS INSTITUTION

Factor 3 also favors institution. The district court proceeding is at an early stage, with relatively little investment from the court and parties. Fact discovery only recently began and is not set to conclude until June 24, 2022. Exs. 1030-1031 (Scheduling Orders). The parties have not exchanged claim terms or proposed constructions, a *Markman* hearing is not scheduled until May 18, 2022, and deadlines for expert discovery and dispositive motions fall many months later. *Id*. No depositions have been taken and no dispositive motions have been filed. *Cf. Apple Inc. v. Seven Networks, LLC*, IPR2020-00266, Paper 12 at 13-14 (PTAB Aug. 14, 2020) (favoring institution when "unclear to what extent the … [c]ourt has invested resources … that bear directly on the issue of … validity"); *Apple v. Parus*,

IPR2020-00686 at 15-17 (no dispositive motions, expert reports, or Daubert challenges).

Second, Petitioner diligently prepared and filed this Petition. As previously noted, Patent Owner filed two cases against Petitioner asserting 13 patents in the span of two days. The infringement contentions in each matter were first served September 29, 2021, and were supplemented on December 24, 2021. Between the two cases, Patent Owner asserts infringement of over 1,000 products from 11 unrelated patent families. *See* Ex. 1040 (Infringement Contentions). Given the broad allegations, Petitioner spent considerable time locating and analyzing prior art for 13 different patents. In addition, as explained below, Petitioner is challenging a claim not asserted in district court, which required additional analysis beyond that needed for district court invalidity contentions.

Petitioner filed this Petition around four months after receiving Patent Owner's voluminous infringement contentions, around one month after Patent Owner supplemented those contentions, and more than three months before the statutory bar.[1] Petitioner diligently prepared and filed this Petition, and has not

[1] Patent Owner filed its complaint on April 20, 2021, and purports to have effectuated service as of May 14, 2021.

delayed filing for any strategic advantage. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 17 (PTAB Dec. 1, 2020) (precedential) (filing petition two weeks before statutory deadline not dilatory, "particularly in view of the large number of patents and claims challenged").

D. FACTOR 4: LACK OF OVERLAP IN ISSUES FAVORS INSTITUTION

This factor favors institution. First, the district court will not determine patentability of all Challenged Claims, because Patent Owner has not asserted claims 2-4 and 9-10 of the '047 patent in the district court. Ex. 1040; *see, e.g., Apple Inc. v. Maxell, Ltd.*, IPR2020-00200, Paper 11 at 22 (PTAB July 15, 2020) (factor 4 favored institution where unasserted claims are challenged before the Board); *Apple Inc. v. Seven Networks, LLC*, IPR2020-00157, Paper 10, 17-20 (PTAB June 15, 2020) ("*Fintiv* factor 4 weighs strongly in favor of Petitioner" where the IPR trial would resolve claims "which the District Court Action will not address").

Second, the issues raised in this Petition will not overlap with the issues in district court. Petitioner (and RPIs) offers a stipulation broader than in *Sand Revolution II*, IPR2019-01393, Paper 24 (June 16, 2020) (informative). Petitioner stipulates that if this IPR is instituted and the Board proceeds with a trial, Petitioner will not, as to any claims upon which institution is granted, pursue in the district court case: (1) the same grounds presented in this Petition, or (2) any invalidity defenses under 35 U.S.C. §§102 or 103 that make use of the prior art references

asserted in the grounds of this Petition (Shimoda, Baek, and Sasaki). Thus, there will be no overlap of issues between the two proceedings, and this factor weighs against the Board exercising discretion to deny.

E. FACTOR 5: WHETHER PETITIONER AND DEFENDANT IN PARALLEL PROCEEDING ARE SAME PARTY

The parties in the two proceedings are the same, and it would be speculative to determine which tribunal will reach a final decision first. This factor is therefore neutral. *Google LLC v. Parus Holdings, Inc.*, IPR2020-00846, Paper 9 at 20-21 (PTAB Oct. 21, 2020) ("[W]e decline to speculate as to whether we are likely to address the challenged patent before the Texas court. Thus, this factor is neutral.").

F. FACTOR 6: THE PETITION'S MERITS ARE STRONG AND FAVOR INSTITUTION

This Petition is strong and merits institution, for all of the reasons explained below. For example, none of the references asserted herein were previously considered by the Patent Office. *Cf. Comcast Cable Commn's, LLC v. Rovi Guides, Inc.*, IPR2019-00231, Paper 14 at 11 (PTAB May 20, 2019) (obviousness challenges not "previously considered by the Office or by any court" weigh in favor of not denying institution).

Finally, "trial here avoids potentially complicated and overlapping jury issues" concerning multiple patents. *Apple Inc. v. Seven Networks, LLC*, IPR2020-00156, Paper 10 at 22 (PTAB June 15, 2020) (finding factor 6 strongly favored

institution). As noted above, the related district court cases involve 13 asserted patents and over 1,000 accused products. Institution of this IPR provides the opportunity for narrowing and simplifying the litigation for the district court and the jury.

III. PERSON OF ORDINARY SKILL IN THE ART ("POSITA")

A. LEVEL OF ORDINARY SKILL

A POSITA would have undergraduate degree in electrical engineering (or equivalent subject) together with two or three years of experience in designing circuits for driving light-emitting devices including organic light-emitting diodes, or a Ph.D. with experience in the same. Ex. 1002, ¶¶53-54.

B. BACKGROUND KNOWLEDGE OF A POSITA

Inquiring into whether "any 'differences' between the invention and the prior art would have rendered the invention obvious … necessarily depends on [a POSITA's] knowledge," including an "assessment of the … background knowledge possessed" by the POSITA. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020). The subjects below were "within the general knowledge" of a POSITA. *See id.* at 1338; *Dish Network L.L.C. v. Broadband iTV, Inc.*, IPR2020-01267, Paper 15 at 10 n.4 (P.T.A.B. Jan. 21, 2021) ("[W]e do not include the general knowledge of a person of ordinary skill in the art in listing the grounds themselves, recognizing that such knowledge is considered in every analysis.").

Dr. Kattamis corroborates the general knowledge of a POSITA with engineering references (Ex. 1007, Ex. 1008, Ex. 1009), published well before the ’047 Patent. Camara published in 2002 “as an all-inclusive reference book for both the practicing engineer and the undergraduate electrical engineering student.” Ex. 1007, Preface. Den Boer published in 2005 and summarizes “Active Matrix Liquid Crystal Displays: Fundamentals and Applications.” Ex. 1008, Title. Han published in 2006 and discusses driving LED displays. Ex. 1009; Ex. 1002, ¶¶57-59. Each of the topics would have been well-known to a POSITA before the priority date of the ’047 Patent. Ex. 1002, ¶¶56, 74.

a. <u>Display Background</u>

It was known that active-matrix displays include millions of pixels (e.g., “1080x1920 pixels”), with each pixel having “three subpixels” (e.g., red-green-blue). Ex. 1008, pp. 3, 176.

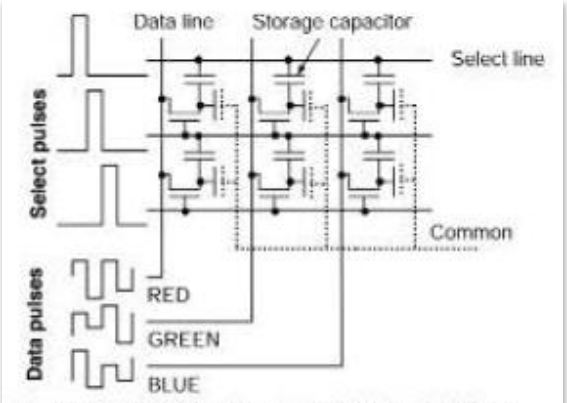


Figure 2.17: Operation of TFT LCD with drive waveforms.

Id., p. 40. It was also known to drive the pixels using a "TFT pixel array circuit (Fig. 2.17) [with] select buslines, data buslines, a TFT at each pixel, and a storage capacitor … at each pixel." *Id.*, pp. 39-40. Source drivers use red-green-blue data to drive the columns of lines running vertically in the displays, and gate or row drivers select the rows of horizontal lines and turn on pixels. *Id.*, p. 93-98; Ex. 1002, ¶¶60-61.

It was known that OLEDs are semiconductors comprising organic materials that convert electrical energy to light, much like LEDs. Individual OLED pixels are "current driven," meaning that a pixel's color and brightness are adjusted by setting the current through the manipulation of TFT(s). Ex. 1009, p. 53 §1; Ex. 1002 ¶62.

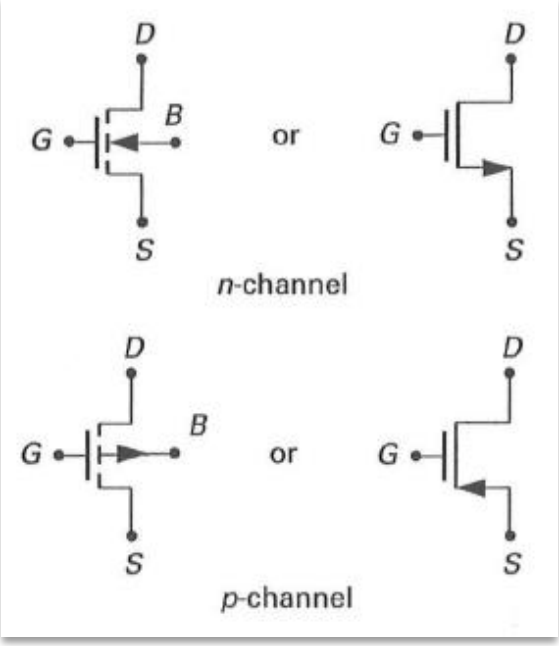
It was known that because of "inherent process variation" that occurs during manufacturing, "[a] number of TFT active matrix pixel circuits have been developed in order to compensate for TFT parameter variations" and to "compensate the non-uniform characteristics of the current" from those TFTs. Ex. 1009, Abstract, Introduction; Ex. 1002, ¶63.

b. <u>Basic Circuit Components for Displays</u>

It was known that an ideal voltage source represents a two-terminal device with fixed voltage across its terminals, regardless of current flow or the load that it drives. An ideal current source represents a two-terminal device that delivers fixed

current through its terminals, regardless of voltage or the load that it drives. Ex. 1007, pp. 26-4, 26-5; Ex. 1002, ¶¶64-65.

It was known to convert a voltage signal to a current signal. For example, it was known to configure a transistor to receive an input voltage (V_G) on its gate terminal and produce an output current flowing between drain and source terminals (I_D).

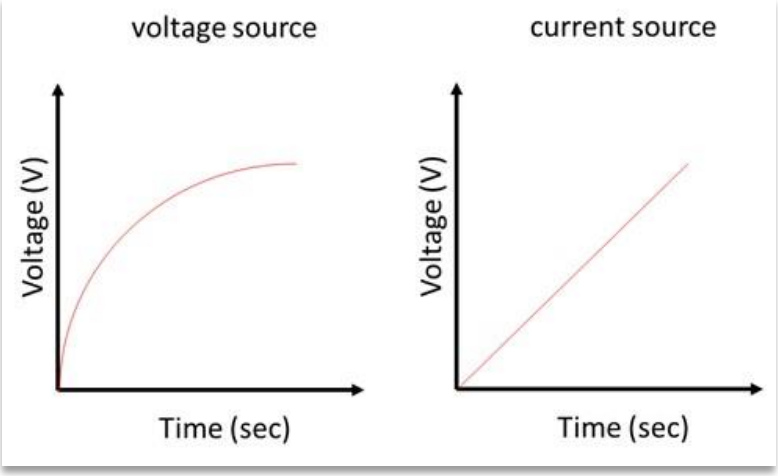


Ex. 1007, pp. 43-31, 43-32; Ex. 1002, ¶66.

c. <u>Voltage and Current Programming</u>

It was known that capacitors store charge, and it was known to use capacitors as a buffer in pixel circuits. Ex. 1008, p. 27. It was known that when charging a capacitor, voltage on the capacitor typically rises: exponentially when using a

voltage source (referred to as voltage programming), and linearly when using a current source (referred to as current programming).



Ex. 1007, pp. 29-4, 30-2 to 30-7. Thus, voltage sources were known to charge the capacitor faster, as compared to current sources. Ex. 1002, ¶¶67-69.

"[C]urrent programming pixel circuits can compensate mobility variation as well as threshold voltage variation." Ex. 1009, p. 53. A known advantage of current programming is that the current remains constant even if there are variations in TFT threshold voltage or mobility. Structures for current programming pixel circuits were known in the art.

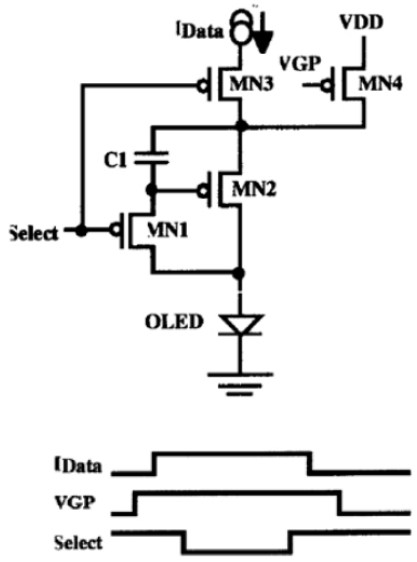


Figure 5. The reported current programming AMOLED pixel in which I_{DATA} is memorized and V_{GATE} of MN2 is determined to allow I_{DATA} [2].

Ex. 1009, Fig. 5. One known problem is that the relatively lengthy amount of time needed to charge a capacitor under current programming could limit the speed of the display. For example, uncompensated pixels with high capacitance were unable to attain the required brightness level within the timespan of an image frame, so extra drive voltage was applied to enable a compensated response.

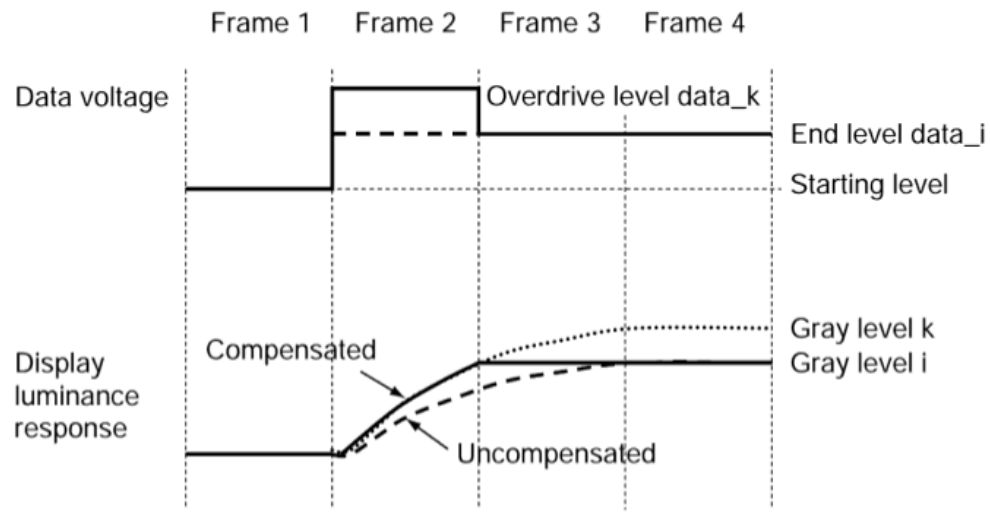


Figure 6.30: Overdrive data levels applied to speed up optical response time of display luminance between gray levels.

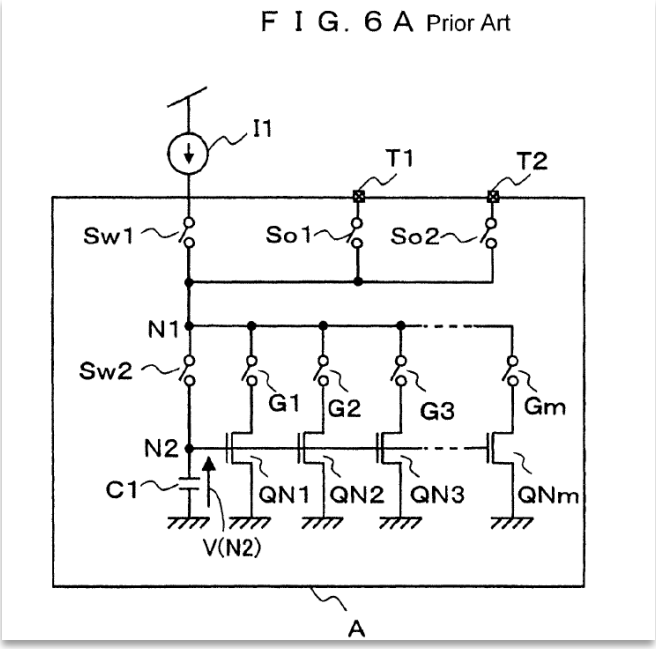
Ex. 1008, p. 168 (Fig. 6.30); Ex. 1002, ¶¶70-73.

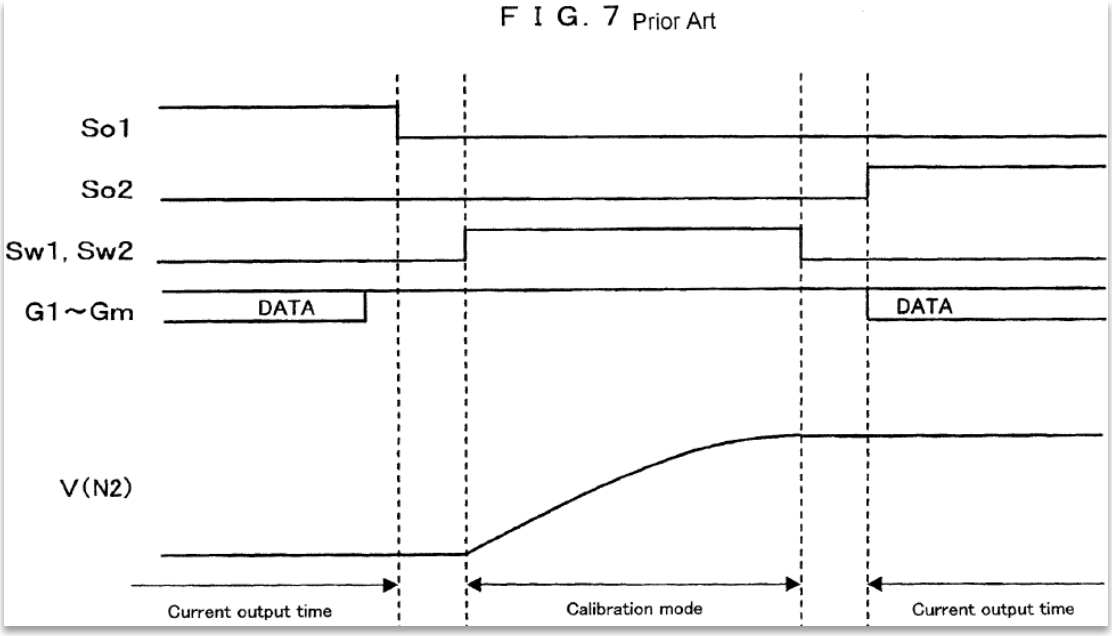
IV. OVERVIEW OF '047 PATENT

A. SUBJECT MATTER

The '047 Patent is directed to a "current driving device … for displays such as organic EL (Electro-luminescence) panels, LED panels, and the like." Ex. 1001, 1:5-7. The '047 Patent repeats a known problem that variations in electric currents are caused "due to fabrication processes of each transistor, causing non-uniformity in the display image. *Id.*, 1:11-20; Ex. 1002, ¶¶34-35.

One known solution, shown in Figures 6A and 7 (each labeled "Prior Art"), includes having two modes of operation: "calibration mode" and "current output mode."

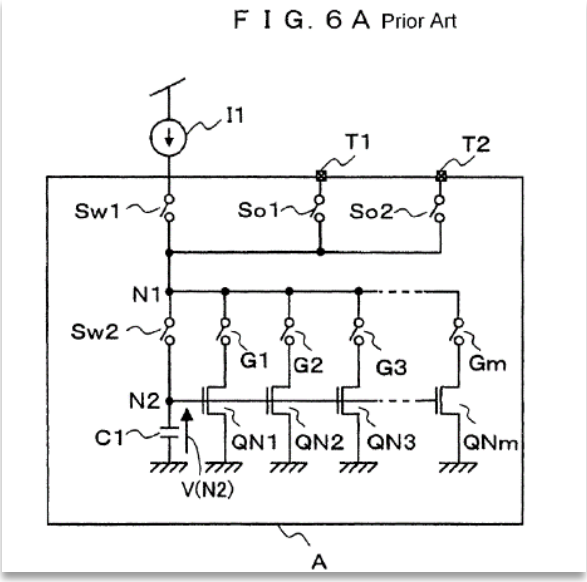


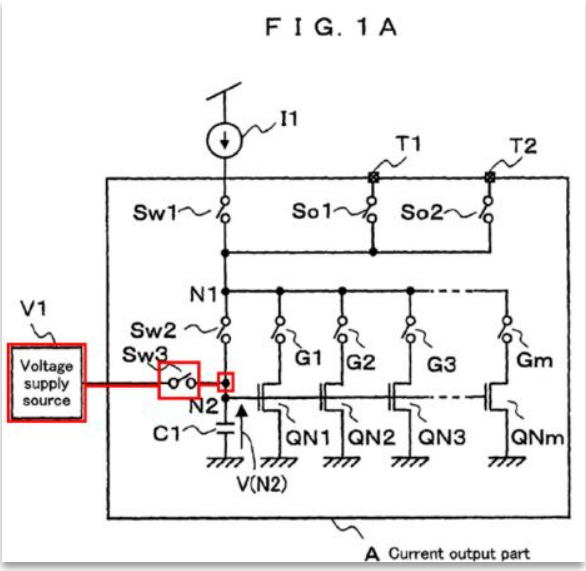


Ex. 1001, Figs. 6-7, 1:33-39, 2:8-13. During "calibration mode," transistors are operated so that current source I1 charges, or programs, storage capacitor C1. *Id.*, 1:37-51, Fig. 6A, Fig. 7. After it has been charged, capacitor C1 provides a voltage

during "current output mode" to control current of the circuit's output terminals. *Id.*, 1:60-2:7, Fig. 6A, Fig. 7. The '047 Patent describes a known shortcoming with these two operation modes of operation, that on account of charging with a current source I1, it takes too long to charge storage capacitor C1, resulting in limited speed at which a display image can be refreshed. *Id.*, 3:1-9, Fig. 6A; Ex. 1002, ¶¶36-42.

The '047 Patent proposes a known solution to these known problems to "perform calibration at a high speed and improve the non-uniformity of the output currents." Ex. 1001, 3:16-20. The '047 Patent modifies Fig. 6A (prior art) by including a voltage supply source, which the asserted prior-art references refer to as a "pre-charge circuit." Figure 6A (admitted prior art) is shown next to Figure 1A (purported invention), annotated to show the additional components added.





Id., Fig. 1A (annotated), Fig. 6A. The purported invention adds a pre-charge circuit (voltage supply source) and a switch (Sw3) to connect/disconnect the pre-charge circuit. Ex. 1002, ¶43.

The ’047 Patent discloses using the pre-charge circuit in an additional mode of operation referred to as a “voltage supply mode.” This voltage supply mode occurs before a current supply mode, and acts to pre-charge the capacitor (C1). Together the voltage supply mode and the current supply mode constitute the new “calibration mode” disclosed in the ’047 Patent. Ex. 1001, 2:8-13, 3:19-22, 9:32-34, Fig. 2. During the voltage supply mode, a voltage source, as opposed to a current source, charges capacitor C1. However, it was well-known that a voltage supply charges a capacitor faster than a current supply. *Supra* §III.B.c. And charging capacitors in two phases—using a voltage supply and current supply—was also known in the art. Ex. 1002, ¶¶44-45.

B. PROSECUTION HISTORY

The ’047 Patent was allowed after applicants amended independent claims 1 and 10 to distinguish prior art. Regarding Claim 1, applicants argued the prior art “fails to disclose that a voltage holding circuit has a terminal being connected to a reference voltage different from the first voltage, and under the voltage supply mode, the first voltage is supplied to another terminal of the voltage holding circuit.” Regarding claim 10, applicants argued the prior art “fails to disclose that the voltage

holding circuit has a first terminal and a second terminal, the first terminal being connected to a fixed voltage, and the current driving device includes a high-speed switch for controlling connection/disconnection states of **said voltage supply source with respect to the second terminal of said voltage holding circuit**." Ex. 1003 at 37-38 (emphasis in original); Ex. 1002, ¶¶47-52. As discussed below, the asserted references disclose these and the other claim limitations.

V. CLAIM CONSTRUCTION

For purposes of this proceeding, Petitioner applies the ordinary and customary meaning of the claims. Ex. 1002, ¶55. Constructions are proposed "only to the extent necessary." *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

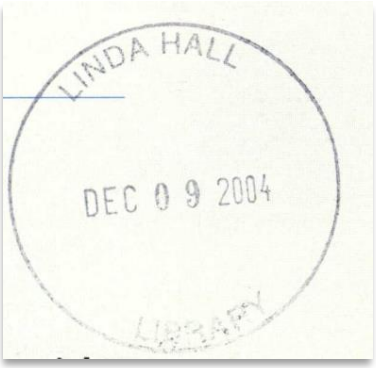
VI. OVERVIEW OF PRIOR ART

The '047 Patent was filed in the United States on 12/12/2007, claiming priority to JP 2006-335850 (filed 12/13/2006). The asserted references qualified as printed publications more than one year before 12/12/2007, and are thus prior art under 35 U.S.C. §102(b). *See* M.P.E.P §2133(II) ("The 1-year time bar is measured from the U.S. filing date").

A. SHIMODA: EX. 1004

Shimoda qualifies as a printed publication under 35 U.S.C. §§102(a) and 102(b) by December 19, 2004. Ex. 1019, ¶¶51-52. Dr. Mullins, a librarian expert,

confirms authenticity by comparing Shimoda (Ex. 1004) to print copies held at two libraries (Ex. 1020, Ex. 1021). Ex. 1019, ¶¶29-36. As evidenced by authentic date stamps, Shimoda was received by: Linda Hall Library on December 9, 2004 (Ex. 1020) and Library of Congress on June 15, 2005 (Ex. 1021). Each library would have made Shimoda publicly accessible 7-10 days afterwards.

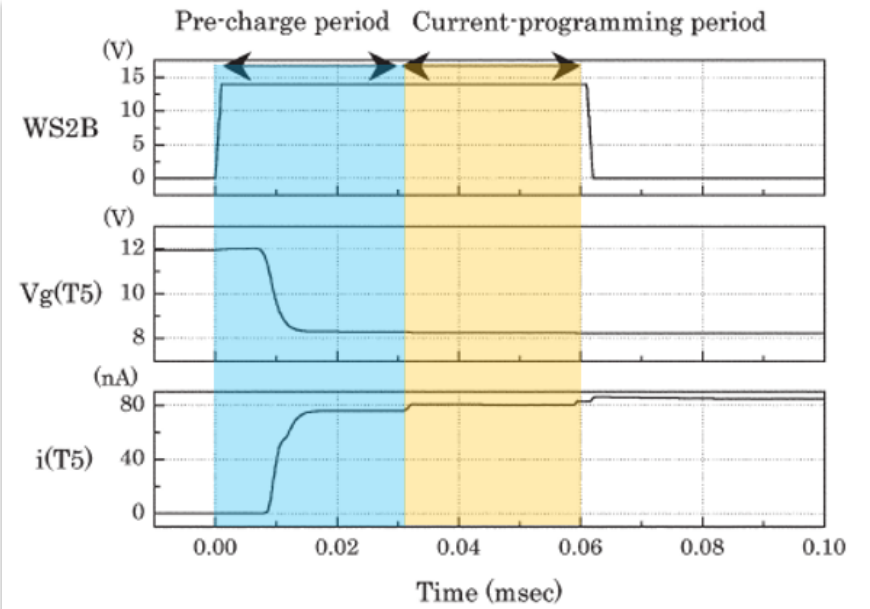


Ex. 1020; Ex. 1021; Ex. 1019, ¶¶34-35, 44-46. Shimoda was catalogued and locatable through the world's largest online catalog, WorldCat. Ex. 1019, ¶¶22, 38. Shimoda was published in Journal of SID. Dr. Kattamis also published in Journal of SID, and explains how it was a periodical devoted to electronic displays. Ex. 1002, ¶¶75-76; Ex. 1010, Ex. 1011. As further evidence of public accessibility,

Shimoda was actually received and cited by others. Ex. 1026 and Exhibit 2017 cite Shimoda in 2004 and 2006, respectively. Ex. 1019, ¶¶47-52.

Shimoda addresses the same problem as the '047 Patent, explaining that "non-uniformity in the current-voltage characteristics of the [TFTs] that form part of the pixel circuit" leads to non-uniform current delivered the pixels. Ex. 1004, §1. Shimoda explains that each pixel is driven by a pixel circuit, and that the "brightness [of the pixel] is dependent on the current in the OLED that is driven by each pixel circuit." *Id.* Similar to the '047 Patent, Shimoda recognizes that the "current-programming approach" was in the prior art, but notes that "programming time will be relatively long." *Id.* Ex. 1002, ¶¶78-79.

Shimoda teaches increasing charging speed of the capacitor by adding to the current-driving device a pre-charge circuit, which "pre-charges" the capacitor before the current-programming period. Ex. 1004, §3.2. After the pre-charge period (annotated blue), a current-programming period (annotated yellow) compensates for errors generated during the pre-charge period.



(a) Pixel-driving with pre-charge

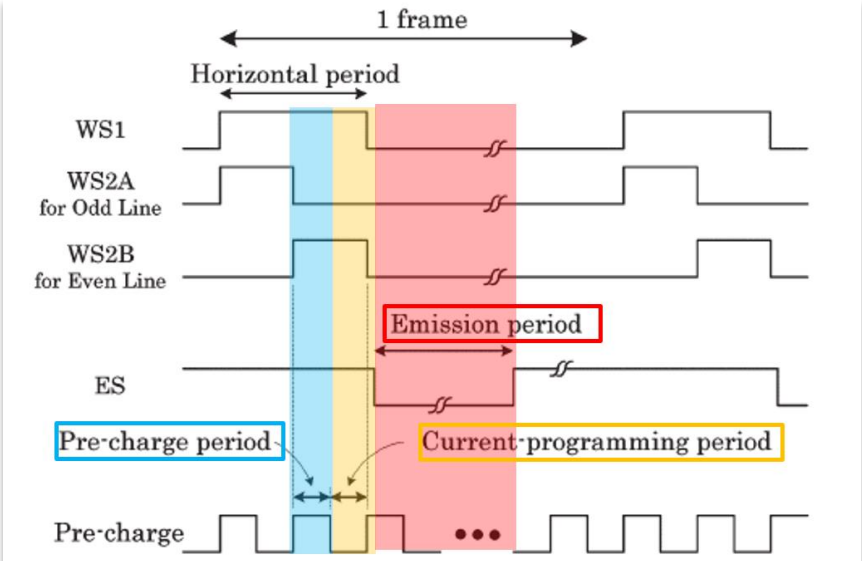


FIGURE 7 — Timing chart illustrating current data driver and pixel circuit operations. The signals Write scan1 (WS1), Write scan 2A/B (WS2A/B), and Erase scan (ES) are output by an integrated gate driver.

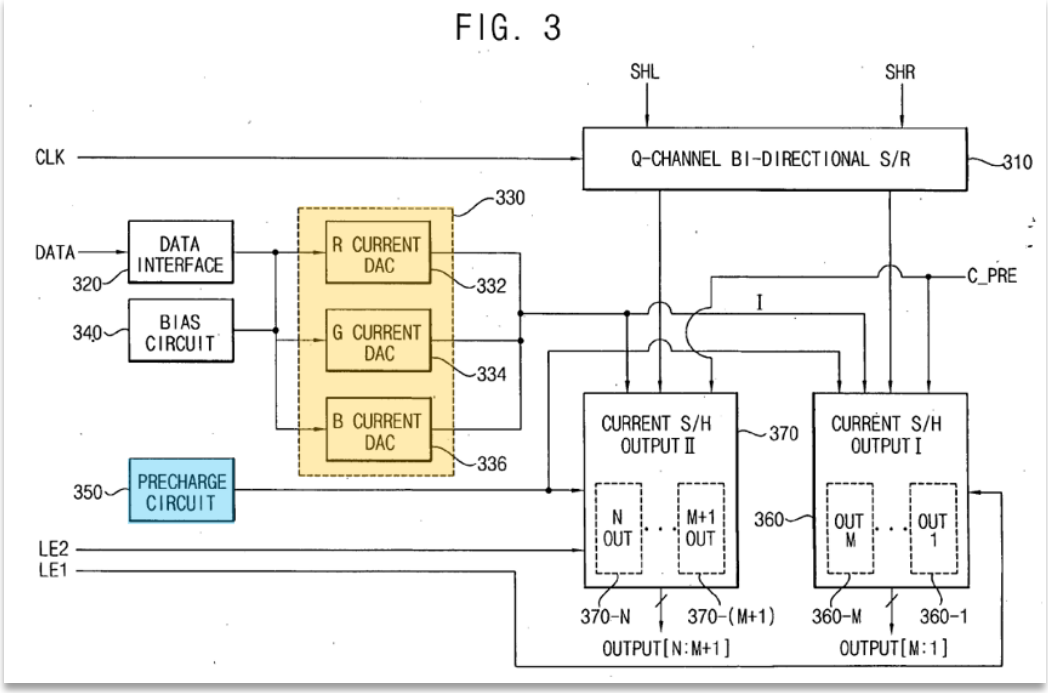
Ex. 1004, Figs. 7 and 8a (annotated). Thus, Shimoda addresses the known problem identified in the ’047 Patent and provides a similar solution. *Id.*, Abstract; Ex. 1002, ¶¶80-81.

B. BAEK: EX. 1005

U.S. Patent Publication 2006/0170629 (“Baek”) published August 3, 2006. Therefore, Baek qualifies as prior art under 35 U.S.C. §§102(b) and 102(e).

Baek discloses “a display driver circuit for a flat display panel,” including for “current-driven active matrix type OLED display devices.” Ex. 1005, ¶¶[0003], [0064]. Similar to the ’047 Patent, Baek adds a pre-charge circuit to a conventional driving circuit in order to reduce charge time. *Id.*, ¶¶[0026], [0062]; Ex. 1002, ¶¶83-84.

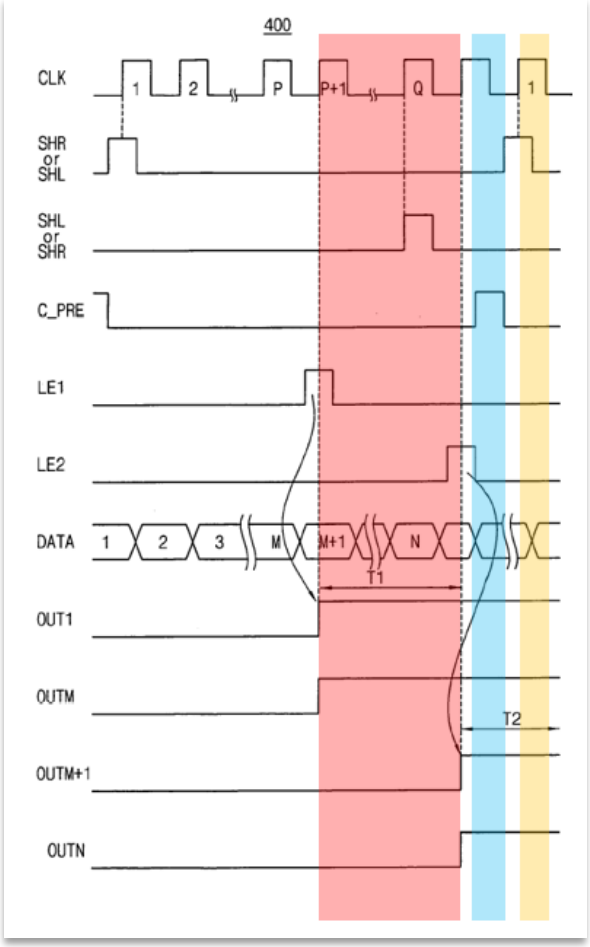
A current digital-to-analog converter (DAC) 330 (annotated gold) supplies current to sample/hold (S/H) output circuits 360 and 370. Ex. 1005, ¶¶[0045]-[0048].



Ex. 1005, Fig. 3 (annotated). Similar to the ’047 Patent, Baek employs a pre-charge circuit (annotated blue) to pre-charge the storage capacitor CST to “reduce a charge time.” Ex. 1005, ¶¶[0062]-[0063]; Ex. 1002, ¶¶85-86.

Similar to the ’047 Patent, Baek discloses the circuit may operate under three modes: voltage-supply mode (annotated red); current supply mode (annotated blue); and current output mode (annotated yellow). When C_PRE signal is activated (annotated red), the pre-charge circuit applies a voltage to the storage capacitor CST to “pre-charge a voltage of the storage capacitor CST….” Ex. 1005, ¶¶[0062]-[0063]. When CLK signal is activated (annotated blue), current from DAC is supplied to storage capacitor CST and further charges the capacitor. *Id.*, ¶[0056].

When a latch enable (LE) signal is activated (annotated yellow), the circuit outputs current based on the voltage stored in storage capacitor CST. *Id.*, ¶¶[0057]-[0058].



Ex. 1005, Fig. 4 (annotated); Ex. 1002, ¶¶87-88.

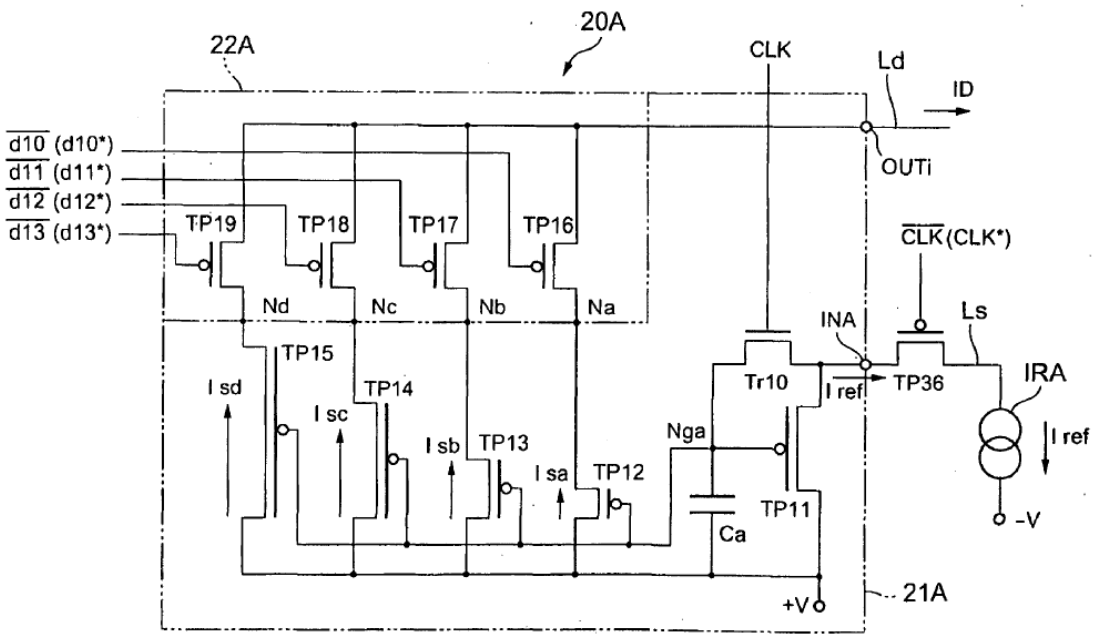
C. <u>SASAKI: EX. 1006</u>

U.S. Patent Publication 2005/0017765 ("Sasaki") published January 27, 2005. Therefore, Sasaki qualifies as prior art under 35 U.S.C. §§102(b) and 102(e).

Sasaki discloses a driving circuit with similar layout as the '047 Patent, for use with "a display panel comprising … display pixels comprising current control

type light emitting devices." Ex. 1006, ¶[0003]. Sasaki recognizes the known problem with "variations in the current values of the light generation drive currents." *Id.*, ¶[0009]. Further, Sasaki recognizes the problem identified in the '047 Patent that "charge and discharge operation takes time and until the potential of the current supply source line is stabilized, a relatively lengthy period is required." *Id.*, ¶[0010]. Sasaki teaches a driving circuit that includes a capacitor Ca "charge storage circuit", which receives a reference current (Iref) from a current supply source (IRA) and holds a voltage corresponding to the reference current Iref. *Id.*, ¶¶[0014], [0071].

FIG. 3



Ex. 1006, Fig. 3. A set of module current transistors generate currents based on the voltage held in the capacitor Ca, which are transmitted to downstream pixels. *Id.*, ¶[0063]; Ex. 1002, ¶¶90-92.

VII. GROUNDS 1-2: SHIMODA

Claims 1-4, and 9 are anticipated by Shimoda (Ex. 1004) (Ground 1). They are also obvious over Shimoda for substantially similar reasons, as further explained below (Ground 2). *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) ("A disclosure that anticipates under § 102 also renders the claim invalid under § 103, for anticipation is the epitome of obviousness") (cleaned up); Ex. 1002, ¶93.

A. CLAIM 1

a. 1(pre): "A current driving device, comprising:"

To the extent the preamble is limiting, Shimoda discloses it. The current driving device of Shimoda includes an integrated current data driver (containing the pre-charge circuit) and a pixel circuit.

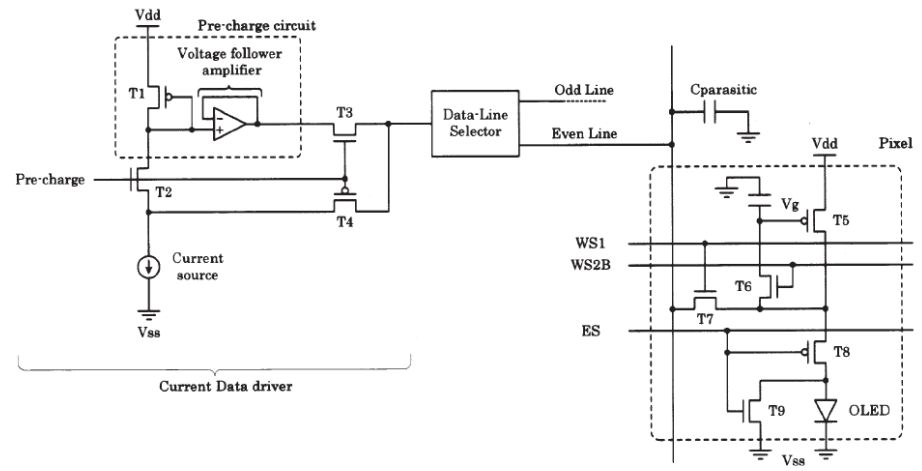


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

Ex. 1004, Fig. 6. "Figure 6 is a diagram of both the pixel circuit and the integrated current data driver containing a pre-charge circuit," as well as an OLED. *Id.*, §3.1; *see* Fig. 1 ("Block diagram of current data driver"). The "current data driver is capable of outputting … current," and "current in the OLED … is driven by each pixel circuit." *Id.*, Abstract, §1; Ex. 1002, ¶¶94-95.

b. <u>1(a): "a first voltage supply source for supplying a first voltage;"</u>

Shimoda discloses this limitation. The "pre-charge circuit" (annotated blue) is an example of the claimed "a first voltage supply source," and it supplies "a first voltage" (annotated green).

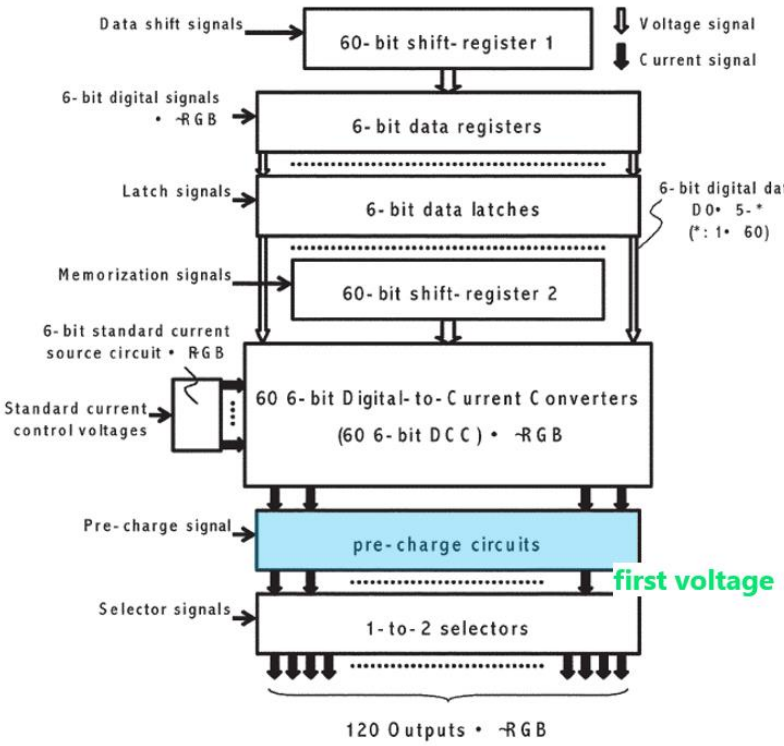


FIGURE 1 — Block diagram of current data driver, which contains shift register 1, 6-bit data registers, 6-bit data latches, shift-register 2, 6-bit digital-to-current converters (DCCs), a standard current source circuit, pre-charge circuits, and 1-to-2 selectors.

Ex. 1004, Fig. 1 (annotated).

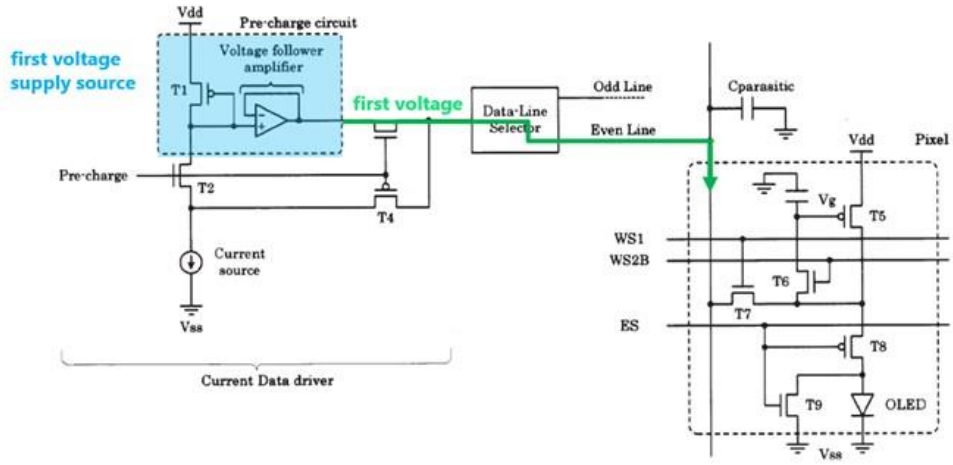


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

Id., Fig. 6 (annotated). "The pre-charge circuit is composed of one TFT (T1) and a voltage-follower amplifier." *Id.*, §3.1. The "voltage-follower amplifier outputs the gate voltage of T1 into the gate electrode of T5, with T6 and T7 turned on. This pre-charge function rapidly pre-charges the voltage in the gate electrode of T5…" *Id.*, §3.2; Ex. 1002, ¶¶96-98.

c. <u>1(b): "a first current supply source for supplying a first electric current;"</u>

Shimoda discloses this limitation. Shimoda discloses the claimed current source (annotated gold) and the lines (annotated red) along which flow the first electric current supplied by that current source.[2]

[2] The red arrow indicates the direction of how energy is supplied in the form of current, while the actual current may flow in an opposite direction depending on the configuration of Vdd and Vss.

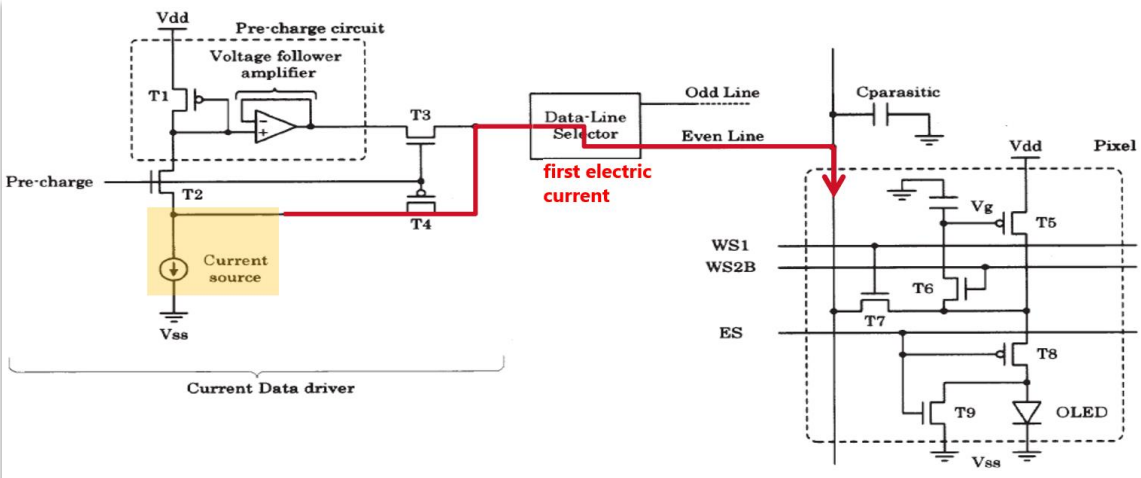


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

Ex. 1004, Fig. 6 (annotated).

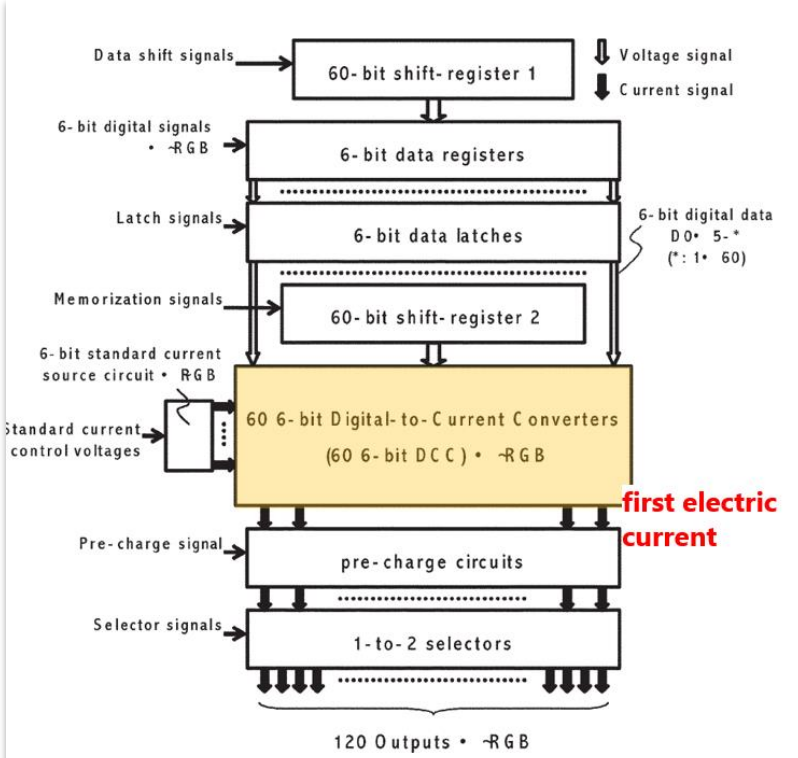


FIGURE 1 — Block diagram of current data driver, which contains shift register 1, 6-bit data registers, 6-bit data latches, shift-register 2, 6-bit digital-to-current converters (DCCs), a standard current source circuit, pre-charge circuits, and 1-to-2 selectors.

Id., Fig. 1 (stating that the "current data driver … contains …. 6-bit digital-to-current converters (DCC)"). The "current source indicated in the diagram represents a 6-bit DCC [digital-to-current converter] which generates an analog current…." *Id.*, §6.1. The current supplied by the current DCC of Shimoda is an example of the claimed "a first electric current." Ex. 1002, ¶99.

d. 1(c): "a plurality of output terminals;"

Shimoda provides at least two examples of structure constituting a plurality of output terminals. Ex. 1002, ¶100.

First, Shimoda discloses that each current data driver comprises at least "120 Outputs" (annotated green).

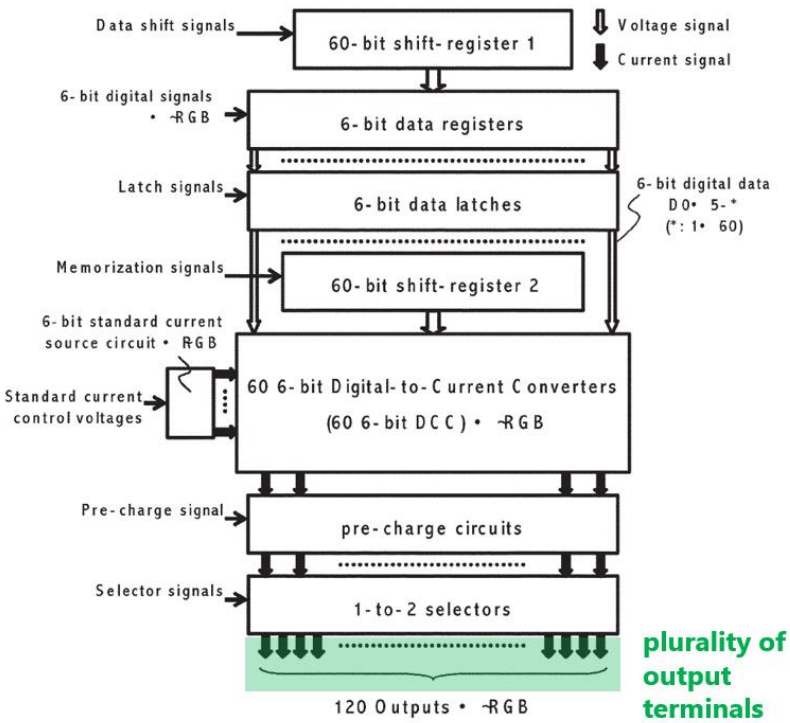
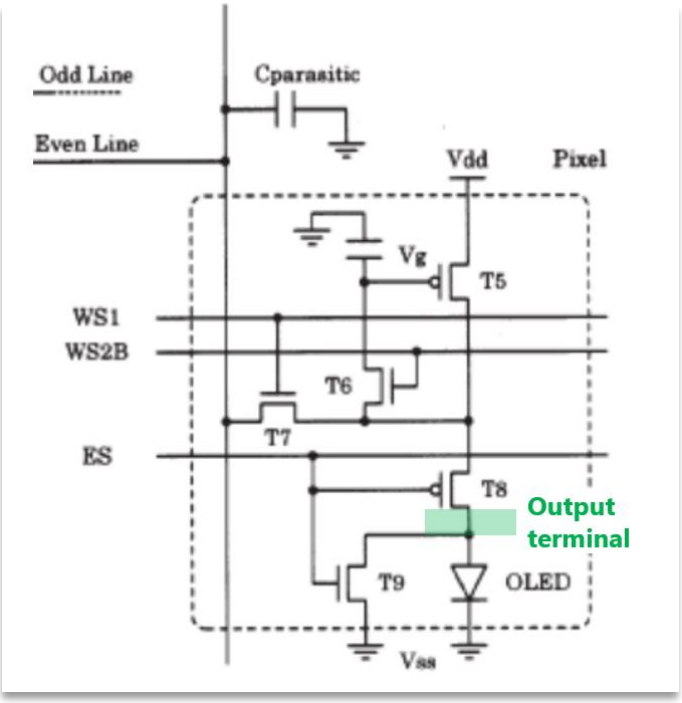


FIGURE 1 — Block diagram of current data driver, which contains shift register 1, 6-bit data registers, 6-bit data latches, shift-register 2, 6-bit digital-to-current converters (DCCs), a standard current source circuit, pre-charge circuits, and 1-to-2 selectors.

Ex. 1004, Fig. 1 (annotated); *see* §5 (Table 1, pixel count of "120×RGB×136"). Thus, the display includes an array of 120×136 pixels, with each pixel providing three colors (red, green, blue). Ex. 1002, ¶101.

Second, Shimoda provides another example of a plurality of output terminals. The drain of transistor T8 (annotated green) is connected to the OLED, outputs calibrated current to the OLED, and is an example of an output terminal:



Id., Fig. 6 (annotated and excerpted). The exemplary device in Shimoda comprises at least 120×136 pixels (*id.*, Abstract), and each individual pixel comprises at least one output terminal (annotated green above). Thus, Shimoda discloses a plurality of output terminals. Ex. 1002, ¶102.

e. <u>1(d)(1): "and a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising"</u>

Shimoda discloses this limitation. Each pixel circuit is an example of the claimed "current output circuit," because for example, it outputs current to an OLED. Though Figure 6 of Shimoda graphically depicts a single pixel circuit, a

POSITA would have recognized (or at least it would have been obvious) that there would be a plurality of such pixel circuits. Ex. 1002, ¶103.

As described for Claim Limitation 1(b), the current supplied by the current DCC is an example of the claimed "a first electric current." Each pixel circuit (annotated purple) receives a current (the claimed "first electric current," annotated red) from the claimed current source (annotated gold) during a current-programming period.[3]

> In the subsequent current-programming period, T4 is turned on, T2 and T3 are turned off, the pre-charge circuit is disconnected, ***and the current from the current source is directly supplied to the pixel circuit***.[4]

Ex. 1004, §3.2.

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[3] *See supra* footnote 2.

[4] Emphasis supplied throughout, unless noted.

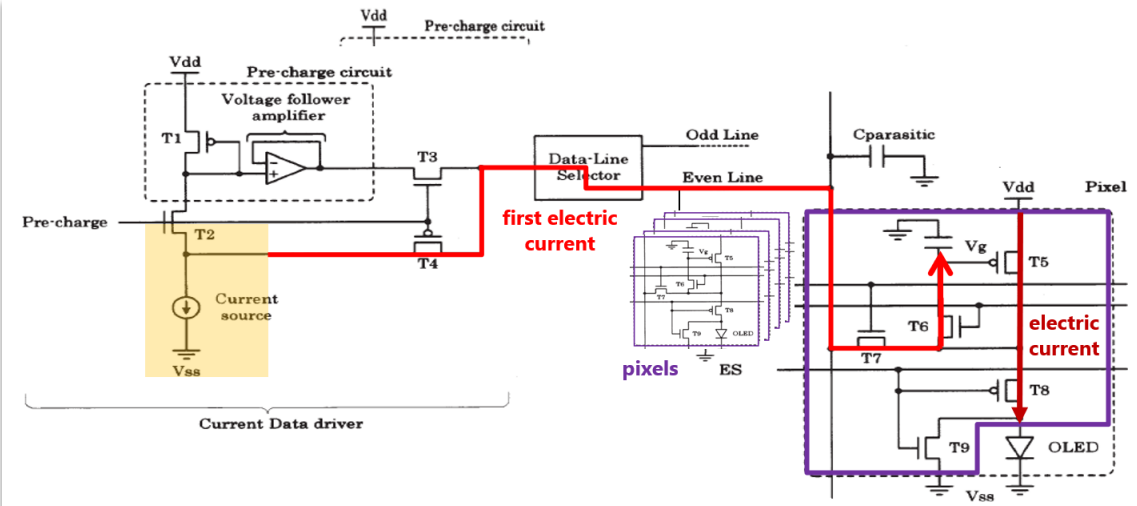


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

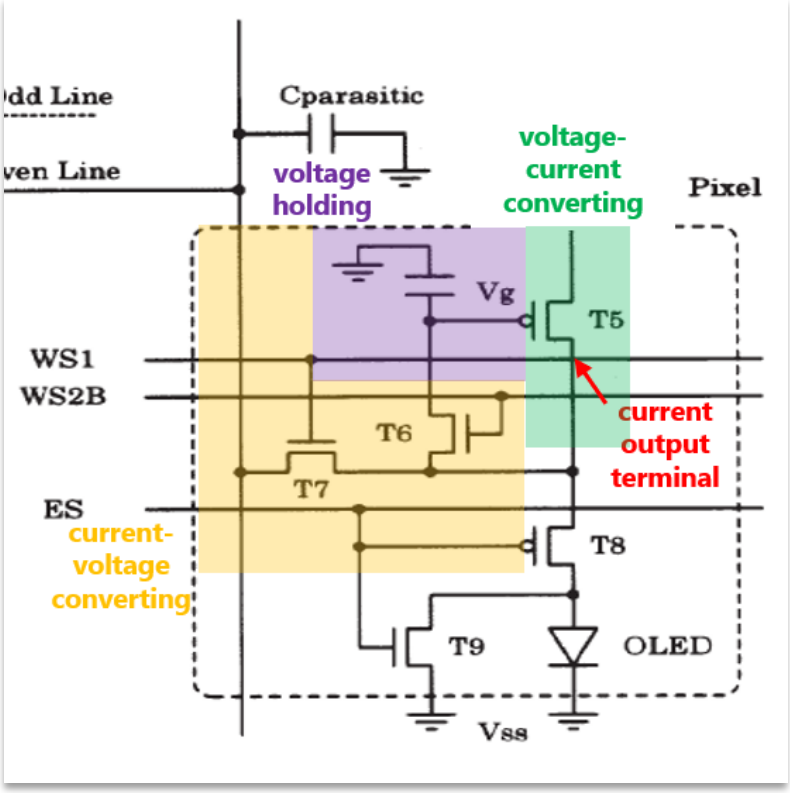
Id., Fig. 6 (annotated to add multiple pixel circuits in purple, because Shimoda discloses that multiple pixels would exist). Then during an emission period, the pixel circuit outputs a current (the claimed "an electric current," annotated dark red) in accordance with the first electric current. *See*, *Id.*, §3.2. The current-programming period and the emission period are explained in more detail below regarding claim elements 1(f)-1(h). Ex. 1002, ¶104.

Each pixel circuit outputs an electric current "in accordance with" the first electric current (e.g., current from the DCC in current source). A POSITA would have recognized that one of the fundamental properties of transistors is that they output a current in accordance with its gate voltage. During an emission period, the current output from transistor T5 is determined by the gate voltage of transistor T5, which was calibrated during the current-programming period by the first electric current. *See*, Ex. 1004, §3.2; Ex. 1002, ¶105.

Figure 6 of Shimoda graphically depicts one pixel circuit (current output circuit), but a POSITA would have recognized (or in the alternative, it would have been obvious) that the device fabricated by Shimoda would have two or more identical such pixel circuits. Shimoda describes that a display has multiple OLED pixels and ("120×136-pixel AMOLED display using these circuits"), and each OLED is driven by a pixel circuit ("This brightness is dependent on the current in the OLED that is driven by each pixel circuit"). Ex. 1004, Abstract, §1; *see* Fig. 3 (output of a pixel circuit is an OLED); Ex. 1002, ¶106.

f. <u>1(d)(2): "a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein,"</u>

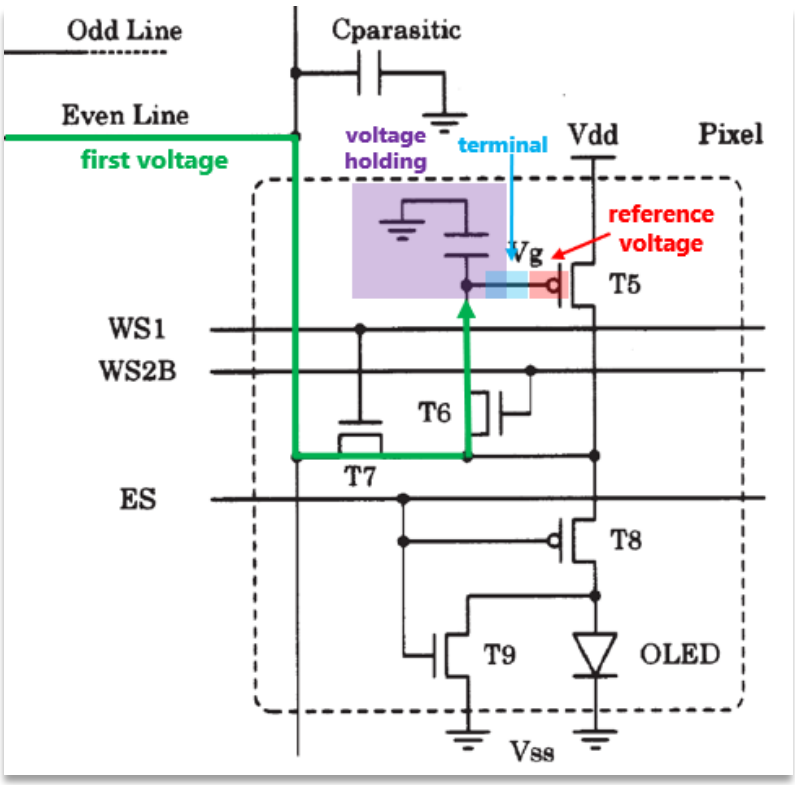
Shimoda discloses this limitation. Each pixel circuit in Shimoda discloses a current-voltage converting circuit (annotated gold), a voltage-current converting circuit (annotated green), a voltage holding circuit (annotated purple) and current output terminal (annotated red).



Ex. 1004, Fig. 6 (annotated and excerpted); Ex. 1002, ¶107.

i. "a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage"

The pixel circuit includes a voltage holding circuit (annotated purple), which further includes a gate capacitor that stores the gate voltage (Vg) of transistor T5 during the current-programming period. *See* Ex. 1004, at §3.2.



Ex. 1004, Fig. 6 (annotated and excerpted). The gate capacitor is connected to ground, and also has a terminal (annotated blue) connected to the gate of transistor T5. The voltage on the capacitor varies depending on operation mode: it corresponds to the claimed "first voltage" during the pre-charge period, and corresponds to a different voltage, the claimed "reference voltage," during the current-programming period. Ex. 1002, ¶¶108-109.

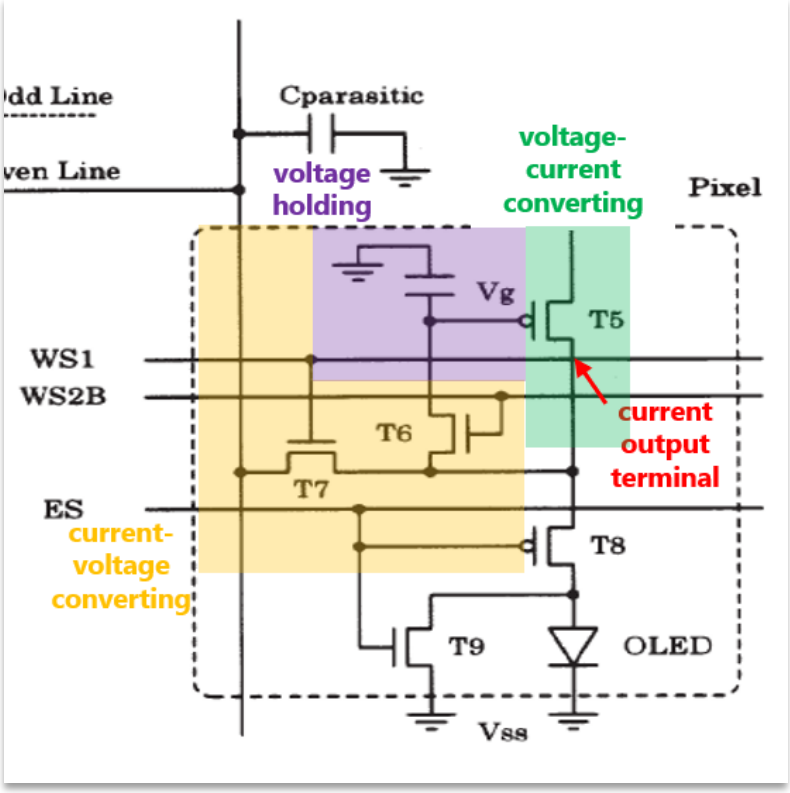
During the pre-charge period, the pre-charge circuit provides the claimed "first voltage" (annotated dark green) to charge the gate capacitor, thus increasing the gate voltage of transistor T5 to such a level that "a current roughly equivalent to the value of the current source flows through T5." Ex. 1004, §3.2. During the

current-programming period, the gate capacitor is further charged until it reaches a reference voltage different than the first voltage. A purpose of the current-programming period is so that errors that occurred during the pre-charge period "can be compensated for." *Id.*, §3.2; Ex. 1002, ¶110.

This analysis is consistent with the description of these elements in the '047 Patent, which also includes capacitor for holding voltage that is connected between ground and a transistor gate. Ex. 1001, 7:3-6, 8:11-15. Similar to Shimoda, two supply modes are described in the '047 Patent: a voltage supply mode (pre-charge period) during which the capacitor voltage corresponds to the claimed "first voltage"; and a current supply mode (current-programming period) during which the capacitor voltage corresponds to the claimed "reference voltage." Ex. 1001, 7:48-52, 8:6-8; Ex. 1002, ¶111.

ii. "a current-voltage converting circuit"

The pixel circuit includes a current-voltage converting circuit (annotated gold):



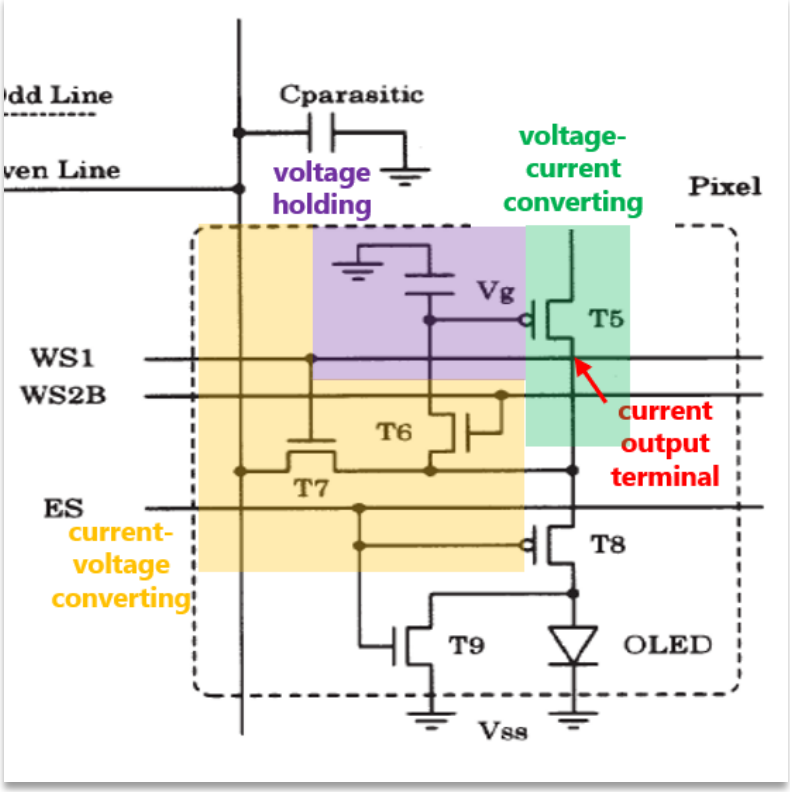
Ex. 1004, Fig. 6 (annotated and excerpted). The current-voltage converting circuit converts the first electric current from the current source to the gate voltage held at the gate capacitor. *Id.*, §3.2. During a current-programming period (the claimed "current supply mode"), switching transistors T6 and T7 are turned on, causing the first electric current to charge the gate capacitor. *Id.* The voltage across the gate capacitor (gate voltage) thus increases until a reference voltage, under which the first current flows through transistor T5. Ex. 1002, ¶112.

This analysis is consistent with the description of these elements in the '047 Patent, which under current-supply mode, "the current supply source" is connected "to the voltage holding capacitor C1 and current-voltage converting elements …."

Ex. 1001, 8:60-64; 10:28-36; Fig. 1A. The reference voltage is provided at the gates of transistors QN1-QNm and held in the voltage holding capacitor C1. *Id.*, 8:3-11; Ex. 1002, ¶113.

iii. "a voltage-current converting circuit"

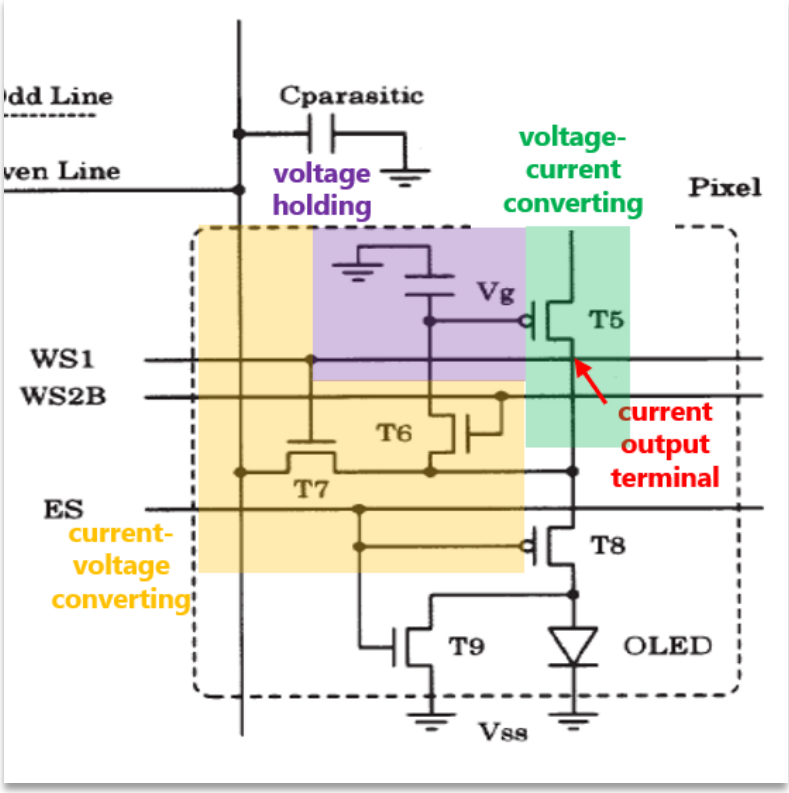
The pixel circuit includes a voltage current converting circuit (annotated green), which further includes thin-film transistor T5. During an emission period: switching transistors T6, T7, and T9 are turned off; switching transistor T8 is turned on; transistor T5 outputs a current to the downstream OLED in accordance with the voltage applied to its gate terminal through its drain terminal.



Ex. 1004, Fig. 6 (annotated and excerpted). This analysis is consistent with the description of these elements in the '047 Patent, which explains that the voltage-current converting function is performed in the current output mode (emission period). Ex. 1001, 8:30-38; Ex. 1002, ¶¶114-115.

iv. "at least one current output terminal"

In the pixel circuit, the drain terminal (annotated red) of transistor T5 is an example of the claimed "current output terminal." As explained above, transistor T5 outputs at the drain a current in accordance with its gate voltage.



Ex. 1004, Fig. 6 (annotated and excerpted). This analysis is consistent with the description of these elements in the '047 Patent, which explains that under a current

output mode that a transistor (T2) includes a current output terminal. Ex. 1001, 8:30-33; Ex. 1002, ¶¶116-117.

g. <u>1(e): "each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,"</u>

Shimoda discloses this limitation. Each of the pixel circuits operates in at least three operation modes: pre-charge period ("voltage supply mode," annotated blue), current-programming period ("current supply mode," annotated gold), and emission period ("current output mode," annotated red). The caption of Figure 7 states, "[t]iming chart illustrating current data driver and pixel circuit operations."

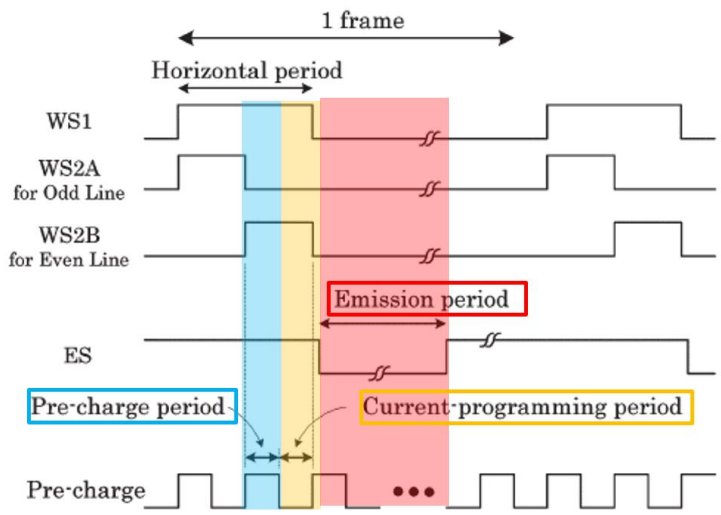


FIGURE 7 — Timing chart illustrating current data driver and pixel circuit operations. The signals Write scan1 (WS1), Write scan 2A/B (WS2A/B), and Erase scan (ES) are output by an integrated gate driver.

Ex. 1004, Fig. 7 (annotated); Ex. 1002, ¶118.

h. <u>1(f): "under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit,"</u>

Shimoda discloses operation under a voltage supply mode, including a pre-charge period (annotated blue). The purpose of a "data-line pre-charge function [is] in order to reduce current-programming times and to achieve accurate current-programming at low gray-scale levels." Ex. 1004, §3.

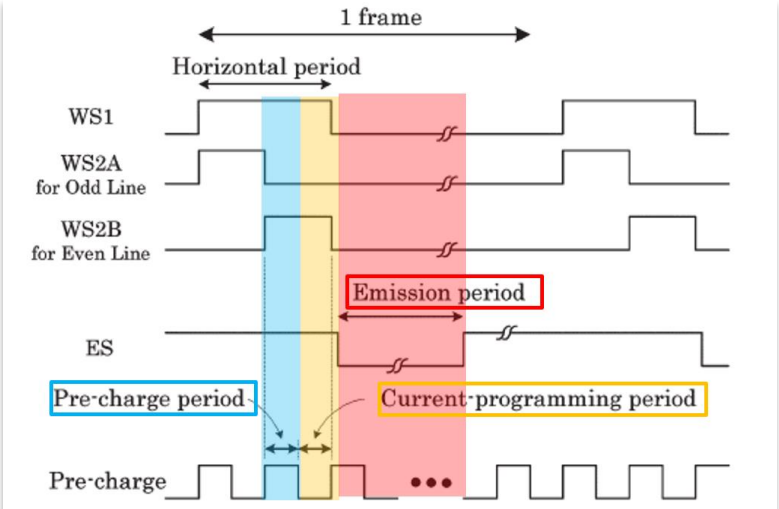


FIGURE 7 — Timing chart illustrating current data driver and pixel circuit operations. The signals Write scan1 (WS1), Write scan 2A/B (WS2A/B), and Erase scan (ES) are output by an integrated gate driver.

Id., Fig. 7 (annotated). Shimoda describes operation during the pre-charge period:

> In the pre-charge period, T2 and T3 are turned on, T4 is turned off, and current from the current source flows into T1. A voltage-follower amplifier outputs the gate voltage of T1 into the gate electrode of T5, with T6 and T7 turned on. This pre-charge function rapidly pre-charges the voltage in the gate electrode of T5 so that a current roughly equivalent to the value of the current source flows through T5.

Id., §3.2; Ex. 1002, ¶119. This operation mode is shown in annotated Figure 6, with a red × placed over transistor lines that are turned off.

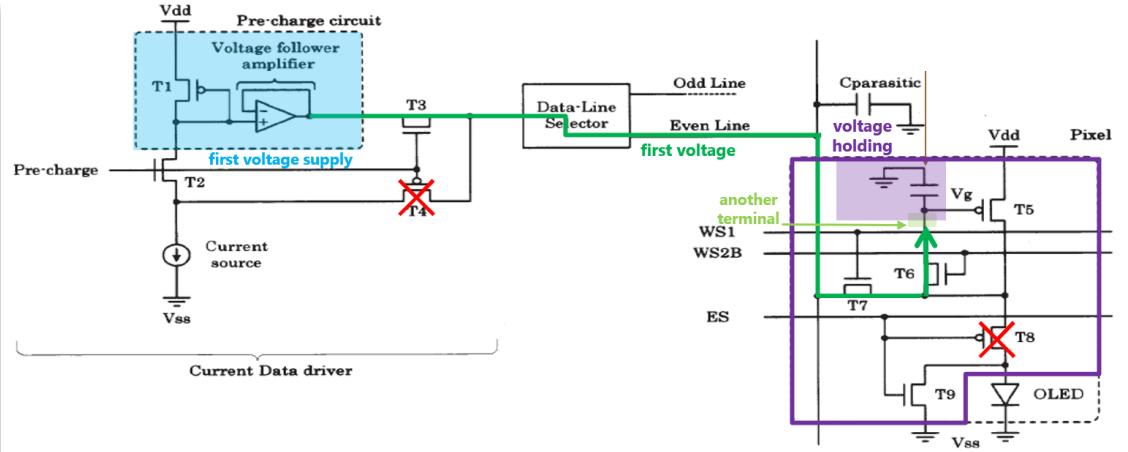


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

During the pre-charge period, a gate capacitor (annotated solid purple) in each pixel circuit ("current output circuits," within purple box) receives a first voltage (annotated dark green) from the pre-charge circuit ("first voltage supply source," annotated blue). Ex. 1002, ¶120.

During the pre-charge period, the first voltage from the pre-charge circuit is also supplied to "another terminal" (annotated light green) of the voltage holding circuit (annotated solid purple). In the pre-charge period, the gate capacitor is connected to the pre-charge circuit and is supplied by the first voltage. *Id.*, §3.2. Therefore, during the pre-charge period, the output of the pre-charge circuit is supplied to the lower terminal of the gate capacitor (annotated light green). *Id.* "This pre-charge function rapidly pre-charges the voltage in the gate electrode of T5 so

that a current roughly equivalent to the value of the current source flows through T5." *Id.* This analysis is consistent with the description of these elements in the '047 Patent, in which the voltage holding capacitor is connected to the voltage supply source during the voltage supply mode. Ex. 1001, 7:44-52; Ex. 1002, ¶¶121-122.

i. <u>1(g): "under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and"</u>

Shimoda discloses this limitation, providing operation under a current supply mode (e.g., during a current-programming period).

i. "under said current supply mode, each of said current output circuits receives said first current from said first current supply source"

The current-programming period is annotated gold in Figure 7.

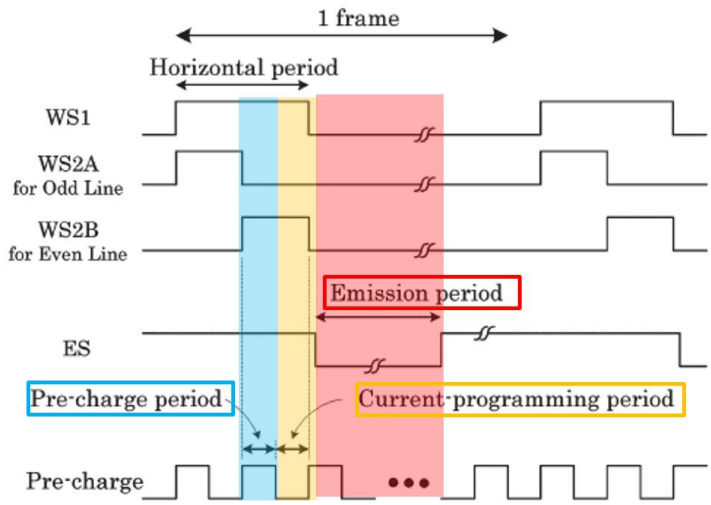


FIGURE 7 — Timing chart illustrating current data driver and pixel circuit operations. The signals Write scan1 (WS1), Write scan 2A/B (WS2A/B), and Erase scan (ES) are output by an integrated gate driver.

Ex. 1004, Fig. 7 (annotated). As shown in annotated Figure 6 below (including a red × over lines that are turned off), during the current-programming period: transistors T2 and T3 are turned off, disconnecting the pre-charge circuit; transistor T4 is turned on, connecting the current source (annotated gold) to the pixel circuit (annotated purple); transistors T7 and T6 remain turned on, connecting the current source to the gate capacitor. Thus, the first electric current (annotated red) from the current source (gold) is supplied to current output circuit (purple). *See*, Ex. 1004, at §3.2 ("the current from the current source is directly supplied to the pixel circuit.").

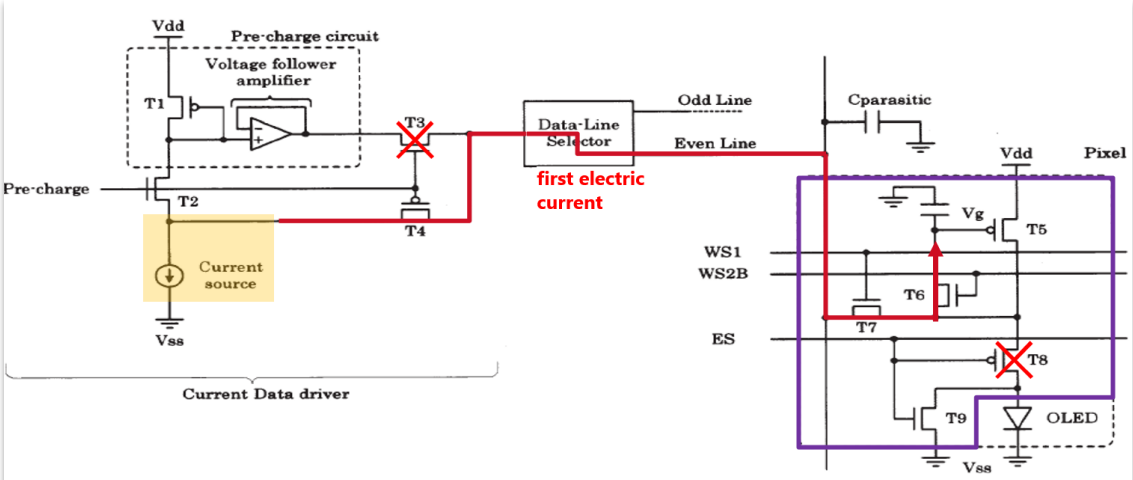


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

Ex. 1004, Fig. 6 (annotated); Ex. 1002, ¶¶123-125.

ii. "generates a second voltage by said current-voltage converting circuit"

During the current-programming period, a voltage (i.e., the claimed second voltage) is generated at the gate of transistor T5 and stored in the gate capacitor. During the current-programming period, a reference current from the current source (i.e., first electric current) continues to charge the capacitor after the capacitor was previously partially charged by the first voltage (during the pre-charge period). Ex. 1004, §3.2, Fig. 8(a). By the end of the current-programming period, the second voltage reaches a level where the transistor T5 outputs a current equivalent to the value of the first electric current. *Id*. Shimoda further explains the difference between the first voltage (during pre-charge period) and the second voltage (during

current-programming period) may exist because of "variations in characteristics between T1 and T5." *See*, Ex. 1004, at §3.2.

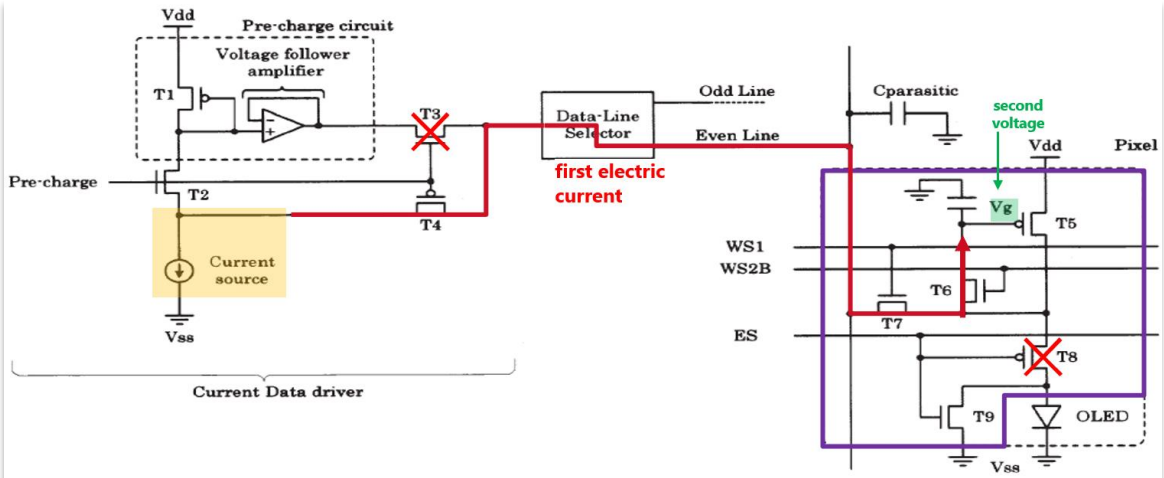


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

Ex. 1004, Fig. 6 (annotated); Ex. 1002, ¶¶126-127.

iii. "the first current is supplied to said another terminal of said voltage holding circuit"

The first current (annotated red) from the current source (annotated gold) is supplied to "another terminal" (annotated light green) and to the gate capacitor (purple). Ex. 1004, §3.1, Fig. 6.

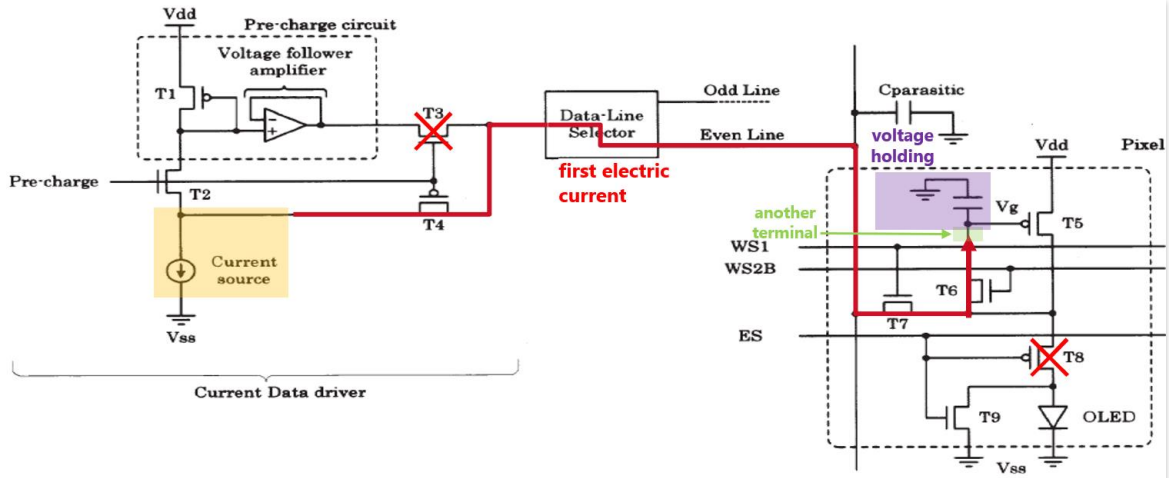
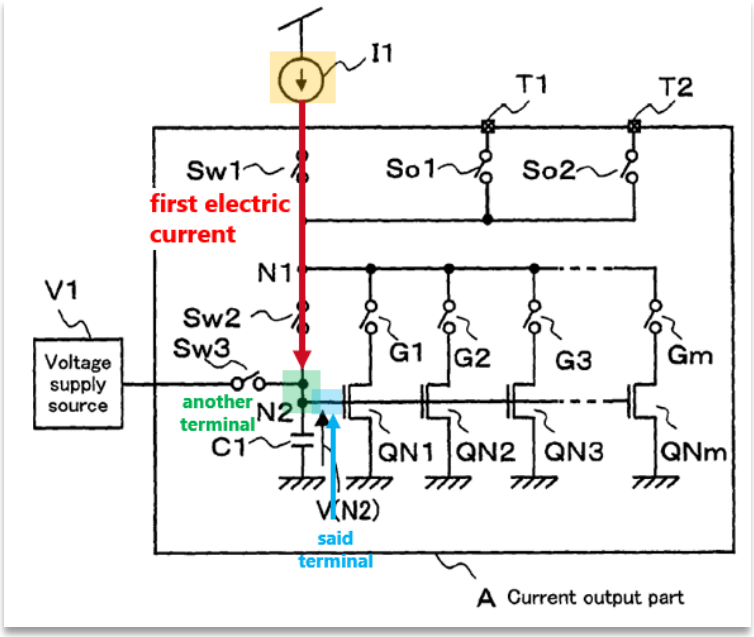


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

Ex. 1004, Fig. 6 (annotated). This analysis is consistent with the description of these elements in the ’047 Patent, where the first current is supplied to the second terminal of the voltage holding capacitor in a similar manner as Shimoda. Figure 1 of the ’047 Patent is annotated to show that a first electric current is supplied to the marked “another terminal” of the voltage holding capacitor.



Ex. 1001, Fig. 1A (annotated), 8:1-15; Ex. 1002, ¶¶128-129.

j. <u>1(h): "under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit."</u>

Shimoda discloses operation under a current output mode (emission period). The emission period (annotated red) is when the pixel circuit outputs a current to a corresponding OLED.

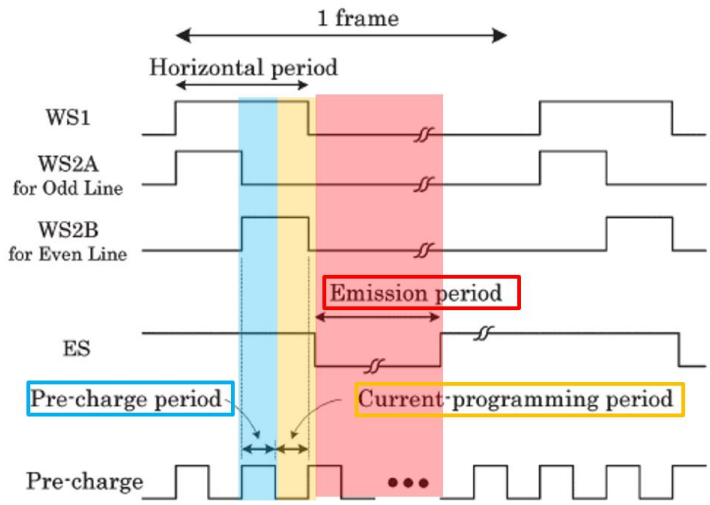
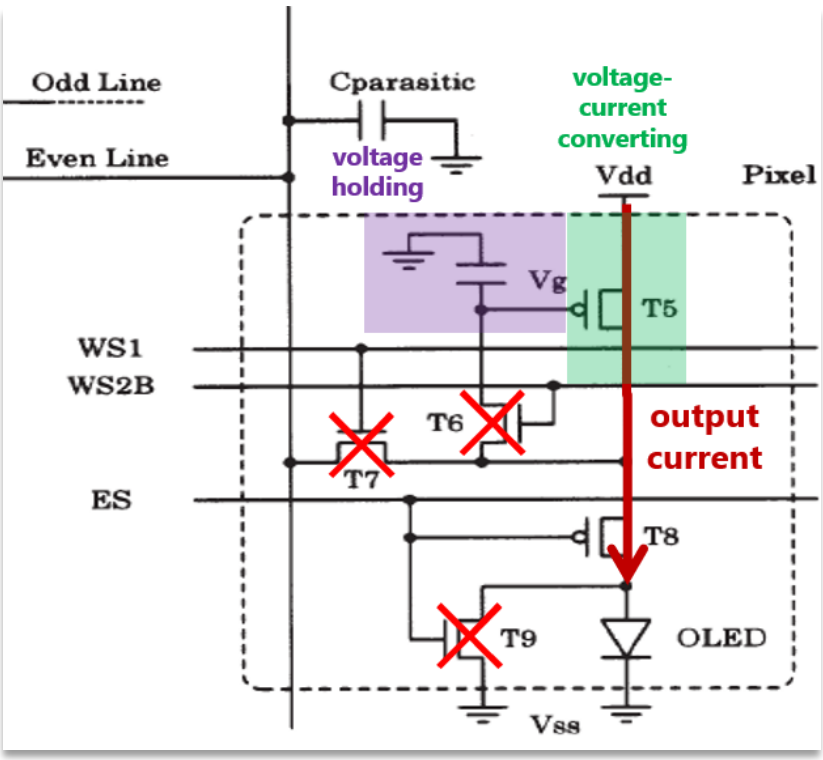


FIGURE 7 — Timing chart illustrating current data driver and pixel circuit operations. The signals Write scan1 (WS1), Write scan 2A/B (WS2A/B), and Erase scan (ES) are output by an integrated gate driver.

Ex. 1004, Fig. 7 (annotated). During emission period, "T6 and T7 are turned off, T8 is turned on, and a current programmed by the data driver is supplied to the OLED." *Id.*, §3.2. This operation is shown below, with a red × placed over transistor lines that are turned off.



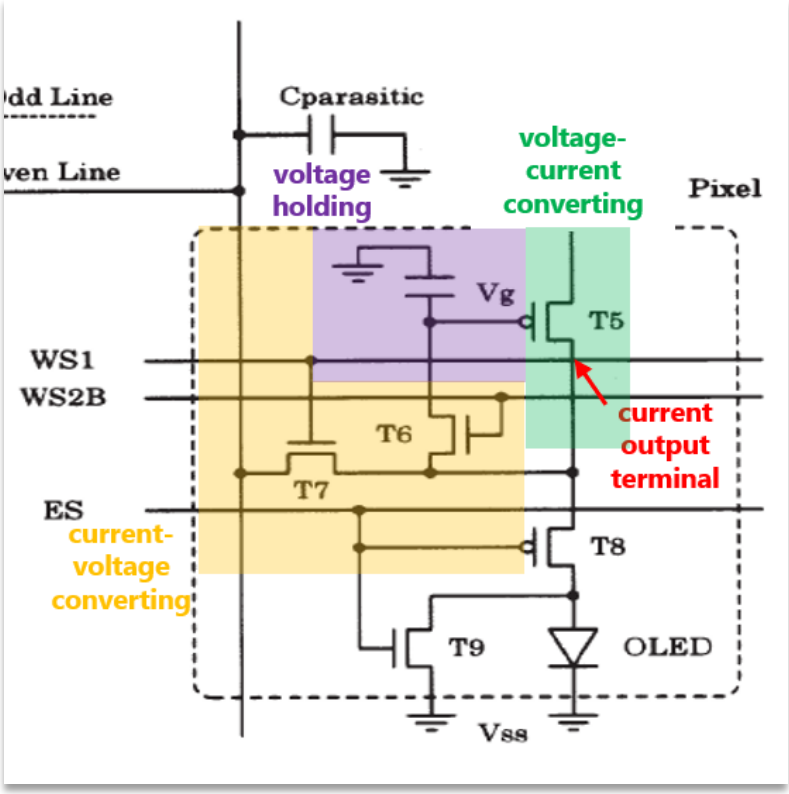
Ex. 1004, Fig. 6 (annotated and excerpted). Turning off transistors T7 and T6 disconnects the pre-charge circuit and the current source from the gate capacitor. The voltage held at the gate capacitor is then supplied to the gate electrode of transistor T5. Consistent with one of the fundamental properties of transistors, transistor T5 outputs a current according to its gate voltage. Thus, during the emission period, the transistor T5 (annotated green) outputs an output current (annotated dark red) according to the voltage held in the gate capacitor (annotated purple). Ex. 1002, ¶130.

B. <u>CLAIM 2</u>

Shimoda discloses, or at least renders obvious, this claim.

> **"The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits"**

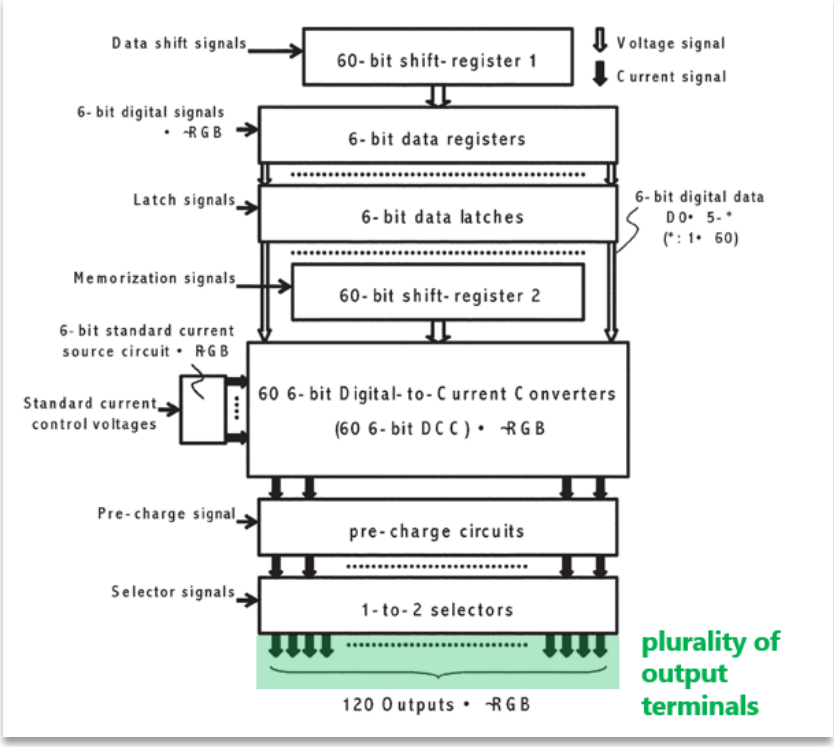
As described above for Claim Limitations 1(d)(1) and 1(d)(2), each pixel circuit is an example of a current output circuit, and a POSITA would have recognized (or at least it would have been obvious) that there would be a plurality of such pixel circuits present. And as described for Claim Limitation 1(d)(2), the drain terminal (annotated red) of transistor T5 is a current output terminal.



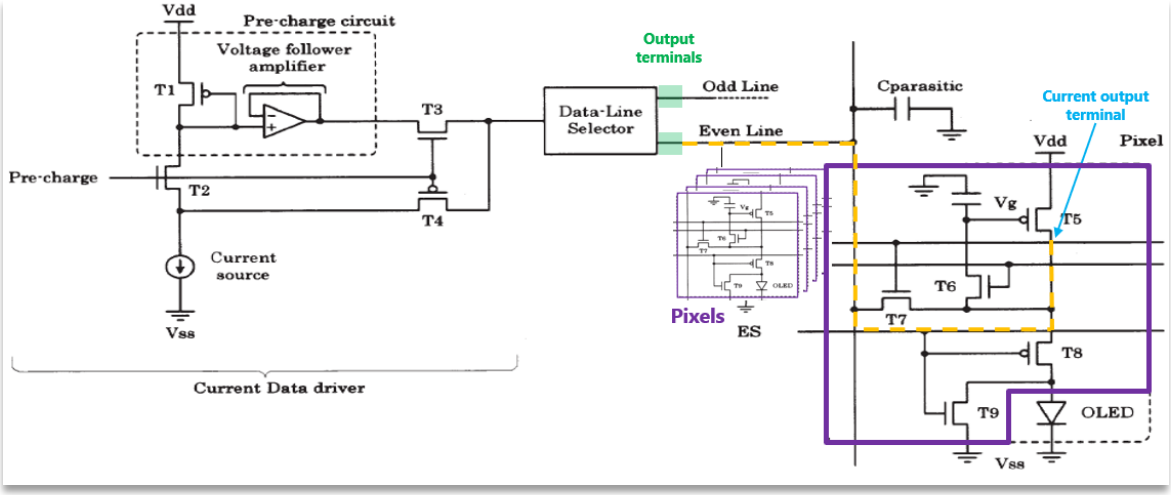
Ex. 1004, Fig. 6 (annotated and excerpted); Ex. 1002, ¶¶131-132.

As described above for Claim Limitation 1(c), Shimoda provides at least two examples of structure that constitutes a plurality of output terminals. Under either example, Shimoda discloses "each of said output terminals is connected to said current output terminals." Ex. 1002, ¶132.

First, the "120 Outputs" in Figure 1 (annotated green) are an example of the claimed output terminals.



Ex. 1004, Fig. 1. Each such output terminal (annotated green) is connected to the drain terminal of transistor T5 (the claimed current output terminal, annotated blue) through a path (annotated yellow):



Ex. 1004, Fig. 6 (annotated). The figure has been annotated to add multiple pixel circuits (purple), for the reasons disclosed in Claim Limitation 1(d)(1). The "Odd Line" and "Even Line" are each connected with multiple pixels. Shimoda explains that a display using the current data drivers and pixel circuits would include a pixel count of "120×RGB×136." Ex. 1004, §5 (Table 1).

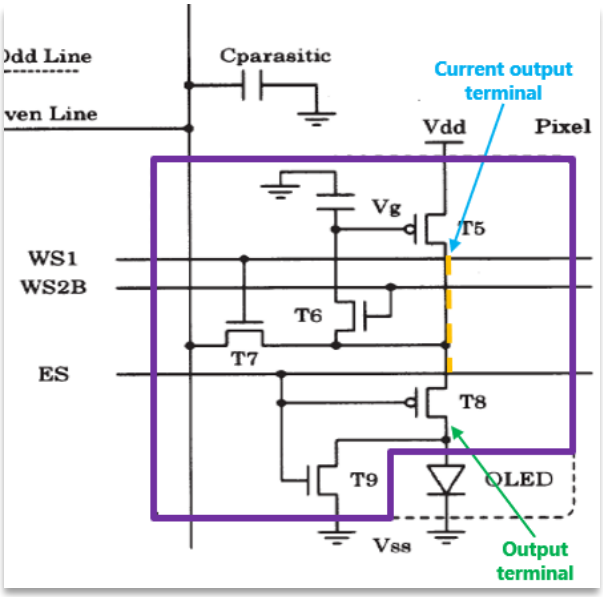
TABLE 1 — Display specifications.

Display size	1.9 in.
Pixel count	120 × RGB × 136
Pixel pitch	96 ppi
Peak luminance	>150 cd/m^2
Input data	Digital 6 bit × RGB
Input level	3 V I/F
Integrated circuits	Current data driver
	Gate driver
	Level shifter

Ex. 1004, at Table 1 (annotated). Thus, the display in Shimoda would include an array of 120×136 pixels, and each line would be connected to 136 pixels. Therefore,

each output terminal is connected to a plurality of drain terminals of T5 (the claimed "current output terminals") provided to current output circuits (the claimed "current output circuits"). Ex. 1002, ¶¶133-135.

Second, the drain terminals of transistor T8 in each pixel circuit are another example of output terminals. Ex. 1004, §3.2. The drain terminal of transistor T8 (annotated green) is connected (through the annotated yellow path) to the drain terminal of transistor T5 ("current output terminals," annotated blue) provided to pixel circuits ("current output circuits," annotated purple).

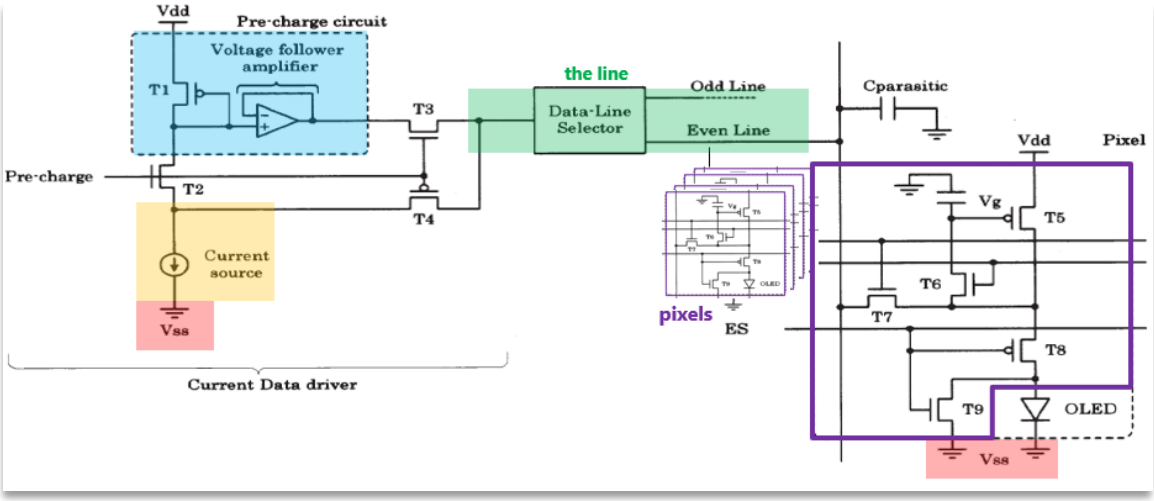


Ex. 1004, Fig. 6 (annotated and excerpted); Ex. 1002, ¶136.

"each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common."

Shimoda discloses this limitation or at least renders it obvious. As indicated in the annotated Fig. 6 below, each of the pixel circuits share Vss in common (annotated red). In addition, each pixel circuit is interposed on an even line (or an odd line), and a POSITA would have recognized (or at least it would have been obvious) that each line (whether even or odd) provides an equal voltage for all pixels interposed on that line. A POSITA would have known that a line in a circuit is equivalent to a common node for the purpose of analyzing parallel or series connection. Thus, all pixel circuits on an even line (or all pixels on an odd line) share two common terminals—the line (annotated green) and Vss (annotated red)—and are thus in parallel with one another. Ex. 1002, ¶137.

The pre-charge circuit (voltage supply source) and the current supply source are also interposed between the even line (or the odd line) and Vss. Ex. 1004, §3.1, Fig. 6. A POSITA would have recognized that the data-line selector comprises a collection switches between the even line and odd line. Whether an even line or an odd line is selected, the current supply, pre-charge circuit, and the pixels of even line or odd line (respectively) share a common node (e.g. the even or odd line).



Ex. 1004, Fig. 6 (annotated). Therefore, the current-output circuits are connected in parallel to the current supply and the first voltage supply source. Ex. 1002, ¶138.

C. <u>CLAIM 3</u>

> **"The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode."**

Shimoda discloses this claim. As discussed above for Claim Limitation 1(d)(2), within each pixel circuit, a current-voltage converting circuit includes an input terminal connected to the current supply source, transistors T6-T7, and gate capacitor.

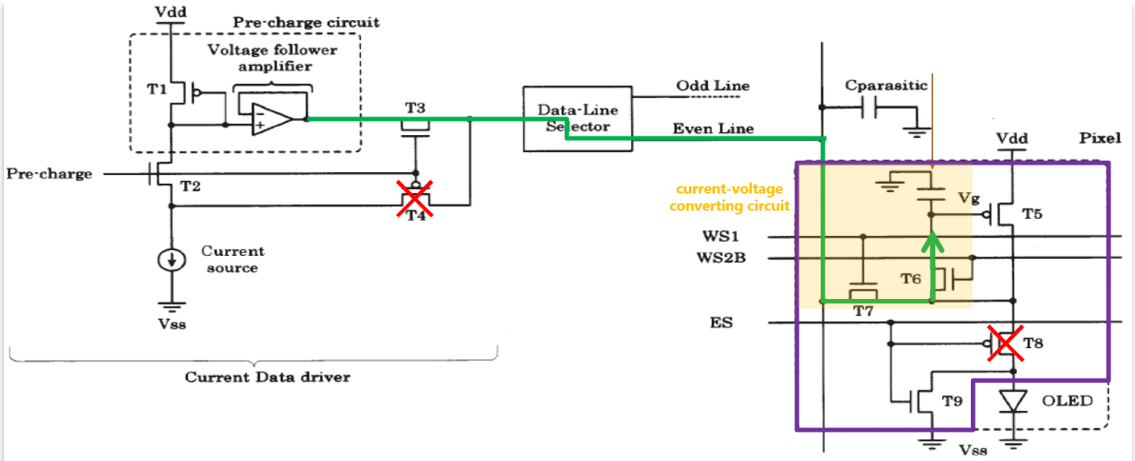


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

Ex. 1004, Fig. 6 (annotated, including with). During the pre-charge period (voltage-supply mode), all components of the current-voltage converting circuit (annotated gold) are set to a conductive state. *See*, Ex. 1004, §3.2. As shown above, the current-voltage converting circuit is annotated gold, with a red × placed over transistor lines that are turned off and a green arrow indicating that a voltage being supplied to the gate capacitor. Ex. 1002, ¶139.

D. <u>CLAIM 4</u>

> **"The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode."**

Shimoda discloses, or at least renders obvious, this limitation. During the pre-charge period (voltage supply mode), the current-voltage converting circuit is stopped from converting a current into a gate voltage for the gate capacitor. This occurs because the current supply source is disconnected from the gate capacitor (by

transistor T4 being turned off), and a voltage from the pre-charge circuit is supplied directly to the gate capacitor. Ex. 1004, §3.2. The current-voltage converting circuit (annotated gold) is shown below, with a red × placed over transistor lines that are turned off and a green arrow indicating a voltage supplied to the gate capacitor.

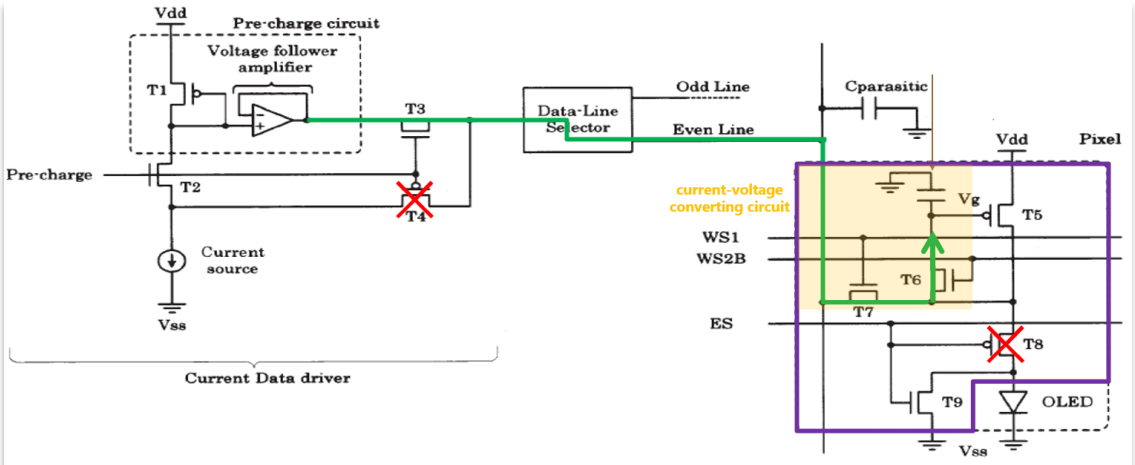


FIGURE 6 — The schematic diagram of both the pixel circuit and the current data driver with the pre-charge circuit.

Ex. 1004, Fig. 6 (annotated); Ex. 1002, ¶140.

E. CLAIM 9

> **"A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device."**

Shimoda discloses this limitation. AMOLED displays are examples of the claimed "current-driving-type display device." Ex. 1004, Abstract ("active-matrix organic light-emitting diode (AMOLED) displays"). Current data drivers are mounted on the displays, and the "brightness is dependent on the current in the OLED that is driven by each pixel circuit." *Id.*, §1. Thus, Shimoda "integrate[s]

high-accuracy current data drivers into the AMOLED display substrate itself." *Id.*; Ex. 1002 ¶141.

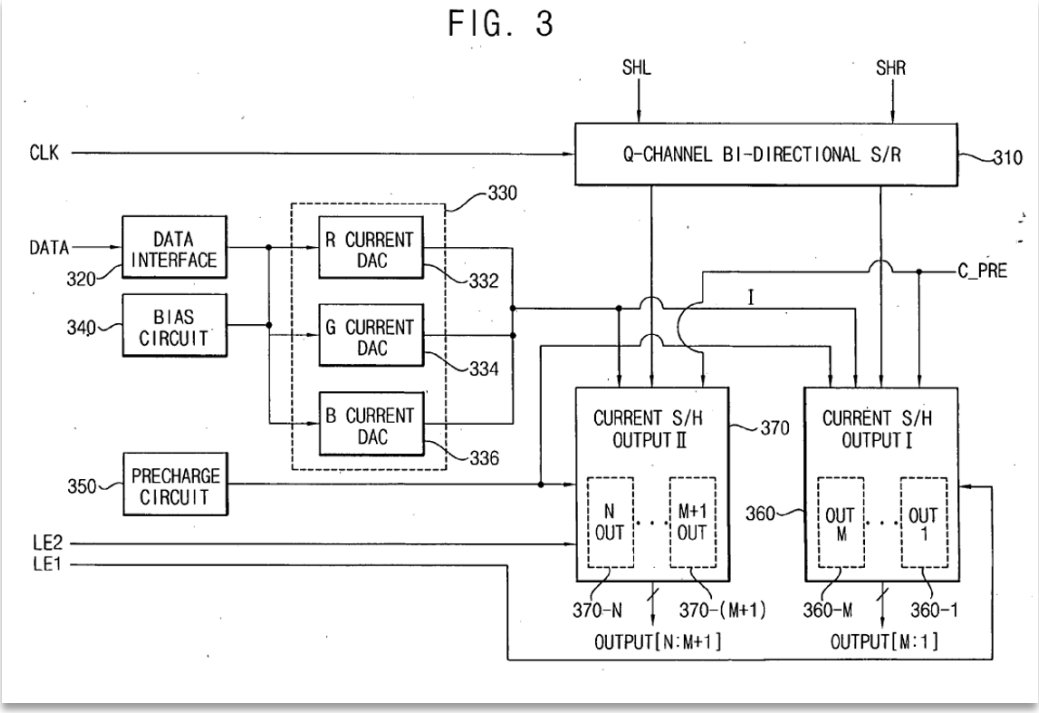
VIII. GROUNDS 3-4: BAEK

Claims 1-4 and 9 are anticipated by Baek (Ex. 1005), corresponding to Ground 3. They are also obvious for substantially similar reasons, as further explained below (Ground 4). *See Realtime*, 912 F.3d at 1373 ("anticipation is the epitome of obviousness"); Ex. 1002, ¶142.

A. CLAIM 1

a. 1(preamble): "A current driving device, comprising:"

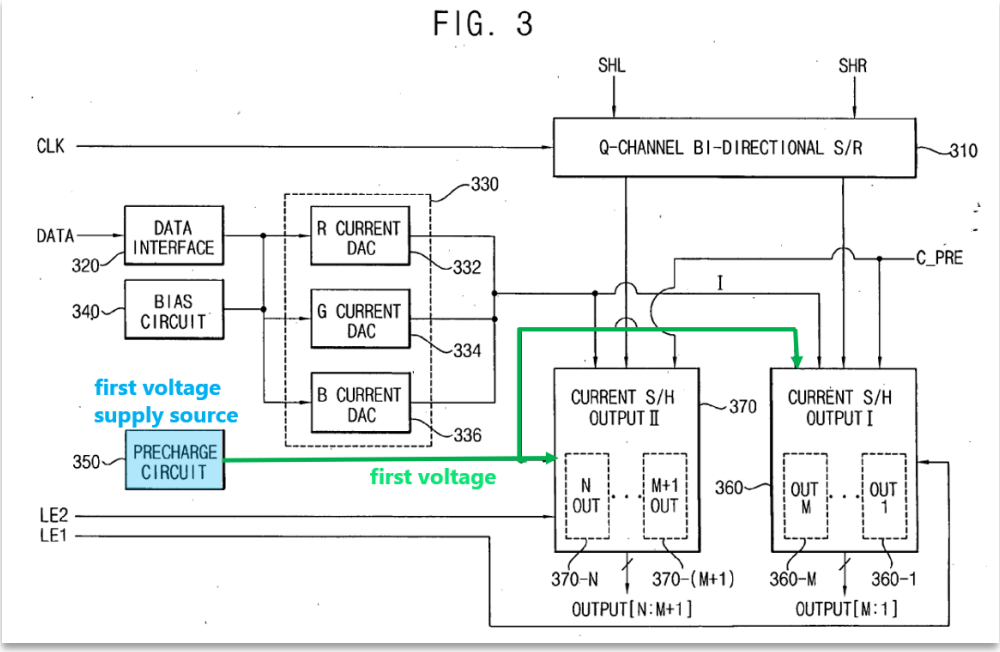
To the extent the preamble is limiting, Baek discloses it. The "display driver circuit" of Baek is an example of the claimed "current driving device." "FIG. 3 is a block diagram illustrating a block driver circuit …." Ex. 1005, ¶[0026].



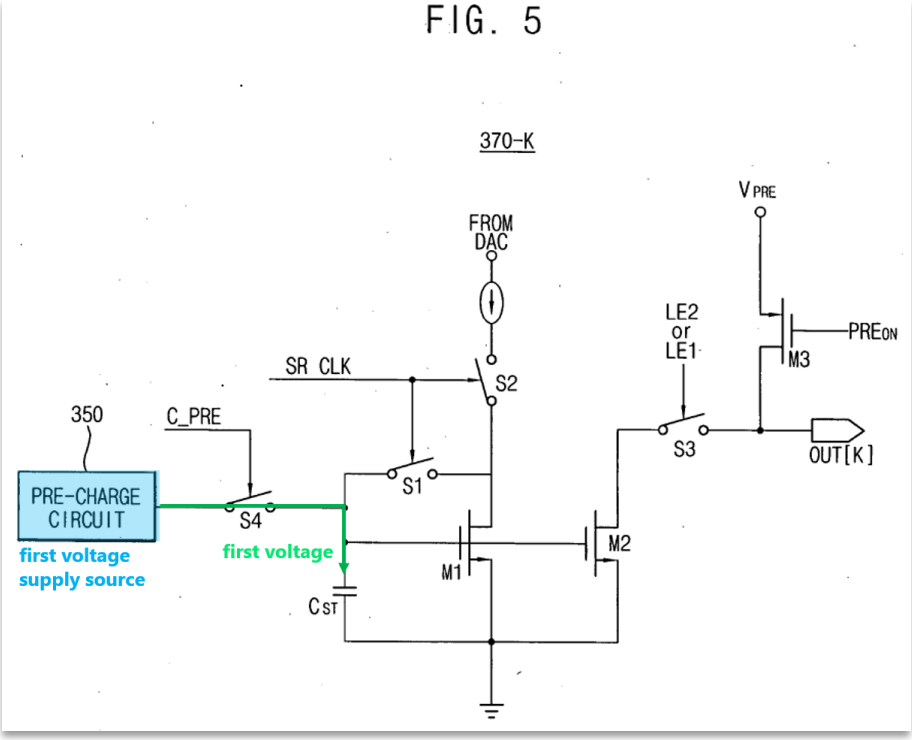
Id., Fig. 3; *see* ¶[0036] (describing circuitry within "display driver circuit"); Ex. 1002, ¶143.

b. <u>1(a): "a first voltage supply source for supplying a first voltage;"</u>

Baek discloses this limitation. The "pre-charge circuit" (annotated blue) in Baek is an example of the claimed "a first voltage supply source," and it supplies a first voltage (annotated green). These are illustrated in Figure 3 (showing the "display driver circuit") and Figure 5 (providing an expanded view of the sample/hold circuit of Figure 3). *Id.* ¶¶[0026], [0028], [0055].



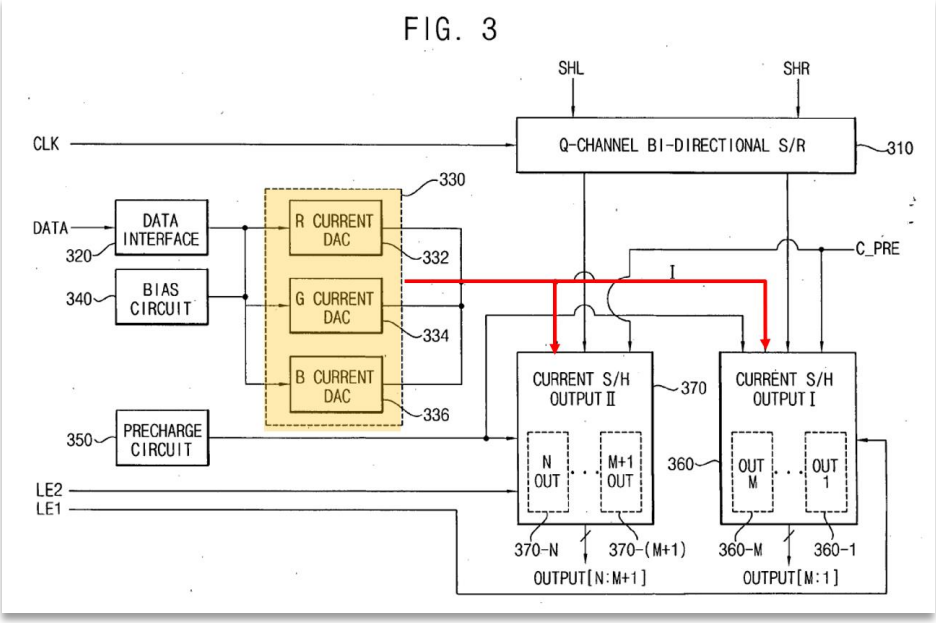
Ex. 1005, Fig. 3 (annotated).



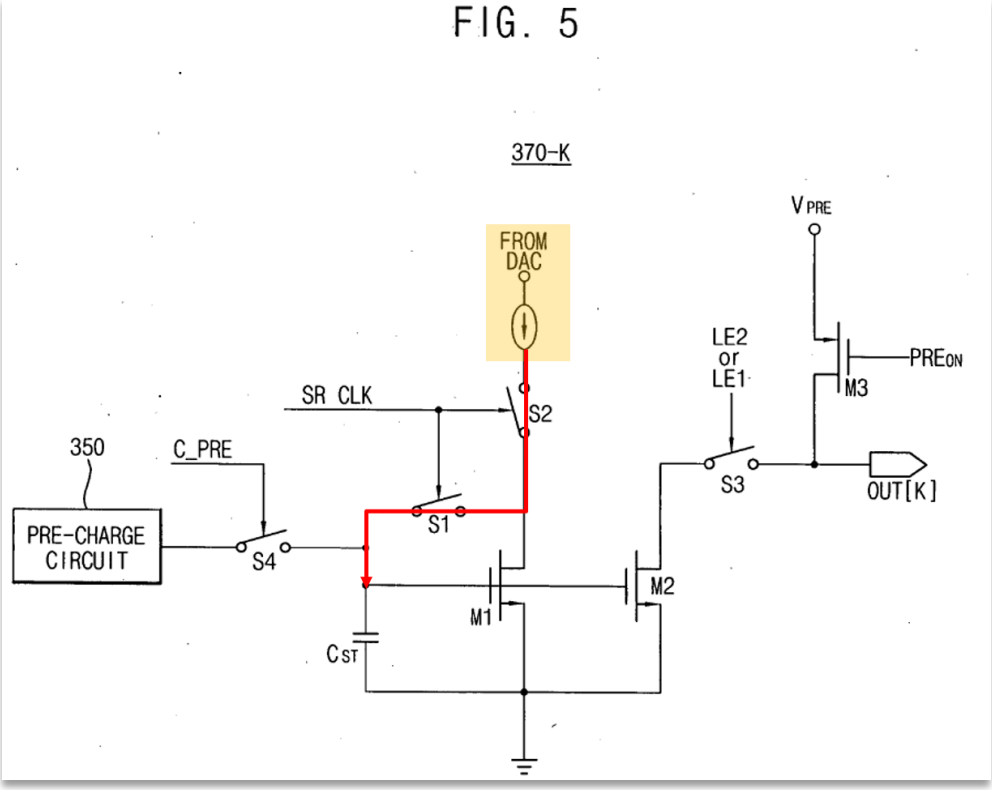
Ex. 1005, Fig. 5 (annotated). The "pre-charge circuit 350" is a component of the "display driver circuit" discussed above. Ex. 1005, ¶[0036]. The pre-charge circuit supplies a first voltage "pre-charge a voltage of the storage capacitor CST." Ex. 1002, ¶144.

c. <u>1(b): "a first current supply source for supplying a first electric current;"</u>

Baek discloses this limitation. Baek discloses the claimed current source (annotated gold) and the lines (annotated red) along which flow the first electric current supplied by that current source.



Ex. 1005, Fig. 3 (annotated).



Ex. 1005, Fig. 5 (annotated). The current digital-to-analog conversion unit 330 ("DAC") in Baek is an example of the claimed "a first current supply source" and is a component of the display driver circuit. *Id.*, ¶[0036]. The current DAC 330 "convert[s] gray-scale data provided from the data interface circuit 320 to an analog gray-scale current based on the gamma reference signal." *Id.*, ¶[0044]. As shown in Figure 5, this analog gray-scale current (first electric current) is supplied to each sample/hold output circuit ("Current S/H Output"); Ex. 1002, ¶¶145-146.

d. 1(c): "a plurality of output terminals;"

Beak discloses limitation. The output terminals OUT[1]-OUT[N] are an example of the claimed "a plurality of output terminals," and Baek even refers to each of them as an "output terminal."

> The output terminal OUT[K] may be used to drive a display panel (not shown) using a smaller current.[5]

Ex. 1005, ¶[0063]. The output terminals are annotated green in Figures 3 and 5 (annotated below).

---

[5] The "OUT[1]-OUT[N]" notation in Baek is shorthand for a multitude of output terminals (terminal 1, terminal 2, terminal 3, … terminal N) that are spread across current sample/hold circuits 360 and 370. Baek refers to an individual terminal as OUT[K]. Thus, the [1-N] notation in Figure 3 represents a series of terminals, and the [K] notation in Figure 5 represents an individual terminal. Ex. 1002, ¶¶147-148.

FIG. 3

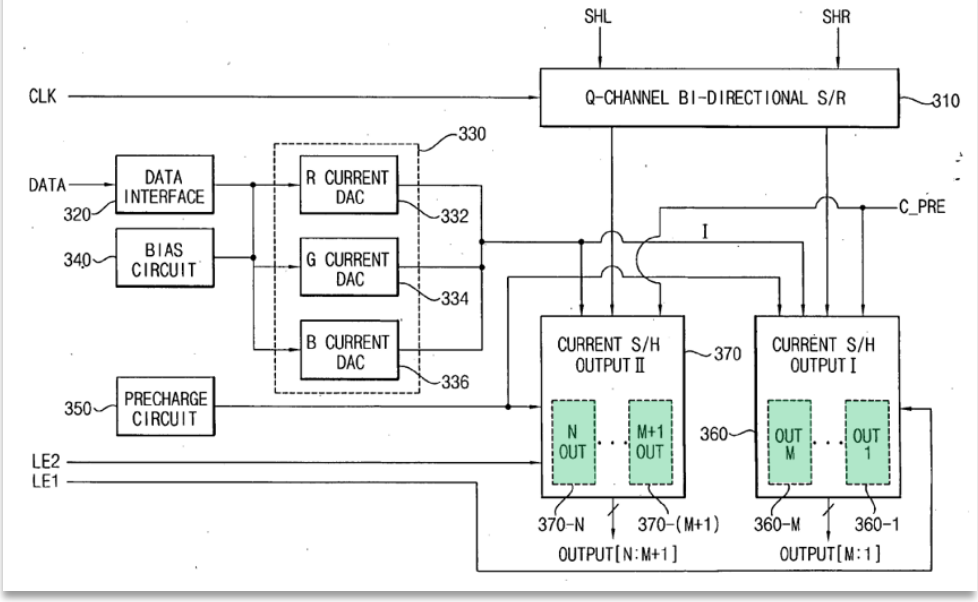
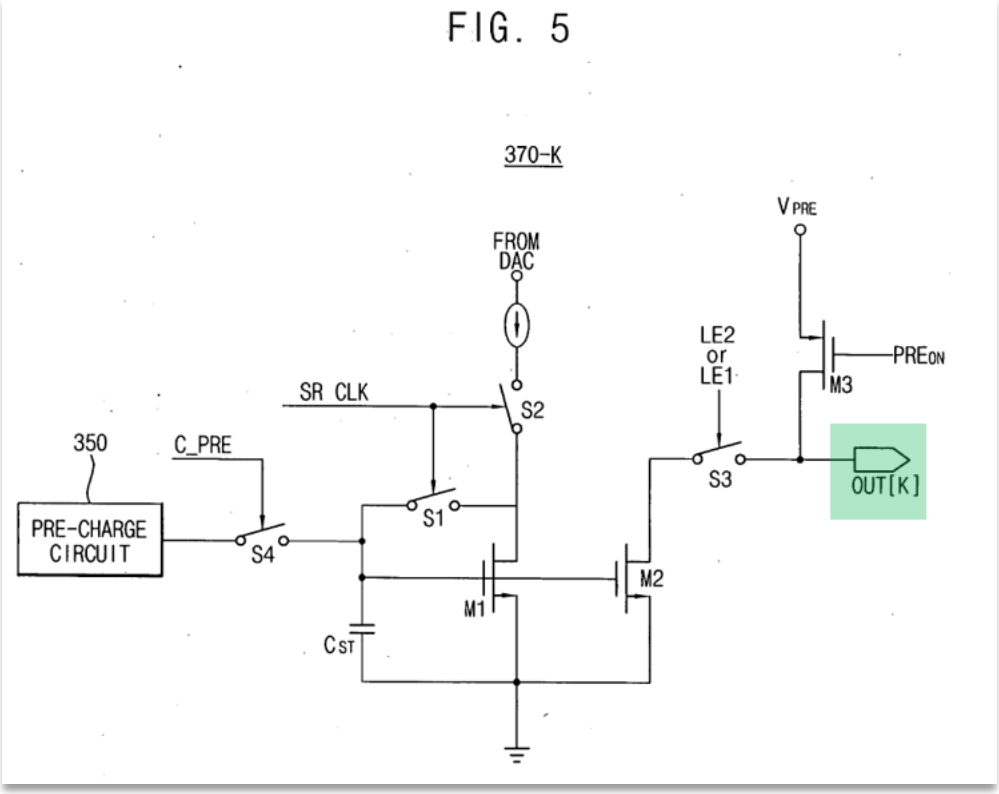

SHL
SHR
CLK
Q-CHANNEL BI-DIRECTIONAL S/R
310
330
DATA
DATA INTERFACE
320
R CURRENT DAC
332
C_PRE
I
340
BIAS CIRCUIT
G CURRENT DAC
334
B CURRENT DAC
336
CURRENT S/H OUTPUT II
370
CURRENT S/H OUTPUT I
350
PRECHARGE CIRCUIT
N OUT
M+1 OUT
360
OUT M
OUT 1
LE2
LE1
370-N
370-(M+1)
360-M
360-1
OUTPUT[N:M+1]
OUTPUT[M:1]

FIG. 5


370-K
VPRE
FROM DAC
LE2 or LE1
PREON
M3
SR CLK
S2
350
C_PRE
S3
OUT[K]
PRE-CHARGE CIRCUIT
S4
S1
M2
M1
CST

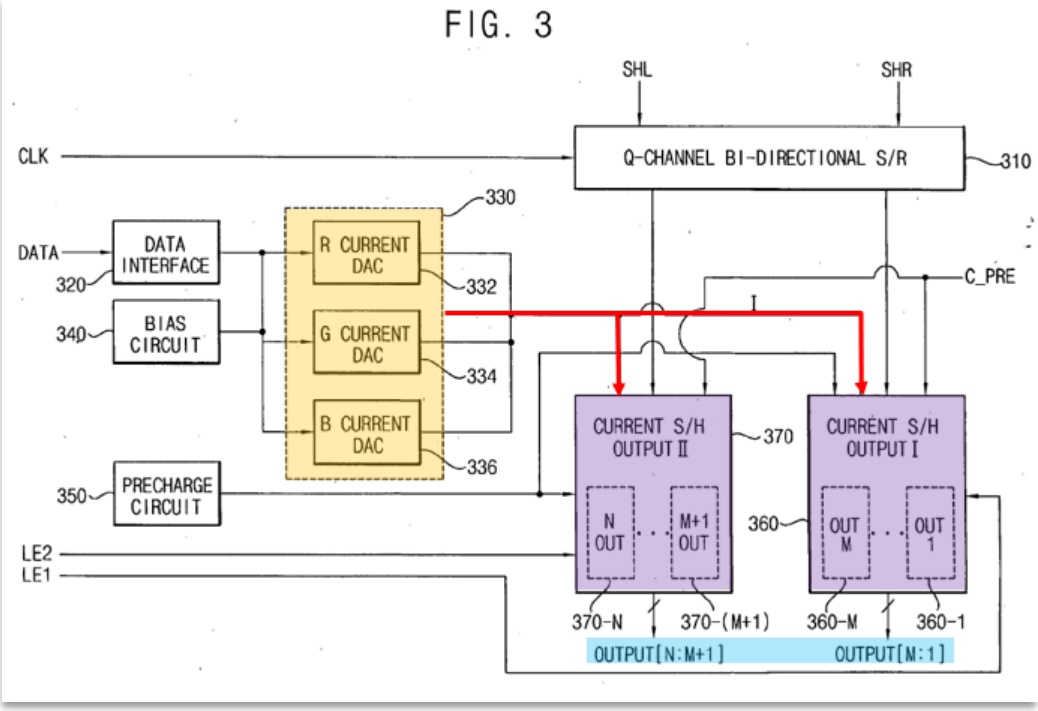
In addition to referring to the series of terminals [1-N] as output terminals, Baek similarly refers to "OUT[K] as an "output terminal." *Id.*, ¶¶[0058], [0061]-[0062]; Ex. 1002, ¶¶147, 149.

Each output terminal is associated with a corresponding current sample/hold circuit. For example, output terminal OUT[K], one of the output terminals of OUT[1]-OUT[N], is associated with current sample/hold circuit 370-K. Each of output terminal (e.g. OUT[K]) provides an output signal (e.g., OUTPUT K) to a corresponding channel (e.g., channel K). As shown in Figure 3, current sample/hold output circuit 360 comprises a plurality of sample/hold circuits 360_1 through 360_M, and current sample/hold output circuit 370 comprises a plurality of sample/hold circuits 370_{M+1} through 370_N (identified as "370-(M+1)" through "370-N"). Thus, Baek refers to OUT[1] through OUT[N] to refer to the output terminals spread across current sample/hold circuit 360 and current sample/hold circuit 370. Ex. 1002, ¶¶148-149.

e. <u>1(d)(1): "and a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising"</u>

Baek discloses this limitation. Figure 3 of Baek shows current sample/hold output circuits 360 and 370 (the claimed "current output circuits," annotated purple),

the input analog gray-scale current (the claimed "first electric current," annotated red) and output signals (the claimed "outputting an electric current," annotated blue).



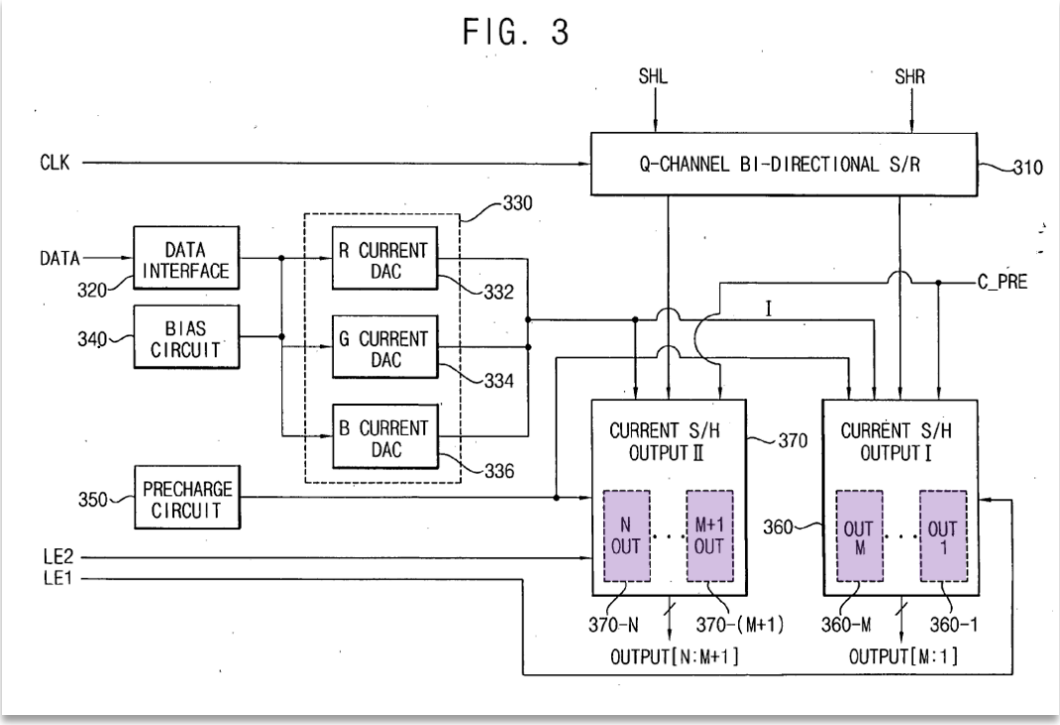
Ex. 1005, Fig. 3 (annotated), ¶[0036]; Ex. 1002, ¶150.

The current sample/hold output circuits 360 and 370 each output an electric current in accordance with said first electric current. Circuits 360 and 370 sample and hold an analog gray-scale current (the claimed "first electric current," as discussed above for Claim Limitation 1(b)). Circuit 360 provides "output signals OUTPUT 1 through OUTPUT M to the channels 1 through M," and circuit 370 outputs signals "M+1 through N." Ex. 1005, ¶¶[0045], [0048]. The electric output signals from circuits 360 and 370 are in accordance with the analog gray-scale current ("first electric current"). *See id.*, claim 1 (each "sample/hold output circuit"

is "configured to provide the sample/hold analog gray-scale signal to a plurality of … channels"); Ex. 1002, ¶¶151-152.

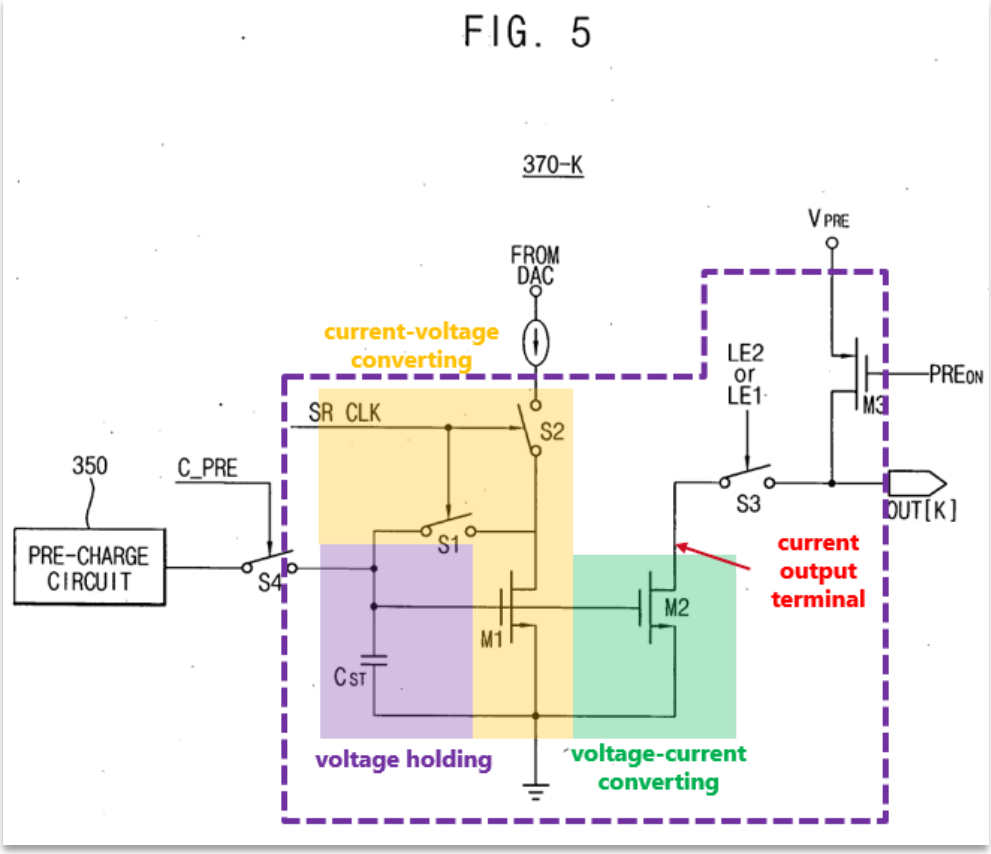
f. <u>1(d)(2) "a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein"</u>

Baek discloses this limitation. As shown in Figure 3, current sample/hold output circuit 360 comprises M current sample/hold circuits (360_1-360_M, annotated purple) and current sample/hold output circuit 370 comprises (N-M) current sample/hold circuits (370_{M+1}-370_N, annotated purple).



Ex. 1005, Fig. 3 (annotated). Figure 5 shows one such current sample/hold circuit 370_K, within the set of 360_1-360_M in Figure 3. *Id.*, ¶[0028]. Each current

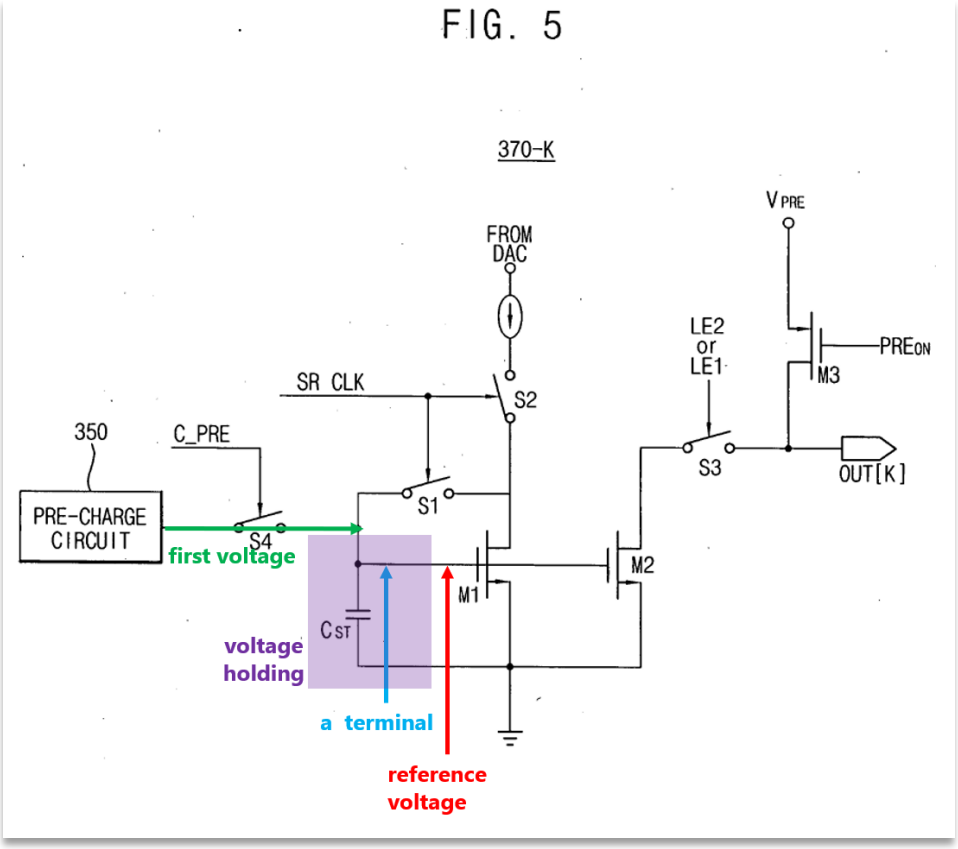
sample/hold circuit (such as current sample/hold circuit 370_K) includes within it a current-voltage converting circuit (annotated gold), voltage-current converting circuit (annotated green), voltage holding circuit (annotated purple), and current output terminal (annotated red).



Ex. 1005, Fig. 5 (annotated); Ex. 1002, ¶¶153-154.

i. "a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage"

The display driver circuit of Baek includes a voltage holding circuit (annotated purple), which further includes a storage holding capacitor CST.



Ex. 1005, Fig. 5 (annotated). The storage capacitor CST has a terminal (annotated blue) connected to the gate of transistor M1, which supplies a reference voltage (annotated red). The capacitor also has another terminal connected to pre-charge circuit 350, which supplies the first voltage (annotated green). Ex. 1002, ¶155.

The storage capacitor CST holds a voltage corresponding to the analog gray-scale current. Ex. 1005, ¶[0057]. A POSITA would have recognized that the analog gray-scale current is stored in the capacitor as a voltage, which is later applied to the gate of transistor M2. Ex. 1002, ¶156.

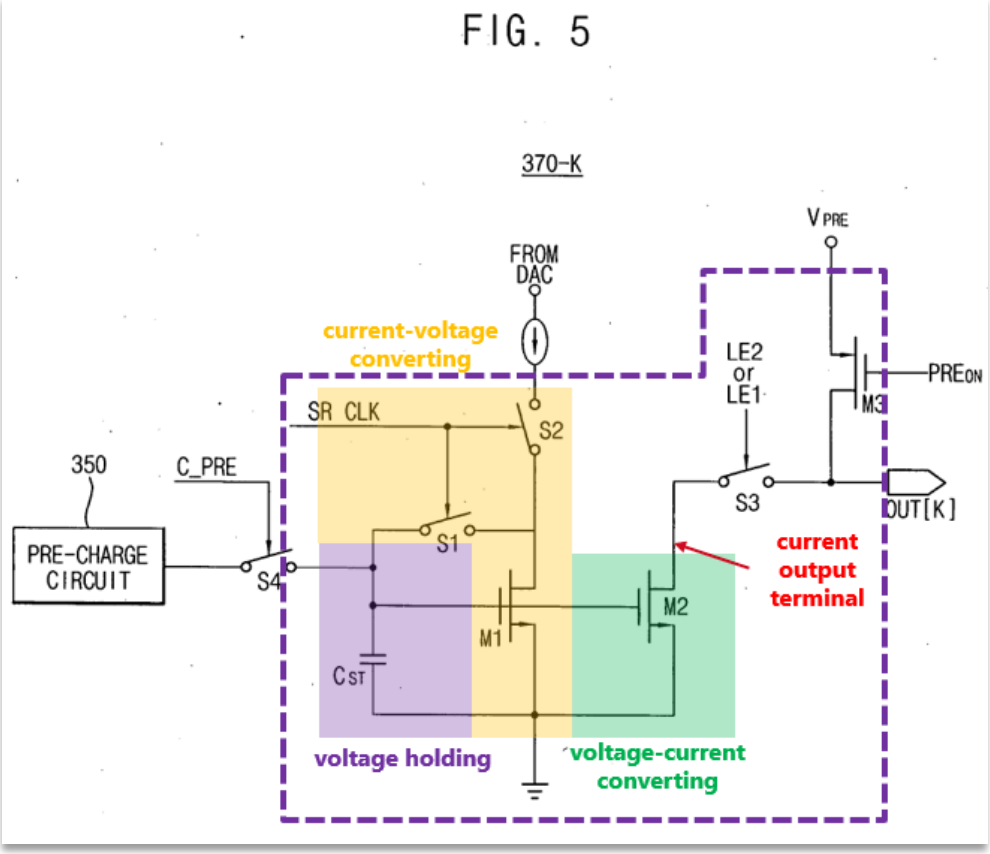
The storage capacitor CST is "coupled to the gate of the first transistor M1." Ex. 1005, ¶[0056]. The voltage at the gate of transistor M1 is an example of the claimed "reference voltage." As discussed further below, there are at least two charging modes in Baek: a pre-charge mode and a current charge mode. The voltage on the storage capacitor CST corresponds to the claimed "first voltage" during the pre-charge mode, and corresponds to the claimed "reference voltage" during the current charge mode. During the pre-charge mode, switches S1 and S2 are closed (i.e., current flows) and the first electric current is applied to the gate and drain of transistor M1. *Id.*, ¶[0056]. A POSITA would have recognized that, when a current is applied to a drain and a gate terminal of a transistor (such as transistor M1), the transistor behaves like a diode, accumulating a voltage at the gate and the drain of the transistor. This gate voltage on transistor M1 is thus an example of the claimed "reference voltage." Ex. 1002, ¶157.

The reference voltage is different than the first voltage provided by the pre-charge circuit. During the pre-charge period, the pre-charge circuit charges storage capacitor CST to "a voltage level slightly lower than a threshold voltage of the first transistor M1." Ex. 1005, ¶[0062]. During the current-charge period, current from DAC (the claimed "first electric current") continues charging the capacitor and thereby accumulates a different voltage at the gate of transistor M1 (the claimed "reference voltage"). Ex. 1005, ¶¶[0056], [0062]. Further, a POSITA would have

recognized that when current passes through M1, the gate voltage of transistor M1 is necessarily higher than its threshold voltage, because current starts flowing through transistors only when their gate voltage meets or exceeds their threshold voltage. Therefore, the reference voltage is different from the first voltage. Ex. 1002, ¶158.

ii. "a current-voltage converting circuit"

Each current sample/hold circuit includes a circuit comprising switches S1 and S2 and transistor M1, which are an example of the claimed "current-voltage converting circuit."

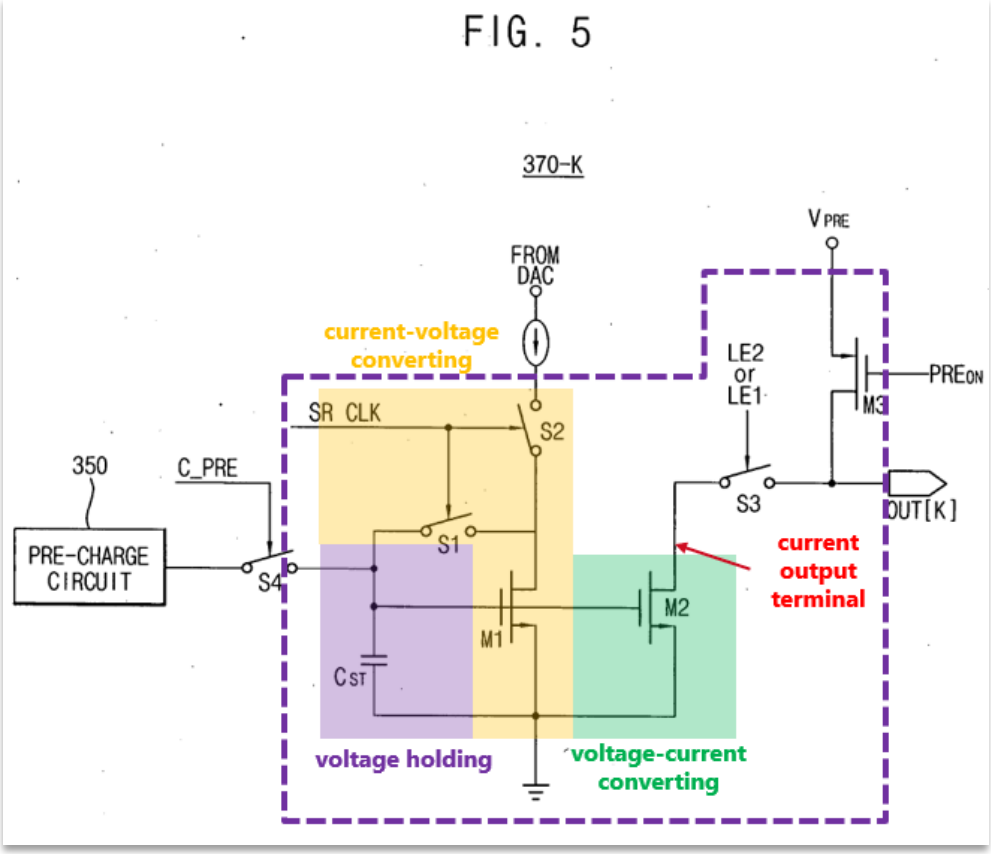


Ex. 1005, Fig. 5 (annotated). The current-voltage converting circuit connects the current DAC (the claimed "current source") to the storage capacitor CST and converts the first electric current into a voltage stored at the storage capacitor CST. During a pre-charge period, switches S1 and S2 are closed (current flows), a reference voltage is generated at the gate of transistor M1, and this voltage is stored in capacitor CST. *Id.*, ¶[0062]; ¶[0057] ("the analog gray-scale current may be held in the storage capacitor CST"); Ex. 1002, ¶159.

This analysis is consistent with the description of these elements in the '047 Patent, which under current-supply mode, "the current supply source" is connected "to the voltage holding capacitor C1 and current-voltage converting elements …." Ex. 1001, 8:61-64; 10:28-36; Fig. 1A. The reference voltage is provided at the gates of transistors QN1-QNm and held in the voltage holding capacitor C1. *Id.*, 8:3-11; Ex. 1002, ¶160.

iii. "a voltage-current converting circuit"

The circuit comprising transistor M2 is an example of the claimed "voltage-current converting circuit" (annotated green).



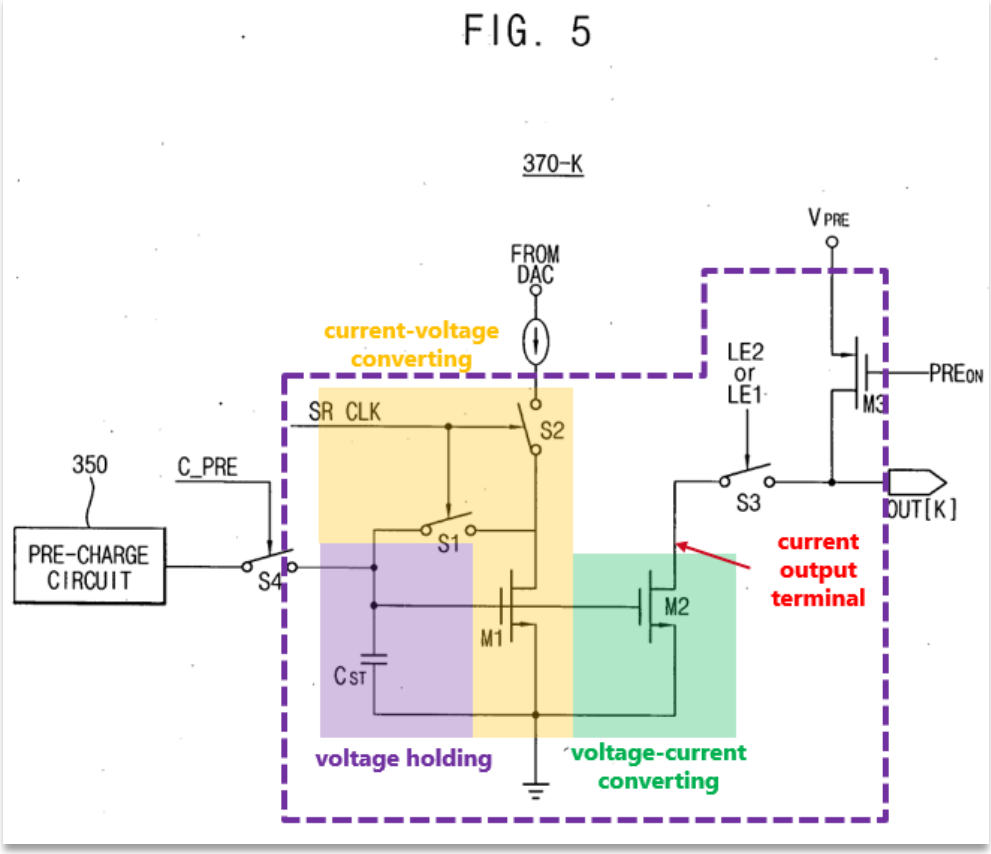
B

Ex. 1005, Fig. 5 (annotated). During current output period (when latch enable signals LE1 or LE2 are activated), switch S3 acts so that transistor M2 "may have its gate coupled to the storage capacitor CST [and] output the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current." *Id.*, ¶[0058]. Thus, a voltage held in storage capacitor CST is applied to the gate of transistor M2. A POSITA would have recognized that transistor M2 converts the voltage applied to its gate into a corresponding output current (between its drain and source), because a fundamental property of transistors is to output current based on their gate voltage. This analysis is consistent with the description

of these elements in the ’047 Patent, where the voltage-current converting function is performed in current output mode. Ex. 1001, 8:30-38; Ex. 1002, ¶¶161-162.

iv. “ at least one current output terminal”

Each current/sample hold circuit contains transistor M2. The drain terminal of transistor M2 in Baek is an example of the claimed “current output terminal.”

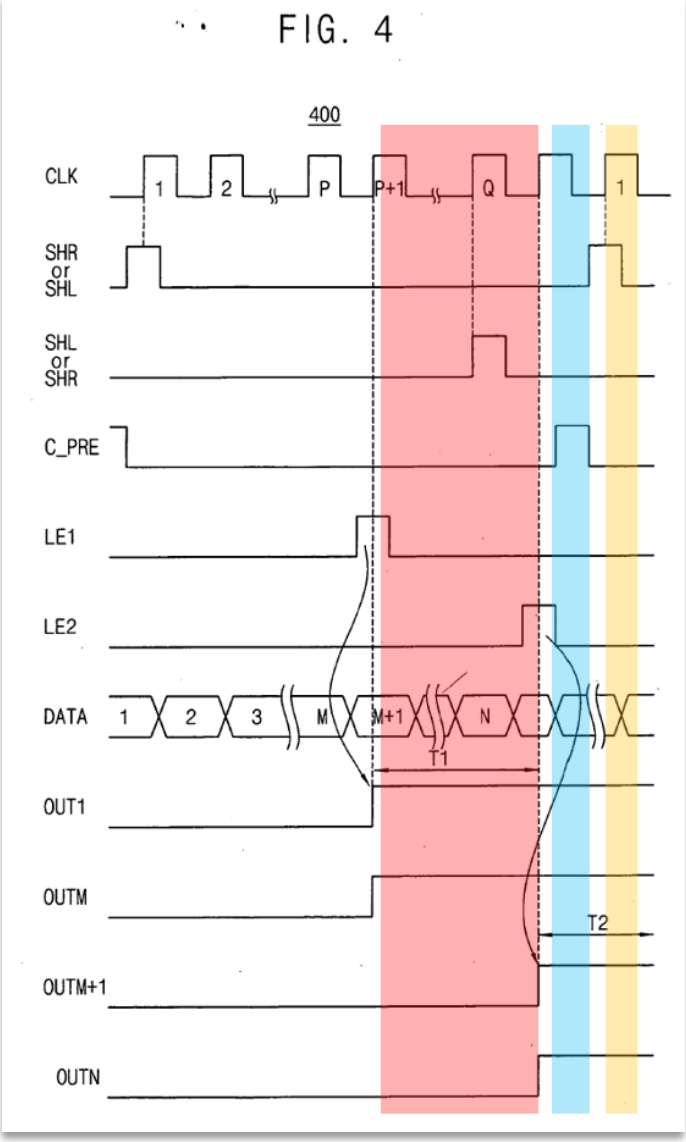


Ex. 1005, Fig. 5 (annotated). During current output period (when latch enable signals LE1 or LE2 are activated), switch S3 acts so that a current from the drain terminal of transistor M2 passes to the output terminal OUT[K]. *Id.*, ¶[0058]. This analysis is consistent with the description of these elements in the ’047 Patent, in

which during a current output mode a transistor (T2) includes a current output terminal. Ex. 1001, 8:30-33; Ex. 1002, ¶¶163-164.

g. <u>1(e): "each of said current output circuits operates in three operation modes including a voltage supply mode, a current supply mode, and a current output mode,"</u>

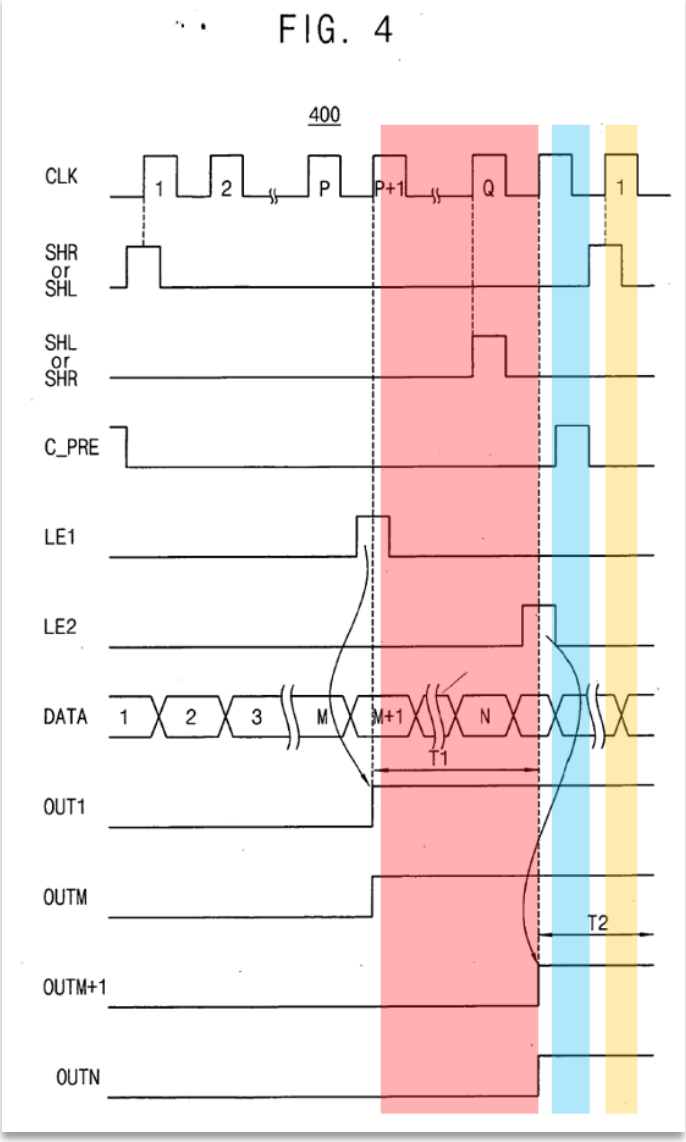
Baek discloses this limitation. Baek discloses applying a pre-charge signal to initiate the claimed "voltage supply mode" (annotated blue), applying a CLK signal to initiate the claimed "current supply mode" (annotated gold), and applying an OUT signal and a latch enable signal (LE1 or LE2) to initiate the claimed "current output mode" (annotated red).



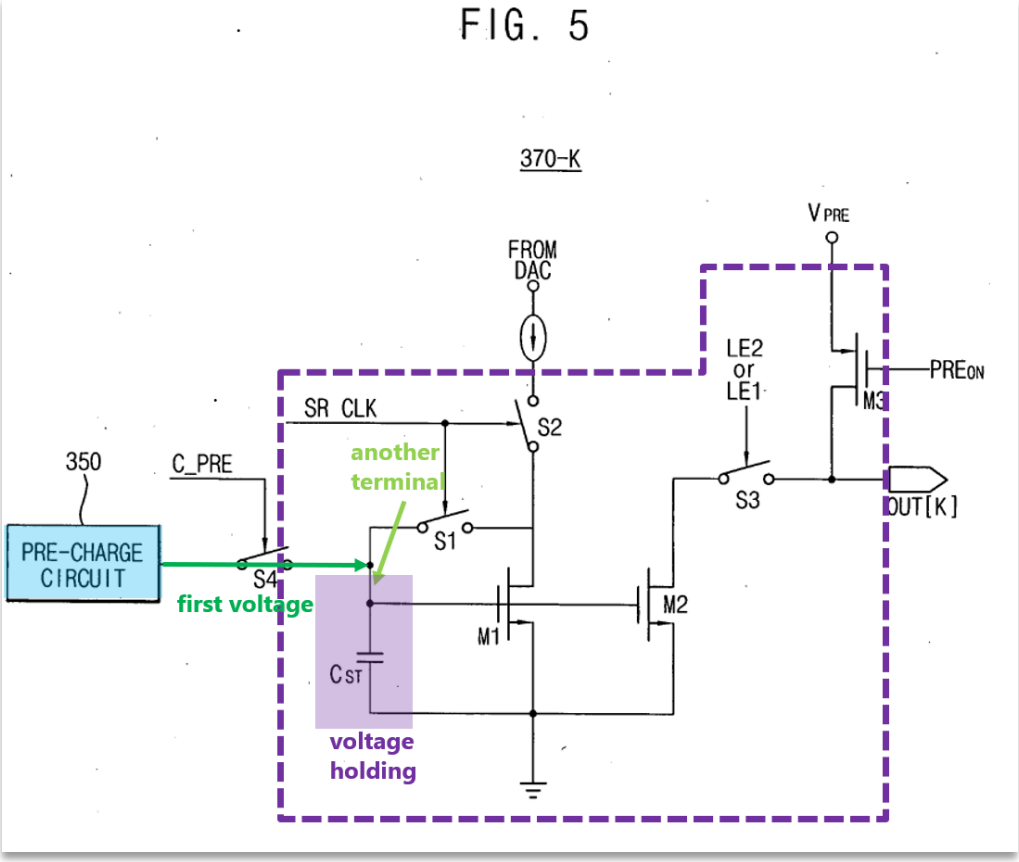
Ex. 1005, Fig. 4 (annotated); Ex. 1002, ¶165,

h. <u>1(f). "under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit,"</u>

Baek discloses operation under a voltage supply mode (annotated blue), including when the C_PRE (pre-charge) signal is set to high.



Ex. 1005, Fig. 4 (annotated). As shown in Figure 5, each current sample/hold circuit (within the dotted purple box, part of current sample/hold output circuit, the claimed "current output circuit") receives the first voltage (annotated green) from the pre-charge circuit (the claimed "first voltage supply source," annotated blue). The first voltage is supplied to another terminal (annotated light green) of the voltage storage circuit (annotated solid purple).



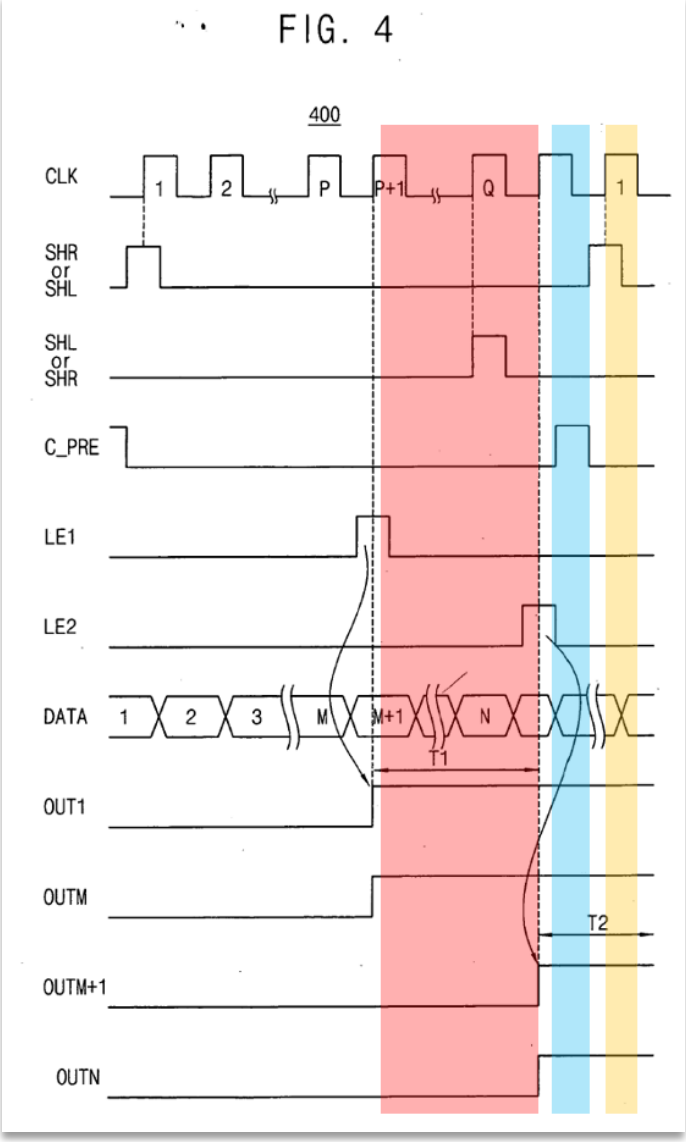
Ex. 1005, Fig. 5 (annotated). Baek explains "a fourth switch S4 may be turned on to pre-charge a voltage of the storage capacitor CST to a voltage level slightly lower than a threshold voltage of the first transistor M1 in response to the capacitor pre-charge signal C_PRE." *Id.*, ¶[0062]. This analysis is consistent with the description of these elements in the '047 Patent, in which the voltage holding capacitor is connected to the voltage supply source during the voltage supply mode. Ex. 1001, 7:44-52; Ex. 1002, ¶¶166-168.

i. <u>1(g). "under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit, and"</u>

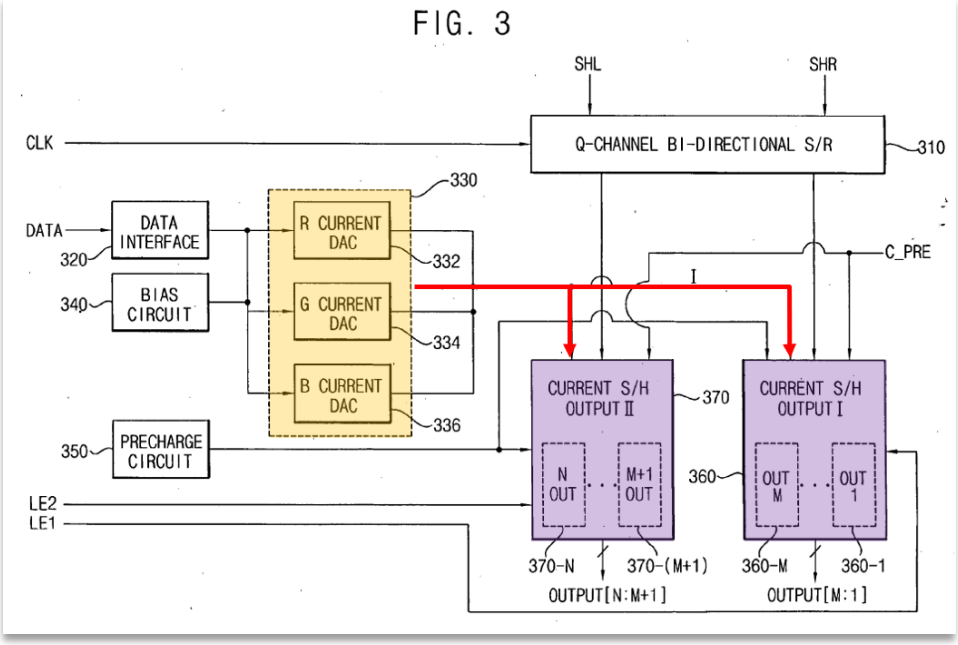
Baek discloses this limitation. When the SR_CLK signal is activated, the current sample/hold circuit operates under the claimed "current supply mode." Ex. 1002, ¶169.

i. "under said current supply mode, each of said current output circuits receives said first current from said first current supply source"

The current supply mode is annotated gold in Figure 4.



Ex. 1005, Fig. 4 (annotated); Ex. 1002, ¶165. Under this mode, switches S1 and S2 are turned on and each current sample/hold output circuit (the claimed "current output circuits") receives the gray-scale analog current from a current DAC. Ex. 1005, ¶¶[0044]-[0045]. Figure 3 shows the current DAC (the claimed "current supply source," annotated gold), the current output circuits (annotated purple), and lines along which the "first electric current" are supplied (annotated red):



Ex. 1005, Fig. 3. Specifically, current is applied to the gate and drain terminals of transistor M1 (shown in Fig. 5), which is part of the current sample/hold output circuit. *Id.*, ¶[0056]. Baek discloses:

> As a result, an analog gray-scale current output from a current digital-to-analog conversion unit 330 may be applied to a drain of the first transistor M1 via the second switch S2. At this time, because the first switch S1 is also turned on, the analog gray-scale current applied to the drain of the first transistor M1 may be applied to a gate of the first transistor M1.

Ex. 1005, ¶[0056]; Ex. 1002, ¶¶169-171.

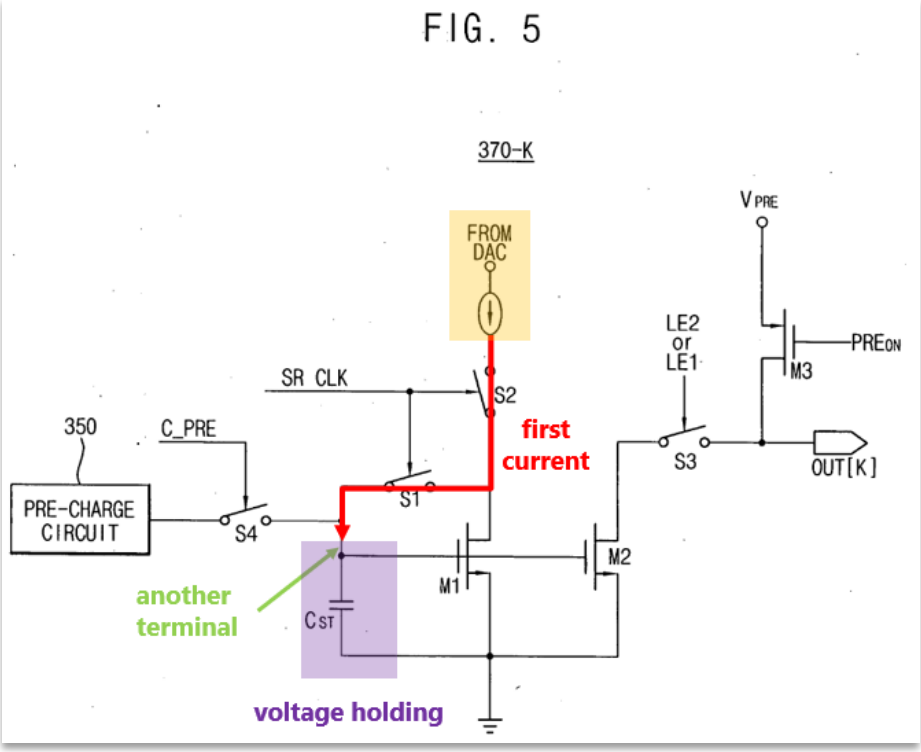
ii. "generates a second voltage by said current-voltage converting circuit, and"

Under the voltage supply mode that preceded the current supply mode, the storage capacitor was charged by pre-charge circuit to "a voltage level slightly lower than a threshold voltage of the first transistor M1." Under the current supply mode,

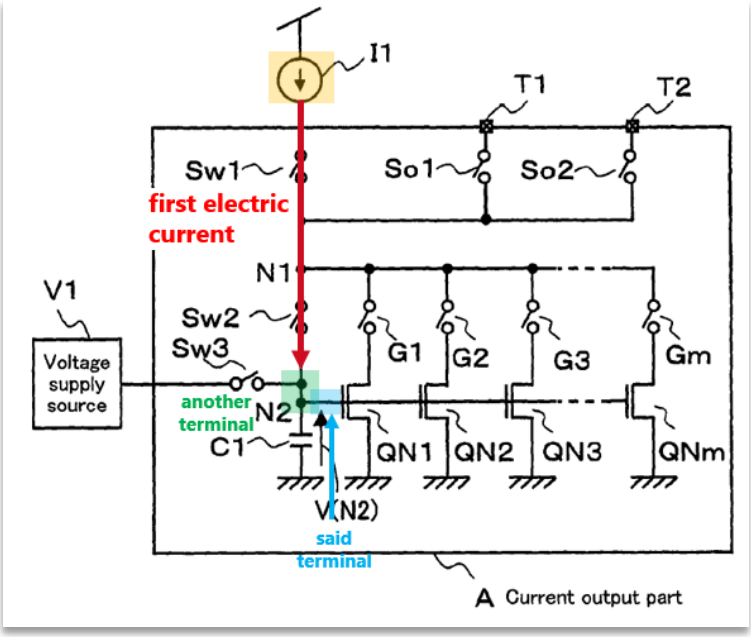
the storage capacitor continues to be charged by current from the DAC. Because current from the DAC continues charging the pre-charged capacitor during the current supply mode, the voltage across the capacitor and the gate voltage of transistor M1 continue to change, thereby reaching a second voltage different from the pre-charge voltage. Ex. 1005, ¶[0056]; Ex. 1002, ¶172.

iii. the first current is supplied to said another terminal of said voltage holding circuit

The first current (annotated red) from the current source (annotated gold) is supplied to the claimed "another terminal" (annotated light green) of the storage capacitor CST (annotated purple).



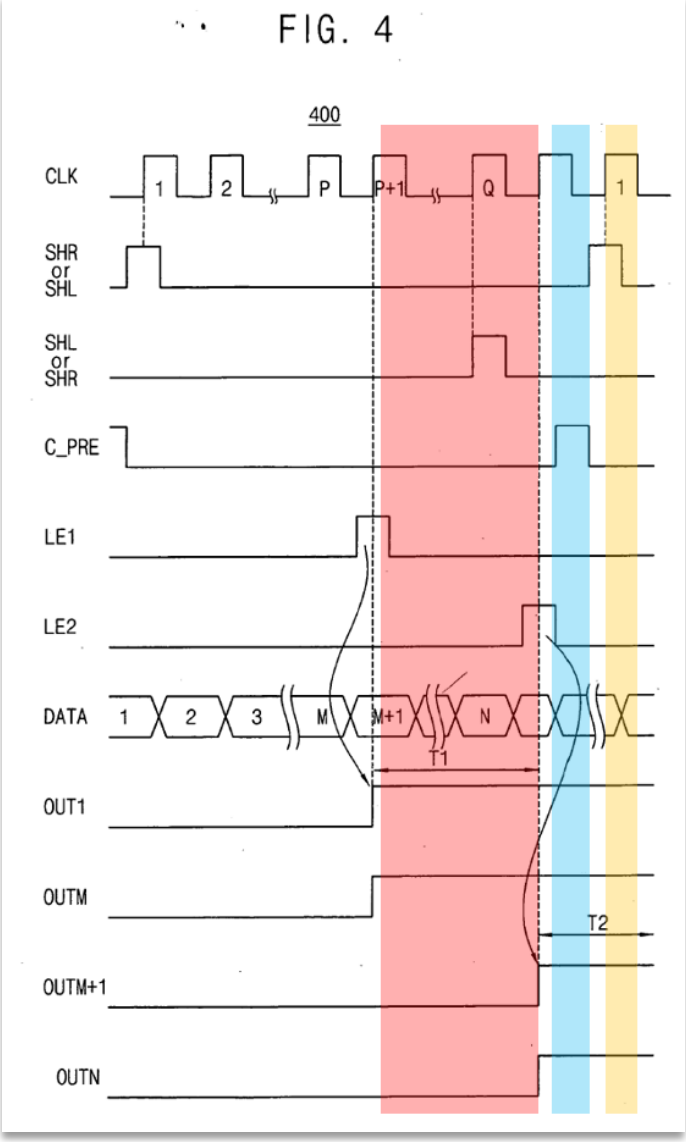
Ex. 1005, Fig. 5 (annotated), ¶[0056]. This analysis is consistent with the description of these elements in the '047 Patent, where the first current is supplied to the second terminal of the voltage holding capacitor in a similar manner as Baek. Figure 1 is annotated to show that a first electric current is supplied to the marked "another terminal" of the voltage holding capacitor.



Ex. 1001, Fig. 1A (annotated), 8:1-15; Ex. 1002, ¶¶173-174.

j. <u>1(h). "under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit."</u>

Baek discloses operation under a current output mode (annotated red), including when a latch signal (LE1 or LE2) is activated.

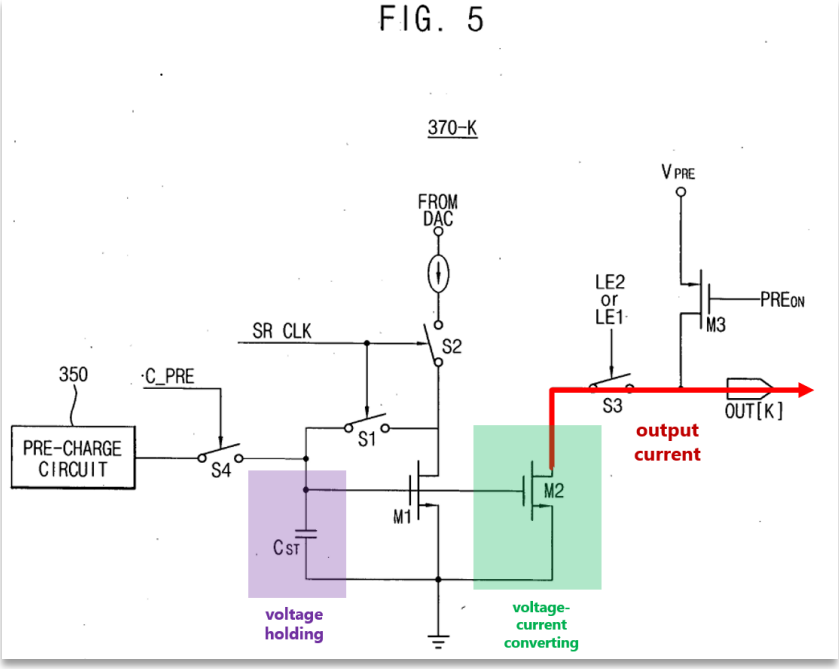


Ex. 1005, Fig. 4 (annotated). Under current output mode, switch S3 is turned on and transistor M2 outputs a current according its gate voltage, which is the voltage stored in the storage capacitor CST.

> When the first latch enable signal LE1 or the second latch enable signal LE2 is activated, a third switch S3 may couple a drain of the second transistor M2 to an output terminal OUT[K], and the second transistor M2, which may have its gate coupled to the storage capacitor CST, may

> output the analog gray-scale current to the output terminal OUT[K] based on the charged analog gray-scale current.

Ex. 1005, ¶[0058].



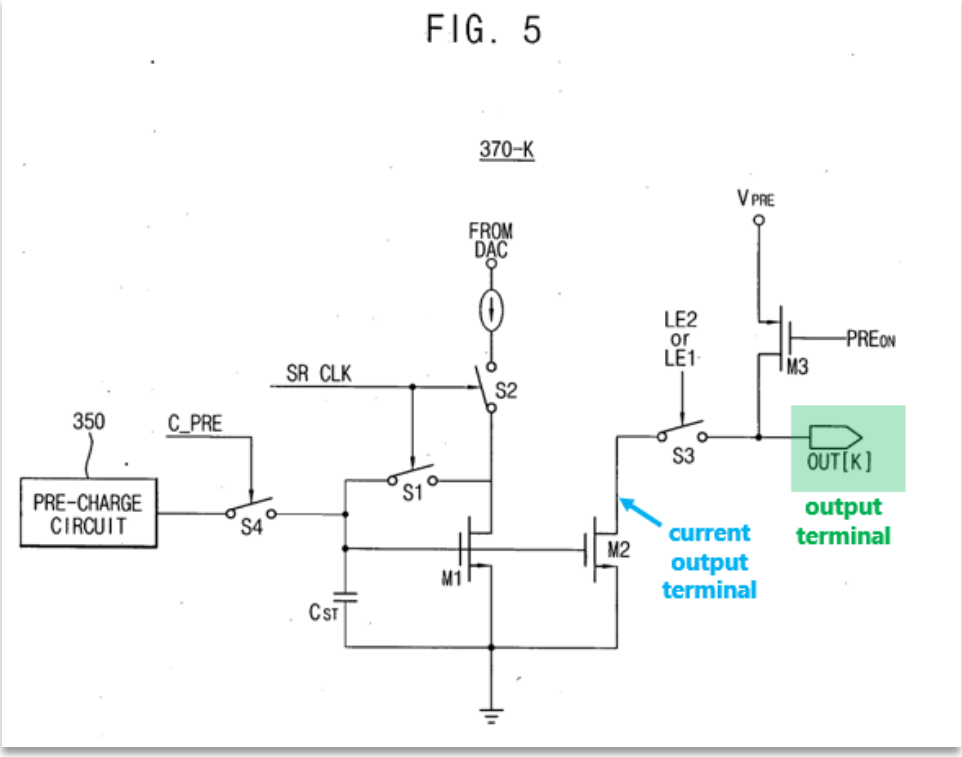
Ex. 1005, Fig. 5 (annotated). Consistent with a fundamental properties of transistors, transistor M2 converts the voltage applied to its gate into a corresponding current. A POSITA would further have recognized that "the second transistor M2 … may output the analog gray-scale current … based on the charged analog gray-scale current," meaning that the transistor M2 outputs a current based on the voltage applied to its gate, which is the voltage stored in the storage capacitor. *Id.*, ¶[0058]; Ex. 1002, ¶¶175-176.

B. <u>CLAIM 2</u>

Baek discloses, or at least renders obvious, this claim.

"The current driving device according to claim 1, wherein: each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits, and"

As described above for Claim Limitation 1(c), terminals OUT[1] through OUT[N] are an example of the claimed "output terminals." As described above for Claim Limitations 1(d)(1) and 1(d)(2), the current sample/hold output circuits 360 and 370 are an example of the plurality of current output circuits. And as described for Claim Limitation 1(d)(2), the drain terminal of each transistor M2 (each located within a corresponding current sample/hold circuit) are an example of current output terminals. As shown in Figure 5 below, the drain terminal of transistor M2 (annotated blue) is connected to the output terminal OUT[K] (annotated green). Ex. 1005, ¶[0058].

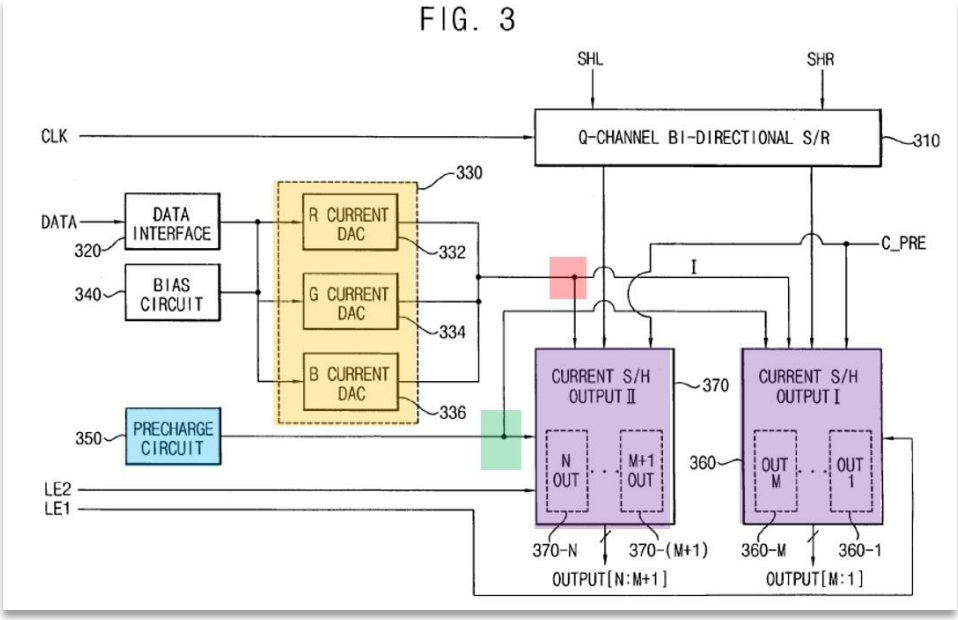


Ex. 1005, Fig. 5 (annotated); Ex. 1002, ¶¶177-178.

Baek discloses each current sample/hold output circuit (360 and 370) comprises a plurality of current sample/hold circuits ($360_{1\text{-}M}$ and $370_{(M+1)\text{-}N}$), each of which comprises a transistor M2. Ex. 1005 ¶¶[0038]-[0039], [0055]; Figs. 3, 5. Therefore, Baek discloses each of said output terminals is connected to said current output terminals provided to said plurality of said current output circuits as recited in claim 2. Ex. 1002, ¶179.

"each of said plurality of current output circuits is connected in parallel to said first current supply source and said first voltage supply source used in common."

Baek discloses this limitation or at least renders it obvious. As shown in Figure 3, current sample/hold output circuits 360 and 370 (annotated purple) and DAC 330 (annotated gold) are connected to a common node (annotated red).



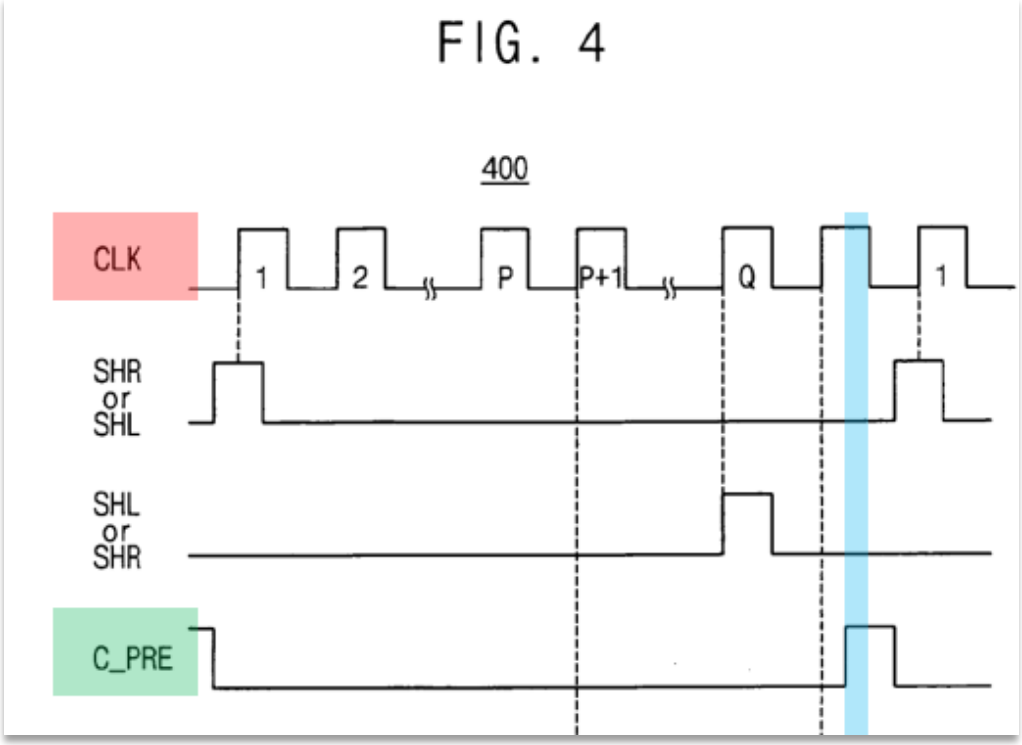
Ex. 1005, Fig. 3. Current sample/hold output circuit 360, current sample/hold output circuit 370, and pre-charge circuit 350 (annotated blue) are connected to a common node (annotated green). Current sample/hold output circuits 360 and 370 are also grounded, because the individual current sample/hold circuits within the current sample/hold output circuits 360 and 370 are grounded. A POSITA would have recognized that DAC 330 (annotated gold) and pre-charge circuit (blue) would also be grounded, or that it would be obvious to do so, because it was necessary for a

power supply to be grounded to form a complete loop. Thus, each of current sample/hold output circuits 360 and 370 is connected in parallel to the pre-charge circuit 350 and DAC 330 used in common. Ex. 1002, ¶¶180-181.

C. CLAIM 3

> **"The current driving device according to claim 1, wherein, in each of said current output circuits, said current-voltage converting circuit is actuated under said voltage supply mode."**

Baek discloses this claim. As discussed above for Claim Limitations 1(f) and 1(g), the current driving device operates under voltage supply mode when control signal C_PRE is activated, and operates under the claimed "current supply mode" when a clock signal CLK is activated. When clock signal CLK is activated, switches S1 and S2 are closed, and current from DAC is supplied to storage capacitor CST and the drain and gate of transistor M1. Ex. 1005, ¶¶[0056]-[0057]. Transistor M1 and storage capacitor CST then convert the current into a voltage stored at the storage capacitor CST. As shown in Figure 4 below, Baek discloses that C_PRE (annotated green) and CLK (annotated red) can be activated simultaneously (e.g., both set to high), such as during the timespan highlighted blue. Therefore, Baek discloses the current-voltage converting circuit is actuated under voltage supply mode.



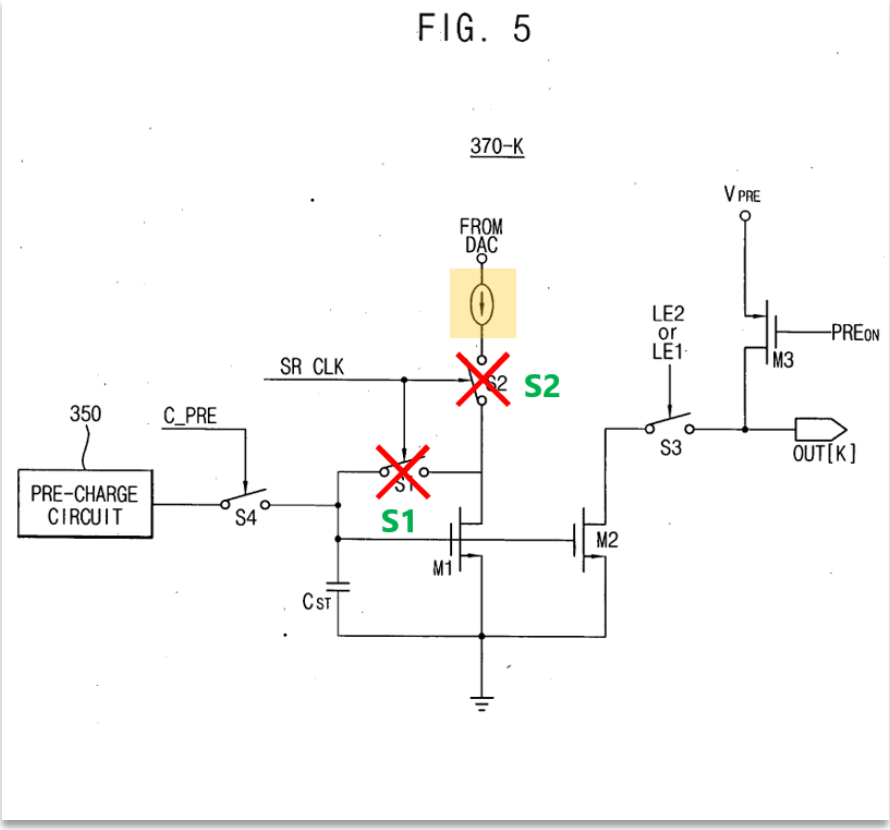
Ex. 1005, Fig. 4 (annotated and excerpted); Ex. 1002, ¶¶182-183.

D. CLAIM 4

> **"The current driving device according to claim 1, wherein each of said current output circuits is configured to stop said current-voltage converting circuit under said voltage supply mode."**

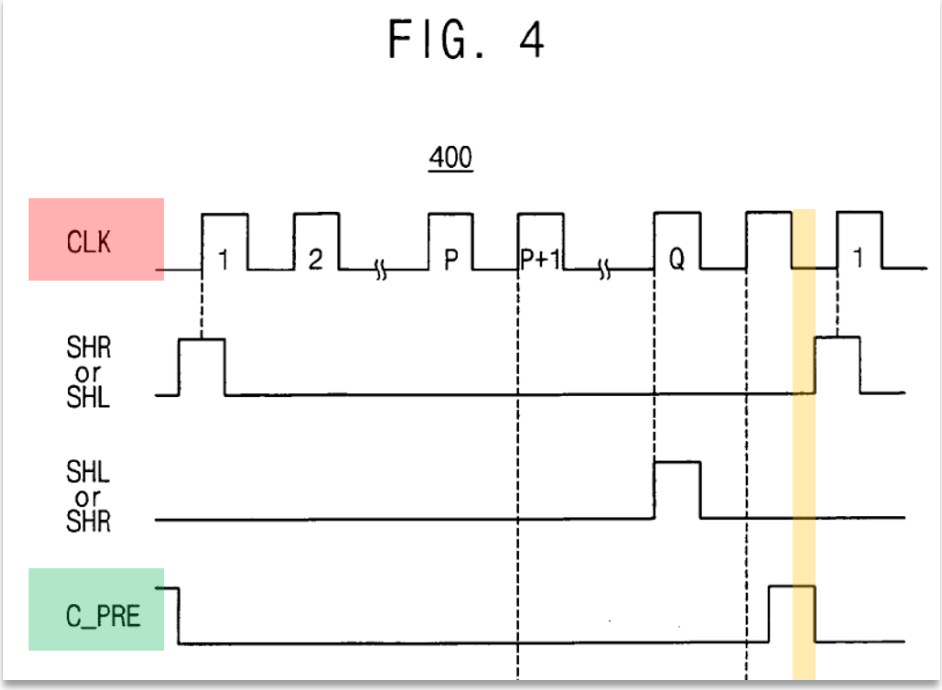
Baek discloses this claim. As discussed above for Claim Limitation 1(f) and 1(g), the current driving device operates under the claimed "voltage supply mode" when control signal C_PRE is activated, and operates under the claimed "current supply mode" when a clock signal CLK is activated. As shown in Figure 5 below, when a clock signal CLK is deactivated, switches S1 and S2 (annotated green) are open, isolating the current source DAC 330 (gold) from the current sample/hold

circuit. The current-voltage converting circuit is thus stopped under voltage supply mode. The current source (annotated gold) and switches S1 and S2 (annotated green) are shown in Figures 5, with a red × placed over transistor lines that are turned off.



Ex. 1005, Fig. 5 (annotated); Ex. 1002, ¶¶184-185.

As shown in Figure 4 below, Baek discloses that CLK (annotated red) can be deactivated when C_PRE (annotated green) is activated, such as during the timespan highlighted gold. Ex. 1005, Fig. 4. Therefore, Baek discloses the current-voltage converting circuit is stopped under voltage supply mode.



Ex. 1005, Fig. 4 (annotated and excerpted); Ex. 1002, ¶186.

E. <u>CLAIM 9</u>

> **"A current-driving-type display device, comprising said current driving device according to claim 1 mounted thereon so as to be driven by said current driving device."**

Baek discloses this limitation. Baek discloses "a display driver circuit for a flat display panel." Ex. 1005, ¶[0003]. Baek further discloses that "the display driver circuit according to example embodiments of the present invention may be applicable to Organic Light Emitting Diode (OLED) display devices, for example, current-driven active matrix type OLED display devices." *Id.*, ¶[0064]. The display driver circuit is mounted on the display. Ex. 1002, ¶187.

IX. GROUND 5-6: SASAKI

Claim 10 is anticipated by Sasaki (Ex. 1006), (Ground 5). It is also obvious over Sasaki (Ground 6). *See Realtime*, 912 F.3d at 1373 ("anticipation is the epitome of obviousness"); Ex. 1002, ¶188.

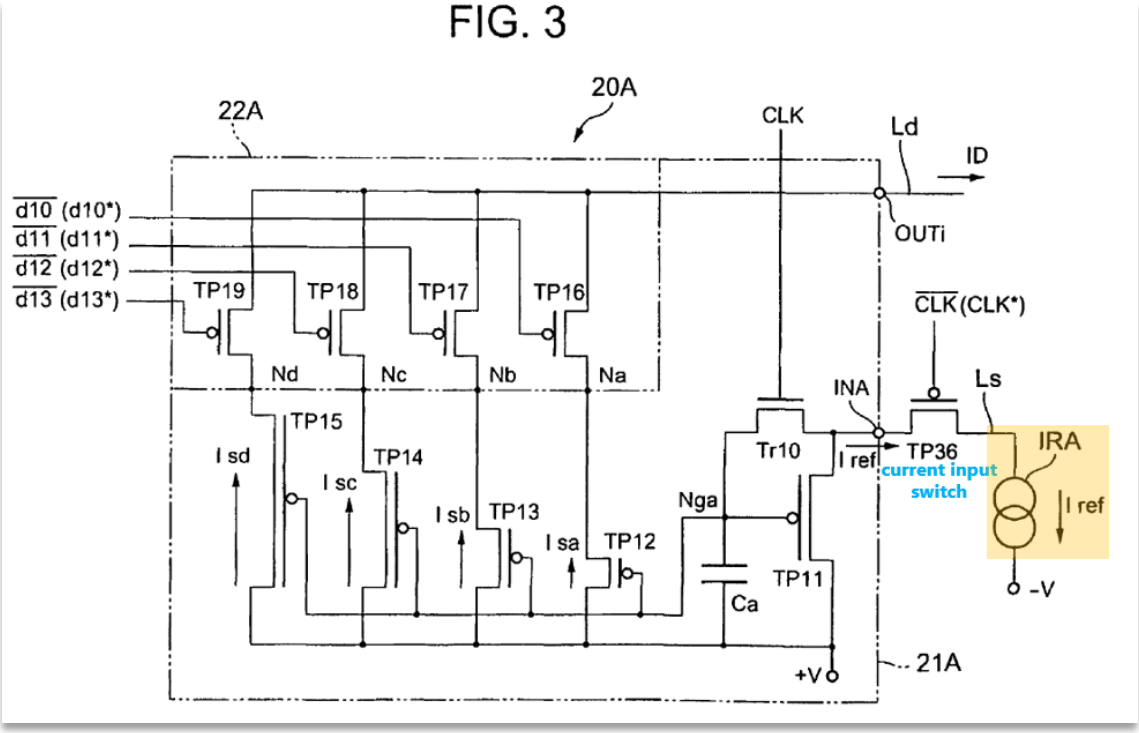
A. CLAIM 10

a. 10(preamble): "A current driving device, comprising:"

To the extent the preamble is limiting, Sasaki discloses it. Sasaki describes "a display device comprising [a] current generation supply circuit," which is an example of the claimed "current driving device." Ex. 1006, ¶[0003]. The current generation supply circuit "supplies drive currents corresponding to digital signals for a plurality of loads." *Id.*, Abstract; Ex. 1002, ¶189.

b. 10(a): "a current input switch for controlling connection/disconnection states with respect to a current supply source;"

Sasaki discloses this limitation. The "current supply source control transistor TP36" in Sasaki is an example of the claimed "current input switch." Ex. 1006, ¶[0063].

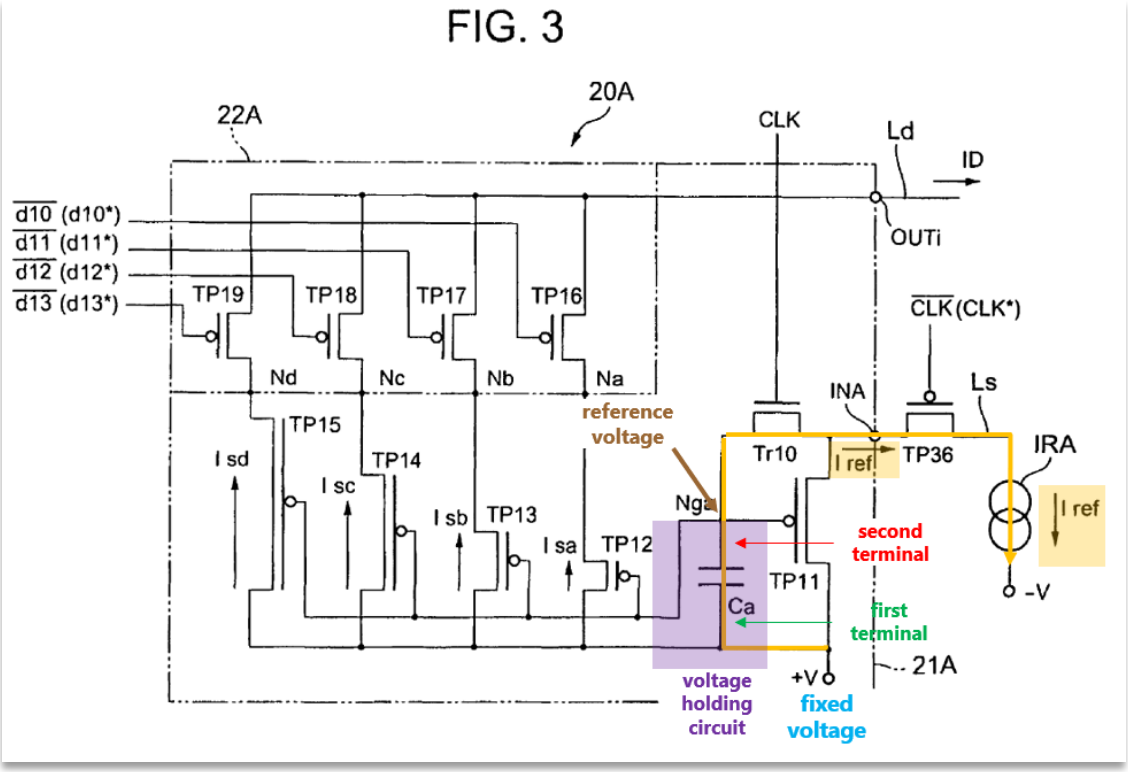


Ex. 1006, Fig. 3 (annotated). The current supply source control transistor TP36 (annotated blue) controls connection/disconnection states of "constant current generation source IRA." *Id.*, ¶¶[0062]-[0063], Fig. 3. Sasaki refers to the item labeled IRA (annotated gold) as "a constant current generation source Iref." *Id.*; Ex. 1002, ¶190.

c. <u>10(b): "a voltage holding circuit for holding a reference voltage, which is charged by a flown current, the voltage holding circuit having a first terminal and a second terminal, the first terminal being connected to a fixed voltage;"</u>

Sasaki discloses this limitation or at least renders it obvious. Sasaki describes a "charge storage circuit," which includes "the capacitor Ca shown in Fig. 3." Ex.

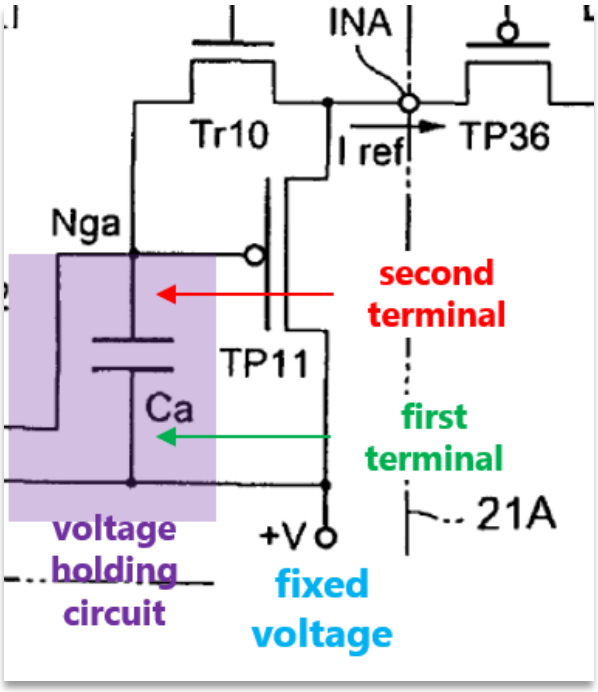
1006, ¶[0138]. The charge storage circuit comprising capacitor Ca is an example of the claimed "a voltage holding circuit" (annotated purple).



Ex. 1006, Fig. 3 (annotated). The charge holding circuit has two terminals: "capacitor Ca is connected between the high electric potential +V and the contact Nga (gate terminal of the reference current transistor TP11)." *Id.*, ¶[0063]; Ex. 1002, ¶191.

The charge storage circuit (the claimed "voltage holding circuit," annotated purple) has a first terminal (annotated green) and a second terminal (annotated red), the first terminal being connected to the high electric potential +V (annotated blue). Sasaki discloses "[t]he capacitor Ca is connected between the high electric potential

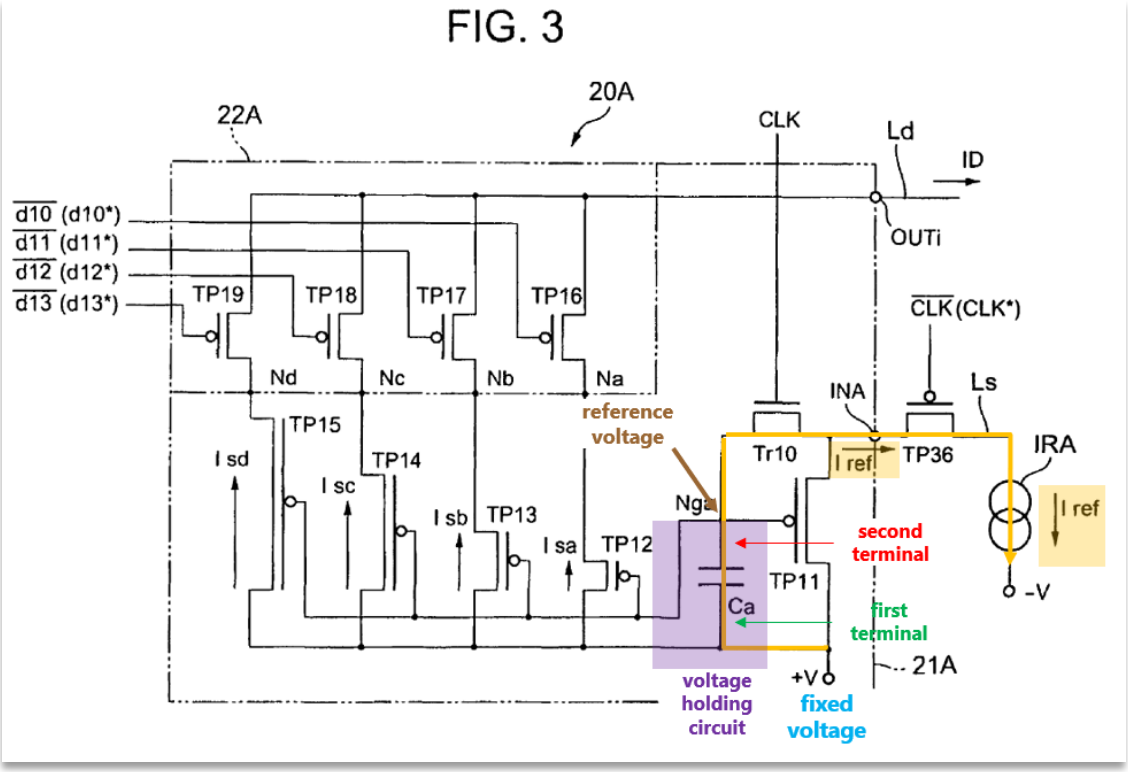
+V and the contact Nga (gate terminal of the reference current transistor TP11). *Id.*, ¶[0063].



Ex. 1006, Fig. 3 (annotated and excerpted). The high electric potential +V represents a constant voltage supply, which is an example of the claimed "fixed voltage." Designations such as "+V," in connection with designations such as V_{DD} and V_{CC}, are commonly used on circuit diagrams to depict a fixed supply voltage that is supplied to the drain of a MOSFET. Ex. 1002, ¶192.

The charge storage circuit (capacitor Ca) holds a "specified voltage" (Ex. 1006, ¶[0077]), and the charge is stored on the capacitor "based on the reference current Iref." *Id.*, ¶[0071]. The reference current Iref (annotated gold) is an example

of the claimed "flown current," and the specified voltage (annotated brown) is an example of the claimed "reference voltage."



Ex. 1006, Fig. 3 (annotated). Sasaki further explains how the reference current flows in order to provide the specified voltage:

> [I]n this non-selection state, when both the current supply source control transistor TP36 and the refresh control transistor Tr10 perform an "ON" operation, the reference current Iref flows in the current path of the reference current transistor TP11 and the electrical charge of the reference current Iref is supplied to the gate terminal (contact Nga) based on the channel width of the reference current transistor TP11.

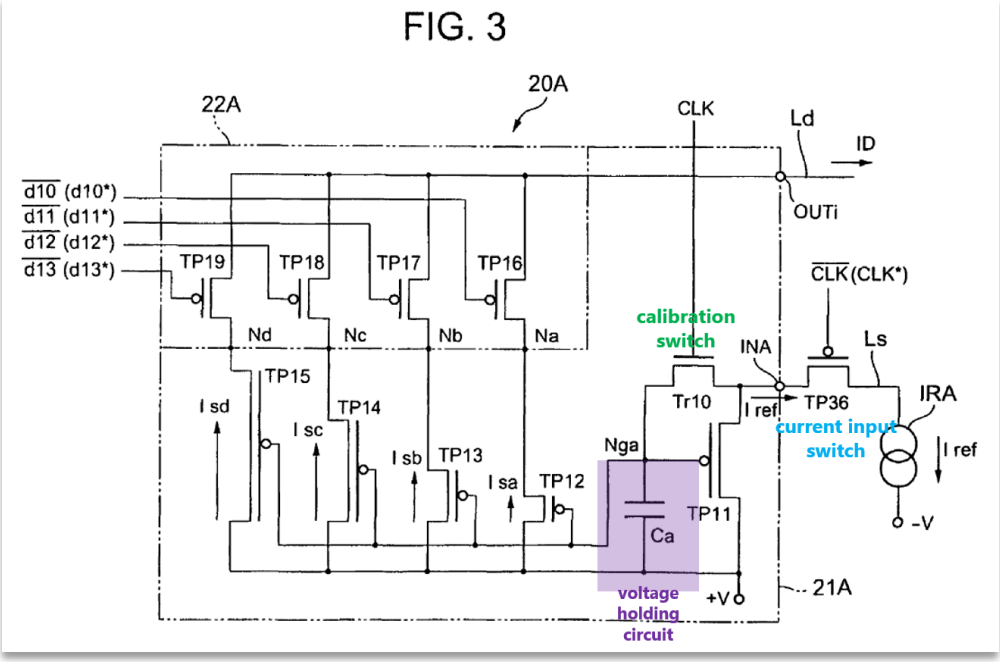
Id., ¶[0077]; Ex. 1002, ¶193.

d. 10(c): "a calibration switch interposed between said current input switch and said voltage holding circuit;"

Sasaki discloses this limitation. Refresh control transistor Tr10 is an example of the claimed "calibration switch." In Sasaki, a refresh is performed to calibrate the voltage across the capacitor Ca.

> Furthermore, in this non-selection state, when both the current supply source control transistor TP36 and the refresh control transistor Tr10 perform an "ON" operation, the reference current Iref flows in the current path of the reference current transistor TP11 and the electrical charge of the reference current Iref is supplied to the gate terminal (contact Nga) based on the channel width of the reference current transistor TP11.

Ex. 1006, ¶[0077]. The refresh control transistor T10 (annotated green) is interposed between the current supply source control transistor TP 36 (the claimed "current input switch," annotated blue) and charge storage circuit (the claimed "voltage holding circuit," annotated purple).



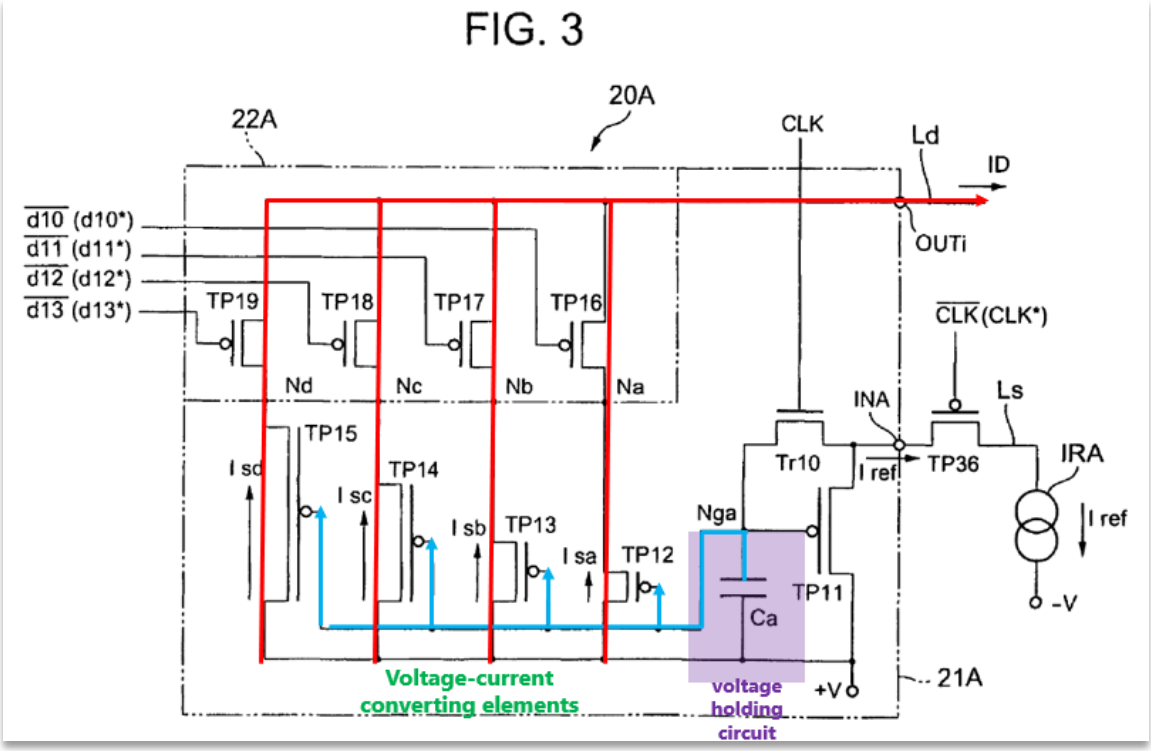
Ex. 1006, Fig. 3 (annotated). In Sasaki, the calibration switch controls whether the reference current Iref from the reference current supply source IRA is supplied to the capacitor CA to adjust the voltage stored in the capacitor. *See Id.*, Fig. 3, ¶[0077]. This analysis is consistent with the description of these elements in the '047 Patent. Ex. 1001, 1:37-49 ("'Calibration' means to have a reference current value by a reference current source stored in the current output part."); Ex. 1002, ¶¶194-195.

e. <u>10(d): "a plurality of voltage-current converting elements for generating an electric current in accordance with said reference voltage held in said voltage holding circuit;"</u>

Sasaki discloses this limitation. The "module current transistors" (TP12-TP15) in Sasaki is an example of the claimed "a plurality of voltage-current converting elements."

> [T]he module currents Isa-Isd which flow to each of the module current transistors TP12~TP15 are set to have a ratio of current values different from each other relative to the constant reference current Iref which flows to the reference current transistor TP11 established in the current mirror circuit section 21A stated above.

Ex. 1006, ¶[0066]. Each of the module current transistors (TP12-TP15) generates an electric current in accordance with the reference voltage held in the capacitor Ca. As shown in Figure 3 below, a voltage held in the capacitor Ca is applied to the gates of transistors TP12 through TP15.



Ex. 1006, Fig. 3 (annotated). Figure 3 shows the lines along which the reference voltage is supplied (annotated blue), and the lines along which output currents flow (annotated red). Ex. 1002, ¶¶196-197.

A POSITA would have recognized that transistors TP12 through TP15 convert the voltage applied to their gate into a corresponding current (between drain and source), because a fundamental property of transistors is to output current based their gate voltage and because there is no current flowing from capacitor Ca to transistors TP12 through TP15. Therefore, this circuit converts the current stored in storage capacitor CST into output current. Ex. 1002, ¶196. Each of the module current transistors (TP12-TP15, annotated green) receives the reference voltage from the capacitor Ca (the claimed "voltage holding capacitor," annotated purple) at its gate and outputs an electric current in accordance with that reference voltage. This analysis is consistent with the description of these elements in the '047 Patent, where the voltage-current converting function is performed in current output mode, where transistors QN1-QNm convert the voltage applied to the gate of QN1-QNm into current flowing through QN1-QNm. Ex. 1001, 8:30-38; Ex. 1002, ¶¶197-198.

f. <u>10(e): "a plurality of signal response switches that are on/off controlled in accordance with inputted signals, each of said response switches being connected in series to a corresponding one of said voltage-current converting elements, and each of which being connected in parallel to said calibration switch;"</u>

Sasaki discloses this limitation. The switching transistors TP16-TP19 are an example of the claimed "signal response switches." The on/off states of TP16-TP19

are controlled by data signals d10 through d13, which are examples of the claimed "inputted signals."

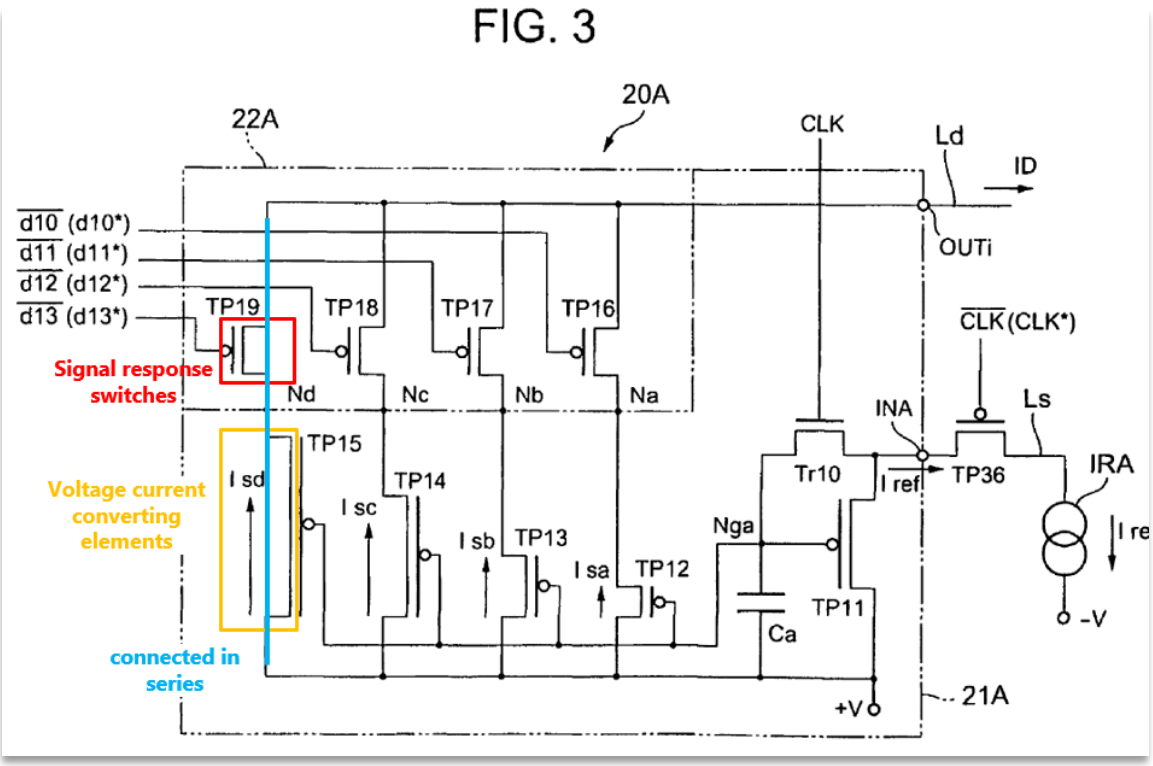
> [I]n response to the signal levels of the output signals d10*~d13* from the above-mentioned latch circuits LC0˜LC3, the particular switching transistors of the switching circuit section 22A perform an "ON" operation (Instances when any one or more of the switching transistors TP16~TP19 perform an "ON" operation, besides occurrences when any of the switching transistors TP16~TP19 perform an "OFF" operation is included.).

Ex. 1006, ¶[0069].

> [B]ased on the inverted output signals d10*˜d13* outputted from the data latch section 102, the "ON/OFF" state of the plurality of switching transistors (equivalent to the switching transistors TP16˜TP19 shown in FIG. 3) is controlled.

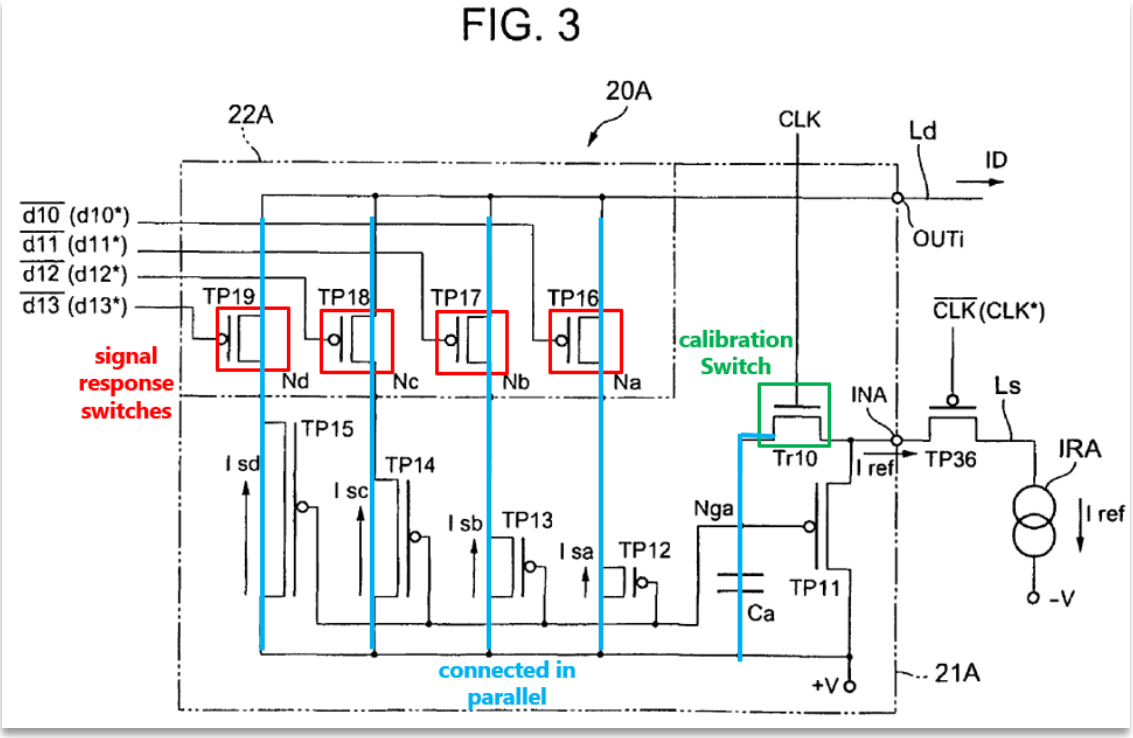
Id., ¶[0152]; Ex. 1002, ¶199.

Transistor TP19 (annotated red) is connected in series to the module current transistor TP15 (one of the claimed "voltage-current converting elements," annotated gold). Similarly, each of the transistors TP16~TP18 is connected in series corresponding one of the module current transistors (TP12~TP14).



Ex. 1006, Fig. 3 (annotated); Ex. 1002, ¶200.

Each of the switches TP16-TP19 is connected in parallel to refresh control switch Tr10 (the claimed "calibration switch," annotated green). The on/off states of a switching transistor does not affect the on/off states of another switching transistor. Ex. 1006, Fig. 3. Each switching transistor is connected to the high electric potential through a voltage-current converting element, while the Tr10 is connected to the high electric potential +v via the capacitor Ca. *Id*.

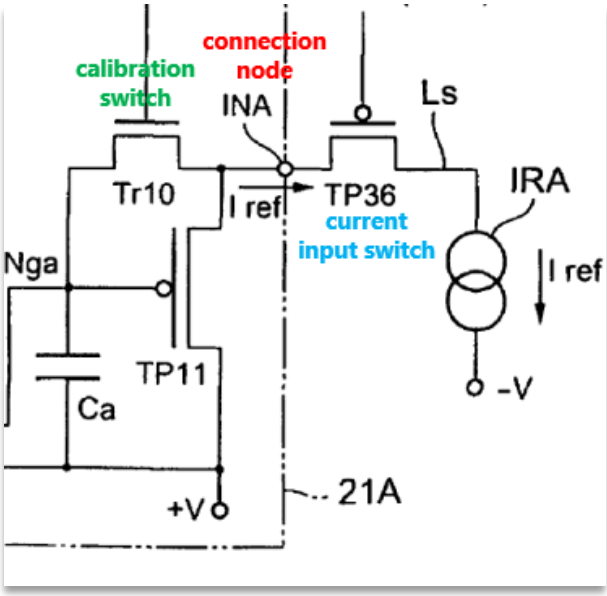


Ex. 1006, Fig. 3 (annotated); Ex. 1002, ¶¶200-201.

g. <u>10(f): "a connection node provided between said current input switch and said calibration switch;"</u>

Sasaki discloses this limitation. The current input contact INA in Sasaki is an example of the claimed "connection node." The current input contact INA (referred as INA in Sasaki) is an input node of a corresponding current generation section 20A, receiving a reference current Iref from a corresponding reference current supplier IRA (referred as IRA in Sasaki). Ex. 1006, ¶[0071]. The current input contact INA is also referred as INi in Figure 10 of Sasaki. As shown in Figure 3 below, the current input contact INA is connected to the fresh control transistor Tr10 (the claimed "calibration switch"). Thus, the current input contact INA (annotated

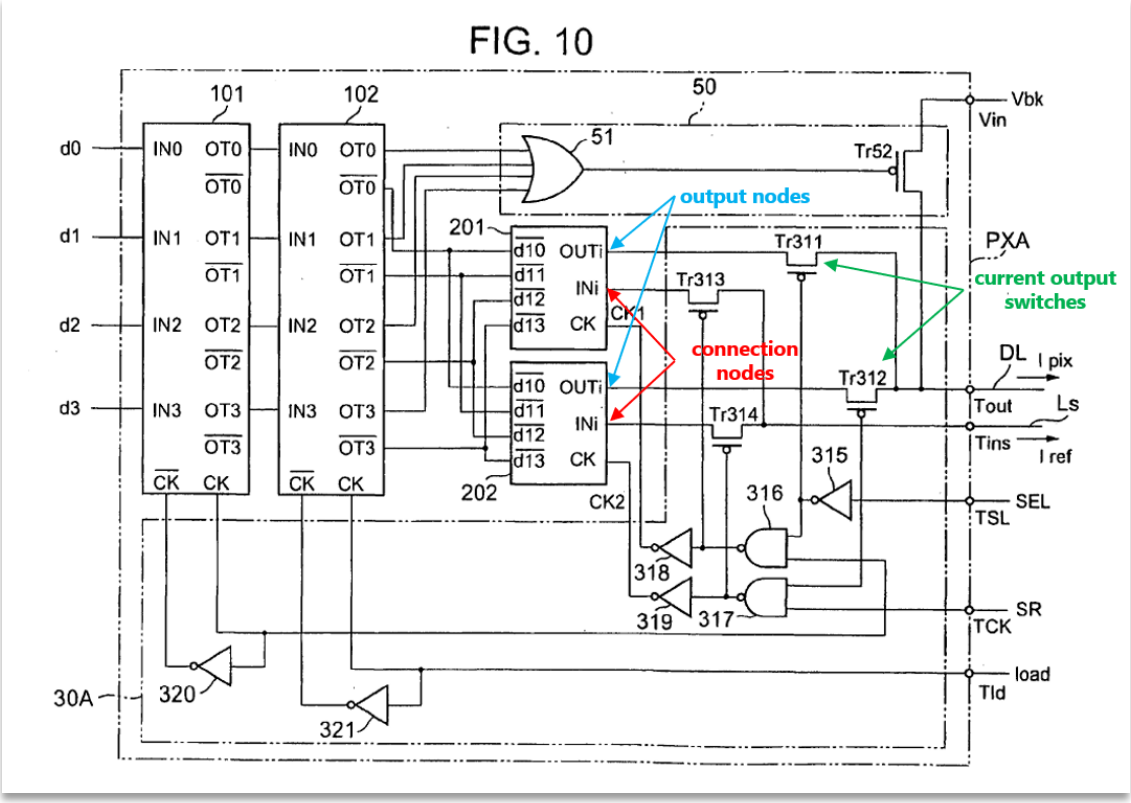
red) is provided between the current supply source control transistor TP 36 (the claimed "current input switch," annotated blue) and refresh control transistor T10 (the claimed "calibration switch," annotated green).



Ex. 1006, Fig. 3 (annotated and excerpted); Ex. 1002, ¶202.

h. <u>10(g): "a plurality of current output switches, each being interposed between the connection node and said plurality of current output terminals; and"</u>

Sasaki discloses this limitation. As shown in Figure 10, Sasaki discloses output control transistors TP311 and TP312 (annotated green), which are an example of the claimed "current output switches."



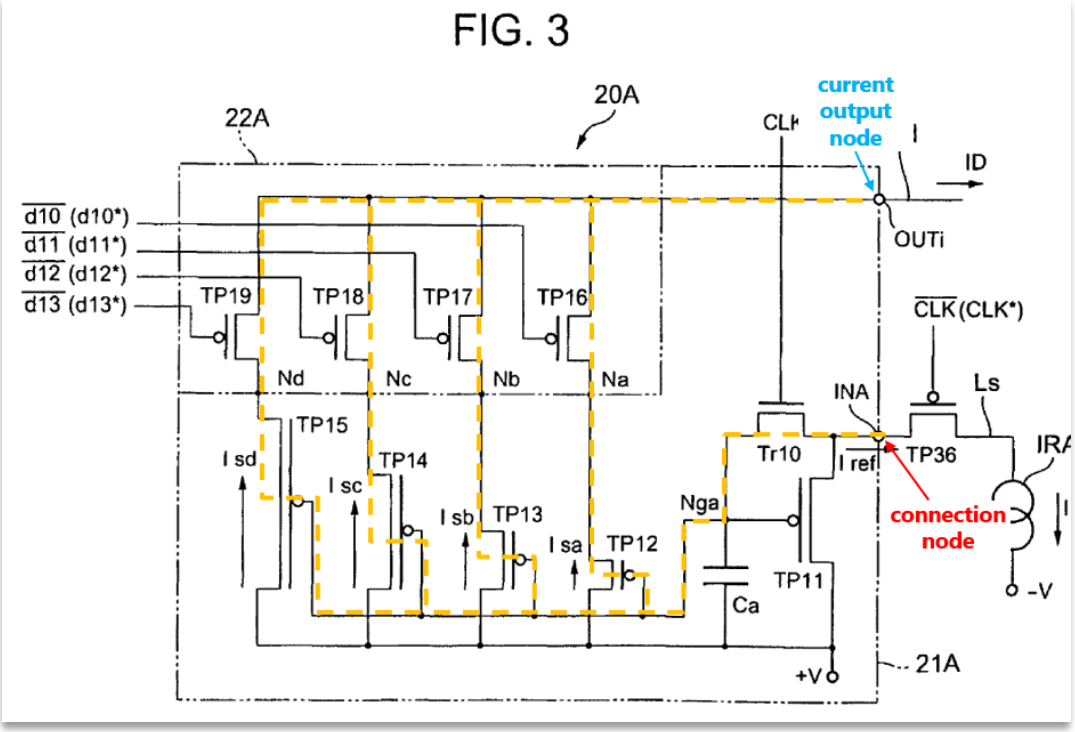
Ex. 1006, Fig. 10. (annotated); Ex. 1002, ¶203.

Output control transistors TP311 and TP312 are referred as TP31 in Figure 1, controlling the output of a corresponding current generation section.

> When the high-level selection setting signal SL is inputted and in conjunction with reversal processing of the signal polarity by the inverter 32, the output control transistor TP31 performs an "ON" operation and the current output terminal OUTi (current output contact OUTi) of the current generation section 20A connects to the drive current supply line Ld via this output control transistor TP31.

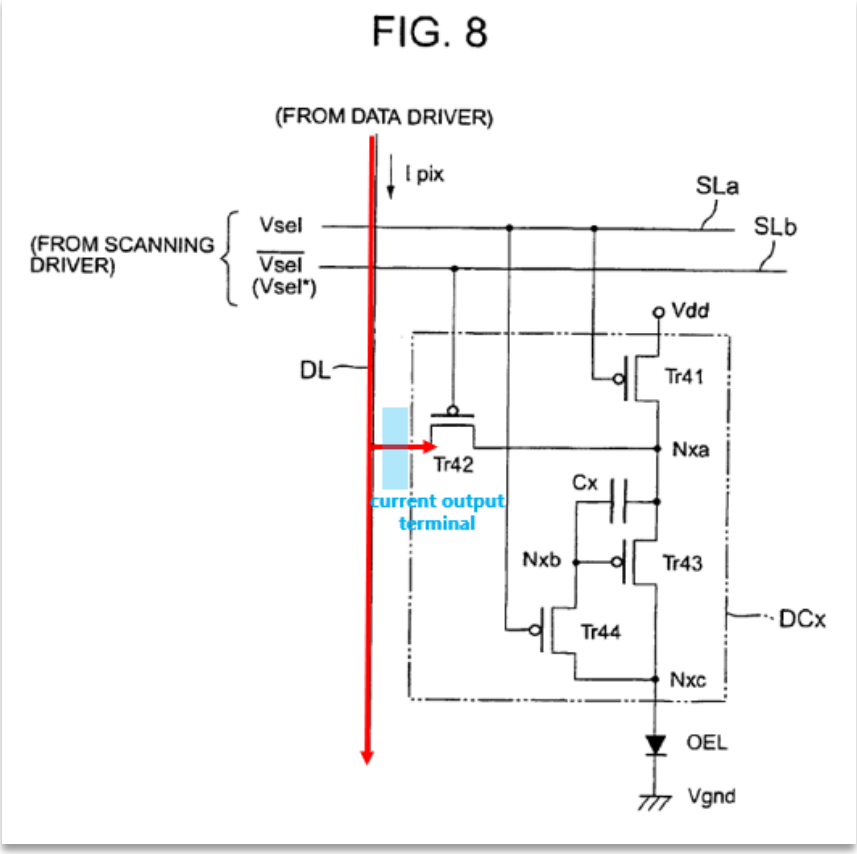
Ex. 1006, ¶[0074]. Each current output switch (TP311, TP312, or TP31) is connected to a corresponding connection node (current input contact INi or INA). As shown in Figure 10 above, each current output switch is connected to a

corresponding output node OUTi (annotated blue), which is further connected to a corresponding current input contact INi (annotated red). Figure 3 of Sasaki below confirms the connection (annotated with yellow dashed lines) between output node OUTi and input contact INi (referred as INA in Figure 3).



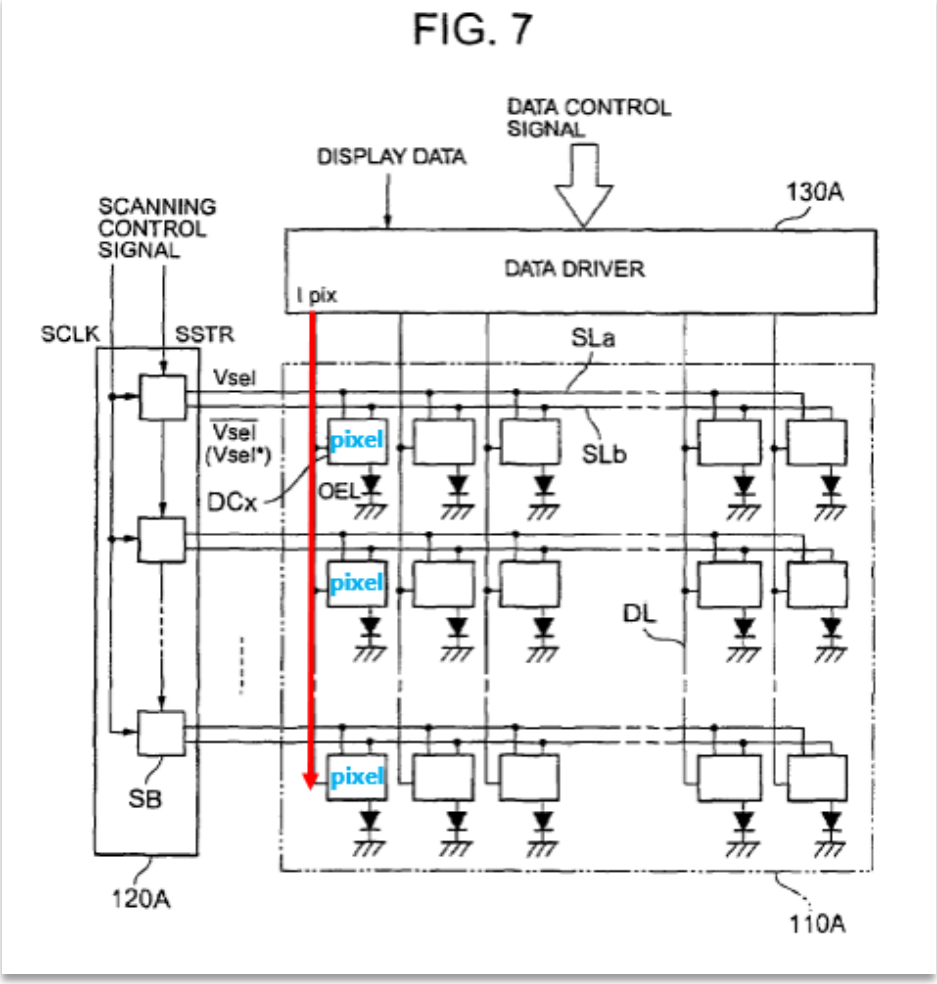
Ex. 1006, Fig. 10 (annotated); Ex. 1002, ¶204.

As shown in Figure 8 below, the terminal (annotated blue) connecting the data line (DL, annotated red) to a pixel driver circuit DCx is an example of the claimed current output terminal, outputting gradation currents Ipix to a pixel driver circuit DCx. Ex. 1006, ¶[0116], Fig. 8.



Ex. 1006, Fig. 8 (annotated); Ex. 1002, ¶205.

Sasaki discloses a plurality of current output terminals. As shown in Figure 7, the data line DL (annotated red) is connected to a plurality of pixel driver circuits DCx (annotated purple), each of which connected to a corresponding current output terminal. Ex. 1006, ¶[0116].



Ex. 1006, Fig. 7 (annotated); Ex. 1002, ¶206.

Each of the current output switches TP311 and 312 is connected to the plurality of current output terminals. As shown in Figures 7, 8, and 10 above, current output switches TP311 and 312 are connected to the data line DL, outputting a gradation currents Ipix and the data line DL is connected to a plurality of current output terminals located in a plurality of pixel driver circuits DCx. Therefore, each

of the current output switches is interposed between the current input node (IN_A) and a plurality of current output terminals. Ex. 1002, ¶¶207-208.

i. <u>10(h): "a high-speed switch for controlling connection/disconnection states of said voltage supply source with respect to the second terminal of said voltage holding circuit."</u>

Sasaki discloses this limitation.[6] Each of transistor TP11 and transistor Tr10 is an example of the claimed "high-speed switch." A POSITA would have recognized that transistors TP11 and Tr10 are high-speed switches, because they can be turned on and off within the timespan of a single frame. A POSITA would have also recognized a high electric potential +V as an example of the claimed "voltage supply source." Each of transistors TP11 and Tr10 (annotated brown) controls connection/ disconnection states of a high electric potential (annotated blue) with respect to the second terminal of the capacitor Ca (the claimed "voltage holding circuit," annotated purple). The connection between the high electric potential +V and the capacitor Ca is annotated gold.

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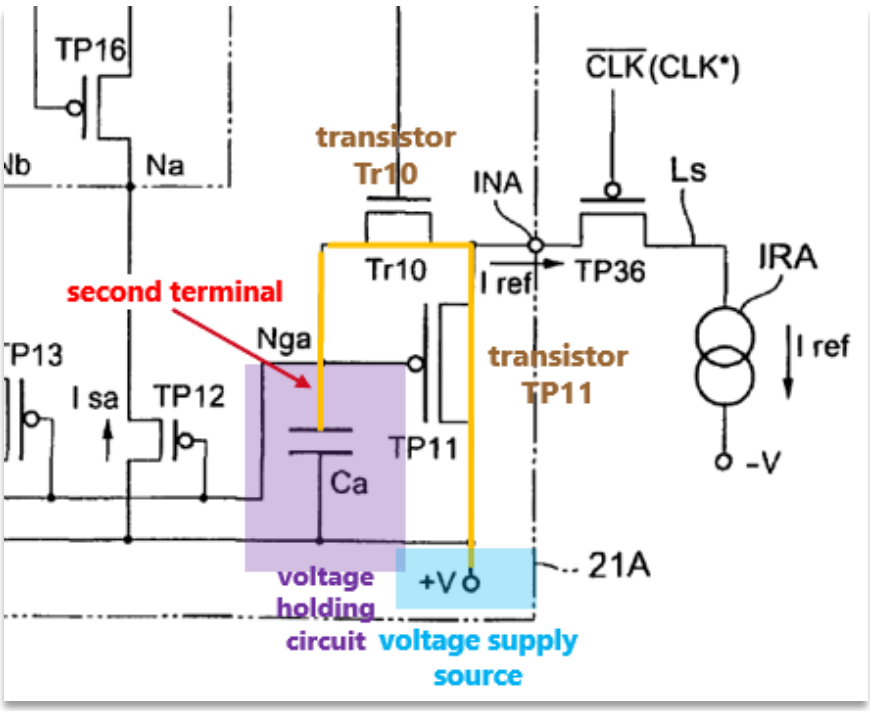
[6] Claim 10 says "<u>said</u> voltage supply source," but lacks antecedent basis as the term "voltage supply source" is not previously used in claim 10. Solely for this petition, Petitioner assumes the term refers to "a fixed voltage," which is recited earlier in the claim.



Ex. 1006, Fig. 3 (annotated and excerpted); Ex. 1002, ¶209.

X. SECONDARY CONSIDERATIONS

Petitioner is aware of no evidence of secondary considerations that would meaningfully rebut a finding of obviousness. Ex. 1002, ¶210.

XI. CONCLUSION

Petitioner respectfully requests institution and that the Challenged Claims be cancelled.

Respectfully submitted,
BAKER BOTTS L.L.P.

Date: January 31, 2022

/s/ Eliot D. Williams
Eliot D. Williams (Reg. No. 50,822)
Lead Attorney for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §42.24(d), the undersigned hereby certifies that the word count under §42.24(a)(1) for the foregoing Petition for *Inter Partes* Review totals 13,940 words, within the 14,000 word limit allowed under §42.24(a)(1)(i).

Respectfully submitted,

BAKER BOTTS L.L.P.

Date: January 31, 2022

/s/ Eliot D. Williams
Eliot D. Williams (Reg. No. 50,822)
Lead Attorney for Petitioner

CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§42.6(e) and 42.105, the undersigned certifies that on the 31st day of January, 2022, a complete and entire copy of the PETITION FOR *INTER PARTES* REVIEW ("petition"), Petitioner's power of attorney, and related Exhibits were served on Patent Owner at the correspondence address of record for the subject patent,

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via Express Mail or by means at least as fast and reliable as Express Mail, and a courtesy copy is also being forwarded to Patent Owner's Litigation Counsel via electronic mail to:

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